PERTEC Application Notes

Double-Density System With PERTEC Flexible Disk Drives

FOREWORD

This Application Note provides the reader with a basic understanding of data-encoding processes employed in digital magnetic recording, with specific reference to disk memory devices. Section I describes different data-encoding procedures, establishes criteria for determining their relative merits, and discusses different parameters affecting the decoding margin. It should be noted that use of certain codes discussed in this document may infringe on existing patents. Section II describes a hardware implementation of the Delay-Modulation encoding procedure used to achieve a two-fold increase in the information-bit density with PERTEC Flexible Disk Drives. Section III describes an efficient hard-sectored format suitable for use in data processing applications. Appendix A provides the schematics and a general circuit description of the recommended PERTEC Phase-Lock Loop used in the hardware implementation of a double-density system.

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I. DIGITAL MAGNETIC RECORDING

1.1 GENERAL

Information stored on rotating magnetic disk memories is organized on the medium in concentric tracks. Each track consists of a continuous string of sectors, each of which contains a group of bytes comprising one record of data. Data are recorded in a sector on a bit-serial basis. Bits of information to be stored are first encoded, then recorded in a specific sector. The user's system will, however, determine the particular data encoding scheme to be used for data storage, depending on the type of recording medium and the bandwidth limitations of the read channel.

The term *information*, as used in this document, refers to any sequence of binary digits to be written on the medium consistent with the data encoding scheme employed by the user. The unit of information is the bit; a group of eight bits comprises one byte.

In digital magnetic recording, the data-encoding process specifies a one-to-one relationship between any given information-bit pattern and the associated sequence or sequences of flux transitions to be recorded on the medium in accordance with the specified rules. A flux transition is defined as the transition of magnetization written by a unit step change of write current, on the medium. An algorithm which produces this sequence of flux transitions for a given information-bit pattern is defined as the recording code. For the code to be useful, this one-to-one relationship must be unique.

The information is thus encoded into flux transitions recorded on the medium in accordance with the specified rules; i.e., a particular sequence of flux transitions is determined by the recording code.

For the purpose of encoding and recording information on the medium, a track is divided into equal elements defined as information-bit cells; each of which contains one encoded bit of information. The information-bit density on the track is expressed in terms of bits (bit cells) per inch of track-distance. The highest bit density is ultimately determined by the maximum flux-transition density that can be achieved with a given magnetic recording system and the nature of the recording code used in the data-encoding process. The information-bit cell is further partitioned into the boundary-half-bit cell and the center-half-bit cell. The boundary-half-bit cell occupies the half-bit space beginning at the imaginary information-bit boundary. Similarly, the center-half-bit cell occupies the half-bit space beginning at the center of information-bit cell. These relationships are defined in Figure 1.

The data-encoding algorithms encountered in digital magnetic recording are restricted to flux transitions only at half-bit boundaries, which implies that the flux-transition intervals for a given recording code will always be multiples of the half-bit distance. In general, each boundary-half bit and center-half bit assumes a value of either one or zero; the magnetization in the (arbitrarily defined) erase direction represents a binary zero and the magnetization in the direction opposite to the erase represents a binary one. It should be noted that in all illustrations presented in this document, a binary zero is represented by a logic low level and a binary one is represented by a logic high level. The values of half-bits can change only at the half-bit boundaries; each of which changes represents a transition of magnetization (flux transition).

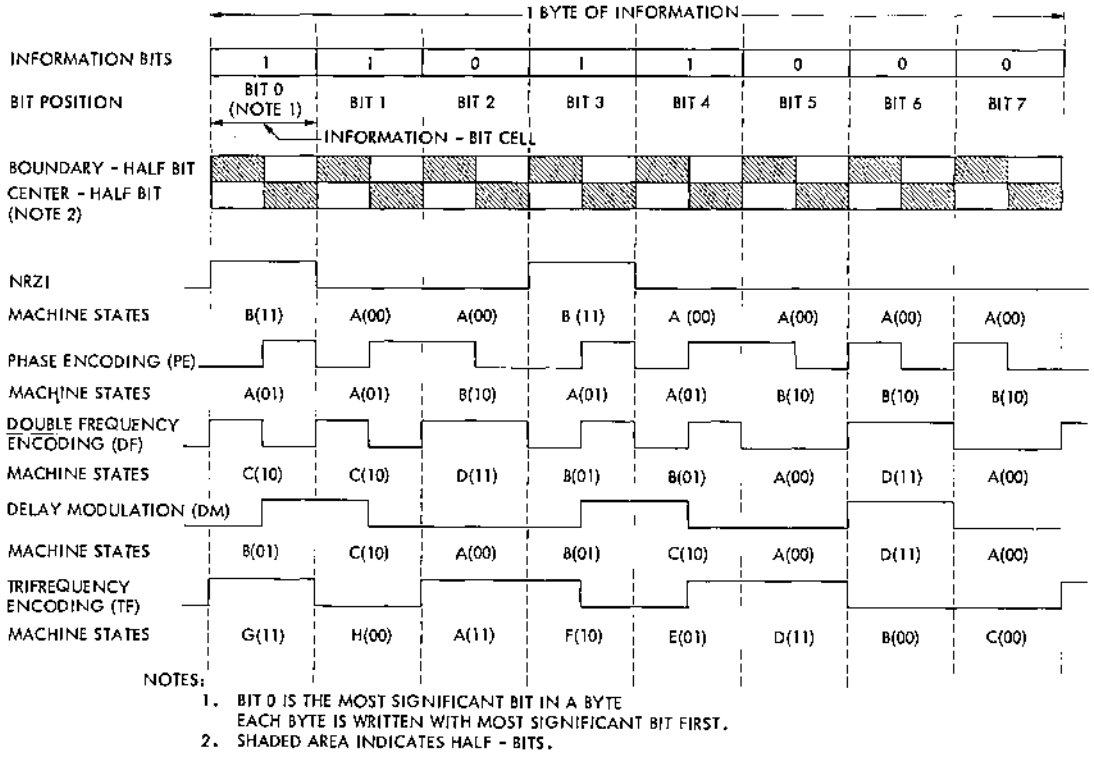


Figure 1. Data Encoding

The data-encoding algorithm produces a sequence of half-bit values to be recorded as magnetization states for a given information-bit pattern. The magnetization states within an information-bit cell can, therefore, be characterized by a pair of half-bit values. The four possible conditions of magnetization within an information-bit cell are designated by half-bit-value pairs<00>, <01>, <10>, and<11>.

The recording codes commonly encountered in digital magnetic recording are described in the following paragraphs.

1.2 RECORDING CODES

A recording code can be characterized by a sequential machine whose next state is determined by the present value of the input (information bits) and the present state (past history). Generally, for a recording code, the magnetization states within an information-bit cell depend not only upon the present value of the input, which in this case happens to be incoming information-bits to be recorded on the medium, but also upon the magnetization states in the previous information-bit cells. Therefore, the data-encoding algorithm for a recording code can be represented by the state diagram of a sequential machine. The nature of a given recording code determines the number of states in the sequential machine. The incoming information bits cause the machine to sequence through states determined by its state diagram. The next-state transitions in the machine occur at information-bit boundaries. Each machine state is assigned a pair of half-bit values which specifies magnetization states within an information-bit cell.

Once the sequential machine is specified completely by its state diagram, the encoder design can be approached as logic implementation of the sequential machine whose present state determines magnetization states within each information-bit cell.

The specific cases of code characterization using the sequential-machine approach are treated separately for modified Non-Return-To-Zero (NRZI), Phase Encoding (PE), Double-Frequency Encoding (DF), Delay-Modulation Encoding (DM), and Tri-Frequency Encoding (TF) as described in Paragraphs 1.2.1 through 1.2.5, respectively.

1.2.1 MODIFIED NON-RETURN-TO-ZERO (NRZI)

Refer to Figure 1 in conjunction with the following definition of the encoding algorithm for the modified Non-Return-To-Zero (NRZI) recording code.

A flux transition is recorded for each incoming information bit with a value of binary one at the information-bit boundary; otherwise, no flux transitions are recorded.

The encoding algorithm for NRZI can be characterized by a sequential machine having two states A(00) and B(11), which are assigned a pair of half-bit values <00> and <11> respectively. These values represent magnetization states within the information-bit cell. The state diagram shown in Figure 2 specifies next-state transitions for the sequential machine. Next-state transitions are made each time the new information bit is received, the next state being determined by the present value of the input and the present state. If the present state is A(00) and the new information-bit has a value of binary one, then the next state will be B(11). The sequential machine remains in the same state if the new information bit has a value of binary zero.

The NRZI encoder design can now be approached as the logic implementation of this sequential machine.

1.2.2 PHASE ENCODING (PE)

Refer to Figure 1 in conjunction with the following definition of the encoding algorithm for the Phase Encoding (PE) recording code.

A flux transition is always recorded at the center of each information-bit cell; the polarity of this flux transition is determined by the value of the information bit. If the information-bit value is binary zero, the flux transition defined by a half-bit-value pair <10> is recorded; for the value of binary one, the flux transition defined by a half-bit-value pair <01> is recorded. Flux transitions at the boundary of the information-bit cell are recorded only if the next information bit has the same binary value as the present information bit. The polarity of boundary flux transitions is fixed by the magnetization states in the information-bit cells on either side of the boundary.

The state diagram for sequential machine having two states, A(01) and B(10), for PE is shown in Figure 3. The logic implementation of this sequential machine provides the circuit for PE.

1.2.3 DOUBLE FREQUENCY ENCODING (DF)

Refer to Figure 1 in conjunction with the following definition of the encoding algorithm for the Double Frequency (DF) recording code.

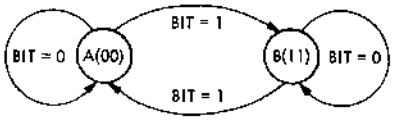


Figure 2. Non-Return-to-Zero (NRZI) State Diagram

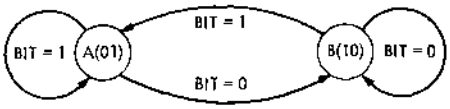


Figure 3. Phase Encoding (PE) State Diagram

A flux transition is always recorded at the boundary of each information-bit cell; a flux transition at the center of the information-bit cell is recorded only if the incoming information bit has a value of binary one. The polarity of flux transitions has no significance in DF encoding.

The state diagram for sequential machine having four states, A(00), B(01), C(10) and D(11), for DF encoding is shown in Figure 4. The logic implementation of this sequential machine provides the DF encoder circuit.

1.2.4 DELAY-MODULATION ENCODING (DM)

Refer to Figure 1 in conjunction with the following definition of the encoding algorithm for the Delay-Modulation (DM) recording code.

A flux transition is always recorded at the center of the information-bit cell for each incoming information-bit with a value of binary one. No flux transition is recorded for the information bit with a value of binary zero unless it is followed by another information bit with a value of binary zero, in which case the flux transition is provided at the end of the first information-bit cell.

The state diagram for a sequential machine having four states, A(00), B(01), C(10), and D(11), for DM encoding is shown in Figure 5. The logic implementation of this sequential machine provides the DM encoder.

Upon close examination of the encoding algorithms for DM and PE, it can be proved that the DM is derived from PE by logically dividing the PE waveform by two. This is shown in Figure 1. Topologically, a striking proof of this fundamental relationship is obtained by merging states A into D and B into C to translate the state diagram for DM into the state diagram for PE.

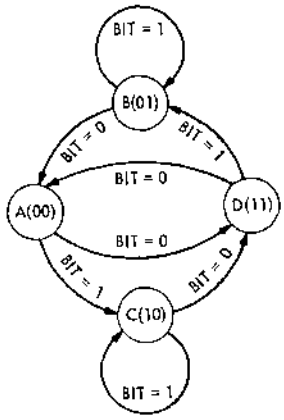


Figure 4. Double-Frequency (DF) Encoding State Diagram

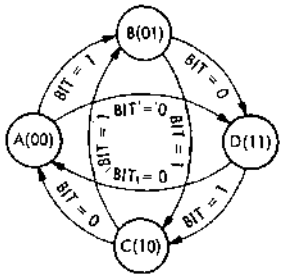


Figure 5. Delay-Modulation (DM) Encoding State Diagram

1.2.5 TRI-FREQUENCY ENCODING (TF)

Refer to Figure 1 in conjunction with the following definition of the encoding algorithm for the Tri-Frequency (TF) recording code.

There are eight conditions for an information-bit cell, four of which represent information bits with a value of binary zero; the other four represent information bits with a value of binary one. Refer to Figure 6.

The state diagram for a sequential machine having eight states for TF encoding is shown in Figure 6. The logic implementation of this sequential machine provides the TF encoder.

As in the case of DM encoding, it can be proved that TF is similarly derived from DF by logically dividing the DF waveform by two. This is shown in Figure 1. Again topologically, the state diagram for TF encoding can be translated into the state diagram for DF encoding by merging states A into C, B into D, E into F, and G into H.

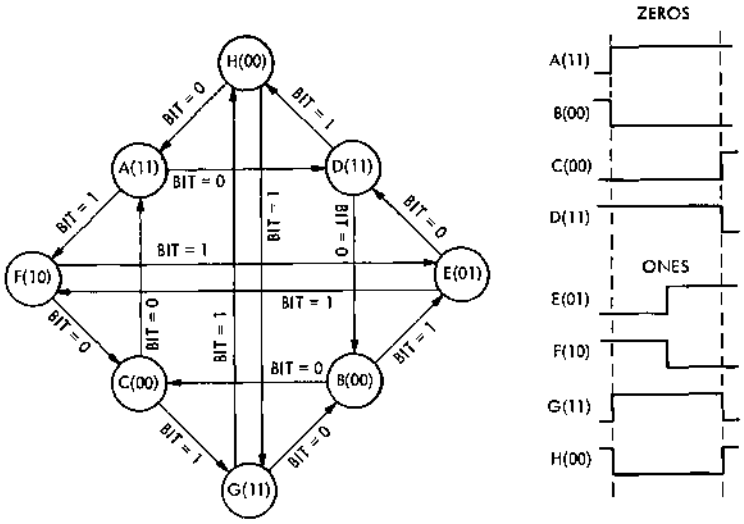


Figure 6. Tri-Frequency (TF) Encoding State Diagram

1.3 FREQUENCY SPECTRUM (ALL CODES)

The frequency spectrum of a recording code is an important factor in determining the recording density on the medium. The state diagram (encoding algorithm) of a code, given the next-state transition probabilities, contains all of the information required to calculate the frequency spectrum although the process of calculating the spectrum is very involved and cumbersome. However, qualitative inferences can be made from the state diagram to evaluate the recording codes for their relative coding efficiency, i.e., the number of flux transitions per information-bit cell averaged over a relatively large sample of independent ones and zeros (equal next-state transition probabilities) in a stream of information bits. Based on random independent binary data (equal next-state transition probabilities), the one-sided spectral density curves are calculated by Hecht and Guida* for NRZI, Phase-Encoding, and Delay-Modulation codes. The results, in which the one-sided spectral density (watts/Hz) is plotted against the normalized frequency in Hz (information-bit time T = 1 second), are given in Figure 7.

The one-sided spectral density curves for Double-Frequency and Tri-Frequency recording codes are not shown; however, it can be reasonably expected that they will be similar to those for Phase Encoding and Delay-Modulation respectively.

The knowledge of frequency components in a given recording code is essential in the design of a read channel for the magnetic recording system. The following paragraphs bring into focus the frequency-component aspect for each recording code discussed in paragraph 1.2.

*Delay Modulation, Hecht and Guida, Proceedings of the IEEE, page 1314, July 1969.

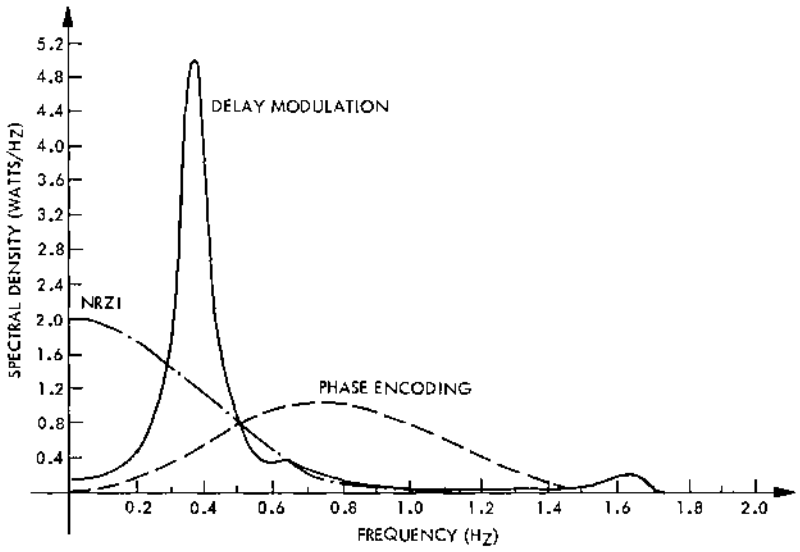


Figure 7. One-Sided Spectral Density Curves for NRZI, Phase Encoding, and Delay Modulation (Information-Bit Time T = 1 Second)

1.3.1 NRZI FREQUENCY SPECTRUM

The encoded waveform for NRZI contains a maximum frequency which is equal to one-half of the information-bit rate for an all ones information-bit pattern. This can be seen from the state diagram for NRZI encoding (Figure 2). In the case of an all zeros information-bit pattern, the encoded waveform contains only the d-c component. For other information-bit patterns, the encoded waveform contains frequencies between these two extreme values. Therefore, the encoded waveform for NRZI contains predominant low-frequency components.

On examination of the encoded waveform for NRZI, it can be seen that the coding efficiency (number of flux transitions per information bit) for NRZI encoding is equal to or less than 1.

1.3.2 PE FREQUENCY SPECTRUM

The PE waveform contains a maximum frequency which is equal to the information-bit rate for an all ones or an all zeros information-bit pattern. This can be seen from the state diagram for PE (Figure 3). When writing alternate ones and zeros, the PE waveform contains the frequency which is one-half of the information-bit rate. Unlike NRZI, the PE waveform, therefore, has a narrow frequency spectrum with reduced low-frequency response.

On examination of the PE waveform, it can be seen that a minimum of one flux transition is always recorded for each information-bit cell; also that the coding efficiency (number of flux transitions per information-bit cell) for PE encoding is greater than 1 but less than 2.

1.3.3 DF FREQUENCY SPECTRUM

The DF waveform contains a maximum frequency which is equal to the information-bit rate for an all ones information-bit pattern. This can be seen from the state diagram for DF encoding (Figure 4). When writing an all zeros information-bit pattern, the encoded waveform contains the frequency which is one-half of the information-bit rate. The frequency spectrum for DF encoding is expected to be similar to that for PE.

A minimum of one flux transition is always recorded for each information-bit cell. The coding efficiency (number of flux transitions per information bit) is greater than 1 but less than 2 for DF, as in the case of PE.

1.3.4 DM FREQUENCY SPECTRUM

The DM waveform contains three different flux-transition intervals of T, 3/2T, and 2T, where T is the information-bit period. This can be seen from the state diagram for DM encoding (Figure 5). The frequency characteristics of the DM waveform are summarized as follows:

(1) The encoded waveform contains the frequency which is one-half of the information-bit rate for an all zeros (000--) and all ones (111--) information-bit pattern.

(2) The encoded waveform contains the frequency which is one-fourth of the information-bit rate for an alternate ones and zeros (1010--) information-bit pattern.

(3) The encoded waveform contains the frequency which is one-third of the information-bit rate when writing ones followed by two zeros (100100--).

The frequency spectrum for DM is narrow as in the case of PE and DF; however, the peak of the spectral curve will be at a much lower frequency (approximately one-half) compared to the spectral curve for PE and DF (Figure 7). Also, the spectrum for DF contains negligible low-frequency response. The coding efficiency (number of flux transitions per information bit) is greater than 1/2 but less than 1.

1.3.5 TF FREQUENCY SPECTRUM

The TF waveform contains three different flux-transition intervals of T, 3/2T, and 2T, where T is the information-bit period, as in the case of DM. This can be seen from the state diagram for TF encoding (Figure 6). The frequency characteristics of the TF waveform are summarized as follows.

(1) The encoded waveform contains the frequency which is one-half of the information-bit rate for an all ones (111---) information-bit pattern.

(2) The encoded waveform contains the frequency which is one-fourth of the information-bit rate for an all zeros (000---) information-bit pattern.

(3) The encoded waveform contains the frequency which is one-third of the information-bit rate for an alternate ones and zeros (1010---) information-bit pattern.

The frequency spectrum for TF is expected to be similar to that for DM encoding. The coding efficiency (number of flux transitions per information bit) is greater than 1/2 but less than 1, as in the case of DM encoding.

1.4 DECODING

During playback, the magnetic recording system produces an electrical pulse for each flux transition recorded on the medium. The first step in the process of decoding information read from the medium is to process these flux-transition pulses through a channel of read electronics to faithfully reproduce the previously recorded encoded waveform. The next step is to reconstruct the clock signal which defines the information-bit cell with its subcells, the boundary-half-bit cell and the center-half-bit cell, for this playback signal. This clock signal must have the same half-bit frequency as the playback signal and should also have a specified phase relationship.

One important technique used to accomplish this is through use of a phase-lock loop to produce a clock signal which is phase-locked to the playback signal, and whose frequency is equal to the half-bit-cell rate. This relationship can be seen in Figure 8. The phase difference between the two waveforms should be such that the clock pulses occur in the middle of the half-bit cell. Thus, the phase-lock loop can be used to regenerate the sequence of half-bit-value pairs (magnetization states) from the playback signal.

The decoder then translates this sequence of half-bit-value pairs into a sequence of information bits by applying the encoding algorithm in reverse. The decoder can best be characterized as a sequential machine, which is the counterpart of the sequential machine for the encoder for a given recording code. The next-state transitions in this sequential machine are determined by the present value of the input (half-bit-value pairs) and the present state; each machine state can be assigned an information-bit value of either binary one or binary zero. The machine sequences through states determined by the state diagram as half-bit-value pairs are assembled, thus producing the sequence of information bits as output.

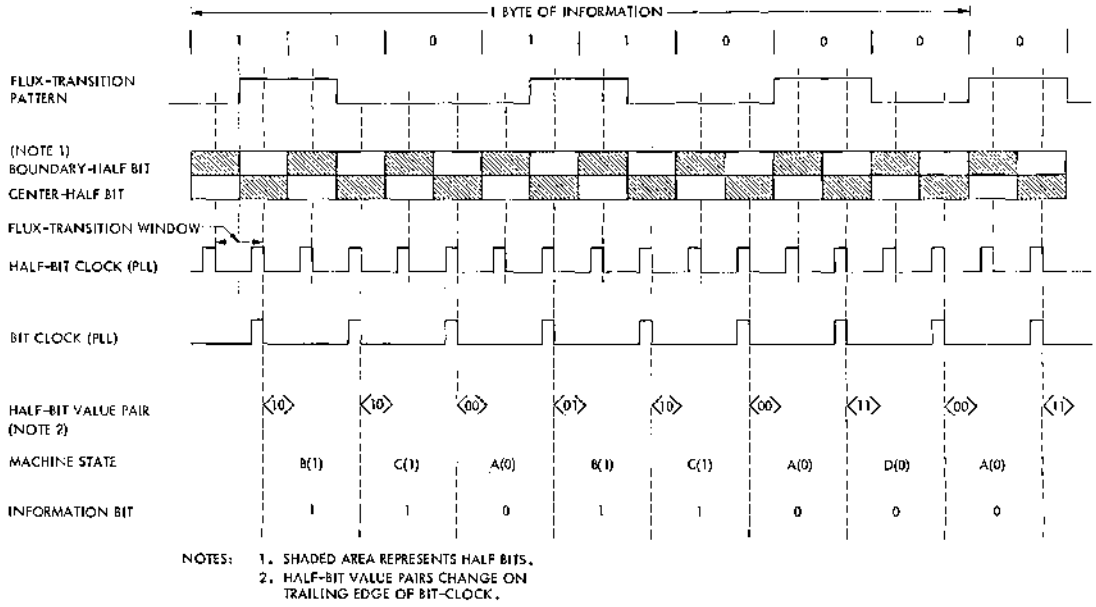


Figure 8. Decoding Delay Modulation, Timing

As an example, Figures 8 and 9 illustrate the decoding process for Delay Modulation. The state diagram in Figure 9 bears a striking resemblance to its counterpart for the encoder (see Figure 5) except for this obvious difference; for decoding, the next-state transitions in the state diagram are caused by half-bit-value pairs, and the machine states now represent information-bits.

Referring to Figure 9, it can be seen that if the sequential machine is in state A, the only legal half-bit-value pairs are <01> and <11>, which cause next-state transitions to states B(1) and D(0) respectively. The sequential machine can be designed such that the illegal half-bit-value pairs <10> and <00> will cause next-state transition into the error state, for the purpose of error detection.

The phase-lock loop must maintain the correct phase difference with respect to the playback signal for proper decoding of information bits. For the phase discriminator in a phase-lock loop circuit to produce the proper error signal for phase-lock, it is necessary that the playback signal contain, on the average, a certain minimum flux-transition rate which is large in comparison to the instantaneous speed variations of the magnetic recording system. A recording code is considered to be self-clocking if it possesses this property. Recording codes having a narrow frequency spectrum are generally self-clocking; therefore, a narrow frequency spectrum is a desirable characteristic in a recording code.

The recording codes discussed in Paragraph 1.2, with the exception of NRZI, are self-clocking. It is possible to make the NRZI code self-clocking by group coding (a four-to-five code-translation device) which provides a five-bit code for each group of four information bits. The five-bit code contains no more than two consecutive zeros in the recorded information, which eliminates low-frequency components from the frequency spectrum of the NRZI code. The resulting narrow frequency spectrum thus makes self-clocking possible for NRZI recording.

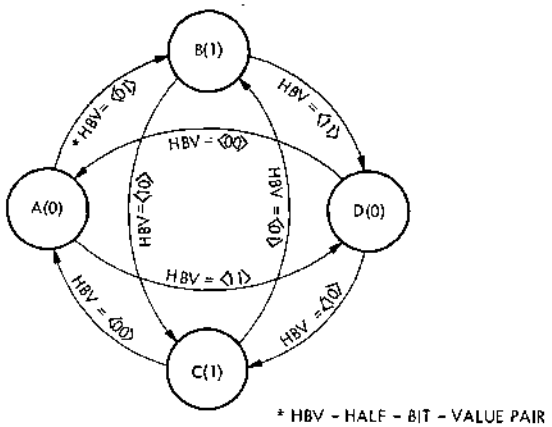


Figure 9. The State Diagram for Decoding, Delay-Modulation

The recording codes discussed so far, again with the exception of NRZI, provide flux transitions at the boundary and the center of the information-bit cell. This requires that the phase-lock loop operate at a frequency which is equal to the half-bit-cell rate, i.e., twice the information-bit rate for proper resolution of boundary and center flux transitions. Therefore, flux transitions must occur within a window which is equal to one-half of the information-bit cell (Figure 8) for proper decoding. However, in the case of group-coded NRZI, only the boundary flux transitions are provided; hence the phase-lock loop operates at a frequency which is equal to the information-bit rate. Flux transitions occur within a decoding window which is equal to the full information-bit cell. The larger window provides more margin for time-distortion in the true positions of flux transitions and, therefore, it is a desirable characteristic in a recording code.

The following paragraph provides the criteria by which the desirability of a recording code can be evaluated.

1.5 DESIRABLE CODE-CHARACTERISTICS

The foregoing discussion points to the desirability of a recording code with the following characteristics:

(1) Permits self-clocking.

(2) The coding efficiency (number of flux transitions per information bit) is equal to or less than 1.

(3) The decoding window is equal to the full information-bit cell.

(4) It has a narrow frequency spectrum with negligible low-frequency response.

The self-clocking property, as previously discussed, is essential to the use of a phase-lock loop for decoding. The coding efficiency, in fact, determines the information-bit density on the medium for a given magnetic recording system. Delay-Modulation (DM), for example, is twice as efficient as Phase Encoding (PE) since it uses, on the average, one-half as many flux transitions to encode the same number of information bits. The proper coding procedure can thus provide a two-fold increase in the information-packing density on the medium.

Also, as previously discussed, the decoding window determines the total available margin for time-distortion in the true positions of flux transitions during playback, for decoding. The NRZI recording, for example, with the decoding window of a full information-bit cell is superior to the DM which has the decoding window of one-half of the information-bit cell. The narrow frequency spectrum of the recording code allows the use of narrow bandwidth for the read channel; the narrow bandwidth improves the signal-to-noise ratio and, therefore, the dynamic range of the read channel. Also, DM, which has negligible low-frequency components, raises the low-frequency cut-off point required in the read amplifier and hence reduces its settling time.

Table 1 summarizes the performance of recording codes with respect to these four desirable code-characteristics. From Table 1 it can be seen that only the group-coded NRZI meets all four conditions, which makes it an ideal recording code. However, the complexity associated with its hardware implementation is not warranted unless the recording density is extremely high and it is necessary to realize the full potential benefits of this code. With the exception of NRZI, all codes exhibit a narrow frequency spectrum. Also, the NRZI code is not self-clocking, thus making it inadequate in most applications of rotating magnetic memories. It should be noted though, that NRZI has been used as a recording code in magnetic tape transports at low recording densities (less than 1000 bits per inch). Although PE and DF are self-clocking, they suffer from poor coding efficiency

Table 1
Summary of Performance for the Recording Codes

Recording Code / Code Characteristic	NRZI	NRZI With Group Coding	Phase Encoding (PE)	Double-Frequency Encoding (DF)	Delay-Modulation Encoding (DM)	Tri-Frequency Encoding (TF)
Self-Clocking	No	Yes	Yes	Yes	Yes	Yes
Code Efficiency (flux transitions per bit) ≤1	Yes	Yes	No	No	Yes	Yes
Decoding Window of One Full Information-Bit Time	Yes	Yes	No	No	No	No
Narrow Frequency Spectrum	No	Yes	Yes	Yes	Yes	Yes

with the number of flux transitions per bit greater than 1 but less than 2. However, the simplicity of their hardware implementation makes them ideal for intermediate recording densities (1000 to 3500 bits per inch). The self-clocking property and the excellent coding efficiency (flux transitions/bit≤1) make DM and TF ideal at high recording densities (3500 to 7000 bits per inch); but the hardware implementation is more complex in comparison to PE and DF. One disadvantage of DM and TF codes, with respect to the group-coded NRZI, is the requirement that the decoding window be one-half of the information-bit time.

The foregoing discussion brings into focus the proper selection of a recording code in the light of recording density and cost of hardware implementation.

1.6 MAGNETIC RECORDING

In digital magnetic recording, the medium is magnetically *saturated* in one direction or the other. Transitions of magnetization between these two states are written by a unit step reversal of write current passing through the windings of a magnetic recording head. The write current remains constant after each change of direction.

If the readback amplitude of the recorded signal is plotted against the write current for different flux-transition densities, the results will be as shown in Figure 10. At low densities where the wavelength is long compared to the magnetic-medium thickness, the output increases and levels off when the whole medium is *saturated*. At higher densities where the wavelength is of the same order as the medium thickness, most of the readback voltage is contributed by the medium layers nearest to the magnetic head. As the write current increases, the output increases as the top layers become increasingly magnetized. Further increase of write current increases the magnetization of the deeper layers but at the same time *over saturates* the top layers causing *transition spreading* and decrease of readback-output contribution from these layers. Although the magnetization of the lower layers increases, the contribution to readback voltages at the higher densities is much less significant. Thus, at higher densities the readback output peaks at a lower value and at a lower current than the *saturation* value at low densities.

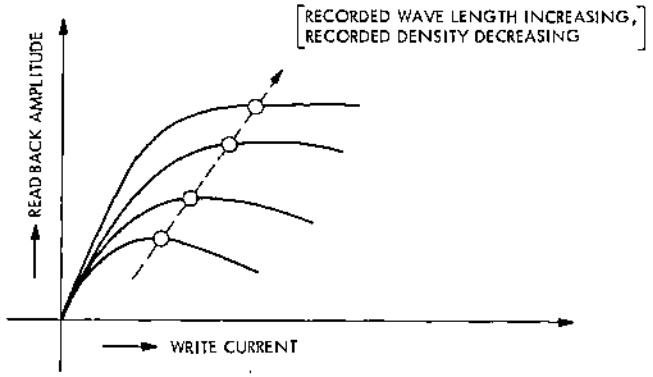


Figure 10. Readback Amplitude Versus Write Current

It is apparent that in practice, values of write current are selected which depend on the flux-transition density being recorded. Additionally, it is clear that the entire medium is not truly saturated, so the question of overwriting previously recorded information arises. Since there is no full-width erase head, the writing process itself must ensure that previous information is *overwritten*. Thus, the overwrite factor is an important parameter. To ensure overwrite, the write-current value must be as high as possible, increasing as the recorded density is decreased. It should be noted that this value must be compromised with that value giving the maximum readback voltage at the density in use. In practice, an operating value is chosen somewhat greater than that required to give the maximum readback voltage at the highest flux-transition density generated by the recording code used.

In rotating magnetic memories, information is generally organized in radial concentric tracks. Since the tracks are located at different radii, their linear speed is dependent upon the radius at which they are located. The innermost track with the smallest radius has the minimum linear speed, and the outermost track with the largest radius has the maximum linear speed. The information-bit rate, however, remains constant over the tracks. Thus, it can be seen that the innermost track produces the highest recording density. From the foregoing and Figure 10 it can be seen that the outermost track with the longer recorded wavelengths requires the higher value of operating current in comparison to the innermost track.

Flux transitions recorded on a rotating magnetic medium undergo time-distortion during playback. This time-distortion is commonly referred to as the peak-shift effect because it has the tendency to shift the analog peaks in the read-amplifier output. The peak shift in the magnetic recording has the following characteristics.

(1) The amount of peak shift is more pronounced at higher recording densities due to increased interaction between adjacent flux transitions.

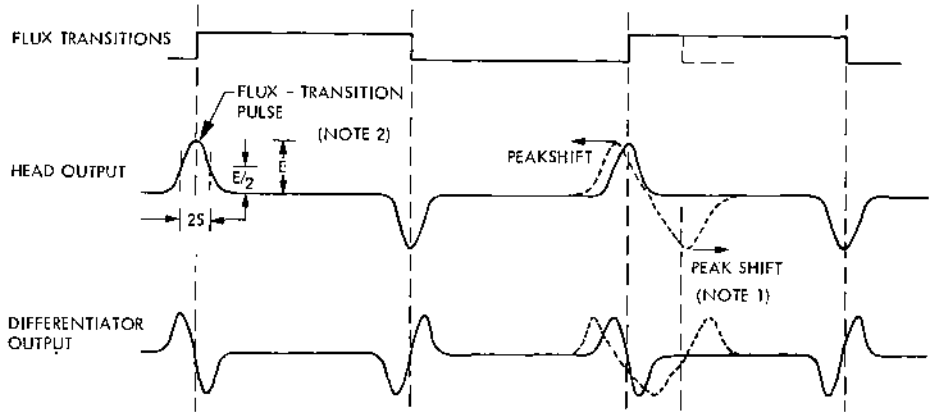
(2) Peak shift is a strong function of head resolution. The ratio of the head-output voltage at 2F to the head-output voltage at 1F is expressed in percentage as:

$$\frac{\text{Amplitude at 2F}}{\text{Amplitude at 1F}} \times 100\%$$

Head resolution is a difficult parameter to control in head manufacturing, and, therefore, a large spread in the value of head resolution should be expected in practice. For a given recording density, peak-shift becomes more pronounced on low-resolution heads, and, as the head resolution is increased, the amount of peak shift decreases.

(3) Write current also has strong influence on peak shift. For a given head resolution and recording density, the amount of peak shift increases as the write current is increased beyond the saturation point. Ideally the value of write current should be selected as low as possible while it is still sufficient to overwrite previously recorded information.

An isolated transition of magnetization written by a unit step change of write current is the most basic written element in digital magnetic recording and is shown in Figure 11. Flux transitions recorded on the medium produce an electrical pulse during playback. The amplitude and width of this pulse are a function of electromagnetic characteristics (parameters such as medium loss, spacing loss, and gap loss) of a given recording system. The width of this pulse is a direct measure of head resolution. As the head resolution increases, the magnetization transition width, 2S (as defined in Figure 11), becomes smaller, thus resulting in a sharper pulse. The peak of this pulse can be used to define the position of a flux transition. As the flux transitions are written into closer proximity of each other (higher recording density), the adjacent flux transitions interact causing resistance to further proximity; this interaction is the major cause of peak shift, as illustrated by dashed lines in Figure 11. Peak shift, therefore, becomes more pronounced at higher recording densities; also, for a given recording density, peak shift decreases as the head resolution is increased.



NOTES:

1. PEAK SHIFT TENDS TO MOVE THE FLUX TRANSITIONS IN THE DIRECTION SHOWN BY THE ARROWS.
2. PULSE BECOMES SHARPER, AS HEAD RESOLUTION IS INCREASED.

Figure 11. Playback Signal for Isolated Flux Transitions

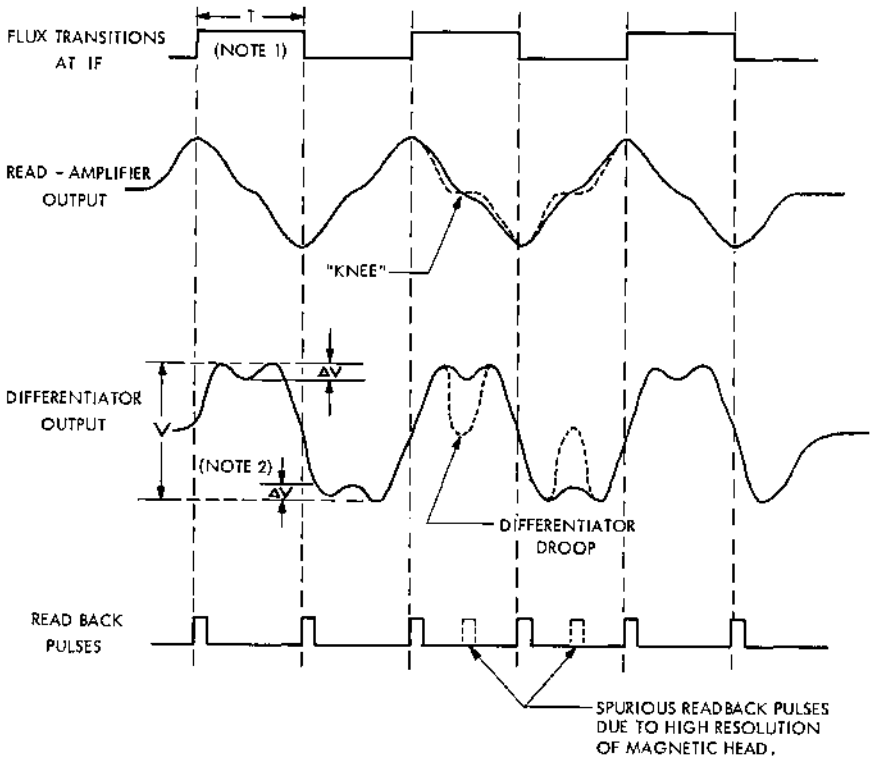
In practice, the maximum flux-transition density (flux transition per inch as measured on the innermost track) for recording information on the medium, is determined by the playback amplitude and peak shift at that density. The minimum head-output signal must meet the signal-to-noise-ratio requirement for the read channel to achieve the desired transient error rate; also, the peak shift at that density must be within the decoding margins for a given recording code.

The analog peaks in the playback signal define the true position of flux transitions recorded on the medium; the read channel produces a logic pulse for each flux transition during playback to faithfully reproduce the encoded waveform by peak detection. Peak detection is comprised of amplification, differentiation, and zero-cross-over detection of the playback signal. This is illustrated in Figure 12. One practical problem, referred to as *shouldering effect* in peak detection, is illustrated by dashed lines in Figure 12. In the case of a high-resolution head, the read-amplifier output shows a *knee* (third harmonic distortion) when it passes through zero. This knee, when differentiated, produces a droop in the differentiator output and causes a spurious readback pulse, representing a false peak if the droop approaches zero. For a given recording density, the knee in the read-amplifier output waveform becomes more discernible as the head resolution is increased, due to the resulting sharper flux-transition pulse (refer to Figure 11).

The differentiator droop becomes more pronounced on the outermost track where the recording density is minimum; also, the differentiator droop is larger for a high-resolution head when compared to a low-resolution head. The differentiator droop can be reduced by selecting a lower head resolution, by increasing the value of write current, or by reducing the differentiator bandwidth. However, these methods for offsetting the *shouldering effect* invariably reduce the decoding margins by increasing the effective peak shift.

The foregoing discussion points to the conflicting requirements for parameters governing the performance of a magnetic recording system; however, a systematic approach can now be presented to arrive at the optimum tradeoff for these parameters. First, the value of write current is established. As discussed previously, different values of write current are required for saturation on tracks located at different radii, i.e., outer tracks requiring higher values of write current than inner tracks. Obviously, it is not practical to have different values of write current for each track. If, for simplicity, a single value of write current (value for the outermost track) is selected for a write operation on all tracks, then, excessive peak shift occurs on the innermost track, thus reducing the decoding margin during playback. This problem can be partially resolved by partitioning tracks into groups (write-current zones) and assigning each group a single value of write current, which is the worst case saturation current for the outermost track in that group. The number of write-current zones, however, depends on the magnitude of change in recording density as it occurs from inner tracks to outer tracks, and the requirement for overall decoding margin to achieve the desired transient error rate. This change in recording density from inner tracks to outer tracks is a function of total number of tracks at a given track density (tracks per inch).

After amplification, the playback signal is normally processed through a filter with linear-phase-response characteristics within the bandpass required for the given information-bit rate and recording code to eliminate noise outside of the bandpass. The playback signal is then differentiated and applied to the zero-cross-over detector for the purpose of peak detection. As previously discussed, for a given head resolution, the differentiator droop increases as the differentiator bandwidth is increased; and conversely, in the case of high-resolution head, the differentiator droop can be reduced by decreasing the differentiator bandwidth. The upper and lower limits of head resolution can



NOTES:
1. T = INFORMATION-BIT TIME
2. THE PERCENTAGE DIFFERENTIATOR "DROOP" = $\frac{\Delta V}{V/2} \times 100$, ASSUMING THAT THE "DROOP" VALUE, ΔV, IS THE SAME FOR POSITIVE AND NEGATIVE PEAKS IN THE DIFFERENTIATOR OUTPUT.

Figure 12. Playback Signal at 1F

now be established by taking into account the factors described in the foregoing discussion. The upper limit of head resolution is determined by the differentiator droop on the outermost track; in common practice, the head resolution is kept below the value which produces fifty percent differentiator droop (as defined in Figure 12) at the given bandwidth. The lower limit of head resolution is determined by the decoding margin on the innermost track; the head resolution is kept above the value required to provide sufficient decoding margin at the given bandwidth. This points to the following conflicting requirements for the differentiator bandwidth.

(1) The bandwidth should be decreased to improve the upper limit of useable head resolution.

(2) The bandwidth should be increased to improve the lower limit of useable head resolution.

At intermediate recording densities, a single value of differentiator bandwidth can be selected for all tracks to provide sufficient overall decoding margin and, at the same time, allow reasonable range of head-resolution values. However, at higher recording densities, a single value of differentiator bandwidth is possible only at the expense of narrowly limiting the range of head-resolution values. This difficulty can be resolved if multiple bandwidths are used for tracks; the lower value of bandwidth can be provided for outer tracks to improve the upper limit of head resolution, and the higher value of bandwidth can be provided for inner tracks to improve the lower limit of head resolution. The lower value of bandwidth for outer tracks does not adversely affect the decoding margin, due to relatively lower recording densities on outer tracks and, therefore, less peak-shift. Similarly, the higher value of bandwidth for inner tracks does not adversely affect the differentiator droop as higher recording densities on inner tracks offset the effect of increased bandwidth.

Finally, the effect of noise on read-channel performance is considered; the magnitude of read-channel noise must be kept below a level which provides the desired transient error rate and sufficient dynamic range. The magnitude of read-channel noise can be reduced by decreasing the read-channel bandwidth, which also reduces the decoding margin. The magnitude of noise sources must be minimized in the design of read channel; the read channel performance must be optimized with respect to the requirements of signal-to-noise ratio and decoding margin during playback.

1.7 SUMMARY

The discussion contained in this section provides a basic understanding of digital magnetic recording. The procedure for selecting a proper recording code is presented; the recording codes are discussed with special emphasis on the requirements of frequency spectrum, coding efficiency, and decoding margin. Also provided is an evaluation of recording codes with regard to desirable code-characteristics.

A discussion of the effects of significantly different recording densities depending on the radial position of tracks is given. How they are offset by the use of multiple write-current zones to optimize the overall decoding margin during playback is also presented.

Finally, the parameters affecting the performance of a read channel are considered. A procedure is suggested to optimize the design of read channel with respect to the conflicting requirements of signal-to-noise ratio and read-channel bandwidth in conjunction with write-current zones.

II. DOUBLING THE STORAGE CAPACITY OF FLEXIBLE DISK DRIVES

2.1 INTRODUCTION

Flexible disk drives currently available for use in data processing applications utilize the Double-Frequency (DF) encoding technique. However, the coding efficiency for DF is poor since it requires a maximum of two flux transitions per information bit. The storage capacity of flexible disk drives can be increased two fold by using the Delay-Modulation (DM) encoding technique. The DM encoding technique requires a maximum of one flux transition per information bit, thus making it possible to increase the information-bit density two fold for a given recording density (flux transitions per inch). It also permits self-clocking, has a narrow frequency spectrum, and provides a relatively simple hardware implementation.

In this section, a possible hardware implementation for a double-density system using the DM encoding technique with PERTEC Flexible Disk Drives is presented.

Given in Table 2 are the recording parameters for the standard (single-density) and double-density PERTEC Flexible Disk Drives. It can be seen from Table 2 that although the information-bit density has doubled with the DM encoding technique, the recording density (flux transitions per inch) remains unchanged; and therefore, the amount of peak shift at both single and double information-bit densities also remains the same. Both the DF and DM recording codes require a decoding window which is one-half of the information-bit time. The information-bit time at double density is reduced to one-half (2 μsec) of its value at single density (4 μsec) and, therefore, the attendant decoding window for double-density is reduced by one-half (1 μsec from 2 μsec). The peak shift thus absorbs a greater proportion of the available decoding margin for double-density operation.

Paragraph 2.2 presents the general requirements for offsetting the reduced decoding margin in a double-density system to achieve the same error rate as that obtained in a single-density system. Paragraph 2.3 presents a hardware implementation of a double-density system which incorporates the design requirements presented in Paragraph 2.2.

Table 2
PERTEC Single-Density and Double-Density Parameters

Parameter	Single Density (Standard)	Double Density
Rotational Speed (rpm)	360	360
Data Transfer Rate (bits per second)	250,000	500,000
Information-Bit Time (μsec)	4	2
Encoding	DF	DM
Information-Bit Density* (bits per inch)	3268	6536
Recording Density* (flux transitions per inch)	6536	6536
Number of Tracks	77	77

*Measured on the innermost track.

2.2 GENERAL REQUIREMENTS FOR DOUBLE-DENSITY SYSTEM

The general requirements for PERTEC Flexible Disk Drives, empirically determined for double-density operation, are given in Paragraphs 2.2.1 through 2.2.4.

2.2.1 HEAD RESOLUTION

The upper and lower limits of head resolution as measured on Track 76 for double-density operation are specified to be 60 percent and 45 percent respectively, to satisfy read-channel performance requirements.

2.2.2 WRITE-CURRENT ZONES

To accommodate different recording densities, two write-current zones are required for inner and outer tracks. The higher value of write-current (10 ma peak-to-peak) is used for outer tracks 0 (decimal) through 42 (decimal) and the lower value of write current (8 ma peak-to-peak) is used for inner tracks 43 (decimal) through 76 (decimal).

The Head Current Switch (IHCS) interface signal is used to switch the value of write current for inner and outer tracks. When IHCS is true (low), the lower value of write current is selected for a write operation; when IHCS is false (high), the higher value of write current is selected for a write operation.

2.2.3 READ-CHANNEL BANDWIDTH

Two different values of read-channel bandwidth are required to allow a sufficient range of head-resolution values for double-density operation. The lower value of read-channel bandwidth is used for outer tracks 0 (decimal) through 42 (decimal) and the higher value of read-channel bandwidth is used for inner tracks 43 (decimal) through 76 (decimal).

The Head Current Switch (IHCS) interface signal must be used during a read operation to switch the read-channel bandwidth. When IHCS is true (low), the higher value of read-channel bandwidth is selected for a read operation; when IHCS is false (high), the lower value of read-channel bandwidth is selected for a read operation. This remote control of read-channel bandwidth through the IHCS interface signal is provided on all PERTEC Flexible Disk Drives configured for double-density operation.

2.2.4 WRITE PRECOMPENSATION

Write precompensation can be used during data encoding to further reduce peak shift in the playback signal. This further reduction of peak shift is required to enable use of the Delay-Modulation (DM) encoding technique for doubling the information-bit density, and still provide sufficient decoding margin to achieve the specified error rate for double-density operation. The principle of write precompensation can be described as follows.

A given flux transition is written with predetermined time-distortion (referred to as write precompensation) in its true position on the medium if it is expected to undergo peak shift during playback, depending on the flux-transition pattern; otherwise no write precompensation is provided. The amount of write precompensation is normally one-tenth of the information-bit time (200 nsec) and is provided in the direction opposite to that of peak shift. The direction of peak shift can be predicted based on the flux-transition pattern; this can be seen by referring to Figure 13. The write precompensation can be calculated by examining the half-bit sequence in the encoded waveform with no distinction being made of information-bit boundary or center flux transitions. A given flux transition in the encoded waveform is examined independently, with respect to only the

FLUX TRANSITION TO BE WRITTEN

HALF-BIT SEQUENCE / WRITE PRECOMPENSATION	n−3	n−2	n−1	n	n+1	n+2	n+3	n+4	DIRECTION OF PEAK SHIFT *
LATE	0	0	0	0	1	1	0	0	←
LATE **	0	0	0	0	1	1	0	1	←
LATE	0	0	0	0	1	1	1	0	←
NOMINAL	0	0	0	0	1	1	1	1	
NOMINAL **	0	1	0	0	1	1	0	0	
NOMINAL **	0	1	0	0	1	1	0	1	
EARLY **	0	1	0	0	1	1	1	0	→
EARLY **	0	1	0	0	1	1	1	1	→
LATE	1	0	0	0	1	1	0	0	←
LATE **	1	0	0	0	1	1	0	1	←
NOMINAL	1	0	0	0	1	1	1	0	
EARLY	1	0	0	0	1	1	1	1	→
NOMINAL	1	1	0	0	1	1	0	0	
NOMINAL **	1	1	0	0	1	1	0	1	
EARLY	1	1	0	0	1	1	1	0	→
EARLY	1	1	0	0	1	1	1	1	→
EARLY	0	0	1	1	0	0	0	0	→
EARLY	0	0	1	1	0	0	0	1	→
NOMINAL **	0	0	1	1	0	0	1	0	
NOMINAL	0	0	1	1	0	0	1	1	
EARLY	0	1	1	1	0	0	0	0	→
NOMINAL	0	1	1	1	0	0	0	1	
LATE **	0	1	1	1	0	0	1	0	←
LATE	0	1	1	1	0	0	1	1	←
EARLY **	1	0	1	1	0	0	0	0	→
EARLY **	1	0	1	1	0	0	0	1	→
NOMINAL **	1	0	1	1	0	0	1	0	
NOMINAL **	1	0	1	1	0	0	1	1	
NOMINAL	1	1	1	1	0	0	0	0	
LATE	1	1	1	1	0	0	0	1	←
LATE **	1	1	1	1	0	0	1	0	←
LATE	1	1	1	1	0	0	1	1	←

* SHADED AREAS REPRESENT NO APPRECIABLE PEAK SHIFT
** INDICATES HALF-BIT SEQUENCES INVALID IN DELAY MODULATION (DM) RECORDING CODE

Figure 13. Rules for Determining Write Precompensation

preceding and following flux transitions to specify the write precompensation for that flux transition as illustrated in Figure 13.

2.3 HARDWARE IMPLEMENTATION

Figure 14 shows the functional block diagram of a double-density system whose main functions are data encoding, write precompensation, and data decoding with a phase-lock loop technique. The 10 MHz Crystal Oscillator, in conjunction with the Clock Generator, provides basic timing for data encoding and write precompensation during a write operation. The Write Clock and Read Clock signals are multiplexed under the control of Read Enable to generate the Bit Clock signal, which can be used by the formatter as the system clock during a data transfer operation. The write data to be recorded on the medium are first encoded using the Delay-Modulation (DM) encoding technique; the Encoded Write Data signal is then precompensated. The precompensated Write Data signal is applied to the Write Amplifier to record the transitions of magnetization onto the medium. During playback, the output signal from the magnetic head is amplified, filtered, and differentiated. The differentiated signal is then applied to the Zero Crossover-Detector-and-Pulse Former which produces a logic pulse for each flux transition recorded on the medium. These readback pulses are applied to the Phase-Lock Loop and Phase Control, which generate the PLL Clock and Readback Pulses (Delayed) signals respectively; these signals are used by the Data Decoder-Synchronizer for the purpose of decoding data. Paragraphs 2.3.1 and 2.3.2 describe each of these functions in detail.

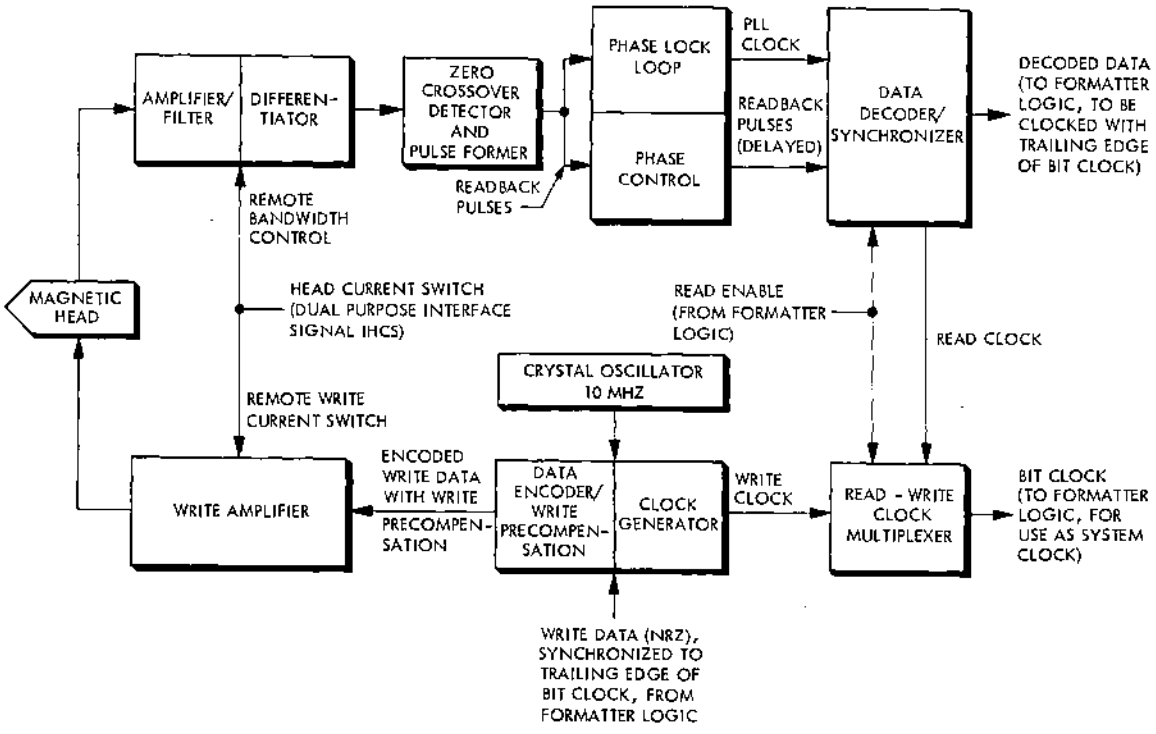


Figure 14. Double-Density Read-Write Electronics, Functional Block Diagram

2.3.1 DATA ENCODING

The DM encoding technique is as follows: a flux transition is always recorded at the center of the information-bit cell for each information bit with a value of binary one. No flux transition is recorded for the information bit with a value of binary zero unless it is followed by another information bit with a value of binary zero, in which case the flux transition is provided at the end of the first information-bit cell. It can be seen from the foregoing encoding technique that, in the case of DM, no significance is attached to the polarity of transitions of magnetization; therefore, the magnetization states within an information-bit cell given by half-bit-value pairs <01> or <10>, both represent the information bit with a value of binary one. Furthermore, the interface specification of PERTEC Flexible Disk Drives requires that the controller provide a logic pulse for each flux transition to be recorded on the medium during a write operation, with no significance attached to the polarity of flux transition. Similarly, during playback, the disk drive provides a logic pulse to the controller for each flux transition recorded on the medium.

The logic implementation for the DM encoding technique, and the precompensation of Encoded Write Data signal and associated timing functions are illustrated in Figures 15 through 19 and should be referred to in conjunction with the following description.

Basic timing for data encoding and precompensation is provided by the 10 MHz Crystal Oscillator shown in Figure 15. The 10 MHz Clock signal is applied to the Clock Generator which in turn provides the Flux-Transition Window, Half-Bit Clock, Clock/L, Clock/E, and Clock/N timing signals. The Clock Generator must be designed such that the timing relationship for these signals is as specified in Figure 19. Referring to Figure 15 it can be seen that the Clock/N signal is logically divided by two through flip-flop U1-A to generate the Clock/N ÷ 2 and Write Clock signals. Further, the Write Clock signal and the Read Clock signal from the data decoder are multiplexed under the control of Read Enable to provide the Bit Clock signal. The Bit Clock signal can be used by the formatter as the system clock during a data transfer operation.

The logic implementation of DM encoding technique shown in Figure 16 is comprised of two-bit shift register U1-A-B, AND-OR-INVERT gate U2-A, and NOR gates U4-A and U4-B. The detailed timing diagram for data encoding is given in Figure 18. The formatter transmits write data in NRZ form to the data encoder, synchronous with the trailing edge of the Bit Clock during a write operation; the encoded write data become available, when Write Enable is true, at the output of data encoder (NOR gate U4-A).

The logic implementation for the precompensation of the Encoded Write Data signal is shown in Figure 17 and is comprised of half-bit shift register U3, Read-Only-Memory U4, flip-flop U2-A, and NAND gates U1 and U5. Refer to the detailed timing diagram given in Figure 19 in conjunction with the description of the precompensation technique.

The Encoded Write Data signal contains a logic pulse for each flux transition to be recorded on the medium; these logic pulses occur within the Flux-Transition Window as shown in the timing diagram of Figure 19. For each flux-transition pulse in the Encoded Write Data signal occuring within the Flux-Transition Window, a logic one is shifted into the half-bit register synchronous with the Half-Bit Clock; otherwise, a logic zero is shifted.

pattern given by parallel outputs Q1 through Q7. The parallel outputs of half-bit shift register U3, Q4, Q1, Q2, Q6, and Q7 are applied to the address inputs of Read-Only-Memory (ROM) U4 whose outputs (Nominal, Early, and Late) determine the respective precompensation as determined by the ROM truth table presented in Figure 20.

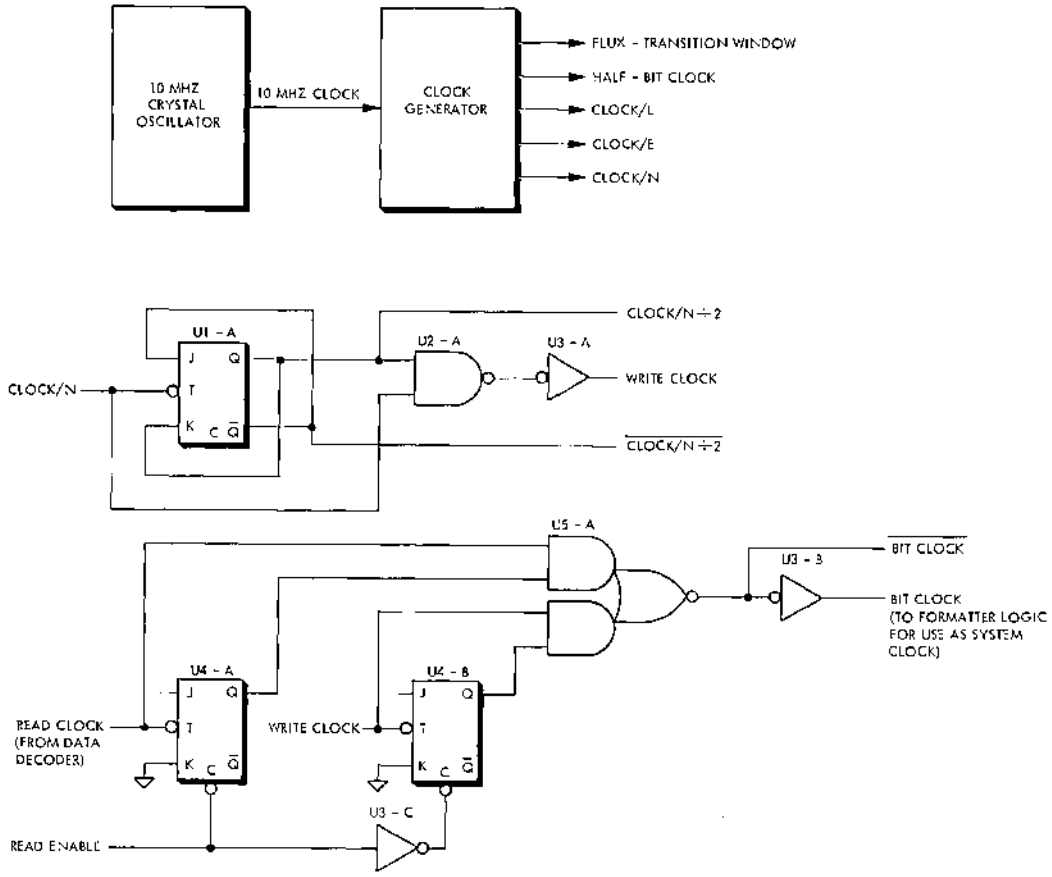
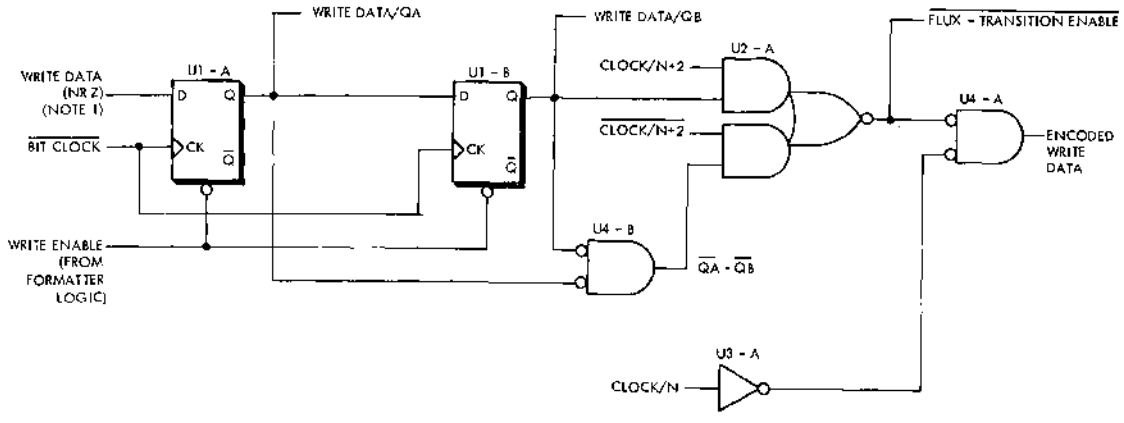
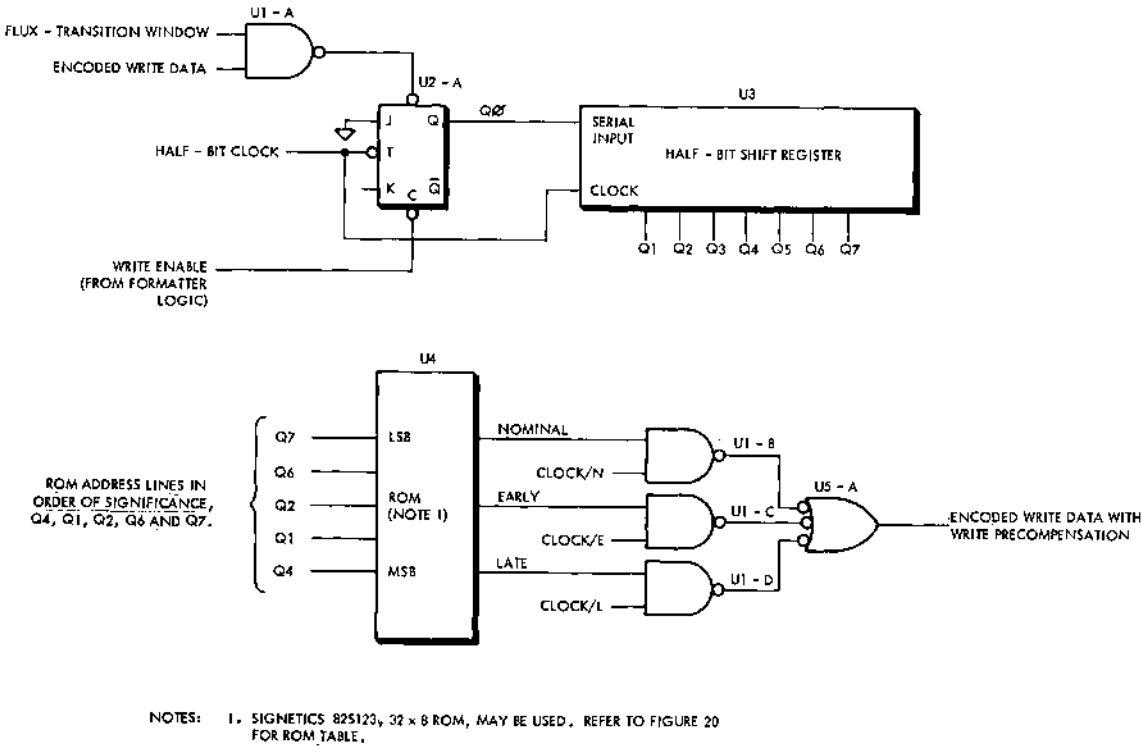


Figure 15. Clock Generator and Read-Write Clock Multiplexer, Logic Diagram



NOTES: 1. NRZ WRITE DATA FROM FORMATTER LOGIC, SYNCHRONIZED TO BIT CLOCK (SYSTEM CLOCK).

Figure 16. Data Encoding, Logic Diagram



NOTES: 1. SIGNETICS 825123, 32 x 8 ROM, MAY BE USED. REFER TO FIGURE 20 FOR ROM TABLE.

Figure 17. Write Precompensation, Logic Diagram

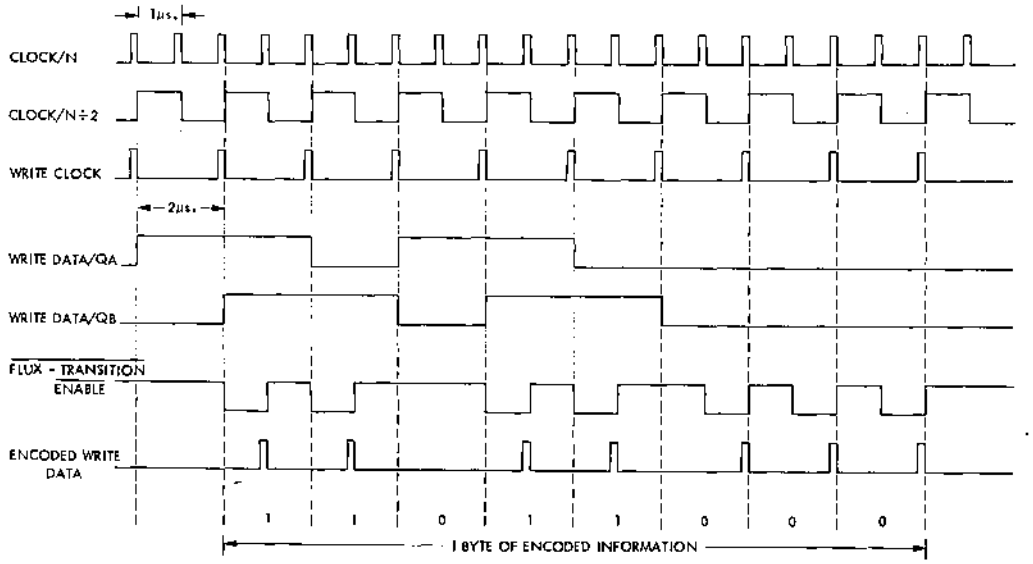
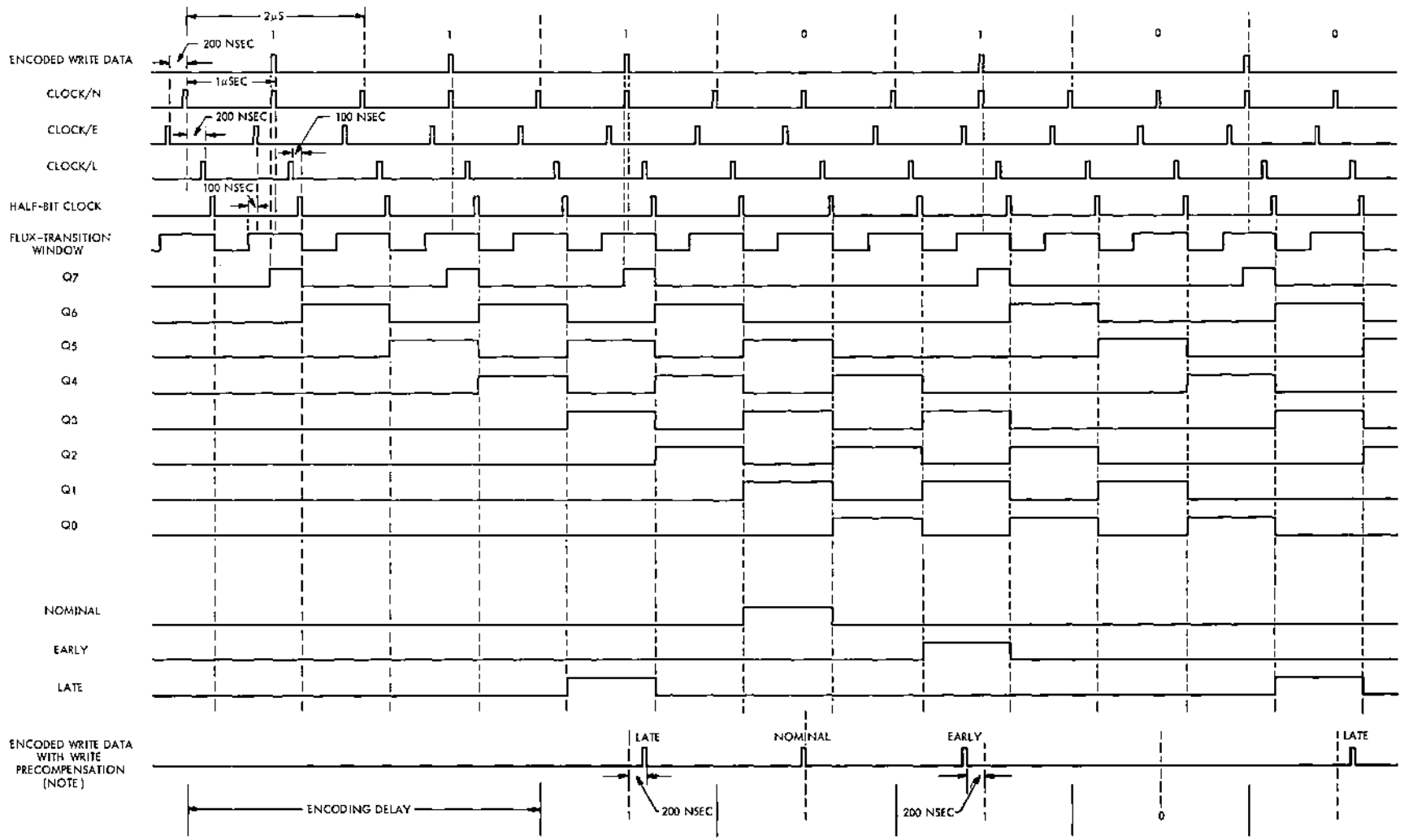


Figure 18. Data Encoding, Timing



NOTE: PULSES REPRESENT FLUX TRANSITIONS TO BE RECORDED.

Figure 19. Write Precompensation, Timing Diagram

Q4	Q1	Q2	Q6	Q7	NOMINAL	EARLY	LATE
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	0	0
0	0	1	0	1	0	0	0
0	0	1	1	0	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	0	0
0	1	0	0	1	0	0	0
0	1	0	1	0	0	0	0
0	1	0	1	1	0	0	0
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	0	0	0	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	1
1	0	1	0	1	0	0	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	0	0	1
1	1	0	0	1	1	0	0
1	1	0	1	0	0	1	0
1	1	0	1	1	0	1	0
1	1	1	0	0	0	0	1
1	1	1	0	1	0	0	1
1	1	1	1	0	1	0	0
1	1	1	1	1	1	0	0

Figure 20. Write Precompensation, Read-Only Memory (ROM) Truth Table

2.3.2 DATA DECODING

The disk drive provides a logic pulse (200 nsec, nominal) during playback, for each flux transition recorded on the medium. The leading edge of these pulses represent the flux transitions recorded on the medium. Flux transitions recorded on the magnetic medium undergo time-distortion during playback, and the amount of distortion becomes more pronounced at higher recording densities. This time-distortion, commonly referred to as the peak-shift effect, has the tendency to shift the analog peaks in the read-amplifier output. Any decoding circuit designed to recover data recorded on the disk surface must take into account the speed variation of the disk drive and the peak shift in the playback signal. Both of these parameters can adversely affect the decoder margins. A decoder circuit must be designed to ensure that the contribution of the circuit to decoder tolerances is negligible compared to peak shift and speed variation effects. The speed variation of the disk drive contributes to deviation of the data rate from its nominal value; however, the use of a phase-lock-loop circuit in decoding data significantly reduces the effect of speed variation on decoder tolerances.

The use of phase-lock-loop technique in data decoding is required to obtain sufficient decoding margins for reliable double-density operation of PERTEC Flexible Disk Drives. The logic implementation of data decoding using a phase-lock-loop technique is given in Figures 21 and 22. Figure 21 provides only the functional block diagram of phase-lock loop and phase control; the complete design of the phase-lock loop is presented in Appendix A. The Readback Pulses from the disk drive are applied to the Phase Comparator, Low Pass Filter/Amplifier, and Voltage Controlled Oscillator, thus generating the PLL Clock signal. The Readback Pulses are also applied to the Phase-Control circuit which provides the adjustable delay used to obtain the proper phase difference between the Readback Pulses (delayed) and PLL Clock signals. The phase difference is adjusted to be as shown in the timing diagram Figure 23.

The Readback Pulses (delayed) and PLL Clock signals are applied to the data decoder as shown in Figure 22. The detailed timing diagram for data decoding is given in Figure 23. The Decoded Data become available at the data-decoder output (flip-flop U1-B), when Read Enable is true, synchronous with the trailing edge of the Bit Clock signal. Another data-decoder output, the Read Clock signal, is applied to the read-write clock multiplexer (see Figure 15) where it is multiplexed with the Write Clock signal under the control of Read Enable to generate the Bit Clock signal.

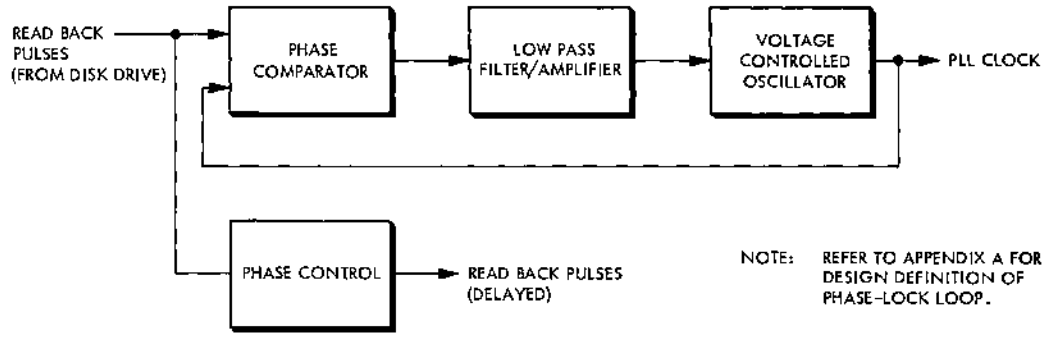


Figure 21. Phase-Lock Loop, Functional Block Diagram

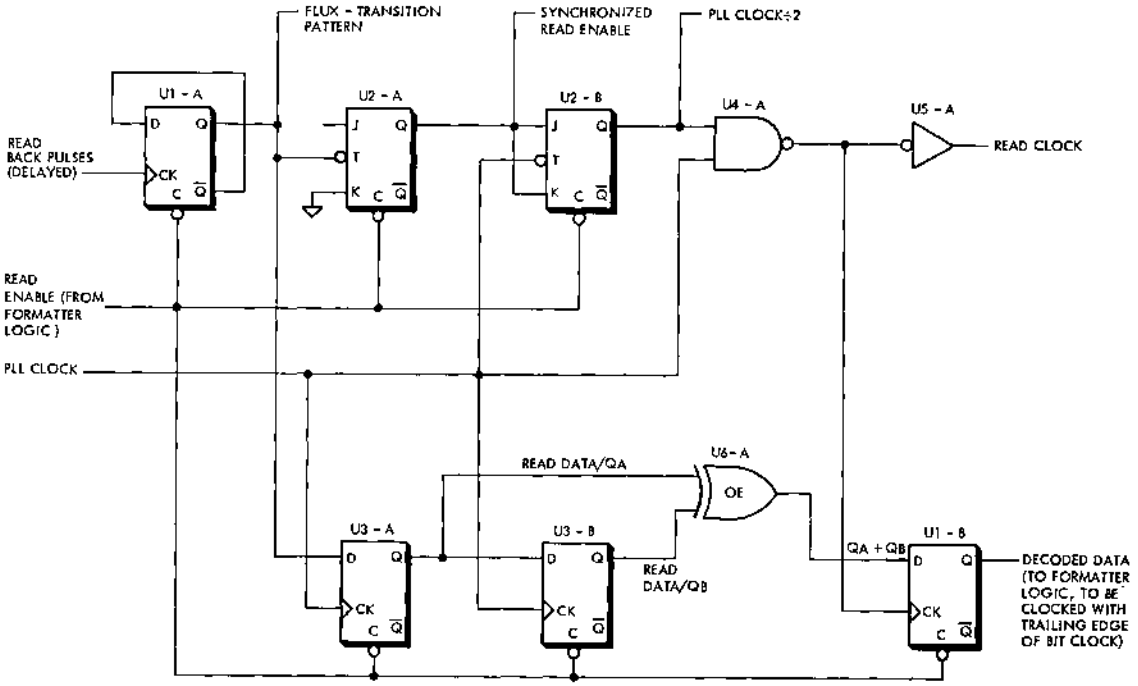
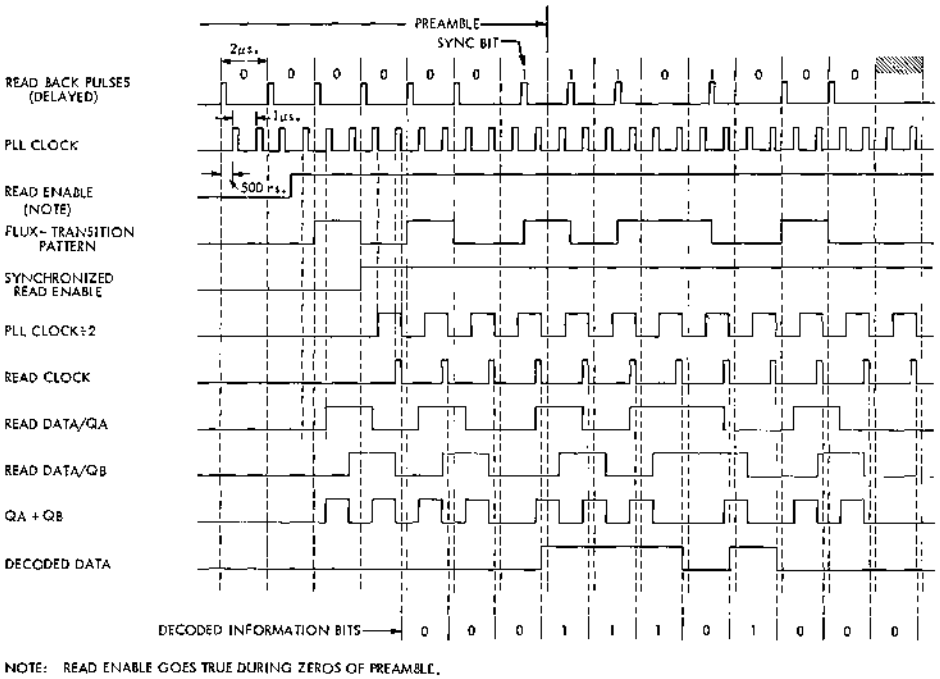


Figure 22. Data Decoding, Logic Diagram



NOTE: READ ENABLE GOES TRUE DURING ZEROS OF PREAMBLE.

Figure 23. Data Decoding, Timing Diagram

III. TRACK FORMAT

3.1 INTRODUCTION

The PERTEC Flexible Disk Drive is a compact random-access memory device suitable for use in data processing applications. The recording medium employed is a circular mylar disk referred to as a diskette.

The standard diskette is designed for use with a format in which the sector information is pre-recorded. In this case, a single hole on the diskette serves as a reference point. The detection of this hole is accomplished by a transducer which is made up of a photo transistor/LED combination. The transducer produces an index pulse once per revolution of the diskette.

A diskette that has equally spaced fixed sector holes on the same radius as the index hole is referred to as being hard sectored. Sector timing is accomplished by sensing these holes. This configuration is shown in Figure 24 along with a timing diagram which compares the hard-sectored diskette with 32 sector holes and the single-hole diskette.

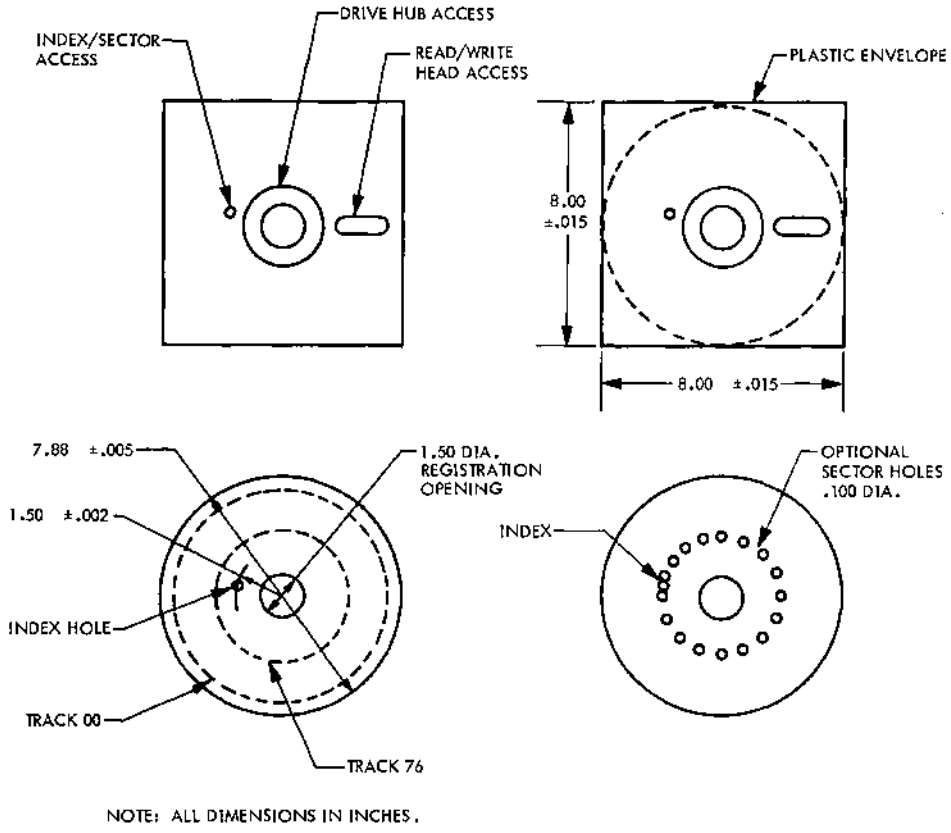
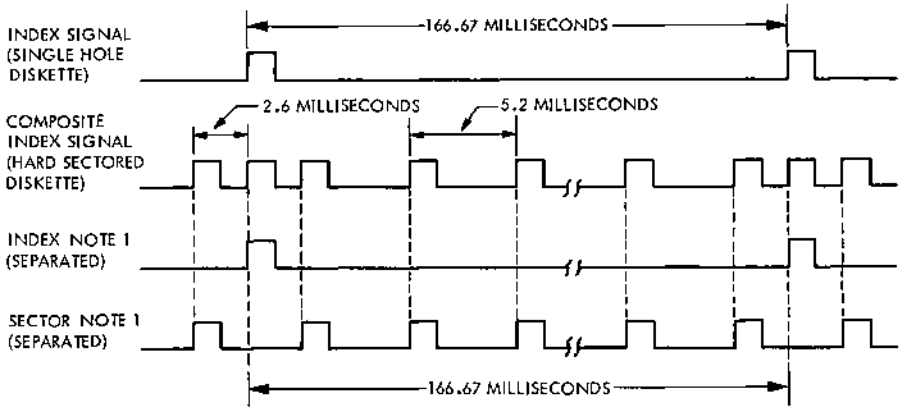


Figure 24A. Diskette Comparison



NOTE: 1. USER SYSTEM SEPARATES INDEX AND SECTOR PULSES.
2. ALL TIME VALUES NOMINAL.

Figure 24B. Diskette Comparison (Timing)

3.2 FORMAT PARAMETERS

The basic parameters used in configuring a hard-sectored format for the PERTEC Flexible Disk Drive are as follows.

- Number of Sectors: 32
- Number of Tracks: 77
- Rotation Rate: 360 RPM
- Data Transfer Rate: 500,000 bits per second
- Nominal Density: 6536 (bits per inch, inside track)

Using the foregoing parameters, a variable header format (shown in Figure 25) can be recommended; which consists of the following.

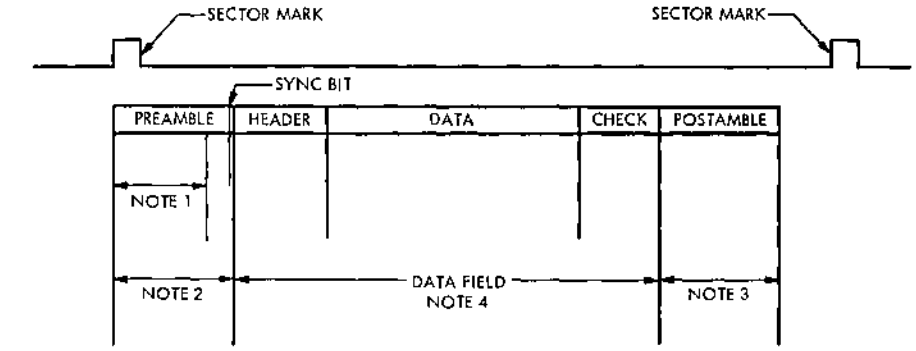
- Preamble — A burst of zero bits required for sector tolerancing and to allow the read electronics to acquire data.
- Sync Bit — A single one bit which flags the beginning of useful data.
- Data Field — Consists of:

  Header — Two bytes which contain the track and sector address of the current sector. This is compared against the expected address before a data transfer takes place.

  Data — n bytes of data; the value n depends on the formatter configuration.

  Check — Two bytes of Cyclic Redundancy Check (CRC) character information for the Header and Data. When reading from the disk, these bytes are compared against a recomputed CRC.
- Postamble — A burst of zero bits which allows the erase head to complete the erasure of the CRC field before write current is switched off.

The standard hard-sectored diskette divides the recording surface into 32 equal sectors; these can be further subdivided (logically) to obtain 16-, 8-, and 4-sector configurations. A method for calculating parameters of the hard-sectored format shown in Figure 25 is described in the Application Note, Hard Sector Formatting for PERTEC Flexible Disk Drives, PERTEC Document No. 75605.



NOTES:
1. READ PREAMBLE DELAY
2. WRITE PREAMBLE DELAY
3. WRITE POSTAMBLE DELAY
4. AVAILABLE DATA FIELD

Figure 25. Basic Format

NOTES

APPENDIX A
PHASE LOCK LOOP

A.1 BASIC PRINCIPLES OF OPERATION

The purpose of the Phase-Lock Loop (PLL) is to provide a clock signal which maintains a fixed phase relationship with the incoming signal. The PLL is a feedback system consisting of a phase comparator, a low-pass filter, an error amplifier in the forward signal path, and a Voltage-Controlled Oscillator (VCO) in the feedback path.

Figure A-1 is a block diagram of the basic PLL system. With no input signal applied the error voltage is equal to zero and the voltage-controlled oscillator operates at a center frequency, f_o, which is called the *free-running* frequency. When an input signal, f_s, is applied to the system, the Phase Comparator compares the phase and frequency of the input with the VCO frequency, f_o, then generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is filtered, amplified, and routed to the control input of the VCO. Thus, the control voltage, $V_d(t)$, forces the VCO frequency to vary in a direction that reduces the frequency difference between f_o and the input signal. If the input signal, f_s, is sufficiently close to f_o, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once locked, the VCO frequency is identical to the input signal, except for a finite phase difference. This net phase difference is necessary to generate the corrective error voltage to shift the VCO frequency from its free-running value to the input signal frequency, f_s, thus keeping the PLL locked. This tracking ability allows the PLL to follow the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain phase-lock with an input signal is defined as the *lock range* of the system. This range is always larger than the band of frequencies over which the PLL can acquire phase-lock with an incoming signal. This latter range of frequencies is called the *capture range* of the system.

The total time taken by the PLL to establish lock-on is called the *pull-in* time. Pull-in time depends on the initial frequency and phase difference between the two signals, as well as the overall loop gain and the bandwidth of the Low Pass Filter.

The Low Pass Filter attenuates the high frequency components at the output of the Phase Comparator, thereby enhancing the noise rejection characteristics of the circuit. Also, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the

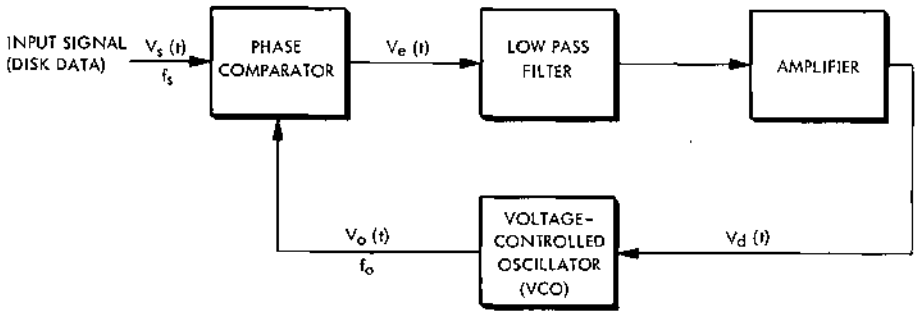


Figure A-1. Phase-Locked Loop Block Diagram

system loses phase-lock due to a noise transient. The Low-Pass Filter, therefore, controls the capture and the transient-response characteristics of the PLL. As the filter bandwidth is decreased the capture process becomes slower, thereby increasing the pull-in time. As the capture range decreases, the interference-rejection properties of the PLL improve and the transient response of the loop becomes under-damped, resulting in a smaller value of the damping factor. The latter effect brings about a practical limitation on the Low-Pass Filter bandwidth.

In a specific PLL application the capture range is minimized. However, it must allow the PLL to acquire phase-lock within the specified lock-up time under worst case fluctuations of the incoming signal frequency. This bandwidth should be sufficiently narrow to ensure that the phase errors in the incoming signal (produced by the peak-shift effect) are not tracked. The value of the damping factor for the PLL is chosen between 0.7 and 1.0 for optimum loop performance. These criteria are applied to the design of the phase-lock loop described in Paragraph A.2.

A.2 CIRCUIT DESCRIPTION

Figures A-2 and A-3 are schematic drawings of the PERTEC Phase-Lock-Loop circuit. Readback Pulses are applied to the one-shot circuit at U1 to obtain a pulse of 1050 ± 25 nsec for every flux transition read from the diskette. The output at U1/5 is applied to the Phase Comparator circuit which is comprised of flip-flop U4/15 and NAND gates U3/11 and U3/8. The Phase Comparator compares the phase of the input signal Readback Pulses with the VCO ÷ 2 signal. The Phase Comparator timing diagram is shown in Figure A-4. Outputs Control A and Control B are applied to the balanced lead-lag type Low Pass Filter formed by resistors R7 and R9, and capacitors C4 and C5 on one leg, and resistors R12 and R14, and capacitors C6 and C7 on the other leg. The output of the balanced filter is applied to the positive and negative inputs of operational amplifier U5.

The output of amplifier U5 is applied to the VCO formed by current source Q1, capacitors C12 and C13, voltage comparator U6, and discharge circuit U7. Values of capacitors C12, C13, current source Q1, and the threshold voltage of comparator U6 determine the free-running frequency of the VCO. This frequency is varied by potentiometer R23. The output of the VCO is applied to the Phase Comparator to generate an error voltage which is proportional to the phase difference between the input signals Readback Pulses and VCO ÷ 2.

The PLL Clock output is applied to the Data Decoder circuit described in Section II along with the Readback Pulses (delayed) signal which is the output of the Phase Control. Potentiometer R4 in the Phase Control circuit provides the means to obtain proper phase relationship between the Readback Pulses (delayed) and PLL Clock signals as shown in the timing diagram of Figure A-4.

The center frequency of the PLL circuit shown can be adjusted by potentiometer R23. With a frequency counter connected at U4/15 (VCO ÷ 2), R23 should be adjusted until the frequency counter indicates 1 MHz. The Readback Pulses line at U2/1 must be in the false (high) state during this adjustment.

In the circuit shown, the proper phase relationship between the Readback Pulses (delayed) and PLL Clock signals can be obtained by adjusting potentiometer R4. Using a dual-trace oscilloscope, the PLL Clock can be observed at U3/3 (channel 1) and the Readback Pulses (delayed) signal at U8/10 (channel 2). With the oscilloscope set to a vertical mode 'add' condition and all-zero data on the Readback Pulses line, the relationship should be as shown in Figure A-4.

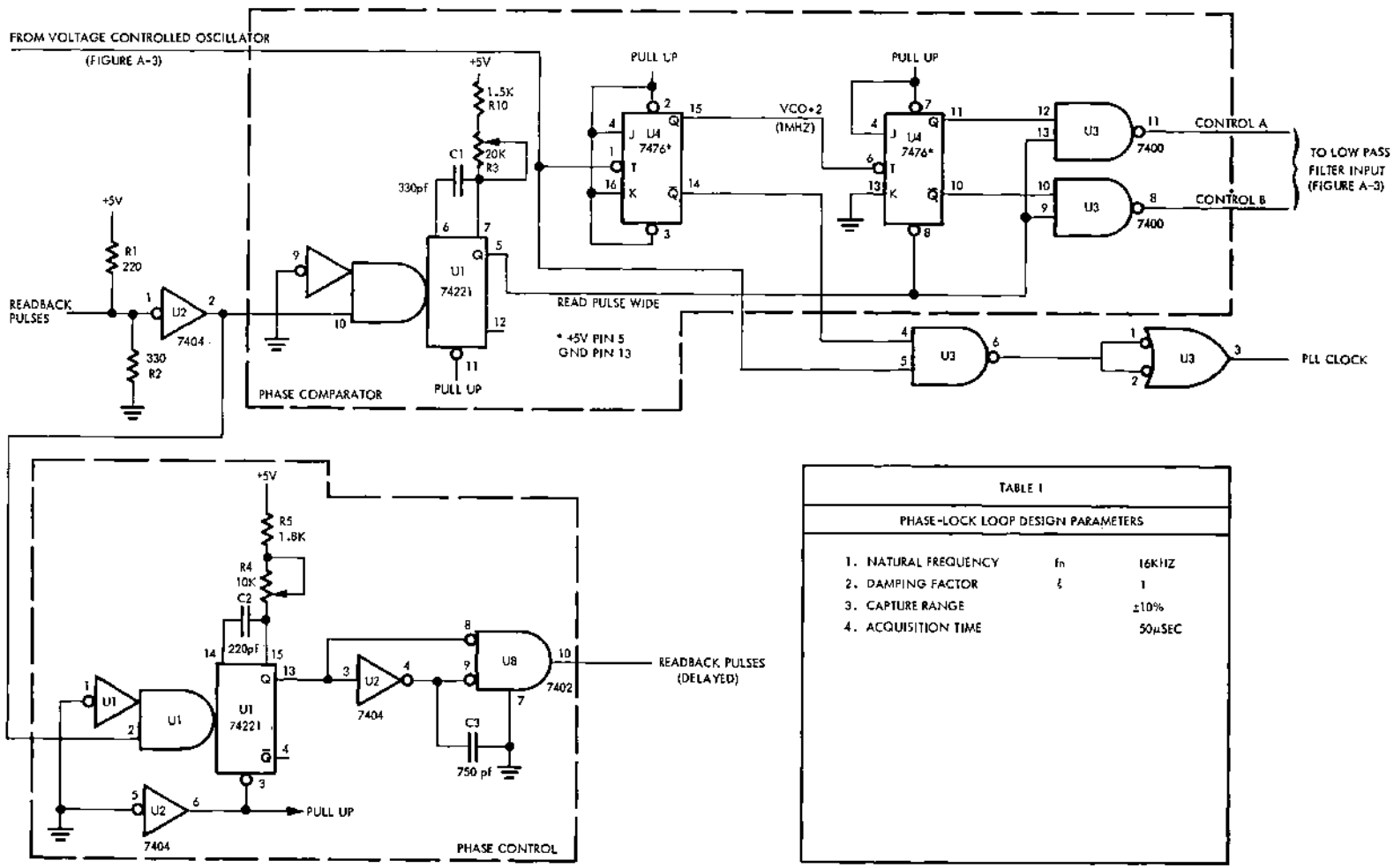
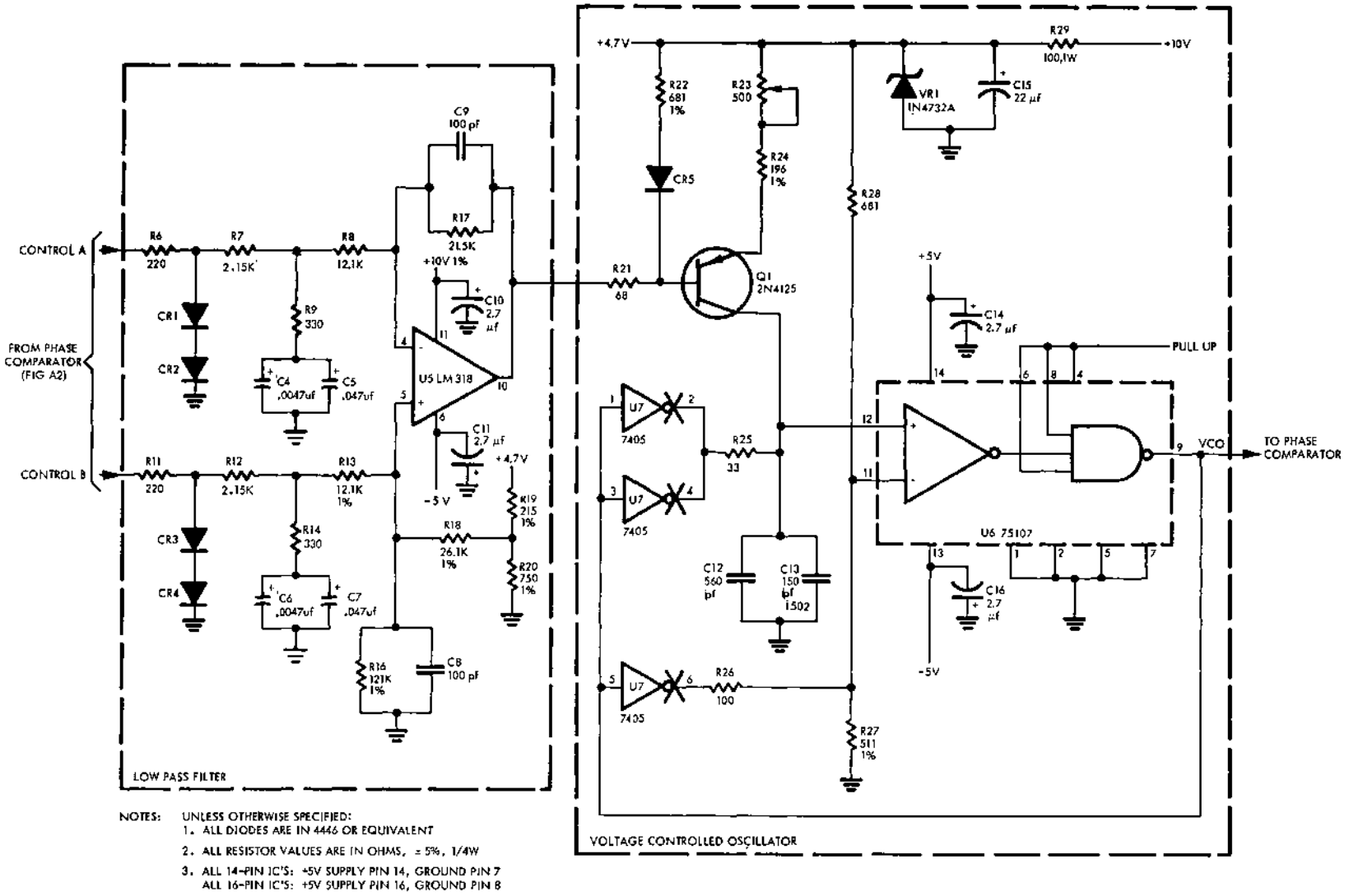


TABLE I		
PHASE-LOCK LOOP DESIGN PARAMETERS		
1. NATURAL FREQUENCY	fn	16KHZ
2. DAMPING FACTOR	ξ	1
3. CAPTURE RANGE		±10%
4. ACQUISITION TIME		50μSEC

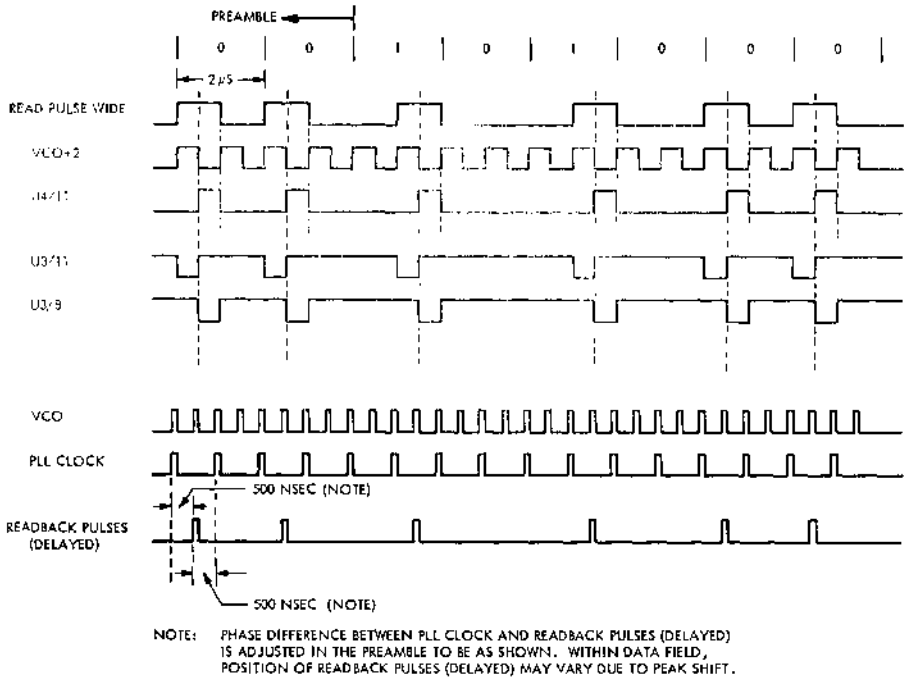
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES ARE IN 4446 OR EQUIVALENT
2. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
3. ALL 14-PIN IC'S: +5V SUPPLY PIN 14, GROUND PIN 7
   ALL 16-PIN IC'S: +5V SUPPLY PIN 16, GROUND PIN 8
4. DESIGN PARAMETERS FOR PLL SHOWN IN TABLE I

Figure A-2. PLL (Phase Comparator, Phase Control) Schematic Diagram



NOTES: UNLESS OTHERWISE SPECIFIED:
1. ALL DIODES ARE IN 4446 OR EQUIVALENT
2. ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4W
3. ALL 14-PIN IC'S: +5V SUPPLY PIN 14, GROUND PIN 7
   ALL 16-PIN IC'S: +5V SUPPLY PIN 16, GROUND PIN 8

Figure A-3. PLL (Low Pass Filter, Voltage Controlled Oscillator) Schematic Diagram



NOTE: PHASE DIFFERENCE BETWEEN PLL CLOCK AND READBACK PULSES (DELAYED) IS ADJUSTED IN THE PREAMBLE TO BE AS SHOWN. WITHIN DATA FIELD, POSITION OF READBACK PULSES (DELAYED) MAY VARY DUE TO PEAK SHIFT.

Figure A-4. Phase Comparator Timing Diagram (Phase-Locked Condition)

NOTES

PERTEC

PERTEC reserves the right to change specifications at any time. It is PERTEC policy to improve products as new techniques and components become available.

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