SECTION V
DETAILED ELECTRICAL AND LOGIC DESCRIPTION

5.1 INTRODUCTION

This section contains the theory of operation of the PCBAs used in the D3000 Disk Drive. Schematic and assembly drawings for each board are contained at the end of Section VII.

5.2 LOGIC TERM MNEMONIC IDENTIFICATION

All digital signals in the D3000 Disk Drive are identified by a name which will be referred to as the logic term.

Logic terms may be descriptive of a condition or an event, or they may be a generalized name used primarily for documentation purposes. If a descriptive name is essential to facilitate the understanding of a function, a generalized term is not used.

Appendix A of this manual contains the mnemonic listing for the standard D3000 Series Disk Drive. An understanding of the mnemonic scheme employed is essential to the total understanding of the D3000 logic drawings. Also included in Appendix A are figures and tables which provide the user with an understanding of the six character logic term.

5.3 SERVO PCBA

The following paragraphs describe the Servo PCBA installed in the D3000 Series Disk Drive. Refer to Schematic No. 102810 and Assembly No. 102811.

The Servo PCBA is approximately 254 mm (10 inches) square with two connectors along one edge. Figure 5-1 illustrates the placement of each connector, test point, and adjustable component on this board. J201 and J202 are the connectors which connect via mating plugs and 3M flat cables to the Logic PCBA. The remainder of connectors are of the Molex type.

In general, the connectors perform the following functions.

(1) Electrically connect the Servo Board to all base casting-mounting assemblies, e.g., power supply, positioner coil, velocity and position transducers, emergency unload capacitor, brush motor, cartridge lock solenoids and heatsinks.

(2) Provide power to the Logic PCBA.

(3) Provide a path for signals and levels between the Servo and the Logic PCBAs.

(4) Provide a path for the +5v and control signals to the motor control board.

(5) Provide a path for temperature compensation signals from the Temperature Compensation PCBA to the Servo PCBA (200 tpi models).

Contained on the Servo PCBA are the electronics for voltage regulators, positioner, emergency unload system, ac motor speed control circuits, brush motor driver, cartridge lock solenoid driver, and power clear circuit.

The circuit board description in the following paragraphs consists of the circuits associated with each of the connectors.

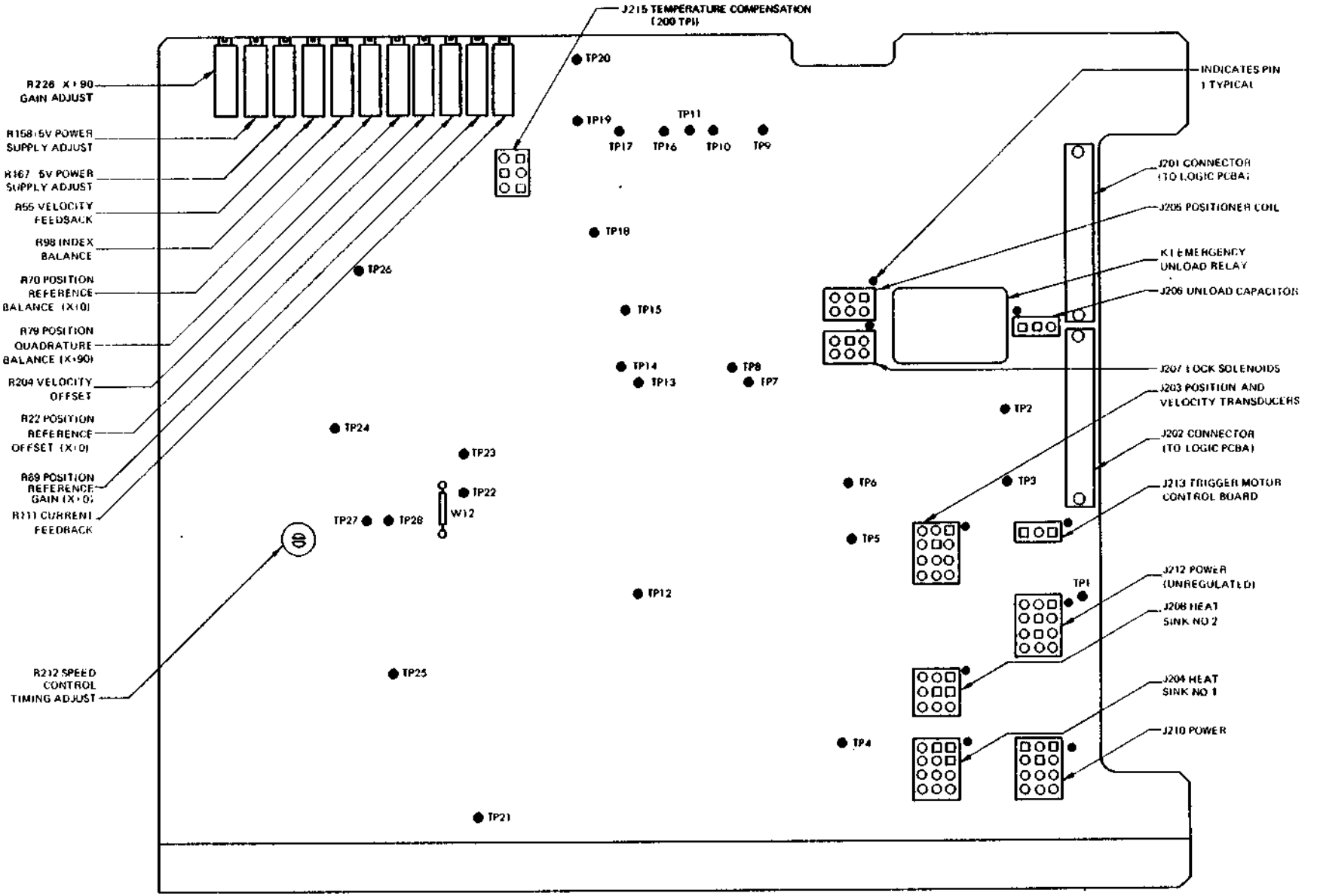

Figure 5-1. Servo PCBA Test Point and Connector Placement

5.3.1 VOLTAGE REGULATORS

The power supply voltage regulators are shown on Schematic No. 102810, sheet 2. J212 (zone F16) connects unregulated +20v, —20v, +10v, and auxiliary 21v ac for the brush motor driver and ac motor control circuit to the Servo PCBA. Note that two pins are allocated to the high current lines to reduce the current density in the pins.

The +10v and —10v regulators are series regulators using zener diodes VR4 and VR10, respectively, for the voltage reference. The emitter base junction of Q28 is in series with VR4, and diode CR43 is in series with VR10, thus improving the temperature stability of the supplies.

The +5v and —5v regulators consist of two similar circuits whose outputs are set by potentiometers R158 (zone F14) and R167 (zone E14). Outputs of the +5v and —5v regulators can be monitored at TP4 and TP12, respectively. Operational amplifiers U15 and U18 are used as voltage followers in the regulating circuit. The high open-loop gain of the operational amplifier in the feedback regulating circuit offers improved line and load regulation characteristics to the +5v and —5v supplies. Zener diodes VR7 and VR11 provide the voltage references for +5v and —5v. Diodes CR38, CR40, and CR42, CR44 improve the temperature stability of the supplies.

Regulator power transistors Q24, Q25, Q26, Q33 are mounted on heatsinks external to the Servo PCBA. J204 and J208 connect the regulators to the external heatsink.

A *crowbar* over-voltage protection circuit is provided for the +5v and —5v supplies. These circuits are employed to detect an increase of 3v in the +5v supplies. Zener diodes VR8 (zone F11) and VR9 (zone E12) detect an increase in the +5v and —5v supplies, respectively. An increase to +8v or —8v causes SCR3 or SCR4 to fire, which in turn causes the +20v or —20v fuse on the power supply module to blow, thus removing the relevant 20v supply.

A *crowbar* over-voltage protection circuit is also provided on +10v and —10v supplies and employ zener diodes VR5 and VR6 (zone F15), VR12 and VR13 (zone D14), respectively, to detect an increase in the +10v supplies. A voltage increase to +15v or —15v causes SCR2 to blow, thus removing the relevant 20v supply.

J209 (zone G,H-10) and J211 (zone D,E-10) are jumper plugs which connect unregulated +20v and regulated +5v and +10v from regulators to the remainder of the circuits on the Servo PCBA and to the Logic PCBA via J210. These jumper plugs enable the isolation of the regulators and power supply for maintenance purposes.

The unregulated +20v supplies are used in the positioner power amplifier and the power clear circuit. In addition, the —20v supply is used in cartridge lock solenoid driver and emergency unload relay driver. The +5v regulators supply power to the digital ICs, linear ICs, mode control electronics, brush motor driver, ac motor control circuit, relay driver, and cartridge lock solenoid driver. The +10v regulators supply power to the operational amplifiers, velocity function generator, mode control electronics, position transducer signal conditioners, and position transducer lamp driver.

5.3.2 POSITIONER SERVO ELECTRONICS

The positioner electronics consists of the Velocity Function Generator, Mode Control circuits, Position Transducer Signal Conditioners, Velocity Transducer Amplifier, Summing Amplifier, Positioner Power Amplifier, Position Transducer Lamp Driver Failure Detector, and the Emergency Unload System. Refer to Paragraph 5.2 for definition of logic term mnemonics used in the following descriptions.

J20l provides a path for the majority of logic command signals for the positioner servo system from the Logic PCBA to the Servo PCBA. J202 provides a path for the remaining logic signals from the Logic PCBA to the Servo PCBA, and vice versa.

5.3.2.1 Velocity Function Generator

The Velocity Function Generator is shown on Schematic No. 102810, sheet 1. This circuit generates a step voltage signal of known polarity (positive or negative) which can be monitored at TP9 (zone H15). The polarity of this signal is dependent upon the state of logic command signals NLAD0G, NLAD1G, NLAD2G, NLAD3G, NLAD4G, NLAD5G, NLAD6G, NLAD7G, NLADEG, and LFDX1. Assume that the address difference is non-zero and is such that the signals at pin 19, 18, 27, 28, 29, 30, 33, 31, 32 of J201 are in the logic low state, i.e., signals are active. Correspondingly, the output logic state of ICs U3-A, U3-B, U3-C, U3-D, and U5-A, U5-D will be high causing diodes CR1, CR3, CR5, CR7, CR9, and CR11 to be reverse-biased.

Diodes CR2, CR4, CR6, CR8, CR10, and CR12 are forward-biased and current flowing through resistor network R1 and R2, R7 and R8, etc., is summed at the summing junction (pin 2) of operational amplifier U8 (zone H15). The otput at TP9 will be +6v depending on the state of Forward Direction (LFDX1) logic signal. When LFDX1 is high, the output at TP9 will be +6v and when LFDX1 is low, the output at TP9 will be —6v. Similarly, when the address difference is zero, the state of the logic command signals NLAD0G through NLADEG is such that the output logic state of ICs U3-A, U3-B, U3-C, U3-D, and U5-A, U5-D will be low, and diodes CR1, CR3, CR5, CR7, CR9, CR11 will be forward-biased. Diodes CR2, CR4, CR6, CR8, CR10, and CR12 are reverse-biased and no current flows from the resistor network into the summing junction of U8 except from R24 and R25. Consequently, the output at TP9 will be +0.3v depending on the state of logic signal LFDX1.

A third possibility exists when the address difference is non-zero and the state of signals NLAD0G through NLADEG is such that some of the output logic states at the outputs of U3-A, U3-B, U3-C, U3-D, and U5-A, U-5D are high and others are low. In that case, the output at TP9 will be a voltage step in between +6v and +0.3v depending on the output logic states of U3-A, U3-B, U3-C, U3-D, and U5-A, U5-D.

Velocity Reference Enable (NLVREG) going low at pin 20 of J201 turns Q3 (zone F15) on and current flows from TP9 through R15 and into the summing junction (pin 2) of the summing amplifier U16 (zone G12). When NLVREG is high, Q3 is turned off and no current flows into the summing junction of U16. Hence, FET Q3 acts as a switch which enables the velocity reference signal at TP9, generated by the velocity function generator, to be passed into the summing junction of the summing amplifier U16.

5.3.2.2 Mode Control

The Mode Control circuitry is shown on Schematic No. 102810, sheet 1. When Track Offset Plus (NLTOPG) at pin 26 of J201 (zone E19) is low and Track Offset Minus (NLTOMG) at pin 25 of J201 is high, transistor Q5 is off and Q6 is on; consequently, the signal at TP11 will be +4.5 ±1.0v. Conversely, a high state of NLTOPG and a low state of NLTOMG turns Q5 on and turns Q6 off, and the voltage at TP11 will be —4.5v ±1.0v. When NLTOPG and NLTOMG both are high, transistors Q5 and Q6 are both on and the voltage at TP11 will be 0v.

Forward Slow Mode (NLFSM1) low at pin 24 of J201, Reverse Slow Mode (NLRSM1) high at pin 23 of J201 and the high output of U10-A pin 4 (i.e., Heads Retracted (SHRXG) low at TP14, zone D11) causes Q7 and Q10 (zone C16) to turn off, and Q8 (zone C17) to turn on. Thus, the signal at TP10 will be +4.5v ±1.0v. Conversely, when NLFSM1 is high,

NLRSM1 is low and SHRXG is low, Q8 and Q10 are turned off and Q7 is turned on. Consequently, the signal at TP10 is —4.5v ±1.0v. When NLFSM1 is high, NLRSM1 is low and SHRXG is high, Q8 is turned off. However, Q10 and Q7 are turned on and the signal at TP10 is approximately 0.3v. Finally, when NLFSM1 and NLRSM1 are high, Q7 and Q8 are turned on, and regardless of the state of SHRXG, the voltage at TP10 is 0v.

Potentiometer R22 (zone F16) is used to adjust for the dc offsets when the servo is in the Position Mode. TP19 and R40 (zone D15) provide a means to introduce an external perturbation signal into the summing amplifier.

5.3.2.3 Position Transducer Signal Conditioners

The Position Transducer Signal Conditioner circuitry is shown on Schematic No. 102810, sheet 1. These circuits are employed to amplify the low level position transducer signals (X + 0, X + 90, Index, Heads Retracted) and convert them to appropriate logic signals (SPRCG, SPQCG, SPTIG, and SHRXG). J203 (zone A15) connects all position transducer signals and velocity transducer signals to the Servo PCBA. Outputs from the Position Transducer Signal Conditioners are routed to the Logic PCBA via edge connector J202 (zone B11).

Figure 5-2 describes the position transducer output signals, namely Heads Retracted, Index, X + 0 and X + 90, at pins 6, 1, 3, and 2, respectively, of connector J203, as the positioner carriage is moved in the forward direction, i.e., toward the spindle. The amplitude of the Heads Retracted and Index signal is approximately 10 mv at pins 6 and 1 of J203, respectively. The amplitude of X + 0 and X + 90 signal is approximately 120 mv to 200 mv, at pins 3 and 2 of J203, respectively.

The output of the Heads Retracted, Index, X + 0, and X + 90 amplifiers can be monitored at TP6, TP3, TP20, and TP2, respectively. Figure 5-3 describes the output of these amplifiers and should be referenced in conjunction with Figure 5-2.

Potentiometers R70 (zone F14), R79 (zone E14), R98 (zone C14) provide dc bias for balance adjustments of the X + 0, and X + 90 and Index signals, respectively. R69 (zone F13) provides gain adjustments for (X + 0) signal at TP20. R226 (zone E14) provides gain adjustments for (X + 90) signal at TP2. Type 741 operational amplifiers (U1, U2, U6, and U7) are used as high gain inverting amplifiers to amplify these signals.

When R69 (the X + 0 gain potentiometer) and R70 (the balance potentiometer) are properly adjusted, the output at TP20 should be 12v peak-to-peak. The X + 0 amplifier output at TP2 should be between 6v peak-to-peak and 12v peak-to-peak. The change in transition (from positive to negative and vice versa) at TP6 and TP3 should be from +7v +5v to —7v +5v and vice versa when R98, the Index balance potentiometer, is properly adjusted.

The amplified Heads Retracted, Index, X + 0, X + 90 (see Figure 5-2) are then converted into their corresponding logic signals shown in Figure 5-3, namely Heads Retracted (SHRXG), Position Transducer Index (SPTIG), Position Reference Clock (SPRCG), and Position Quadrature Clock (SPQCG). These logic signals can be monitored at TP14, TP7, TP8, and TP13, respectively. Type 75107 dual line receivers (U11-A, U11-B, U10-A, U10-B) are used in the circuit as comparators for analog-to-digital conversion.

The R-C network in the feedback loop around comparators U11-A, U11-B, and U10-A, U10-B provides ac and dc hysteresis. An example of this network is C5, R76, R77, and R85 in the feedback path of U11-B (zone D13). These networks assure a single transition crossover detection of the analog input signals and provide good dc noise margins for analog inputs to the comparators.

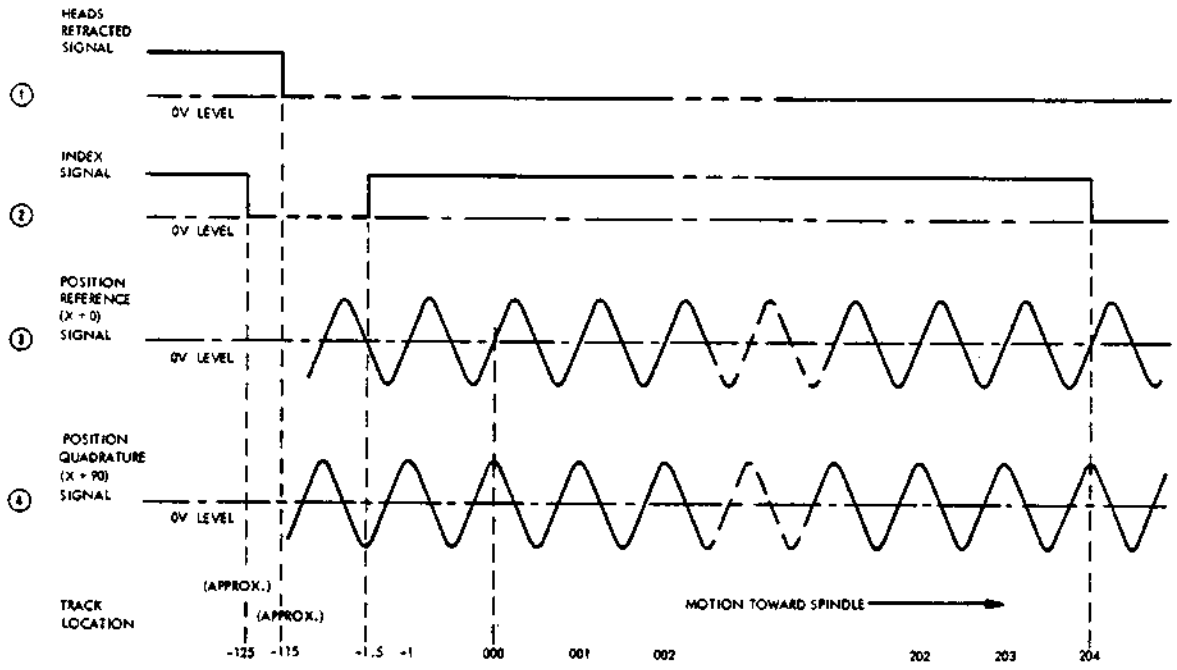

Figure 5-2. Position Transducer Output Signals

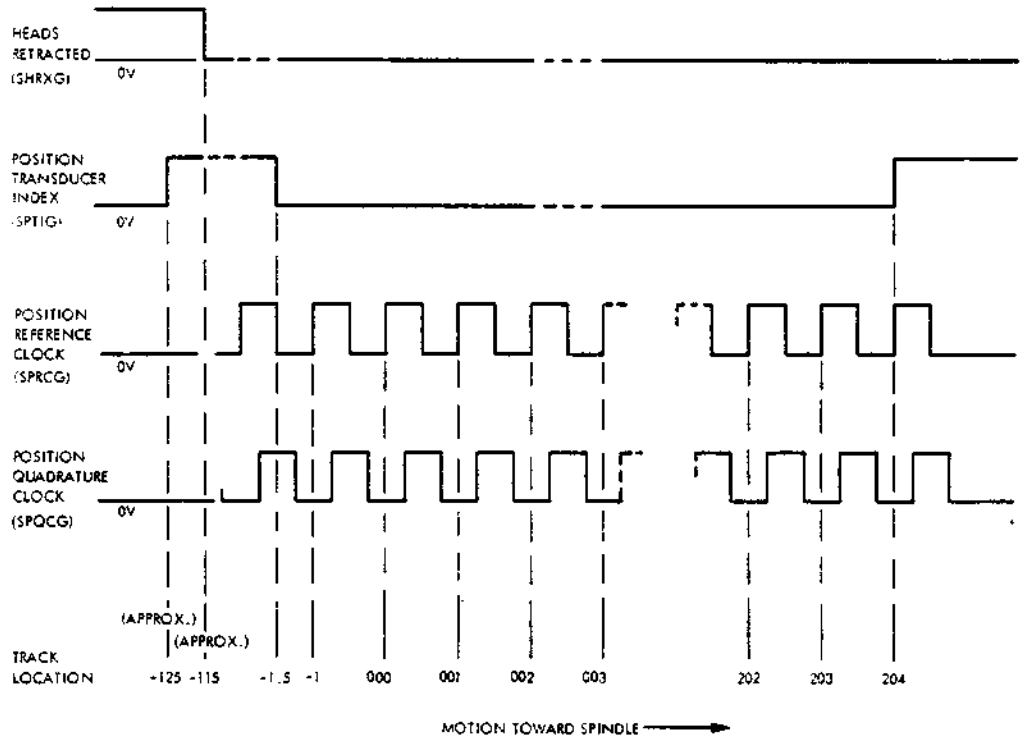

Figure 5-3. Position Transducer Signal Amplifier Outputs

5.3.2.4 Tachometer Amplifier

The Tachometer Amplifier shown on Schematic No. 102810, sheet 1, amplifies and inverts the velocity feedback signal from velocity transducer. This feedback signal is routed from pin 9 of J203 (zone A15) to the input of U14 (zone G14). U14 is a Type 741 operational amplifier which is used as a summing amplifier. Potentiometer R204 provides offset balance adjustments for U14.

When Reverse Slow Mode (NLRSM1) at pin 23 of J201 is low and Heads Retracted (SHRXG) at pin 28 of J202 is high (i.e., when the positioner servo is in the Reverse Slow Mode and the heads are retracted) Q11 (zone G14) turns on and the output of velocity transducer is grounded. This action removes the velocity feedback signal from the input of U14 and causes the output of U14 at TP16 to go to 0v.

5.3.2.5 Summing Amplifier

The Summing Amplifier U16 (zone G13) is shown on Schematic No. 102810, sheet 1. This amplifier sums the following reference, feedback or control signals of the positioner servo system.

(1) Velocity reference signal.
(2) Velocity feedback signal.
(3) (X + 0) position feedback signal.
(4) Offset signal.
(5) Track offset-plus and track offset-minus signal.
(6) Reverse slow velocity mode, forward slow velocity mode, and reverse slow and heads up velocity mode signal.
(7) External perturbation input signal.
(8) Temperature compensation and head alignment (200 tpi).

The positioner servo system normally operates in the Velocity Mode. Velocity feedback is provided continuously except when Reverse Slow Mode (NLRSM1) is low and Heads Retracted (SHRXG) is high, i.e., the servo is in the Reverse Slow Mode and the heads are retracted. At this point velocity feedback is cut off.

The Velocity Reference Enable signal (NLVREG) (pin 20 of J201) going low turns on Q3 (zone F15) and enables the velocity reference signal from TP9 into the summing junction of U16 (zone G13). The Position Mode signal (LPMXG) (pin 22 of J201) going high turns on Q13 (zone G13) enabling the X + 0 signal from U7 (zone F14) into the summing junction of U16. Thus, the servo is placed in the Position Mode.

The Forward Slow Mode signal (NLFSM1) low, and the Reverse Slow Mode signal (NLRSM1) high at pins 24 and 23 of J201, respectively, introduces a Forward Slow Mode signal (at TP10) into the summing junction of U16. This can be monitored at TP10 (zone D16). Conversely, NLFSM1 high and NLRSM1 low introduces a Reverse Slow Mode signal (monitored at TP10) into the summing amplifier.

Track Offset Plus (NLTOPG) and Track Offset Minus (NLTOMG) signals are introduced at the summing junction of U16 only when the servo is in the Position mode of operation. NLTOPG (pin 26 of J201) low and NLTOMG (pin 25 of J201) high introduces the Track Offset Plus signal; NLTOPG high and NLTOMG low introduces the Track Offset Minus signal into the summing junction of U16. These signals can be monitored at TP11 (zone E16.) TP19 is provided to introduce an external perturbation signal into the summing junction. Potentiometer R22 (zone F16) is provided for nulling the X + 0 signal in reference to servo ground.

Referring to the summing junction of U16 it can be seen that the amplifier gains for any particular input signal is determined by the ratio of feedback resistor R60 (zone G12) and the resistor in series with the input signal. For example, the gain of the summing amplifier for any external input signal at TP19 (external perturbation signal) is R60 divided by R40. Zener diodes VR1 and VR2 (zone H13,12) are employed to limit the output of summing amplifier at TP17 to +6v. TP18 is the test point for servo ground. It should be noted that servo ground is depicted on the schematic as G(S) and logic ground is shown as G(L).

5.3.2.6 Positioner Power Amplifier

The Positioner Power Amplifier is shown on Schematic No. 102810, sheet 1 (zone G11). This amplifier is a linear feedback transconductance amplifier. It is referred to as a transconductance amplifier because its output current is proportional to the input voltage to the power amplifier.

The input to the power amplifier circuit is the output signal of the Summing Amplifier U16, which can be monitored at TP17. When the signal at TP17 is positive, Q16 turns on, causing Q19 to conduct which, when relay K1 (zone C10) is energized, connects —20v through R125, the positioner coil via J205 and R110 to ground. Conversely, when the signal at TP17 is negative, Q15 turns on, causing Q18 to conduct which, when relay K1 (zone C10) is energized, connects +20v through R114, the positioner coil via J205 and R110 to ground.

J205 (zone C7) connects the positioner coil to the Servo PCBA, thus establishing a path for current through the coil and corresponding series resistors. The voltage drop across R110, which is proportional to the current through R110, is fed back to the power preamplifier U17 (zone G11). U17 compares the input voltage and the feedback voltage which is proportional to the current through the coil, and turns off Q16 or Q15 and Q19 or Q18 when the output current at TP5 is equal to some constant of proportionality times the input voltage at TP17. Potentiometer R111 (zone F12) is provided to adjust and vary this transconductance of the power amplifier.

Q14 (zone H10) and Q17 (zone E10) limit the maximum output current of the amplifier. The voltage drop across R125 or R114 and the value of R122 and R124 or R115 and R113 determine the maximum value of current through Q19 or Q18, respectively.

Additional current limiting is provided by VR1 and VR2 which limit the voltage at TP17 to +6v, and the adjustment of R111. This value of current is normally adjusted lower than that provided by the limiting values of Q14 and Q17.

Resistors R118 and R119 (zone F10) provide an internal voltage feedback loop in the power amplifier stage. R-C networks C12 and R117, C13 and R120, C29 and R203 assures the high frequency stability of the power amplifier and eliminates high frequency oscillations.

5.3.2.7 Position Transducer Lamp Failure Detector

J203 pins 10 and 12 shown on Schematic No. 102810, sheet 1 (zone E12), connect the Position Transducer Lamp to the Servo PCBA. In normal operation, the lamp is driven from +10v with resistor R128 in series between the lamp and ground. When the lamp is operating normally, i.e., illuminated, the voltage drop across R128 turns on Q20. Thus, the Position Transducer Failure signal (SPTFG) at pin 18 of J202 is low. Should the lamp fail, Q20 is turned off and SPTFG goes high, thereby detecting the lamp failure.

5.3.2.8 Emergency Unload System

The Emergency Unload system, shown on Schematic No. 102810, sheet 1, consists of an Emergency Unload Relay (zone C9), a Relay Driver (zone E6), and an Emergency Unload Charging Network (zone A9). The Emergency Unload Enable signal (LEUEG) going low at J202 pin 32 turns on Q21 (zone E6), energizing the relay coil. The relay contacts are connected in such a manner that when the relay is energized the power amplifier is connected to the positioner coil. When relay is de-energized, the positioner coil is connected to the unload capacitor which in series with the parallel combination of R129 and R130.

J206 (zone A7) connects the unload capacitor to the Servo PCBA. When the Emergency Unload Relay is energized, the unload capacitor is charged to —10v with R131 limiting the charging current. When the relay de-energizes, the positioner coil is connected to the unload capacitor and the capacitor discharges via the parallel combination of R129 and R130 and the positioner coil, thus retracting the carriage and heads to the fully retracted position.

Capacitors C63, C64, C65, and C66 are provided across the contacts of the Emergency Unload Relay to suppress high frequency noise (RFI) generated while switching the positioner coil to either the Power Amplifier or the Unload Capacitor.

The Emergency Unload Relay Driver consists of Q21 which is connected as a transistor switch in series with the relay coil and resistor R136. Diode CR30, across the relay coil, is provided to protect transistor Q21 from large negative voltage surges when Q21 is turned on and off. In normal operation, LEUEG is low, emitter-base junction of Q21 is forward-biased, turning on Q21. If LEUEG goes high, or if LEUEG is low and the +5v drops to approximately 3.8v, Q21 turns off, de-energizing the relay, and retracting the carriage.

5.3.3 AC MOTOR CONTROL CIRCUITS

AC Motor Speed Control circuits, shown on Schematic No. 102810, sheet 1 (zone E3), convert logic control signals, namely Increase Motor Speed (NLIMS1), Brake Cycle Enable (NLBCEG), and Drive Motor Enable (NLDMEG) at J202 pins 21, 23, and 20, respectively, to the appropriate control signal at TP22 which fires the triac control circuit on the AC Motor Control PCBA. This control signal and +5v is connected via J213 (zone E2) to the Motor Control PCBA.

The 21v ac (peak) 60 Hz sine wave (zone D5) is clamped by diodes CR34 and CR35 (zone D5), then converted into 60 Hz square wave digital signal by comparator U21-A. The ac and dc hysteresis in the comparator circuit is provided by the network formed by C15, R146, R147, and R138.

Referring to the 21v (peak) voltage at zone D5 of the schematic, it can be seen that the voltage is phase advanced by the network formed by C50, C51, C52, R208 and R209, then converted into a 60 Hz square wave digital signal at TP28 using comparator U25-B (zone C4).

The digital signal outputs of comparators U21-A and U25-B at TP23 and TP28 are fed into an Inverse Exclusive OR circuit formed by U20-C, U20-D, and U19-B, U19-C. The output signal at pin 8 of U19-C is a 120 Hz digital signal which is used as the switching signal for transistor switch U26-A.

The circuit consists of R212, R213, R214, C54, C55 and the transistor switch U26-A. This combination generates a sawtooth waveform at 120 Hz. When the signal at U26-A pin 1 and 2 is high, the transistor in the output state is cut off and capacitors C54 and C55 charge through R212, R213, and R214 to generate a ramp output at TP27. Conversely, when the signal at U26-A pin 1 and 2 goes low, the transistor in the output stage is turned on and discharges capacitors C54 and C55 through R214. Since the value of R214 is much smaller than the sum of R212 and R213, the discharge time constant is much smaller than the charge time constant. Thus, the 120 Hz sawtooth waveform is generated and can be monitored at TP27. Potentiometer R212 (zone C2) is used to adjust the peak-to-peak amplitude of the sawtooth waveform which is fed to pin 1 of comparator U25-A (zone C3) along with the output of operational amplifier U24 (zone F5).

The network associated with the operational amplifier U24 (zone F5) is an integrator circuit. When the Increase Motor Speed signal (NLIMS1) is high, the output at TP24 is a ramp function whose time constant is dependent upon the value of R215, R216, R217, C56, C57, C58, and C59. Diodes CR51, CR52, CR53, and CR54 limit the maximum positive voltage to approximately 2.0v. Diodes CR55, CR56, and resistor R218, limit the lower excursion of the voltage to approximately 0v. Thus, when NLIMS1 is low, the steady state value of the output voltage at TP24 is approximately 0v.

The dc voltage at TP24, which is proportional to the NLIMS1 pulses, and the reference 120 Hz sawtooth waveform from U26-A (zone C3) are compared in comparator U25-A (zone E3). Thus, the signal at TP22 is either high or low, depending on the error in voltage between these two signals.

The operation of the AC Motor Speed Control circuit during start-up, constant speed control, and brake cycle can be summarized briefly as follows. During start-up, NLIMS1 is low, NLBCEG is high, and NLDMEG is low at J202 (zone F6). The output of the integrator at TP24 is approximately 0v which, when compared with the reference 120 Hz sawtooth waveform, makes TP22 low. The low output of U25-A at TP22 triggers the triac on the Motor Control PCBA every cycle, with practically full cycle power to the motor, allowing the motor to come up to the speed.

When the motor comes to correct speed, depending on the error in speed, NLIMS1 is either high or low and the voltage at TP24 is such that when compared with the reference sawtooth waveform at TP27, it will generate a correction pulse at TP22. This correction pulse triggers the triac on the Motor Control PCBA at a specific part of the ac waveform so that power is on for only part of the cycle. In other words, firing the triac at a specific time in one cycle of an ac waveform achieves the phase angle control of the ac waveform, thereby controlling the power to the motor.

During a stop sequence, NLDMEG is high. When NLBCEG is also high (i.e., brake cycle is not enabled), the output at U19-A pin 3 (zone E4) is low and the signal at TP22 is high all the time, and the triac is turned off. Hence, the power to the motor is cut off and the motor speed coasts down. When a brake cycle is enabled, NLBCEG is low, the signal at U19-A pin 3 is high. Also, the signal at TP28 (zone C4) is high all the time; hence signals at TP23 and U19-C pin 8 (zone C3) are 60 Hz square wave digital output. Consequently, the frequency of the reference sawtooth waveform at TP27 is 60 Hz. The low state of NLBCEG also makes U26-B pin 5 at ground potential. Since NLIMS1 is high, the voltage at TP24 is approximately 2v and U25-A pin 2 is approximately 0.7v. Thus the output at TP22 is a 60 Hz pulse train. Since the frequency of the trigger pulses at TP22 is 60 Hz as opposed to 120 Hz, the triac fires during only one-half of each cycle. The width of the pulse at TP22 controls the firing angle on the ac waveform, therefore braking power applied during each half cycle.

5.3.4 CARTRIDGE LOCK SOLENOID DRIVER

The Cartridge Lock Solenoid Driver circuit is shown on Schematic No. 102810, sheet 2 (zone B6). This circuit consists of a transistor switch connected in series with lock solenoids across +5v and −20v. J207 (zone B3) connects the coil of the lock solenoids to the Servo PCBA circuitry.

The Lock Cartridge Mechanism signal (LLCMG) low at J202 pin 33 causes Q43 and Q42 to turn on. This action applies approximately 24v across the solenoid coil which energizes the solenoids, pulling the plungers into the coil. When LLCMG is high, Q43 and Q42 are turned off, and the solenoid is de-energized, releasing the plungers.

5.3.5 POWER CLEAR CONTROL CIRCUIT

The Power Clear Control circuit is shown on Schematic No. 102810, sheet 2 (zone F4). This circuit detects fault conditions in the +5v, +20v, and −20v dc supplies and provides the Power Clear signal (SPCSA) to the Logic PCBA. J202 pin 30 (zone B8) connects the Plus 5 Volts signal (LP5VA) to the Power Clear Circuit at TP26. J202 pin 31 (zone E3) supplies the Power Clear signal (SPCSA) to the Logic PCBA.

Figure 5-4 illustrates the waveforms associated with fault detection on the +5v line. The signals at various nodes in the circuit have been drawn on the functional timing diagram for explanation purposes and should be referred to in conjunction with Schematic 102810, sheet 2.

LP5VA high (plot 1) charges capacitor C28 (zone D4) through R181. Zener diode VR18 clamps and maintains the base of Q38 to +2.7v nominal (plot 2). Capacitor C27 (zone D5) is charged to approximately +2.1v nominal through diode CR49 and resistor network R179 and R195. The charging time constant of C27, R179 and R195 is much longer than that of C28 and R181. Consequently, the base of Q37 comes to the +2.7v level with a slow rise time (plot 3). When the base of Q37 is +2.7v nominal, transistor Q37 turns on and lowers the voltage on the base of Q36 to less thatn +5v, turning on Q36. The collector of Q36 will be at approximately +4.8v nominal. Resistor R188 provides positive feedback to the base of Q37, hence, a clean, fast edge of the signal is obtained at the point of transition (plot 4) and at J202 pin 31 (SPCSA) (plot 5).

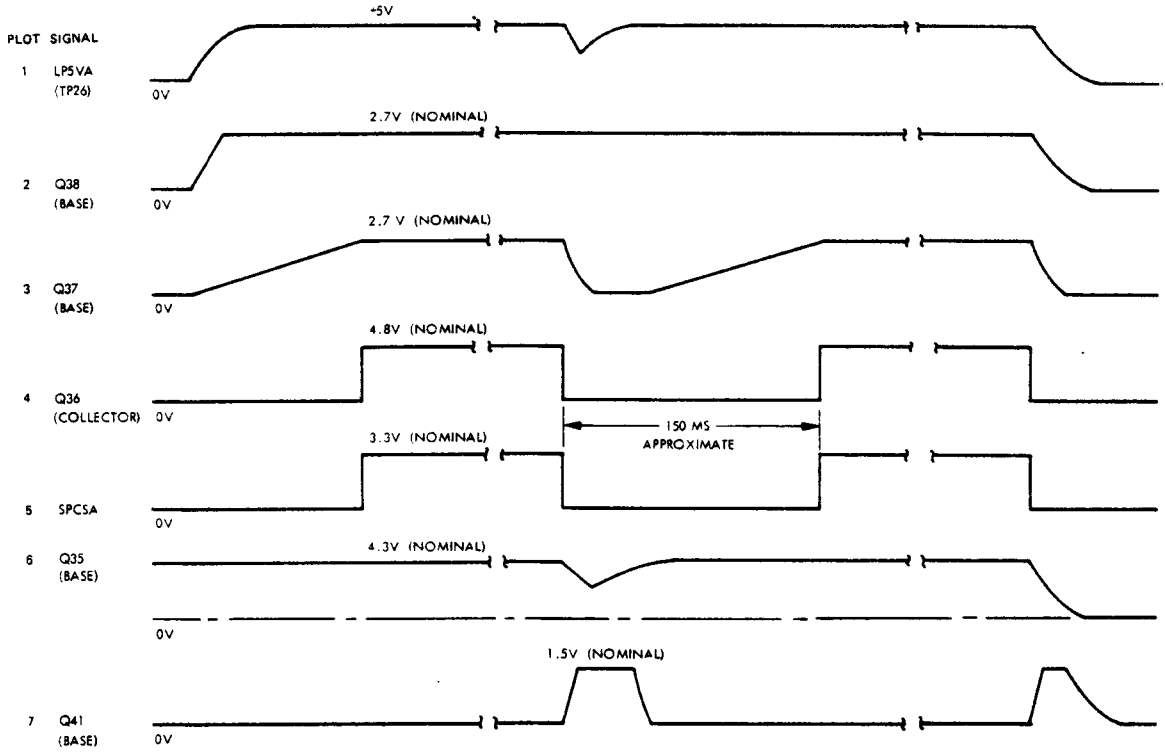

Figure 5-4. Fault Detection Waveforms

The amplitude of SPCSA is approximately 3.3v when high since there is a 150-ohm resistor inserted on the Logic PCBA between the SPCSA signal line and ground.

In the case where the +5v at TP26 sags momentarily and correspondingly the voltage at the base of Q37 goes below 2.7v such that Q37 is turned off, the following actions occur. Q36 turns off instantaneously and R188 provides positive feedback to achieve the sharp transition at the collector of Q36. Since Q36 is off, the collector of Q36 is at ground potential and capacitor C26 is charged from the charge of C25. The difference in potential at the base of Q35 turns on Q35 which turns on Q41. Capacitor C27 discharges through R193. The discharge and charge time constants associated with C25 and C26 are such that transistor Q35 is turned on for a longer time than the time required to discharge C27 through R193. Plots 6 and 7 of Figure 5-4 describe typical waveforms of Q35 base and Q41 base voltages, respectively. SPCSA will also be low since the collector of Q36 is at ground potential.

Once the base of Q35 recovers to the same potential as its emitter (4.3v), Q41 is turned off and C27 charges through the network formed by R179 and R195 until the base of Q37 is at +2.7v. This, in turn, turns on Q37 and Q36 and the collector of Q36 goes to +4.8v and SPCSA goes high (plots 3, 4, 5). The approximate time taken for SPCSA to go high after it has been in a low state is 150 msec.

The following action occurs when LP5VA at TP26 goes low permanently from its high state. The collector of Q36 goes to ground potential and SPCSA goes low. The signals at the base of Q38, Q37, Q35, and Q41 are shown in plots 2, 3, 6, 7, respectively.

Similarly, if the +20v goes below approximately +13v nominal, Q34 turns off and the cathode of CR48 goes to ground potential. This, in turn, causes Q37 to turn off and the sequence of events that occurs is identical to +5v drop-off previously described. When the +20v is approximately +16v or higher, Q34 turns on and the cathode of CR48 is at approximately 5.4v (if the +20v line is at +20v) which reverse-biases CR48, and the base of Q37 gets charged to 2.7v again to turn on Q37.

Similarly, if the —20v is maintained at its nominal potential, Q40 is on and the base of Q39 is at approximately —2v which turns off Q39. The cathode of CR48 is at +5.4v, which reverse-biases CR48 and hence a normal charging sequence of C27 occurs until Q37 turns on. When the —20v goes above —13v, Q40 turns off and Q39 turns on. CR48 cathode goes to ground potential and the sequence of events that occur is identical to +5v drop-off previously described.

It should also be noted that resistors R188 and R190 provide hysteresis in the circuit so that the voltage (+5v, +20v, or —20v) at which SPCSA goes high is always slightly higher than when it goes low.

5.4 READ/WRITE C PCBA

The following paragraphs describe the Read/Write C PCBA installed in D3000 Series Disk Drives. Refer to Schematic No. 103750 and Assembly No. 103751.

The PCBA is approximately 247.7 mm (9.75 inches) long by 165.1 mm (6.5 inches) wide. Figure 5-5 illustrates the placement of each connector, test point, and adjustable component on the PCBA. J305 connects via a mating plug and 3M flat cable to the Logic PCBA. J304 is a molex connector which connects via a mating plug and standard cabling to the Logic PCBA. J300, J301, J302, and J303 connect via shielded cabling to the magnetic Read/Write heads.

The Read/Write PCBA description is divided into the following elements.

(1) Head Selection Matrix and Select Switches
(2) Write and Erase Driver
(3) Read Switch
(4) Read Preamplifier
(5) Filter
(6) Variable Gain Amplifier
(7) Peak Detector, Squarer, and Pulse Former
(8) Data Decoder
(9) Emergency Condition Detection

A block diagram of the Read/Write electronics is shown in Figure 4-4 and should be referred to in conjunction with Schematic No. 103750 and the electrical description described in the following paragraphs.

5.4.1 HEAD SELECTION MATRIX AND SELECT AMPLIFIER

Head selection is accomplished using a conventional diode matrix in conjunction with center-tapped heads. Each head is comprised of a balanced Read/Write (R/W) center-tapped winding and a separate erase winding which has one end connected to the R/W center tap. Referring to Schematic No. 103750, zone E14, 13, and 12, four heads are shown connected to J300, J301, J302, and J303. Three diodes are associated with each head: two diodes (CR28 and CR30 for the J300 head) connected to the balanced R/W bus and the third diode (CR29) is connected to the erase bus.

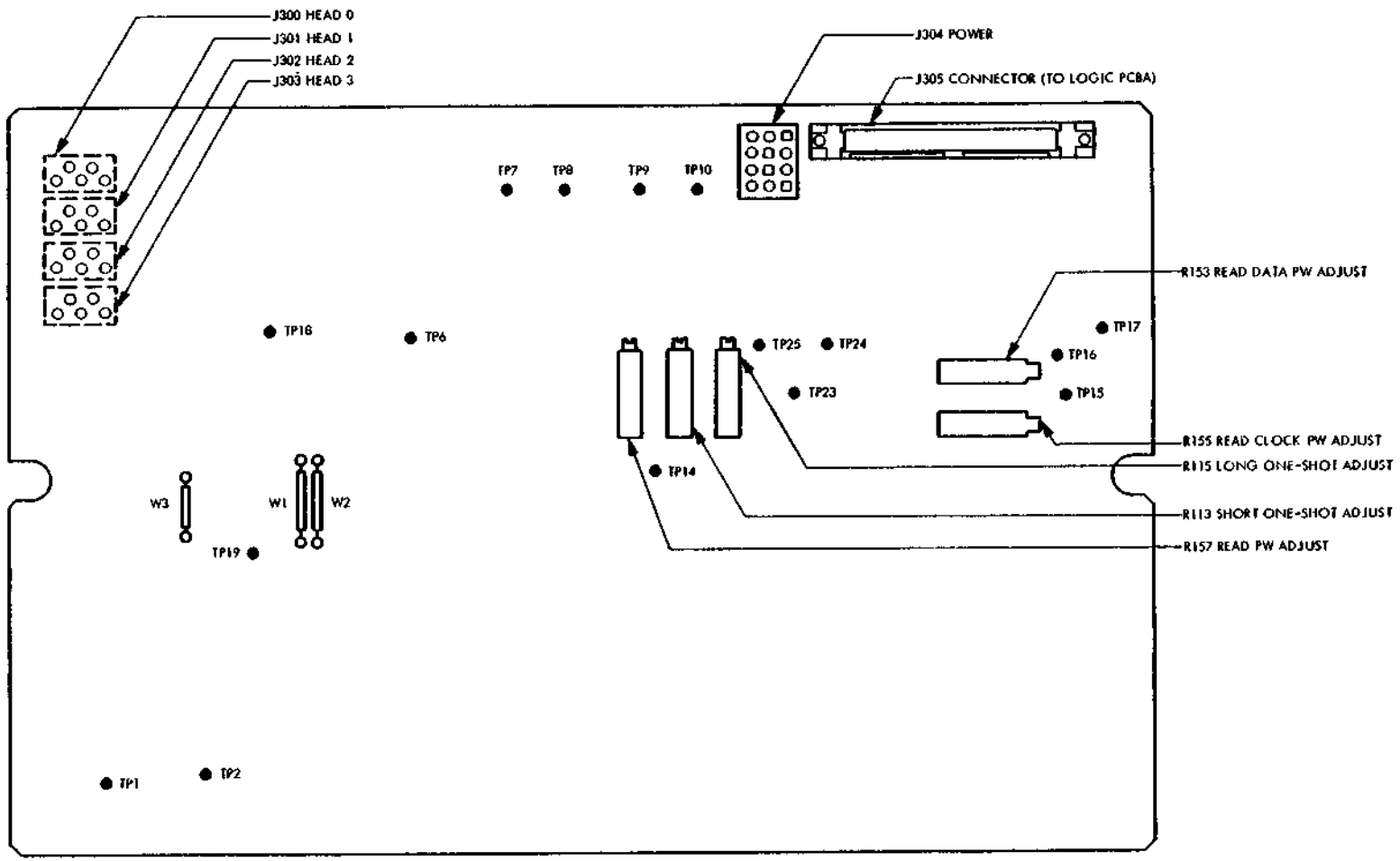

Figure 5-5. Read/Write C PCBA, Test Point and Connector Placement

The four head center taps are pulled to —10v by resistors R69, R72, R76, and R79 when the associated head is not selected. When selected, the appropriate head center tap is pulled positive by the corresponding head select switches (Q9, Q10, Q11, and Q12).

During a Write operation, +10v is applied to the emitters of the head select switches via Q1 when tracks 0 through 127 are selected. This voltage is decreased to approximately +7.0v via Q2 and resistor R5 when tracks 128 through 202 are selected. The appropriate selection is performed as follows: Write Mode (NLWMXG) and Erase Current Enable (NLECEG) signals are inverted by U13-A and U18-E, ORed by U15-D and fed to AND gates U15-A and U15-B. The Demand Address Most Significant Bit (128) signal (LDAMG) is fed directly to U15-A and inverted to U15-B. The outputs of U15-A and U15-B are fed via open-collector drivers U11-A and U11-B to Q1 and Q2. This system ensures that write current is appropriately reduced when writing on inner tracks where the flying height of the head is reduced.

During a Read operation, the head select switches are fed from approximately 0v via Q3. The NOT (Write Mode or Erase Enable) signal from U18-F is used to drive the open-collector driver U12-C which in turn is fed to the emitter of Q3.

5.4.2 WRITE AND ERASE DRIVERS

During a Write operation, the Write Mode (NLWMXG) signal is inverted and, when true, enables J-K flip-flop U9 (zone F17). Inverters U13-F and U13-E provide an extra delay which ensures that flip-flop U9 is always enabled in the reset state. Write Double Frequency pulses (NLWDFT) are received and fed to the clock input of U9. These clock pulses toggle the flip-flop for every pulse received as required by the double-frequency code used.

The Q and Q outputs of U9 are fed to two identical pre-drivers Q13 and Q15. The outputs of Q13 and Q15 drive the write drivers Q14 and Q16 whose emitters are returned to approximately —9v. When Q14 or Q16 conduct, write current flows in one half of the selected head. This current is defined by resistor R65 or R66 (as appropriate), the —10v supply, and the center tap voltage (+10v or +7v as required). This yields typical write currents of 35 ma peak for tracks 0 through 127 and 29 ma for tracks 128 through 202. The base drive circuits of all four transistors (Q13, Q15, and Q14, Q16) have anti-saturation diodes CR13, CR14, CR15, CR16, CR18, CR21, CR19, CR22 incorporated. Diodes CR26 and CR27 are used to isolate the head bus from the write circuitry during a Read operation, thus reducing noise injection. CR23 and CR24 prevent the inductive kickback of the magnetic head windings from exceeding +10v. Capacitors C8 and C9 are *speed up* capacitors which decrease write current rise time.

The erase driver is separately enabled by the Erase Current Enable (NLECEG) signal since the erase current can be left on for a longer time than the write current. When NLECEG is low, Q17 (zone D16) is turned on via inverters U18-E and U11-E. This causes the base of Q18 to be switched to approximately —4.3v which enables the current source components Q18 and R59. The erase current is typically 40 ma, independent of the status of Q1 and Q2.

The return path for both write and erase drivers is via the emitter base junction of Q19 through Q22, and then to —10v via the S10SS line which is returned to —10v through the emergency unload relay. Q22 is only enabled via Q21 and Q20 when the Power Clear Signal (SPCSA) is at a high (positive) level. Q19 is used as a write current detector and is detailed in Paragraph 5.4.9.

5.4.3 READ SWITCH

The diode switch CR46, CR51 (zone F10, 11), CR48 and CR52 (zone E10, 11) is used to isolate the head bus from the read amplifier during Write operations to prevent overload of the read preamplifier.

During a Write operation, Q8 (zone H14) is turned on via open-collector driver U12-D. This pulls the junction of R83 and R84 (zone E11) to +10v cutting off all four diodes. This follows since the head bus voltage cannot exceed +10v and the anode voltage of CR51 and CR52 cannot exceed +0.7v due to CR55 and CR56.

During a Read operation, Q8 is turned off and the junction of R83 and R86 is returned to approximately —6v via R85. Thus, approximately 1 ma flows through R83 (and R84) and approximately 0.5 ma is supplied by R88 (and R86). Thus, a current of 0.5 ma flows through each of the diodes CR46, CR51, CR48, and CR52 enabling the read switch.

5.4.4 READ PREAMPLIFIER

The balanced read signal from the head bus is terminated by R89 or L7, C11 and R90 or L8, C12 (zone E10) and fed to the type 733 differential video amplifier U1. When used in this configuration the amplifier has a wide bandwidth and a balanced-to-single-ended output gain of approximately 50 for 100 tpi or 150 for 200 tpi.

5.4.5 FILTER

The single-ended preamplifier output of video amplifier U1 is fed via matching resistor R100 to a linear phase filter. This filter has sharp cut-off characteristics combined with a group delay characteristic which is constant over the signal frequency band. The insertion loss of this filter is 0.5.

5.4.6 VARIABLE GAIN AMPLIFIER

The Variable Gain Amplifier consists of transistor amplifier Q27 (zone E8) employing emitter feedback to control its gain. It can be seen that the emitter resistance of this amplifier can be one of two values: 680 ohms (R106) when Q26 is not conducting, and 220 ohms (R106 in parallel with R104) when Q26 is conducting. Normally, Q26 is conducting and the gain of the stage is approximately

$$\frac{1800}{200} \simeq 8$$

However, when both margin test signals NLTOMG and NLTOPG are low, the output of U15-C goes high and Q26 ceases to conduct. Under these conditions the state again becomes approximately

$$\frac{1800}{680} \simeq 2.6$$

which gives a 3:1 reduction in gain. The appropriate dc base voltage (approximately 4.4v) for correct operation of Q27 is supplied via the voltage divider network R96, R101.

5.4.7 PEAK DETECTOR, SQUARER, AND PULSE FORMER

The signal from the variable gain amplifier stage is fed via emitter follower Q28 (zone E7) to the feedback differentiator stage U2 which utilizes a type 715 operational amplifier. C22 and R41 are the differentiator elements; R110 and C51 are used to limit the high frequency

response while diodes CR11 and CR12 provide clipping action which allows the stage to operate over a large dynamic range. C24 is used for stabilization and CR69 prevents latch-up.

For 100 tpi operation, the stage gain is designed to be approximately 9 at all-zeros frequency at 1500 rpm, and 18 at all-ones frequency at 1500 rpm. For higher speed versions of 100 tpi and for all 200 tpi operation, the gain is appropriately scaled. The system is designed so that the minimum all-ones frequency gain to the peak detector output is 1800 under normal conditions at 1500 rpm. Thus, for a head output of 0.5 mv peak-to-peak at the all-ones frequency, the peak detector output is approximately 1.2v peak-to-peak.

The output of the peak detector is fed to U30 which provides a pulse output for each zero crossing of the input signal. The width of the output pulse is proportional to R157, R156, and C74, R157 is employed to adjust the output pulse width to 40 to 45 nanoseconds.

5.4.8 DATA DECODER CIRCUITRY

The Data Decoder circuitry acts upon the pulse former output to generate separated data and clock signals. A functional discussion of this circuit is contained in Paragraph 4.6.3.7.

The RPN waveform consists of clock pulses which occur every 640 nanoseconds (1500 rpm and 2200 bpi) interspersed with a pulse for every one bit recovered.

The RPN waveform consists of clock pulses which occur every 640 nanoseconds (1500 rpm and 2200 bpi) interspersed with a pulse for every one bit recovered.

RPN is gated through U27-C and its leading edge is used to clock the appropriate one-shot to set the ones window. If the preceding clock period had a one interspersed, then the short one-shot (U7-B) is used to form the ones window via U27-B. If the preceding clock period did not contain a one, then the long one-shot (U7-A) is used to form the ones window via U27-B. U28-B inverts the ones window to form the zeros or clock window. This signal is applied to U27-C and gates RPN through R113 and R115. This is used to set the period for the short and long one-shots.

If a RPN (data) occurs during the time that the ones window is high, it will be gated through U27-A. This pulse sets U8-A which results in the short one-shot determining the next one-shot period.

The output of U27-A and U27-C are fed back to the inputs of U27-B and U28-B, respectively, and act as pulse stretchers. The outputs are also applied to U29-A and U29-B where the decoding pulse is lengthened prior to sending down interface lines. The output of U29-A is lengthened by R153 but is also proportional to R152 and C76. The output of U29-B is lengthened by R155 but is also proportional to R154 and C77.

5.4.9 EMERGENCY CONDITION DETECTION

Two conditions are detected by the Emergency Condition Detector circuitry and cause the Write Emergency Condition (RWECG) signal to go high. The NRWECG signal is fed to the Logic PCBA via J305 pin 30 (zone C6) where it is used to initiate an emergency unload sequence. The emergency unload sequence causes the unit to go Not Ready, thereby turning off write current in less than 1 µsec. The emergency unload sequence also causes the emergency unload relay to operate, thereby interrupting the S10SS supply. Interruption of this supply precludes any write current flowing in the heads.

One emergency condition detected is the condition when more than one head is selected while the disk drive is in a Write mode of operation. When a head is selected in the write

condition (e.g., the head connected to J300) the appropriate center tap is pulled to approximately 10v for tracks 0 through 127 and 7v for tracks 128 through 202 (Paragraph 5.4.1).

This voltage is clipped by CR31 (zone E14) to +0.7v and fed via R71 and diode CR32 to the inverting input of the type 741 operational amplifier U4 (zone D11) which is used as a comparator. A precision current drain for this circuit is established via R75 to —10v.

The non-inverting input of U4 is set at a nominal voltage of —4.5v such that when one head is selected the inverting input is more negative than —4.5v and the output of U4 is high. When two heads are selected (e.g., the heads connected to J300 and J301) additional current is fed via R74 and CR37 to the inverting input of U4 raising this point above —4.5v and causing the output of U4 to switch to a negative state. This output is fed via R134 and CR53 to one input of the low active OR gate U26-A (zone B15) causing RWECG to go high at J305 pin 30 (zone C6). R138 and CR58 prevent the input to U26-A from going more negative than —0.7v.

The second emergency condition detected by this circuitry is when write current is on during a Read operation. It is important to note that during a Read operation no write current or erase current should flow.

Write and erase current must flow through R63 (zone D15) and the emitter base diode of Q19. If a total current in excess of approximately 0.7 ma flows, then the voltage across R63 (1K ohm) will exceed 0.7v causing Q19 to turn on. Q19 conducting causes the input to inverter U26-C (zone A15) to go low which, in turn, enables one input of NAND gate U26-B.

Recall that during a Read Mode, the Write Mode (NLWMXG) and Erase Current Enable (NLECEG) signals are high, thus the output of U22-C (zone B17) is low.

In the Read Mode the outputs of inverter U22-C and non-inverting driver U25 are both high, enabling the other two inputs of NAND gate U26-B. Thus, the output of OR gate U26-A goes high and the RWECG waveform goes high at J305 pin 30 (zone C6). Resistor R143 and capacitor C63 are used to provide masking delays to avoid false indications during Read/Write switching.

During a Write operation, transistor Q19 is on but one or both of the NLECEG and NLWMXG waveforms are low. Therefore, the output of UJ22-C is high, inhibiting gate U26-B and hence preventing RWECG from going high.

5.5 LOGIC PCBA

The following paragraphs describe the Logic PCBA installed in D3000 Series Disk Drives. Refer to Schematic No. 102830 and Assembly No. 102831.

The Logic PCBA is approximately 393.7 mm (15.5 inches) long by 273.1 mm (10.75 inches) wide. Figure 5-6 illustrates the placement of each connector, test point, and adjustable component on this PCBA. J104 and J105 connect via 3M flat cable to the Servo PCBA; J108, J109, J110, J111, and J112 are molex connectors which are also connected to the Servo PCBA. J103 mates to the Read/Write PCBA via 3M flat cable. J101 provides connection between the D3000 and a controller or another disk drive. J102 provides connection to the PERTEC I/O Terminator PCBA or another disk drive. J114 (200 tpi models only) transmits the three most significant bits from the current address counter to the Temperature Compensation PCBA.

The PCBA description is addressed to Schematic No. 102830 on a sheet-by-sheet basis beginning with sheet 2.

5.5.1 SHEET 2 (SCHEMATIC NO. 102830)

Sheet 2 of the Logic PCBA schematic contains the Start/Stop Control logic portion of the disk drive function control logic. Refer to the functional description and simplified block diagram contained in Paragraph 4.7 in conjunction with this discussion.

The crystal oscillator is comprised of transistor amplifiers Q1 and Q2 (zone C14) in conjunction with the 10 MHz crystal Y1. The crystal is connected in the feedback path of the oscillator and is operated in a series resonant mode. The output signal of the oscillator is developed across R13 and is fed through inverter U186 (which acts as a buffer) to the clock countdown circuitry. The output of the oscillator can be monitored at TP13. The clock countdown circuitry consists of cascaded 4-bit binary counters operating in a binary countdown mode. The first counter of the countdown chain is a synchronous counter, the remainder are ripple counters. The clock signals derived from the clock countdown chain are square-waves which are fed to various parts of the logic to provide the primary timing. One of the clock signals is used in the spindle speed control logic to determine the speed of the disk and functions as the primary time reference for the spindle speed control. Another of the clock signals, LC09F (U245 zone B10) is gated by the Sequence Timing Pulse Flip-Flop (U345 zone F5) output pulse at AND gate U284-13 (zone D9) to produce the gated clock to the Purge Cycle Flip-Flop (U344 zone G12) and the Load Heads Flip-Flop (U344 zone G10). The frequency and the period of each one of the clock signals is listed in Table 5-1. Referring to Table 5-1, it can be seen that each successive clock signal is one-half the frequency and twice the period of the previous signal in the clock countdown.

NOTE

Generated clock signals are listed in Table 5-1 to aid in troubleshooting; all of these signals are not used in the D3000.

The major states of the Start/Stop Control Logic are defined by the Run Flip-Flop (U364 zone H14), the End Of Run Flip-Flop (U364 zone H13), the Purge Cycle Flip-Flop (U344 zone H12), the Load Heads Flip-Flop (U344 zone H10), the Sequence Control Flip-Flop (U384 zone H9), the Brake Cycle Enable Flip-Flop (U384 zone H7), the Emergency Unload Flip-Flop (U345 zone E13), and the Disk Rotation Detector Counter (U283 zone D14).

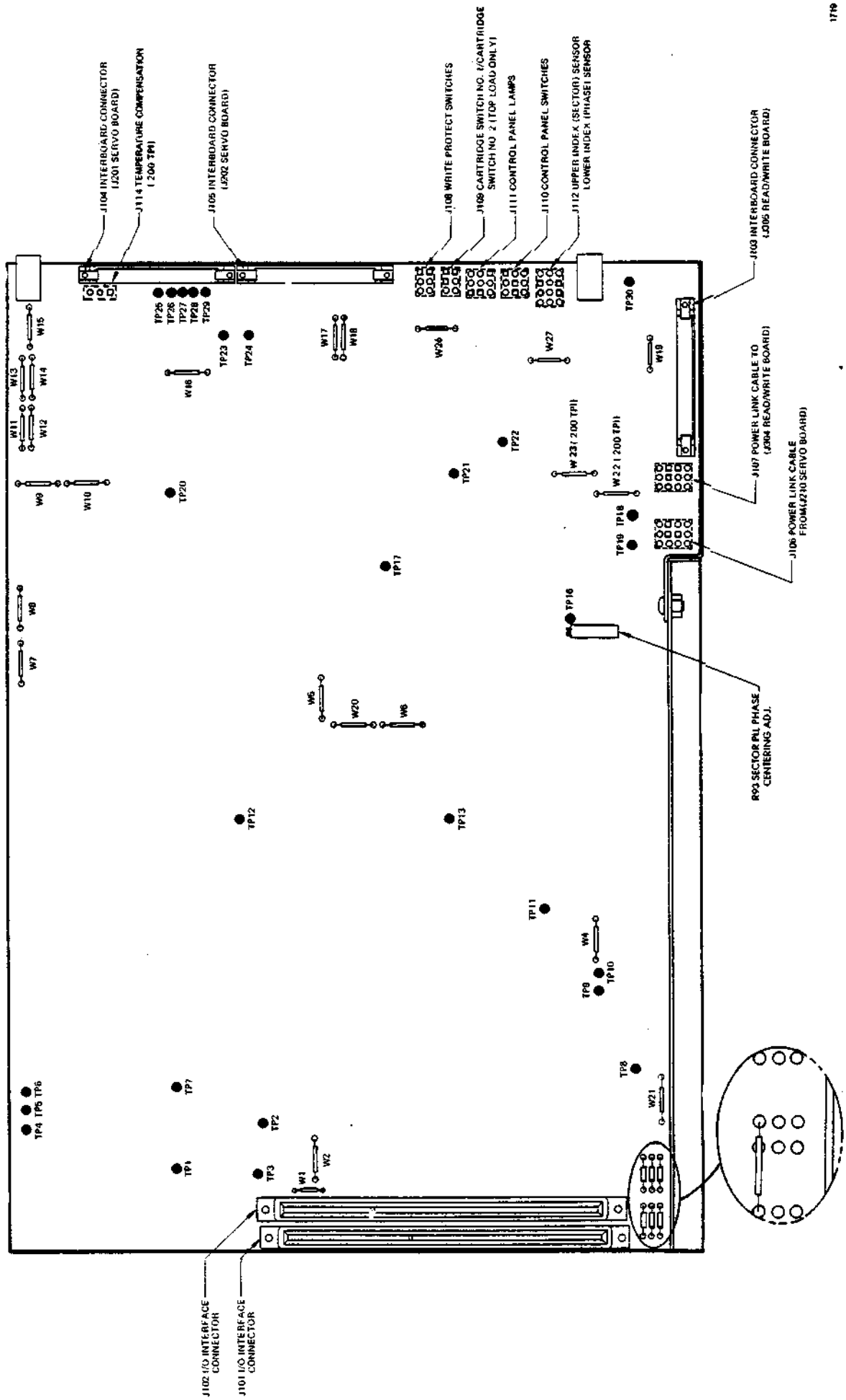

Figure 5-6. Logic PCBA, Test Point and Connector Placement

Table 5-1
Clock Countdown

Clock No.	Frequency (in Hz)	Period
01	5000000.0	200 nsec
02	2500000.0	400 nsec
03	1250000.0	800 nsec
04	625000.0	1.6 μsec
05	312500.0	3.2 μsec
06	156250.0	6.4 μsec
07	78125.0	12.8 μsec
08	39062.5	25.6 μsec
09	19531.25	51.2 μsec
10	9765.625	102.4 μsec
11	4882.8125	204.8 μsec
12	2441.40625	409.6 μsec
13	1220.703125	819.2 μsec
14	610.3515625	1.6384 msec
15	305.17578125	3.2768 msec
16	152.5878906250	6.5536 msec
17	76.2939453125	13.1072 msec
18	38.14697265625	26.2144 msec
19	19.073486328125	52.4288 msec
20	9.5367431640625	104.8576 msec

A delay counter is mechanized by taking the last of the Clock Countdown LC20F (pin 11, U285 zone B7) and applying it to the input of two 4-bit binary counters (U305, U325 zone C8). The Delay Counter, in conjunction with the Sequence Timing Pulse Flip-Flop (U345 zone F5), and the appropriate combinational logic generate timing sequence pulses at specific time intervals according to the states of the logic. The counter is controlled by resetting the counter with either a pulse or a level change via OR gate U326-6 (zone F6). This gate combines the Sequence Timing Pulse (LSTPF) with the output of combinational logic U385-3 (NLNRSG) and U385-8 (NLSNHG) and applies this gated signal to the Delay Counter.

NOTE

External commands, either directly or in conjunction with the combination of the external commands and the present states, may affect the next state of the start/stop control logic. Refer to the block diagram of the digital sequential machine [Figure 4-9] used to mechanize Start/ Stop Control Logic.

The logic is initialized during power ON and power OFF events by the Power Clear Signal (SPCSA) from the Servo PCBA at J105 pin 31 (zone E17). SPCSA is an analog signal which is converted into logic levels by Schmitt trigger U405 (zone E16). It should be noted that when the output of U405, pin 8, is high, power to the machine is either off or below the minimum acceptable value as determined by the Power Clear circuit on the Servo PCBA.

SPCSA clears the Disk Rotation Detector Counter, pre-sets the Emergency Unload Flip-Flop, clears the End Of Run Flip-Flop, clears the Run/Stop Pulse Register, the Run Flip-Flop, and the Sequence Timing Pulse Flip-Flop. The Power Clear Signal (SPCSA) assures that the logic is properly initialized during power turn-on and that the logic assumes the correct states in the event of power removal.

Commands which can cause the Start/Stop Control to execute either a start sequence or a stop sequence are obtained from the RUN/STOP control signal (CRSSS) connected to J110, pins 1, 2, and 3 (zone H18). A cross-coupled inverter latch U447 is used to *clean up* the input signal and eliminate the problem of switch contact bounce. The output of this latch is ORed with the Start/Stop Disk Drive (ISSDR) line from the I/O interface at U49. The output of U49, pin 3, is the input to the Run/Stop Pulse Register (U347 zone G17). A level change occurring either from an assertion of the Start/Stop Disk Drive line or from actuation of the RUN/STOP control is edge-detected by the Run/Stop Pulse Register. The Run/Stop Pulse Register is a shift-register type of edge detector whose purpose is to produce a pulse having a period of one clock time upon detection of the leading edge of a level change propagating through the register.

The one-clock period pulse output from U347 is the Run Switch Pulse (LRSPG) used for clocking the Run Flip-Flop (U364 zone H14). In addition, the Run/Stop Pulse Register generates the Start Drive Motor (NLSDMG) signal if, and only if, the Run Flip-Flop is one-set as a result of the level change propagating through the Run/Stop Pulse Register. This will be the case when the Run Flip-Flop has been properly enabled and is one-set to commence a start sequence. The Start Drive Motor pulse initializes flip-flops in the Spindle Speed Control logic on sheet 3 of the schematic.

The Delay Counter Decode logic (zone E7) is enabled by the outputs of the Sequence Control Logic as well as the Sequence Control Flip-Flop. Delay Counter Decode decodes specific values of delay by ANDing various bits from the Delay Counter according to the states presented by the Sequence Control Logic and the Sequence Control Flip-Flop.

The Sequence Timing Pulse Flip-Flop (U345 zone E5) is used to generate a pulse with a period of one clock interval when a high level is applied to the J input from the Delay Counter Decode logic.

The sequence timing pulse is used to define the timing of events during the start sequence and the stop sequence. It also tests the states of certain signals during the start sequence for the purposes of determining if an emergency condition exists.

The timing of two of the flip-flops is accomplished by using the sequence timing pulse to gate the clock to the Load Heads Flip-Flop and the Purge Cycle Flip-Flop. This is done to ensure clocking these flip-flops only at the end of specific delay intervals.

The Disk Rotation Detector Counter is used to detect disk rotation for purposes of interlocking and to determine the duration of the brake cycle. Additionally, the Disk Rotation Detector Counter provides a time delay at the end of the power clear condition.

The Sequence Control Logic (zone E12) is employed to decode the states of the Purge Cycle Flip-Flop and the Load Heads Flip-Flop. This provides signals for steering the start sequence and for initializing the position monitor circuit in the Position Control Logic.

The signal outputs from the Sequence Control Logic are also used to enable the tests in the Emergency Unload Logic.

The Run Flip-Flop will be zero-set by any Run Switch Pulse (LRSPG) if it is already one-set. If the Run Flip-Flop is previously zero-set, then LRSPG will one-set the flip-flop only if proper interlocking has occurred. Detection that the disk cartridge is correctly inserted interlocks the Run Flip-Flop. Gate U264-12 (zone F15) ORs the Cartridge Correctly Inserted (LCCIG) signal with the Clear Or Unload (NLCOUG) signal to clear the Run Flip-Flop if either or both of these signals are low.

Cartridge Correctly Inserted (LCCIG) signal is developed from the states of the cartridge inserted switches. The Clear Or Unload (NLCOUG) signal is the OR condition of the Power Clear Signal (SPCSA) and the output of the Emergency Unload Logic.

Determination of correct cartridge insertion is accomplished by two switches in top load models and by a single switch in front load models. These switches connect to J109 (zone F18) and operate the Cartridge Inserted Latches. The output of the Cartridge Inserted Latches is ANDed by U445-4 (zone F17) to generate the LCCIG signal. The cartridge inserted latches are cross-coupled inverters in the same configuration as those used at the input to the Run/Stop Pulse Register. In front load models, where only one switch is used, one of the latches is held permanently in the correct state by a jumper at P109.

The Run condition is defined as any time that the disk is rotating and a stop sequence is not in progress, i.e., Run Flip-Flop one-set. The Run Flip-Flop cannot be one-set by a Run Switch Pulse signal unless the J input to the flip-flop is at a logic one level. The signal which enables the Run Flip-Flop J input is NLLCMG which is the result of combinational logic containing the remaining interlocking signals. These interlocking signals are: Heads Retracted (SHRXG) which prevents entering a run condition unless the heads are retracted; Not Disk Rotating (NLDRXG), from the Disk Rotation Detector Counter, which prevents entering a run condition unless the disk is stationary; Not Brake Cycle (NLBCFF), from the Brake Cycle Flip-Flop, which prevents entering a run condition if a brake cycle is in progress; and, finally, the logic condition resulting from the combination of the state of the Sequence Control Flip-Flop (LSCFF) and the Run Flip-Flop (LRFFF) which is combined in U385-3 (zone E6) to generate NLNRSG. This signal is used in the interlocking control portion of the logic. The use of this arrangement prevents re-entry into a run condition (Run Flip-Flop one-set) unless a correct stop sequence has been executed.

As previously mentioned, there are two basic sequences executed by the Start/Stop Control Logic; the start sequence, and the stop sequence.

A start sequence begins when the Run Flip-Flop is one-set and progresses through the one-setting of the Purge Cycle Flip-Flop (U344 zone G12), the one-setting of the Load Heads Flip-Flop (U344 zone G10), and finally, the one-setting of the Sequence Control Flip-Flop (U384 zone G9). One-setting the Run Flip-Flop defines the run condition. The Purge Cycle Flip-Flop then defines that portion of the start sequence when the disk speed is increased to 10 percent above the nominal speed. This is done to increase the air flow across the platter(s) prior to loading the heads. The Load Heads Flip-Flop is used to define that state when the heads are loaded onto the disk(s). The Sequence Control Flip-Flop defines the state which indicates the successful completion of a start sequence, or the beginning of a stop sequence.

A stop sequence begins with zero-setting the Run Flip-Flop. This causes one-setting the End Of Run Flip-Flop which, in turn, causes the Sequence Control Flip-Flop to be pre-set in the event that it has not yet been one-set. To complete the stop sequence, the Brake Cycle Enable Flip-Flop is one-set at the same time that the Sequence Control Flip-Flop is zero-set. The stop sequence ends with zero-setting the Brake Cycle Enable Flip-Flop. The End Of Run Flip-Flop is used to detect the high-to-low transition of the Run Flip-Flop when the Run Flip-Flop is zero-set. The End Of Run Flip-Flop, therefore, acts as an edge detector which is used to force a pre-set condition to the Sequence Control Flip-Flop. This guarantees correct entry into the stop sequence. The Brake Cycle Enable Flip-Flop is then one-set to define that portion of time when braking current is supplied to the disk motor to stop the disk.

The Emergency Unload Flip-Flop (U345 zone E13) defines the condition which causes the emergency unload relay to disconnect the positioner servo from the positioner coil and connect the positioner coil to the emergency unload network. This is done when executing an emergency unload, or for preventing the connection of the positioner coil to the servo electronics, prior to the time when the disk drive logic is capable of detecting certain positioner electronic faults.

The Emergency Unload Logic is comprised of three basic parts: U266 (zone D16) which ANDs the Sequence Timing Pulse Flip-Flop with outputs from the Sequence Control Logic and the specific signals to be tested for emergency condition indications during a start sequence. The signals tested by U266 logic are NLBPSL, NLPMXG, and LSOTF. The ANDing of these signals generates, respectively, Brush Parking Error (NLBPEG), Head Loading Error (NLHLEG), and Disk Starting Fault (NLDSFG).

Position Transducer Failure (SPTFG) from the Servo PCBA is ORed with Write Emergency Condition (RWECG) from the Read/Write PCBA at gate U327 (zone C17) to produce NLEOFG which is Emergency Or Failure condition.

The Activate Emergency Unload (IAEUR) line from the I/O interface is processed by a minimum pulse width detector consisting of U147-8, R10 and C1 in conjunction with U286-6 (zone B16) to produce Emergency Unload Command (NLEUCG).

These signals plus Position Limit Error (NLPLEG), Disk Speed Error (NLDSEG), and Seek Time Error (NLSTEG) from other portions of the logic are combined in OR gate U306 (zone C15) to produce Any Emergency (LAEXG). Assertion of LAEXG by one or more of the emergency situations detected by the Emergency Unload Logic results in clearing the Run Flip-Flop and aborting the run condition. This pre-sets the Emergency Unload Flip-Flop (U-345 zone E13) causing emergency retraction of the heads.

Lamp drivers U407-5, U386-5, and U407-3 (zone E4) provide drive to the front panel indicator lamps for the SAFE, RUN, and READY lamps, respectively.

The Ready Logic (zone E4) combines the outputs of the Sequence Control Flip-Flop and the Load Heads Flip-Flop with the Q output of the Emergency Unload Flip-Flop to produce the Ready signal at the output of U365 (zone E5). The Ready signal is combined with the Selected signal at U385 (zone F4) to obtain the Selected And Ready condition for purposes of gating the line receivers and drivers for the I/O interface.

The Selected And Ready (LSARG) signal is processed by the trailing edge delay circuit consisting of U444-6, R16, C4 (zone C4) in conjunction with Schmitt trigger U405-6 to produce the Delayed Ready Condition (LDRCG). The Delayed Ready Condition signal is utilized in other parts of the logic for generating Malfunction Detected (IMDXD) which is an I/O interface signal.

5.5.2 SHEET 3 (SCHEMATIC NO. 102830)

Sheet 3 of the Logic PCBA schematic contains the remainder of the Disk Drive Function Control Logic, i.e., all of the Disk Drive Function Control Logic which is not part of the Start/Stop Control Logic. The Start/Stop Control Logic description is contained in Paragraph 5.5.1. Refer to the functional description and simplified block diagram contained in Paragraph 4.7 in conjunction with the following discussion.

Four of the I/O interface lines that control disk drive functions are routed directly to the Holding Register (U308 zone H21) on the Logic PCBA. These lines are: Head Select (IHSXR), Platter Select (IPSXR), Track Offset Plus (ITOPR), and Track Offset Minus (ITOMR). Note that Selected And Ready (NLSARG) is brought to the holding register load-input. When NLSARG is low, the states on these I/O interface lines will be copied into the register. Thus, the state in the register will correspond to the state at the I/O interface line and will change accordingly for any changes on the I/O interface line.

When the disk drive is de-selected, NLSARG will go high causing the holding register to trap the last value of the inputs from the I/O interface. The register will then hold that state until the next time the disk drive is selected. Note that Ready (NLRXXG) is used as the clear input to the Holding Register U308. When high, NLRXXG causes the register to be cleared to the all-zero's condition on each of its outputs. This condition will occur at any time the machine is in the Not-Ready condition. In other words, the pre-determined states of logic zero on each of the output lines from the Holding Register, determine specific states for the Upper Head Select (NLUSHG), Upper Platter Select (NLUPSG), Track Offset Plus (NLTOPG), and Track Offset Minus (NLTOMG) lines on the Logic PCBA.

Upper Head Select (NLUHSG) is routed directly to the Read/Write PCBA, and the Temperature Compensation PCBA, for head selection according to the state in the Holding Register. Upper-Platter Select (LUPSG), and its complement (NLUPSG), are connected to various circuits on the Logic PCBA. These circuits are: the Write Protect Logic for determining which Protect switches will be sampled, and the Multiplexer Control Logic for determining which platter information will be multiplexed to the I/O interface output lines. In addition, NLUPSG is routed to the Read/Write PCBA for selecting a specific storage surface, and to the Temperature Compensation PCBA, to enable the Head Compensation Select circuitry.

NAND gates U328 (zone G19) combine the Track Offset signals from the Holding Register with NLBTFF from the Position Control Logic. The results are that the Track Offset signals will not be asserted to the Read/Write PCBA and the Servo PCBA during the time that the positioner is busy. The outputs of these NAND gates are connected to the Servo PCBA and the Read/Write PCBA via pins 22 and 23 of J103 and pins 26 and 25 of J104.

NOTE

These signals control change of gain in the read amplifier on the Read/Write PCBA when both signals are asserted. The signals are also fed to the Servo PCBA and are used to assume operation of the Track Offset circuitry.

The Write Double Frequency Data Retransmitter (U70 zone F21) functions as a line receiver and as a line driver. The Write Data Signal (IWDSR) from the I/O interface is received by U70 acting as a line receiver. IWDSR is the double frequency encoded write data from the I/O interface which must be transmitted to the Read/Write PCBA. Transmission of the write data signal is also accomplished by U70. Acting as a line driver, it drives the NLWDFT signal to the Read/Write PCBA through J103 pin 27. Thus, the Write data signal is retransmitted to the Read/Write PCBA where it is used by the Read/Write electronics.

The Unit Select Logic and the Busy Output Logic are shown in zone 17 through 21. The Unit Select Logic is the decoding arrangement and the Busy Output Logic is an encoding arrangement. Four separate Unit Select lines (IUS1R, IUS2R, IUS3R, and IUS4R) are provided at the I/O interface and are presented to the circuit via J102. This allows selection of one of four disk drives on the common I/O bus. Internally, it is necessary for the drive to provide a signal which indicates that it is being selected by the I/O interface.

Since there are four separate and distinct select lines presented to the disk drive, they must be decoded. The Unit Select lines are brought through J101, J102, and are decoded according to the state of the Unit Number Selector Switch, which connects to J110, pins 5, 8, 9, 6, and 7, by U89 and U328-11 to produce the Select Signal (LSXXG). When the Unit Number Select Switch on the front panel is set to one of the position numbers (one through four), one and only one of the signals at U448-4, U448-10, U448-8, and U448-6 will be high. This will result in the Select Signal (LSXXG) being generated only when there is an assertion on the specific Unit Select line that corresponds with the number as designated by the Unit Number Selector Switch on the operator's panel.

The busy output logic utilizes the same signals developed from the Unit Number Selector switch to gate the Busy Signal from the Position Control Logic onto the specific busy seeking line that corresponds to the particular setting of the Unit Number Selector switch. This is accomplished by U86-6, U86-5, U86-8, and U86-11 (zone B, C-19). The common inputs to these NAND gates are enabled by the AND condition of the Busy Signal (from the Position Control Logic) and the Ready signal. When the disk drive is Ready, NLRXXG will be low, enabling U263-4 (zone B19) to provide a high output level whenever the Busy Signal (NLBSXG) is low. This condition causes the Busy Signal to be transmitted on that line selected by the setting of the Unit Number Selector switch. U68 and U69 (zone B, C-18) are line drivers for driving the Busy Seeking Signals onto the respective I/O lines.

The Read/Write Control Logic controls the Write, Erase and Read signals to the Read/Write PCBA. These signals depend upon the conditions of the input interface lines and certain signals generated on the Logic PCBA. Additionally, the Read/Write Control Logic generates NLWOEG which is supplied to the Write Protect Logic and the Start/Stop Control Logic.

The Write Enable (IWEXR) signal and the Erase Enable (IEEXR) signal are received and gated with Selected And Ready (NLSARG) by U48-1 and U48-4 (zone G16). These gates provide outputs only if the disk drive is selected and ready. The outputs of U48-1 and U48-4 are then gated by the AND condition of Position Mode (NLPMXG) and File Protect Mode (LFPML). These signals are then routed to the Read/Write PCBA (via J103) as Write Mode NLWMXG) and Erase Current Enable (NLECEG) by two NAND gates, U87-3 and U87-4. The Write Mode and Erase Current Enable signals to the Read/Write PCBA will be asserted if, and only if, the respective signal is received from the I/O interface, the disk drive is selected and ready, the drive is not in a file-protect mode, and the positioner is in the position mode.

If either Write Enable, Erase Enable, or both is present, the low active Write Or Erase signal (NLWOEG) will be generated at the output of U48 (zone G16). This signal is used in the Start/Stop Control Logic to prevent clearing of the Load Heads Flip-Flop when either a Write or an Erase operation is in progress. The signal is also used in the Write Protect Logic to allow changing the state of the file protect mode latch only when a Write and/or Erase operation is not in progress. The Read Enable signal (IREXR) from the I/O interface is gated only by Selected And Ready (LSARG) at NAND gate U87-8 (zone F16) before being supplied to the Read/Write PCBA at J103.

The Write Protect Logic performs several functions on the Logic PCBA; one of these is to provide front panel indication via the Protect Lamp indicators as to the state of the Protect Switches. The Write Protect switches connect to J108 and their states are sampled by the Protect Switch Latches (U446 zone D16) and the Protect Lamp Drivers (U424 zone C13). Drive is provided to the front panel Protect Lamp indicators according to the states of the respective Protect Switch Latches. There is one switch latch for each platter. For single-disk machines with only one Write Protect switch the other switch input at J108 is permanently wired by a jumper in P108 to disable the lower platter latch. Likewise, for those machines not fitted with Write Protect switches, jumpers in P108 will permanently disable both Write Protect Switch Latches. The state of the Protect Switch Latches is decoded according to the specific platter selected by the interface. This is accomplished by U406-6 (zone D14). LUPSG and NLUPSG are inputs to this AND/OR invert gate and determine the specific Protect Switch Latch which is sampled and fed to the File Protect Mode Latch U88 (zone D13).

The state of the respective Protect Switch Latch is fed to the File Protect Mode Latch if, and only if, a Write or an Erase operation is not in progress. This is the result of NAND gates U88-11 and U88-3 (zone D13). The purpose of this is to provide a signal that indicates the specific platter that is protected from Write and/or Erase operations. The state of the File Protect Mode Latch is driven onto the File Protected (IFPXD) I/O interface line by the File Protected Status driver (U44 zone D12) according to the state of a File Protect Mode Latch.

Also included on sheet 3 of the Logic PCBA schematic are line drivers for several of the interface output lines. The Read Signal Drivers (U67 zone H12) take the Read Clock Signal (NRRCSG) and the Read Data Signal (NRRDSG) from the Read/Write PCBA via J103 and drive these signals onto the interface lines Read Clock (IRCXD) and Read Data (IRDXD) via J102.

The Malfunction Signal Driver (U64 zone G12), and associated gate U282 provide an indication when an internal malfunction is detected. The Malfunction Detected (IMDXD) line is pulsed when an internal malfunction is detected. This is accomplished by NANDing the Delayed-Ready Condition (LDRCG) with the Emergency Unload Flip-Flop (LEUFF) at NAND gate U282-8 and driving the resulting signal onto the Malfunction Detected (IMDXD) line at J102.

Assuming that the disk drive is in the Ready condition as evidenced by the high level of LDRCG at pin 9 of U282, any emergency will cause the Emergency Unload Flip-Flop to one-set. One-setting the Emergency Unload Flip-Flop causes the other input to U282 to go high. The high level at pin 9 will persist for a short period of time even though the disk drive will go Not-Ready as soon as the Emergency Unload Flip-Flop is one-set. This is true since the transition from Ready to Not-Ready will take a short period of time to propagate through the Delayed Ready Condition circuit. Therefore, for that length of time, both inputs of U282 will remain at the high logic level.

As soon as the Ready to Not-Ready transition has propagated through the Delayed Ready Condition circuit, pin 9 of U282 will go low. This will terminate the Malfunction Detected pulse that is applied to the interface output by line driver U64-5.

Double Track Drive (IDTDD) is indicated on certain models by driving the Selected (NLSXXG) signal onto this interface line. Illegal Cylinder Address (IICAD) is indicated at the interface by driving that line with the Illegal Address (NLIAXG) signal via U3 (zone E12). NLIAXG is generated in the Position Control Logic.

A dual platter drive is indicated at the interface by driving the Dual Platter Drive line with the Dual Platter Signal via U45 (zone C12). Dual Platter Signal (NLDPSG) is made up in the Sectoring Electronics (sheet 5 of the Logic PCBA schematic) from either a steady logic

one signal or the low active Selected signal (NLSXXG) depending on whether the machine is a single platter or a dual platter drive, respectively. This selection is accomplished by the sectoring selection programming array that is plugged into J125.

The Termination Voltage Power Supply is shown in zone B11 of the schematic. This is a nominal 3.5v source which is provided to the interface for those models requiring compatibility with D5000 termination voltage. This supply is derived by using diodes CR1 and CR2 in conjunction with R25 to provide a voltage drop from the internal +5v supply for supplying termination voltage to connector J102. Likewise, CR3 and CR4, in conjunction with R26, provides a reduced voltage from the +5v supply at J101. For those versions of the Logic PCBA that do not use the Termination Voltage Power Supply, pins A45 and B45 on J102, are wired to like pins on J101 by jumper W3. This provides feed-through of the termination voltage when this voltage is supplied by the controller. In that case, CR1, CR2, R25, CR3, CR4, and R26 are omitted.

The Special Signal Driver (U65 zone C12) is a line-driver reserved for driving special interface signals in those machines having that option (see Paragraph 3.17.13).

The Chassis Ground Connection is shown in zone B8 of the schematic. For disk drives having ordinary grounding, W21 connects the I/O ground directly to the chassis. For machines requiring ground isolation, W21 is omitted and the I/O ground is connected to the chassis ground through a complex impedence consisting of R72 and C78.

The remainder of sheet 3 of the schematic pertains to the speed control electronics. The purpose of this circuitry is to compare the time of occurrence of the positive transition of the LPLFF flip-flop square-wave with the time reference obtained from the crystal oscillator countdown (refer to Paragraph 5.5.1). The result of the comparison is two signals, one indicating the instantaneous speed error (NLIMSI) and, if appropriate, another signal which will indicate a gross malfunction of the speed control (LSOTF).

When the Drive-Motor Enable (LDMEG) signal is high and the drive motor is enabled to operate, the Speed Sequence Register U244 (zone C8), the Increase Motor Speed Flip-Flop (U243 zone G4) and the speed out-of-tolerance Flip-Flop (U243 zone F3) are released to operate. The Speed Sequence Register, in conjunction with gates U224-10, U263-1, U223-3, and U224-8 function as an edge detector. They also establish the sequencing of the events in determining the disk speed. For each low to high transition of the Phase Lock Flip-Flop signal (LPLFF) a one-clock-time pulse, Transfer Speed Count (LTSCG), is generated. One-clock-time thereafter Speed Count Reset (NLSCRG) is generated to reset the speed counting logic. The clock frequency utilized by the Speed Sequence Register is the same clock frequency counted by the Speed Control Counter and is determined by the particular programming array plugged into J121 (zone F10), the Speed Control Programming array. This selects one of three possible clock signals from the clock countdown.

At the time the Transfer Speed Count (LTSCG) pulse is generated, the states held in the Speed High Limit Flip-Flop (U142 zone H5), the Disk Speed Low Flip-Flop (U242) and Speed Low Limit Flip-Flop (U242) is transferred into the Increase Motor Speed Flip-Flop (U243 zone F3) and the Speed Out Of Tolerance Flip-Flop (U243 zone F3). Specifically, the state of the Disk Speed Low Flip-Flop is transferred to the Increase Motor Speed Flip-Flop. Either a one-set condition of the Speed High Limit Flip-Flop, or a one-set condition of the Low Limit Flip-Flop is transferred to the Speed Out Of Tolerance Flip-Flop if either of those flip-flops were one-set. This would be the case only if a gross speed error is being detected.

The Speed High Limit Flip-Flop, the Disk Speed Low Limit Flip-Flop, and the Speed Low Limit Flip-Flop are referred to as the speed value flip-flops. The specific values stored in these flip-flops is the result of the previous speed count. After the values stored in the speed value flip-flops are transferred to the speed status flip-flops (consisting of Increase Motor Speed Flip-Flop and the Speed Out Of Tolerance Flip-Flop) by the Transfer Speed Count (LTSCG) pulse, then, one-clock time later the speed control logic is reset by NLSCRG which is a one-clock period low active pulse. This resets the Disk Speed Low Flip-Flop, the Speed Low Limit Flip-Flop, and pre-sets the Speed High Limit Flip-Flop to establish the initial conditions at the speed value flip-flops for the next count. Also, the Speed Control Counter is loaded with a pre-determined number from the Disk Speed Count Programming array plug-in J122. This determines the disk speed count programming according to the state of the Purge Cycle Flip-Flop.

The speed control counter, U202, U221, and U241 (zone F6, 7, 8), then counts from the value loaded until the next Transfer Speed Count pulse occurs. The rate of counting is determined by the specific clock signals selected by the Speed Control Programming array plug-in J121. If a count condition occurs in the Speed Control Counter which satisfies the decode of either U223-8 or U223-11, or U241, pin 11, then that value will be stored in the respective speed value flip-flop. At the time of the next Transfer Speed Count pulse, the value decoded and stored in the speed-value flip-flop will then be transferred to the speed status flip-flops. Note that two different values may be loaded into the Speed Control Counter at the time of a Speed Count Reset pulse. One is the normal running speed which will occur when the Purge Cycle Flip-Flop is zero-set, and the other value is a 10 percent overspeed which will be loaded when the Purge Cycle Flip-Flop is one-set.

The state of the Speed Out Of Tolerance Flip-Flop (U243 zone F3) is directly tested during a start sequence to determine if there is a gross speed error prior to loading the heads. Once the machine has reached the ready condition, an occurrence of a logic one at the Speed Out Of Tolerance Flip-Flop output (LSOTF) will be gated by U343-6 with the Ready signal producing the Disk Speed Error (NLDSEG) signal. Disk Speed Error can therefore occur only during the time that the disk drive is Ready.

The state of the Increase Motor Speed Flip-Flop at the end of each speed count interval will indicate a basic binary error signal derived from the comparison of the time reference to the actual speed. This flip-flop will be pre-set by the Start Drive Motor (NLSDMG) pulse as a means of initializing the speed status during a start sequence. Note that the result of the time-speed comparison is a single binary digit that can have only two possible states; one or zero, indicating that the speed is either too fast or too slow. If it is too slow, the Increase Motor Speed Flip-Flop will be in the one-set condition indicating that the motor speed should be increased. Conversely, if the speed is too fast, the Increase Motor Speed Flip-Flop will be zero-set, indicating that it is unnecessary for the motor speed to be increased and allowing the motor to coast down through the desired speed value.

5.5.3 SHEET 4 (SCHEMATIC NO. 102830)

Sheet 4 of the Logic PCBA schematic contains the Position Control Logic. Refer to the functional description and simplified block diagram contained in Paragraph 4.7 in conjunction with this discussion.

The overall purpose of the Position Control Logic is to accept cylinder addresses from the I/O interface and control the positioning and holding of the positioner at those addresses. The subsidiary function of this logic is to execute Restore operations and to control loading and unloading of the heads. The actual control functions within this logic are performed by the Load Address Logic and Busy Logic, the Mode Control Logic, and Operation Control Logic.

The Mode Control portion of the Position Control Logic consists of the Position/Velocity Mode Logic (zone E5), the Forward Slow Mode Flip-Flop (zone C4), and the REVERSE Slow Mode Flip-Flop (zone B4). The Position/Velocity Mode Logic determines when the positioner servo should be operated in the Position Mode and when it should be operated in the Velocity Mode. This logic also supplies the Position Mode (LPMXG) signal and the Velocity Reference Enable (NLVREG) signal to the Servo PCBA.

The Forward Slow Mode Flip-Flop (U167 zone C4) determines the state of the Forward Slow Mode (NLFSM1) signal, which is supplied to the Servo PCBA, to cause the positioner servo to operate in the Forward Slow Velocity Mode. Likewise, the Reverse Slow Mode Flip-Flop (U206 zone B4) functions to store and provide a state which asserts Reverse Slow Mode (NLRSM1) to the positioner servo for operating the positioner in the Reverse Slow Velocity Mode. The Forward Slow Mode is used when loading heads and during the last portion of a restore operation. The Reverse Slow Mode is used when unloading heads and during the first portion of a restore operation.

The Forward Slow-Mode Flip-Flop (U167) is released for operation when the Load Heads Flip-Flop (LLHFF) is one-set. Prior to loading, the heads will be retracted. This condition is indicated by Heads Retracted (SHRXG) being high, which in conjunction with one-setting the Load Heads Flip-Flop, results in a high logic level from U187-4 (zone C5). A high output at U187-4 causes the Forward Slow Mode Flip-Flop to be pre-set to commence loading the heads.

Recall that the Forward Slow Mode Flip-Flop (U167) is used also when performing a Restore operation. In this case, pre-setting the Forward Slow Mode Flip-Flop is controlled by the setting of the Restore Operation Flip-Flop (U206 zone A4). The Restore Operation Flip-Flop determines whether the address as asserted by the interface will be examined or whether it will be disregarded and a Restore operation performed.

The Restore Operation Flip-Flop (U206) will be pre-set by the low active pulse from U49-6 (zone B6). This pulse will occur if the Restore Initial Cylinder (IRICR) line is active at the time that a Cylinder Address Strobe (ICASR) is supplied from the I/O interface. At that time, pins 4 and 5 of U49 will be high, pre-setting the Restore Operation Flip-Flop. When this flip-flop is pre-set, U187-10 is enabled to pre-set the Forward Slow Mode Flip-Flop by the negation of Position Transducer Index (SPTIG) during the latter portion of a restore operation.

The Forward Slow Mode Flip-Flop is zero-set by the first high-to-low transition of Position Quadrature Clock (SPQCG) that occurs after the change of state of Position Transducer Index (SPTIG) during loading of the heads. Since this occurrence must follow after the change of state of Heads Retract (SHRXG), both SHRXG and SPTIG are ANDed by U187-1 (zone C5).

The Reverse Slow Mode Flip-Flop (U206 zone B4) is pre-set at the same time that the Restore Operation Flip-Flop (U206 zone A4) is pre-set when a Restore operation is commanded. The Reverse Slow Mode Flip-Flop can also be one-set when the Load Heads Flip-Flop is zero-set. This results from (NLLHFF) being high, enabling the J input of the Reverse Slow Mode Flip-Flop. The Reverse Slow Mode Flip-Flop is cleared when the Forward Slow Mode Flip-Flop is pre-set.

When either of the slow mode flip-flops are one-set, the demand address clear condition will occur via U49-8 (zone C3). This will clear the Demand Address Registers (U301, U321, U302 zone E, F, G, H-17). In addition, Demand Address Clear, in the form of a low active signal (NLDACG), will disable the Count Clock Detector Register (U323 zone C14) by clearing it to an all-zeros condition and will cause the Current Address Counter (U322,

U381, U342 zone E11, 12, 13) to load all-ones. NLDACG also forces NLVREG to the high logic level via U403-8 (zone E4) disabling the velocity reference, and forcing Not Position Mode (NLPMXG). In this manner, the logic is initialized and conditioned during the time the heads are being loaded or retracted, or during the execution of a Restore operation.

When a demand address clear condition does not exist (both the Forward Slow Mode Flip-Flop and the Reverse Slow Mode Flip-Flop zero-set), the Count Clock Detector Register (U323 zone C14), the Demand Address Registers (U301, U321, U302), and the Current Address Counter (U381 zone E12) will be released. The Velocity Reference Enable and Position Mode signals will be under control of the other gates.

In the Position/Velocity Mode Logic, when Not Demand Address Clear (NLDACG) is high (a Demand Address Clear condition is not occurring), the Position Mode signal will be asserted when the address difference is zero and Position Quadrature Clock is low. This will be the case when the Current Address Counter contents agree with the Demand Address Register contents and the positioner is within one-quarter track of the true-track center line.

The purpose of the Load Address Logic is to generate a low-active pulse, Load Address (NLLAXG) when a Cylinder Address Strobe (ICASR) is received from the I/O interface and the address on the Cylinder Address Lines is a valid address. Another function of this circuitry is to generate a Busy signal to the I/O interface when a Strobe is received, or when the positioner is Busy Seeking. Another function of this logic is to generate an illegal address indication to the I/O interface when the address on the interface lines is invalid at the time that a strobe is received.

Cylinder Address Strobe (ICASR) is received via J101, inverted, and shifted through the Strobe Shift Register (U108 zone C12). When the level change first occurs at bit A of the strobe shift register, the Hold Busy Time Flip-Flop (U128 zone C9) is caused to one-set, which results in immediate assertion of the Busy Signal to the interface. This also releases the previously cleared Hold Delay Shift Register (U146 zone C-9). The Hold Delay Shift Register, however, does not propagate logic ones because the Strobe Shift Register A bit is still in the logic one condition. The strobe trailing edge is edge-detected by the combination of U127-4 and U127-1 to generate Address Pulse (LAPXG) (zone D11). LAPXG samples the state on the Restore Initial Cylinder Line (IRICR) at U49-6 (zone B6) to determine if the Restore Operation Flip-Flop and the Reverse Slow Mode Flip-Flop should be pre-set to commence a Restore operation.

The Address Pulse also enables the input (pin 1) of U107 (zone D11) and, if the cylinder demand address is valid (as determined by the Valid Address Decoder), and if the positioner is not seeking (as determined by the state of the Busy Time Flip-Flop), then the Load Address Pulse (NLLAXG) will be generated. This pulse causes the Demand Address Register to load the address that is present on the Cylinder Demand Address Lines.

NLLAXG also clears the Illegal Address Flip-Flop (U167 zone B7) if it was one-set from any previous illegal address condition. When Strobe Shift Register Bit A goes low, at the time of the trailing edge of the Strobe, this causes logic ones to propagate through the Hold Delay Shift Register. This level change propagating through the register may result in zero setting the Busy Time Flip-Flop (U128 zone B11). This removes the Busy Signal from the interface if the positioner has not gone busy. This would be the case if an illegal address or an address that is the same as the current position has been received.

It is important to note that the Strobe Shift Register is able to accept Cylinder Address Strobes from the I/O interface only when it is released for operation by a high-logic level on the Selected And Ready (LSARG) line. Note also that the Illegal Address Flip-Flop

(U167 zone C7) is clocked by the high to low transition of the Strobe Shift Register, bit A. If the J input of the flip-flop is a logic one at the time of that transition, then the Illegal Address Flip-Flop will be one-set. This would be the case if the Busy Time Flip-Flop is one-set, or if the output of the Valid Address Decoder is at the low logic level, indicating an invalid address. Therefore, the Illegal Address Flip-Flop will indicate an illegal address if the positioner is already busy, or if the address is invalid at the time of a Cylinder Address Strobe. Notice that the Illegal Address Flip-Flop can be cleared by either unloading of the heads, when LLHFF goes low, or by a valid address being accepted, when NLLAXG is generated, or by one-setting the Restore Operation Flip-Flop when a Restore operation is commenced.

The Illegal Address (NLIAXG) signal from U167 (zone B7) is supplied to the interface by a line driver (on sheet 3 of the schematic) only if the Selected And Ready (LSARG) line is at a logic one level. Also, during the time that the Strobe Shift Register, bit B, is in the logic one condition, the illegal address signal to the interface is disabled by U107-11 (zone C7). If an address is loaded into the Demand Address Register which is different than the address stored in the Current Address Counter, then an address difference will be produced. This difference results in the Position Mode (LPMXG) signal going low. This will cause pre-setting of the Busy Time Flip-Flop which indicates that the positioner will be busy executing a seek. This signal is supplied to the I/O interface. Additionally, the Settle-Time Delay Register (U109 zone A11) is cleared in preparation for determining the settling time at the end of the seek.

Notice that the Busy Signal (NLBXG) to the I/O interface from the Hold Busy Time Flip-Flop (U128 zone C10) and the Busy Time Flip-Flop (U128 zone B11) is enabled only when these flip-flops are released by a high logic level of the Ready signal (LRXXG). As the positioner completes the seek, the address difference will reach zero and the positioner will reach a position that is within a quarter-track of the true-track center line. At this time, Position Mode will be asserted causing LPMXG (zone D3) to go to the high logic level. Since LPMXG is applied to the Settle-Time Delay Register, it will commence propagating logic-one's through the register. After the delay, determined by the register propagation time, the End Busy (LEBXG) signal will cause zero-setting of the Busy Time Flip-Flop and the Restore Operation Flip-Flop. This terminates the Busy Signal to the interface and also terminates any Restore operation status in the Operation Control portion of the Position Control Logic.

The Settle Time Delay Register (U109 zone A11) is clocked by LC13F from the clock countdown. Therefore, the delay time established by the Settle-Time Delay Register is determined by the clock frequency and the number of bits that must be propagated after the level change on Position Mode (LPMXG).

The validity of a demand address on the I/O interface lines is tested by the Valid Address Decoders. There is one decoder for 100-track per inch addresses (zone C16) and another decoder for 200-track per inch addresses (zone D16). Only one of the decoders is connected depending upon the specific configuration of the machine.

The Valid Address Decoder is combinational logic configured to provide an output signal that will be high if the input Cylinder Demand Address is within the legal range of values, and to provide a low logic level output when the Cylinder Demand Address lines have an address outside of the legal range. The range of legal addresses for 203 cylinder models is from 000 to and including 202. The range for legal addresses for 406 cylinder models is from 000 to and including 405.

As previously described, the Demand Address Register (U301, U321, U302 zone E, F, G, 16) will either hold the last value, load a new value if the NLLAXG pulse occurs, or will be cleared and held if a Demand Address Clear condition occurs. Therefore, the contents of the Demand Address Register will either be all zeros or the last Demand Address loaded. The contents of the demand address register therefore specify the present cylinder demanded.

The current position of the positioner is stored in the Current Address Counter (U381 zone E12). The Current Address Counter is an up/down counter. The direction and amount of the count is determined by the count control on the basis of the Position Reference Clock (SPRCG) and the Position Quadrature Clock (SPQCG) signals from the Servo PCBA. These digital signals are derived from the outputs of the position transducer. During loading of the heads, the Current Address Counter is first loaded to a condition of all-ones and then counted by one up-count clock to an all-zeros condition to initialize the Current Address Counter at cylinder 000.

Each high-to-low transition of the Position Quadrature Clock (SPQCG) is detected by the Count Clock Detector Register (U323 zone C13). A one-clock time pulse is generated for each high-to-low transition of SPQCG, and this pulse, via U383-4, is used to strobe the Up/Down Count Logic (zone E13). If during the time of the count clock pulse, Position Reference Clock (SPRCG) is high, the Current Address Counter will be counted down. If, however, SPRCG is low during the time of a count clock, the Current Address Counter will be counted up. A UP count increases the value in the address counter indicating that the positioner is moving toward the spindle, and a DOWN count clock decreases the value stored in the Current Address Counter indicating that the positioner is moving away from the spindle.

During a seek, the positioner servo is operated as a velocity type of servo. A particular velocity level is determined on the basis of the amount of difference between the current address and the demand address. This difference is specified to the Velocity Function Generator on the Servo PCBA by the Address Difference Lines (NLAD0G through NLAD7G and including NLADEG) (zone E, F, G, H-6).

The address difference, that is the difference between the Current Address Counter contents and the Demand Address Register contents, is obtained by performing a ones-compliment arithmetic subtraction on the binary values of those counter and register contents. This subtraction process is performed by the Subtractor (zone F, G, H-10) and Complimentor (zone F, G, H-8). The actual subtraction is mechanized using an integrated circuit binary full-adder.

Since the arithmetic is ones-compliment arithmetic an end around carry is used. This carry is under control of the Carry Control Logic (zone E9). The algebraic sign of the velocity is determined on the basis of the binary value of the carry which specifies the binary state that is on the Forward Direction Line (LFDX1).

The end around carry circuit can be traced on the schematic starting at U402 (zone H10) at the C4 output and preceding to U361 (zone D9), pin 2 and 13, and from there through the Carry Control Flip-Flop U341, pin 15, and then to the input of U382 (zone E10). Note that the input to Carry Control Flip-Flop determines the state on the Forward Direction Line (LFDX1).

As shown on the schematic the integrated circuit binary full-adder is connected in a ripple-carry fashion to close the remainder of the end around carry loop. Notice also that the input to the least significant adder from the output of the Carry Control Flip-Flop (U341-15) also controls the complimentor.

The complimentor circuit is required for the situation where negative arithmetic is being performed. The complimentor provides conditional inversion of the outputs of the subtractor according to the state of the carry into the subtractor. Note that the subtractor uses the content of the Current Address Counter directly, whereas the contents of the Demand Address Register are complimented or inverted by the inverters shown in zone F and G13.

When the heads are being loaded, it is necessary to force the carry to a particular state. This is accomplished by the Carry Control on the basis of the states from certain bits in the Current Address Counter. U361-6 (zone D10) essentially decodes all one states in the most significant bits of the Current Address Counter and forces the carry to a specific state during the time that the heads are being loaded. Only during that time will the Current Address Counter have logic ones in the most significant positions of the counter. By forcing the carry during the loading of the heads, a least significant velocity reference level is specified by NLAD0G, such that between the time when the Forward Slow Mode operation is ended and the Position Mode is commenced the positioner servo is operated as a true velocity servo with a least significant velocity reference.

For 200 tpi operation the three most significant bits of the current address counter are buffered by U441 and U443 and sent to the Temperature Compensation PCBA via J114.

The Error Check Logic (zone F, G, H-3, 4, 5) performs two types of checks concerned with the operation of the positioner. The first check determines if the positioner has completed a seek within the maximum allowable time. This is done by the Seek Time Error Check Counter U287 (zone G4). This is a gross type of check to determine that the positioner has not become stalled due to a fault. While each and every seek is checked by the circuit it does not verify that a specific distance moved was accomplished within the specific time associated with that length of seek. Rather, it determines that the positioner has not become stalled while attempting a seek.

The Seek Time Error Check Counter is enabled to count the LC17F clock from the clock countdown whenever the Busy Time Flip-Flop is one-set. This is a result of Not Busy Time (NLBTFF) being fed to the input of U246, pin 9 (zone G5).

If the counter has not counted up to the state where the carry-out has occurred, then the inputs at pins 9 and 10 of U246 will be high when the positioner is not busy. This causes U246-8 to go low, loading all zeros into the Seek Time Error Check Counter U287.

When all-zeros are loaded into the counter and the load input is held at the low level, the counter is locked up and cannot count the LC17F clock. However, when the positioner goes busy, NLBTFF goes low causing U246-8 to go high, releasing the counter and allowing it to count LC17F clocks.

If the Busy Time ends before the counter has counted up to the carry-out condition, then the seek has been completed well within the maximum allowable time; the Busy Flip-Flop will again load zeros into the counter before the carry-out has occurred. Should the positioner become stalled, or other faults develop which cause the Busy signal to exist for a sufficient period of time for the counter to count to the carry-out condition, then the carry-out (U287, pin 12) will go low indicating a Seek Time Error (NLSTEG). This results in execution of an Emergency Unload.

Notice that the Restore Operation Flip-Flop (LROFF) is fed to the clear input of the Seek Time Error Check Counter. This signal clears the counter during the time of a Restore Operation. It is not desirable to check Seek Time during a Restore operation.

The other check performed by the Error Check Logic is to determine that the positioner has not traveled outside of the legal range of travel. This is performed by the Position Limit Monitor circuitry shown in zone F4. This circuit generates a Position Limit Error signal (NLPLEG) if the positioner exceeds the normal range of travel. This check is performed only during the time that the heads are loaded onto the disk.

The Position Limit Monitor Flip-Flop (U267 zone F4) is cleared by NLLPNG. This signal will be low and therefore clear the flip-flop whenever the Purge Cycle Flip-Flop and the Load-Heads Flip-Flop are both zero-set. This will occur when the disk drive is not in a Run Condition or is in the Run Condition but not yet in a Purge Cycle. This can be seen by examining the logic shown on sheet 2 of the Logic PCBA schematic.

When loading heads, the Load Heads Flip-Flop will be one-set thus assuring that the Position Limit Monitor Flip-Flop is released for operation. Note that the J input of the Position Limit Monitor Flip-Flop is a continuous logic one, and therefore any high-to-low transition on the clock input of the flip-flop (U267 pin 6) will clock the flip-flop into a one-set condition. The flip-flop will remain one-set until it is cleared by NLLPNG going to the low-logic level.

During the loading of the heads, the Restore Operation Flip-Flop will be zero-set. As the positioner moves forward SPTIG will come to the high logic level causing pins 4 and 5 of U246 (zone F5) to be high, thus causing a low-to-high transition at U267, pin 6. As the heads load, SPTIG will go from the high level back to the low level, which will cause U267, pin 6, to go from a high to a low. This will one-set the Position Limit Monitor Flip-Flop, arming the monitor.

When the Position Limit Monitor flip-flop one-sets, the NAND gate U246 (zone F3) is enabled at its input on pin 12. A positioner fault may be indicated by either an occurrence of Position Transducer Index (SPTIG), or by the occurrence of Heads Retract, after the heads have been loaded. If SPTIG goes high it indicates that the positioner has traveled outside of its legal range. This will cause U246, pin 2 (zone E4) to go low which in turn will result in U246, pin 11 (zone E3), going low, thus indicating Position Limit Error (NLPLEG).

The other method for detecting a fault is if Heads Retract (SHRXG) goes high. This will force U246, pin 1 (zone E4), to the low-logic level, and again U246, pin 11 will go low, indicating Position Limit Error (NLPLEG). Either condition results in emergency unload.

The success of emergency unload will depend on the nature of the fault which originally caused the occurrence of Position Transducer Index (SPTIG), or Heads Retract (SHRXG).

If a multiple Position Transducer Index (SPTIG) occurs during the loading of the heads, this circuit will detect that occurrence and immediately commence an emergency unload before allowing completion of loading the heads. Likewise, this circuit will detect certain faults in the position transducer.

Refer to the circuitry contained in zones H12 and 13. The most significant bit of the Demand Address Register for either 100-track per inch or 200-track per inch machines can be selected by the jumper arrangement W11 or W12, as appropriate. This Demand Address Most Significant (LDAMG) signal is fed to the Read/Write PCBA where it is used for switching the write current to the particular value utilized for high order cylinder addresses.

5.5.4 SHEET 5 (SCHEMATIC NO. 102830)

Sheet 5 of the Logic PCBA schematic contains the Sector Electronics portion of the D3000 logic. Refer to the functional discussion and simplified block diagram contained in Paragraph 4.7 in conjunction with this discussion.

The purpose of the circuitry contained on sheet 5 of the schematic is to provide pulses at the I/O interface for electrically subdividing the storage surface into sectors. In addition to the pulses provided, the specific number of the sector passing under the Read/Write heads is also transmitted as a sector count which is used for addressing data stored on the disk. An index pulse is also provided as an output. This provides a signal which is a pulse occurring once per revolution of the disk that can be utilized to define the sector reference.

There are two basic types of sectoring: mechanical and electronic. The electronic type of sectoring may be further classified into electronic sectoring with the index-only type of cartridge and electronic sectoring with a multi-notch cartridge.

The primary inputs to the sector circuits are derived from two sensors located in the disk drive, and from clock signals derived from the Clock Countdown in the Start/Stop Control logic (sheet 2 of schematic). The Drive/Motor Enable signal is also used in the sector electronics circuits. The Upper Platter Select signal and the Selected And Ready signal is employed to control the output multiplexer. These signals are also obtained from the Start/Stop Control Logic.

The outputs of the sector electronics are the Sector Pulse (ISPXD), the Index Pulse (IIPXD), and the Sector Count (ISC0D-ISC6D).

The Sector Pulse (ISPXD) provides a train of pulses at regular intervals during each revolution of the disk. These pulses divide the disk surface into 'n' equal segments, where 'n' is the number of pulses and the number of sectors.

The Index Pulse (IIPXD) is a pulse train with a single pulse occurring once per revolution of the disk. This pulse always occurs just prior to sector zero.

The Sector Count lines (ISC0D-ISC6D) specify the sector count which is presented to the I/O interface in a binary format. This count indicates the particular segment of the disk surface currently under the Read/Write heads. The signals on these lines are, in essence, the states of a binary counter and in all cases correspond only to the respective platter as selected by the Platter Select Line.

The particular type of sectoring for which a disk drive is configured is determined by the programming arrays that are installed in the Logic PCBA. The parameters that are programmed into these arrays determine the nature of the sectoring. These parameters are: type of sectoring, number of sectors, and related disk speed.

The type of sectoring is programmed by the programming array plug installed in J125 (zone C, D, E, F-14). The values for the Upper and Lower Demultiplexer Counters, which are relative to the speed of the disk, are programmed by J121, shown in zone 15.

The number of sectors for electronic sectoring is programmed by J126 and J127 shown in zones 10, 11, and 12. The electronic sectoring is configured by the programming array plugs installed in J123 and J124. These arrays determine certain parameters of the electronic sectoring.

The Upper Sensor Detector (zone H19) and the Lower Sensor Detector (zone F19) receive signals from the upper and lower sensors, via J112 (zone E, F, G, H-20), and convert these analog signals into digital form. The Lower Sensor Detector circuit is similar to the upper sensor detector except that it has the additional capability of changing thresholds.

The Upper Sensor Detector has two amplifiers U425 and U387, which are not required in the Lower Sensor Detector. Otherwise, the circuit functions are similar. The Upper Sensor Detector receives the signal derived from sensing thinto a digital pulse train. The Lower Sensor Detector converts the analog signal obtained from the Lower Magnetic Sensor, which senses the Phase Lock Ring, into a digital pulse train.

NOTE

The removable cartridge may be sectored either electronically or mechanically. The lower platter is always sectored electronically in dual disk machines.

Standard top loading cartridges are fitted with an armature plate having one notch which is the Index notch. Some specially modified top loading cartridges will have, in addition to the index notch, notches used for purposes of mechanical sectoring.

Standard front loading cartridges have slots for the purpose of mechanical sectoring, and a single index slot. The sector slots and the index slot are located in the sector ring. Some specially designed front-load cartridges have only an index slot in the sector ring.

Front loading models of the D3000 employ a photoelectric type of sensor for the upper sensor. Top loading models use a magnetic transducer for the upper sensor. On all models, the lower sensor is a magnetic type transducer. The upper sensor for front loading models connects to J112, pin 9 (zone H20). For top loading models, the upper sensor is connected to J112, pin 6 (zone G20).

U425 (zone G20) serves as a fixed voltage gain amplifier when the magnetic sensor is connected and functions as a current-to-voltage converter when the photoelectric sensor is connected. Gain for the circuit is established by R28, R29, and R30 (or W19) for the magnetic sensor connection and by R27, R29, and R30 (or W19), for the photoelectric sensor. C5 determines the band width. C6 and C7 decouple power supply voltages for U425. The signal from U425 is coupled to a voltage follower U387 by an R-C network, C8 and R31.

The output of the voltage follower, U387, is fed directly to a Schmitt trigger comprised of one section of U409 (zone G18). The Schmitt trigger threshold is determined by R35, R33, R32, and the +5.0v power supply voltage. The output of the Schmitt trigger is buffered by U408-8 and fed to the Upper Time-Demultiplexer. The signal at this point will be a pulse-train with one pulse per slot, or notch detected by the sensor. The purpose of the Schmitt trigger then is to convert the analog signal from the amplifier circuits into a digital signal suitable for use in the Upper Time-Demultiplexer and the remainder of the logic.

Referring to J112 (zone D18) it can be seen that power for operating the photoelectric sensor for front load machines is supplied via this connector.

The lower-sensor detector functions in a manner similar to the upper sensor detector. The lower magnetic sensor connects to J112, pin 4 (zone F20). The output of this sensor is filtered by R36 and C12; then fed directly to a Schmitt trigger consisting of the other half of U409 (zone F19). The threshold for the high threshold mode is determined by R43, R42, R39, R37, and R38. For the high threshold mode the output transistor of U444-4 (zone E19) will not be conducting; therefore R40 will be essentially open circuited. In the low threshold mode, which will be the case whenever Drive Motor Enable (LDMEG) is low, the end of R40 which is connected to U444-4 will be essentially connected to ground. Therefore, the threshold for the low-threshold mode will be determined by R43, R42, R40, R39, R37, and R38. The output of the Schmitt trigger is buffered by U408-4 and U408-2 and fed to the Lower Time-Demultiplexer. In addition, U408-4 also feeds the Lower Detector Pulse (LLDPG) to the Disk Rotation Detector Counter (sheet one of the schematic) for detecting disk rotation.

The pulse trains obtained from the Sensor Detectors will have an index pulse intermixed with the other pulses if the sensor is detecting multiple notches. This, of course, will be the case at all times for the Lower Magnetic Sensor which senses the Phase Lock Ring. However, the pulse obtained from the index notch from the Upper Sensor will be inter-spersed with the pulses obtained from the sector notch only if it is a multi-notch

cartridge. In the case of an index-only cartridge, the pulse train will be comprised entirely of index pulses. In any event, the pulse obtained from the index notch must be separated from the sector notches as appropriate. This function is performed by the time demultiplexers for those situations requiring demultiplexing. The pulse obtained from the index notch is placed onto a line separate from the other pulses.

The Lower Time Demultiplexer (zone E16) separates the pulse obtained from the index notch on the Phase Lock Ring from the phase lock pulses. The phase lock pulses will be demultiplexed and output at U183, pins 10 and 13 (zone D15). The pulse obtained from an index notch on the Phase Lock Ring is output at U183-10 (zone D15). Only a single clock frequency is utilized by the Lower Time Demultiplexer; this is LCO8F (zone D17) obtained from the clock countdown in the Start/Stop Control Logic.

The Upper Time Demultiplexer outputs the pulse obtained from the index notch, in index-only cartridges, at U183, pin 4 (zone F15). Since there are no sector notches in index-only cartridges, there will be no output at U183, pin 1, for the index-only cartridge situation. When using a multi-notch cartridge, the Upper Time Demultiplexer will output the demultiplexed index pulse at U183, pin 1 (zone E15) and the demultiplexed sector pulses at U183, pin 4. The clock frequencies used with the Upper Time Demultiplexer are determined by a jumper installed at W20, W5, or W6 (zone F16). Clock LCO8F, LCO9F or LC10F from the clock countdown are available at W20, W5, and W6, respectively.

For both Time Demultiplexers, the specific value of the demultiplexing gate time is determined by the programming array installed in J121 (zone D, F15). The Time Demultiplexer functions by generating a gate time according to the value loaded into the demultiplexer counter. The Upper Time Demultiplexer Counter (Upper Demux. Counter) is U184 (zone G15) and the Lower Time Demultiplexer Counter (Lower Demux. Counter) is U164 (zone E15). The value loaded into these demultiplexer counters is determined by the programming array plug-in J121.

Generation of the demultiplexer gate is controlled by the respective Demultiplexer Control Flip-Flop, U203 (zone G17) for the Upper Time Demultiplexer and U163 (zone E17) for the Lower Time Demultiplexer. The outputs of U203 and U163 are fed to the Upper and Lower Time Demultiplexer Gate Flip-Flops, respectively. The actual demultiplexer gate is obtained from the respective demultiplexer gate flip-flop. The output of the respective demultiplexer flip-flop is the enabling input to demultiplexing gates U183-4, U183-1, U183-10, and U183-13 (zone D, F15).

The time demultiplexer functions on the principle that for a pulse occurrence a gate is generated. If, during the time of that gate, another pulse occurs, that pulse is a pulse derived from the index notch. All other pulses are taken as being derived from other than the index notch.

The specific demultiplexed pulses are connected to the Sectoring Selection Programming array at J125 (zone C, D, E, F-14). The outputs of the Sectoring Selection Programming array are fed to pulse formers and sector number counters.

The pulses obtained from the Time Demultiplexers or from the electronic sectoring electronics are unsuitable for direct output at the I/O interface; therefore they must be formed into pulses compatible with the interface requirements. This is accomplished by the Pulse Formers shown in zones G, H5 through 9. There are four pulse formers. One for the Upper Sector Pulse, one for the Lower Sector Pulse, one for the Lower Index Pulse and one for the Upper Index Pulse.

The pulse formers are essentially shift registers (U22, U2, U23 and U43) connected as delays and edge detectors. The actual pulse forming is accomplished by NOR-gates, U63 (zone G, H through 8). The clock used for determining pulse timing and delay is LCO4F obtained from the clock countdown in the Start/Stop Control Logic.

The outputs of the Upper and Lower Sector Pulse Formers are multiplexed onto the single Sector Pulse line (ISPXER U62-8 (zone G4). The pulse driven by U44-3 (zone G4) depends upon the particular platter selected by the interface. Likewise, the outputs of the Upper and Lower Index Pulse Formers are multiplexed by the Index Pulse Multiplexer (U62-6) and fed to the single Index Pulse line (IIPXD) according to the particular platter selected by the interface.

The Sector Pulse Multiplexer and the Index Pulse Multiplexer are controlled by the Multiplexer Control Logic (zone F9) which also controls the Sector Count Multiplexer according to the states of the Platter Select Line (LUPSG) and the Selected And Ready (NLSARG) line. NLSARG enables the Multiplexer Control gates only when the disk drive is selected and ready. Thus, the output of the Multiplexer Control Logic is gated with Selected And Ready signal.

The specific multiplexer enabled, either the upper multiplexer or the lower multiplexer, is determined at the input to the Multiplexer Control Logic by the states on NLUPSG and LUPSG. These signals are derived from the Platter Select Line input to the Disk Drive Function Control Logic, as shown in sheet 3 of the schematic.

When the disk drive is not selected, or not ready, then both LUMEG and LLMEG will be low, disabling the multiplexers. When the disk drive is Selected And Ready, then either Upper Multiplexer Enable (LUMEG) will be high or Lower Multiplexer Enable (LLMEG) will be high, according to whether the upper or the lower platter is being selected by the Platter Select Line. Thus, the action of the Multiplexer Control Logic is to determine which of the pulse and sector count outputs will be enabled and supplied to the I/O interface, J102.

The pulses obtained from the Sectoring Selection Programming array at J125 are also applied to the Sector Number Counters and the Count Control Logic to generate the sector count. The Upper Sector Number Counter (zone E7, 8) and the Upper Count Control Flip-Flop (zone D8) generate the upper sector number count. U144 and U143 are the Upper Sector Number Counters, and the count is controlled by the Upper Count Control Flip-Flop U83. The Lower Sector Number Counter (zone B7, 8) and the Lower Count Control Flip-Flop (zone B8) generate the sector number count for the lower platter. U125 and U124 are the Lower Sector Number Counters, and the count is controlled by the Lower Count Control Flip-Flop U83.

The contents of the particular sector number counter are multiplexed onto the Sector Count Lines (ISC0D through ISC6D) through the Sector Count Multiplexer (zone A, B, C, D, E-5) according to the control signals generated by the Multiplexer Control Logic. U84, U104, U105, and U85 form the Sector Count Multiplexer. One or the other of the sector number counter contents will be selected and supplied to the line drivers according to the control signals from the Multiplexer Control Logic. For each sector count line, there is a separate line driver. The specific sector number count, multiplexed onto the sector count lines, is determined by which platter is selected by the Platter Select Line and will only be presented to the I/O interface if the disk drive is Selected and Ready.

The mechanization of the Upper Sector Number Counter and Upper Count Control is identical to that used with the Lower Sector Number Counter and Lower Count Control. Therefore, only the Upper Sector Number Counter and Upper Count Control Flip-Flop will be explained.

The sector number count is represented by the binary value contained in the sector number counter. The Q_A output of U144 is the least significant bit and the Q_C output of U143 is the most significant bit of the number. The counter is clocked, or counted up, by the raw sector pulse obtained from the Sectoring Selection Programming array plug at J125 (zone C, D, E, F-14). For each pulse the counter will be incremented by one count. The Index Pulse which occurs once per revolution of the disk, is defined as occurring during the sector just prior to sector zero; i.e., during sector N minus one where N is the maximum number of sectors. Therefore, at the time of occurrence of the index pulse, U83, the Upper Count Control Flip-Flop (zone E8) will be pre-set by the occurrence of the Index Pulse. This will cause the Q output of U83, pin 10, to go low, enabling the load inputs (LD) of U144 and U143. However, the counter will not load zeros until the next sector pulse. At that time, instead of incrementing the count, it will be clocked to load all zeros. At the time that this clocking occurs, the Upper Sector Count Flip-Flop will be zero-set since the K-input of the flip-flop is enabled at all times. This will remove the enable from the load inputs (LD) of the Sector Number Counter and allow it to be incremented or clocked by the raw sector pulse. The Sector Pulse immediately following an Index Pulse defines the beginning of sector zero. At the time of that Sector Pulse, the Sector Count lines will present a zero value as the result of having loaded the Sector Number Counter with all zeros. Thereafter, the value will be incremented until the maximum count is achieved. The maximum count that will occur is N minus one, where N is the number of sector pulses.

Recall from the previous discussion that the lower platter is always sectored electronically in dual-disk machines. Recall also that the removable cartridge in either single-disk machines or dual-disk machines may be sectored electronically. The exception to this is if the cartridge has an index-only notch, then it must be sectored electronically.

Electronic sectoring is selected by the Sectoring Selection Programming array installed in J125. When electronic sectoring is selected, the output of the electronic sectoring electronics is connected to the Upper Sector Pulse Former, the Upper Sector Number Counter, and the Upper Count Control Flip-Flop.

NOTE

The Lower Sector Number Counter, Lower Count Control, and Lower Sector Pulse Former are connected to the electronic sectoring electronics at all times since the lower platter is always sectored electronically.

Electronic sectoring requires that the disk drive generate pulses electronically for sectoring in lieu of the mechanical slots normally used for sectoring. Since the lower disk is sectored electronically regardless of the mechanical configuration, pulses must always be generated for sectoring the lower disk. These pulses are generated by counting down, with an electronic counter, the output of a high frequency oscillator. Because the sector pulses must be synchronous with the instantaneous speed of rotation of the spindle, it is necessary to phase lock this high-frequency oscillator to the spindle.

The high-frequency oscillator is a voltage controlled oscillator which is a part of the Sector Phase Lock Loop. The function and purpose of the Phase Lock Loop is to phase-lock the voltage controlled oscillator frequency to the phase lock pulses obtained from the Phase Lock Ring through the Lower Time Demultiplexer. The sector phase lock loop is shown in zones 12 through 20 at the bottom of the schematic. The input to the Sector Phase Lock Loop is from U183, pin 13, (zone D15), which is the phase lock pulse output from the Lower Time Multiplexer. It should be recalled that the phase lock pulses are separated from the lower index pulse by the Lower Time Demultiplexer.

It is necessary to count down the output of the high-frequency voltage controlled oscillator (VCO) in order to obtain the desired number of pulses per revolution for sectoring. This is accomplished by the Upper Sector Countdown Counter and the Lower Sector Countdown Counter shown in zones 10 through 12. Also associated with these counters are the Upper Electronic Sector Programming array and the Lower Electronic Sector Programming array that are installed in J126 and J127, respectively (zone C, E, 10, 11, 12). These programming arrays determine the particular number of sectors.

Since it is necessary to synchronize the countdown with the index for the respective platter, there is a synchronizer for each counter. These are used to synchronize the count with the index pulse. The index pulse is obtained from the respective Time Demultiplexer. In the case of the lower platter, the index notch on the Phase Lock Ring generates a pulse which is separated by the Time Multiplexer and applied to the Lower Synchronizer. In the case of the upper platter, the index slot or notch will generate a pulse which is separated as necessary by the Upper Time Demultiplexer and applied to the Upper Synchronizer.

The output of the respective Countdown Counter is a pulse, which is the raw sector pulse, for use by the pulse formers and the Sector Number Counter when electronic sectoring is employed.

The Sector Phase Lock Loop will be discussed first, then one of the countdown counters and synchronizers will be discussed since the Upper Synchronizer and Lower Synchronizer function in the same manner. This is also true of the Upper Sector Countdown Counter and the Lower Sector Countdown Counter. Therefore only the Lower Synchronizer and Lower Sector Countdown Counter will be discussed in this document.

The Sector Phase Lock Loop is, in essence, an electronic servo loop designed to servo the voltage controlled oscillator frequency to phase lock that frequency to the pulse-train derived from the demultiplexed phase lock ring notches.

The Sector Voltage controlled Oscillator (Sector VCO) consists of Q3, R66, R71, U227, C22, C23, C24, R67, and R68 shown in zones B and C17. C25 and C26 are used only to decouple the power supply voltages that are supplied to U227. The voltage controlled oscillator is a R-C oscillator with part of the resistive component comprised of Q3, which is made variable by the voltage applied to the gate of Q3. The output of the oscillator is derived from pin 7 of U227 and coupled into a SCHMITT TRIGGER BY C27 and R69. The Schmitt trigger consists of one section of U268 with its threshold established by R70. The output of the VCO is at U268, pin 4, which also connects to TP16 (zone C15). Thus, U268 converts the output of the oscillator into a digital signal that is suitable for use by the counters. In order to phase lock the VCO frequency to the phase locked pulses derived from the spindle, it is necessary to detect the phase difference between the Sector VCO and the phase lock pulses, to produce a control voltage to servo the frequency of the Sector VCO to the proper value. This is accomplished using a Phase Comparator and Filter shown in zones B17 through 20.

The phase lock pulses are applied to the clock input of the Phase Lock Flip-Flop U129 (zone C20). The Phase Lock Flip-Flop divides the frequency of the phase-lock pulse train by a factor of 2 and converts it into a square wave. This square wave is then applied to the Phase Comparator and Filter. Additionally, the Phase Lock Flip-Flop, Q output (LPLFF), is also fed to the Spindle Speed Control Electronics as previously described.

The other input to the phase comparator is the output of the VCO, suitably counted down. The countdown of the sector VCO is accomplished by the Sector PLL Countdown Counter (zone B13, 14, 15). The particular division ratio obtained with this countdown counter is determined by the programming array installed in J124 (Sector PLL Countdown Programming).

The output of the Sector PLL Countdown Counter is fed to the clock input of the Sector Countdown Divider Flip-Flop U129 (zone B20). The Sector Countdown Divider Flip-Flop converts the output of the Sector PLL Countdown Counter into a square wave. This square wave is the other input to the Phase Comparator and Filter. The phase comparator is comprised of U147 (zone A, B, C-19), R46, R49, R47, and R48.

The output of the Phase Comparator is filtered and applied to the input of the Sum-And-Difference Amplifier, U168 (zone B19). The filter is comprised of R51, R52, R53, R58, C16, R54, R55, R56, R59, C17. The particular filter characteristics required are programmed by part of J123 depending upon the disk speed utilized in the particular disk drive.

R60, R64, R61, R62, and R63 determine the characteristics and gain of the Sum-And-Difference Amplifier, U168. C19 and C20 decouple the power supply to U168. Adjustment of the PLL is accomplished by R57 (zone A18). The combination of R50, CR5, CR6, R57, C18, R62, and R63 provide a bias to the Sum-And-Difference Amplifier and the Sector VCO.

The output of the Sum-And-Difference Amplifier, U168, pin 6, is the control voltage to control the frequency of the Sector VCO. It is filtered by R65 in conjunction with C21. This control voltage causes the Sector VCO frequency to become phase-locked to the pulse-trained derived from the Phase Lock Ring.

The output of the VCO, which connects to TP16 (zone B15), is the input to the Countdown Counter and the VCO divider flip-flop. The Divider Flip-Flop divides the frequency of the Sector VCO by a factor of 2 for use as an alternate input to the Countdown Counters depending upon the desired number of sectors. Whether the output of the VCO Divider Flip-Flop or the output of the VCO directly is applied to the Sector Countdown Counter is a function of the particular programming array installed in J125.

The Lower Sector Countdown Counter and the Lower Synchronizer will now be described.

Operation of the Upper Synchronizer and the Upper Sector Countdown Counter is similar.

The Lower Sector Countdown Counter consists of U121, U161, and U181 (zone D10, 11, 12). These are 4-bit binary synchronous counters that may be loaded with one of two different values obtained from the Lower Electronic Sector Programming array installed at J127. The value loaded is determined by the Lower Synchronizer Register and associated circuitry which generate the I and NI signals applied to the Lower Electronic Sector Programming array, pins 5 and 6, respectively.

The Lower Sector Countdown Counter is clocked by the signal obtained from the Sectoring Selection Programming array which will be either the output of the VCO Divider Flip-Flop or the output of the Sector VCO directly.

When the Lower Sector Countdown Counter is counted from the value loaded until a carry-out occurs at U181 (zone D10), a pulse will be output at U122, pin 4. This pulse train output has a frequency which corresponds to the number of desired sectors. This pulse train will be synchronized with the index by the Lower Synchronizer Register (zone D13) and the associated synchronizing circuitry. That circuitry consists of U182 (Lower Synchronizer Register), U162-12, and U122-1 which edge detects the pulse obtained for the lower platter index by the Lower Time Demultiplexer which outputs from U183, pin 10 (zone D15).

The output of U122-1 (zone D12) is applied to the Lower Electronic Sector Programming array for purposes of determinng the value loaded into the Sector Countdown Counter.

As previously discussed, the output of U122, pin 4 (zone D10) is the raw sector pulse which is utilized by the Sector Number Counter, Count Control, and the Sector Pulse Former.

5.6 MOTOR CONTROL PCBA

The following paragraphs describe the Motor Control PCBA installed in the D3000 Series Disk Drives. Refer to Schematic No. 103570 and Assembly No. 103571.

The Motor Control PCBA is approximately 101.6 mm (4 inches) square and is physically located on top of the power transformer. This PCBA is one of the subassemblies which comprise the Power Supply Chassis. The circuitry contained on the Motor Control PCBA performs a ground isolation function and provides the drive current necessary for controlling a triac, which, in turn, switches power to the disk drive motor. This PCBA is one of the functional elements in the spindle speed control.

Figure 5-7 illustrates the placement of the six molex connectors located on the face of the PCBA. These connectors are used to provide inputs to the circuit board consisting of the line voltage, the line voltage common, a reference voltage derived from a secondary winding on the main power transformer, and a trigger from the speed control circuitry on the Servo PCBA.

Additionally, the connectors and jumpers on the face of the Motor Control PCBA are used to provide an alterable interconnection scheme for selecting different connections to the motor capacitors and the drive motor depending upon the type of line voltage operation desired. Therefore, the connectors which connect to the Motor Control PCBA, plus the jumpers on the face of the board, provide a switchable junction box to allow alteration of the connections of the drive motor windings and the motor capacitors. This can be visualized by referring to the Power Supply Schematic, Drawing No. 103580.

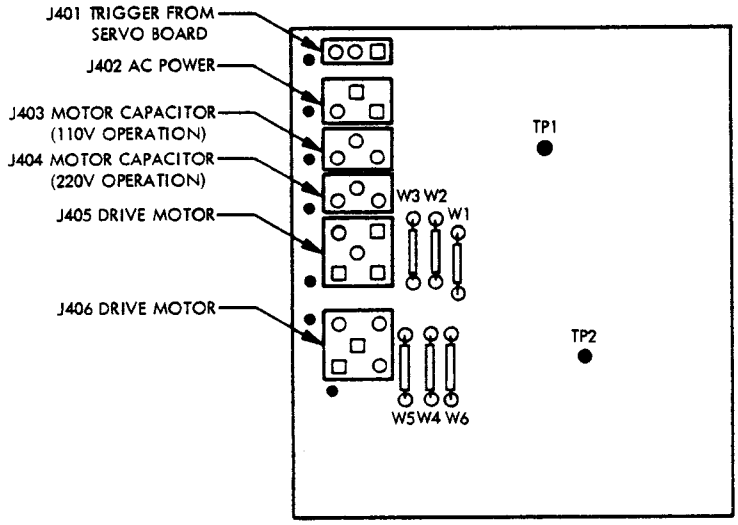

Figure 5-7. Motor Control PCBA, Test Point and Connector Placement

Note that there are two classes of line voltage operation, i.e., 110v and 220v. When a particular disk drive is configured for operation on nominal line voltages between 95v and 125v, P403 is connected to J403 on the Motor Control PCBA, and jumpers W1, W3, W4, W5 are installed. P403 is the plug from the motor capacitors and P405, P406 are the plugs from the disk drive motor. For operation on nominal line voltages of 190v to 250v, P403 connects to J404, and jumpers W2 and W6 are installed. Nominal line voltage of 95v to 125v is defined as 110v operation classification; nominal line voltage of 190v to 250v is defined as 220v operation classification. Refer to Paragraph 4.8 for the functional details of 110v and 220v operation of the drive motor.

Other than the interconnection arrangement previously described, all circuitry on the Motor Control PCBA is dedicated to switching the triac and suppressing any transients that result from this switching. A dc power supply voltage is required to provide current to the gate of the triac and must be developed with respect to the line voltage common. This is a function which is performed by a special power supply made up of CR1, R8, and C1 (zone D, 6, 7). The voltage is negative dc with respect to the ac common (pin 3 of J402). An ac signal of approximately 8v rms is provided to pin 5 of J402 from a separate secondary winding of the main transformer mounted on the power supply chassis. The voltage provided by this winding is rectified by CR1 and charges C1 to provide a relatively steady dc voltage; current limiting is provided by R8.

The trigger from the Servo PCBA is supplied to the Motor Control PCBA at J401 (zone E7). This trigger is the output of the Motor Speed Control circuitry on the Servo PCBA and is, in essence, a transistor switch closure to ground when the trigger is asserted.

When the transistor switch on the Servo PCBA is conducting and the trigger is asserted, current from the +5v supply flows through R1 (zone E7) and a Light Emitting Diode (LED), which is part of U1. U1 is an optical isolator consisting of a light-emitting diode optically coupled to a photo-transistor. When current passes through the LED it causes the LED to emit light; this light is coupled to the photo-transistor causing it to conduct. Conduction of the photo-transistor in U1 causes a base current to flow in Q1 (zone E6) which, in turn, causes a base current in Q2. Q2 conducts and provides the current to triac SCR1 (zone E5). Gate current flowing in SCR1 results in the triac conducting current through the motor winding. Conversely, when the trigger signal is absent there is no current flow through the LED in U1; therefore, the voltage across R2 causes Q1 to turn off and the voltage across R7 causes Q2 to turn off. Therefore, there is no current into the gate of the triac and conduction will stop as soon as the current through the triac passes below the holding current value, a characteristic of the device.

Resistors R3, R6, R4, and R5 provide the proper values of current in the collectors of transistors Q1 and Q2, and into the gate of the triac. R9 ensures that the gate current is sufficiently low that the triac will stop conducting. C2 and R10 (zone D5) provide a network for compensating for the fact that the drive motor is an inductive load. This means that at the time the current falls below the holding current value and the triac ceases to conduct, there will exist a certain voltage across the triac. If this voltage appears too rapidly, the triac will resume conduction and control is lost. In order to achieve control with such an inductive load the rate of rise in voltage (dv/dt) must be limited by a series R-C network across the triac. The capacitor will then limit the rate of change of voltage across the triac. The resistor is necessary to limit the surge of current from the capacitor when the triac fires and to damp the resonance of the capacitor with the load and circuit inductance.

5.7 TEMPERATURE COMPENSATION PCBA

The Temperature Compensation PCBA is installed in 200 tpi D3000 Disk Drives. The PCBA is located adjacent to the Read/Write PCBA and is approximately 203.2 mm (8 inches) long by 101.6 mm (4 inches) high. The Temperature Compensation PCBA operates in conjunction with one externally mounted termistor to provide thermal compensation to 200 tpi models. Refer to Schematic No. 103976 (sheet 3 only) and Assembly No. 103977.

Figure 5-8 illustrates the placement of the five molex connectors located on the Temperature Compensation PCBA. These connectors provide power to the PCBA in addition to providing input and output signal paths between this PCBA and the Logic PCBA, the Servo PCBA, and the externally mounted thermister. Refer to Schematic No. 103976 (sheet 3 only) for the following discussion.

Capacitors C1, C2 (zone E7), and C4, C5, C6, C7 (zone H7) are employed for power supply decoupling. The internal temperature sensing thermister, RT2, is mounted on the positioner baseplate and is connected to the input of amplifier U6 (zone C7) via pin 1 of J505. R12 is used for linearization of the input; R13, R14, and R15 are used for scaling the closed-loop gain of U6 as monitored at TP3.

The output of amplifier U6 (zone C7) is applied to pin 2 of amplifier U8 (zone C6). The second input to U8 is applied to pin 3 and is provided from R16. U8 is a X1 gain difference amplifier whose output is proportional to the difference between the output of U6 and the reference voltage generated from R16.

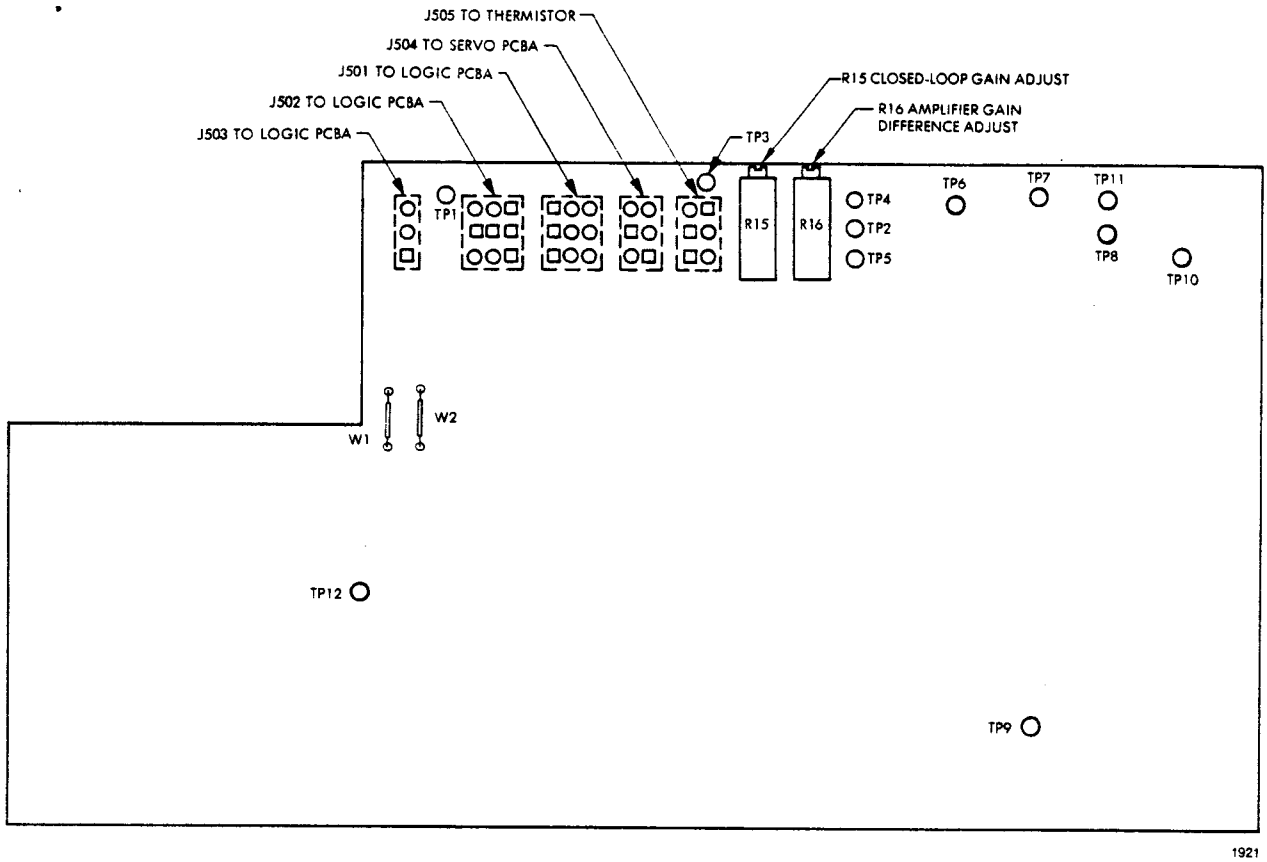

Figure 5-8. Temperature Compensation PCBA, Test Point and Connector Placement

The output of amplifier U8 (TP2) (zone C6) also drives a multiplexer digital-to-analog converter. This multiplexer digital-to-analog converter consists of FETs Q4, Q5, Q6 (zone D6) and amplifier U7 and U9 as well as the associated computing resistors R4, R5, R6, R21, R22, R23, R24, and R25. The switched current resistors (R4, R5, R6) receive their commands from the current address counter on the logic card via J503 (zone D, E-8). The three most significant bits are employed to provide off-track compensation and are comprised of LCAE1, LCA71, LCA61, in order of declining bit weight. These signals are buffered by U1 and U2 and applied to transistors Q1, Q2, and Q3. These transistors translate their input levels to output levels which are compatible with the FET switches Q4, Q5, Q6. The outputs of the multiplexer digital-to-analog converters are applied to the servo summing junction (pin 2 of U7), then through U7 to R26 and pin 1 of J504.

In addition to the temperature compensation electronics, the Temperature Compensation PCBA contains a time delay circuit. This circuit consists of a monolithic timer, U5 (zone B6), a 4-bit binary counter, U3 (zone B5), and associated components. Transistor Q7 resets the timer. When Q7 is turned off, the timer will *free run*, generating one pulse per 24 seconds as determined by R27, R28, R29, and C3. The binary counter is clocked by each pulse and counts thirteen of these pulses before an output is delivered at J502-9 (zone A3). This 5.2-minute timer circuit allows the internal temperature of the disk drive to near stabilization before a Temperature GO signal is generated at the interface. The timer circuit operates after the completion of the start-up sequence, or 57 seconds after the RUN/STOP switch is depressed. (R38 is used for reducing testing time only.)