SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section provides a description of the D3000 Disk Drive theory of operation.

The disk drive consists of the mechanical and electrical components necessary to read and record digital data on a magnetic disk. The disk drive consists of the following major groups.

(1) Main chassis group
(2) Positioner assembly
(3) Power supply assembly
(4) Read/Write PCBA
(5) Servo PCBA
(6) Logic PCBA
(7) Temperature Compensation PCBA (200 tpi)

4.2 ORGANIZATION OF THE DISK DRIVE

Figure 4-1 is a block diagram illustrating the overall organization of the disk drive. This organization can be subdivided into the mechanical and the electrical/electronics group. The mechanical group can be further divided into the main chassis group and the positioner assembly group.

4.2.1 MAIN CHASSIS GROUP

The main chassis group consists of the following components and assemblies.

(1) Base casting
(2) Air system filter and blower
(3) Spindle assembly
(4) Drive motor
(5) Drive train components
(6) Cartridge adapter (top load models)
(7) Receiver assembly (front load models)
(8) Disk cover (top load models)
(9) Lower disk cover (front load models)
(10) Bezel assembly
(11) Dust cover
(12) Control switch and indicator group

The main mechanical element of the disk drive is the base casting. This casting is a machined aluminum alloy casting which is the supporting structure for all of the components in the disk drive. When rack mounting the disk drive, the rack mounting slides are mounted directly to the sides of the base casting. This provides a means of sliding the unit in and out of rack installations.

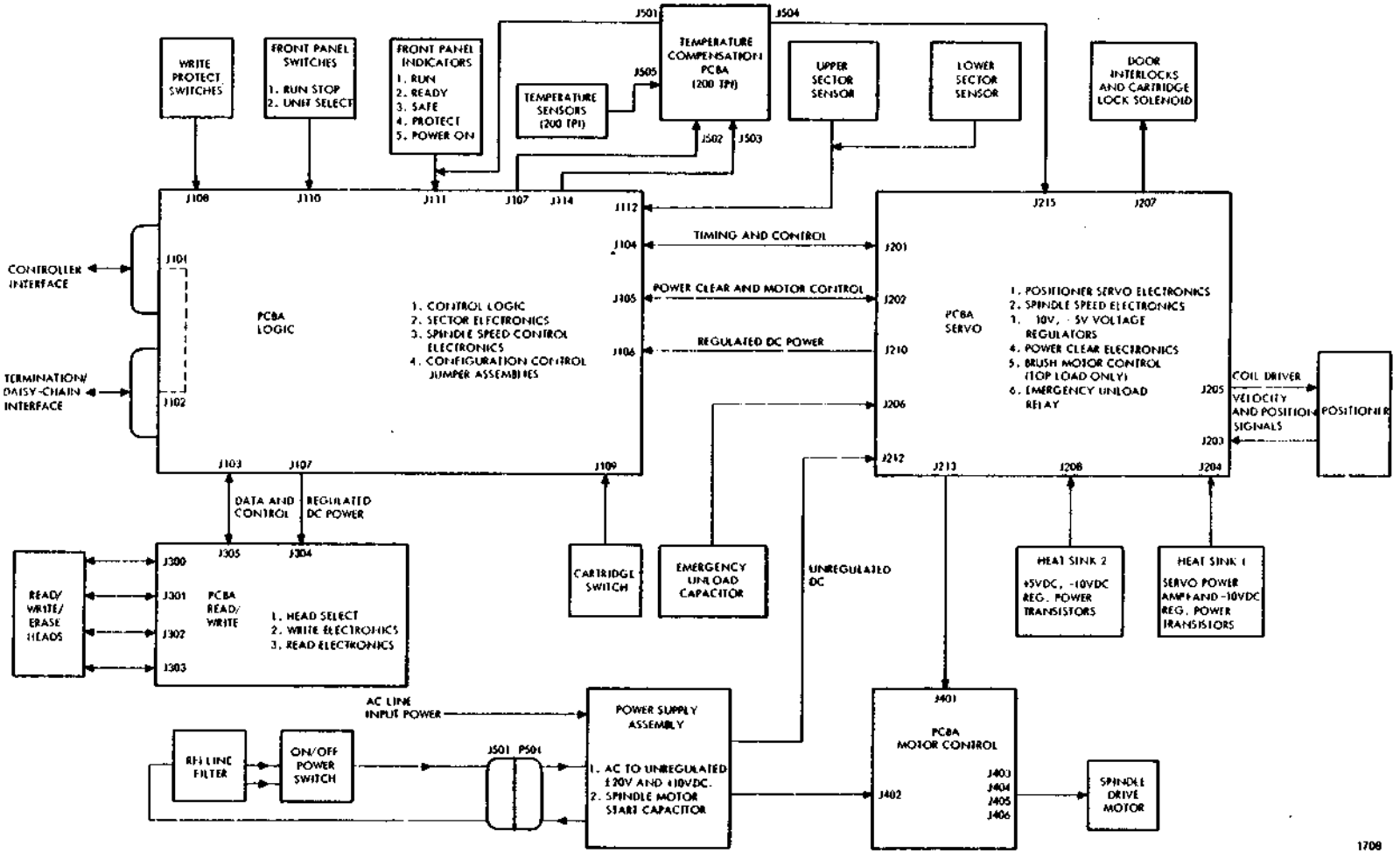


Figure 4-1. D3000 Disk Drive Organization

The absolute filter and high efficiency blower are components of the air system and are mounted into the base casting. In addition, duct work, either integral with the base casting or formed by suitable cover plates, provides the means for channeling the filtered air into the area of the disk and heads. The air system provides a highly filtered air flow into the area of the disks and disk cartridge. Operational characteristics of the *flying head* type of magnetic head employed in the disk drive require that the air bearing formed between the head and the disk surface be relatively free of particle contamination. Therefore, the filtered air flow provided by the air system causes a continual flow of clean air to purge this area of the disks and ensure correct operation of this air bearing. The air cushion which causes the heads to fly above the surface of the disk is dependent only upon the surface velocity of the disk and not upon the air flow through the filter.

The spindle assembly mounts into the base casting and provides the central axis of rotation for the disks. This spindle is a precision machined assembly utilizing ball bearings which are pre-loaded to provide a runout of less than several hundred micro inches. The assembly contains the phase lock ring which is used for sectoring the lower disk and for the spindle speed control. It also provides a mounting location for the lower disk in dual disk drives. A permanent magnet clutch, used to engage the hub of the removable cartridge, is mounted on top of the spindle hub. A precision ground cone is also on the top of the spindle hub to accurately center the cartridge hub. The hub of the spindle assembly acts as an air pump to pump the filtered air into the area of the cartridge.

The drive motor is mounted on a mounting plate which, in turn, is mounted to the base casting. The drive motor provides the power to rotate the disks at the prescribed speed and drive the blower in the air system. This motor is a multiple winding, permanent split phase induction motor which is used to drive the spindle and the blower through a belt drive system. The drive train components consist of the pulleys at the spindle, the blower shaft, the motor, and the tension idler. The necessity of having a belt tension adjustment is avoided by spring-loading the tension idler to maintain a constant belt tension.

The design of the D3000 disk drive provides maximum commonality of mechanical components between top load and front load models. The major difference between top load and front load machines is in that area which receives or adapts the cartridge to the disk drive.

In top load models, the cartridge adapter is a machined aluminum alloy casting which mounts to the top of the base casting. Mounted on this adapter is the cartridge lock mechanism with an arm that pivots out over the top of the cartridge dust cover. The position of this arm is sensed with a snap-action switch. The arm can be locked or unlocked by a solenoid arrangement fitted to the adapter. Also mounted on the adapter are booms for supporting the magnetic transducers.

In front load models, a receiver assembly is fitted to the top of the base casting and is pivoted from supports attached to the base casting. This arrangement provides a mechanism for properly locating the cartridge into the disk drive. It is also the mechanism for disengaging the cartridge hub from the magnetic clutch on the spindle. A link arm which is integral with the bezel assembly provides the camming action to disengage the cartridge hub from the magnetic clutch.

Also, on front load models, a lower disk cover is fitted which supports the magnetic transducer and photo-electric sensor pickups and provides a covering for the lower disk in dual disk machines. The analogous component in top load models is the disk cover which is an aluminum alloy separator mounted in the cartridge adapter, just above the lower disk area. The bezel assembly provides the decorative trim at the front of the disk drive and a suitable cover for the air system intake. In addition, for front load models only, the mounting arrangement for the door and the link arms provide the camming action for the receiver.

A dust cover, consisting of formed metal, is used to cover the disk drive and protect it from contamination. This cover is held in place by machine screws on both top and front load models. The cover directs the air flow through the interior of the drive.

The ON/OFF power switch, RUN/STOP switch, and the indicators are mounted to the base casting by the use of a bracket located directly behind the bezel. The bezel, on top load models, may be removed without disturbing the operator switches or the wiring since there is no mechanical connection between the bezel and the switch bracket.

4.2.2 POSITIONER ASSEMBLY

The positioner assembly is a separate modular unit that is mounted on a base casting. Also mounted on the base casting are the positioner magnet structure, and the shaft for supporting the carriage. The carriage is supported on a bearing structure riding on this shaft. The read/write heads are mounted into the carriage.

Also attached to the carriage is the positioner coil. This arrangement of magnet and coil provide a linear motor actuator for positioning the read/write heads. This type of arrangement is also referred to as a voice coil positioner. Carriage velocity is sensed using a velocity transducer consisting of a magnet within a specially wound coil. The transducer is mounted on the positioner base plate and the magnet is attached to a shaft connected to the carriage. The position of the carriage is detected and sensed using a photoelectric position transducer which is attached to the positioner base plate by a mounting strip.

The 200 tpi models have a temperature sensing element mounted on the positioner base plate. This thermistor is part of the temperature compensation circuitry included in 200 tpi models.

4.2.3 POWER SUPPLY ASSEMBLY

The power supply assembly is a major subassembly which mounts to the underside of the base casting and contains the power transformer, rectifiers, and filter capacitors. Also located on the power supply assembly is the Motor Control PCBA and the motor start capacitors.

4.2.4 READ/WRITE, SERVO, AND LOGIC PCBAS

The partitioning of the electronics system is primarily functional; the three major PCBAs, in many ways, constitute the major partitioning of the D3000 electronics. These PCBAs are the Read/Write PCBA, the Servo PCBA, and the Logic PCBA. In addition to the functional descriptions contained in this section, detailed descriptions of these PCBAs are contained in Section V.

The electrical and electronic components comprising the main chassis group, the positioner assembly, and the power supply chassis are interconnected with the PCBAs through use of interconnecting cable assemblies. The Read/Write PCBA is located adjacent to the positioner assembly and the head cables connect directly to this board. The Read/Write PCBA is constrained by self-locking card guides. The Logic PCBA is mounted on pivoting supports which are directly mounted to the base casting. Hinged on the face of the Logic PCBA is the Servo PCBA; these PCBAs are interconnected by interboard flat cables.

4.2.5 TEMPERATURE COMPENSATION PCBA (200 TPI MODELS)

The temperature compensation assembly, which is included in 200 tpi models, is comprised of a Temperature Compensation PCBA and a thermistor assembly. The thermistor assembly is mounted on the positioner base plate.

4.3 FUNCTIONAL SUBSYSTEMS

The major functional groups of the disk drive are illustrated in Figure 1-4; these major groups, functionally discussed in the following paragraphs, are:

(1) Positioner and Positioner Electronics
(2) Read/Write Electronics
(3) Disk Drive Function Control
(4) Spindle Speed Control
(5) Position Control Logic
(6) Sector Electronics
(7) Motor Control
(8) Power Supply
(9) Temperature Compensation

4.4 POSITIONER AND POSITIONER ELECTRONICS

An essential function in a moving head disk drive is the positioning of the read/write head at the correct cylinder. This is accomplished in the D3000 Disk Drive by the Positioner Servo Electronics and the Positioner Assembly.

4.4.1 POSITIONER ASSEMBLY

The Positioner Coil and Moving Mass (linear motor), Velocity Transducer, and Position Transducer are the three major functional entities which comprise the Positioner Assembly. Figure 4-2* shows the relationship of these subsystems to the Positioner Servo Analog Circuits and the Positioner Control Logic.

The linear motor consists of a stationary permanent magnet and a positioner coil attached to the moving-mass, i.e., the carriage and magnetic head assembly. A description of the physical arrangement of the Positioner is contained in Paragraph 4.2.2.

*Foldout drawing, see end of this section.

Functionally, the magnet structure and the ways that the carriage rides on are the stationary portion of the linear motor. The moving structure consists of the carriage, the positioner coil, the heads mounted into the carriage, the bearings which support the carriage on the ways, and the moving portions of the Velocity Transducer and the Position Transducer. The force that is necessary to move the moving-mass portion of the Positioner is a function of the interreaction of the magnetic fields produced by the permanent magnet structure and the magnetic field resulting from the current in the positioner coil. This force may be used for purposes of accelerating or decelerating the moving-mass, or as a restoring force for the purposes of holding the moving-mass in a given position. To a first approximation, the force developed is proportional to the current in the positioner coil.

The Velocity Transducer provides an electrical signal that is proportional to the velocity of the moving-mass and consists of a permanent magnet moving inside of the specially wound coil. This coil is attached to the positioner baseplate and is stationary; the magnet is mounted on a shaft which is attached to the carriage. The amplitude of the signal derived from the Velocity Transducer is approximately equal to the actual moving-mass velocity. The magnitude of this signal is indicative of the speed of the mass and its polarity indicates the algebraic sign of the velocity.

The Position Transducer is a photoelectric sensor that develops four electrical signals, each serving a specific function for use in controlling the positioner. An incandescent lamp, mounted in the position transducer body, supplies illumination to a group of photodiodes located opposite the lamp and within the body of the Position Transducer. The transducer body is mounted stationary to the positioner baseplate by the use of a mounting strip.

Attached to the carriage is a precision scale which is part of the moving-mass. This scale is interposed between the lamp and the photodiode and consists of opaque and transparent areas in specific patterns. Also interposed between the scale and the photodiodes is a precision reticle which is also made up of opaque and transparent areas in specific patterns. The combination of the reticle patterns and the scale patterns are used to control the amount of illumination reaching the photodiode group.

Two of the signals developed by the Position Transducer as a function of carriage position are level change type of signals. One signal, the Heads Retracted signal, changes state when the carriage is approximately ¼-inch from the fully retracted position and is used to indicate the gross carriage position, specifically, the retracted position of the heads. The other signal is the Position Transducer Index signal which is used to define the legal range of the carriage position. This signal is a multi-change-of-state signal. One of the transitions of this signal is used in the initialization process during a head loading operation.

The other two signals derived from the Position Transducer are referred to as X + 0 and X + 90. These signals are linear signals that are cyclic as a function of cylinder position, and bi-polar in terms of polarity. They are displaced in electrical phase by approximately 90 degrees.

All of the signals from the Position Transducer are current signals proportional in amplitude to the illumination of the specific photodiode associated with that signal. The X + 0 and X + 90 signals are actually derived from photodiode pairs rather than a single photodiode.

4.4.2 POSITIONER ELECTRONICS

The Positioner Electronics consists of two major groups; the Position Control Logic and the Positioner Servo Analog Circuitry. The relationship of these subsystems to the Linear Motor, Velocity Transducer, and Position Transducer is shown in Figure 4-2. The entire arrangement comprises a servo mechanism whose purpose is to control the mechanical position of the carriage and, hence, the position of the heads or a time derivative of carriage position such as the carriage velocity.

The servo mechanism may be operated in one of two modes, a Position Mode where the position of the carriage is controlled, or the Velocity Mode where the velocity of the carriage is controlled. The servo is switched between Position Mode and Velocity Mode, or vice versa, by means of transistor switches which are controlled by the Position Control Logic. The Position Control Logic determines the specific mode of operation on the basis of commands input to it from the interface and the status of the signals derived from the Position Transducer.

Additionally, as shown in Figure 4-2, the Linear Motor can be disconnected from the servo and operated off the Emergency Unload Capacitor. This emergency unload system provides a means of independently supplying power to the Linear Motor during emergency situations. This network is independent of the servo electronics for purposes of high-speed retraction of the heads from the storage surface during emergencies. The Emergency Unload Relay acts as a double-pole, double-throw switch to connect the Positioner Coil to either the output of the Power Amplifier and the Current Sensor, or to the Emergency Unload system. It should be noted that when the positioner is executing an emergency unload, it is not operated as a servo and, therefore, functions in an open-loop manner.

The Emergency Unload Relay Driver receives its commands from the Logic PCBA via the Emergency Unload Enable (LEUEG) line. When the Emergency Unload Relay is energized, the positioner coil is connected to the servo; specifically, it is connected to the output of the Power Amplifier and to the Current Sensor. The Power Amplifier, in conjunction with this Current Sensor, forms a voltage-to-current converter providing a current in the positioner coil that is proportional to the applied input voltage to the Power Amplifier. As previously mentioned, the available force for moving the carriage is proportional to the positioner coil current to a first approximation, and the Power Amplifier, being a voltage-to-current converter, provides a current that is proportional to its input voltage.

Therefore, the output of the Summing Amplifier, which is the input to the Power Amplifier, determines the force applied to the carriage where the force is approximately proportional to the output voltage of the Summing Amplifier.

The Summing Amplifier input is the major summing junction of the servo. Applied to this Summing Amplifier are the servo commands and the feedback which nulls these commands. Therefore, the servo loop functions to reduce the voltage at the Summing Amplifier input by providing an output voltage which results in a feedback signal which nulls the command signal. Additionally, on 200 tpi models, a temperature compensation signal is applied to this summing junction.

One of the input commands to the Summing Amplifier is the velocity reference. The velocity reference command is a request for a specific velocity when the loop is operating in the fast velocity mode. This velocity reference is derived from the Velocity Function Generator. The polarity of this reference is determined by the Polarity Select Network and is applied to the input of the Summing Amplifier through a transistor switch. The Polarity Select Network consists of U9, Q2, and transistor switch Q3, located on the Servo PCBA (Schematic No. 102810).

The Velocity Function Generator is a digital-to-analog converter which has a single polarity output. The address difference input is a digital signal that is the binary representation of the difference between the demand address from the interface and the current address defining the current positioner position. The output of the Velocity Function Generator is an analog voltage representative of the address difference. Therefore, the specific velocity requested is a function of the distance to be traveled in achieving the demand address.

The address difference is specified on the Address Difference lines in binary form where NLAD0G is the least significant bit and NLADEG is the most significant bit. The decimal address difference number may be expressed as the sum of the active bit weights. Each address difference being assigned a specific bit weight. The bit weights are ascending powers of two, where bit number 0 is decimal bit weight number 1; bit number 1 is decimal bit weight number 2; bit number 2 is decimal bit weight number 4, etc., to the extension bit number where the bit weight is 256. The address difference as specified on the Address Difference lines determines the magnitude of the velocity reference generated by the Velocity Function Generator.

Referring to the Servo Board Schematic No. 102810, it can be seen that the Velocity Function Generator portion of the velocity function decoder/encoder consists of U12C, U12B, U5B, U5A, U4C, U5C, U4B, U5D, U4D, U3D, U4A, U3C, U4E, U3B, U4F, U3A. The remainder of the Velocity Function Generator is the digital-to-analog conversion arrangement consisting of a resistor network, a current-to-voltage converter, and diode switches. The purpose of this arrangement is to take the digital signal encoded by the velocity function decoder/encoder and convert it into a current of a specific value which is then applied to the current-to-voltage converter. The summing junction of U8 (located on the Servo PCBA) functions as a current-to-voltage converter producing a voltage level which is determined by the address difference value. The resistor network is R1, R2, R7, R8, R10, R11, R16, R17, R18, R19, R20, R21, R24, R25. The diode switches are CR1 through CR12. The current-to-voltage converter consists of U8 in conjunction with Q1.

Referring to Figure 4-2, the output magnitude of the Velocity Function Generator is the velocity reference which is utilized during seeks. This reference is determined by the address difference value. The polarity of the velocity reference which determines the direction of the velocity is controlled by the Polarity Select Network. The Polarity Select Network in turn is controlled by the Forward Direction (LFDX1) line from the Position Control Logic. The Transistor Switch, which switches the velocity reference to the Summing Amplifier, is controlled by the Velocity Reference Enable (NLVREG) line from the Position Control Logic. When the positioner is executing a high-speed seek and is not operating as a position servo, the Velocity Reference Enable (NLVREG) line will be active, thereby switching to the velocity reference from the Velocity Function Generator.

Other commands which may be applied to the input of the Summing Amplifier are for controlling the positioner in the Slow Velocity mode, i.e., during loading and unloading of the heads. The Slow Velocity mode is also used when executing a Restore operation. The Slow Velocity mode is determined by a velocity reference in the Mode Control Circuits, which in turn are controlled by two logic signals, Forward Slow Mode (NLFSM1) and Reverse Slow Mode (NLRSM1).

The two slow mode control signals, NLFSM1 and NLRSM1, are developed by the Position Control Logic and control transistor switches in the Mode Control Circuits which establish the Slow Mode velocity reference. Transistor switch Q7, in conjunction with R44, CR21, R45, and R46 on the Servo PCBA, are used for switching and determining the level of the Forward Slow Mode velocity reference.

It should be noted that the polarity of the reference, and hence the direction of motion, is determined by the power supply voltage in the particular circuit. Likewise, Q8, in conjunction with R49, CR25, and R50, R46, determine the Reverse Slow Mode velocity reference.

Additionally, command signals Track Offset Plus (NLTOPG) and Track Offset Minus (NLTOMG) from the Position Control Logic can be used to determine position mode offset through use of position reference voltages derived in the Mode Control Circuits. The track offset function is employed in the position mode for diagnostic purposes. The two logic signals, Track Offset Plus (NLTOPG) and Track Offset Minus (NLTOMG) operate transistor switches in the Mode Control Circuits to generate a position mode reference, thereby offsetting the heads from the nominal track cenerline.

Referring to the Servo Board Schematic No. 102810, it can be seen that NLTOPG controls transistor switch Q5 which, in conjunction with R33, CR15, R34, and R35, determines the magnitude of the Track Offset Plus position reference. Likewise, Track Offset Minus controls transistor switch Q6 which, in conjunction with R38, CR19, R39 and R35, determines the Track Offset Minus position reference.

In addition to the commands controlled by logic signals that may be input to the main summing junction, an offset correction may be introduced by the Servo Offset Adjust, R22, on the Servo PCBA. There is also an external input test point provided to enable the introduction of external test signals into the summing amplifier. TP19 and R40 on the Servo PCBA perform this function.

Two separate and distinct feedback paths to the main summing junction are provided. One of these feedback loops is closed at all times when the servo is energized. This path, as shown in Figure 4-2, is from the Velocity Transducer, through the Velocity Transducer Amplifier, to the Summing Amplifier input. The Velocity Transducer Amplifier merely amplifies the low level signal from the Velocity Transducer to a high level signal that is proportional to the velocity of the carriage. Since this feedback path is closed at all times, a damping in the Position mode of operation is provided. In the Velocity mode, this feedback nulls velocity commands.

The other feedback path is used only in the Position mode. This path takes the X + 0 signal from the Position Transducer, conditions it to a voltage signal in the Position Transducer Amplifier, and then switches it to the Summing Amplifier input. The transistor switch Q13 on the Servo PCBA performs the switching function and is controlled by the Position Mode signal (LPMXG) from the Position Control Logic.

As previously discussed, four signals are provided to the Position Control Logic which are derived from Position Transducer signals. These four signals are the X + 0, X + 90, Heads Retracted, and Position Transducer Index. They are converted from current signals into voltage signals by current-to-voltage converters that are contained in the Position Transducer Amplifiers. These current-to-voltage converters are U1, U6, U2, and U7 located on the Servo PCBA.

Since the output of the Position Transducer Amplifiers is an analog voltage and therefore unsuitable for direct application to logic, they are converted into digital signals by analog-to-digital converters. These converters are, in essence, a special type of Schmitt trigger and are comprised of U11 and U10 on the Servo PCBA. The signals which are fed back to the Position Control Logic are: Position Reference Clock (SPRCG), Position Quadrature Clock (SPQCG), Heads Retracted (SHRXG), and Position Transducer Index (SPTIG). These signals are utilized by the position control logic to determine the operation of the positioner servo in conjunction with commands from other parts of the logic and the I/O interface.

Additionally, failure of the lamp in the Position Transducer is detected by the Lamp Failure Detector. A signal derived from this detector is fed back to the Position Control Logic for purposes of determining when an emergency condition exists. This signal is Position Transducer Failure (SPTFG).

4.5 READ/WRITE OPERATIONS

A double frequency recording method is used in the D3000 Disk Drive. Read/Write operations are accomplished by a read/write head. During a write operation, a bit is recorded on the disk whenever the coils of the read/write head are switched by the Write Driver circuits. During a read operation, a clock or data bit is sensed on the disk whenever the flux direction induced in the coil winding is reversed as a result of a change in polarity of the flux pattern presently passing under the head gap.

The recording head is a split-ring core containing coil windings so that a magnetic field with a given flux direction prevails at the core gap while the coil is energized. When current flows through the coil, the flux induced in the core establishes a fringe flux at the gap. As a magnetic recording surface passes by the gap, the fringe flux magnetizes the surface of the disk.

During a write operation, a bit is recorded when the flux direction in the core is reversed by switching between coils of the read/write head. The fringe flux is reversed at the gap and, hence, the portion of the flux flowing through the recording medium is reversed. If the flux reversal is considered instantaneous in comparison to the motion of the recording surface, and the gap is observed at the moment of reversal, it can be seen that the portion of the surface that just passed the gap is magnetized in one horizontal direction while the portion directly under the gap is magnetized in the opposite direction. Between these two areas, the flux must reverse 180 degrees; this recorded flux reversal represents a bit.

During a read operation, the gap first passes over an area that is magnetized in one horizontal direction, and a constant flux is induced into the core and the coil. The coil provides no instantaneous output voltage for this condition. However, when the recorded bit (180 degrees horizontal flux reversal) passes the gap, the flux induced into the core and coil must go through a 180-degree reversal. This reversal means that the coil sees a change in flux which results in a voltage output pulse.

A basic clock frequency signal is encoded in the data pulses to produce a single composite signal at the read/write head. The composite signal represents either a logic zero bit condition or a logic one bit condition for each bit-cell time defined by the clock.

Figure 4-3 illustrates the use of a clock frequency to establish the basic bit-cell timing cycle. The insertion of a data pulse between clock pulses in a bit-cell period produces a composite read/write signal which uses only clock pulses for a logic zero bit indication, and data pulses for a logic one bit indication. A zero bit-cell (clock pulses only) produces a single change in direction of the flux pattern. A one bit-cell (data pulse located between two clock pulses) produces a double change in direction of the flux pattern. In either case, the clock signal causes a change in direction of magnetism from plus to minus or minus to plus polarity, thus causing the storage of a bit. Because both clock and data information are synchronized on a composite signal, double frequency recording is sometimes referred to as *self-clocking*.

In double-frequency recording, a clock bit is always inserted at the beginning of each bit-cell time to establish the basic recording frequency. A data bit is inserted between clock bits (at twice the frequency) so that the data bit results in two flux reversals within a single bit-cell time. If the data bit is not present, a single flux reversal occurs in a bit-cell time.

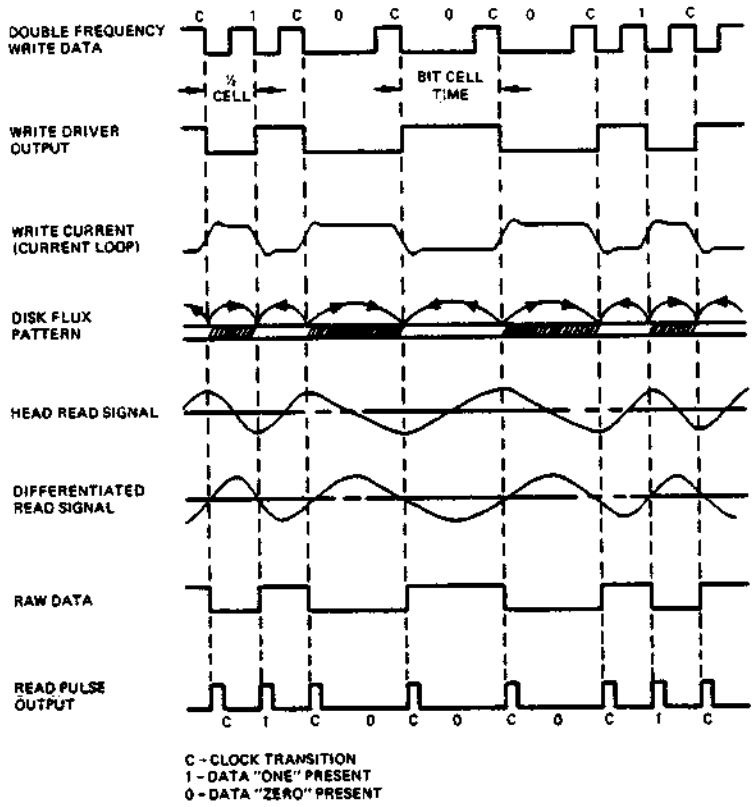


Figure 4-3. Double Frequency Recording Flux and Pulse Relationship

4.6 READ/WRITE ELECTRONICS

The Read/Write electronics are contained on a single PCBA. Figure 4-4* is a functional block diagram of the D3000 Read/Write system and should be referred to for the following discussion.

4.6.1 HEAD SELECT

Head selection in the D3000 is accomplished by signals from the using system via the Platter Select (IPXSR) and Head Select (IHSXR) I/O interface lines. The signals on these lines are required to select one of four read/write heads. Table 3-1 shows the head select decoding used in the D3000 Disk Drive.

4.6.2 WRITE ELECTRONICS

Information to be recorded is supplied to the disk drive via the Write Data Signal (IWDSR) I/O interface line. The writing process is under complete control of the logic functions and control circuitry (Paragraph 4.7). Verification of system readiness, a software function, is required prior to initiation of a write operation. The conditions that must be satisfied before a write operation can be performed are:

(1) The unit must be in the Ready condition and Selected. This implies that only one head is selected.

(2) The heads must be positioned over a legal track address.

(3) The WRITE PROTECT switch for the disk selected is switched to the OFF position and the Power Clear signal is at a high level.

*Foldout drawing, see end of this section.

The disk drive is conditioned to perform a write operation when the Write Enable (IWEXR) line is low. At this time the Write drivers are receptive to Write Data pulses. When the Write Enable line is active and system readiness is satisfied, current flows through the write coil recording new data and causing all previous data to be overwritten, i.e., obliterated.

The read/write coil is a split center-tapped winding. During a write operation, current flows in alternate halves of the read/write coil. Switching of write current in each half leg causes magnetic flux reversals on the disk surface. It is important to note that when the disk drive is in the Write mode, the erase coil is also energized. The read/write gap is located in front of the erase gaps in both 100 and 200 tpi models. In 100 tpi models the alternating write flux pattern magnetizes a band approximately 0.1905 mm (0.0075 inch) wide on the surface of the disk; in 200 tpi models the magnetized band is approximately 0.10 mm (0.004 inch) wide. The erase gaps, which straddle the read/write gap, erase part of the write flux pattern leaving a recorded band that is approximately 0.1651 mm (0.0065 inch) wide for 100 tpi models and approximately 0.0914 mm (0.0036 inch) wide for 200 tpi models. This provides a signal guard-band between adjacent tracks.

4.6.2.1 Write Encoder and Driver

The Write Driver circuitry, shown in Figure 4-4, switches the write current to alternate halves of the read/write head winding. The rate at which the write current is switched is determined by the write Double Frequency (NLWDFT) signal from the Logic PCBA. NLWDFT toggles a flip-flop whose outputs drive two write current control switching transistors into alternately conducting states. The write current drivers are enabled by a low logic level input on the Write Mode (NLWMXG) line at the Read/Write PCBA.

4.6.2.2 Erase Driver

The Erase Driver circuit is a transistor switch current source that is energized by the Erase Current Enable (NLECEG) signal input to the Read/Write PCBA. A low logic level at the NLECEG input enables the erase current to flow into the read/write head erase windings.

4.6.2.3 Write Current Control

The write current control causes the current level in the read/write coils to change as a function of the positioner cylinder address. In 100 tpi models, for cylinder addresses of 0 through 127, the current level is set at approximately 35 ma; at cylinder address 128 and above, the current level is reduced to approximately 27 ma. This current level change is required because of the increased bit density at the innermost tracks on the disk surface. The lower write current levels reduce the flux pattern fringe effects on neighboring bits. It is important to note that in 200 tpi models the write currents are slightly different than those given for 100 tpi models and the lower current level is switched at cylinder address 256.

4.6.2.4 Write Emergency Monitor

This circuitry continuously monitors the legality of conditions within the read/write system. If conditions are improper, the write emergency monitor outputs an active high logic level to the emergency unload circuitry on the Logic PCBA. This causes the disk drive to execute an emergency unload operation. Conditions that would cause a read/write emergency unload operation are:

(1) More than one head is selected at one time.

(2) The current monitor circuitry indicates the presence of a current in either the write or erase circuits when such a current is not enabled by NLWMXG and/or NLECEG.

4.6.2.5 Current Monitor

The current monitor circuitry continuously checks the current outputs at a low logic level to the write emergency circuitry during a write/erase operation. When both the Write Mode and Erase Current Enable lines are at a high logic level, the write emergency circuitry assumes that a read operation is in progress and looks for a high logic level from the current monitor. Should the output of the current monitor be a low logic level at this time, the write emergency monitor will sense an illegal condition and cause the system to perform an emergency unload.

In addition to the current monitoring function, the current monitor circuitry can disable the flow of write or erase currents to the read/write heads. The Power Clear signal (SPCSA) generated on the Servo PCBA indicates the status of the regulated dc voltages and controls a transistor switch in series with the common write/erase current path. In case of a power failure, SPCSA goes to a low level, causing the transistor switch to open the write/erase current line. This action prevents the writing of erroneous information on the disk surface during a power failure emergency unload condition.

4.6.3 READ ELECTRONICS

A Read Enable (IREXR) signal from the system I/O interface conditions the Read/Write circuitry to perform a read operation. Certain readiness checks must be performed by the disk drive Function Control Logic circuitry before information can be transferred from the surface of the disk to the system I/O interface. The selected disk drive must be in the Ready condition; this implies that the following conditions exist:

(1) The heads are positioned over a legal track address.

(2) Only one head is selected.

(3) The Write Enable and Erase Current Enable lines are both high and the current monitor senses no write or erase current flow.

The Read Electronics are activated when both the Write Mode and Erase Current Enable inputs to the Read/Write PCBA are at a high level. This condition is locally ANDed resulting in the Read/Write head windings being connected to the read preamplifier. The amplifier read data are filtered, peak detected, digitized, and decoded before being suitable for transmission to the using system interface. When the Read Enable Control (NLRECG) signal to the Read/Write PCBA goes low, the Read Data (IRDXR) and Read Clocks (IRCXD) are gated onto the system I/O interface lines. A detailed discussion of the Read Electronics portion of Figure 4-4 is contained in the following paragraphs.

4.6.3.1 Head Switch Circuitry

The Head Switch circuitry disconnects the Read preamplifier signal inputs from the read/write heads during a write/erase operation. This is done to prevent the large voltage signal levels that are applied to the head's read/write windings during a write operation from entering the low level inputs of the read preamplifier. Thus, the Head Switch circuitry prevents the amplifier from being driven into saturation during a write operation.

4.6.3.2 Read Preamplifier

The Read Preamplifier is a single integrated circuit consisting of a wide band, linear differential amplifier stage. Read signals from the read/write heads are typically quasi-sinusoidal with typical amplitudes of approximately 1 mv to 5 mv. The nominal voltage gain of this amplifier is 50 in 100 tpi models and 150 in 200 tpi models; the read signal output has an amplitude of approximately 200 to 400 mv peak-to-peak. The amplifier gain is determined by a resistor of appropriate size across the gain-adjust terminals.

The amplified read signal is ac-coupled to a L-C filter stage which removes the undesirable high-frequency noise signals superimposed on the read signal. The special quality of the filter is its ability to pass the read signal with only small attenuation and negligible phase variation.

4.6.3.4 Variable Gain Amplifier

The filtered read signal is amplified by the Variable Gain Amplifier stage. This amplifier has a nominal voltage gain of approximately 7.3 under normal operating conditions; thus, the read signal output is normally 350 to 650 mv peak-to-peak. In the read margin test mode, the gain of the amplifier stage is reduced to approximately 2.6.

4.6.3.5 Peak Detector and Squarer

The 350 to 650 mv read signal drives a differentiating type peak detector which converts the sinusoidal read signal into digital data by switching its output voltage level at each positive and negative peak of the read data signal. The operation of the peak detector is illustrated in Figure 4-5.

The output voltage signal from the differentiator is a 1.2v peak-to-peak amplitude that swings +0.6v peak about a zero voltage reference. Prior to decoding, the read data are converted into a pulse train at a frequency that is twice the read data rate. The action of the double-frequency generator is shown in Figure 4-6. The pulsewidth of the signal is controlled by component values within the circuitry.

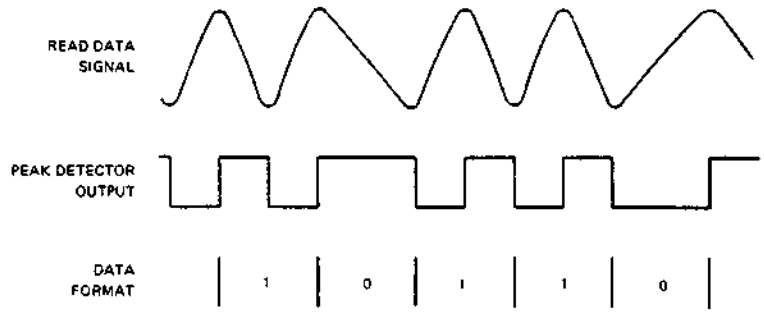


Figure 4-5. Peak Detector and Squarer Waveform

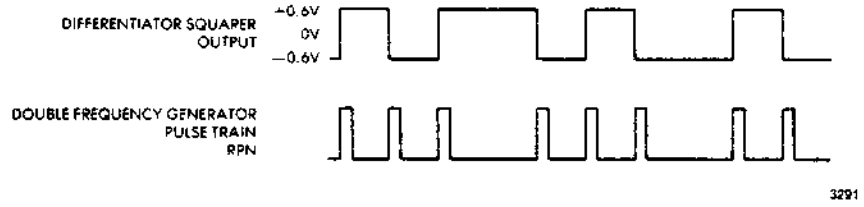


Figure 4-6. Double Frequency Generator Timing Relationship

4.6.3.6 Data Decoder Circuitry

The Data Decoder circuitry is essentially a data/clock separator. It is comprised of two one-shot multivibrators, a decoding window generator, and a window polarizing circuit. The Read Pulse Narrow (RPN) signal has a nominal data rate frequency when read data are all zeros, and is twice this frequency when read data are all ones. It is this characteristic that enables the Data Decoder circuitry to separate read data from the clocks.

The first RPN pulse is treated as a clock pulse. Its leading edge clocks the ones window one shot to look for a data bit. At the end of the one-shot timing, the ones gate is reset and the next RPN pulse is another clock pulse. If an RPN pulse is present between the clock pulses, it is treated as a data bit or a *one* bit and presented to the Read Data interface line. The *ones* data output repetition rate will therefore be at the read clock rate. The timing diagram shown in Figure 4-7 details these timing relationships. Two pulse former one-shots determine the output pulsewidth.

4.6.3.7 Read Data Control

The Read Data Control gates the Read Clocks and Read Data onto the system I/O interface lines, via line drivers on the Logic PCBA, in response to the Read Enable Control (NLRECG) signal. When Read Enable Control is initiated, the Read Clock and Read Data gate control is clocked to the enable state. This prevents pulse *shaving* of the Read Data and Read Clock signals.

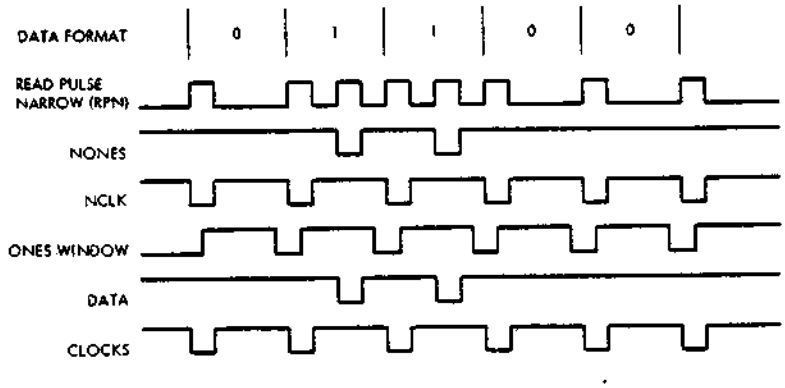


Figure 4-7. Data Decoder Timing Relationship

4.7 LOGIC FUNCTIONS AND CONTROL

There are five major areas in the D3000 Series Disk Drives which require logic for control of functions and timing, these are: Disk Drive Function Control, Read/Write Electronics, Spindle Speed Control Electronics, Position Control Electronics, and Sector Electronics. They are functionally shown in Figure 1-4. Since the majority of logic in the D3000 is packaged on the Logic PCBA, the following is primarily a functional description of the Logic PCBA. Only those areas on other circuit boards having logic functions of interest are included.

NOTE

In order to fully understand the logic functions described, the reader should acquaint himself with the discussion of the specific integrated circuits contained in Section V. He should also become familiar with the schematics contained in Section VII.

4.7.1 LOGIC ARRANGEMENT

The Logic PCBA is depicted on sheets 2 through 5 of Schematic No. 102830. These sheets have been divided on the basis of function and, therefore, a specific sheet is a complete (or nearly complete) schematic representation of a specific function. The following discussion identifies these functions by schematic sheet number.

4.7.1.1 Logic Schematic, Sheet Two

Sheet two of the Logic schematic contains the Start/Stop Control which is used in the control and timing process of executing the start cycle of the disk drive and for executing the stop cycle of the disk drive. Also shown on this sheet is the main clock generation circuitry which consists of the crystal oscillator, clock countdown and clock gating circuitry. This arrangement provides the reference for all timing functions on the Logic PCBA.

A subdivision of the Start/Stop Control is also included. This circuitry is used for the detection of run/stop commands, emergency and fault mode control, interlocking control, start cycle sequencing, stop cycle sequencing, and condition indication.

4.7.1.2 Logic Schematic, Sheet Three

Sheet three of the Logic schematic contains a number of minor functions; these are the select enable controls, the read outputs, the status outputs, the termination voltage power supply, and the spindle speed control digital logic.

A subdivision of the select function is the head and disk select control, track offset enable control, write/erase enable control, unit select decoding, busy signal encoding, write protection control, and the status and indication circuitry.

4.7.1.3 Logic Schematic, Sheet Four

The functions shown on sheet four of the Logic schematic deal entirely with position control; these are the demand address register, the valid address decoder, the current address counter, the count control, subtractor and complementor, carry control, the load address and illegal address control, busy logic, mode control, operation control, and error check logic.

4.7.1.4 Logic Schematic, Sheet Five

The functions shown on sheet five of the Logic schematic consist entirely of sector electronics. These functions consist of the upper sensor detector, the upper time demultiplexer, the lower sensor detector, lower time demultiplexer, sector phase lock loop, upper sector countdown, lower sector countdown, sector multiplexer, index multiplexer, sector pulse formers, index pulse formers, upper sector number counter, lower sector number counter, sector count multiplexer, and the multiplexer control.

4.7.2 DISK DRIVE FUNCTION CONTROL

The Disk Drive Function Control Logic is one of the major sub-divisions of the disk drive which require logic for the control of functions performed. Figure 1-4 is a functional block diagram of the D3000 Disk Drive and should be referred to in conjunction with the following paragraphs.

The major block identified as Disk Drive Function Control in Figure 1-4 can be sub-divided into two parts: a major block consisting of the Start/Stop Control, and a minor block containing minor control functions, e.g., head select control, unit select decoding. The following paragraphs contain a functional discussion of these blocks.

4.7.2.1 Start/Stop Control

Essentially, the Start/Stop Control is a digital sequential machine mechanized with integrated circuit logic. The purpose of this logic is to take external commands, combine them with internal conditions plus suitable timing, and generate output signals for control and indication purposes. Figure 4-8 is a block diagram of the digital sequential machine used to mechanize the start/stop control.

The three essential blocks, shown in Figure 4-8, are State Storage, Combinational Logic, and Delay Generator. The purpose of the State Storage block is to store the machine states, This is mechanized with flip-flops and a counter. The present states are combined in the Combinational Logic with external commands which allows the generation of output signals for indication and control by the output signal combinational logic. All of the combinational logic is mechanized with gates. It should be noted that external commands can modify directly the stored states. This is in addition to the capability of external commands in combination with the present states to provide output signals and modification of the stored states.

Included in the block diagram is a Delay Generator which is mechanized with counters and a flip-flop. The generator provides specific delays under control of certain of the Combinational Logic output signals. The Time Reference to the Delay Generator is obtained from a crystal oscillator and clock countdown circuits.

Figure 4-9* is a functional block diagram of the Start/Stop Control. All of the logic depicted in this figure is contained on sheet two of the Logic PCBA schematic. The time reference for this arrangement is provided by a Crystal Oscillator whose output signal is frequency divided by the Clock Countdown circuitry. This circuitry consists of a series chain of counters that generate clock signals that are used by the Start/Stop Control logic. These clock frequencies are also used in other portions of the disk drive logic.

Within the Start/Stop Control, gating of the clock signals is accomplished by allowing clock pulses to be fed to the flip-flops only at specific times, thereby permitting these flip-flops to change state only when a clock pulse is present. The delay generation portion

*Foldout drawing, see end of this section.

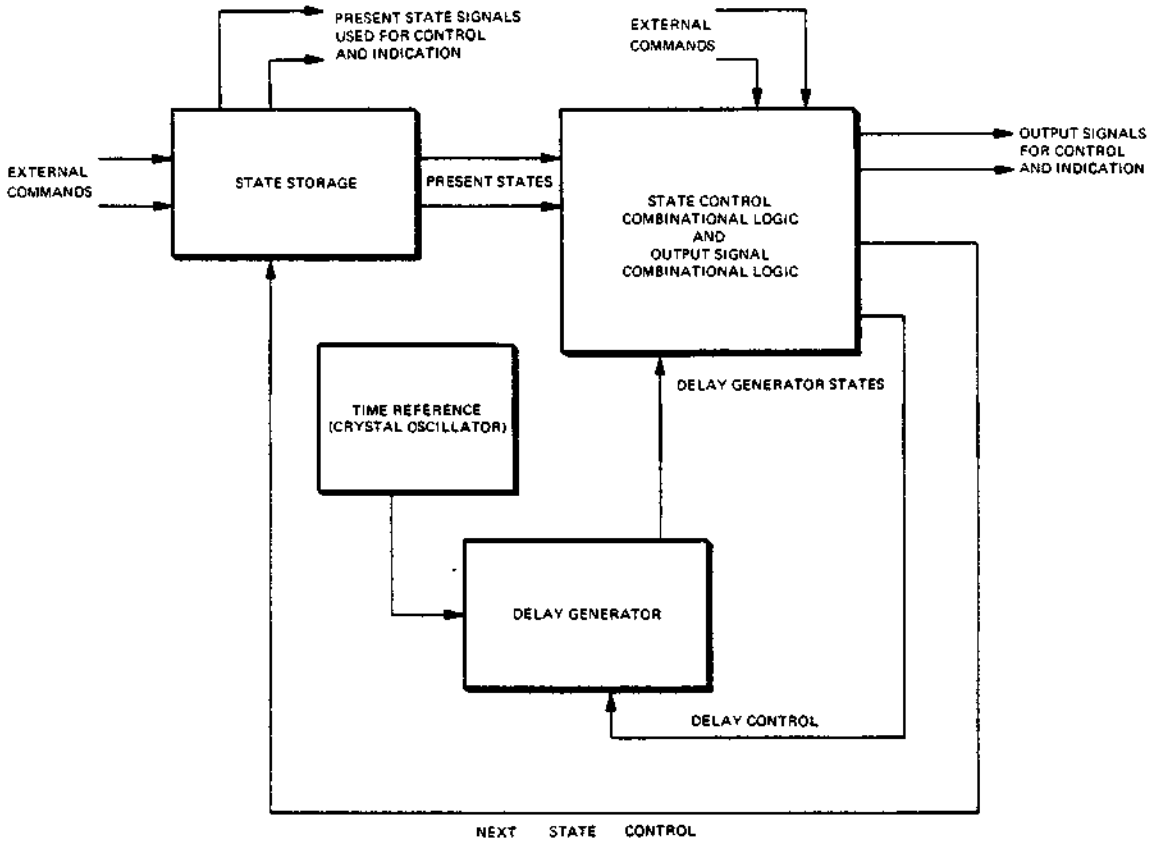


Figure 4-8. Digital Sequential Machine Block Diagram

of Start/Stop Control is handled by a Delay Counter which is operated from a clock signal generated by the Clock Countdown circuitry.

In addition to the state storage there are three major functions performed by the Start/Stop Control; these are interlocking control, emergency unload logic, and condition indication.

Referring to Figure 4-9, commands used to start or stop the disks may be received either from the RUN/STOP operator control or from the Start/Stop Disk Drive I/O interface line (ISSDR). These commands are detected by the Run/Stop command and Detection circuitry and cause the Start/Stop Control to execute a start or a stop, as appropriate.

Interlocking is obtained by using a number of signals which are available within the disk drive. These signals, used in conjunction with each other, allow interlocking of various mechanical functions, e.g., locking the door on front load machines, and locking the cartridges in top load machines when the disk is rotating. The Lower Detector Pulse (LLDPG) input to the Interlock Control portion of the logic is used to establish that the disk is rotating. The Not Write Or Erase signal (NLWOEG) is generated by some of the minor control logic within the Disk Drive Function Control block and is used to prevent

retracting the heads during a normal unload when either a Write or an Erase command from the I/O interface is occurring.

Correct insertion of the cartridge is detected by two switches in top load machines, and by one switch in front load machines. This interlock prevents starting the disk drive when the cartridge is not inserted. In top load machines the parked position of the cleaning brushes is interlocked by a switch for purposes of determining that the brush cleaning cycle has been satisfactorily completed.

The Power Clear signal (SPCSA) from the Servo PCBA signals when an unacceptable power supply condition is sensed. The SPCSA signal is provided to the Start/Stop Control logic as well as to the Read/Write PCBA. Also supplied from the Servo PCBA is the Heads Retracted signal (SHRXG) which is used by the Interlock Control to ensure that the disk does not stop rotating unless the heads are retracted.

The purpose of the Emergency Unload Logic is to begin an emergency unload operation when commanded externally, or when this logic detects certain fault situations which require emergency unloading of the heads from the storage surface. One of these fault conditions is the Position Transducer Failure (SPTFG) condition. This condition is detected on the Servo PCBA and is provided to the Emergency Unload Logic should a failure occur in the position transducer. Another signal, the Write Emergency Condition (RWECG) is generated on the Read/Write PCBA should a write emergency condition be detected. Additionally, the Activate Emergency Unload (IAEUR) I/O interface line is provided for commanding emergency unloads from the I/O interface.

All other emergency unload conditions are detected by logic circuitry on the Logic PCBA. Three of these emergency conditions are detected within the Start/Stop Control arrangement by the Emergency Unload Logic. The signals utilized are: Not Position Mode (NLPMXG), Speed Out of Tolerance (LSOTF), and an internal signal within the Start/Stop Control logic. This internal signal is generated by the Interlock Control Logic from the state of the Brushes Parked switch and is not shown on the block diagram. The Not Position Mode (NLPMXG) logic state is tested by the Emergency Unload Logic to determine if the heads have properly loaded during a start sequence. Speed Out of Tolerance (LSOTF) is tested during the start sequence to determine if the disks have reached the proper speed prior to loading the heads. The internally generated signal from the brushes parked switch is tested to determine that the brush cleaning cycle has been correctly completed.

Elsewhere within the logic, three signals are generated upon detection of a specific fault condition and are provided to the Emergency Unload Logic. These signals are Not Position Limit Error (NLPLEG), Not Disk Speed Error (NLDSEG), and Not Seek Time Error (NLSTEG). The Not Position Limit Error signal commands emergency unload when the positioner exceeds its legal range of travel. The Not Disk Speed Error signal commands an emergency unload when a disk speed error is detected after the system achieves the Ready condition. The Not Seek Time Error signal commands an emergency unload when the time for a seek exceeds the allowable maximum.

The major function control output signals from the Start/Stop Control are:

(1) Start Drive Motor (NLSDMG), a pulse used for initializing the spindle speed control logic.

(2) Purge Cycle (LPCFF), a flip-flop output state used for controlling the disk speed during the purge cycle.

(3) Load Heads (LLHFF), a flip-flop output state used for controlling the position control logic and loading and unloading the heads.

(4) Emergency Unload (LEUFF), a flip-flop output state used to indicate that an emergency unload condition has started or presently exists.

(5) Load or Purge Not (NLLPNG), the output of combinational logic within the Start/Stop Control; this combinational logic decodes the states of two of the major state storage flip-flops, Purge Cycle and Load Heads. NLLPNG is used for initializing the position limit monitor contained within the Position Control Logic.

(6) Brush Motor Enable (NLBMEG), controls the power to the brush motor in top load models of the disk drive for operating the disk cleaning brushes.

(7) Brake Cycle Enable (NLBCEG), the control signal which determines when the braking current is applied to the disk drive motor.

(8) Lock Cartridge Mechanism (LLCMG), controls the solenoid drivers on the Servo PCBA and is the signal which determines when the cartridge mechanism is locked or unlocked.

(9) Emergency Unload Enable (LEUEG), controls the emergency unload relay driver on the Servo PCBA; this relay driver, in turn, actuates the emergency unload relay as commanded by the Emergency Unload Enable signal.

The output signals from the Start/Stop Control circuitry described in (1) through (5) are used on the Logic PCBA for specific control functions. The signals described in (6) through (9) are fed directly to the Servo PCBA.

Three signals for driving the operator control panel lamps are generated by the Condition Indication portion of the Start/Stop Control logic. These signals are Safe Lamp Drive (NLSLDT), Run Lamp Drive (NLRXDT), and the Ready Lamp Drive (NLRLDT). The SAFE lamp is used to indicate when it is safe for the operator to remove or insert a cartridge into the disk drive; the RUN lamp is used to indicate when a machine is executing a start sequence, or the disk is running. Illumination of the READY lamp indicates that the disk drive has achieved the Ready condition.

Other signals generated by the Condition Indication logic are: Ready (LRXXG), Selected And Ready (LSARG), Delayed Ready Condition (LDRCG). The Ready signal is the output of combinational logic and is the combination of several flip-flop states within the Start/Stop Contol. The Selected and Ready signal is the Ready signal combined with the Selected signal from the unit select logic. The Delayed Ready condition is the Ready signal passed through a delay network. Ready, Selected And Ready, and Delayed Ready Condition signals are used in other parts of the Function Control Logic as well as enabling certain portions of the Position Control Logic and the Sector Electronics Logic.

4.7.2.2 Minor Control Functions

The minor functions discussed in the following paragraphs are contained within the Disk Drive Function Control logic block shown in Figure 1-4. Due to the nature of these minor control functions, no attempt is made to relate these functions to a simplified block diagram. The circuitry which performs these logic functions is contained on sheet three of the Logic PCBA schematic.

The Select and Control Logic consists of a holding register and associated control gates for processing the Platter and Head Select lines, the Track Offset Plus, and Track Offset Minus lines. Also included is the Write Double Frequency Data Re-transmitter which acts

as a line receiver and a line driver between the I/O interface and the Read/Write PCBA. The Unit Select Logic, the Busy Output logic, and the Ready driver are also included as minor elements in the Disk Drive Function Control Logic. Likewise, the Read/Write Control logic, the Write Protect logic including the Write Protect Lamp Drivers are part of the Disk Drive Function Control Logic. Additional minor functions are performed by the Read Signal Drivers, the Malfunction Signal Driver, the Double Track Status Driver, the Illegal Address Status Driver, and the Dual Platter Status Driver. These functions are described in terms of function and purpose, as follows.

Two I/O interface control lines are provided for selecting a specific storage surface. These lines are the Head Select (IHXSR) and Platter Select (IPSXR). Two other I/O interface control lines, Track Offset Plus (ITOPR) and Track Offset Minus (ITOMR) are provided for selecting specific track offsets for diagnostic purposes. The four lines, Head Select, Platter Select, Track Offset Plus, and Track Offset Minus are processed by the holding register and distributed to the Read/Write PCBA. The Track Offset Plus and Track Offset Minus lines are also distributed to the Servo PCBA.

The Holding Register performs a holding function to store the status of these lines under certain conditions. These conditions are determined by the Selected And Ready and the Not Ready conditions. The Write Double Frequency Data Re-transmitter acts as a line receiver for the I/O interface line Write Data Signal (IWDSR) and re-transmits the signal to the Read/Write PCBA as the Write Double Frequency signal. This acts as a buffer and maintains timing of the Write Double Frequency signal.

Another minor function provided by the Disk Drive Function Control Logic is contained in the Unit Select logic. This logic combines the setting of the Unit Number Selector switch on the operator panel with the specific Unit Select Number signal from the I/O interface. Decoding is performed and the Select signal is generated only when the Unit Select line from the I/O interface corresponds to the number designated for the specific disk drive by the Unit Number Selector switch on the operator panel.

Also contained within the Disk Drive Function Control Logic is the Busy Output logic. This logic combines the busy signal from the Position Control Logic with the Ready signal and encodes on a specific Busy Seeking line according to the setting of the Unit Number Selector switch on the operator panel.

A number of line driver functions are performed by various signal drivers. These drive internal logic signals onto the I/O interface lines as outputs of the disk drive. These are:

(1) The Ready Driver for driving the selected and ready signal onto the Ready line at the interface.

(2) The Read Signal Drivers for transmitting the outputs of the Read/Write PCBA on the Read Data and Read Clock I/O interface lines.

(3) The Malfunction Signal driver for transmitting the malfunction pulse on the I/O interface line.

(4) A Double Track Status interface line for indicating at the I/O interface when a disk drive is a 200-tpi model.

(5) The Illegal Address Status driver for transmitting the illegal address signal to the Illegal Cylinder Address I/O interface line.

(6) Dual Platter Status signal driver for indicating on the Dual Platter Drive I/O interface line that the disk drive contains two platters.

Another minor function control performed is the processing of the Write Enable (IWEXR) and Erase Enable (IEEXR) signals from the I/O interface. These signals are gated by Selected And Ready, Position Mode, and File Protect Mode, then transmitted to the Read/Write PCBA for controlling those functions on the Read/Write PCBA. In addition, the Not Write or Erase signal is generated for application to the Start/Stop Control Logic. Also performed within the Read/Write control logic is the gating of Read Enable with Selected and Ready. This signal is then transmitted to the Read/Write PCBA.

The Write Protect logic combines the state of the specific WRITE PROTECT switch on the operator panel with the state of the Platter Select (IPSXR) line such that the respective protect switch and the Platter Select line are decoded to set or reset the File Protect Mode latch. The state of the File Protect Mode latch determines whether a particular platter is permitted write and erase operations, depending upon whether it is designated as a protected platter by the respective WRITE PROTECT switch on the operator panel.

The state of the File Protect Mode latch is gated with Selected and Ready and is transmitted to the I/O interface by the File Protected Status Driver which transmits the file protect condition of the disk drive to the controller on the File Protected (IFPXD) I/O line. The state of the WRITE PROTECT switches is indicated by the operator panel PROT (Protect) lamps regardless of which platter is selected. The lamp indication depends entirely on the state of the respective switch. The lamp drive signals are generated by the protect lamp drivers according to the switch states.

4.7.3 SPINDLE SPEED CONTROL

The rotational speed of the spindle is controlled to within ±1 percent of the nominal value. This tight control is maintained so that the spindle speed is not affected by line frequency variations and to avoid disk speed variations due to tolerances of the drive train components. The time reference for the spindle speed control is derived from the Crystal Oscillator and Clock Countdown logic that is shown in Figure 4-9 as part of the Start/Stop Control Logic.

The actual speed of the spindle is derived by sensing notches in the phase lock ring with a magnetic transducer. In addition to the speed sensing function, Phase Lock Ring and the Magnetic Transducer are used in conjunction with the Sector Electronics (Paragraph 4.7.5). The Phase Lock Ring is a flat circular plate with notches in the periphery. It is mounted integral with the spindle and therefore the rotational speed of the Phase Lock Ring is the same as that of the spindle. The Spindle Speed Control is a true servo loop in that power is controlled to the drive motor which, in turn, rotates the spindle; the actual speed of the spindle is sensed and compared with a time reference and the result of the comparison is used to correct the amount of power applied to the drive motor. In this manner, the loop corrects the existing speed of the spindle to the correct speed within the ability of its resolution and response capability. It is important to note that although the loop is a true closed loop servo, it is not a linear servo system. The reason is that the result of the time/speed comparison is a single binary digit and therefore can have only two possible states, a zero or a one, i.e., the speed is either too fast or too slow. For this reason the actual speed regulation takes place in a limit cycle type of operation where the actual spindle speed varies between an upper and a lower boundry as determined by the response time of the loop and the resolution of the error detector. However, certain of the loop characteristics are like a linear servo, in that power to the drive motor is varied for control by changing the time of occurrence of the application of power within a given power line cycle in a manner which is usually referred to as phase angle control. In other

words, the actual phase angle during the power line cycle where power is applied to the main winding of the drive motor is the result of the integral of the binary speed error. This determination is made from the comparison of the actual speed sensed by the Magnetic Transducer to the time reference derived from the Crystal Oscillator.

Refer to Figure 4-10*, a functional block diagram of the Spindle Speed Control Logic, for the following discussion. Operation of the spindle speed control can best be understood by starting at the Spindle and going around the loop. The Magnetic Transducer senses the notches in the Phase Lock Ring and produces a signal which is then processed by the Sector Electronics Logic (refer to Paragraph 4.7.5).

The results of the action taken by the Sector Electronics logic is the output of a flip-flop called the Phase Lock Flip-Flop (LPLFF). This flip-flop functions as a frequency divider on the basic frequency derived from the Phase Lock Ring and converts the pulse as processed by the sector electronics into a square wave. The Phase Lock Flip-Flop signal (LPLFF) is fed into the Speed Sequence Control as shown in the block diagram.

Clock signals derived from the Crystal Oscillator and Clock Countdown (LC02F, LC03F, LC04F) are fed to the Speed Control Programming logic, then to the Speed Control Counter. The time between the occurrences of low to high transitions of the Phase Lock Flip-Flop signal is detected by the Speed Sequence Control logic. Detection of this transition causes the Speed Sequence Control to generate two pulses which are synchronous with the clock signal specified by the Speed Control Programming logic. These pulses determine the sequence of the time comparison.

The desired value of disk speed is programmed by the Disk Speed Count Programming array. The program value fed to the Speed Control Counter is determined by the array and the state of the Purge Cycle Flip-Flop (LPCFF), thereby providing a nominal speed for normal operation and an over-speed value for use during the purge cycle. The programmed value of the disk speed count is fed to the Speed Control Counter logic and the selected clock signal from the Speed Control Programming logic is then counted by the Speed Control Counter. The results of the count are stored in the Speed Value Flip-Flops and, when appropriate, transferred to the Speed Status Flip-Flops as determined by the Speed Sequence Control logic. The actual comparison of the spindle speed to the reference signal occurs on the basis of the count totalized in the Speed Control Counter logic during the time interval defined between transitions of the Phase Lock Flip-Flop.

There are two outputs derived from the Speed Status Flip-Flops; the Increase Motor Speed (NLIMS1) signal and the Speed Out Of Tolerance (LSOTF) signal. The Speed Out Of Tolerance signal indicates when the disk speed is detected as being out of tolerance by the Speed Value Flip-Flops. This information is tested during the start sequence and is also combined in a Gate with the Ready signal (LRXXG) to produce Disk Speed Error (NLSDEG). The Increase Motor Speed signal is fed to the Servo PCBA and is the basic binary error signal derived from the comparison of the time reference to the actual speed. The Start Drive Motor pulse (NLSDMG) is used for intializing the speed status flip-flops during a start sequence and the Drive Motor Enable (LDMEG) line is used for initializing the Speed Sequence Control and the Speed Status Flip-Flops.

It can be seen that the purpose of the circuitry on the Logic PCBA is to convert the analog signal obtained from the Magnetic Transducer into a suitable digital square wave, then compare the time of occurrence of the positive transitions of that square wave with a time reference obtained from a Crystal Oscillator. The result of that comparison is two signals, one indicating the instantaneous speed error signal and, if appropriate, to provide a signal

*Foldout drawing, see end of this section.

which would indicate a gross malfunction of the speed control. The Increase Motor Speed (NLIMS1) obtained from the Speed Status Flip-Flops is fed to the Servo PCBA.

A portion of the Spindle Speed control circuitry is located on the Servo PCBA. Basically, there are two functions performed by this circuitry; the generation of a signal to the Motor Control PCBA which is synchronized to the line frequency and causes the trigger to occur at a specific time during the power line cycle.

Generation of a signal which is synchronized to the line frequency is necessary because the basic power line is the power applied to the drive motor by the Motor Control PCBA. This line synchronization is accomplished by a Zero Crossing type of synchronizing network in which a pulse is developed by the Line Synchronizer when the line voltage passes through the zero volt condition.

The trigger to the Motor Control PCBA must be supplied at a specific time during the power line cycle. The time of occurrence of this trigger must be proportional to the integral of the binary error signal. This is done to provide a proportional power control to the drive motor main winding that is the time average of the binary error signal (NLIMS1).

Phase angle control is obtained by the use of a Ramp Generator which is synchronized to the line voltage by the line synchronizer. The output of the integrator is compared with the voltage developed by the Ramp Generator in a Voltage Comparator. The results of this comparison are used to generate a trigger signal which is fed to the Motor Control PCBA.

The Motor Control PCBA is, in essence, a bi-directional power switch isolated from the normal machine ground. The switch is turned on by the trigger signal from the Servo PCBA and then turns itself off as the line current passes through zero. Also contained on the Motor Control PCBA is the necessary interconnection wiring for configuring the drive motor for the two basic types of power line operation, 110v and 220v (refer to Paragraph 4.8).

The trigger signal obtained from the Servo PCBA is applied to Current Amplifier Transistor Switches via an Opto-Isolator device. The Current Amplifier Transistor Switches apply gate current to the Triac Switch which selects the power line onto the main winding of the drive motor. During normal speed control, when power is to be applied to the drive motor, the specific time for switching in the power is determined by the voltage comparator on the Servo PCBA. The Triac Switch allows current to pass through the drive motor winding for that portion of the line cycle. Since the power line voltage has both a positive and a negative excursion in a given cycle, power may be applied twice during a cycle. The phase angle of that power application can be determined and controlled by the comparison of the Ramp Generator with the integrated increase motor speed signal.

The control circuitry contained on the Servo PCBA is enabled by the Not Drive Motor Enable (NLDMEG) signal. Thus, when it is desired to have no power applied to the drive motor (e.g., when the machine is stopped) the circuitry is correspondingly commanded by the state on the drive motor enable line. When it is desired to stop the disk from rotating and bring it to a halt, it is necessary to develop a braking torque to slow the disk down to the stop condition in a reasonable amount of time. This is necessary because the rotating assemblies have a considerable inertia and the time for the spindle to coast down to a stop without an additional braking force would be excessive. In order to develop this braking torque, the drive motor is operated in a special mode during that portion of the stop cycle. This is referred to as a brake cycle and is defined by the Brake Cycle Enable (NLBCEG) signal derived from the Start/Stop Control Logic on the Logic PCBA. When the Brake

Cycle Enable signal is asserted, the Servo PCBA circuitry is caused to operate in a slightly different mode wherein full power is applied to the drive motor main winding but only for one-half of a line cycle. This develops a magnetic field in the drive motor which results in a braking torque rather than in a running or starting torque. It is this torque which is used to slow the spindle to a stop.

4.7.4 POSITION CONTROL LOGIC

Figure 4-11* is a functional block diagram of the Position Control logic and should be referred to in conjunction with the following discussion.

The major function of the Position Control logic is to accept address commands from the I/O interface and cause the positioner to move to the address demanded by the interface. This involves generating suitable signals to control the mode of operation of the positioner servo and to control the velocity that is used by the positioner servo. Additionally, certain signals are generated which are supplied to the interface for purposes of indicating the Position Control Logic status. Error checking of the Position Control Logic functions are also accomplished by this logic.

The major inputs from the I/O interface are the Cylinder Demand Address (ICDNR) lines, the Cylinder Address Strobe (ICASR), and the Restore Initial Cylinder (IRICR) lines. Inputs to the Position Control logic from the Servo PCBA are: Position Reference Clock (SPRCG), Position Quadrature Clock (SPQCG), Position Transducer Index (SPTIG), Heads Retracted (SHRXG). The signals from the Servo PCBA are derived from the position transducer. Additionally, the Load Head signal (LLHFF) is provided as an input to the Position Control logic from the Start/Stop logic and is used in the Mode Control logic.

Major output signals from the Position Control logic to the Servo PCBA are the Address Difference (NLADNG), Forward Direction (LFDX1), Velocity Reference Enable (NLVREG), Position Mode (LPMXG), Forward Slow Mode (NLFSM1), and Reverse Slow Mode (NLRSM1). The major output signals which determine interface outputs are the Illegal Address (NLIAXG) and the Busy (NLBSXG) signal. The auxiliary output suppied to the Read/Write PCBA from the Position Control logic is Demand Address Most Significant (LDAMG). In 200 tpi models an auxiliary output consisting of the three most significant bits from the current address counter are supplied to the Temperature Compensation PCBA.

A Cylinder Demand Address from the I/O interface specifies the address that is required by the controller. If the address is accepted by the Position Control logic, it is stored in the Demand Address Register. Loading of this register is under control of the Load Address and Illegal Address Control logic. The validity of a demand address on the I/O interface lines is tested by the Valid Address Decoders, one decoder for 100 tpi addresses, and another decoder for 200 tpi addresses. Only one decoder is connected, depending upon the specific configuration of the machine.

The inspection and test of the address is made only when accompanied by a Cylinder Address Strobe (ICASR) from the I/O interface. In addition, the state of Restore Initial Cylinder (IRICR) line is examined at the time of a Cylinder Address Strobe and the state of that line determines if the address is to be accepted or ignored, and if a restore operation is to be performed. When the Restore Initial Cylinder line is asserted at the time of a Cylinder Address Strobe, the Demand Address lines are ignored and the Position Control logic commences a Restore operation. A Restore operation initializes the Position Control logic and returns the positioner to cylinder 000. If a Restore is not asserted at the time of a

*Foldout drawing, see end of this section.

Cylinder Address Strobe then the Demand Address lines are examined to determine if they contain a valid address. If a valid address is present, this address is accepted by the Position Control logic. If the address is an illegal address, i.e., it lies outside the range of the valid addresses, then this is signalled by the Illegal Address (NLIAXG) line.

During a strobe, and any time during a Seek operation, the Position Control logic and the positioner status are indicated on the Busy Signal (NLBSXG) line. Illegal Address and Busy Signal are outputs of the Load Address and Illegal Address Control and the Busy logic.

Information describing the current position of the positioner is stored in the Current Address Counter which is an up/down type of counter. The direction of the count and the amount of the count are determined by the Count Control logic on the basis of the Position Reference Clock (SPRCG) and Position Quadrature Clock (SPQCG) signals from the Servo PCBA. These are the digital position transducer signals derived from the outputs of the position transducer.

The positioning system in the D3000 Disk Drive functions on the basis that the physical position of the positioner is known to the Position Control Logic at all times. This is because the logic has kept track of all moves made by the positioner since initialization, i.e., current position information is initialized at the time the heads are loaded. In other words, the system knows where it is because it was told where it started from and it kept track of every move thereafter. Furthermore, it knows how far it has to go to achieve the demand address because it knows where its current location is. The particular mode of operation of the Position Control logic is determined by the Mode Control portion of the logic in conjunction with the Operation Control logic. The various inputs and outputs of this portion of the Position Control logic can be seen in the block diagram (Figure 4-16).

There are four modes of operation of the Position Control logic. One mode is the Position Mode which causes the positioner servo to operate as a position type servo and hold a particular cylinder position.

During a Seek operation it is necessary to operate the positioner servo as a velocity type of servo. This, of course, is a negation of the Position Mode line. In addition to the velocity reference enabled by the Velocity Reference Enable (NLVREG) line, the direction of the velocity is specified by the Forward Direction (LFDX1) line, and the particular velocity reference level is determined on the basis of the amount of difference between the current address and the demand address. This difference is specified to the Velocity Function Generator on the Servo PCBA by the Address Difference lines. It is important to note that the difference between the current address and the demand address is obtained by performing a ones-complement arithmetic subtraction on the binary values contained in Current Address Counter and the Demand Address Register. This subtraction process is performed by the Subtractor and Complementor logic. Since the arithmetic is ones-complement arithmetic, an end-around carry is used. This carry is under control of the Carry Control logic and the algebraic sign of the velocity desired is determined on the basis of the binary value of the carry. The actual subtraction is mechanized using an integrated circuit binary full-adder. When the heads are being loaded, it is necessary to force the carry to a particular state; this is accomplisched by the Carry Control logic on the basis of the states of certain bits in the Current Address Counter.

The other two modes of operation of the Position Control logic are the Forward Slow Mode and the Reverse Slow Mode. The two slow modes are a slow velocity type of operation. The Forward Slow Mode is used during loading of the heads and the latter portion of a

Restore operation. The Reverse Slow Mode is used for unloading the heads and for performing the first portion of a Restore operation. When operating in the Slow Velocity Mode, the velocity reference developed from the Address Difference lines is not used and therefore Velocity Reference Enable (NLVREG) is not activated.

The Error Check Logic performs two types of checks concerned with operation of the positioner. The first check determines if the positioner has completed a seek within the maximum allowable time. This check is done by the Seek Time Error (NLSTEG) check circuitry and is a gross type of check to determine simply that the positioner has not become stalled due to a fault. Although each seek is checked by this circuit, it does not verify that the time for the specific distance moved was compatible with the specific time associated with that length of seek. Rather, it determines that the positioner has not become stalled while attempting a seek.

The other error check performed is to determine that the positioner has not travelled outside of the legal range of travel. This is performed by the position limit monitor circuitry which generates a Position Limit Error (NLPLEG) signal if the positioner exceeds the normal range of travel. This check is performed only during the time that the heads are loaded onto the disk.

4.7.5 SECTOR ELECTRONICS

Figure 4-12* is a functional block diagram of the Sector Electronics logic and should be referred to in conjunction with the following discussion.

The major function of the Sector Electronics logic is to provide Sector pulses at the I/O interface which electrically subdivide the disk storage surface into a number of sectors for the purpose of addressing data stored on the disk. Additionally, the specific number of the sector passing under the Read/Write heads is transmitted to the I/O interface on the Sector Count lines. These lines specify the sector count presented in a binary format. The count indicates the particular segment of the disk surface currently under the Read/Write heads.

In addition to the Sector Pulse and Sector Count, the Index Pulse is provided as an output of the Sector Electronics. This line provides a signal which is a pulse occurring once per revolution of the disk and may be utilized to define the sector reference, i.e., sector zero.

Referring to Figure 4-12, it can be seen that the inputs to the Sector Electronics logic are a signal from the Upper Sector/Index Sensor, a signal from the Lower Phase/Index Sensor, Clock Signals obtained from the clock countdown portion of the Start/Stop Control logic and the Drive Motor Enable (LDMEG) signal also obtained from the Start/Stop Control logic.

The removable cartridge may be sectored either electronically or mechanically while the lower (fixed) platter in dual disk machines is sectored electronically.

Electronic sectoring can be in one of two configurations since the removable cartridge may be one of two configurations, i.e., an index notch only, or with sector slots and an index slot. The associated types of electronic sectoring are provided from an index-only type of cartridge and from a sector-plus-index-slot type of cartridge.

The normal top-loading cartridge has one slot in the armature plate which is referred to as the index notch. This is the standard top-loading cartridge arrangement. Some specially modified top-loading cartridges have additional notches used for mechanical sectoring purposes.

*Foldout drawing, see end of this section.

The normal front-loading cartridge has sector slots for the purpose of sectoring and a single index slot in the sector ring for purposes of mechanical sectoring. Special front-load cartridges may be designed with only an index slot.

Referring to Figure 4-12, the Upper Sector/Index Sensor is a photoelectric type of sensor for front load models and a magnetic transducer for top load models. The Lower Phase/Index Sensor is a magnetic transducer on all D3000 models. This magnetic transducer senses the notches in the Phase Lock Ring mounted on the spindle. The Phase Lock Ring is used for electronic sectoring and for speed control of the spindle. The slots or notches in the removable cartridge are sensed by the appropriate sensor type and the signal is fed to the Upper Sensor Detector which converts the analog signal from the sensor to a digital pulse train. The pulse train, however, contains either all the pulses for the sector slots, or notches, and in addition a pulse for the index slot or notch, or in the case of index-only cartridges just a single pulse for the index notch.

In the event that pulses for the sector slots or notches and the index slot or notch is present, these will be separated by the Upper Time Demultiplexer. The pulse representing the index will be output on one line from the Upper Time Demultiplexer and the sector pulses will be output on another line. Therefore, it can be said that the Upper Time Demultiplexer functions to separate the index pulse from the sector pulse. It is important to note that these pulses are pulses representative of sensing of the slot and are not the signals fed to the interface. The specific gate time required by the Upper Time Demultiplexer is programmed by a Programming Array, and the basic time reference used is obtained from a clock signal generated in the Clock Countdown portion of the Start/Stop Control logic.

In the case when an index-only cartridge is being used, a single pulse per revolution is applied to the input of the Upper Time Demultiplexer. The output of the Upper Time Demultiplexer will be a single pulse on the same line that was used for outputting the demultiplexed sector information in the previously mentioned case.

The Lower Sensor Detector is a circuit similar to the Upper Sensor Detector except that it has a variable threshold. The circuit converts the analog signal from the Phase Lock Ring magnetic transducer to a digital signal which is applied to the Lower Time Demultiplexer. The purpose of the Threshold Control for the Lower Sensor Detector is to provide a means for changing the sensitivity of the Lower Sensor Detector. When executing a stop sequence, or when the disk drive is in the Safe condition, it is desirable to be able to detect any rotation of the spindle; this is accomplished by causing the Lower Sensor Detector to operate in a high sensitivity mode via the Threshold Control logic. This high sensitivity threshold is enabled when Drive Motor Enable (LDMEG) is not asserted. When Drive Motor Enable is asserted, the threshold is changed to a threshold similar to that used in the Upper Sensor Detector. Drive Motor Enable is asserted whenever the disk drive is in the Run condition.

The Lower Time Demultiplexer functions in a manner similar to the Upper Time Demultiplexer except that the Phase Lock Ring always has a single index notch per revolution which is interposed between the phase lock notches. The Lower Time Demultiplexer will output the Index pulse on one line and all the other phase lock notch pulses on the other line. Thus, the Lower Time Demultiplexer separates the pulses obtained from the phase-lock notches from the single index notch. The value of the gate time required by the Lower Time Demultiplexer is programmed by the Programming Array. The time reference for the Lower Time Demultiplexer is obtained from a clock signal generated by the Clock Countdown circuitry in the Start/Stop Control logic.

The specific sectoring configuration is selected by the connections of the Sectoring Selection Programming Array shown as two blocks in Figure 4-17. The raw pulses output from this interconnection array are unsuitable for application to the I/O interface directly and must be formed into suitable pulses by the Upper Sector Pulse Former, the Lower Sector Pulse Former, the Upper Index Pulse Former, and the Lower Index Pulse Former. Each of these pulse former circuits takes the raw input pulse and converts it into a pulse having a time duration that is suitable for transmitting over the I/O interface. The outputs of the Upper Sector Pulse Former and Lower Sector Pulse Former are multiplexed onto the single Sector Pulse (ISPXD) line by the Sector Pulse Multiplexer according to the particular platter selected by the I/O interface.

Likewise, the outputs of the Upper Index Pulse Former and Lower Index Pulse Former are multiplexed by the Index Pulse Multiplexer and fed to the single Index Pulse (IIPXD) line according to the particular platter selected by the interface. The Multiplexer Control Logic controls the pulse multiplexers according to the state on the Upper Platter Select (LUPSG), the Not-Upper Platter Select (NLUPSG), and the Selected and Ready (NLSARG) line.

Additionally, the raw pulses obtained from the Sectoring Selection Programming Array are applied to the sector number counters for purposes of generating the sector count. The Upper Sector Number Counter and Upper Count Control are used to generate the sector number count for the upper platter. The Lower Sector Number Counter and Lower Count Control are used to generate the sector number count for the lower platter. A particaular sector count is multiplexed by the Sector Count Multiplexer logic according to the control signals generated by the Multiplexer Control logic. These control signals, generated by the Multiplexer Control logic, are a function of the specific platter selected and the Selected and Ready condition. The count control for each sector number counter determines when the counter will be returned to a zero count. This is determined automatically as a result of the count control action obtained from the raw index pulse occurrence.

Electronic pulses are generated by the disk drive as selected by the Sectoring Selection Programming Array when the removable cartridge has the index slot only, or when it is desired to electronically sector a multi-notch removable cartridge. Additionally, the Sectoring Selection Programming Array causes the disk drive to generate pulses for sectoring the lower disk which is sectored electronically regardless of the configuration. These pulses are generated by counting down, with an electronic counter, the output of a high-frequency oscillator. Because the sector pulses must be synchronous with the instantaneous speed of rotation of the spindle, it is necessary to phase lock this high-frequency oscillator to the spindle.

Those particular functions are implemented by the Sector Phase Lock Loop through the Upper and Lower Sector Countdown Counters. Associated with these counters are Electronic Sector Programming Arrays used to determine a particular number of sectors and a synchronizer for each counter to synchronize the count with the Index pulse obtained from their respective Time Demultiplexer. The output derived from the phase lock ring notches are fed via the Lower Time Demultiplexer to a Phase Lock Flip-Flop which divides the frequency of that pulse train by a factor of 2, and converts it into a square wave. This square wave is used not only by the Sector Phase Lock Loop but is one of the outputs of the Phase Lock Flip-Flop fed to the Spindle Speed Control electronics.

The Voltage Controlled Oscillator (VCO) within the Sector Phase Lock Loop is electronically servoed to the square wave obtained from the Phase Lock Flip-Flop. This is

accomplished by taking the output of the VCO and counting it down with the Sector PLL Countdown Counter. The specific countdown value is programmed by the Countdown Programming Array and the output of the counter is converted to a square wave by the Sector Countdown Divider Flip-Flop. The outputs of the Sector Countdown Divider Flip-Flop are compared with the Phase Lock Flip-Flop output by the Phase Comparator. The output of the Phase Comparator is suitably filtered and applied to a Sum-And-Difference Amplifier which generates the control voltage for servoing the frequency of the VCO. This causes the output of the VCO to become phase-locked to the phase lock pulses obtained from the phase-locked ring.

The output of the VCO may be taken directly or the frequency may be divided by a factor of 2 by the VCO Divider Flip-Flop and applied to the Sectoring Selection Programming Array for purposes of selecting the specific electronic sectoring configuration. This high-frequency oscillator signal is then frequency divided by the Sector Countdown Counter for the particular platter. The exact value of a count used for the division is determined by the respective Electronic Sector Programming Array. The count is synchronized to a specific platter by the associated synchronizer in conjunction with the index pulse derived for use with that particular platter. The pulse train output from the particular sector countdown counter has a repetition rate corresponding to the number of desired sectors as programmed by the respective Electronics Sector Programming Array. This pulse train is synchronized with the respective index pulse.

When electronic sectoring is selected by the Sectoring Selection Programming Array, this pulse train is fed directly to the respective pulse former.

4.8 MOTOR CONTROL

A functional element of disk rotational speed control is provided by the Motor Control circuitry. The current switching necessary to control drive current for the drive motor is provided by this subsystem. Additionally, provisions are made to accommodate drive motor operation at different line voltages in this subsystem.

The disk drive motor is a permanent split-phase induction motor with multiple windings to accommodate the two classes of line voltage operation. A permanent split induction motor requires the use of a capacitor or other type of phase shifting arrangement connected in series with the start winding (or windings). This is done to provide a current in that winding, phase shifted with respect to the main winding, such that the net magnetic field produced by the windings is a pseudo rotating magnetic field. In the D3000 Disk Drive, motor capacitors mounted on the power supply chassis are connected to provide the phase shift of current in the start windings with respect to the main winding.

For 110v operation, main winding number 1 is connected in parallel with main winding number 2 and is operated directly from the line voltage. Current through the winding is switched on and off by a triac on the Motor Control PCBA. For 220v operation, main winding number 1 is connected in series with main winding number 2 and the series combination of these windings is operated directly from the line voltage. The current is switched on and off by the triac on the Motor Control PCBA. The motor capacitors are parallel-connected for 110v operation and series-connected for 220v operation.

Therefore, the effective arrangement for 110v operation is that the parallel combination of the motor capacitors is connected in series with the parallel combination of start winding number 1 and start winding number 2. This parallel series network is operated directly from the line voltage and is not switched by the triac. For 220v operation, the series

combination of the motor capacitors is connected to the series combination of start winding number 1 and start winding number 2 and this series network is operated directly from the line voltage and is not switched by the triac. Thus, it can be seen that current flows in the start winding at all times when power is applied via the ON/OFF switch on the operator panel.

Torque will not be developed by the motor to an extent which will allow starting rotation of the disks unless the main winding is energized for a sufficient amount of time to provide the net rotating magnetic field. Likewise, sufficient torque to maintain rotation will be available only if the main winding is energized sufficiently often that the available field from a combination of the main and the start winding can provide the necessary torque to the load. Torque available from the drive motor is therefore provided by switching on and off the current in the main winding. The ability to control the speed of the drive motor and the torque that it supplies to the load is therefore contingent upon switching the triac on the Motor Control PCBA at the correct times and allowing current to flow in the main winding as required.

The current amplification necessary to provide the high current drive for the gate of the triac is provided by transistor current switches on the Motor Control PCBA.

Since the main winding of the drive motor is an inductive load, there can exist a phase shift between the current through the motor and the applied voltage. This means that at the time the triac current falls below the holding current value and the triac ceases to conduct, there will exist a certain voltage across the triac. If this voltage appears too rapidly, the triac will resume conduction and control will be lost. In order to achieve control with certain inductive loads, such as the drive motor, the rate of rise in voltage must be limited by a series R-C network across the triac. The capacitor limits the rate of change of voltage across the triac with respect to time; the resistor limits the surge of current from the capacitor discharging when the triac first conducts. It is also used to damp the ringing of the capacitance with the drive motor inductance and the inductance of a series inductor mounted on the Motor Control PCBA. This additional inductor is required to reduce transients caused by the triac switching into conduction.

4.9 POWER SUPPLY

Figure 4-13 is a block diagram of the disk power supply which is in two parts. The first part, the power supply module mounted on the power supply chassis, is fastened to the base casting and contains the power transformer, rectifiers, capacitors, fuses, and power resistors. Three unregulated dc supplies are generated at nominal voltages of ±20v and ±10v dc. Three ac supplies are generated at nominal voltages of ac line voltage, 8v ac (rms) and 21v ac (peak).

The second part of the power supply consists of the ±10v and ±5v voltage regulators which are located on the Servo PCBA. Interconnection between the two parts is provided by a harness from the power supply chassis which plugs into the Servo PCBA via a 12-pin connector. Interconnection for ac line voltage, ac common, and 8v ac (rms) to the Motor Control PCBA is provided via a 6-pin connector.

The transformer primary connections are shown in Figure 4-14 for several line voltages. Line voltage is connected to the transformer via the ON/OFF switch. The ac line voltage is also used directly to power the disk drive motor. Also, 8v ac (rms) and 21v ac (peak) are used for drive motor speed control circuits and to power the brush motor and associated circuits. Unregulated dc (at a nominal of +20v under load) is used to provide power to the

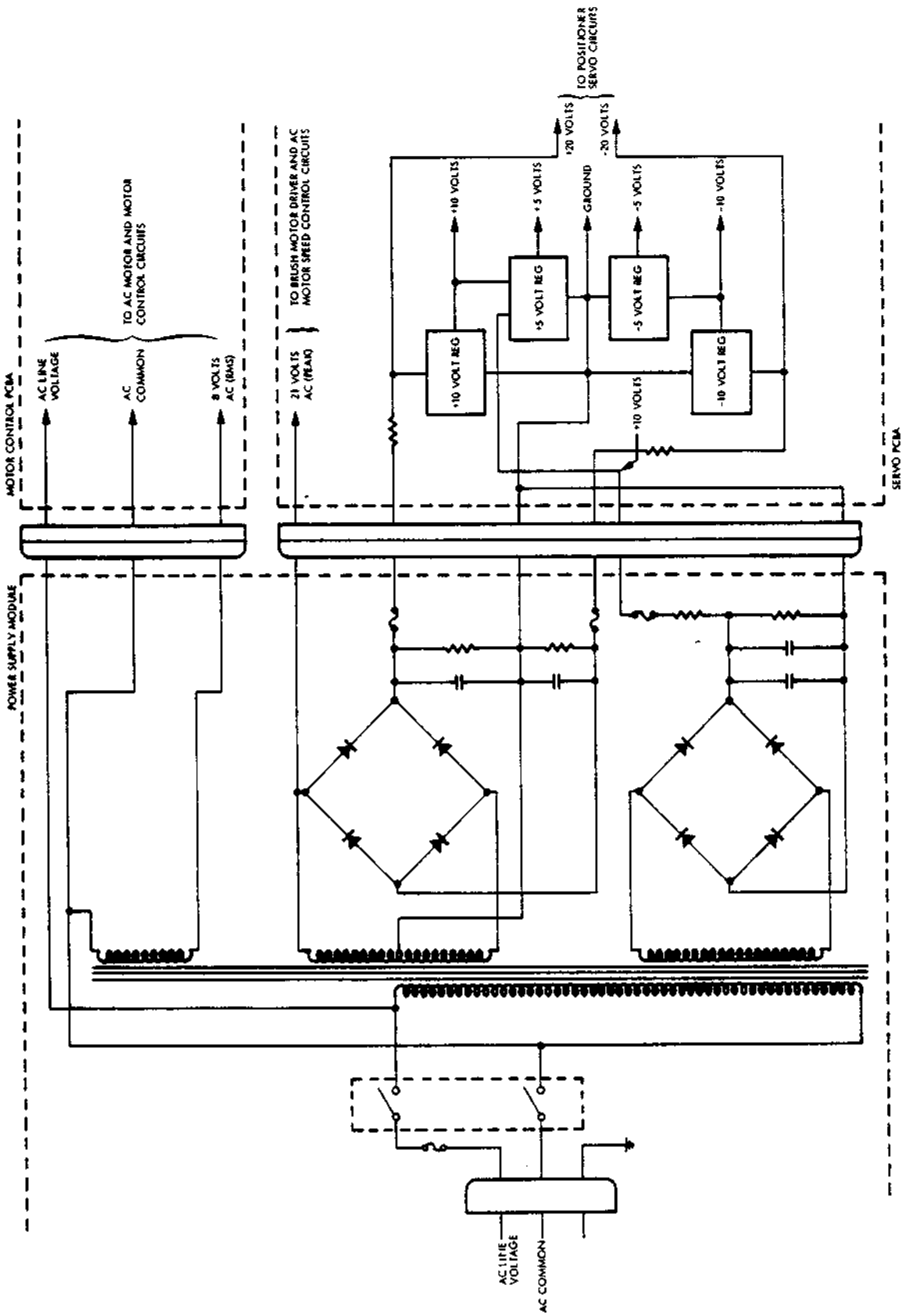
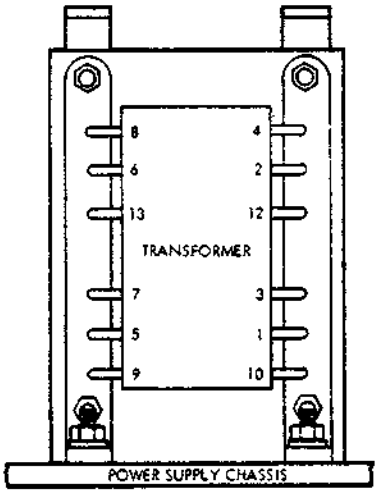


Figure 4-13. Power Supply Functional Block Diagram



LINE VOLTAGE	LINE BETWEEN	CONNECT
95	13 AND 3	12 TO 13 AND 3 TO 7
100	6 AND 3	2 TO 6 AND 3 TO 7
110	5 AND 3	1 TO 5 AND 3 TO 7
115	6 AND 4	2 TO 6 AND 4 TO 8
125	5 AND 4	1 TO 5 AND 4 TO 8
190	13 AND 3	12 TO 7
200	6 AND 3	2 TO 7
210	6 AND 3	1 TO 7
215	6 AND 4	2 TO 7
220	5 AND 3	1 TO 7
225	5 AND 4	2 TO 7
230	6 AND 4	2 TO 8
235	5 AND 4	1 TO 7
240	6 AND 4	1 TO 8
250	5 AND 4	1 TO 8

NOTE: THIS TABLE APPLIES TO POWER SUPPLY ASSEMBLY NUMBER 102741-01

Figure 4-14. Transformer Primary Connections

positioner, voltage regulators, relay driver, and the solenoid driver. The voltage regulators generate four regulated voltage supplies. The ±10v supplies are zener regulated but not adjustable. The ±5v supplies are adjustable and regulated.

All regulated dc voltages are protected against overvoltage by means of SCR *crowbar* protection circuits. When any of the regulated voltage lines exceed its pre-set overvoltage value, the corresponding SCR fires. This holds the voltage down on the circuits connected to this voltage line until the fuse blows a few milliseconds later. The power resistors, in series with the unregulated ±20v dc and unregulated ±10v dc, limit short circuit currents to a finite value when the SCR fires in the corresponding circuit. The bleeder resistors, provided across capacitors, discharge the capacitors when the power supply input line cord is disconnected.

4.10 TEMPERATURE COMPENSATION (200 TPI)

Figure 4-15* is a functional block diagram of the temperature compensation circuitry used in 200 tpi models. One thermistor is employed to sense the positioner baseplate temperature. The analog signal from this thermistor is amplified and scaled to yield signals which are accurately related to temperature. This signal is then amplified and applied to the servo summing junction on the Servo PCBA and used as warm-up transient compensation.

The positioner baseplate temperature signal is also compared to a temperature reference signal from the temperature compensation circuitry and the difference applied to a multiplying digital-to-analog converter. The multiplying digital-to-analog converter also accepts as an input from the Logic PCBA the three most significant bits of the current address counter. These signals are then applied to the servo summing junction for compensation of the disk tracks.

A delay circuit which is timed to start at the end of the normal starting sequence is an optional item that delays the interface IRDY signal. This circuitry is controlled by the Logic PCBA and ensures stabilization of the disk drive before the temperature GO signal is generated.

*Foldout drawing, see end of this section.

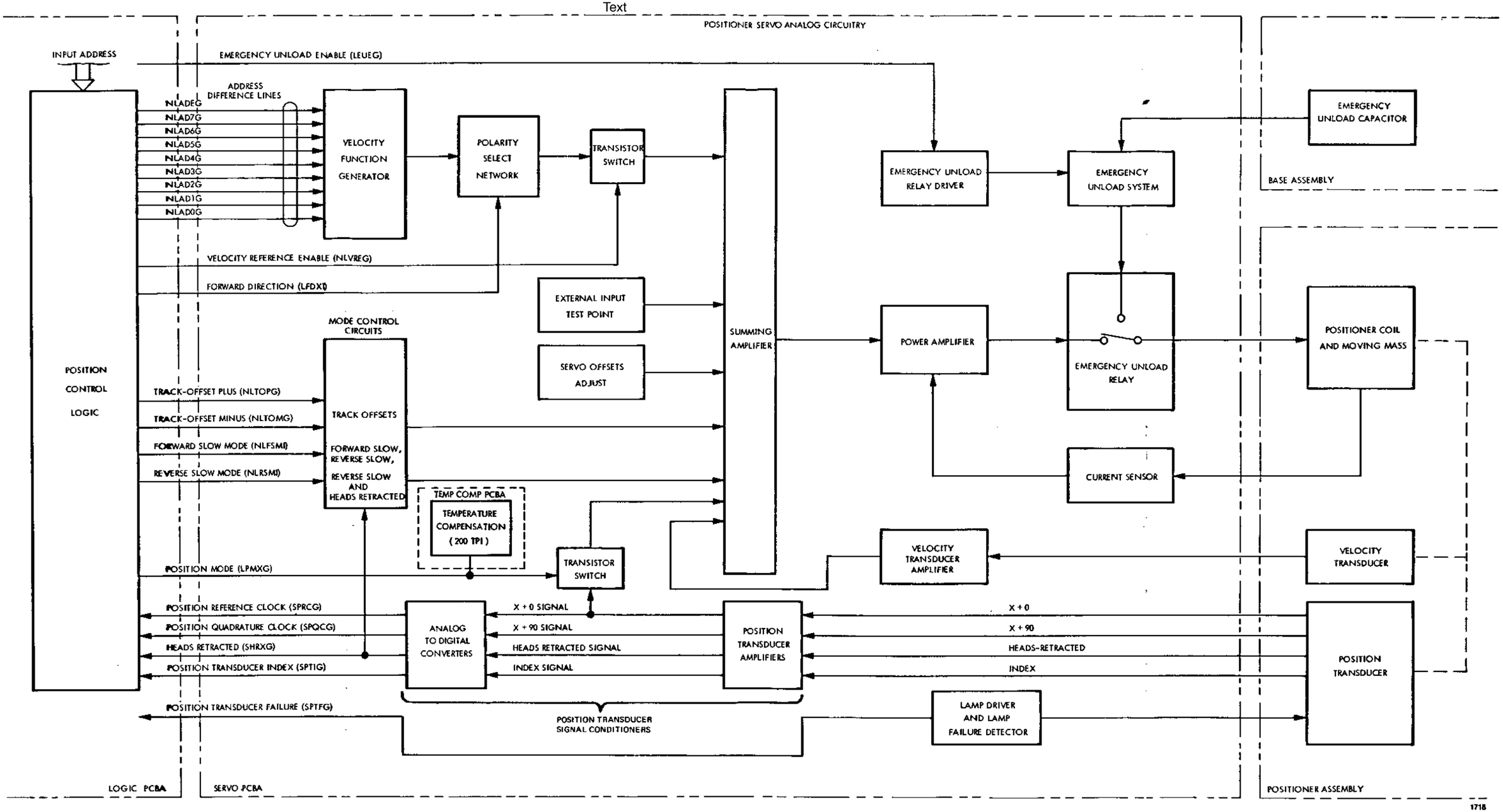


Figure 4-2. Positioner and Positioner Electronics, Functional Block Diagram

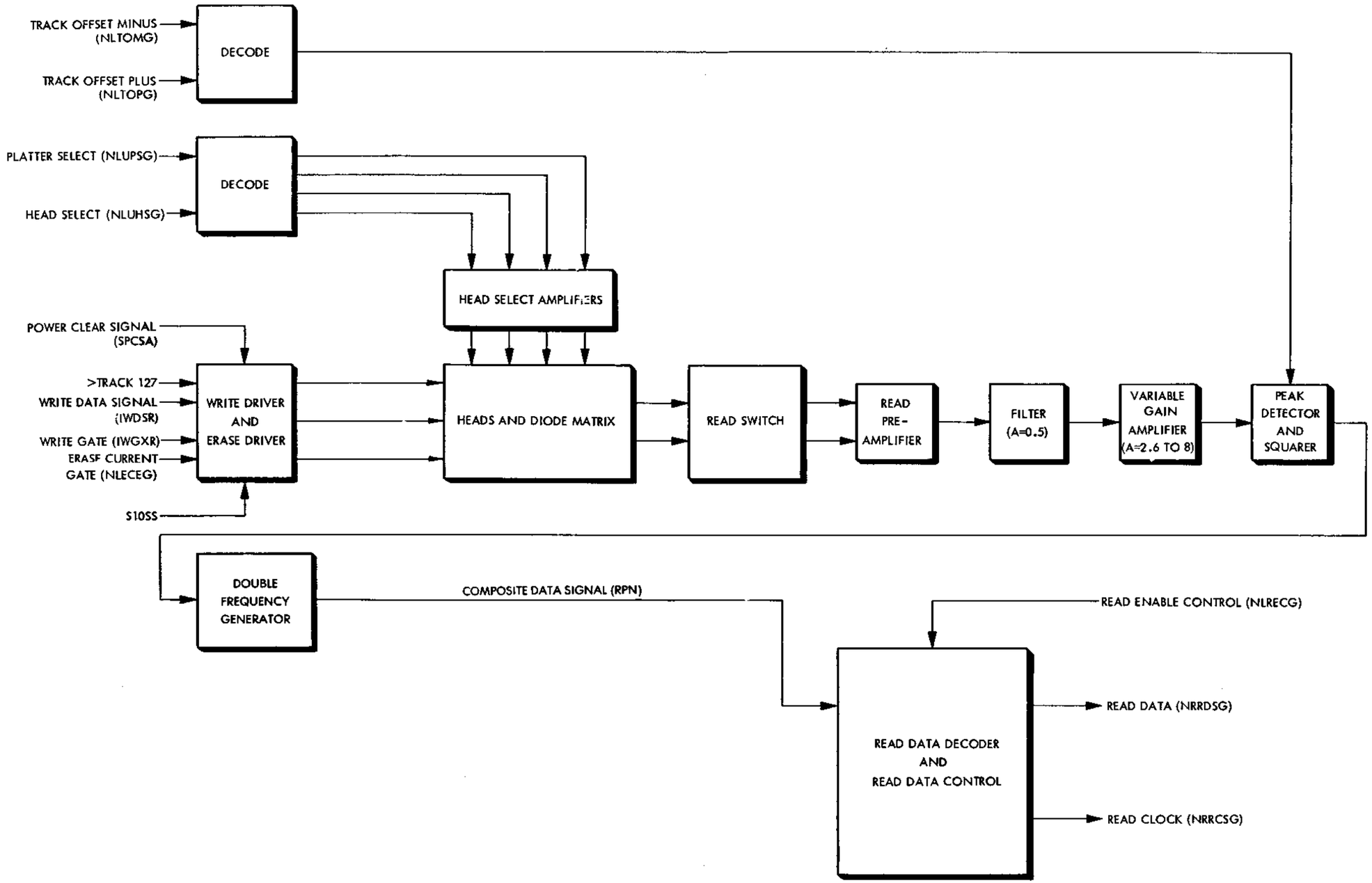


Figure 4-4. Read/Write Electronics, Functional Block Diagram

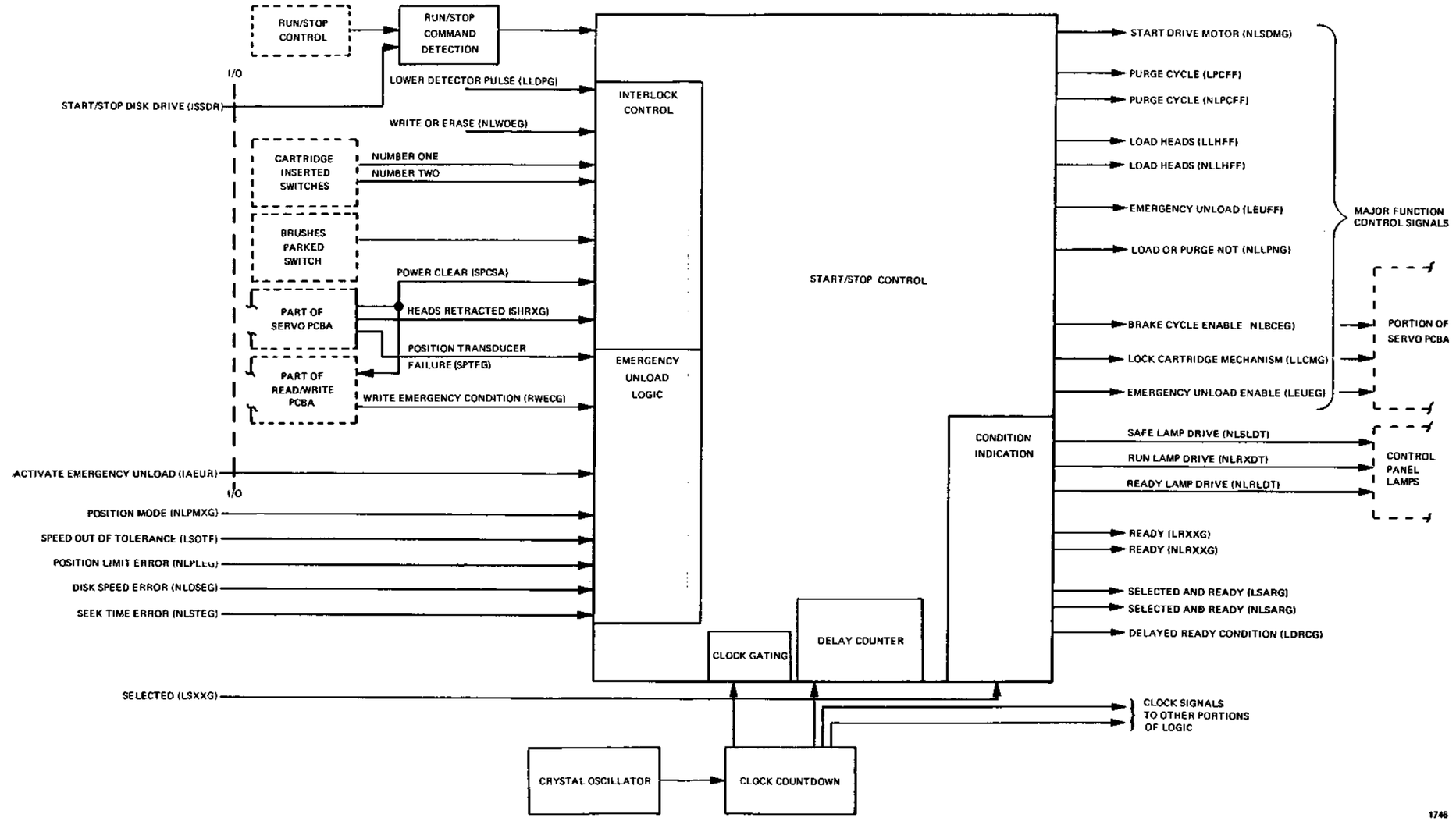


Figure 4-9. Start/Stop Control, Functional Block Diagram

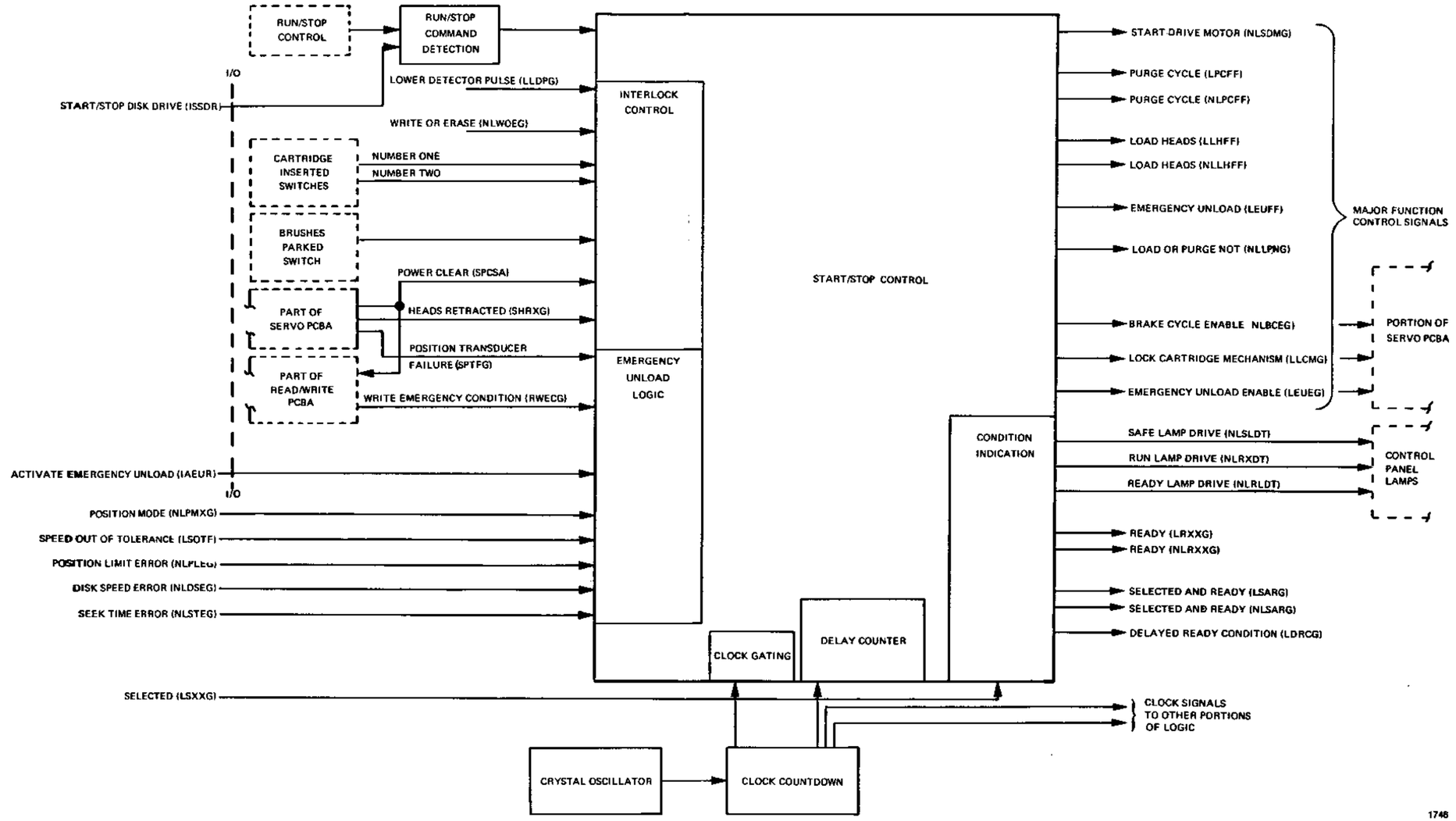


Figure 4-9. Start/Stop Control, Functional Block Diagram

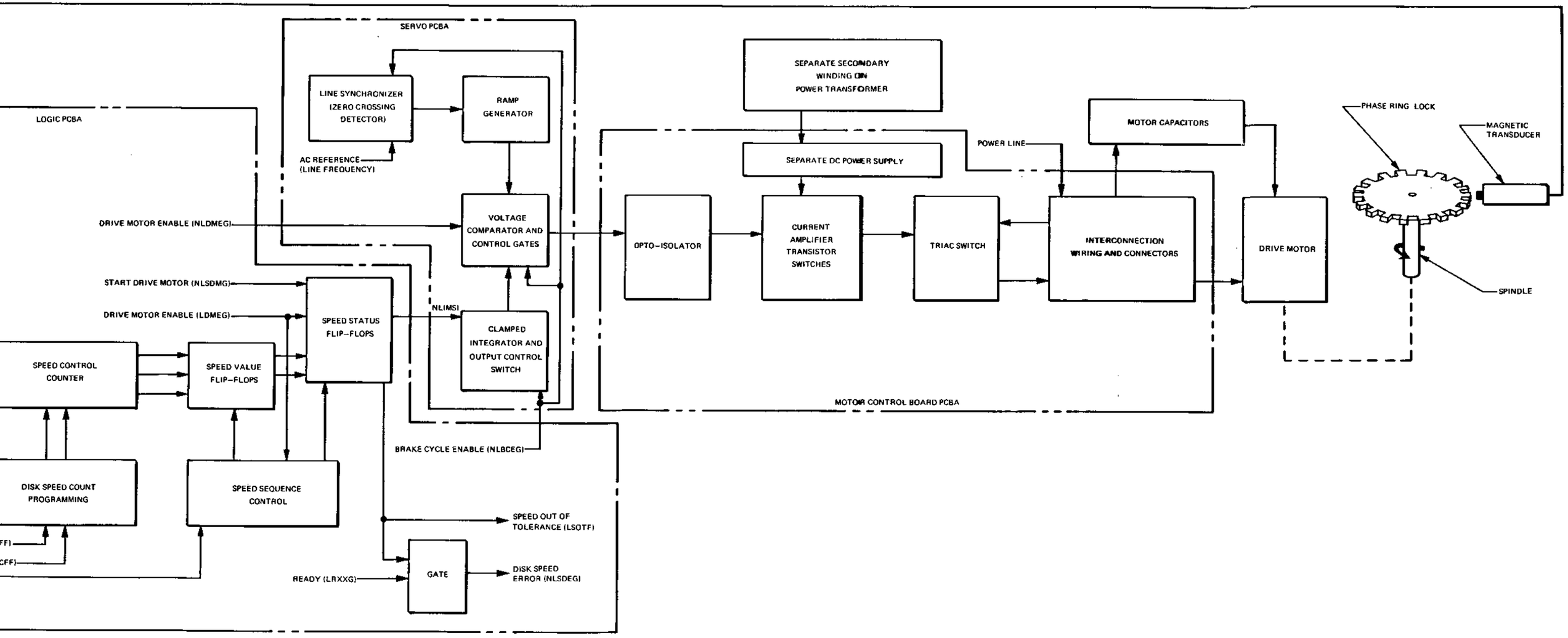
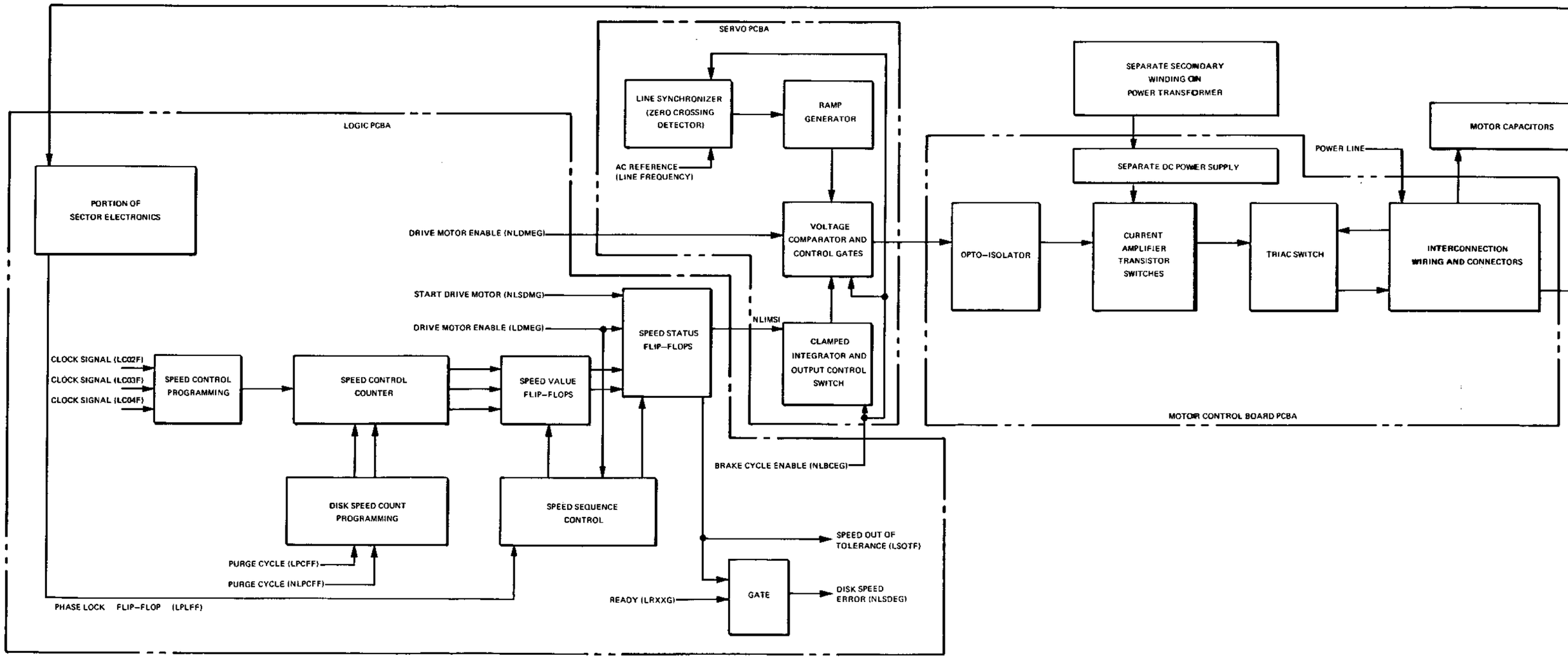


Figure 4-10. Spindle Speed Control, Functional Block Diagram


LOGIC PCBA
PORTION OF SECTOR ELECTRONICS
SERVO PCBA
LINE SYNCHRONIZER (ZERO CROSSING DETECTOR)
RAMP GENERATOR
AC REFERENCE (LINE FREQUENCY)
DRIVE MOTOR ENABLE (NLDMEG)
VOLTAGE COMPARATOR AND CONTROL GATES
START DRIVE MOTOR (NLSDMG)
DRIVE MOTOR ENABLE (LDMEG)
SPEED STATUS FLIP–FLOPS
NLIMSI
CLAMPED INTEGRATOR AND OUTPUT CONTROL SWITCH
CLOCK SIGNAL (LC02F)
CLOCK SIGNAL (LC03F)
CLOCK SIGNAL (LC04F)
SPEED CONTROL PROGRAMMING
SPEED CONTROL COUNTER
SPEED VALUE FLIP–FLOPS
DISK SPEED COUNT PROGRAMMING
SPEED SEQUENCE CONTROL
PURGE CYCLE (LPCFF)
PURGE CYCLE (NLPCFF)
PHASE LOCK FLIP–FLOP (LPLFF)
BRAKE CYCLE ENABLE (NLBCEG)
SPEED OUT OF TOLERANCE (LSOTF)
READY (LRXXG)
GATE
DISK SPEED ERROR (NLSDEG)
SEPARATE SECONDARY WINDING ON POWER TRANSFORMER
SEPARATE DC POWER SUPPLY
OPTO–ISOLATOR
CURRENT AMPLIFIER TRANSISTOR SWITCHES
TRIAC SWITCH
POWER LINE
MOTOR CAPACITORS
INTERCONNECTION WIRING AND CONNECTORS
MOTOR CONTROL BOARD PCBA

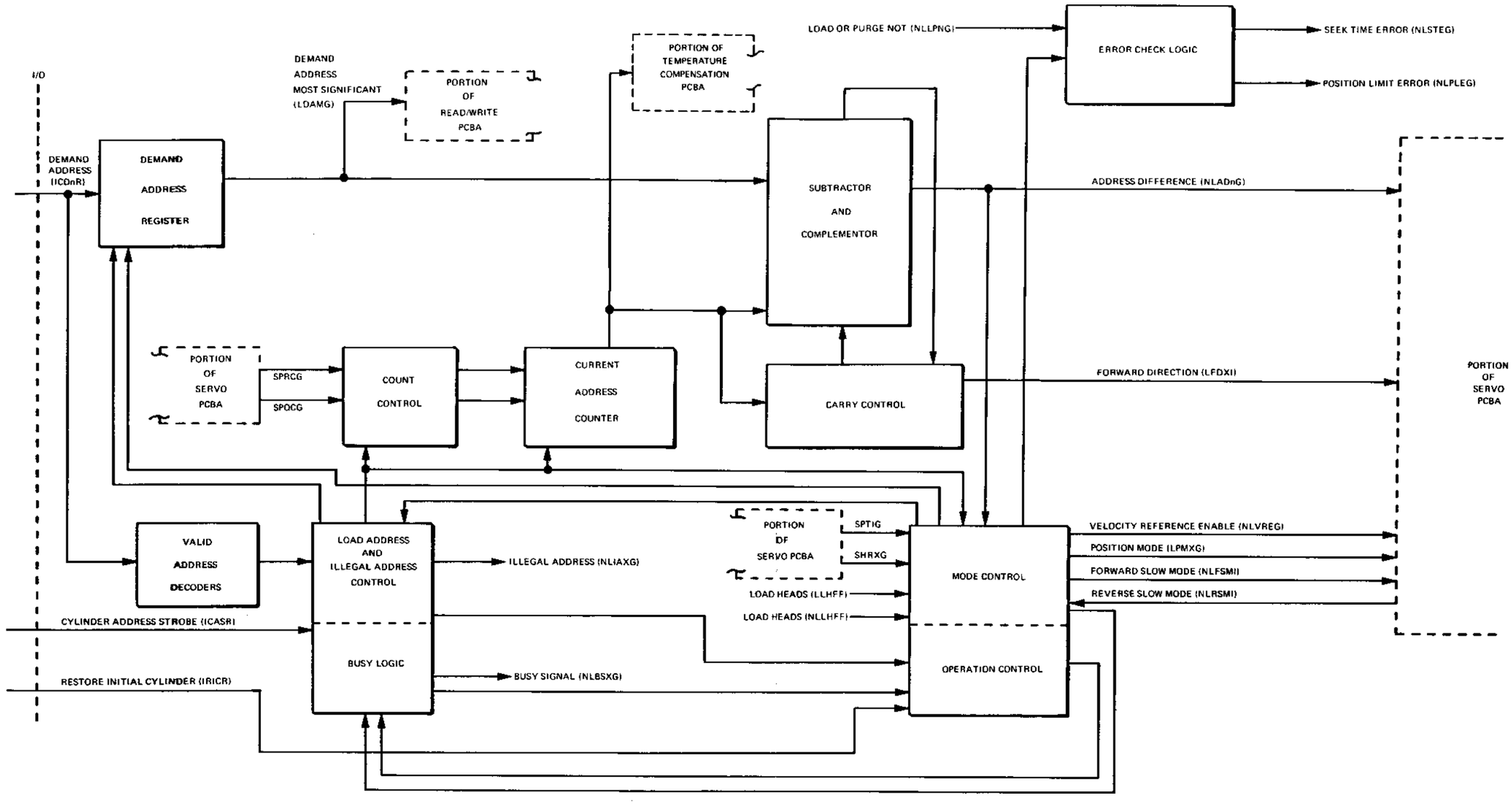


Figure 4-11. Position Control Logic, Functional Block Diagram

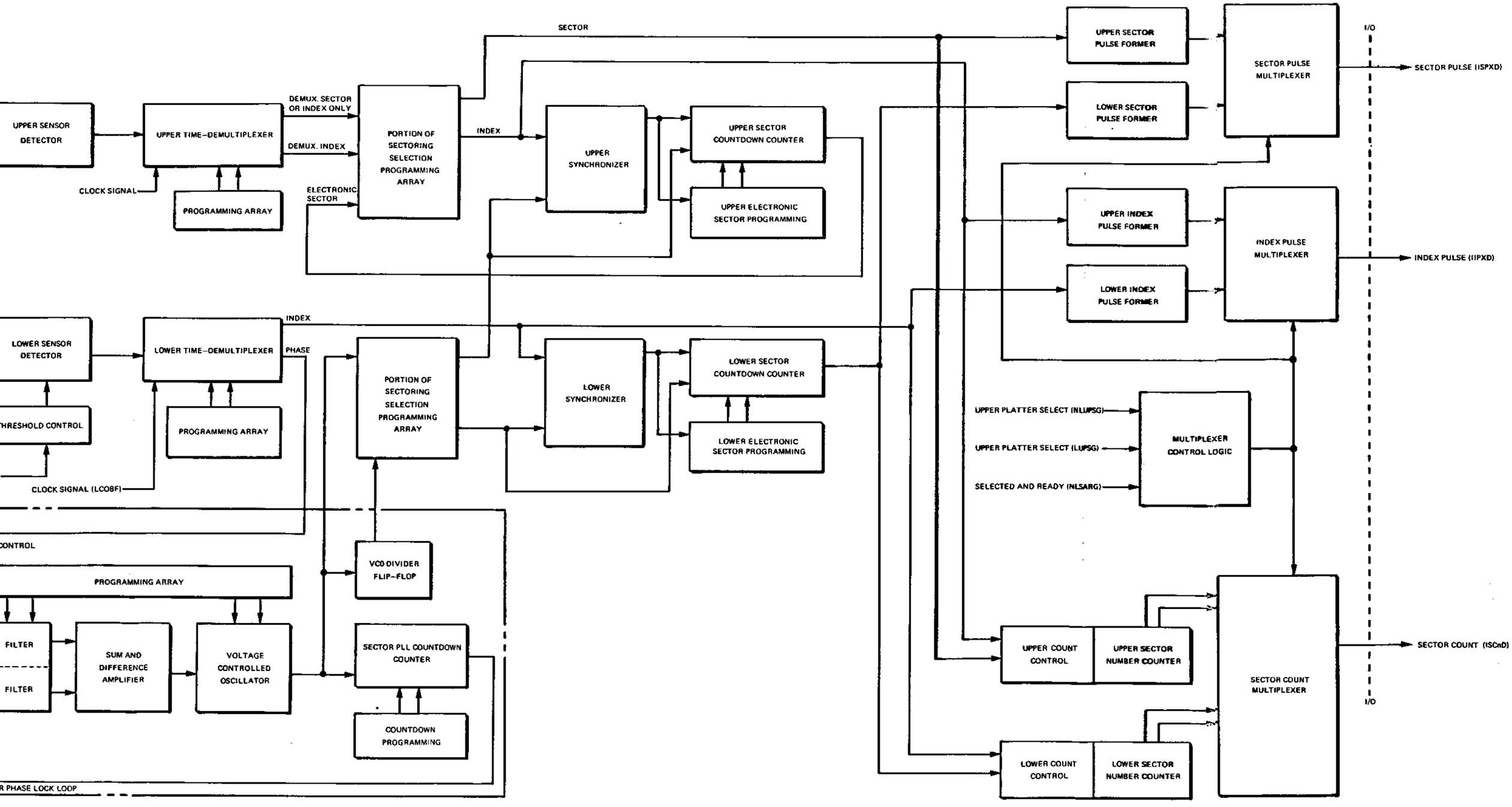


Figure 4-12. Sector Electronics, Functional Block Diagram

UPPER SECTOR/INDEX SENSOR

TOP LOAD MODELS:
MAGNETIC TRANSDUCER

FRONT LOAD MODELS:
PHOTOELECTRIC SENSOR

UPPER SENSOR DETECTOR

UPPER TIME-DEMULTIPLEXER

CLOCK SIGNAL

PROGRAMMING ARRAY

DEMUX. SECTOR OR INDEX ONLY

DEMUX. INDEX

ELECTRONIC SECTOR

PORTION OF SECTORING SELECTION PROGRAMMING ARRAY

SECTOR

INDEX

UPPER SYNCHRONIZER

UPPER SECTOR COUNTDOWN COUNTER

UPPER ELECTRONIC SECTOR PROGRAMMING

UPPER SECTOR PULSE FORMER

LOWER SECTOR PULSE FORMER

UPPER INDEX PULSE FORMER

LOWER INDEX PULSE FORMER

LOWER PHASE/INDEX SENSOR

(MAGNETIC TRANSDUCER)

LOWER SENSOR DETECTOR

THRESHOLD CONTROL

DRIVE MOTOR ENABLE (LDMEG)

CLOCK SIGNAL (LCOBF)

LOWER TIME-DEMULTIPLEXER

PROGRAMMING ARRAY

INDEX

PHASE

PORTION OF SECTORING SELECTION PROGRAMMING ARRAY

LOWER SYNCHRONIZER

LOWER SECTOR COUNTDOWN COUNTER

LOWER ELECTRONIC SECTOR PROGRAMMING

UPPER PLATTER SELECT (NLUPSG)

UPPER PLATTER SELECT (LUPSG)

SELECTED AND READY (NLSARG)

MULTIPLE CONTROL L

(LPLFF) TO SPINDLE SPEED CONTROL

PHASE LOCK FLIP-FLOP

PROGRAMMING ARRAY

VCO DIVIDER FLIP-FLOP

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PHASE COMPARATOR

FILTER

FILTER

SUM AND DIFFERENCE AMPLIFIER

VOLTAGE CONTROLLED OSCILLATOR

SECTOR PLL COUNTDOWN COUNTER

COUNTDOWN PROGRAMMING

SECTOR PHASE LOCK LOOP

UPPER COUNT CONTROL

UPPER SECTOR NUMBER COUNTER

LOWER COUNT CONTROL

LOWER SECTOR NUMBER COUNTER

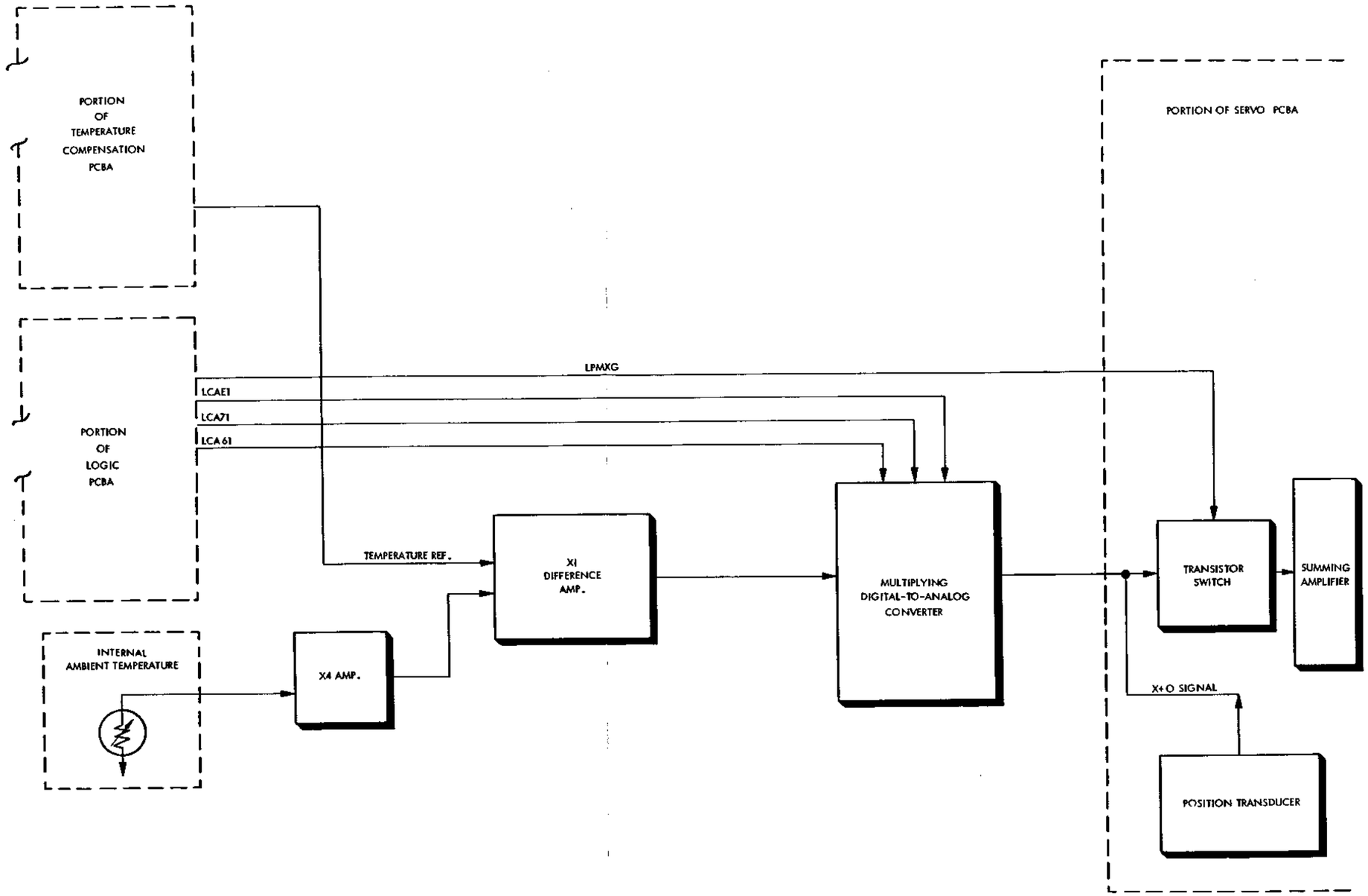

Figure 4-15. Temperature Compensation, Functional Block Diagram