MODEL NO. _____

SERIAL NO. _____

MODEL D3000
DISK DRIVE
WITH DIABLO
COMPATIBLE INTERFACE

PERTEC
PERIPHERAL EQUIPMENT
DIVISION

9600 IRONDALE AVE., CHATSWORTH, CALIF. 91311
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OPERATING AND SERVICE MANUAL NO. 103715

FOREWORD

This manual provides operating and service instructions for D3000 Series Disk Drives with Diablo Compatible Interface, Models D3300 and D3400, manufactured by PERTEC Peripheral Equipment Division, Chatsworth, California.

The content includes a detailed description, specifications, installation instructions, and checkout of the disk drive. Also included are theory of operation and preventive maintenance instructions. Section VII contains photo parts lists and schematics.

All graphic symbols used in logic diagrams conform to the requirements of MIL-STD-806 and all symbols used in schematic diagrams are as specified in MIL-STD-15.

The disk drive models covered by this manual are listed below.

Model	Tracks per Inch	Bits per Inch	Cartridge Type Load		Fixed Disk	Spindle Speed (rpm)
			Front	Top		
D331X	100	2200		X		1500 or 2400
D332X	100	2200		X	X	1500 or 2400
D334X	100	2200	X		X	1500 or 2400
D342X	200	2200		X	X	1500 or 2400
D344X	200	2200	X		X	1500 or 2400

SERVICE AND WARRANTY

This PERTEC product has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected wherever possible from manufacturer's off-the-shelf stock. Should a component fail, it may be readily replaced from PERTEC or your local supplier. The unit has been designed for plug-in replacement of circuit boards or major components which will ensure a minimum of equipment down time.

PERTEC warrants products of its manufacture to be free from defect in design, workmanship, and material under normal use and service for a period twelve (12) months, or in the case of flexible disk products 120 days, after the date of shipment. PERTEC agrees to repair or replace at its authorized repair center, without charge, all defective parts in systems which are returned for inspection to said center within the applicable warranty period; provided such inspection discloses that the defects are as specified above, and provided further the equipment has not been altered or repaired other than with authorization from PERTEC and by its approved procedures, not been subjected to misuse, improper maintenance, negligence or accident, damaged by excessive current or otherwise had its serial number or any part thereof altered, defaced or removed. All defective items released hereunder shall become the property of seller. THIS WARRANTY IS IN LIEU OF, AND BUYER WAIVES, ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING THOSE OF MERCHANTABILITY OR FITNESS FOR PURPOSE.

Please read the instruction manual thoroughly as to installation, operation, maintenance, and component reference list. Should you require additional assistance in servicing this equipment, please contact the following conveniently located regional service centers — our trained service staff will be pleased to assist you.

WESTERN REGION

PERTEC Service Center
17835 Ventura Blvd,
Encino, California 91316
Phone (213) 996-1333
TWX (910) 493-2075

EASTERN REGION

PERTEC Service Center
235 Bear Hill Road
Waltham, Massachusetts 02154
Phone (617) 890-6230
TWX (710) 324-1154

CENTRAL REGION

PERTEC Service Center
6300 North River Road
O'Hare International Transportation Center
Rosemont, Illinois 60018
Phone (312) 696-2460
TWX (910) 253-5918

EUROPEAN REGION

PERTEC Service Center
PERTEC International
10 Portman Road
Reading, Berkshire RG3 1DU, England
Phone Reading (734) 582-115
TWX (851) 847-101

AUTHORIZED REPAIR CENTER

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9600 Irondale Avenue
Chatsworth, California 91311
Phone (213) 882-0030
TWX (910) 494-2093

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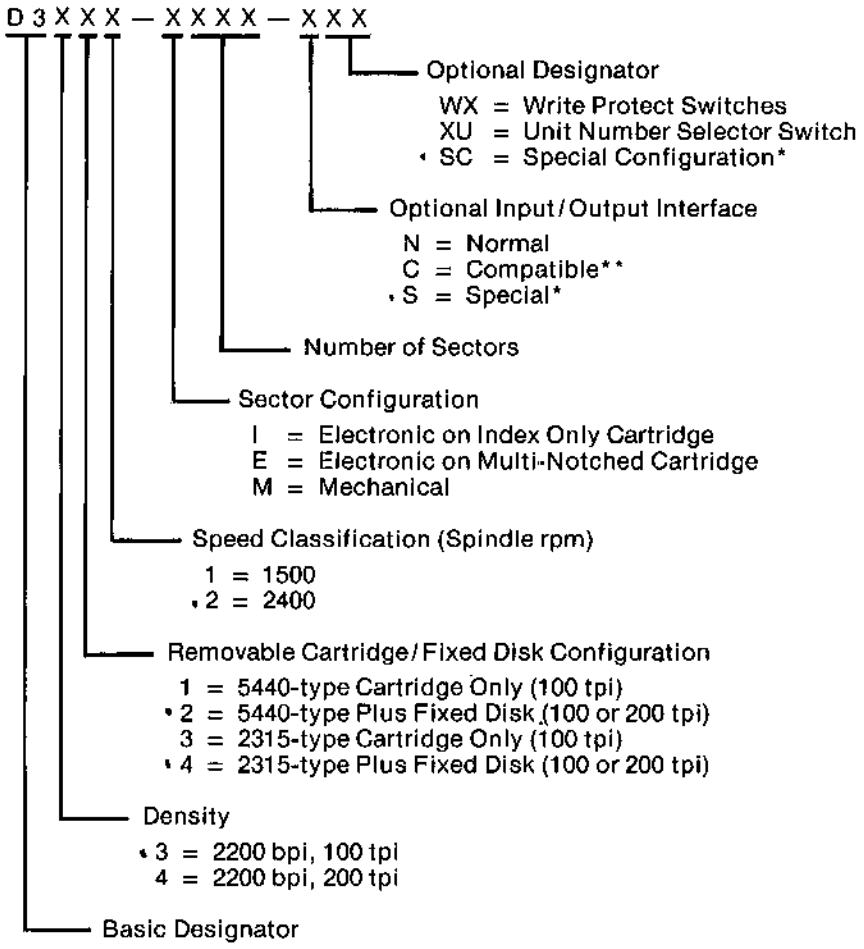
SECTION I
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides a physical description, functional description, and specifications for the D3000 Series Disk Drive with Diablo Compatible Interface, Models D3300 and D3400, manufactured by PERTEC Peripheral Equipment Division, Chatsworth, California.

1.1.1 MODEL IDENTIFICATION

To simplify identification of D3000 Series Disk Drives, Figure 1-1 illustrates the breakdown of code combinations employed by PERTEC.



*As specifically ordered; not described in this manual.

**Electrically compatible with Diablo Series 30 Interface.

Figure 1-1. Model Identification

Referring to Figure 1-1, the following illustrates the ease of identification, using Model D3322-I064-NWU as an example.

(1) D3 is the basic prefix used on all D3000 Series.

(2) 3 in the third position indicates a 2200 bpi, 100 tpi device.

(3) 2 in the fourth position indicates a 5440-type cartridge plus fixed disk is used.

(4) 2 in the fifth position indicates a spindle speed of 2400 rpm.

(5) I in the sixth position indicates that the 5440-type cartridge to be utilized has a normal index notch only.

(6) 064 in the seventh, eighth, and ninth positions indicate a 64-sector device.

(7) N in the tenth position indicates a Normal (standard) interface configuration option.

(8) W in the eleventh position indicates the unit is provided with Write Protect switches.

(9) U in the twelfth position indicates the unit is provided with Unit Number Selector switch.

1.2 PURPOSE OF EQUIPMENT

The disk drive has the capability of recording digital data on IBM 2315 or 5440 type cartridges utilizing the double frequency method of recording. Spindle speeds up to 2400 rpm and data storage of up to 100 mega bits are provided by the D3000 Series Disk Drive. Data recorded on the removable media can be recovered when played back on any D3000 or D5000 Series having the same cartridge type, density, format, and speed.

The D3000 is a rotating magnetic memory capable of storing and retrieving data in digital form. The storage media is an aluminum disk coated on both surfaces with a layer of ferro magnetic material suspended in a binder. Data are stored serially in concentric tracks on both surfaces of the disk.

The basic disk drive is available as a single disk or dual disk device. All models are capable of accepting removable media with the removable disk enclosed in a cartridge assembly. Depending on the model, the disk drive will accept either the top loading 5440-type or the front loading 2315-type cartridge.

Single disk models have provisions for the removable cartridge only; dual disk models have provisions for the removable cartridge and a fixed disk enclosed within the drive housing.

The disk drive is intended for use in conjunction with a formatter or controller to provide rapid access mass memory for small and medium size computers.

An integral power supply is included in the disk drive and operates directly from single phase power.

1.3 PHYSICAL DESCRIPTION OF EQUIPMENT

The top loading configuration of the D3000 Disk Drive utilizes a 5440 type cartridge and is shown in Figure 1-2; the front loading configuration utilizes a 2315 type cartridge and is shown in Figure 1-3.

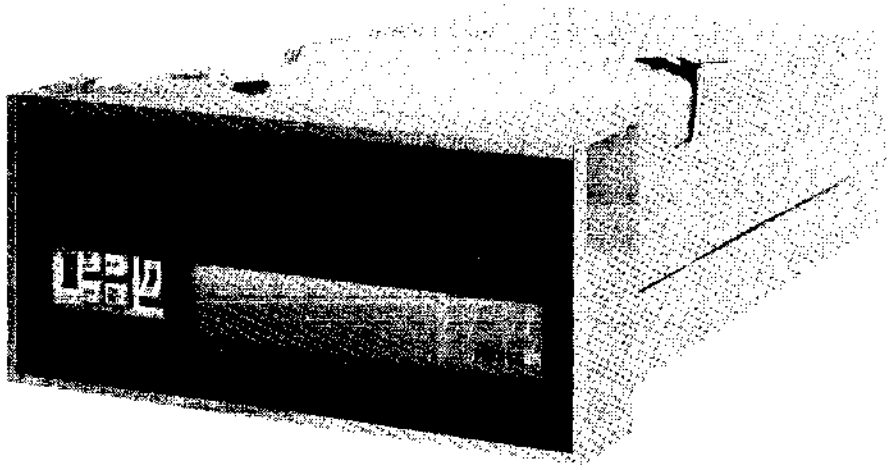


Figure 1-2. D3000 Disk Drive, Top Load Model

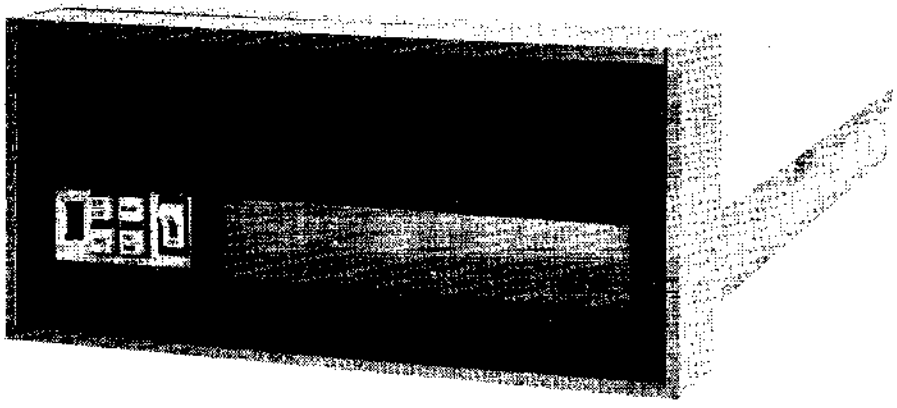


Figure 1-3. D3000 Disk Drive, Front Load Model

All electrical and mechanical components necessary to operate the disk drive are mounted internally within the housing of the drive. The housing is designed to be mounted in a standard 19-inch EIA rack, or utilized as a table top unit.

All models are equipped with the necessary electronics to provide recording and retrieval of stored data.

Access to the interior of the disk drive is gained by removing the dust cover. This cover is mounted to the base assembly and protects the interior of the drive from dust and other environmental contaminants.

The operational controls, which include indicators that are illuminated when the relevant functions are being performed, are mounted on the front control panel. These controls are accessible to the operator at all times. Power is supplied through a strain-relieved cord having a standard 3-prong plug. Interface signals are routed through the interface cables to input/output connectors located within the disk drive housing.

The major electronic assemblies are located near the rear of the drive. These assemblies are mounted to allow ready access without the use of extender cards or other special tools.

1.4 FUNCTIONAL DESCRIPTION

Data storage is accomplished by utilizing the non-contact method of magnetic recording. The disk recording media is rotated at a constant speed and the recording heads, capable of either reading or writing, are flown over the surface of the disk on a gas film bearing and positioned to the appropriate track by the use of a voice coil type of linear motor positioner. This type of disk drive, which utilizes a single head per surface, is referred to as a moving head disk drive.

Addressing of the stored data is accomplished by means of specifying the desired head position and the applicable segment of the disk surface. The read/write electronics are capable of non-simultaneous reading or writing of data on a single surface at a given time.

Figure 1-4 is a functional block diagram of the disk drive, which consists of the disk drive control logic, start and stop control plus auxiliary controls such as the brush cleaning cycle for top loading machines, and the necessary select and enable gating.

The positioner servo electronics comprise a major functional block. As the disk rotates at a fixed speed, and the recording heads are flown over the disk surface, the positioner is controlled in both the velocity and position modes. The positioner moves to the correct address under control of the positioner servo control electronics. Data are then written on the desired surface by selecting the corresponding head through the head select network.

The read/write electronics are sub-divided into three functional blocks consisting of the head select network, the write electronics, and the read channel. Write data causes write current to be switched according to the pulse train on the WRITE DATA SIGNAL line. The storage surface will then be magnetized accordingly.

During retrieval of the stored data the corresponding head is again selected by the head select network and the signal obtained from the read/write head is processed by the read channel into separate READ DATA and READ CLOCK signals for transmission via the interface. The particular segment of the disk which is passing under the read/write head is specified by the sector pulse and sector count lines from the sector electronics.

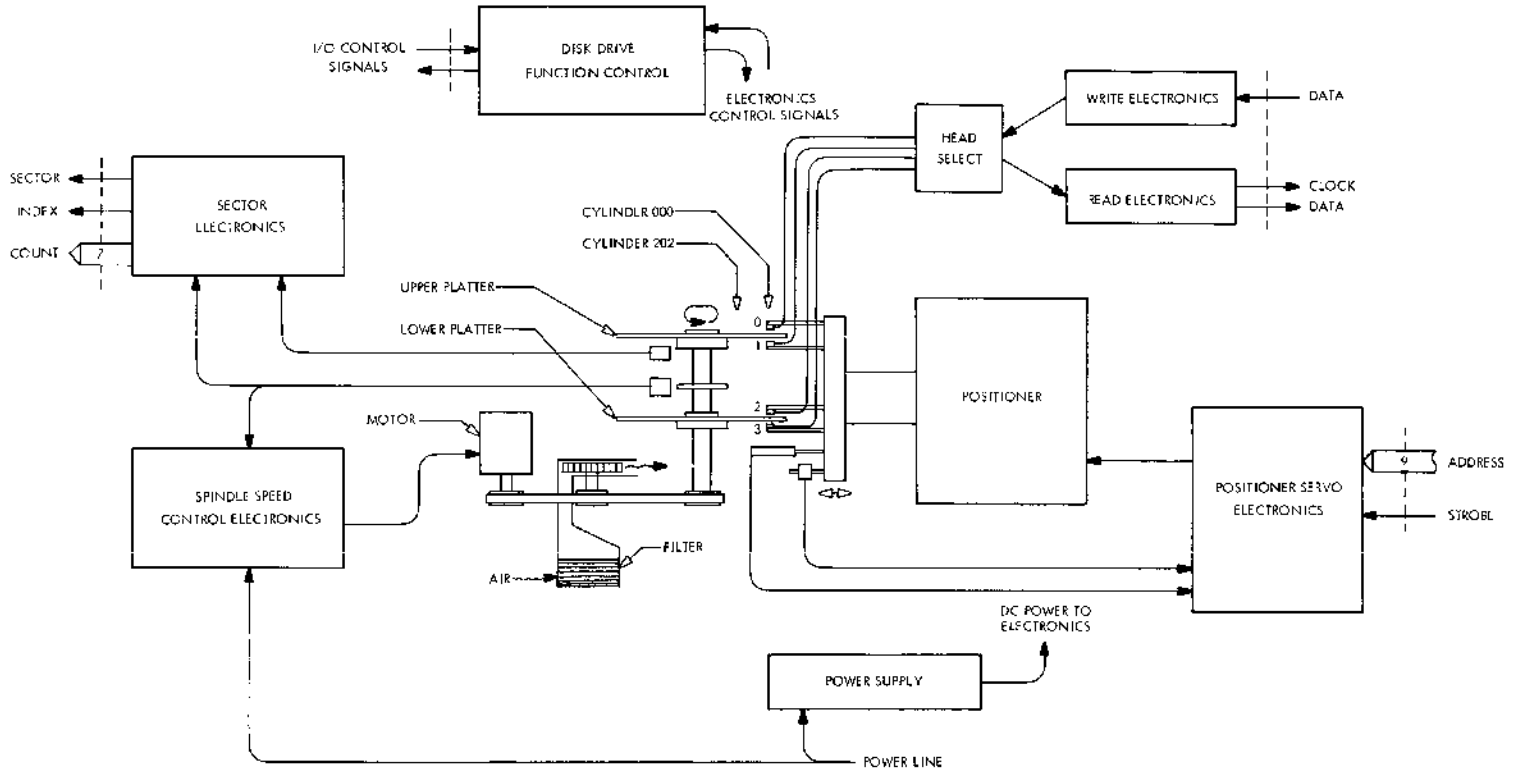


Figure 1-4. Functional Block Diagram

Control of the rotational speed of the disk is accomplished by the speed control electronics group which establishes a known, fixed speed for the disk rotation within ±1 percent speed tolerance. The sector electronics block provides pulses at the interface which electrically subdivides the disk into a number of sectors for the purpose of addressing data stored on the disk. Figure 1-5 illustrates the subdivision of a platter into 8 sectors by means of mechanical sectoring.

The air system consists of an absolute filter preceded by a pre-filter, and a blower driven by the same motor which provides drive to the disk spindle. This air system provides a well-filtered flow of clean air in the disk area to remove contaminants.

Power to the various electronic circuits is provided by an integral power supply. This power provides dc voltages at suitable levels derived from the line voltage.

All major components are mounted to the base assembly. An aluminum alloy casting is the basic component of the base assembly. Mounted onto the casting is the drive mechanism which consists of a precision spindle, an ac induction drive motor, a squirrel cage blower, and an idler system. Power to rotate the blower and spindle is transmitted from the drive motor by means of a flat belt. The idler system provides constant tension of the belt and compensates for stretch of the belt.

Mounted to the spindle assembly is a ring with equally spaced notches and one additional notch spaced midway between two of the other notches; this is referred to as the Phase Lock Ring and is used for sectoring and speed control.

In dual disk models, a fixed disk is mounted to the spindle assembly; it is referred to as the lower platter and is not removable in the same manner as the cartridge.

The disk is contained within the removable cartridge and is driven by a magnetic clutch which is located on top of the spindle assembly. A precision ground cone on the end of the spindle suitably locates the hub of the disk which is mounted in the cartridge. Rotary motion is imparted to the removable disk (upper platter).

The blower is rotated while the drive motor is running and the disk is spinning. Air flow from the blower travels through the disk area and purges the air of any contaminants in this area. Air is drawn in at the lower front part of the front bezel and passes through a high efficiency absolute filter located in the lower front portion of the base assembly.

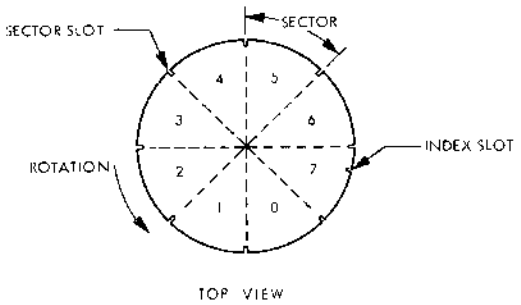


Figure 1-5. Mechanical Sectoring

Air is ducted to the squirrel cage blower and thence to the area below the fixed disk. Suitable vanes on the spindle provide additional pumping action to cause air to flow into the area of the upper platter. Air is exhausted at the rear of the disk drive. As a function of exhausting the air, the electronics package is provided with suitable cooling.

Additional cooling is provided through convection cooling of the heatsink assemblies mounted at the rear of the base assembly. Power transistors mounted on these heatsink assemblies are used in the power supply regulators and the positioner power amplifiers.

The base assembly provides mounting attachment points for the rack mounting slides, switch brackets, front bezel, and the supporting structure for the printed circuit boards and dust cover.

The positioner, in conjunction with the positioner servo and control electronics, is used to position the read/write heads to one of a possible 203 or 406 cylinders. Figure 1-6 defines the relationship between platter, cylinder, and track as used throughout this document.

The positioner assembly consists of a large permanent magnet, a carriage which utilizes ball bearings, a magnetic velocity transducer, and a photo-electric position transducer. Attached to the carriage are the read/write heads, and the positioner coil (voice coil).

The positioner is a moving coil type of linear motor wherein the signal applied to the coil results in a magnetic field which reacts with the magnetic field of the permanent magnet. The force thus produced is used for purposes of controlling the position of the carriage. Speed of the positioner carriage movement is controlled by sensing its instantaneous velocity utilizing the magnetic velocity transducer.

The magnetic velocity transducer consists of a moving magnet within a fixed coil. The position of the positioner carriage is sensed by using the optical detent type of position transducer.

NOTE

There is no actual mechanical detenting of the positioner carriage. The positioning at a given cylinder is achieved entirely by electronic techniques.

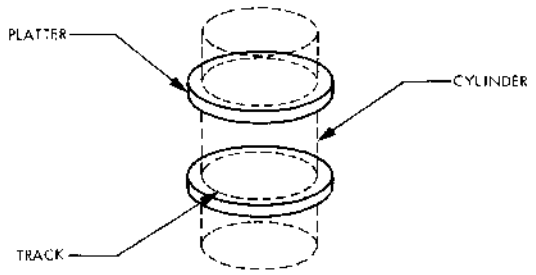


Figure 1-6. Platter, Cylinder, Track Relationship

DC power to various electronic circuits is provided by the power supply which takes the line voltage input, transforms it to a suitable voltage level, then rectifies and filters the output of the transformer. The output is then provided to the power regulators located on the Servo PCBA.

Also contained on the power supply assembly are the motor start capacitors for the ac induction drive motor and a small Motor Control PCBA. The Motor Control PCBA contains ground isolation and power control circuitry for operating the drive motor. This PCBA is separate from other PCBAs in order to isolate the line voltage.

1.5 MECHANICAL AND ELECTRICAL SPECIFICATIONS

The mechanical and electrical specification summary for the disk drive is shown in Table 1-1.

1.5.1 INTERFACE SPECIFICATIONS

Levels:

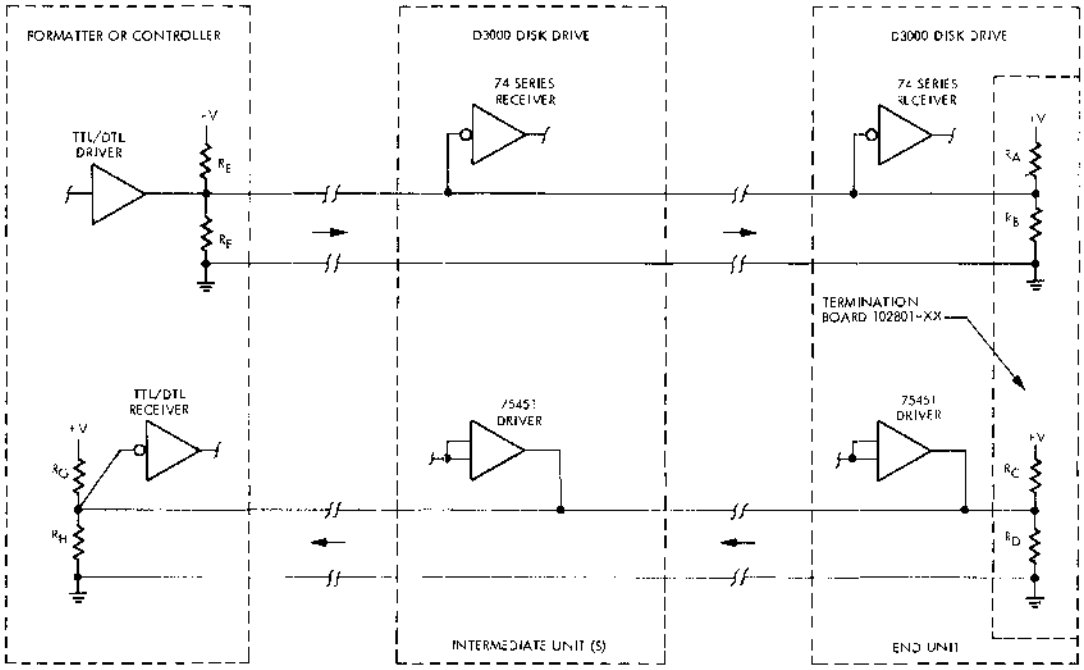
True = Low = +0.2 ±0.2v
False = High = +3.0 +2.3 —0.6v

The interface circuits are designed so that any disconnected wire results in a false signal.

Figure 1-7 shows the configuration for which the transmitters and receivers have been designed.

Table 1-1
Mechanical and Electrical Specifications

	100 tpi Models	200 tpi Models
Storage Capacity (Unformatted)		
Single Disk Models at 2200 bpi	25.3750 megabits	50.75 megabits
Dual Disk Models at 2200 bpi	50.750 megabits	101.5 megabits
Cylinders/Tracks		
Single Disk Models	203 cylinders/406 tracks	406 cylinders/812 tracks
Dual Disk Models	203 cylinders/812 tracks	406 cylinders/1624 tracks
Sectors	6, 8, 10, 12, 14, 16, 18, 20, 24, 28, 30, 32, 36, 40, 42, 48, 56, 60, 64	6, 8, 10, 12, 14, 16, 18, 20, 24, 28, 30, 32, 36, 40, 42, 48, 56, 60, 64
Bits per Inch/Tracks per Inch	2200 bpi/100 tpi	2200 bpi/200 tpi
Data Transfer Rate		
2200 bpi, 1500 rpm	1.56250 megabits per second	1.56250 megabits per second
2200 bpi, 2400 rpm	2.50000 megabits per second	2.50000 megabits per second
Disk Speed	1500 or 2400 rpm (±1%)	1500 or 2400 rpm (±1%)
Latency Time (Average)		
1500 rpm Models	20 milliseconds (±1%)	20 milliseconds (±1%)
2400 rpm Models	12.5 milliseconds (±1%)	12.5 milliseconds (±1%)
Head Positioner	Voice Coil Linear Motor with Optical Detent	Voice Coil Linear Motor with Optical Detent
Seek Time		
Adjacent Track	9 milliseconds maximum	10 milliseconds maximum
Average (One-third Stroke)	35 milliseconds maximum	40 milliseconds maximum
Maximum (Full Stroke)	60 milliseconds maximum	65 milliseconds maximum
Start Time	57 seconds maximum	57 seconds maximum
Stop Time	22 seconds maximum	22 seconds maximum
Removable Media Type	IBM 5440 or 2315 type Cartridge	IBM 5440 or 2315 type cartridge
Read/Write Heads		
Type	Ramp Loaded, Radially Aligned	Ramp Loaded, Radially Aligned
Number	2 or 4 (One per Disk Surface)	2 or 4 (One per Disk Surface)
Recording Mode	Double Frequency	Double Frequency
Dimensions		
Height	8¾ inches maximum	8¾ inches maximum
Width	19 inches	19 inches
Depth from Mounting Surface	26 inches	26 inches
Front Projection from Mounting Surface	3⅛ inches	3¼ inches
Total Depth	29¼ inches	29¼ inches
Mounting	Standard 19-inch EIA	Standard 19-inch EIA
Weight (Excluding Slides and Cartridge)		
Top Loading Models	116 pounds (Including Integral Power Supply)	116 pounds (Including Integral Power Supply)
Front Loading Models	112 pounds (Including Integral Power Supply)	112 pounds (Including Integral Power Supply)
Operating Temperature	10°C (50°F) to 40°C (104°F)	15.6°C (60°F) to 38.0°C (100°F)
Non-Operating Temperature	−10°C (14°F) to 65°C (149°F)	−10°C (14°F) to 65°C (149°F)
Operating Humidity	5% to 85% Non-Condensing	5% to 85% Non-Condensing
Storage Humidity	to 95% Non-Condensing at 40°C to 80% Non-Condensing at 65°C	to 95% Non-Condensing at 40°C to 80% Non-Condensing at 65°C
Operating Altitude	0 to 7500 feet	0 to 7500 feet
Non-Operating Altitude	0 to 20,000 feet	0 to 20,000 feet
Power		
Volts ac	95, 100, 110, 115, 125, 190, 200, 210, 215, 220, 225, 230, 235, 240, 250	95, 100, 110, 115, 125, 190, 200, 210, 215, 220, 225, 230, 235, 240, 250
Watts (Maximum on High Line) (Typical)	1100 Peak (Start/Stop Cycles Only) 400	1100 Peak (Start/Stop Cycles Only) 400
Hertz	48 to 52, and 58 to 62	48 to 52, and 58 to 62
Electronics	All Silicon	All Silicon
Underwriters Laboratory	UL Approved	UL Approved
Canadian Standard	Designed to Qualify for CSA Approval	Designed to Qualify for CSA Approval



D3000 INSTALLATION CONFIGURATION	USE TERMINATION BOARD PART NO.	CORRESPONDING VALUES AT D3000 DISK DRIVE					TYPICAL VALUES AT CONTROLLER					NOTES AND COMMENTS
		R_A	R_B	R_C	R_D	+V	R_E	R_F	R_G	R_H	+V	
D3000 STANDARD MULTIPLE UNIT INSTALLATION (DAISY CHAIN)	102801-03	220	330	220	330	+5.0	220	330	220	330	+5.0	MAY ALSO BE USED FOR SINGLE UNIT INSTALLATION
D3000 STANDARD SINGLE UNIT INSTALLATION	102801-02	220	330	NONE	NONE	+5.0	NONE	NONE	220	330	+5.0	
COMPATIBLE WITH D5000 DAISY CHAIN TYPE INTERFACE	102801-04	120	NONE	120	NONE	+3.5	120	NONE	120	NONE	+3.5	
COMPATIBLE WITH D5000 SINGLE UNIT TYPE INTERFACE	102801-05	270	NONE	120	NONE	+3.5	160	NONE	120	NONE	+3.5	
D3000 STANDARD MULTIPLE UNIT INSTALLATION, EXTERNAL VOLTAGE (DAISY CHAIN)	102801-06	220	330	220	330	+5.0	220	330	220	330	+5.0	MAY BE USED FOR SINGLE UNIT INSTALLATION
SPECIAL DESIGN BY CUSTOMER	102801-01											ORDER DRAWINGS: 102800, 102804, 102835, 102836, 102841, 102770

Figure 1-7. Interface Configuration

SECTION II
INSTALLATION AND INITIAL CHECKOUT

2.1 INTRODUCTION

This section contains a summary of interface lines, information for uncrating and mounting the unit, as well as the procedure for electronically connecting and initially checking out the disk drive.

2.2 UNCRATING THE DISK DRIVE

The D3000 Disk Drive is shipped in a heavy duty container consisting of an inner and outer carton. Use of the dual carton minimizes the possibility of damage during shipment. To uncrate the disk drive:

(1) Place the shipping container in the position indicated by the arrows on the outer carton.

(2) Open the outer carton and remove the packing material.

(3) Lift the drive and its shipping frame and set it on a clean work surface. Ensure access to the top of the unit.

CAUTION

THE D3000 DISK DRIVE WEIGHS 130 POUNDS IN ITS SHIPPING CONFIGURATION. DO NOT ATTEMPT TO LIFT THE DRIVE WITHOUT SUFFICIENT PERSONNEL.

(4) Check the contents of the shipping container against the packing slip and investigate for possible damage. Notify the carrier if damage is noted.

CAUTION

TO AVOID DAMAGE TO EQUIPMENT, DO NOT ATTEMPT TO APPLY POWER TO THE DISK DRIVE UNTIL ALL POSITIONER AND MECHANISM SHIPPING RESTRAINTS HAVE BEEN REMOVED.

(5) Remove the polyethylene bag that surrounds the unit; remove the dust cover as follows.

- ☐ Top Load Models
  - (i) Remove the 8 screws around the adapter bowl.
  - (ii) Remove the 5 screws along the sides of the unit.
  - (iii) Lift the rear of the dust cover approximately 30°, then carefully move the cover toward the rear of the unit until the front edge of the cover clears the bezel.
  - (iv) Remove the dust cover.
- ☐ Front Load Models
  - (i) Remove the 2 screws on top of the dust cover.
  - (ii) Remove the 5 screws along the sides of the unit.
  - (iii) Slide the dust cover toward the rear of the unit until the front edge clears the bezel.
  - (iv) Remove the dust cover.
  - (v) Remove the tie-down strap used to secure the front door and cartridge receiver during shipment. Figure 2-1 shows the relationship of these restraints to the shipping frame and disk drive.

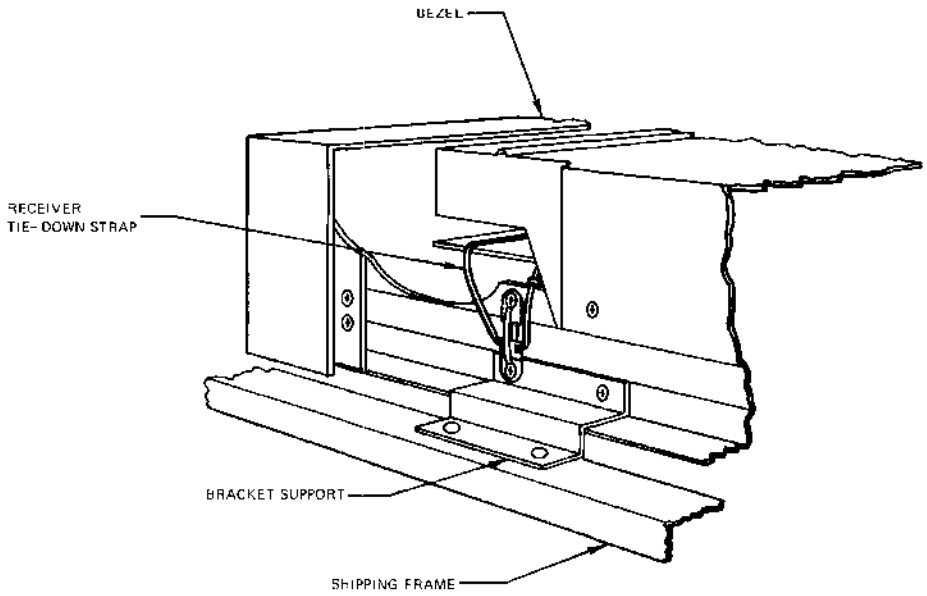


Figure 2-1. Cartridge Receiver and Front Door Shipping Restraints

(6) Locate and loosen the two captive screws (shown in Figure 2-2) on top of the Logic PCBA; rotate the hinged card structure up and to the rear. The spring-loaded PCBA pivot-lock will automatically lock the Logic PCBA into the vertical position as shown in Figure 2-3.

NOTE

Illustrations used in this manual to depict parts and locations which are common to front and top loading versions will normally be of front loading models.

(7) Loosen the two captive screws which secure the Servo PCBA to the Logic PCBA (see Figure 2-3).

(8) Swing the Servo PCBA into its extended position; engage the locking pin and the PCBA support bracket (see Figure 2-4).

(9) Remove the protective plastic tube from the upper positioner shaft. Care must be taken to ensure that the precision surface of the shaft is not scored or scratched during this operation.

NOTE

The plastic tube should be saved as it will be needed if the unit is to be shipped again.

(10) Check that the identification label on the rear of the unit bears the correct model number, line voltage, and line frequency. If the actual line voltage or frequency at the installation differs from that on the identification label, refer to Section IV of this manual.

CAUTION

OPERATOR MUST EXERCISE CAUTION WHEN EXTENDING OR LOWERING THE LOGIC AND SERVO PCBAS TO AVOID CRIMPING CABLING AND/OR DISENGAGING MOLEX CONNECTORS.

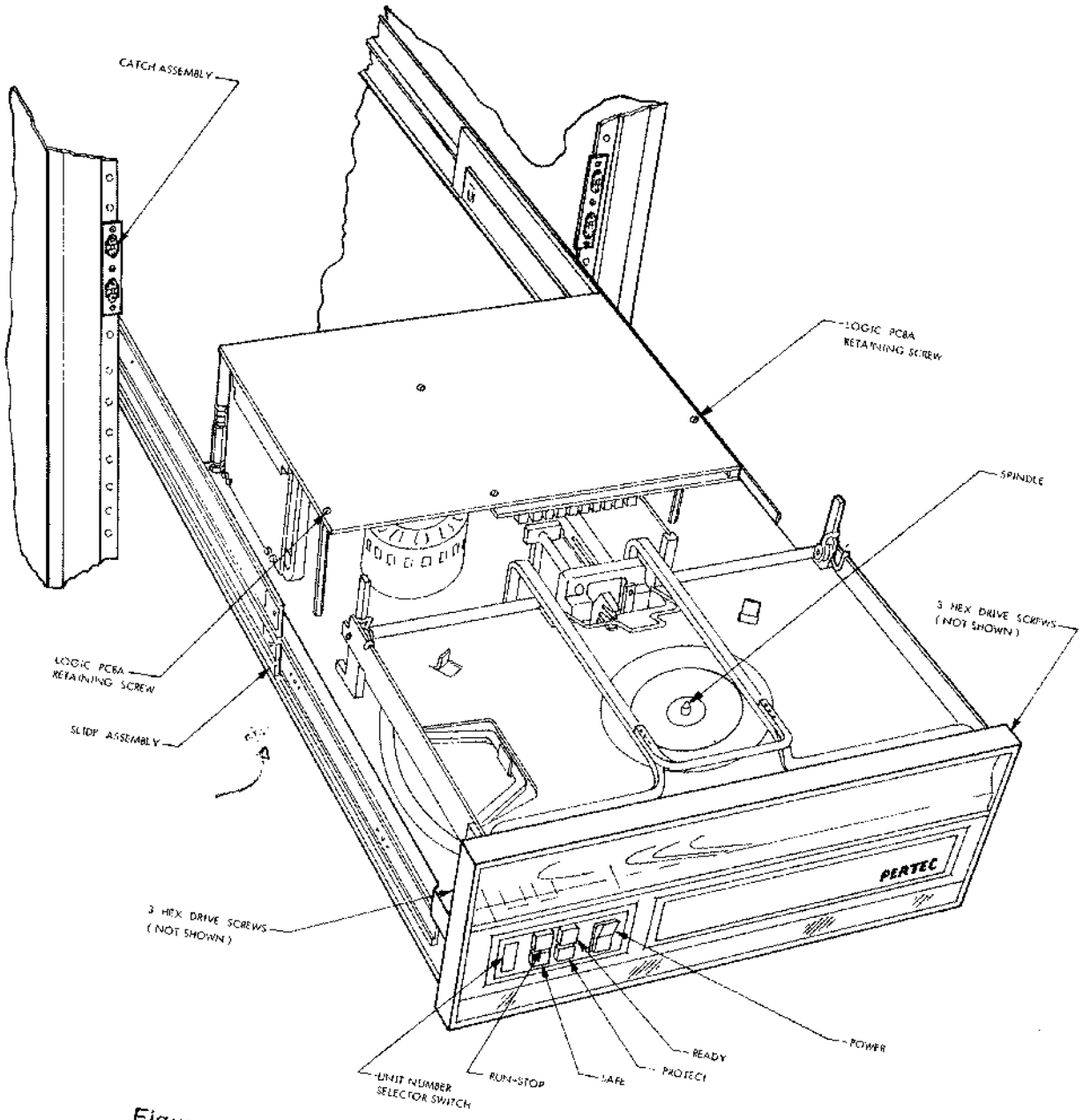


Figure 2-2. Rack Mounting the D3000 Disk Drive

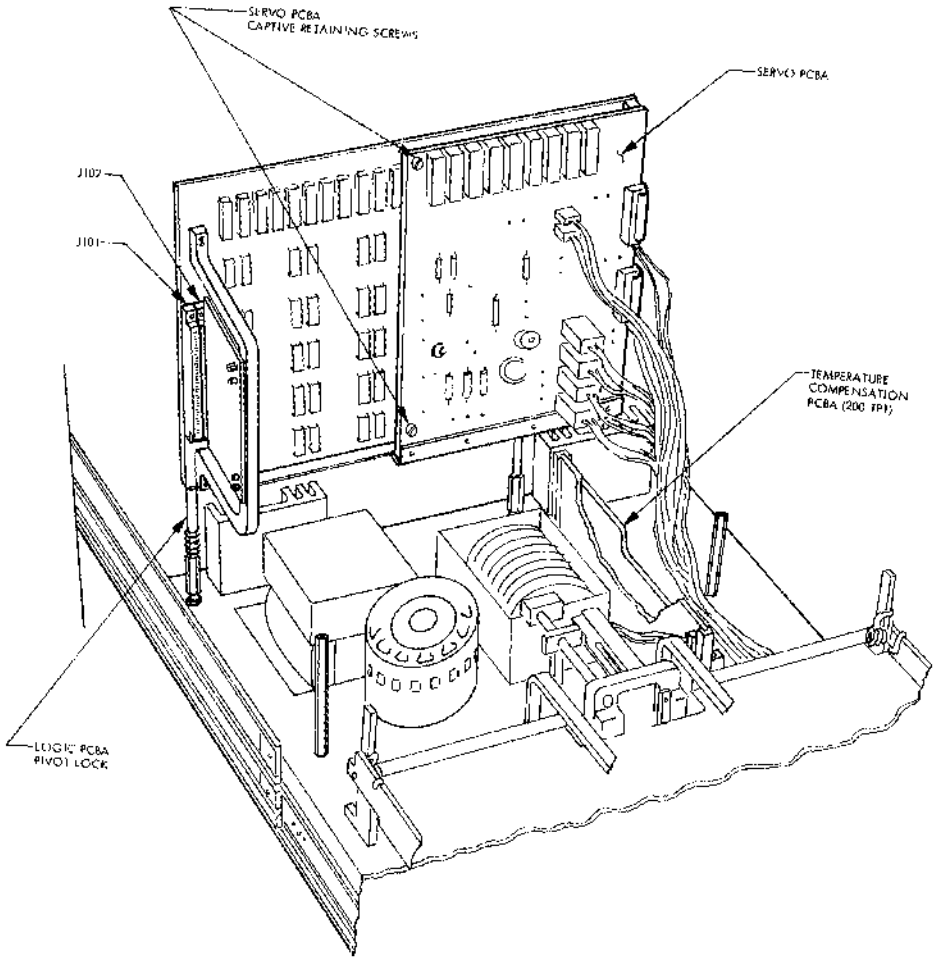


Figure 2-3. Component Identification, Logic and Servo PCBAs Extended

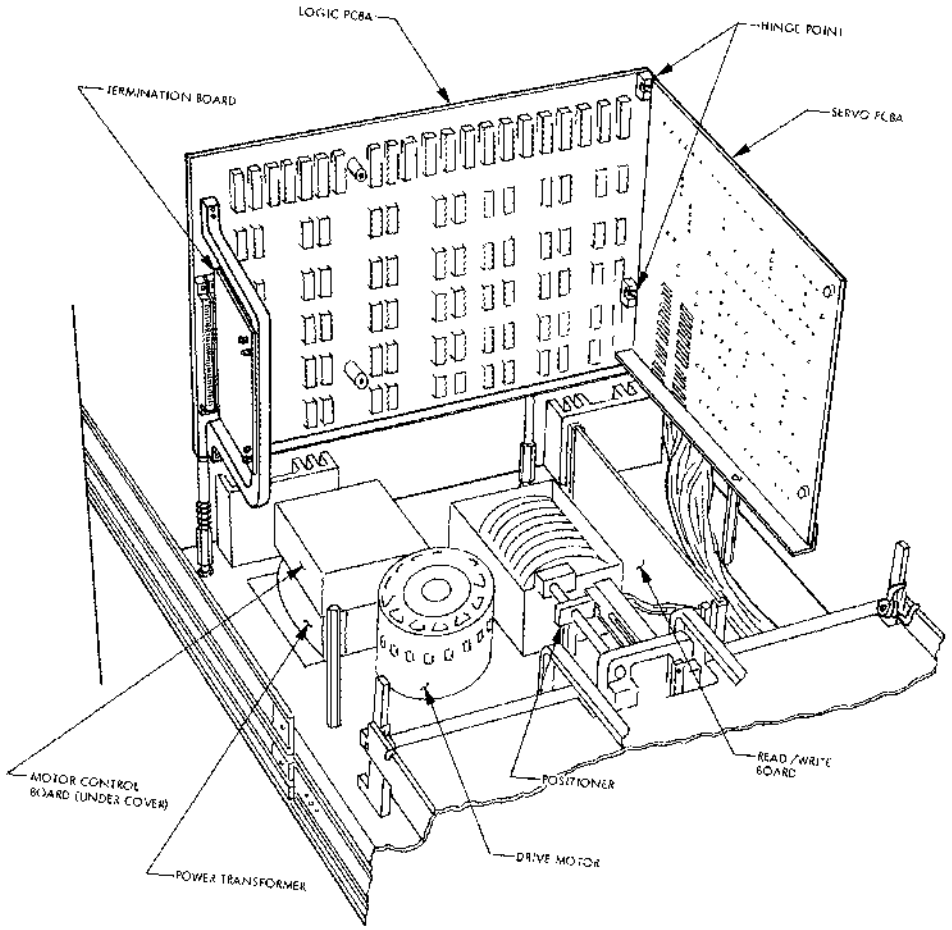


Figure 2-4. Component Identification

2.3 POWER CONNECTIONS

A fixed power cord is supplied for use in a polarized 115v outlet. For other power sockets, the supplied plug must be removed and the correct plug installed. Table 2-1 lists (in several languages) the color code scheme used to identify the supplied power cord.

Table 2-1

Power Cord Color Code

Black AC 'Hot' (Live)	**Noir** Phase	**Nero** Vivo	**Schwarz** Heiss
White AC Ret. (Neutral)	**Blanc** Neutre	**Bianco** Neutro	**Weiss** Neutral
Green Chassis GND (Earth)	**Vert** Chassis (Terre)	**Verde** Terra	**Grun** Grund

2.4 INITIAL CHECKOUT PROCEDURE

A description of the controls and indicators used for operation of the D3000 Disk Drive is contained in Section III. To check the proper operation of the disk drive before placing it in a system, the following procedure should be performed.

(1) With the protective dust cover removed and with the Servo PCBA in the raised position (as shown in Figure 2-4), inspect the printed circuit boards, connectors, and cables. Verify that shipping damage has not occurred. Check the connectors and plug-in relay for proper installation.

(2) Verify that the positioner is in the fully retracted position.

(3) Verify that the cartridge area is free of dirt, contaminates, and shipping material.

(4) Verify that the power ON/OFF switch is set to OFF.

CAUTION

CONNECTING THE DISK DRIVE TO A LINE VOLTAGE OTHER THAN THE VOLTAGE SELECTED VIA THE TRANSFORMER TAPS CAN RESULT IN DAMAGE TO THE UNIT.

(5) Verify that connections to the power transformer are compatible with the local power source to which the disk drive is to be connected (see Paragraph 4.9); connect the power cord to the correct line voltage.

(6) Place the power ON/OFF switch to the ON position; the ON indicator and the SAFE indicator should illuminate within 2 seconds.

CAUTION

ON TOP LOAD MODELS, IF CARTRIDGE LOCK ARMS ARE PIVOTED OUT OVER THE BOWL, DO NOT ATTEMPT TO ROTATE LOCK ARMS TO THEIR STORED POSITION UNTIL POWER IS APPLIED AND THE ON/OFF SWITCH IS IN THE ON POSITION.

(7) Load the cartridge as described in Paragraph 3.4.1 or 3.4.3.

CAUTION

LOADING AND OPERATING WITH DIRTY, DAMAGED, OR DEFECTIVE CARTRIDGES WILL CAUSE DAMAGE TO THE DISK DRIVE.

(8) Depress and release the RUN/STOP switch/indicator; verify that, during the Start sequence:

- The RUN/STOP indicator becomes illuminated immediately.
- The SAFE indicator is extinguished.
- The disk comes up to speed.
- The cleaning brush sweeps the disk(s) (top load versions only).
- The positioner loads the heads over the disk(s).
- The READY indicator becomes illuminated within 60 seconds after actuation of the RUN/STOP switch/indicator.

(9) Depress and release the RUN/STOP switch/indicator; verify that, during the Stop sequence:

- The READY and RUN/STOP indicators are extinguished.
- The heads are slowly unloaded from over the disk(s).
- The disk(s) come to a stop.
- The SAFE indicator becomes illuminated within 25 seconds after RUN/STOP is actuated.

(10) Repeat Step (8) to return the disk drive to the Ready condition.

(11) Place the power ON/OFF switch to the OFF position; verify that:

- The positioner immediately retracts the heads from over the disk(s) at a high rate of speed (emergency unload).
- The cartridge access door is locked (front load models); the cartridge lock arms are locked (top load models).

(12) Before the disk has the opportunity to coast to a stop, place the power ON/OFF switch to the ON position; verify that the SAFE indicator does not become illuminated until after the disk(s) has coasted to a stop.

(13) Remove the cartridge as described in Paragraph 3.4.2 or 3.4.4.

(14) Place the power ON/OFF switch to the OFF position.

(15) Position the Servo PCBA in the closed position and secure it to the Logic PCBA with the two captive retaining screws (shown in Figure 2-3).

(16) Slide the spring-loaded sleeve of the Logic PCBA pivot lock downward to release the pivot lock (see Figure 2-3).

CAUTION

OPERATOR MUST EXERCISE CAUTION WHEN EXTENDING OR LOWERING THE LOGIC PCBA AND SERVO PCBA TO AVOID CRIMPING CABLING AND/OR DISENGAGING MOLEX CONNECTORS.

(17) Lower the Logic PCBA and secure it to the PCBA support brackets using the two captive retaining screws (shown in Figure 2-2).

2.5 INTERFACE CONNECTIONS

The D3000 interface is configured to provide flexibility in the design of new controllers and remain compatible with existing controllers designed for the D5000 Disk Drive. The D3000 will also operate in conjunction with the F3000 Disk Formatter.

The 3M flat cable used in the fabrication of the D3000 Input/Output (I/O) cables has the following specifications.

(1) Number of conductors: 36

(2) Conductor size: 24

(3) Impedance: 100 ohm

The maximum length of conductor between the D3000 and the Controller/Formatter in a multiple disk drive installation is 20 feet. The maximum length of conductor between adjacent disk drives in a daisy-chain configuration is 10 feet.

D3000 Disk Drives are normally supplied with a mating input/output cable board and a termination board. These boards must be installed as shown in Figure 2-5. Interface signals are routed to and from the disk unit via the input/output cable board. Table 2-2 shows the input/output lines required. Details of the interface are contained in Section III.

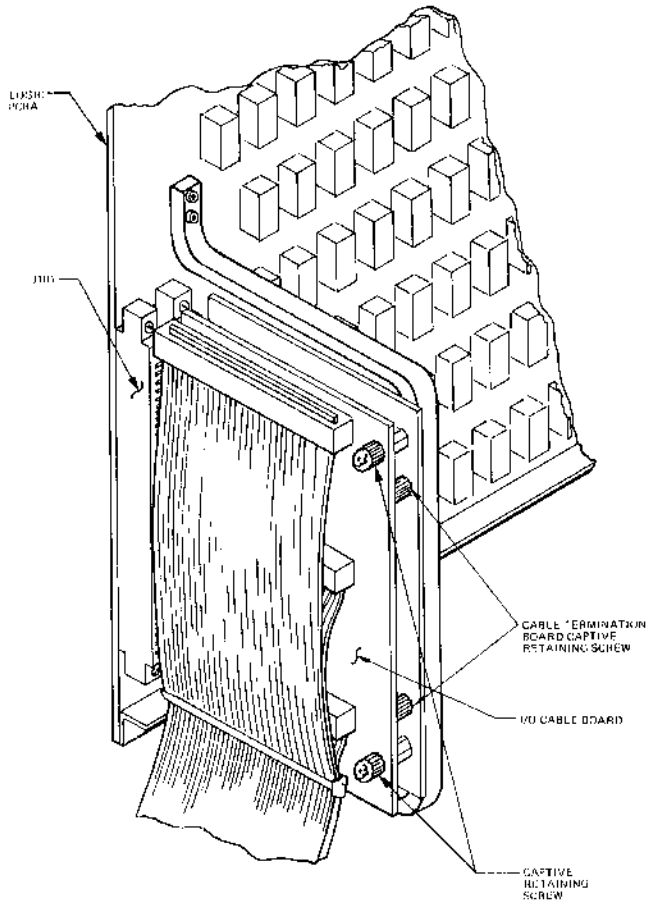


Figure 2-5. Interface Connector Board Installation

Table 2-2
Interface Input/Output Lines

Signal Name	Term	Signal Pin	Return Pin	Remarks
Inputs				
UNIT SELECT NO. 1	IUS1R	B42	B41	
UNIT SELECT NO. 2	IUS2R	A42	A41	
UNIT SELECT NO. 3	IUS3R	B43	B44	
UNIT SELECT NO. 4	IUS4R	A43	A44	
PLATTER SELECT	IPSXR	B27	B26	
HEAD SELECT	IHSXR	A27	A26	
STROBE	ISTRR	B33	B32	
TRACK ADDRESS BIT 1	ITA0R	A39	A38	LSB
TRACK ADDRESS BIT 2	ITA1R	B39	B38	
TRACK ADDRESS BIT 4	ITA2R	A37	A38	
TRACK ADDRESS BIT 8	ITA3R	B37	B38	
TRACK ADDRESS BIT 16	ITA4R	A36	A35	
TRACK ADDRESS BIT 32	ITA5R	B36	B35	
TRACK ADDRESS BIT 64	ITA6R	A34	A35	
TRACK ADDRESS BIT 128	ITA7R	B34	B35	
TRACK ADDRESS BIT 256	ITAER	A33	A32	MSB 100 tpi
RESTORE	IRTRR	A31	A32	
WRITE GATE	IWGXR	B22	B23	
ERASE GATE	IEGXR	A22	A23	
WRITE DATA AND CLOCK	IWDXR	A28	A29	
READ GATE	IRGXR	B24	B23	
TRACK OFFSET PLUS	ITOPR	B25	B26	
TRACK OFFSET MINUS	ITOMR	A25	A26	
WRITE PROTECT INPUT	IWPIR	B31	B32	
START/STOP DISK DRIVE	ISSDR	B30	B29	
Total Input Lines: 25				
Outputs				
FILE READY	IRXXD	B1	B2	
READY TO SEEK, READ OR WRITE	ISRWD	B18	B20	
ADDRESS ACKNOWLEDGE	IAAXD	A18	A17	
PSEUDO SECTOR MARK	IPSMD	A3	A2	
SECTOR MARK	ISMXD	A4	A5	
SECTOR BIT 1	ISC0D	A15	A14	LSB
SECTOR BIT 2	ISC1D	B15	B14	
SECTOR BIT 4	ISC2D	A13	A14	
SECTOR BIT 8	ISC3D	B13	B14	
SECTOR BIT 16	ISC4D	A12	A11	
SECTOR BIT 32	ISC5D	B12	B11	
SECTOR BIT 64	ISC6D	A10	A11	MSB
INDEX MARK	IIMXD	B4	B5	
READ CLOCK	IRCXD	B16	B17	
READ DATA	IRDXD	A16	A17	
LOGICAL ADDRESS INTERLOCK	IAIXD	B3	B2	
WRITE PROTECT STATUS	IWPSD	A1	A2	
WRITE CHECK	IWCKD	B6	B5	
DUAL PLATTER DRIVE	IDPDD	B7	B8	
SEEK INCOMPLETE	ISIXD	B28	B26	
HIGH DENSITY INDICATION	IHDID	A30	A29	
Termination Voltage		A45 B45		
Total Output Lines: 21				

There are three cable types available for use with the D3000 Disk Drives.

(1) Controller to Disk Drive cable for a non-specified controller. This cable is 3M flat cable with an input/output cable board on one end to mate with the D3000; the other end is free to accommodate connection to a controller input/output board. This cable is available from PERTEC in lengths of 5, 10, and 20 feet; refer to the Spare Parts List, Table 7-8, for specific part numbers.

(2) I/O Link cable (daisy-chain). This cable is 3M flat cable with an input/output cable board on each end to join two D3000 drives. This cable is available from PERTEC in lengths of 5, 7, and 10 feet; refer to Spare Parts List, Table 7-8, for specific part numbers.

(3) F3000 Formatter cable. This cable is 3M flat cable with an input/output cable board on one end to mate with a D3000 drive and an input/output cable board on the other end to mate with an F3000 Formatter. This cable is available from PERTEC in lengths of 5, 10, and 20 feet; refer to Spare Parts List, Table 7-8 for specific part numbers.

2.6 RACK MOUNTING THE DISK DRIVE

The disk drive is entirely self-contained (including the power supply). The unit is 8¾ inches high, requires 26 inches of rack depth, and extends 3¼ inches from the front mounting surface. The unit is designed to be mounted in any equipment rack or desk having standard EIA mounting rails at the front and rear. Mounting for two slide configurations is described.

All models are supplied with heavy duty chassis slides, carefully selected to give the optimum in unit serviceability. When mounted in the rack the chassis may be extended fully forward for servicing; where servicing from the front is not practical the unit may be extended from the rear.

CAUTION

DUE TO THE WIDE RANGE OF SLIDE TRAVEL, A CABINET OF SUFFICIENT STATURE MUST BE USED TO REDUCE THE POSSIBILITY OF UPSETTING THE CABINET WHEN THE UNIT IS FULLY EXTENDED TO THE FRONT OR REAR. REFER TO DWG NO. 103587 [SECTION VII] FOR CG LOCATIONS AT THESE EXTREMES BEFORE INSTALLING THE UNIT.

2.6.1 SLIDES

Remove the slide set (Part No. 102731 or 103670) and the installation kit (Part No. 102723) from the shipping container. (Slide set Part No. 102731 extends the disk drive 30.0 inches to the front and 25.0 inches to the rear of the cabinet; slide set Part No. 103670-01 extends the disk drive 19.25 or 29.5 inches to the front or rear.)

2.6.2 INSTALLATION OF SLIDE SET PART NO. 102731

Refer to Figure 2-2 and Drawing No. 103587 in conjunction with the following mounting procedure. The front and rear slide brackets and the slides are marked 'LH' and 'RH' for correct assembly.

CAUTION

TO EXTEND THE DISK CHASSIS FROM THE REAR OF THE CABINET THE BEZEL MUST BE REMOVED; REFER TO PARAGRAPH 2.6.2, STEP [4].

(1) Assemble the front and rear right-hand brackets to the right-hand slide assembly; assemble the front and rear left-hand brackets to the left-hand slide assembly. The bracket screw heads must be installed on the track side of the slide; the nuts will therefore appear on the bracket side, or outside, of the slide assembly. Use lock washers under the nuts.

(2) Install the right and left slide assemblies to the front and rear EIA rails. Adjust the distance between the slide brackets to 17.78 inches. Ensure that the right front and rear slide brackets, as well as the left slide brackets, are installed at the same height as on the front and rear rails. The screw heads must be on the outside of the EIA rails.

(3) Pull the smaller chassis slide member forward to expose the screw holes that will be used to attach the small slide member to the disk chassis.

(4) Remove the bezel assembly from the disk drive by loosening the three screws on each side of the bezel and sliding the bezel assembly forward until free of the chassis (refer to Figure 2-2 for location of these screws). For clearance, remove the three bezel mounting screws on each side of the chassis.

(5) Remove 8 screws which attach the shipping frame to the disk chassis and lift the unit free of the frame.

(6) With the right and left chassis slides extended fully forward, slide the disk drive chassis between the inner members until the front slide mounting hole pattern lines up with the tapped holes in the chassis. Thread three 8-32 X ¼-inch button-head screws through the slide and into the chassis. Perform this on each side of the chassis.

(7) Slide the unit through the cabinet to the rear and thread two additional 8-32 X ¼-inch button-head screws through the slide and into the chassis on each side.

(8) Locate the chassis in the closed position in the cabinet. Adjust each slide bracket height by loosening the slide bracket screws to obtain the 0.235-inch dimensions as shown in Drawing No. 103587.

(9) Reinstall the bezel.

(10) Install the slide restraining blocks (Part No. 102776) at the rear of the cabinet using the hardware provided. Adjust the restraining blocks to prevent the intermediate slide member from working to the rear during normal operation.

(11) For top loading models only, install the brim (Part No. 102691) using the hardware provided.

(12) Install the catch assemblies as shown in Figure 2-2 using the hardware provided. Adjust the catch spring on the EIA rail so the ball stud assembly installed on the bezel strikes the catch spring on the EIA rail squarely. Apply a small amount of lubricant (PERTEC Part No. 665-0004, or equivalent) to each ball stud.

2.6.3 INSTALLATION OF SLIDE SET PART NO. 103670

Figure 2-6 and Drawing No. 103587 show the relationship of the rail mounting brackets to a standard EIA cabinet and should be referred to in conjunction with the following procedure.

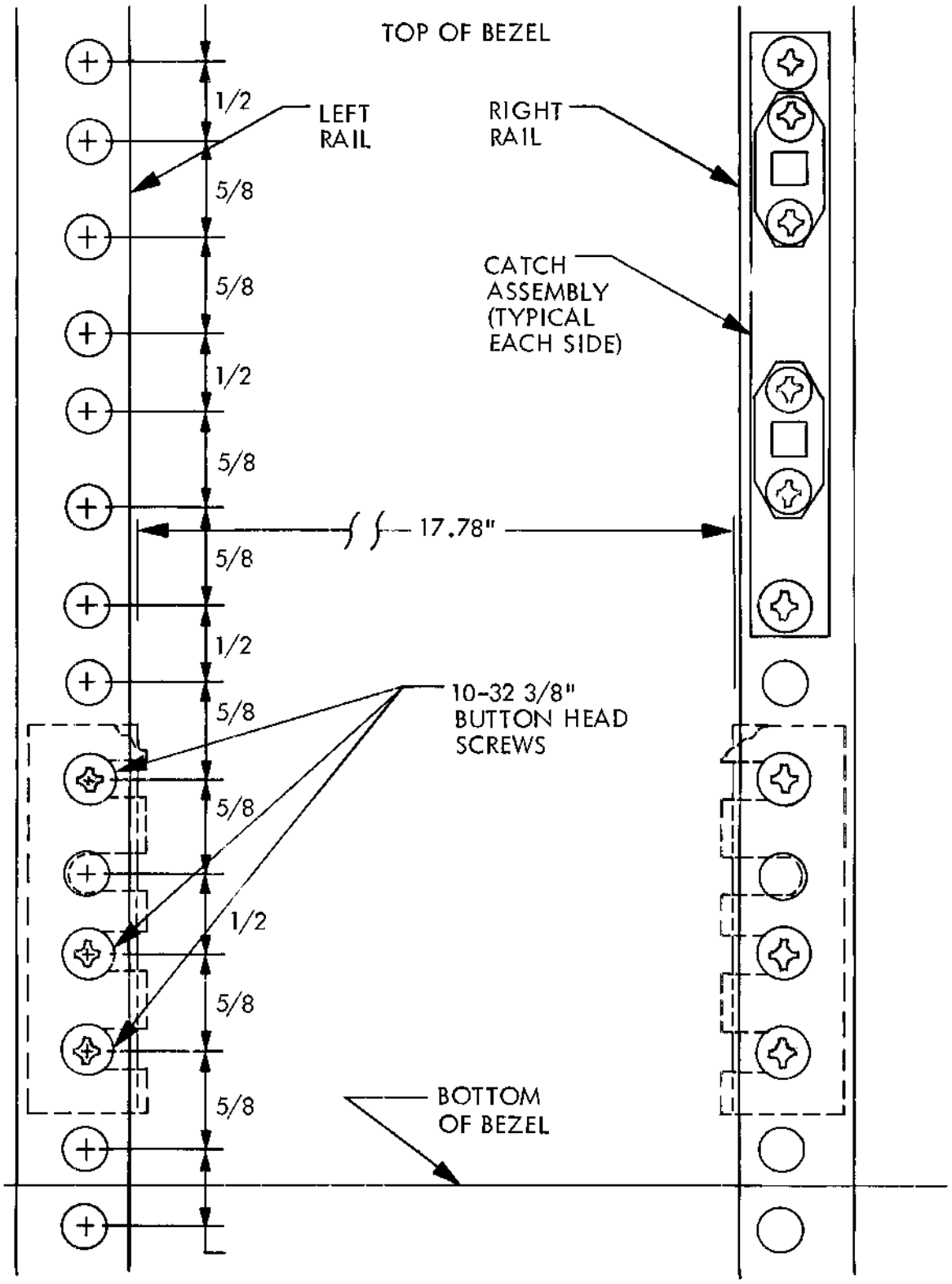


Figure 2-6. Mounting Bracket to EIA Cabinet; Hardware Orientation for use with P/N 103670

Prior to installation of the disk mounting slides, determine the exact location in the cabinet that the disk drive is to be mounted.

NOTE

To ensure correct hole spacing positions for the slide mounting bracket, catch assemblies, and top load brim assembly, the location of the bottom surface of the bezel must lie between a pair of rail holes spaced one-half-inch apart.

(1) Thread and tighten three 10-32 X 3/8-inch button-head Phillips screws for each pair of front and rear brackets into the EIA rails; spacing must be as shown in Figure 2-6.

(2) Place a star lockwasher and 10-32 nut on each of the three screws. The nuts should be started onto the screw only far enough to hold. The mounting bracket will be secured between the back of the EIA mounting surface and the lockwasher.

NOTE

If the cabinet rails have untapped mounting holes, the nut bars furnished in the hardware kit are to be used in place of the 10-32 nuts.

(3) Install the right and left brackets to the rails and tighten the 10-32 nuts sufficiently to hold them in place.

(4) Determine that the bracket surface adjacent to the rail is parallel to the rail and to the side of the cabinet.

(5) Establish that the measurement between the brackets is 17.78 inches as shown in Figure 2-7. Tighten the 10-32 nuts on the right and left brackets. If this measurement is not held the bezel may not fit between the trim molding on the cabinet. Note that dimension 'A' must equal dimension 'B'.

NOTE

Steps [1] through [5] must be repeated when the rear brackets are installed.

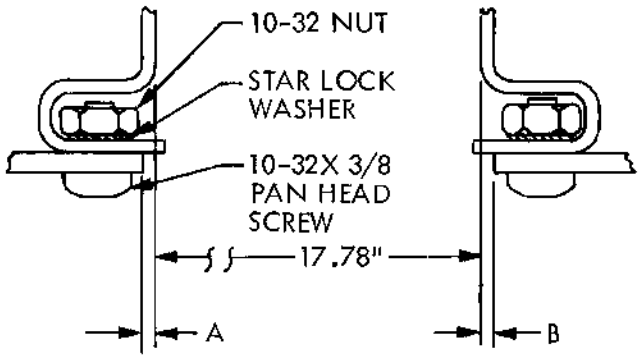


Figure 2-7. Inside Measurement Between Slide Brackets

(6) By inspection, determine which slide assembly and mounting holes will be used for the installation.

(7) Install the slide assemblies to the brackets using 8-32 X 3/8-inch Phillips screws; tighten hardware finger tight.

(8) Extend the small slide bar as far forward as possible to expose two Allen-head stop screws located in the body of the lower slide of the slide assembly.

(9) Loosen the two Allen-head stop screws so that 4 or 5 threads are showing. Move each small slide bar to the extreme rear position (all the way out the rear of the cabinet) to ensure that they do not become disengaged from the main slide assembly.

(10) Remove the small slide bar from the main slide assembly by moving the small slides all the way out the front of the cabinet.

NOTE

The small slide bar will be attached to the disk drive.

(11) Install restraining blocks to each of the rear rails with 10-32 X 3/8-inch Phillips button-head screws. Position each restraining block so that the slide member will be prevented from projecting beyond the rear of the cabinet.

(12) Install the small slides (removed in Step 10) to the right and left sides of the disk drive casting with 8-32 X 3/8-inch button-head Phillips screws.

CAUTION

ENSURE THAT THE DIMPLE ON EACH SMALL SLIDE MEMBER APPEARS BELOW THE CENTERLINE OF THE SLIDE BAR; FAILURE TO DO SO WILL ALLOW THE DISK DRIVE TO BE PULLED FROM THE SLIDE ASSEMBLY.

(13) Extend each cabinet mounted slide assembly fully forward until a mechanical stop is reached.

(14) Install the disk drive to the two main slide assemblies which project from the front of the cabinet by engaging the small slides on the disk drive with each of the extended slide assemblies.

(15) Slide the disk drive into the cabinet to the closed position, i.e., the point at which the bezel is seated against the cabinet rails.

(16) Carefully pull the disk drive forward about 6 inches until the first setscrew is exposed on the right and left slide assemblies.

(17) Tighten the left and right setscrews untiltheybottom out on their respective slide assemblies; at this point, back off each setscrew one full turn.

(18) Carefully pull the disk drive forward about 16 inches until the second setscrew is exposed on the right and left slide assemblies.

(19) Repeat Step (17).

(20) Carefully extend the disk drive forward about 30 inches, at which point the slides strike the second setscrews in each slide assembly.

(21) In the position indicated in Step (20) the PCBAs may be raised for servicing.

SECTION III
OPERATION

3.1 INTRODUCTION

This section explains the manual operation of the disk drive and defines the interface functions with regard to timing, levels, and interrelationships.

3.2 CARTRIDGE HANDLING AND STORAGE

The magnetic coatings on the disk surface have the ability to retain recorded intelligence for an indefinite period. The recorded data does not tend to weaken or fade with age; however, the physical properties of the recording medium are susceptible to damage.

It is important that the disk cartridge be properly handled and stored so that the integrity of the recorded data are maintained. A damaged or contaminated cartridge can impair or prevent recovery of data and can result in damage to the disk drive.

CAUTION

DO NOT ATTEMPT TO INSTALL OR USE A CARTRIDGE WHICH IS SUSPECTED OF CONTAMINATION OR DAMAGE.

A disk drive which has been damaged or contaminated due to use of a defective cartridge should not be operated with other cartridges until the disk drive has been inspected and/or reconditioned by qualified service personnel.

The following methods will ensure maximum protection of disk cartridges.

(1) The head port door on front load cartridges should be kept closed when the cartridge is not inserted in a disk drive. This prevents the ingress of dirt and secures the disk internally.

(2) Top load cartridges should have the bottom cover in place at all times when the cartridge is not inserted in a disk drive. Do not allow the bottom cover to accumulate dirt or other debris.

(3) Cartridges can be stored either horizontally or vertically. Front load cartridges must always be positioned to avoid objects which could damage the hub or cause the air inlet door to be pushed open.

CAUTION

DO NOT PLACE CARTRIDGES IN A STACK CONTAINING MORE THAN 5 CARTRIDGES.

(4) Avoid exposure of the cartridge to any magnetizing force in excess of 50 oersted or loss of stored data may result.

NOTE

The 50 oersted level of magnetizing force is reached at a distance of approximately 3 inches from a typical source, e.g., motors, generators, transformers.

(5) Do not store the cartridge in direct sunlight; temperatures outside the range of 33°F (0.6°C) to 140°F (60°C) should be avoided for non-operational storage.

(6) Internal, as well as external, damage to a cartridge can result when dropped. If a cartridge is dropped, it should be inspected by a qualified service representative.

(7) Front load cartridges should be labeled only in the area of the label frame which is molded as part of the handle; top load cartridges should be labeled only in the handle recess area. Placement of labels in any other areas may cause improper operation or contamination.

3.3 DISK DRIVE PREPARATION

The initial check-out procedure in Section II should be performed prior to placing the disk drive in a system environment.

Optimum data reliability can be obtained only when the protective dust cover is installed on the disk drive. Also, to ensure proper operation and data reliability, it is necessary that disk cartridges be temperature stabilized at the disk drive ambient temperature for 2 hours.

For 200 tpi models, the time required to ensure cartridge interchangeability and data compatibility is as follows.

(1) Initial Power Turn-on: the disk drive shall be considered stabilized after 15 minutes in the Run mode.

(2) Extended Safe Operation: the time required for the disk drive to stabilize in the Run mode after an extended period (greater than 15 minutes) in the Safe mode is 15 minutes.

(3) Cartridge Interchange: the time required for the disk drive to stabilize in the Run mode following a cartridge change is 2 minutes.

The following initial preparation must be performed before attempting to insert a cartridge into the disk drive.

(1) Ensure that the power cord is connected to the correct line voltage.

(2) Place the ON/OFF switch in the ON position and observe that the associated indicator becomes illuminated.

(3) Observe that the SAFE indicator becomes illuminated within 2 seconds of the ON indicator illumination.

3.4 CARTRIDGE LOADING AND UNLOADING

The following paragraphs describe the proper method to load and unload disk cartridges. Procedures for front load models are contained in Paragraphs 3.4.1 and 3.4.2; procedures for top load models are contained in Paragraphs 3.4.3 and 3.4.4.

3.4.1 LOADING A CARTRIDGE, FRONT LOAD MODELS

Refer to Figures 3-1 through 3-3 in conjunction with the following procedure.

(1) Verify that the SAFE indicator is illuminated as described in Paragraph 3.3.

(2) Referring to Figure 3-1, grip the handle formed by the top of the front bezel and move the handle out and downward; this will open the disk drive door and cam the cartridge receiver into position to accept a cartridge.

(3) Grip the cartridge by the molded handle and position the cartridge in the receiver opening as shown in Figure 3-2. Note that the raised portion of the cartridge top is aligned between the guide rails at the top of the receiver. Slant the cartridge to match the slope of the bottom of the receiver.

(4) Press the cartridge slowly but firmly most of the way into the receiver; relax the grip on the cartridge handle and press the cartridge fully into the receiver, seating it completely within the receiver as shown in Figure 3-3.

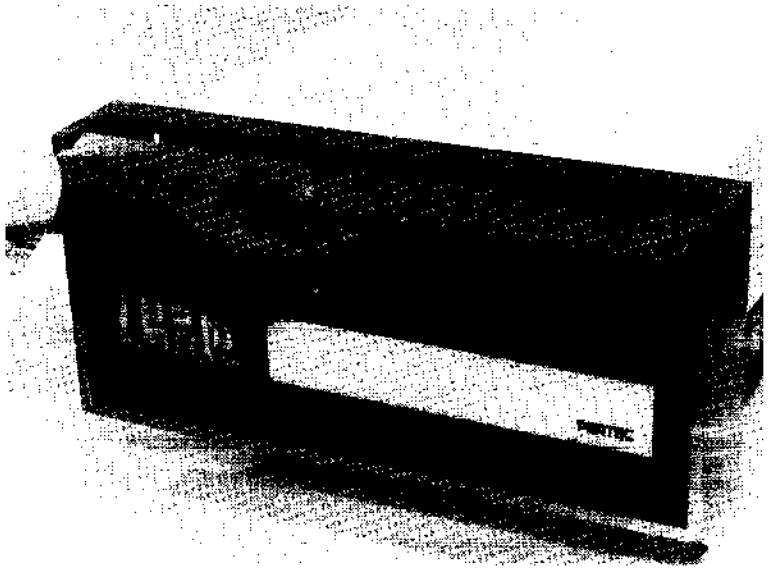


Figure 3-1. Cartridge Loading/Unloading, Front Load Models

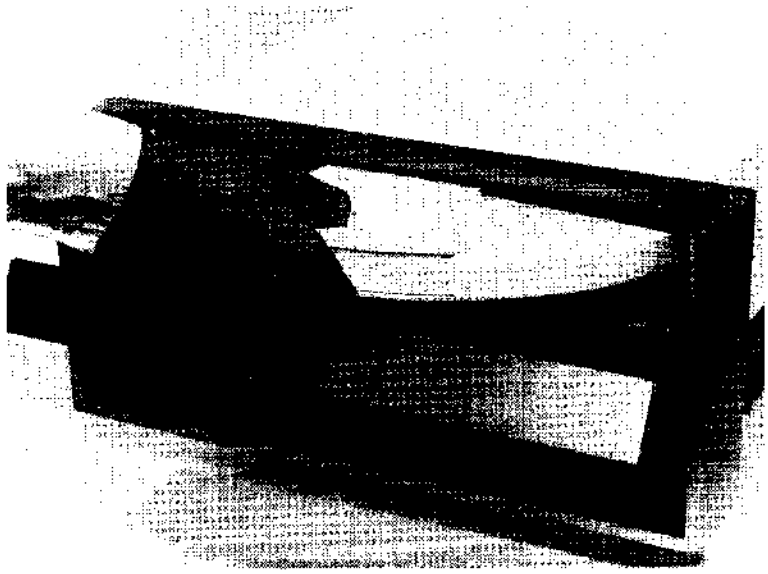


Figure 3-2. Cartridge Loading/Unloading, Front Load Models

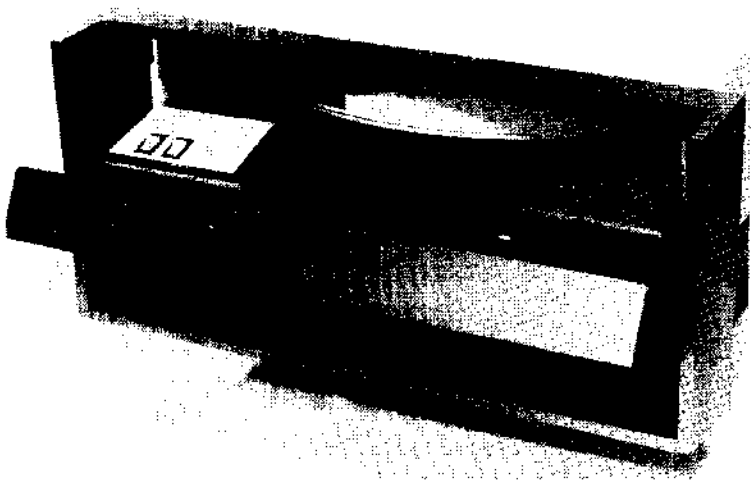


Figure 3-3. Cartridge Inserted, Front Load Models

(5) Close the door on the front of the disk drive by moving the door handle (top of the front bezel) up and toward the drive. As the door is closed, the cartridge will be positioned onto the spindle.

CAUTION

IF THE CARTRIDGE IS NOT PROPERLY INSERTED IN RECEIVER, THE DOOR WILL NOT CLOSE. DO NOT ATTEMPT TO FORCE THE DOOR CLOSED OR DAMAGE TO THE CARTRIDGE AND THE DISK DRIVE WILL RESULT; REPEAT STEPS [1] THROUGH [5].

DO NOT ATTEMPT TO START THE DISK DRIVE UNTIL THE DOOR IS FULLY CLOSED.

3.4.2 UNLOADING A CARTRIDGE, FRONT LOAD MODELS

Refer to Figures 3-1 and 3-2 in conjunction with the following procedure.

(1) Verify that the SAFE indicator is illuminated as described in Paragraph 3.3.

(2) Referring to Figure 3-1, grip the door handle formed by the top of the front bezel and move the handle out and downward, opening the door.

(3) Grip the cartridge by the molded handle and pull the cartridge slowly out of the receiver (Figure 3-2).

(4) Unless another cartridge is to be inserted immediately, close the door to exclude dirt and contamination from the interior of the drive.

3.4.3 LOADING A CARTRIDGE, TOP LOAD MODELS

Refer to Figures 3-4 through 3-9 in conjunction with the following procedure.

(1) Verify that the SAFE indicator is illuminated as described in Paragraph 3.3.

(2) Grip the handle formed by the top of the front bezel and slowly pull the disk drive from the cabinet on its slides until the cartridge area is accessible.

(3) Ensure that the two cartridge lock arms are positioned away from the disk area as shown in Figure 3-4.

NOTE

The cartridge lock arms must be rotated completely into their respective recesses.

(4) With the cartridge positioned as shown in Figure 3-5, press the cartridge release/lock (with the thumb) all the way to the side. Holding the cartridge release/lock, grip and pull the cartridge handle smartly to the vertical position shown in Figure 3-6. The cartridge is now released from the cover.

(5) Referring to Figure 3-7, place the cartridge over the cartridge adapter bowl with the handle recess pointing toward the rear of the drive. Lower the cartridge into the adapter, positioning it so that the keys on the wall of the adapter engage the key notches in the base of the cartridge.

NOTE

Correct positioning of the cartridge has been obtained if the cartridge rim is fully seated against the adapter bowl along the complete periphery of the rim. When the cartridge is correctly seated it cannot be rotated or tilted.

(6) Lower the cartridge handle into the handle recess and allow the release/lock to return (Figure 3-8). This will cause the cartridge hub to engage the spindle clutch.

(7) Invert the cartridge cover (removed in Step (4)) and place it over the cartridge, aligning the cover edge over the ridge along the cartridge rim.

(8) Position both cartridge lock arms over the cartridge cover (allowing the arms to cam upward) until the arms come to rest against the stops provided by the side of the recesses in the adapter bowl (Figure 3-9).

CAUTION

IF EITHER THE CARTRIDGE OR COVER HAS NOT BEEN PROPERLY POSITIONED IT WILL NOT BE POSSIBLE TO ROTATE THE ARMS INTO THE CORRECT POSITION; THIS WILL PREVENT THE DISK DRIVE FROM STARTING. DO NOT ATTEMPT TO FORCE THE ARMS. PLACE THE ARMS BACK IN THE RECESSES AND CORRECTLY POSITION THE CARTRIDGE COVER.

(9) Push the disk drive into the cabinet until the catches engage.

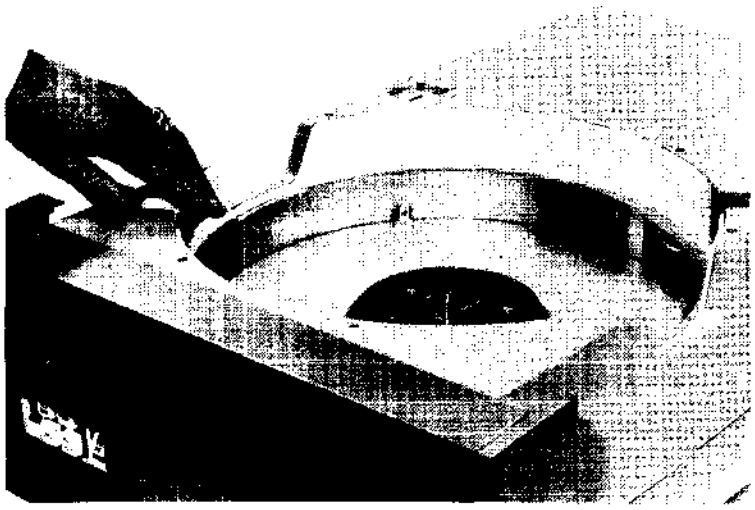


Figure 3-4. Cartridge Loading, Top Load Models (Lock Arms Away from Disk Area)

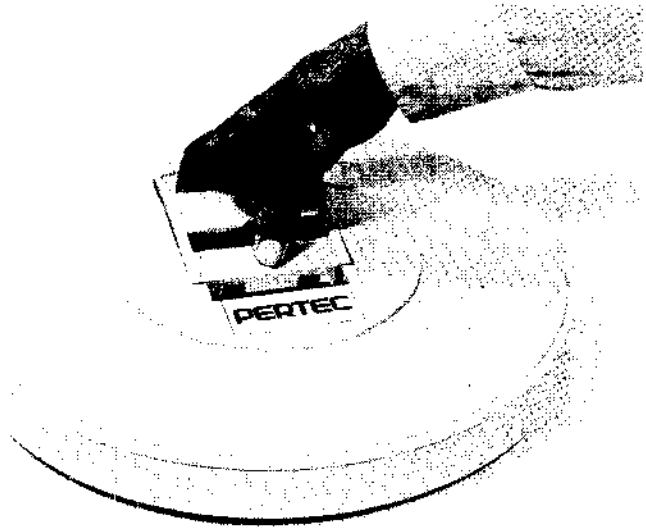


Figure 3-5. Cartridge Loading, Top Load Models (Release/Lock Down)

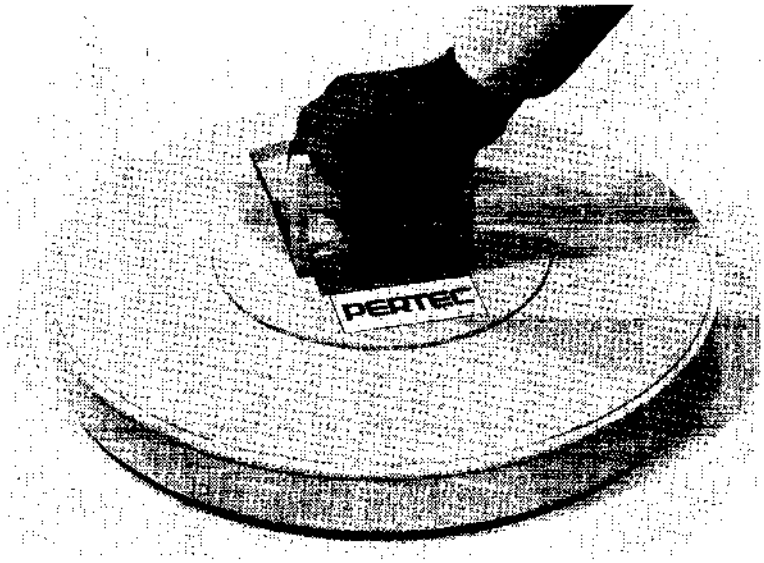


Figure 3-6. Cartridge Loading, Top Load Models (Release/Lock Up)

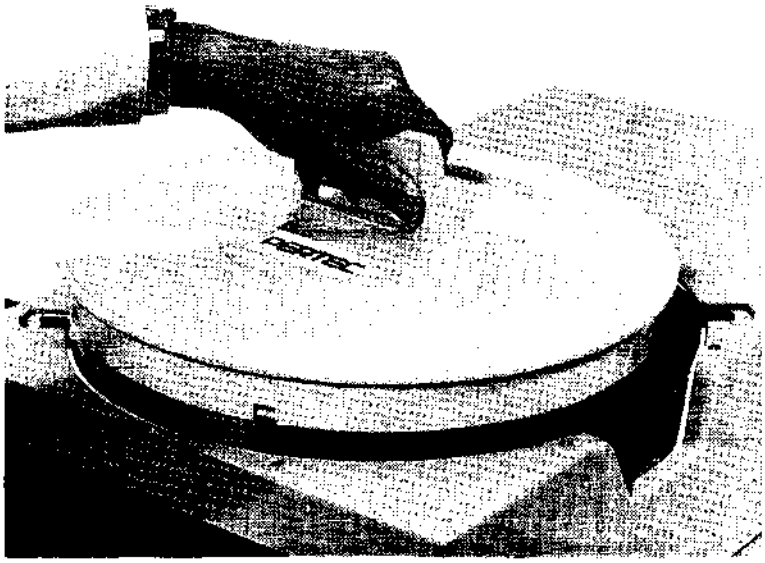


Figure 3-7. Cartridge Loading, Top Load Models (Cartridge Positioned over Adapter Bowl)

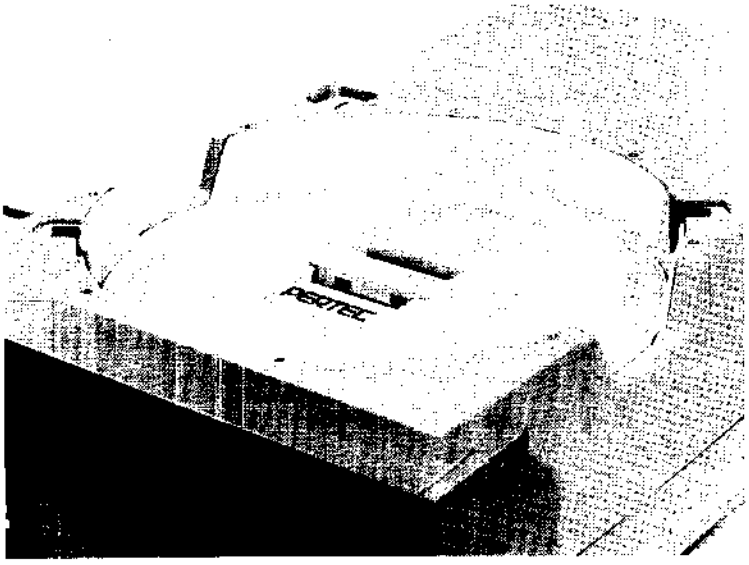


Figure 3-8. Cartridge Loading, Top Load Models (Cartridge Loaded, Release/Lock Down)

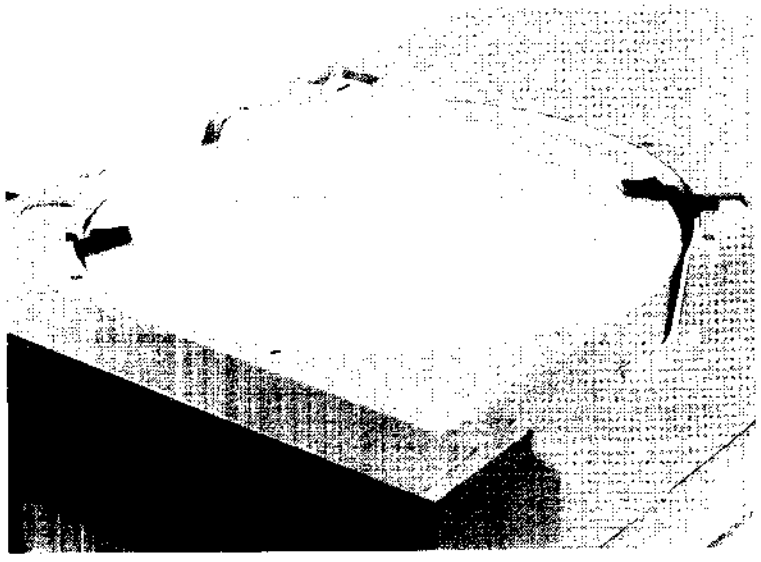


Figure 3-9. Cartridge Loading, Top Load Models (Lock Arms Over Cartridge Cover)

3.4.4 UNLOADING A CARTRIDGE, TOP LOAD MODELS

Refer to Figures 3-10 and 3-11 in conjunction with the following procedure.

(1) Verify that the SAFE indicator is illuminated as described in Paragraph 3.3.

(2) Grip the handle formed by the top of the front bezel and slowly pull the disk drive from the cabinet on its slides until the cartridge area is accessible.

(3) Rotate the two cartridge lock arms away from their position over the cartridge cover to their respective recesses in the bowl as shown in Figure 3-4.

(4) Lift the cartridge cover out of the disk drive (Figure 3-8) and invert it.

(5) Press the cartridge release/lock (with the thumb) all the way to the side. Holding the cartridge release/lock as shown in Figure 3-10, grip and pull the cartridge handle smartly to the vertical position. The cartridge is now disengaged from the clutch.

(6) Carefully lift the cartridge out of the adapter bowl and place it into the cartridge cover as shown in Figure 3-11.

(7) Press the cartridge handle into the cartridge cover recess and release; this causes the cartridge hub to engage the cover, thus securing the disk.

3.5 SELECTING WRITE PROTECTION

When the disk drive is equipped with WRITE PROTECT switches, the operator should select the appropriate switch setting at the time the cartridge is inserted. On front load models the switches are mounted inside the door, behind the operator switch panel; the drive must be in a Safe condition as indicated by the SAFE indicator in order to open the door and gain access to these switches. On top load models the switches are mounted at the left rear of the cartridge adapter and are accessible only when the unit is pulled forward out of the cabinet.

To select protection for a particular platter, set the applicable switch to the ON position. To enable writing for a particular platter, set the applicable switch to the OFF position.

When a WRITE PROTECT switch is set to the ON position, the particular disk is protected from write operations regardless of any write commands which may be received. When a WRITE PROTECT switch is set to the OFF position, write operations may then be executed unless the write protect status is set by the controller through the WRITE PROTECT INPUT line on the interface.

3.6 STARTING THE DISK DRIVE

Upon completion of the relevant cartridge load procedure, the disk drive may be started as follows.

(1) Depress and release the RUN/STOP switch/indicator located on the operator control panel.

NOTE

Illumination of RUN/STOP indicates that there are no inhibiting conditions and that the disk drive is rotating the disk[s].

(2) Observe that the READY indicator becomes illuminated within 60 seconds after actuating the RUN/STOP switch/indicator.

NOTE

Illumination of READY indicates that the disk drive is ready to accept interface commands.

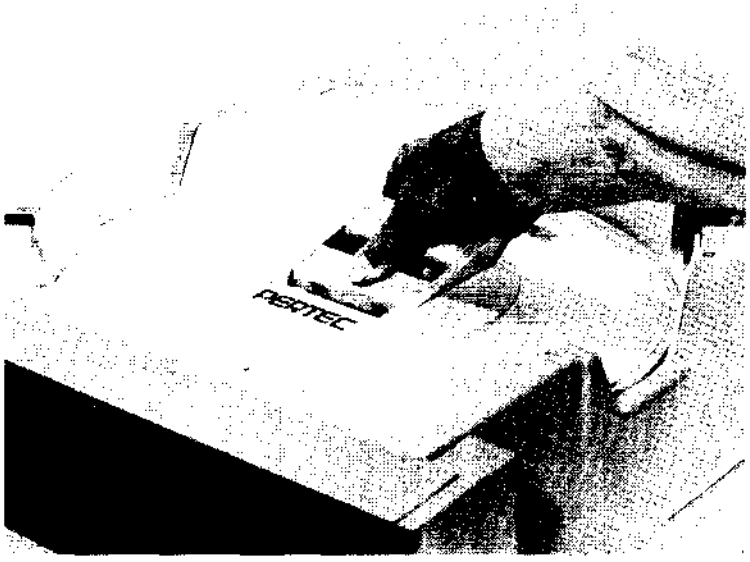


Figure 3-10. Cartridge Unloading, Top Load Models

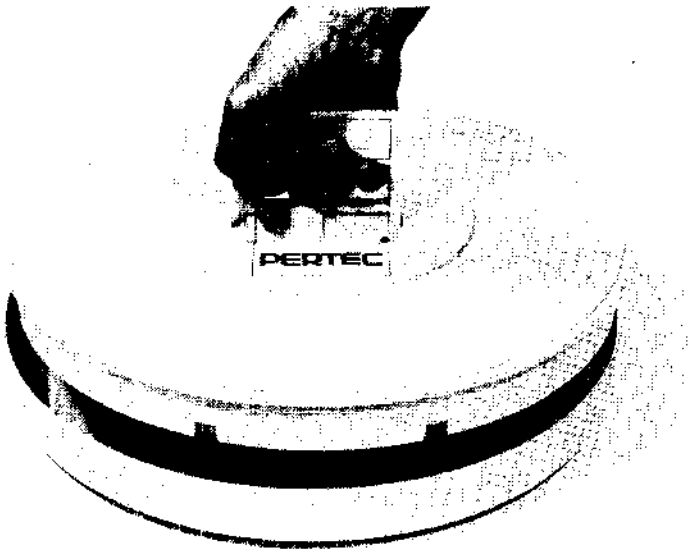


Figure 3-11. Cartridge Unloading, Top Load Models

3.7 STOPPING THE DISK DRIVE

To stop the disk drive while RUN/STOP is illuminated, perform the following procedure.

(1) Depress and release the RUN/STOP switch/indicator.

(2) Observe that the SAFE indicator becomes illuminated within 25 seconds; this indicates that the disk(s) has come to a stop and the cartridge may be removed or changed.

3.8 DESIGNATING UNIT NUMBER

When the disk drive is equipped with a Unit Number Selector Switch, the setting of this switch determines which interface UNIT SELECT line the drive will respond to, i.e., the switch position specifies the device (unit) address.

The operator should set the switch to the appropriate position as specified by the system and software operating procedures for the particular installation.

The switch is set by moving the thumbwheel until the desired number appears in the window adjacent to the thumbwheel. Positions 1, 2, 3, or 4 may have significance.

A drive may be designated a particular unit number, subject to the restriction that different units on the common I/O bus must not have the same number assigned. Since the switches in different units are not interlocked, if two (or more) drives are accidently assigned the same unit number and that number is then selected by the controller, undefined operation may occur.

CAUTION

LOSS OF DATA MAY OCCUR IF THE UNIT NUMBER SELECTOR SWITCH IS REPOSITIONED DURING A WRITE OPERATION.

3.9 CE ALIGNMENT

Prior to placing the disk drive into operation, it is recommended that the CE alignment procedure contained in Section VI be performed. Since misalignment of only 200 μinches is significant and PERTEC cannot control the amount of shock a unit may encounter during shipping, it is recommended that the CE alignment procedure be performed on 100 tpi models; the CE alignment is mandatory on 200 tpi models.

3.10 PERIODIC MAINTENANCE

Periodic maintenance requirements of the disk drive are detailed in Section VI of this manual. Periodic cleaning of heads and disks, and filter changing should be performed according to the prescribed schedules and procedures.

3.11 INTERLOCK PROTECTION

The operator should not attempt to force or overrlde the various protection interlocks provided by the disk drive. These interlocks are designed to prevent damage to data contained in disk cartridges, and to the disk drive equipment. Front load models are interlocked by a switch which senses when a cartridge is correctly inserted into the receiver. When a cartridge is not inserted in the receiver, or the cartridge is incorrectly inserted, the switch will not be actuated and this condition is sensed by the logic which prevents the disk drive from responding to RUN/STOP operator commands and START/STOP DISK DRIVE interface line commands.

If the door is not properly closed on front load models, either as a result of the cartridge being incorrectly inserted or because of operator error, the switch will not be actuated by the cartridge; this results from the fact that as the receiver lowers a properly inserted cartridge down onto the spindle clutch, the cartridge body (if it is in the correct position) actuates the switch lever. Additionally, the door is locked whenever the disk drive is not in a Safe condition. The Safe condition is indicated when the SAFE indicator is illuminated.

Top load models are interlocked by 2 switches which sense the position of the cartridge lock arms. These switches will be actuated only when the lock arms are fully rotated toward the spindle and when the correct height is sensed by the cartridge lock arms. This condition will exist when a cartridge has been correctly seated on the aligning keys and the cartridge bottom cover has been correctly positioned over the top of the cartridge. In the case of an incorrectly inserted cartridge, the correct height will not be sensed by the switches and therefore the disk drive will be unable to respond to RUN/STOP operator commands or START/STOP DISK DRIVE interface line commands. Additionally, if a cartridge is inserted without a cover, or only a cover is inserted, the correct height will not be sensed and the disk drive will not respond to commands.

To prevent removal of a cartridge during unsafe conditions, the cartridge lock arms will be locked whenever the drive is not in a Safe condition.

In addition to the electro-mechanical interlock protection, additional interlocking is provided via certain logic within the disk drive. If the operator should actuate the RUN/STOP switch/indicator, or if the interface should command a Stop sequence as a result of a change of state on the START/STOP DISK DRIVE line, during the time that a Write and/or Erase operation is in progress, the heads will not be unloaded immediately from the storage surfaces even though the disk drive prepares to execute a Stop sequence.

Only when the controller has completed the current Write and/or Erase operation will the heads be unloaded from the storage surface. This prevents the loss of data in the event that the operator attempts to stop the disk drive during the time that a write data transfer is in progress.

An additional interlock prevents changing the Write Protect status during a Write and/or Erase operation. If either a Write and/or operation is in progress, the status of the write protection cannot be changed electrically regardless of the positions of the WRITE PROTECT switches.

Only after completion of the current Write and/or Erase operation will the write protection status change to agree with the particular switch setting.

This is primarily applicable to top load models, although the same logic is present in all machines. The purpose of this arrangement is to prevent loss of data in the event an operator should change the condition of the WRITE PROTECT switches during the time the controller is in the process of a write data transfer.

3.12 SAFE CONDITION

The Safe condition for both front and top load models is indicated by illumination of the SAFE indicator and is defined by:

(1) Power correctly applied.

(2) Disk not rotating.

(3) Heads retracted.

(4) Emergency or fault conditions not being detected by the logic.

(5) Disk drive not executing a brake cycle or a stop sequence.

Additionally, for top load models, the disk cleaning brushes must be parked in the home position. It should be noted that although the disk drive is in a Safe condition it is not necessarily enabled to respond to start commands. The conditions which inhibit starting the disk drives are:

(1) The cartridge is not properly inserted.

(2) Power is not applied.

(3) An internal emergency or fault condition exists and is being detected.

3.13 EMERGENCY AND FAULT DETECTION

When power to a disk drive is lost when the disk is spinning, it is impossible for the disk drive to maintain disk speed at a value which assures that the heads will continue to fly above the surface of the disk.

In order to protect the data and the cartridge, as well as the disk drive, it is necessary to remove the heads from the surface of the disk as fast as possible when a power fault is detected. The process of removing the heads from over the disk in an emergency situation is referred to as Emergency Unload. Additionally, there are other conditions which are undesirable, either from the standpoint of potential hazard to data or to the disk drive.

The conditions which can cause an emergency unload are summarized as follows.

(1) Loss of ac or dc power.

(2) Disk speed does not remain within tolerance or is at an incorrect speed at the time it is tested.

(3) Positioner error is detected.

(4) Write circuit faults that could affect the stored data are detected.

3.14 MANUAL CONTROLS

The operational controls and indicators are located on the front panel of the disk drive; additionally, one or two rocker-type switches may be located inside the drive which provide protection from inadvertent write operations. The following paragraphs describe the functions of these controls.

3.14.1 ON/OFF

The ON/OFF power control is a rocker-type switch/indicator which provides the operator a means of energizing and de-energizing the power to the drive. The indicator is illuminated when power is ON and the internal +5v power is operational.

3.14.2 RUN/STOP

The RUN/STOP control is a momentary action switch/indicator which provides a means for selecting the operational status of the drive. The alternate action arrangement is provided by the disk drive logic. The control will be illuminated when actuated and the drive has been properly conditioned to allow the disk to be brought to operating speed.

When the illuminated switch/indicator is depressed again, a Stop sequence will be entered and the disk will decelerate to a stop. The cartridge may be unloaded at this time.

If a cartridge has been incorrectly inserted or an emergency condition exists, the operation of the RUN/STOP control is inhibited. Under this condition the control will not become illuminated and the Run status will not be achieved.

3.14.3 READY

This is an indicator which is illuminated when the disk drive achieves a Ready condition. The Ready condition is defined in Paragraph 3.17.1.

3.14.4 SAFE

This is an indicator which is illuminated when it is possible to safely insert or remove the disk cartridge. When the SAFE indicator is extinguished, protective cartridge locks prevent removal of the disk cartridge.

CAUTION

DO NOT ATTEMPT TO FORCE REMOVAL OF A DISK CARTRIDGE WHEN THE SAFE INDICATOR IS EXTINGUISHED. FAILURE TO OBSERVE UNSAFE CONDITION CAN RESULT IN DAMAGE TO THE EQUIPMENT.

3.14.5 PROT (PROTECT)

Two indicators, mounted in a common housing, are provided to indicate the data protection status of the disk(s). This status information can be from the WRITE PROTECT switches (Paragraph 3.14.7), or from a hard-wired configuration.

When the upper PROT indicator is illuminated, the upper (removable) disk is protected from a write operation; protection of the lower (fixed) disk is indicated by illumination of the lower PROT indicator.

The indicators are extinguished when the respective switch (or hard-wired configuration) is set to permit write operations.

3.14.6 UNIT NUMBER SELECTOR SWITCH

A 4-position thumbwheel switch may be included on the front panel of the disk drive to provide a means for selecting one of several peripheral units on a common I/O bus.

Any drive may be assigned (designated) a particular unit number (unit address) subject to the restriction that different units on the bus may not have the same number assigned. Since the switches in different units are not interlocked, if two (or more) drives are accidently assigned the same unit number and that number is then selected by the controller, undefined operation may occur.

When the thumbwheel switch is not included, the disk drive will respond only to UNIT SELECT NO. 1 line.

3.14.7 WRITE PROTECT SWITCHES

One or two rocker switches may be included in the D3000 Series Disk Drive. The purpose of these switches is to selectively protect the disks from inadvertent write operations. One switch selects protection for the upper (removable) disk; the other selects protection for the lower (fixed) disk.

The switches are located inside the drive enclosure, near the removable disk cartridge. On front load models the switches are mounted to the rear of the operator control panel. Access can be obtained to these switches only after the door is opened. On top load models the switches are mounted at the left rear of the cartridge adapter and are accessible only when the unit is pulled forward out of the cabinet.

When a WRITE PROTECT switch is set to the ON position, the particular disk is protected from write operations regardless of any write commands which may be received. When a WRITE PROTECT switch is set to the OFF position, write operations may then be executed unless the write protect status is set by the controller through the WRITE PROTECT INPUT line on the interface.

The PROT indicators (Paragraph 3.14.5) indicate the status of the protect switches.

3.15 D3000 INTERFACING

The D3000 interface is described in two sections: Controller (or Formatter) to Disk Drive, and Disk Drive to Controller (or Formatter).

The interface is arranged such that as many as four different disk drives may be operated on the interface by a common controller. This is accomplished by providing a group of (disk drive) input lines and a group of output lines which become a common I/O bus. This bus is time-shared by the various drives that may be connected with the bus, i.e., daisy-chain arrangement.

3.16 INTERFACE INPUTS (CONTROLLER TO DISK DRIVE)

All signal names are chosen to correspond to the logical true condition. All interface lines are low-true at the interface with the low (true) condition considered to be 0v, and the high (false) condition considered to be +3v.

3.16.1 UNIT SELECT LINES

There are four UNIT SELECT lines. A low level on one of these lines will connect one pre-determined disk drive to the common I/O bus.

The low level on one of these lines enable all input/output lines except the START/STOP DISK DRIVE line which is enabled at all times.

When the Unit Number Selector Switch is included, the units are identified to switch positions and select lines on a one-to-one basis, i.e., switch position 1, UNIT SELECT NO. 1 line, etc.

After a unit has been selected and the I/O bus has been allowed 2 μsec to stabilize, the selected disk unit will recognize inputs and provide stable outputs.

3.16.2 PLATTER SELECT

This is a level which determines which platter is selected in dual platter models. When the level on this line is low, the bottom (fixed) platter is selected; when the level on this line is high, the top (removable) platter is selected, as shown in Table 3-1.

Table 3-1
Platter and Head Selection

PLATTER SELECT Line Logic Level	HEAD SELECT Line Logic Level	Dual Platter Models		Single Platter Models	
		Platter	Storage Surface	Platter	Storage Surface
High	High	Top	Bottom	Top	Bottom
High	Low	Top	Top	Top	Top
Low	High	Bottom	Bottom	None	None
Low	Low	Bottom	Top	None	None

3.16.3 HEAD SELECT

This is a level which determines which head and corresponding storage surface (top or bottom) is selected.

In dual platter models a low condition on this line selects the top storage surface of the selected platter. When high, the line selects the bottom storage surface of the selected platter.

In single platter models, a low condition on this line selects head 0 and the top storage surface of the platter; when high, head 1 and the bottom storage surface are selected, as shown in Table 3-1.

3.16.4 STROBE

This is a pulse which, when true when the unit is selected and ready, causes the RESTORE and TRACK ADDRESS lines to be sampled. This will initiate a restore operation or a cylinder seek operation depending on the state of the RESTORE line (Paragraph 3.16.6).

For a restore operation, the TRACK ADDRESS lines are ignored and the positioner will initialize at cylinder 000 (decimal).

For a seek operation, if a legal address is presented on the TRACK ADDRESS lines, the positioner will seek the cylinder address specified by the stages on these lines. If an illegal address is presented, then the positioner will not move and the illegal condition will be reported on the LOGICAL ADDRESS INTERLOCK line.

The STROBE line must be held low until either the ADDRESS ACKNOWLEDGE or the LOGICAL ADDRESS INTERLOCK signal is issued by the disk drive. This may occur any time between 22.5 μsec and 37.5 μsec after the leading edge of the STROBE.

When the ADDRESS ACKNOWLEDGE or the LOGICAL ADDRESS INTERLOCK signal is issued, the STROBE signal must be removed within 5 μsec. Rise and fall times of the STROBE signal must be compatible with commercially available DTL or TTL integrated circuits.

The READY TO SEEK, READ OR WRITE line will go to a high logic level in no less than 2.5 μsec after the leading edge of the STROBE.

If the STROBE signal is issued to the disk drive when the positioner is executing a previous command, and the READY TO SEEK, READ OR WRITE line is at a high logic level, the disk will ignore the command. However, if the RESTORE line is true when the STROBE is applied, the status of the READY TO SEEK, READ OR WRITE line is ignored and the RESTORE sequence is executed.

The leading edge of the strobe should appear only after the TRACK ADDRESS lines and the RESTORE line have fully settled.

The STROBE signal should never be issued when the unit is selected and the READY TO SEEK, READ OR WRITE line is at a high (false) logic level.

3.16.5 TRACK ADDRESS LINES

These lines specify the cylinder address for accessing a specific cylinder. The address is represented by the binary value with a low logic level corresponding to a binary one.

The most significant bit for 203 cylinder models is TRACK ADDRESS BIT — 128, the most significant bit for 406 cylinder models is TRACK ADDRESS BIT — 256; the least significant bit for all models is TRACK ADDRESS BIT — 1.

The decimal cylinder number may be expressed as the sum of the *true* bit weights as expressed by the bit number, e.g., the TRACK ADDRESS BIT — 128 has a bit weight of 128.

The range of legal addresses for 203 cylinder models is from 000 through 202 (decimal), for 406 cylinder models the range is from 000 through 405 (decimal).

3.16.6 RESTORE

The state of this line at the time that the STROBE is issued determines the type of positioning operation that will be performed.

Logic Level	Type of Operation Specified
Low	Restore position to initial cylinder (cylinder 000)
High	Seek to cylinder specified by address

This line is used primarily in conjunction with bootstrap loader programs to obtain an effective address without having to actually specify a specific address. Another use is to re-initialize the positioner as a diagnostic check in the event that a header disagreement has occurred.

3.16.7 WRITE GATE

A low level on this line when the unit is selected and ready causes the write electronics to be conditioned for writing data (the read electronics are disabled). This signal simultaneously turns on write current in the selected head if the write protection condition does not exist and the positioner is not moving.

Data are written under control of the WRITE DATA AND CLOCK signal line.

Certain applications may require that all write data pulses be correctly recorded. Therefore, it is recommended that changes of state on the WRITE GATE line be

accomplished during a time when no data pulses are being transmitted on the WRITE DATA AND CLOCK signal line.

When the WRITE GATE line is at a high logic level, all write electronics are disabled.

3.16.8 ERASE GATE

This is a level which, when low and the unit is selected and ready and a write protection condition does not exist and the positioner is not moving, erase current will be allowed to flow in the selected erase head.

Erase must be enabled during any write operation. The erase current is disabled when the ERASE GATE line is at a high logic level.

The ERASE GATE line must be placed in the low state within 1 μsec when the WRITE GATE is placed in the low state.

When the WRITE GATE line is placed in the high state (any low to high change of state) the erase current must remain enabled for a period of time thereafter. The minimum time is defined as the minimum erase gap time.

3.16.9 WRITE DATA AND CLOCK SIGNAL

The bit-serial write data pulses on this line control the switching of the write current in the head. The write electronics must be conditioned for writing.

For each high to low transition on the WRITE DATA AND CLOCK signal line, a flux change will be produced at the write head gap. This will cause a flux change to be stored on the selected disk surface.

The double frequency encoding technique is used in which data and clock form the combined WRITE DATA AND CLOCK signal. The repetition rate of the high to low transitions when writing all zeros is equal to the nominal data rate ±0.25 percent. The repetition rate of the high to low transitions when writing all ones is equal to twice the nominal data rate ±0.25 percent. The nominal data rate for a specific model is listed in Table 1-1.

3.16.10 WRITE PROTECT INPUT

This is a level which, when used in conjunction with the WRITE PROTECT switches, provides a means of write protect control.

The WRITE PROTECT switches are described in Paragraph 3.14.7.

The write protect control may be exercised using one of two methods.

(1) The upper and/or lower platter may be write protected by setting the respective switch(es) to the ON position before loading the cartridge. WRITE PROTECT remains ON when the disk is running.

(2) The WRITE PROTECT switch(es) may be set to the OFF position, in which case WRITE PROTECT remains OFF when the disk is running. The write protect may then be set, if desired, by pulsing the WRITE PROTECT INPUT line; this line must remain at low logic level for the minimum duration of 350 nsec. The write protect, once set in this manner, can only be turned off by depressing the RUN/STOP switch and thereby stopping the disk drive.

If the PLATTER SELECT line is at a high logic level when the WRITE PROTECT INPUT line is pulsed, the top (removable) platter is write protected.

If the PLATTER SELECT line is at a low logic level when the WRITE PROTECT INPUT line is pulsed, the bottom (fixed) platter is write protected.

3.16.11 READ GATE

This is a level which, when low and the unit is selected and ready, enables the read electronics (READ DATA and READ CLOCK). After READ GATE is placed at the low logic level, the read electronics must detect one clock transition before any clock and data pulses may be transmitted, i.e., the first clock transition of preamble or gap will not be transmitted but all others will be transmitted assuming the required conditions are met. This arrangement prevents pulses of less than normal duration from being transmitted.

When the READ GATE line is high, the read electronics outputs are immediately disabled and, if any data or clock pulses are in progress these pulses will be shaved.

NOTE

It is recommended that the controller be designed such that the low to high transition of READ GATE is timed or caused by a clock pulse transition.

3.16.12 TRACK OFFSET

The TRACK OFFSET PLUS line and the TRACK OFFSET MINUS line provide a means of margin testing.

When one of these lines is low and the unit is selected and ready, the heads are slightly offset from the normal track center. The direction of the offset is determined by the active line. An active direction is defined as being toward the disk center; a minus direction is defined as being away from the disk center. Table 3-2 defines the operational condition of the disk drive when the track offset function is used.

When either of the TRACK OFFSET lines is placed at a low logic level, the positioner requires one-fourth of adjacent track seek time to seek the new position and settle out. A busy signal on the READY TO SEEK, READ OR WRITE line will not be given for TRACK OFFSET settling. The settling time for any TRACK OFFSET is in addition to seek time as indicated by the READY TO SEEK, READ OR WRITE line.

In general, the use of the TRACK OFFSET lines during a write operation is not recommended. Unless there is some means to guarantee that the entire track will later be erased (with the same offset control), then errors may be induced.

Prior to a read operation, the TRACK OFFSET lines should be conditioned for the type of operation desired. Assume a track of data has been previously recorded under normal conditions; the margin for recovery can be tested by reading and checking the data first with TRACK OFFSET PLUS, and then with TRACK OFFSET MINUS. If adequate margins exist, then all data will be correctly read.

For the case when both TRACK OFFSET PLUS and TRACK OFFSET MINUS are simultaneously TRUE, read amplifier gain is reduced and the recovery margin is tested with the heads centered over the track.

3.16.13 START/STOP DISK DRIVE

This is a level which, when low and the following conditions and restrictions are met, allows the controller to start and stop the disk drive remotely. The function performed and the resulting actions depend on the condition of the drive at the time this line goes low. When the START/STOP DISK DRIVE line is held at a high logic level, or is not connected, the line has no effect on the operation of the disk drive.

Conditions and restrictions effecting this line are:

(1) This line is enabled at all times regardless of the state of the UNIT SELECT lines. Therefore, all disk drives on the common I/O line may respond to this line.

(2) A true level on this line will cause the disk drive to commence a Start sequence if the drive is not already in a Run condition, or if the RUN/STOP switch/indicator is not depressed and none of the following inhibiting conditions exist.

- The disk cartridge is improperly inserted.
- Power is not applied.
- An internal emergency condition exists.

When used for commanding a start operation, a pulse of not less than 260 μsec, or level change may be used.

(3) A true level on this line will cause the disk drive to enter a Stop sequence if the drive is in a Run condition and the RUN/STOP switch/indicator is not depressed. The sequence will be completed if the WRITE ENABLE and ERASE ENABLE interface signals are high.

When used for commanding a Stop operation, a pulse of not less than 60 μsec, or a level change, may be used.

(4) Since the START/STOP DISK DRIVE line performs the same function as the RUN/STOP switch/indicator, priority is by first actuation.

If the START/STOP DISK DRIVE line is actuated continuously, the RUN/STOP switch/indicator is locked out during this period; conversely, if the RUN/STOP switch/indicator is depressed and held, the START/STOP DISK DRIVE line is locked out during this period.

3.17 INTERFACE OUTPUTS (DISK DRIVE TO CONTROLLER)

All signal names are chosen to correspond to the logical true condition. All interface lines are low-true at the interface with the low condition considered to be 0v, and the high condition considered to be +3v.

3.17.1 FILE READY

This is a level which, when true, indicates that the disk unit is in a Ready condition. If the unit is not in a Ready condition and is selected, the FILE READY line will be at a high logic level.

The applicable indication on the FILE READY line will become valid within 2 μsec after a unit is selected. The indication will remain until either the unit status changes (the disk drive becomes Ready or loses Ready condition) or until it is de-selected.

The Ready condition is defined as that condition which exists when the following requirements are met.

(1) All power is applied and correct.
(2) A cartridge is correctly inserted.
(3) The disk is rotating at the correct speed.
(4) The heads are loaded.
(5) No equipment faults are detected.
(6) The logic is prepared to recognize commands.

3.17.2 READY TO SEEK, READ, OR WRITE

A low logic level on this line indicates that the disk drive is in File Ready condition and is not in the process of executing a seek or restore operation.

This signal line goes to a high level in no less than 2.5 μsec after detecting the leading edge of the STROBE signal associated with a SEEK command to a valid address (other than the present address), or a RESTORE command.

3.17.3 SECTOR MARK

This line provides a signal which may be used for sectoring a disk. The signal on this line consists of pulses at regular intervals during each revolution of the disk. These pulses, in essence, divide the disk (surface) into 'N' equal segments, where 'N' is the number of pulses.

For disk drive models that accept the 5440-type cartridge, the SECTOR MARK line provides electronically generated pulses of pre-determined number. The number is specified at the time of order. This may be readily changed in the field by plugging in a different programming-array plug. This plug configures the disk drive to generate a specific number of sector pulses.

For disk drives incorporating a fixed disk as well as a 5440-removable disk, the number of sector pulses for the fixed disk are also determined by a plug-in array.

For disk drives that accept the 2315-type cartridge, the SECTOR MARK line provides pulses derived from the sector ring on the cartridge. One pulse for each sector slot will be issued (this applies only to the removable disk). In some applications it may be desirable to utilize electronically generated sector pulses in lieu of sectoring by the 2315 cartridge sector ring. This can be configured by plugging in the appropriate programming-array plug. The sector pulses for the removable disk will then be similar to the arrangement described previously for the 5440-type cartridge.

For disk drives incorporating a fixed disk as well as a 2315 removable disk, the number of sector pulses for the fixed disk are also determined by plug-in array.

In all cases, the pulses on the SECTOR MARK line correspond only to the respective platter as selected by the PLATTER SELECT line. This is accomplished by a multiplexer internal to the disk drive.

The number of sector pulses that may be accommodated by the electronically generated sectoring are listed in Table 1-1.

The number of sector pulses that may be accommodated by a 2315-type cartridge sector ring is determined by machining and mechanical limitations. Therefore, cartridges are available in 8, 12, 16, 24, and 32 as standard items. Other values are available only on special order.

The duration of any sector pulse is 5 ±2.0 μsec. The SECTOR MARK line is low during the duration of the pulse; at all other times the line is high.

Should a unit be selected at the moment a sector pulse is in progress, that pulse duration will be shortened, i.e., the pulse will be shaved an indeterminate amount. This will have the effect of introducing a time uncertainty (instantaneous jitter) for the shaved pulse.

3.17.4 SECTOR ADDRESS LINES

These lines specify the sector count presented in binary format. This count indicates the particular segment of the disk surface currently under the read/write heads. The signals on these lines are, in essence, the status of a binary counter. In all cases, the count presented corresponds only to the respective platter as selected by the PLATTER SELECT line. This is accomplished through the use of separate counters multiplexed internal to the disk drive.

The count is represented by the binary value with a low level corresponding to a binary one. The most significant bit is bit number 16; the least significant bit is bit number 1.

The decimal sector number may be expressed as the sum of the *true* bit weights as expressed by the bit number, e.g., SECTOR BIT 16 has the bit weight of 16.

The signals on the SECTOR ADDRESS lines will change state 3.2 ±1.2 μsec prior to the leading edge of the sector pulse, assuming non-shaved pulses.

The sector pulse immediately following an index pulse defines the beginning of sector zero and at the time of this sector pulse the SECTOR ADDRESS lines will present a zero value. Thereafter, the value will be incremented until the maximum count is achieved. The maximum count that will occur is (N — 1) where 'N' is the number of sector pulses. This is determined by the particular configuration as described under SECTOR MARK (Paragraph 3.17.3).

3.17.5 INDEX MARK

This is a pulse which occurs once per disk revolution and is used to define the sector reference (sector zero). The pulse will always occur during the sector just prior to sector zero, i.e., during sector N — 1, where 'N' is the maximum number of sectors.

The duration of the index pulse is 5 ±2.0 μsec. The INDEX MARK line will be at the low logic level during the duration of the pulse. At all other times the line will be high. If a unit is selected at the moment that an index pulse is in progress, that pulse duration will be shortened, i.e., the pulse will be shaved an indeterminate amount.

In all cases, the pulse on the INDEX MARK line corresponds only to the respective platter as selected by the PLATTER SELECT line. This is accomplished by a multiplexer internal to the disk drive.

3.17.6 PSEUDO SECTOR MARK

The PSEUDO SECTOR MARK line provides 2000 ± 20 square wave clock pulses per revolution at the interface. This signal line may be used to obtain desired number of pseudo sectors per revolution.

The PSEUDO SECTOR MARK line is a no-cost option and must be specified at the time of order.

3.17.7 READ CLOCK

This is a pulse which goes true at the beginning of a new bit cell during a read operation. The leading edge of this pulse defines the beginning of a new (next) bit-cell. The line will be at the low logic level during the time of the pulse.

During a portion of each bit-cell time, the READ CLOCK line will be placed high and remain in this state until the next bit cell time is to be defined by a pulse leading edge.

This line is utilized to establish a timing reference for purposes of interpreting pulses on the READ DATA line.

3.17.8 READ DATA

The signals on this line define the content of the data read during a Read operation.

The signal will be a pulse for each *logic-one* bit read from the disk. The line will be low during the time of the pulse and high for each *logic-zero* bit read from the disk.

The timing of pulses on this line is relative to the READ CLOCK line. The relative timing is such that a *logic-one* bit should be interpreted if the READ DATA line is low at any time when the READ CLOCK line is high between consecutive pulses on the READ CLOCK line.

3.17.9 ADDRESS ACKNOWLEDGE

The ADDRESS ACKNOWLEDGE line indicates to the controller that a command to move the heads to a specified address has been accepted, and that the execution of the command has commenced.

The signal on the ADDRESS ACKNOWLEDGE line is a pulse with a duration of 5 $\pm$2.5 μsec, and occurs in a minimum of 22.5 μsec, 37.5 μsec maximum, after the STROBE signal.

TheADDRESS ACKNOWLEDGE signal is issued after a seek command to a valid address even if it is the same as the previous command. The ADDRESS ACKNOWLEDGE signal is not issued for a seek command to an illegal address in which case the LOGICAL ADDRESS INTERLOCK signal is issued. The TRACK ADDRESS lines and the STROBE line must be held until either the ADDRESS ACKNOWLEDGE or the LOGICAL ADDRESS INTERLOCK signal is issued by the disk drive.

3.17.10 LOGICAL ADDRESS INTERLOCK

The LOGICAL ADDRESS INTERLOCK signal indicates to the controller that a seek command to an illegal address is received, and therefore the command is not executed.

The LOGICAL ADDRESS INTERLOCK is a pulse with a duration of 5 $\pm$2.5 μsec, and occurs in a minimum of 22.5 μsec, 37.5 μsec maximum, after the STROBE signal.

The STROBE signal must be removed within 5 μsec after either the ADDRESS ACKNOWLEDGE or the LOGICAL ADDRESS INTERLOCK signal is issued.

3.17.11 WRITE PROTECT STATUS

The level on this line indicates whether the selected platter is protected from a Write operation.

When the WRITE PROTECT STATUS line is low the drive will not perform a Write or Erase operation regardless of a command on the WRITE GATE or ERASE GATE lines.

When the WRITE PROTECT STATUS line is high the selected platter is not protected and data may be written.

Changes of state on this line, as applicable, will occur within 1.0 μsec of a platter select change (assuming the unit is selected).

It is recommended that the controller test the state of this line prior to attempting a Write operation.

3.17.12 WRITE CHECK

The signal on this line is a pulse which, when low, indicates that one or more of the following conditions are detected.

(1) Write circuit faults that could affect stored data.

(2) Servo/Positioner failure.

(3) Disk speed does not remain within tolerance.

(4) Loss of ac or dc power.

Any of the above conditions necessitates unloading the heads and the disk drive will commence an emergency unload sequence.

3.17.13 SEEK INCOMPLETE

This line always remains at high logic level (false). Any Servo/Positioner type failure causes an unload sequence to commence and the disk drive becomes Not Ready. The RESTORE command cannot be given to clear the SEEK INCOMPLETE condition because the disk drive is in Not Ready condition. Any Servo/Positioner type failure is reported through the interface line WRITE CHECK instead of SEEK INCOMPLETE to assure software compatibility. SEEK INCOMPLETE line is therefore not used on the interface.

3.17.14 HIGH DENSITY INDICATION

This is a level which, when true, indicates that the disk drive is installed with the high density capability. High density corresponds to 2200 bits per inch as measured on the innermost track. The HIGH DENSITY INDICATION line is a no-cost option and must be specified at the time of order.

3.17.15 DUAL PLATTER DRIVE

The logic level on this line indicates the number of different platters contained in the disk drive.

A valid level will exist on the line whenever the particular disk drive is selected, regardless of whether the particular disk drive is ready or not.

Logic Level	Type of Disk Drive Indicated	Number of Platters
High	Single Removable Platter	1
Low	Dual Platter; One Fixed, One Removable	2

This line may be used by the controller or formatter to determine in advance the legal number of storage surfaces available in a specific disk drive. This allows utilization of different model disk drives on a common Input/Output bus.

DUAL PLATTER DRIVE, if not used, may be left open on the interface.

SECTION IV
THEORY OF OPERATION

4.1 INTRODUCTION

This section provides a description of the D3000 Disk Drive theory of operation.

The disk drive consists of the mechanical and electrical components necessary to record and read digital data recorded on a magnetic disk. The disk drive consists of the following major groups.

(1) Main chasis group
(2) Positioner assembly
(3) Power supply assembly
(4) Read/Write PCBA
(5) Servo PCBA
(6) Logic PCBA
(7) Temperature Compensation PCBA (200 tpi)

4.2 ORGANIZATION OF THE DISK DRIVE

Figure 4-1 is a block diagram illustrating the overall organization of the disk drive. This organization can be sub-divided into the mechanical and the electrical/electronics group. The mechanical group can be be further divided into the main chassis group and the positioner assembly group.

4.2.1 MAIN CHASSIS GROUP

The main chassis group consists of the following components and assemblies.

(1) Base casting
(2) Air system filter and blower
(3) Spindle assembly
(4) Drive motor
(5) Drive train components
(6) Brush cleaning mechanism (top load models)
(7) Cartridge adapter (top load models)
(8) Receiver assembly (front load models)
(9) Disk cover (top load models)
(10) Lower disk cover (front load models)
(11) Bezel assembly
(12) Dust cover
(13) Control switch and indicator group

The main mechanical element of the disk drive is the base casting. This casting is a machined aluminum alloy casting which is the supporting structure for all of the components in the disk drive. When rack mounting the disk drive, the rack mounting slides are mounted directly to the sides of the base casting. This provides a means of sliding the unit in and out of rack installations.

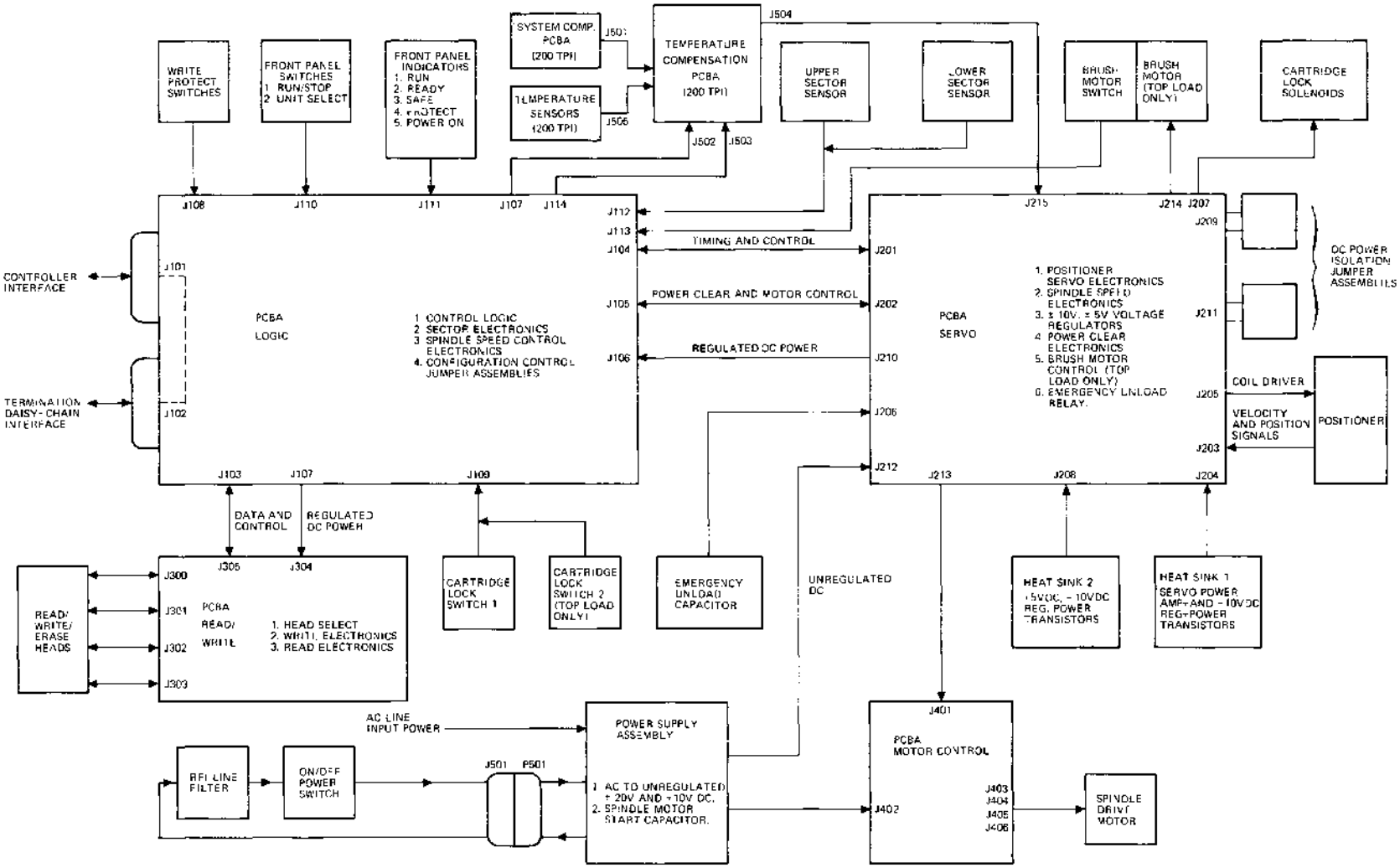


Figure 4-1. D3000 Disk Drive Organization

The absolute filter and high efficiency blower are components of the air system and are mounted into the base casting. In addition, duct work, either integral with the base casting or formed by suitable cover plates, provides the means for channeling the filtered air into the area of the disk and heads. The air system provides a highly filtered air flow into the area of the disks and disk cartridge. Operational characteristics of the *flying head* type of magnetic head employed in the disk drive require that the air bearing formed between the head and the disk surface be relatively free of particle contamination. Therefore, the filtered air flow provided by the air system causes a continual flow of clean air to purge this area of the disks and ensure correct operation of this air bearing. The air cushion which causes the heads to fly above the surface of the disk is dependent only upon the surface velocity of the disk and not upon the air flow through the filter.

The spindle assembly mounts into the base casting and provides the central axis of rotation for the disks. This spindle is a precision machined assembly utilizing ball bearings which are pre-loaded to provide a runout of less than several hundred micro inches. The assembly contains the phase lock ring which is used for sectoring the lower platter and for the spindle speed control. It also provides a mounting location for the lower platter is dual platter disk drives. A permanent magnet clutch, used to engage the hub of the removable cartridge, is mounted on top of the spindle hub. A precision ground cone is also on the top of the spindle hub to accurately center the cartridge hub. The hub of the spindle assembly acts as an air pump to pump the filtered air into the area of the cartridge.

The drive motor is mounted on a mounting plate which, in turn, is mounted to the base casting. The drive motor provides the power to rotate the disks at the prescribed speed and drive the blower in the air system. This motor is a multiple winding, permanent split phase induction motor which is used to drive the spindle and the blower through a belt drive system. The drive train components consist of the pulleys at the spindle, the blower shaft, the motor, and the tension idler. The necessity of having a belt tension adjustment is avoided by spring-loading the tension idler to maintain a constant belt tension.

Top load models are provided with a brush cleaning mechanism which is fitted to the base casting. This system is made up of an induction gear motor and a cam which is fitted to the shaft of the gear box. The cam drives an arm assembly on which the cleaning brushes are mounted. The position of the cam is sensed by a snap-action switch.

The design of the D3000 disk drive provides maximum commonality of mechanical components between top load and front load models. The major difference between top load and front load machines is in that area which receives or adapts the cartridge to the disk drive.

In top load models of the disk drive, the cartridge adapter is a machined aluminum alloy casting which mounts to the top of the base casting. Mounted on this adapter is the cartridge lock mechanism with arms that pivot out over the top of the cartridge dust cover. The position of these arms is sensed with a snap-action switch. The arms can be locked or unlocked by a solenoid arrangement fitted to the adapter. Also mounted on the adapter are booms for supporting the magnetic transducers.

In front load models, a receiver assembly is fitted to the top of the base casting and is pivoted from supports attached to the base casting. This arrangement provides a mechanism for properly locating the cartridge into the disk drive. It also is the mechanism for disengaging the cartridge hub from the magnetic clutch on the spindle. A link arm which is integral with the bezel assembly provides the camming action to disengage the cartridge hub from the magnetic clutch.

Also, on front load models, a lower disk cover is fitted which supports the magnetic tranducer and photo-electric sensor pickups and provides a covering for the lower disk in dual disk machines. The analogous component in top load models is the disk cover which is an aluminum alloy separator mounted in the cartridge adapter, just above the lower disk area. The bezel assembly provides the decorative trim at the front of the disk drive and a suitable cover for the air system intake. In addition, for front load models only, the mounting arrangement for the door and the link arms provide the camming action for the receiver.

A dust cover, consisting of formed metal, is used to cover the disk drive and protect it from contamination. This cover is used on both top and front load models. The cover directs the air flow through the interior of the drive. It is held in place by the use of machine screws.

The ON/OFF power switch, RUN/STOP switch, and the indicators are mounted to the base casting by the use of a bracket located directly behind the bezel. The bezel, on top load models, may be removed without disturbing the operator switches or the wiring since there is no mechanical connection between the bezel and the switch bracket.

4.2.2 POSITIONER ASSEMBLY

The positioner assembly is a seperate modular unit that is mounted on a base plate which, in turn, mounts to the base casting. Mounted on this base plate are the positioner magnet structure, the ramp tower, and the shafts for supporting the carriage. The carriage is supported on a bearing structure by these shafts. The read/write heads are mounted into the carriage.

Also attached to the carriage is the positioner coil. This arrangement of magnet and coil provide a linear motor actuator for positioning the read/write heads. This type of arrangement is also referred to as a voice coil positioner. Carriage velocity is sensed using a velocity transducer consisting of a magnet within a specially wound coil. The transducer is mounted on the positioner base plate and the magnet is attached to a shaft connected to the carriage. The position of the carriage is detected and sensed using a photoelectric position transducer which is attached to the positioner base plate by a mounting strip.

200 tpi models have a temperature sensing element mounted on the positioner base plate. This thermistor is part of the temperature compensation circuitry included in 200 tpi models.

4.2.3 POWER SUPPLY ASSEMBLY

The power supply assembly is a major subassembly which mounts to the underside of the base casting and contains the power transformer, rectifiers, and filter capacitors. Also located on the power supply assembly is the Motor Control PCBA and the motor start capacitors.

4.2.4 READ/WRITE, SERVO, AND LOGIC PCBAS

The partitioning of the electronics system is primarily functional; the three major PCBAs in many ways constitute the major partitioning of the D3000 electronics. These PCBAs are the Read/Write PCBA, the Servo PCBA, and the Logic PCBA. In addition to the functional descriptions contained in this section, detailed descriptions of these PCBAs are contained in Section V.

The electrical and electronic components comprising the main chassis group, the positioner assembly, and the power supply chassis are interconnected with the PCBAs

through use of interconnecting cable assemblies. THE Read/Write PCBA is located adjacent to the positioner assembly and the head cables connect directly to this board. The Read/Write PCBA is constrained by self-locking card guides. The Logic PCBA is mounted on pivoting supports which are directly mounted to the base casting. Hinged on the face of the Logic PCBA is the Servo PCBA; these PCBAs are interconnected by interboard flat cables.

4.2.5 TEMPERATURE COMPENSATION AND SYSTEM COMPENSATION PCBAS (200 TPI MODELS)

The temperature compensation assembly which is included in 200 tpi models is comprised of a Temperature Compensation PCBA and a thermistor assembly. The thermistor assembly is mounted on the positioner base plate, and the System Compensation PCBA is mounted on the front switch bracket and is functionally associated with the Temperature Compensation PCBA.

4.3 FUNCTIONAL SUBSYSTEMS

The major functional groups of the disk drive are illustrated in Figure 1-4; these major groups, functionally discussed in the following paragraphs, are:

(1) Positioner and Positioner Electronics
(2) Read/Write Electronics
(3) Disk Drive Function Control
(4) Spindle Speed Control
(5) Position Control Logic
(6) Sector Electronics
(7) Motor Control
(8) Power Supply
(9) Temperature Compensation and System Compensation

4.4 POSITIONER AND POSITIONER ELECTRONICS

An essential function in a moving head disk drive is the positioning of the read/write head at the correct cylinder. This is accomplished in the D3000 Disk Drive by the Positioner Servo Electronics and the Positioner Assembly.

4.4.1 POSITIONER ASSEMBLY

The Positioner Coil and Moving Mass (linear motor), Velocity Transducer, and Position Transducer are the three major functional entities which comprise the Positioner Assembly. Figure 4-2* shows the relationship of these subsystems to the Positioner Servo Analog Circuits and the Positioner Control Logic.

The linear motor consists of a stationary permanent magnet and a positioner coil attached to the moving-mass, i.e., the carriage and magnetic head assembly. A description of the physical arrangement of the Positioner is contained in Paragraph 4.2.2.

Functionally, the magnet structure and the ways that the carriage rides on are the stationary portion of the linear motor. The moving structure consists of the carriage, the positioner coil, the heads mounted into the carriage, the bearings which support the carriage on the ways, and the moving portions of the Velocity Transducer and the Position

*Foldout drawing, see end of this section.

Transducer. The force that is necessary to move the moving-mass portion of the Positioner is a function of the inter-reaction of the magnetic fields produced by the permanent magnet structure and the magnetic field resulting from the current in the positioner coil. This force may be used for purposes of accelerating or decelerating the moving-mass, or as a restoring force for the purposes of holding the moving-mass in a given position. To a first approximation, the force developed is proportional to the current in the positioner coil.

The Velocity Transducer provides an electrical signal that is proportional to the velocity of the moving mass and consists of a permanent magnet moving inside of the specially wound coil. This coil is attached to the positioner baseplate and is stationary; the magnet is mounted on a shaft which is attached to the carriage. The amplitude of the signal derived from the Velocity Transducer is approximately equal to the actual moving-mass velocity. The magnitude of this signal is indicative of the speed of the mass and its polarity indicates the algebraic sign of the velocity.

The Position Transducer is a photoelectric sensor that develops four electrical signals, each serving a specific function for use in controlling the positioner. An incandescent lamp, mounted in the position transducer body, supplies illumination to a group of photodiodes located opposite the lamp and within the body of the Position Transducer. The transducer body is mounted stationary to the positioner baseplate by the use of a mounting strip.

Attached to the carriage is a precision scale which is part of the moving-mass. This scale is interposed between the lamp and the photodiode and consists of opaque and transparent areas in specific patterns. Also interposed between the scale and the photodiodes is a precision reticule which is also made up of opaque and transparent areas in specific patterns. The combination of the reticule patterns and the scale patterns are used to control the amount of illumination reaching the photodiode group.

Two of the signals developed by the Position Transducer as a function of carriage position are level change type of signals. One signal, the Heads Retracted signal, changes state when the carriage is approximately one-fourth-inch from the fully retracted position and is used to indicate the gross carriage position, specifically, the retracted position of the heads. The other signal is the Position Transducer Index signal which is used to define the legal range of the carriage position. This signal is a multi-change-of-state signal. One of the transitions of this signal is used in the initialization process during a head loading operation.

The other two signals derived from the Position Transducer are referred to as X+0 and X+90. These signals are linear signals that are cyclic as a function of cylinder position, and bi-polar in terms of polarity. They are displaced in electrical phase by approximately 90 degrees.

All of the signals from the Position Transducer are current signals proportional in amplitude to the illumination of the specific photodiode associated with that signal. The X+0 and X+90 signals are actually derived from photodiode pairs rather than a single photodiode.

4.4.2 POSITIONER ELECTRONICS

The Positioner Electronics consists of two major groups; the Position Control Logic and the Positioner Servo Analog Circuitry. The relationship of these subsystems to the Linear Motor, Velocity Transducer, and Position Transducer is shown in Figure 4-2. The entire

arrangement comprises a servo mechanism whose purpose is to control the mechanical position of the carriage and, hence, the position of the heads or a time derivative of carriage position such as the carriage velocity.

The servo mechanism may be operated in one of two modes, a Position Mode where the position of the carriage is controlled, or the Velocity Mode where the velocity of the carriage is controlled. The servo is switched between Position Mode and Velocity Mode, or vice versa, by means of transistor switches which are controlled by the Position Control Logic. The Position Control Logic determines the specific mode of operation on the basis of commands input to it from the interface and the status of the signals derived from the position Transducer.

Additionally, as shown in Figure 4-2, the Linear Motor can be disconnected from the servo and operated off of the Emergency Unload Capacitor. This emergency unload system provides a means of independently supplying power to the Linear Motor during emergency situations. This network is independent of the servo electronics for purposes of high-speed retraction of the heads from the storage surface during emergencies. The Emergency Unload Relay acts as a double-pole, double-throw switch to connect the Positioner Coil to either the output of the Power Amplifier and the Current Sensor, or to the Emergency Unload system. It should be noted that when the positioner is executing an emergency unload it is not operated as a servo and therefore functions in an open-loop manner.

The Emergency Unload Relay Driver receives its commands from the Logic PCBA via the Emergency Unload Enable (LEUEG) line. When the Emergency Unload Relay is energized, the positioner coil is connected to the servo; specifically, it is connected to the output of the Power Amplifier and to the Current Sensor. The Power Amplifier, in conjunction with this Current Sensor, forms a voltage-to-current converter providing a current in the positioner coil that is proportional to the applied input voltage to the Power Amplifier. As previously mentioned, the available force for moving the carriage is proportional to the positioner coil current to a first approximation, and the Power Amplifier, being a voltage-to-current converter provides a current that is proportional to its input voltage.

Therefore, the output of the Summing Amplifier, which is the input to the Power Amplifier, determines the force applied to the carriage where the force is approximately proportional to the output voltage of the Summing Amplifier.

The Summing Amplifier input is the major summing junction of the servo. Applied to this Summing Amplifier are the servo commands and the feedback which nulls these commands. Therefore, the servo loop functions to reduce the voltage at the Summing Amplifier input by providing an output voltage which results in a feedback signal which nulls the command signal. Additionally, on 200 tpi models, a temperature compensation signal is applied to this summing junction.

One of the input commands to the Summing Amplifier is the velocity reference. The velocity reference command is a request for a specific velocity when the loop is operating in the fast velocity mode. This velocity reference is derived from the Velocity Function Generator. The polarity of this reference is determined by the Polarity Select Network and is applied to the input of the Summing Amplifier through a transistor switch. The Polarity Select Network consists of U9, Q2, and transistor switch Q3, located on the Servo PCBA (Schematic No. 102810).

The Velocity Function Generator is a digital-to-analog converter which has a single polarity output. The address difference input is a digital signal that is the binary representation of the difference between the demand address from the interface and the current address defining the current positioner position. The output of the Velocity Function Generator is an analog voltage representative of the address difference. Therefore, the specific velocity requested is a function of the distance to be traveled in achieving the demand address.

The address difference is specified on the Address Difference lines in binary form where NLAD0G is the least significant bit and NLADEG is the most significant bit. The decimal address difference number may be expressed as the sum of the active bit weights. Each address difference being assigned a specific bit weight. The bit weights are ascending powers of two, where bit number 0 is decimal bit weight number 1; bit number 1 is decimal bit weight number 2; bit number 2 is decimal bit weight number 4, etc., to the extension bit number where the bit weight is 256. The address difference as specified on the Address Difference lines determines the magnitude of the velocity reference generated by the Velocity Function Generator.

Referring to the Servo Board Schematic No. 102810, it can be seen that the Velocity Function Generator portion of the velocity function decoder/encoder consists of U12C, U12B, U5B, U5A, U4C, U5C, U4B, U5D, U4D, U3D, U4A, U3C, U4E, U3B, U4F, U3A. The remainder of the Velocity Function Generator is the digital-to-analog conversion arrangement consisting of a resistor network, a current-to-voltage converter, and diode switches. The purpose of this arrangement is to take the digital signal encoded by the velocity function decoder/encoder and convert it into a current of a specific value which is then applied to the current-to-voltage converter. The summing junction of U8 (located on the Servo PCBA) functions as a current-to-voltage converter producing a voltage level which is determined by the address difference value. The resistor network is R1, R2, R7, R8, R10, R11, R16, R17, R18, R19, R20, R21, R24, R25. The diode switches are CR1 through CR12. The current-to-voltage converter consists of U8 in conjunction with Q1.

Referring to Figure 4-2, the output magnitude of the Velocity Function Generator is the velocity reference which is utilized during seeks. This reference is determined by the address difference value. The polarity of the velocity reference which determines the direction of the velocity is controlled by the Polarity Select Network. The Polarity Select Network in turn is controlled by the Forward Direction (LFDX1) line from the Position Control Logic. The Transistor Switch, which switches the velocity reference to the Summing Amplifier, is controlled by the Velocity Reference Enable (NLVREG) line from the Position Control Logic. When the positioner is executing a high-speed seek and is not operating as a position servo the Velocity Reference Enable (NLVREG) line will be active, thereby switching to the velocity reference from the Velocity Function Generator.

Other commands which may be applied to the input of the Summing Amplifier are for controlling the positioner in the Slow Velocity mode, i.e., during loading and unloading of the heads. The Slow Velocity mode is also used when executing a Restore operation. The Slow Velocity mode is determined by a velocity reference in the Mode Control Circuits, which in turn are controlled by two logic signals, Forward Slow Mode (NLFSM1) and Reverse Slow Mode (NLRSM1).

The two slow mode control signals, NLFSM1 and NLRSM1, are developed by the Position Control Logic and control transistor switches in the Mode Control Circuits which establish the Slow Mode velocity reference. Transistor switch Q7, in conjunction with R44, CR21, R45, and R46 on the Servo PCBA, are used for switching and determining the level of the Forward Slow Mode velocity reference.

It should be noted that the polarity of the reference, and hence the direction of motion, is determined by the power supply voltage in the particular circuit. Likewise, Q8, in conjunction with R49, CR25, and R50, R46, determine the Reverse Slow Mode velocity reference.

Additionally, command signals Track Offset Plus (NLTOPG) and Track Offset Minus (NLTOMG) from the Position Control Logic can be used to determine position mode offset through use of position reference voltages derived in the Mode Control Circuits. The track offset function is employed in the position mode for diagnostic purposes. The two logic signals, Track Offset Plus (NLTOPG) and Track Offset Minus (NLTOMG) operate transistor switches in the Mode Control Circuits to generate a position mode reference, thereby offsetting the heads from the nominal track center-line.

Referring to the Servo Board Schematic No. 102810, it can be seen that NLTOPG controls transistor switch Q5 which, in conjunction with R33, CR15, R34, and R35, determines the magnitude of the Track Offset Plus position reference. Likewise, Track Offset Minus controls transistor switch Q6 which, in conjunction with R38, CR19, R39 and R35, determines the Track Offset Minus position reference.

In addition to the commands controlled by logic signals that may be input to the main summing junction, an offset correction may be introduced by the Servo Offset Adjust, R22, on the Servo PCBA. There is also an external input test point provided to enable the introduction of external test signals into the summing amplifier. TP19 and R40 on the Servo PCBA perform this function.

Two separate and distinct feedback paths to the main summing junction are provided. One of these feedback loops is closed at all times when the servo is energized. This path, as shown in Figure 4-2, is from the Velocity Transducer, through the Velocity Transducer Amplifier, to the Summing Amplifier input. The Velocity Transducer Amplifier merely amplifies the low level signal from the Velocity Transducer to a high level signal that is proportional to the velocity of the carriage. Since this feedback path is closed at all times, a damping in the Position mode of operation is provided. In the Velocity mode, this feedback nulls velocity commands.

The other feedback path is used only in the Position mode. This path takes the X + 0 signal from the Position Transducer, conditions it to a voltage signal in the Position Transducer Amplifiers, and then switches it to the Summing Amplifier input. The transistor switch Q13 on the Servo PCBA performs the switching function and is controlled by the Position Mode signal (LPMXG) from the Position Control Logic.

As previously discussed, four signals are provided to the Position Control Logic which are derived from Position Transducer signals. These four signals are the X + 0, X + 90, Heads Retracted, and Position Transducer Index. They are converted from current signals into voltage signals by current-to-voltage converters that are contained in the Position Transducer Amplifiers. These current-to-voltage converters are U1, U6, U2, and U7 located on the Servo PCBA.

Since the output of the Position Transducer Amplifiers are an analog voltage and therefore unsuitable for direct application to logic, they are converted into digital signals by analog-to-digital converters. These converters are, in essence, a special type of Schmitt trigger and are comprised of U11 and U10 on the Servo PCBA. The signals which are fed back to the Position Control Logic are: Position Reference Clock (SPRCG), Position Quadrature Clock (SPQCG), Heads Retracted (SHRXG), and Position Transducer Index

(SPTIG). These signals are utilized by the position control logic to determine the operation of the positioner servo in conjunction with commands from other parts of the logic and the I/O interface.

Additionally, failure of the lamp in the Position Transducer is detected by the Lamp Failure Detector. A signal derived from this detector is fed back to the Position Control Logic for purposes of determining when an emergency condition exists. This signal is Position Transducer Failure (SPTFG).

4.5 READ/WRITE OPERATIONS

The double frequency recording method is used in reading and writing data in the D3000 Disk Drive. Read/Write operations are accomplished by a read/write head. During a Write operation, a bit is recorded on the disk whenever the coils of the read/write head are switched by the Write Driver circuits. During a Read operation, a clock or data bit is sensed on the disk whenever the flux direction induced in the coil winding is reversed as a result of a change in polarity of the flux pattern presently passing under the head gap.

4.5.1 DOUBLE FREQUENCY RECORDING

A basic clock frequency signal is encoded in the data pulses to produce a single composite signal at the read/write head. The composite signal represents either a logic zero bit condition or a logic one bit condition for each bit-cell time defined by the clock.

The double frequency method, shown in Figure 4-3, makes use of a clock frequency to establish the basic bit-cell timing cycle. The insertion of a data pulse between clock pulses in a bit-cell period produces a composite read/write signal which uses only clock pulses for a logic zero bit indication, and data pulses for a logic one bit indication. A zero (0) bit-cell (clock pulses only) produces a single change in direction of the flux pattern. A one (1) bit-cell (data pulse located between two clock pulses) produces a double change in direction of the flux pattern. In either case, the clock signal causes a change in direction of magnetism from plus to minus or minus to plus polarity, thus causing the storage of a bit. Because both clock and data information are synchronized on a composite signal, double frequency recording is sometimes referred to as *self-clocking.*

In double-frequency recording, a clock bit is always inserted at the beginning of each bit-cell time to establish the basic recording frequency. A data bit is inserted between clock bits (at twice the frequency) so that the data bit results in two flux reversals within a single bit-cell time. If the data bit is not present, a single flux reversal occurs in a bit-cell time.

The recording head is a split-ring core containing coil windings so that a magnetic field with a given flux direction prevails at the core gap while the coil is energized. When current flows through the coil, the flux induced in the core establishes a fringe flux at the gap. As a magnetic recording surface passes by the gap, the fringe flux magnetizes the surface of the disk.

During a write operation, a bit is recorded when the flux direction in the core is reversed by switching between coils of the read/write head. The fringe flux is reversed at the gap and, hence, the portion of the flux flowing through the recording medium is reversed. If the flux reversal is considered instantaneous in comparison to the motion of the recording surface, and the gap is observed at the moment of reversal, it can be seen that the portion of the surface that just passed the gap is magnetized in one horizontal direction while the portion directly under the gap is magnetized in the opposite direction. Between these two areas, the flux must reverse 180 degrees; this recorded flux reversal represents a bit.

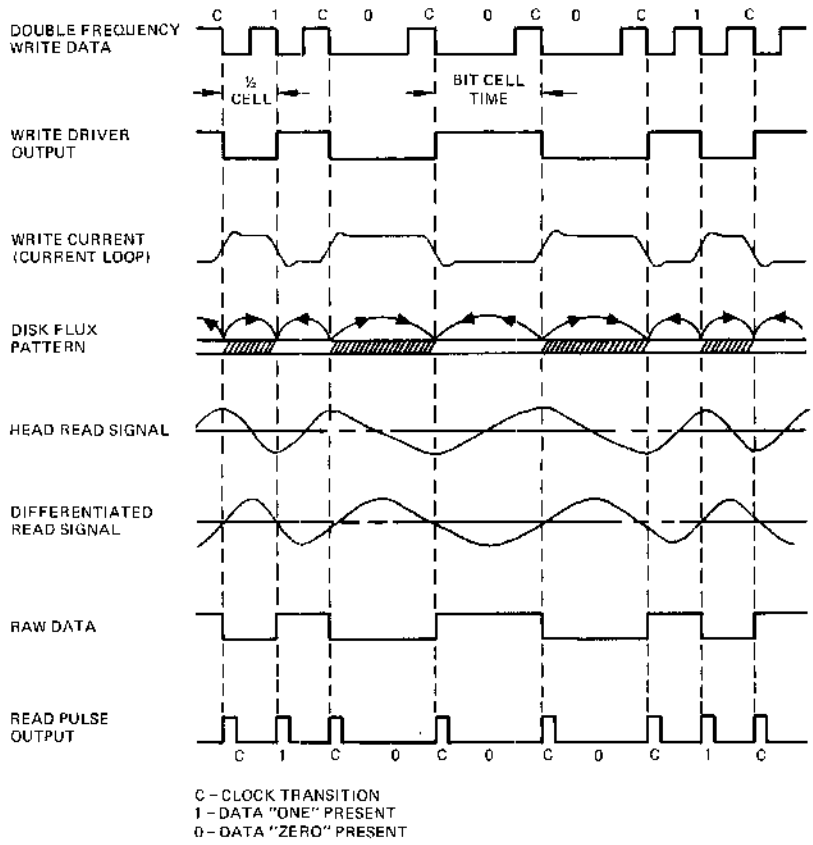


Figure 4-3. Double Frequency Recording Flux and Pulse Relationship

During a read operation, the gap first passes over an area that is magnetized in one horizontal direction, and a constant flux is induced into the core and the coil. The coil provides no instantaneous output voltage for this condition. However, when the recorded bit (180 degrees horizontal flux reversal) passes the gap, the flux induced into the core and coil must go through a 180-degree reversal. This reversal means that the coil sees a change in flux which results in a voltage output pulse.

4.6 READ/WRITE ELECTRONICS

The Read/write Electronics are contained on a single printed circuit board assembly (PCBA). Figure 4-4* is a functional block diagram of the D3000 read/write system and should be referred to for the following discussion.

4.6.1 HEAD SELECT

Head selection in the D3000 is accomplished by signals from the using system via the Platter Select (IPXSR) and Head Select (IHSXR) I/O interface lines. The signals on these lines are required to select one of four read/write heads. Table 3-1 shows the head select decoding used in the D3000 Disk Drive.

*Foldout drawing, see end of this section.

4.6.2 WRITE ELECTRONICS

Information to be recorded is supplied to the disk drive via the Write Data Signal (IWDSR) I/O interface line. The writing process is under complete control of the logic functions and control circuitry (Paragraph 4.7). Verification of system readiness, a software function, is required prior to initiation of a write operation. The conditions that must be satisfied before a write operation can be performed are:

(1) The unit must be in the Ready condition and Selected. This implies that only one head is selected.

(2) The heads must be positioned over a legal track address.

(3) The WRITE PROTECT switch for the platter selected is switched to the OFF position and the Power Clear signal is at a high level.

The disk drive is conditioned to perform a Write operation when the Write Enable (IWEXR) line is low. At this time the Write drivers are receptive to Write Data pulses. When the Write Enable line is active and system readiness is satisfied, current flows through the write coil recording new data and causing all previous data to be overwritten, i.e., obliterated.

The read/write coil is a split center-tapped winding. During a write operation, current flows in alternate halves of the read/write coil. Switching of write current in each half leg causes magnetic flux reversals on the disk surface. It is important to note that when the disk drive is in the Write mode the erase coil is also energized. The read/write gap is located in front of the erase gaps in both 100 and 200 tpi models. In 100 tpi models the alternating write flux pattern magnetizes a band approximately 0.0075 inches wide on the surface of the disk; in 200 tpi models the magnetized band is approximately 0.004 inches wide. The erase gaps, which straddle the read/write gap, erase part of the write flux pattern leaving a recorded band that is approximately 0.0065 inches wide for 100 tpi models and approximately 0.0036 inches wide for 200 tpi models. This provides a signal guard-band between adjacent tracks.

4.6.2.1 Write Driver

The Write Driver circuitry, shown in Figure 4-4, switches the write current to alternate halves of the read/write head winding. The rate at which the write current is switched is determined by the Write Double Frequency (NLWDFT) signal from the Logic PCBA. NLWDFT toggles a flip-flop whose outputs drive two write current control switching transistors into alternately conducting states. The write current drivers are enabled by a low logic level input on the Write Mode (NLWDFT) line at the Read/Write PCBA.

4.6.2.2 Erase Driver

The Erase Driver circuit is a transistor switch current source that is energized by the Erase Current Enable (NLECEG) signal input to the Read/Write PCBA. A low logic level at the NLECEG input enables the erase current to flow into the read/write head erase windings.

4.6.2.3 Write Current Control

The write current control causes the current level in the read/write coils to change as a function of the positioner cylinder address. In 100 tpi models, for cylinder addresses of 0 through 127 the current level is set at approximately 35 ma; at cylinder address 128 and above the current level is reduced to approximately 27 ma. This current level change is required because of the increased bit density at the inner-most tracks on the disk surface. The lower write current levels reduce the flux pattern fringe effects on neighboring bits. It is important to note that in 200 tpi models the write currents are slightly different than those given for 100 tpi models, and the lower current level is switched at cylinder address 256.

4.6.2.4 Write Emergency Monitor

This circuitry continuously monitors the legality of conditions within the read/write system. If conditions are improper, the write emergency monitor outputs an active high logic level to the emergency unload circuitry on the Logic PCBA. This causes the disk drive to execute an emergency unload operation. Conditions that would cause a read/write emergency unload operation are:

(1) More than one head is selected at one time.

(2) The current monitor circuitry indicates the presence of a current in either the write or erase circuits when such a current is not enabled by NLWMXG and/or NLECEG.

4.6.2.5 Current Monitor

The current monitor circuitry continuously checks the current level in the Write Driver and Erase Driver circuits and outputs a low logic level to the write emergency circuitry during a Write/Erase operation. When both the Write Mode and Erase Current Enable lines are at a high logic level the write emergency circuitry assumes that a Read operation is in progress and looks for a high logic level from the current monitor. Should the output of the current monitor be a low logic level at this time, the write emergency monitor will sense an illegal condition and cause the system to perform an emergency unload.

In addition to the current monitoring function, the current monitor circuitry can disable the flow of write or erase currents to the read/write heads. The Power Clear signal (SPCSA) generated on the Servo PCBA indicates the status of the regulated dc voltages and controls a transistor switch in series with the common write/erase current path. In case of a power failure, SPCSA goes to a low level, causing the transistor switch to open the write/erase current line. This action prevents the writing of erroneous information on the disk surface during a power failure emergency unload condition.

4.6.3 READ ELECTRONICS

A Read Enable (IREXR) signal from the system I/O interface conditions the Read/Write circuitry to perform a Read operation. Certain readiness checks must be performed by the disk drive Function Control Logic circuitry before information can be transferred from the surface of the disk to the system I/O interface. The selected disk drive must be in the Ready condition; this implies that the following conditions exist:

(1) The heads are positioned over a legal track address.

(2) Only one head is selected.

(3) The Write Enable and Erase Current Enable lines are both high and the current monitor senses no write or erase current flow.

The Read Electronics are activated when both the Write Mode and Erase Current Enable inputs to the Read/Write PCBA are at a high level. This condition is locally ANDed resulting in the Read/Write head windings being connected to the read preamplifier. The amplified read data are filtered, peak detected, digitized, and decoded before being suitable for transmission to the using system interface. When the Read Enable Control (NLRECG) signal to the Read/Write PCBA goes low, the Read Data (IRDXR) and Read Clocks (IRCXD) are gated onto the system I/O interface lines. A detailed discussion of the Read Electronics portion of Figure 4-4 is contained in the following paragraphs.

4.6.3.1 Head Switch Circuitry

The Head Switch circuitry disconnects the Read preamplifier signal inputs from the read/write heads during a Write/Erase operation. This is done to prevent the large voltage signal levels that are applied to the head's read/write windings during a Write operation from entering the low level inputs of the read preamplifier. Thus, the Head Switch circuitry prevents the amplifier from being driven into saturation during a Write operation.

4.6.3.2 Read Preamplifier

The Read Preamplifier is a single integrated circuit consisting of a wide band, linear differential amplifier stage. Read signals from the read/write heads are typically quasi-sinusoidal with typical amplitudes of approximately 1 mv to 5 mv. The nominal voltage gain of this amplifier is 50 in 100 tpi models and 150 in 200 tpi models; the read signal output has an amplitude of approximately 200 mv peak-to-peak. The amplifier gain is determined by a resistor of appropriate size across the gain-adjust terminals.

4.6.3.3 Filter

The amplified read signal is ac-coupled to an L-C filter stage which removes the undesirable high-frequency noise signals superimposed on the read signal. The special quality of the filter is its ability to pass the read signal with only small attenuation and negligible phase variation.

4.6.3.4 Variable Gain Amplifier

The filtered read signal is amplified by the Variable Gain Amplifier stage. This amplifier has a nominal voltage gain of approximately 7.3 under normal operating conditions; thus, the read signal output is normally 350 to 650 mv peak-to-peak. In the read margin test mode, the gain of the amplifier stage is reduced to approximately 2.6.

4.6.3.5 Peak Detector and Squarer

The 350 to 650 mv read signal drives a differentiating type peak detector which converts the sinusoidal read signal into digital data by switching its output voltage level at each positive and negative peak of the read data signal. The operation of the peak detector is illustrated in Figure 4-5.

The output voltage signal from the differentiator is a 1.2v peak-to-peak amplitude that swings +0.6v peak about a zero voltage reference. Prior to decoding, the read data are converted into a pulse train at a frequency that is twice the read data rate. The action of the edge detector is shown in Figure 4-6. The pulse width of the signal is controlled by component values within the edge detector circuitry.

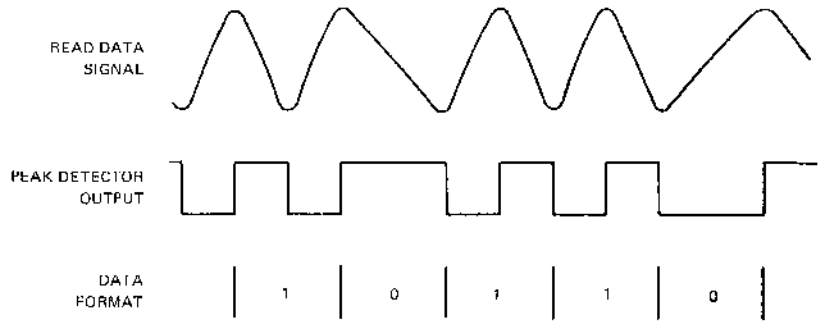


Figure 4-5. Peak Detector and Squarer Waveform

4.6.3.6 Data Decoder Circuitry

The Data Decoder circuitry is essentially a data/clock separator. It is comprised of two one-shot multivibrators, a decoding window generator and a window polarizing circuit. The Read Pulse Narrow (RPN) signal has a nominal data rate frequency when read data are all zeros, and is twice this frequency when read data are all ones. It is this characteristic that enables the Data Decoder circuitry to separate read data from the clocks.

The first RPN pulse is treated as a clock pulse. Its leading edge clocks the ones window flip-flop to look for a data bit. At the end of the one-shot timing, the ones gate is reset and the next RPN pulse is another clock pulse. If a RPN pulse is present between the clock pulses, it is treated as a data bit or a *one* bit and presented to the Read Data interface line. The *ones* data output repetition rate will therefore be at the read clock rate. The timing diagram shown in Figure 4-7 details these timing relationships. Two pulse former one-shots determine the output pulse width.

4.6.3.7 Read Data Control

The Read Data Control gates the Read Clocks and Read Data onto the system I/O interface lines, via line drivers on the Logic PCBA, in response to the Read Enable Control (NLRECG) signal. When Read Enable Control is initiated, the Read Clock and Read Data gate control is clocked to the enable state. This prevents pulse *shaving* of the Read Data and Read Clock signals.

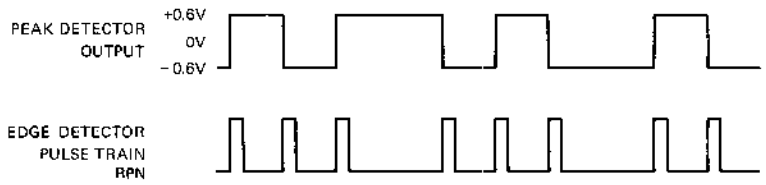


Figure 4-6. Edge Detector Timing Relationship

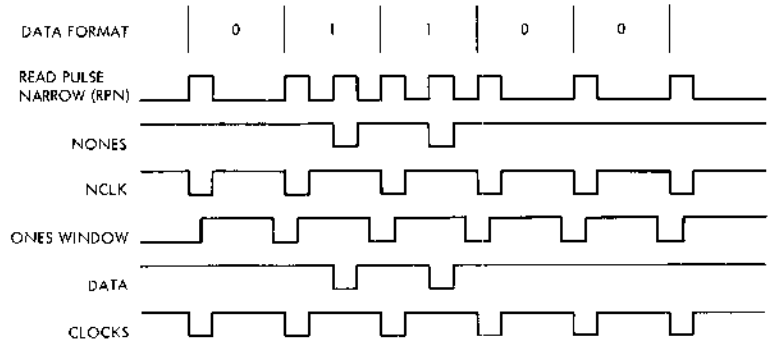


Figure 4-7. Data Decode Timing Relationships

4.7 LOGIC FUNCTIONS AND CONTROL

There are five major areas in the D3000 Series Disk Drives which require logic for control of functions and timing, these are: Disk Drive Function Control, Read/Write Electronics, Spindle Speed Control Electronics, Position Control Electronics, and Sector Electronics. They are functionally shown in Figure 1-4. Since the majority of logic in the D3000 is packaged on the Logic PCBA, the following is primarily a functional description of the Logic PCBA. Only those areas on other circuit boards having logic functions of interest are included.

NOTE

In order to fully understand the logic functions described, the reader should acquaint himself with the discussion of the specific integrated circuits contained in Section V. He should also become familiar with the schematics contained in Section VII.

4.7.1 LOGIC ARRANGEMENT

The Logic PCBA is depicted on sheets 2 through 5 of Schematic No. 103704. These sheets have been divided on the basis of function and, therefore, a specific sheet is a complete (or nearly complete) schematic representation of a specific function. The following discussion identifies these functions by schematic sheet number.

4.7.1.1 Logic Schematic, Sheet Two

Sheet two of the Logic schematic contains the Start/Stop Control which is used in the control and timing process of executing the start cycle of the disk drive and for executing the stop cycle of the disk drive. Also shown on this sheet is the main clock generation circuitry which consists of the crystal oscillator, clock countdown and clock gating circuitry. This arrangement provides the reference for all timing functions on the Logic PCBA.

A subdivision of the Start/Stop Control is also included. This circuitry is used for the detection of run/stop commands, emergency and fault mode control, interlocking control, start cycle sequencing, stop cycle sequencing, and condition indication.

4.7.1.2 Logic Schematic, Sheet Three

Sheet three of the Logic schematic contains a number of minor functions; these are the select enable controls, the read outputs, the status outputs, the termination voltage power supply, and the spindle speed control digital logic.

A subdivision of the select enable function is the head and platter select control, track offset enable control, write/erase enable control, unit select decoding, busy signal encoding, write protection control, and the status and indication circuitry.

4.7.1.3 Logic Schematic, Sheet Four

The functions shown on sheet four of the Logic schematic deal entirely with position control; these are the demand address register, the valid address decoder, the current address counter, the count control, subtractor and complementor, carry control, the load address and illegal address control, busy logic, mode control, operation control, and error check logic.

4.7.1.4 Logic Schematic, Sheet Five

The functions shown on sheet five of the Logic schematic consist entirely of sector electronics. These functions consist of the upper sensor detector, the upper time demultiplexer, the lower sensor detector, lower time demultiplexer, sector phase lock loop, upper sector countdown, lower sector countdown, sector multiplexer, index multiplexer, sector pulse formers, index pulse formers, upper sector number counter, lower sector number counter, sector count multiplexer, and the multiplexer control.

4.7.2 DISK DRIVE FUNCTION CONTROL

The Disk Drive Function Control Logic is one of the major sub-divisions of the disk drive which require logic for the control of functions performed. Figure 1-4 is a functional block diagram of the D3000 Disk Drive and should be referred to in conjunction with the following paragraphs.

The major block identified as Disk Drive Function Control in Figure 1-4 can be sub-divided into two parts: a major block consisting of the Start/Stop Control, and a minor block containing minor control functions, e.g., head select control, unit select decoding. The following paragraphs contain a functional discussion of these blocks.

4.7.2.1 Start/Stop Control

Essentially, the Start/Stop Control is a digital sequential machine mechanized with integrated circuit logic. The purpose of this logic is to take external commands, combine them with internal conditions plus suitable timing, and generate output signals for control and indication purposes. Figure 4-8 is a block diagram of the digital sequential machine used to mechanize the start/stop control.

The three essential blocks, shown in Figure 4-8, are State Storage, Combinational Logic, and Delay Generator. The purpose of the State Storage block is to store the machine states. This is mechanized with flip-flops and a counter. The present states are combined in the Combinational Logic with external commands which allows the generation of output signals for indication and control by the output signal combinational logic. All of the combinational logic is mechanized with gates. It should be noted that external commands can modify directly the stored states. This is in addition to the capability of external commands in combination with the present states to provide output signals and modification of the stored states.

Included in the block diagram is a Delay Generator which is mechanized with counters and a flip-flop. The generator provides specific delays under control of certain of the Combinational Logic output signals. The Time Reference to the Delay Generator is obtained from a crystal oscillator and clock countdown circuits.

Figure 4-9* is a functional block diagram of the Start/Stop Control. All of the logic depicted in this figure is contained on sheet two of the Logic PCBA schematic. The time reference for this arrangement is provided by a Crystal Oscillator whose output signal is frequency divided by the Clock Countdown circuitry. This circuitry consists of a series chain of counters that generate clock signals that are used by the Start/Stop Control logic. These clock frequencies are also used in other portions of the disk drive logic.

Within the Start/Stop Control, gating of the clock signals is accomplished by allowing clock pulses to be fed to the flip-flops only at specific times, thereby permitting these flip-flops to change state only when a clock pulse is present. The delay generation portion

*Foldout drawing, see end of this section.

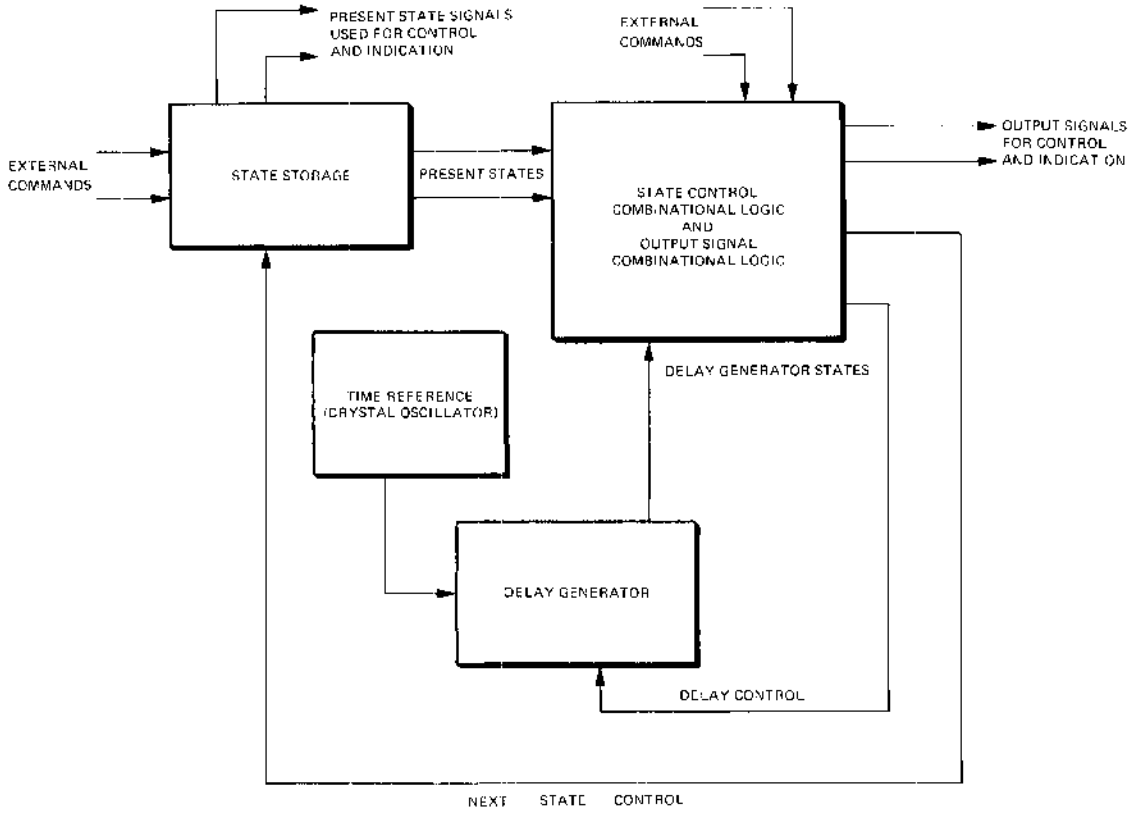


Figure 4-8. Digital Sequential Machine Block Diagram

of Start/Stop Control is handled by a Delay Counter which is operated from a clock signal generated by the Clock Countdown circuitry.

In addition to the state storage there are three major functions performed by the Start/Stop Control; these are interlocking control, emergency unload logic, and condition indication.

Referring to Figure 4-9, commands used to start or stop the disks may be received either from the RUN/STOP operator control or from the Start/Stop Disk Drive I/O interface line (ISSDR). These commands are detected by the Run/Stop command and Detection circuitry and cause the Start/Stop Control to execute a start or a stop, as appropriate.

Interlocking is obtained by using a number of signals which are available within the disk drive. These signals, used in conjunction with each other, allow interlocking of various mechanical functions, e.g., locking the door on front load machines, and locking the cartridges in top load machines when the disk is rotating. The Lower Detector Pulse (LLDPG) input to the Interlock Control portion of the logic is used to establish that the disk is rotating. The Not Write Or Erase signal (NLWOEG) is generated by some of the minor control logic within the Disk Drive Function Control block and is used to prevent

retracting the heads during a normal unload when either a Write or an Erase command from the I/O interface is occurring.

Correct insertion of the cartridge is detected by two switches in top load machines, and by one switch in front load machines. This interlock prevents starting the disk drive when the cartridge is not inserted. In top load machines the parked position of the cleaning brushes is interlocked by a switch for purposes of determining that the brush cleaning cycle has been satisfactorily completed.

The Power Clear signal (SPCSA) from the Servo PCBA signals when an unacceptable power supply condition is sensed. The SPCSA signal is provided to the Start/Stop Control logic as well as to the Read/Write PCBA. Also supplied from the Servo PCBA is the Heads Retracted signal (SHRXG) which is used by the Interlock Control to ensure that the disk does not stop rotating unless the heads are retracted.

The purpose of the Emergency Unload Logic is to begin an emergency unload operation when commanded externally, or when this logic detects certain fault situations which require emergency unloading of the heads from the storage surface. One of these fault conditions is the Position Transducer Failure (SPTFG) condition. This condition is detected on the Servo PCBA and is provided to the Emergency Unload Logic should a failure occur in the position transducer. Another signal, the Write Emergency Condition (RWECG) is generated on the Read/Write PCBA should a write emergency condition be detected. Additionally, the Activate Emergency Unload (IAEUR) I/O interface line is provided for commanding emergency unloads from the I/O interface.

All other emergency unload conditions are detected by logic circuitry on the Logic PCBA. Three of these emergency conditions are detected within the Start/Stop Control arrangement by the Emergency Unload Logic. The signals utilized are: Not Position Mode (NLPMXG), Speed Out of Tolerance (LSOTF), and an internal signal within the Start/Stop Control logic. This internal signal is generated by the Interlock Control Logic from the state of the Brushes Parked switch and is not shown on the block diagram. The Not Position Mode (NLPMXG) logic state is tested by the Emergency Unload Logic to determine if the heads have properly loaded during a start sequence. Speed Out of Tolerance (LSOTF) is tested during the start sequence to determine if the disks have reached the proper speed prior to loading the heads. The internally generated signal from the brushes parked switch is tested to determine that the brush cleaning cycle has been correctly completed.

Elsewhere within the logic, three signals are generated upon detection of a specific fault condition and are provided to the Emergency Unload Logic. These signals are Not Position Limit Error (NLPLEG), Not Disk Speed Error (NLDSEG), and Not Seek Time Error (NLSTEG). The Not Position Limit Error signal commands emergency unload when the positioner exceeds its legal range of travel. The Not Disk Speed Error signal commands an emergency unload when a disk speed error is detected after the system achieves the Ready condition. The Not Seek Time Error signal commands an emergency unload when the time for a seek exceeds the allowable maximum.

The major function control output signals from the Start/Stop Control are:

(1) Start Drive Motor (NLSDMG), a pulse used for initializing the spindle speed control logic.

(2) Purge Cycle (LPCFF), a flip-flop output state used for controlling the disk speed during the purge cycle.

(3) Load Heads (LLHFF), a flip-flop output state used for controlling the position control logic and loading and unloading the heads.

(4) Emergency Unload (LEUFF), a flip-flop output state used to indicate that an emergency unload condition has started or presently exists.

(5) Load or Purge Not (NLLPNG), the output of combinational logic within the Start/Stop Control; this combinational logic decodes the states of two of the major state storage flip-flops, Purge Cycle and Load Heads. NLLPNG is used for initializing the position limit monitor contained within the Position Control Logic.

(6) Brush Motor Enable (NLBMEG), controls the power to the brush motor in top load models of the disk drive for operating the disk cleaning brushes.

(7) Brake Cycle Enable (NLBCEG), the control signal which determines when the braking current is applied to the disk drive motor.

(8) Lock Cartridge Mechanism (LLCMG), controls the solenoid drivers on the Servo PCBA and is the signal which determines when the cartridge mechanism is locked or unlocked.

(9) Emergency Unload Enable (LEUEG), controls the emergency unload relay driver on the Servo PCBA; this relay driver, in turn, actuates the emergency unload relay as commanded by the Emergency Unload Enable signal.

The output signals from the Start/Stop Control circuitry described in (1) through (5) are used on the Logic PCBA for specific control functions. The signals described in (6) through (9) are fed directly to the Servo PCBA.

Three signals for driving the operator control panel lamps are generated by the Condition Indication portion of the Start/Stop Control logic. These signals are Safe Lamp Drive (NLSLDT), Run Lamp Drive (NLRXDT), and the Ready Lamp Drive (NLRLDT). The SAFE lamp is used to indicate when it is safe for the operator to remove or insert a cartridge into the disk drive; the RUN lamp is used to indicate when a machine is executing a start sequence, or the disk is running. Illumination of the READY lamp indicates that the disk drive has achieved the Ready condition.

Other signals generated by the Condition Indication logic are: Ready (LRXXG), Selected And Ready (LSARG), Delayed Ready Condition (LDRCG). The Ready signal is the output of combinational logic and is the combination of several flip-flop states within the Start/Stop Contol. The Selected and Ready signal is the Ready signal combined with the Selected signal from the unit select logic. The Delayed Ready condition is the Ready signal passed through a delay network. Ready, Selected And Ready, and Delayed Ready Condition signals are used in other parts of the Function Control Logic as well as enabling certain portions of the Position Control Logic and the Sector Electronics Logic.

4.7.2.2 Minor Control Functions

The minor functions discussed in the following paragraphs are contained within the Disk Drive Function Control logic block shown in Figure 1-4. Due to the nature of these minor control functions, no attempt is made to relate these functions to a simplified block diagram. The circuitry which performs these logic functions is contained on sheet three of the Logic PCBA schematic.

The Select and Control Logic consists of a holding register and associated control gates for processing the Platter and Head Select lines, the Track Offset Plus, and Track Offset Minus lines. Also included is the Write Double Frequency Data Re-transmitter which acts

as a line receiver and a line driver between the I/O interface and the Read/Write PCBA. The Unit Select Logic, the Busy Output logic, and the Ready driver are also included as minor elements in the Disk Drive Function Control Logic. Likewise, the Read/Write Control logic, the Write Protect logic including the Write Protect Lamp Drivers are part of the Disk Drive Function Control Logic. Additional minor functions are performed by the Read Signal Drivers, the Malfunction Signal Driver, the Double Track Status Driver, the Illegal Address Status Driver, and the Dual Platter Status Driver. These functions are described in terms of function and purpose, as follows.

Two I/O interface control lines are provided for selecting a specific storage surface. These lines are the Head Select (IHXSR) and Platter Select (IPSXR). Two other I/O interface control lines, Track Offset Plus (ITOPR) and Track Offset Minus (ITOMR) are provided for selecting specific track offsets for diagnostic purposes. The four lines, Head Select, Platter Select, Track Offset Plus, and Track Offset Minus are processed by the holding register and distributed to the Read/Write PCBA. The Track Offset Plus and Track Offset Minus lines are also distributed to the Servo PCBA.

The Holding Register performs a holding function to store the status of these lines under certain conditions. These conditions are determined by the Selected And Ready and the Not Ready conditions. The Write Double Frequency Data Re-transmitter acts as a line receiver for the I/O interface line Write Data Signal (IWDSR) and re-transmits the signal to the Read/Write PCBA as the Write Double Frequency signal. This acts as a buffer and maintains timing of the Write Double Frequency signal.

Another minor function provided by the Disk Drive Function Control Logic is contained in the Unit Select logic. This logic combines the setting of the Unit Number Selector switch on the operator panel with the specific Unit Select Number signal from the I/O interface. Decoding is performed and the Select signal is generated only when the Unit Select line from the I/O interface corresponds to the number designated for the specific disk drive by the Unit Number Selector switch on the operator panel.

Also contained within the Disk Drive Function Control Logic is the Busy Output logic. This logic combines the busy signal from the Position Control Logic with the Ready signal and encodes on a specific Busy Seeking line according to the setting of the Unit Number Selector switch on the operator panel.

A number of line driver functions are performed by various signal drivers. These drive internal logic signals onto the I/O interface lines as outputs of the disk drive. These are:

(1) The Ready Driver for driving the selected and ready signal onto the Ready line at the interface.

(2) The Read Signal Drivers for transmitting the outputs of the Read/Write PCBA on the Read Data and Read Clock I/O interface lines.

(3) The Malfunction Signal driver for transmitting the malfunction pulse on the I/O interface line.

(4) A Double Track Status interface line for indicating at the I/O interface when a disk drive is a 200-tpi model.

(5) The Illegal Address Status driver for transmitting the illegal address signal to the Illegal Cylinder Address I/O interface line.

(6) Dual Platter Status signal driver for indicating on the Dual Platter Drive I/O interface line that the disk drive contains two platters.

Another minor function control performed is the processing of the Write Enable (IWEXR) and Erase Enable (IEEXR) signals from the I/O interface. These signals are gated by Selected And Ready, Position Mode, and File Protect Mode, then transmitted to the Read/Write PCBA for controlling those functions on the Read/Write PCBA. In addition, the Not Write or Erase signal is generated for application to the Start/Stop Control Logic. Also performed within the Read/Write control logic is the gating of Read Enable with Selected and Ready. This signal is then transmitted to the Read/Write PCBA.

The Write Protect logic combines the state of the specific WRITE PROTECT switch on the operator panel with the state of the Platter Select (IPSXR) line such that the respective protect switch and the Platter Select line are decoded to set or reset the File Protect Mode latch. The state of the File Protect Mode latch determines whether a particular platter is permitted write and erase operations, depending upon whether it is designated as a protected platter by the respective WRITE PROTECT switch on the operator panel.

The state of the File Protect Mode latch is gated with Selected and Ready and is transmitted to the I/O interface by the File Protected Status Driver which transmits the file protect condition of the disk drive to the controller on the File Protected (IFPXD) I/O line. The state of the WRITE PROTECT switches is indicated by the operator panel PROT (Protect) lamps regardless of which platter is selected. The lamp indication depends entirely on the state of the respective switch. The lamp drive signals are generated by the protect lamp drivers according to the switch states.

4.7.3 SPINDLE SPEED CONTROL

The rotational speed of the spindle is controlled to within ± 1 percent of the nominal value. This tight control is maintained so that the spindle speed is not affected by line frequency variations and to avoid disk speed variations due to tolerances of the drive train components. The time reference for the spindle speed control is derived from the Crystal Oscillator and Clock Countdown logic that is shown in Figure 4-9 as part of the Start/Stop Control Logic.

The actual speed of the spindle is derived by sensing notches in the phase lock ring with a magnetic transducer. In addition to the speed sensing function, Phase Lock Ring and the Magnetic Transducer are used in conjunction with the Sector Electronics (Paragraph 4.7.5). The Phase Lock Ring is a flat circular plate with notches in the periphery. It is mounted integral with the spindle and therefore the rotational speed of the Phase Lock Ring is the same as that of the spindle. The Spindle Speed Control is a true servo loop in that power is controlled to the drive motor which, in turn, rotates the spindle; the actual speed of the spindle is sensed and compared with a time reference and the result of the comparison is used to correct the amount of power applied to the drive motor. In this manner, the loop corrects the existing speed of the spindle to the correct speed within the ability of its resolution and response capability. It is important to note that although the loop is a true closed loop se,vo it is not a linear servo system. The reason is that the result of the time/speed comparison is a single binary digit and therefore can have only twc possible states, a zero or a one, i.e., the speed is either too fast or too slow. For this reason the actual speed regulation takes place in a limit cycle type of operation where the actual spindle speed varies between an upper and a lower boundry as determined by the response time of the loop and the resolution of the error detector. However, certain of the loop characteristics are like a linear servo, in that power to the drive motor is varied for control by changing the time of occurrence of the application of power within a given power line cycle in a manner which is usually referred to as phase angle control. In other

words, the actual phase angle during the power line cycle where power is applied to the main winding of the drive motor is the result of the integral of the binary speed error. This determination is made from the comparison of the actual speed sensed by the Magnetic Transducer to the time reference derived from the Crystal Oscillator.

Refer to Figure 4-10*, a functional block diagram of the Spindle Speed Control Logic, for the following discussion. Operation of the spindle speed control can best be understood by starting at the Spindle and going around the loop. The Magnetic Transducer senses the notches in the Phase Lock Ring and produces a signal which is then processed by the Sector Electronics Logic (refer to Paragraph 4.7.5).

The results of the action taken by the Sector Electronics logic is the output of a flip-flop called the Phase Lock Flip-Flop (LPLFF). This flip-flop functions as a frequency divider on the basic frequency derived from the Phase Lock Ring and converts the pulse as processed by the sector electronics into a square wave. The Phase Lock Flip-Flop signal (LPLFF) is fed into the Speed Sequence Control as shown in the block diagram.

Clock signals derived from the Crystal Oscillator and Clock Countdown (LC02F, LC03F, LC04F) are fed to the Speed Control Programming logic, then to the Speed Control Counter. The time between the occurrences of low to high transitions of the Phase Lock Flip-Flop signal is detected by the Speed Sequence Control logic. Detection of this transition causes the Speed Sequence Control to generate two pulses which are synchronous with the clock signal specified by the Speed Control Programming logic. These pulses determine the sequence of the time comparison.

The desired value of disk speed is programmed by the Disk Speed Count Programming array. The program value fed to the Speed Control Counter is determined by the array and the state of the Purge Cycle Flip-Flop (LPCFF), thereby providing a nominal speed for normal operation and an over-speed value for use during the purge cycle. The programmed value of the disk speed count is fed to the Speed Control Counter logic and the selected clock signal from the Speed Control Programming logic is then counted by the Speed Control Counter. The results of the count are stored in the Speed Value Flip-Flops and, when appropriate, transferred to the Speed Status Flip-Flops as determined by the Speed Sequence Control logic. The actual comparison of the spindle speed to the reference signal occurs on the basis of the count totalized in the Speed Control Counter logic during the time interval defined between transitions of the Phase Lock Flip-Flop.

There are two outputs derived from the Speed Status Flip-Flops; the Increase Motor Speed (NLIMS1) signal and the Speed Out Of Tolerance (LSOTF) signal. The Speed Out Of Tolerance signal indicates when the disk speed is detected as being out of tolerance by the Speed Value Flip-Flops. This information is tested during the start sequence and is also combined in a Gate with the Ready signal (LRXXG) to produce Disk Speed Error (NLSDEG). The Increase Motor Speed signal is fed to the Servo PCBA and is the basic binary error signal derived from the comparison of the time reference to the actual speed. The Start Drive Motor pulse (NLSDMG) is used for intializing the speed status flip-flops during a start sequence and the Drive Motor Enable (LDMEG) line is used for initializing the Speed Sequence Control and the Speed Status Flip-Flops.

It can be seen that the purpose of the circuitry on the Logic PCBA is to convert the analog signal obtained from the Magnetic Transducer into a suitable digital square wave, then compare the time of occurrence of the positive transitions of that square wave with a time reference obtained from a Crystal Oscillator. The result of that comparison is two signals, one indicating the instantaneous speed error signal and, if appropriate, to provide a signal

*Foldout drawing, see end of this section.

which would indicate a gross malfunction of the speed control. The Increase Motor Speed (NLIMS1) obtained from the Speed Status Flip-Flops is fed to the Servo PCBA.

A portion of the Spindle Speed control circuitry is located on the Servo PCBA. Basically, there are two functions performed by this circuitry; the generation of a signal to the Motor Control PCBA which is synchronized to the line frequency and causes the trigger to occur at a specific time during the power line cycle.

Generation of a signal which is synchronized to the line frequency is necessary because the basic power line is the power applied to the drive motor by the Motor Control PCBA. This line synchronization is accomplished by a Zero Crossing type of synchronizing network in which a pulse is developed by the Line Synchronizer when the line voltage passes through the zero volt condition.

The trigger to the Motor Control PCBA must be supplied at a specific time during the power line cycle. The time of occurrence of this trigger must be proportional to the integral of the binary error signal. This is done to provide a proportional power control to the drive motor main winding that is the time average of the binary error signal (NLIMS1).

Phase angle control is obtained by the use of a Ramp Generator which is synchronized to the line voltage by the line synchronizer. The output of the integrator is compared with the voltage developed by the Ramp Generator in a Voltage Comparator. The results of this comparison are used to generate a trigger signal which is fed to the Motor Control PCBA.

The Motor Control PCBA is, in essence, a bi-directional power switch isolated from the normal machine ground. The switch is turned on by the trigger signal from the Servo PCBA and then turns itself off as the line current passes through zero. Also contained on the Motor Control PCBA is the necessary interconnection wiring for configuring the drive motor for the two basic types of power line operation, 110v and 220v (refer to Paragraph 4.8).

The trigger signal obtained from the Servo PCBA is applied to Current Amplifier Transistor Switches via an Opto-Isolator device. The Current Amplifier Transistor Switches apply gate current to the Triac Switch which selects the power line onto the main winding of the drive motor. During normal speed control, when power is to be applied to the drive motor, the specific time for switching in the power is determined by the voltage comparator on the Servo PCBA. The Triac Switch allows current to pass through the drive motor winding for that portion of the line cycle. Since the power line voltage has both a positive and a negative excursion in a given cycle, power may be applied twice during a cycle. The phase angle of that power application can be determined and controlled by the comparison of the Ramp Generator with the integrated increase motor speed signal.

The control circuitry contained on the Servo PCBA is enabled by the Not Drive Motor Enable (NLDMEG) signal. Thus, when it is desired to have no power applied to the drive motor (e.g., when the machine is stopped) the circuitry is correspondingly commanded by the state on the drive motor enable line. When it is desired to stop the disk from rotating and bring it to a halt, it is necessary to develop a braking torque to slow the disk down to the stop condition in a reasonable amount of time. This is necessary because the rotating assemblies have a considerable inertia and the time for the spindle to coast down to a stop without an additional braking force would be excessive. In order to develop this braking torque, the drive motor is operated in a special mode during that portion of the stop cycle. This is referred to as a brake cycle and is defined by the Brake Cycle Enable (NLBCEG) signal derived from the Start/Stop Control Logic on the Logic PCBA. When the Brake

Cycle Enable signal is asserted, the Servo PCBA circuitry is caused to operate in a slightly different mode wherein full power is applied to the drive motor main winding but only for one-half of a line cycle. This develops a magnetic field in the drive motor which results in a braking torque rather than in a running or starting torque. It is this torque which is used to slow the spindle to a stop.

4.7.4 POSITION CONTROL LOGIC

Figure 4-11* is a functional block diagram of the Position Control logic and should be referred to in conjunction with the following discussion.

The major function of the Position Control logic is to accept address commands from the I/O interface and cause the positioner to move to the address demanded by the interface. This involves generating suitable signals to control the mode of operation of the positioner servo and to control the velocity that is used by the positioner servo. Additionally, certain signals are generated which are supplied to the interface for purposes of indicating the Position Control Logic status. Error checking of the Position Control Logic functions are also accomplished by this logic.

The major inputs from the I/O interface are the Cylinder Demand Address (ICDNR) lines, the Cylinder Address Strobe (ICASR), and the Restore Initial Cylinder (IRICR) lines. Inputs to the Position Control logic from the Servo PCBA are: Position Reference Clock (SPRCG), Position Quadrature Clock (SPQCG), Position Transducer Index (SPTIG), Heads Retracted (SHRXG). The signals from the Servo PCBA are derived from the position transducer. Additionally, the Load Head signal (LLHFF) is provided as an input to the Position Control logic from the Start/Stop logic and is used in the Mode Control logic.

Major output signals from the Position Control logic to the Servo PCBA are the Address Difference (NLADNG), Forward Direction (LFDX1), Velocity Reference Enable (NLVREG), Position Mode (LPMXG), Forward Slow Mode (NLFSM1), and Reverse Slow Mode (NLRSM1). The major output signals which determine interface outputs are the Illegal Address (NLIAXG) and the Busy (NLBSXG) signal. The auxiliary output suppied to the Read/Write PCBA from the Position Control logic is Demand Address Most Significant (LDAMG). In 200 tpi models an auxiliary output consisting of the three most significant bits from the current address counter are supplied to the Temperature Compensation PCBA.

A Cylinder Demand Address from the I/O interface specifies the address that is required by the controller. If the address is accepted by the Position Control logic, it is stored in the Demand Address Register. Loading of this register is under control of the Load Address and Illegal Address Control logic. The validity of a demand address on the I/O interface lines is tested by the Valid Address Decoders, one decoder for 100 tpi addresses, and another decoder for 200 tpi addresses. Only one decoder is connected, depending upon the specific configuration of the machine.

The inspection and test of the address is made only when accompanied by a Cylinder Address Strobe (ICASR) from the I/O interface. In addition, the state of Restore Initial Cylinder (IRICR) line is examined at the time of a Cylinder Address Strobe and the state of that line determines if the address is to be accepted or ignored, and if a restore operation is to be performed. When the Restore Initial Cylinder line is asserted at the time of a Cylinder Address Strobe, the Demand Address lines are ignored and the Position Control logic commences a Restore operation. A Restore operation initializes the Position Control logic and returns the positioner to cylinder 000. If a Restore is not asserted at the time of a

*Foldout drawing, see end of this section.

Cylinder Address Strobe then the Demand Address lines are examined to determine if they contain a valid address. If a valid address is present, this address is accepted by the Position Control logic. If the address is an illegal address, i.e., it lies outside the range of the valid addresses, then this is signalled by the Illegal Address (NLIAXG) line.

During a strobe, and any time during a Seek operation, the Position Control logic and the positioner status are indicated on the Busy Signal (NLBSXG) line. Illegal Address and Busy Signal are outputs of the Load Address and Illegal Address Control and the Busy logic.

Information describing the current position of the positioner is stored in the Current Address Counter which is an up/down type of counter. The direction of the count and the amount of the count are determined by the Count Control logic on the basis of the Position Reference Clock (SPRCG) and Position Quadrature Clock (SPQCG) signals from the Servo PCBA. These are the digital position transducer signals derived from the outputs of the position transducer.

The positioning system in the D3000 Disk Drive functions on the basis that the physical position of the positioner is known to the Position Control Logic at all times. This is because the logic has kept track of all moves made by the positioner since initialization, i.e., current position information is initialized at the time the heads are loaded. In other words, the system knows where it is because it was told where it started from and it kept track of every move thereafter. Furthermore, it knows how far it has to go to achieve the demand address because it knows where its current location is. The particular mode of operation of the Position Control logic is determined by the Mode Control portion of the logic in conjunction with the Operation Control logic. The various inputs and outputs of this portion of the Position Control logic can be seen in the block diagram (Figure 4-11).

There are four modes of operation of the Position Control logic. One mode is the Position Mode which causes the positioner servo to operate as a position type servo and hold a particular cylinder position.

During a Seek operation it is necessary to operate the positioner servo as a velocity type of servo. This, of course, is a negation of the Position Mode line. In addition to the velocity reference enabled by the Velocity Reference Enable (NLVREG) line, the direction of the velocity is specified by the Forward Direction (LFDX1) line, and the particular velocity reference level is determined on the basis of the amount of difference between the current address and the demand address. This difference is specified to the Velocity Function Generator on the Servo PCBA by the Address Difference lines. It is important to note that the difference between the current address and the demand address is obtained by performing a ones-complement arithmetic subtraction on the binary values contained in Current Address Counter and the Demand Address Register. This subtraction process is performed by the Subtractor and Complementor logic. Since the arithmetic is ones-complement arithmetic, an end-around carry is used. This carry is under control of the Carry Control logic and the algebraic sign of the velocity desired is determined on the basis of the binary value of the carry. The actual subtraction is mechanized using an integrated circuit binary full-adder. When the heads are being loaded, it is necessary to force the carry to a particular state; this is accomplisched by the Carry Control logic on the basis of the states of certain bits in the Current Address Counter.

The other two modes of operation of the Position Control logic are the Forward Slow Mode and the Reverse Slow Mode. The two slow modes are a slow velocity type of operation. The Forward Slow Mode is used during loading of the heads and the latter portion of a

Restore operation. The Reverse Slow Mode is used for unloading the heads and for performing the first portion of a Restore operation. When operating in the Slow Velocity Mode, the velocity reference developed from the Address Difference lines is not used and therefore Velocity Reference Enable (NLVREG) is not activated.

The Error Check Logic performs two types of checks concerned with operation of the positioner. The first check determines if the positioner has completed a seek within the maximum allowable time. This check is done by the Seek Time Error (NLSTEG) check circuitry and is a gross type of check to determine simply that the positioner has not become stalled due to a fault. Although each seek is checked by this circuit, it does not verify that the time for the specific distance moved was compatible with the specific time associated with that length of seek. Rather, it determines that the positioner has not become stalled while attempting a seek.

The other error check performed is to determine that the positioner has not travelled outside of the legal range of travel. This is performed by the position limit monitor circuitry which generates a Position Limit Error (NLPLEG) signal if the positioner exceeds the normal range of travel. This check is performed only during the time that the heads are loaded onto the disk.

4.7.5 SECTOR ELECTRONICS

Figure 4-12* is a functional block diagram of the Sector Electronics logic and should be referred to for the following discussion.

The major function of the Sector Electronics logic is to provide Sector pulses at the I/O interface which electrically subdivide the disk storage surface into a number of sectors for the purpose of addressing data stored on the disk. Additionally, the specific number of the sector passing under the Read/Write heads is transmitted to the I/O interface on the Sector Count lines. These lines specify the sector count presented in a binary format. The count indicates the particular segment of the disk surface currently under the Read/Write heads.

In addition to the Sector Pulse and Sector Count, the Index Pulse is provided as an output of the Sector Electronics. This line provides a signal which is a pulse occurring once per revolution of the disk and may be utilized to define the sector reference, i.e., sector zero.

Referring to Figure 4-12, it can be seen that the inputs to the Sector Electronics logic are a signal from the Upper Sector/Index Sensor, a signal from the Lower Phase/Index Sensor, Clock Signals obtained from the clock countdown portion of the Start/Stop Control logic and the Drive Motor Enable (LDMEG) signal also obtained from the Start/Stop Control logic.

The removable cartridge may be sectored either electronically or mechanically while the lower (fixed) platter in dual disk machines is sectored electronically.

Electronic sectoring can be in one of two configurations since the removable cartridge may be one of two configurations, i.e., an index notch only, or with sector slots and an index slot. The associated types of electronic sectoring are provided from an index-only type of cartridge and from a sector-plus-index-slot type of cartridge.

The normal top-loading cartridge has one slot in the armature plate which is referred to as the index notch. This is the standard top-loading cartridge arrangement. Some specially modified top-loading cartridges have additional notches used for mechanical sectoring purposes.

*Foldout drawing, see end of this section.

The normal front-loading cartridge has sector slots for the purpose of sectoring and a single index slot in the sector ring for purposes of mechanical sectoring. Special front-load cartridges may be designed with only an index slot.

Referring to Figure 4-12, the Upper Sector/Index Sensor is a photoelectric type of sensor for front load models and a magnetic transducer for top load models. The Lower Phase/Index Sensor is a magnetic transducer on all D3000 models. This magnetic transducer senses the notches in the Phase Lock Ring mounted on the spindle. The Phase Lock Ring is used for electronic sectoring and for speed control of the spindle. The slots or notches in the removable cartridge are sensed by the appropriate sensor type and the signal is fed to the Upper Sensor Detector which converts the analog signal from the sensor to a digital pulse train. The pulse train, however, contains either all the pulses for the sector slots, or notches, and in addition a pulse for the index slot or notch, or in the case of index-only cartridges just a single pulse for the index notch.

In the event that pulses for the sector slots or notches and the index slot or notch is present, these will be separated by the Upper Time Demultiplexer. The pulse representing the index will be output on one line from the Upper Time Demultiplexer and the sector pulses will be output on another line. Therefore, it can be said that the Upper Time Demultiplexer functions to separate the index pulse from the sector pulse. It is important to note that these pulses are pulses representative of sensing of the slot and are not the signals fed to the interface. The specific gate time required by the Upper Time Demultiplexer is programmed by a Programming Array, and the basic time reference used is obtained from a clock signal generated in the Clock Countdown portion of the Start/Stop Control logic.

In the case when an index-only cartridge is being used, a single pulse per revolution is applied to the input of the Upper Time Demultiplexer. The output of the Upper Time Demultiplexer will be a single pulse on the same line that was used for outputting the demultiplexed sector information in the previously mentioned case.

The Lower Sensor Detector is a circuit similar to the Upper Sensor Detector except that it has a variable threshold. The circuit converts the analog signal from the Phase Lock Ring magnetic transducer to a digital signal which is applied to the Lower Time Demultiplexer. The purpose of the Threshold Control for the Lower Sensor Detector is to provide a means for changing the sensitivity of the Lower Sensor Detector. When executing a stop sequence, or when the disk drive is in the Safe condition, it is desirable to be able to detect any rotation of the spindle; this is accomplished by causing the Lower Sensor Detector to operate in a high sensitivity mode via the Threshold Control logic. This high sensitivity threshold is enabled when Drive Motor Enable (LDMEG) is not asserted. When Drive Motor Enable is asserted, the threshold is changed to a threshold similar to that used in the Upper Sensor Detector. Drive Motor Enable is asserted whenever the disk drive is in the Run condition.

The Lower Time Demultiplexer functions in a manner similar to the Upper Time Demultiplexer except that the Phase Lock Ring always has a single index notch per revolution which is interposed between the phase lock notches. The Lower Time Demultiplexer will output the Index pulse on one line and all the other phase lock notch pulses on the other line. Thus, the Lower Time Demultiplexer separates the pulses obtained from the phase-lock notches from the single index notch. The value of the gate time required by the Lower Time Demultiplexer is programmed by the Programming Array. The time reference for the Lower Time Demultiplexer is obtained from a clock signal generated by the Clock Countdown circuitry in the Start/Stop Control logic.

The specific sectoring configuration is selected by the connections of the Sectoring Selection Programming Array shown as two blocks in Figure 4-12. The raw pulses output from this interconnection array are unsuitable for application to the I/O interface directly and must be formed into suitable pulses by the Upper Sector Pulse Former, the Lower Sector Pulse Former, the Upper Index Pulse Former, and the Lower Index Pulse Former. Each of these pulse former circuits takes the raw input pulse and converts it into a pulse having a time duration that is suitable for transmitting over the I/O interface. The outputs of the Upper Sector Pulse Former and Lower Sector Pulse Former are multiplexed onto the single Sector Pulse (ISPXD) line by the Sector Pulse Multiplexer according to the particular platter selected by the I/O interface.

Likewise, the outputs of the Upper Index Pulse Former and Lower Index Pulse Former are multiplexed by the Index Pulse Multiplexer and fed to the single Index Pulse (IIPXD) line according to the particular platter selected by the interface. The Multiplexer Control Logic controls the pulse multiplexers according to the state on the Upper Platter Select (LUPSG), the Not-Upper Platter Select (NLUPSG), and the Selected and Ready (NLSARG) line.

Additionally, the raw pulses obtained from the Sectoring Selection Programming Array are applied to the sector number counters for purposes of generating the sector count. The Upper Sector Number Counter and Upper Count Control are used to generate the sector number count for the upper platter. The Lower Sector Number Counter and Lower Count Control are used to generate the sector number count for the lower platter. A particaular sector count is multiplexed by the Sector Count Multiplexer logic according to the control signals generated by the Multiplexer Control logic. These control signals, generated by the Multiplexer Control logic, are a function of the specific platter selected and the Selected and Ready condition. The count control for each sector number counter determines when the counter will be returned to a zero count. This is determined automatically as a result of the count control action obtained from the raw index pulse occurrence.

Electronic pulses are generated by the disk drive as selected by the Sectoring Selection Programming Array when the removable cartridge has index only, or when it is desired to electronically sector a multi-notch removable cartridge. Additionally, the Sectoring Selection Programming Array causes the disk drive to generate pulses for sectoring the lower disk which is sectored electronically regardless of the configuration. These pulses are generated by counting down with an electronic counter the output of a high-frequency oscillator. Because the sector pulses must be synchronous with the instantaneous speed of rotation of the spindle, it is necessary to phase lock this high-frequency oscillator to the spindle.

Those particular functions are implemented by the Sector Phase Lock Loop through the Upper and Lower Sector Countdown Counters. Associated with these counters are Electronic Sector Programming Arrays used to determine a particular number of sectors and a synchronizer for each counter to synchronize the count with the Index pulse obtained from their respective Time Demultiplexer. The output derived from the phase lock ring notches are fed via the Lower Time Demultiplexer to a Phase Lock Flip-Flop which divides the frequency of that pulse train by a factor of 2, and converts it into a square wave. This square wave is used not only by the Sector Phase Lock Loop but is one of the outputs of the Phase Lock Flip-Flop fed to the Spindle Speed Control electronics.

The Voltage Controlled Oscillator (VCO) within the Sector Phase Lock Loop is electronically servoed to the square wave obtained from the Phase Lock Flip-Flop. This is

accomplished by taking the output of the VCO and counting it down with the Sector PLL Countdown Counter. The specific countdown value is programmed by the Countdown Programming Array and the output of the counter is converted to a square wave by the Sector Countdown Divider Flip-Flop. The outputs of the Sector Countdown Divider Flip-Flop are compared with the Phase Lock Flip-Flop output by the Phase Comparator. The output of the Phase Comparator is suitably filtered and applied to a Sum-And-Difference Amplifier which generates the control voltage for servoing the frequency of the VCO. This causes the output of the VCO to become phase-locked to the phase lock pulses obtained from the phase-locked ring.

The output of the VCO may be taken directly or the frequency may be divided by a factor of 2 by the VCO Divider Flip-Flop and applied to the Sectoring Selection Programming Array for purposes of selecting the specific electronic sectoring configuration. This high-frequency oscillator signal is then frequency divided by the Sector Countdown Counter for the particular platter. The exact value of a count used for the division is determined by the respective Electronic Sector Programming Array. The count is synchronized to a specific platter by the associated synchronizer in conjunction with the index pulse derived for use with that particular platter. The pulse train output from the particular sector countdown counter has a repetition rate corresponding to the number of desired sectors as programmed by the respective Electronics Sector Programming Array. This pulse train is synchronized with the respective index pulse.

When electronic sectoring is selected by the Sectoring Selection Programming Array, this pulse train is fed directly to the respective pulse former.

4.8 MOTOR CONTROL

A functional element of disk rotational speed control is provided by the Motor Control circuitry. The current switching necessary to control drive current for the drive motor is provided by this subsystem. Additionally, provisions are made to accommodate drive motor operation at different line voltages in this subsystem.

The disk drive motor is a permanent split-phase induction motor with multiple windings to accommodate the two classes of line voltage operation. A permanent split induction motor requires the use of a capacitor or other type of phase shifting arrangement connected in series with the start winding (or windings). This is done to provide a current in that winding, phase shifted with respect to the main winding, such that the net magnetic field produced by the windings is a pseudo rotating magnetic field. In the D3000 Disk Drive, motor capacitors mounted on the power supply chassis are connected to provide the phase shift of current in the start windings with respect to the main winding.

For 110v operation, main winding number 1 is connected in parallel with main winding number 2 and is operated directly from the line voltage. Current through the winding is switched on and off by a triac on the Motor Control PCBA. For 220v operation, main winding number 1 is connected in series with main winding number 2 and the series combination of these windings is operated directly from the line voltage. The current is switched on and off by the triac on the Motor Control PCBA. The motor capacitors are parallel-connected for 110v operation and series-connected for 220v operation.

Therefore, the effective arrangement for 110v operation is that the parallel combination of the motor capacitors is connected in series with the parallel combination of start winding number 1 and start winding number 2. This parallel series network is operated directly from the line voltage and is not switched by the triac. For 220v operation, the series

combination of the motor capacitors is connected to the series combination of start winding number 1 and start winding number 2 and this series network is operated directly from the line voltage and is not switched by the triac. Thus, it can be seen that current flows in the start winding at all times when power is applied via the ON/OFF switch on the operator panel.

Torque will not be developed by the motor to an extent which will allow starting rotation of the disks unless the main winding is energized for a sufficient amount of time to provide the net rotating magnetic field. Likewise, sufficient torque to maintain rotation will be available only if the main winding is energized sufficiently often that the available field from a combination of the main and the start winding can provide the necessary torque to the load. Torque available from the drive motor is therefore provided by switching on and off the current in the main winding. The ability to control the speed of the drive motor and the torque that it supplies to the load is therefore contingent upon switching the triac on the Motor Control PCBA at the correct times and allowing current to flow in the main winding as required.

The current amplification necessary to provide the high current drive for the gate of the triac is provided by transistor current switches on the Motor Control PCBA.

Since the main winding of the drive motor is an inductive load, there can exist a phase shift between the current through the motor and the applied voltage. This means that at the time the triac current falls below the holding current value and the triac ceases to conduct, there will exist a certain voltage across the triac. If this voltage appears too rapidly, the triac will resume conduction and control will be lost. In order to achieve control with certain inductive loads, such as the drive motor, the rate of rise in voltage must be limited by a series R-C network across the triac. The capacitor limits the rate of change of voltage across the triac with respect to time; the resistor limits the surge of current from the capacitor discharging when the triac first conducts. It is also used to damp the ringing of the capacitance with the drive motor inductance and the inductance of a series inductor mounted on the Motor Control PCBA. This additional inductor is required to reduce transients caused by the triac switching into conduction.

4.9 POWER SUPPLY

Figure 4-13 is a block diagram of the disk power supply which is in two parts. The first part, the power supply module mounted on the power supply chassis, is fastened to the base casting and contains the power transformer, rectifiers, capacitors, fuses, and power resistors. Three unregulated dc supplies are generated at nominal voltages of ±20v and ±10v dc. Three ac supplies are generated at nominal voltages of ac line voltage, 8v ac (rms) and 21v ac (peak).

The second part of the power supply consists of the ±10v and ±5v voltage regulators which are located on the Servo PCBA. Interconnection between the two parts is provided by a harness from the power supply chassis which plugs into the Servo PCBA via a 12-pin connector. Interconnection for ac line voltage, ac common, and 8v ac (rms) to the Motor Control PCBA is provided via a 6-pin connector.

The transformer primary connections are shown in Figure 4-14 for several line voltages. Line voltage is connected to the transformer via the ON/OFF switch. The ac line voltage is also used directly to power the disk drive motor. Also, 8v ac (rms) and 21v ac (peak) are used for drive motor speed control circuits and to power the brush motor and associated circuits. Unregulated dc (at a nominal of +20v under load) is used to provide power to the

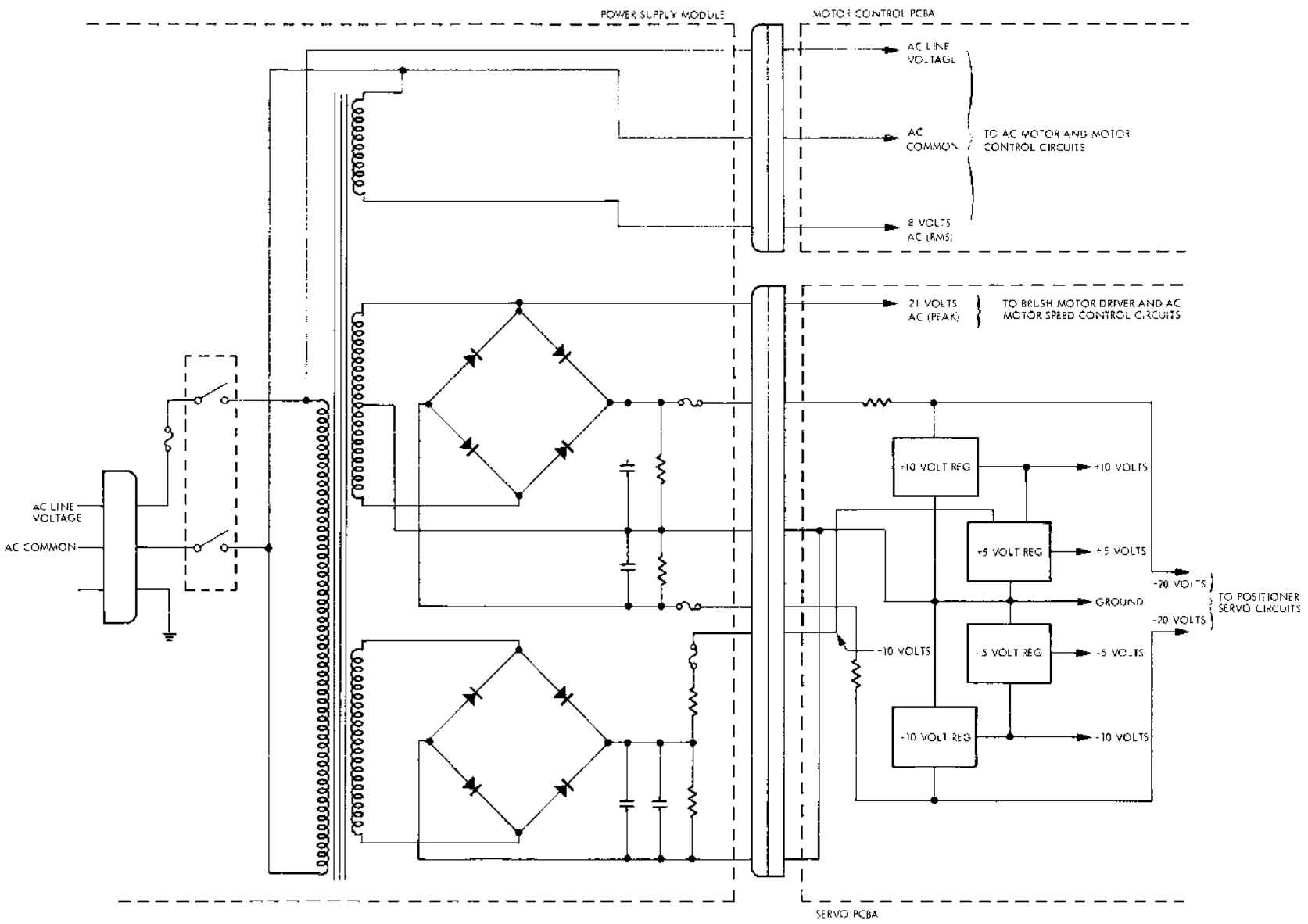
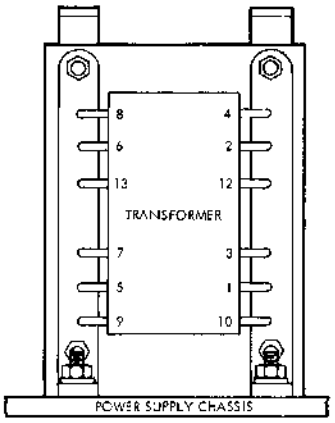


Figure 4-13. Power Supply Functional Block Diagram



LINE VOLTAGE	LINE BETWEEN	CONNECT
95	13 AND 3	12 TO 13 AND 3 TO 7
100	6 AND 3	2 TO 6 AND 3 TO 7
110	5 AND 3	1 TO 5 AND 3 TO 7
115	6 AND 4	2 TO 6 AND 4 TO 8
125	5 AND 4	1 TO 5 AND 4 TO 8
190	13 AND 3	12 TO 7
200	6 AND 3	2 TO 7
210	6 AND 3	1 TO 7
215	6 AND 4	2 TO 7
220	5 AND 3	1 TO 7
225	5 AND 4	2 TO 7
230	6 AND 4	2 TO 8
235	5 AND 4	1 TO 7
240	6 AND 4	1 TO 8
250	5 AND 4	1 TO 8

NOTE: THIS TABLE APPLIES TO POWER SUPPLY ASSEMBLY NUMBER 102741-01

Figure 4-14. Transformer Primary Connections

positioner, voltage regulators, relay driver, and the solenoid driver. The voltage regulators generate four regulated voltage supplies. The ±10v supplies are zener regulated but not adjustable. The ±5v supplies are adjustable and regulated.

All regulated dc voltages are protected against overvoltage by means of SCR *crowbar* protection circuits. When any of the regulated voltage lines exceed its pre-set overvoltage value, the corresponding SCR fires. This holds the voltage down on the circuits connected to this voltage line until the fuse blows a few milliseconds later. The power resistors, in series with the unregulated ±20v dc and unregulated ±10v dc, limit short circuit currents to a finite value when the SCR fires in the corresponding circuit. The bleeder resistors, provided across capacitors, discharge the capacitors when the power supply input line cord is disconnected.

4.10 TEMPERATURE COMPENSATION (200 TPI)

Figure 4-15* is a functional block diagram of the temperature compensation circuitry and the electrical head compensation used in 200 tpi models. One thermistor is employed to sense the positioner baseplate temperature. The analog signal from this thermistor is amplified and scaled to yield signals which are accurately related to temperature. This signal is then amplified and applied to the servo summing junction on the Servo PCBA and used as warm-up transient compensation.

The positioner baseplate temperature signal is also compared to a temperature reference signal from the system compensation circuitry and the difference applied to a multiplying digital-to-analog converter. The multiplying digital-to-analog converter also accepts as an input from the Logic PCBA the three most significant bits of the current address counter. These signals are then applied to the servo summing junction for compensation of the disk tracks.

Additionally, two signals are provided to the Temperature Compensation PCBA from the System Compensation PCBA. These signals permit fine electrical CE head alignment when the disk drive cover is in place and the drive is rack mounted. The Upper Head Fine Adjust and Lower Head Fine Adjust signals are derived from two potentiometers on the

*Foldout drawing, see end of this section.

System Compensation PCBA. These signals provide for fine tuning the upper and lower heads of the removable platter heads and are fed to the servo summing junction via a multiplexing circuit. This circuit also receives as commands Upper Platter Select (NLUPSG) and Upper Head Select (NLUHSG) signals which permit automatic compensation after the initial CE adjustment.

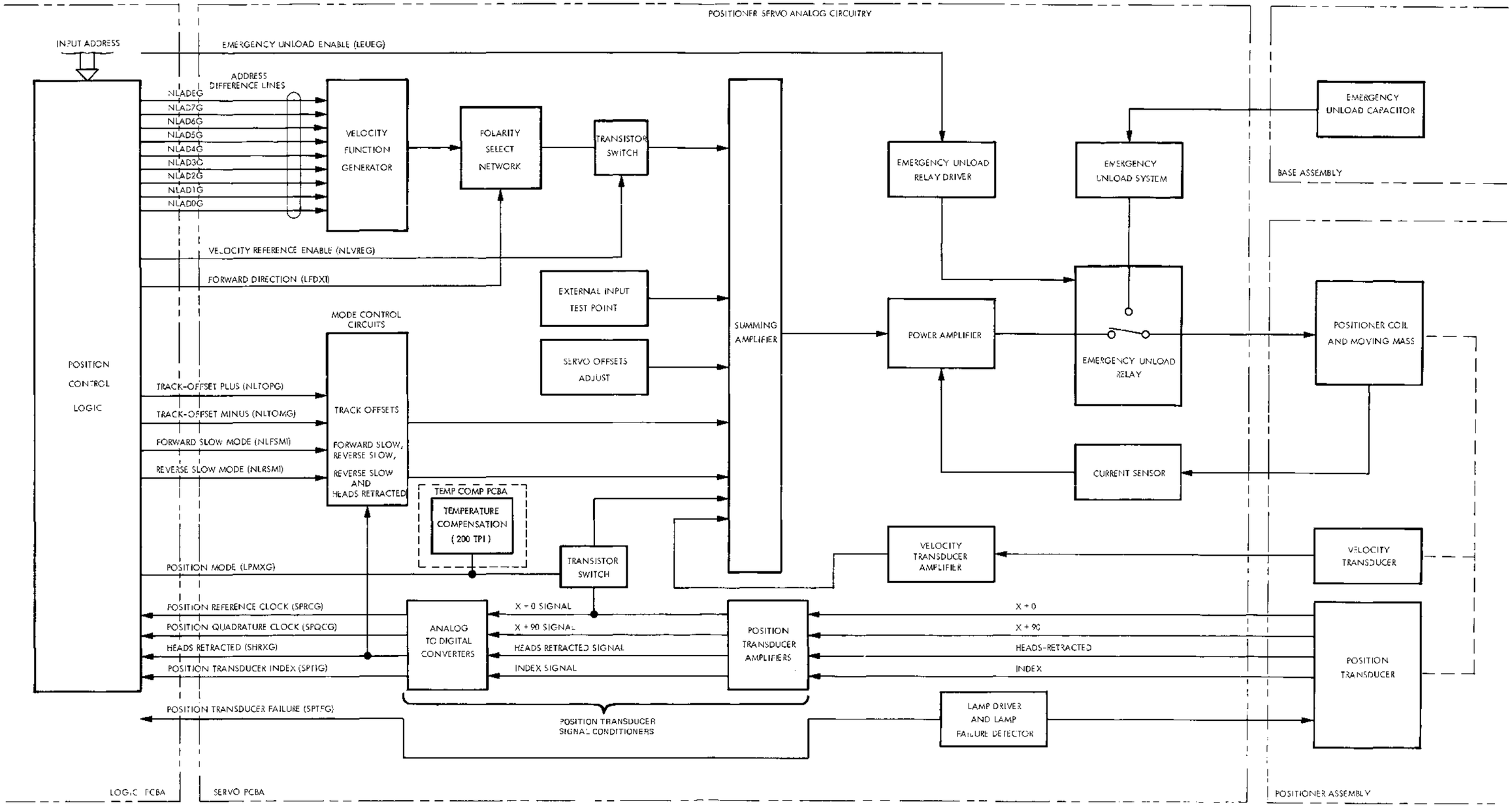


Figure 4-2. Positioner and Positioner Electronics, Functional Block Diagram

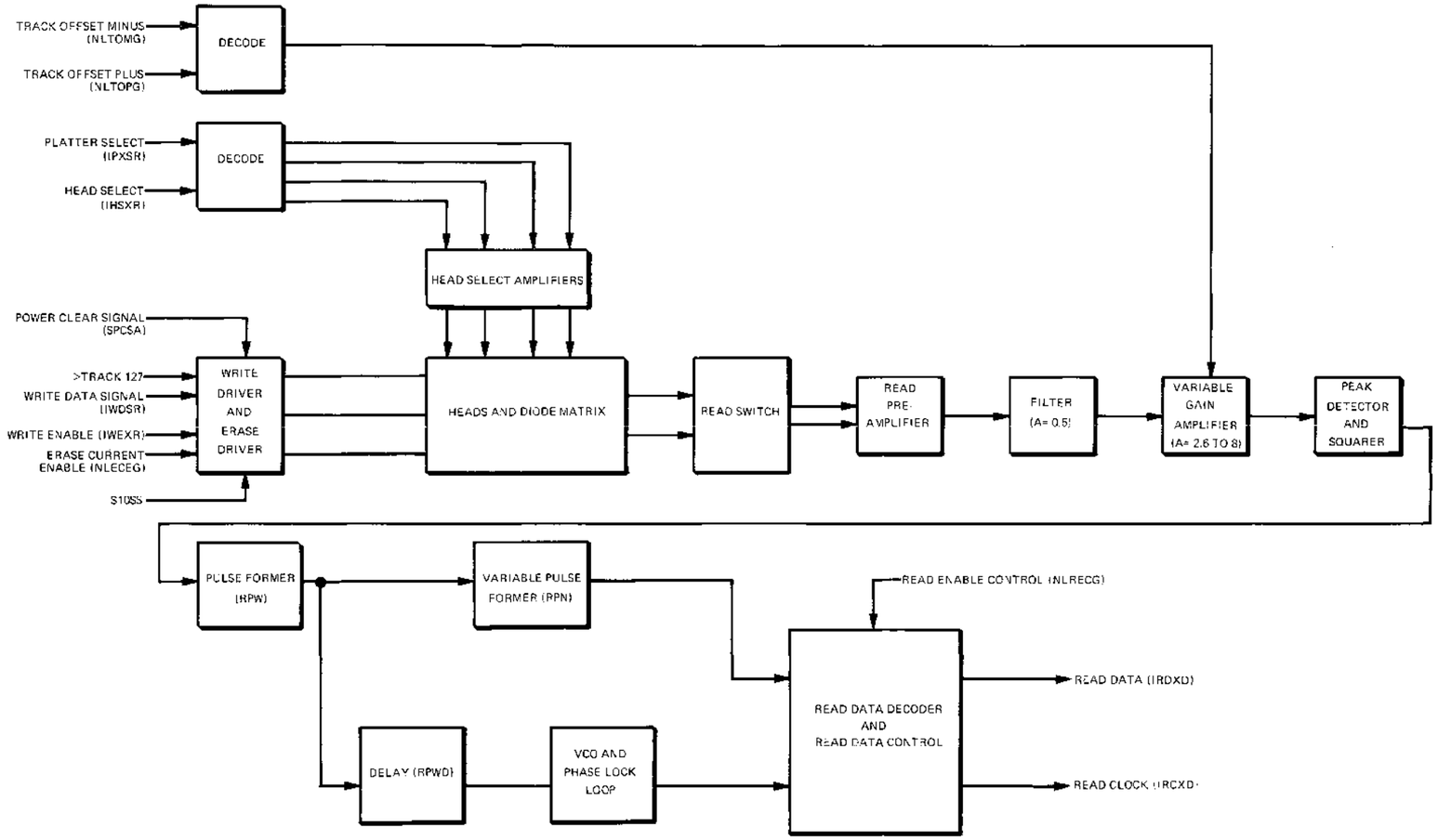


Figure 4-4. Read/Write Electronics, Functional Block Diagram

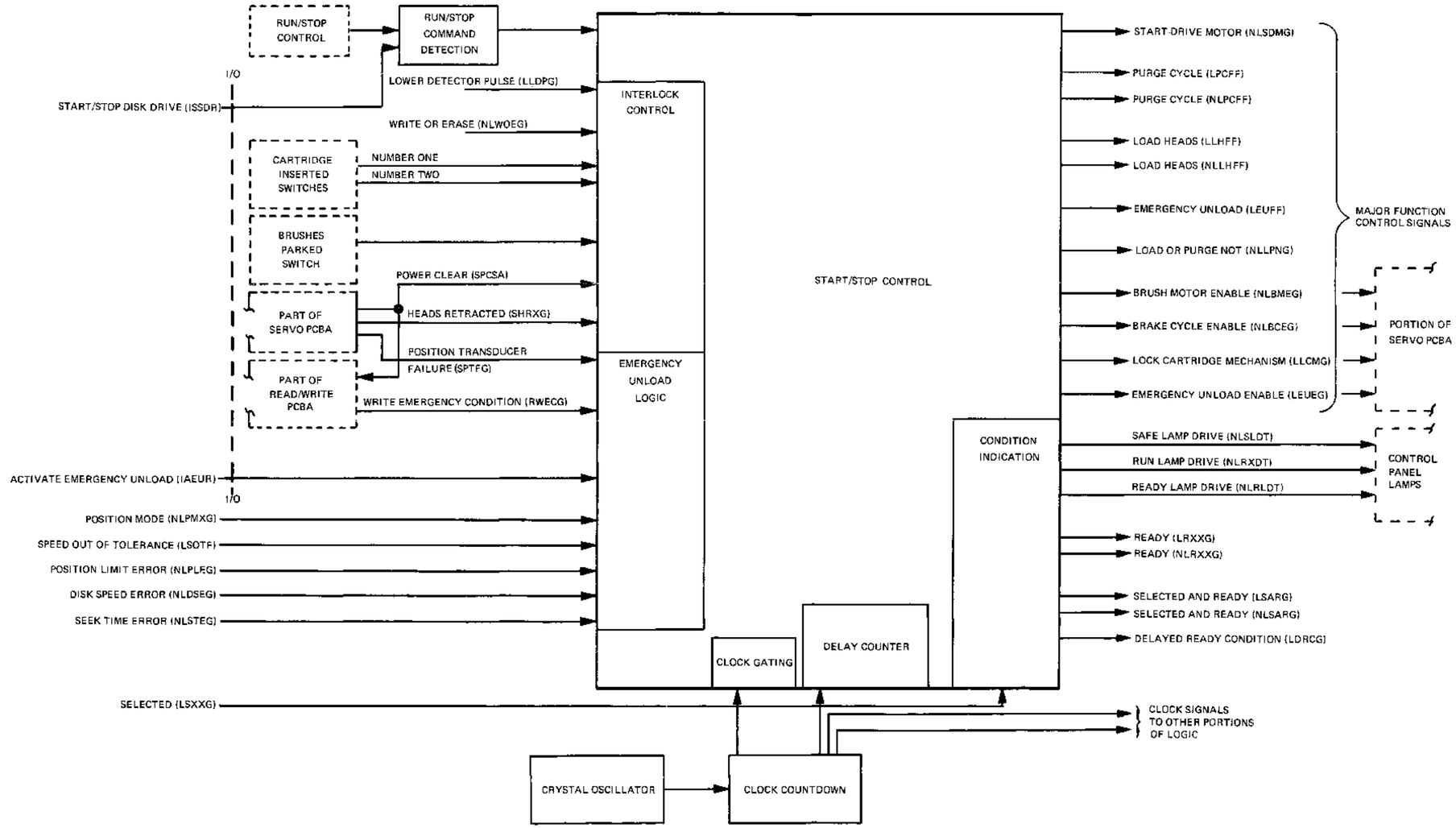
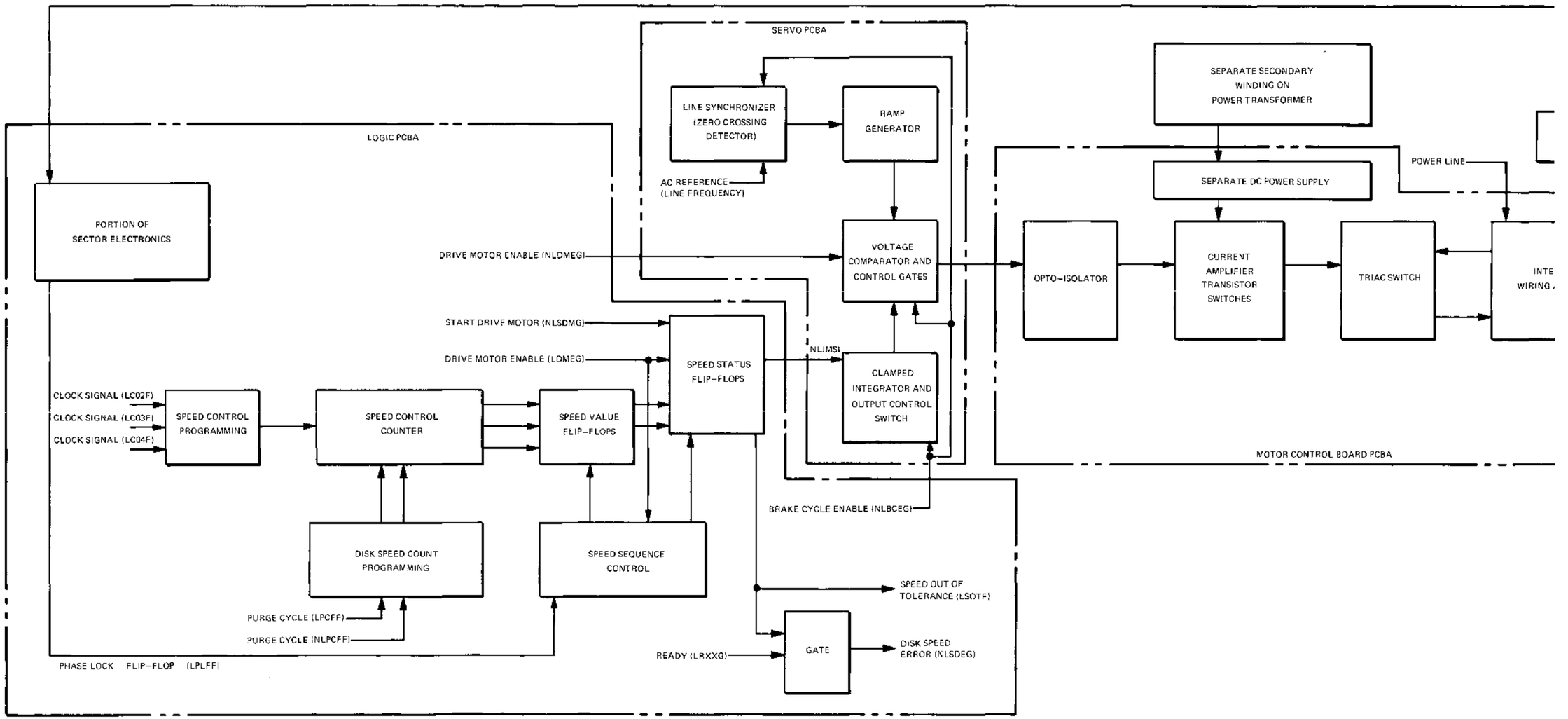


Figure 4-9. Start/Stop Control, Functional Block Diagram


SERVO PCBA
LOGIC PCBA
PORTION OF SECTOR ELECTRONICS
LINE SYNCHRONIZER (ZERO CROSSING DETECTOR)
RAMP GENERATOR
AC REFERENCE (LINE FREQUENCY)
VOLTAGE COMPARATOR AND CONTROL GATES
DRIVE MOTOR ENABLE (NLDMEG)
START DRIVE MOTOR (NLSDMG)
DRIVE MOTOR ENABLE (LDMEG)
SPEED STATUS FLIP-FLOPS
NLIMSI
CLAMPED INTEGRATOR AND OUTPUT CONTROL SWITCH
CLOCK SIGNAL (LC02F)
CLOCK SIGNAL (LC03F)
CLOCK SIGNAL (LC04F)
SPEED CONTROL PROGRAMMING
SPEED CONTROL COUNTER
SPEED VALUE FLIP-FLOPS
DISK SPEED COUNT PROGRAMMING
SPEED SEQUENCE CONTROL
PURGE CYCLE (LPCFF)
PURGE CYCLE (NLPCFF)
PHASE LOCK FLIP-FLOP (LPLFF)
BRAKE CYCLE ENABLE (NLBCEG)
SPEED OUT OF TOLERANCE (LSOTF)
READY (LRXXG)
GATE
DISK SPEED ERROR (NLSDEG)
SEPARATE SECONDARY WINDING ON POWER TRANSFORMER
SEPARATE DC POWER SUPPLY
POWER LINE
OPTO-ISOLATOR
CURRENT AMPLIFIER TRANSISTOR SWITCHES
TRIAC SWITCH
MOTOR CONTROL BOARD PCBA

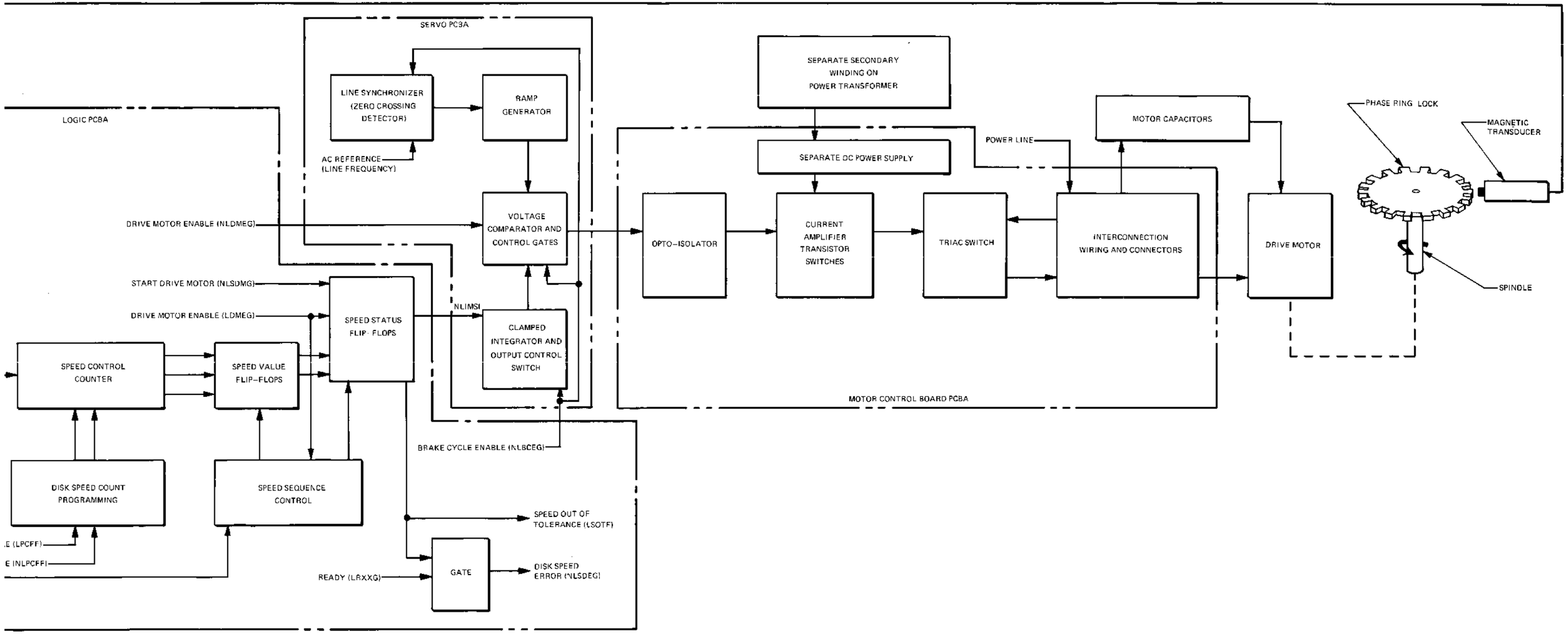


Figure 4-10. Spindle Speed Control, Functional Block Diagram

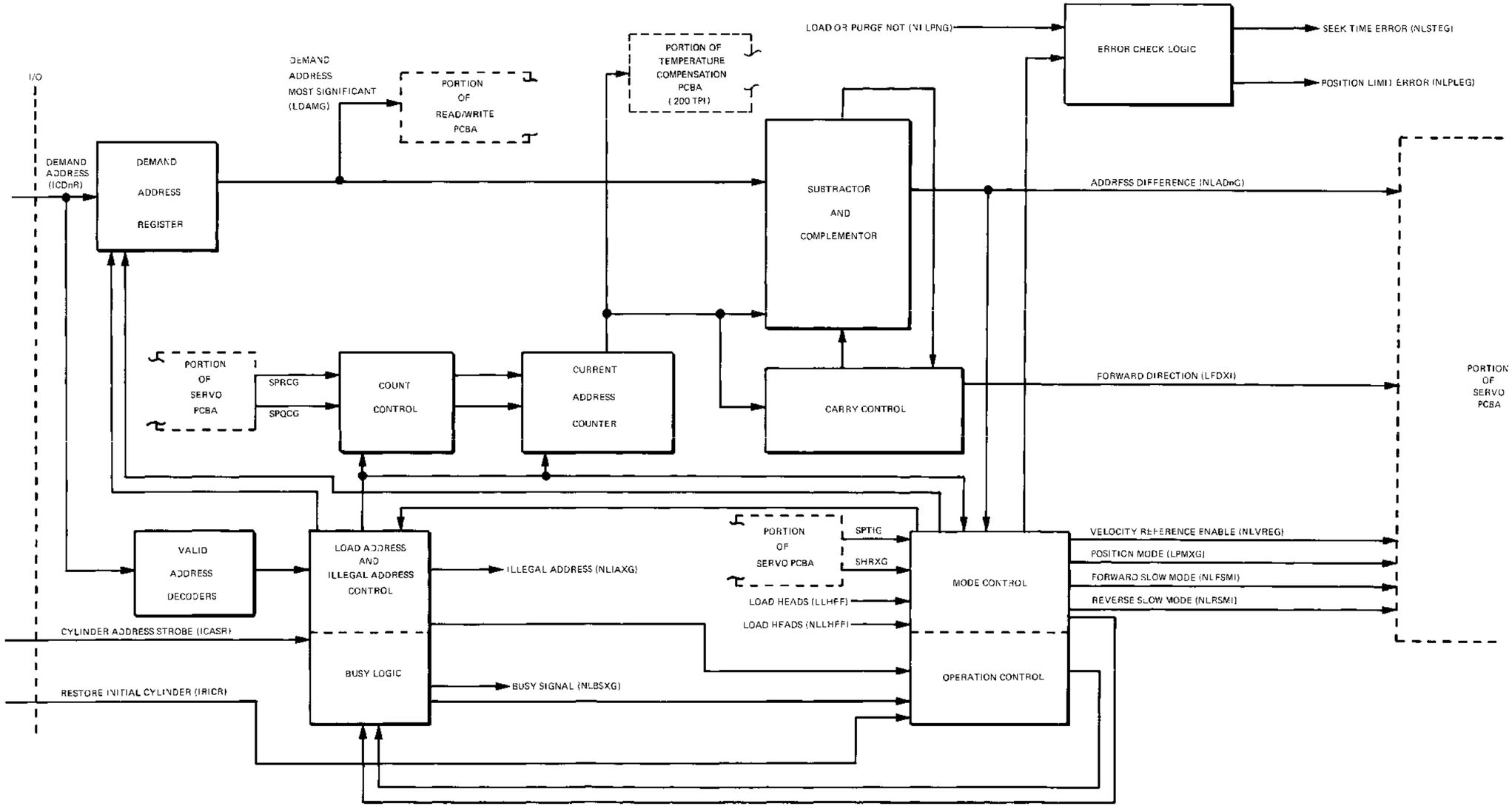
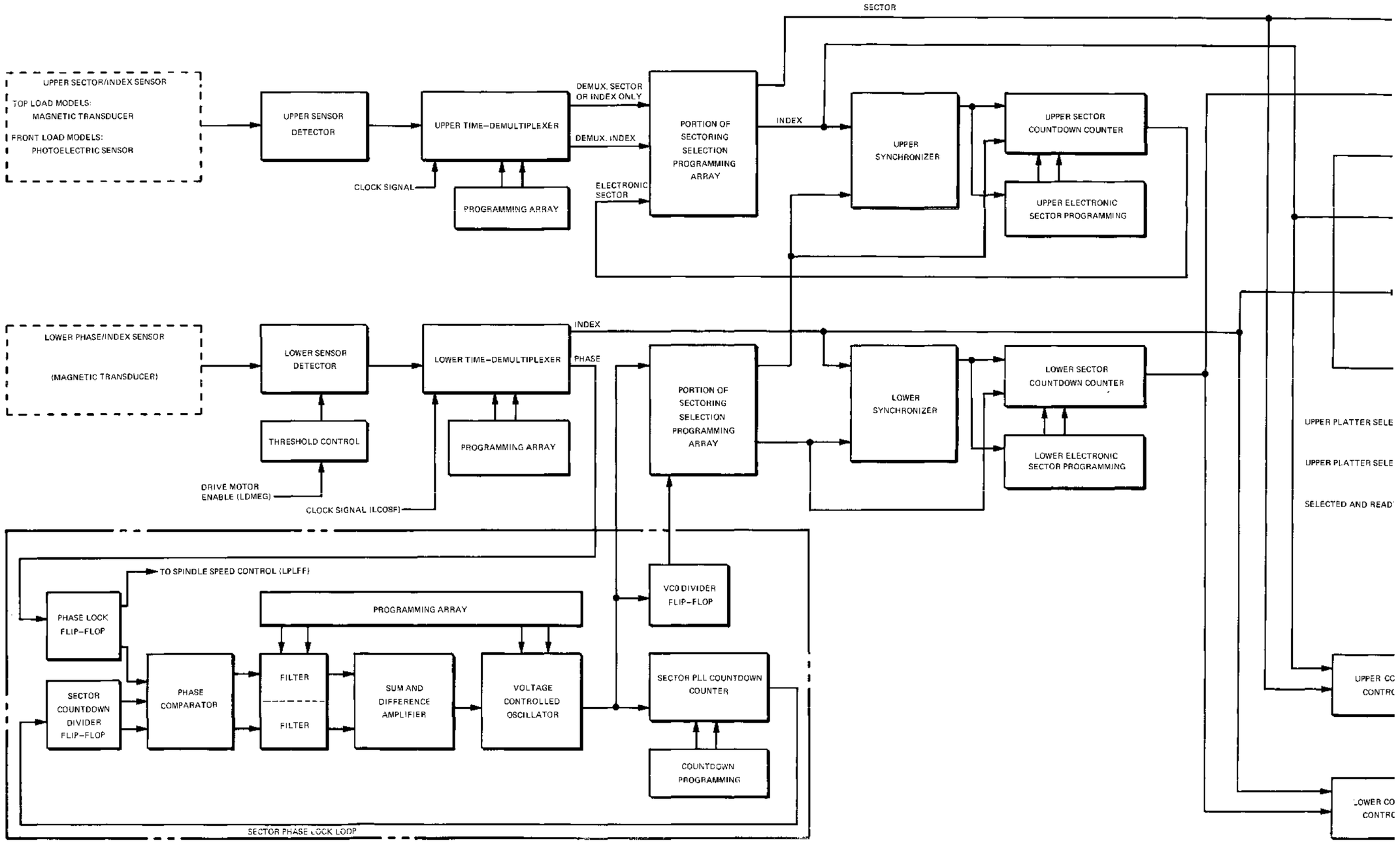


Figure 4-11. Position Control Logic, Functional Block Diagram


UPPER SECTOR/INDEX SENSOR
TOP LOAD MODELS:
MAGNETIC TRANSDUCER
FRONT LOAD MODELS:
PHOTOELECTRIC SENSOR
UPPER SENSOR DETECTOR
UPPER TIME–DEMULTIPLEXER
CLOCK SIGNAL
PROGRAMMING ARRAY
DEMUX. SECTOR OR INDEX ONLY
DEMUX. INDEX
ELECTRONIC SECTOR
PORTION OF SECTORING SELECTION PROGRAMMING ARRAY
SECTOR
INDEX
UPPER SYNCHRONIZER
UPPER SECTOR COUNTDOWN COUNTER
UPPER ELECTRONIC SECTOR PROGRAMMING
LOWER PHASE/INDEX SENSOR
(MAGNETIC TRANSDUCER)
LOWER SENSOR DETECTOR
THRESHOLD CONTROL
DRIVE MOTOR ENABLE (LDMEG)
CLOCK SIGNAL (LCOSF)
LOWER TIME–DEMULTIPLEXER
PROGRAMMING ARRAY
INDEX
PHASE
PORTION OF SECTORING SELECTION PROGRAMMING ARRAY
LOWER SYNCHRONIZER
LOWER SECTOR COUNTDOWN COUNTER
LOWER ELECTRONIC SECTOR PROGRAMMING
UPPER PLATTER SELE
UPPER PLATTER SELE
SELECTED AND READ
UPPER CO CONTRO
LOWER CO CONTRO
TO SPINDLE SPEED CONTROL (LPLFF)
PHASE LOCK FLIP–FLOP
SECTOR COUNTDOWN DIVIDER FLIP–FLOP
PHASE COMPARATOR
PROGRAMMING ARRAY
FILTER
FILTER
SUM AND DIFFERENCE AMPLIFIER
VOLTAGE CONTROLLED OSCILLATOR
VCO DIVIDER FLIP–FLOP
SECTOR PLL COUNTDOWN COUNTER
COUNTDOWN PROGRAMMING
SECTOR PHASE LOCK LOOP

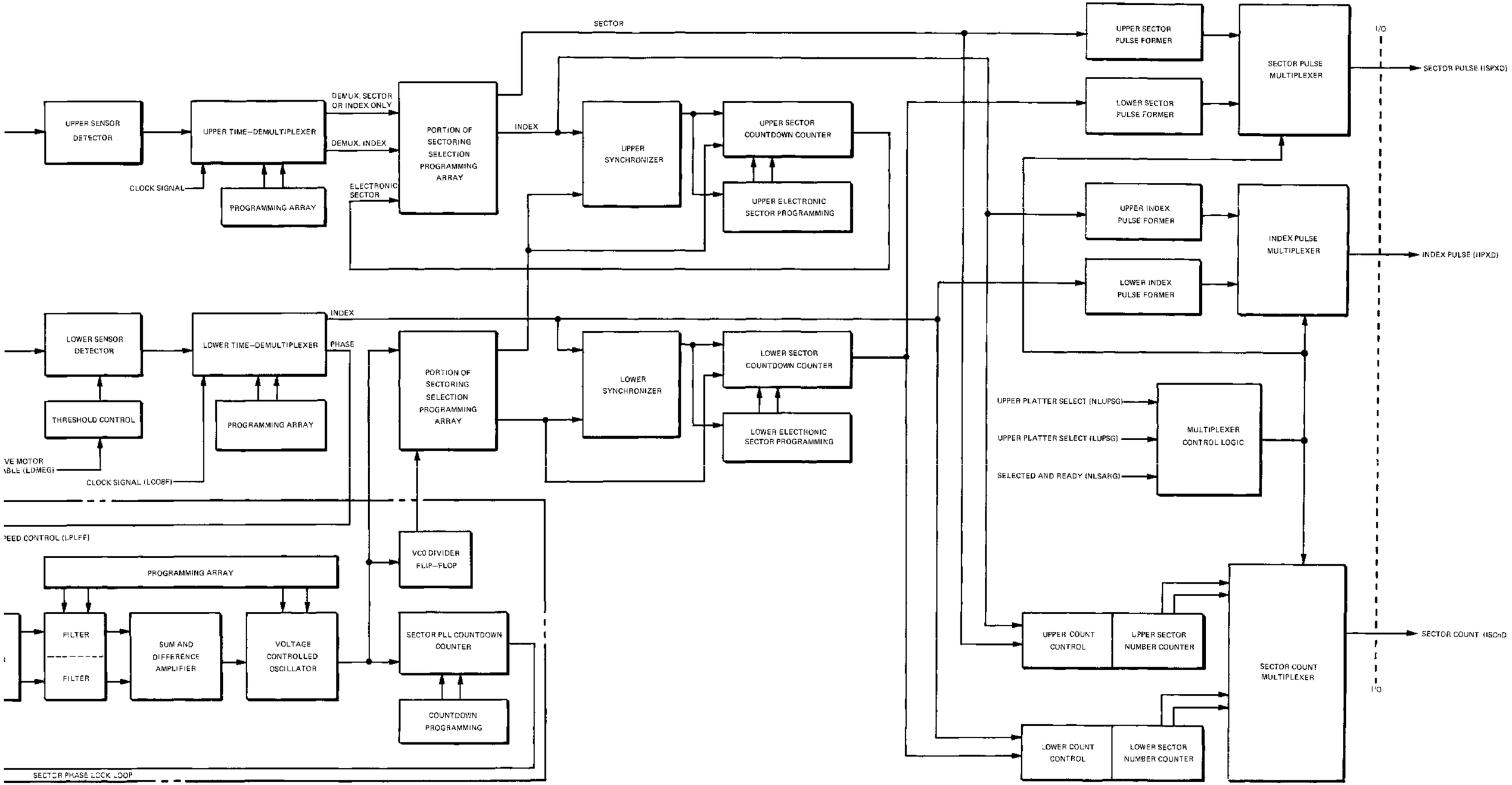


Figure 4-12. Sector Electronics, Functional Block Diagram

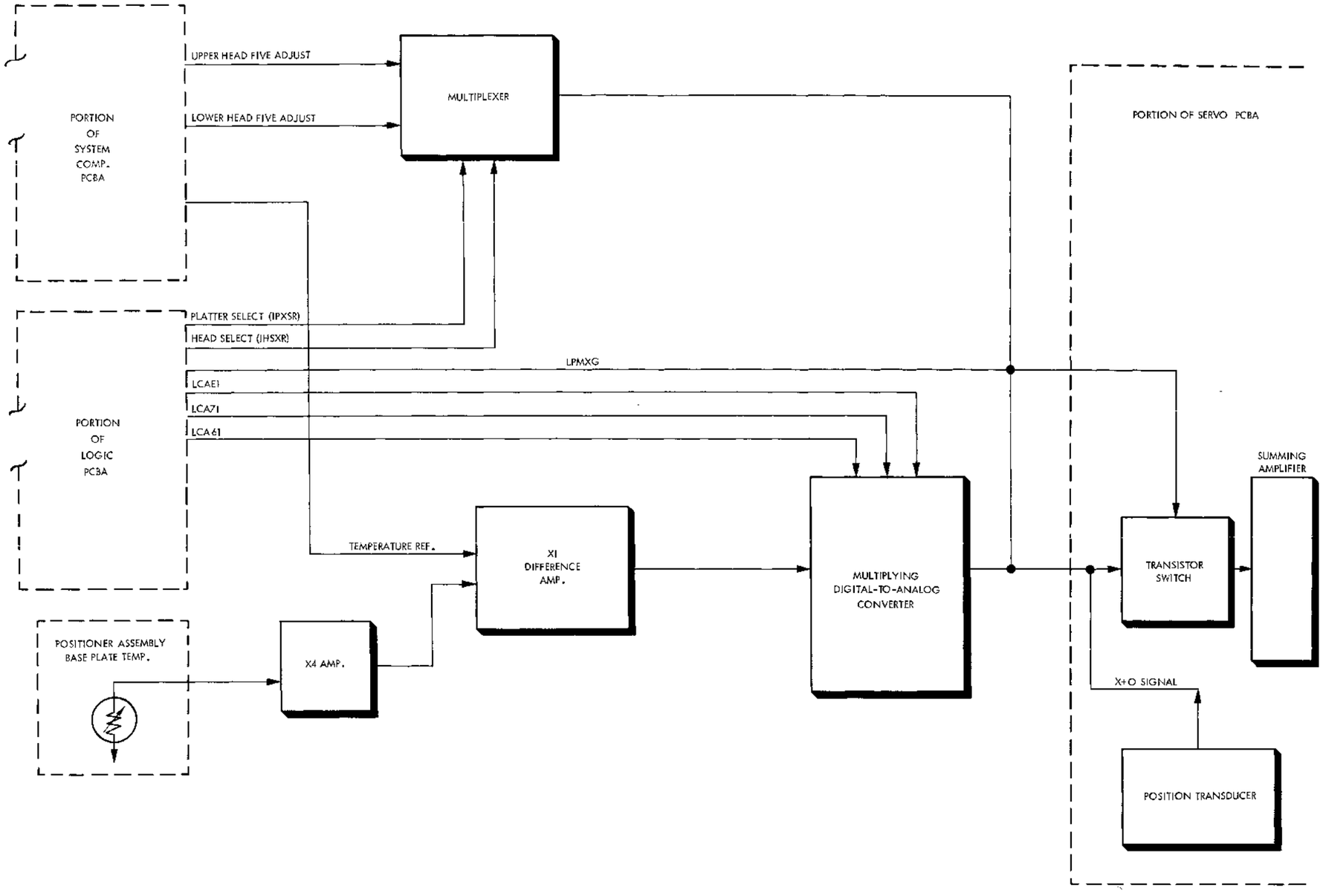


Figure 4-15. Temperature/System Compensation, Functional Block Diagram

SECTION V
DETAILED ELECTRICAL AND LOGIC DESCRIPTION

5.1 INTRODUCTION

This section contains the theory of operation of the printed circuit boards used in the D3000 Series Disk Drives. Schematic and assembly drawings for each board are contained at the end of Section VII.

A better understanding of the logic used in the disk drive can be gained when the operation of the various integrated circuit (IC) types is understood. Paragraphs 5.2 and 5.3 contain these descriptions and should be referred to in conjunction with the theory of operation for the individual PCBAs. A summary of integrated circuit function control and a summary of integrated circuit power and grounds are contained in Section VII.

5.2 TYPICAL TTL PARAMETERS AND CIRCUITS

Figure 5-1 shows typical NAND and NOR TTL circuits used in PERTEC devices. Also shown are the electrical parameters and switching characteristics of these typical 7400 series TTL circuits. (Component values given in Figures 5-1 through 5-21 are nominal.)

5.2.1 2-INPUT NAND GATE (TYPE 7400)

Figure 5-2 shows the logic symbol and truth table for the Type 7400 2-input NAND gate. Typically, each IC of this type contains 4 gates.

5.2.2 2-INPUT NOR GATE (TYPE 7402)

Figure 5-3 shows the logic symbol and truth table for the Type 7402 2-input NOR gate. Typically, each IC of this type contains 4 gates.

5.2.3 INVERTER (TYPE 7404)

Figure 5-4 shows the logic and truth table for the Type 7404 inverter. Typically, each IC of this type contains 6 inverters.

5.2.4 INVERTER (TYPE 7405)

Figure 5-5 shows the schematic and logic for the Type 7405 inverter. This inverter differs from the Type 7404 (Paragraph 5.2.3) in that the Type 7405 has an open-collector output. Typically, each IC of this type contains 6 inverters.

5.2.5 3-INPUT NAND GATE (TYPE 7410)

Figure 5-6 shows the logic symbol and truth table for the Type 7410 3-input NAND gate. Typically, each IC of this type contains 3 gates.

5.2.6 NAND SCHMITT TRIGGER (TYPE 7413)

Figure 5-7 shows the Type 7413 dual Schmitt trigger which consists of two identical Schmitt trigger circuits in monolithic integrated circuit form. Logically, each circuit functions as a 4-input NAND gate, but because of the Schmitt action the gate has different input threshold levels for positive and negative-going signals.

5.2.7 INVERTER BUFFER/DRIVER (TYPE 7416)

The Type 7416 inverter buffer/driver is a monolithic TTL circuit which features high-voltage open-collector outputs for interfacing with high-level circuits. It can also be used as an

inverter buffer for driving TTL inputs. The 7416, shown in Figure 5-8, has a minimum breakdown voltage of 15v and the maximum sink current is 40 ma. Typically, 6 inverters are packaged in this type IC.

5.2.8 8-INPUT NAND GATE (TYPE 7430)

Figure 5-9 shows the logic symbol and truth table for the Type 7430 8-input NAND gate. Typically, there is one gate per package.

5.2.9 2-INPUT NAND BUFFER (TYPE 7438)

The Type 7438 2-input NAND buffer is shown in Figure 5-10. This type buffer has an open-collector output and is typically packaged with 4 buffers per IC.

5.2.10 2-WIDE 2-INPUT AND-OR-INVERT GATE (TYPE 7450)

The logic, schematic, and truth table for the Type 7450 2-wide 2-input AND-OR-INVERT gate are shown in Figure 5-11. This type is normally packaged with 2 gates per IC.

5.2.11 J-K MASTER-SLAVE FLIP-FLOP (TYPE 7476)

The Type 7476 J-K Master Flip-Flop with pre-set and clear inputs is shown in Figure 5-12. Operation is based upon the master-slave principle with inputs to the master section controlled by the clock pulse. The clock also regulates the state of the coupling transistors which connect the master and slave sections.

Operationally, the slave section is isolated from the master section. Information is entered via the J and K inputs to the master section; the J and K inputs are then disabled. Information is then transferred from the master section to the slave section.

Two flip-flops are packaged in each IC of this type.

5.2.12 4-BIT BINARY FULL ADDERS (TYPE 7483)

The Type 7483 4-bit full adder, shown in Figure 5-13, is packaged on a single IC. The adder performs addition of two 4-bit binary numbers. The sum ( ) of each bit and the resultant carry (C4) is obtained from the fourth bit. Used in medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, this circuit utilizes high-speed, high-fanout transistor-to-transistor logic (TTL).

The necessity for extensive *look-ahead* and carry-cascading circuits is minimized by the use of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit.

5.2.13 2-INPUT EXCLUSIVE-OR GATE (TYPE 7486)

Figure 5-14 shows the logic symbol and truth table for the Type 7486 2-input EXCLUSIVE-OR gate. Typically packaged 4 gates per IC, each gate utilizes TTL circuitry to perform the function $Y = \overline{A}B + A\overline{B}$. When the input states are complementary, the output is a logic 1.

5.2.14 4-BIT BINARY COUNTER (TYPE 7493)

The Type 7493 4-bit binary counter, shown in Figure 5-15, consists of four master-slave flip-flops which are interconnected internally to provide a divide-by-two counter and a divide-by-eight counter. A reset line, which is gated directly, inhibits the count inputs and simultaneously returns the four flip-flop output to a logic zero.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN\ (1)}$	LOGIC 1 INPUT VOLTAGE REQUIRED AT INPUT TERMINAL TO ENSURE LOGIC 0 LEVEL AT OUTPUT		2			V
$V_{IN\ (0)}$	LOGIC 0 INPUT VOLTAGE REQUIRED AT ANY INPUT TERMINAL TO ENSURE LOGIC 1 LEVEL AT OUTPUT				0.8	V
$V_{OUT\ (1)}$	LOGIC 1 OUTPUT VOLTAGE	V_{CC} = MIN. V_{IN} = 0.8V I_{LOAD} = -400μA	2.4	3.3		V
$V_{OUT\ (0)}$	LOGIC 0 OUTPUT VOLTAGE	V_{CC} = MIN. V_{IN} = 2V I_{SINK} = 16mA		0.22	0.4	V
$I_{IN\ (0)}$	LOGIC 0 LEVEL INPUT CURRENT	V_{CC} = MAX. V_{IN} = 0.4V			1.6	mA
$I_{IN\ (1)}$	LOGIC 1 LEVEL INPUT CURRENT	V_{CC} = MAX. V_{IN} = 2.4V			40	μA
		V_{CC} = MAX. V_{IN} = 5.5V			1	mA

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD\ 0}$	PROPAGATION DELAY TIME TO LOGIC 0 LEVEL	C_L = 15pF R_L = 400Ω		8	15	ns
$T_{PD\ 1}$	PROPAGATION DELAY TIME TO LOGIC 1 LEVEL	C_L = 15pF R_L = 400Ω		12	22	ns

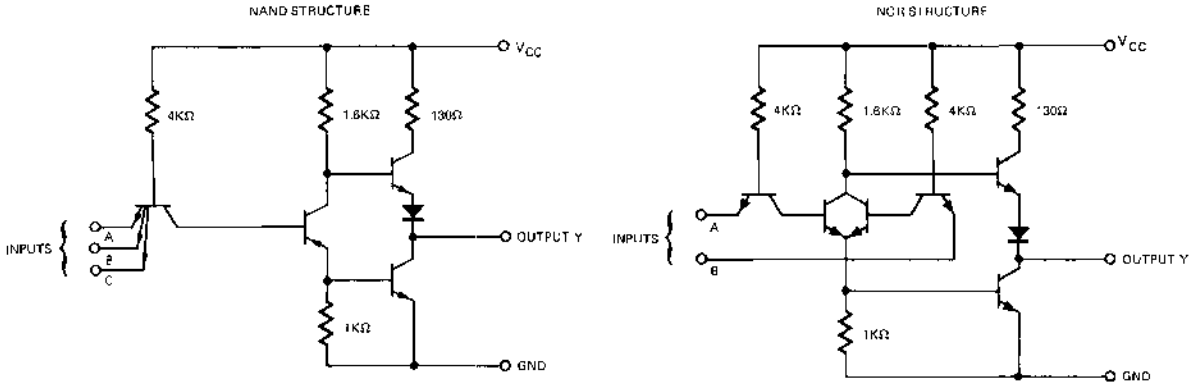
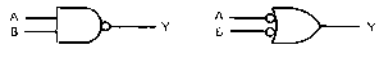
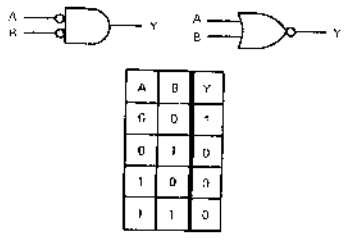


Figure 5-1. Typical TTL Parameters



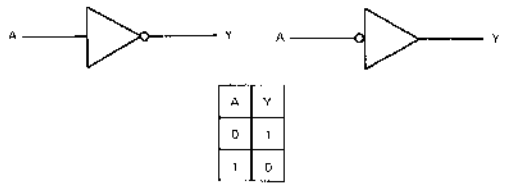
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure 5-2. 2-Input NAND Gate



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Figure 5-3. 2-Input NOR Gate



A	Y
0	1
1	0

Figure 5-4. Inverter (Type 7404)

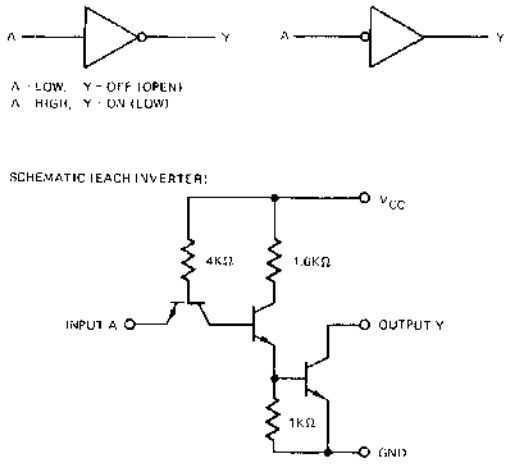
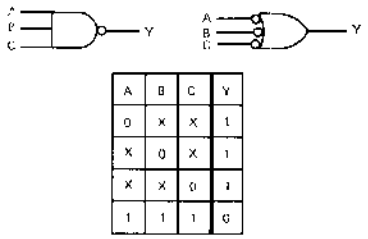
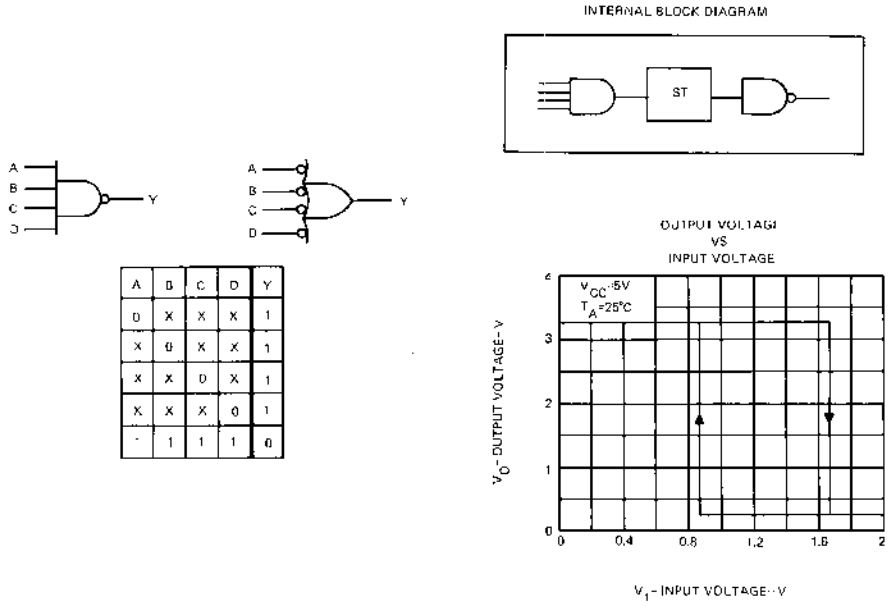


Figure 5-5. Inverter (Type 7405)



A	B	C	Y
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

Figure 5-6. 3-Input NAND Gate



A	B	C	D	Y
0	X	X	X	1
X	0	X	X	1
X	X	0	X	1
X	X	X	0	1
1	1	1	1	0

Figure 5-7. NAND Schmitt Trigger

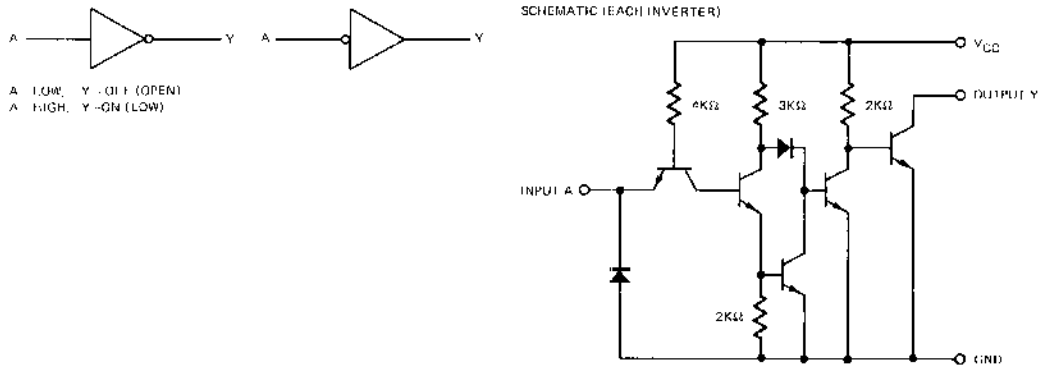
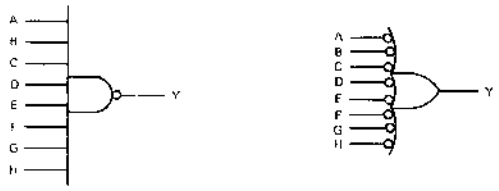
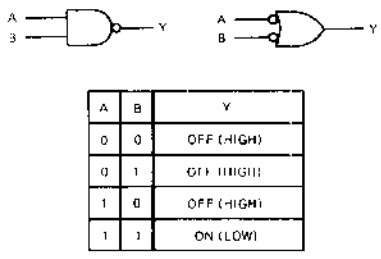


Figure 5-8. Inverter Buffer/Driver



A	B	C	D	E	F	G	H	Y
0	X	X	X	X	X	X	X	1
X	0	X	X	X	X	X	X	1
X	X	0	X	X	X	X	X	1
X	X	X	0	X	X	X	X	1
X	X	X	X	0	X	X	X	1
X	X	X	X	X	0	X	X	1
X	X	X	X	X	X	0	X	1
X	X	X	X	X	X	X	0	1
1	1	1	1	1	1	1	1	0

Figure 5-9. 8-Input NAND Gate



A	B	Y
0	0	OFF (HIGH)
0	1	OFF (HIGH)
1	0	OFF (HIGH)
1	1	ON (LOW)

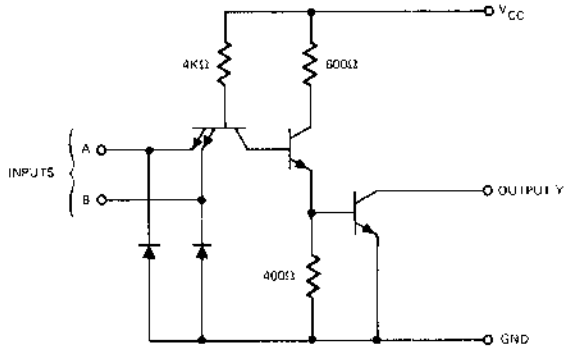
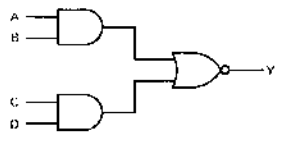


Figure 5-10. 2-Input NAND Buffer



A	B	C	D	Y
0	X	0	X	1
X	0	X	0	1
1	1	0	X	0
1	1	X	0	0
0	X	1	1	0
X	0	1	1	0
1	1	1	1	0

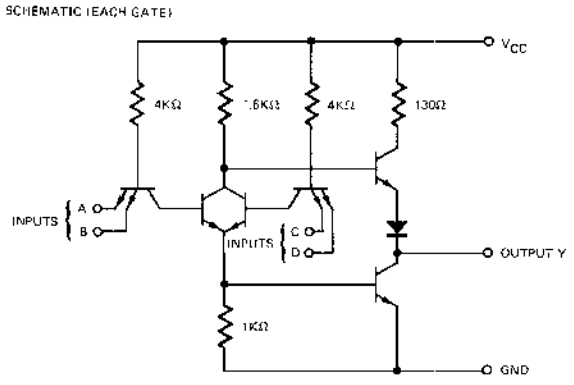
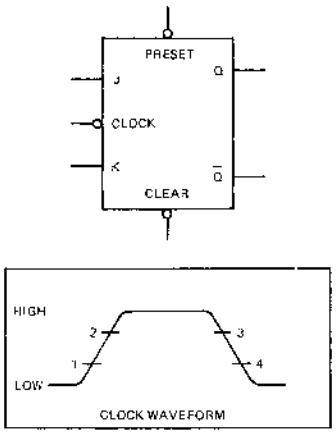


Figure 5-11. 2-Wide 2-Input AND-OR-INVERT Gate



TRUTH TABLE (EACH FLIP-FLOP)		
T_n		T_{n+1}
J	K	Q
0	0	$\overline{Q_n}$
0	1	0
1	0	1
1	1	$\overline{Q_n}$

NOTES: 1. T_n=BIT TIME BEFORE CLOCK PULSE.
2. T_{n+1}=BIT TIME AFTER CLOCK PLUSE.
3. POSITIVE LOGIC:
LOW INPUT TO PRESET SETS Q TO LOGIC 1
LOW INPUT TO CLEAR SETS Q TO LOGIC 0
CLEAR AND PRESET ARE INDEPENDENT OF CLOCK.

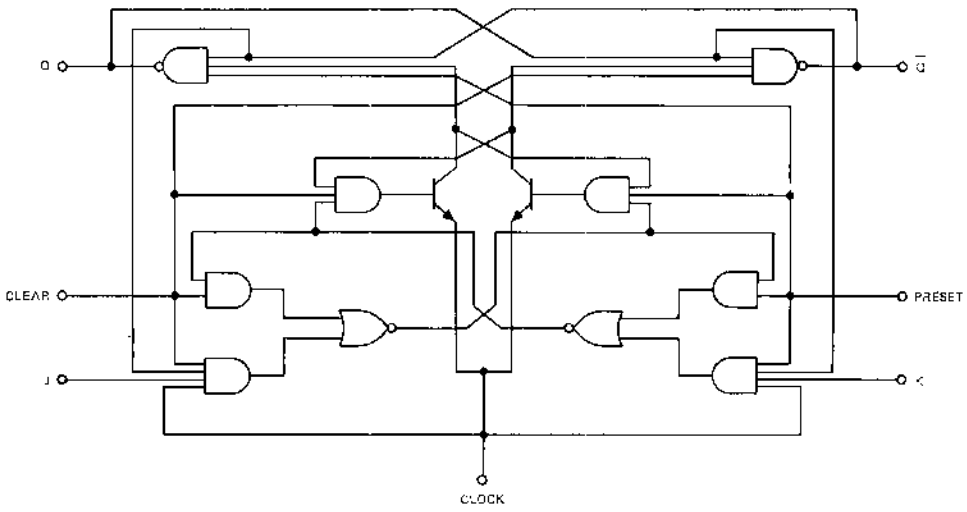
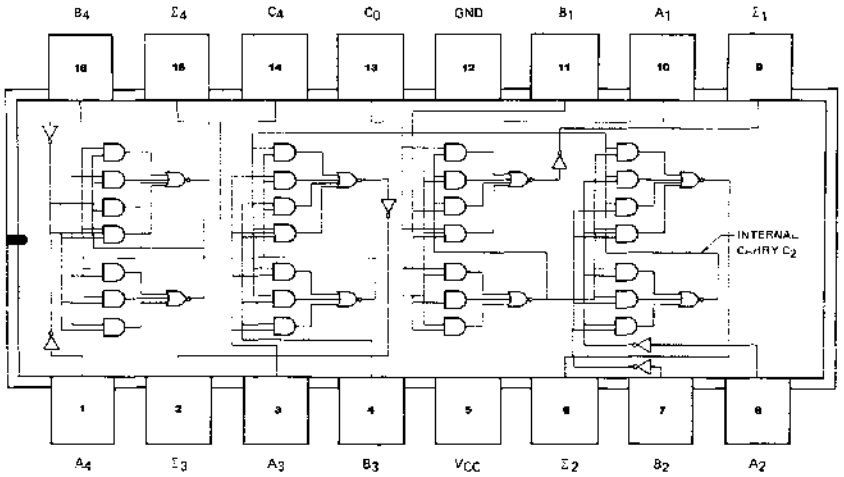


Figure 5-12. J-K Flip-Flop

INPUT				OUTPUT					
				WHEN $C_0=0$ / WHEN $C_2=0$			WHEN $C_0=1$ / WHEN $C_2=1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTE 1: INPUT CONDITIONS AT A_1, A_2, B_1, B_2, AND C_0 ARE USED TO DETERMINE OUTPUTS Σ_1 AND Σ_2, AND THE VALUE OF THE INTERNAL CARRY C_2. THE VALUES AT C_2, A_3, B_3, A_4, AND B_4, ARE THEN USED TO DETERMINE OUTPUTS Σ_3, Σ_4, AND C_4.



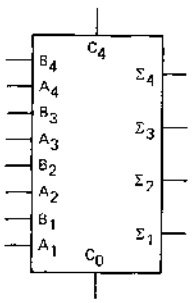


Figure 5-13. 4-Bit Binary Adder

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

POSITIVE LOGIC: Y=A⊕B

Figure 5-14. EXCLUSIVE-OR Gate

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES: 1. OUTPUT A CONNECTED TO INPUT B
2. TO RESET ALL OUTPUTS TO LOGIC 0, BOTH R1 AND R2 INPUTS MUST BE AT LOGIC 1.
3. EITHER (OR BOTH) RESET INPUTS R1 AND R2 MUST BE AT A LOGIC 0 TO COUNT.

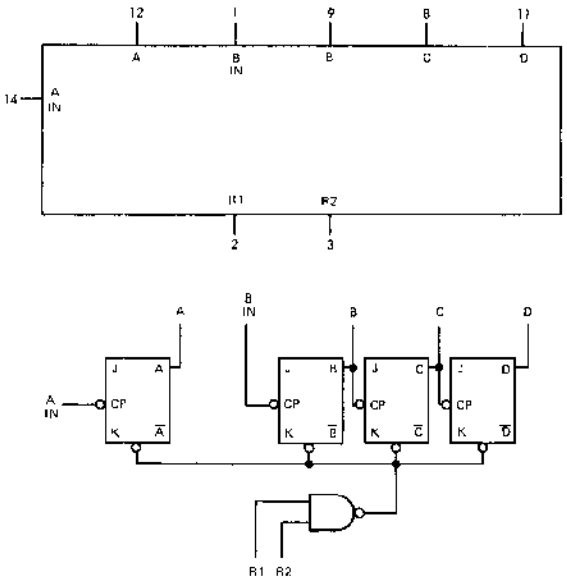


Figure 5-15. 4-Bit Binary Counter

Since the output of flip-flop A is not internally connected to the succeeding flip-flops, when this counter is used as a ripple-through counter output A is externally connected to input B. The input count pulses to the counter are applied to input A. Simultaneous division of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table in Figure 5-15. A single counter is typically contained on a single IC.

5.2.15 5-BIT SHIFT REGISTER (TYPE 7496)

The logic symbol and functional block diagram for the Type 7496 5-bit shift register is shown in Figure 5-16. This register is typically contained on a single IC. This register is made up of five R-S master-slave flip-flops connected to perform serial-to-parallel conversion of binary data. Since both inputs and outputs of all flip-flops are easily accessible, parallel-in/parallel-out or serial-in/serial-out operations may be performed.

Referring to Figure 5-16, all flip-flops may be simultaneously set to logic zero by the application of a logic zero voltage to the *clear* input. This condition may be applied independent of the state of the clock input.

The flip-flops in the shift register may be independently set to the logic one state by applying a logic one voltage to both the pre-set input of the specific flip-flop and the common pre-set input. The purpose of the pre-setenable input is to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. The pre-set input is also independent of the state of the clock input or clear input.

Information is transferred to the output pin of the flip-flop when the clock input changes from a logic zero to a logic one.

The serial input to the shift register provides information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logic one and the pre-set input must be at a logic zero when clocking occurs.

5.2.16 SYNCHRONOUS 4-BIT COUNTER (TYPE 74161)

The logic symbol and functional block diagram of Type 74161 synchronous 4-bit binary counter is shown in Figure 5-17. This counter is contained on a single IC.

The synchronous, pre-settable counters feature an internal carry look-ahead for application in high-speed counting schemes. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

The counters are fully programmable; that is, the outputs may be pre-set to either state. As pre-setting is synchronous, placing a low level on the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The clear function for the 74161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the state of the clock.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications. Instrumental in accomplishing this function are two count-enable inputs,

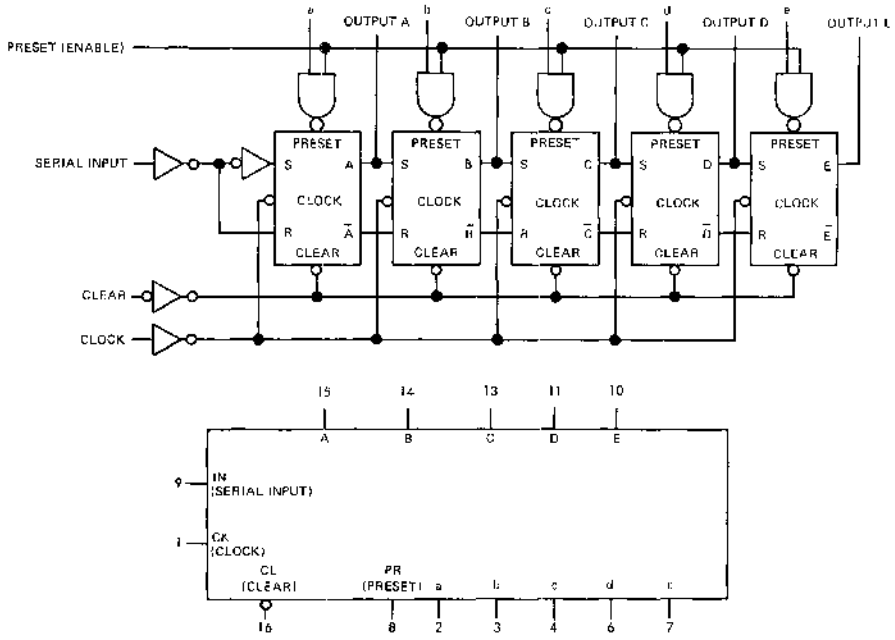
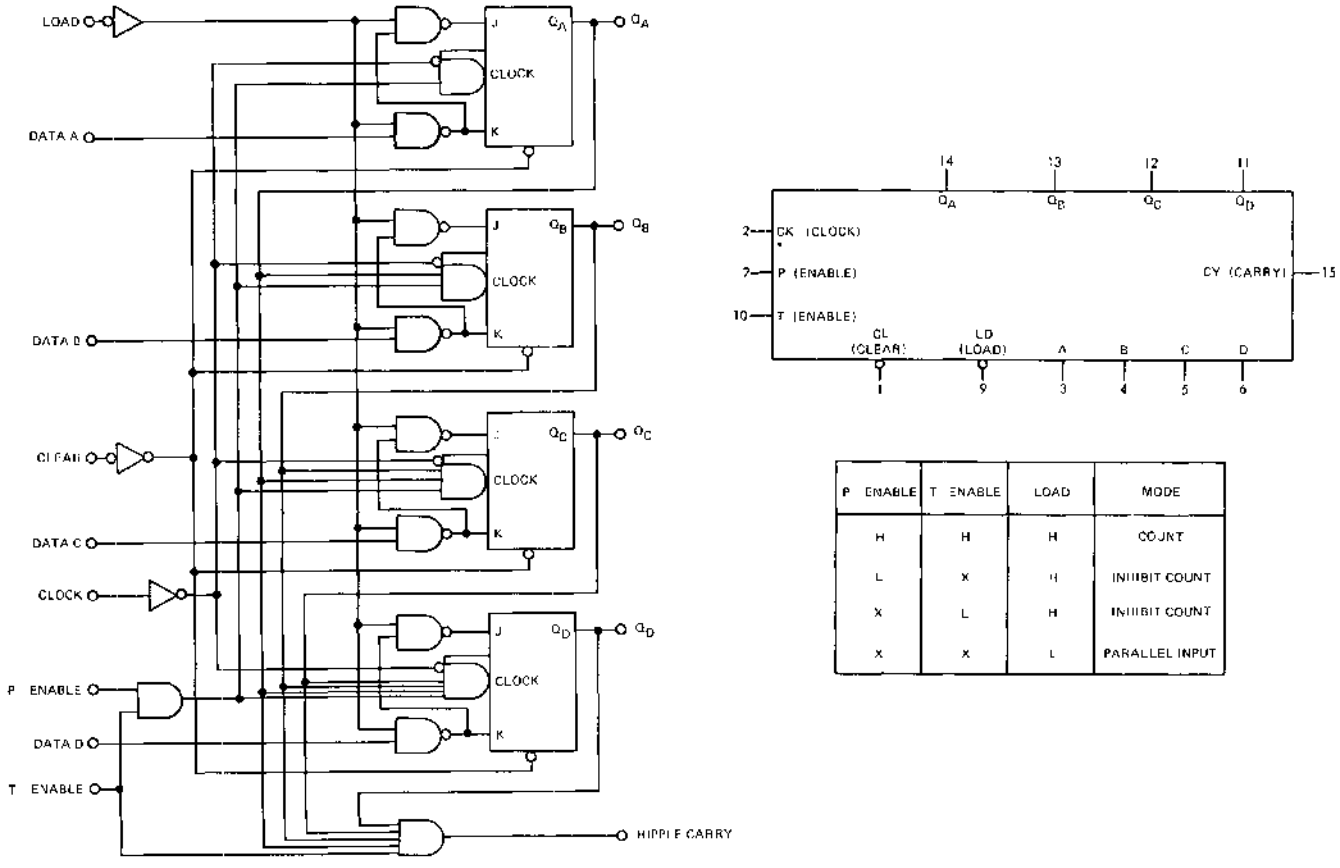


Figure 5-16. 5-Bit Shift Register



P ENABLE	T ENABLE	LOAD	MODE
H	H	H	COUNT
L	X	H	INHIBIT COUNT
X	L	H	INHIBIT COUNT
X	X	L	PARALLEL INPUT

Figure 5-17. Synchronous 4-Bit Counter

and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages.

Typical clear, pre-set, count, and inhibit sequences for the Type 74161 counter are shown in Figure 5-18. The actual sequences illustrated are: clear outputs to zero; pre-set to binary 12; count to 13, 14, 15, 0, 1, and 2; inhibit.

5.2.17 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER (TYPE 74164)

The logic symbol, functional block diagram of the 8-bit parallel-out serial shift register is illustrated in Figure 5-19. The timing diagram shown in Figure 5-20 should be referred to in conjunction with the functional block diagram.

Referring to Figure 5-19, it can be seen that these registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data since a low at either (or both) input(s) inhibit entry of new data and zero-sets the first flip-flop to the low level at the next clock pulse. A high level input enables the other input which then determines the state of the first flip-flop. Clocking occurs on the low-to-high transition of the clock.

5.2.18 SYNCHRONOUS 4-BIT UP/DOWN COUNTER (TYPE 74193)

The Type 74193 synchronous 4-bit up/down counters are synchronous reversible counters, i.e., up/down. The logic symbol and functional block diagram for the 74193 are shown in Figure 5-21. The associated timing diagram is shown in Figure 5-22. The logic symbol, horizontally oriented as illustrated, is used as a counter. Conversely, when the Type 74193 is used as a register in PERTEC equipment, the symbol is vertically oriented. The counter is typically contained on a single IC.

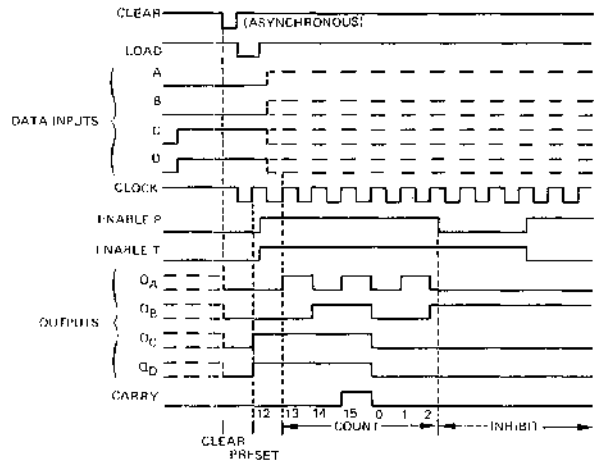


Figure 5-18. Clear, Preset, Count, and Inhibit Sequences for Type 74161 4-Bit Counter

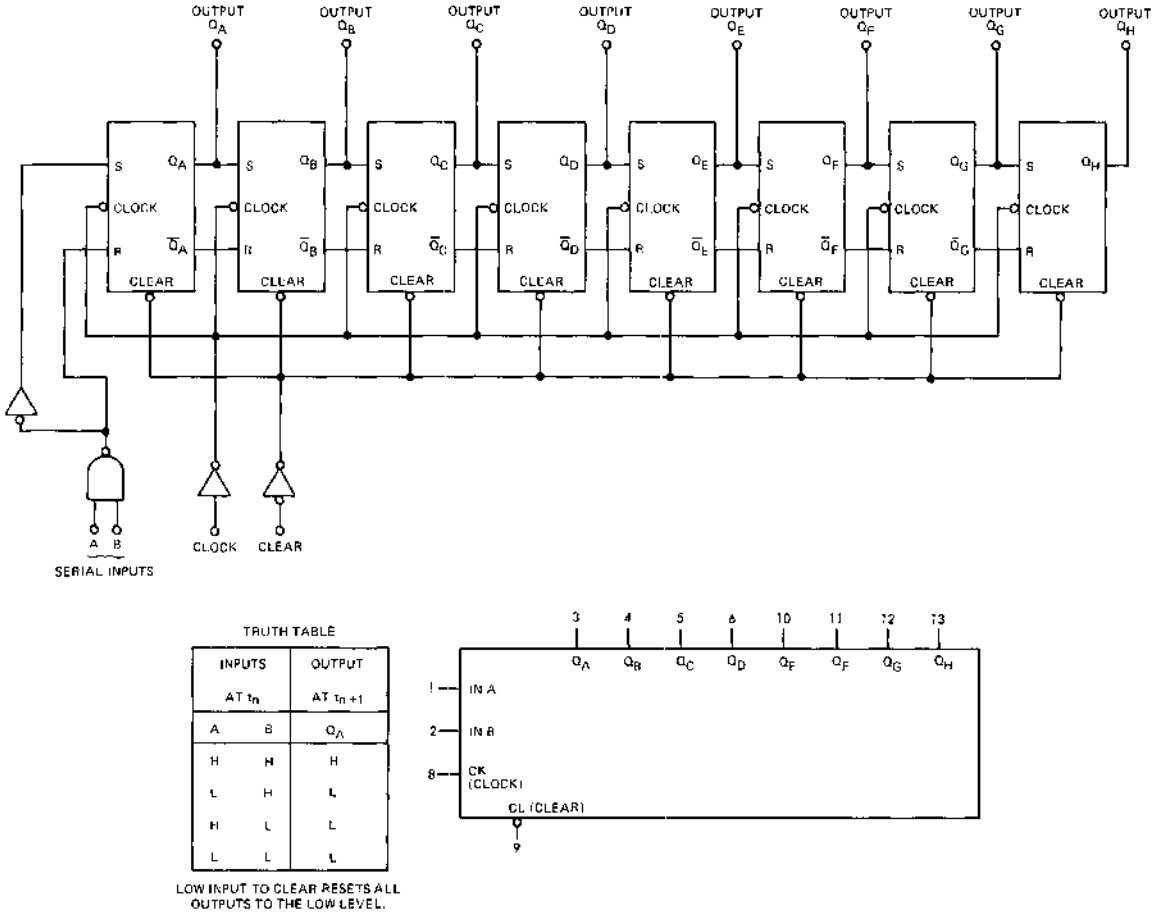


Figure 5-19. 8-Bit Parallel-Out Serial Shift Register

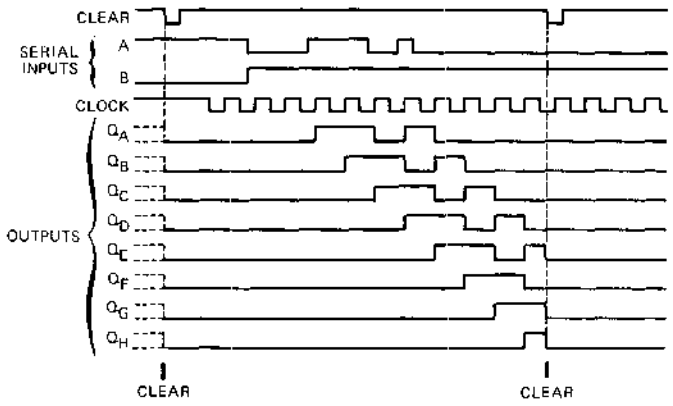


Figure 5-20. Typical Clear, Inhibit, Shift, Clear and Inhibit Sequence for Type 74164

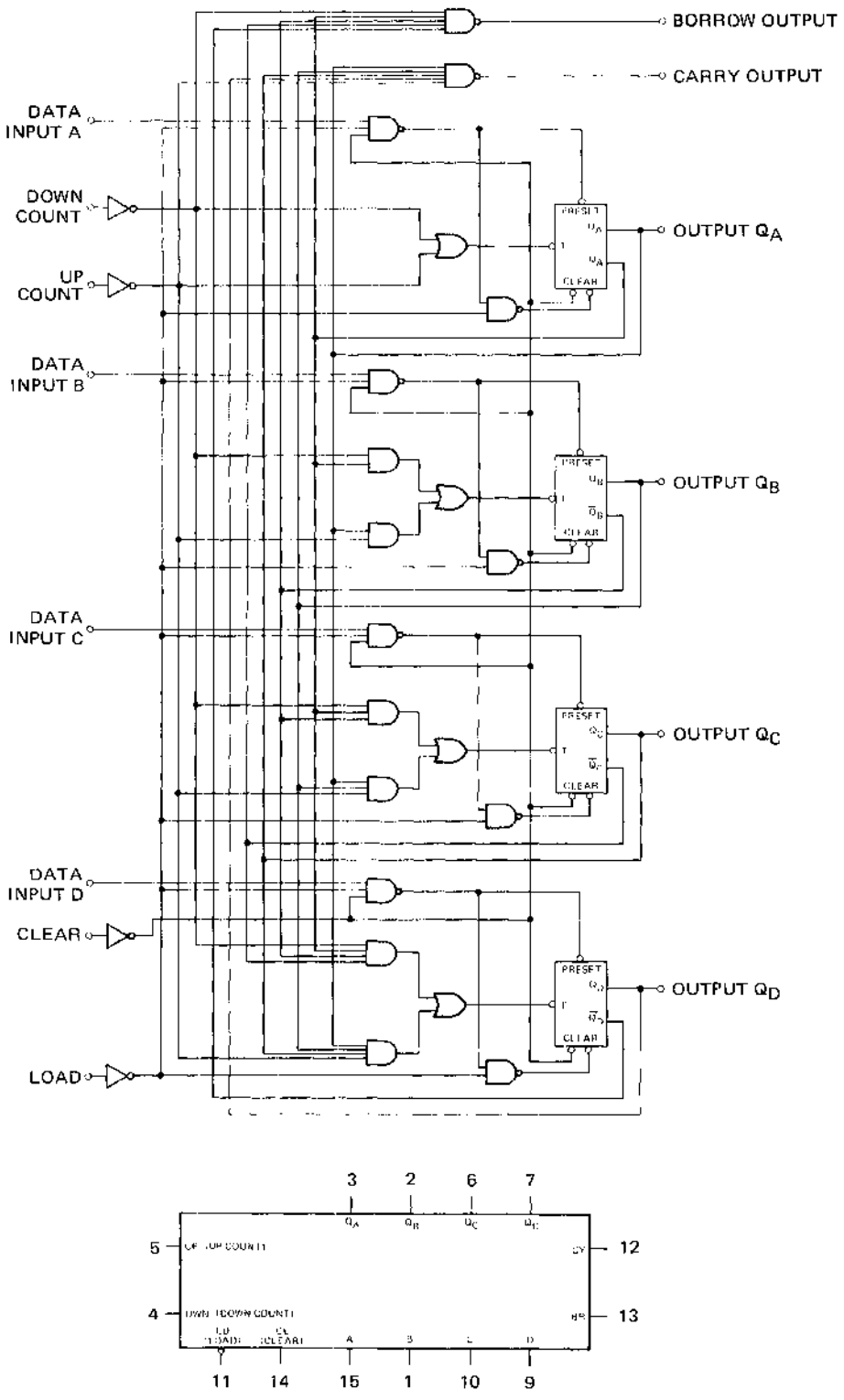
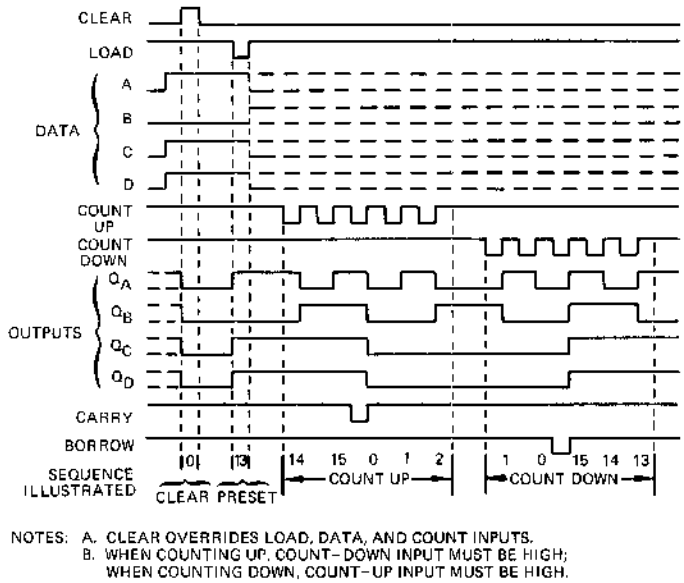


Figure 5-21. Synchronous 4-Bit Up/Down Counter



NOTES: A. CLEAR OVERRIDES LOAD, DATA, AND COUNT INPUTS.
B. WHEN COUNTING UP, COUNT-DOWN INPUT MUST BE HIGH;
WHEN COUNTING DOWN, COUNT-UP INPUT MUST BE HIGH.

Figure 5-22. Typical Clear, Load, and Count Sequence for Type 74193

As a counter, synchronous operation is achieved by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when instructed by the steering logic. It is important to note that this mode eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

Referring to Figure 5-21, the outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, the outputs may be pre-set to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses.

The 74193 is provided with a clear input which forces all outputs to the low level when a high level is applied. This clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized load.

The actual timing sequence illustrated in Figure 5-22 is: clear outputs to 0; load (pre-set) to BCD 13; count up to 14, 15, carry, 0, 1, 2; count down to 1, 0, borrow, 15, 14, and 13.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter. When used as a register, a low input to Load sets $Q_A = A, Q_B = B, Q_C = C$, and $Q_D = D$.

5.3 HIGH-SPEED TTL PARAMETERS

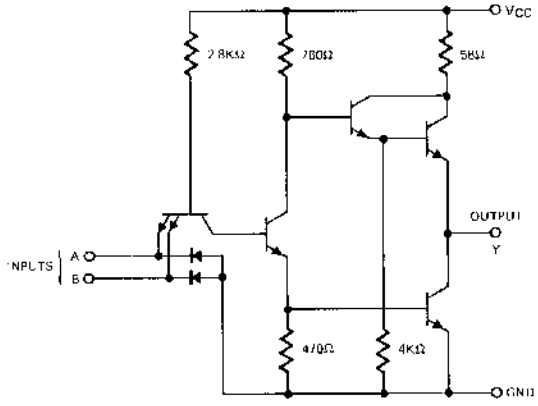
Figure 5-23 shows a typical HIGH SPEED TTL NAND circuit employed in PERTEC devices. Also shown are the electrical parameters and switching characteristics for the 74H series of devices. (Component values given in Figures 5-23 through 5-33 are nominal.)

5.3.1 HIGH SPEED 2-INPUT NAND GATE (TYPE 74H00)

The Type 74H00 2-input NAND gate logic symbot and truth table are shown in Figure 5-24. Typically, each IC of this type contains four gates.

5.3.2 HIGH SPEED INVERTER (TYPE 74H04)

Figure 5-25 shows the Type 74H04 high-speed inverter logic symbol and truth table. Normally, 6 inverters are packaged in a single IC.



ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} (1)	LOGIC 1 INPUT VOLTAGE REQUIRED AT INPUT TERMINAL TO ENSURE LOGIC 0 LEVEL AT OUTPUT		2			V
V_{IN} (0)	LOGIC 0 INPUT VOLTAGE REQUIRED AT INPUT TERMINAL TO ENSURE LOGIC 1 LEVEL AT OUTPUT				0.8	V
V_{OUT} (1)	LOGIC 1 OUTPUT VOLTAGE	V_{CC}=MIN. V_{IN} = 0.8 V I_{LOAD} = 500μA	2.4			V
V_{OUT} (0)	LOGIC 0 OUTPUT VOLTAGE	V_{CC}=MIN. V_{IN} = 2 V I_{SINK}=20 mA			0.4	V
I_{IN} (0)	LOGIC 0 LEVEL INPUT CURRENT	V_{CC} = MAX. V_{IN} = 0.4 V			-2	mA
I_{IN} (1)	LOGIC 1 LEVEL INPUT CURRENT	V_{CC} = MAX. V_{IN} = 2.4 V			50	uA
		V_{CC} = MAX. V_{IN} = 5.5 V			1	mA

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PD} 0	PROPAGATION DELAY TIME TO LOGIC 0 LEVEL	C_L = 25 PF R_L = 280Ω		6.5	10	NS
T_{PD} 1	PROPAGATION DELAY TIME TO LOGIC 1 LEVEL	C_L = 25 PF R_L 280Ω		6	10	NS

Figure 5-23. Typical High-Speed TTL Parameters

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure 5-24. 2-Input High-Speed NAND Gate

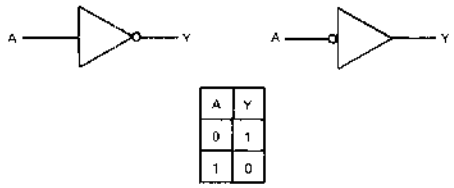


Figure 5-25. High-Speed Inverter

5.3.3 HIGH SPEED J-K MASTER-SLAVE FLIP-FLOP (TYPE 74H76)

The Type 7476 J-K Master-Slave Flip-Flop with pre-set and clear inputs is shown in Figure 5-26. Operation is based upon the master-slave principle. Inputs to the master section are controlled by the clock inpulse. The clock also regulates the state of the coupling transistors which correct the master and slave sections.

Operationally, the slave section is isolated from the master section. Information is entered via the J and K inputs to the master section; the J and K inputs are then disabled. Information is transferred from the master section to the slave section.

Two flip-flops are packaged in each IC of this type.

5.3.4 HIGH SPEED J-K EDGE-TRIGGERED FLIP-FLOP (TYPE 74H106)

Figure 5-27 illustrates the logic symbol, truth table, and functional block diagram of the Type 74H106 high-speed flip-flop. These flip-flops are negative-edge-triggered dual monolithic J-K flip-flops featuring individual J, K, clock, and asynchronous pre-set and clear inputs. Data are accepted when the clock input goes high. Input data are transferred to the output on the negative edge of the clock pulse.

Two flip-flops are packaged on a single IC.

5.3.5 DUAL LINE RECEIVER (COMPARATOR) (TYPE 75107)

The Type 75107 monolithic dual line receivers feature two independent channels as shown in Figure 5-28. Each IC of this type contains the logic shown plus a common current source, supply voltages, and ground. An individual receiver consists of a differential input stage which provides a high input impedance, a level-shifting stage, a second differential amplifier which enhances the common-mode rejection ratio, and a typical TTL output stage.

Two strobes are provided at the input of each gate. The receiver may be enabled or inhibited, respectively, when a logic 1 is applied to both strobes or a logic 0 is applied to either strobe. A strobe or gating input may be used on the output stage of either channel to hold the output at a logic 1 regardless of the input signal.

There are many applications for line receiver when used as differential comparators, such as voltage comparators, threshold detectors, controlled Schmitt triggers, and pulse width controls.

In the D3000 Disk Drive, the Type 75107 is employed as dual differential comparators. As a differential comparator, a 75107 may be connected so as to compare the non-inverting

input terminal with the inverting input. Thus, a logic 1 or 0 is experienced as the output resulting from one input being greater than the other. The strobe inputs allow additional control over the circuit so that either output (or.both) may be inhibited.

5.3.6 DUAL PERIPHERAL DRIVER (TYPE 75451)

The logic symbol for the Type 75451 dual peripheral driver is shown in Figure 5-29 along with its schematic and alternate logic symbol. Two of this type driver a typically packaged on a single IC.

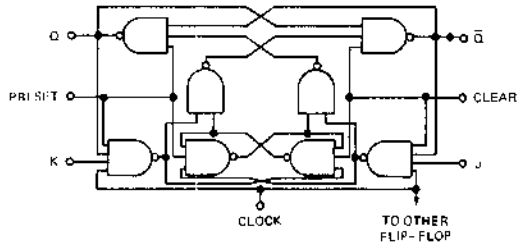


Figure 5-26. High-Speed J-K Master-Slave Flip-Flop

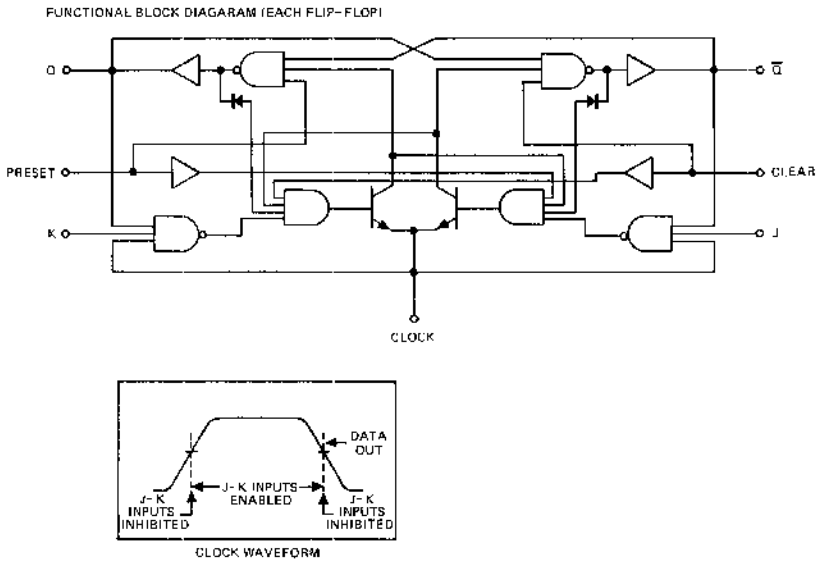
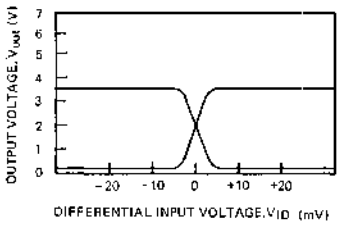


Figure 5-27. High-Speed J-K Edge-Triggered Flip-Flop

DIFFERENTIAL INPUTS A–B	STROBES		OUTPUT
	G	S	Y
$V_{ID} \geq 25$ mV	L OR H	L OR H	H
25 mV < V_{ID} < 25 mV	L OR H	L	H
	L	L OR H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L OR H	L	H
	L	L OR H	H
	H	H	L

V_{ID} =VOLTAGE INPUT DIFFERENCE



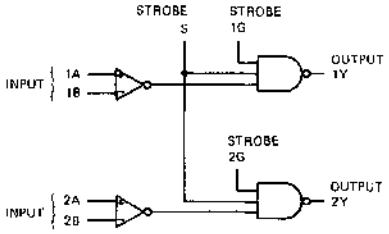
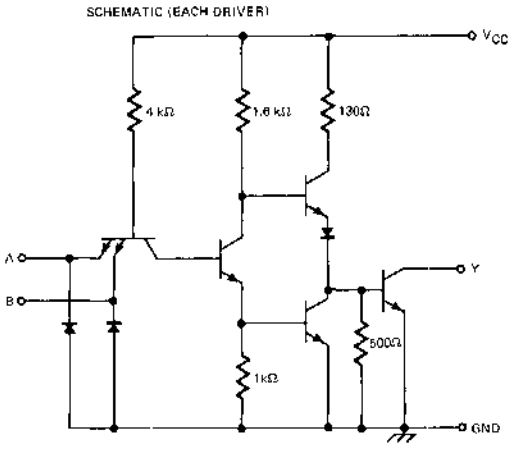
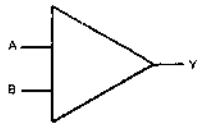


Figure 5-28. Dual Line Receiver



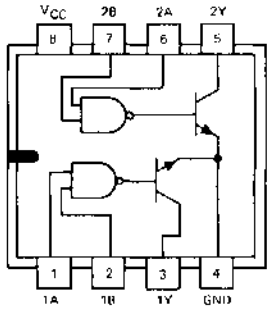


PRIMARY LOGIC SYMBOL

TRUTH TABLE

A	B	Y
L	L	L (ON STATE)
L	H	L (ON STATE)
H	L	L (ON STATE)
H	H	H (OFF STATE)

H=HIGH LEVEL, L=LOW LEVEL



ALTERNATE LOGIC SYMBOL

Figure 5-29. Dual Peripheral Driver

5.3.7 OPTO-ISOLATOR

The opto-isolator is an NPN silicon planar phototransistor optically coupled to a diffused planar gallium arsenide light-emitting diode. This device is shown in Figure 5-30; it is used to provide electrical isolation between input and output. Each device is contained in a separate package.

5.3.8 HIGH SPEED OPERATIONAL AMPLIFIER (TYPE 715)

The 715 is a linear integrated circuit type of high speed operational amplifier. The logic symbol for the Type 715 is shown in Figure 5-31.

Constructed on a single silicon chip using the epitaxial process, it is designed for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The Type 715 has a fast settling time, high slew rate, low offsets, and a high output swing.

5.3.9 DIFFERENTIAL VIDEO AMPLIFIER (TYPE 733)

The logic symbol and pin identification for the Type 733 linear integrated circuit type of differential amplifier is shown in Figure 5-32. The Type 733 is a monolithic differential input, differential output, wideband (120 MHz) video amplifier.

It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth, and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads.

5.3.10 OPERATIONAL AMPLIFIER (TYPE 741)

The logic symbol for the Type 741 linear integrated circuit type of operational amplifier is shown in Figure 5-33. The 741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the epitaxial process. It is intended for a wide range of analog applications. The high gain and wide range of operating voltages provide for operation in integrator, summing amplifier, and general feedback applications. In addition, it is short-circuit protected and requires no external components for frequency compensation.

5.3.11 TIMER (TYPE 555)

The block diagram for the monolithic timer is shown in Figure 5-34. The monolithic timer is a highly stable controller capable of producing accurate time delays or oscillations. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor.

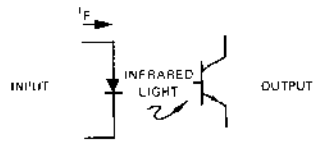


Figure 5-30. Opto-Isolator

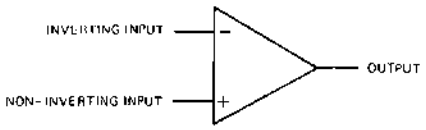
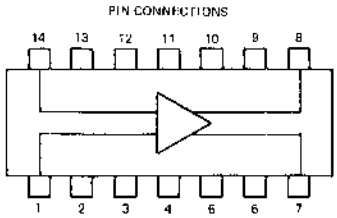


Figure 5-31. High-Speed Operational Amplifier



1. INPUT 2
2. NC
3. G_{2B} GAIN SELECT
4. G_{1B} GAIN SELECT
5. V^-
6. NC
7. OUTPUT 2
8. OUTPUT 1
9. NC
10. V^+
11. G_{1A} GAIN SELECT
12. G_{2A} GAIN SELECT
13. NC
14. INPUT 1

Figure 5-32. Differential Video Amplifier

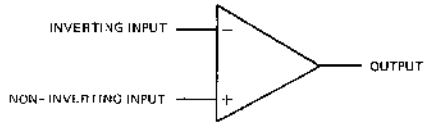


Figure 5-33. Operational Amplifier

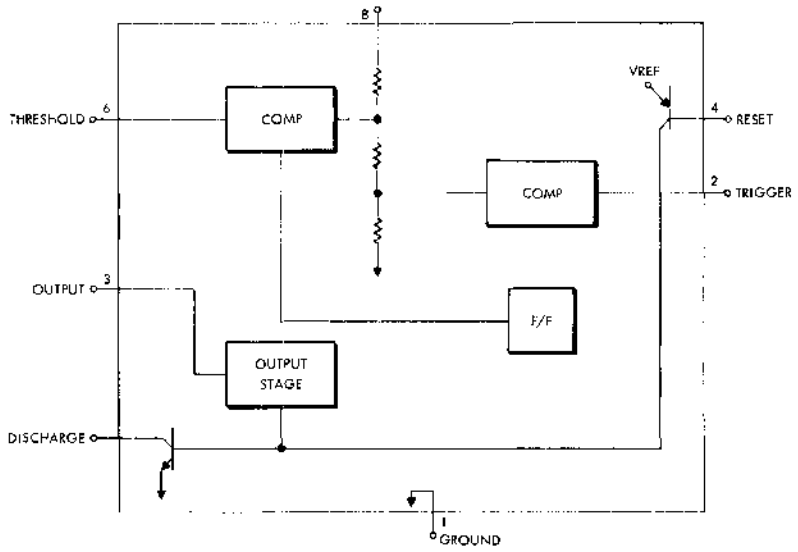


Figure 5-34. Timer

5.4 LOGIC TERM MNEMONIC IDENTIFICATION

All digital signals in the D3000 Disk Drive are identified by a name which will be referred to as the logic term.

Logic terms may be descriptive of a condition or an event, or they may be a generalized name used primarily for documentation purposes. If a descriptive name is essential to facilitate the understanding of a function, a generalized term is not used.

Appendix A of this manual contains the mnemonic listing for the standard D3000 Series Disk Drive. An understanding of the mnemonic scheme employed is essential to the total understanding of the D3000 logic drawings. Also included in Appendix A are figures and tables which provide the user with an understanding of the six character logic term.

5.5 SERVO PCBA

The following paragraphs describe the Servo PCBA installed in the D3000 Series Disk Drive. Refer to Schematic No. 102810 and Assembly No. 102811.

The Servo PCBA is approximately 10 inches square with two connectors along one edge. Figure 5-35 illustrates the placement of each connector, test point, and adjustable component on this board. J201 and J202 are the connectors which connect via mating plugs and 3M flat cables to the Logic PCBA. The remainder of connectors are of the Molex type.

In general, the connectors perform the following functions.

(1) Electrically connect the Servo Board to all base casting-mounted assemblies, e.g., power supply, positioner coil, velocity and position transducers, emergency unload capacitor, brush motor, cartridge lock solenoids and heatsinks.

(2) Provide power to the Logic PCBA.

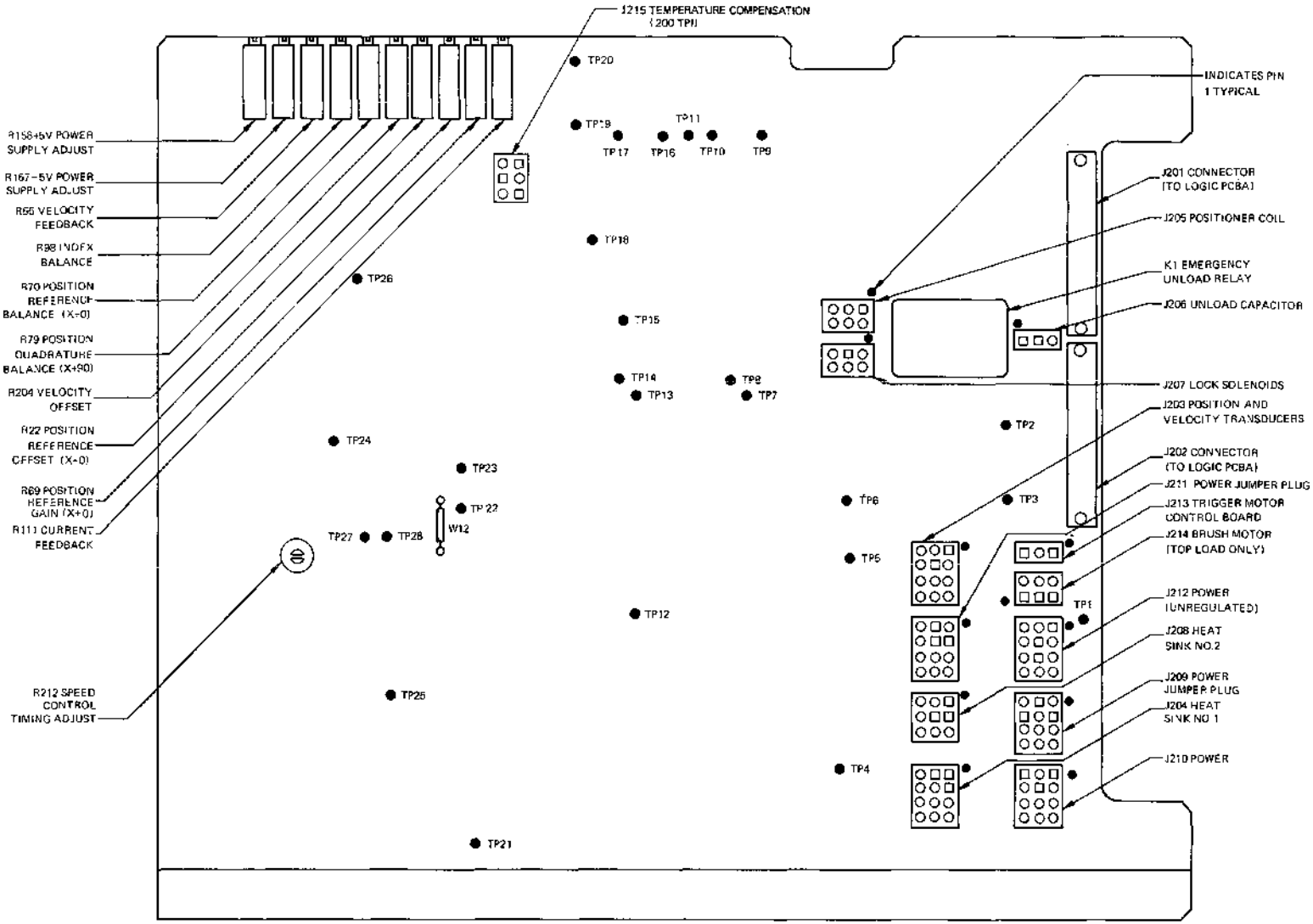


Figure 5-35. Servo PCBA Test Point and Connector Placement

(3) Provide a path for signals and levels between the Servo and the Logic PCBAs.

(4) Provide a path for the +5v and control signals to the motor control board.

(5) Provide a path for temperature compensation signals from the Temperature Compensation PCBA to the Servo PCBA (200 tpi models).

Contained on the Servo PCBA are the electronics for voltage regulators, positioner, emergency unload system, ac motor speed control circuits, brush motor driver, cartridge lock solenoid driver, and power clear circuit.

The circuit board description in the following paragraphs consists of the circuits associated with each of the connectors.

5.5.1 VOLTAGE REGULATORS

The power supply voltage regulators are shown on Schematic No. 102810, sheet 2 of 3. J212 (zone F16) connects unregulated +20v, —20v, +10v, and auxiliary 21v ac for the brush motor driver and ac motor control circuit to the Servo PCBA. Note that two pins are allocated to the high current lines to reduce the current density in the pins.

The +10v and —10v regulators are series regulators using zener diodes VR4 and VR10, respectively, for the voltage reference. The emitter base junction of Q28 is in series with VR4, and diode CR43 is in series with VR10, thus improving the temperature stability of the supplies.

The +5v and —5v regulators consist of two similar circuits whose outputs are set by potentiometers R158 (zone F14) and R167 (zone E14). Outputs of the +5v and —5v regulators can be monitored at TP4 and TP12, respectively. Operational amplifiers U15 and U18 are used as voltage followers in the regulating circuit. The high open-loop gain of the operational amplifier in the feedback regulaing circuit offers improved line and load regulation characteristics to the +5v and —5v supplies. Zener diodes VR7 and VR11 provide the voltage references for +5v and —5v. Diodes CR38, CR40, and CR42, CR44 improve the temperature stability of the supplies.

Regulator power transistors Q24, Q25, Q26, Q33 are mounted on heatsinks external to the Servo PCBA. J204 and J208 connect the regulators to the external heatsink.

A *crowbar* over-voltage protection circuit is provided for the +5v and —5v supplies. These circuits are employed to detect an increase of 3v in the +5v supplies. Zener diodes VR8 (zone F11) and VR9 (zone E12) detect an increase in the +5v and —5v supplies, respectively. An increase to +8v or —8v causes SCR3 or SCR4 to fire, which in turn causes the +20v or —20v fuse on the power supply module to blow, thus removing the relevant 20v supply.

A *crowbar* over-voltage protection circuit is also provided on +10v and —10v supplies and employ zener diodes VR5 and VR6 (zone F15), VR12 and VR13 (zone D14), respectively, to detect an increase in the +10v supplies. A voltage increase to +15v or —15v causes SCR2 or SCR4 to fire which, in turn, causes the +20v or —20v fuse on the power supply module to blow, thus removing the relevant 20v supply.

J209 (zone G,H-10) and J211 (zone D,E-10) are jumper plugs which connect unregulated +20v and regulated +5v and +10v from regulators to the remainder of the circuits on the Servo PCBA and to the Logic PCBA via J210. These jumper plugs enable the isolation of the regulators and power supply for maintenance purposes.

The unregulated +20v supplies are used in the positioner power amplifier and the power clear circuit. In addition, the —20v supply is used in cartridge lock solenoid driver and emergency unload relay driver. The +5v regulators supply power to the digital ICs, linear ICs, mode control electronics, brush motor driver, ac motor control circuit, relay driver, and cartridge lock solenoid driver. The +10v regulators supply power to the operational amplifiers, velocity function generator, mode control electronics, position transducer signal conditioners, and position transducer lamp driver.

5.5.2 POSITIONER SERVO ELECTRONICS

The positioner electronics consists of the Velocity Function Generator, Mode Control circuits, Position Transducer Signal Conditioners, Velocity Transducer Amplifier, Summing Amplifier, Positioner Power Amplifier, Position Transducer Lamp Driver Failure Detector, and the Emergency Unload System. Refer to Paragraph 5.4 for definition of logic term mnemonics used in the following descriptions.

J201 provides a path for the majority of logic command signals for the positioner servo system from the Logic PCBA to the Servo PCBA. J202 provides a path for the remaining logic signals from the Logic PCBA to the Servo PCBA, and vice versa.

5.5.2.1 Velocity Function Generator

The Velocity Function Generator is shown on Schematic No. 102810, sheet 1 of 3. This circuit generates a step voltage signal of known polarity (positive or negative) which can be monitored at TP9 (zone H15). The polarity of this signal is dependent upon the state of logic command signals NLAD0G, NLAD1G, NLAD2G, NLAD3G, NLAD4G, NLAD5G, NLAD6G, NLAD7G, NLADEG, and LFDX1. Assume that the address difference is non-zero and is such that the signals at pin 19, 18, 27, 28, 29, 30, 33, 31, 32 of J201 are in the logic low state, i.e., signals are active. Correspondingly, the output logic state of ICs U3-A, U3-B, U3-C, U3-D, and U5-A, U5-D will be high causing diodes CR1, CR3, CR5, CR7, CR9, and CR11 to be reverse-biased.

Diodes CR2, CR4, CR6, CR8, CR10, and CR12 are forward-biased and current flowing through resistor network R1 and R2, R7 and R8, etc., is summed at the summing junction (pin 2) of operational amplifier U8 (zone H15). The output at TP9 will be +6v depending on the state of Forward Direction (LFDX1) logic signal. When LFDX1 is high, the output at TP9 will be +6v and when LFDX1 is low, the output at TP9 will be —6v. Similarly, when the address difference is zero, the state of the logic command signals NLAD0G through NLADEG is such that the output logic state of ICs U3-A, U3-B, U3-C, U3-D, and U5-A, U5-D will be low, and diodes CR1, CR3, CR5, CR7, CR9, CR11 will be forward-biased. Diodes CR2, CR4, CR6, CR8, CR10, and CR12 are reverse-biased and no current flows from the resistor network into the summing junction of U8 except from R24 and R25. Consequently, the output at TP9 will be +0.3v depending on the state of logic signal LFDX-1.

A third possibility exists when the address difference is non-zero and the state of signals NLAD0G through NLADEG is such that some of the output logic states at the outputs of U3-A, U3-B, U3-C, U3-D, and U5-A, U5-D are high and others are low. In that case, the output at TP9 will be a voltage step in between +6v and +0.3v depending on the output logic states of U3-A, U3-B, U3-C, U3-D, and U5-A, U5-D.

Velocity Reference Enable (NLVREG) going low at pin 20 of J201 turns Q3 (zone F15) on and current flows from TP9 through R15 and into the summing junction (pin 2) of the summing amplifier U16 (zone G12). When NLVREG is high, Q3 is turned off and no current

flows into the summing junction of U16. Hence, FET Q3 acts as a switch which enables the velocity reference signal at TP9, generated by the velocity function generator, to be passed into the summing junction of the summing amplifier U16.

5.5.2.2 Mode Control

The Mode Control circuitry is shown on Schematic No. 102810, sheet 1 of 3. When Track Offset Plus (NLTOPG) at pin 26 of J201 (zone E19) is low and Track Offset Minus (NLTOMG) at pin 25 of J201 is high, transistor Q5 is off and Q6 is on; consequently, the signal at TP11 will be +4.5v +0.5v. Conversely, a high state of NLTOPG and a low state of NLTOMG turns Q5 on and turns Q6 off, and the voltage at TP11 will be —4.5v +0.5v. When NLTOPG and NLTOMG both are high, transistors Q5 and Q6 are both on and the voltage at TP11 will be 0v.

Forward Slow Mode (NLFSM1) low at pin 24 of J201, Reverse Slow Mode (NLRSM1) high at pin 23 of J201 and the high output of U10-A pin 4 (i.e., Heads Retracted (SHRXG) low at TP14, zone D11) causes Q7 and Q10 (zone C16) to turn off, and Q8 (zone C17) to turn on. Thus, the signal at TP10 will be +4.5v +0.5v. Conversely, when NLFSM1 is high, NLRSM1 is low and SHRXG is low, Q8 and Q10 are turned off and Q7 is turned on. Consequently, the signal at TP10 is —4.5v +0.5v. When NLFSM1 is high, NLRSM1 is low and SHRXG is high, Q8 is turned off. However, Q10 and Q7 are turned on and the signal at TP10 is approximately 0.3v. Finally, when NLFSM1 and NLESM1 are high, Q7 and Q8 are turned on, and regardless of the state of SHRXG, the voltage at TP10 is 0v.

Potentiometer R22 (zone F16) is used to adjust for the dc offsets when the servo is in the Position Mode. TP19 and R40 (zone D15) provide a means to introduce an external perturbation signal into the summing amplifier.

5.5.2.3 Position Transducer Signal Conditioners

The Position Transducer Signal Conditioner circuitry is shown on Schematic No. 102810, sheet 1 of 3. These circuits are employed to amplify the low level position transducer signals (X + 0, X + 90, Index, Heads Retracted) and convert them to appropriate logic signals (SPRCG, SPQCG, SPTIG, and SHRXG). J203 (zone A15) connects all position transducer signals and velocity transducer signals to the Servo PCBA. Outputs from the Position Transducer Signal Conditioners are routed to the Logic PCBA via edge connector J202 (zone B11).

Figure 5-36 describes the position transducer output signals, namely Heads Retracted, Index, X + 0 and X + 90, at pins 6, 1, 3, and 2, respectively, of connector J203, as the positioner carriage is moved in the forward direction, i.e., toward the spindle. The amplitude of the Heads Retracted and Index signal is approximately 10 mv at pins 6 and 1 of J203, respectively. The amplitude of X + 0 and X + 90 signal is approximately 120 mv to 200 mv, at pins 3 and 2 of J203, respectively.

The output of the Heads Retracted, Index, X + 0, and X + 90 amplifiers can be monitored at TP6, TP3, TP20, and TP2, respectively. Figure 5-37 describes the output of these amplifiers and should be referenced in conjunction with Figure 5-36.

Potentiometers R70 (zone F14), R79 (zone E14), R98 (zone C14) provide dc bias for balance adjustments of the X + 0, and X + 90 and Index signals, respectively. R69 (zone F13) provides gain adjustments for (X + 0) signal at TP20. Type 741 operational amplifiers (U1, U2, U6, and U7) are used as high gain inverting amplifiers to amplify these signals.

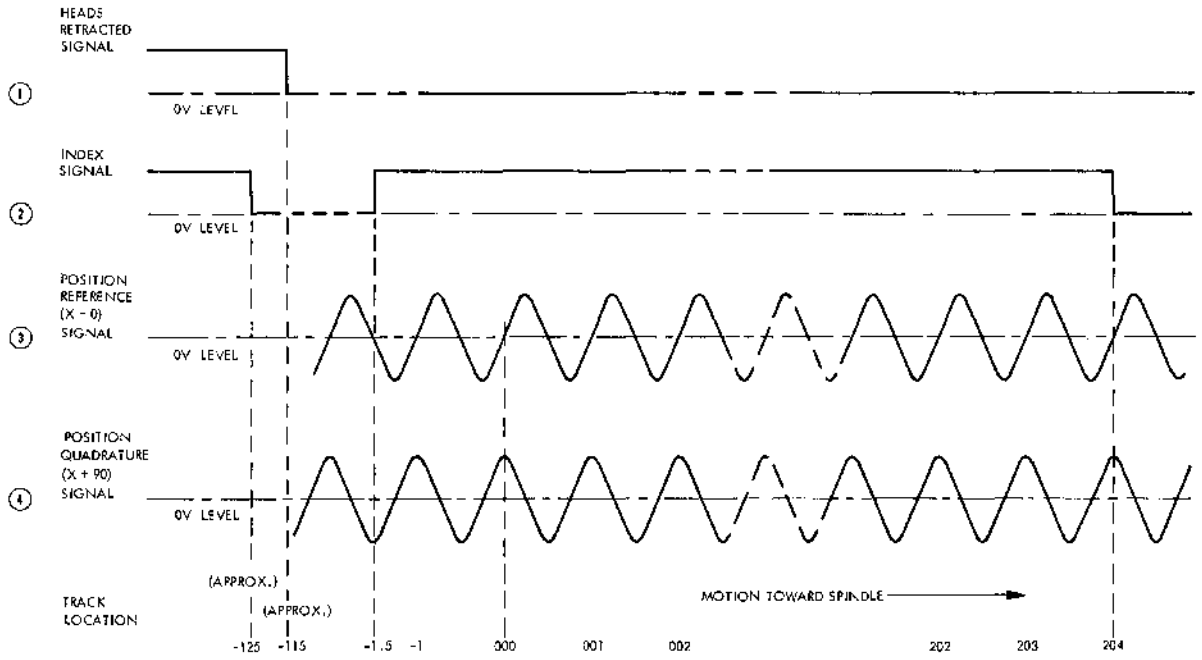


Figure 5-36. Position Transducer Output Signals

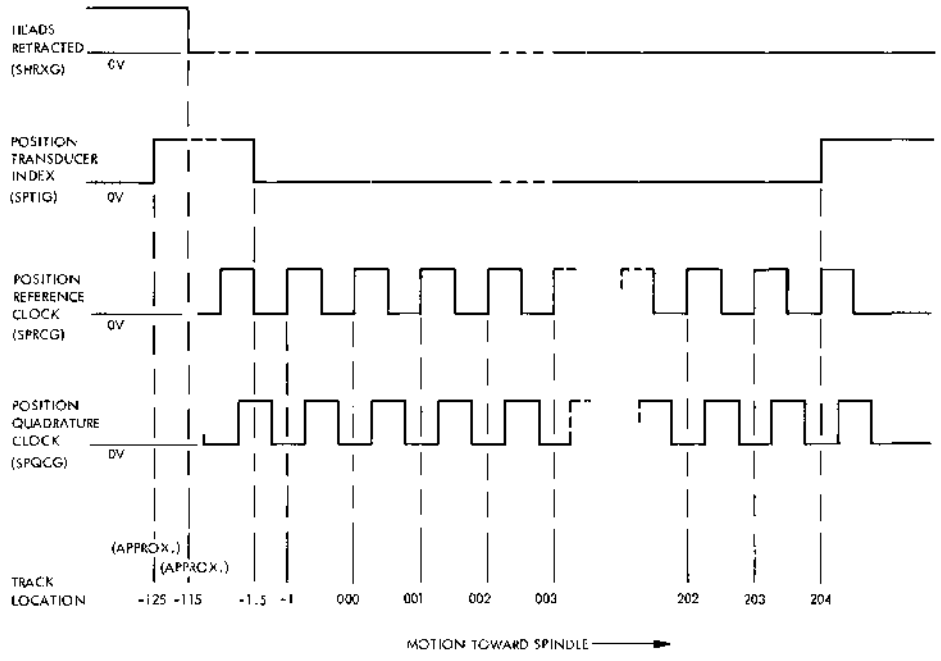


Figure 5-37. Position Transducer Signal Amplifier Outputs

When R69, the X + 0 gain potentiometer and R70, the balance potentiometer are properly adjusted, the output at TP20 should be 12v peak-to-peak. The X + 90 amplifier output at TP2 should be between 6v peak-to-peak and 12v peak-to-peak. The change in transition (from positive to negative and vice versa) at TP6 and TP3 should be from —6v +4v to +6v +4v, and vice versa when R98, the Index balance potentiometer, is properly adjusted.

The amplified Heads Retracted, Index, X + 0, X + 90 (see Figure 5-36) are then converted into their corresponding logic signals shown in Figure 5-37, namely Heads Retracted (SHRXG), Position Transducer Index (SPTIG), Position Reference Clock (SPRCG), and Position Quadrature Clock (SPQCG). These logic signals can be monitored at TP14, TP7, TP8, and TP13, respectively. Type 75107 dual line receivers (U11-A, U11-B, U10-A, U10-B) are used in the circuit as comparators for analog-to-digital conversion.

The R-C network in the feedback loop around comparators U11-A, U11-B, and U10-A, U10-B provides ac and dc hysteresis. An example of this network is C5, R76, R77, and R85 in the feedback path of U11-B (zone D12). These networks assure a single transition crossover detection of the analog input signals and provide good dc noise margins for analog inputs to the comparators.

5.5.2.4 Tachometer Amplifier

The Tachometer Amplifier shown on Schematic No. 102810, sheet 1 of 3, amplifies and inverts the velocity feedback signal from velocity transducer. This feedback signal is routed from pin 9 of J203 (zone A15) to the input of U14 (zone G14). U14 is a Type 741 operational amplifier which is used as a summing amplifier. Potentiometer R204 provides offset balance adjustments for U14.

When Reverse Slow Mode (NLRSM1) at pin 23 of J201 is low and Heads Retracted (SHRXG) at pin 28 of J202 is high (i.e., when the positioner servo is in the Reverse Slow Mode and the heads are retracted) Q11 (zone G14) turns on and the output of velocity transducer is grounded. This action removes the velocity feedback signal from the input of U14 and causes the output of U14 at TP16 to go to 0v.

5.5.2.5 Summing Amplifier

The Summing Amplifier U16 (zone G13) is shown on Schematic No. 102810, sheet 1 of 3. This amplifier sums the following reference, feedback or control signals of the positioner servo system.

(1) Velocity reference signal.

(2) Velocity feedback signal.

(3) (X + 0) position feedback signal.

(4) Offset signal.

(5) Track offset-plus and track offset-minus signal.

(6) Reverse slow velocity mode, forward slow velocity mode, and reverse slow and heads up velocity mode signal.

(7) External perturbation input signal.

(8) Temperature compensation and head alignment (200 tpi).

The positioner servo system normally operates in the Velocity Mode. Velocity feedback is provided continuously except when Reverse Slow Mode (NLRSM1) is low and Heads Retracted (SHRXG) is high, i.e., the servo is in the Reverse Slow Mode and the heads are retracted. At this point velocity feedback is cut off.

The Velocity Reference Enable signal (NLVREG) (pin 20 of J201) going low turns on Q3 (zone F15) and enables the velocity reference signal from TP9 into the summing junction of U16 (zone G13). The Position Mode signal (LPMXG) (pin 22 of J201) going high turns on Q13 (zone G13) enabling the X + 0 signal from U7 (zone F14) into the summing junction of U16. Thus, the servo is placed in the Position Mode.

The Forward Slow Mode signal (NLFSM1) low, and the Reverse Slow Mode signal (NLRSM1) high at pins 24 and 23 of J201, respectively, introduces a Forward Slow Mode signal (at TP10) into the summing junction of U16. This can be monitored at TP10 (zone D16). Conversely, NLFSM1 high and NLRSM1 low introduces a Reverse Slow Mode signal (monitored at TP10) into the summing amplifier.

Track Offset Plus (NLTOPG) and Track Offset Minus (NLTOMG) signals are introduced at the summing junction of U16 only when the servo is in the Position mode of operation. NLTOPG (pin 26 of J201) low and NLTOMG (pin 25 of J201) high introduces the Track Offset Plus signal; NLTOPG high and NLTOMG low introduces the Track Offset Minus signal into the summing junction of U16. These signals can be monitored at TP11 (zone E16). TP19 is provided to introduce an external perturbation signal into the summing junction. Potentiometer R22 (zone F16) is provided for nulling the X + 0 signal in reference to servo ground.

Referring to the summing junction of U16 it can be seen that the amplifier gains for any particular input signal is determined by the ratio of feedback resistor R60 (zone G12) and the resistor in series with the input signal. For example, the gain of the summing amplifier for any external input signal at TP19 (external perturbation signal) is R60 divided by R40. Zener diodes VR1 and VR2 (zone H13,12) are employed to limit the output of summing amplifier at TP17 to +6v. TP18 is the test point for servo ground. It should be noted that servo ground is depicted on the schematic as G(S) and logic ground is shown as G(L).

5.5.2.6 Positioner Power Amplifier

The Positioner Power Amplifier is shown on Schematic No. 102810, sheet 1 of 3 (zone G11). This amplifier is a linear feedback transconductance amplifier. It is referred to as a transconductance amplifier because its output current is proportional to the input voltage to the power amplifier.

The input to the power amplifier circuit is the output signal of the Summing Amplifier U16, which can be monitored at TP17. When the signal at TP17 is positive, Q16 turns on, causing Q19 to conduct which, when relay K1 (zone C10) is energized, connects —20v through R125, the positioner coil via J205 and R110 to ground. Conversely, when the signal at TP17 is negative, Q15 turns on, causing Q18 to conduct which, when relay K1 (zone C10) is energized, connects +20v through R114, the positioner coil via J205 and R110 to ground.

J205 (zone C7) connects the positioner coil to the Servo PCBA, thus establishing a path for current through the coil and corresponding series resistors. The voltage drop across R110, which is proportional to the current through R110, is fed back to the power preamplifier U17 (zone G11). U17 compares the input voltage and the feedback voltage which is proportional to the current through the coil, and turns off Q16 or Q15 and Q19 or Q18 when the output current at TP5 is equal to some constant of proportionality times the input voltage at TP17. Potentiometer R111 (zone F12) is provided to adjust and vary this transconductance of the power amplifier.

Q14 (zone H10) and Q17 (zone E10) limit the maximum output current of the amplifier. The voltage drop across R125 or R114 and the value of R122 and R124 or R115 and R113 determine the maximum value of current through Q19 or Q18, respectively.

Additional current limiting is provided by VR1 and VR2 which limit the voltage at TP17 to +6v, and the adjustment of R111. This value of current is normally adjusted lower than that provided by the limiting values of Q14 and Q17.

Resistors R118 and R119 (zone F10) provide an internal voltage feedback loop in the power amplifier stage. R-C networks C12 and R117, C13 and R120, C29 and R203 assures the high frequency stability of the power amplifier and eliminates high frequency oscillations.

5.5.2.7 Position Transducer Lamp Failure Detector

J203 pins 10 and 12 shown on Schematic No. 102810, sheet 1 of 3 (zone E12), connect the Position Transducer Lamp to the Servo PCBA. In normal operation, the lamp is driven from +10v with resistor R128 in series between the lamp and ground. When the lamp is operating normally, i.e., illuminated, the voltage drop across R128 turns on Q20. Thus, the Position Transducer Failure signal (SPTFG) at pin 18 of J202 is low. Should the lamp fail, Q20 is turned off and SPTFG goes high, thereby detecting the lamp failure.

5.5.2.8 Emergency Unload System

The Emergency Unload system, shown on Schematic No. 102810, sheet 1 of 3, consists of an Emergency Unload Relay (zone C9), a Relay Driver (zone E6), and an Emergency Unload Charging Network (zone A9). The Emergency Unload Enable signal (LEUEG) going low at J202 pin 32 turns on Q21 (zone E6), energizing the relay coil. The relay contacts are connected in such a manner that when the relay is energized the power amplifier is connected to the positioner coil. When relay is de-energized, the positioner coil is connected to the unload capacitor which in series with the parallel combination of R129 and R130.

J206 (zone A7) connects the unload capacitor to the Servo PCBA. When the Emergency Unload Relay is energized, the unload capacitor is charged to —10v with R131 limiting the charging current. When the relay de-energizes, the positioner coil is connected to the unload capacitor and the capacitor discharges via the parallel combination of R129 and R130 and the positioner coil, thus retracting the carriage and heads to the fully retracted position.

Capacitors C63, C64, C65, and C66 are provided across the contacts of the Emergency Unload Relay to suppress high frequency noise (RFI) generated while switching the positioner coil to either the Power Amplifier or the Unload Capacitor.

The Emergency Unload Relay Driver consists of Q21 which is connected as a transistor switch in series with the relay coil and resistor R136. Diode CR30, across the relay coil, is provided to protect transistor Q21 from large negative voltage surges when Q21 is turned on and off. In normal operation, LEUEG is low, emitter-base junction of Q21 is forward-biased, turning on Q21. If LEUEG goes high, or if LEUEG is low and the +5v drops to approximately 3.8v, Q21 turns off, de-energizing the relay, and retracting the carriage.

5.5.3 BRUSH MOTOR DRIVER

The circuitry of the Brush Motor Driver is shown on Schematic No. 102810, sheet 1 of 3 (zone H5,4). The ac brush motor is connected between 21v ac (peak) and the triac SCR1

(zone G3) via J214. Additionally, the 21v ac (peak), 60 Hz sine wave is clamped by diodes CR34 and CR35 (zone D5), then converted into a 60 Hz square wave digital output by comparator U21-A. This 60 Hz square wave digital output at pin 4 of U21-A is fed to the clock input of flip-flop U22-A (zone H4). The ac and dc hysteresis in the comparator circuit is provided by the network formed by C15, R146, R147, and R138.

The Brush Motor Enable signal (NLBMEG) going low at pin 22 of J202 (zone G6) resets flip-flop U22-A, making the Q output at pin 14 of the flip-flop low at the trailing edge of the next clock pulse. U22-A stays low as long as NLRMEG is low, since the set side of U22-A is disabled by inverted U20-A. The low Q output of U22-A causes transistors Q22 and Q23 to conduct. When Q23 is conducting, —10v is applied through R142, to the gate of the triac SCR1 (zone G3) causing it to fire. Firing SCR1 causes the brush motor, which is connected in series with SCR1 to turn on. The R-C series network formed by C14 and R145 limits the rate of rise in voltage across the triac.

Conversely, NLBMEG high causes the Q output of U22-A to go high at the trailing edge of the next clock pulse and stay high as long as NLBMEG is high. The high Q output of U22-A turns off Q22 and Q23, thus causing SCR1 to cease firing. The brush motor is then turned off.

5.5.4 AC MOTOR CONTROL CIRCUITS

AC Motor Speed Control circuits, shown on Schematic No. 102810, sheet 1 of 3 (zone E3), convert logic control signals, namely Increase Motor Speed (NLIMS1), Brake Cycle Enable (NLBCEG), and Drive Motor Enable (NLDMEG) at J202 pins 21, 23, and 20, respectively, to the appropriate control signal at TP22 which fires the triac control circuit on the AC Motor Control PCBA. This control signal and +5v is connected via J213 (zone E2) to the Motor Control PCBA.

The 21v ac (peak) 60 Hz sine wave (zone D5) is clamped by diodes CR34 and CR35 (zone D5), then converted into 60 Hz square wave digital signal by comparator U21-A. The ac and dc hysteresis in the comparator circuit is provided by the network formed by C15, R146, R147, and R138.

Referring to the 21v (peak) voltage at zone D5 of the schematic, it can be seen that the voltage is phase advanced by the network formed by C50, C51, C52, R208 and R209, then converted into a 60 Hz square wave digital signal at TP28 using comparator U25-B (zone C4).

The digital signal outputs of comparators U21-A and U25-B at TP23 and TP28 are fed into an Inverse Exclusive OR circuit formed by U20-C, U20-D, and U19-B, U19-C. The output signal at pin 8 of U19-C is a 120 Hz digital signal which is used as the switching signal for transistor switch U26-A.

The circuit consists of R212, R213, R214, C54, C55 and the transistor switch U26-A. This combination generates a sawtooth waveform at 120 Hz. When the signal at U26-A pin 1 and 2 is high, the transistor in the output state is cut off and capacitors C54 and C55 charge through R212, R213, and R214 to generate a ramp output at TP27. Conversely, when the signal at U26-A pin 1 and 2 goes low, the transistor in the output stage is turned on and discharges capacitors C54 and C55 through R214. Since the value of R214 is much smaller than the sum of R212 and R213, the discharge time constant is much smaller than the charge time constant. Thus, the 120 Hz sawtooth waveform is generated and can be monitored at TP27. Potentiometer R212 (zone C2) is used to adjust the peak-to-peak amplitude of the sawtooth waveform which is fed to pin 1 of comparator U25-A (zone C3) along with the output of operational amplifier U24 (zone F5).

The network associated with the operational amplifier U24 (zone F5) is an integrator circuit. When the Increase Motor Speed signal (NLIMS1) is high, the output at TP24 is a ramp function whose time constant is dependent upon the value of R215, R216, R217, C56, C57, C58, and C59. Diodes CR51, CR52, CR53, and CR54 limit the maximum positive voltage to approximately 2.0v. Diodes CR55, CR56, and resistor R218, limit the lower excursion of the voltage to approximately 0v. Thus, when NLIMS1 is low, the steady state value of the output voltage at TP24 is approximately 0v.

The dc voltage at TP24, which is proportional to the NLIMS1 pulses, and the reference 120 Hz sawtooth waveform from U26-A (zone C3) are compared in comparator U25-A (zone E3). Thus, the signal at TP22 is either high or low, depending on the error in voltage between these two signals.

The operation of the AC Motor Speed Control circuit during start-up, constant speed control, and brake cycle can be summarized briefly as follows. During start-up, NLIMS1 is low, NLBCEG is high, and NLDMEG is high at J202 (zone F6). The output of the integrator at TP24 is approximately 0v which, when compared with the reference 120 Hz sawtooth waveform, makes TP22 low. The low output of U25-A at TP22 triggers the triac on the Motor Control PCBA every cycle, with practically full cycle power to the motor, allowing the motor to come up to the speed.

When motor comes to correct speed, depending on the error in speed, NLIMS1 is either high or low and the voltage at TP24 is such that when compared with the reference sawtooth waveform at TP27 will generate a correction pulse at TP22. This correction pulse triggers the triac on Motor Control PCBA at a specific part of the ac waveform so that power is on for only part of the cycle. In other words, firing the triac at a specific time in one cycle of an ac waveform achieves the phase angle control of the ac waveform, thereby controlling the power to the motor.

During a stop sequence, NLDMEG is high. When NLBCEG is also high (i.e., brake cycle is not enabled), the output at U19-A pin 3 (zone E4) is low and the signal at TP22 is high all the time, and the triac is turned off. Hence, the power to the motor is cut off and the motor speed coasts down. When a brake cycle is enabled, NLBCEG is low, the signal at U19-A pin 3 is high. Also, the signal at TP28 (zone C4) is high all the time; hence signals at TP23 and U19-C pin 8 (zone C3) are 60 Hz square wave digital output. Consequently, the frequency of the reference sawtooth waveform at TP27 is 60 Hz. The low state of NLBCEG also makes U26-B pin 5 at ground potential. Since NLIMS1 is high, the voltage at TP24 is approximately 2v and U25-A pin 2 is approximately 0.7v. Thus the output at TP22 is a 60 Hz pulse train. Since the frequency of the trigger pulses at TP22 is 60 Hz as opposed to 120 Hz, the triac fires during only one-half of each cycle. The width of the pulse at TP22 controls the firing angle on the ac waveform, therefore braking power applied during each half cycle.

5.5.5 CARTRIDGE LOCK SOLENOID DRIVER

The Cartridge Lock Solenoid Driver circuit is shown on Schematic No. 102810, sheet 2 of 3 (zone B6). This circuit consists of a transistor switch connected in series with lock solenoids across +5v and —20v. J207 (zone B3) connects the coil of the lock solenoids to the Servo PCBA circuitry.

The Lock Cartridge Mechanism signal (LLCMG) low at J202 pin 33 causes Q43 and Q42 to turn on. This action applies approximately 24v across the solenoid coil which energizes the solenoids, pulling the plungers into the coil. When LLCMG is high, Q43 and Q42 are turned off, and the solenoid coil is de-energized, releasing the plungers.

5.5.6 POWER CLEAR CONTROL CIRCUIT

The Power Clear Control circuit is shown on Schematic No. 102810, sheet 2 of 3 (zone F4). This circuit detects fault conditions in the +5v, +20v, and —20v dc supplies and provides the Power Clear signal (SPCSA) to the Logic PCBA. J202 pin 30 (zone B8) connects the Plus 5 Volts signal (LP5VA) to the Power Clear Circuit at TP26. J202 pin 31 (zone E3) supplies the Power Clear signal (SPCSA) to Logic PCBA.

Figure 5-38 illustrates the waveforms associated with fault detection on the +5v line. The signals at various nodes in the circuit have been drawn on the functional timing diagram for explanation purposes and should be referred to in conjunction with Schematic 102810, sheet 2 of 3.

LP5VA high (plot 1) charges capacitor C28 (zone D4) through R181. Zener diode VR18 clamps and maintains the base of Q38 to +2.7v nominal (plot 2). Capacitor C27 (zone D5) is charged to approximately +2.1v nominal through diode CR49 and resistor network R179 and R195. The charging time constant of C27, R179 and R195 is much longer than that of C28 and R181. Consequently, the base of Q37 comes to the +2.7v level with a slow rise time (plot 3). When the base of Q37 is +2.7v nominal, transistor Q37 turns on and lowers the voltage on the base of Q36 to less than +5v, turning on Q36. The collector of Q36 will be at approximately +4.8v nominal. Resistor R188 provides positive feedback to the base of Q37, hence, a clean, fast edge of the signal is obtained at the point of transition (plot 4) and at J202 pin 31 (SPCSA) (plot 5).

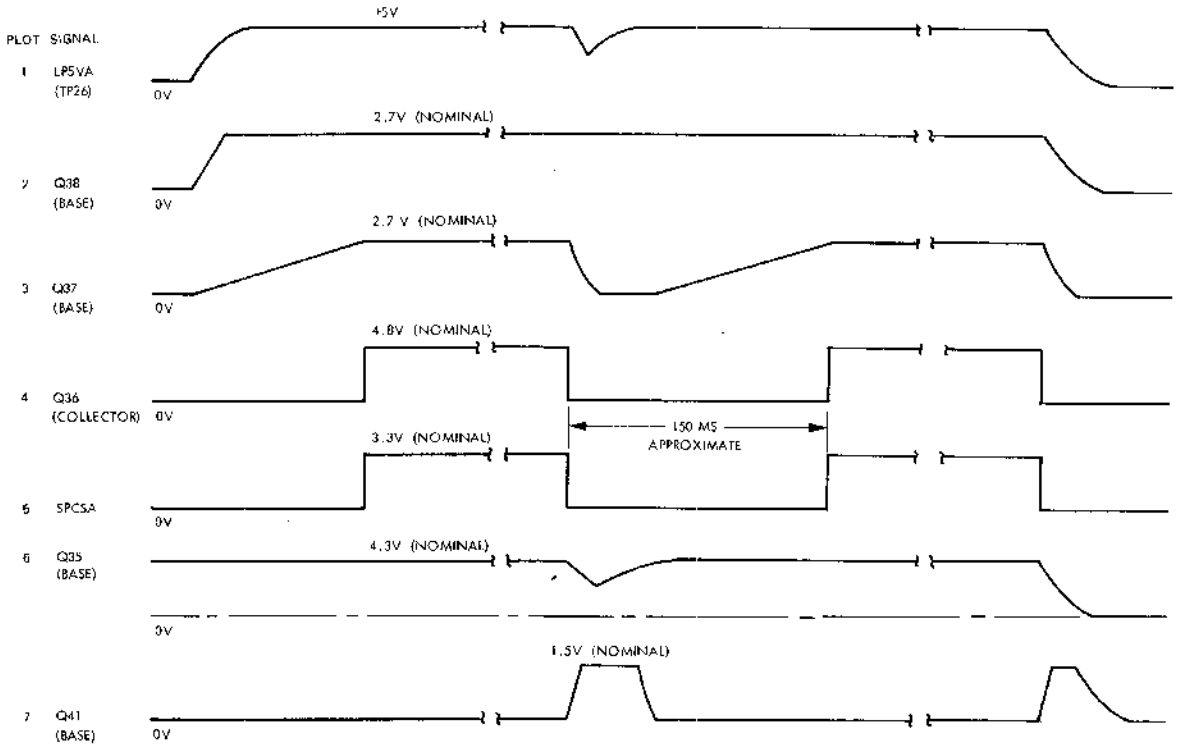


Figure 5-38. Fault Detection Waveforms

The amplitude of SPCSA is approximately 3.3v when high since there is a 150-ohm resistor inserted on the Logic PCBA between the SPCSA signal line and ground.

In the case where the +5v at TP26 sags momentarily and correspondingly the voltage at the base of Q37 goes below 2.7v such that Q37 is turned off, the following actions occur. Q36 turns off instantaneously and R188 provides positive feedback to achieve the sharp transition at the collector of Q36. Since Q36 is off, the collector of Q36 is at ground potential and capacitor C26 is charged from the charge of C25. The difference in potential at the base of Q35 turns on Q35 which turns on Q41. Capacitor C27 discharges through R193. The discharge and charge time constants associated with C25 and C26 are such that transistor Q35 is turned on for a longer time than the time required to discharge C27 through R193. Plots 6 and 7 of Figure 5-38 describe typical waveforms of Q35 base and Q41 base voltages, respectively. SPCSA will also be low since the collector of Q36 is at ground potential.

Once the base of Q35 recovers to the same potential as its emitter (4.3v), Q41 is turned off and C27 charges through the network formed by R179 and R195 until the base of Q37 is at +2.7v. This, in turn, turns on Q37 and Q36 and collector of Q36 goes to +4.8v and SPCSA goes high (plots 3, 4, 5). The approximate time taken for SPCSA to go high after it has been in a low state is 150 msec.

The following action occurs when LP5VA at TP26 goes low permanently from its high state. The collector of Q36 goes to ground potential and SPCSA goes low. The signals at base of Q38, Q37, Q35, and Q41 are shown in plots 2, 3, 6, 7, respectively.

Similarly, if the +20v goes below approximately +13v nominal, Q34 turns off and the cathode of CR48 goes to ground potential. This, in turn, causes Q37 to turn off and the sequence of events that occurs is identical to +5v drop-off previously described. When the +20v is approximately +16v or higher, Q34 turns on and the cathode of CR48 is at approximately 5.4v (if the +20v line is at +20v) which reverse-biases CR48, and the base of Q37 gets charged to 2.7v again to turn on Q37.

Similarly, if the —20v is maintained at its nominal potential, Q40 is on and the base of Q39 is at approximately —2v which turns off Q39. The cathode of CR48 is at +5.4v, which reverse-biases CR48 and hence a normal charging sequence of C27 occurs until Q37 turns on. When the —20v goes above —13v, Q40 turns off and Q39 turns on. CR48 cathode goes to ground potential and the sequence of events that occur is identical to +5v drop-off previously described.

It should also be noted that resistors R188 and R190 provide hysteresis in the circuit so that the voltage (+5v, +20v, or —20v) at which SPCSA goes high is always slightly higher than when it goes low.

5.6 READ/WRITE PCBA

The following paragraphs describe the Read/Write C PCBA installed in D3000 Series Disk Drives. Refer to Schematic No. 103750 and Assembly No. 103751.

The PCBA is approximately 9.75 inches long by 6.5 inches wide. Figure 5-39 illustrates the placement of each connector, test point, and adjustable component on the PCBA. J305 connects via a mating plug and 3M flat cable to the Logic PCBA. J304 is a molex connector which connects via a mating plug and standard cabling to the Logic PCBA. J300, J301, J302, and J303 connect via shielded cabling to the magnetic read/write heads.

The Read/Write PCBA description is divided into the following elements.

(1) Head Selction Matrix and Select Switches
(2) Write and Erase Driver
(3) Read Switch
(4) Read Preamplifier
(5) Filter
(6) Variable Gain Amplifier
(7) Peak Detector, Squarer, and Pulse Former
(8) Data Decoder
(9) Emergency Condition Detection

A block diagram of the Read/Write electronics is shown in Figure 4-4 and should be referred to in conjunction with Schematic No. 103750 and the electrical description described in the following paragraphs.

5.6.1 HEAD SELECTION MATRIX AND SELECT AMPLIFIER

Head selection is accomplished using a conventional diode matrix in conjunction with center-tapped heads. Each head is comprised of a balanced Read/Write (R/W) center-tapped winding and a separate erase winding which has one end connected to the R/W center tap. Referring to Schematic No. 103750, zone E14, 13, and 12, four heads are shown connected to J300, J301, J302, and J303. Three diodes are associated with each head: two diodes (CR28 and CR30 for the J300 head) connected to the balanced R/W bus and the third diode (CR29) is connected to the erase bus.

The four head center taps are pulled to —10v by resistors R69, R72, R76, and R79 when the associated head is not selected. When selected, the appropriate head center tap is pulled positive by the corresponding head select switches (Q9, Q10, Q11, and Q12).

During a Write operation, +10v is applied to the emitters of the head select switches via Q1 when tracks 0 through 127 are selected. This voltage is decreased to approximately +7.0v via Q2 and resistor R5 when tracks 128 through 202 are selected. The appropriate selection is performed as follows: Write Mode (NLWMXG) and Erase Current Enable (NLECEG) signals are inverted by U13-A and U18-E, ORed by U15-D and fed to AND gates U15-A and U15-B. The Demand Address Most Significant Bit (128) signal (LDAMG) is fed directly to U15-A and inverted to U15-B. The outputs of U15-A and U15-B are fed via open-collector drivers U11-A and U11-B to Q1 and Q2. This system ensures that write current is appropriately reduced when writing on inner tracks where the flying height of the head is reduced.

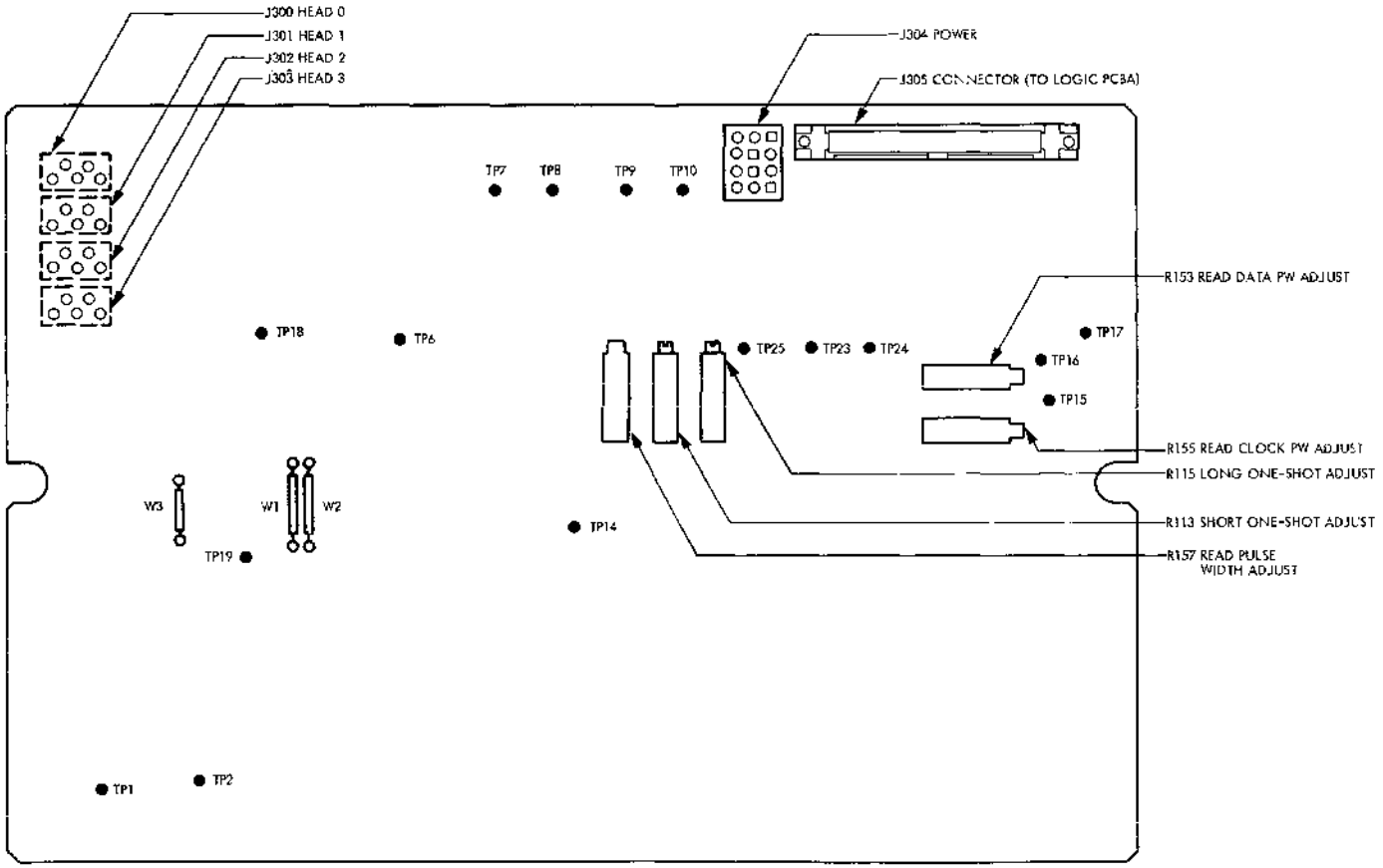


Figure 5-39. Read/Write PCBA, Test Point and Connector Placement

During a Read operation, the head select switches are fed from approximately 0v via Q3. The NOT (Write Mode or Erase Enable) signal from U18-F is used to drive the open-collector driver U12-C which in turn is fed to the emitter of Q3.

5.6.2 WRITE AND ERASE DRIVERS

During a Write operation, the Write Mode (NLWMXG) signal is inverted and, when true, enables J-K flip-flop U9 (zone F17). Inverters U13-F and U13-E provide an extra delay which ensures that flip-flop U9 is always enabled in the reset state. Write Double Frequency pulses (NLWDFT) are received and fed to the clock input of U9. These clock pulses toggle the flip-flop for every pulse received as required by the double-frequency code used.

The Q and Q outputs of U9 are fed to two identical pre-drivers Q13 and Q15. The outputs of Q13 and Q15 drive the write drivers Q14 and Q16 whose emitters are returned to approximately —9v. When Q14 or Q16 conduct, write current flows in one half of the selected head. This current is defined by resistor R65 or R66 (as appropriate), the —10v supply, and the center tap voltage (+10v or +7v as required). This yields typical write currents of 35 ma peak for tracks 0 through 127 and 29 ma for tracks 128 through 202. The base drive circuits of all four transistors (Q13, Q15, and Q14, Q16) have anti-saturation diodes CR13, CR14, CR15, CR16, CR18, CR21, CR19, CR22 incorporated. Diodes CR26 and CR27 are used to isolate the head bus from the write circuitry during a Read operation, thus reducing noise injection. CR23 and CR24 prevent the inductive kickback of the magnetic head windings from exceeding +10v. Capacitors C8 and C9 are *speed up* capacitors which decrease write current rise time.

The erase driver is separately enabled by the Erase Current Enable (NLECEG) signal since the erase current can be left on for a longer time than the write current. When NLECEG is low, Q17 (zone D16) is turned on via inverters U18-E and U11-E. This causes the base of Q18 to be switched to approximately —4.3v which enables the current source components Q18 and R59. The erase current is typically 40 ma, independent of the status of Q1 and Q2.

The return path for both write and erase drivers is via the emitter base junction of Q19 through Q22, and then to —10v via the S10SS line which is returned to —10v through the emergency unload relay. Q22 is only enabled via Q21 and Q20 when the Power Clear Signal (SPCSA) is at a high (positive) level. Q19 is used as a write current detector and is detailed in Paragraph 5.6.9.

5.6.3 READ SWITCH

The diode switch CR46, CR51 (zone F10, 11), CR48 and CR52 (zone E10, 11) is used to isolate the head bus from the read amplifier during Write operations to prevent overload of the read preamplifier.

During a Write operation, Q8 (zone H14) is turned on via open-collector driver U12-D. This pulls the junction of R83 and R84 (zone E11) to +10v cutting off all four diodes. This follows since the head bus voltage cannot exceed +10v and the anode voltage of CR51 and CR52 cannot exceed +0.7v due to CR55 and CR56.

During a Read operation, Q8 is turned off and the junction of R83 and R86 is returned to approvimately —6v via R85. Thus, approximately 1 ma flows through R83 (and R84) and approximately 0.5 ma is supplied by R88 (and R86). Thus, a current of 0.5 ma flows through each of the diodes CR46, CR51, CR48, and CR52 enabling the read switch.

5.6.4 READ PREAMPLIFIER

The balanced read signal from the head bus is terminated by R89 or L7, C11 and R90 or L8, C12 (zone E10) and fed to the type 733 differential video amplifier U1. When used in this configuration the amplifier has a wide bandwidth and a balanced-to-single-ended output gain of approximately 50 for 100 tpi or 150 for 200 tpi.

5.6.5 FILTER

The single-ended preamplifier output of video amplifier U1 is fed via matching resistor R100 to a linear phase filter. This filter has sharp cut-off characteristics combined with a group delay characteristic which is constant over the signal frequency band. The insertion loss of this filter is 0.5.

5.6.6 VARIABLE GAIN AMPLIFIER

The Variable Gain Amplifier consists of transistor amplifier Q27 (zone E8) employing emitter feedback to control its gain. It can be seen that the emitter resistance of this amplifier can be one of two values: 680 ohms (R106) when Q26 is not conducting, and 220 ohms (R106 in parallel with R104) when Q26 is conducting. Normally, Q26 is conducting and the gain of the stage is approximately

$$\frac{1800}{200} \simeq 8\Omega$$

However, when both margin test signals NLTOMG and NLTOPG are low, the output of U15-C goes high and Q26 ceases to conduct. Under these conditions the state again becomes approximately

$$\frac{1800}{680} \simeq 2.6\Omega$$

which gives a 3:1 reduction in gain. The appropriate dc base voltage (approximately 4.4v) for correct operation of Q27 is supplied via the voltage divider network R96, R101.

5.6.7 PEAK DETECTOR, SQUARER, AND PULSE FORMER

The signal from the variable gain amplifier stage is fed via emitter follower Q28 (zone E7) to the feedback differentiator stage U2 which utilizes a type 715 operational amplifier. C22 and R41 are the differentiator elements; R110 and C51 are used to limit the high frequency response while diodes CR11 and CR12 provide clipping action which allows the stage to operate over a large dynamic range. C24 is used for stabilization and CR69 prevents latch up.

For 100 tpi operation the stage gain is designed to be approximately 9 at all-zeros frequency at 1500 rpm, and 18 at all-ones frequency at 1500 rpm. For higher speed versions of 100 tpi and for all 200 tpi operation, the gain is appropriately scaled. The system is designed so that the minimum all-ones frequency gain to the peak detector output is 1800 under normal conditions at 1500 rpm. Thus, for a head output of 0.5 mv peak-to-peak at the all-ones frequency the peak detector output is approximately 0.9v peak-to-peak.

The output of the peak detector is fed to U30 where it is amplified and clipped. U30 also provides a pulse output for each zero crossing of the input signal. The width of the output pulse is proportional to R157, R156, and C74. R157 is employed to adjust the output pulse width to 40 to 45 nanoseconds.

5.6.8 DATA DECODER CIRCUITRY

The Data Decoder circuitry acts upon the pulse former output to generate separated data and clock signals. A functional discussion of this circuit is contained in Paragraph 4.6.3.6.

The RPN waveform consists of clock pulses which occur every 640 nanoseconds (1500 rpm and 2200 bpi) interspersed with a pulse for every one bit recovered.

RPN is gated through U27-C and its leading edge is used to clock the appropriate one-shot to set the ones window. If the preceding clock period had a one interspersed, then the short one-shot (U7-B) is used to form the ones window via U27-B. If the preceding clock period did not contain a one, then the long one-shot (U7-A) is used to form the ones window via U27-B. U28-B inverts the ones window to form the zeros or clock window. This signal is applied to U27-C and gates RPN through R113 and R115. This is used to set the period for the short and long one-shots.

If a RPN (data) occurs during the time that the ones window is high, it will be gated through U27-A. This pulse sets U8-A which results in the short one-shot determining the next one-shot period.

The output of U27-A and U27-C are fed back to the inputs of U27-B and U28-B, respectively, and act as pulse stretchers. The outputs are also applied to U29-A and U29-B where the decoding pulse is lengthened prior to sending down interface lines. The output of U29-A is lengthened by R153 but is also proportional to R152 and C76. The output of U29-B is lengthened by R155 but is also proportional to R154 and C77.

5.6.9 EMERGENCY CONDITION DETECTION

Two conditions are detected by the Emergency Condition Detector circuitry and cause the Write Emergency Condition (RWECG) signal to go high. The NRWECG signal is fed to the Logic PCBA via J305 pin 30 (zone C6) where it is used to initiate an emergency unload sequence. The emergency unload sequence causes the unit to go Not Ready, thereby turning off write current in less than 1 sec. The emergency unload sequence also causes the emergency unload relay to operate, thereby interrupting the S10SS supply. Interruption of this supply precludes any write current flowing in the heads.

One emergency condition detected is the condition when more than one head is selected while the disk drive is in a Write mode of operation. When a head is selected in the Write condition (e.g., the head connected to J300) the appropriate center tap is pulled to approximately 10v for tracks 0 through 127 and 7v for tracks 128 through 202 (Paragraph 5.6.1).

This voltage is clipped by CR31 (zone E14) to +0.7v and fed via R71 and diode CR32 to the inverting input of the type 741 operational amplifier U4 (zone D11) which is used as a comparator. A precision current drain for this circuit is established via R75 to —10v.

The non-inverting input of U4 is set at a nominal voltage of —4.5v such that when one head is selected the inverting input is more negative than —4.5v and the output of U4 is high. When two heads are selected (e.g., the heads connected to J300 and J301) additional current is fed via R74 and CR37 to the inverting input of U4 raising this point above —4.5v and causing the output of U4 to switch to a negative state. This output is fed via R134 and CR53 to one input of the low active OR gate U26-A (zone B15) causing RWECG to go high at J305 pin 30 (zone C6). R138 and CR58 prevent the input to U26-A from going more negative than —0.7v.

The second emergency condition detected by this circuitry is when write current is on during a Read operation. It is important to note that during a Read operation no write current or erase current should flow.

Write and Erase current must flow through R63 (zone D15) and the emitter base diode of Q19. If a total current in excess of approximately 0.7 ma flows, then the voltage across R63 (1K ohm) will exceed 0.7v causing Q19 to turn on. Q19 conducting causes the input to inverter U26-C (zone A15) to go low which, in turn, enables one input of NAND gate U26-B.

Recall that during a Read Mode, the Write Mode (NLWMXG) and Erase Current Enable (NLECEG) signals are high, thus the output of U22-C (zone B17) is low.

In the Read Mode the outputs of inverter U22-D and non-inverting driver U25 are both high, enabling the other two inputs of NAND gate U26-B. Thus, the output of OR gate U26-A goes high and the RWECG waveform goes high at J305 pin 30 (zone C6). Resistor R143 and capacitor C63 are used to provide masking delays to avoid false indications during Read/Write switching.

During a Write operation, transistor Q19 is on but one or both of the NLECEG and NLWMXG waveform are low. Therefore, the output of U22-C is high, inhibiting gate U26-B and hence preventing RWECG from going high.

5.7 LOGIC PCBA

The following paragraphs describe the Logic PCBA installed in the D3000 Series Disk Drive with Diablo compatible logic interface. Refer to Schematic No. 103704 and Assembly No. 103705.

The Logic PCBA is approximately 15.5 inches long by 10.75 inches high. Figure 5-40 illustrates the placement of each connector, test point, and adjustable component on this PCBA. J104 and J105 connect via 3M flat cable to the Servo PCBA; J108, J109, J110, J111, and J112 are molex connectors which are also connected to the Servo PCBA. J103 mates to the Read/Write PCBA via 3M flat cable. J101 provides for connection between the D3000 and a controller or another disk drive. J102 provides connection to the PERTEC I/O terminator PCBA or another disk drive.

For ease of understanding, the description of this PCBA is addressed to Schematic No. 103704 on a sheet-by-sheet basis beginning with sheet 2.

5.7.1 SHEET 2 (SCHEMATIC NO. 103704)

Sheet 2 of the Logic PCBA schematic contains the Start/Stop Control Logic portion of the disk drive function control logic. Refer to the functional description and simplified block diagram contained in Paragraph 4.7 in conjunction with this discussion.

The crystal oscillator is comprised of transistor amplifiers Q1 and Q2 (zone C14) in conjunction with the 10 MHz crystal Y1. The crystal is connected in the feedback path of the oscillator and is operated in a series resonant mode. The output signal of the oscillator is developed across R13 and is fed through inverter U186, which acts as a buffer, to the clock countdown circuitry. The output of the oscillator can be monitored at TP13. The clock countdown circuitry consists of cascaded 4-bit binary counters operating in a binary countdown mode. The first counter of the countdown chain is a synchronous counter, the remainder are ripple counters. The clock signals derived from the clock countdown chain are square-waves which are fed to various parts of the logic to provide the primary timing.

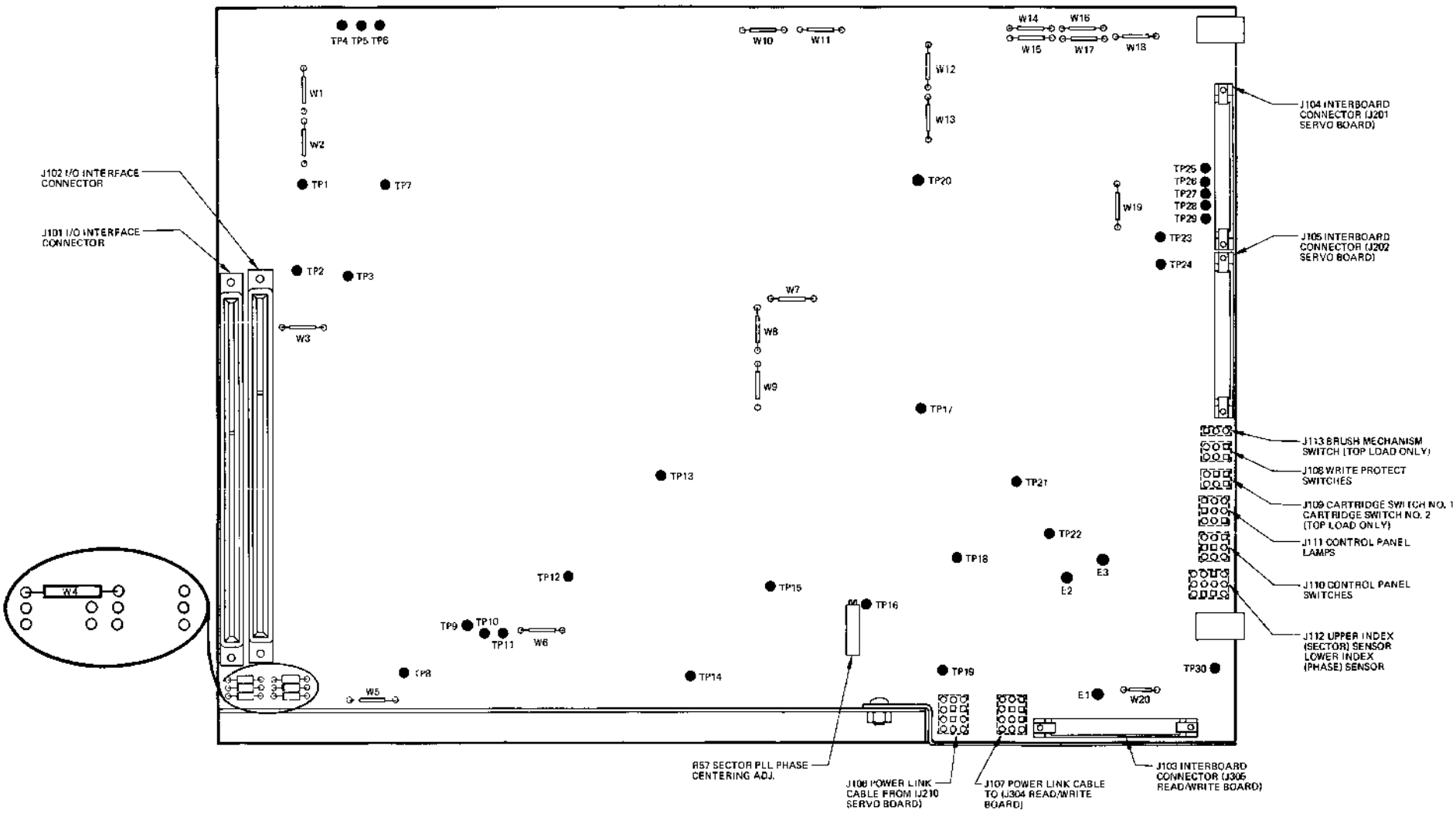


Figure 5-40. Logic PCBA, Test Point and Connector Placement

One of the clock signals is used in the spindle speed control logic to determine the speed of the disk and functions as the primary time reference for the spindle speed control. Another of the clock signals, LC09F (U245 zone B10) is gated by the Sequence Timing Pulse Flip-Flop (U345 zone F5) output pulse at AND gate U284-13 (zone D9) to produce the gated clock to the Purge Cycle Flip-Flop (U344 zone G12) and the Load Heads Flip-Flop (U344 zone G10). The frequency and the period of each one of the clock signals is listed in Table 5-1. Referring to Table 5-1, it can be seen that each successive clock signal is one-half the frequency and twice the period of the previous signal in the clock countdown.

NOTE

Generated clock signals are listed in Table 5-1 to aid in troubleshooting; all of these signals are not used in the D3000.

The major states of the Start/Stop Control Logic are defined by the Run Flip-Flop (U364 zone H14), the End Of Run Flip-Flop (U364 zone H13), the Purge Cycle Flip-Flop (U344 zone H12), the Load Heads Flip-Flop (U344 zone H10), the Sequence Control Flip-Flop (U384 zone H9), the Brake Cycle Enable Flip-Flop (U384 zone H7), the Emergency Unload Flip-Flop (U345 zone E13), and the Disk Rotation Detector Counter (U283 zone D14).

A delay counter is mechanized by taking the last of the Clock Countdown LC20F (pin 11 U285 zone B7) and applying it to the input of two 4-bit binary counters (U305, U325 zone

Table 5-1
Clock Countdown

Clock No.	Frequency (in Hz)	Period
01	5000000.0	200 nsec
02	2500000.0	400 nsec
03	1250000.0	800 nsec
04	625000.0	1.6 μsec
05	312500.0	3.2 μsec
06	156250.0	6.4 μsec
07	78125.0	12.8 μsec
08	39062.5	25.6 μsec
09	19531.25	51.2 μsec
10	9765.625	102.4 μsec
11	4882.8125	204.8 μsec
12	2441.40625	409.6 μsec
13	1220.703125	819.2 μsec
14	610.3515625	1.6384 msec
15	305.17578125	3.2768 msec
16	152.5878906250	6.5536 msec
17	76.2939453125	13.1072 msec
18	38.14697265625	26.2144 msec
19	19.073486328125	52.4288 msec
20	9.536743164062 5	104.8576 msec

C8). The Delay Counter, in conjunction with the Sequence Timing Pulse Flip-Flop (U345 zone F5), and the appropriate combinational logic generate timing sequence pulses at specific time intervals according to the states of the logic. The counter is controlled by resetting the counter with either a pulse or a level change via OR gate U326-6 (zone F6). This gate combines the Sequence Timing Pulse (LSTPF) with the output of combinational logic U385-3 (NLNRSG) and U385-8 (NLSNHG) and applies this gated signal to the Delay Counter.

NOTE

External commands, either directly or in conjunction with the combination of the external commands and the present states, may affect the next state of the Start/Stop Control Logic. Refer to the block diagram of the digital sequential machine [Figure 4-8] used to mechanize Start/Stop Control Logic.

The logic is initialized during power ON and power OFF events by the Power Clear Signal (SPCSA) from the Servo PCBA at J105 pin 31 (zone E17). SPCSA is an analog signal which is converted into logic levels by Schmitt trigger U405 (zone E16). It should be noted that when the output of U405 pin 8 is high, power to the machine is either off or below the minimum acceptable value as determined by the Power Clear circuit on the Servo PCBA.

SPCSA clears the Disk Rotation Detector Counter, pre-sets the Emergency Unload Flip-Flop, clears the End Of Run Flip-Flop, clears the Run/Stop Pulse Register, the Run Flip-Flop, and the Sequence Timing Pulse Flip-Flop. The Power Clear Signal (SPCSA) assures that the logic is properly initialized during power turn-on and that the logic assumes the correct states in the event of power removal.

Commands which can cause the Start/Stop Control to execute either a start sequence or a stop sequence are obtained from the RUN/STOP control signal (CRSSS) connected to J110, pins 1, 2, and 3 (zone H18). A cross-coupled inverter latch U447 is used to *clean up* the input signal and eliminate the problem of switch contact bounce. The output of this latch is ORed with the Start/Stop Disk Drive (ISSDR) line from the I/O interface at U49. The output of U49, pin 3, is the input to the Run/Stop Pulse Register (U347 zone G17). A level change occurring either from an assertion of the Start/Stop Disk Drive line or from actuation of the RUN/STOP control is edge-detected by the Run/Stop Pulse Register. The Run/Stop Pulse Register is a shift-register type of edge detector whose purpose is to produce a pulse having a period of one clock time upon detection of the leading edge of a level change propagating through the register.

The one-clock period pulse output from U347 is the Run Switch Pulse (LRPXG) used for clocking the Run Flip-Flop (U364 zone H14). In addition, the Run/Stop Pulse Register generates the Start Drive Motor (NLSDMG) signal if, and only if, the Run Flip-Flop is one-set as a result of the level change propagating through the Run/Stop Pulse Register. This will be the case when the Run Flip-Flop has been properly enabled and is one-set to commence a start sequence. The Start Drive Motor pulse initializes flip-flops in the Spindle Speed Control logic on sheet 3 of the schematic.

The Delay Counter Decode logic (zone E7) is enabled by the outputs of the Sequence Control Logic as well as the Sequence Control Flip-Flop. Delay Counter Decode decodes specific values of delay by ANDing various bits from the Delay Counter according to the states presented by the Sequence Control Logic and the Sequence Control Flip-Flop.

The Sequence Timing Pulse Flip-Flop (U345 zone E5) is used to generate a pulse with a period of one clock interval when a high level is applied to the J input from the Delay Counter Decode logic.

The sequence timing pulse is used to define the timing of events during the start sequence and the stop sequence. It also tests the states of certain signals during the start sequence for the purpose of determining if an emergency condition exists.

The timing of two of the flip-flops is accomplished by using the sequence timing pulse to gate the clock to the Load Heads Flip-Flop and the Purge Cycle Flip-Flop. This is done to ensure clocking these flip-flops only at the end of specific delay intervals.

The Disk Rotation Detector Counter is used to detect disk rotation for purposes of interlocking and to determine the duration of the brake cycle. Additionally, the Disk Rotation Detector Counter provides a time delay at the end of the power clear condition.

The Sequence Control Logic (zone E12) is employed to decode the states of the Purge Cycle Flip-Flop and the Load Heads Flip-Flop. This provides signals for steering the start sequence and for initializing the position monitor circuit in the Position Control Logic.

The signal outputs from the Sequence Control Logic are also used to enable the tests in the Emergency Unload Logic.

The Run Flip-Flop will be zero-set by any Run Switch Pulse (LRPXG) if it is already one-set. If the Run Flip-Flop is previously zero-set, then LRPXG will one-set the flip-flop only if proper interlocking has occurred. Detection that the disk cartridge is correctly inserted interlocks the Run Flip-Flop. Gate U264-12 (zone F15) ORs the Cartridge Correctly Inserted (LCCIG) signal with the Clear Or Unload (NLCOUG) signal to clear the Run Flip-Flop if either or both of these signals are low.

Cartridge Correctly Inserted (LCCIG) signal is developed from the states of the cartridge inserted switches. The Clear Or Unload (NLCOUG) signal is the OR condition of the Power Clear Signal (SPCSA) and the output of the Emergency Unload Logic.

Determination of correct cartridge insertion is accomplished by two switches in top load models and by a single switch in front load models. These switches connect to J109 (zone F18) and operate the Cartridge Inserted Latches. The output of the Cartridge Inserted Latches is ANDed by U445-4 (zone F17) to generate the LCCIG signal. The cartridge inserted latches are cross-coupled inverters in the same configuration as those used at the input to the Run/Stop Pulse Register. In front load models, where only one switch is used, one of the latches is held permanently in the correct state by a jumper at P109.

In top load models the position of the brush cleaning mechanism cam, which drives the brush cleaning arms, is sensed by a switch to determine the parked position of the brushes. The outputs of the brushes parked switch are connected to J113 (zone D18) and operate the Brushes Parked Latch (U446-10 and U446-12) producing the Brushes Parked Switch (LBPSL) signal. U445-1 (zone 4) provides logic which causes the cleaning brushes in a top load model to park automatically after the Purge Cycle is terminated.

The Run condition is defined as any time that the disk is rotating and a stop sequence is not in progress, i.e., Run Flip-Flop one-set. The Run Flip-Flop cannot be one-set by a Run Switch Pulse signal unless the J input to the flip-flop is at a logic one level. The signal which enables the Run Flip-Flop J input is NLLCMG which is the result of combinational

logic containing the remaining interlocking signals. These interlocking signals are: Heads Retracted (SHRXG) which prevents entering a run condition unless the heads are retracted; Brushes Parked Switch signal (LBPSL) which prevents entering a run condition unless the cleaning brushes on a top load model are correctly parked; Not Disk Rotating (NLDRXG), from the Disk Rotation Detector Counter, which prevents entering a run condition unless the disk is stationary; Not Brake Cycle (NLBCFF), from the Brake Cycle Flip-Flop, which prevents entering a run condition if a brake cycle is in progress; and, finally, the logic condition resulting from the combination of the state of the Sequence Control Flip-Flop (LSCFF) and the Run Flip-Flop (LRFFF) which is combined in U385-3 (zone E6) to generate NLNRSG. This signal is used in the interlocking control portion of the logic. The use of this arrangement prevents re-entry into a run condition (Run Flip-Flop one-set) unless a correct stop sequence has been executed.

As previously mentioned, there are two basic sequences executed by the Start/Stop Control Logic; the start sequence, and the stop sequence.

A start sequence begins when the Run Flip-Flop is one-set and progresses through the one-setting of the Purge Cycle Flip-Flop (U344 zone G12), the one-setting of the Load Heads Flip-Flop (U344 zone G10), and finally, the one-setting of the Sequence Control Flip-Flop (U384 zone G9). One-setting the Run Flip-Flop defines the run condition. The Purge Cycle Flip-Flop then defines that portion of the start sequence when the disk speed is increased to 10 percent above the nominal speed. This is done to increase the air flow across the platter(s) prior to loading the heads. In addition, it initiates the brush cleaning cycle in top load models. The Load Heads Flip-Flop is used to define that state when the heads are loaded onto the disk(s). The Sequence Control Flip-Flop defines the state which indicates the successful completion of a start sequence, or the beginning of a stop sequence.

A stop sequence begins with zero-setting the Run Flip-Flop. This causes one-setting the End Of Run Flip-Flop which, in turn, causes the Sequence Control Flip-Flop to be pre-set in the event that it has not yet been one-set. To complete the stop sequence, the Brake Cycle Enable Flip-Flop is one-set at the same time that the Sequence Control Flip-Flop is zero-set. The stop sequence ends with zero-setting the Brake Cycle Enable Flip-Flop. The End Of Run Flip-Flop is used to detect the high-to-low transition of the Run Flip-Flop when the Run Flip-Flop is zero-set. The End Of Run Flip-Flop, therefore, acts as an edge detector which is used to force a pre-set condition to the Sequence Control Flip-Flop. This guarantees correct entry into the stop sequence. The Brake Cycle Enable Flip-Flop is then one-set to define that portion of time when braking current is supplied to the disk motor to stop the disk.

The Emergency Unload Flip-Flop (U345 zone E13) defines the condition which causes the emergency unload relay to disconnect the positioner servo from the positioner coil and connect the positioner coil to the emergency unload network. This is done when executing an emergency unload, or for preventing the connection of the positioner coil to the servo electronics, prior to the time when the disk drive logic is capable of detecting certain positioner electronic faults.

The Emergency Unload Logic is comprised of three basic parts: U266 (zone D16) which ANDs the Sequence Timing Pulse Flip-Flop with outputs from the Sequence Control Logic and the specific signals to be tested for emergency condition indications during a start sequence. The signals tested by U266 logic are NLBPSL, NLPMXG, and LSOTF. The ANDing of these signals generates, respectively, Brush Parking Error (NLBPEG), Head Loading Error (NLHLEG), and Disk Starting Fault (NLDSFG).

Position Transducer Failure (SPTFG) from the Servo PCBA is ORed with Write Emergency Condition (RWECG) from the Read/Write PCBA at gate U327 (zone C17) to produce NLEOFG which is Emergency Or Failure condition.

These signals plus Position Limit Error (NLPLEG), Disk Speed Error (NLDSEG), and Seek Time Error (NLSTEG) from other portions of the logic are combined in OR gate U306 (zone C15) to produce Any Emergency (LAEXG). Assertion of LAEXG by one or more of the emergency situations detected by the Emergency Unload Logic results in clearing the Run Flip-Flop and aborting the run condition. This pre-sets the Emergency Unload Flip-Flop (U345 zone E13) causing emergency retraction of the heads.

Lamp drivers U407-5, U386-5, and U407-3 (zone E4) provide drive to the front panel indicator lamps for the SAFE, RUN, and READY lamps, respectively.

The Ready Logic (zone E4) combines the outputs of the Sequence Control Flip-Flop and the Load Heads Flip-Flop with the Q output of the Emergency Unload Flip-Flop to produce the Ready signal at the output of U365 (zone E5). The Ready signal is combined with the Selected signal at U385 (zone F4) to obtain the Selected And Ready condition for purposes of gating the line receivers and drivers for the I/O interface.

The Pseudo Sector Mark interface signal (IPSMD) is derived from a 10MHz crystal controlled oscillator using decade counters U146 and U127. The Pseudo Sector Mark is a 50 kHz square wave clock signal with 2000 $\pm$ 20 pulses per revolution.

The decade counter consists of two independent logic sections of divide by five and divide by two. The decade counters U146 and U127 are used to count down the 5MHz clock (U205/14) to obtain a 100 kHz clock (LC2DF) at U127/12 which is used in the Position Control Logic. The clock signal LC2DF is again divided by two at U146/12 to obtain the Pseudo Sector Mark interface signal (IPSMD).

5.7.2 SHEET 3 (SCHEMATIC NO. 103704)

Sheet 3 of the Logic PCBA schematic contains the remainder of the Disk Drive Function Control Logic, i.e., all of the Disk Drive Function Control Logic which is not part of the Start/Stop Control Logic. The Start/Stop Control Logic description is contained in Paragraph 5.7.1. Refer to the functional description and simplified block diagram contained in Paragraph 4.7 in conjunction with the following discussion.

Four of the I/O interface lines that control disk drive functions are routed directly to the Holding Register (U308 zone H21) on the Logic PCBA. These lines are: Head Select (IHSXR), Platter Select (IPSXR), Track Offset Plus (ITOPR), and Track Offset Minus (ITOMR). Note that Selected And Ready (NLSARG) is brought to the holding register load-input. When NLSARG is low, the states on these I/O interface lines will be copied into the register. Thus, the state in the register will correspond to the state at the I/O interface line and will change accordingly for any changes on the I/O interface line.

When the disk drive is deselected, NLSARG will go high causing the holding register to trap the last value of the inputs from the I/O interface. The register will then hold that state until the next time the disk drive is selected. Note that Ready (NLRXXG) is used as the clear input to the Holding Register U308. When high, NLRXXG causes the register to be cleared to the all-zeros condition on each of its outputs. This condition will occur at any time the machine is in the Not-Ready condition. In other words, the predetermined states of logic zero on each of the output lines from the Holding Register determine specific states for the Upper Head Select (NLUSHG), Upper Platter Select (NLUPSG), Track Offset Plus (NLTOPG), and Track Offset Minus (NLTOMG) lines on the Logic PCBA.

Upper Head Select (NLUHSG) is routed directly to the Read/Write PCBA for head selection according to the state in the Holding Register. Upper-Platter Select (LUPSG), and its complement (NLUPSG), are connected to various circuits on the Logic PCBA. These circuits are: the Write Protect Logic for determining which Protect switches will be sampled, and the Multiplexer Control Logic for determining which platter information will be multiplexed to the I/O interface output lines. In addition, NLUPSG is routed to the Read/Write PCBA for selecting a specific storage surface.

NAND gates U328 (zone G19) combine the Track Offset signals from the Holding Register with NLBTFF from the Position Control Logic. The results are that the Track Offset signals will not be asserted to the Read/Write PCBA and the Servo PCBA during the time that the positioner is busy. The outputs of these NAND gates are connected to the Servo PCBA and the Read/Write PCBA via pins 22 and 23 of J103 and pins 26 and 25 of J104.

NOTE

These signals control change of gain in the read amplifier on the Read/Write PCBA when both signals are asserted. The signals are also fed to the Servo PCBA and are used to assume operation of the Track Offset circuitry.

The Write Double Frequency Data Re-transmitter (U70 zone F21) functions as a line receiver and as a line driver. The Write Data Signal (IWDSR) from the I/O interface is received by U70 acting as a line receiver. IWDSR is the double frequency encoded write data from the I/O interface which must be transmitted to the Read/Write PCBA. Transmission of the write data signal is also accomplished by U70. Acting as a line driver, it drives the NLWDFT signal to the Read/Write PCBA through J103 pin 27. Thus, the Write data signal is re-transmitted to the Read/Write PCBA where it is used by the Read/Write electronics.

The Unit Select Logic and the Busy Output Logic are shown in zone 17 through 21. The Unit Select Logic is the decoding arrangement and the Busy Output Logic is an encoding arrangement. Four separate Unit Select lines (IUS1R, IUS2R, IUS3R, and IUS4R) are provided at the I/O interface and are presented to the circuit via J102. This allows selection of one of four disk drives on the common I/O bus. Internally, it is necessary for the drive to provide a signal which indicates that it is being selected by the I/O interface.

Since there are four separate and distinct select lines presented to the disk drive, they must be decoded. The Unit Select lines are brought through J101, J102, and are decoded according to the state of the Unit Number Selector Switch, which connects to J110, pins 5, 8, 9, 6, and 7, by U89 and U328-11 to produce the Select Signal (LSXXG). When the Unit Number Select Switch on the front panel is set to one of the position numbers (one through four), one and only one of the signals at U448-4, U448-10, U448-8, and U448-6 will be high. This will result in the Select Signal (LSXXG) being generated only when there is an assertion on the specific Unit Select line that corresponds with the number as designated by the Unit Number Selector Switch on the operator's panel.

The Busy Signal (NLBTFF) from the Position Control Logic is gated by the Selected and Ready signal (LSARG) to obtain the Ready to Seek, Read and Write interface signal at the output of NAND gate U86/8.

Jumpers W1 and W2 allows selection of the High Density Indication interface signal (IHDID). The A side of the jumper W1 is connected to the Selected signal (NSXXG) whereas the A side of the jumper W2 is connected to the Logic One signal (LL0X7). The B sides of the jumpers W1 and W2 are tied together to obtain the High Density Indication signal at the output of the interface driver U69/3.

The Read/Write Control Logic controls the Write, Erase, and Read signals to the Read/Write PCBA. These signals depend upon the conditions of the input interface lines and certain signals generated on the Logic PCBA. Additionally, the Read/Write Control Logic generates NLWOEG which is supplied to the Start/Stop Control Logic.

The Write Gate (IWGXR) signal and the Erase Gate (IEGXR) signal are received and gated with Selected And Ready (NLSARG) by U48-1 and U48-4 (zone G16). These gates provide outputs only if the disk drive is selected and ready. The outputs of U48-1 and U48-4 are then gated by the AND condition of Position Mode (NLPMXG) and File Protect Mode (LFPML). These signals are then routed to the Read/Write PCBA (via J103) as Write Mode (NLWMXG) and Erase Current Enable (NLECEG) by two NAND gates, U87-3 and U87-4. The Write Mode and Erase Current Enable signals to the Read/Write PCBA will be asserted if, and only if, the respective signal is received from the I/O interface, the disk drive is selected and ready, the drive is not in a file-protect mode, and the positioner is in the position mode.

If either Write Gate, Erase Gate, or both is present, the low active Write Or Erase signal (NLWOEG) will be generated at the output of U48 (zone G16). This signal is used in the Start/Stop Control Logic to prevent clearing of the Load Heads Flip-Flop when either a Write or an Erase operation is in progress. The Read Gate signal (IRGXR) from the I/O interface is gated only by Selected And Ready (LSARG) at NAND gate U87/8 (zone F16) before being supplied to the Read/Write PCBA at J103.

The Write Protect Logic performs several functions on the Logic PCBA. It provides front panel indication of the Write Protect Status through the protect lamp indicators. It reports to the controller whether or not the selected platter is write protected through the Write Protect Status interface line (IWPSD). It disables write operation if the selected platter is write protected.

The Write Protect Switches connect to J108 and their states are sampled by the Protect Switch Latches. The Protect Switch Latch outputs are LUP0S and LLP0S corresponding to the upper and the lower platter, respectively.

The Write Protect Input interface signal IWPIR (J101/B31) may be used by the controller to set the Write Protect Status for the selected platter. The specified minimum pulse width for this interface signal to set the Write Protect Status F/F for the selected platter is 350 nanoseconds. This is achieved by transmitting this signal through the pulse width discriminator circuit. This circuit consists of open collector inverter U147/8 which is used in conjunction with the low pass filter network formed by resistor R10 and capacitor C1 (sheet 2, zone B17). The output of this pulse width discriminator is applied to the Schmitt trigger type 4-input NAND gate U286 (sheet 2, zone B16) which is enabled by the Selected And Ready signal (LSARG). The output of this NAND gate NLWPIG is applied to the NOR gate U406/8 (sheet 3, zone A10) used as a low true AND gate. It is ANDed with the Upper Platter Select signal NLUPSG (U406/9) and the result is NORed with the output of the Write Protect Latch corresponding to the upper platter LUP0S. The output of this NOR gate is applied to the asynchronous pre-set input of the Write Protect Status F/F U267/2 (sheet 3, zone B9) corresponding to the upper platter. The Write Protect Input interface signal may therefore be asserted for the minimum duration of 350 nanoseconds to set the Write Protect Status. The Write Protect Status F/F U341/11 may be set in a similar manner.

As previously described, the output of the Write Protect Latches are NORed with the Write Protect Input signal by the NOR gates U406/1 and U406/13 (sheet 3, zone A9). This allows setting up the Write Protect Status F/Fs via the Write Protect Switches. Once set, the Write Protect Status F/Fs can only be reset by depressing the Start/Stop switch on the front panel, thereby stopping the disk drive. This is achieved by zero-setting the Write Protect Status F/Fs via the Run Switch Pulse (LRPXG) obtained at U327/13 (sheet 2, zone H16). It should be noted that Logical Zero and Logical One signals are always applied to the J and K inputs of the Write Protect Status F/Fs, respectively.

The AND/OR invert gate U104/8 is used to decode the Write Protect Status of the selected platter using LUPSG and NLUPSG (sheet 3, zone B8) to obtain Write Protected signal (LWPTG) at U123/10. LWPTG is NANDed with Selected and Ready signal (LSARG) to obtain NLWPSG which is applied to the interface driver U44/5 for transmission over the interface. LWPTG is also internally used to disable write operation on the selected platter if the platter is write protected (sheet 3, zone F16). When the power is turned on the Write Protect Status F/Fs are initialized by the Power Clear signal (NLPCXG). The Write Protect Status for the respective platters is displayed on the front panel Protect Lamp indicators. The states of the Write Protect Status F/Fs are sampled by the Protect Lamp indicators which are driven by the logic signals NLUPLG (U267/14) and NLLPLG (U341/10) through the lamp drivers U424/5 and U424/3, respectively.

Also included on sheet 3 of the Logic PCBA schematic are line drivers for several of the interface output lines. The Read Signal Drivers (U67 zone H12) take the Read Clock Signal (NRRCSG) and the Read Data Signal (NRRDSG) from the Read/Write PCBA via J103 and drive these signals onto the interface lines Read Clock (IRCXD) and Read Data (IRDXD) via J102.

The Seek Incomplete interface signal (ISIXD) is driven to the interface by driving the interface driver U68/5 with steady logical one signal LL0X7 (zone C11).

When an Emergency Unload conditon exists, the Activate Emergency Unload signal (LAEXG) is true. LAEXG is applied to the three input NAND gate U346/6 used as an inverter (zone B14). The output of this NAND gate one-sets the F/F U167/11 indicating the Write Check condition. The Write Check signal (NLWCKG) is generated by gating the output of the Write Check F/F U167/11 with the Selected signal (LSXXG). The Write Check condition is reported to the controller from the selected disk drive via the interface line IWCKD by driving the interface driver U65/3 (zone D12) with NLWCKG. The Write Check F/F is reset by the Run Switch Pulse (LRPXG) (zone A14). The steady logical zero and steady logical one signal are applied to the J and K inputs of the Write Check F/F, respectively. When the power is turned on the Write Check F/F is initialized by the Power Clear signal NLPCXG.

Double Track Drive (IDTDD) is indicated on certain models by driving the Selected (NLSXXG) signal onto this interface line. Address Acknowledge (IAAXD) and Logical Address Interlock (IAIXD) are indicated at the interface by driving these lines with the Address Acknowledge (NLAAXG) signal via U68/3 (zone E11) and Logical Address Interlock signal via U3/5 (zone E12), respectively. NLAAXG and NLAIXG signals are generated in the Position Control Logic.

A dual platter drive is indicated at the interface by driving the Dual Platter Drive line with the Dual Platter Signal via U45 (zone C12). Dual Platter Signal (NLDPSG) is made up in the Sectoring Electronics (sheet 5 of the Logic PCBA schematic) from either a steady logic one signal or the low active Selected signal (NLSXXG) depending on whether the machine is a single platter or a dual platter drive, respectively. This selection is accomplished by the sectoring selection programming array that is plugged into J125.

The Termination Voltage Power Supply is shown in zone B11 of the schematic. This is a nominal 3.5v source which is provided to the interface for those models requiring single resistor termination scheme. This supply is derived by using diodes CR1 and CR2 in conjunction with R25 to provide a voltage drop from the internal +5v supply for supplying termination voltage to connector J102. Likewise, CR3 and CR4, in conjunction with R26, provides a reduced voltage from the +5v supply at J101. For those versions of the Logic PCBA that do not use the Termination Voltage Power Supply, pins A45 and B45 on J102, are wired to like pins on J101 by jumper W3. This provides feed-through of the termination voltage when this voltage is supplied by the controller. In that case, CR1, CR2, R25, CR3, CR4, and R26 are omitted.

The Chassis Ground Connection is shown in zone B8 of the schematic. For disk drives having ordinary grounding, W5 connects the I/O ground directly to the chassis. For machines requiring ground isolation, W5 is omitted and the I/O ground is connected to the chassis ground through a complex impedence consisting of R72 and C78.

The remainder of sheet 3 of the schematic pertains to the speed control electronics. The purpose of this circuitry is to compare the time of occurrence of the positive transition of the LPLFF flip-flop square-wave with the time reference obtained from the crystal oscillator countdown (refer to Paragraph 5.7.1). The result of the comparison is two signals, one indicating the instantaneous speed error (NLIMSI) and, if appropriate, another signal which will indicate a gross malfunction of the speed control (LSOTF).

When the Drive-Motor Enable (LDMEG) signal is high and the drive motor is enabled to operate, the Speed Sequence Register U244 (zone C8), the Increase Motor Speed Flip-Flop (U243 zone G4) and the speed out-of-tolerance Flip-Flop (U243 zone F3) are released to operate. The Speed Sequence Register, in conjunction with gates U224-10, U263-1, U223-3, and U224-8 function as an edge detector. They also establish the sequencing of the events in determining the disk speed. For each low to high transition of the Phase Lock Flip-Flop signal (LPLFF) a one-clock-time pulse, Transfer Speed Count (LTSCG), is generated. One-clock-time thereafter Speed Count Reset (NLSCRG) is generated to reset the speed counting logic. The clock frequency utilized by the Speed Sequence Register is the same clock frequency counted by the Speed Control Counter and is determined by the particular programming array plugged into J121 (zone F10), the Speed Control Programming array. This selects one of three possible clock signals from the clock countdown.

At the time the Transfer Speed Count (LTSCG) pulse is generated, the states held in the Speed High Limit Flip-Flop (U142 zone H5), the Disk Speed Low Flip-Flop (U242) and Speed Low Limit Flip-Flop (U242) is transferred into the Increase Motor Speed Flip-Flop (U243 zone F3) and the Speed Out Of Tolerance Flip-Flop (U243 zone F3). Specifically, the state of the Disk Speed Low Flip-Flop is transferred to the Increase Motor Speed Flip-Flop. Either a one-set condition of the Speed High Limit Flip-Flop, or a one-set condition of the Low Limit Flip-Flop is transferred to the Speed Out Of Tolerance Flip-Flop if either of those flip-flops were one-set. This would be the case only if a gross speed error is being detected.

The Speed High Limit Flip-Flop, the Disk Speed Low Limit Flip-Flop, and the Speed Low Limit Flip-Flop are referred to as the speed value flip-flops. The specific values stored in these flip-flops is the result of the previous speed count. After the values stored in the speed value flip-flops are transferred to the speed status flip-flops (consisting of Increase Motor Speed Flip-Flop and the Speed Out Of Tolerance Flip-Flop) by the Transfer Speed Count (LTSCG) pulse, then, one-clock time later the speed control logic is reset by

NLSCRG which is a one-clock period low active pulse. This resets the Disk Speed Low Flip-Flop, the Speed Low Limit Flip-Flop, and pre-sets the Speed High Limit Flip-Flop to establish the initial conditions at the speed value flip-flops for the next count. Also, the Speed Control Counter is loaded with a predetermined number from the Disk Speed Count Programming array plug-in J122. This determines the disk speed count programming according to the state of the Purge Cycle Flip-Flop.

The speed control counter, U202, U221, and U241 (zone F6, 7, 8), then counts from the value loaded until the next Transfer Speed Count pulse occurs. The rate of counting is determined by the specific clock signals selected by the Speed Control Programming array plug-in J121. If a count condition occurs in the Speed Control Counter which satisfies the decode of either U223-8 or U223-11, or U241 pin 11, then that value will be stored in the respective speed value flip-flop. At the time of the next Transfer Speed Count pulse, the value decoded and stored in the speed-value flip-flop will then be transferred to the speed status flip-flops. Note that two different values may be loaded into the Speed Control Counter at the time of a Speed Count Reset pulse. One is the normal running speed which will occur when the Purge Cycle Flip-Flop is zero-set, and the other value is a 10 percent overspeed which will be loaded when the Purge Cycle Flip-Flop is one-set.

The state of the Speed Out Of Tolerance Flip-Flop (U243 zone F3) is directly tested during a start sequence to determine if there is a gross speed error prior to loading the heads. Once the machine has reached the Ready condition, an occurrence of a logic one at the Speed Out Of Tolerance Flip-Flop output (LSOTF) will be gated by U343-6 with the Ready signal producing the Disk Speed Error (NLDSEG) signal. Disk Speed Error can, therefore, occur only during the time that the disk drive is Ready.

The state of the Increase Motor Speed Flip-Flop at the end of each speed count interval will indicate a basic binary error signal derived from the comparison of the time reference to the actual speed. This flip-flop will be pre-set by the Start Drive Motor (NLSDMG) pulse as a means of initializing the speed status during a start sequence. Note that the result of the time-speed comparison is a single binary digit that can have only two possible states; one or zero, indicating that the speed is either too fast or too slow. If it is too slow, the Increase Motor Speed Flip-Flop will be in the one-set condition indicating that the motor speed should be increased. Conversely, if the speed is too fast, the Increase Motor Speed Flip-Flop will be zero-set, indicating that it is unnecessary for the motor speed to be increased and allowing the motor to coast down through the desired speed value.

5.7.3 SHEET 4 (SCHEMATIC NO. 103704)

Sheet 4 of the Logic PCBA schematic contains the Position Control Logic. Refer to the functional description and simplified block diagram contained in Paragraph 4.7 in conjunction with this discussion.

The overall purpose of the Position Control Logic is to accept cylinder addresses from the I/O interface and control the positioning and holding of the positioner at those addresses. The subsidiary function of this logic is to execute Restore operations and to control loading and unloading of the heads. The actual control functions within this logic are performed by the Load Address Logic and Busy Logic, the Mode Control Logic, and Operation Control Logic.

The Mode Control portion of the Position Control Logic consists of the Position/Velocity Mode Logic (zone E5), the Forward Slow Mode Flip-Flop (zone C4), and the Reverse Slow Mode Flip-Flop (zone B4). The Position/Velocity Mode Logic determines when the positioner servo should be operated in the Position Mode and when it should be operated in the Velocity Mode. This logic also supplies the Position Mode (LPMXG) signal and the Velocity Reference Enable (NLVREG) signal to the Servo PCBA.

The Forward Slow Mode Flip-Flop (U167 zone C4) determines the state of the Forward Slow Mode (NLFSM1) signal, which is supplied to the Servo PCBA, to cause the positioner servo to operate in the Forward Slow Velocity Mode. Likewise, the Reverse Slow Mode Flip-Flop (U206 zone B4) functions to store and provide a state which asserts Reverse Slow Mode (NLRSM1) to the positioner servo for operating the positioner in the Reverse Slow Velocity Mode. The Forward Slow Mode is used when loading heads and during the last portion of a restore operation. The Reverse Slow Mode is used when unloading heads and during the first portion of a restore operation.

The Forward Slow-Mode Flip-Flop (U167) is released for operation when the Load Heads Flip-Flop (LLHFF) is one-set. Prior to loading, the heads will be retracted. This condition is indicated by Heads Retracted (SHRXG) being high, which in conjunction with one-setting the Load Heads Flip-Flop, results in a high logic level from U187-4 (zone C5). A high output at U187-4 causes the Forward Slow Mode Flip-Flop to be pre-set to commence loading the heads.

Recall that the Forward Slow Mode Flip-Flop (U167) is used also when performing a Restore operation. In this case, pre-setting the Forward Slow Mode Flip-Flop is controlled by the setting of the Restore operation Flip-Flop (U206 zone A4). The Restore Operation Flip-Flop determines whether the address as asserted by the interface will be examined or whether it will be disregarded and a Restore operation performed.

The Restore Operation Flip-Flop (U206) will be pre-set by the low active pulse from U49-6 (zone B6). This pulse will occur if the Restore Initial Cylinder (IRICR) line is active at the time that a Cylinder Address Strobe (ICASR) is supplied from the I/O interface. At that time, pins 4 and 5 of U49 will be high, pre-setting the Restore Operation Flip-Flop. When this flip-flop is pre-set, U187-10 is enabled to pre-set the Forward Slow Mode Flip-Flop by the negation of Position Transducer Index (SPTIG) during the latter portion of a restore operation.

The Forward Slow Mode Flip-Flop is zero-set by the first high-to-low transition of Position Quadature Clock (SPQCG) that occurs after the change of state of Position Transducer Index (SPTIG) during loading of the heads. Since this occurrence must follow after the change of state of Heads Retract (SHRXG), both SHRXG and SPTIG are ANDed by U187-1 (zone C5).

The Reverse Slow Mode Flip-Flop (U206 zone B4) is pre-set at the same time that the Restore Operation Flip-Flop (U206 zone A4) is pre-set when a Restore operation is commanded. The Reverse Slow Mode Flip-Flop can also be one-set when the Load Heads Flip-Flop is zero-set. This results from (NLLHFF) being high, enabling the J input of the Reverse Slow Mode Flip-Flop. The Reverse Slow Mode Flip-Flop is cleared when the Forward Slow Mode Flip-Flop is pre-set.

When either of the slow mode flip-flops are one-set, the demand address clear condition will occur via U49-8 (zone C3). This will clear the Demand Address Registers (U301, U321, U302 zone E, F, G, H-17). In addition, Demand Address Clear, in the form of a low active signal (NLDACG), will disable the Count Clock Detector Register (U323 zone C14) by clearing it to an all-zeros condition and will cause the Current Address Counter (U322, U381, U342 zone E11, 12, 13) to load all-ones. NLDACG also forces NLVREG to the high logic level via U403-8 (zone E4) disabling the velocity reference, and forcing Not Position Mode (NLPMXG). In this manner, the logic is initialized and conditioned during the time the heads are being loaded or retracted, or during the execution of a Restore operation.

When a demand address clear condition does not exist (both the Forward Slow Mode Flip-Flop and the Reverse Slow Mode Flip-Flop zero-set), the Count Clock Detector Register (U323 zone C14), the Demand Address Registers (U301, U321, U302), and the Current Address Counter (U381 zone E12) will be released. The Velocity Reference Enable and Position Mode signals will be under control of the other gates.

In the Position/Velocity Mode Logic, when Not Demand Address Clear (NLDACG) is high (a Demand Address Clear condition is not occurring), the Position Mode signal will be asserted when the address difference is zero and Position Quadature Clock is low. This will be the case when the Current Address Counter contents agree with the Demand Address Register contents and the positioner is within one-quarter track of the true-track center line.

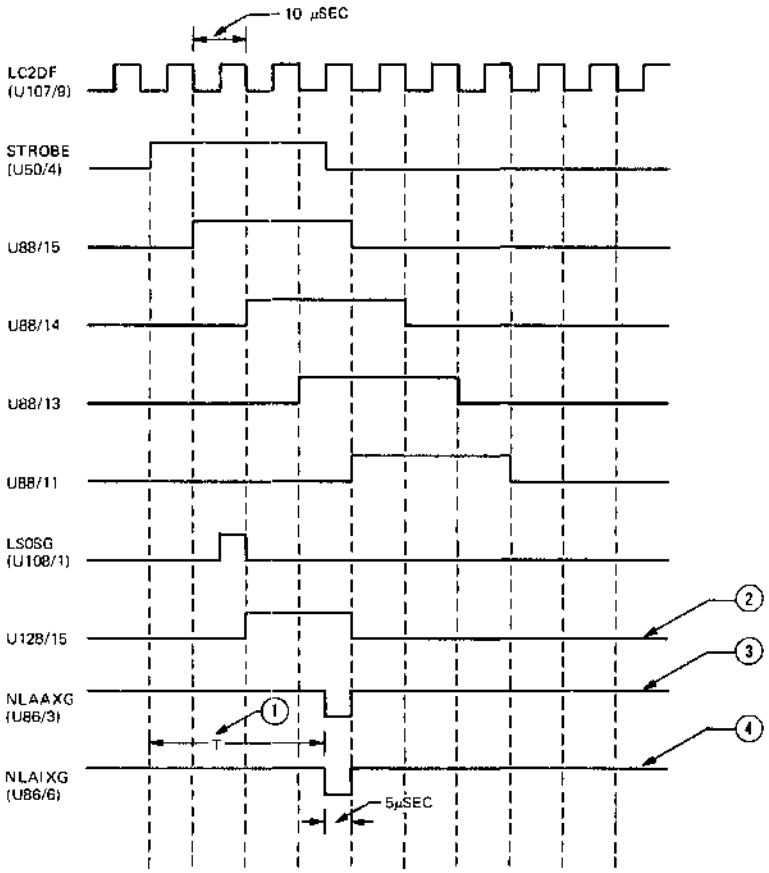
The purpose of the Load Address Logic is to generate a low-active pulse at U107/6 (sheet 4, zone C10) when a Strobe (ISTRR) is received from the I/O interface and the address on the Cylinder Address Lines is a valid address. Another function of this logic is to generate an illegal address indication to the I/O interface when the address on the interface lines is invalid at the time that a strobe is received.

Strobe is received via J101, inverted, and shifted through the Strobe Shift Register (U88 zone C11). The strobe leading edge is edge-detected and gated with the clock LC2DF by the gate U107/8. It is inverted to generate LS0SG at U108/1. LS0SG is ANDed with Not Busy (NLBTFF) and Address Valid (LAVCG) the result of which is used to copy the Cylinder Address Lines into Demand Address Register. The Restore Line is received via J101, inverted, and gated with LS0SG by U49/6 to determine if the Restore Operation Flip-Flop and the Reverse Slow Mode Flip-Flop should be pre-set to commence a restore operation.

The valid Address Decoder circuit consists of three 4-bit comparators, U262, U261, and U281 connected in series (zones C16, C17, and C18). It receives its A inputs from Cylinder Address Lines. Cylinder Demand Address Lines are compared against B inputs to the comparators which are programmed through jumpers W10 and W11 to generate the smallest illegal address; 203 decimal in the case of 100 TPI drive or 406 decimal in the case of 200 TPI drive. The binary value of Demand Address Lines is compared with the address programmed on the B inputs to generate the output Address Valid LAVCG which goes high if A value is less than B. If A is equal to or greater than B, then LAVCG goes low. LAVCG is inverted through U108/4 (zone B11) to provide J input to the flip-flop U128/15. The K input to this flip-flop is at steady ground. This allows the flip-flop U128/15 to one-set by LS0SG if the illegal address is presented on the Demand Address Lines and the asynchronous clear input to this flip-flop is released. The asynchronous clear input to this flip-flop is generated by ORing the Strobe signal at U50/4 with the delayed Strobe signal at U88/15 through the NOR gate U108/10 and the inverter U226/10. Figure 5-41 shows the timing relationship for this portion of Position Control Logic.

The $\overline{Q}$ and Q output of the illegal address flip-flop U128/15 are gated with the delayed pulse generated at U186/6 to provide Address Acknowledge signal (NLAAXG) and Logical Address Interlock signal (NLAIXG) through the NAND gates U86/3 and U86/6, respectively. NLAAXG and NLAIXG are transmitted to the controller interface through the interface drivers U68/3 and U3/5, respectively (sheet 3, zone F11).

It is important to note that the Strobe Shift Register is able to accept the Strobe from the I/O interface only when it is released for operation by a high-logic level on the Selected And Ready (LSARG) line.



NOTES:

1. 22.5µSEC < T <37.5µSEC
2. ILLEGAL ADDRESS F/F U128/15 IS SET IF THE ADDRESS PRESENTED ON DEMAND ADDRESS LINES IS ILLEGAL.
3. IAAXD INTERFACE LINE IS PULSED IF ILLEGAL ADDRESS F/F IS NOT SET i.e. THE VALID ADDRESS IS PRESENTED.
4. IAIXD INTERFACE LINE IS PULSED IF ILLEGAL ADDRESS F/F IS SET i.e. THE ILLEGAL ADDRESS IS PRESENTED.

Figure 5-41. Valid Address Decoder Timing Waveforms

If an address is loaded into the Demand Address Register which is different than the address stored in the Current Address Counter, then an address difference will be produced. This difference results in the Position Mode (LPMXG) signal going low. This will cause pre-setting of the Busy Time Flip-Flop which indicates that the positioner will be busy executing a seek. This signal is supplied to the I/O interface. Additionally, the Settle-Time Delay Register (U109 zone A11) is cleared in preparation for determining the settling time at the end of the seek. Note that the Busy Time Flip-Flop is enabled by the Ready signal (LRXXG).

As the positioner completes the seek, the address difference will reach zero and the positioner will reach a position that is within a quarter-track of the true-track center line. At this time, Position Mode will be asserted causing LPMXG (zone D3) to go to the high logic level. Since LPMXG is applied to the Settle-Time Delay Resister, it will commence propagating logic-ones through the register. After the delay, determined by the register propagation time, the End Busy (U109/12) signal will cause zero-setting of the Busy Time Flip-Flop and the Restore Operation Flip-Flop. This terminates the Busy Signal to the interface and also terminates any Restore operation status in the Operation Control portion of the Position Control Logic.

The Settle Time Delay Register (U109 zone A11) is clocked by LC13F from the clock countdown. Therefore, the delay time established by the Settle-Time Delay Register is determined by the clock frequency and the number of bits that must be propagated after the level change on Position Mode (LPMXG).

As previously described, the Demand Address Register (U301, U321, U302 zone E, F, G-16) will either hold the last value, load a new value if the NLLAXG pulse occurs, or will be cleared and held if a Demand Address Clear condition occurs. Therefore, the contents of the Demand Address Register will either be all zeros or the last Demand Address loaded. The contents of the Demand Address Register therefore specify the present cylinder demanded.

The current position of the positioner is stored in the Current Address Counter (U381 zone E12). The Current Address Counter is an up/down counter. The direction and amount of the count is determined by the count control on the basis of the Position Reference Clock (SPRCG) and the Position Quadature Clock (SPQCG) signals from the Servo PCBA. These digital signals are derived from the outputs of the position transducer. During loading of the heads, the Current Address Counter is first loaded to a condition of all-ones and then counted by one upcount clock to an all-zeros condition to initialize the Current Address Counter at cylinder 000.

Each high-to-low transition of the Position Quadature Clock (SPQCG) is edge detected by the Count Clock Detector Register (U323 zone C13). A one-clock time pulse is generated for each high-to-low transition of SPQCG, and this pulse, via U383-4, is used to strobe the Up/Down Count Logic (zone E13). If during the time of the count clock pulse, Position Reference Clock (SPRCG) is high, the Current Address Counter will be counted down. If, however, SPRCG is low during the time of a count clock, the Current Address Counter will be counted up. An UP count increases the value in the address counter indicating that the positioner is moving toward the spindle, and a DOWN count clock decreases the value stored in the Current Address Counter indicating that the positioner is moving away from the spindle.

During a seek, the positioner servo is operated as a velocity type of servo. A particular velocity level is determined on the basis of the amount of difference between the current address and the demand address. This difference is specified to the Velocity Function Generator on the Servo PCBA by the Address Difference Lines (NLAD0G through NLAD7G and including NLADEG) (zone E, F, G, H-6).

The address difference, that is the difference between the Current Address Counter contents and the Demand Address Register contents, is obtained by performing a ones-compliment arithmetic subtraction on the binary values of those counter and register contents. This subtraction process is performed by the Subtractor (zone F, G, H-10) and Complimentor (zone F, G, H-8). The actual subtraction is mechanized using an integrated circuit binary full-adder.

Since the arithmetic is ones-compliment arithmetic an end around carry is used. This carry is under control of the Carry Control Logic (zone E9). The algebraic sign of the velocity is determined on the basis of the binary value of the carry which specifies the binary state that is on the Forward Direction Line (LFDX1).

The end around carry circuit can be traced on the schematic starting at U402 (zone H10) at the C4 output and preceding to U361 (zone D9), pin 2 and 13, and from there through the Carry Control Flip-Flop U341, pin 15, and then to the input of U382 (zone E10). Note that the input to Carry Control Flip-Flop determines the state on the Forward Direction Line (LFDX1).

As shown on the schematic the integrated circuit binary full-adder is connected in a ripple-carry fashion to close the remainder of the end around carry loop. Notice also that the input to the least significant adder from the output of the Carry Control Flip-Flop (U341-15) also controls the complimentor.

The complimentor circuit is required for the situation where negative arithmetic is being performed. The complimentor provides conditional inversion of the outputs of the subtractor according to the state of the carry into the subtractor. Note that the subtractor uses the content of the Current Address Counter directly, whereas the contents of the Demand Address Register are complimented or inverted by the inverters shown in zone F and G13.

When the heads are being loaded, it is necessary to force the carry to a particular state. This is accomplished by the Carry Control on the basis of the states from certain bits in the Current Address Counter. U361-6 (zone D10) essentially decodes all one states in the most significant bits of the Current Address Counter and forces the carry to a specific state during the time that the heads are being loaded. Only during that time will the Current Address Counter have logic ones in the most significant positions of the counter. By forcing the carry during the loading of the heads, a least significant velocity reference level is specified by NLAD0G, such that between the time when the Forward Slow Mode operation is ended and the Position Mode is commenced the positioner servo is operated as a true velocity servo with a least significant velocity reference.

The Error Check Logic (zone F, G, H-3,4,5) performs two types of checks concerned with the operation of the positioner. The first check determines if the positioner has completed a seek within the maximum allowable time. This is done by the Seek Time Error Check Counter U287 (zone G4). This is a gross type of check to determine that the positioner has not become stalled due to a fault. While each and every seek is checked by the circuit, it does not verify that a specific distance moved was accomplished within the specific time associated with that length of seek. Rather, it determines that the positioner has not become stalled while attempting a seek.

The Seek Time Error Check Counter is enabled to count the LC17F clock, from the clock countdown, whenever the Busy Time Flip-Flop is one-set. This is a result of Not Busy Time (NLBTFF) being fed to the input of U246 pin 9 (zone G5).

If the counter has not counted up to the state where the carry-out has occurred, then the inputs at pins 9 and 10 of U246 will be high when the positioner is not busy. This causes U246-8 to go low, loading all-zeros into the Seek Time Error Check Counter U287.

When all-zeros are loaded into the counter and the load input is held at the low level, the counter is locked up and cannot count the LC17F clock. However, when the positioner goes busy NLBTFF goes low, causing U246-8 to go high, releasing the counter and allowing it to count LC17F clocks.

If the Busy Time ends before the counter has counted up to the carry-out condition, then the seek has been completed well within the maximum allowable time, the Busy Flip-Flop will again load zeros into the counter before the carry-out has occurred. Should the positioner become stalled, however, or other faults develop which cause the Busy signal to exist for a sufficient period of time for the counter to count to the carry-out condition, then the carry-out (U287 pin 12) will go low indicating a Seek Time Error (NLSTEG). This results in execution of an Emergency Unload.

Notice that the Restore Operation Flip-Flop (LROFF) is fed to the clear input of the Seek Time Error Check Counter. This signal clears the counter during the time of a Restore Operation. It is not desirable to check Seek Time during a Restore Operation.

The other check performed by the Error Check Logic is to determine that the positioner has not traveled outside of the legal range of travel. This is performed by the Position Limit Monitor circuitry shown in zone F4. This circuit generates a Position Limit Error signal (NLPLEG) if the positioner exceeds the normal range of travel. This check is performed only during the time that the heads are loaded onto the disk.

The Position Limit Monitor Flip-Flop (U267 zone F4) is cleared by NLLPNG. This signal will be low and therefore clear the flip-flop whenever the Purge Cycle Flip-Flop and the Load Heads Flip-Flop are both zero-set. This will occur when the disk drive is not in a Run Condition or it is in the Run Condition but not yet in a Purge Cycle. This can be seen from examining the logic shown on sheet 2 of the Logic PCBA schematic.

When loading heads, the Load Heads Flip-Flop will be one-set thus assuring that the Position Limit Monitor Flip-Flop is released for operation. Note that the J input of the Position Limit Monitor Flip-Flop is a continuous logic one, and therefore any high-to-low transition on the clock input of the flip-flop (U267 pin 6) will clock the flip-flop into a one-set condition. The flip-flop will remain one-set until it is cleared by NLLPNG going to the low-logic level.

During the loading of the heads, the Restore Operation Flip-Flop will be zero-set. As the positioner moves forward SPTIG will come to the high logic level causing pins 4 and 5 of U246 (zone F5) to be high, thus causing a low-to-high transition at U267 pin 6. As the heads load, SPTIG will go from the high level back to the low level, which will cause U267 pin 6 to go from a high to a low. This will one-set the Position Limit Monitor Flip-Flop, arming the monitor.

When the Position Limit Monitor flip-flop one-sets, the NAND gate U246 (zone F3) is enabled at its input on pin 12. A positioner fault may be indicated by either an occurrence of Position Transducer Index (SPTIG), or by the occurrence of Heads Retract, after the heads have been loaded. If SPTIG goes high it indicates that the positioner has traveled outside of its legal range. This will cause U246 pin 2 (zone E4) to go low which in turn will result in U246 pin 11 (zone E3) going low, thus indicating Position Limit Error (NLPLEG).

The other method for detecting a fault is if Heads Retract (SHRXG) goes high. This will force U246 pin 1 (zone E4) to the low-logic level, and again U246 pin 11 will go low, indicating Position Limit Error (NLPLEG). Either condition results in emergency unload.

The success of emergency unload will depend on the nature of the fault which originally caused the occurrence of Position Transducer Index (SPTIG), or Heads Retract (SHRXG).

If a multiple Position Transducer Index (SPTIG) occurs during the loading of the heads, this circuit will detect that occurrence and immediately commence an emergency unload before allowing completion of loading the heads. Likewise, this circuit will detect certain faults in the position transducer.

Refer to the circuitry contained in zones H12 and H13. The most significant bit of the Demand Address Register for either 100-track per inch or 200-track per inch machines can be selected by the jumper arrangement W14 or W15, as appropriate. This Demand Address Most Significant (LDAMG) signal is fed to the Read/Write PCBA where it is used for switching the write current to the particular value utilized for high order cylinder addresses.

5.7.4 SHEET 5 (SCHEMATIC NO. 103704)

Sheet 5 of the Logic PCBA schematic contains the Sector Electronics portion of the D3000 logic. Refer to the functional discussion and simplified block diagram contained in Paragraph 4.7 in conjunction with this discussion.

The purpose of the circuitry contained on sheet 5 of the schematic is to provide pulses at the I/O interface for electrically subdividing the storage surface into sectors. In addition to the pulses provided, the specific number of the sector passing under the Read/Write heads is also transmitted as a sector count which is used for addressing data stored on the disk. An index pulse is also provided as an output. This provides a signal which is a pulse occurring once per revolution of the disk that can be utilized to define the sector reference.

There are two basic types of sectoring: mechanical and electronic. The electronic type of sectoring may be further classified into electronic sectoring with the index-only type of cartridge and electronic sectoring with a multi-notch cartridge.

The primary inputs to the sector circuits are derived from two sensors located in the disk drive, and from clock signals derived from the Clock Countdown in the Start/Stop Control logic (sheet 2 of schematic). The Drive/Motor Enable signal is also used in the sector electronics circuits. The Upper Platter Select signal and the Selected And Ready signal are employed to control the output multiplexer. These signals are also obtained from the Start/Stop Control Logic.

The outputs of the sector electronics are the Sector Mark (ISMXD), the Index Mark (IIMXD), and the Sector Count (ISC0D-ISC6D).

The Sector Mark (ISMXD) provides a train of pulses at regular intervals during each revolution of the disk. These pulses divide the disk surface into 'n' equal segments, where 'n' is the number of pulses and the number of sectors.

The Index Mark (IIMXD) is a pulse train with a single pulse occurring once per revolution of the disk. This pulse always occurs just prior to sector zero.

The Sector Count lines (ISC0D-ISC6D) specify the sector count which is presented to the I/O interface in a binary format. This count indicates the particular segment of the disk surface currently under the Read/Write heads. The signals on these lines are, in essence, the states of a binary counter and in all cases correspond only to the respective platter as selected by the Platter Select Line.

The particular type of sectoring for which a disk drive is configured is determined by the programming arrays that are installed in the Logic PCBA. The parameters that are programmed into these arrays determine the nature of the sectoring. These parameters are: type of sectoring, number of sectors, and related disk speed.

The type of sectoring is programmed by the programming array plug installed in J125 (zone C, D, E, F-14). The values for the Upper and Lower Demultiplexer Counters, which are relative to the speed of the disk, are programmed by J121, shown in zone 15.

The number of sectors for electronic sectoring is programmed by J126 and J127 shown in zones 10, 11, and 12. The electronic sectoring is configured by the programming array plugs installed in J123 and J124. These arrays determine certain parameters of the electronic sectoring.

The Upper Sensor Detector (zone H19) and the Lower Sensor Detector (zone F19) receive signals from the upper and lower sensors, via J112 (zone E, F, G, H-20), and convert these analog signals into digital form. The Lower Sensor Detector circuit is similar to the upper sensor detector except that it has the additional capability of changing thresholds.

The Upper Sensor Detector has two amplifiers U425 and U387, which are not required in the Lower Sensor Detector. Otherwise, the circuit functions are similar. The Upper Sensor Detector receives the signal derived from sensing the upper cartridge sector ring or armature plate and converts it into a digital pulse train. The Lower Sensor Detector converts the analog signal obtained from the Lower Magnetic Sensor, which senses the Phase Lock Ring, into a digital pulse train.

NOTE

The removable cartridge may be sectored either electronically or mechanically. The lower platter is always sectored electronically in dual disk machines.

Standard top loading cartridges are fitted with an armature plate having one notch which is the Index notch. Some specially modified top loading cartridges will have, in addition to the index notch, notches used for purposes of mechanical sectoring.

Standard front loading cartridges have slots for the purpose of mechanical sectoring, and a single index slot. The sector slots and the index slot are located in the sector ring. Some specially designed front-load cartridges have only an index slot in the sector ring.

Front loading models of the D3000 employ a photoelectric type of sensor for the upper sensor. Top loading models use a magnetic transducer for the upper sensor. On all models, the lower sensor is a magnetic type transducer. The upper sensor for front loading models connects to J112 pin 9 (zone H20). For top loading models, the upper sensor is connected to J112 pin 6 (zone G20).

U425 (zone G20) serves as a fixed voltage gain amplifier when the magnetic sensor is connected and functions as a current-to-voltage converter when the photoelectric sensor is connected. Gain for the circuit is established by R28, R29, and R30 (or W20) for the magnetic sensor connection and by R27, R29, and R30 (or W20), for the photoelectric sensor. C5 determines the bandwidth. C6 and C7 decouple power supply voltages for U425. The signal from U425 is coupled to a voltage follower U387 by a R-C network, C8 and R31.

The output of the voltage follower, U387, is fed directly to a Schmitt trigger comprised of one section of U409 (zone G18). The Schmitt trigger threshold is determined by R35, R33, R32, and the +5.0v power supply voltage. The output of the Schmitt trigger is buffered by U408-8 and fed to the Upper Time-Demultiplexer. The signal at this point will be a pulse-train with one pulse per slot, or notch detected by the sensor. The purpose of the Schmitt trigger then is to convert the analog signal from the amplifier circuits into a digital signal suitable for use in the Upper Time-Demultiplexer and the remainder of the logic.

Referring to J112 (zone D18) it can be seen that power for operating the photoelectric sensor for front load machines is supplied via this connector.

The lower-sensor detector functions in a manner similar to the upper sensor detector. The lower magnetic sensor connects to J112 pin 4 (zone F20). The output of this sensor is filtered by R36 and C12; then fed directly to a Schmitt trigger consisting of the other half of U409 (zone F19). The threshold for the high threshold mode is determined by R43, R42, R39, R37, and R38. For the high threshold mode the output transistor of U444-4 (zone E19) will not be conducting; therefore R40 will be essentially opened circuited. In the low threshold mode, which will be the case whenever Drive Motor Enable (LDMEG) is low, the end of R40 which is connected to U444-4 will be essentially connected to ground. Therefore, the threshold for the low-threshold mode will be determined by R43, R42, R40, R39, R37, and R38. The output of the Schmitt trigger is buffered by U408-4 and U408-2 and fed to the Lower Time-Demultiplexer. In addition, U408-4 also feeds the Lower Detector Pulse (LLDPG) to the Disk Rotation Detector Counter (sheet one of the schematic) for detecting disk rotation.

The pulse trains obtained from the Sensor Detectors will have an index pulse intermixed with the other pulses if the sensor is detecting multiple notches. This, of course, will be the case at all times for the Lower Magnetic Sensor which senses the Phase Lock Ring. However, the pulse obtained from the index notch from the Upper Sensor will be interspursed with the pulses obtained from the sector notch only if it is a multi-notch cartridge. In the case of an index-only cartridge, the pulse train will be comprised entirely of index pulses. In any event, the pulse obtained from the index notch must be separated from the sector notches as appropriate. This function is performed by the time demultiplexers for those situations requiring demultiplexing. The pulse obtained from the index notch is placed onto a line separate from the other pulses.

The Lower Time Demultiplexer (zone E16) separates the pulse obtained from the index notch on the Phase Lock Ring from the phase lock pulses. The phase lock pulses will be demultiplexed and output at U183 pins 10 and 13 (zone D15). The pulse obtained from an index notch on the Phase Lock Ring is output at U183-10 (zone D15). Only a single clock frequency is utilized by the Lower Time Demultiplexer; this is LC08F (zone D17) obtained from the clock countdown in the Start/Stop Control Logic.

The Upper Time Demultiplexer outputs the pulse obtained from the index notch, in index-only cartridges, at U183 pin 4 (zone F15). Since there are no sector notches in index-only cartridges, there will be no output at U183 pin 1 for the index-only cartridge situation. When using a multi-notch cartridge, the Upper Time Demultiplexer will output the demultiplexed index pulse at U183 pin 1 (zone E15) and the demultiplexed sector pulses at U183 pin 4. The clock frequencies used with the Upper Time Demultiplexer are determined by a jumper installed at W8, W7, or W9 (zone F16). Clock LC08F, LC09F, or LC10F from the clock countdown are available at W8, W7, and W9, respectively.

For both Time Demultiplexers, the specific value of the demultiplexing gate time is determined by the programming array installed in J121 (zone D, F15). The Time Demultiplexer functions by generating a gate time according to the value loaded into the demultiplexer counter. The Upper Time Demultiplexer Counter (Upper Demux. Counter) is U184 (zone G15) and the Lower Time Demultiplexer Counter (Lower Demux. Counter) is U164 (zone E15). The value loaded into these demultiplexer counters is determined by the programming array plug in J121.

Generation of the demultiplexer gate is controlled by the respective Demultiplexer Control Flip-Flop U203 (zone G17) for the Upper Time Demultiplexer and U163 (zone E17) for the Lower Time Demultiplexer. The outputs of U203 and U163 are fed to the Upper and Lower Time Demultiplexer Gate Flip-Flops, respectively. The actual demultiplexer gate is obtained from the respective demultiplexer gate flip-flop. The output of the respective demultiplexer flip-flop is the enabling input to demultiplexing gates U183-4, U183-1, U183-10, and U183-13 (zone D, F15).

The time demultiplexer functions on the principle that for a pulse occurrence a gate is generated. If, during the time of that gate, another pulse occurs, that pulse is a pulse derived from the index notch. All other pulses are taken as being derived from other than the index notch.

The specific demultiplexed pulses are connected to the Sectoring Selection Programming array at J125 (zone C, D, E, F14). The outputs of the Sectoring Selection Programming array are fed to pulse formers and sector number counters.

The pulses obtained from the Time Demultiplexers or from the electronic sectoring electronics are unsuitable for direct output at the I/O interface; therefore they must be formed into pulses compatible with the interface requirements. This is accomplished by the Pulse Formers shown in zones G, H5 through 9. There are four pulse formers. One for the Upper Sector Pulse, one for the Lower Sector Pulse, one for the Lower Index Pulse, and one for the Upper Index Pulse.

The pulse formers are essentially shift registers (U22, U2, U23, and U43) connected as delays and edge detectors. The actual pulse forming is accomplished by NOR gates, U63 (zone G, H through 8). The clock used for determining pulse timing and delay is LC04F obtained from the clock countdown in the Start/Stop Control Logic.

The outputs of the Upper and Lower Sector Pulse Formers are multiplexed onto the single Sector Mark line (ISMXD) at the I/O interface by the Sector Pulse Multiplexer U62-8 (zone G4). The pulse driven by U44-3 (zone G4) depends upon the particular platter selected by the interface. Likewise, the outputs of the Upper and Lower Index Pulse Formers are multiplexed by the Index Pulse Multiplexer (U62-6) and fed to the single Index Mark line (IIMXD) according to the particular platter selected by the interface.

The Sector Pulse Multiplexer and the Index Pulse Multiplexer are controlled by the Multiplexer Control Logic (zone F9) which also controls the Sector Count Multiplexer according to the states of the Platter Select Line (LUPSG) and the Selected And Ready (NLSARG) line. NLSARG enables the Multiplexer Control gates only when the disk drive is selected and ready. Thus, the output of the Multiplexer Control Logic is gated with Selected And Ready signal.

The specific multiplexer enabled, either the upper multiplexer or the lower multiplexer, is determined at the input to the Multiplexer Control Logic by the states on NLUPSG and LUPSG. These signals are derived from the Platter Select Line input to the Disk Drive Function Control Logic, as shown in sheet 3 of the schematic.

When the disk drive is not selected, or not ready, then both LUMEG and LLMEG will be low, disabling the multiplexers. When the disk drive is Selected And Ready, then either Upper Multiplexer Enable (LUMEG) will be high or Lower Multiplexer Enable (LLMEG) will be high, according to whether the upper or the lower platter is being selected by the Platter Select Line. Thus, the action of the Multiplexer Control Logic is to determine which of the pulse and sector count outputs will be enabled and supplied to the I/O interface, J102.

The pulses obtained from the Sectoring Selection Programming array at J125 are also applied to the Sector Number Counters and the Count Control Logic to generate the sector count. The Upper Sector Number Counter (zone E7, 8) and the Upper Count Control Flip-Flop (zone D8) generate the upper sector number count. U144 and U143 are the Upper Sector Number Counters, and the count is controlled by the Upper Count Control Flip-Flop U83. The Lower Sector Number Counter (zone B7, 8) and the Lower Count Control Flip-Flop (zone B8) generate the sector number count for the lower platter. U125 and U124 are the Lower Sector Number Counters, and the count is controlled by the Lower Count Control Flip-Flop U83.

The contents of the particular sector number counter are multiplexed onto the Sector Count Lines (ISC0D through ISC6D) through the Sector Count Multiplexer (zone A, B, C, D, E-5) according to the control signals generated by the Multiplexer Control Logic. U84, U104, U105, and U85 form the Sector Count Multiplexer. One or the other of the sector number counter contents will be selected and supplied to the line drivers according to the control signals from the Multiplexer Control Logic. For each sector count line, there is a separate line driver. The specific sector number count, multiplexed onto the sector count lines, is determined by which platter is selected by the Platter Select Line and will only be presented to the I/O interface if the disk drive is Selected And Ready.

The mechanization of the Upper Sector Number Counter and Upper Count Control is identical to that used with the Lower Sector Number Counter and Lower Count Control. Therefore, only the Upper Sector Number Counter and Upper Count Control Flip-Flop will be explained.

The sector number count is represented by the binary value contained in the sector number counter. The Q_A output of U144 is the least significant bit and the Q_C output of U143 is the most significant bit of the number. The counter is clocked, or counted up, by the raw sector pulse obtained from the Sectoring Selection Programming array plug at J125 (zone C, D, E, F-14). For each pulse the counter will be incremented by one count. The Index Pulse, which occurs once per revolution of the disk, is defined as occurring during the sector just prior to sector zero; i.e., during sector N minus one where N is the maximum number of sectors. Therefore, at the time of occurrence of the index pulse, U83, the Upper Count Control Flip-Flop (zone E8) will be pre-set by the occurrence of the Index Pulse.

This will cause the $\bar{Q}$ output of U83 pin 10 to go low enabling the load inputs (LD) of U144 and U143. However, the counter will not load zeros until the next sector pulse. At that time, instead of incrementing the count, it will be clocked to load all zeros. At the time that this clocking occurs, the Upper Sector Count Flip-Flop will be zero-set since the K-input of the flip-flop is enabled at all times. This will remove the enable from the load inputs (LD) of the Sector Number Counter and allow it to be incremented or clocked by the raw sector pulse. The Sector Pulse immediately following an Index Pulse defines the beginning of sector zero. At the time of that Sector Pulse, the Sector Count lines will present a zero value as the result of having loaded the Sector Number Counter with all zeros. Thereafter, the value will be incremented until the maximum count is achieved. The maximum count that will occur is N minus one, where N is the number of sector pulses.

Recall from the previous discussion that the lower platter is always sectored electronically in dual-disk machines. Recall also that the removable cartridge in either single-disk machines or dual-disk machines may be sectored electronically. The exception to this is if the cartridge has an index-only notch, then it must be sectored electronically.

Electronic sectoring is selected by the Sectoring Selection Programming array installed in J125. When electronic sectoring is selected, the output of the electronic sectoring electronics is connected to the Upper Sector Pulse Former, the Upper Sector Number Counter, and the Upper Count Control Flip-Flop.

NOTE

The Lower Sector Number Counter, Lower Count Control, and Lower Sector Pulse Former are connected to the electronic sectoring electronics at all times since the lower platter is always sectored electronically.

Electronic sectoring requires that the disk drive generate pulses electronically for sectoring in lieu of the mechanical slots normally used for sectoring. Since the lower disk is sectored electronically regardless of the mechanical configuration, pulses must always be generated for sectoring the lower disk. These pulses are generated by counting down, with an electronic counter, the output of a high frequency oscillator. Because the sector pulses must be synchronous with the instantaneous speed of rotation of the spindle, it is necessary to phase lock this high-frequency oscillator to the spindle.

The high-frequency oscillator is a voltage controlled oscillator which is a part of the Sector Phase Lock Loop. The function and purpose of the Phase Lock Loop is to phase-lock the voltage controlled oscillator frequency to the phase lock pulses obtained from the Phase Lock Ring through the Lower Time Demultiplexer. The sector phase lock loop is shown in zones 12 through 20 at the bottom of the schematic. The input to the Sector Phase Lock Loop is from U183 pin 13 (zone D15), which is the phase lock pulse output from the Lower Time Multiplexer. It should be recalled that the phase lock pulses are separated from the lower index pulse by the Lower Time Demultiplexer.

It is necessary to count down the output of the high-frequency voltage controlled oscillator (VCO) in order to obtain the desired number of pulses per revolution for sectoring. This is accomplished by the Upper Sector Countdown Counter and the Lower Sector Countdown Counter shown in zones 10 through 12. Also associated with these counters are the Upper Electronic Sector Programming array and the Lower Electronic Sector Programming array that are installed In J126 and J127, respectively (zone C, E, 10, 11, 12). These programming arrays determine the particular number of sectors.

Since it is necessary to synchronize the countdown with the index for the respective platter, there is a synchronizer for each counter. These are used to synchronize the count with the index pulse. The index pulse is obtained from the respective Time Demultiplexer. In the case of the lower platter, the index notch on the Phase Lock Ring generates a pulse which is separated by the Time Multiplexer and applied to the Lower Synchronizer. In the case of the upper platter, the index slot or notch will generate a pulse which is separated as necessary by the Upper Time Demultiplexer and applied to the Upper Synchronizer.

The output of the respective Countdown Counter is a pulse, which is the raw sector pulse, for use by the pulse formers and the Sector Number Counter when electronic sectoring is employed.

The Sector Phase Lock Loop will be discussed first, then one of the countdown counters and synchronizers will be discussed since the Upper Synchronizer and Lower Synchronizer function in the same manner. This is also true of the Upper Sector Countdown Counter and the Lower Sector Countdown Counter. Therefore, only the Lower Synchronizer and Lower Sector Countdown Counter will be discussed in this document.

The Sector Phase Lock Loop is, in essence, an electronic servo loop designed to servo the voltage controlled oscillator frequency to phase lock that frequency to the pulse-train derived from the demultiplexed phase lock ring notches.

The Sector Voltage controlled Oscillator (Sector VCO) consists of Q3, R66, R71, U227, C22, C23, C24, R67, and R68 shown in zones B and C17. C25 and C26 are used only to decouple the power supply voltages that are supplied to U227. The voltage controlled oscillator is a R-C oscillator with part of the resistive component comprised of Q3, which is made variable by the voltage applied to the gate of Q3. The output of the oscillator is derived from pin 7 of U227 and coupled into a Schmitt trigger by C27 and R69. The Schmitt trigger consists of one section of U268 with its threshold established by R70. The output of the VCO is at U268 pin 4 which also connects to TP16 (zone C15). Thus, U268 converts the output of the oscillator into a digital signal that is suitable for use by the counters. In order to phase lock the VCO frequency to the phase locked pulses derived from the spindle, it is necessary to detect the phase difference between the Sector VCO and the phase lock pulses, to produce a control voltage to servo the frequency of the Sector VCO to the proper value. This is accomplished using a Phase Comparator and Filter shown in zones B17 through 20.

The phase lock pulses are applied to the clock input of the Phase Lock Flip-Flop U129 (zone C20). The Phase Lock Flip-Flop divides the frequency of the phase-lock pulse train by a factor of 2 and converts it into a square wave. This square wave is then applied to the Phase Comparator and Filter. Additionally, the Phase Lock Flip-Flop, Q output (LPLFF), is also fed to the Spindle Speed Control Electronics as previously described.

The other input to the phase comparator is the output of the VCO, suitably counted down. The countdown of the sector VCO is accomplished by the Sector PLL Countdown Counter (zone B13, 14, 15). The particular division ratio obtained with this countdown counter is determined by the programming array installed in J124 (Sector PLL Countdown Programming).

The output of the Sector PLL Countdown Counter is fed to the clock input of the Sector Countdown Divider Flip-Flop U129 (zone B20). The Sector Countdown Divider Flip-Flop converts the output of the Sector PLL Countdown Counter into a square wave. This square wave is the other input to the Phase Comparator and Filter. The phase comparator is comprised of U147 (zone A, B, C-19), R46, R49, R47, and R48.

The output of the Phase Comparator is filtered and applied to the input of the Sum-And-Difference Amplifier, U168 (zone B19). The filter is comprised of R51, R52, R53, R58, C16, R54, R55, R56, R59, C17. The particular filter characteristics required are programmed by part of J123 depending upon the disk speed utilized in the particular disk drive.

R60, R64, R61, R62, and R63 determine the characteristics and gain of the Sum-And-Difference Amplifier, U168. C19 and C20 decouple the power supply to U168. Adjustment of the PLL is accomplished by R57 (zone A18). The combination of R50, CR5, CR6, R57, C18, R62, and R63 provide a bias to the Sum-And-Difference Amplifier and the Sector VCO.

The output of the Sum-And-Difference Amplifier, U168 pin 6, is the control voltage to control the frequency of the Sector VCO. It is filtered by R65 in conjunction with C21. This control voltage causes the Sector VCO frequency to become phase-locked to the pulse-trained derived from the Phase Lock Ring.

The output of the VCO, which connects to TP16 (zone B15), is the input to the Countdown Counter and the VCO divider flip-flop. The Divider Flip-Flop divides the frequency of the Sector VCO by a factor of 2 for use as an alternate input to the Countdown Counters depending upon the desired number of sectors. Whether the output of the VCO Divider Flip-Flop or the output of the VCO directly is applied to the Sector Countdown Counter is a function of the particular programming array installed in J125.

The Lower Sector Countdown Counter and the Lower Synchronizer will now be described.

Operation of the Upper Synchronizer and the Upper Sector Countdown Counter is similar.

The Lower Sector Countdown Counter consists of U121, U161, and U181 (zone D10, 11, 12). These are 4-bit binary synchronous counters that may be loaded with one of two different values obtained from the Lower Electronic Sector Programming array installed at J127. The value loaded is determined by the Lower Synchronizer Register and associated circuitry which generate the I and NI signals applied to the Lower Electronic Sector Programming array, pins 5 and 6, respectively.

The Lower Sector Countdown Counter is clocked by the signal obtained from the Sectoring Selection Programming array which will be either the output of the VCO Divider Flip-Flop or the output of the Sector VCO directly.

When the Lower Sector Countdown Counter is counted from the value loaded until a carry-out occurs at U181 (zone D10), a pulse will be output at U122 pin 4. This pulse train output has a frequency which corresponds to the number of desired sectors. This pulse train will be synchronized with the index by the Lower Synchronizer Register (zone D13) and the associated synchronizing circuitry. That circuitry consists of U182 (Lower Synchronizer Register), U162-12, and U122-1 which edge detects the pulse obtained for the lower platter index by the Lower Time Demultiplexer which outputs from U183 pin 10 (zone D15).

The output of U122-1 (zone D12) is applied to the Lower Electronic Sector Programming array for purposes of determining the value loaded into the Sector Countdown Counter.

As previously discussed, the output of U122 pin 4 (zone D10) is the raw sector pulse which is utilized by the Sector Number Counter, Count Control, and the Sector Pulse Former.

5.8 MOTOR CONTROL PCBA

The following paragraphs describe the Motor Control PCBA installed in the D3000 Series Disk Drives. Refer to Schematic No. 103570 and Assembly No. 103571.

The Motor Control PCBA is approximately 4 inches square and is physically located on top of the power transformer. This PCBA is one of the subassemblies which comprise the Power Supply Chassis. The circuitry contained on the Motor Control PCBA performs a ground isolation function and provides the drive current necessary for controlling a triac, which, in turn, switches power to the disk drive motor. This PCBA is one of the functional elements in the spindle speed control.

Figure 5-42 illustrates the placement of the six molex connectors located on the face of the PCBA. These connectors are used to provide inputs to the circuit board consisting of the line voltage, the line voltage common, a reference voltage derived from a secondary winding on the main power transformer, and a trigger from the speed control circuitry on the Servo PCBA.

Additionally, the connectors and jumpers on the face of the Motor Control PCBA are used to provide an alterable interconnection scheme for selecting different connections to the motor capacitors and the drive motor depending upon the type of line voltage operation desired. Therefore, the connectors which connect to the Motor Control PCBA, plus the jumpers on the face of the board, provide a switchable junction box to allow alteration of the connections of the drive motor windings and the motor capacitors. This can be visualized by referring to the Power Supply Schematic, Drawing No. 103580.

Note that there are two classes of line voltage operation, i.e., 110v and 220v. When a particular disk drive is configured for operation on nominal line voltages between 95v and 125v, P403 is connected to J403 on the Motor Control PCBA, and jumpers W1, W3, W4, W5 are installed. P403 is the plug from the motor capacitors and P405, P406 are the plugs from

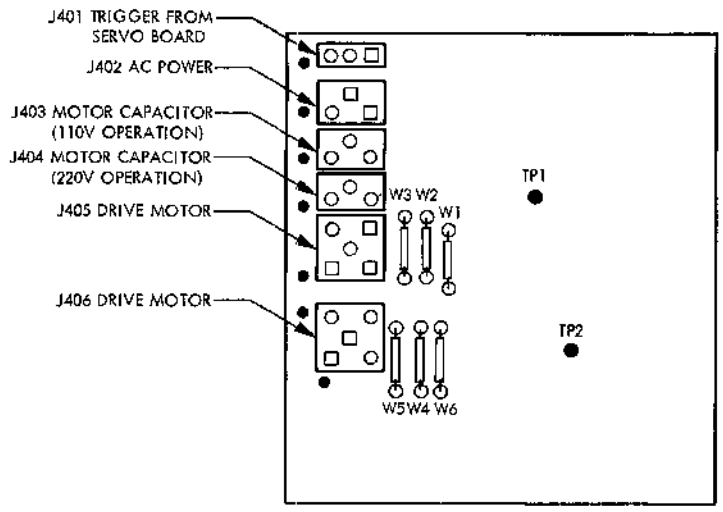


Figure 5-42. Motor Control PCBA, Test Point and Connector Placement

the disk drive motor. For operation on nominal line voltages of 190v to 250v, P403 connects to J404, and jumpers W2 and W6 are installed. Nominal line voltage of 95v to 125v is defined as 110v operation classification; nominal line voltage of 190v to 250v is defined as 220v operation classification. Refer to Paragraph 4.8 for the functional details of 110v and 220v operation of the drive motor.

Other than the interconnection arrangement previously described, all circuitry on the Motor Control PCBA is dedicated to switching the triac and suppressing any transients that result from this switching. A dc power supply voltage is required to provide current to the gate of the triac and must be developed with respect to the line voltage common. This is a function which is performed by a special power supply made up of CR1, R8, and C1 (zone D6, 7). The voltage is negative dc with respect to the ac common (pin 3 of J402). An ac signal of approximately 8v rms is provided to pin 5 of J402 from a separate secondary winding of the main transformer mounted on the power supply chassis. The voltage provided by this winding is rectified by CR1 and charges C1 to provide a relatively steady dc voltage; current limiting is provided by R8.

The trigger from the Servo PCBA is supplied to the Motor Control PCBA at J401 (zone E7). This trigger is the output of the Motor Speed Control circuitry on the Servo PCBA and is, in essence, a transistor switch closure to ground when the trigger is asserted.

When the transistor switch on the Servo PCBA is conducting and the trigger is asserted, current from the +5v supply flows through R1 (zone E7) and a Light Emitting Diode (LED), which is part of U1. U1 is an optical isolator consisting of a light-emitting diode optically coupled to a photo-transistor. When current passes through the LED it causes the LED to emit light; this light is coupled to the photo-transistor causing it to conduct. Conduction of the photo-transistor in U1 causes a base current to flow in Q1 (zone E6 which, in turn, causes a base current in Q2. Q2 conducts and provides the current to triac SCR1 (zone E5). Gate current flowing in SCR1 results in the triac conducting current through the motor winding. Conversely, when the trigger signal is absent there is no current flow through the LED in U1; therefore, the voltage across R2 causes Q1 to turn off and the voltage across R7 causes Q2 to turn off. Therefore, there is no current into the gate of the triac and conduction will stop as soon as the current through the triac passes below the holding current value, a characteristic of the device.

Resistors R3, R6, R4, and R5 provide the proper values of current in the collectors of transistors Q1 and Q2, and into the gate of the triac. R29 ensures that the gate current is sufficiently low that the triac will stop conducting. C2 and R20 (zone D5) provide a network for compensating for the fact that the drive motor is an inductive load. This means that at the time the current falls below the holding current value and the triac ceases to conduct, there will exist a certain voltage across the triac. If this voltage appears too rapidly, the triac will resume conduction and control is lost. In order to achieve control with such an inductive load the rate of rise in voltage (dv/dt) must be limited by a series R-C network across the triac. The capacitor will then limit the rate of change of voltage across the triac. The resistor is necessary to limit the surge of current from the capacitor when the triac fires and to damp the resonance of the capacitor with the load and circuit inductance.

5.9 TEMPERATURE COMPENSATION PCBA

The Temperature Compensation PCBA is installed in 200 tpi D3000 Disk Drives. The PCBA is located adjacent to the Read/Write PCBA and is approximately 8 inches long by 4 inches high. The Temperature Compensation PCBA operates in conjunction with the System Compensation PCBA and one externally mounted thermistor to provide thermal compensation and fine electrical CE alignment to 200 tpi models. Refer to Schematic 103449 and Assembly 103450 for the following discussion.

Figure 5-43 illustrates the placement of the five molex connectors located on the Temperature Compensation PCBA. These connectors provide power to the PCBA in addition to providing input and output signal paths between this PCBA and the Logic PCBA, the Servo PCBA, and the externally mounted thermistor.

The Upper Platter Select signal (NLUPSG) and the Upper Head Select Signal (NLUHSG) are applied to the Temperature Compensation PCBA via pins 1 and 4 of J502 (zone F8) from the Logic PCBA. These signals are gated so that Q1 is energized when the upper head of the upper platter is selected and Q2 is energized when the lower head of the upper platter is selected. Q1 and Q2 are both turned off when the lower (fixed) platter is selected. Test points TP9 and TP10 are provided as monitor points for the lower head and upper head fine electrical CE alignment inputs from the System Compensation PCBA. R2, R3, and R64 through R67 are scaling resistors for these CE alignment inputs. S1 (zone C5) is provided to remove these electrical CE alignment inputs while the mechanical CE alignment is performed.

Capacitors C1, C2, C3, C4, C5, C6, and C7 are employed for power supply decoupling purposes.

The internal temperature sensing thermistor, RT2, is mounted on the positioner baseplate and is connected to the input of amplifier U1 (zone C7) via pin 1 of J505. R14 is used for linearization of the input; R15, R16, and R17 are used for scaling the closed loop gain of U1 as monitored at TP1.

The output of amplifier U1 (zone C7) is applied to pin 2 of amplifier U3 (zone C6). The second input to U3 is applied to pin 3 and is provided from the System Compensation PCBA. U3 is a X1 gain difference amplifier whose output is proportional to the difference between the output of U1 and the reference voltage generated on the System Compensation PCBA. This output is applied to the System Compensation PCBA via pin 9 of J501.

In addition to the temperature compensation electronics, the Temperature Compensation PCBA contains a time delay circuit. This circuit consists of a monolithic timer, U13, a 4-bit binary counter, U15, and associated components. Transistor Q12 resets the timer. When Q12 is turned off, the timer will *free run* generating one pulse per minute as determined by R68, R69, R74, and C9. The binary counter is clocked by each pulse and counts five of these pulses before an output is delivered at J502-9. This five minute timer circuit allows the internal temperature of the disk drive to near stabilization before a Temperature GO signal is generated at the interface.

The output of amplifier U3 (TP12) also drives a multiplexer digital-to-analog converter. This multiplexer digital-to-analog converter consists of FETs Q8, Q9, Q10 (zone D, E-6) and amplifier U5 and U6 as well as the associated computing resistors R31, R32, R33, R35, R36, R39, R30, and R40. The switched current resistors (R31, R32, R33) receive their

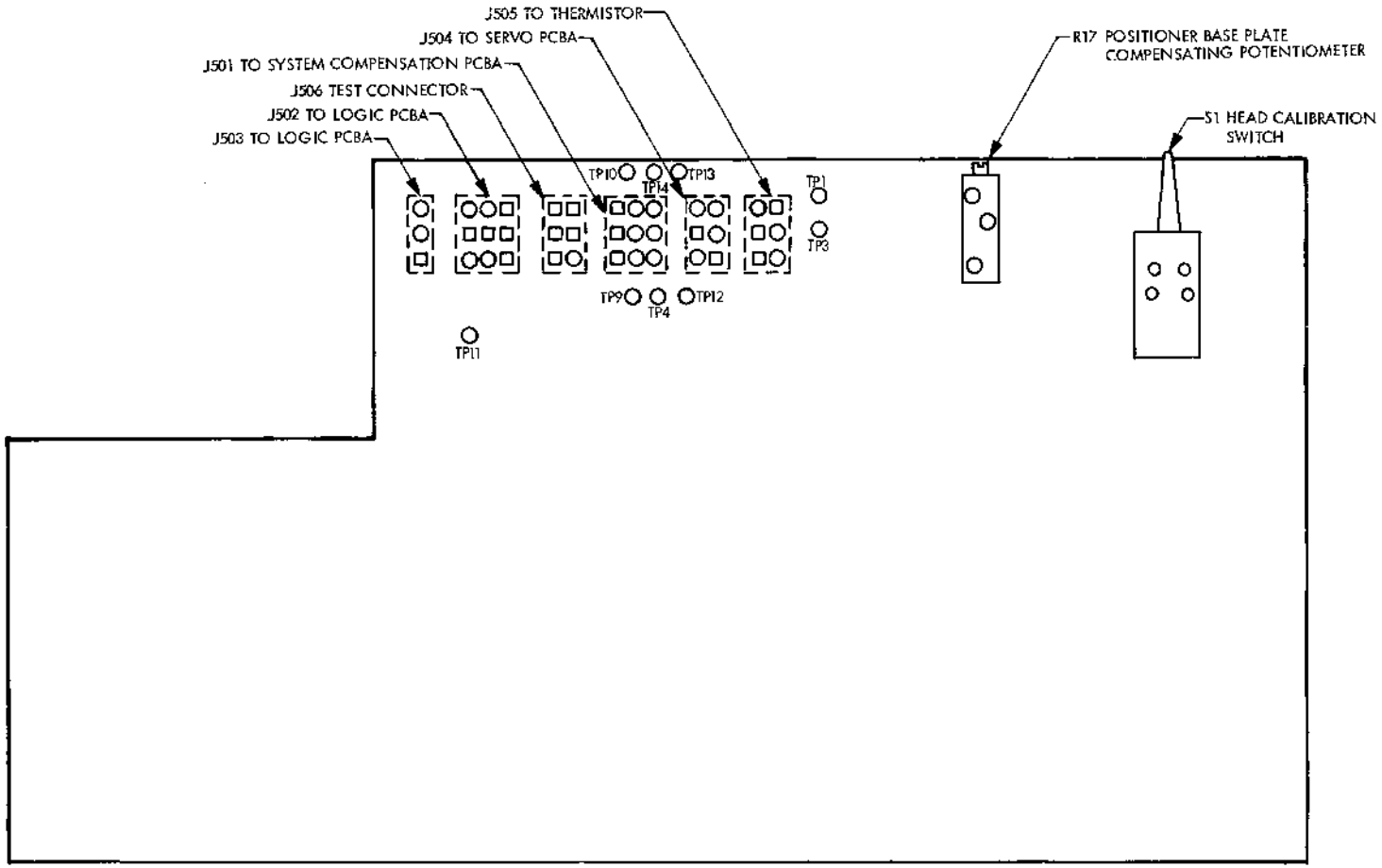


Figure 5-43. Temperature Compensation PCBA, Test Point and Connector Placement

commands from the current address counter on the logic card via J503 (zone D, E-8). The three most significant bits are employed to provide off-track compensation and are comprised of LCAE1, LCA71, LCA61, in order of declining bit weight. These signals are buffered by U9 and U11 and applied to transistors Q5, Q6, and Q7. These transistors translate their input levels to output levels which are compatible with the FET switches Q8, Q9, Q10. The outputs of the multiplexer digital-to-analog converters are applied to the servo summing junction via R53 and pin 1 of J504.

5.10 SYSTEM COMPENSATION PCBA

The System Compensation PCBA is installed in 200 tpi D3000 Disk Drives. The PCBA is located at the front of the disk drive and is physically secured to the underside of the switch panel bracket. The PCBA measures approximately 2-1/4 by 1-1/2 inches. This PCBA operates in conjunction with the Temperature Compensation PCBA and provides potentiometers for fine electrical CE alignment of the removable platter. Refer to Schematic 103444 and Assembly 103445 for the following discussion.

Figure 5-44 illustrates the placement of the three potentiometers and test points on the System Compensation PCBA. R1 is the potentiometer which provides for fine electrical CE alignment of the lower head of the removable platter; R2 provides for fine electrical CE alignment of the upper head of the removable platter. R3 is used to adjust the output of amplifier U3 on the Temperature Compensation PCBA. It is important to note that the output of amplifier U3 on the Temperature Compensation PCBA can be monitored at TP3 on the System Compensation PCBA.

TP1 and TP2 are provided to monitor the read amplifier output during CE alignment. To enable this function, TP19 on the Read/Write PCBA must be temporarily jumpered to TP13 on the Temperature Compensation PCBA. TP14 on the Temperature Compensation PCBA must be temporarily jumpered to TP18 (ground) on the Read/Write PCBA. TP13 and TP14 on the Temperature Compensation PCBA are tied to TP2 and TP1 on the System Compensation PCBA via J501/P501. It is important to note that these jumpers must be removed upon completion of CE alignment to prevent noise from being induced into the read amplifier.

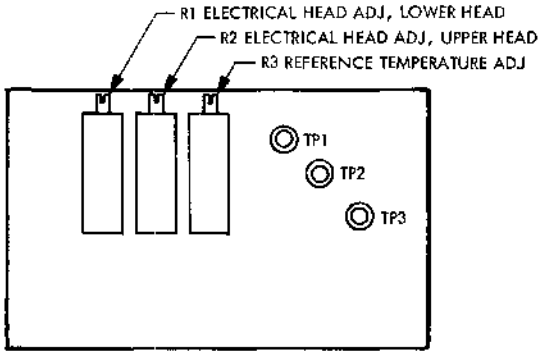


Figure 5-44. System Compensation PCBA, Test Point and Connector Placement

SECTION VI
MAINTENANCE AND TROUBLESHOOTING

6.1 INTRODUCTION

This section provides information necessary to perform electrical and mechanical adjustments, parts replacement, and troubleshooting. Sections IV and V contain the theory of operation and schematics required for reference when electrical adjustments or troubleshooting become necessary.

6.2 FUSE REPLACEMENT

The four fuses which protect the disk drive electrical components are located under the left rear corner of the base casting. Fuse identification and types are listed in Table 6-1.

6.3 SCHEDULED MAINTENANCE

The disk drive is designed to operate with a minimum of maintenance and adjustments. Part replacement is planned to be as simple as possible. Repair equipment is kept to a minimum and only common tools are required in most cases. A list of hand tools required to service the disk drive is given in Paragraph 6.14.

6.3.1 MAINTENANCE PHILOSOPHY

To ensure reliable operation of the disk drive at its optimum design potential a scheduled preventive maintenance program is recommended.

The objective of any maintenance program is to provide maximum machine readiness with a minimum of downtime. To provide this type of reliability it is necessary to perform preventive maintenance at the specified intervals. This schedule is given in Table 6-2.

In general, it is unnecessary to alter any adjustment on equipment that is performing in a satisfactory manner.

Table 6-1
Fuse Requirements

	Function	Type
F1	Line Fuse	5 Amp, 3AG, SB, 125v and below 2.5 Amp, 3AG, SB, 190v and above
F2	+20v dc (Unregulated)	10 Amp, 3AG, FB
F3	—20v dc (Unregulated)	10 Amp, 3AG, FB
F4	+10v dc (Unregulated)	10 Amp, 3AG, FB

Table 6-2
Preventive Maintenance Schedule

Interval*	Item	Manual Paragraph Ref.
1000 Hours**	Clean Heads and Disks. Check Disk Cleaning Brushes (Top Load Only).	6.4, 6.4.1, and 6.25
1000 Hours**	Clean Pre-filter.	6.23.1
2000 Hours	Lubricate Static Discharge	6.20
2000 Hours	Check Belt for Wear and Proper Tension.	6.19
2000 Hours or 6 Months**	Replace Air Filter.	6.23.3
2000 Hours	Lubricate Catch Assembly Ball Studs in Bezel.	6.17
2000 Hours or 6 Months	Clean Spindle Magnetic Chuck and Cone.	6.4.3
4000 Hours or 12 Months	Clean Positioner.	6.4.4
4000 Hours or 12 Months (100 tpi Models) 1000 Hours or 3 Months, and when Unit is Moved (200 tpi Models)	Check CE Alignment.	6.13
4000 Hours or 12 Months	Clean Base Casting and Inspect Machine.	6.4.5
12,000 Hours	Replace Disk Cleaning Brushes, Check Brush Cleaning Motor and Drive Mechanism for Wear. Lubricate Brush Arm Pivot and Drive Slot (Top Load Only).	6.25 and 6.26
24,000 Hours	Replace Drive Motor. Replace Spindle.	6.27

*The listed preventive maintenance frequency is based on operating hours. Typically, about 200 hours operating time per month will be accumulated for the average installation. When operating hours are less than the specified time interval, perform the maintenance on the basis of time interval only if stated in the table above.

**More frequent servicing may be required if operating in an abnormally dirty environment or if a high rate of cartridge loading is encountered.

6.3.2 GENERAL MAINTENANCE

Perform a visual inspection of the disk drive for loose electrical connections, dirt, cracks, binding, excessive wear, and loose hardware while conducting any maintenance function.

Cleanliness is essential for proper operation. Minute particles of dirt trapped between the flying heads and the disk causes the disk surface to become scored. This condition may result in an unusable disk or head damage, or both.

Accumulated foreign matter can also cause the read/write heads to fly at an excessive distance from the disk surface. This will severely impair the retrieval of data and result in improper writing.

6.3.3 GENERAL PRECAUTIONS

Any work performed on the drive should be accomplished with the power off and, preferably, with the power cord disconnected from the power line unless otherwise necessary.

CAUTION

THE DISK DRIVE POSITIONER ASSEMBLY CONTAINS A PERMANENT MAGNET; KEEP ALL ITEMS MADE OF FERROUS MATERIALS [TOOLS, WRIST WATCHES, RINGS, ETC.] AWAY FROM THIS AREA.

WARNING

AVOID PLACING HANDS IN THE VICINITY OF THE CARTRIDGE OR VOICE COIL WHEN THE DISK DRIVE IS OPERATING. AN EMERGENCY UNLOAD OF THE MAGNETIC HEADS COULD CAUSE SERIOUS INJURY TO MAINTENANCE OR OPERATING PERSONNEL.

CAUTION

CIGARETTE SMOKE AND TOBACCO ASHES ARE A COMMON CAUSE OF PROBLEMS INDUCED DURING SERVICING. AVOID SMOKING IN THE IMMEDIATE VICINITY WHEN SERVICING THE DRIVE WITH THE COVER OFF OR THE AIR FILTER REMOVED.

NOTE

Avoid operating the disk drive with the top cover removed unless maintenance cannot be performed otherwise. If the disk drive must be operated with the dust cover off, use a work cartridge.

6.4 CLEANING THE DISK DRIVE

The disk drive requires cleaning in these major areas: heads, disks, filters, spindle, positioner, base casting and cover. Details are given in Paragraphs 6.4.1 through 6.4.5, respectively.

The following cleaning materials are recommended for use when cleaning the disk drive.

(1) Lint-free wiper such as Microwipes TX500* or equivalent.

*Available from Texwipe Co., Hillsdale, New Jersey 07642.

(2) Isopropyl alcohol, 91 percent by volume.

CAUTION

USE ONLY 91 PERCENT ISOPROPYL ALCOHOL TO CLEAN DISK AND HEADS. USE OF ANY OTHER TYPE OF CLEANER OR SOLVENT, SUCH AS CARBON TETRACHLORIDE OR TRICHLORETHYLENE MAY RESULT IN DAMAGE TO THE DISKS OR HEADS. DO NOT USE CONTAMINATED ALCOHOL WHICH COULD CONTAIN ANY FORM OF RESIDUE.

WARNING

THE 91 PERCENT ISOPROPYL ALCOHOL SOLUTION IS A FLAMMABLE LIQUID. KEEP THE BOTTLE CONTAINING ISOPROPYL ALCOHOL STORED IN A SEALED METAL CONTAINER EXCEPT WHEN IN USE.

WARNING

WHEN SHIPPING 91 PERCENT ISOPROPYL ALCOHOL, COMPLY WITH THE APPROPRIATE REGULATIONS FOR SHIPMENT OF FLAMMABLE LIQUIDS.

(3) Disk cleaning wands (2 required) Texwipe Part No. TX800*, PERTEC Part No. 623-0002.

(4) Masking tape ½-inch or ¾-inch wide.

6.4.1 CLEANING THE HEADS

Remove the cover from the disk drive and raise the Logic PCBA to the extended position. Instructions for removal of the disk drive cover are contained in Paragraph 2.2.

NOTE

In dual disk models, the Read/Write PCBA should be removed prior to performing the head cleaning operation.

The following procedure is performed for each head.

(1) Prepare two cleaning wands (PERTEC Part No. 623-0002) as follows.

- Insert a lint-free wiper into the barbed slot of wand.
- Rotate wand counterclockwise thereby wrapping wiper completely around wand. Take care not to contaminate wiper.

(2) Dampen wiper with isopropyl alcohol.

CAUTION

DO NOT TOUCH THE FACE OF THE MAGNETIC HEADS WITH YOUR FINGERS. ACIDS EMITTED FROM SKIN CAN CAUSE PERMANENT DAMAGE TO A HEAD. DO NOT BLOW ON THE HEADS AS MOISTURE WILL CONTAMINATE THE HEADS.

(4) Carefully wipe the slider face of the head assembly with the dampened wiper. Take care not to over-stress the gimbal spring or the load spring on the head assembly.

*Available from Texwipe Co., Hillsdale, New Jersey 07642.

(5) Wipe the slider face dry using the second cleaning wand; this operation must be done before the alcohol has evaporated.

(6) Use a dental mirror to inspect each head after cleaning. It is important that all debris be removed from the head since debris not removed is a potential problem.

Examples of slider defects and head contamination are shown in Figures 6-1 and 6-2 with explanations for each example. In the event that contamination shown in Figure 6-1 cannot be removed with alcohol without scratching slider surface, affected heads must be replaced.

Any physical damage to the gimbal spring, the load spring, slider, or the load pin will necessitate replacement of the head assembly.

6.4.2 CLEANING THE FIXED DISK

The lower disk in dual disk drives is cleaned as follows.

(1) Gain access to the fixed (lower disk).

- Front Load Models: remove the access cover plate on the side of the lower disk cover.
- Top Load Models: remove the brush air deflector plate on the side of the cartridge adapter bowl.

(2) Prepare two cleaning wands as follows.

- Insert a lint-free wiper into the barbed slot of wand.
- Rotate wand counterclockwise thereby wrapping wiper completely around wand. Take care not to contaminate wiper.

(3) Dampen wiper with isopropyl alcohol.

(4) While rotating the spindle chuck counterclockwise, insert the cleaning wand at a 90-degree angle to the disk pointing directly at center. The wand should remain flat and stationary opposing the rotation of the disk, thereby removing all foreign matter.

(5) Using the procedure in Step (4), wipe the disk surface dry using the second cleaning wand. This operation must be done before the alcohol has evaporated from the disk surface.

CAUTION

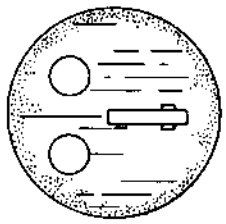
EXCESSIVE WAND PRESSURES CAN CAUSE DRY FRICTION HEAT WHICH CAN DESTROY RECORDED DATA.

CAUTION

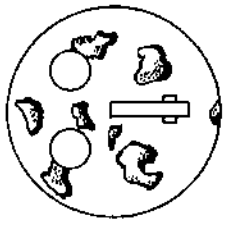
DO NOT ALLOW ALCOHOL TO DRY ON THE DISK SURFACE. DO NOT TOUCH THE DISK WITH FINGERS. ACIDS EMITTED FROM SKIN CAN CAUSE PERMANENT DAMAGE TO THE DISK SURFACE.

(6) Inspect the disk surface by illuminating the lower disk area with a suitable light source, e.g., flashlight.

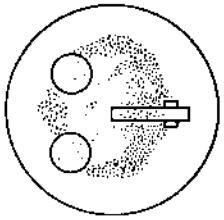
(7) Repeat Steps (4) through (6) for the second surface of the lower disk.



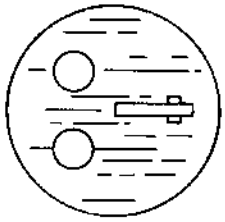
SLIGHT OXIDE ACCUMULATION
ON SLIDER SURFACE



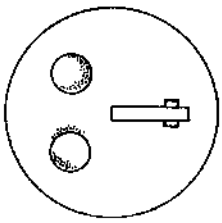
ALCOHOL RESIDUE DRIED ON
SLIDER SURFACE



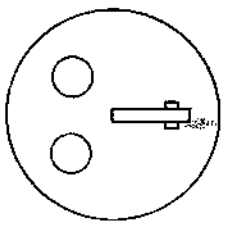
FINGERPRINTS ON SLIDER SURFACE



LIGHT SCRATCHES ON SLIDER
SURFACE WITHOUT OXIDE
ACCUMULATION



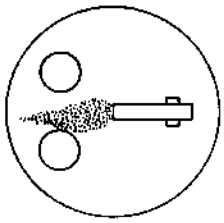
EXCESSIVE LOOSE OXIDE PARTICLE
BUILD UP IN BLEED HOLES



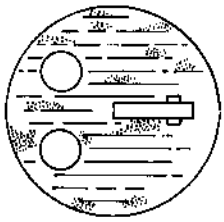
MINOR OXIDE STREAK

DIRECTION OF DISK ROTATION

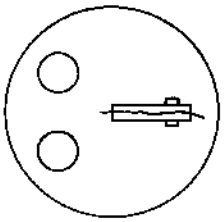
Figure 6-1. Slider Defects and Head Contamination which Require Cleaning Action



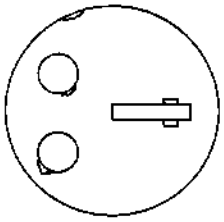
SLIDER SURFACE HAS A HEAVY OXIDE ACCUMULATION IN POLE TIP AREA WHICH CANNOT BE REMOVED



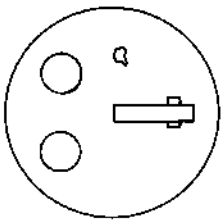
SLIDER SURFACE HAS DEEP SCRATCHES WITH OXIDE ACCUMULATION



DEEP SCRATCH OR SCRATCHES THRU CORE FACE OR POLE TIPS



CHIPPED EDGE OR EDGES OF SLIDER SURFACE PERIPHERY OR CHIPS AT EDGE OF BLEED HOLES



LARGE PIT OR VOID IN SLIDER SURFACE

DIRECTION OF DISK ROTATION

Figure 6-2. Slider Defects and Head Contamination which Require Head Replacement

(8) Reinstall the plate and hardware removed in Step (1) above.

NOTE

Removable cartridge disks can be cleaned in a similar manner, or they can be disassembled for cleaning. It is important that the slots [notches] in cartridge hubs be kept clean and free of dirt and particles.

6.4.3 CLEANING THE SPINDLE

Wipe the spindle cone and the magnetic chuck with a dry lint-free wiper. Metal particles that have become attracted to the magnetic chuck may be removed using masking tape.

6.4.4 CLEANING THE POSITIONER

The positioner shafts on 100 tpi models can be cleaned with a lint-free wiper slightly moistened with isopropyl alcohol; the scale on 200 tpi models can be cleaned in the same manner. Carefully wipe the surfaces to remove any accumulated matter.

CAUTION

DO NOT WET THE SHAFT, SCALE, OR WIPER WITH AN EXCESSIVE AMOUNT OF ISOPROPYL ALCOHOL AS IT COULD SEEP INTO THE CARRIAGE BEARINGS CAUSING BREAKDOWN OF THE BEARING LUBRICANT.

CAUTION

DO NOT DISASSEMBLE THE POSITIONER FOR CLEANING.

6.4.5 CLEANING THE BASE CASTING AND COVER

The base casting and the other associated areas, including the cover, should be cleaned using a vacuum cleaner.

CAUTION

DO NOT USE COMPRESSED AIR AS THIS WILL BLOW DIRT INTO THE DISK CHAMBERS AND AIR SYSTEM.

6.5 PART REPLACEMENT ADJUSTMENTS

Table 6-3 defines the adjustments that may be necessary when a part is replaced in the disk drive; details are given in Paragraphs 6.6 and 6.7.

6.6 ELECTRICAL ADJUSTMENTS

In addition to the tools listed in Paragraph 6.28, the following equipment (or equivalent) will be required for electrical adjustments.

(1) Oscilloscope, dual trace, having at least a 50 MHz bandwidth. Vertical and horizontal sensitivity specified to ± 3 percent accuracy.

(2) Three calibrated X10 test probes with ground clips.

(3) One X1 test probe with ground clip.

(4) Digital Volt Meter, Fairchild 7050 (± 0.1 percent specified accuracy) or equivalent, with test leads.

Table 6-3
Part Replacement Adjustments

Part Replaced	Auxillary Adjustments	Time Required (Hrs)	Paragraph Ref.
Spindle	Circumference Alignment, Radial Alignment, Sector PLL Adjustment	2:00	6.13, 6.13.5 or 6.13.7, 6.11
Servo PCBA	Servo, Power Supplies, and Spindle Speed Control	1:00	6.7, 6.9, 6.6.2, 6.6.3
Position Transducer Assy	Servo Readjustment	1:00	6.7, 6.9
Logic PCBA	Sector PLL Adjustment	0:45	6.11
Read/Write PCBA	Read PLL and RPN Pulsewidth Adj.	0:30	6.12.1, 6.12.1
Magnetic Transducer, Upper	Magnetic Transducer Gap, CE		6.18.1, 6.13
Magnetic Transducer, Lower	Magnetic Transducer Gap	0:35	6.18.2 or 6.18.3
Photoelectric Sensor, Upper (Front Load Only)	Circumferential Alignment	0:30	6.13
Cartridge Interlock Switch	Interlock Adjustment	0:30	6.15, 6.16
Cartridge Interlock Solenoid	Solenoid and Interlock Adjustment	0:30	6.15, 6.16
Head	CE Alignment	1:00	6.13
Fixed Disk	Check Data Reliability	1:00	
Power Supply	Power Supply Adjustment	1:00	6.6.2
Bezel Assy (Front Load Only)	Solenoid and Interlock Adjustment	0:30	6.15

(5) Disk Exerciser and 6-foot extender cable.

(6) Counter Timer, Monsanto Model 100B (±0.1 percent specified accuracy) or equivalent.

(7) Jumper, not to exceed 6 inches in length, with alligator clips on each end.

(8) Reticle Adjustment Tool, PERTEC Part No. 103659.

(9) Emergency Unload Bypass Jumper Plug, PERTEC Part No. 103608.

(10) Voice Coil Polarity Tester, PERTEC Part No. 103607.

(11) Circumferential Adjustment Tool, PERTEC Part No. 103609, or equivalent (required for front load models only).

6.6.1 ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified in Paragraph 6.6.

When the measured value of any parameter is within the specified acceptable limits, NO ADJUSTMENTS should be made. Should the measured value fall outside the specified acceptable limits, adjustments should be made in accordance with the relevant procedure.

NOTE

Some adjustments may require corresponding adjustments in other parameters. Ensure corresponding adjustments are made as specified in the individual procedures. The +5v, —5v, +10v, and —10v voltages must be checked prior to attempting any electrical adjustments.

When adjustments are made, the value set should be the exact value specified, to the best of the operator's ability.

CAUTION

PRIMARY POWER SHOULD BE REMOVED FROM THE DISK DRIVE WHEN ACCESS IS REQUIRED EXCEPT IN CASES OF ELECTRICAL TESTING AND ADJUSTMENTS.

Allowable line voltage variation is ±10 percent of nominal. See Figure 4-14 for transformer primary connections. Allowable line frequency variations are:

- 50 Hz line
  - 48 Hz minimum
  - 52 Hz maximum
- 60 Hz line
  - 58 Hz minimum
  - 62 Hz maximum

6.6.2 10V AND 5V REGULATORS

The 10v and 5v regulator circuitry is located on the Servo PCBA. The 10v sources are established by zener diodes and cannot be adjusted. The 5v sources are adjustable by

means of potentiometers located on the Servo PCBA. Potentiometer R158 adjusts the +5v source; potentiometer R167 adjusts the —5v source.

NOTE

When a new Servo PCBA is installed, or any change is made to the power supply circuitry, do not perform the following tests but go directly to the adjustment procedure, Paragraph 6.6.2.4.

6.6.2.1 Test Configuration

(1) Connect the disk drive to appropriate ac power source and set the ON/OFF switch to the ON position.

(2) All test points are located on the Servo PCBA unless otherwise noted.

6.6.2.2 Test Procedure, 10v

(1) Using a DVM (Fairchild 7050 or equivalent), connect the positive test lead to TP21 and the common test lead to TP1.

(2) Acceptable limits (+10v)

- +11.5v maximum
- +9.9v minimum

(3) Change the positive DVM test lead connection to TP25.

(4) Acceptable limits (—10v)

- —10.9v maximum
- —9.3v minimum

NOTE

In the event the readings obtained in Steps [2] and [4] fall outside of the acceptable limits, remove power from the disk drive and disconnect isolation plugs J209, J210, and J211 from the Servo PCBA. Apply power to the disk drive and proceed to troubleshoot using the schematic contained in Section VII. While troubleshooting, the 10v measurements will be made with J209, J210, and J211 removed.

6.6.2.3 Test Procedure, 5v

(1) Establish test configuration described in Paragraph 6.6.2.1.

(2) Verify that isolation plugs J209, J210, and J211 are installed.

(3) Using a DVM, connect the positive test lead to TP18 on the Logic PCBA and the common test lead to TP15 on the Logic PCBA.

(4) Acceptable limits (+5v)

- +5.25v maximum
- +4.75v minimum

(5) Change the positive DVM test lead connection to TP19 on the Logic PCBA.

(6) Acceptable limits (—5v)

- —5.25v maximum
- —4.75v minimum

6.6.2.4 Adjustment Procedure

When the acceptable limits are exceeded the following adjustments are performed.

(1) Remove power from the disk drive and remove isolation plugs J209, J210, and J211 from the Servo PCBA.

(2) Apply power to the disk drive.

NOTE

The ON/OFF switch will not be illuminated when J210 is disconnected from the Servo PCBA.

(3) Connect the positive test lead of the DVM to TP4 and the common test lead to TP1 on the Servo PCBA.

(4) Adjust potentiometer R158 on the Servo PCBA to +5v as observed at TP4.

(5) Change the connection of the DVM positive test lead to TP12.

(6) Adjust potentiometer R167 on the Servo PCBA to —5v as observed at TP12.

(7) Remove power from the disk drive and replace isolation plugs J209, J210, and J211.

(8) Apply power to the disk drive and recheck the +10v and —10v measurements (see Paragraph 6.6.2.2).

(9) Perform recheck of +5v and —5v power supplies under load, i.e., jumper plugs J209, J210, and J211 re-installed.

- Acceptable limits at TP18 on the Logic PCBA
  - +5.05v maximum
  - +4.95v minimum
- Acceptable limits at TP19 on the Logic PCBA
  - —5.05v maximum
  - —4.95v minimum

(10) If the limits established in Step (9) are exceeded, readjust R158 and R167 to obtain +5v and —5v at TP18 and TP19, respectively.

6.6.2.5 Related Adjustments

When adjustments are made to the +5v and —5v supplies, tests and/or adjustments are required in all procedures described in Paragraphs 6.6.3 through 6.6.

6.6.3 AC MOTOR SPEED CONTROL

The speed control adjustment for the ac drive motor is made to establish the correct spindle speed (1500 rpm or 2400 rpm) within a ±1 percent tolerance.

6.6.3.1 Test Configuration

(1) Remove power from the disk drive.

(2) Disconnect connector J205 from the Servo PCBA.

(3) Disconnect connectors J405 and J406 from the Motor Control PCBA.

(4) Ensure that the Emergency Unload Bypass Jumper is installed at connector J128 on the Logic PCBA.

(5) Connect oscilloscope Channel 1 probe to TP24 on the Servo PCBA.

(6) Connect oscilloscope Channel 2 probe to TP14 on the Servo PCBA.

(7) Connect the ground clip of each X10 probe to TP1 on the Servo PCBA.

(8) Set oscilloscope as follows

- Voltage sensitivity to 0.2v per division (both channels). Use dc input mode.
- Sweep rate to 5 ms per division.
- Set to automatic trigger mode.
- Use internal sync and set to trigger on negative slope.

6.6.3.2 Test Procedure

(1) Establish test configuration described in Paragraph 6.6.3.1.

(2) Select Channel 2 on the oscilloscope.

(3) Apply power to the disk drive and allow it to come SAFE; insert a disk cartridge into the disk drive.

The following sequence of events must be performed within 10 seconds from actuation of the RUN/STOP switch.

- Press RUN/STOP switch one time.
- Press RUN/STOP switch a second time.
- Manually pull the positioner carriage forward not more than 1/2-inch from its fully retracted position and observe that the signal at TP14, Trace 2 on oscilloscope, goes from a logic high to a logic low state.

CAUTION

EXTENSION OF POSITIONER CARRIAGE FORWARD MORE THAN 1/2-INCH FROM ITS FULLY RETRACTED POSITION WILL LOAD HEADS ONTO DISKS WHICH ARE NOT ROTATING, RESULTING IN DAMAGE TO HEADS AND DISKS.

- Observe the signal at TP24; it must be at a high logic level.

NOTE

If the logic level observed at TP24 is low, recycle ac power and repeat the above procedure.

- Leave positioner carriage extended to maintain logic control.

(4) Select Channel 1 on the oscilloscope; set the oscilloscope trigger to normal mode. Sync on negative-going edge of the pulse.

(5) Connect Channel 1 oscilloscope probe to TP22 on the Servo PCBA.

[ ] 50 Hz Line Frequency Operated Disk Drives: observe a pulse train of approximately 100 Hz at TP22.

[ ] 60 Hz Line Frequency Operated Disk Drives: observe a pulse train of approximately 120 Hz at TP22.

NOTE

Both 50- and 60-Hz pulse trains will reflect variations in line frequency.

NOTE

If a pulse train is not visible, adjust potentiometer R212 on the Servo PCBA until the train is visible; a clockwise adjustment of R212 increases the pulse width. Perform the adjustment procedure in Para. 6.6.3.3 if R212 is adjusted.

6.6.3.3 Adjustment Procedure

(1) Establish test configuration described in Paragraph 6.6.3.1.

(2) Change the sweep rate of the oscilloscope to 0.1 msec per division.

(3) Observing the waveform displayed on Channel 1 (TP22), adjust potentiometer R212 so that the positive-going edge of the pulse occurs between 3 to 6 divisions on the graticule as shown in Figure 6-3. Ensure oscilloscope is still synced on negative-going edge of pulse. Some hysteresis effect, approximately 1 division, may be noted on the positive-going edge due to variations in line frequency.

(4) Return the positioner carriage to the fully retracted position.

(5) Remove power from the disk drive.

(6) Replace connector J205 on the Servo PCBA.

(7) Replace connectors J405 and J406 on the Motor Control PCBA.

(8) Remove the jumper plug from connector J128 on the Logic PCBA.

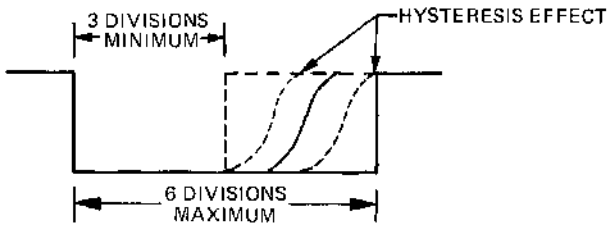


Figure 6-3. AC Motor Speed Control Signal Pulsewidth

6.7 POSITIONER SERVO CALIBRATION

Paragraphs 6.8 and 6.9 describe the test configurations, test procedures, and adjustment procedures relevant to both static and dynamic operation of the D3000 Positioner Servo. It is important to note that if static positioner adjustments are performed the dynamic positioner adjustments must also be performed.

To ensure accurate calibration of the positioner, the preliminary tests and adjustments described in Paragraph 6.7.1 must be performed prior to calibration of the positioner.

NOTE

The only ground reference test point to be used for measurement purposes is TP1. All test points referred to are located on the Servo PCBA unless otherwise noted.

6.7.1 POSITIONER PREPARATION STATIC TESTS

The following functions are required to prepare the positioner for calibration.

(1) Remove power from the disk drive.

(2) Disconnect connector J205 from the Servo PCBA.

(3) Install Emergency Unload Bypass Jumper at connector J128 on the Logic PCBA.

(4) Apply power to the disk drive and observe that the SAFE indicator becomes illuminated.

(5) Insert a disk cartridge into the disk drive.

(6) Measure +10.7 ±0.8v between TP1 and TP21.

(7) Measure —10.1 ±0.8v between TP1 and TP25.

(8) Measure regulated +5.0 ±0.25 v between TP1 and TP4.

(9) Measure regulated —5.0 ±0.25v between TP1 and TP12.

(10) Voltages in Steps (6) through (9) must fall within the limits listed. In the case where voltages measured fall outside these limits, perform the test and adjustment procedures described in Paragraph 6.6.2.

(11) Depress and release the RUN/STOP switch. Verify that the disk drive comes up to speed.

(12) After approximately 33 seconds from actuation of the RUN/STOP switch, manually load heads onto the platter at or near cylinder 000.

NOTE

It is important to load the heads onto the platter at this time. If heads are not loaded, the control logic will assume an improper state. To reset, recycle power.

(13) On top load disk drives only, verify that the cleaning brushes make two complete sweeps across the platters.

(14) The positioner is now prepared for testing. With the disk drive operating in this configuration, establish the oscilloscope configuration detailed in Paragraph 6.7.1.1 and perform the static positioner adjustments described in Paragraph 6.8.

6.7.1.1 Oscilloscope Configuration

(1) Set oscilloscope as follows.

- Set sensitivity of both channels to 0.2v per division. Use X10 calibrated oscilloscope probes with ground leads.
- Set verticle input mode switch to dc unless otherwise specified.
- Set sweep rate to 10 msec per division.
- Use automatic or normal sync, and internal trigger modes.
- Use TP1 on Servo PCBA as ground reference.

(2) Maintain disk drive in operating mode established in Paragraph 6.7.1.

6.8 STATIC POSITIONER ADJUSTMENTS

The following static measurements and adjustments are required to check the integrity of the position transducer signals (amplitude and polarity), the velocity transducer feedback signal, and the voice-coil polarity.

NOTE

On 200 tpi models, connector J504 on the Temperature Compensation PCBA should be removed prior to any Servo tests or adjustments. Ensure that this connector is replaced after any test or adjustment performed on the Servo.

6.8.1 X + 0 GAIN AND BALANCE

Values are given for all versions of the D3000 with values for 200 tpi models parenthetically stated.

6.8.1.1 Test Configuration

(1) Prepare the positioner and oscilloscope as described in Paragraph 6.7.

(2) Connect Channel 1 test probe to TP20.

(3) Connect Channel 2 test probe to TP8.

(4) Select Channel 1 and position the ground referenced sweep trace on center line of the oscilloscope graticule.

NOTE

A ground referenced sweep trace is obtained by centering the trace to a particular graticule line with the verticle input mode switch set to ground position.

6.8.1.2 Test Procedure

(1) Manually move the positioner carriage back and forth through its full stroke, i.e., cylinder 000 to cylinder 202. Do not allow heads to unload from the disk.

(2) Monitor TP20 and observe the Position Reference (X + 0) waveform shown in Figure 6-4 as the positioner is being moved.

(3) If required, re-position Channel 1 sweep trace to center line of graticule.

6.8.1.3 Adjustment Procedure

(1) Adjust potentiometer R69 (X + 0 gain) to obtain a 12 ±0.8v (12 ±1.2v for 200 tpi) peak-to-peak sine wave at TP20 on the oscilloscope screen while the positioner carriage is being slowly moved by hand.

NOTE

Clockwise rotation of R69 will increase amplitude.

(2) Adjust potentiometer R70 (X +0 balance) to obtain a 12 ±0.8v (12 ±1.2v for 200 tpi) peak-to-peak sine wave centered about ground, i.e., 6v ±0.4v on either side of ground. If required, re-position the ground referenced sweep trace to the center graticule line.

NOTE

In the event that the waveform at TP20 shown in Figure 6-4 and the peak-to-peak value is not generated over the entire stroke, optical adjustment of the positioner transducer scale is required; see Paragraph 6.9.6.

(3) Set oscilloscope to the chopped mode.

(4) Position Channel 2 ground referenced sweep trace to center line of the graticule.

(5) While moving the positioner carriage by hand, concurrently monitor the signal at TP8 appearing on Channel 2 with the signal at TP20 appearing on Channel 1.

(6) The Channel 2 signal output should represent a digital signal of 0v to 5.0v that corresponds to the approximate zero crossover points of the analog signal seen on Channel 1.

NOTE

If at any time R69, R70, or the reticle of the transducer scale are adjusted, the X+0 signal peak-to-peak amplitude should be checked over the full stroke of the positioner.

6.8.2 X + 90 BALANCE

6.8.2.1 Test Configuration

(1) Prepare the positioner and oscilloscope as described in Paragraph 6.7.

(2) connect Channel 1 test probe to TP2.

(3) Set Channel 1 sensitivity to 0.5v per division.

(4) Connect Channel 2 test probe to TP13.

(5) Select Channel 1 and position ground referenced sweep trace on center line of the graticule.

(6) Maintain disk drive in operating mode established in Paragraph 6.7.1.

6.8.2.2 Test Procedure

(1) Manually move the positioner carriage back and forth through its full stroke while monitoring waveform at TP2 (X + 90) (refer to Figure 6-4).

(2) Observe an analog sine wave signal between 6v and 18v peak-to-peak at TP2. Note that either or both peaks of this signal may be clipped.

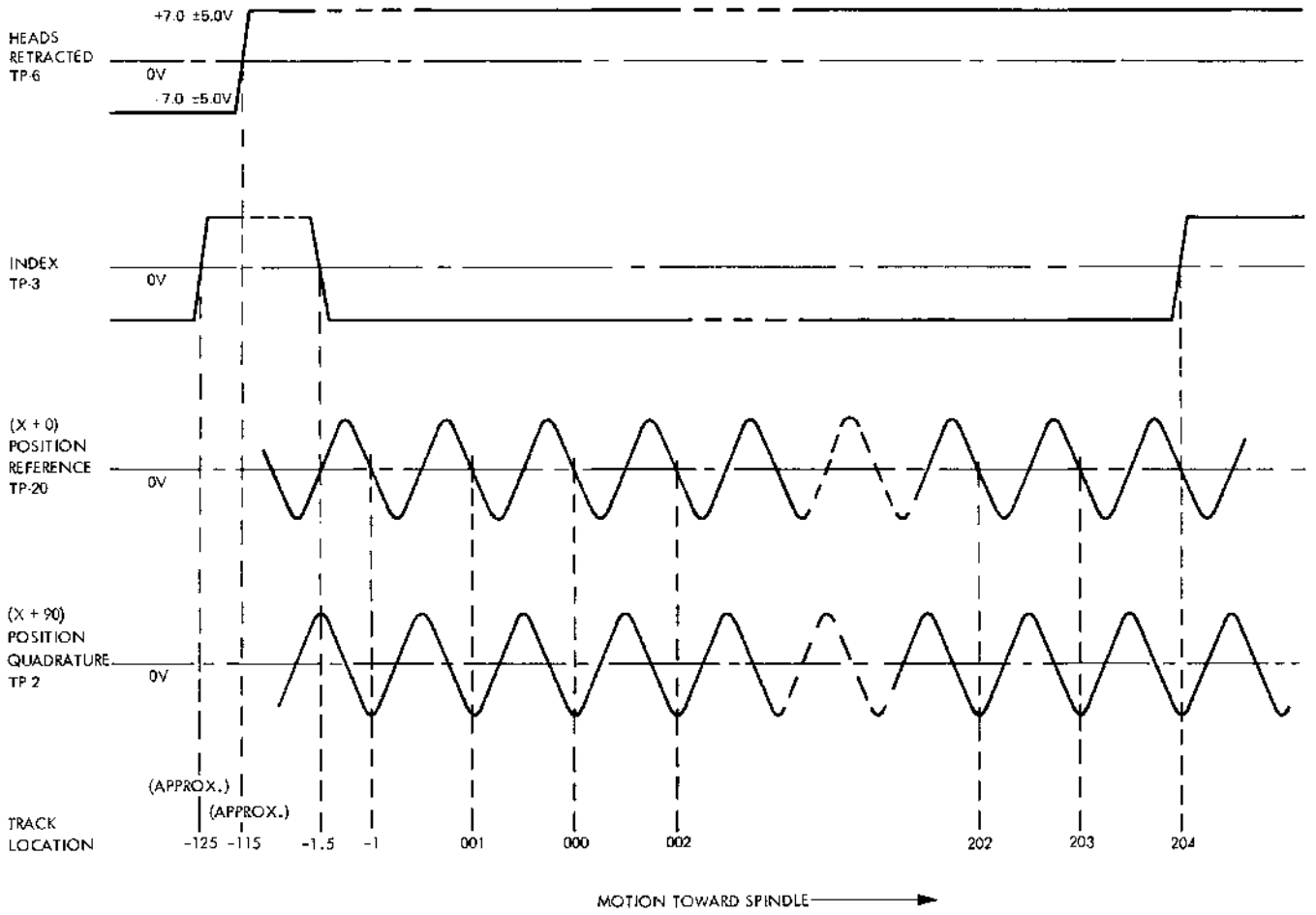


Figure 6-4. Position Transducer Signal Amplifier Outputs

6.8.2.3 Adjustment Procedure

(1) Adjust potentiometer R79 (X + 90 Balance) until the 6v to 18v peak-to-peak sine wave observed at TP2 is approximately balanced about ground, i.e., peak-to-peak value ÷ 2 (± 0.4v) about ground.

NOTE

In the event that the waveform at TP2 shown in Figure 6-4 and the peak-to-peak value of 6v to 18v is not generated over the entire stroke, optical adjustment of the position transducer scale is required. See Paragraph 6.9.6.

6.8.3 X + 0 AND X + 90 SIGNAL POLARITY AND QUADRATURE CHECK

6.8.3.1 Test Configuration

(1) Prepare the positioner and oscilloscope as described in Paragraph 6.7.

(2) Set oscilloscope to the chopped mode.

(3) Connect Channel 2 test probe to TP13.

(4) Connect Channel 1 test probe to TP2.

(5) Position the ground referenced sweep trace of both channels to the center graticule line.

(6) Maintain disk drive in the operating mode established in Paragraph 6.7.1, Steps (1) through (4) and (10).

6.8.3.2 Test Procedure

(1) Concurrently monitor signal at TP13 (Channel 2) with signal at TP2 (Channel 1) while manually moving the positioner carriage through its full stroke.

(2) The Channel 2 output should be a digital signal of 0v to 5v which corresponds to the approximate zero crossover points of the analog signal on Channel 1.

(3) Connect Channel 1 test probe to TP20.

(4) Re-adjust the gain of Channel 2 to 2v per division, and the Channel 1 gain to 0.2v per division.

(5) Set Channel Select switch to Add mode (Channel 1 plus Channel 2).

(6) Sync internally off of Channel 1 on the positive portion of the analog signal.

(7) Manually move the positioner carriage back and forth through its full stroke.

(8) Observe that the X + 90 digital signal, added to the X + 0 analog signal, appear on both the positive and negative peaks of the sine wave as illustrated in Figure 6-5.

(9) Determine that the digital signal occurs above the + 4v level on the positive peak and below the —4v level on the negative peak.

(10) While moving the positioner carriage forward (toward the spindle) check that the added digital signal has its trailing edge on the positive peak of the sine wave. (See Figure 6-5.)

NOTE

The signal observed may not be balanced about ground due to adding the two signals together.

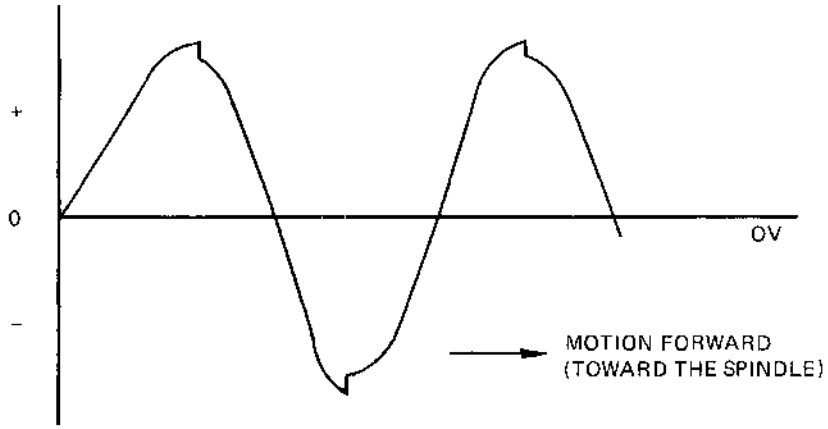


Figure 6-5. X + 0 Analog Signal Added to X + 90 Digital Signal

6.8.3.3 Adjustment Procedure

In the event that the ± 4v signal measured in Step (9) of Paragraph 6.8.3.2 cannot be obtained, refer to Paragraph 6.9.6 relating to the reticle adjustment.

6.8.4 HEADS RETRACTED SIGNAL CHECK

The Heads Retract Signal Check is made to ascertain the approximate position at which the signal occurs and to determine if the voltages generated are within acceptable limits and have the correct polarity.

6.8.4.1 Test Configuration

All test conditions remain the same as in previous tests except those changes required to perform the Heads Retract Signal Check.

(1) Connect Channel 1 test probe to TP6.

(2) Connect Channel 2 test probe to TP14.

(3) Set Channel 1 sensitivity to 0.5v per division.

(4) Set Channel 2 sensitivity to 0.2v per division.

(5) Use automatic or normal sync, internal trigger mode, and trigger on positive slope.

(6) Set sweep rate to 20 msec per division.

(7) Maintain disk drive in operating mode.

6.8.4.2 Test Procedure

(1) Retract the positioner carriage all the way to the back stop. Note that heads are unloaded and the spindle speed increases.

(2) Select Channel 1.

- Observe that the analog signal at TP6 is ≤—2v at this position. Refer to Figure 6-4.
- Slowly move the positioner carriage approximately 1/2 inch toward the spindle and at the same time observe that the signal at TP6 changes in polarity from ≤—2v to ≥+ 2v.

- Continue to move the positioner carriage slowly toward the spindle all the way to the front stop. Note that the signal voltage remains at ≥+2v as shown in Figure 6-4.

NOTE

There may be some analog crosstalk present on the signal; however, the voltage tolerances specified above must be met.

(3) Select Channel 2

- Return the positioner carriage all the way to the back stop.
- Observe that the digital signal at TP14 is high.
- Slowly move the positioner carriage approximately 1/2 inch toward the spindle and at the same time observe that the digital signal at TP14 changes from a high to a low state. See Figure 5-36.
- Continue to move positioner carriage slowly toward the spindle all the way to the front stop. Note that the signal always remains in the low state.

6.8.4.3 Adjustment Procedure

In the event that the ≥+2v signal measured in Paragraph 6.8.4.2 Step (2), cannot be obtained, refer to Paragraph 6.9.6 relating to the reticle adjustment.

6.8.5 INDEX BALANCE

The index area is located very close to where the heads are either loaded on or unloaded from the ramp. This load-unload position is within one-quarter-inch from the outside rim of the platter.

6.8.5.1 Test Configuration

(1) Prepare positioner and oscilloscope as described in Paragraph 6.7.
(2) Connect Channel 1 probe to TP3.
(3) Position Channel 1 ground referenced sweep trace on the center line of graticule.
(4) Connect Channel 2 probe to TP7.
(5) Set Channel 1 sensitivity to 0.5v per division.
(6) Set Channel 2 sensitivity to 0.2v per division.
(7) Use automatic or normal sync, internal trigger mode, and trigger on positive slope.
(8) Set sweep rate to 20 msec per division.
(9) Maintain disk drive in operating mode.

6.8.5.2 Test Procedure - Channel 1

(1) Select oscilloscope Channel 1.
(2) Within the first 1/4 inch after the heads are loaded onto the disk index area, manually move the positioner carriage back and forth.

(3) Observe a signal change on Channel 1 from ≥+ 2v to ≤—2v (refer to Figure 6-4). Adjust potentiometer R98 (Index Balance) to obtain these values.

NOTE

Clockwise adjustment of R98 will bias the signal more positive.

(4) Continue to adjust R98 until the transition region is approximately centered about ground.

NOTE

Within the ± 2v signal transition there should not be any analog crosstalk.

(5) Fully retract positioner carriage.

(6) Slowly move positioner carriage approximately 1/2 inch closer toward the spindle.

(7) Observe on Channel 1 at TP3 a signal change from ≤—2v to ≥+ 2v (refer to Figure 6-4).

(8) Moving the positioner carriage further forward toward the spindle through the index area (heads now loaded) will again reverse the signal from ≥+ 2v to ≤—2v.

(9) Ensure that the signal remains at ≤ —2v as the positioner carriage is moved through the full stroke and that this condition is maintained to a point just prior to touching the front end of the positioner assembly at approximately cylinder 203.

(10) Note that at approximately the point where the positioner carriage touches the front end of the positioner, which is approximately cylinder 204, the signal reverses once again ≤—2v to ≥+ 2v. Also observe that at each transition point only a single transition from high to low or low to high occurs.

NOTE

If a transition does not occur, adjustment of the transducer assembly position is required. Refer to Paragraph 6.9.6 for adjustment procedure.

6.8.5.3 Test Procedure - Channel 2

(1) Select oscilloscope Channel 2.

(2) Fully retract positioner carriage to the back stop.

(3) Slowly move the positioner carriage one-half-inch toward the spindle.

(4) Observe on Channel 2 that the digital signal at TP7 changes from a low to a high state. Refer to Figure 5-36.

(5) Observe, as the positioner carriage is moved forward through the index area (head now loaded), the signal changes from a high to a low state.

(6) Observe that the signal remains low as the positioner carriage is moved further toward the spindle. Ensure that this condition is maintained to a point just prior to touching the front end of the positioner assembly.

(7) Note that at approximately the end of the stroke the signal reverses again from a

low to a high state. Also note that at each transition point only a single transition of the logic state, from low to high or from high to low, occurs.

NOTE

A multiple transition occurring in the Index areas can cause an emergency unload during a normal load operation.

6.8.5.4 Adjustment Procedure

In the event that a transition does not occur near the end of the stroke, adjustment of the transducer assembly position is required. Refer to Paragraph 6.9.6 for adjustment procedure.

6.8.6 VELOCITY TRANSDUCER PHASING

This test will establish if the connections to the velocity transducer are correctly phased.

6.8.6.1 Test Configuration

(1) Prepare positioner and oscilloscope as described in Paragraph 6.7.
(2) Connect Channel 1 test probe to TP16.
(3) Set Channel 1 gain to 0.02v per division. Ensure that the polarity switch is set to the positive position.
(4) Position Channel 1 ground referenced sweep trace to the center line of graticule.
(5) Set sweep rate to 20 msec per division.
(6) Use automatic sync mode and internal trigger.

6.8.6.2 Test Procedure

(1) Manually move the positioner carriage such that the heads remain loaded and are approximately one inch in from the end of the platter.
(2) Select Channel 1.
(3) Monitor signals at TP16. The waveform at TP16 should go negative with respect to ground when the positioner carriage is moved forward toward the spindle.
(4) Return positioner carriage to the retracted position.

6.8.6.3 Adjustment Procedure

If the waveform observed at TP16 goes positive with respect to ground when the positioner carriage is moved toward the spindle (Paragraph 6.8.6.2, Step (3), reverse the wiring to pins 4 and 9 on connector J203 on the Servo PCBA.

6.8.7 POSITIONER VOICE COIL POLARITY CHECK

This test will establish that the electrical connections to the positioner voice coil have the correct polarity.

6.8.7.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.7.
(2) Insert the Voice Coil Polarity tester (PERTEC Part No. 103607) onto J205.
(3) Maintain the disk drive in the operating mode with the heads loaded onto the platter.

6.8.7.2 Test Procedure

(1) Manually move the positioner carriage forward toward the spindle in a brisk manner. Observe that the red indicator on the voice coil polarity tester becomes illuminated. Also note that the red indicator becomes extinguished and remains extinguished as the positioner carriage is moved away from the spindle.

(2) Return carriage to the retracted position.

(3) Remove power from the disk drive.

(4) Remove the voice coil polarity tester.

(5) Reconnect J205 to the Servo PCBA.

6.8.7.3 Adjustment Procedure

(1) If the red indicator on the voice coil polarity tester (PERTEC Part No. 103607) stays extinguished when the positioner carriage is moved toward the spindle and becomes illuminated when the positioner carriage is moved away from the spindle, the wiring at J205 must be reversed between pins 1 and 4, and between pins 2 and 5.

(2) Check operation by performing test procedure detailed in Paragraph 6.8.7.2.

6.9 DYNAMIC POSITIONER ADJUSTMENTS

The dynamic tests and adjustments required to ensure proper operation of the Positioner Servo are contained in the following paragraphs.

NOTE

On 200 tpi models, connector J504 on the Temperature Compensation PCBA should be removed prior to any Servo tests or adjustments. Ensure that this connector is replaced after any test or adjustment performed on the Servo.

6.9.1 INITIAL POTENTIOMETER SETTINGS

Paragraphs 6.9.1.1 through 6.9.1.4 detail the initial setting of various potentiometers located on the Servo PCBA. Adjusting the listed potentiometers to the positions given is required ONLY when the Servo PCBA, Positioner, Position Transducer, or Velocity Transducer have been replaced or when repairs have been made (i.e., parts replaced) in the 10v power supplies or the Positioner Servo circuit.

NOTE

The only ground reference test point to be used for measurement purposes is TP1. All test points referred to are located on the Servo PCBA unless otherwise noted.

6.9.1.1 Velocity Feedback Potentiometer

Adjust potentiometer R55 fully counterclockwise; then adjust to a setting of 7 turns in the clockwise direction.

6.9.1.2 Current Feedback Potentiometer

Adjust potentiometer R111 to the center position of its adjustable range which is approximately 10 turns from full counterclockwise or clockwise position.

6.9.1.3 X + 0 Offset Potentiometer

Adjust potentiometer R22 to the center position of its adjustable range which is approximately 10 turns from full ccw or full cw position.

6.9.1.4 Velocity Offset Potentiometer

Adjust potentiometer R204 to the center position of its adjustable range which is approximately 10 turns from full ccw or full cw position.

6.9.2 POSITIONER PREPARATION, DYNAMIC TESTS

The following functions are required to prepare the positioner for calibration.

(1) Remove power from the disk drive.

(2) Verify that connector J205 is connected to the Servo PCBA.

(3) Remove jumper plug J128 from the Logic PCBA.

(4) Remove the interface connector and terminator board from connectors J101 and J102 located on the Logic PCBA.

(5) Install exerciser into interface connector J101.

(6) Apply power to the disk drive and allow it to come SAFE.

(7) Insert a disk cartridge into the disk drive.

(8) Depress the START/STOP switch once and observe that the positioner loads heads after approximately 33 seconds.

(9) Observe that the disk drive comes to READY in approximately 56 seconds.

CAUTION

DURING ALL DYNAMIC CALIBRATION TESTS, IT IS REQUIRED THAT THE DISK DRIVE ROTATE THE PLATTERS AT THEIR DESIGN SPEED; OTHERWISE, DAMAGE TO PLATTERS AND HEADS WILL RESULT.

6.9.3 SETTLING RESPONSE, INITIAL ADJUSTMENTS

The settling response times will establish the operating conditions required for the velocity offset, the X + 0 offset, and the current feedback circuits.

6.9.3.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.2.

(2) Set oscilloscope as follows.

- Set Channel 1 sensitivity to 0.2v per division.
- Connect Channel 1 test probe to TP20.
- Set Channel 2 sensitivity to 0.01v per division.
- Connect Channel 2 test probe to TP16.
- Using a X10 probe, connect external trigger input to TP12 on the Logic PCBA.
- Set sweep rate to 1 msec per division.
- Use normal sync, external trigger mode, and trigger slope negative.

(3) Set the disk exerciser to perform a one-track repetitive seek from cylinder 000 to cylinder 001.

6.9.3.2 Test Procedure

(1) Select Channel 1.

(2) Observe the waveform at TP20 as shown in Figure 6-6 while performing the one-track repetitive seek. Only one cycle will appear in either the forward or reverse direction; this one cycle will be approximately balanced about ground.

(3) Determine that the overshoot of the settling waveform about the ground point does not exceed ± 3v (see Figure 6-6).

NOTE

Careful observation of the X + 0 signal at TP20 will show a small disturbance near the forward and reverse waveform peaks. This disturbance is normal and occurs at the point where the Servo switches into the Position Mode.

6.9.3.3 Adjustment Procedure

To obtain a velocity offset adjustment which is related to the waveform shown in Figure 6-7 perform the following.

(1) Set oscilloscope:

- Select Channel 2 (TP16).
- Set sweep rate to 0.5 msec per division.
- Figure 6-7 represents a one-track seek of the velocity signal at TP16 on Channel 2. Check the area enclosed within the circle to determine if the waveform is balanced around ground.

(2) If the waveform is not balanced around ground, adjust velocity offset potentiometer, R204, to obtain the balanced waveform shown in Figure 6-7.

(3) Select Channel 1 and observe the X + 0 waveform at TP20.

NOTE

Adjustment of R204 may cause the signal at TP20 to shift away from ground. If this condition is noted perform the following adjustment.

(4) Set oscilloscope as follows.

- Select Channel 1.
- Set Channel 1 gain to 0.02v per division.
- Set sweep rate to 2 msec per division and observe the waveform at TP20 as shown in Figure 6-8.

(5) Re-adjust potentiometer R22 to balance (X + 0) waveform about ground.

6.9.4 CURRENT ADJUSTMENT

Values are given for all versions of the D3000 with values for 200 tpi models parenthetically stated.

The following current adjustment procedure is made to ensure that the positioner carriage will perform a 67-track seek within a time interval of approximately 35 msec (or 134-track seek within a time interval of approximately 38 msec for 200 tpi).

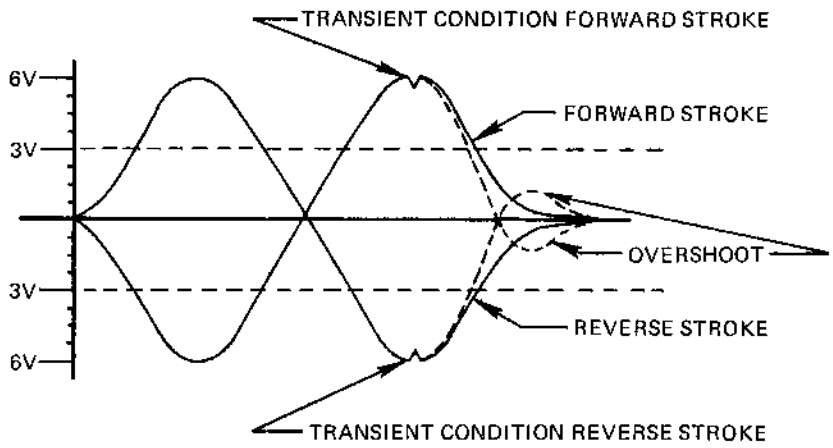


Figure 6-6. X + 0 Waveform, One-Track Seek

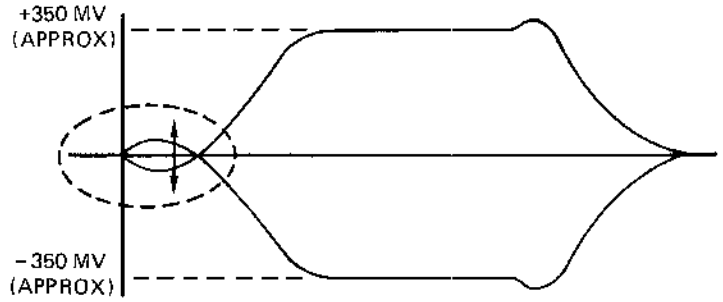


Figure 6-7. Velocity Signal at TP16, One-Track Repetitive Seek

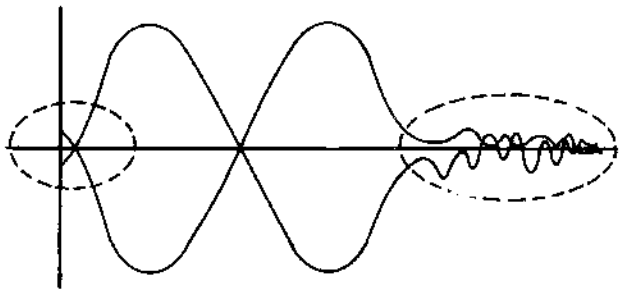


Figure 6-8. X + 0 Balanced Waveform at TP20, One-Track Repetitive Seek

6.9.4.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.2.

(2) Set the oscilloscope as follows.

- Set the Channel 1 sensitivity to 0.02v per division.
- Set sweep rate to 5 msec per division.
- Connect Channel 1 test probe to TP15.

(3) Set disk exerciser to produce a 67-track (134-track for 200 tpi) repetitive seek from cylinder 000 to cylinder 067 (134 for 200 tpi). Do not use Busy Time Delay Mode.

6.9.4.2 Test Procedure

(1) Select Channel 1.

(2) Observe the current waveform at TP15 as shown in Figure 6-9.

(3) Set oscilloscope sweep rate to 1 msec per division.

(4) Observe the waveform shown in Figure 6-10.

6.9.4.3 Adjustment Procedure

(1) Adjust potentiometer R111 to obtain the current waveform shown in Figure 6-10. The peak-to-peak value of the waveform is measured at the center line of the oscilloscope graticule.

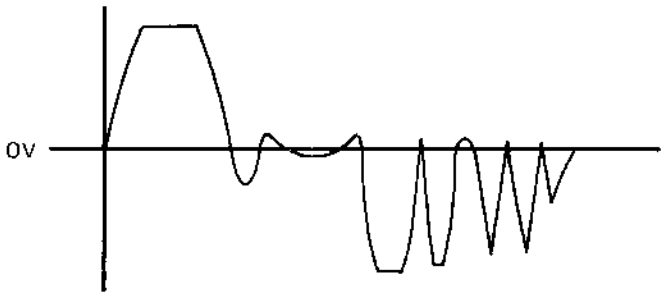


Figure 6-9. Current Waveform at TP15

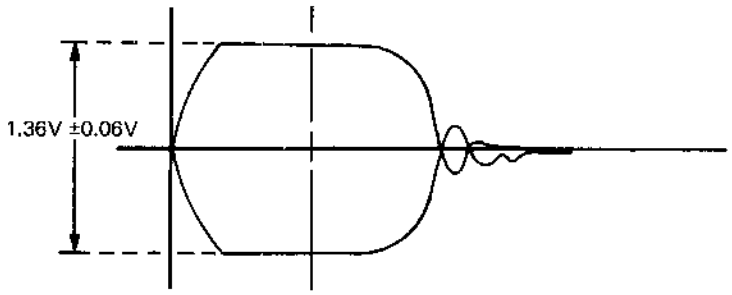


Figure 6-10. Current Waveform After Adjustment of R111

6.9.5 SEEK TIME - PRELIMINARY ADJUSTMENT

6.9.5.1 Test Configuration

(1) Prepare the positioner as described in Paragraph 6.9.2.

(2) Set oscilloscope as follows.

- Select Channel 2 (TP16).
- Set Channel 2 sensitivity to 0.2v per division.
- Set sweep rate to 5 msec per division.

6.9.5.2 Test Procedure

(1) Using the oscilloscope Channel 2 test probe, observe that the waveform at TP16 appears as shown in Figure 6-11.

6.9.5.3 Adjustment Procedure

R55 is used to establish preliminary adjustment of Seek Time prior to final adjustment detailed in Paragraph 6.9.8.

NOTE

Procedures contained in Paragraphs 6.9.6 and 6.9.7 are required prior to final Seek Time adjustments.

(1) Adjust potentiometer R55 to obtain a seek time of approximately 35 msec (38 msec for 200 tpi). When adjusting R55 look for the last step when the positioner goes into the position mode. This time is shown in Figure 6-11 occurring at approximately 30 msec (34 msec for 200 tpi).

NOTE

The following steps are performed to ensure that the X + 0 waveform is correct.

(2) Set exerciser to perform a one-track repetitive seek. Use Busy Time Delay on disk exerciser if required.

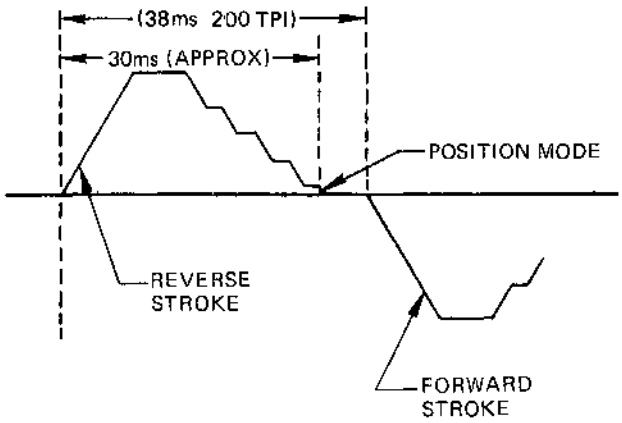


Figure 6-11. Velocity Feedback Signal Waveform, 67(134)-Track Repetitive Seek

(3) Set oscilloscope as follows.

- Set Channel 1 sensitivity to 0.2v per division.
- Connect Channel 1 test probe to TP20.
- Set Channel 2 sensitivity to 0.01v per division.
- Connect Channel 2 test probe to TP16.
- Using a X10 probe, connect external trigger input to TP12 on the Logic PCBA.
- Set sweep rate to 1 msec per division.
- Use normal sync, external trigger mode, and trigger slope negative.

(4) Recheck (X + 0) waveform at TP20 and determine that it represents the waveform shown in Figure 6-12.

(5) Readjust potentiometers R70 and/or R69 as required to obtain the waveform shown in Figure 6-12.

NOTE

If the settling waveforms do not have symmetrical overshoots or undershoots as shown in Figure 6-13, adjustment of the reticle is required. Refer to Paragraph 6.9.6.

6.9.6 RETICLE ADJUSTMENT

Adjustment of the reticle is required when the settling waveform does not have symmetrical overshoots or undershoots.

CAUTION

ONLY A SLIGHT ADJUSTMENT OF THE ANGLE BETWEEN THE RETICLE AND THE SCALE OF THE POSITION TRANSDUCER IS REQUIRED; CARELESS ADJUSTMENT MAY CAUSE LOSS OF POSITIONER TRANSDUCER SIGNALS AND ALLOW THE POSITIONER TO GO UNCONTROLLED.

6.9.6.1 Test Configuration

(1) Establish oscilloscope settings as follows.

- Set Channel 1 sensitivity to 0.2v per division.
- Connect Channel 1 test probe to TP20.
- Set Channel 2 sensitivity to 0.2v per division.
- Connect Channel 2 test probe to TP2.
- Using a X10 probe, connect external trigger input to TP12 on the Logic PCBA.
- Set sweep rate in the 1 msec per division range, or to a time base where the X + 0 waveform can be easily observed.
- Use normal sync, external trigger mode, and trigger slope negative.

(2) Set exerciser to Busy Time Delay, if required.

6.9.6.2 Test Procedure

(1) Select Channel 1.

(2) Observe an X + 0 waveform at TP20 as shown in Figure 6-12.

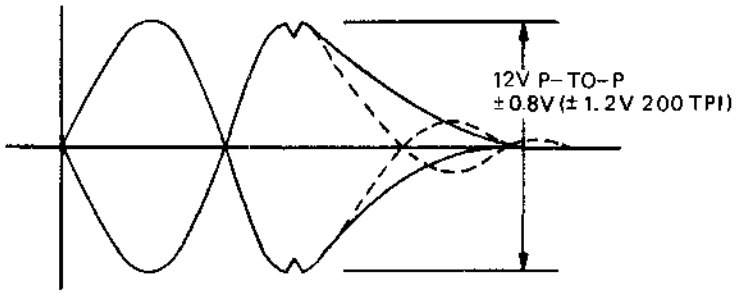


Figure 6-12. X + 0 Waveform, Overshoots and Undershoots, One-Track Repetitive Seek

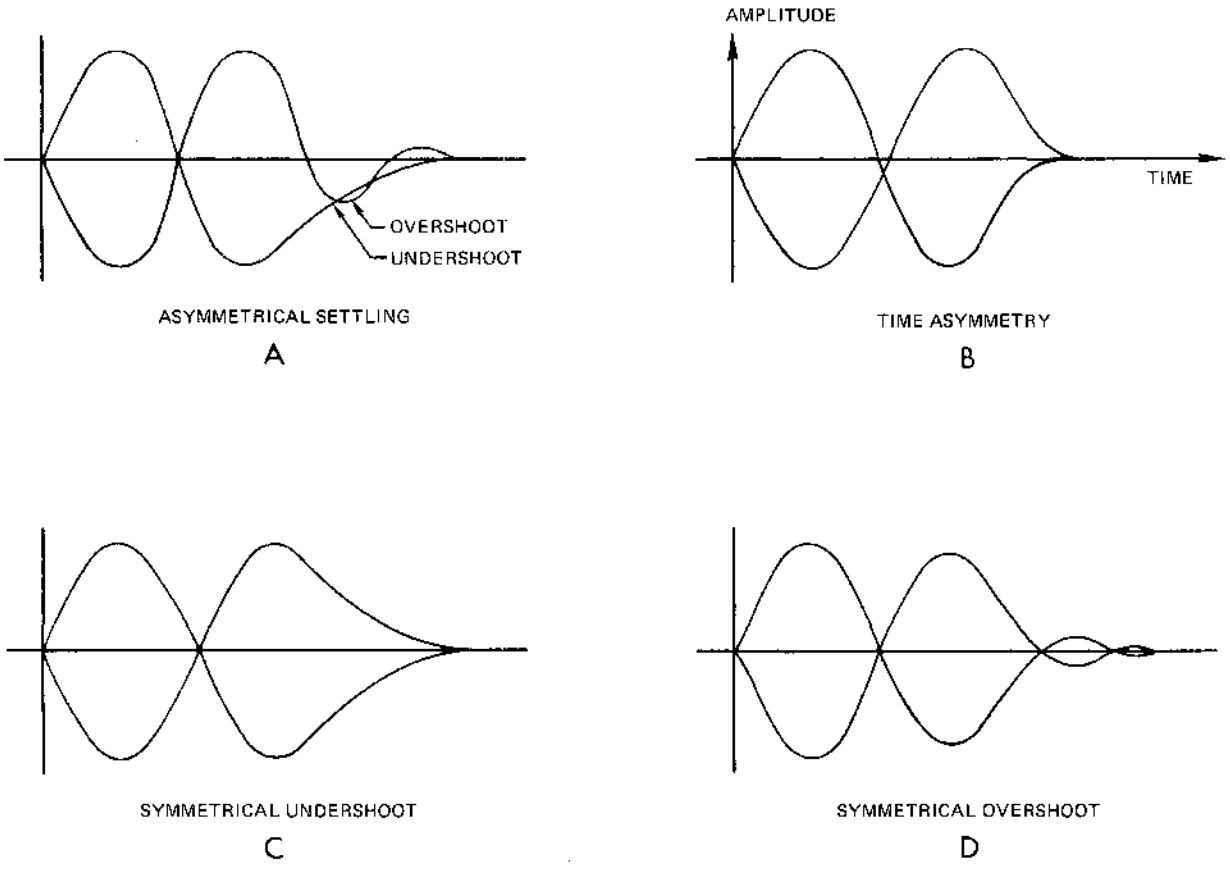


Figure 6-13. Settling Waveform Examples

6.9.6.3 Adjustment Procedure, X + 0 Waveform (100 tpi)

(1) Loosen the two machine screws which hold the reticle in place.

(2) Using the reticle adjustment tool (PERTEC Part No. 103659) very carefully adjust the reticle to obtain a symmetrical settling waveform; this waveform can have either symmetrical overshoots or undershoots as shown in Figure 6-13.

NOTE

Amplitude symmetry of the waveform is the only requirement. There can be some small asymmetric time variations between the forward and reverse seek waveforms as shown in Figure 6-13B.

NOTE

The following adjustment is made to ensure that the X + 0 waveform is balanced about ground.

(3) Adjust potentiometers R69 and/or R70 to obtain a 12 ±0.8v peak-to-peak waveform that is balanced about ground.

6.9.6.4 Adjustment Procedure, X + 0 Waveform (200 tpi)

(1) With a 5/16-inch ignition open-end wrench, loosen the bolt on the thermal block which holds the sensor receiver assembly in place.

(2) Using a Phillips screwdriver in the lens holder attaching screw, or a 1/16-inch Allen wrench in the slot on the lamp lens holder, very carefully adjust the reticle to obtain a symmetrical settling waveform. This waveform can have either symmetrical overshoots or undershoots as shown in Figure 6-13.

NOTE

Amplitude symmetry of the waveform is the only requirement. There can be some small asymmetric time variations between the forward and reverse seek waveforms as shown in Figure 6-13B.

NOTE

The following adjustment is made to ensure that the X + 0 waveform is balanced about ground.

(3) Adjust potentiometers R69 and/or R70 to obtain a 12 ±1.2v peak-to-peak waveform that is balanced about ground.

6.9.7 SETTLING RESPONSE ADJUSTMENTS, X + 0 WAVEFORM

The settling response adjustment is made to obtain a critically damped settling response of the X + 0 waveform.

6.9.7.1 Test Configuration

(1) Establish oscilloscope settings as follows.

- Set Channel 1 sensitivity to 0.2v per division.
- Connect Channel 1 test probe to TP20.
- Set Channel 2 sensitivity to 2.0v per division.
- Connect Channel 2 test probe to TP13.

- Using an X10 probe, connect external trigger input to TP12 on the Logic PCBA.
- Set sweep rate in the 1 msec per division range, or to a time base where the X + 0 waveform can be easily observed.
- Use normal sync, external trigger mode, and trigger slope negative.

(2) Set exerciser to perform one-track repetitive seek from track 00 to track 01.

(3) Set exerciser to Busy Time Delay, if required.

6.9.7.2 Test Procedure

(1) Select Channel 1. Observe that the X + 0 waveform at TP20 has a critically damped settling response as shown in Figure 6-14A. If the observed settling response is different than that shown in Figure 6-14A, perform the adjustment procedure in Paragraph 6.9.7.3.

(2) Set Channel Select switch to ADD. Observe that the SPQCG signal added to X + 0 waveform occurs at greater than + 4v on the positive peak and more negative than —4v on the negative peak when balanced about ground as shown in Figure 6-14B (sweep rate of 0.5 msec per division may be desirable). If the observed waveform is different than that shown in Figure 6-14B, perform the adjustment procedure contained in Paragraph 6.9.7.3.

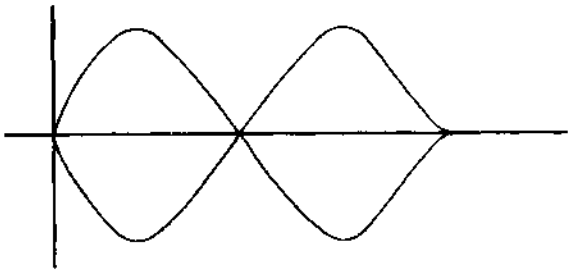


Figure 6-14A. X + 0 Waveform, Critically Damped, One-Track Repetitive Seek

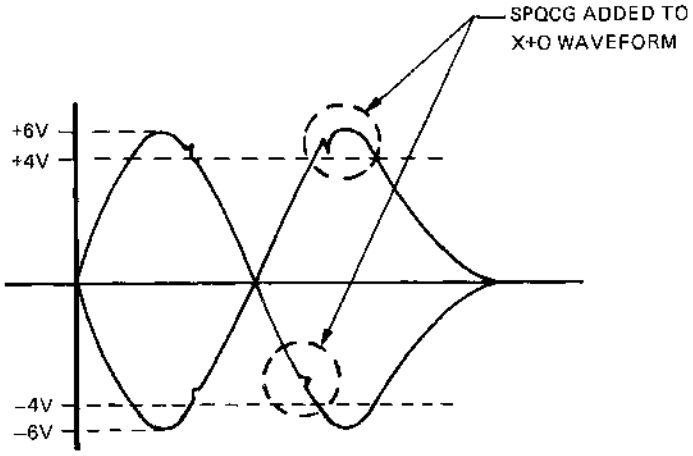


Figure 6-14B. SPQCG Signal Added to X + 0 Waveform, One-Track Repetitive Seek

(3) Select Channel 2 and change sensitivity to 0.2v per division; connect Channel 2 test probe to TP2. For 100 tpi models observe that the X + 90 waveform at TP2 has transitions of +2v or greater about ground reference as shown in Figure 6-15A; for 200 tpi models observe that the X + 90 waveform at TP2 has transitions balanced around ground reference as shown in Figure 6-15B. If the observed waveform is different than that shown in Figure 6-15A or B, perform the adjustment procedure in Paragraph 6.9.7.3 or 6.9.7.4.

6.9.7.3 Adjustment Procedure (100 tpi)

(1) Select Channel 2. Adjust potentiometer R79 (X + 90 Balance) until the X + 90 waveform at TP2 has its positive peak at +3v above ground potential (see Figure 6-15A).

NOTE

It is possible that potentiometer R79 may run out of adjustable range before the X + 90 waveform is adjusted to the +3v positive peak. In this case, leave the R79 setting at the minimum positive level of the X + 90 waveform peak obtainable that is greater than +3v.

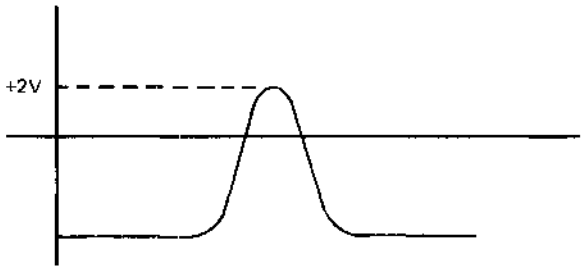


Figure 6-15A. X + 90 Waveform, One-Track Repetitive Seek (100 tpi)

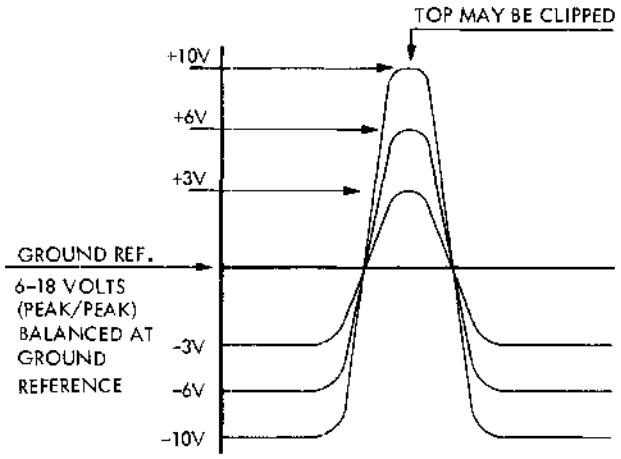


Figure 6-15B. X + 90 Waveform, One-Track Repetitive Seek (200 tpi)

(2) Select Channel 1. Observe settling response of the X + 0 waveform at TP20. If the response is over-damped (e.g., a response with undershoots), adjust R79 clockwise to obtain a critically damped settling response. If the response is underdamped, adjust R79 counterclockwise to obtain a critically damped settling response; see Figure 6-14A.

NOTE

A critically damped settling response may not be obtained by adjusting R79, yet meet the criterion of Paragraph 6.9.7.2 Step [3]; in this case, obtain the best settling response and check that it passes the test in Paragraph 6.10.

(3) Select Channel 2. Establish that the X + 90 waveform at TP2 has transitions of ± 2v or greater about ground reference as shown in Figure 6-15A; adjust R79 if necessary.

(4) Connect Channel 2 test probe to TP13. Change Channel 2 sensitivity to 2v per division. Set Channel Select switch to ADD. Observe that SPQCG signal added to X + 0 waveform occurs at greater than + 4v on the positive peak and more negative than —4v on the negative peak when balanced about ground as shown in Figure 6-14B (sweep rate of 0.5 msec per division may be desirable). Adjust R79 if necessary.

6.9.7.4 Adjustment Procedure (200 tpi)

(1) Select Channel 2. Adjust potentiometer R79 (X + 90) and balance until the X + 90 waveform at TP2 is balanced at ground.

(2) Select Channel 1. Observe the settling response of the X + 0 waveform at TP20; if the response overshoots greater than + 2v about ground readjust the reticle (Paragraph 6.9.6.4).

(3) Select Channel 2. Establish that the X + 90 waveform at TP2 has transitions balanced about ground reference as shown in Figure 6-15B; adjust R79 if necessary.

(4) Connect Channel 2 test probe to TP13. Change Channel 2 sensitivity to 2v per division. Set Channel Select switch to ADD. Observe that SPQCG signal added to X + 0 waveform occurs at greater than + 4v on the positive peak and more negative than —4v on the negative peak when balanced about ground as shown in Figure 6-14B. (Sweep rate of 0.5 msec per division may be desirable.)

6.9.8. SEEK TIME FINAL ADJUSTMENTS

The final seek time adjustments are performed subsequent to the preliminary adjustments contained in Paragraphs 6.9.5 through 6.9.7 and are used to check and adjust the positioner carriage seek times for a 67-track (134-track for 200 tpi), a 202-track (405-track for 200 tpi), and a one-track seek. The final adjustment of the X + 0 waveform settling response is also made at this time.

Values are given for all versions of the D3000 with values for 200 tpi models parenthetically stated.

6.9.8.1 Test Configuration — Step 1

(1) Set the oscilloscope as follows.

- Set Channel 1 sensitivity to 0.2v per division.
- Set sweep rate to 5 msec per division.
- Connect Channel 1 test probe to TP12 on the Logic PCBA.
- Set Channel 2 sensitivity to 0.2v per division.
- Connect Channel 2 test probe to TP16.

(2) Set the exerciser to perform a 67-track (134-track for 200 tpi) repetitive seek between cylinder 000 and 067 (000 and 134 for 200 tpi). Use Busy Time Delay.

6.9.8.2 Test Procedure — Step 1

(1) Set the oscilloscope to Chopped Mode. Observe the velocity profile at TP16 on Channel 2 in relationship to the Busy Signal (NLBSXG) on Channel 1. See Figure 6-16. Measure the seek time between the beginning of the seek, when NLBSXG goes from a logic high to a low state, to the end of the seek when NLBSXG goes from a logic low to a high state.

(2) Observe that the seek time for a 67-track (134-track for 200 tpi) seek, either a forward or a reverse stroke, should be less than or equal to 34.2 msec (37 msec for 200 tpi); if the seek time is greater, perform the adjustments detailed in Paragraph 6.9.8.3.

(3) Select Channel 2. Observe the velocity profile at TP16 for a 67-track (134-track) seek for both a forward and a reverse stroke. Ensure that all velocity steps are met as shown in Figure 6-16.

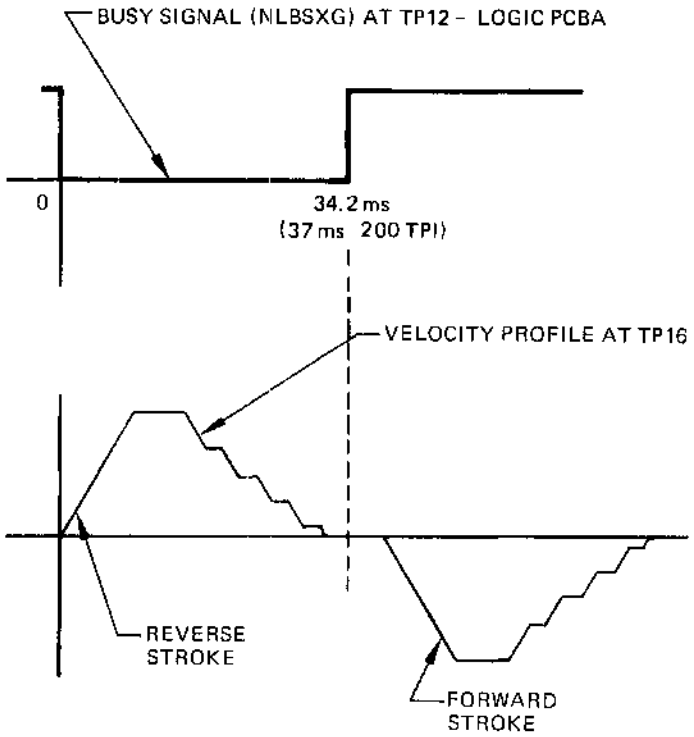


Figure 6-16. Velocity Profile Waveform, 67-Track (134-Track for 200 tpi) Repetitive Seek

6.9.8.3 Adjustment Procedure — Step 1

(1) Set the oscilloscope to Chopped Mode.

(2) Adjust velocity feedback potentiometer R55 so that the seek time measured in Step (1) of Paragraph 6.9.8.2, is 34.2 msec (38 msec for 200 tpi).

(3) Recheck the X+0 settling response waveform per Paragraph 6.9.7; adjust if necessary.

(4) Re-establish the test configuration detailed in Paragraph 6.9.8.1.

(5) Set the oscilloscope to the Chopped Mode. Measure the velocity profile at TP16 on Channel 2 in relationship to the Busy Signal (NLBSXG) on Channel 1. Re-adjust R55 for a seek time of 34.2 msec (38 msec for 200 tpi).

NOTE

Perform velocity offset adjustments of Paragraph 6.9.3.3, if required.

6.9.8.4 Test Configuration — Step 2

(1) Set oscilloscope as follows.

- Set Channel 1 sensitivity to 0.2v per division.
- Connect Channel 1 test probe to TP20.
- Set sweep rate to 10 msec per division.
- Set Channel 2 sensitivity to 0.2v per division.
- Connect Channel 2 test probe to TP16.

(2) Set the exerciser to perform a 202-track (405-track for 200 tpi) repetitive seek.

6.9.8.5 Test Procedure — Step 2

(1) Select Channel 1.

(2) Observe the X+0 waveform at TP20. When the positioner is in the positive mode, note that the settling waveform does not have any overshoots greater than 2.0v.

(3) Select Channel 2.

(4) Observe that the velocity profile signal at TP16 conforms to the waveform shown in Figure 6-17. Adjust oscilloscope trigger as required.

6.9.8.6 Adjustment Procedure — Step 2

If overshoots of greater than ±2v are observed, perform the settling response adjustments detailed in Paragraph 6.9.7.

6.9.8.7 Test Configuration — Step 3

(1) Set oscilloscope as follows.

- Set Channel 1 sensitivity to 0.02v per division.
- Connect Channel 1 test probe to TP20.
- Set Channel 2 sensitivity to 0.2v per division.
- Connect Channel 2 test probe to TP12 on Logic PCBA.
- Set sweep rate to 2 msec per division.
- Set channel select switch to Chopped Mode.

(2) Set up exerciser to perform a one-track repetitive seek.

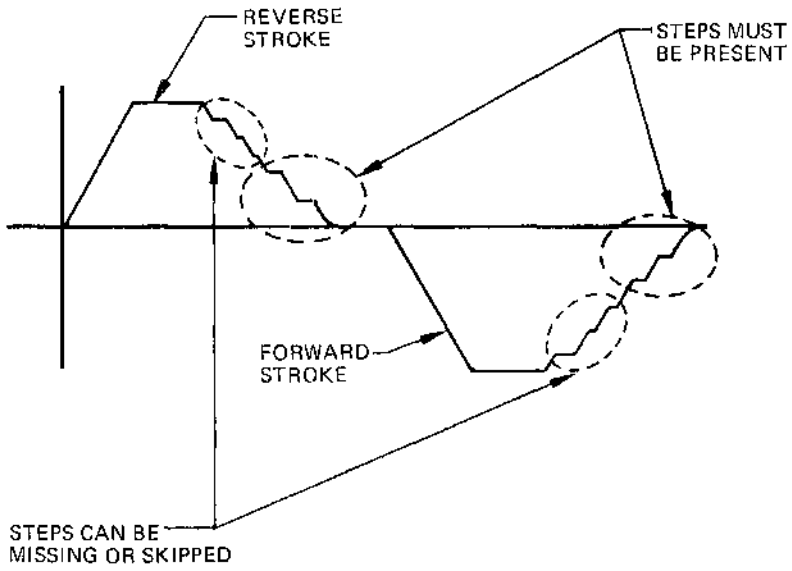


Figure 6-17. Velocity Profile Waveform Check, 202-Track (405-Track for 200 tpi) Repetitive Seek

6.9.8.8 Test Procedure — Step 3

(1) Observe the X + 0 waveform at TP20 as shown in Figure 6-18.

(2) Determine that the settling band does not exceed ±0.8v about ground after the signal at TP12 goes high.

6.9.8.9 Adjustment Procedure — Step 3

(1) If settling band limits of ±0.8v established in Paragraph 6.9.8.8 are exceeded, perform the settling response adjustments detailed in Paragraph 6.9.7.

6.9.9. INDEX TO QUADRATURE CLOCK RELATIONSHIP

This adjustment is used to correctly establish the relationship between the trailing edge of the Quadrature Clock (SPQCG) with respect to the trailing edge of the Index Logic Signal (SPTIG) as shown in Figure 6-19.

6.9.9.1 Test Configuration — Step 1

(1) Set oscilloscope as follows.

- Set sensitivity of both channels to 0.2v per division.
- Connect Channel 1 test probe to TP7.
- Connect Channel 2 test probe to TP13.
- Sync internal on Channel 1, use positive trigger slope.
- Set sweep rate to 1 msec per division.
- Set channel select switch to the Chopped Mode.

(2) Set exerciser to operate in the repetitive restore mode.

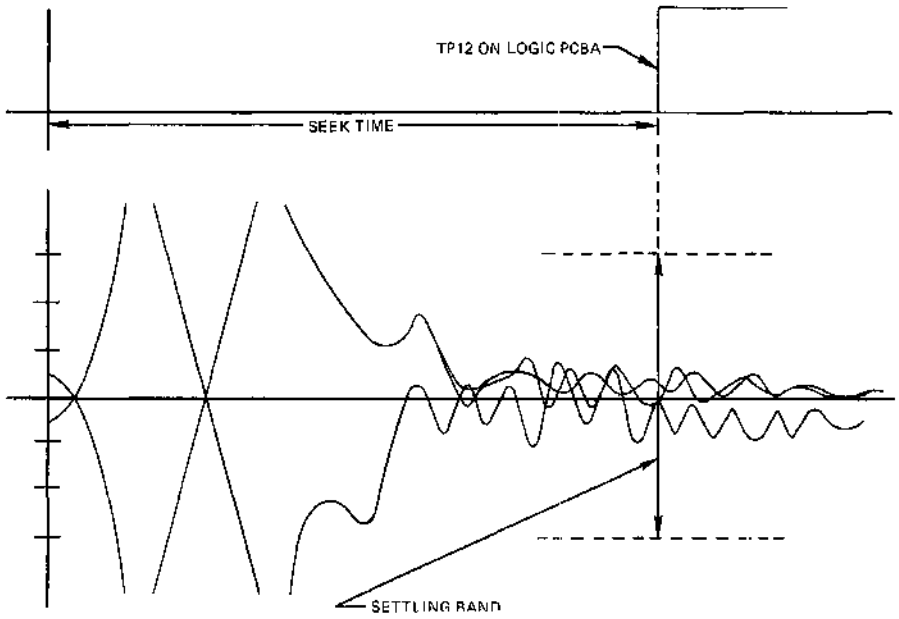


Figure 6-18. Symmetrical Settling Waveform About Ground
(Sensitivity Increased to Show Waveform Detail)

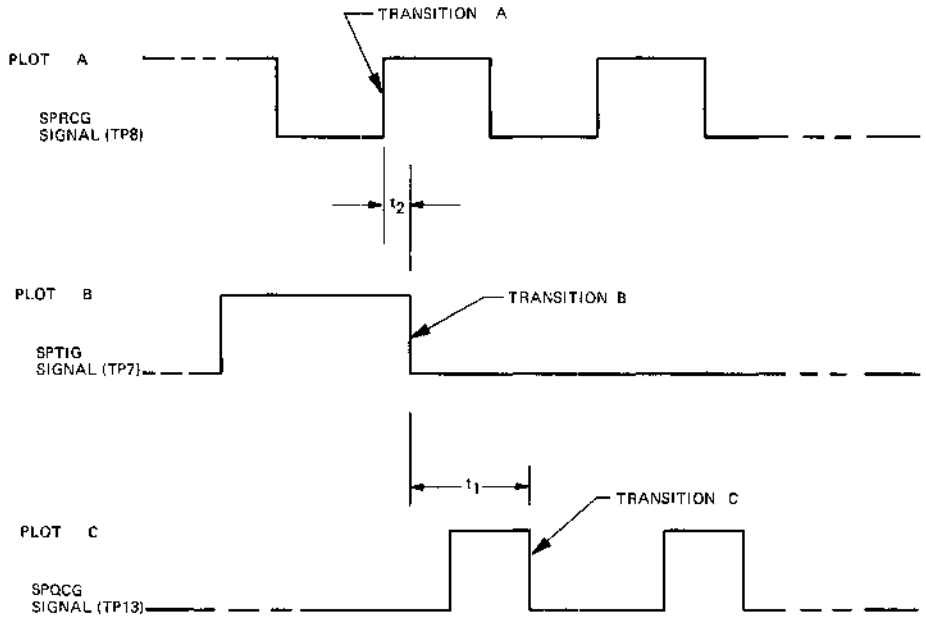


Figure 6-19. SPRCG, SPTIG, SPQCG Signals, Repetitive Restore Mode

6.9.9.2 Test Procedure — Step 1

(1) Observe the relative position of the high to low transition of signal SPQCG on Channel 2 (TP13) in relation to the high to low transition of signal SPTIG on Channel 1 (TP7). The waveform relationship must be approximately as shown in Figure 6-19, Plots B and C.

NOTE

There must be exactly two high to low transitions of SPQCG signal after the high to low transition of SPTIG signal. However, there can be one or two low to high TRANSITIONS OF SPQCG after the high to low transition of SPTIG.

(2) Connect Channel 2 test probe to TP8. Observe SPRCG on Channel 2 in relation to the high to low transition of SPTIG (see Figure 6-19, Plots A and B).

NOTE

After the high to low transition of SPTIG, there must be exactly one low to high transition and either one or two high to low transitions of SPRCG.

NOTE

When this procedure is performed on 200 tpi models, stable nulls for either of two distinct tracks may result. A CE check should be made after performing an index adjustment. If the CE track has shifted and fixed disk information is not required, readjust the heads. If fixed disk information is required, readjust the index.

(3) The high to low transition of SPTIG (transition B of Figure 6-19) should occur at or after the low to high transition of SPRCG (transition A of Figure 6-19), i.e., time t_2 should be greater than or equal to zero seconds.

NOTE

If the requirements of Paragraph 6.9.9.2 are not satisfied, perform the adjustment procedure outlined in Paragraph 6.9.9.3. If adjustments to satisfy the above requirements cannot be made, replacement of position transducer scale may be necessary.

(4) Change the oscilloscope settings established in Paragraph 6.9.9.1 as follows.

- Connect Channel 2 test probe to TP13.
- Sync internal on Channel 1, use negative trigger slope.

NOTE

It may be necessary to change the sweep rate to a more desirable setting.

(5) Observe the first high to low transition of SPQCG (TP13) with respect to the high to low transition of SPTIG (TP7) signal (see Figure 6-20).

NOTE

The high to low transition of SPQCG [transition C of Figure 6-20] should occur after a time delay [t_1] of 200 μsec or greater, after the occurrance of high to low transition of SPTIG [transition B of Figure 6-20]. See Figure 6-19, Plots B and C, and Figure 6-20.

6.9.9.3 Adjustment Procedure — Step 1

(1) Adjust Index Balance potentiometer R98 to position the trailing edge of SPTIG (TP7) to occur prior to the trailing edge of SPQCG (TP13) as shown in Figure 6-19.

(2) Change the oscilloscope settings established in Paragraph 6.9.9.2 as follows.

- Set sweep rate to 50 μsec per division.
- Sync internal on Channel 1, use negative trigger slope.

(3) Continue to adjust potentiometer R98 so that the high to low transition of SPTIG occurs approximately 300 ±100μsec before the high to low transition of SPQCG as shown in Figure 6-20.

NOTE

Change sweep rate if required.

6.9.9.4 Test Configuration — Step 2

(1) Set oscilloscope as follows.

- Set Channel 1 sensitivity to 0.5v per division.
- Connect Channel 1 test probe to TP3.
- Set sweep rate to 1 msec per division.
- Sync internal on Channel 1, use positive trigger slope.
- Set Channel 1 ground referenced sweep trace to the center line of graticule.

(2) Exerciser remains operating in the repetitive restore mode.

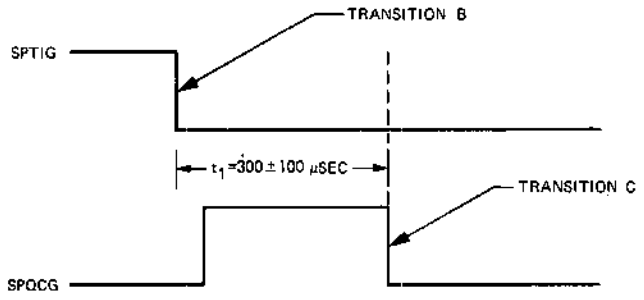


Figure 6-20. Correct Relationship Between SPQCG and SPTIG Signals, Expanded

6.9.9.5 Test Procedure — Step 2

(1) Select Channel 1.

(2) Observe that the Index signal at TP3 has at least a ±2.0v transition about ground as shown in Figure 6-21.

6.9.9.6 Adjustment Procedure — Step 2

(1) Readjust Index Balance potentiometer R98 to obtain a ±2.0v or greater transition of the index waveform about ground as shown in Figure 6-21.

(2) Ensure that the relationship between SPQCG and SPTIG established in Paragraph 6.9.9.3 Step (3) is maintained.

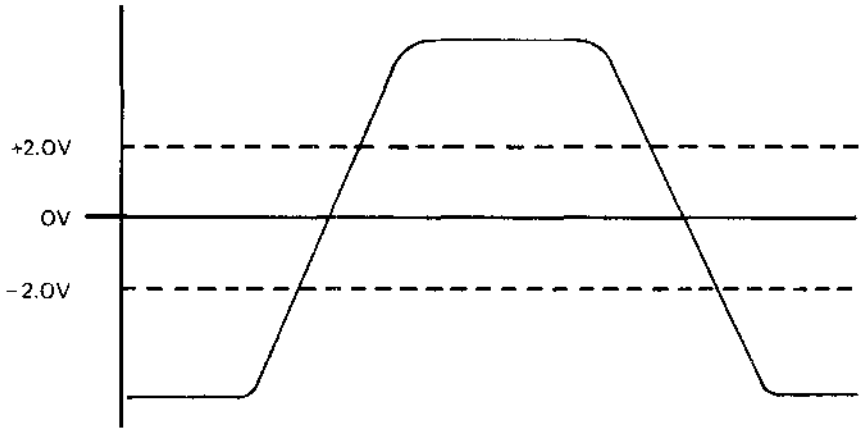


Figure 6-21. Index Signal, TP3, Repetitive Restore Mode

6.10 PERFORMANCE CHECKS

The performance checks detailed in Paragraphs 6.10.1 through 6.10.9 should be made after making any adjustments to ensure that the access and settling time parameters meet the design specifications of the disk drive. Values are given for all versions of the D3000 with values for 200 tpi models parenthetically stated.

NOTE

On 200 tpi models, connector J504 on the Temperature Compensation PCBA should be removed prior to any Servo tests or adjustments. Ensure that this connector is replaced after any test or adjustment performed on the Servo.

NOTE

All test points are on the Servo PCBA, unless otherwise noted. TP1 is used as the test probe ground.

6.10.1 TEST CONFIGURATION

(1) Set the oscilloscope as follows.

- Set Channel 1 sensitivity to 0.2v per division.
- Set Channel 2 sensitivity to 0.02v per division.
- Connect Channel 1 test probe to TP12 on Logic PCBA (NLBSXG Busy Signal).
- Connect Channel 2 test probe to TP20 (X + 0 signal).
- Use normal sync, chopped mode and external trigger. Trigger on Channel 1 using negative trigger slope.

(2) Apply power to the disk drive.

(3) After the SAFE indicator becomes illuminated, insert a disk cartridge into the disk drive.

(4) Actuate the RUN/STOP switch once and observe that the disk drive comes READY in approximately 56 seconds.

6.10.2 TEST PROCEDURE — ONE TRACK REPETITIVE SEEK (000 TO 001)

(1) Set oscilloscope sweep rate to 2 msec per division.

(2) Set exerciser to perform a repetitive seek between cylinder 000 to cylinder 001 Use Busy Time Delay.

(3) Observe the X + 0 signal at TP20 with respect to the Busy Signal (NLBSXG) at TP12 on the Logic PCBA.

(4) The X + 0 waveform at TP20 must settle within ±0.8v about ground after the Busy Signal goes high; refer to Figure 6-18.

(5) The Busy Signal observed at TP12 must go high in less than 9 msec (10 msec for 200 tpi) from the start of the seek (i.e., seek time).

6.10.3 TEST PROCEDURE — REPETITIVE 67-TRACK SEEK (000 TO 067) (134-TRACK SEEK, 000 TO 134 FOR 200 TPI)

(1) Change oscilloscope sweep rate to 5 msec per division.

(2) Set exerciser to perform a 67-track (134-track for 200 tpi) repetitive seek.

(3) The X + 0 waveform at TP20 must settle within ±0.8v about ground after the Busy Signal goes high; refer to Figure 6-18.

(4) The seek time for the 67-track seek (134-track for 200 tpi) must be less than 35 msec (40 msec for 200 tpi) in both forward and reverse directions.

6.10.4 TEST PROCEDURE — REPETITIVE 202-TRACK SEEK (405-TRACK FOR 200 TPI)

(1) Change oscilloscope sweep rate to 10 msec per division.

(2) Set exerciser to perform a 202-track (405-track for 200 tpi) repetitive seek.

(3) The X + 0 waveform at TP20 must settle within ±0.8v about ground after the Busy Signal goes high; refer to Figure 6-18.

(4) The time for a 202-track (405-track for 200 tpi) must be less than 60 msec (65 msec for 200 tpi) in both the forward and reverse directions.

6.10.5 TEST PROCEDURE — FORWARD ONE TRACK INCREMENTAL SEEK

(1) Change oscilloscope sweep rate to 2 msec per division.

(2) Set exerciser to perform an incremental one track seek in the forward direction.

(3) The X + 0 waveform at TP20 must settle within ±0.8v about ground after the Busy Signal goes high. Refer to Figure 6-18.

(4) Set Channel 2 sensitivity to 0.2v per division.

(5) The X + 0 signal at TP20 must not have overshoots which exceed ±2.0v around ground. See Figure 6-22.

6.10.6 TEST PROCEDURE — REVERSE ONE TRACK INCREMENTAL SEEK

(1) Set exerciser to perform a one-track reverse seek starting at track 202 (track 405 for 200 tpi) and repeat the test procedure detailed in Paragraph 6.10.5.

6.10.7 TEST PROCEDURE — INCREMENTAL SEEKS

(1) Change oscilloscope settings as follows.

- Set Channel 2 sensitivity at 0.02v per division.
- Set sweep rate to 10 msec per division.

(2) Set exerciser to perform 0 to N-incremental track seeks (crescendo mode).

(3) Repeat Steps (3), (4), and (5) of Paragraph 6.10.5.

6.10.8 TEST PROCEDURE — DECREMENTAL SEEKS

(1) Oscilloscope settings remain as established in Paragraph 6.10.7.

(2) Set exerciser to perform 0 to N-decremental track seeks (crescendo mode).

(3) Repeat Steps (3), (4), and (5) of Paragraph 6.10.5.

NOTE

Seek time checks are not required for procedures in Paragraphs 6.10.7 and 6.10.8.

6.10.9 ADJUSTMENT PROCEDURES

If the test specifications detailed in Paragraphs 6.10.1 through 6.10.8 are not satisfied, refer to the Positioner Servo Dynamic adjustment procedures beginning with Paragraph 6.9.

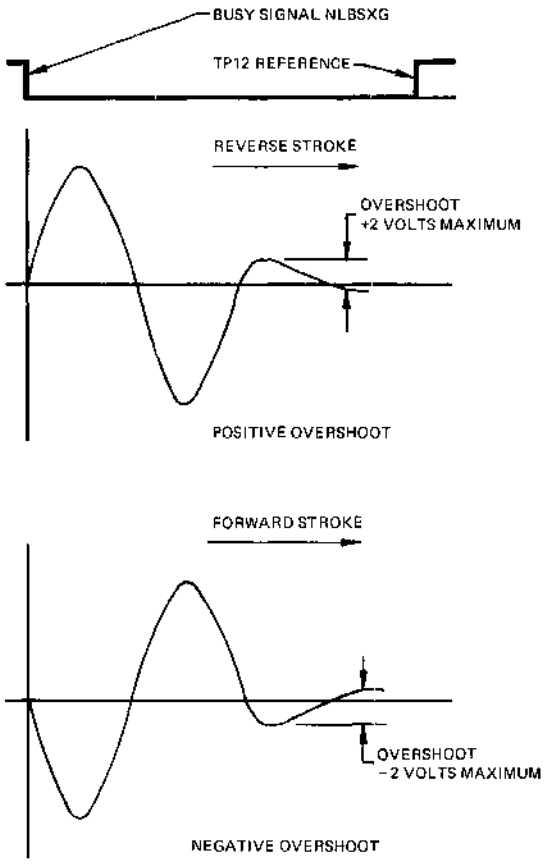


Figure 6-22. X + 0 Waveform Overshoots

6.10.10 SPINDLE SPEED ACCURACY TEST

This test verifies the spindle speed control accuracy and is a functional integrity check of the control loop.

6.10.11 TEST CONFIGURATION

(1) Apply power to the disk drive.

(2) After the SAFE indicator becomes illuminated, insert a disk cartridge into the disk drive.

(3) Actuate the RUN/STOP switch once and observe that the disk drive comes READY in approximately 56 seconds.

(4) Connect an electronic counter to TP7 on the Logic PCBA using a X10 oscilloscope probe.

(5) Use TP1 as a ground reference.

(6) Set the counter as follows.

- Period measurement with 1 μsec (1 MHz) time base.
- Trigger at the maximum readable sampling rate (use negative slope, if applicable).

6.10.12 TEST PROCEDURE

The minimum and maximum readings obtained during a 30-second observation time should be within the limits tabulated in Table 6-4.

6.10.13 ADJUSTMENT PROCEDURE

If the requirements specified in Table 6-4 are not satisfied, perform the ac motor speed control adjustment procedure detailed in Paragraph 6.6.3.

Table 6-4

Spindle Speeds

Nominal Spindle Speed	Minimum Revolution Time	Maximum Revolution Time
1500 rpm	39,600 μsec	40,400 μsec
2400 rpm	24,750 μsec	25,250 μsec

6.11 SECTOR PHASE LOCK LOOP ADJUSTMENT

The sector phase lock loop adjustment establishes the correct relationship between the phase lock pulse signal and the Voltage Controlled Oscillator (VCO) countdown signal. This relationship is shown in Figure 6-23.

NOTE

Each signal should be of the same frequency and should correspond on a cycle-to-cycle basis.

6.11.1 TEST CONFIGURATION

(1) Set oscilloscope as follows.

- Set vertical sensitivity of both channels to 0.2v per cm.
- Set channel select switch to the Chopped Mode.
- Trigger internal from Channel 1; use positive trigger slope.
- For 1500 rpm disk drives, set the sweep at 0.5 msec per division; for 2400 rpm disk drives, set the sweep at 0.2 msec per division.

(2) Connect test probe ground clips to TP15 on the Logic PCBA.

(3) Connect Channel 1 test probe to TP11 on the Logic PCBA.

(4) Connect Channel 2 test probe to TP8 on the Logic PCBA.

(5) Apply power to the disk drive. When the SAFE indicator becomes illuminated, insert a disk cartridge. Depress the RUN/STOP switch once and allow the disk drive to come Ready as indicated by the READY indicator being illuminated.

NOTE

A square wave should be observed on Channels 1 and 2 as the disk drive comes up to speed.

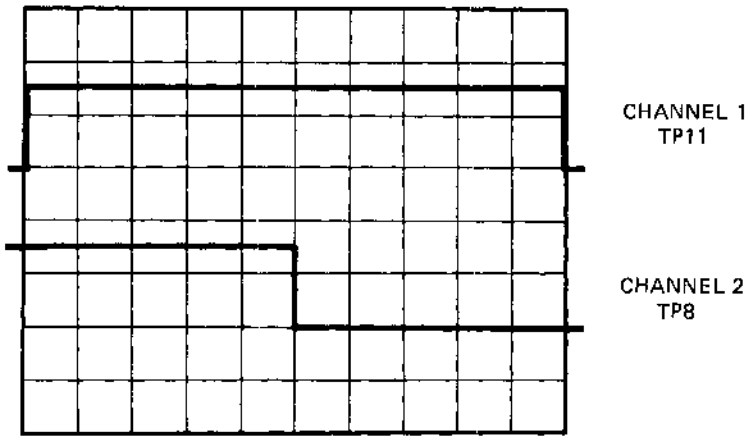


Figure 6-23. Quadrature Relationship Between Sector Phase Lock Loop Square Waves

6.11.2 TEST PROCEDURE

(1) Adjust Channel 1 trigger to display the low to high transition waveform. Adjust the sweep rate and horizontal position controls to position the leading and trailing edge of the waveform exactly 10 divisions apart. Refer to Figure 6-23.

(2) Observe the waveform on Channel 2. The high to low transition should occur at the center vertical graticule line within ±1/2 of a major division. Refer to Figure 6-23.

NOTE

This relationship is specified for an ambient [room] temperature of 23 ±5 degrees C [73.4 ±9 degrees F].

(3) If the relationship established in Steps (1) and (2) is not correct, and the spindle speed accuracy has been verified, perform the adjustment procedure detailed in Paragraph 6.11.3.

6.11.3 ADJUSTMENT PROCEDURE

(1) Adjust the Sector Phase Lock Loop centering potentiometer R57 to position the high to low transition of the waveform on Channel 2 (TP8) to the center vertical graticule line.

(2) Refer to Figure 6-23 for the correct positioning of the waveform

NOTE

This adjustment should be made at a room temperature of 23 ±5 degrees C [73.4 ±9 degrees F].

6.12 READ DECODE CIRCUIT ADJUSTMENTS

The following circuit adjustments are relevant to Read/Write Assembly 103751 (refer to schematic 103750).

NOTE

The oscilloscope time base must be calibrated either via exterior calibration device or using the 10 MHz oscillator on the Logic PCBA.

6.12.1 RPN PULSE WIDTH ADJUSTMENT

6.12.1.1 Test Configuration

(1) Remove the interface connector and terminator PCBA from connector J101 and J102 on the Logic PCBA.

(2) Connect a disk exerciser having read/write capability to J101 or J102 on the Logic PCBA.

(3) Apply power to the exerciser and the disk drive. Observe that the READY indicator is illuminated; allow a 5-minute warm up period.

(4) Write an all-zeros pattern via the disk exerciser.

(5) Connect oscilloscope Channel 1 probe to TP25. Connect the test probe ground clip to ground reference TP17.

(6) Position sweep trace 1.5 cm below centerline of graticule.

(7) Set oscilloscope Channel 1 sensitivity to 0.10v per division.

(8) Set sync to internal, normal mode.

(9) Set oscilloscope to trigger on the position slope of RPN.

6.12.1.2 Test Procedure

(1) Establish test configuration described in Paragraph 6.12.1.1.

(2) Observe RPN waveform on oscilloscope Channel 1 (TP25) as shown in Figure 6-24.

(3) Measure RPN pulse width at the 50 percent points (on oscilloscope center line).

(4) Acceptable Limits

- 40 nanoseconds (minimum)
- 45 nanoseconds (maximum)

6.12.1.3 Adjustment Procedure

When the acceptable limits are exceeded the following adjustment is performed.

(1) Establish test configuration detailed in Paragraph 6.12.1.1.

(2) Adjust R157 on the Read/Write PCBA to 42 nanoseconds.

6.12.2 'ONES' WINDOW SETTING

6.12.2.1 Test Configuration

(1) Remove the interface connector and terminator PCBA from connector J101 and J102 on the Logic PCBA.

(2) Connect a disk exerciser having read/write capability to J101 or J102 on the Logic PCBA.

(3) Apply power to the exerciser and the disk drive. Observe that the READY indicator is illuminated; allow a 5-minute warm up period.

(4) Write an all-zeros pattern via the disk exerciser.

(5) Connect oscilloscope Channel 1 probe to TP25. Connect the test probe ground clip to ground reference TP17.

(6) Position sweep trace 1.5 cm below center line of graticule.

(7) Set oscilloscope Channel 1 sensitivity to 0.10v per division.

(8) Set sync to internal, normal mode.

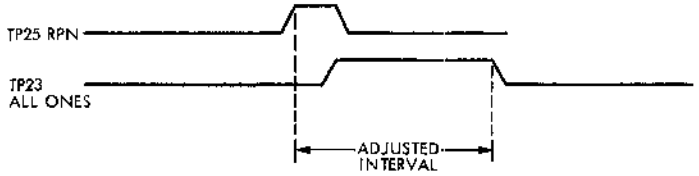


Figure 6-24. Read Pulse Narrow/'Ones' Window

(9) Set oscilloscope to trigger on the positive slope of RPN.

(10) Connect oscilloscope Channel 2 probe to TP23. Connect the test probe ground clip to ground reference TP17.

(11) Position sweep trace 1.5 cm below center line of graticule.

(12) Set oscilloscope Channel 2 sensitivity to 0.10v per division.

6.12.2.2 Test And Adjustment Procedure (Long)

(1) Observe 'ones' window on oscilloscope Channel 2 (TP23) as shown in Figure 6-24.

(2) Measure the adjusted interval, i.e., leading edge of RPN TP25 to trailing edge of 'ones' window TP23.

(3) If the pulse width is not within ±3 nanoseconds of setting listed in Table 6-5, adjust R115 for the specified value.

6.12.2.3 Test And Adjustment Procedure (Short)

(1) Write all 'ones' pattern via the disk exerciser.

(2) Observe 'ones' window on oscilloscope Channel 2 (TP23) as shown in Figure 6-24.

(3) Measure the adjusted interval, i.e., leading edge of RPN TP25 to trailing edge of 'ones' window (TP23).

(4) If the pulse width is not within ±3 nanoseconds of setting listed in Table 6-5, adjust R113 for the specified value.

Table 6-5
RPN Pulsewidth Values

Speed	Zeros	Ones
4500 rpm	500 nsec	480 nsec
2400 rpm	312 nsec	302 nsec

6.12.3 DATA AND CLOCK PULSE WIDTH

6.12.3.1 Test Configuration

(1) Remove the interface connector and terminator PCBA from connector J101 and J102 on the Logic PCBA.

(2) Connect a disk exerciser having read/write capability to J101 or J102 on the Logic PCBA.

(3) Apply power to the exerciser and the disk drive. Observe that the READY indicator is illuminated; allow a 5-minute warm up period.

(4) Write an all-ones pattern via the disk exerciser.

(5) Connect oscilloscope Channel 1 probe to TP25. Connect the test probe ground clip to ground reference TP17.

(6) Position sweep trace 1.5 cm below center line of graticule.

(7) Set oscilloscope Channel 1 sensitivity to 0.10v per division.

(8) Set sync to internal, normal mode.

(9) Set oscilloscope to trigger on the positive slope of RPN.

(10) Connect oscilloscope Channel 2 probe to read data TP15 (or read clock TP16). Connect the test probe ground clip to ground reference TP17.

(11) Position sweep trace 1.3 cm below center line of graticule.

(12) Set oscilloscope Channel 2 sensitivity to 0.10v per division.

6.12.3.2 Test Procedure

(1) Observe Read Data TP15 (or Read Clock TP16) on oscilloscope Channel 2 as shown in Figure 6-25.

(2) Measure and note the adjusted interval.

(3) Acceptable Limits

- 100 nanoseconds (minimum)
- 150 nanoseconds (maximum)

6.12.3.3 Adjustment Procedure

If the acceptable limits detailed in Paragraph 6.12.3.2 Step (3) are exceeded perform the following adjustment.

(1) Establish test configuration detailed in Paragraph 6.12.3.1.

(2) Adjust R153 (Read Data TP15) on R155 (Read Clock TP16) for 125 nanoseconds.

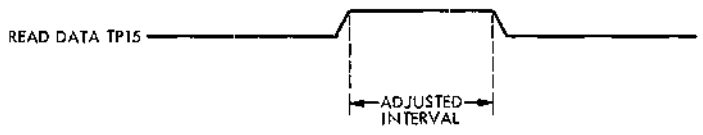


Figure 6-25. Read Clock/Read Data Pulsewidth

6.13 CE ALIGNMENT PROCEDURE

The circumferential and radial alignment of a disk drive is performed using a special CE disk cartridge that can usually be identified by a special top color and/or label. The CE cartridge platter contains two or three pre-recorded cylinders (dependening on the manufacturer) which are used to adjust the Read/Write head radial alignment and the index to data circumferential alignment.

CE alignment procedures for a front load disk drive differ from that used with a top load model. Primarily, the differences are due to the differences between the top load and front load CE disk cartridge configurations. The alignment tracks used are at different locations even though the read data patterns for radial alignment are similar. There is also a difference between the location of the circumferential alignment adjustment and the tool required to perform this alignment. Therefore, separate CE alignment procedures are given for front load disk drives and top load disk drives. The 200 tpi radial alignment procedure is given separately in order to stress key elements.

Paragraphs 6.13.1 and 6.13.2 provide descriptions of front and top loading CE disk cartridges; Paragraph 6.13.3 describes the environmental stabilization requirements for the CE cartridges.

The test configuration for both top and front loading machines is given in Paragraph 6.13.4.

Paragraphs 6.13.5 and 6.13.6 detail the radial and circumferential alignment procedures, respectively, for front loading models. Paragraphs 6.13.7 and 6.13.8 detail the radial and circumferential alignment procedures, respectively, for top loading models.

6.13.1 FRONT LOADING CE DISK CARTRIDGE

The 100 tpi front loading CE disk cartridge contains three pre-recorded cylinders (95, 100, and 105) which are used during adjustment procedures to the head/arm carriage assembly and to the (upper) photoelectric sensor. The 200 tpi CE disk cartridge is identical to the 100 tpi cartridge except that the two pre-recorded cylinders are in different locations.

CAUTION

CARE SHOULD BE TAKEN TO ENSURE THAT CYLINDERS 094 THROUGH 110 ON 100 TPI, OR CYLINDERS 190 THROUGH 200 ON 200 TPI, ARE NOT INADVERTENTLY WRITTEN ON; WRITING ON THESE CYLINDERS WILL CAUSE THE PRE-RECORDED DATA TO BE DESTROYED.

6.13.1.1 Radial Alignment Cylinder

The radial alignment cylinder is used for adjustment of the head arm location. The cylinder consists of an eccentric cylinder with an average radius of the cylinder. Radial adjustment of the head is carried out by monitoring the read signal envelope at this cylinder. Due to the amount of eccentricity, when a head is reading the pattern and the head is mis-aligned from the true cylinder radius, then a lobed envelope pattern will be produced. As the head is aligned to the true cylinder radius, a particular pattern will be produced.

6.13.1.2 Circumferential Alignment Cylinder (Index to Data)

This cylinder has a single flux transition marker recorded approximately 180 degrees from the center line of the index slot. To assist in identifying this marker, a burst of flux transitions occurs 10 μsec after the marker.

This cylinder is used for circumferential adjustment of the (upper) photoelectric sensor.

NOTE

On some 100 tpi front loading CE cartridges, there is another cylinder written five tracks toward the spindle. It is written eccentric to the disk rotational center. Because of its identical appearance to the true radial alignment cylinder it is possible to become confused and misalign the heads on the incorrect cylinder. Care should be used when performing a radial adjustment with front loading cartridges to avoid this mis-alignment caused by incorrectly using the wrong pattern.

6.13.2 TOP LOADING CE DISK CARTRIDGE

The 100 tpi top loading CE disk cartridge contains two pre-recorded cylinders 005 and 073 which are used during adjustment procedures to the head arm carriage assembly and to the upper magnetic transducer.

The 200 tpi CE disk cartridge is identical to the 100 tpi cartridge except that the two pre-recorded cylinders are 010 and 146.

CAUTION

WHEN USING 100 TPI CE PACKS, ENSURE THAT CYLINDERS 004, 005, 006, AND 071 THROUGH 075 ARE NOT INADVERTENTLY WRITTEN ON. WHEN USING 200 TPI CE PACKS, ENSURE THAT CYLINDERS 008 THROUGH 012 AND 142 THROUGH 150 ARE NOT INADVERTENTLY WRITTEN ON. WRITING ON THESE CYLINDERS WILL CAUSE PRE-RECORDED DATA TO BE DESTROYED.

6.13.2.1 Cylinder 073 (100 tpi), Cylinder 146 (200 tpi)

For 100 tpi CE packs, cylinder 073 is used for adjustment of the head arm location; for 200 tpi, cylinder 146 is used for this adjustment. Two circular concentric cylinders, either side of cylinder 073 and cylinder 146, are spaced 0.010-inch apart and are eccentric to the center of rotation of the disk by 0.0015-inch. The cylinders are written with slightly different frequencies. Radial adjustment of the head is carried out by monitoring the beat frequency at cylinder 073 (100 tpi), 146 (200 tpi). A head that is correctly centered over track 073 (100 tpi), 146 (200 tpi), gives an oscilloscope trace with an equal 2-lobe fringe pattern. Due to the amount of eccentricity, when a head is reading the pattern and the head is misaligned from the true cylinder radius, then a lobed envelope pattern will be produced.

6.13.2.2 Cylinder 005 (100 tpi), Cylinder 010 (200 tpi)

For 100 tpi CE packs, cylinder 005 is used for circumferential adjustment of the upper magnetic transducer; for 200 tpi, cylinder 010 is used for this adjustment. The cylinder has a single flux transition marker recorded approximately 180 degrees from the center line of the index notch. To assist in identifying this marker, a burst of flux transitions occurs 10 μsec after the marker.

6.13.3 CE CARTRIDGE STABILIZATION

Prior to attempting alignment, the CE cartridge must be conditioned in the same environment in which the disk drive (to be aligned) is located. This conditioning must not be less than 2 hours. In addition to this stabilization period, the CE cartridge must be operated for at least 15 minutes in the disk drive with the disk drive in the Run condition. This allows the cartridge to reach the proper temperature just prior to performing the alignment.

6.13.4 TEST CONFIGURATION — ALL MODELS

The following procedure is used to establish the test configuration for CE alignment of both top and front loading disk drives.

(1) Remove the cover from the disk drive and open the circuit boards to their fully extended positions.

(2) If installed, remove the I/O cable and the terminator PCBA from interface connectors J101 and J102 on the Logic PCBA.

(3) Connect a disk exerciser without read/write capabilities to one of the interface connectors, J101 or J102.

(4) Set the upper platter Write Protect switch to the ON position.

(5) Connect the disk drive to the ac power source and set the ON/OFF switch to the ON position.

(6) When the SAFE indicator becomes illuminated, insert the special CE disk cartridge into the machine.

(7) Depress the RUN/STOP switch once and allow the disk drive to come READY. Allow the disk drive to warm up for at least 15 minutes before proceeding.

(8) Disconnect the emergency unload capacitor connector P206 from the Servo PCBA, thereby de-activating the emergency unload system. If the disk speed slows noticeably due to the loss of ac power or other malfunction, the heads must be manually unloaded by the operator.

NOTE

It is the responsibility of the person performing the CE alignment to perform the emergency unload function when P206 is disconnected.

(9) A dual trace oscilloscope having a 50 MHz vertical bandwidth or greater is required to perform CE alignment procedures.

NOTE

Depending on the type of oscilloscope utilized and its grounding arrangement, it may be necessary to use a differential measurement of the Read/Write PCBA signal in lieu of a single channel method. This will usuallly be the case when a ground loop exists between the scope and the disk drive. Refer to the applicable oscilloscope manual for differential measurement set-up, if necessary.

(10) One X1 probe is required for single-ended measurement method; two X1 probes are required for differential measurement method.

(11) Front load disk drive CE alignment procedures are outlined in Paragraphs 6.13.5 and 6.13.6; top load disk drive CE alignment procedures are outlined in Paragraphs 6.13.7 and 6.13.8.

6.13.5 RADIAL ALIGNMENT — FRONT LOAD

6.13.5.1 Test Procedure (100 tpi)

The test configuration detailed in Paragraph 6.13.4 must be performed prior to performing the following procedure.

(1) Set up oscilloscope as follows.
- Connect oscilloscope vertical input to TP19 on the Read/Write PCBA; use TP18 for ground reference.
- Set vertical sensitivity to 0.1v per division and select the ac input mode.
- Connect a X10 test probe from the external trigger input of the oscilloscope to TP3 (Index) on the Logic PCBA.
- Use external trigger and normal sync, ac coupled, on the negative trigger slope.
- Set sweep rate to 5 msec per division.

(2) Set exerciser to position the heads to cylinder 100.

(3) Select head 0 (upper surface of upper platter).

(4) Observe the waveform at TP19 and compare the waveform to the relevant waveform shown in Figure 6-26.

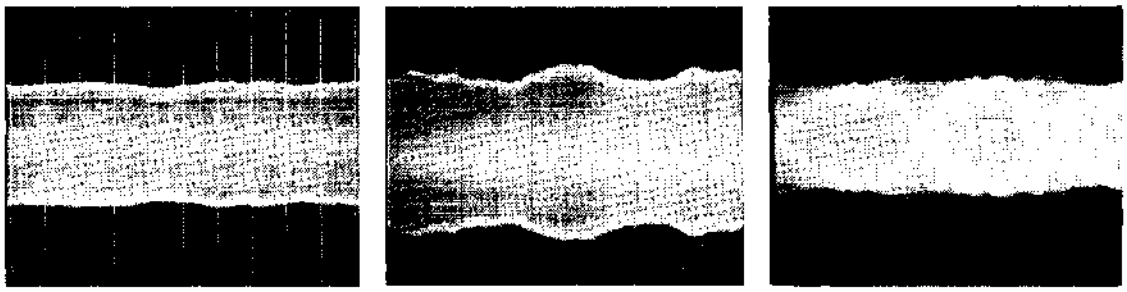
(5) Select head 1 and repeat Step (4).

NOTE

If no waveform or the improper waveform is observed, go directly to the adjustment procedure, Paragraph 6.13.5.3.

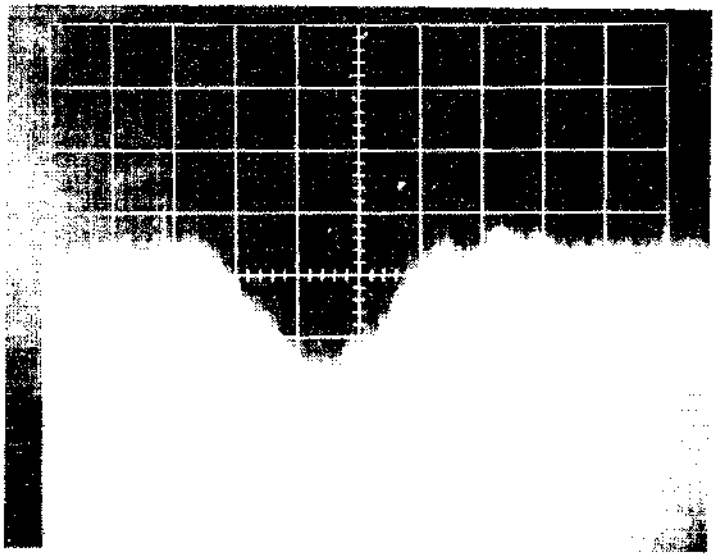
(6) Change vertical sensitivity to 20 mv per division and change vertical positioning to observe the edge of the waveform envelope.

(7) For each head selected, observe the edge of the waveform and compare it to the relevant waveform shown in Figures 6-27A, 6-27B, or 6-27C.

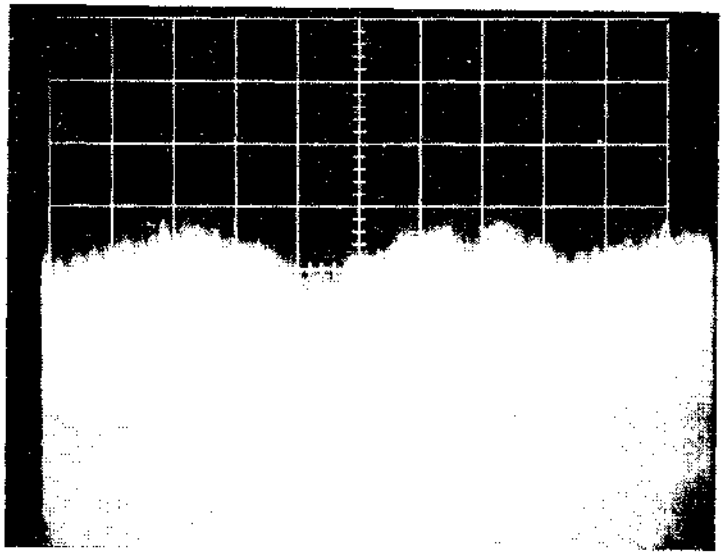


IBM C.E. Cartridge 3M C.E. Cartridge CDC C.E. Cartridge

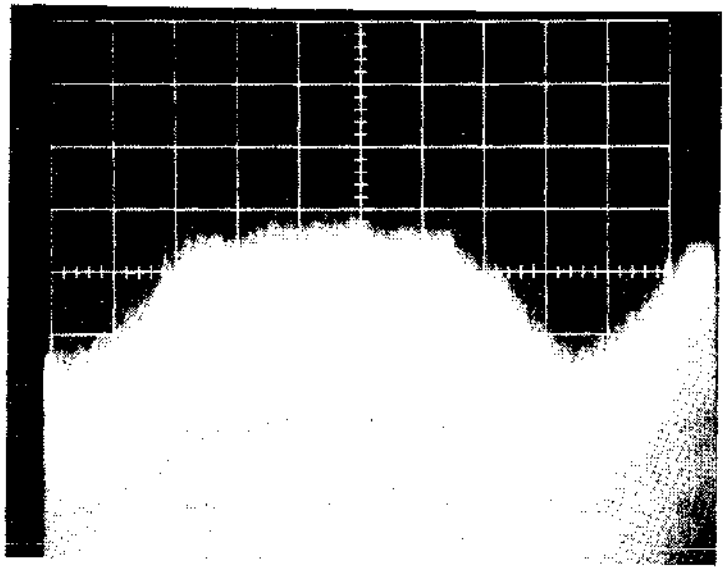
Figure 6-26. Approximately Aligned Front Load Disk Drive



Heads Too Far Back, Trk 100, Front Load

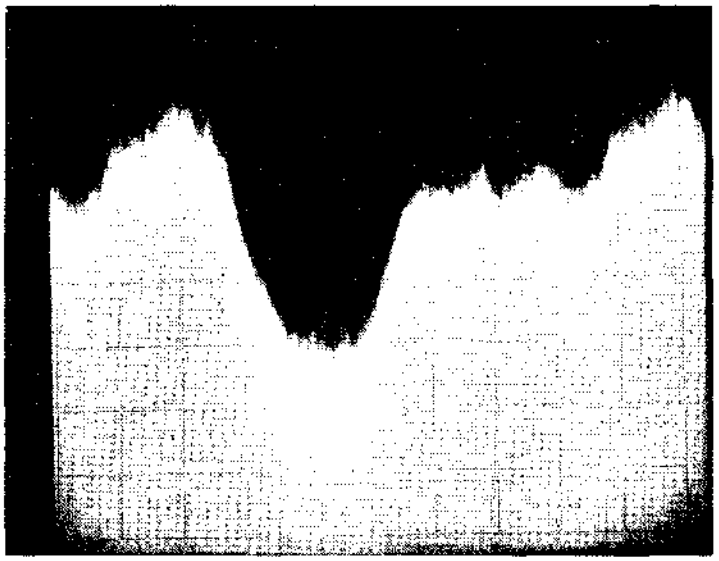


Correct Alignment, Trk 100, Front Load

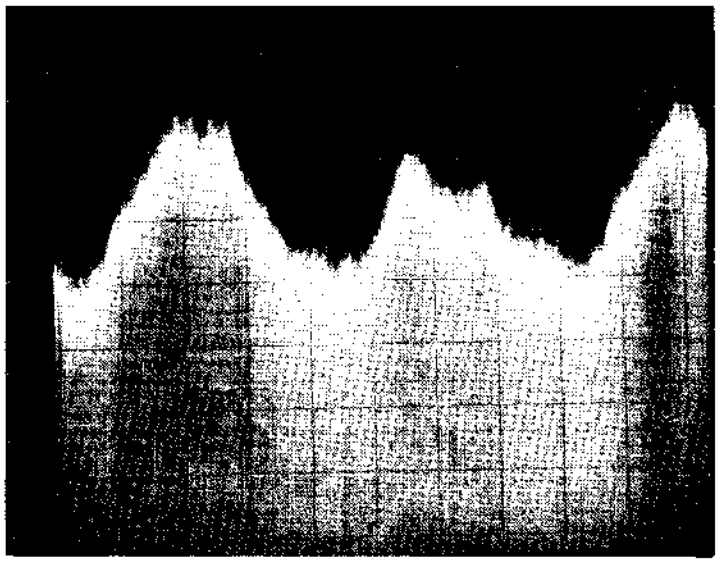


Heads Too Far Forward, Trk 100, Front Load

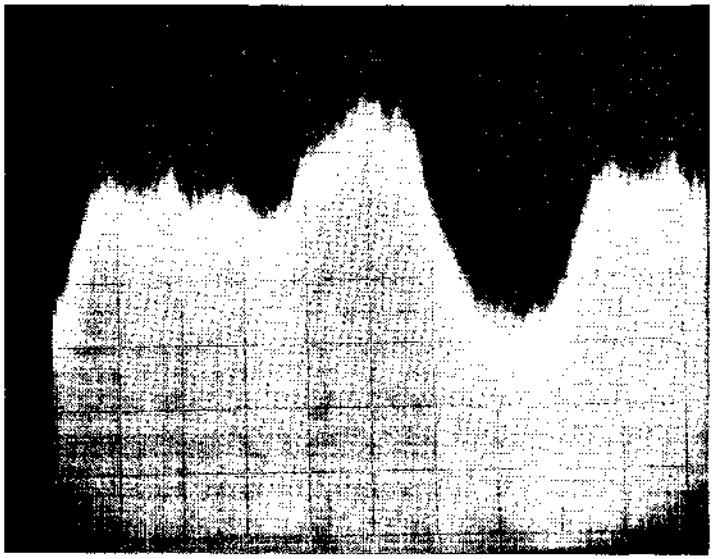
Figure 6-27A. Head Alignment, IBM C.E. Cartridge



Heads Too Far Back, Trk 100, Front Load



Correct Alignment, Track 100, Front Load



Heads Too Far Forward, Trk 100, Front Load

Figure 6-27B. Head Alignment, 3M C. E. Cartridge

Heads Too Far Back, Track 100, Front Load

Heads Too Far Forward, Track 100, Front Load

Correct Alignment, Track 100, Front Load

Figure 6-27C. Head Alignment, CDC Cartridge

6.13.5.2 Test Procedure (200 tpi)

(1) Set up oscilloscope as follows.

- Connect oscilloscope vertical input to TP19 on the Read/Write PCBA. Use TP18 for ground reference.
- Set vertical sensitivity to 50 mv per division and select the ac input mode.
- Connect a X10 test probe from the external trigger input of the oscilloscope to TP3 (index) on the Logic PCBA.
- Use external trigger, and normal sync, ac-coupled on the negative trigger slope.
- Set sweep rate to 5 msec per division.

(2) Set exerciser to position heads to cylinder 200.

(3) Select head 0.

(4) Observe the waveform at TP19 and compare it to the waveform shown in Figure 6-28.

(5) Select head 1 and repeat Step (4).

NOTE

If no waveform or the improper waveform is observed, go directly to the adjustment procedure, Paragraph 6.13.5.4.

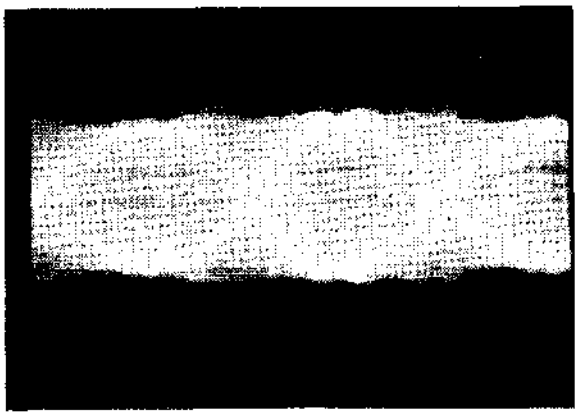


Figure 6-28. Radial Alignment, Head Aligned

6.13.5.3 Adjustment Procedure (100 tpi)

If radial alignment is required, perform the following adjustment procedure.

NOTE

For alignment of Diablo low density [1024, 1100 bpi] machines, perform Steps [1] through [6] only; for alignment of Diablo high density [2200 bpi] machines, perform Steps [1] through [8], inclusive.

(1) Maintain the oscilloscope settings established in Paragraph 6.13.5.1.

(2) Observe the waveforms shown in Figure 6-27A, B, and C, and determine which direction the heads must be moved.

NOTE

If no waveform is observed at TP19, and no malfunction of the disk drive is suspected, a gross adjustment of the heads is required. To determine which direction the heads must be moved, use the exerciser to re-position the heads to cylinder address 90 and change Channel 1 sensitivity to 0.1v per division. Increment the cylinder address, one cylinder at a time, until the correct waveform at TP19 is observed. Make note of this address. Refer to Figure 6-26.

(3) Locate the two radial positioning screws on the selected head.

(4) By loosening one screw and tightening the other, position the selected head until the correct alignment waveform, shown in Figure 6-27A, B, or C, is obtained; then tighten both screws without disturbing the adjustment.

(5) Align both heads in the same manner.

(6) Using the exerciser, position the heads to cylinder 000, then re-position them to cylinder 105 and observe that the correct alignment waveform appears as in Figure 6-27A, B, or C. This ensures that the heads have not been aligned to cylinder 105 which is a duplicate of cylinder 100.

NOTE

If a head cannot be adjusted to obtain the minimal lobe pattern, the head may not be flying correctly. This condition can be caused by either a dirty disk or head, incorrect head load force, or damaged head[s].

(7) Leaving the heads positioned at cylinder address 105, repeat Steps (4) and (5) but reposition both heads back toward cylinder radius 100 until the waveforms observed at TP19 appear as in correct alignment waveform shown in Figures 6-27A, B, or C.

(8) Using the exerciser, position the heads with a cylinder address of 110 and observe that the waveform still appears as correct alignment waveform as shown in Figures 6-27A, B, or C. This ensures that the heads have been aligned correctly and that the new cylinder address 000 has a radius of 6.550 inches (this is larger than standard; PERTEC standard is 6.500 inches).

6.13.5.4 Adjustment Procedure (200 tpi)

CAUTION

THE POLARITY OF THE COMPENSATION VALUE FOR EACH CE CARTRIDGE IS CRITICAL. IF CARTRIDGE INTERCHANGE IS NOT A PREREQUISITE, PERFORM THE ADJUSTMENT PROCEDURE FOR FRONT LOAD 100 TPI MODELS DESCRIBED IN PARAGRAPH 6.13.5.3 EXCEPT USE FIGURE 6-28.

(1) Position Switch S-1 on the Temperature Compensation PCBA (Assembly 103450) to the OFF position.

(2) Maintain oscilloscope setting established in Paragraph 6.13.5.2 except change Channel 1 sensitivity to 50 — 100 mv per division.

(3) Observe the waveforms shown in Figure 6-29 and determine which direction the heads must be moved.

(4) Note the value of the compensation factor which is printed on the CE cartridge.

- If the compensation factor is zero, perform the radial head alignment described in Paragraph 6.13.5.2, then perform Steps (5) through (11) of this procedure.
- A positive (+70) compensation factor indicates that the CE track was written offset away from the spindle. The CE alignment is correct when the head is displaced 70 μinches toward the spindle. See Figure 6-29B.

  The compensation factor (+70) is stated in μinches and represents a Δ lobe height of one-half of one major oscilloscope graticule division when the maximum lobe pattern is adjusted to fill eight major divisions.
- A negative (—70) compensation factor indicates that the CE track was written offset toward the spindle. The CE alignment is correct when the head is displaced 70 μinches away from the spindle. See Figure 6-27B.

  The compensation factor (—70) is stated in μinches and represents a Δ lobe height of one-half of one major division when the maximum lobe pattern is adjusted to fill eight major divisions.

(5) Position Switch S-1 on the Temperature Compensation PCBA to the ON position.

(6) Connect a jumper between TP19 on the Read/Write PCBA and TP13 on the Temperature Compensation PCBA.

(7) Connect a jumper between TP18 on the Read/Write PCBA and TP14 on the Temperature Compensation PCBA.

(8) Replace the dust cover on the unit; secure in place with enough screws to ensure clearance when the unit is positioned in the rack.

(9) Slide the unit into its normal operating position, i.e., into the rack. Allow the unit to stabilize in the Ready mode for 30 minutes (minimum).

(10) Repeat Step (4) with the oscilloscope vertical input connected to TP2 on the System Compensation PCBA (Assembly 103445). Use TP1 on the System Compensation PCBA for the oscilloscope ground reference.

NOTE

TP1 and TP2 on the System Compensation PCBA are connected via internal cabling to TP14 and TP13 on the Temperature Compensation PCBA.

Head adjustment is accomplished using R1 and R2 on the System Compensation PCBA. R1 is the potentiometer which provides fine electrical adjustment for the lower head of the removable platter; R2 provides this adjustment for the upper head of this platter.

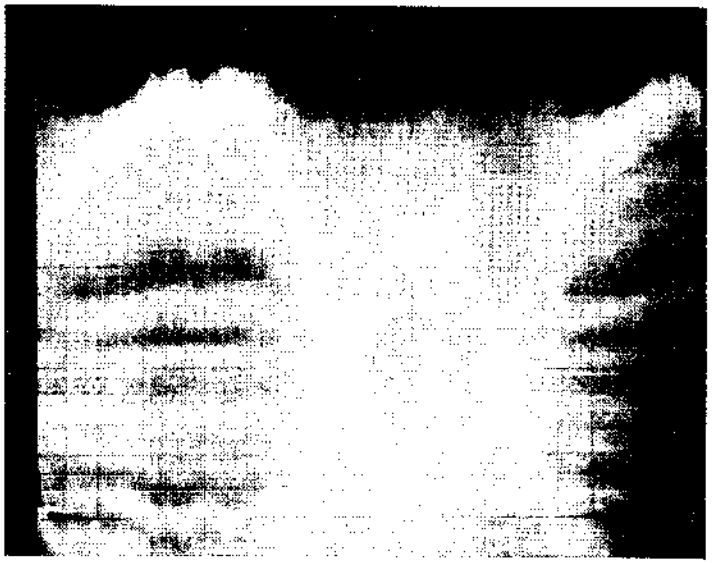


Figure 6-29A. Radial Alignment, Heads Too Far Back

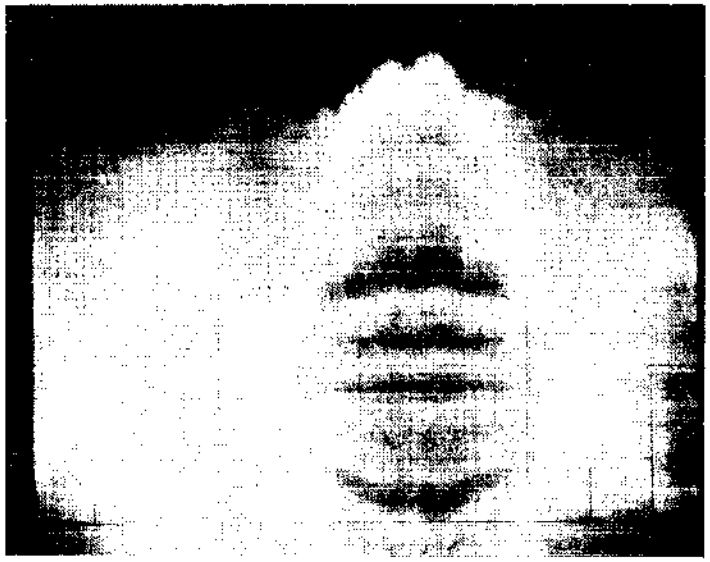


Figure 6-29B. Radial Alignment, Head Too Far Forward

Figure 6-29C. Radial Alignment, Heads Aligned

(11) When the CE alignment is complete, remove power from the equipment using the procedure contained in Section II.

(12) Extend the disk drive from the rack enclosure and remove the cover. Remove the jumper connections between TP19, TP18, on the Read/Write PCBA and TP13, TP14 on the Temperature Compensation PCBA.

(13) Secure all PCBAs into their normal operating configuration and replace the dust cover.

6.13.6 CIRCUMFERENTIAL ALIGNMENT — FRONT LOAD

Values are given for all versions of the D3000 with values for 200 tpi models parenthetically stated.

6.13.6.1 Test Procedure

(1) Set oscilloscope per Paragraph .6.13.5.1 with the following exceptions if a differential measurement method is not utilized.

- Disconnect test probe from external trigger input and connect it to Channel 2 input. (Compensation of the probe may be necessary.)
- Set Channel 2 sensitivity to 0.2v per division.
- Set Channel 1 sensitivity to 0.1v per division.
- Set sweep rate to 10 μsec per division.
- Set Channel Select to the Alternate mode.
- Use internal sync and sync negative on leading edge of Index signal on Channel 2.

NOTE

If a differential measurement method is used, set oscilloscope per Paragraph 6.13.5.1 with the exceptions listed in the steps below.

- Set sweep rate to 10 μsec per division.
- Adjust horizontal position to place start of sweep on left-most vertical graticule line. This will establish a time-zero reference to be used in lieu of actual viewing of the negative transition of the index pulse.

  Take care not to disturb the horizontal position during the measurement. (This technique presumes that the start of the sweep corresponds to the triggering of the sweep. Verify this if in doubt.)

(2) Set exerciser to position heads to cylinder 95 (190 for 200 tpi).

(3) Select head 0.

(4) Observe the waveform at TP19 with respect to the falling edge of the Index signal (time-zero reference).

(5) The first pulse of the waveform (TP19) should occur 75 ±5 μsec from the negative going edge of the Index signal (time-Zero reference). See Figure 6-30.

(6) Select head 1.

(7) Observe the waveform at TP19. The first pulse should occur 75 +5 sec from the negative going edge of the Index signal (time-zero reference).

(8) Alternately switch between heads 0 and 1, and observe the relative displacement of the pulse for each head. The total displacement (separation) between pulse positions must be +10 sec. See Figure 6-31.

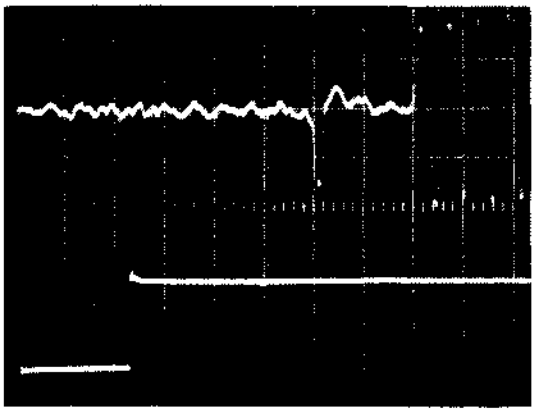


Figure 6-30. Circumferential Alignment, Front Load Disk Drives

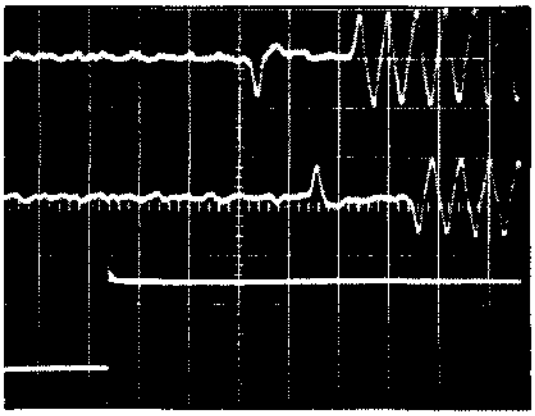


Figure 6-31. Compromise Circumferential Alignment, Front Load

6.13.6.2 Adjustment Procedure

If circumferential alignment is required, perform the following procedure.

NOTE

If the separation between pulses, as measured in Step [8] of Paragraph 6.13.6.1, exceeds 10 μsec, remove power from the disk drive and remove the upper two heads. Check for foreign material or burrs on the head seating surfaces. Replace one or both heads if a head problem is suspected. Reinstall heads and perform the radial alignment procedure.

(1) Maintain setup per Paragraph 6.13.6.1, Steps (1) and (2).

(2) Insert the special 7-1/2-inch (Allen wrench) circumferential adjustment tool (PERTEC Part No. 103609) into the circumferential alignment adjusting screw located under the cartridge receiver toward the right front of the machine (viewed facing the front of the drive).

NOTE

It may be necessary to lift the receiver slightly until the tool can be inserted.

CAUTION

CARE MUST BE TAKEN WHEN LIFTING THE RECEIVER. LIFTING THE RECEIVER TOO HIGH WILL CAUSE THE SPINNING DISK TO COME INTO CONTACT WITH THE CARTRIDGE HOUSING.

NOTE

Rotation of the tool in the CCW direction increases the pulse delay from Index.

(3) Select either head (0 or 1) and, while observing the waveform at TP19, turn the adjusting screw until the first pulse after the falling edge of Index (Channel 2) falls within the 75 ±5 μsec specification.

(4) Select the other head and ensure that the specification detailed in Step (3) is met. A compromise adjustment may be required to meet the 75 ±5 μsec requirement for both heads. See Figure 6-31.

(5) Turn the alignment tool slightly in the opposite direction of the last turn to cause the adjusting screw to relax the force on the mechanism (i.e., mid-range of the screw backlash).

(6) Recheck head 0 and 1 to verify that the measurement is still within tolerance. Repeat Steps (3), (4), and (5) as necessary.

(7) Remove the alignment tool and bring the disk drive to the SAFE condition, then remove the CE disk cartridge. Return the disk drive to its former configuration. Do not forget to reset the write protect switch if the protect is not desired, and re-connect P206 on the Servo PCBA.

6.13.7 RADIAL ALIGNMENT — TOP LOAD

Paragraphs 6.13.7.1 and 6.13.7.2 describe the test procedure and adjustment procedure for radial alignment of 100 tpi disk drives; Paragraphs 6.13.7.3 and 6.13.7.4 describe the test procedure and adjustment procedure for radial alignment of 200 tpi disk drives.

6.13.7.1 Test Procedure (100 tpi)

(1) Set up oscilloscope as follows.

- Connect oscilloscope vertical input to TP19 on the Read/Write PCBA. Use TP18 for ground reference.
- Set vertical sensitivity to 50 mv per division and select the ac input mode.
- Connect a X10 test probe from the external trigger input of the oscilloscope to TP3 (Index) on the Logic PCBA.
- Use external trigger, and normal sync, ac-coupled on the negative trigger slope.
- Set sweep rate to 5 msec per division.

(2) Set exerciser to position heads to cylinder 73.

(3) Select head 0.

(4) Observe the waveform at TP19 and compare it to the waveform shown in Figure 6-32.

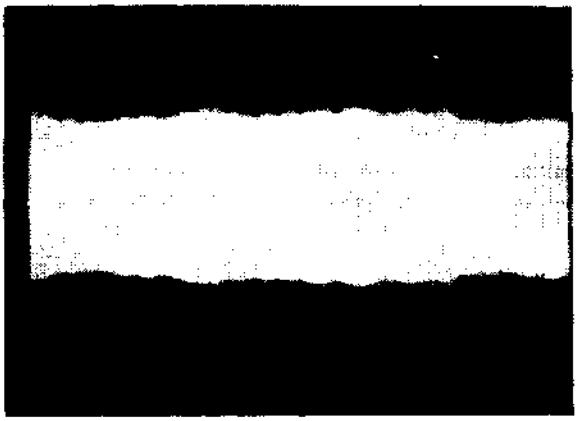


Figure 6-32. Radial Alignment, Head Aligned

(5) Select head 1 and repeat Step (4).

NOTE

If no waveform or the improper waveform is observed, go directly to the adjustment procedure, Paragraph 6.13.7.2.

6.13.7.2 Adjustment Procedure (100 tpi)

If radial alignment is required, perform the following procedure.

(1) Maintain oscilloscope setting established in Paragraph 6.13.7.1 except change Channel 1 sensitivity to 20 mv per division.

(2) Observe the waveforms shown in Figure 6-33 and determine which direction the heads must be moved.

(3) Perform adjustment procedure according to Paragraph 6.13.5.2 starting with the Note in Step (2), using cylinder address 63 for search operation, through Step (5). Refer to waveforms in Figure 6-33 during these adjustments.

NOTE

The radial adjustments for a top load machine are very sensitive. There is only one correct head alignment position. If available, use a hood over the scope screen and adjust the oscilloscope intensity control for maximum clarity of the beat-frequency lobed pattern [Figure 6-32]. The head adjustments may interact slightly. Adjust for the best compromise of equal lobed patterns.

6.13.7.3 Test Procedure (200 tpi)

(1) Set up oscilloscope as follows.

- Connect oscilloscope vertical input to TP19 on the Read/Write PCBA. Use TP18 for ground reference.
- Set vertical sensitivity to 50 mv per division and select the ac input mode.
- Connect a X10 test probe from the external trigger input of the oscilloscope to TP3 (Index) on the Logic PCBA.
- Use external trigger, and normal sync, ac-coupled on the negative trigger slope.
- Set sweep rate to 5 msec per division.

Figure 6-33A. Radial Alignment, Head Too Far Back

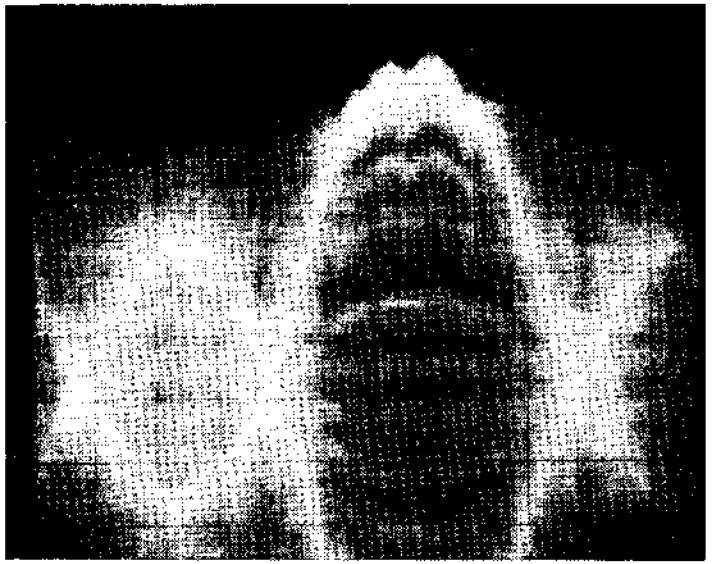


Figure 6-33B. Radial Alignment, Head Too Far Forward

Figure 6-33C. Radial Alignment, Heads Aligned

(2) Set exerciser to position heads to cylinder 146.

(3) Select head 0.

(4) Observe the waveform at TP19 and compare it to the waveform shown in Figure 6-32.

(5) Select head 1 and repeat Step (4).

NOTE

If no waveform or the improper waveform is observed, go directly to the adjustment procedure, Paragraph 6.13.7.4.

6.13.7.4 Adjustment Procedure (200 tpi)

CAUTION

THE POLARITY OF THE COMPENSATION VALUE FOR EACH CE CARTRIDGE IS CRITICAL. IF CARTRIDGE INTERCHANGE IS NOT A PREREQUISITE, PERFORM THE ADJUSTMENT PROCEDURE FOR TOP LOAD 100 TPI MODELS DESCRIBED IN PARAGRAPH 6.13.7.2.

(1) Position Switch S-1 on the Temperature Compensation PCBA (Assembly No. 103450) to the OFF position.

(2) Maintain oscilloscope setting established in Paragraph 6.13.7.2 except change Channel 1 sensitivity to 50 — 100 mv per division.

(3) Observe the waveforms shown in Figure 6-33 and determine which direction the heads must be moved.

(4) Note the value of the compensation factor which is printed on the CE cartridge.

- If the compensation factor is zero, perform the radial head alignment described in Paragraph 6.13.7.2, then perform Steps (5) through (11) of this procedure.
- A positive (+100) compensation factor indicates that the CE track was written offset away from the spindle. The CE alignment is correct when the head is displaced 100 μinches toward the spindle. See Figure 6-33B.

  The compensation factor (+100) is stated in μinches and represents a Δ lobe height of one-half of one major oscilloscope graticule division when the maximum lobe pattern is adjusted to fill eight major divisions.
- A negative (—100) compensation factor indicates that the CE track was written offset toward the spindle. The CE alignment is correct when the head is displaced 100 μinches away from the spindle. See Figure 6-33A.

  The compensation factor (—100) is stated in μinches and represents a Δ lobe height of one-half of one major division when the maximum lobe pattern is adjusted to fill eight major divisions.

(5) Position Switch S-1 on the Temperature Compensation PCBA to the ON position.

(6) Connect a jumper between TP19 on the Read/Write PCBA and TP13 on the Temperature Compensation PCBA.

(7) Connect a jumper between TP18 on the Read/Write PCBA and TP14 on the Temperature Compensation PCBA.

(8) Replace the dust cover on the unit; secure in place with enough screws to ensure clearance when the unit is positioned in the rack.

(9) Slide the unit into its normal operating position, i.e., into the rack. Allow the unit to stabilize in the Ready mode for 30 minutes (minimum).

(10) Repeat Step (4) with the oscilloscope vertical input connected to TP2 on the System Compensation PCBA (Assembly No. 103445). Use TP1 on the System Compensation PCBA for the oscilloscope ground reference.

NOTE

TP1 and TP2 on the System Compensation PCBA are connected via internal cabling to TP14 and TP13 on the Temperature Compensation PCBA.

Head adjustment is accomplished using R1 and R2 on the System Compensation PCBA. R1 is the potentiometer which provides fine electrical adjustment for the lower head of the removable platter; R2 provides this adjustment for the upper head of this platter.

(11) When the CE alignment is complete, remove power from the equipment using the procedure contained in Section II.

(12) Extend the disk drive from the rack enclosure and remove the cover. Remove the jumper connections between TP19, TP18 on the Read/Write PCBA and TP13, TP14 on the Temperature Compensation PCBA.

(13) Secure all PCBAs into their normal operating configuration and replace the dust cover.

6.3.8 CIRCUMFERENTIAL ALIGNMENT — TOP LOAD

Values are given for all versions of the D3000 with values for 200 tpi models parenthetically stated.

6.13.8.1 Test Procedure

(1) Set oscilloscope per Paragraph 6.13.5.1 with the following exceptions if a differential measurement method is not utilized.

- Disconnect test probe from external trigger input and connect it to Channel 2 input. (Compensation of the probe may be necessary.)
- Set Channel 2 sensitivity to 0.2v per division.
- Set Channel 1 sensitivity to 0.1v per division.
- Set sweep rate to 5 μsec per division.
- Set Channel Select to the Alternate mode.
- Use internal sync and sync negative on leading edge of Index signal on Channel 2.

NOTE

If a differential measurement method is used, set oscilloscope per Paragraph 6.13.5.1 with the following exceptions.

- Set sweep rate to 5 μsec per division.
- Adjust horizontal position to place start of sweep on left-most vertical graticule line. This will establish a time-zero reference to be used in lieu of actual viewing of the negative transition of the index pulse.

  Take care not to disturb the horizontal position during the measurement. (This technique presumes that the start of the sweep corresponds to the triggering of the sweep. Verify this if in doubt.)

(2) Set exerciser to position heads to cylinder 005 (010 for 200 tpi).

(3) Select head 0.

(4) Observe the waveform at TP19 with respect to the falling edge of the Index signal (time-zero reference).

(5) The first pulse of the waveform (TP19) should occur 30 +5 sec from the negative going edge of the Index signal (time-zero reference). See Figure 6-30.

(6) Select head 1.

(7) Observe the waveform at TP19. The first pulse should occur 30 ±5 μsec from the negative going edge of the Index signal (time-zero reference).

(8) Alternately switch between heads 0 and 1, and observe the relative displacement of the pulse for each head. The total displacement (separation) between pulse positions must be ±10 μsec. See Figure 6-31.

6.13.8.2 Adjustment Procedure

If circumferential alignment is required, perform the following procedure.

NOTE

If the separation between pulses, as measured in Step [8] of Paragraph 6.13.8.1, exceeds 10 μsec, remove power from the disk drive and remove the upper two heads. Check for foreign material or burrs on the head seating surfaces. Replace one or both heads if a head problem is suspected. Reinstall heads and perform the radial alignment procedure.

(1) Maintain test conditions established in Paragraph 6.13.8.1, Steps (1) and (2).

(2) Remove the bezel from the front of the disk drive.

(3) Loosen the locking screw that is located midway between the two large nuts on the front of the cartridge adapter bowl. Do not loosen the nuts.

(4) Insert an Allen wrench into the circumferential alignment adjusting screw located at the front of the cartridge adapter bowl.

(5) Select either head (0 or 1) and, while observing the waveform at TP19, turn the adjusting screw until the first pulse after the falling edge of Index (Channel 2) falls within the 30 ±5 μsec specification.

(6) Select the other head and ensure that the specification detailed in Step (5) is met. A compromise adjustment may be required to meet the 30 ±5 μsec requirement for both heads. See Figure 6-31.

(7) Turn the alignment tool slightly in the opposite direction of the last turn to cause the adjusting screw to relax the force on the mechanism (i.e., mid-range of the screw backlash).

(8) Recheck head 0 and 1 to verify that the measurement is still within tolerance. Repeat Steps (5), (6), and (7), as necessary.

(9) Tighten the locking screw that was loosened in Step (3) above.

(10) Recheck head 0 and 1 to verify that the measurement is still within tolerance. Repeat Steps (3) through (9) above, as necessary.

(11) Remove the Allen wrench and re-install the bezel.

6.14 MECHANICAL ADJUSTMENTS

6.15 CARTRIDGE INTERLOCK SYSTEM — FRONT LOAD MODELS

The front load disk drive is protected against physical damage by an electromechanical interlock system. This system, described in Paragraph 3.10, prevents the operator from removing a disk cartridge unless the disk drive is in the Safe condition, the spindle has stopped rotating, and the heads have been fully retracted. Two solenoids limit the opening of the front door until these conditions have been satisfied.

The interlock system also inhibits the start sequence if a disk cartridge has not been properly inserted by the operator. This condition is sensed by the interlock switch. The interlock is actuated by appropriate logic and driver circuits located on the Servo and Logic PCBAs.

CAUTION

BEFORE ATTEMPTING TO START A FRONT LOAD DISK DRIVE THE DOOR MUST BE FULLY CLOSED.

6.15.1 CHECKING THE INTERLOCK SYSTEM — FRONT LOAD MODELS

Proper adjustment of the interlock system may be verified as follows.

(1) Prepare the disk drive to receive a disk cartridge as detailed in Paragraph 3.3.

(2) Install an approved disk cartridge as detailed in Paragraph 3.4.1. Depress the RUN/STOP switch.

(3) When the READY indicator is illuminated, pull on the door handle with a pulling force of approximately 10 pounds.

(4) If the unit continues to function normally, as evidenced by continuous illumination of the READY indicator, the interlock system adjustments are within tolerance. If the Ready condition is not maintained, perform the relevant adjustment procedures detailed in Paragraph 6.15.3.

6.15.2 ADJUSTING INTERLOCK SYSTEM

6.15.2.1 Test Configuration

(1) Withdraw the disk drive forward to the full extent of the slides.

(2) Remove the dust cover. (Refer to Paragraph 2.2, Step (5).

(3) Apply power to the disk drive and allow the disk drive to come SAFE.

(4) Determine if a cartridge is installed in the disk drive by following the unloading instructions contained in Paragraph 3.4.2, Steps (1) through (4).

(5) Remove the cartridge from the disk drive if one is installed.

(6) Remove power from the disk drive.

6.15.2.2 Solenoid Plunger Clearance Test and Adjustment

When a solenoid plunger is manually depressed, the clearance between the right and left door link arms and the end of each solenoid plunger should measure between 0.040 to 0.060 inches. See Figure 6-34.

Solenoid adjustments are made as follows.

(1) Right-hand solenoid. Back off the two solenoid mounting screws and slide the solenoid toward or away from the link arm to decrease or increase the gap as required. Securely tighten solenoid adjusting screws.

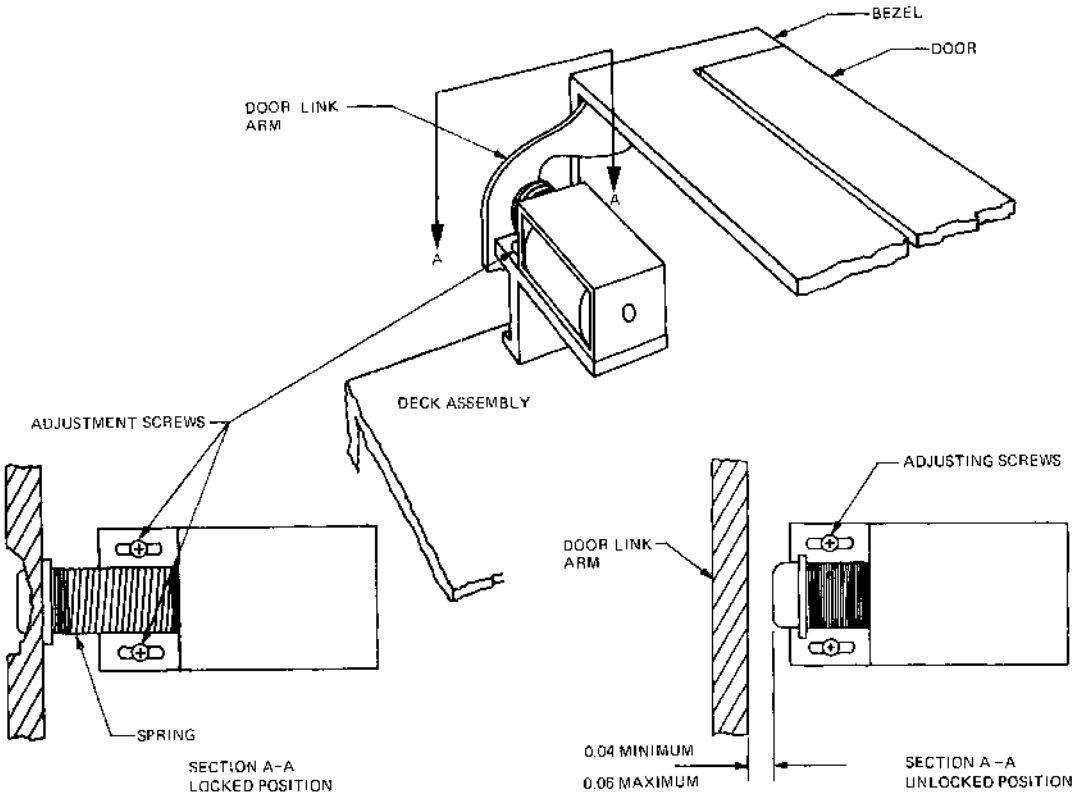


Figure 6-34. Solenoid Location and Clearance

(2) Left-hand solenoid. This adjustment is made with the door open using a long shank Phillips screwdriver to loosen the left-hand solenoid adjusting screws.

(3) Slide the solenoid toward or away from the link arm to decrease or increase the gap as required. Securely tighten the solenoid adjusting screws.

NOTE

To reach forward adjusting screw, the shank of the screwdriver must pass between the top edge of the bezel and the left edge of the switch bracket. Avoid scratching either surface.

6.15.2.3 Cartridge Seating Test and Adjustment

Check the clearance between the right and left cartridge posts and the top surface of the cartridge receiver deck. Refer to Figure 6-35.

If the surface of the cartridge receiver falls outside the illustrated dimensions (i.e., 0.010 inch minimum, 0.030 inch maximum) perform the following adjustment procedure.

NOTE

The front door must be closed to make the following adjustments.

(1) Determine that the front edge of each door cam is perpendicular to the surface of the base.

(2) Prior to making any adjustments between either of the cartridge posts and the top surface of the cartridge receiver deck, be sure that the foot of the door cam is in full contact with the deck.

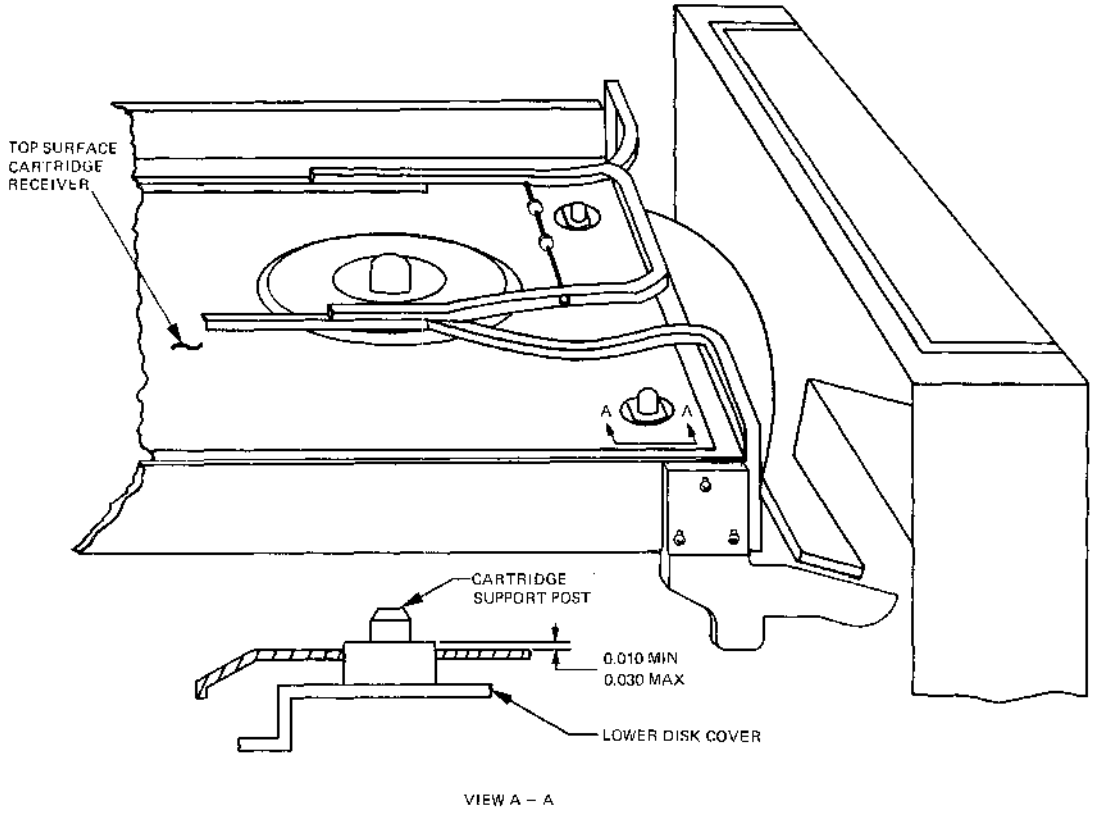


Figure 6-35. Cartridge Support Post Clearance Limits

(3) Loosen the door cam screws on each door cam and elevate or lower the cartridge receiver surface until the clearances are obtained in relation to each cartridge post as shown in Figure 6-35.

(4) Tighten the door cam retaining screws. Recheck dimensions and determine the foot of each door cam is in full contact with the base.

(5) Open and close the door several times to ensure adjustment is correctly made.

(6) Insert and remove a disk cartridge several times; recheck clearance.

(7) Check door opening clearance and perform the adjustment outlined in Paragraph 6.15.2.4 if necessary.

6.15.2.4 Door Opening Clearance Test and Adjustment

With power removed from the disk drive, the allowable door opening travel, shown in Figure 6-36, is between 0.22 and 0.41 inches. The door opening travel is measured between the door handle and the bezel at the right and left sides with approximately 8 ounces of opening pressure.

If required, the clearance adjustment is made by loosening the 3 screws holding the cam in place and rotating the cam. See Figure 6-37. Increasing or decreasing the pin gap corresponds to increasing or decreasing the door clearance.

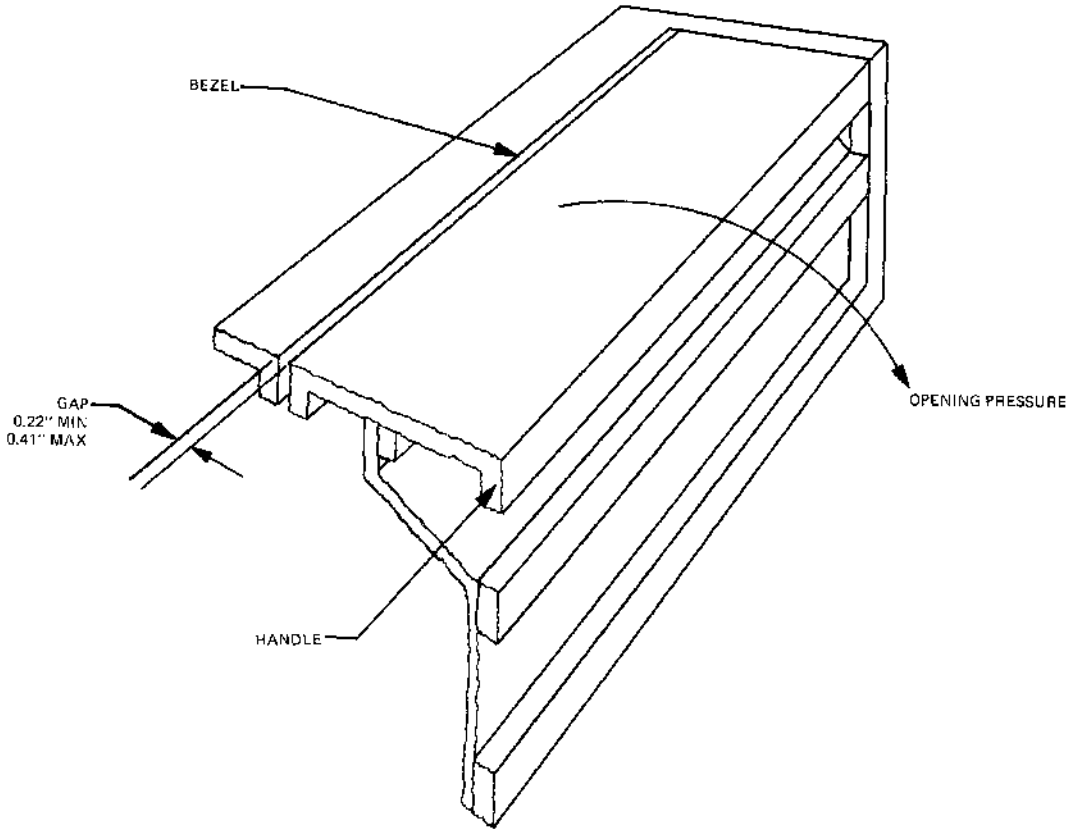


Figure 6-36. Door Opening Limits

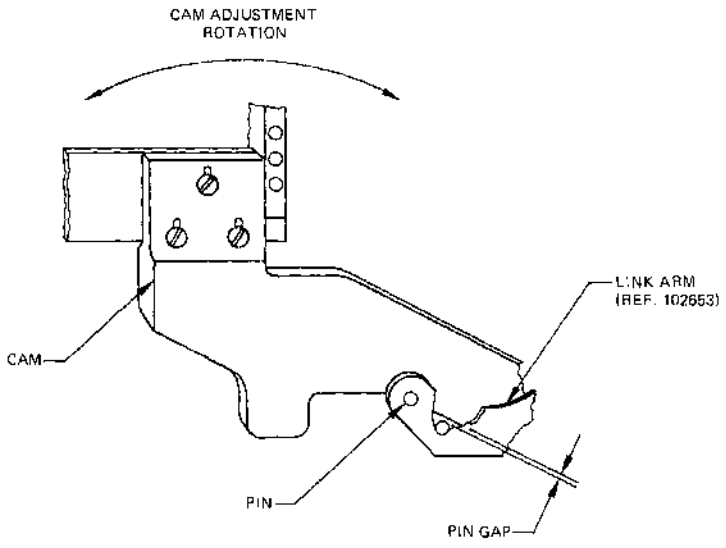


Figure 6-37. Cam Adjustment Rotation

Ensure that the cartridge seating clearance established in Paragraph 6.15.2.3 is maintained. Note that when opening the door the pins in the link arm should contact their respective cams at the same time to maintain even receiver elevation.

6.15.2.5 Interlock Switch Test

The cartridge interlock switch is a leaf-actuated snap-action switch that is part of the upper sector sensor assembly attached to the top of the lower disk cover. The actuating leaf arm of the switch extends upward through the front center of the cartridge receiver and contacts the cartridge case.

The switch senses the correct location of the cartridge in the disk drive; this ensures that the cartridge is properly located upon the spindle and is ready for operation. The switch is electrically connected to control circuits on the Logic PCBA via connector P109.

To test for correct operation, perform the following.

(1) Remove power from the disk drive.

(2) Elevate the Logic and Servo PCBAs to the maintenance position.

(3) Remove connector P109 from the Logic PCBA.

(4) Connect a suitable continuity indicating device, such as an ohmmeter, to pins 1 and 2 of P109.

(5) Apply power to the disk drive.

(6) When the SAFE indicator becomes illuminated, open the front door and install a disk cartridge.

(7) Slowly close the door and note where the switch establishes continuity.

NOTE

The cartridge must not have completed its travel at this point and should not be completely seated.

(8) Reinstall P109 onto the Logic PCBA.

(9) If the requirements of Step (7) are not met, perform the adjustment procedure contained in Paragraph 6.15.2.6.

6.15.2.6 Interlock Switch Adjustment

(1) Remove the disk cartridge.

(2) Adjust the actuating leaf of the interlock switch by bending the leaf with a pair of long-nose pliers.

(3) Return the disk cartridge into cartridge receiver and perform the test procedure contained in Paragraph 6.15.2.5, Steps (1) through (7).

(4) Open and close the door several times with the disk cartridge in place to ensure reliable operation.

(5) Disconnect the indicating device connected to P109 in Paragraph 6.15.2.5, Step (4).

(6) Reinstall P109 onto the Logic PCBA.

(7) Lower the Logic PCBA from the maintenance position to the normal operating position.

(8) Replace dust cover and return the disk drive into enclosure.

6.16 CARTRIDGE INTERLOCK SYSTEM — TOP LOAD MODELS

The top load disk cartridge is protected against physical damage by an electromechanical interlock system. This system, which is described in Paragraph 3.10, prevents the operator from removing a disk cartridge unless the drive is in the Safe condition, the spindle has stopped rotating and the heads have been fully retracted. It also inhibits the Start sequence when the cartridge has been improperly installed by the operator.

There are two identical interlock mechanisms located around the rim of the cartridge adapter assembly. Each mechanism consists of a locking cartridge sense arm, a snap action interlock switch, and a solenoid. When properly positioned, the sense arms and the solenoids prevent disk cartridge removal. The interlock switches sense when a disk cartridge is properly installed.

In addition to the interlock mechanism, suitable logic and drivers are provided on the Servo and Logic PCBAs to control the system. Electrical connections are made via connector P109 to the Logic PCBA.

6.16.1 CHECKING THE INTERLOCK SYSTEM

Proper adjustment of the interlock system may be verified as follows.

(1) Prepare the disk drive to receive a disk cartridge as outlined in Paragraph 3.3.

(2) Install a disk cartridge as detailed in Paragraph 3.4.3. Depress the RUN/STOP switch.

(3) When the READY indicator is illuminated, apply approximately a 5-pound torque to each cartridge sense arm in the unlocking direction.

(4) If the disk drive continues to function normally, as evidenced by continuous illumination of the READY indicator, the interlock system upper limit adjustments are within tolerance.

(5) Actuate the RUN/STOP switch. When the SAFE indicator is illuminated, remove the disk cartridge and reinstall the lower cover of the cartridge and lock the arms.

(6) Actuate the RUN/STOP switch. If the solenoids do not lock in place the interlock system lower limit is within tolerance.

CAUTION

SHOULD THE ARMS LOCK, REMOVE THE POWER IMMEDIATELY AND PROCEED TO MAKE CORRECTIVE ADJUSTMENTS.

6.16.2 ADJUSTING THE INTERLOCK SYSTEM

6.16.2.1 Test Configuration

(1) Extend the disk drive fully forward out of the rack; remove the disk cartridge and remove the source of power by disconnecting the line cord.

(2) Remove the dust cover as described in Paragraph 2.2, Step (5). Elevate the Logic PCBA to the maintenance position.

6.16.2.2 Solenoid Stroke Test and Adjustment

NOTE

Instructions apply to each solenoid, unless otherwise indicated.

Check the stroke adjustment of the solenoid. With the solenoid plunger manually depressed and the lock arm unlocked, the distance from the end of the plunger to the curved surface of the lock arm body must be from 0.04 to 0.08 inches as shown in Figure 6-38. If adjustment is required, loosen the adjusting screws and position the solenoid body until the proper clearance is obtained.

6.16.2.3 Lock Arm Travel Test and Adjustment

NOTE

Instructions apply to each solenoid, unless otherwise indicated.

Check the lock arm travel by rotating the lock arm to the locked position; attempt to insert an 0.030-inch thick feeler gauge between the neck of the lock arm and the adapter casting, as shown in Figure 6-39. If the clearance is greater than 0.030-inch, adjust to correct clearance by loosening the retaining screws and sliding the solenoid body laterally across the mounting bosses until the clearance is less than 0.030-inch. After completing the adjustment, determine that the solenoid plunger is not binding against the lock arm body and is free to engage and disengage under its own spring force. Ensure that the stroke adjustment detailed in Paragraph 6.16.2.2 has not changed.

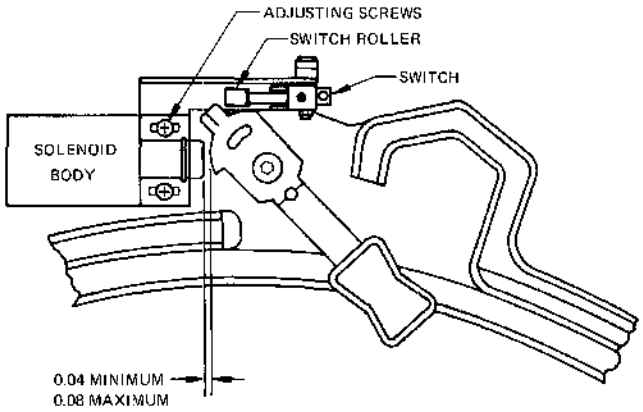


Figure 6-38. Retracted Solenoid Plunger and Lock Arm Clearance

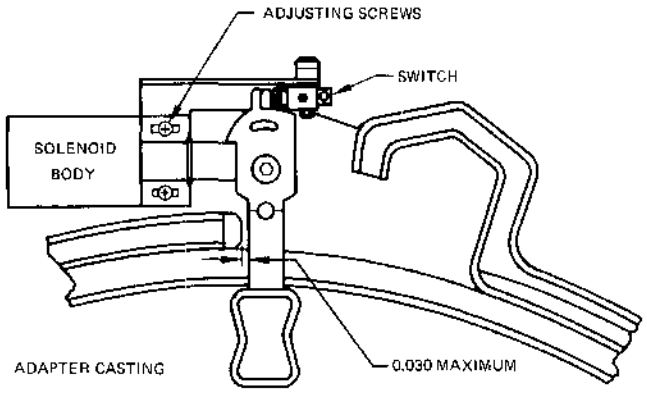


Figure 6-39. Adapter Casting and Lock Arm Clearance

6.16.2.4 Snap Action Switch Test and Adjustment

NOTE

Instructions apply to each solenoid, unless otherwise indicated.

(1) Remove power from the disk drive.

(2) Remove P109 from the Logic PCBA.

(3) With a suitable continuity indicating device, monitor the switch closure between pins 1 and 2 in the connector for the left side interlock, and pins 4 and 5 in the connector for the right side interlock.

(4) Install adapter bowl setup tool, PERTEC Part No. 103619-01, onto the spindle cone. See Figure 6-40.

(5) Manually depress the solenoid plunger and rotate the lock arm to the locked position over the NO-GO position marked on the tool. See Figure 6-41. There should be no switch closure observed between pins 1 and 2 or between pins 4 and 5.

(6) Retract the lock arm and move the tool to the GO position.

(7) Manually depress the solenoid plunger and rotate the lock arm to the locked position over the GO portion of the tool. Contact closure should be observed between pins 1 and 2 and between pins 4 and 5.

(8) Adjust the closure point if required by loosening the No. 2 machine screws securing the switch in place and sliding the switch body vertically until the previously established requirements are met. Remove the tool.

(9) Reinstall P109 onto the Logic PCBA.

(10) Return the Logic PCBA to the normal position.

(11) Reinstall the dust cover and return the disk drive to the enclosure.

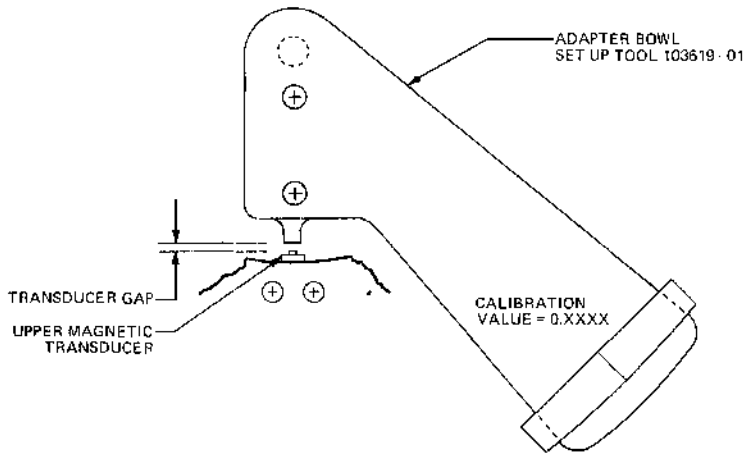


Figure 6-40. Upper Magnetic Transducer Gap

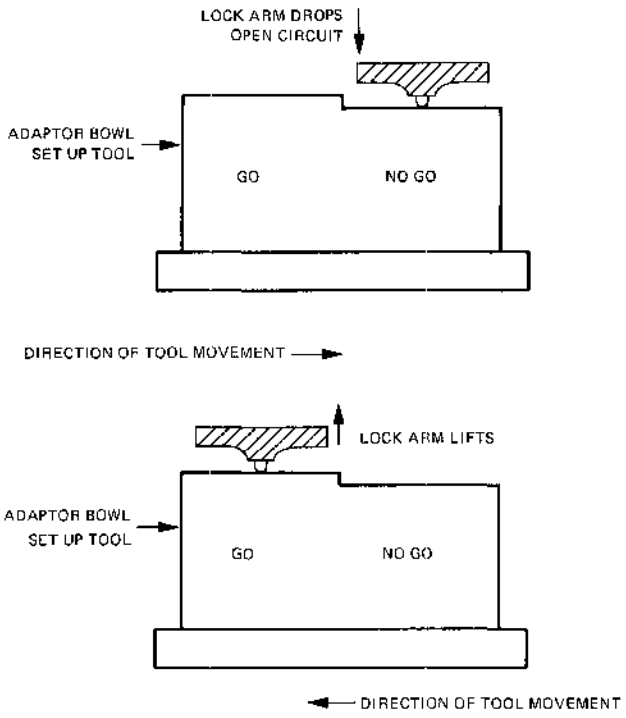


Figure 6-41. GO/NO GO Adjustment Tool, End View

6.17 BEZEL AND POWER SWITCH

6.17.1 REMOVAL OF BEZEL

Removal or adjustment of the bezel is made by loosening three socket-head countersunk Allen machine screws securing the assembly to the base assembly.

NOTE

The holes through which the screws pass are slotted to allow for bezel removal without removing screws.

To remove the bezel, proceed as follows.

(1) Back-off the six machine screws enough to clear the bezel supports on each side of the bezel.

(2) Pull the assembly forward and away from the deck assembly.

(3) Access to parts requiring replacement or adjustment is now available.

6.17.2 INSTALLATION OF BEZEL

To install the bezel, proceed as follows.

(1) Ensure that the six machine screws are backed-off enough to clear the bezel support on each side of the bezel.

(2) Carefully position the bezel to the deck assembly and secure the bezel mounting screws.

NOTE

Front loading disk drives require that the door gap adjustments described in Paragraph 6.15.3 be performed after reinstallation of the bezel.

6.17.3 REMOVAL OF POWER SWITCH BRACKET

Remove the bezel as outlined in Paragraph 6.17.1. Access to three switch bracket screws is now available. Two mounting screws are located below the bracket and one is located to the right side of the bracket. See Figure 6-42.

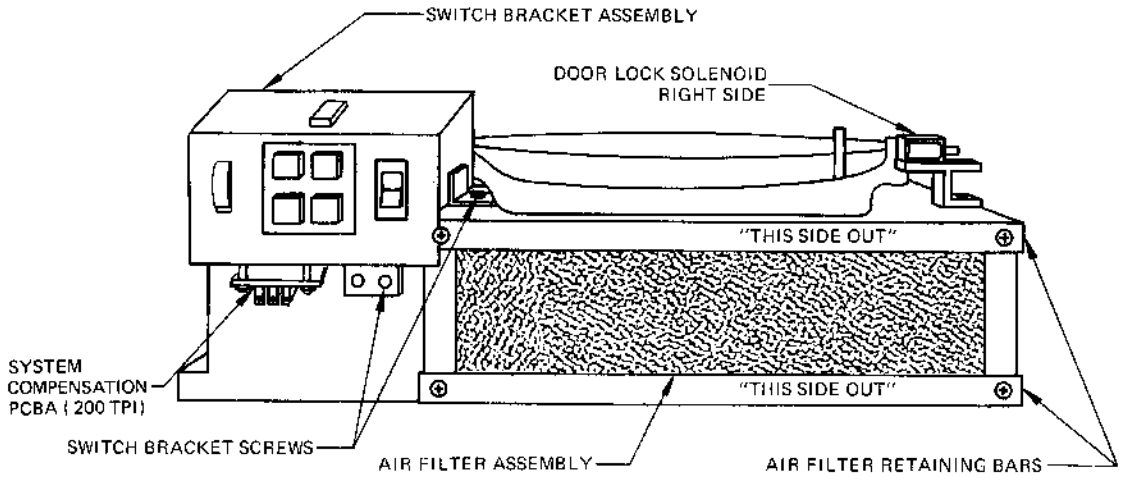


Figure 6-42. Switch Bracket, Solenoid Bracket and Air Filter Retaining Screw Locations

6.18 MAGNETIC TRANSDUCER GAP

Magnetic transducers are used in one place on front load models, and are used in two places on top load models. In each case the distance between the transducer pole tip and its respective rotating surface must be precisely controlled to produce acceptable signal levels.

Paragraphs 6.18.1 and 6.18.2 describe the test and adjustment procedures. The transducer gap is checked and adjusted as follows for top loading disk drives; Paragraph 6.18.3 provides test and adjustment instructions for front loading disk drives.

6.18.1 UPPER TRANSDUCER TEST AND ADJUSTMENT — TOP LOAD MODELS

Extend the unit forward out of the rack and install the Adapter Bowl Setup Tool (PERTEC Part No. 103619-01) onto the spindle cone. Exercise care to ensure that cone and tool are clean and free of dirt.

CAUTION

WHEN GAUGING GAP CLEARANCE, ENSURE THAT NO DAMAGE IS MADE TO THE SENSING TIP OF THE TRANSDUCER BY THE FEELER GAUGE.

A feeler gauge is used to measure the gap distance between the transducer pole tip and the tool. See Figure 6-40. Each adapter bowl setup tool will have marked on it a calibration value to be added to the nominal feeler gauge value.

The nominal feeler gauge value is given in Table 6-6. The calibration value for the particular tool is added to the value obtained from the table and rounded to the nearest half mil to obtain the actual feeler gauge thickness to be used. A single feeler gauge blade, or two or more stacked, may be used to obtain the thickness required. Use clean dry blades.

Table 6-6

Upper Transducer Calibration Data

Adapter Bowl Setup Tool Revision Level	Allowable Nominal Armature Plate Notch Width	Nominal Feeler Gauge Value	Allowable Armature Plate Diameter	Maximum Allowable Armature Plate Runout (TIR*)
A	0.080"	0.019"	5.738 +0.005"	0.010"
B and subsequent	0.080" 0.040" 0.020"	0.009"	5.738 +0.002"	0.003"
	0.080"	0.029"	5.738 +0.005'	0.010"
	2,03mm	0.029	145,745 +0,2mm	0,4mm

*Total Indicated Runout.

If the gap clearance requires adjustment, carefully loosen the No. 4 machine screws which secure the transducer clamp a slight amount. Position the transducer body to the required clearance. Tighten screws and recheck gap clearance. When the gap is adjusted, the circumferential alignment procedure detailed in Paragraph 6.13.8 must be performed.

CAUTION

LOOSENING BOTH CLAMP SCREWS COMPLETELY WILL CAUSE THE LOWER HALF OF THE TRANSDUCER CLAMP TO DROP ONTO THE LOWER DISK.

6.18.2 LOWER TRANSDUCER ALIGNMENT — TOP LOAD MODELS

The gap clearance between the transducer pole tip and the phase lock ring located on the spindle should be 0.007 ± 0.001 inch. See Figure 6-43. A feeler gauge is used to establish the clearance between the transducer pole tip and the center of a phase lock ring segment located on the spindle.

CAUTION

WHEN GAUGING GAP CLEARANCE ENSURE THAT DAMAGE IS MADE TO THE SENSING TIP OF THE TRANSDUCER BY THE FEELER GAUGE.

When the gap clearance requires adjustment, slightly loosen the No. 4 machine screws securing the transducer clamp.

CAUTION

LOOSENING BOTH CLAMP SCREWS COMPLETELY WILL CAUSE THE LOWER HALF OF THE TRANSDUCER CLAMP TO DROP ONTO THE LOWER DISK.

Position the transducer to establish correct gap clearance and retighten clamping screws. Recheck gap clearance.

6.18.3 LOWER TRANSDUCER ALIGNMENT — FRONT LOAD MODELS

The gap clearance between the transducer pole tip and the phase lock ring located on the spindle should be 0.007 ± 0.001 inch. See Figure 6-44. A feeler gauge is used to establish the clearance between the transducer pole tip and the center of a phase lock ring segment located on the spindle.

CAUTION

WHEN GAUGING GAP CLEARANCE, ENSURE THAT NO DAMAGE IS MADE TO THE SENSING TIP OF THE TRANSDUCER BY THE FEELER GAUGE.

When the gap clearance requires adjustment, slightly loosen the No. 4 machine screws securing the transducer clamp.

CAUTION

LOOSENING BOTH CLAMP SCREWS COMPLETELY WILL CAUSE THE LOWER HALF OF THE TRANSDUCER CLAMP TO DROP ONTO THE LOWER DISK.

Position the transducer to establish correct gap clearance and retighten clamping screws. Recheck gap clearance.

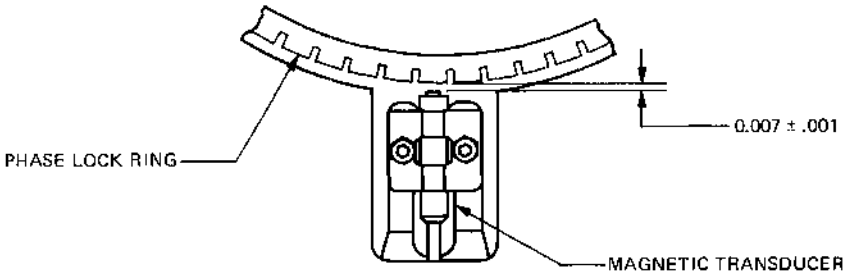


Figure 6-43. Lower Transducer Alignment, Top Load

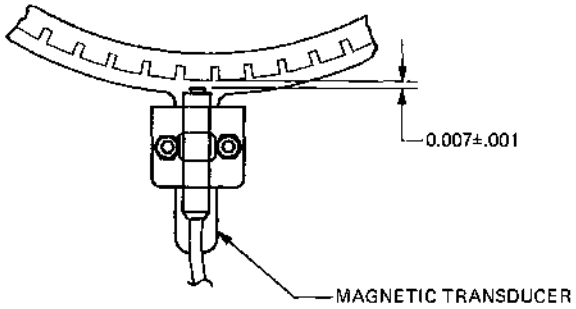


Figure 6-44. Lower Transducer Alignment, Front Load

6.19 DISK DRIVE PULLEY SYSTEM

The disk drive utilizes a flat belt and crowned pulleys to operate the spindle and blower at correct speeds. Operation at 1500 and 2400 rpm is obtained at 50 or 60 Hz by changes of pulley sizes and belt length. Refer to Table 6-7 for identification of belt and pulley combinations.

6.19.1 BELT REMOVAL

Location of pulleys and direction of rotation is indicated in Figure 6-45. To replace a belt, proceed as follows.

(1) Remove three No. 10 machine screws securing the belt guard in place.

(2) Slide the belt guard forward until it drops away from the base.

(3) Insert a large shanked screwdriver between the tension idler plate and the base. Compress the tension idler spring until the belt is released from the motor pulley.

(4) Remove the belt from area.

6.19.2 BELT REPLACEMENT

The following sequence is followed when replacing a drive belt. Refer to Figure 6-45 for threading pattern.

(1) Loop one end of drive belt around spindle pulley. Center the belt on crown of pulley and, by hand, hold the remainder of belt taut until Step (2) is completed.

(2) Feed the remainder of the belt loop under the idler tension roller arm.

NOTE

At this point the outside face of the belt contacts the crown of the tension roller.

(3) Feed the remainder of the belt loop again under the tension roller arm and up toward the blower pulley.

Table 6-7

Pulley and Belt Identification

Disk Speed	Line Frequency	Motor Pulley P/N and Crown Dia.	Blower Pulley P/N and Crown Dia.	Spindle Pulley P/N and Dia.	Belt P/N and Inside Circum.
1500 rpm	60 Hz	102636-01 1.720"	102722-01 1.720"	102635-02 3.470"	102634-01 42.1875"
1500 rpm	50 Hz	102636-02 2.143"	102722-01 1.720"	102635-02 3.470"	102634-02 42.7812"
2400 rpm	60 Hz	102636-02 2.143"	102722-02 2.143"	102635-01 2.686"	102634-01 42.1875"
2400 rpm	50 Hz	102636-03 2.563"	102742-02 2.143"	102635-01 2.686"	102634-02 42.7812"

*Inside circumference + 0.125".

- Tension Roller P/N 102609-01; 1.950" Dia.
- Drive Motor P/N 103579-01

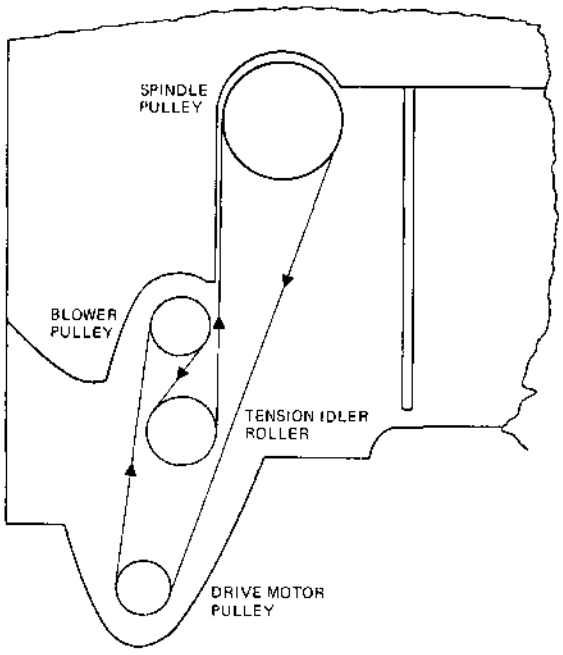


Figure 6-45. Belt Threading Pattern

(4) Loop the belt around the blower pulley. Release the loop and extend the remainder of the belt loop to the drive motor pulley.

NOTE

At this point the inside face of the belt contacts the traction area of the blower pulley.

(5) Continue the remainder of the belt loop up to the drive motor pulley. Spread the belt apart to form a loop which can be slid down and around the traction area of the drive motor pulley.

(6) With a large shank screwdriver (used as a crowbar) pry the tension arm forward by compressing the tension arm spring toward the front of the base. This action will establish enough slack in the belt to allow the belt loop mentioned in Step (5) to be slipped down and around the drive motor pulley. Release pressure on the tension arm.

(7) Inspect the belt for location on all driven surfaces and also determine that the belt does not contact any surface that will cause belt abrasion.

(8) By hand, pull the belt through several revolutions of the drive system in order to allow the belt to seek its normal operating path. This action will also establish the correct tension of the belt between pulley spans.

NOTE

If the belt comes in contact with any structural member, either raise or lower the drive motor pulley on the motor shaft until the belt clears the obstruction.

(9) Lubricate the static discharge contact located on the end of the spindle shaft with conductive lubricant, PERTEC Part No. 665-0006, or equivalent. (See Paragraph 6.20.)

(10) Reinstall the belt guard.

(11) Return the disk drive into the enclosure.

6.20 STATIC DISCHARGE LUBRICATION

The static discharge contact is located on the guide pulley cover. This contact provides a ground path from the spindle shaft to ground. The grounding of the spindle shaft thus prevents a buildup of static electricity on the disk surface. Lubrication is required to minimize wear between the spring and contact.

Lubrication is made as follows.

(1) Remove three No. 10 machine screws securing the belt guard in place.

(2) Slide the belt guard forward until it is free of the base.

(3) Lubricate the static discharge contact located on the end of the spindle shaft with conductive lubricant, PERTEC Part No. 665-0006, or equivalent.

(4) Reinstall the belt guard.

(5) Return the disk drive into the enclosure.

6.21 CARE AND HANDLING OF HEADS

Figure 6-46 shows examples of proper care and handling of the magnetic heads. Peak performance of the disk drive cannot be expected unless proper care is taken when handling these heads.

Figure 6-47 shows examples of improper handling of the magnetic heads; these examples are only a few of the ways a head can be damaged by improper care.

6.21.1 LOAD PIN SEATING

Proper seating of the load pin is essential to ensure gimbaling and flying characteristics of the ceramic slider. Examples of correct and incorrect positions of the load pin are shown in Figure 6-48. If any of the incorrect examples exist upon any head or if the gimble spring is damaged, the head assembly must be replaced.

6.22 HEAD REMOVAL AND INSTALLATION

Removal of a head is occasioned by mechanical damage, electrical failure, or for the purpose of cleaning. In the event one head needs attention, it is recommended that all heads be removed from the carriage, inspected, and cleaned. It is also recommended that data stored on the lower platter be transferred to a cartridge prior to any head removal.

6.22.1 HEAD REMOVAL PROCEDURE

The magnetic head is removed as follows.

(1) Disconnect the disk drive from the source of power.

(2) Extend the drive fully forward from the enclosure.

(3) Remove the dust cover (refer to Paragraph 2.2).

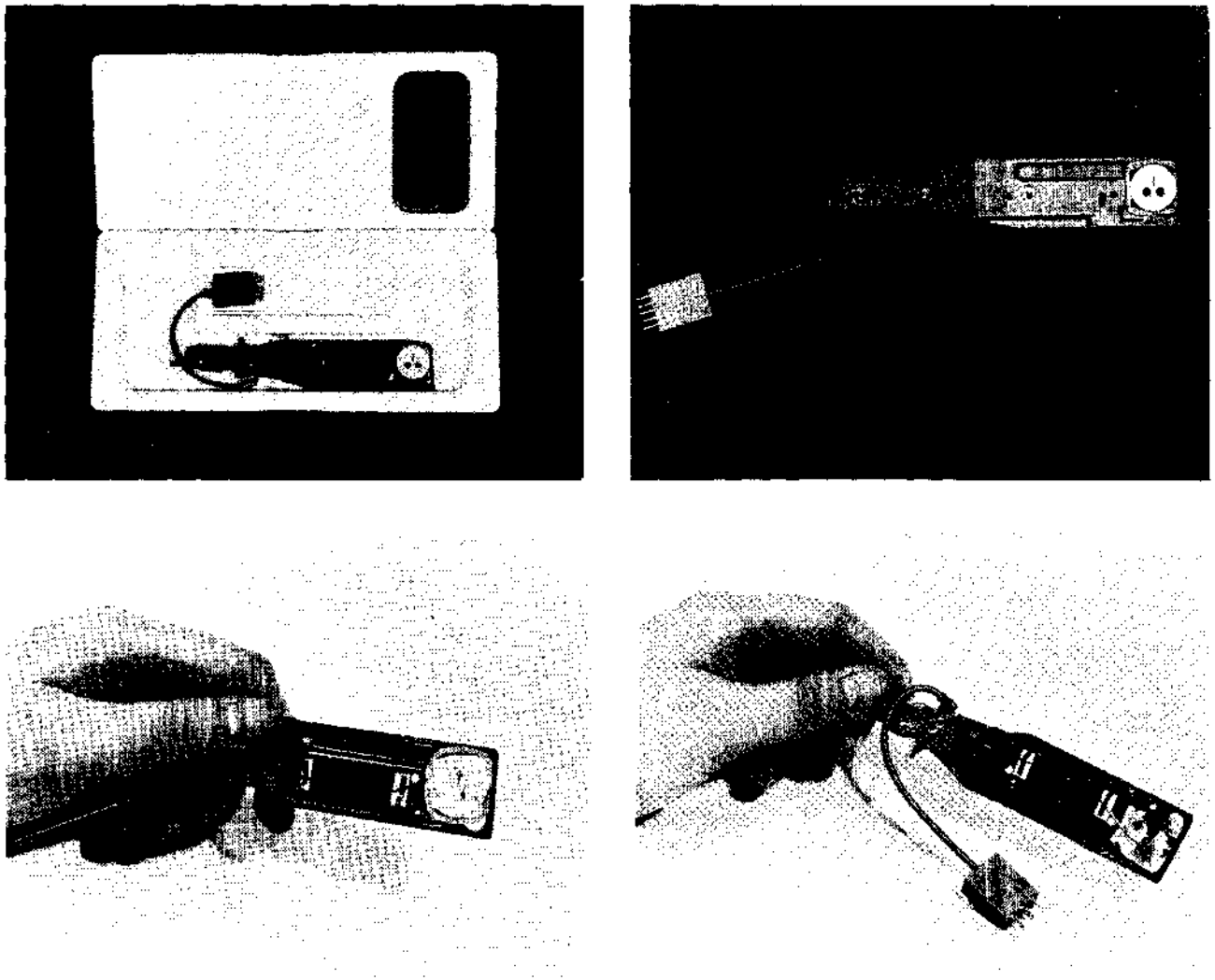


Figure 6-46. Examples of Proper Care and Handling of Heads

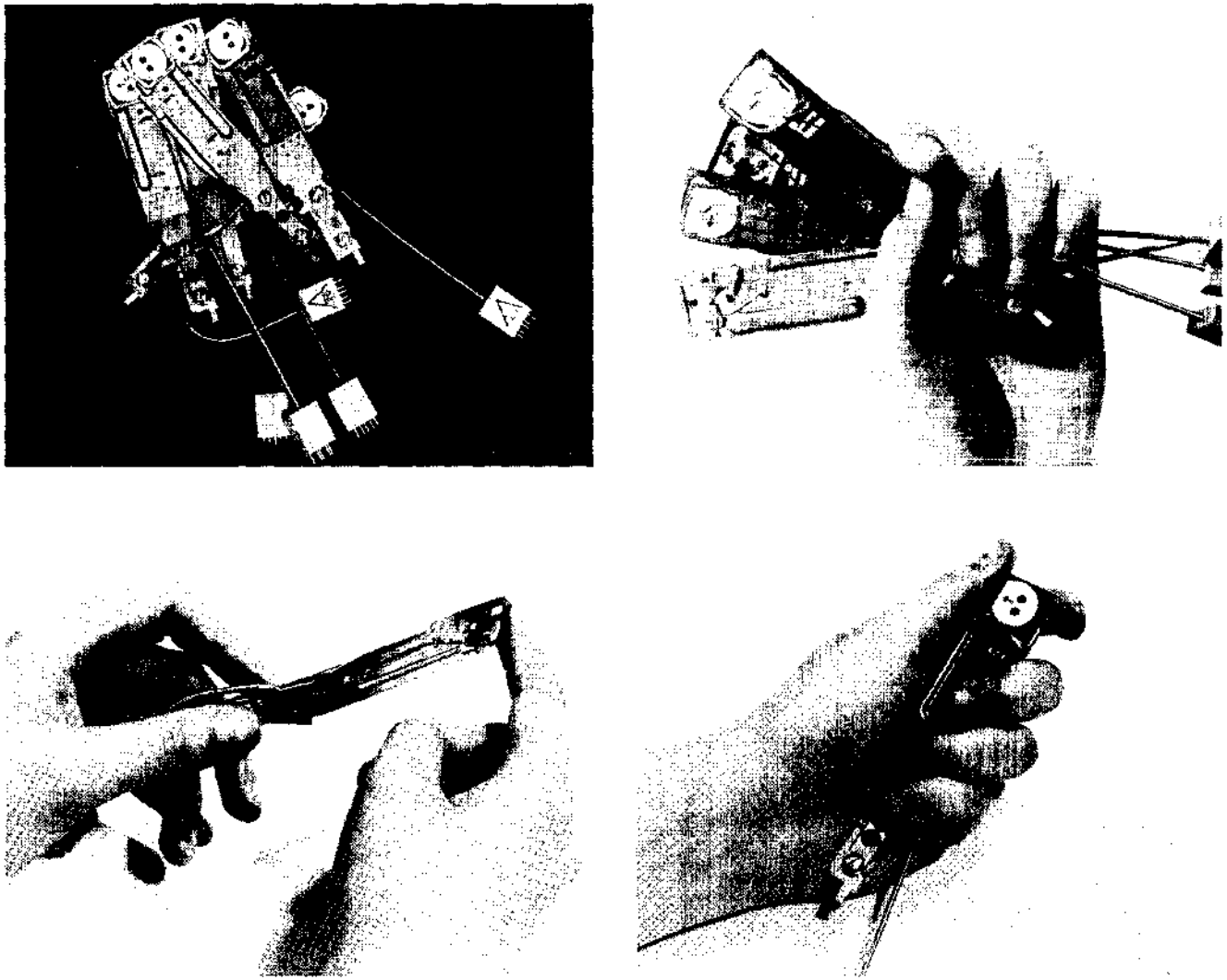
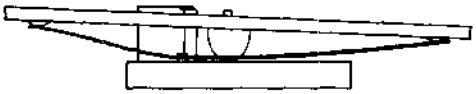
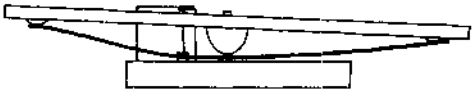


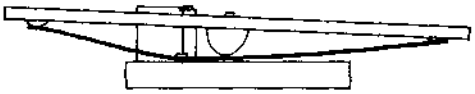
Figure 6-47. Examples of Improper Care and Handling of Heads



LOAD PIN PROPERLY IN CONTACT WITH SLIDER



LOAD PIN NOT CONTACTING THE SLIDER



LOAD PIN IMPROPERLY SEATED ON FLEXURE ARM

Figure 6-48. Load Pin Seating

(4) Disconnect head connectors from the Read/Write PCBA.

NOTE

The steel protective sheath on each connector lead is magnetic and will allow the connectors to be laid on the side surface of the magnet, thus preventing damage to the connectors while removing other components.

(5) Disconnect all connectors from the Read/Write PCBA and remove the PCBA from the disk drive.

(6) On 100 tpi models, determine that the protective cover is in place over the position transducer scale.

(7) Prepare two lint-free pads, approximately 1-inch square and 1/8-inch thick. Lay a lint-free wipe on a clean flat surface on which to lay the heads when they are removed from the carriage.

(8) Refer to Figure 6-49 for parts identification of 100 tpi models.

(9) Insert between the ceramic sliders of each pair of heads the pads prepared in Step (7); these will protect the ceramic sliders if they clash together as they are being removed.

(10) Backoff the eight Allen head setscrews in the clamp plate(s) to a position where the point of each screw is recessed below the surface of the clamp plate.

CAUTION

THE CARRIAGE MUST BE FULLY RETRACTED AND REMAIN RETRACTED WHILE REMOVING HEAD ASSEMBLIES.

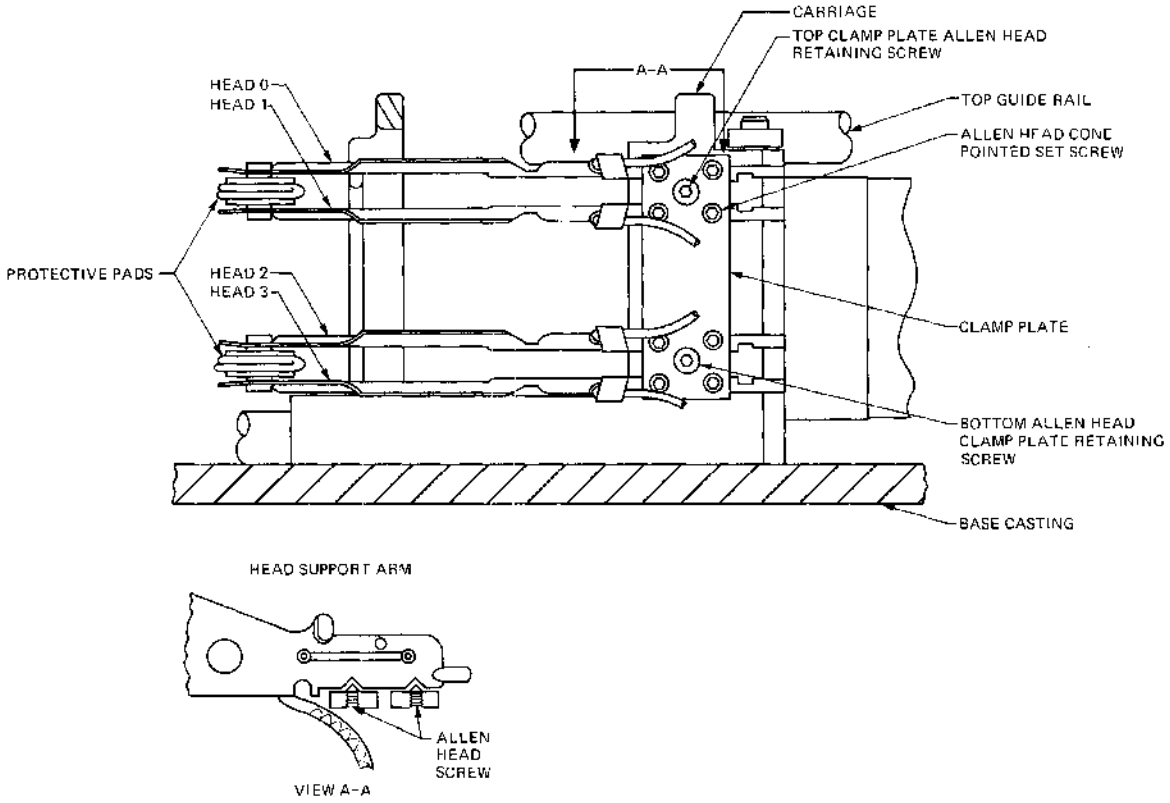


Figure 6-49. Heads Installed on Positioner Carriage

(11) Remove the top and bottom clamp plate Allen head machine screws. Remove the clamp plate screws and spacers from the carriage.

(12) Determine that spacers between each pair of heads remain on screw shanks when the clamp plate was removed from carriage; if not, individually remove each spacer from carriage area before proceeding further.

(13) Remove the heads in the following sequence: head 0 (top), head 1 (second), head 2 (third), and head 3 (bottom).

CAUTION

EXERT EVERY PRECAUTION TO PREVENT DAMAGE TO THE GIMBLE SPRING AND THE CERAMIC SLIDER WHILE REMOVING AND HANDLING HEADS.

- Apply to the head end of the support arm sufficient pressure with thumb and forefinger to separate the body of the support arm from the ramp. Push the head arm approximately 3/8-inch straight forward into the disk cavity by applying pressure to the die cast positioning arm while holding positioning arm flat against carriage mounting surface until the arm is free of carriage slots. Again, use extreme caution not to allow the gimble spring or the ceramic slider to come in contact with any other surrounding part.
- When a head is free, place it upon a lint-free wipe in the clean area with the ceramic slider facing up.
- Remove the other heads in succession observing equal precautions for each head.

6.22.2 HEAD INSTALLATION PROCEDURE

Installation of the heads after cleaning or when replacing a damaged head is accomplished as follows.

(1) If required, perform the necessary Steps (1) through (5) of Paragraph 6.22.1.

(2) On 100 tpi models, determine that the protective cover is in place over the position transducer scale.

(3) Prior to installing heads, inspect carriage and the surrounding area for any foreign material that could contaminate heads or interfere with installation. Clean head mounting area with 91 percent isopropyl alcohol.

NOTE

Use only 91 percent isopropyl alcohol to clean disks and heads. Use of any other type of cleaner or solvent, such as carbon tetrachloride or trichlorethylene may result in damage. Do not use contaminated alcohol which could contain any form of residue.

Examine the carriage slots into which the supporting arm of the head is placed for any nicks or burrs that would obstruct installation or alignment.

(4) Examine the ceramic slider of each head for cleanliness. Also inspect gimble spring and slider pivot for proper alignment. Refer to Figure 6-48.

(5) Prepare two lint-free wipe pads, approximately 1-inch square and 1/8-inch thick; these pads will be used to separate each pair of heads to prevent possible damage to the ceramic slider during installation.

(6) Note that there are two V-shaped indentations on the side of the die-cast support arm. Fore and aft head alignment of several thousands of an inch can be made when the pointed screws in the clamp plate engage with the V slots in the support arm. (Figure 6-49 illustrates the support arm on 100 tpi models.)

6.22.2.1 Installation of Head to Carriage Slots

(1) Locate the threaded holes on the carriage used for the clamp plate(s) retaining screws.

CAUTION

CARRIAGE MUST BE FULLY RETRACTED AND REMAIN RETRACTED WHILE INSTALLING HEAD ASSEMBLIES.

NOTE

When installing heads, it is recommended that the bottom head [the lowest] be installed first and then progress up to the top head.

CAUTION

CARRIAGE MUST NOT BE MOVED FROM THE FULLY RETRACTED POSITION UNTIL ALL HEADS ARE SECURED IN PLACE BY THE CLAMP PLATE.

(2) Carefully guide the bottom head into place with the ceramic slider facing upward and insert the die-cast body of the support arm into the carriage slots part of the way.

(3) Visually position the support arm Vs to be approximately on center with the two retainer clamp screw holes.

(4) Firmly press the support arm back against the carriage surface and at the same time position the flange of the head on the underside of the lower ramp.

CAUTION

DO NOT OVER-STRESS HEAD GIMBLE SPRING DURING INSTALLATION.

(5) Place a lint-free wipe protective pad on the ceramic slider.

(6) In succession, install the other heads in the manner as described in the preceding steps.

6.22.2.2 Installation of Clamp Plate(s)

When all heads are in place on the carriage, proceed as follows.

NOTE

As a precaution, before installing the clamp plate[s], determine that all pointed setscrews are recessed below the surface of the clamp plate.

(1) Install the upper and lower retaining screws through the holes in the clamp plate and install the spacers previously removed over the shank of each screw.

NOTE

Under no circumstances should a clamp plate screw or a spacer be substituted for the original hardware.

(2) Tighten the clamp plate retaining screws. Torque to approximately 10 to 12-inch pounds.

CAUTION

WHEN TIGHTENING THE CLAMP RETAINING SCREWS CAUTION MUST BE TAKEN NOT TO OVER-TORQUE THE SCREWS. OVER-TORQUEING CAN CAUSE THREADS IN THE CARRIAGE CASTING TO STRIP OUT.

CAUTION

ON 200 TPI MODELS, THE TOP HEAD CLAMP IS MADE OF STEEL; THE LOWER HEAD CLAMP IS MADE OF ALUMINUM AND HAS A RED FINISH.

6.22.2.3 Head Positioning

(1) Starting with the bottom heads (three and two), run in each pair of pointed set screws so that each engages with a side of the V on the support arm to an approximate equal depth. Do not allow points of set screws to bottom out in the Vs on the arm.

NOTE

Horizontal position of Head 3 and Head 2 is not critical.

(2) Install Head 1 and Head 0 in like manner.

(3) Inspect installation; install the connectors to Read/Write PCBA.

(4) To correctly position Head 1 and Head 0, a CE alignment must be made. Refer to Paragraph 6.13 for procedure.

(5) After a satisfactory CE alignment is made, return disk drive to original configuration.

6.23 AIR FILTER

The filter assembly consists of two parts, the pre-filter which is a fine meshed foam material covering the air intake area of the absolute filter and the absolute filter. The absolute filter consists of a labyrinth of small metallic separators, forming the filter path, between the filter media.

The absolute filter is encased within a plastic frame for ease of handling and to prevent damage to the internal structure.

Handle the absolute filter by the edges of the plastic framework. Use caution not to compress the sides or center of the filter as puncturing of the filtering media could result, thereby lessening the effectiveness of the filter.

6.23.1 PRE-FILTER CLEANING

(1) Remove the bezel as described in Paragraph 6.17.1.

(2) The pre-filter is removed by lifting one corner of the meshed material and gently pulling it away from the front surface of the absolute filter.

NOTE

The pre-filter may be washed in soap and water and reused. The pre-filter must be absolutely dry and free from any cleaning residue before replacing it on the front of the absolute filter.

6.23.2 REMOVAL OF ABSOLUTE FILTER

The following procedure is used to remove the pre-filter.

(1) Refer to Paragraph 6.17.1 for the procedure to remove the bezel.

(2) Remove bezel and observe two retaining bars marked THIS SIDE OUT (see Figure 6-42). Remove the two retaining bars that are purposely curved to hold the absolute air filter under tension against the base casting.

(3) Withdraw the absolute filter from the air duct cavity in the base by grasping the two edges and pulling straight forward. After removing, inspect for any plastic chips or other matter remaining in the air duct cavity.

(4) Discard the used absolute filter.

NOTE

Always replace the absolute filter rather than attempting to clean it.

6.23.3 REPLACEMENT OF ABSOLUTE FILTER

Before installing a new absolute filter, inspect the plastic framework for any contamination. Especially inspect for plastic flashing clips or excess plastic that could be shaved off the edges by the air duct during installation. If the filter is not easily inserted into the air duct or its shape is distorted, there is a likelihood that the filter is defective and should not be used.

CAUTION

TOBACCO ASHES AND TOBACCO SMOKE WILL CONTAMINATE THE AIR SYSTEM AND THE ABSOLUTE FILTER. HANDLE THE FILTER IN THE CLEANEST ENVIRONMENT AVAILABLE.

Inspect the air duct leading up to the blower for any other matter that could have passed through the filter system. Clean with a lint-free cloth, if required. Replace the filters and secure the assembly into place. Be sure the retaining bars are correctly installed with the *THIS SIDE OUT* showing (see Figure 6-42).

6.24 POWER SUPPLY

The power supply is a removable module located in an area on the underside of the base assembly.

6.24.1 POWER SUPPLY REMOVAL

The power supply chassis may be removed as follows.

(1) Disconnect power.

WARNING

VOLTAGES MAY BE PRESENT IN THE POWER SUPPLY AREA WHICH ARE CONSIDERED DANGEROUS TO LIFE. THE EMERGENCY UNLOAD AND MOTOR START CAPACITORS MAY REMAIN CHARGED FOR A CONSIDERABLE LENGTH OF TIME, EVEN THOUGH POWER HAS BEEN REMOVED. OBSERVE EXTREME CAUTION.

(2) Extend the unit out of the cabinet and remove the dust cover (refer to Paragraph 2.2, Step (5).

(3) Position the Logic and Servo PCBAs to the maintenance position.

(4) Disconnect the power switch cable connector J501.

(5) Disconnect the power supply cables P212 and P213 at the Servo PCBA.

(6) Remove the high voltage cover from the Motor Control PCBA and disconnect P401, P402, P403, or P404.

(7) Remove the belt guard (refer to Paragraph 6.19.1, Steps (1) and (2).

(8) On 200 tpi models, the Temperature Compensation PCBA and retaining hardware should be removed prior to power supply removal.

(9) Remove 8 (or 9, depending upon the model) No. 10 screws which secure the power supply chassis to the base. Carefully lower the power supply chassis out and away from the base.

CAUTION

AVOID SQUEEZING ANY CABLES BETWEEN THE BASE AND CHASSIS DURING REMOVAL AS DAMAGE TO THE CABLING CAN RESULT.

6.24.2 POWER SUPPLY INSTALLATION

Installation of the power supply is accomplished as follows.

(1) Verify that power is removed from the drive.

WARNING

VOLTAGES MAY BE PRESENT IN THE POWER SUPPLY AREA WHICH ARE CONSIDERED DANGEROUS TO LIFE. THE EMERGENCY UNLOAD AND MOTOR START CAPACITORS MAY REMAIN CHARGED FOR A CONSIDERABLE LENGTH OF TIME, EVEN THOUGH POWER HAS BEEN REMOVED. OBSERVE EXTREME CAUTION.

(2) Extend the unit out of the cabinet and remove the dust cover (refer to Paragraph 2.2, Step (5).

(3) Position the Logic and Servo PCBAs to the maintenance position.

(4) Check connections at power transformer primary and ensure that it is connected for the correct line voltage (refer to Figure 4-14 for line voltage connections).

(5) Secure the power supply in place using the screws removed in Step (9) of Paragraph 6.24.1.

(6) Inspect all wiring extended through casting to upper deck area for crushed or abraded wires.

(7) Install the belt guard.

(8) Reconnect all cables disconnected in Steps (4) through (6) of Paragraph 6.24.1.

(9) On 200 tpi models, remount the Temperature Compensation PCBA and retaining hardware.

(10) Lower the Logic and Servo PCBAs into operating position.

(11) Inspect the interior of the disk drive for any items or parts that could interrupt operation.

(12) Return the disk drive to normal operating condition.

6.25 DISK CLEANING BRUSHES -- TOP LOAD

Top load disk drives are equipped with brushes to clean the surface of the disk(s). After the SAFE indicator is extinguished and the operating speed has been attained, the cleaning brushes sweep the disk(s). Following this cleaning operation, the positioner loads the heads over the disk(s) and the READY indicator becomes illuminated.

6.25.1 INSPECTION OF CLEANING BRUSHES

The disk cleaning brushes must be inspected for wear after every 1000 hours of operation. These nylon brushes are subject to wear as a result of contact with the high-speed rotating disk.

Acceptable brush condition is defined as when the upper and lower bristles are in contact with the brush mechanism in the parked position. Figure 6-50 illustrates both acceptable and unacceptable conditions of disk cleaning brushes.

The upper and lower disk cleaning brushes are accessible for inspection by removing the dust cover. When an unacceptable wear condition exists the brush removal and installation procedures contained in Paragraphs 6.25.2 and 6.25.3 must be performed.

6.25.2 BRUSH ASSEMBLY REMOVAL

Access to the shoulder screw that secures the brush assembly in place is made through a hole in the bowl casting beneath the right cartridge lock arm.

(1) Extend the disk drive fully forward on the slides.

(2) Remove the dust cover.

(3) Insert a long-shank 1/8-inch Allen bit through access hole and loosen the shoulder screw to the point the threads are no longer engaged with the base casting.

(4) Lift the shoulder screw and brush assembly up as a unit and free of the link pin on the actuating arm of deck casting.

(5) Remove the brushes from the actuating arm(s) by slipping them free of the retainer spring.

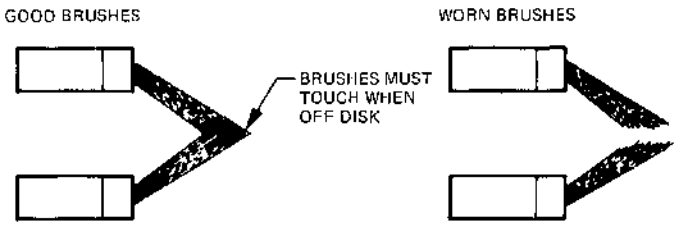


Figure 6-50. Condition of Disk Cleaning Brushes

6.25.3 BRUSH ASSEMBLY INSTALLATION

(1) Lift the brush retaining spring up and install new brushes. Note that actuating arms are matched and that there are corresponding extensions on the nylon base of the brush that must engage with the arm notches for proper alignment and spacing.

CAUTION

EXERT EVERY PRECAUTION WHEN HANDLING THE CLEANING BRUSHES. BENT OR DAMAGED BRUSHES WILL CAUSE EXCESSIVE FRICTION, RESULTING IN THE BRUSH BRISTLES MELTING ONTO THE DISK SURFACE; THIS WILL CAUSE HEAD CRASHES.

(2) Inspect the brush installation and determine that no portion of the base of the brush or any part of the retaining spring extends beyond the width of the brush actuating arm(s).

(3) With the brush assembly shoulder screw in place, place the assembly in position over the actuating arm pin on the base assembly.

NOTE

Ensure captive linking pin on actuating arm is engaged with hole in base of brush arm assembly.

(4) When all parts are lined up and properly engaged, rethread the shoulder retaining screw into the base assembly.

(5) Prepare the disk drive for operation; see Paragraph 3.3, Steps (1) through (4).

(6) Load the disk cartridge as directed in Paragraph 3.4.3, Steps (1) through (8).

(7) Operate the disk drive and observe the cleaning cycle of the brushes.

(8) Shut down the disk drive.

(9) Replace the dust cover and place the disk drive in the rack.

6.26 BRUSH ACTUATING MOTOR

The brush actuating motor is located on the underside of the deck casting; it is a 6-rpm geared induction motor. This motor, in conjunction with the brush parking switch and the linking cam, causes the disk cleaning brushes to make complete sweeps across the surface of the disk.

6.26.1 BRUSH ACTUATING MOTOR REMOVAL

The motor is removed from the disk drive as follows (refer to Figure 6-51).

(1) Remove the brush assembly as described in Paragraph 6.25.2.

(2) From the topside of the deck casting, remove the rotating brush cam from end of motor shaft.

(3) Disconnect the wiring to the brush motor.

(4) Remove the two motor mounting screws to free the motor.

6.26.2 BRUSH ACTUATING MOTOR INSTALLATION

(1) Install the replacement motor with screws originally used to mount the motor.

(2) Before securing mounting screws, center the motor shaft through the access hole in the casting and secure screws in place.

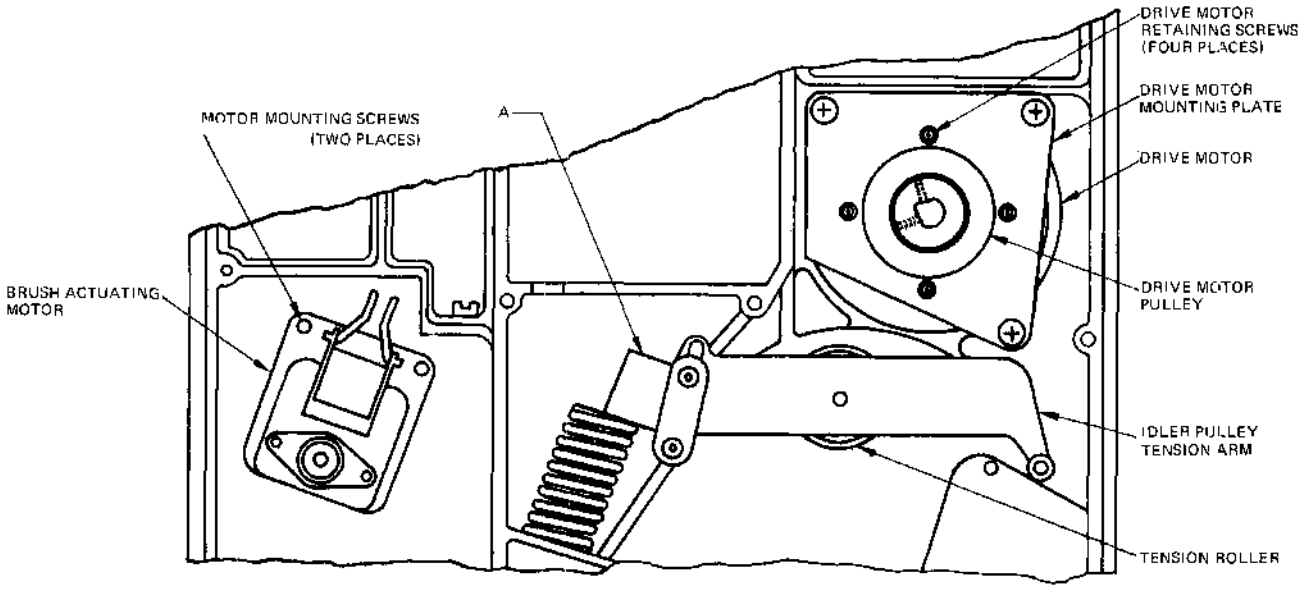


Figure 6-51. Brush Actuating Motor and Drive Motor Placement

(3) Apply power to the motor and allow the motor to operate for 10 or 20 revolutions to ensure smooth operation.

NOTE

The flat on the motor shaft must be positioned as shown in Figure 6-52 prior to installation of rotating brush cam to ensure proper retraction of the brush assembly and actuation of the brushes parked switch.

(4) Install the cam on the motor shaft. Ensure that the cam setscrew is seated on flat of the motor shaft.

6.26.3 BRUSHES PARKED SWITCH TEST AND ADJUSTMENT

Proper switch adjustment is verified as follows.

(1) Remove the dust cover and raise the Logic PCBA into the maintenance position.

(2) Apply power to the disk drive and observe that the SAFE indicator becomes illuminated.

(3) Actuate the RUN/STOP switch and observe that the brush cycle commences approximately 13 seconds after actuation of the switch. Immediately place the ON/OFF switch to OFF when the pin side of the cam is opposite the switch roller as shown in Figure 6-52.

(4) Disconnect P113 from the Logic PCBA. Remove the brush block (with brushes attached) by loosening the shoulder screw pivot and lifting the assembly off of the base.

(5) Place a 0.040 feeler gauge blade(s) between the cam and the switch roller as shown in Figure 6-52.

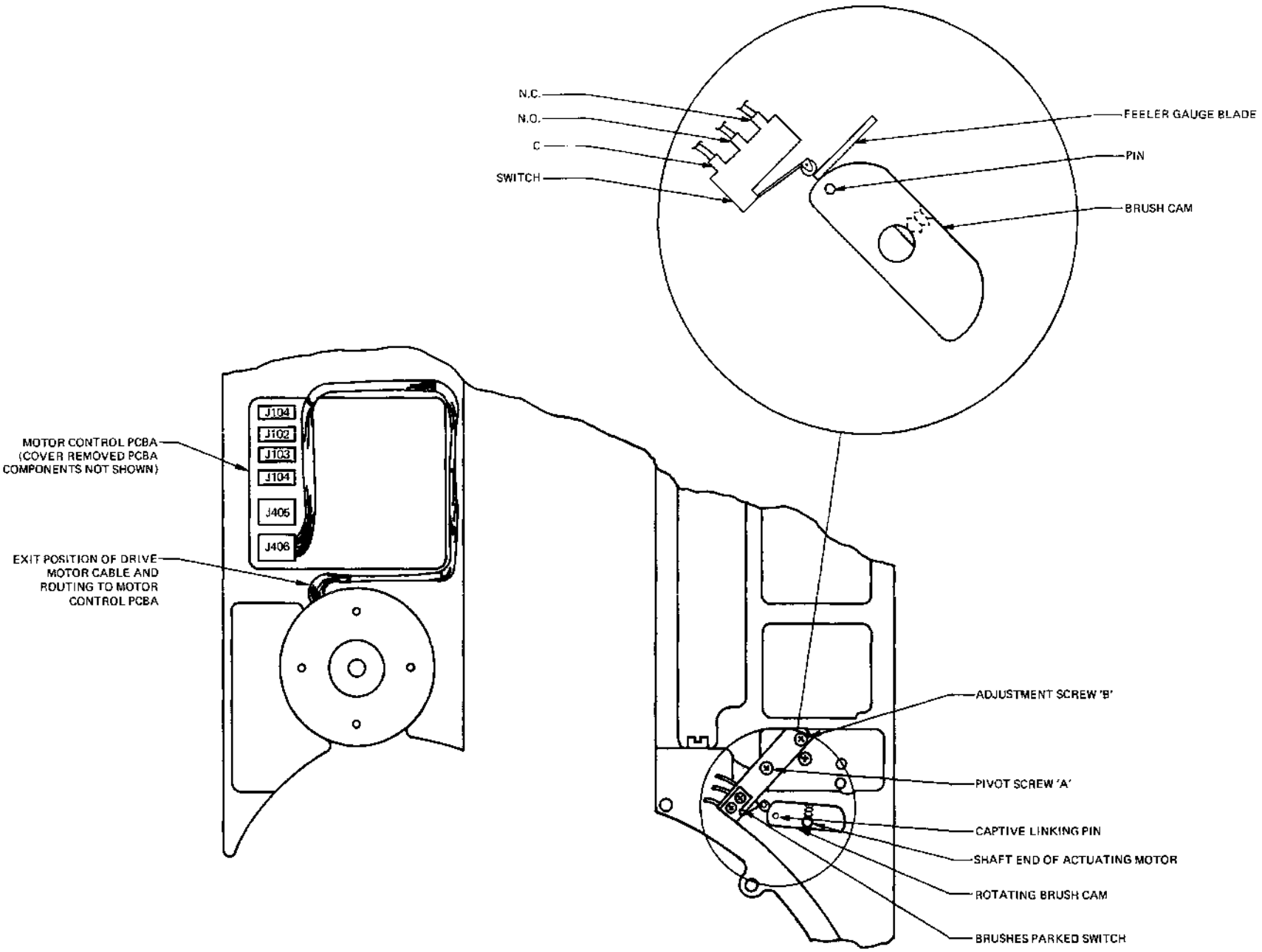


Figure 6-52. Brush Cam Installation and Drive Motor Cable Routing

(6) Verify continuity between P113 pin 1 and pin 3. Verify open circuit between P113 pin 1 and pin 2.

(7) Place a 0.060 feeler gauge blade(s) between the cam and the switch roller as shown in Figure 6-52.

(8) Verify continuity between P113 pin 1 and pin 2. Verify open circuit between P113 pin 1 and 3.

If the criteria of Step (6) or (8) cannot be met, switch adjustment is required. To adjust the switch perform the following.

(9) Place a 0.050 thick feeler gauge between the roller and the cam as shown in Figure 6-52.

(10) Loosen pivot screw A and adjustment screw B slightly. Refer to Figure 6-52.

With the switch roller in contact with the cam and gauge, move switch bracket assembly to just trip switch to read continuity from P113 pin 1 and pin 2.

(11) Secure adjustment screw B and pivot screw A.

(12) Verify adjustment by repeating Steps (5) through (8).

(13) Remove the feeler gauge.

(14) Reconnect P113 to Logic PCBA.

(15) Place the ON/OFF switch to ON and verify that brush cam correctly parks.

(16) Reinstall brush assembly onto base.

6.27 DRIVE MOTOR

6.27.1 DRIVE MOTOR REMOVAL

Refer to Figure 6-52.

(1) Pull the disk drive forward to the full extent of the slides; remove the dust cover as described in Paragraph 2.2.

(2) Raise the Servo and Logic PCBA units to the maintenance position.

(3) Remove the cover from the Motor Control PCBA.

(4) Carefully remove cable ties from the cable bundle terminating at connectors on the Motor Control PCBA and to the point where wiring to the drive motor breaks out of the cable bundle.

CAUTION

DO NOT CUT OR NICK ANY WIRES IN THE CABLE BUNDLE.

(5) Disconnect connectors P405 and P406 from the Motor Control PCBA and separate out the cable to the drive motor.

(6) Remove the belt guard; remove belt from motor pulley only (refer to Paragraph 6.19.1).

(7) Remove the motor pulley from the motor shaft.

(8) Use a thin-shank Phillips head screwdriver to remove four motor mounting screws from motor mounting plate. Refer to Figure 6-51.

(9) Remove the drive motor from the mounting plate and from the disk drive.

6.27.2 DRIVE MOTOR INSTALLATION

From the top side of the disk drive, proceed as follows. Refer to Figure 6-52.

(1) Position the motor so the motor cable exits from the motor frame as shown in Figure 6-52.

(2) From beneath the disk drive, install four motor mounting screws through the motor mounting plate. See Figure 6-51. Secure motor to plate.

(3) Install the drive motor pulley on the motor shaft.

(4) Replace belt as noted in Paragraph 6.19.2.

(5) From the top side of the disk drive, route the motor cable as shown in Figure 6-52. Install connectors P405 and P406 to the Motor Control PCBA.

(6) Retie the motor cable into the existing cable bundle.

(7) Secure the motor cable to the motor frame with tie wrap.

(8) Replace the cover on the Motor Control PCBA.

(9) Lower the Servo and Logic PCBA into operating position.

(10) Reinstall dust cover and return disk drive into enclosure.

6.28 MAINTENANCE TOOLS·

The following is a list of tools required to maintain the disk drive. All tools, except the PERTEC aligning and adjustment tools, may be obtained from local sources.

(1) Hex socket key set, 1/16- through 5/32-inch sizes.

(2) Thickness gauge.

(3) Open-end wrenches, sizes 3/16-, 1/4-, 5/16-, and 3/8-inch.

(4) Long-nose pliers.

(5) Phillips screwdriver set.

(6) Standard blade screwdriver set (heavy shank).

(7) Soldering aid.

(8) Soldering iron.

(9) Small diameter (3/16-inch shank, 8-inch long) No. 1 Phillips screwdriver.

(10) Lint-free wipes, e.g., Microwipes TX500.

(11) Lint-free cloth.

(12) Cotton swabs.

(13) Isopropyl alcohol (91 percent).

(14) Torque wrench, 0 — 15 in-lbs.

(15) Molex pin extractor (Mfg Part No. HT2285).

(16) Loctite Sealant, Grade C.

(17) Reticle adjustment tool, PERTEC Part No. 103659.

(18) Voice Coil Polarity Tester, PERTEC Part No. 103607.

(19) Circumferential adjustment tool, PERTEC Part No. 103609-01.

(20) Adapter bowl setup tool, PERTEC Part No. 103619-01.

(21) Conductive lubricant, 7 oz can, PERTEC Part No. 665-006, or equivalent.

(22) Four 6-inch mini-ball clip leads.

(23) 5/16-inch ignition open-end wrench.

SECTION VII
PARTS LISTS AND SCHEMATIC/ASSEMBLY DRAWINGS

7.1 INTRODUCTION

This section includes illustrated parts lists, spare parts lists, interconnect lists, and schematic/assembly drawings.

7.2 ILLUSTRATED PARTS BREAKDOWN (IPB)

Figures 7-1 through 7-7, used in conjunction with Tables 7-1 through 7-7, respectively, provide identification by PERTEC part number of the mechanical and electrical components of the D3000 Diablo Compatible Series Disk Drives. Notations are made for front load and top load configurations where parts do not apply to both configurations.

7.3 SPARE PARTS

Table 7-8 provides a description of the suggested spare parts for the D3000 Series Disk Drives. The Customer should always furnish the model number and the serial number of the disk drive when ordering parts.

7.4 PART NUMBER CROSS REFERENCE

Table 7-9 provides a cross reference to the manufacturers' part numbers and typical PERTEC part numbers.

7.5 INTEGRATED CIRCUIT PIN SUMMARY

A summary of the power and ground pins for the various integrated circuits employed in the D3000 Disk Drives Is contained in Table 7-10. A summary of the function control for certain integrated circuits is listed in Table 7-11.

7.6 PCBA INTERCONNECTIONS

Interconnections between PCBAs installed in the D3000 Series Disk Drives are listed in Table 7-12 and are illustrated in Figure 7-8.

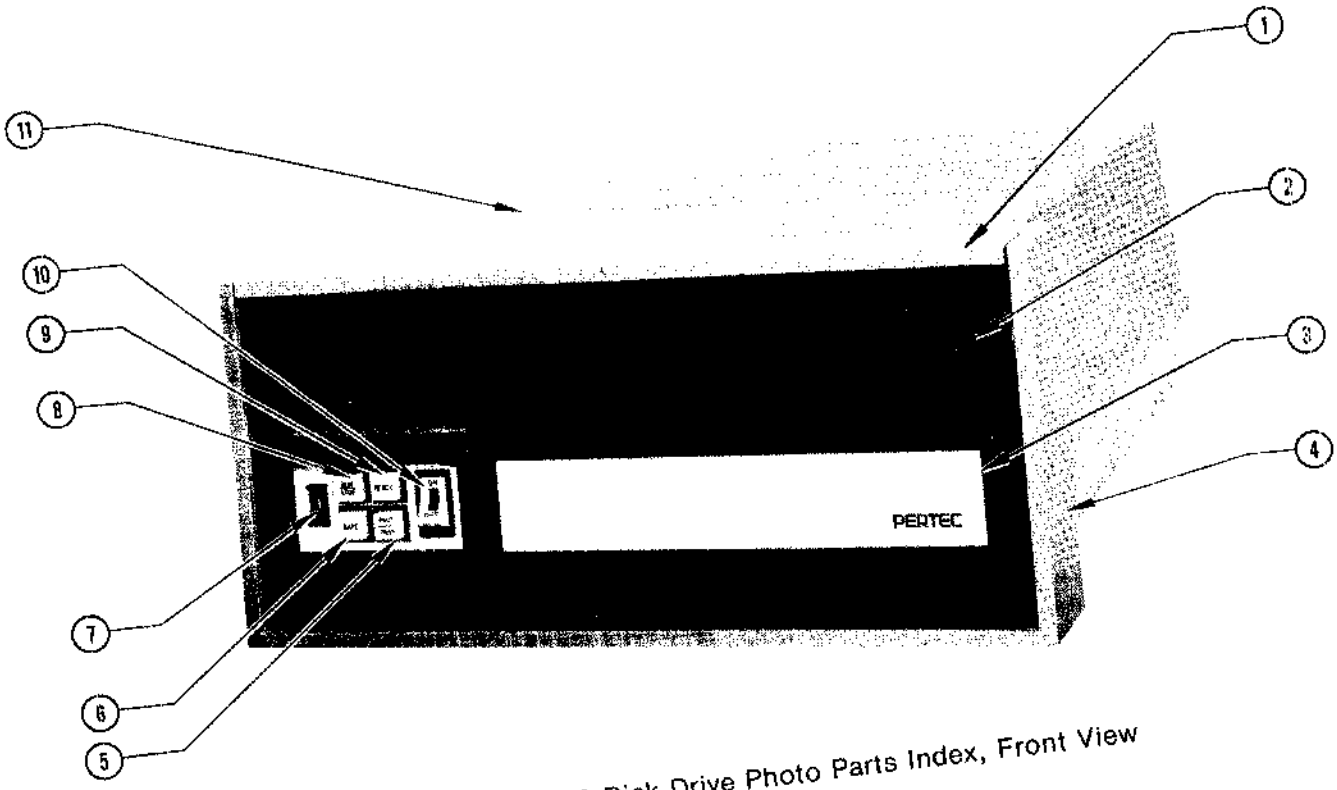


Figure 7-1. D3000 Disk Drive Photo Parts Index, Front View

Table 7-1
D3000 Disk Drive Photo Parts Index

Figure and Index No.	Part No.	Description
Figure 7-1		
-1	102644-01	Door Handle (Front Load Only)
-2	102643-01	Door
-3	102647-*	Accent Panel
-4	102703-01	Bezel Assembly (Front Load Only)
-5	509-0008 509-0005 659-0330	PROT/PROT Indicator Cap Indicator Body Lamp
-6	509-0006 509-0004 659-0330	SAFE Indicator Cap Indicator Body Lamp
-7	102759-01	Unit Selector Switch
-8	505-0002 505-0001 659-0330	RUN/STOP Switch/Indicator Cap Momentary Switch Lamp
-9	509-0007 509-0004 659-0330	READY Indicator Cap Indicator Body Lamp
-10	506-1806	ON/OFF Power Switch/Indicator
-11	103669-01 103697-01	Dust Cover (Front Load Only) Dust Cover (Top Load Only)

*Refer to Spare Parts List for Relevant Part No.

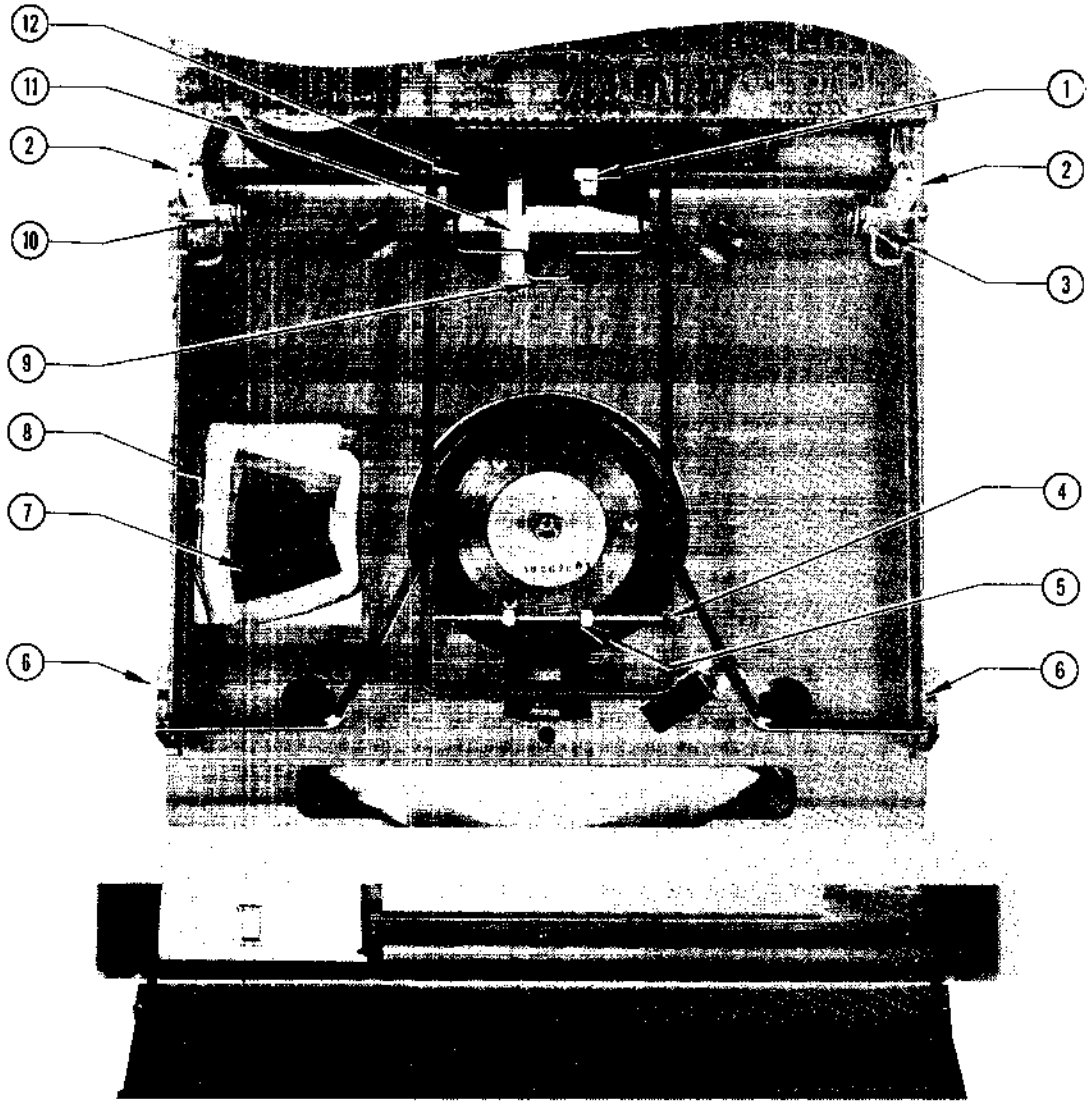


Figure 7-2. D3000 Disk Drive, Photo Parts Index

Table 7-2
D3000 Disk Drive Photo Parts Index

Figure and Index No.	Part No.	Description
Figure 7-2		
-1	102848-01	Ramp Stop
-2	102625-01	Receiver Pivot Support
-3	102721-01	Receiver Spring, Right-Hand
-4	611-3205	Truarc Ring
-5	613-0016	Nylon Bushing
-6	102734-01	Door Cam
-7	102669-01	Air Screen
-8	102740-01	Air Duct Gasket
-9	102624-01	Door Opener
-10	102721-02	Receiver Spring, Left-Hand
-11	102683-01	Disk Guide
-12	102753-01	Door Opener Spring

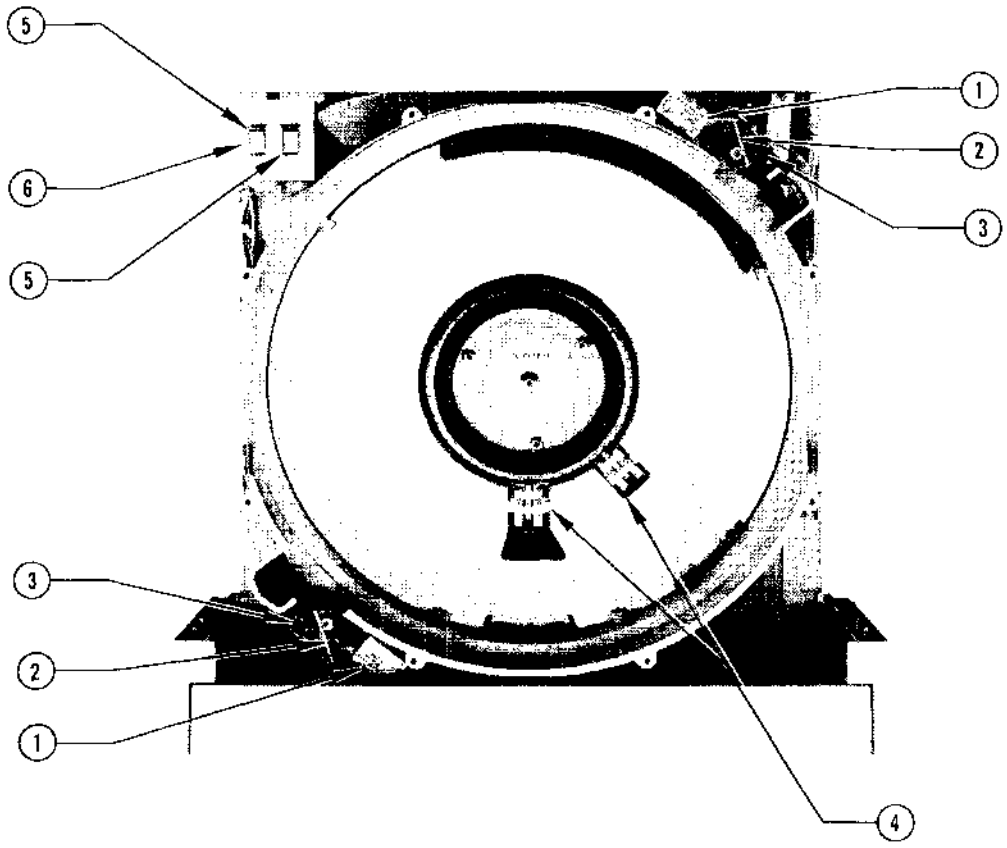


Figure 7-3. D3000 Disk Drive Photo Parts Index (Top Load Models)

Table 7-3
D3000 Disk Drive Photo Parts Index (Top Load Models)

Figure and Index No.	Part No.	Description
Figure 7-3		
-1	102754-02 517-0001	Solenoid Assembly Solenoid Only
-2	616-0016	Spring
-3	506-6360	Sub-miniature Switch
-4	102764-01 520-0002	Transducer Assembly (Dual Disk Only) Transducer Only
-5	506-0001	Rocker Switch
-6	102658-01	Name Plate

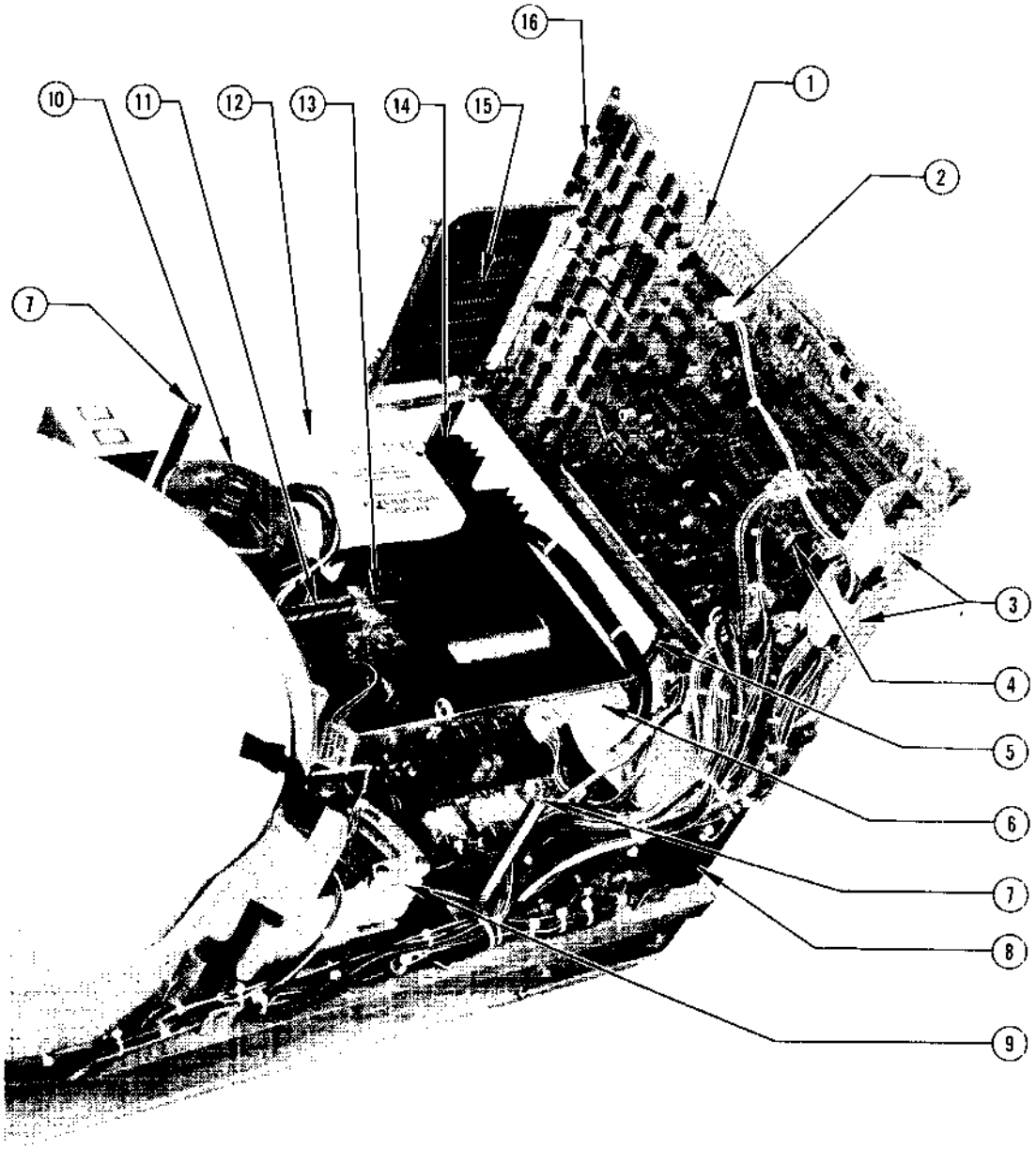
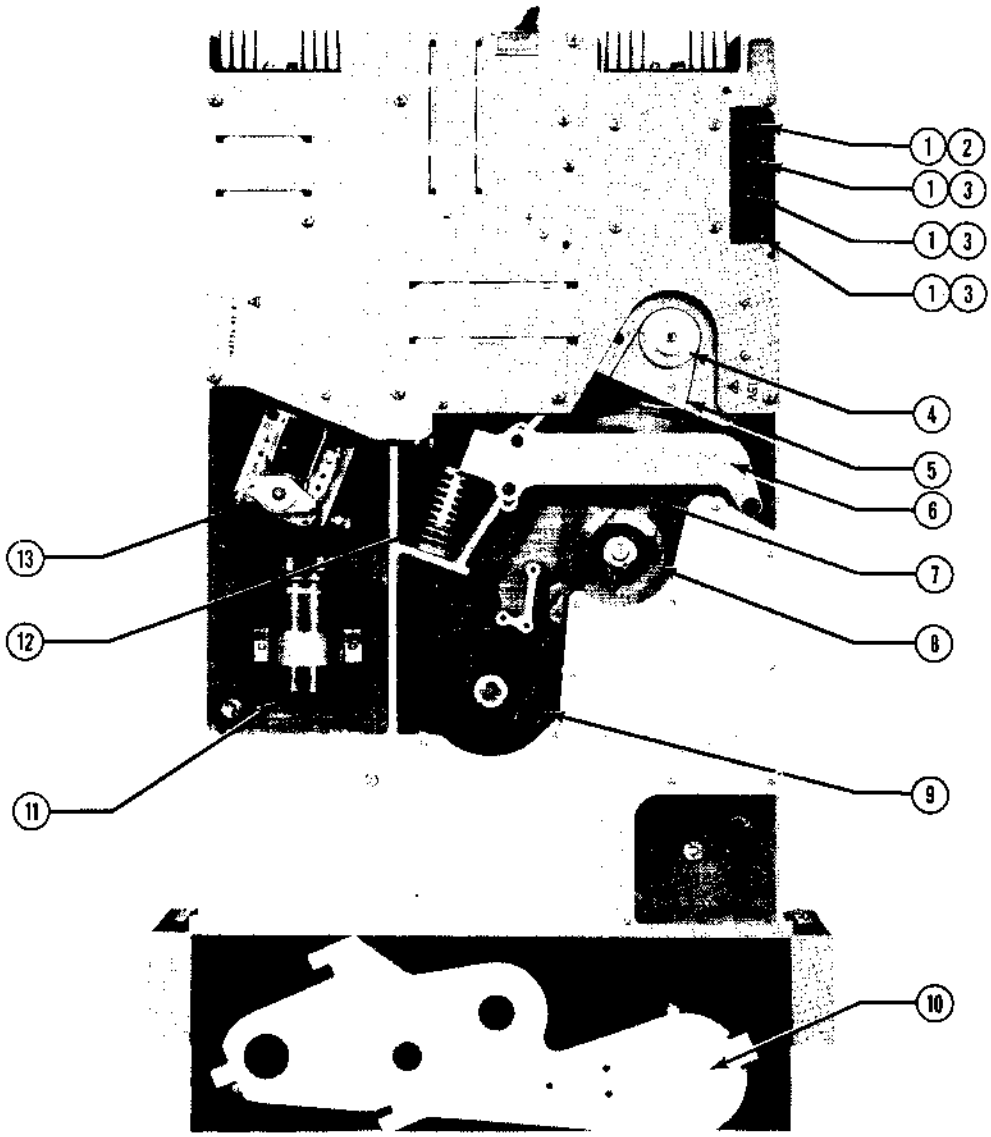


Figure 7-4. D3000 Disk Drive Photo Parts Index, PCBAs in Extended Position

Table 7-4
D3000 Disk Drive Photo Parts Index

Figure and Index No.	Part No.	Description
Figure 7-4		
-1	102611-*	Servo PCBA
-2	103461-01	Cable (Servo to Temperature Comp. PCBA)
-3	102755-01	Interboard Cable Assembly
-4	502-6113	Emergency Unload Relay
-5	102729-01	Hinged Standoff
-6	102755-03	Interboard Cable Assembly
-7	102709-01	Standoff
-8	102746-01	Heatsink Assembly (12-inch Cable)
-9	102615-01 102615-02	Brush Cleaner Assembly (Top Load, Single Disk) Brush Cleaner Assembly (Top Load, Dual Disk)
-10	103579-01	Drive Motor Assembly
-11	106291-01	Positioner Tie-down Tubing
-12	102666-01	Cover (Motor Control PCBA)
-13	102888-01 103411-01	Positioner Assembly, 100 tpi Positioner Assembly, 200 tpi
-14	102746-02	Heatsink Assembly (26-inch Cable)
-15	102801-*	Termination PCBA
-16	103705-*	Logic PCBA

*Refer to Spare Parts List for Relevant Part No.



NOTE:
BELT GUARD PLATE REMOVED
TO SHOW PULLEY AND BELT
CONFIGURATION.

Figure 7-5. D3000 Disk Drive Photo Parts Index, Bottom View

Table 7-5
D3000 Disk Memory Drive Photo Parts Index

Figure and Index No.	Part No.	Description
Figure 7-5		
-1	658-9160	Fuse Holder, Panel Mount, 3AG Miniature
-2	663-3550	Fuse, F1, 3AG, 5A, Slow Blow, 95-125v Operation
	663-3525	Fuse, F1, 3AG, 2.5A, Slow Blow, 190-250v Operation
-3	663-3100	Fuses, F2, F3, and F4; 3AG, 10A, Fast Blow
-4	102636-01	Drive Motor Pulley, 1500 rpm 60 Hz Disk Drives
	102636-02	Drive Motor Pulley, 2400 rpm 60 Hz Disk Drives, or 1500 rpm 50 Hz Disk Drives
	102636-03	Drive Motor Pulley, 2400 rpm 50 Hz Disk Drives
-5	102634-01	Belt, 60 Hz Operation
	102634-02	Belt, 50 Hz Operation
-6	102639-01	Tension Idler Plate
-7	102637-01	Tension Idler Assembly
	102609-01	Roller
	613-0012	Bearing
-8	102722-01	Blower Pulley, 1500 rpm Models
	102722-02	Blower Pulley, 2400 rpm Models
-9	102635-01	Spindle Pulley, 2400 rpm Models
	102635-02	Spindle Pulley, 1500 rpm Models
-10	102748-01	Belt Guard Plate
-11	134-4792	Capacitor, 47,000µf, -10%, +75%, 15v
-12	102667-01	Spring
-13	102671-01	Brush Motor Assembly (Top Load Only)
	519-0014	Motor (Less Cable)
	521-0004	Line Filter

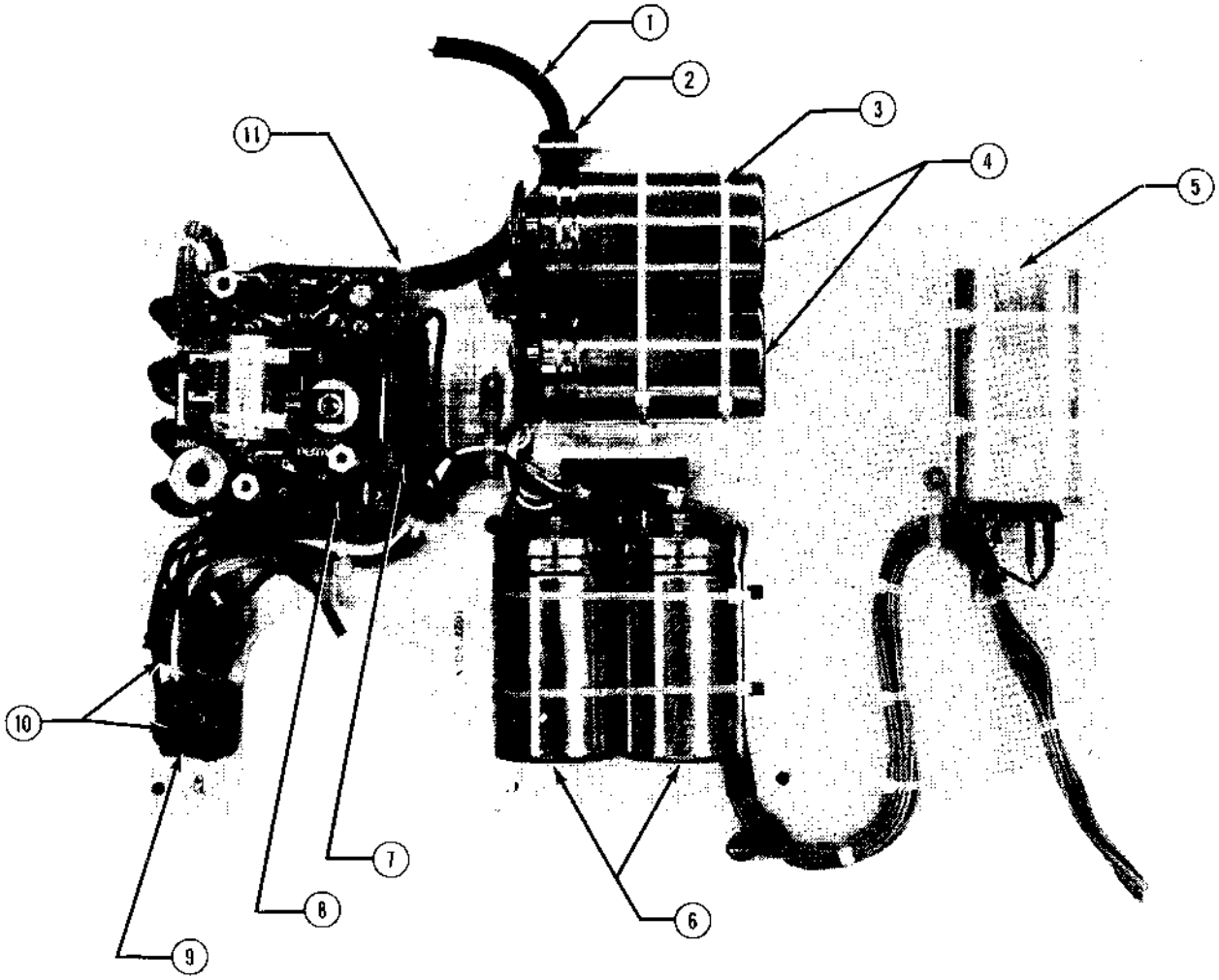


Figure 7-6. D3000 Disk Drive Photo Parts Index, Power Supply Assembly

Table 7-6
D3000 Disk Drive Photo Parts Index

Figure and Index No.	Part No.	Description
Figure 7-6		
-1	692-2717	Power Cord
-2	660-0010	Power Cord Bushing
-3	661-0013	Tie Wrap
-4	134-4792	Capacitor, 47,000 μf, —10%, +75%, 15v
-5	140-0001	Capacitor, 10 μf, ±10%, 165v
-6	134-2492	Capacitor, 24,000 μf, —10%, +75%, 25v
-7	511-3000	Power Transformer
-8	103571-*	Motor Control PCBA
-9	135-4742	Capacitor, 0.47 μf, ±20%, 50v
-10	320-9802	Rectifier Bridge, 10A, 100v
-11	661-0007	Tie Wrap, No. 10 Mount

*Refer to Spare Parts List for Relevant Part No.

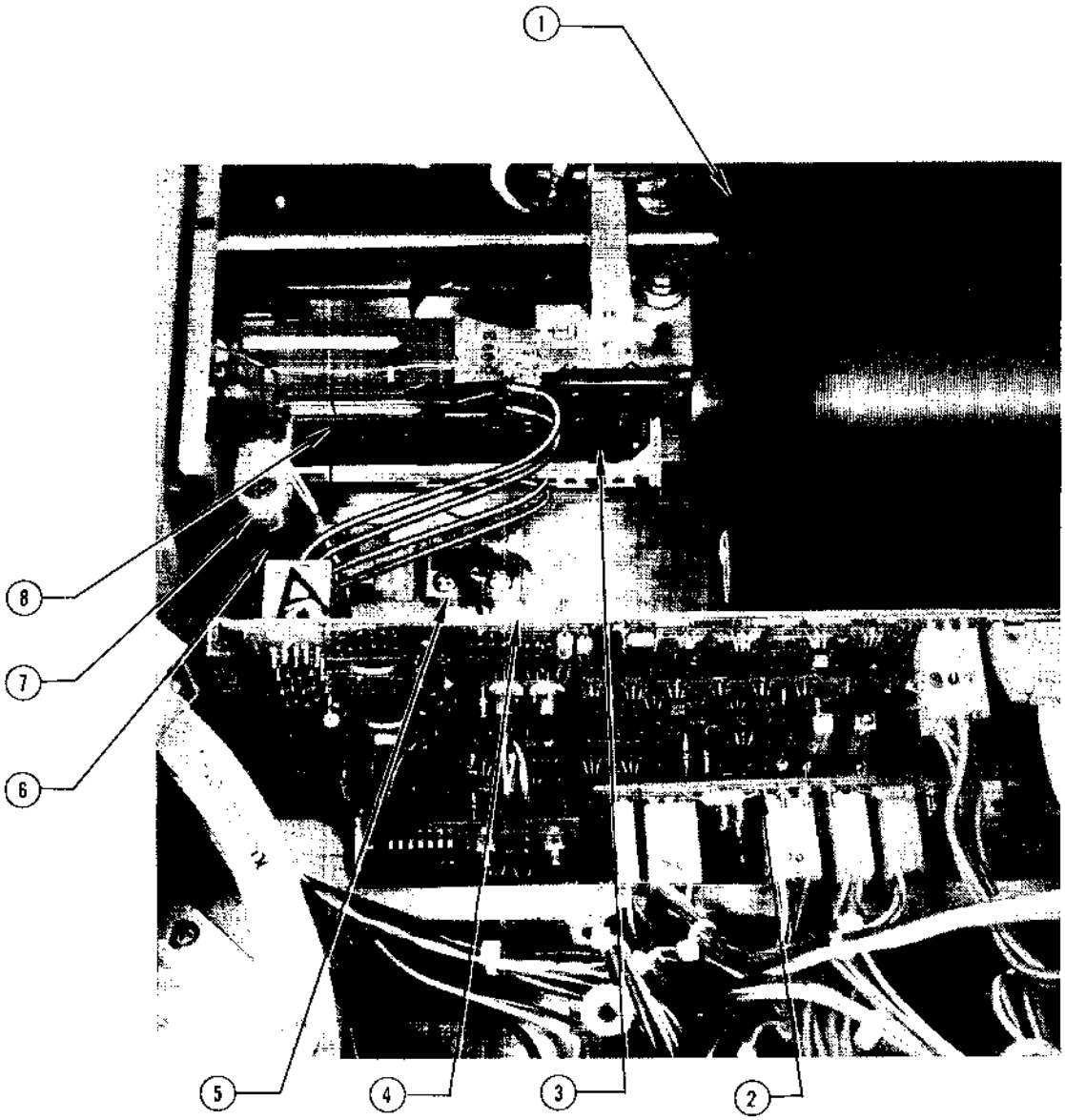


Figure 7-7. D3000 Disk Drive Photo Parts Index (200 tpi Models Only)

Table 7-7
D3000 Disk Drive Photo Parts Index

Figure and Index No.	Part No.	Description
Figure 7-7		
-1	103411	Positioner Assembly
-2	103440-* 103450-01 103456-01	Temperature Compensation Assembly Temperature Control PCBA Thermistor Mount Assembly
-3	103462	Scale Assembly
-4	103751-*	Read/Write C PCBA
-5	Ref. Only	R2 Thermistor Mount Assembly
-6	103416	Sensor Receiver Assembly
-7	103424	Lamp and Lens Assembly
-8	526-*	Read/Write Head
Refer to Spare Parts List for Relevant Part No.		

Table 7-8
D3000 Disk Drive Spare Parts List

Item	Part No.
1. Fuse	
5A, 3AG, Slow Blow, 95 — 125v Operation	663-3550
2.5A, 3AG, Slow Blow, 190 — 250v Operation	663-3525
10A, 3AG, Fast Blow	663-3100
2. Head, Read/Write, 100 tpi Models	
2200 bpi, 2400 rpm, Up*	526-0008
2200 bpi, 2400 rpm, Down*	526-0009
2200 bpi, 1500 rpm, Up*	526-0007
2200 bpi, 1500 rpm, Down*	526-0006
Head, Read/Write, 200 tpi Models	
2200 bpi, 2400 rpm, Up*	526-0016
2200 bpi, 2400 rpm, Down*	526-0017
2200 bpi, 1500 rpm, Up*	526-0014
2200 bpi, 1500 rpm, Down*	526-0015
3. Drive Belt	
60 Hz Models	102634-01
50 Hz Models	102634-02
4. Motor Pulley	
1500 rpm, 60 Hz Models	102636-01
2400 rpm, 60 Hz Models	102636-02
1500 rpm, 50 Hz Models	102636-02
2400 rpm, 50 Hz Models	102636-03
5. Drive Motor Assembly	103579-01
6. Positioner Assembly	
100 tpi Models	102888-01
200 tpi Models	103411-01
7. Logic PCBA	
100 tpi Models	103705-01
200 tpi Models	103705-02
8. Servo Board PCBA	
100 tpi Models	102811-01
200 tpi Models	102811-02
9. Read/Write C PCBA, 100 tpi Models	
2400 rpm, 2200 bpi	103751-01
1500 rpm, 2200 bpi	103751-02
Read/Write C PCBA, 200 tpi Models	
2400 rpm, 2200 bpi	103751-03
1500 rpm, 2200 bpi	103751-04
10. Temperature Compensation PCBA (200 tpi Models)	103450-01
11. System Compensation PCBA (200 tpi Models)	103445-01
12. Motor Control PCBA	
95v ac — 125v ac	103571-01
190v ac — 250v ac	103571-02
13. Motor Brush Assembly, Top Load Models	102671-01
14. Disk Cleaning Brush, Top Load Models (2 req'd for Single Platter; 4 req'd for Dual Platter)	102616-01
15. Brush Retainer (2 req'd for Single Platter, 4 req'd for Dual Platter)	102617-01

Table 7-8
D3000 Disk Drive Spare Parts List (continued)

Item	Part No.
16. Air Filter (Including Pre-Filter)	614-0006
17. Air Screen	102669-01
18. Air Duct Gasket	102740-01
19. Dust Cover	
Front Load Models	103669-01
Top Load Models	103697-01
20. Magnetic Sector Sensor Assembly	
Top Load Models	102764-01
Front Load Models	102685-01
Transducer	520-0002
Microswitch (Front Load Models)	506-9203
21. Disk Cartridge, 100 tpi Models	
2200 bpi, 8-Sector, 3M 902-8	522-0002
2200 bpi, 24-Sector, 3M 902-24	522-0004
2200 bpi, 12-Sector, 3M 902-12	522-0010
2200 bpi, Index Only, 3M 903-0	522-0012
Disk Cartridge, 200 tpi Models	
2200 bpi, 16-Sector, IBM 5440	522-0013
2200 bpi, 24-Sector, IBM 5440	522-0014
2200 bpi, Index Notch Only, IBM 5440	522-0015
2200 bpi, 8-Sector, IBM 2315	522-0019
2200 bpi, 16-Sector, IBM 2315	522-0020
2200 bpi, 24-Sector, IBM 2315	522-0021
22. Disk Platter (Without Hub)	
100 tpi, 2200 bpi, IBM 2316	522-0007
200 tpi, 2200 bpi, CDC	522-0016
23. CE Cartridge, 100 tpi Models	
Front Load, IBM 2315	522-0005
Top Load, IBM 5440	522-0011
CE Cartridge, 200 tpi Models	
IBM 5440	522-0017
IBM 2315	522-0018
24. RUN/STOP Cap	505-0002
Switch	505-0001**
25. READY Cap	509-0007
Indicator Body	509-0004**
26. SAFE Cap	509-0006
Indicator Body	509-0004**
27. PROT/PROT Cap	509-0008
Dual Lamp Indicator Body	509-0005**
28. ON/OFF Power Switch DPST	506-1806
29. Unit Select Switch Assembly	102759-01
30. Termination Board	102801-***
31. Cable (Controller to Disk Drive)	
5 ft	102836-04
10 ft	102836-03
20 ft	102836-02

Table 7-8
D3000 Disk Drive Spare Parts List (continued)

Item	Part No.
32. Cable (Daisy Chain)	
5 ft	102770-08
7 ft	102770-02
10 ft	102770-01
33. Cable (F3000 Disk Formatter to Disk Drive)	
5 ft	103224-03
10 ft	103224-02
20 ft	103224-01
34. Accent Panel	
Off-White with Logo	102647-01
Off-White without Logo	102647-02
Clear with Logo	102647-03
Clear without Logo	102647-04

*Up — Slider surface positioned to underside of disk recording area.
Down — Slider surface positioned adjacent to top of disk recording area.

**Incandescent Lamp P/N 505-0330, GE330 or Chicago Miniature CM330.

***Specify version as detailed on schematic.

Table 7-9
Part Number Cross Reference

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Composition Resistors	(Comply with MIL-R-11)	
100-1015		100 ohms ±5%, ¼w
100-1525		1.5k ohms ±5%, ¼w
101-1015		100 ohms ±5%, ½w
101-6805		68 ohms ±5%, ½w
102-0565		5.6 ohms ±5%, 1w
102-6815		680 ohms ±5%, 1w
103-1015		100 ohms ±†%, 2w
Precision Film Resistors	(Comply with MIL-R-11)	
104-1002		10k ohms, ±1%, ¼w
104-6812		68.1k ohms ±1%, ¼w
Wire Wound Resistors		
109-0002	Dale Electronics	0.2 ohms ±3%, 5w
109-0003	Dale Electronics	0.1 ohms ±3%, 5.5w
110-0011	Dale Electronics	0.1 ohms ±3%, 10w
113-0103	Dale Electronics	1.0 ohms ±3%, 1w
Variable Resistors		
121-2030	Beckman/Helipot	20k ohms ±10%, ¾w
121-5040	Beckman/Helipot	500k ohms ±10%, ¾w
123-5020	Spectrol Electronics	5k ohms, 1 turn cermat
Dipped Mica Capacitors	(Comply with MIL-C-5)	
130-1005		10 pf ±5%, 500v dc
130-4705		47 pf ±5%, 500v dc
Mylar Film Capacitors		
131-1020	Callens Industries	424B102K, 0.001 µfd ±10%, 100v dc
131-6820	Callens Industries	424B683K, 0.068 µfd ±10%, 100v dc
Solid Tantalum Polarized Capacitors		
132-2262	Components, Inc. Mallory	EG06-226-20, 22 µfd ±20%, 6v dc TIM226M006POW
Aluminum Foil Polarized Capacitors		
133-7060	Mallory	MTA70E20, 70 µfd —10 +100%, 20v dc
Aluminum Electrolytic Fixed Polarized Capacitors		
134-3000	Sprague	3,000 µfd —10 +75%, 15v dc
Ceramic Capacitors		
135-4742	Erie 'Red Cap'	8131-050651, 0.47 µfd ±2%, 50v
Transistors		
200-3053	RCA	2N3053, NPN Silicon Annular, T0-5
200-3055	Motorola	2N3055, NPN Silicon Power, T0-3
200-3251	Motorola	2N3251, PNP Silicon Annular, T0-18

Table 7-9
Part Number Cross Reference (continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* / Description
Transistors (cont'd)		
200-4037	RCA	2N4037, PNP High-Power Silicon, T0-5
200-4123	Motorola	2N4123, NPN Silicon, T0-92
200-4125	Motorola	2N4125, PNP Silicon, T0-92
200-5323	RCA	2N5323, PNP High-Power Silicon, T0-5
200-6051	Motorola	2N6051, PNP, Darlington
200-6058	Motorola	2N6058, NPN, Darlington
Rectifiers		
201-3228	RCA	2N3228, Rectifier T0-66
Field Effect Transistors		
204-3993	Motorola	2N3993, Silicon, P-Channel Junction
204-4393	Teledyne	2N4393, Silicon, N-Channel Junction
Bi-Directional Thyristor		
205-4010	GE	10A, 400v
205-6152	Motorola	10A, 400v, Bi-Directional
Diodes		
300-4002	Motorola	1N4002, 1A, 100v
300-4446	Components, Inc.	1N4446, Planer Silicon Switching Diode
Bridge Rectifier		
320-9802	Motorola	MDA980-2, 10A, 100v
Zener Diodes		
330-0685	Motorola	1N4736A, 6.8v, ±5%, 1w
330-1005	Motorola	1N4740A, 10.0v ±5%, 1w
331-0275	Motorola	1N5223B, 2.7v, ±5%, 500mw
331-0335	Motorola	1N5226B, 3.3v, ±5%, 500mw
331-0605	Motorola	1N5233B, 6.0v, ±5%, 500mw
Operational Amplifiers		
400-0715	Fairchild	U6A7715393, Wide Bandwidth (65 MHz)
400-2741	Texas Instruments	SN72741P, 8-pin, Internal Compensation
Light Emitting Diodes		
403-0001	Monsanto	MCT2, Opto-Isolator, 20% Current Transfer Ratio
Relays		
502-1243	Potter Brumfield	R10E-1 W4 V185, 12v dc, 4 PDT; Contact Rating 10A at 28v dc
Inductors		
515-2405	Delevan	Type 1537-6, 24 µh, ±5%
515-3305	Delevan	Type 1537-52, 33 µh, ±5%
515-6805	Delevan	Type 1537-68, 68 µh, ±5%
Solenoids		
517-0001	Anderson Solenoids Deltrol Controls	D16 Solenoid, Special Terminals and Plunger, 24v dc, 4.5w, continuous duty

Table 7-9
Part Number Cross Reference (continued)

PERTEC Part No.	Manufacturer	Manufacturer Part No.*/Description
Integrated Circuits		
700-0001	Texas Instruments	SN74H76N, Dual J-K Master Slave FF
700-0002	Texas Instruments	SN74H04N, Hex Inverters
700-0003	Texas Instruments	SN74H00N, Quad 2-Input Pos NAND Gate
700-0004	Texas Instruments	SN74H106N, Edge Triggered High Speed FF
700-4161	Texas Instruments	SN74161N, Synchronous 4-Bit Binary Counter
700-4164	Texas Instruments	SN74164N, 8-Bit Shift Register, Serial In, Parallel Out, Asynchronous Clear
700-5107	Texas Instruments	SN75107N, Dual Line Receiver
700-5733	Signetics	55733A, Differential Video Amplifier
700-7400	Texas Instruments	SN7400N, Quad 2-Input Pos NAND Gate
700-7402	Texas Instruments	SN7402N, Quad 2-Input Pos NOR Gate
700-7404	Texas Instruments	SN7404N, Hex Inverter
700-7405	Texas Instruments	SN7405N, Hex Inverter with Open Collector Output
700-7410	Texas Instruments	SN7410N, 3-Input Pos NAND Gate
700-7413	Texas Instruments	SN7413N, Dual NAND Schmitt Triggers
700-7416	Texas Instruments	SN7416N, Hex Inverter Buffer with Open Collector High Voltage Output
700-7419	Texas Instruments	SN74193N, 4-Bit U/D Synchronous Binary Counter
700-7430	Texas Instruments	SN7430N, 8-Input Pos NAND Gate
700-7438	Texas Instruments	SN7438N, Quad 2-Input Pos NAND Buffer, Open Col
700-7450	Texas Instruments	SN7450N, Expandable Dual 2-wide, 2-Input AND/OR Inv
700-7476	Texas Instruments	SN7476N, Dual J-K Master Slave FF
700-7483	Texas Instruments	SN7483N, 4-Bit Binary Full Adder
700-7486	Texas Instruments	SN7486N, Quad 2-Input Exclusive-OR Gate
700-7493	Texas Instruments	SN7493N, 4-Bit Binary Counter
700-7496	Texas Instruments	SN7496N, 5-Bit Shift Register
700-7545	Texas Instruments	SN75451P, Dual 2-Wide, 2-Input AND/OR Gate

*or equivalent

Table 7-10
IC Power and Ground Pin Summary

Type	Gnd	+5V	−5V	+V	−V
715	—	—	—	13	10
733	—	—	—	10	5
741	—	—	—	11	6
7400	7	14	—	—	—
7402	7	14	—	—	—
7404	7	14	—	—	—
7405	7	14	—	—	—
7410	7	14	—	—	—
7413	7	14	—	—	—
7430	7	14	—	—	—
7450	7	14	—	—	—
7476	13	5	—	—	—
7483	12	5	—	—	—
7486	7	14	—	—	—
7493	10	5	—	—	—
7496	12	5	—	—	—
74161	8	16	—	—	—
74164	7	14	—	—	—
74193	8	16	—	—	—
75107	7	14	13	—	—
75451	4	8	—	—	—

Table 7-11
Function Control Summary

Type	Clocking Transition	Clearing Level	Loading Level
7476	H to L	Low	—
74H106	H to L	Low	—
7493	H to L	High	—
7496	L to H	Low	High
74161	L to H	Low	Low (and clock)
74164	L to H	Low	—
74193	L to H	High	Low

Table 7-12
PCBA Interconnections

Logic PCBA	
J101	Interface Connector
J102	Interface Connector
J103	Interboard Connector (J305 Read/Write PCBA)
J104	Interboard Connector (J201 Servo PCBA)
J105	Interboard Connector (J202 Servo PCBA)
J106	Power Link Cable (J210 Servo PCBA)
J107	Power Link Cable (J304 Read/Write PCBA)
J108	Write Protect Switches
J109	Cartridge Switch No. 1/Cartridge Switch No. 2 (Top Load)
J110	Control Panel Switches
J111	Control Panel Lamps
J112	Upper Index (Sector) Sensor/Lower Index (Phase) Sensor
J113	Brush Mechanism Switch (Top Load)
J114	Current Cylinder Address to Temp. Comp PCBA (200 tpi)
Servo PCBA	
J201	Interboard Connector (Logic PCBA J104)
J202	Interboard Connector (Logic PCBA J105)
J203	Position and Velocity Transducer
J204	Heatsink No. 1
J205	Positioner Coil
J206	Unload Capacitor
J207	Lock Solenoids
J208	Heatsink No. 2
J209	Power Jumper
J210	Power Link Cable to Logic PCBA
J211	Power Jumper
J212	Unregulated Power from Power Supply
J213	Trigger to Motor Control PCBA
J214	Brush Motor (Top Load Only)
J215	Temperature Compensation PCBA Offset (200 tpi)
Read/Write PCBA	
J300	Head 0
J301	Head 1
J302	Head 2
J303	Head 3
J304	Power Link Cable from Logic PCBA
J305	Interboard Connector (Logic J103)
Motor Control PCBA	
J401	Trigger from Servo PCBA (Servo PCBA J213)
J402	AC Power from Power Supply Circuits
J403	Motor Capacitor (115v Operation)
J404	Motor Capacitor (220v Operation)
J405	Drive Motor (115v Operation)
J406	Drive Motor (220v Operation)
Temperature Compensation PCBA (200 tpi)	
J501	System Compensation PCBA Interconnect
J502	Logic PCBA — Power Link Cable
J503	Logic PCBA Current Address
J504	Servo PCBA Temperature Compensation Offset
J505	Thermistor Cable Assembly
J506	Test Connector

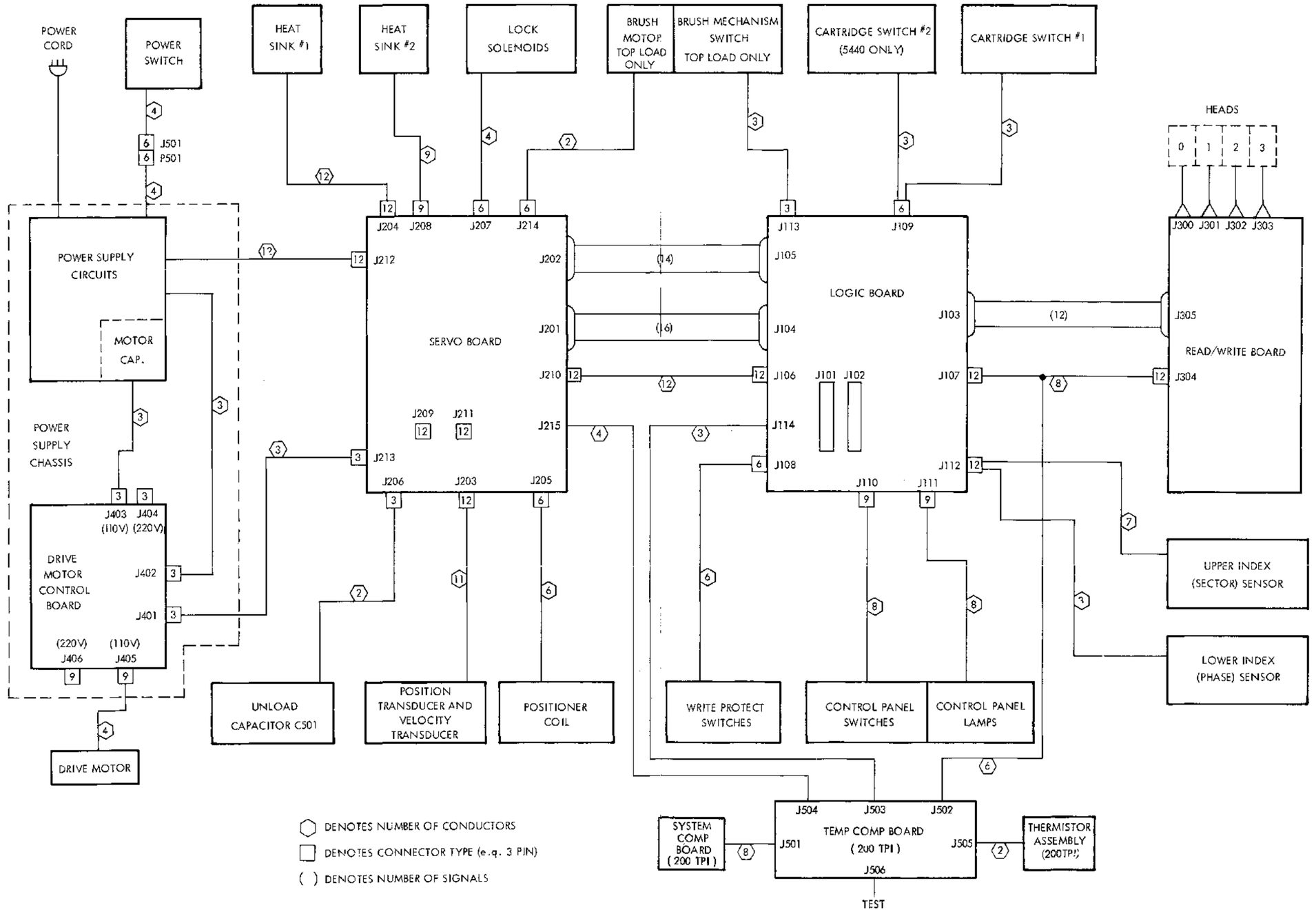
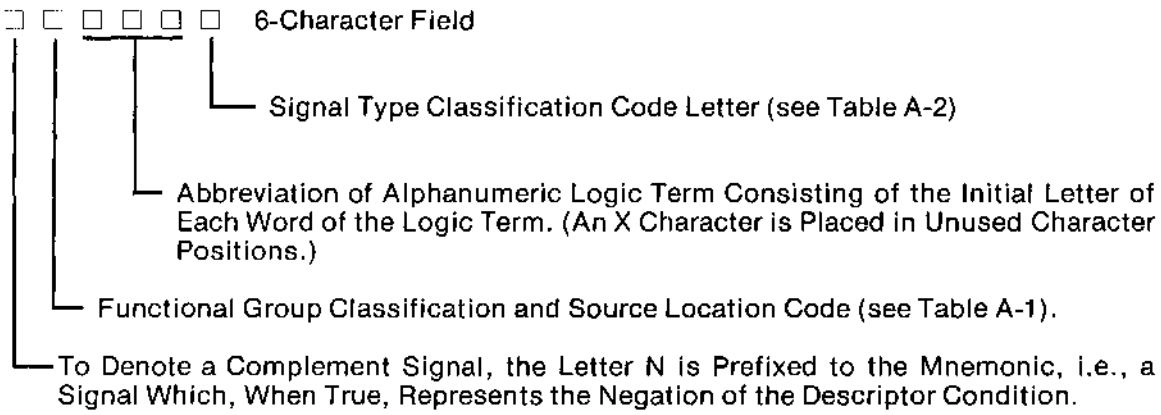


Figure 7-8. PCBA Interconnections, Block Diagram

APPENDIX A
D3000 MNEMONICS

A D3000 mnemonic term consists of a 6-character field and is defined in Figure A-1; Figure A-1 should be used in conjunction with Tables A-1 and A-2 for interpretation of the D3000 mnemonics scheme.



Note:

The mnemonic zero (0) has no slash through it; the alphabet O has a slash through it and is presented as Ø.

Figure A-1. Mnemonic Construction

Table A-1
Functional Group Classification

Symbol	Definition
I	Interface
R	Read/Write PCBA
C	Components Group (Base Assy Components)
S	Servo PCBA
L	Logic PCBA

Table A-2
Signal Type Classification

Symbol	Definition
F	Flip-Flop Output
L	Latch Flip-Flop Output*
G	Gate Output, Active Pullup or Open Collector with Pullup to +5v; Includes Transistors
S	Switch or Relay Contact Generated Signals
A	Analog Signals and Returns, Shields and Similar Signals; Buffering Levels of 1 through 9
R	Receiver, Line Receiver Input
D	Driver, Line Driver Output
T	Translator, Open Collector Gate Output without Pullup, or Pullup to Other Than +5v such as Special Logic Levels

*Used only if latch is mechanized by cross-couple gates.

Mnemonic	Logic Term Name	Mnemonic	Logic Term Name
CBPRS	Brushes Parked (Switch) Return	IRCXD	Read Clock
CBPSS	Brushes Parked Switch	IRDXD	Read Data
CCR1S	Cartridge (Switch) Return No. 1	IREXR	Read Enable
CCR2S	Cartridge (Switch) Return No. 2	IRICR	Restore Initial Cylinder
CCS1S	Cartridge Switch No. 1	IRXXD	Ready
CCS2S	Cartridge Switch No. 2	ISC0D	Sector Count Bit 0
CLMRA	Lower Magnetic (Sensor) Return	ISC1D	Sector Count Bit 1
CLMSA	Lower Magnetic Sensor Signal	ISC2D	Sector Count Bit 2
CLPOS	Lower Protect (Switch) On	ISC3D	Sector Count Bit 3
CLSRS	Lower (Protect) Switch Return	ISC4D	Sector Count Bit 4
CLSSA	Lower Sensor Shield	ISC5D	Sector Count Bit 5
CRSRS	Run/Stop (Switch) Return	ISC6D	Sector Count Bit 6
CRSSS	Run/Stop Switch	ISMXD	Sector Pulse
CSSRS	(Unit) Selector Switch Return	ISSDR	Start/Stop Disk Drive
CUESA	Upper Electronic Sensor Signal	ITØMR	Track Offset Minus
CUMSA	Upper Magnetic Sensor Signal	ITØPR	Track Offset Plug
CUPOS	Upper Protct (Switch) On	IUS1R	Unit Select No. 1
CUS1S	Unit Selector (Switch) No. 1 Position	IUS2R	Unit Select No. 2
CUS2S	Unit Selector (Switch) No. 2 Position	IUS3R	Unit Select No. 3
CUS3S	Unit Selector (Switch) No. 3 Position	IUS4R	Unit Select No. 4
CUS4S	Unit Selector (Switch) No. 4 Position	IWDSR	Write Data Signal
CUSRA	Upper Sensor Return	IWGXR	Write Enable
CUSRS	Upper (Protect) Switch Return	LAD0G	Address Difference Bit 0
CUSSA	Upper Sensor Shield	LAD1G	Address Difference Bit 1
IAEUR	Activate Emergency Unload	LAD2G	Address Difference Bit 2
IBS1D	Busy Seeking No. 1	LAD3G	Address Difference Bit 3
IBS2D	Busy Seeking No. 2	LAD4G	Address Difference Bit 4
IBS3D	Busy Seeking No. 3	LAD5G	Address Difference Bit 5
IBS4D	Busy Seeking No. 4	LAD6G	Address Difference Bit 6
ICASR	Cylinder Address Strobe	LAD7G	Address Difference Bit 7
ICD0R	Cylinder Demand (Address) Bit 0	LADEG	Address Difference Extension Bit
ICD1R	Cyliner Demand (Address) Bit 1	LAEXG	Any Emergency
ICD2R	Cylinder Demand (Address) Bit 2	LAPXG	Address Pulse
ICD3R	Cylinder Demand (Address) Bit 3	LBCEG	Brake Cycle Enable
ICD4R	Cylinder Demand (Address) Bit 4	LBCFF	Brake Cycle Enable Flip-Flop
ICD5R	Cylinder Demand (Address) Bit 5	LBMEG	Brush Motor Enable
ICD6R	Cylinder Demand (Address) Bit 6	LBPEG	Brush Parking Error
ICD7R	Cylinder Demand (Address) Bit 7	LBPSL	Brushes Parked Switch Signal
ICDER	Cylinder Demand (Address) Extension	LBSXG	Busy Signal
IDPDD	Dual Platter Drive	LBTFF	Busy Time Flip-Flop
IDTDD	Double Track Drive	LC01F	Clock No. 01
IEGXR	Erase Gate	LC02F	Clock No. 02
IFPXD	File Protected	LC03F	Clock No. 03
IHSXR	Head Select	LC04F	Clock No. 04
IICAD	Illegal Cylinder Address	LC08F	Clock No. 08
IIMXD	Index Mark	LC09F	Clock No. 09
IMDXD	Malfunction Detected	LC09G	Clock No. 09
IPSXR	Platter Select	LC10F	Clock No. 10

Mnemonic	Logic Term Name	Mnemonic	Logic Term Name
LC13F	Clock No. 13	LLØX4	Logic One (No. 4)
LC17F	Clock No. 17	LLØX5	Logic One (No. 5)
LC20F	Clock No. 20	LLØX6	Logic One (No. 6)
LCCIG	Cartridge Correctly Inserted	LLPLT	Lower Protect Lamp (Drive)
LCØUG	Clear Or Unload	LLPNG	Load + Purge Not
LDACG	Demand Address Clear	LLPXG	Load • Purge
LDAMG	Demand Address Most (Significant) Bit	LNLPG	Not Load • Purge
LDMEG	Drive Motor Enable	LNRSG	Not Run • Sequence Not
LDPSG	Dual Platter Signal	LP05A	Plus 05 Volts Power Indicator Voltage
LDRCG	Delayed Ready Condition	LP10A	Plus 10 Volts Lamp Power
LDRXG	Disk Rotating	LP5VA	Plus Five Volts Signal
LDSEG	Disk Speed Error	LPCFF	Purge Cycle Flip-Flop
LDSFG	Disk Starting Fault	LPCXG	Power Clear
LEBXF	End Busy	LPIRA	Power Indicator Return
LECEG	Erase Current Enable	LPLEG	Position Limit Error
LEØFG	Emergency Or Failure Condition	LPLFF	Phase Lock Flip-Flop
LERFF	End (of) Run Flip-Flop	LPMXG	Position Mode
LESDG	Enabled Selected Drive	LRECG	Read Enable Control
LEUCG	Emergency Unload Command	LRFFF	Run Flip-Flop
LEUEG	Emergency Unload Enable	LRLDT	Ready Lamp Driver
LEUFF	Emergency Unload Flip-Flop	LRØFF	Restore Operation Flip-Flop
LFDX1	Forward Direction	LRSM1	Reverse Slow Mode
LFPML	File Protect Mode	LRPXG	Run Switch Pulse
LFSM1	Forward Slow Mode	LRXDT	Run (Lamp) Driver
LHLEG	Head Loading Error	LRXXG	Ready
LHRXG	Heads Retracted	LSARG	Selected and Ready
LIAXG	Illegal Address	LSCFF	Sequence Control Flip-Flop
LIMS1	Increase Motor Speed	LSCRG	Speed Count Reset
LL1DA	LED No. 1 Drive	LSDMG	Start Drive Motor
LL2DA	LED No. 2 Drive	LSLDT	Safe Lamp Driver
LLAXG	Load Address	LSNHG	Sequence • Not Heads Retracted
LLCMG	Lock Cartridge Mechanism	LSØTF	Speed Out (Of) Tolerance
LLDPG	Lower Detector Pulse	LSTEG	Seek Time Error
LLDRA	LED Drive Return	LSTPF	Sequence Timing Pulse Flip-Flop
LLHFF	Load Heads Flip-Flop	LSXXG	Selected
LLMEG	Lower Multiplexer Enable	LTOMG	Track Offset Minus
LLNPG	Load • Not Purge	LTOPG	Track Offset Plus
LLØL1	Logic One Level (No. 1)	LTSCG	Transfer Speed Count
LLØL2	Logic One Level (No. 2)	LUDPG	Upper Detector Pulse
LLØL3	Logic One Level(No 3)	LUHSG	Upper Head Select
LLØL4	Logic One Level (No. 4)	LUMEG	Upper Multiplexer Enable
LLØL5	Logic One Level (No. 5)	LUPLT	Upper Protect Lamp Drive
LLØL6	Logic One Level (No. 6)	LUPSG	Upper Platter Select
LLØL7	Logic One Level (No. 7)	LVREG	Velocity Reference Enable
LLØL8	Logic One Level (No. 8)	LWDFT	Write Double Frequency
LLØL9	Logic One Level (No. 9)	LWMXG	Write Mode
LLØX1	Logic One (No. 1)	LWØEG	Write Or Erase
LLØX2	Logic One (No. 2)	RRCSG	Read Clock Signal
LLØX3	Logic One (No. 3)	RRDSG	Read Data Signal

Mnemonic	Logic Term Name
RWECG	Write Emergency Condition
S10SS	10 Volts Switched
SHRXG	Heads Retracted
SPCSA	Power Clear Signal
SPQCG	Position Quadrature Clock
SPRCG	Position Reference Clock
SPTFG	Position Transducer Failure
SPTIG	Position Transducer Index

ERRATA SHEET

Manual No. 103715
D3000 Diablo Compatible
September 1975

Make the following changes to the subject Operating and Service Manual.

1. Page 6-47, Paragraph 6.11.1, Test Configuration

   Change Step (3) to read as follows:

   Connect Channel 1 test probe to TP12 on the Logic PCBA.

2. Page 6-47, Figure 6-23, Quadrature Relationship between Sector Phase Lock Loop Square Waves

   Change Channel 1 TP11 to read Channel 1 TP12.

REVISIONS

REV	DESCRIPTION	DATE	DR	CHK	APPR
A	7411 PRODUCTION RELEASE	8/11/75	JHH	[illegible]	[illegible]

AUG 28 1975

SIGNATURES	DATE
DR J. Hollywood	8/11/75
CHK [illegible]	8/20/75
ENGR	
APPR [illegible]	8/20/75

PERTEC PERIPHERAL EQUIPMENT

TITLE
LOGIC PCBA,
INTERDATA COMPATIBLE
SPECIAL CONFIGURATION (SC030)

NEXT ASSY	USED ON	SIZE	CODE IDENT	SHT 1 OF 5	DWG NO	REV
APPLICATION		A			103726	A

PERTEC-2228

1.0 SCOPE

This special configuration drawing defines the modifications to a 103705-7 Logic PCBA required to interface a D3000 Disk Drive to controllers designed to be Inter Data compatible.

2.0 CONFIGURATION MODIFICATIONS

2.1 This unit is selected at all times. When testing this unit on the Audit Polling Test System, this unit must be the only one On Line. Due to the changes made on the Logic PCBA, this Disk Drive will not be compatible when tested in a daisy chain with other standard configuration Disk Drives.

2.2 I/O Signal Characteristic Changes:

a. Platter select inverted from the standard Diablo 30 (low level selects upper platter).

b. ISRWD is gated with READY (LRXXG) instead of Selected and Ready (LSARG).

c. IRXXD is generated from Ready (NLRXXG) instead of Selected and Ready (NLSARG).

d. IUS1R is selected at all times, the other select lines have been disabled.

e. The valid address has been extended to 204 (100 TPI) and to 408 (200 TPI).

2.3 Components Added/Deleted

a. 2 diodes (CR1, CR2) and 1 resistor (R26), deleted.

b. 1 resistor (R74), added.

3.0 LOGIC PCBA MODIFICATIONS

3.1 Make from Assembly: 103705-7

3.1.1 Trace Cuts List

a. Cut trace going to U3-2, trace is running below U3-5 (component side).

b. Cut trace between U86-10 and first feedthru (circuit side).

c. Cut trace between U71-4 and U71-13 (circuit side).

d. Cut trace at U262-9 (component side). U262 will have to be removed. Perform trace cuts at e,f,g,h, and i before replacing U262.

e. Cut trace at U262-1 (component side). (See q below).

f. Cut trace on both sides of U262-11 (component side - 2 cuts).

g. Cut trace at U262-11 (circuit side).

h. Cut trace at U262-14 (circuit side).

i. Cut trace leaving J121-15 adjacent to J121-16 (circuit side). J121-15, U205-11 and U225-14 must still be tied together. Cut must be made at a point between J121 and U203.

3.1.2 Jumper List

Add the following jumper wires, using #30 AWG Kynar Wire (691-6030). Use bare wire where convenient. Jumper wire to be added on circuit side.

a. From U3-2 to U226-4.

b. From U86-10 to U128-8.

c. From U71-3 to U71-13.

d. From U262-9 to U262-11.

e. From U262-9 to U262-8 (GND).

f. From U262-1 to U262-3.

g. From U262-14 to U263-4.

h. From U262-3 to W11-B.

i. From U262-3 to U267-9.

3.1.3 Modification Instructions (component addition and deletion)

a. Remove CR1, CR2, and R26.

b. Add R74 (Pertec P/N 100-1215, 120 OHMS, 1/4W, 5%) in the holes for CR1.

c. Jumper wire additions (using AWG #30 Kynar Wire, P/N 691-6030) on the circuit side.

1. From hole for CR2 anode to U51-3.

2. From hole of R26 that is connected to CR4 cathode to hole for CR2 cathode.

d. Modification instructions for always selecting Unit 1 is made on the cable assy. and is called out on the Top Assembly Drawing.

4.0 REFERENCE DOCUMENTS

4.1 List of Materials: 103726-7

4.2 Schematic: 103725

a. This schematic is identical to 103704, except as noted on F/D.

5.0 IDENTIFICATION

After modification of the 103705-7 PCBA, per Paragraphs 3.1.1 thru 3.1.2, mark the assembly with Part No. 103726 including version number and issue letter. Delete or mark out all 103705-7 markings.

6.0 NOTES

6.1 Test and adjust per Specification 103716.

6.2 Refer to 2.0 Configuration Modification.

(7) VERSION TABLE

103726	Make from 103705
-01	-01
-02	-02
-03	-03
-04	-04
-05	-05
-06	-06
-07	-07
-08	-08
-09	-09

PERTEC PERIPHERAL EQUIPMENT

DWG. NO. 103726

SIZE A

SHEET 5 OF