

# PANEL MONITOR

## XCON-8

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## INTRODUCTION

This Manual describes the functions and operations of the Heath H8 Panel Monitor Program, XCON-8, which resides permanently in a ROM on the H8 CPU board. XCON-8 provides a sophisticated front panel display and keyboard emulation as well as handling master clear and interrupt operations. Some of the major features of XCON-8 are:

- Memory contents display and alteration.
- Register contents display and alteration.
- Program execution control (both breakpoint and single instruction operation).
- Self-contained bootstraps for program loading and dumping.
- Port input and output routines.

In addition to the above features, XCON-8 can be instructed (by means of a flag byte contained in the H8 RAM) to bypass some or all of its normal functions so the sophisticated user can augment or totally replace them.

Communication with the Panel Monitor is accomplished through three devices: the keypad, the 7-segment displays, and the audio alert. The user enters commands and values through the 16-key keypad, and XCON-8 responds visually through the front panel displays. In addition to the front panel displays, XCON-8 provides the keypad entry and function feedback to the built-in speaker. Appropriate signals (short, medium, and long beeps) indicate that commands and data are accepted or rejected.

## THEORY OF OPERATION

This section will supplement the information contained in the "Operation" and "Circuit Description" sections of your H8 Operation Manual. In order to fully understand how XCON-8 operates, you must be familiar with the H8 front panel and CPU. A thorough knowledge of the 8080 instruction set and its architecture is also essential.

### Power Up and Master Clear

XCON-8 initializes the H8 whenever you power-up or master clear (RST). You initiate the power-up operation by turning on the rear panel Power switch. You can master clear by simultaneously depressing both the lower right-hand (RST/Ø) and lower left-hand (Ø) keys of the H8 front panel keypad. Both power-up and RST cause a level zero (highest priority) interrupt and result in a long beep from the audio alert.

During initialization, XCON-8 enters a routine which determines the high limit of continuous RAM. Once the high limit of available RAM is determined, the H8 stack pointer (SP) is set to this value. XCON-8 then determines if the RAM starts at Ø, and copies itself from ROM into that RAM space. Control is passed to the front panel command loop. Using this feature, you can immediately determine the total amount of continuous memory above 8K by displaying the stack pointer value.

### Clock Interrupts

The Clock Interrupt is a crucial element in the operation of the H8 front panel system. This level one interrupt is generated by the front panel hardware every 2,000  $\mu$ S. XCON-8 uses this interrupt to check for some keyboard commands, to check for user program breakpoints, and to refresh the front panel displays.

XCON-8 performs these functions using a series of subroutines which are executed as necessary when indicated by the interrupts. For this reason, all user programs must maintain a valid stack (at high memory) containing at least 80 free bytes at all times. If this stack space is not available and XCON-8 is running (it can be disabled; see the Advanced Control Section), unpredictable software damage can occur in your program. In the same manner, if your program should execute a DI (Disable Interrupt) instruction, no front panel services including the RTM (Return To Monitor) function are available until an EI (Enable Interrupt) instruction is executed or until a master clear (RST/Ø) is performed.

## XCON-8 Modes /Using RST and RTM

XCON-8 is always in either the monitor mode or the user mode. In the monitor mode no user program is executing, XCON-8 loops reading the keypad and refreshing the displays. All commands entered via the keypad are valid; however, the RTM command is meaningless.

When your program is being executed, XCON-8 is in the user mode and the MON LED on the front panel is extinguished. Only two keyboard commands are valid in this mode: RST (master clear) and RTM (Return To Monitor). NOTE: Both of these commands are dual key commands. No single key command is recognized, so a user program may have free use of the entire keypad.

You can return XCON-8 to the monitor mode by using the RTM command (simultaneously press the Ø and the # keys). This command stops program execution at the end of the current instruction, stores the current value of each register, and returns XCON-8 to the monitor mode. You can then continue your program by pressing the GO key. The RST command (simultaneously press the Ø and the / keys) performs the master clear operation described earlier and does not save any register values.

Normally, when a user program is running, XCON-8 is also running. Thus, if XCON-8 is displaying the contents of the HL register pair and the user program is started, it continues to display the contents of this register pair as the program is run. If the user program changes the contents of the HL pair, the change is immediately reflected in the front panel displays. In a similar manner, if a memory location is displayed when a user program is started, it is displayed during the time the user program is run. If the user program changes the contents of the display memory location, the front panel display changes.

Since XCON-8 does not recognize keypad commands in the user mode, the RTM command must be used before the memory location or register being displayed is changed to a new location or a different register. Once you select the new location or different register, you can resume program execution by pressing GO.

NOTE: XCON-8 requires about 10% of the H8 CPU's resources to process the display interrupts. Programs which are compute-bound may be slowed down by simultaneous operation of XCON-8. In this situation, you may wish to turn off the clock interrupts to improve execution time. See "Using Interrupts" on Page 1-24.

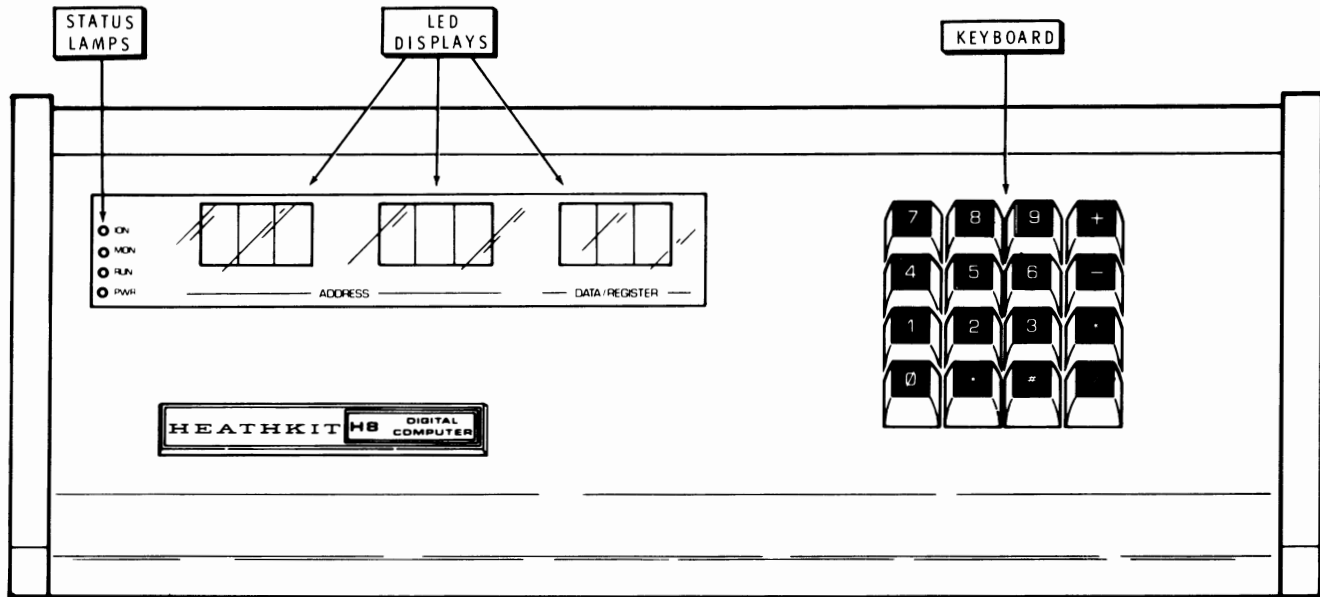


Figure 1-1

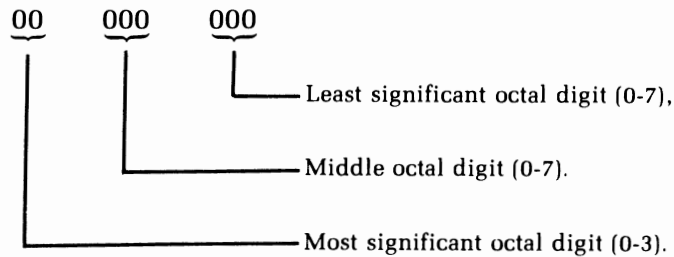
## H8 Displays

You must understand the H8 front panel presentation in order to use XCON-8. The display is made up of 9 digits, in three groups of three digits each. See Figure 1-1. Each group of three digits displays one byte (eight bits) of information. This information may be the contents of a designated register or memory location, or it may be the address of a memory location itself. The register names are also displayed.

All binary numbers are converted to octal format for display on the H8 front panel. The following table shows binary to octal conversion.

<u>BINARY NUMBER</u>	<u>OCTAL NUMBER</u>
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Each byte is displayed as two-and-one-half octal digits. The octal numbers lie in the range of 000 to 377 for binary numbers in the range 00000000 to 11111111, as shown below.



NOTE: As there are only eight bits in a byte, the most significant octal digit only represents two bits and is therefore displayed as 0 to 3. If the user should inadvertently enter the octal digits 4 to 7 into the most significant digit, the most significant bit is lost. Losing this bit converts 4 through 7 into the digits 0 through 3 respectively.

Also note that 16-bit numbers, such as memory addresses and certain register contents, are still displayed as two eight-bit numbers. Therefore, the H8 front panel representation of the number is made up of **two** groups of three octal numbers in the range of 000 to 377. This representation of 16-bit binary numbers is known as **offset octal**, and is used consistently throughout all H8 displays of 16-bit numbers. Offset octal must not be confused with octal. For example:

$\overbrace{11111} \overbrace{1111} \overbrace{1111} \quad \overbrace{11111} \overbrace{1111} \overbrace{1111}$	A 16-bit binary number
$\begin{array}{c}   \\ 3 \end{array} \quad \begin{array}{c}   \\ 7 \end{array} \quad \begin{array}{c}   \\ 7 \end{array} \quad \begin{array}{c}   \\ 3 \end{array} \quad \begin{array}{c}   \\ 7 \end{array} \quad \begin{array}{c}   \\ 7 \end{array}$	Offset octal representation (377 377)

$\overbrace{1111} \overbrace{1111} \overbrace{1111} \overbrace{1111} \overbrace{1111}$	A 16-bit binary number
$\begin{array}{c}   \\ 1 \end{array} \quad \begin{array}{c}   \\ 7 \end{array} \quad \begin{array}{c}   \\ 7 \end{array} \quad \begin{array}{c}   \\ 7 \end{array} \quad \begin{array}{c}   \\ 7 \end{array} \quad \begin{array}{c}   \\ 7 \end{array}$	True Octal representation (177777)

The lower example shows true octal representation of a 16-bit binary number. This is **not** used by the H8 front panel displays or any H8 software. Occasionally you will see offset octal numbers printed with a decimal point separating the upper and lower bytes. For example:

377.377

Hi Byte      Lo Byte



## H8 Keypad

The H8 Keypad consists of 16 keys, as shown in Figure 1-1 on Page 1-7. When the keypad is operating under the control of XCON-8, it exhibits a number of unique properties.

- Each keystroke is verified by a short beep from the audio alert.
- Octal digits are entered using the keys 0 through 7.
- Holding a key down continuously repeats the key's function.
- The + key increments memory port or register locations.
- The – key decrements memory port or register locations.
- The \* key cancels previous keypad entries.
- The ALTER key causes XCON-8 to enter the alter mode.
- The MEM key causes XCON-8 to enter the display memory mode.
- The REG key causes XCON-8 to enter the register mode.

Many of the keys on the keypad have multiple functions, depending on the XCON-8 mode being used. In the register mode, for example, the numeric keys (1-6) call the register indicated in the upper left-hand corner of the key. When the XCON-8 is in neither the register nor the memory mode, the keys perform the functions indicated in the lower right-hand corner of the key.

The # and / keys have additional special functions, as indicated earlier. When the / key is pressed simultaneously with the Ø key, the RST (master clear) sequence is initiated. When the # sign key is pressed simultaneously with the Ø key, the RTM (Return To Monitor) function is initiated, the user program is stopped, and XCON-8 regains control.

Each key is covered in greater detail as the various function are discussed.

## DISPLAYING AND ALTERING MEMORY LOCATIONS

One of the major features of XCON-8 is its ability to examine the contents of any H8 memory location and to modify the contents of that memory location if it is RAM.

When the H8 is first powered up, XCON-8 is in the display memory mode. This mode is indicated by all digits displaying octal numbers and no decimal points being on.

### Specifying a Memory Address

If you wish to display or alter the contents of a memory location, you must first place XCON-8 in the memory address mode and then enter the desired memory address. Place XCON-8 in the memory address mode (if not already there) by pressing the MEM (Memory) key. Specify the address to be displayed or altered by entering the 6-digit address (offset octal).

When you press the MEM key, all the decimal points will light. This indicates that the address may now be entered. Once the full 6-digit address is entered, the decimal points turn off, indicating that address entry is completed. After all 6 digits are entered, the address is displayed in the left-most six displays, and the contents of the addressed memory location are displayed in the right-hand 3 digits.

**NOTE:** As you press each key, including the MEM key, a short beep indicates successful entry. As each group of three octal digits is successfully entered, a medium beep is sounded. The sequence by which you specify a memory address is shown in Figure 1-2.

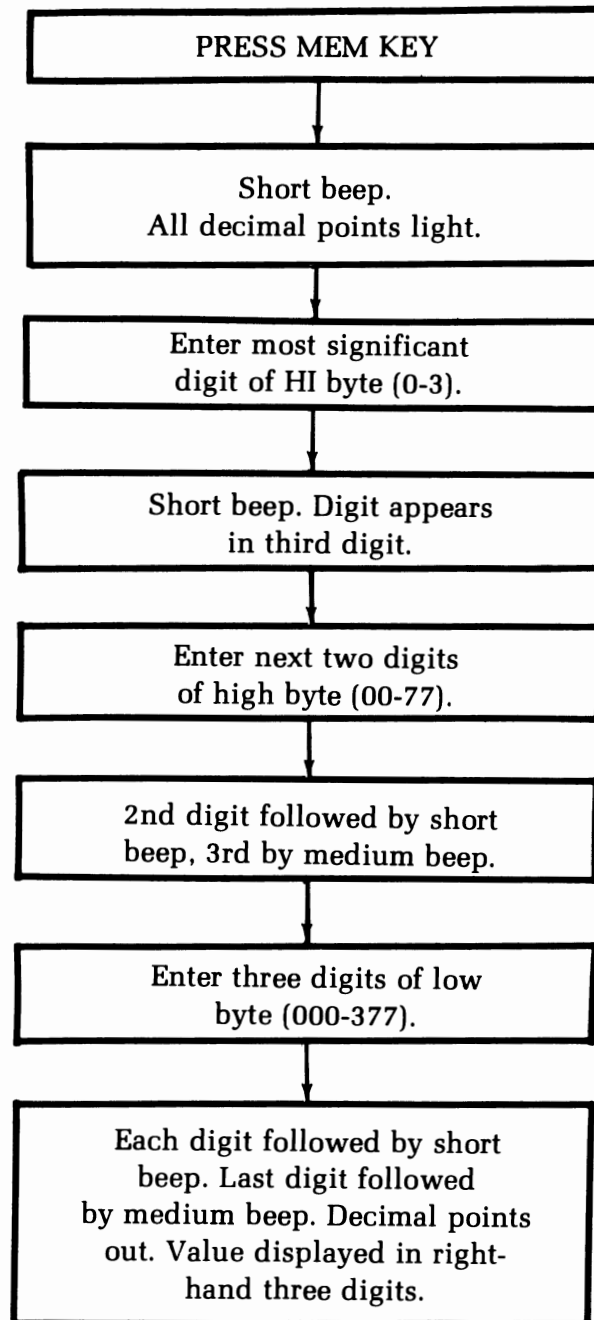


Figure 1-2

Entering a memory address through XCON-8.

NOTE: If you press a non-octal digit key as one of the six address digits, an error is flagged (a long beep). Once this error is flagged, the XCON-8 considers the address complete and extinguishes the decimal points. The entire sequence must be repeated.

## Altering a Memory Location

Before you can alter a memory location, you must first display the contents of the memory location by specifying the memory address as described in the preceding paragraphs. After you specify the memory address, press the ALTER key. This will cause XCON-8 to enter the memory alter mode.

When XCON-8 enters the memory alter mode, a single decimal point rotates from right to left through all 9 digits. You can now alter the contents of the displayed location by entering the new octal value (three digits on the keypad). When the three digits have been entered, acoustical verification (a short beep) is given **and the memory address is incremented**. You can then alter this new location by entering three more digits or pressing one of the following keys, causing the monitor to perform the indicated function:

<u>KEY</u>	<u>FUNCTION</u>
+	Increment the address.
-	Decrement the address.
MEM	Specify a new memory address (leave the memory alter mode).
REG	Specify a register for display (leave the memory alter mode).
ALTER	Exit from the alter mode (into the display mode).

NOTE: XCON-8 automatically increments the memory address as each entry (3 octal digits) is complete. Therefore, you may load a program in sequential locations very rapidly. Each location is modified by simply entering the three octal digits.

The following example reviews each step as the H8 is turned on; the memory address mode is entered; and the location 040 123 is addressed, altered to 345, checked, and closed.

<u>DISPLAY</u>			<u>COMMENTS</u>
X X X	X X X	X X X	Random memory display at power up (X=random number.)
X.X.X.	X.X.X.	X.X.X.	MEM key pressed. (In memory address mode, a short beep.)
X.X.0.	X.X.X.	X.X.X.	0 key pressed. (Short beep.)
X.0.4.	X.X.X.	X.X.X.	4 key pressed. (Short beep.)
0.4.0.	X.X.X.	X.X.X.	0 key pressed. (Medium beep.) Contents of location 040 XXX displayed.)
0.4.0.	X.X.1.	X.X.X.	1 key pressed. (Short beep. Contents of 040 XX1 displayed.)
0.4.0.	X.1.2.	X.X.X.	2 key pressed. (Short beep. Contents of 040 X12 displayed.)
0 4 0	1 2 3	X X X	3 key pressed. (Medium beep. Contents of desired location 040 123 displayed, decimal points out.)
0.4.0	1.2.3	X.X.X	ALTER key pressed. (Short beep. Decimal points <b>rotate.</b> )
0.4.0.	1.2.3.	X.X.3.	3 key pressed. (Short beep. Decimal points <b>rotate.</b> )
0.4.0.	1.2.3.	X.3.4.	4 key pressed. (Short beep. Decimal points <b>rotate.</b> )
0.4.0.	1.2.4.	X.X.X.	5 key pressed. (Medium beep. Address increments one location. Decimal points <b>rotate.</b> )
0.4.0	1.2.3	3.4.5	- key pressed. (Short beep. Address decrements one location. Decimal points <b>rotate.</b> )
0 4 0	1 2 3	3 4 5	ALTER key pressed. (Short beep. Decimal points go out.)

## Stepping Through Memory

When XCON-8 is either in the display memory or alter memory modes, the + and - keys increment and decrement the memory address. Each time you press the key, XCON-8 increments (or decrements) the memory address one location. If you hold the key down, the auto-repeat function of XCON-8 causes the memory address to increment or decrement repeatedly (approximately one location every second).

## DISPLAYING AND ALTERING REGISTERS

XCON-8 can display and alter the contents of the 8080 CPU registers, just as it displays and alters the contents of H8 memory locations. Although the process is quite similar, a few special features should be noted.

### Specifying a Register for Display

Press the REG key to specify that a register is to be displayed. After you press the REG key, press a second key (SP through PC, see the Table below) to specify the desired register or register pair.

When the REG key is pressed, six decimal points light, indicating that you must now select a register. NOTE: Simply pressing the REG key causes a register name to appear in the right-hand digits. However, you must select a register using the Register Select key before a register is definitely selected and its true contents are displayed. Once a register is selected, the decimal points are extinguished.

The contents of the selected register pair are displayed in the six left-most displays. The register name (or names) are displayed in the two right-most digits of the right-hand three displays. The registers are selected and displayed in accordance with the following table:

<u>KEY</u>	<u>LEFT 3 DIGITS</u>	<u>MIDDLE 3 DIGITS</u>	<u>RIGHT PAIR</u>	<u>COMMENTS</u>
SP (1)	000 to 377	000 to 377	SP	Stack pointer
AF (2)	000 to 377	000 to 377	AF	AF Register pair
BC (3)	000 to 377	000 to 377	BC	BC Register pair
DE (4)	000 to 377	000 to 377	DE	DE Register pair
HL (5)	000 to 377	000 to 377	HL	HL Register pair
PC (6)	000 to 377	000 to 377	PC	Program counter

NOTE: The contents of any single eight-bit register may lie in the range of 000 to 377 octal. The stack pointer (SP) and the program counter (PC) are 16-bit registers and are displayed as two sets of three octal numbers. Each 3-digit grouping corresponds to one byte (8 bit number). When a register pair is displayed, the left three digits correspond to the left register and the middle three digits correspond to the right register. For example:

256 312 AF

Register A contains 256 and register F contains 312.

## Altering the Contents of a Selected Register

To alter the contents of a register (or register pair), you must first specify it as described in the preceding paragraphs. After you select the register or register pair, press the ALTER key. This will cause the six left-hand decimal points to rotate right to left, indicating that you may enter 6 digits to alter the contents of the indicated register or register pair.

Alternately, you may press one of the following command keys.

<u>KEY</u>	<u>FUNCTION</u>
+	Changes the register pair being displayed.
-	Changes the register pair being displayed.
MEM	Specify a new memory address (leave the alter register mode).
REG	Specify a new register for display (leave the alter register mode).
ALTER	Exit the register alter mode.

**NOTE:** Stack pointer register (SP) is not a direct display of the real stack pointer register, but simply a copy of the real stack pointer register and is used for display purposes only. The stack pointer cannot be altered from the front panel. To alter the stack pointer register, an SPHL (SPHL = 371) instruction must be written into memory. The desired new stack pointer value is then placed in the HL register pair. XCON-8 single instruction mode is used to execute the SPHL swap instructions, loading the stack pointer with the contents loaded in the HL register pair.

## Stepping Through the Registers

Use + and - keys to change the register pair being displayed. For example, if the DE register pair is being displayed, pressing the + key causes the next sequential register pair to be displayed (the HL pair). In the same manner, pressing the - key causes the register to decrement to the preceding pair. For example, if the DE pair is being displayed, pressing the - key displays the BC register pair. **NOTE:** Holding down either the + key or the - key causes the display to continuously increment or decrement through all the six registers/register pairs.

## PROGRAM EXECUTION CONTROL

XCON-8 supports three basic program execution control facilities:

- Beginning or starting execution.
- Breakpointing.
- Single instruction.

Each of these execution controls permits the programmer to execute the desired portions of a program and examine its effects. He may execute the entire program, or a small group of instructions, or a single program instruction.

### Initiating Program Execution

To begin the execution of a program residing in H8 memory, place the address of the first instruction to be executed in the PC (program counter). Use the methods described in “Displaying and Altering Registers” (Page 1-14). Once the address of this first instruction is placed in the program counter, press the GO key and program execution will begin. NOTE: Unless the program disables the front panel, the display continues to be actively updated, although the front panel commands are no longer active (except for RST and RTM). If the program counter is displayed when you press the GO key, XCON-8 continuously monitors the program counter.

### Breakpointing

Breakpointing permits the programmer to execute small portions of a program and then return to XCON-8. Breakpointing is especially useful when a program is being “debugged.” Small portions of the program may be executed and their results observed. If there is an error, it may be corrected before an entire program is involved.

When the H8 executes a program and encounters a halt instruction, it re-enters XCON-8 and sounds the alarm. All of the registers are preserved and the program counter points to the address **following** the address of the halt instruction. Thus, you can breakpoint a program from the front panel by inserting halt instructions (HLT = 166) at the desired points throughout the program. When a particular



section of the program is tested and the breakpoint feature is no longer required, you can change the halt to a “no operation” (NOP = 000). Once the halts are changed to NOPs, execution of the NOP simply passes control to the next successive instruction. Program execution for breakpointing uses the GO key as previously described.

NOTE: If you temporarily replace an existing instruction with a halt, you must restore the instruction before resuming program execution. The contents of the program counter point to the address **following** the halt. Therefore, if the instruction which replaced the halt is to be executed, when the program continues, the contents of the program counter must be decremented one location before execution is resumed.

## Single Instruction Operation

Any user program may be operated in the single instruction mode. This procedure is identical to the GO command, except that the SI key is pressed rather than the GO key. When the SI key is pressed, a single **instruction** (not a single machine cycle) is executed and then control is returned to XCON-8. Single instruction operation is available for careful inspection of program results and for executing special programs, such as swapping the HL register pair with the stack pointer as discussed in “Altering the Contents of a Selected Register” (Page 1-15).

## Interrupting a Program During Execution

You can interrupt a running program (with all registers preserved at the point of interruption) by pressing RTM & Ø. You can then examine and/or alter the contents of various memory locations and all the registers as required. Resume execution of the program at the next sequential instruction by simply pressing the GO key. NOTE: Although all registers and memory locations are preserved when RTM & Ø are pressed, it is very difficult to stop a program at an exact location. Therefore, use the breakpoint feature if you want to stop the program at an exact location.

## LOAD/DUMP ROUTINES

XCON-8 contains a routine that lets you load and dump memory contents from or to a tape. This feature is especially important, as most computers require one of two successive “boot strap” routines to be hand-loaded before a desired program can be loaded into the main memory. All these “boot strap” routines are contained within the XCON-8 ROM, and use sophisticated error checking techniques. Thus, a program can be loaded or dumped by simply pressing a single key.

### Loading From Tape

To load from a tape, ready the reader device with the tape to be loaded prior to executing the load command. Place XCON-8 in the display memory mode and press the LOAD key. Once the LOAD key is pressed, XCON-8 starts the tape transport and scans the tape for the first file record.

No change will be seen on the front panel displays until XCON-8 finds the first file. When the first file record is located, XCON-8 checks it to see if it is the first (or only) record in a sequence, and the record is a memory dump record. If it is not a memory dump record, a number two error is flagged (see “Tape Errors” on Page 1-20).

Once a correct record is found, loading proceeds. The loading procedure places the entry point address of the program being loaded in the H8 program counter. The H8 memory is then loaded. The displays continuously show the address being loaded and the data being loaded at these addresses. When the load is complete, XCON-8 sounds a long beep and displays the final memory address. If the load is faulty, a number one error is displayed and the audio alarm continuously beeps. (See “Tape Errors,” Page 1-20.)

NOTE: You may abort a partial load by using the CANCEL key. Naturally, the load image resulting from this action is incorrect, and should not be executed.

### Dumping to Tape

Before dumping a memory image onto tape, the following three dump parameters are required:

- The entry point address (the program starting address).
- The dump starting address.
- The dump ending address.

Set the desired entry point address by placing this value in the program counter (PC). This value will be placed in the program counter whenever you load the program so execution will begin at this address when you press the GO key.

Place the dump starting address into the first two H8 RAM cells. These are: 040 000 (offset octal) and 040 001 (offset octal). NOTE: The low order byte of the address should be placed into location 040 000 and the high order byte of the starting address should be placed into location 040 001.

Enter the dump ending address as a memory address using the # (MEM) key. Then ready the tape transport and press the DUMP key. As the tape dump takes place, the number of bytes left to be dumped and the contents of the memory location being dumped are displayed on the front panel. You can abort a dump by using the CANCEL key. If the CANCEL key is used, an incomplete dump image is left on the tape. This cannot be loaded at a future date. NOTE: A successful load automatically sets up the following three dump parameters:

- A. The program starting locations are stored in locations 040 000 and 040 001.
- B. The program ending location is displayed.
- C. The program counter contains the program entry point.

Figure 1-3A shows the steps of a typical dump sequence and Figure 1-3B shows the steps of a typical load sequence.

1. Set PC to 040 100; (040 100 = entry address).
2. Set 040 000 to 100 (100 = low byte of dump start).
3. Set 040 001 to 040 (040 = high byte of dump start).
4. Enter memory address 052 340 (052 340 = end address of dump).
5. Be sure tape is ready.
6. Press DUMP.

Figure 1-3A  
The H8 memory image dump.

1. Be sure tape is ready.
2. Press LOAD.

Figure 1-3B  
The H8 memory image load.

## Copying a Tape

The beginning and final address of the load image are placed at the appropriate points. Thus, to copy a tape, simply load the tape as described in “Loading From Tape” (Page 1-18). Then ready the dump tape drive and press the DUMP key. A dump then takes place, including entry point, initial address, and final address.

In a similar manner, to load, alter, and then dump, enter only the ending address. The other parameters are unchanged from the load if locations 040 000, 040 001 or the program counter have not been modified during the altering procedure.

## Tape Errors

XCON-8 detects two types of tape errors: record errors and checksum errors. In either case, when an error is detected, the tape transport is halted. The error number is then displayed in the center three digits (001 for a checksum error, 002 for a record error) and the alarm is repeatedly sounded. To halt the alarm and return to the command mode, press the CANCEL key.

### RECORD ERRORS

The following are typical causes of record errors.

- Attempting to load a file which is not a memory image. For example, loading an editor text file or a BASIC program file.
- Attempting to start a load in the middle of a load image. Therefore missing the initialization information at the start of the file.
- A tape error which causes a portion of the load image to be missed so the next record read is not in the proper sequence.

### CHECKSUM ERRORS

A checksum error is flagged when the CRC (Cyclical Redundancy Check) checksum following a record does not match the CRC calculated by PAM-8. This error means that the record is either incorrectly recorded or the load is faulty. In either case, the load should be attempted again. If successive loads result in repeated failures, the original tape must be suspected as faulty.

## I/O FACILITIES

XCON-8 supports two commands that allow you to perform input and output functions on H8 I/O ports. These front panel instructions permit simple manipulation of the H8 I/O ports without your having to write extensive routines to perform these functions.

### Inputting From a Port

To input from a port, press the # key. Then enter three zero digits and the three-digit address (octal) of the desired port. NOTE: The front panel should now display 000 AAA, where AAA is the port address and 000 is meaningless. Press the IN key to read the port, the value is displayed in the three left-most digits of the front panel display.

### Outputting to a Port

To output to a specified port, press the # key. Then enter the value to be supplied to the port in the three left-most displays. The port address is entered into the middle three displays. The display is of the form VVV AAA, where V stands for value, and A for address. Pressing the OUT key causes the value to be outputted to the indicated port.

### Addressing Port Pairs

Frequently, ports are assigned in pairs, where one of the two port addresses is the control and status register and the other port is the data port. Address port pairs by using the + and - key to change ports. Once the initial port has been defined, the + key increments the port address to a new higher numbered port, and the - key is used to decrement to a lower numbered port.

## ADVANCED CONTROL

One of the advanced features of XCON-8 is its provisions allowing sophisticated users to augment or replace XCON-8's functions. Augmenting or replacing XCON-8 functions is usually done in conjunction with assembly language programs. Sometimes it is possible to implement these features by using the POKE and PEEK commands in BASIC.

### 16-Bit Tick Counter (TICCNT)

XCON-8 maintains a 16-bit (2 byte) tick counter known as TICCNT. The value of this counter is incremented each time a clock interrupt is processed. As an interrupt occurs once every 2 mS, the counter is incremented once every 2 mS. As long as clock interrupts are not disabled, this value can be used by any program to compute elapsed time. The tick counter may be set to any desired value, but it should not be frequently reset, as this interferes with the front panel refresh cycle. The contents of the tick counter are contained in memory locations 040 033 (the least significant byte) and 040 034 (the most significant byte).

### Using the Keypad

When your program is running, XCON-8 does not recognize any single key command. Thus, all single key patterns are available for your program. To read keypad patterns, you can use one of two routines. First, you may take an input from port IP. PAD; or second, your program may use XCON-8 RCK (read Console Keypad) routine. The input port IP. PAD is permanently assigned to port location 360. Inputting a binary number from this port detects which of the 16 keys are depressed.

The RCK routine provides keypad decoding, keypad debounce routines, auto-repeat routines, and acoustical feedback.

NOTE: If you use two key combinations, each key must reside in a separate bank. The first bank includes keys 0-7 and the second bank includes keys 8-#. RCK cannot decode two key combinations.

## Display Usage

When a user program is running, XCON-8 normally displays the contents of the selected register or memory location. However, you may disable this process and display any arbitrary segment pattern, or completely disable the display to provide greater computational through-put. The display usage is primarily controlled by setting various bits in the .MFLAG memory cell. This memory cell is found at location 040 010.

### MANUAL UPDATING

By setting the UO.DDU bit in the .MFLAG memory location, you can instruct XCON-8 to continue refreshing the front panel displays and to disable updating. When this is done, XCON-8 continues to refresh the LED's from a 9-byte block of RAM cells found at locations 040 013 through 040 023. When the UO.DDU bit is set in .MFLAG, the contents of these bytes are not altered in any manner by XCON-8.

You can use this technique to display numbers, letters, or arbitrary bar patterns on the front panel displays. For instance, your program may alter the display by inserting any value into FPLEDS. The front panel LED segments will display a decimal integer if you use the octal to 7-segment pattern (DODA) display.

### MANUAL DISPLAY REFRESHING

By setting the UO.NFR (User Option.No Front Panel Refresh) bit in the .MFLAG memory cell, you can instruct XCON-8 to stop refreshing the front panel displays. Setting the UO.NFR bit does not disable the clock interrupts; therefore, the tick counter (TICCNT) is still incremented. But XCON-8 does not refresh the displays from the information contained in the FPLEDS bytes.

**NOTE:** If you desire, you may write a program to refresh the front panel LED displays. Usually this is done using the clock interrupts. If you undertake an independent front panel refresh program, take extreme care to avoid burning the displays due to excessive refreshing. **The total power dissipated in the LEDs is determined by the refresh cycle, and too frequent refreshing will result in excessive display heating.**

## Using Interrupts

All H8 interrupts cause control to be transferred into the low 64 bytes of memory. XCON-8 occupies this memory space so all interrupts are first processed by XCON-8. Except for level zero interrupts, which are used as master clears, you can supply an interrupt processing routine for each of the seven additional interrupts. The following sections explain the use of each of these interrupts.

### I/O INTERRUPTS

Interrupts numbered 3 through 7 are I/O interrupts. XCON-8 does not process these interrupts in any way. When a level 3 through level 7 interrupt is received, XCON-8 immediately transfers to the user interrupt vectors contained in memory locations 040 037 through 040 064. Each location must contain a jump instruction pointing to the appropriate program location which processes these interrupts.

NOTE: If any of these interrupts occur, you must supply a processing routine for them. This routine must be complete including both entry and exit processing. When you use H8 interrupts, you must use only the available vector which is 6 to insure compatibility with future H8 products. You may also use 2 if you will not be using BUG-8.

### CLOCK INTERRUPTS

The level one interrupts are generated by the front panel hardware every 2 mS. XCON-8 normally processes these interrupts. However, by setting a processing vector in UIVEC and setting the UO.INT bit in the .MFLAG cell, XCON-8 enters the users routine each time a clock interrupt is generated.

### SINGLE INSTRUCTION AND BREAKPOINT INTERRUPTS

Level two interrupts are generated by the single instruction hardware contained on the CPU card. When a single instruction is requested, the result of the interrupt is processed by XCON-8. If the single instruction interrupt was generated by XCON-8 in response to a Monitor Mode Single Instruction register condition, XCON-8 processes it. Otherwise, XCON-8 jumps to the user level two interrupt vector (UIVEC). Since the level two interrupt does not affect XCON-8, a level two restart instruction can be used as a breakpoint instruction by the user programs.

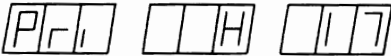



## FLOPPY BOOT



XCON-8 contains the code necessary to boot-up an operating system from a floppy disk. Two forms of "Boot" let you select the device (H17 or H47) and drive number (0-2 or 0-3). "Boot Primary" refers to the device that you will use most often. "Boot Secondary" provides you with a convenient way to boot from your alternate device, if you have one.

### BOOT PRIMARY

The primary boot device is selected by switch SW1 sections 4, 1, and 0 on the extended configuration board. This switch is preset for H17 primary device. You may change the switch sections to select H47 primary device.

<u>DISPLAY</u>	<u>ACTION</u>	<u>COMMENTS</u>
	Press "1"	Boot H17 primary
or		
	Press "1"	Boot H47 primary

### BOOT SECONDARY

	Press "2"	Boot H17 secondary
or		
	Press "2"	Boot H47 secondary

You may use the "CANCEL" key to abort the boot command and return to the monitor.

## AUTO BOOT

If Switch SW1 section 7 is set to 1, the floppy disk will boot from the primary device automatically at power-up and master clear.

NOTE: We do not recommend auto-booting with a diskette in the drive and the door closed at power-up. Damage could occur to the diskette if you attempt to do so. Rather, power-up the H8 and H17 (H47), insert the diskette, and close the door within 15 seconds. Rebooting with Auto-Boot is the prime reason for its implementation. Software may accomplish this by executing an RST Ø.

## BOOT FROM DRIVE OTHER THAN DRIVE Ø

Primary and secondary Boot are both designed to access drive Ø on either the H17 or the H47. However, if you have not selected Auto Boot, you may boot from H47 drive 1 or 2 or H17 drive 1, 2, or 3 by following this procedure:

1. Use XCON-8 "Altering the Contents of a Selected Register" procedures to set register A to the drive number that you want to boot from.
2. If you are booting from a primary alternate drive, simply press "GO."
3. If you are booting from a secondary alternate drive, set register PC to 007 367 (the secondary drive address) and press "GO."

NOTE: Register PC is already set for the primary drive address (007 364) at power-up and master clear.

## ERRORS

The front panel will display    if any of the following conditions occur:

1. The boot device does not respond within 15 seconds.
2. Switch SW1 is set to an undefined setting.
3. A disk error occurs.

NOTE: The "boot Err" message will only remain on the display a few seconds. XCON-8 will then return to the panel monitor mode.

## SWITCH SW1

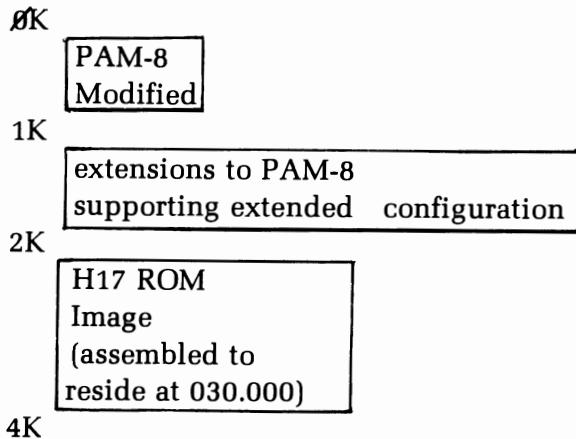
The sections of SW1 (on the HA8-8 Extended Configuration Board) have been defined as follows:

SWITCH SECTION	DESCRIPTION
<u>7 6 5 4 3 2 1 0</u>	_____
X X X X X X 0 0	Port 174/177 = H17
X X X X X X 0 1	Port 174/177 = H47
X X X X 0 0 X X	Port 170/173 = unused
X X X X 0 1 X X	Port 170/173 = H47
X X X 0 X X X X	Boot primary from port 174/177
X X X 1 X X X X	Boot primary from port 170/173
0 X X X X X X X	Normal
1 X X X X X X X	Auto-Boot

Note that switches 5 and 6 are reserved.

## MEMORY MAP

The lower 4K of memory is used as follows:



```

4 *** PAM/8 - H8 FRONT PANEL MONITOR.
5 *
6 * J. G. LEIMIN, 05/01/76.
7 *
8 * FOR *MINTEK* INC.
9 *
10 * COPYRIGHT 05/1976, MINTEK CORPORATION,
11 * 902 N. 9TH ST.
12 * LAFAYETTE, IND.
13 *
14 * Modified: 25 Aug 79. JMitlsler.
15 * PAM860 added single button boot from H17
16 * PAM8AT JMitlsler.
17 * added automatic power on boot from H17
18 * PAM860 JMitlsler.
19 * changed default display to PC
20 * KAM860 JMitlsler.
21 * added RAM at zero capability
22 * Ram860 G. Chandler /Ram860.2/
23 * Issue: 01.02.00
24 * H17 Boot
25 * H47 Boot
26 * Auto-Boot
27 * Primary/Secondary Support
28 * Modified RAM at Zero (No double move)
29 * Remove 030.000 default PC to avoid confusion
30 *

```

```

32 *** PAM/8 - H8 FRONT PANEL MONITOR.
33 *
34 * THIS PROGRAM RESIDES (IN ROM) IN THE LOW 1024 BYTES OF THE HEATH
35 * H8 COMPUTER. IT ACTUALLY CONSISTS OF TWO VIRTUALLY INDEPENDANT
36 * ROUTINES: A TASK-TIME PROGRAM WHICH PROVIDES SOPHISTICATED
37 * FRONT PANEL MONITOR SERVICE, AND AN INTERRUPT-TIME PROGRAM WHICH
38 * PROVIDES BOTH A REAL-TIME CLOCK AND EMULATES AN EFFECTIVE
39 * HARDWARE FRONT PANEL.

```

```

41 *** INTERRUPTS.
42 *
43 * PAM/8 IS THE PRIMARY PROCESSOR FOR ALL INTERRUPTS.
44 * THEY ARE PROCESSED AS FOLLOWS:
45 *
46 * RST USE
47 *
48 * 0 MASTER CLEAR. (NEVER USED FOR I/O OR RST)
49 *
50 * 1 CLOCK INTERRUPT. NORMALLY TAKEN BY PAM/8,
51 * SETTING BIT #00-CLK# IN BYTE #MFLAG# ALLOWS
52 * USER PROCESSING (VIA A JUMP THROUGH #UIVEC#).
53 * UPON ENTRY OF THE USER ROUTINE, THE STACK
54 * CONTAINS:

```

```

55 * (STACK+0) = RETURN ADDRESS (TO PAM/8)
56 * (STACK+2) = (STACKPTR+I4)
57 * (STACK+4) = (AF)
58 * (STACK+6) = (BC)
59 * (STACK+8) = (DE)
60 * (STACK+10) = (HL)
61 * (STACK+12) = (PC)
62 * THE USER'S ROUTINE SHOULD RETURN TO PAM/8 VIA
63 * A *RET* WITHOUT ENABLING INTERRUPTS.
64 *
65 *
66 * 2. SINGLE STEP. SINGLE STEP INTERRUPTS GENERATED
67 * BY PAM/8 ARE PROCESSED BY PAM/8.
68 * ANY SINGLE STEP INTERRUPT RECEIVED WHEN IN
69 * USER MODE CAUSES A JUMP THROUGH *UIVEC**3.
70 * STACK UPON USER ROUTINE ENTRY:
71 * (STACK+0) = (STACKPTR+I2)
72 * (STACK+2) = (AF)
73 * (STACK+4) = (BC)
74 * (STACK+6) = (DE)
75 * (STACK+8) = (HL)
76 * (STACK+10) = (PC)
77 * THE USER'S ROUTINE SHOULD HANDLE IT'S OWN RETURN
78 * FROM THE INTERRUPT.
79 *
80 * THE FOLLOWING INTERRUPTS ARE VECTORED DIRECTLY THROUGH *UIVEC*.
81 * THE USER ROUTINE MUST HAVE SETUP A JUMP IN *UIVEC* BEFORE ANY
82 * OF THESE INTERRUPTS MAY OCCUR.
83 *
84 * 3 I/O 3. CAUSES A DIRECT JUMP THROUGH *UIVEC**6
85 *
86 * 4 I/O 4. CAUSES A DIRECT JUMP THROUGH *UIVEC**9
87 *
88 * 5 I/O 5. CAUSES A DIRECT JUMP THROUGH *UIVEC**12
89 *
90 * 6 I/O 6. CAUSES A DIRECT JUMP THROUGH *UIVEC**15
91 *
92 * 7 I/O 7. CAUSES A DIRECT JUMP THROUGH *UIVEC**18
    
```

95 \*\* ASSEMBLY CONSTANTS

97 \*\* IO PORTS

```

000.360 IP.PAD EQU 3600 PAU INPUT PORT
000.360 OP.CTL EQU 3600 CONTROL OUTPUT PORT
000.360 OP.DIG EQU 3600 DIGIT SELECT OUTPUT PORT
000.361 OP.SEG EQU 3610 SEGMENT SELECT OUTPUT PORT
000.371 IP.TPC EQU 3710 TAPE CONTROL IN
000.371 OP.TPC EQU 3710 TAPE CONTROL OUT
000.370 IP.TPD EQU 3700 TAPE DATA IN
000.370 OP.TPD EQU 3700 TAPE DATA OUT
000.362 IP.COM EQU 3620 Configure Port /Ram8Go 2/
000.362 OP.CTL2 EQU 3620 Secondary Control Port /Ram8Go 2/
    
```

110 \*\* ASCII CHARACTERS.

```

111 A.SYN EQU 0260 SYNC CHARACTER
112 A.STX EQU 0020 STX CHARACTER
    
```

115 \*\* FRONT PANEL HARDWARE CONTROL BITS.

```

116 C8.SSI EQU 00010000B SINGLE STEP INTERRUPT
117 C8.MTL EQU 00100000B MONITOR LIGHT
118 C8.CLI EQU 01000000B CLOCK INTERRUPT ENABLE
119 C8.SPK EQU 10000000B SPEAKER ENABLE
    
```

122 \*\* Secondary Control Bytes

```

123 C82.SSI EQU 00000001B Single-Step Enable /Ram8Go 2/
124 C82.CLI EQU 00000100B Clock Interrupt Enable
125 C82.DKG EQU 00100000B UKG-0 Enable
126 C82.SID EQU 01000000B Side-1 Select
    
```

129 \*\* DISPLAY MODE FLAGS (IN \*DSPMOD\*)

```

130 DM.MR EQU 0 MEMORY READ
131 DM.MW EQU 1 MEMORY WRITE
132 DM.RR EQU 2 REGISTER READ
133 DM.RW EQU 3 REGISTER WRITE
    
```

```

136 ** Configuration Flags /Ram8Go 2/
137
000.003 CN.174M EQU 00000011B Port 1740 Device-Type Mask
000.014 CN.170M EQU 00001100B Port 1700 Device-Type Mask
000.020 CN.PRI EQU 00010000B Primary/Secondary: 1 -> Primary == 1700
000.040 CN.MEM EQU 00100000B Memory Test/Normal
000.100 CN.8AU EQU 01000000B Baud Rate: 0 -> 9600; 1 -> 19200
000.200 CN.A80 EQU 10000000B Auto-Boot: 1 -> Auto-Boot

000.000 M-17 Disk Valid only in CN.174M
000.000 No Disk Installed Valid only in CN.170M
000.001 H-47
    
```

```

149 ** Boot Constants (HI7 Rom Dependant) /Ram8Go 2/
150
041.061 A10.UNI EQU 41061A Boot Device Unit Number
037.132 800TA EQU 37132A Disk Constants ROM Source
000.130 800TAL EQU 1300 Disk Constants Length
000.012 ERPTCNT EQU 10 Soft Error Retry Count
036.073 R.SDP EQU 36073A Common ROM Code
034.031 RORCLK EQU 34031A HI7 Clock Vector
    
```

```

158 ** Segment Definitions /Ram8Go 2/
159
000.001 S0 EQU 00000001B
000.002 S1 EQU 00000010B
000.004 S2 EQU 00000100B
000.010 S3 EQU 00001000B
000.020 S4 EQU 00010000B
000.040 S5 EQU 00100000B
000.100 S6 EQU 01000000B
000.200 S7 EQU 10000000B
    
```

```

169 ** Key Definitions /Ram8Go 2/
170
000.257 K.PLUS EQU 10101111B +
000.217 K.MINU EQU 10001111B -
000.157 K.STAR EQU 01101111B *
000.117 K.DIVD EQU 01001111B /
000.057 K.NUM8 EQU 00101111B #
000.017 K.DOT EQU 00001111B .
000.000 XTEXT TAPE TAPE DEFINITIONS
    
```

```

179X ** TAPE EQUIVALENCES.
180X
181X RT.MI EQU 1 RECORD TYPE - MEMORY DUMP IMAGE
182X RT.BP EQU 2 RECORD TYPE - BASIC PROGRAM
183X RT.CT EQU 3 RECORD TYPE - COMPRESSED TEXT
184X RT.NB EQU 4 RECORD TYPE - NEW BASIC PROG.
185X RT.BD EQU 5 RECORD TYPE - BASIC DATA
186X RT.PD EQU 6 RECORD TYPE - BASIC PROG. AND DATA
187X
188X ** BLOCK SIZE FOR INTER-PRODUCT COMMUNICATION.
189X
190X BLKSIZ EQU 512
191X
192X ** IO PORT VALUES.
193X
194X TD.IN EQU 3700 TAPE DATA IN
195X TD.OUT EQU 3700 TAPE DATA OUT
196X TS.IN EQU 3710 TAPE STATUS IN
197X TS.OUT EQU 3710 TAPE STATUS OUT
198X
199 ** MACHINE INSTRUCTIONS.
200
201 MI.HLT EQU 011101108 HALT
202 MI.RET EQU 110010018 RETURN
203 MI.IN EQU 110110118 INPUT
204 MI.JMP EQU 110000118 Jump
205 MI.OUT EQU 110100118 OUTPUT
206 MI.LDA EQU 001110108 LDA
207 MI.ANI EQU 111001108 ANI
208 MI.LXID EQU 000100018 LXI D
209
210 ** USER OPTION BITS.
211 *
212 * THESE BITS ARE SET IN CELL .MFLAG.
213
214 UO.HLT EQU 100000008 DISABLE HALT PROCESSING
215 UO.NFR EQU CB.CLI NO REFRESH OF FRONT PANEL
216 UO.DDU EQU 000000108 DISABLE DISPLAY UPDATE
217 UO.CLK EQU 000000018 ALLOW PRIVATE INTERRUPT PROCESSING
218
219 XTEXT HOSEQU

```

/Ram8Go 2/



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```

221X **      HDOS SYSTEM EQUIVALENCES.
222X *
223X
024.000      S.GRT0 EQU      24000A      SYSTEM AREA FOR  GRT0
025.000      S.GRT1 EQU      25000A      SYSTEM AREA FOR  GRT1
026.000      S.GRT2 EQU      26000A      SYSTEM AREA FOR  GRT2
227X
030.000      ROMBOOT EQU     30000A      ROM BOOT ENTRY
229X
230X      ORG      40100A      FREE SPACE FROM PAM-8
231X
232X      DS      8          JUMP TO SYSTEM EXIT
233X      DS      16         DISK CONSTANTS
234X      EQU     *          SYSTEM DISK ENTRY POINT
235X      DS      24*3       SYSTEM ROM ENTRY VECTORS
040.240      D.RAM DS      31         SYSTEM ROM WORK AREA
040.277      S.VAL DS      36         SYSTEM VALUES
040.343      S.INT DS      115        SYSTEM INTERNAL WORK AREAS
239X      DS      16         STACK OVERFLOW WARNING
240X      S.SOVR DS      2          SYSTEM STACK
041.146      DS      4200A-*     STACK SIZE
041.150      D2X  STACKL EQU     *    LMA+1 SYSTEM STACK
001.032      EQU     *          USER FWA
042.200      EQU     *          EDRAH
245X      USERFMA EQU     *
246      XTEXT EDRAH
    
```

```

248X **      EDRAH - DISK RAM WORKAREA DEFINITION.
249X *
250X *      ZEROED UPON BOOTING UP.
251X *
252X *      HOSEQU MUST BE CHANGED WHEN THIS DECK IS CHANGED.
253X
254X      ORG      0.0RAM
255X
256X
040.240      D.TT DS      1          TARGET TRACK (CURRENT OPERATION)
040.241      D.TS DS      1          TARGET SECTOR (CURRENT OPERATION)
259X
260X      D.DVCTL DS      1          DEVICE CONTROL BYTE
261X
262X      D.DLYM0 DS      1          MOTOR ON DELAY COUNT
040.244      D.DLYH0 DS      1          HEAD SETTLE DELAY COUNTER
264X
265X      D.TRAPT DS      2          ADDRESS IN 0.DRYTB FOR TRACK NUMBER
040.245      D.VOLPT DS      2          ADDRESS IN 0.DRYTB FOR VOLUME NUMBER
267X
268X      D.DRYTB DS      2*4        TRACK NUMBER AND VOLUME NUMBER FOR 4 DRIVES
269X
270X      D.HECNT DS      1          HARD ERROR COUNT
040.261      D.SEGNT DS      2          SOFT ERROR COUNT
040.262      D.OEGNT DS      1          OPERATION ERROR COUNT
273X
    
```

GLOBAL DISK ERROR COUNTERS

```

274X * GLOBAL DISK ERROR COUNTERS
275X
040.265 276X D.ERR DS 0 BEGINNING OF ERROR BLOCK
040.265 277X D.E.MDS DS 1 MISSING DATA SYNC
040.266 278X D.E.HSY DS 1 MISSING HEADER SYNC
040.267 279X D.E.CHK DS 1 DATA CHECKSUM
040.270 280X D.E.HCK DS 1 HEADER CHECKSUM
040.271 281X D.E.VOL DS 1 WRONG VOLUME NUMBER
040.272 282X D.E.TRK DS 1 BAD TRACK SEEK
040.273 283X D.ERRL DS 0 LIMIT OF ERROR COUNTERS
284X
285X * I/O OPERATION COUNTS
286X
040.273 287X D.OPR DS 2
040.275 288X D.OPM DS 2
289X
000.037 290X D.RAML EQU *-D.RAM
040.277 291 XTEXT EDVEC
    
```

JMP VECTORS FOR ROM CODE

```

293X ** JMP VECTORS FOR ROM CODE
294X *
295X * SEE DISK ROM FOR ADDRESSES
296X *
297X * HOSEQ MUST BE ALTERED WHEN THIS TABLE IS ALTERED.
298X
040.130 299X ORG D.VEC
300X
040.130 301X D.SYDD DS 3 JMP R.SYDD (MUST BE FIRST)
040.133 302X D.MOUNT DS 3 JMP R.MOUNT
040.136 303X D.XOK DS 3 JMP R.XOK
040.141 304X D.ABORT DS 3 JMP R.ABORT
040.144 305X D.XIT DS 3 JMP R.XIT
040.147 306X D.READ DS 3 JMP R.READ
040.152 307X D.READR DS 3 JMP R.READR
040.155 308X D.WRITE DS 3 JMP R.WRITE
040.160 309X D.CDE DS 3 JMP R.CDE
040.163 310X D.DTS DS 3 JMP R.DTS
040.166 311X D.SDT DS 3 JMP R.SDT
040.171 312X D.MAI DS 3 JMP R.MAI
040.174 313X D.MAD DS 3 JMP R.MAD
040.177 314X D.LPS DS 3 JMP R.LPS
040.202 315X D.RDB DS 3 JMP R.RDB
040.205 316X D.SDP DS 3 JMP R.SDP
040.210 317X D.STS DS 3 JMP R.STS
040.213 318X D.STZ DS 3 JMP R.STZ
040.216 319X D.UJLY DS 3 JMP R.UJLY
040.221 320X D.MSC DS 3 JMP R.MSC
040.224 321X D.MSP DS 3 JMP R.MSP
040.227 322X D.WNB DS 3 JMP R.WNB
040.232 323X D.ERRT DS 3 JMP R.ERRT
040.235 324X D.DLY DS 3 JMP R.DLY
040.240 325 XTEXT H17DEF
    
```

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```

327X ** H17 CONTROL INFORMATION.
328X
000.177 329X DP.DC EQU 07FH DISK CONTROL PORT
000.001 330X DF.HD EQU 00000001B HOLE DETECT
000.002 331X DF.T0 EQU 00000010B TRACK 0 DETECT
000.004 332X DF.T1 EQU 00000100B WRITE PROTECT
000.010 333X DF.MP EQU 00000100B SYNC DETECT
000.010 334X DF.SD EQU 00001000B
000.001 335X
000.001 336X DF.WG EQU 00000001B WRITE GATE ENABLE
000.002 337X DF.DS0 EQU 00000010B DRIVE SELECT 0
000.004 338X DF.DS1 EQU 00000100B DRIVE SELECT 1
000.010 339X DF.DS2 EQU 00001000B DRIVE SELECT 2
000.020 340X DF.M0 EQU 00100000B MOTOR ON (BOTH DRIVES)
000.040 341X DF.OI EQU 00100000B DIRECTION (0=OUT)
000.100 342X DF.ST EQU 01000000B STEP COMMAND (ACTIVE HIGH)
000.200 343X DF.WR EQU 10000000B WRITE ENABLE RAM
344X
345X
346X
347X ** DISK UART PORTS AND CONTROL FLAGS.
348X
000.174 349X UP.DP EQU 07CH DATA PORT
000.175 350X UP.FC EQU 07DH FILL CHARACTER
000.176 351X UP.ST EQU 07DH STATUS FLAGS
000.176 352X UP.SC EQU 07EH SYN CHARACTER (OUTPUT)
000.176 353X UP.SR EQU 07EH SYNC RESET (INPUT)
354X
000.001 355X UF.RDA EQU 00000001B RECEIVE DATA AVAILABLE
000.002 356X UF.ROR EQU 00000010B RECEIVER OVERRUN
000.004 357X UF.RPE EQU 00000100B RECEIVER PARITY ERROR
000.100 358X UF.FCT EQU 01000000B FILL CHAR TRANSMITTED
000.200 359X UF.TBM EQU 10000000B TRANSMITTER BUFFER EMPTY
360X
361X
362X
363X ** CHARACTER DEFINITIONS.
364X
000.375 365X C.DSYN EQU 0FDH PREFIX SYNC CHARACTER
040.240 366 XTEXT M47DEF
368X ** M470DEF - M47 Constant Definitions
369X *

```

371X \* 2-80 INSTRUCTIONS

372X EQU 101000108\*256+111011010 INI INSTRUCTION  
 373X M.INI EQU 101000118\*256+111011010 OUTI INSTRUCTION  
 242.355  
 243.355

376X \*\* DISK INTERFACE CONSTANTS

377X \*  
 378X EQU 0 INTERFACE STATUS PORT Index  
 380X D.STAI EQU D.STAI+1 DATA PORT Index  
 381X  
 382X S.ERR EQU 00000001B ERROR BIT  
 383X S.DDM EQU 00100000B DONE  
 384X S.IEM EQU 01000000B INTERRUPT ENABLE  
 385X S.DTR EQU 10000000B DATA TERMINAL REQUEST  
 386X  
 387X S.SW0 EQU 00000010B DIP SWITCH: 0  
 388X S.SW1 EQU 00001000B DIP SWITCH: 1  
 389X S.SW2 EQU 00001000B DIP SWITCH: 2  
 390X S.SW3 EQU 00010000B DIP SWITCH: 3  
 391X  
 392X M.RES EQU 00000010B RESET COMMAND

394X \*\* STATUS BYTE FLAGS

395X \*  
 396X  
 397X SB.UMR EQU 10000000B UNIT NOT READY  
 398X SB.WPD EQU 01000000B WRITE PROTECTED DRIVE  
 399X SB.DLD EQU 00100000B DELETED DATA  
 400X SB.NRF EQU 00010000B NO RECORD FOUND  
 401X SB.CRC EQU 00001000B CRC ERROR  
 402X SB.LTD EQU 00000100B LATE DATA  
 403X SB.ILC EQU 00000010B ILLEGAL COMMAND  
 404X SB.8TD EQU 00000001B BAD TRACK OVERFLOW

406X \*\* AUXILIARY STATUS BYTE FLAGS

407X \*  
 408X  
 409X AS.0DD EQU 01000000B TRACK 0 DOUBLE DENSITY  
 410X AS.1DD EQU 00100000B TRACK 1-76 DOUBLE DENSITY  
 411X AS.S1A EQU 00010000B SIDE 1 AVAILABLE  
 412X AS.SLM EQU 00000011B SECTOR LENGTH MASK

```

414X **      DISK COMMANDS
415X *
416X
417X          ORG          0
000.000
000.000  DD.800T DS      1
000.001  DD.RST DS      1
000.002  DD.RAS DS      1
000.003  DD.LSC DS      1
000.004  DD.RAD DS      1
000.005  DD.REA DS      1
000.006  DD.WRI DS      1
000.007  DD.REAB DS     1
000.010  DD.WRIB DS     1
000.011  DD.WRD DS      1
000.012  DD.WR8D DS     1
000.013  DD.CPY DS      1
000.014  DD.FRM0 DS     1
000.015  DD.FRM1 DS     1
000.016  DD.FRM2 DS     1
000.017  DD.FRM3 DS     1
000.020  DD.RRDY DS     1
    BOOT
    READ STATUS
    READ AUX. STATUS
    LOAD SECTOR COUNT
    READ ADDRESS OF LAST SECTOR ACCESSED
    READ SECTORS
    WRITE SECTORS
    READ SECTORS BUFFERED
    WRITE SECTORS BUFFERED
    DD.WRI + DELETED
    DD.WRIB + DELETED
    COPY
    FORMAT IBM SD
    FORMAT IBM SD
    FORMAT IBM DD
    FORMAT IBM DD
    Read Ready (conflict with DD.SPF0)
    
```

```

436X **      Special De-Bug Functions
437X *
438X
439X          ORG          010H
000.020
000.020  DD.SPF0 DS     1
000.021  DD.SPF1 DS     1
000.022  DD.SPF2 DS     1
000.023  DD.SPF3 DS     1
000.024  DD.SPF4 DS     1
000.025  DD.SPF5 DS     1
    SPECIAL FUNCTION 0
    SPECIAL FUNCTION 1
    SPECIAL FUNCTION 2
    SPECIAL FUNCTION 3
    SPECIAL FUNCTION 4
    SPECIAL FUNCTION 5
    
```

```

447X **      Special Heath Functions
448X *
449X
450X          ORG          080H
000.200
000.200  DD.SDC DS      1
000.201  DD.ST DS       1
000.202  DD.DS DS       1
000.203  DD.RDL DS      1
000.204  DD.WTL DS      1
000.205  DD.R08L DS     1
000.206  DD.WTBL DS     1
000.207  DD.WTDL DS     1
000.210  DD.WDLB DS     1
    SET DRIVE CHARACTERISTICS
    SEEK TO TRACK
    DISK STATUS
    READ LOGICAL
    WRITE LOGICAL
    READ BUFFERED LOGICAL
    WRITE BUFFERED LOGICAL
    WRITE DELETED DATA LOGICAL
    WRITE BUFFERED DELETED DATA LOGICAL
    
```

```

461X ** Useful Flags
462X *
463X
464X UNIT.0 EQU 000000008 Unit: 0
465X UNIT.1 EQU 001000008 Unit: 1
466X UNIT.2 EQU 010000008 Unit: 2
467X UNIT.3 EQU 011000008 Unit: 3
468X
469X UNIT.M EQU UNIT.0|UNIT.1|UNIT.2|UNIT.3 Unit Mask
470X
471X
472X
473X SID.0 EQU 000000008 Side: 0
474X SID.1 EQU 100000008 Side: 1
475X
476X SID.M EQU SID.0|SID.1 Side Mask
477X
478X
479X
480X SEC.M EQU 000111118 Track Mask
481X
482X
483X
484X SSIZ.M EQU 1024 Maximum Sector Size
485X
486X
487X #C.128 EQU 128
488X #C.256 EQU 256
489X #C.26 EQU 26
490 XTEXT U8251 DEFINE 8251 USART BITS
490

```

```

493X **      8251 USART BIT DEFINITIONS.
494X *
495X
496X **      PORT ADDRESSES
497X
498X UDR      EQU 0      DATA REGISTER IS EVEN
499X USR      EQU 1      STATUS REGISTER IS NEXT
500X
501X SC.UART  EQU 3720   CONSOLE USART ADDRESS (IFF 8251)
502X
503X
504X **      MODE INSTRUCTION CONTROL BITS.
505X
506X UMI.1B   EQU 01000000B 1 STOP BIT
507X UMI.HB   EQU 10000000B 1 1/2 STOP BITS
508X UMI.2B   EQU 11000000B 2 STOP BITS
509X UMI.PE   EQU 00100000B EVEN PARITY
510X UMI.PA   EQU 00010000B USE PARITY
511X UMI.L5   EQU 00000000B 5 BIT CHARACTERS
512X UMI.L6   EQU 00001000B 6 BIT CHARACTERS
513X UMI.L7   EQU 00001000B 7 BIT CHARACTERS
514X UMI.L8   EQU 00001100B 8 BIT CHARACTERS
515X UMI.1X   EQU 00000001B CLOCK X 1
516X UMI.16X EQU 00000010B CLOCK X 16
517X UMI.64X  EQU 00000011B CLOCK X 64
518X
519X **      COMMAND INSTRUCTION BITS.
520X
521X UCI.IR   EQU 01000000B INTERNAL RESET
522X UCI.RD   EQU 00100000B READER-ON CONTROL FLAG
523X UCI.ER   EQU 00010000B ERROR RESET
524X UCI.RE   EQU 00001000B RECEIVE ENABLE
525X UCI.IE   EQU 00000010B ENABLE INTERRUPTS FLAG
526X UCI.ITE  EQU 00000001B TRANSMIT ENABLE
527X
528X **      STATUS READ COMMAND BITS.
529X
530X USR.FE    EQU 00100000B FRAMING ERROR
531X USR.DE    EQU 00010000B OVERRUN ERROR
532X USR.PE    EQU 00001000B PARITY ERROR
533X USR.TXE   EQU 00000100B TRANSMITTER EMPTY
534X USR.RXR  EQU 00000010B RECEIVER READY
535X USR.TXR  EQU 00000001B TRANSMITTER READY

```

538 \*\*\* INTERRUPT VECTORS.  
 539 \*  
 540

542 \*\* LEVEL 0 - RESET  
 543 \*  
 544 \* THIS 'INTERRUPT' MAY NOT BE PROCESSED BY A USER PROGRAM.  
 545

000.000 ORG 00A  
 547  
 548 RAM8GO EQU \* RAM8GO Address /Ram8Go 2/  
 549

550 \*  
 000.000 021 000 000 LXI D,RAM8GO ROM COPY OF RAM /Ram8Go 2/  
 000.003 303 016 004 JMP XINIT DO EXTENDED INITIALIZATION (ROM)/RAM8GO JUN80/  
 000.006 303 073 000 JMP INIT INITIALIZE  
 377.073 ERRPL INIT-1000A BYTE IN WORD 10A MUST BE 0

556 \*\* LEVEL 1 - CLOCK  
 557  
 558 INT1 EQU 100 INTERRUPT ENTRY POINT  
 559

000.000 ERNZ \*-11Q INTO TAKES UP ONE BYTE  
 000.011 315 132 000 CALL SAVALL SAVE USER REGISTERS  
 000.014 026 000 MVI 0,0  
 000.016 303 201 000 JMP CLOCK PROCESS CLOCK INTERRUPT  
 377.201 ERRPL CLOCK-1000A EXTRA BYTE MUST BE 0

566 \*\* LEVEL 2 - SINGLE STEP  
 567 \*  
 568 \* IF THIS INTERRUPT IS RECEIVED WHEN NOT IN MONITOR MODE,  
 569 \* THEN IT IS ASSUMED TO BE GENERATED BY A USER PROGRAM  
 570 \* (SINGLE STEPPING OR BREAKPOINTING). IN SUCH CASES, THE  
 571 \* USER PROGRAM IS ENTERED THROUGH (UIVEC+3)

572  
 573 INT2 EQU 20A LEVEL 2 ENTRY  
 574

000.000 ERNZ \*-21A INT1 TAKES EXTRA BYTE  
 000.021 315 132 000 CALL SAVALL SAVE REGISTERS  
 000.024 032 LDAX D (A) = (CTLFLG)  
 040.011 SET CTLFLG  
 000.025 303 244 001 JMP STPRM STEP RETURN



```

581 *** I/O INTERRUPT VECTORS.
582 *
583 * INTERRUPTS 3 THROUGH 7 ARE AVAILABLE FOR GENERAL I/O USE.
584 *
585 * THESE INTERRUPTS ARE NOT SUPPORTED BY PAM/8, AND SHOULD
586 * NEVER OCCUR UNLESS THE USER HAS SUPPLIED HANDLER ROUTINES
587 * (THROUGH UIVEC)
588
000.030 ORG 30A JUMP TO USER ROUTINE
000.030 303 045 040 JMP UIVEC+6
000.033 064 064 064 DB '44470' Heath Part Number /Ram8Go 2/

000.040 ORG 40A
000.040 303 050 040 JMP UIVEC+9 JUMP TO USER ROUTINE
000.043 100 112 107 DB 100q,112q,107q,114q,100q Support Code /Ram8Go 2/

000.050 ORG 50A
000.050 303 053 040 JMP UIVEC+12 JUMP TO USER ROUTINE
601
602
603 ** DLY - DELAY TIME INTERVAL.
604 *
605 * ENTRY (A) = MILLISECOND DELAY COUNT/2
606 * EXIT NONE
607 * USES A,F
608
000.053 365 PUSH PSH SAVE COUNT
000.054 257 XRA A DONT SOUND HORN
000.055 303 143 002 JMP HRNO PROCESS AS HORN

000.060 ORG 60A
000.060 303 056 040 JMP UIVEC+15 JUMP TO USER ROUTINE
615
616
617 GO. MVI A,C8,SSI+C8,CL1+C8,SPK OFF MONITOR MODE LIGHT
000.065 303 235 001 JMP SSI1 RETURN TO USER PROGRAM

000.070 ORG 70A
000.070 303 061 040 JMP UIVEC+18 JUMP TO USER ROUTINE
    
```

```

624 **      INIT - INITIALIZE SYSTEM
625 *
626 *      INIT IS CALLED WHENEVER A HARDWARE MASTER-CLEAR IS INITIATED.
627 *
628 *      SETUP PAM/8 CONTROL CELLS IN RAM.
629 *      DECODE HOW MUCH MEMORY EXISTS, SETUP STACKPOINTER, AND
630 *      ENTER THE MONITOR LOOP.
631 *
632 *      ENTRY FROM MASTER CLEAR
633 *      EXIT INTO PAM/8 MAIN LOOP
634
635
636 INIT      LDAX D      COPY *PRSRM* INTO RAM
637 MOV      M,A      MOVE BYTE
638 DCX      H      DECREMENT DESTINATION
639 INR      E      INCREMENT SOURCE
640 JNZ      INIT     IF NOT DONE
641
642 SINCRA   EQU      4000A      SEARCH INCREMENT
643
644 MVI      D,SINCRA/256      (DE) = SEARCH INCREMENT
645 LXI      H,START          (HL) = FIRST RAM
646
647 *      DETERMINE MEMORY LIMIT.
648
649 INITI    JMP      XINITI    JUMP TO FREE SPACE
650
651 DB       *HEATH*
652 ERRNZ   *-000117A
653
654 *      RETURN TO INLINE CODE WITH HL SET TO FIRST NON-EXISTANT LOCATION
655
656 INIT2   DCX      H      SET STACKPOINTER = MEMORY LIMIT -1
657 SPHL
658 LXI      H,DEFFC      Set *PC* value on stack
659 PUSH    H      Tape UART/Auto-Boot
660 CALL    PATCH1      Set Return Address
661 PUSH    H      Leave addresses the same & A=0
662 XRA     A      /Ram8Gq 2/
    
```

```

665 ** SAVALL - SAVE ALL REGISTERS ON STACK.
666 *
667 * SAVALL IS CALLED WHEN AN INTERRUPT IS ACCEPTED, IN ORDER TO
668 * SAVE THE CONTENTS OF THE REGISTERS ON THE STACK.
669 *
670 * ENTRY CALLED DIRECTLY FROM INTERRUPT ROUTINE.
671 * EXIT ALL REGISTERS PUSHED ON STACK,
672 * IF NOT YET IN MONITOR MODE, REGPTR = ADDRESS OF REGISTERS
673 * ON STACK.
674 * (DE) = ADDRESS OF CTLFLG
675
676
677 SAVALL XTHL SET H9L ON STACK TOP
678 PUSH D
679 PUSH B
680 PUSH PSM
681 XCHG (D,E) = RETURN ADDRESS
682 LXI H910
683 DAD SP (H9L) = ADDRESS OF USERS SP
684 PUSH H SET ON STACK AS *REGISTER*
685 PUSH D SET RETURN ADDRESS
686 LXI D,CTLFLG (A) = CTLFLG
687 LOAX D
688 CHA
689 ANI CB.MTL+CB.SSI SAVE REGISTER ADDR IF USER OR SINGLE-STEP
690 RZ RETURN IF WAS INTERRUPT OF MONITOR LOOP
691 LXI H2
692 DAD SP (H9L) = ADDRESS OF *STACKPTR* ON STACK
693 SHLD REGPTR
694 RET
695
696 ** CUI - CHECK FOR USER INTERRUPT PROCESSING.
697 *
698 * CUI IS CALLED TO SEE IF THE USER HAS SPECIFIED PROCESSING
699 * FOR THE CLOCK INTERRUPT.
700
701
702 * CUI1 SET *MFLAG REFERENCE TO MFLAG
703 LDAX B (A) = *MFLAG
704 ERNZ UD.CLK-1 CODE ASSUMED = 01
705 RRC
706 CC UIVEC IF SPECIFIED, TRANSFER TO USER
707
708 * RETURN TO PROGRAM FROM INTERRUPT.
709
710 INTXIT POP PSM REMOVE FAKE *STACK REGISTER*
711 POP PSM
712 POP B
713 POP D
714 POP H
715 EI
716 RET
    
```

```

719 *** CLOCK - PROCESS CLOCK INTERRUPT
720 *
721 * CLOCK IS ENTERED WHENEVER A MILLISECOND CLOCK INTERRUPT IS
722 * PROCESSED.
723 *
724 * TICCNT IS INCREMENTED EVERY INTERRUPT.
725
726
000.201 052 033 040 CLOCK LHL0 TICCNT
000.204 043 INX H
000.205 042 033 040 SHLD TICCNT INCREMENT TICCNT
730
731 ** REFRESH FRONT PANEL.
732 *
733 * THIS CODE DISPLAYS THE APPROPRIATE PATTERN ON THE
734 * FRONT PANEL LEDS. THE LEDS ARE PAINTED IN REVERSE ORDER,
735 * ONE PER INTERRUPT. FIRST, NUMBER 9 IS LIT, THEN NUMBER 8,
736 * ETC.
737
738
000.210 041 010 040 LXI H,MFLAG
000.213 176 MOV A,M
000.214 107 B,A (H) = CURRENT FLAG
000.215 346 100 ANI UD,MFR SEE IF FRONT PANEL REFRESH WANTED
743 INX H
000.000 CTLFLG-MFLAG-1
000.220 176 MOV A,M (A) = CTLFLG
000.221 112 MOV C,D (C) = 0 IN CASE NO PANEL DISPLAY
000.222 302 237 000 JNZ CLK3 IF NOT
000.225 043 INX H (H,L) = (REFIND)
749 ERRNZ REFIN0-CTLFLG-1
000.226 065 DCR M DECREMENT DIGIT INDEX
000.227 302 234 000 JNZ CLK2 IF NOT WRAP-AROUND
000.232 066 011 MVI M,9 WRAP DISPLAY AROUND
753 MOV E,M (H,L) = ADDRESS OF PATTERN
000.235 031 DAD D
755 MOV C,E (A) = CTLNLG
000.237 113 EQU * (A) = INDEX + FIXED BITS
000.237 261 ORA C SELECT DIGIT
000.240 323 360 OUT OP,DIG
000.242 176 MOV A,M SELECT SEGMENT
000.243 323 361 OUT OP,SEG
761
762 * SEE IF TIME TO DECODE DISPLAY VALUES.
763
764 MVI L,#TICCNT
765 MOV A,M
766 ANI 37Q EVERY 32 INTERRUPTS
000.252 314 161 003 CZ UFD UPDATE FRONT PANEL DISPLAYS
768
769 * EXIT CLOCK INTERRUPT.
770
000.255 001 011 040 LXI B,CITFLG (A) = CTLFLG
000.260 012 LOAX B
000.261 346 040 ANI CB,MIL
000.263 302 172 000 JNZ INTXIT IF IN MONITOR MODE

```

RAM860 - H8 FRONT PANEL MONITOR #01.02.00. Unix H8ASM V1.4.1 5-Jul-80 Page 18  
 PROCESS CLOCK INTERRUPTS 16:52:58 11-SEP-80

```

000.266 013          DCX      B
000.000          ERRNZ    CYLFLG--MFLAG-I
000.267 012          LDAX   B      (A) = .MFLAG
000.000          ERRNZ    UD-HLT-2000  ASSUME HIGH-ORDER
000.270 027          RAL
000.271 332 313 000 JC      CLK4    SKIP IT
781
782 *             NOT IN MONITOR MODE. CHECK FOR HALT
783
000.274 076 012     MVI     A,10   (A) = INDEX OF *P* REG
000.276 315 052 003 CALL   LRA.    LOCATE REGISTER ADDRESS
000.301 136         MOV     E,M
000.302 043         INX     H
000.303 126         MOV     D,M   (D+E) = PC CONTENTS
000.304 033         DCX     D
000.305 032         LDAX   D
000.306 376 166     CPI     MI-HLT  CHECK FOR HALT
000.310 312 322 000 JE      ERROR  IF HALT, BE IN MONITOR MODE
791
792
793
794 *             CHECK FOR 'RETURN TO MONITOR' KEY ENTRY.
795
000.313          EQU     CLK4 *
000.313 333 360     IN      IP.PAD
000.315 376 056     CPI     560    SEE IF '0' AND '#'
000.317 302 165 000 JNE     CUIL   IF NOT, ALLOW USER PROCESSING OF CLOCK
    
```

```

803 ***      ERROR - COMMAND ERROR.
804 *
805 *      ERROR IS CALLED AS A 'BAIL-OUT' ROUTINE.
806 *
807 *      IT RESETS THE OPERATIONAL MODE, AND RESTORES THE STACKPOINTER.
808 *
809 *      ENTRY      NONE
810 *      EXIT      TO MTR LOOP
811 *      CTLFLG SET
812 *      *MFLAG CLEARED
813 *      USES      ALL
814
815
816 ERROR EQU *
817 LXI H, MFLAG
818 MOV A, M (A) = *MFLAG
819 ANI 3770-UO, DDU-UO, MFR RE-ENABLE DISPLAYS
820 MOV M, A REPLACE
821 INX H
822 MVI M, CB, SSI+CB, MTL+CB, CLI+CB, SPK RESTORE *CTLFLG*
823 ERRNZ CTLFLG-, MFLAG-1
824 EI
825 LHLD REGPTR
826 SPHL RESTORE STACK POINTER TO EMPTY STATE
827 CALL ALARM ALARM FOR 200 MS

```

```

829 **      MTR - MONITOR LOOP.
830 *
831 *      THIS IS THE MAIN EXECUTIVE LOOP FOR THE FRONT PANEL EMULATOR.
832
833
834 MTR EQU *
835 EI
836
837 MTR1 LXI H, MTR1
838 PUSH H
839 LXI B, DSPMOD SET *MTR1* AS RETURN ADDRESS
840 LDAX B (BC) = #DSPMOD
841 ANI 1 (A) = 1 IF ALTER
842 CMA
843 STA DSPROT SET FLAG BIT IF ALTER
844
845 *      READ KEY
846
847 CALL RCK READ CONSOLE KEYSET
848 LHLD ABRUSS
849 CPI 10
850 JNC MTR4 IF IN 'ALWAYS VALID' GROUP
851 MOV E, A SAVE VALUE
852 SET DSPMOD (A) = DSPMOD
853 LDAX B
854 RRC
855 JC MTR5 IF IN ALTER MODE

```

```

001.004 173      MOV     A,E      (A) - CODE
856
857
858 *      HAVE A COMMAND (NOT A VALUE)
859
001.005 326 004  MTR#    SUI     (A) - COMMAND
001.007 332 160 004 JC      Extended Commands /Ram8Go 2/
001.012 137      MOV     E,A
001.013 345      PUSH   H
001.014 041 035 001 LXI     H,MTR#
001.017 026 000  MVI     D,0
001.021 031      DAD     D
001.022 136      MOV     E,M
001.023 031      DAD     D
001.024 343      XTHL
001.025 021 005 040 LXI     D,REGI
040.007 012      SET     DSPMOD
001.030 012      LDAX   B
001.031 346 002  ANI     2
001.033 012      LDAX   B
001.034 311      RET

001.035
001.035 165      EQU     MTR#
001.036 141      DB
001.037 143      DB
001.040 165      DB
001.041 220      DB
001.042 332      DB
001.043 067      DB
001.044 104      DB
001.045 102      DB
001.046 060      DB
001.047 116      DB
001.050 034      DB

001.035      EQU     MTR#
001.035 165      DB
001.036 141      DB
001.037 143      DB
001.040 165      DB
001.041 220      DB
001.042 332      DB
001.043 067      DB
001.044 104      DB
001.045 102      DB
001.046 060      DB
001.047 116      DB
001.050 034      DB

JUMP TABLE
4 - GO
5 - INPUT
6 - OUTPUT
7 - SINGLE STEP
8 - CASSETTE LOAD
9 - CASSETTE DUMP
+ - NEXT
- - LAST
* - ABORT
/ - DISPLAY/ALTER
# - MEMORY MODE
. - REGISTER MODE

```

```

892 **      PROCESS MEMORY/REGISTER ALTERATIONS.
893 *
894 *      THIS CODE IS ENTERED IF
895 *
896 *      1) AM IN ALTER MODE, AND
897 *      2) A KEY FROM 0-7 WAS ENTERED.
898
001.051 017      RRC
001.052 173      MOV     A,E
001.053 332 072 001 JC      MTR#
001.056 067      STC
001.057 315 066 003 CALL   I08
001.062 043      INX     H

```

```

906 ** SAE - STORE ABUSS AND EXIT.
907 *
908 * ENTRY (HL) = ABUSS VALUE
909 * EXIT TO (RET)
910 * USES NONE
911
001.063 042 024 040 SHLD ABUSS
001.066 311 RET
000.000
001.067 303 066 007 ERRNZ *-1067A
001.067 303 066 007 H89PIN JMP PIN H89 Compatible PIN routine /Ram8Go 2/
917
001.072 365 MTR6 PUSH P SW SAVE CODE
001.073 315 047 003 CALL LRA LOCATE REGISTER ADDRESS
001.076 247 ANA A Reserve Space /Ram8Go 2/
001.077 303 274 007 JMP PATCH2 /Ram8Go 2/
001.102 DS 2 Insure good routine addresses /Ram8Go 2/
000.000 ERRNZ *-1104A
923

```



```

927 ** REGM - ENTER REGISTER DISPLAY MODE.
928 *
929 * ENTRY (A) = DSPMOD
930
931 REGM A,2 SET DISPLAY REGISTER MODE
932 * SET DSPMOD
933 STAX B SET DISPLAY REGISTER MODE
934 ERRNZ DSPMOD-DSPROT-1 (BC) = #DSPROT
935 DCX B
936 XRA A
937 STAX B SET ALL PERIODS ON
938 CALL RCK READ KEY ENTRY
939 DCR A DISPLACE
940 CPI 6
941 JNC ERROR NOT 1-6
942 RLC
943 STAX D SET NEW REG IND
944 * SET REGI
945 RET

947 ** RSM - TOGGLE DISPLAY/ALTER MODE.
948 *
949 * ENTRY (A) = DSPMOD
950 * (BC) = ADDRESS OF DSPMOD
951
952 * SET DSPMOD
953 XRI 1
954 STAX B
955 RET

957 ** NEXT - INCREMENT DISPLAY ELEMENT.
958 *
959 * ENTRY (HL) = (ABUSS)
960 * (DE) = ADDRESS OF REGIND
961
962 NEXT INX H
963 JZ SAE IF MEMORY, STORE ABUSS AND EXIT
964
965 * IS REGISTER MODE.
966
967 * SET REGI
968 LDAX D (A) = REGI
969 ADI 2 INCREMENT REG INNEX
970 STAX D WRAP TO *SP*
971 CPI 12
972 RC IF NOT TOO LARGE, EXIT
973 XKA A OVERFLOW
974 STAX D
975 ABORT RET
    
```

```

977 ** LAST - DECREMENT DISPLAY ELEMENT.
978 *
979 * ENTRY (HL) = (ABUSS)
980 * (DE) = ADDRESS OF REGIND
981
982
983 LAST DCX H
984 JZ SAE IF MEMORY, STORE AND EXIT
985
986 * IS REGISTER MODE.
987
988 * SET REGI
989 LST2 LDAX D (A) = REGI
990 SUI 2
991 STAX D
992 RMC IF OK
993 MVI A,10 UNDERFLOW TO *PC*
994 STAX D
995 RET
996

```

```

998 ** MEMM - ENTER DISPLAY MEMORY MODE.
999 *
1000 * ENTRY (BC) = ADDRESS OF DSPMOD
1001
1002 MEMM XRA A (A) = 0
1003 SET DSPMOD
1004 STAX B SET DISPLAY MEMORY MODE
1005 ERNZ DSPMOD-DSPROT-1
1006 DCX B (BC) = #DSPROT
1007 STAX B SET ALL PERIODS ON
1008 LXI H,ABUSS+1
1009 JMP IOA INPUT OCTAL ADDRESS

```

```

1011 ** IN - INPUT DATA BYTE.
1012 *
1013
1014 ** OUT - OUTPUT DATA BYTE.
1015 *
1016 * ENTRY (HL) = (ABUSS)
1017
1018 IN MVI B,MI-IN SKIP NEXT INSTRUCTION
1019 DB MI-LXIO
1020 OUT MVI B,MI-OUT
1021 MOV A,H (A) = VALUE
1022 MOV H,L (H) = PORT
1023 MOV L,B (L) = IN/OUT INSTRUCTION
1024 SHLD IOMRK PERFORM IO
1025 CALL IOMRK CALL
1026 MOV L,H (L) = PORT
1027 MOV H,A (H) = VALUE

```

RAM8GD - H8 FRONT PANEL MONITOR #01.02.00. IN Unix H8ASM V1.4.1 5-Jul-80 Page 24  
MONITOR TASK SUBROUTINES. 16:53:03 11-SEP-80

001.217 303 063 001 1028 JMP SAE STORE ABUSS AND EXIT

```

1033 **      GO - RETURN TO USER MODE
1034 *
1035 *      ENTRY NONE
1036
001.222 303 063 000 1037 GO          ROUTINE IS IN WASTE SPACE
    
```

```

1039 **      SSTEP - SINGLE STEP INSTRUCTION.
1040 *
1041 *      ENTRY NONE
1042
001.225      SSTEP EQU *          SINGLE STEP
001.225 363      DI              DISABLE INTERRUPTS UNTIL THE RIGHT TIME
001.226 072 011 040 LDA CTLFLG    CLEAR SINGLE STEP INHIBIT
001.231 356 020 XRI CB.SSI     PRIME SINGLE STEP INTERRUPT
001.233 323 360 OUT OP.CTL    SET NEW FLAG VALUES
001.235 062 011 040 STA CTLFLG  CLEAN STACK
001.240 341      POP H          RETURN TO USER ROUTINE FOR STEP
001.241 303 172 000 JMP INTXIT
    
```

```

1052 **      STPRIN - SINGLE STEP RETURN
1053
001.244      STPRIN EQU *
001.244 366 020 ORI CB.SSI     DISABLE SINGLE STEP INTERRUPTION
001.246 323 360 SET OP.CTL    TURN OFF SINGLE STEP ENABLE
040.011      *
1057 *      STAX D              SEE IF IN MONITOR MODE
001.250 022      ANI CB.MTL    TRANSFER TO USER'S ROUTINE
001.251 346 040 JNZ MTR
001.253 302 344 000 JMP UIVEC+3
001.256 303 042 040
    
```

```

1063 **      RMEM - LOAD MEMORY FROM TAPE.
1064 *
1065
001.261 041 244 002 LXI H,TPABT
001.264 042 031 040 SHLD TPERRX  SETUP ERROR EXIT ADDRESS
1068 *      JMP LOAD
    
```

```

1070 *** LOAD - LOAD MEMORY FROM TAPE.
1071 *
1072 * READ THE NEXT RECORD FROM THE CASSETTE TAPE.
1073 *
1074 * USE THE LOAD ADDRESS IN THE TAPE RECORD.
1075 *
1076 * ENTRY (HL) = ERROR EXIT ADDRESS
1077 * EXIT USER P-REG (IN STACK) SET TO ENTRY ADDRESS
1078 * TO CALLER IF ALL OK
1079 * TO ERROR EXIT IF TAPE ERRORS DETECTED.
1080
1081
1082 EQU *
1083 LXI B,1000A-RT.MI*256-256 (BC) = - REQUIRED TYPE AND #
1084 CALL SRS SCAN FOR RECORD START
1085 MOV L,A (HL) = COUNT
1086 XCHG (DE) = COUNT, (HL) = TYPE AND #
1087 DCR C (C) = -NEXT #
1088 DAD B
1089 MOV A,H
1090 PUSH B
1091 PUSH PSW
1092 ANI L770
1093 ORA L
1094 MVI A,2
1095 JNE TPEAR
1096 CALL RNP
1097 MOV B,H
1098 MOV C,A
1099 MVI A,10
1100 PUSH D
1101 CALL L,A.
1102 POP D
1103 MOV M,C
1104 INX H
1105 MOV M,B
1106 CALL RNP
1107 MOV L,A
1108 SHLD START
1109
1110 LOAI
1111 CALL RNB
1112 MOV M,A
1113 SHLD ABUSS
1114 INX H
1115 DCR D
1116 MOV A,D
1117 ORA E
1118 JNZ LOAI
1119
1120 CALL CTC
1121 * READ NEXT BLOCK
1122
1123 POP PSW
1124 POP B
1125 RLC
    
```

(A) = FILE TYPE BYTE  
 (BC) = -(LAST TYPE, LAST #)

RAM800 - H8 FRONT PANEL MONITOR #01-02-00.  
 \*CO\* AND \*STEP\* FUNCTIONS

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LOAD

Page 27

001.366 332 133 002 1126 JC TFT  
 001.371 303 272 001 1127 JMP LOAD  
 ALL DONE - TURN OFF TAPE  
 READ ANOTHER RECORD

JC  
 JMP  
 TFT  
 LOAD

JC  
 JMP

001.366 332 133 002 1126  
 001.371 303 272 001 1127

( A series of 25 horizontal dotted lines for writing, located on the right side of the page. )

```

1130 *** DUMP MEMORY TO MAG TAPE.
1131 *
1132 * DUMP SPECIFIED MEMORY RANGE TO MAG TAPE.
1133 *
1134 * ENTRY (START) = START ADDRESS
1135 * (ABUSS) = END ADDRESS
1136 * USER PC = ENTRY POINT ADDRESS
1137 * EXIT TO CALLER.
1138
1139
001.374 EQU *
001.374 M:TPABY
001.377 SHLD TPERRX          SETUP ERROR EXIT

002.002 MVI A,UCI.ITE
002.004 OUT OP.TPC          SETUP TAPE CONTROL
002.006 MVI A,A.SYN
002.010 MVI M:32          (H) = # OF SYNC CHARACTERS
002.012 CALL MNB
002.015 DCR H
002.016 JNZ M:1          WRITE SYN HEADER
002.021 MVI A,A.STX
002.023 CALL MNB          WRITE STX
002.026 MOV L,H           (HL) = 00
002.027 CLR C            CLEAR CRC 16
002.032 LXI M,RT.MI*80H*256+1  FIRST AND LAST MI RECORD
002.035 CALL WNP          WRITE HEADER
002.040 LHL START
002.043 XCHG
002.044 LHL ABUSS
002.047 INX H
002.050 MOV A,L
002.051 SUB E
002.052 MOV L,A
002.054 MOV A,H
002.055 D
002.056 MOV H,A
002.061 CALL MNP          (HL) = COUNT
002.062 PUSH H           WRITE COUNT
002.064 MOV D,A
002.065 CALL LRA        SAVE (DE)
002.071 MOV A,M          LOCATE P-REG ADDRESS
002.072 INX H
002.073 MOV H,M
002.074 MOV L,A
002.077 CALL MNP          (HL) = CONTENTS OF PC
002.100 POP D            WRITE HEADER
002.101 POP D            (HL) = ADDRESS
002.104 CALL MNP          (DE) = COUNT
002.105
002.110 M:2
002.113 MNB
002.114 SHLD ABUSS          WRITE BYTE
002.115 DCX H            SET ADDRESS FOR DISPLAY
002.116
002.117
002.118
002.119
002.120
002.121
002.122
002.123
002.124
002.125
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002.179
002.180
002.181
002.182
002.183
002.184
002.185
    
```

```

002.115 172      MOV      A,D
002.116 263      ORA      E
002.117 302 104 002 JNZ      WMEZ      IF MORE TO GO
1189      *
1190      *      WRITE CHECKSUM
1191
002.122 052 027 040 LHL      CRCSUM
002.125 315 017 003 CALL     WMP
002.130 315 017 003 CALL     WMP
1195      *      JMP      TFT
1197      **      TFT - TURN OFF TAPE.
1198      *
1199      *      STOP THE TAPE TRANSPORT.
1200      *
1201
002.133 257      XRA      A
002.134 323 371  OUT     DP,TPC      TURN OFF TAPE
1205      **      HORN - MAKE NOISE.
1206      *
1207      *      ENTRY (A) = (MILLISECOND COUNT)/2
1208      *      EXIT  NONE
1209      *      USES  A,F
1210
1211
002.136 076 144  ALARM   MVI     A,200/2      200 MS BEEP
002.140 365      PUSH    PSH
002.141 076 200  HORN    MVI     A,CB,SPK      TURN ON SPEAKER
1215
002.143 343      HRNO    XTHL     0          SAVE (HL), (H) = COUNT
002.144 325      PUSH    0          SAVE (DE)
002.145 353      XCHG   H,CYTLFLG      (D) = LOOP COUNT
002.146 041 011 040 LXI     H,CYTLFLG
002.151 256      XRA      M
002.152 136      MOV     M,A
002.153 167      MOV     M,A
002.154 056 033  MVI     L,#TICCNT      (E) = OLD CYTLFLG VALUE
1225
002.156 172      MOV     A,D          (A) = CYCLE COUNT
002.157 206      ADD     M
002.160 276      CMP     H          WAIT REQUIRED TICCOUNTS
002.161 302 160 002 HRN2    JNE     HRN2
002.164 056 011  MVI     L,#CYTLFLG
002.166 163      MOV     M,E
002.167 321      POP     D
002.170 341      POP     D
002.171 311      RET

```



```

1238 ** CTC - VERIFY CHECKSUM.
1239 *
1240 * ENTRY TAPE JUST BEFORE CRC
1241 * EXIT TO CALLER IF OK
1242 * TO *TPERR* IF BAD
1243 * USES A,F,H,L
1244 *
1245
002.172 315 325 002 CALL RMP READ NEXT PAIR
002.175 052 027 040 LHLD CRCSUM
002.200 174 MOV A,H
002.201 265 ORA L
002.202 310 RZ
002.203 076 001 MVI A,1 RETURN OF OK
                                CHECKSUM ERROR
                                (8) = CODE
1251 * JMP TPERR
1252 *

1254 ** TPERR - PROCESS TAPE ERROR.
1255 *
1256 * DISPLAY ERR NUMBER IN LOW BYTE OF ABUSS
1257 *
1258 * IF ERROR NUMBER EVEN, DONT ALLOW #
1259 * IF ERROR NUMBER ODD, ALLOW #
1260 *
1261 * ENTRY (8) = PATTERN
1262 *
1263
002.205 062 024 040 TPERR STA ABUSS
002.210 107 MOV B,A (8) = CODE
002.211 315 133 002 CALL IFT TURN OFF TAPE

1268 * IS #, RETURN (IF PARITY ERROR)
1269
1270 DB MI,ANI FALL THROUGH WITH CARRY CLEAR
002.214 346 MOV A,B
002.215 170 MOV A,B
1271 TER3
1272
002.216 017 RRC
002.217 330 RC RETURN IF OK

1275 * BEEP AND FLASH ERROR NUMBER
1276 *
1277
002.220 334 136 002 TER1 CC ALARM ALARM IF PROPER TIME
002.223 315 252 002 TER1 CALL TPXIT SEE IF #
002.226 333 360 IN IP,PAD
002.230 376 057 CPI 0010111B CHECK FOR #
002.232 312 215 002 JE TER3 IF #
002.235 072 034 040 LDA TICCNT+1
002.240 037 RAR
002.241 303 220 002 JMP TER1
    
```

```

1287 ** TPABT - ABORT TAPE LOAD OR DUMP.
1288 *
1289 * ENTERED WHEN LOADING OR DUMPING, AND THE *** KEY
1290 * IS STRUCK.
1291
1292
1293 TPABT XRA A
1294 OUT OP.TPC OFF TAPE
1295 JMP ERROR
002.244 257
002.245 323 371
002.247 303 322 000

1297 ** TPXIT - CHECK FOR USER FORCED EXIT.
1298 *
1299 * TPXIT CHECKS FOR AN *** KEYPAD ENTRY. IF SO, TAKE
1300 * THE TAPE DRIVER ABNORMAL EXIT.
1301 *
1302 * ENTRY NONE
1303 * EXIT TO *RET* IF NOT ***
1304 * (A) - PORT STATUS
1305 * TO (TPERRX) IF *** DOWN
1306 * USES A,F
1307
1308
1309 TPXIT IN IP.PAD
1310 CPI 01101111B *
1311 IN IP.TPC READ TAPE STATUS
1312 RNE NOT ***, RETURN WITH STATUS
1313 LHLD TPERRX
1314 PCHL ENTER (TPERRX)

1316 ** SRS - SCAN RECORD START
1317 *
1318 * SRS READS BYTES UNTIL IT RECOGNIZES THE START OF A RECORD.
1319 *
1320 * THIS REQUIRES
1321 * AT LEAST 10 SYNC CHARACTERS
1322 * 1 SIX CHARACTER.
1323 *
1324 * THE CRC-16 IS THEN INITIALIZED.
1325 *
1326 * ENTRY NONE
1327 * EXIT TAPE POSITIONED (AND MOVING), CRCSUM = 0
1328 * (DE) = HEADER BYTES
1329 * (HA) = RECORD COUNT
1330 * USES A,F,D,E,H,L
1331
1332
1333 SRS EQU *
1334 SRS1 MVI D,0
1335 MOV M,D
1336 MOV L,D (HL) = 0
    
```

```

002.271 315 331 002 1337 SRS2 CALL RNB READ NEXT BYTE
002.274 024 1338 INR D
002.275 376 026 1339 CPI A.SYM
002.277 312 271 002 1340 JE SRS2 HAVE SYN
002.302 376 002 1341 CPI A.STX
002.304 302 265 002 1342 JNE SRS1 NOT STX - START OVER
002.307 076 012 1343 MVI A,10
002.311 272 1344 CMP D
002.312 322 265 002 1346 JNC SRS1 SEE IF ENOUGH SYN CHARACTERS
002.315 042 027 040 1347 SHLD CRCSUM NOT ENOUGH
002.320 315 325 002 1348 CALL RNP CLEAR CRC-16
002.323 124 1349 MOV D,H READ LEADER
002.324 137 1350 MOV E,A
002.324 137 1351 * JMP RNP READ COUNT
    
```

```

1353 ** RNP - READ NEXT PAIR.
1354 *
1355 * RNP READS THE NEXT TWO BYTES FROM THE INPUT DEVICE.
1356 *
1357 * ENTRY NONE
1358 * EXIT (H,A) = BYTE PAIR
1359 * USES A,F,H
1360
1361
002.325 315 331 002 1362 RNP CALL RNB READ NEXT BYTE
002.330 147 1363 MOV H,A
002.330 147 1364 * JMP RNB READ NEXT BYTE
    
```

```

1366 ** RNB - READ NEXT BYTE
1367 *
1368 * RNB READS THE NEXT SINGLE BYTE FROM THE INPUT DEVICE.
1369 * THE CHECKSUM IS TAKEN FOR THE CHARACTER.
1370 *
1371 * ENTRY NONE
1372 * EXIT (A) = CHARACTER
1373 * USES A,F
1374
1375
    
```

```

002.331 076 064 1376 RNB MVI A,UCI.RO+UCI.ER+UCI.RE TURN ON READER FOR NEXT BYTE
002.333 323 371 1377 OP,TPC
002.335 315 252 002 1378 RMB1 CALL TPXIT CHECK FOR *, READ STATUS
002.340 346 002 1379 ANI USR,RXR
002.342 312 335 002 1380 JZ RMB1 IF NOT READY
002.345 333 370 1381 IN IP,TPD INPUT DATA
002.345 333 370 1382 * JMP RNB CHECKSUM
    
```

```

1384 ** CRC - COMPUTE CRC-16
1385 *
1386 * CRC COMPUTES A CRC-16 CHECKSUM FROM THE POLYNOMIAL
1387 *
1388 * (X + 1) * (X+15 + X + 1)
1389 *
1390 * SINCE THE CHECKSUM GENERATED IS A DIVISION REMAINDER,
1391 * A CHECKSUMED DATA SEQUENCE CAN BE VERIFIED BY RUNNING
1392 * THE DATA THROUGH CRC, AND THEN RUNNING THE PREVIOUSLY OBTAINED
1393 * CHECKSUM THROUGH CRC. THE RESULTANT CHECKSUM SHOULD BE 0.
1394 *
1395 * ENTRY (CRCSUM) = CURRENT CHECKSUM
1396 * (A) = BYTE
1397 * (CRCSUM) UPDATED
1398 * (A) UNCHANGED.
1399 * USES
1400 * F
1401
002.347 305 1402 CRC PUSH B B
002.350 006 010 1403 MVI B,B SAVE (8C)
002.352 345 1404 PUSH H (B) = 8BIT COUNT
002.353 052 027 040 1405 LHLD CRCSUM
002.356 007 1406 RLC
002.357 117 1407 MOV C,A (C) = BIT
002.360 175 1408 MOV A,L
002.361 207 1409 ADD A
002.362 157 1410 MOV L,A
002.363 174 1411 MOV A,H
002.364 027 1412 RAL
002.365 147 1413 MOV H,A
002.366 027 1414 RAL
002.367 251 1415 XRA C
002.370 017 1416 RRC
002.371 322 004 003 1417 JNC CRC2 IF NOT TO XOR
002.374 174 1418 MOV A,H
002.375 356 200 1419 XRI 2000
002.377 147 1420 MOV H,A
003.000 175 1421 MOV A,L
003.001 356 005 1422 XRI 50
003.003 157 1423 MOV L,A
003.004 171 1424 MOV A,C
003.005 005 1425 DCR B
003.006 302 356 002 1426 JNZ CRC1 IF MORE TO GO
003.011 042 027 040 1427 SMLD CRCSUM
003.014 341 1428 POP H RESTORE (HL)
003.015 301 1429 POP B RESTORE (8C)
003.016 311 1430 RET EXIT
    
```

```

1432 ** MNP - WRITE NEXT PAIR.
1433 *
1434 * MPT WRITES THE NEXT TWO BYTES TO THE CASSETTE DRIVE.
1435 *
1436 * ENTRY (H,L) = BYTES
1437 * EXIT WRITTEN.
1438 * USES A,F
1439
1440
003.017 174 MOV A,H
003.020 315 024.003 CALL MNB
003.023 175 MOV A,L
1444 * JMP MNB WRITE NEXT BYTE
1446 ** MNB - WRITE BYTE
1447 *
1448 * MNB WRITES THE NEXT BYTE TO THE CASSETTE TAPE.
1449 *
1450 * ENTRY (A) = BYTE
1451 * EXIT NONE.
1452 * USES F
1453
1454
003.024 365 MNB PUSH PSM
003.025 315 252.002 CALL TPXIT CHECK FOR *, READ STATUS
003.030 346.001 ANI USR,TRX IF MORE TO GO
003.032 312.025.003 JZ MNB1 MNB1
003.035 076.021 MVI A,UCI,ER+UCI,TE ENABLE TRANSMITTER
003.037 323.371 OUT OP,TPC TURN ON TAPE
003.041 361 POP PSM
003.042 323.370 OUT OP,TPD OUTPUT DATA
003.044 303.347.002 JMP CRC COMPUTE CRC

```

```

1467 **      LRA - LOCATE REGISTER ADDRESS.
1468 *
1469 *      ENTRY NONE.
1470 *      EXIT (A) = REGISTER INDEX
1471 *           (H,L) = STORAGE ADDRESS
1472 *           (D,E) = (0,A)
1473 *      USES A,D,E,H,L,F
1474
1475
1476
003.047 072 005 040 1477 LRA      LDA      REGI
003.052 137      LRA.      MOV      E,A
003.053 026 000 1479      MVI      D,0
003.055 052 035 040 1480      LHL      REGPTR
003.060 031      DAD      D
003.061 311      RET

```

```

1484 **      IOA - INPUT OCTAL ADDRESS.
1485 *
1486 *      ENTRY (H,L) = ADDRESS OF RECEPTION DOUBLE BYTE.
1487 *      EXIT TO *RET* IF ERROR.
1488 *           TO *RET+1 IF OK, VALUE IN MEMORY.
1489 *      USES A,D,E,H,L,F
1490
1491
003.062 315 066 003 1492 IOA      CALL   IOB      INPUT BYTE
003.065 053      DCX      H

```

```

1495 **      IOB - INPUT OCTAL BYTE.
1496 *
1497 *      READ ONE OCTAL BYTE FROM THE KEYSSET.
1498 *
1499 *      ENTRY (H,L) = ADDRESS OF BYTE TO HOLD VALUE
1500 *           'C' SET IF FIRST DIGIT IN (A)
1501 *      EXIT TO *RET* IF ALL OK
1502 *           TO *ERROR* IF ERROR
1503 *      USES A,D,E,H,L,F
1504
1505
1506
003.066 026 003 1507 IOB      MVI      D,3      (D) = DIGIT COUNT
003.070 324 260 003 1508 IOB1     CNC      RCK      READ CONSOLE KEYSSET
1509
003.073 376 010 1510      CPI      8
003.075 322 322 000 1511      JNC      ERROR      IF ILLEGAL DIGIT
1512
003.100 137 1513      MOV      E,A      (E) = VALUE
003.101 176 1514      MOV      A,M
003.102 007 1515      RLC
003.103 007 1516      RLC

```

```

003.104 007 1517 RLC
003.105 346 370 ANI 3700
003.107 263 1519 ORA E
003.110 167 1520 MOV M,A
003.111 025 1521 DCR D
003.112 302 070 003 JNZ IOB1
003.115 076 017 1522 MVI A,30/2
003.117 303 140 002 1524 JMP HORN
    
```

REPLACE

IF NOT DONE

BEEP FOR 30 MS

000 - DECODE FOR OCTAL DISPLAY.

ENTRY (H,L) - ADDRESS OF LED REFRESH AREA  
 (B) - \*OR\* PATTERN TO FORCE ON BARS OR PERIODS  
 (A) - OCTAL VALUE  
 (H,L) - NEX DIGIT ADDRESS  
 USES A,B,C,D,H,L

```

1526 ** 000 - DECODE FOR OCTAL DISPLAY.
1527 *
1528 * ENTRY (H,L) - ADDRESS OF LED REFRESH AREA
1529 * (B) - *OR* PATTERN TO FORCE ON BARS OR PERIODS
1530 * (A) - OCTAL VALUE
1531 * (H,L) - NEX DIGIT ADDRESS
1532 * USES A,B,C,D,H,L
1533
1534
003.122 325 1535 000 PUSH D
003.123 026 003 MVI D,000A/256
003.125 016 003 MVI C,3
003.127 027 1538 0001 RAL
003.130 027 RAL
003.131 027 RAL
003.132 365 1541 PUSH PSM
003.133 346 007 ANI 7
003.135 306 356 ADI #000A
003.137 137 1544 MOV E,A
003.140 032 1545 LDAX D
003.141 250 1546 XRA B
003.142 346 177 ANI 1770
003.144 250 1548 XRA B
003.145 167 1549 MOV M,A
003.146 043 1550 INX H
003.147 170 1551 MOV A,B
003.150 007 1552 RLC
003.151 107 1553 MOV B,A
003.152 361 1554 POP PSM
003.153 015 1555 DCR C
003.154 302 127 003 JNZ D001
003.157 321 1557 POP D
003.160 311 1558 RET
    
```

LEFT 3 PLACES

SAVE FOR NEXT DIGIT

(D) = INDEX  
 (A) = PATTERN

SET IN MEMORY

(A) = VALUE

IF MORE TO GO

RETURN

```

1561 ** UFD - UPDATE FRONT PANEL DISPLAYS.
1562 *
1563 *
1564 * UFD IS CALLED BY THE CLOCK INTERRUPT PROCESSOR WHEN IT IS
1565 * TIME TO UPDATE THE DISPLAY CONTENTS. CURRENTLY, THIS IS DONE
1566 * EVERY 32 INTERRUPTS, OR ABOUT 32 TIMES A SECOND.
1567 *
1568 * ENTRY (H,L) = ADDRESS OF REFCNT
1569 * EXIT NONE
1570 * USES ALL
1571 *
1572 *
003.161 EQU *
003.161 MVI A,U0.00U
003.163 ANA B
003.164 RNZ
                IF NOT TO HANDLE UPDATE
1577 MVI L,#DSPROT
1578 MOV A,M
1579 RLC
1580 MOV M,A
1581 MOV B,A
1582 INX H
1583 ERNZ DSPMOD-DSPROT-1
1584 MOV A,M
1585 ANI 2
1586 LHL ABUSS
1588 JZ UFD1
1589 * AM DISPLAYING REGISTERS.
1591 *
003.205 CALL LRA
003.210 PUSH H
003.211 LXI H,DSPA
003.214 DAD D
003.215 MOV A,M
003.216 INX H
003.217 MOV H,M
003.220 MOV L,A
003.221 XTHL
003.222 ORA H
003.223 MOV A,M
003.224 INX H
003.225 MOV H,M
003.226 MOV L,A
                LOCATE REGISTER ADDRESS
                (H,L) = ADDRESS OF REG NAME PATTERNS
                (H,L) = REG NAME PATTERN
                CLEAR 'Z'
                (HL) = ADDRESS OF REGISTER PAIR CONTENTS
1606 * SETUP DISPLAY
1607 *
1608 *
003.227 PUSH PSM
003.230 XCHG
003.231 LXI H,HALEDS
003.234 MOV A,D
003.235 CALL DDD
003.240 MOV A,E
003.241 CALL DDD
003.244 POP PSM
                FORMAT ABANK HIGH HALF
                FORMAT ABANK LOW HALF

```



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UFD - UPDATE FRONT PANEL DISPLAYS. 16:53:17 11-SEP-80

```

003.245 032 1617 LOAX D
003.246 312 122 003 1618 JZ 000 IF MEMORY, DECODE BYTE VALUE
1619
1620 * IS REGISTER. SET REGISTER NAME.
1621
003.251 066 377 1622 MVI M,3770 CLEAR DIGIT
003.253 341 1623 POP H
003.254 042 022 040 1624 SHLD DLEDS+I
003.257 311 1625 RET

```

```

1629 ** RCK - READ CONSOLE KEYSET.
1630 *
1631 * RCK IS CALLED TO READ A KEYSTROKE FROM THE CONSOLE KEYSET.
1632 * WHENEVER A KEY IS ACCEPTED.
1633 * RCK PERFORMS DEBOUNCING, AND AUTO-REPEAT. A *BIP* IS SOUNDED
1634 * WHEN A VALUE IS ACCEPTED.
1635 *
1636 * KEY PAD VALUES:
1637 *
1638 * 1111 1110 - 0
1639 * 1111 1100 - 1
1640 * 1111 1010 - 2
1641 * 1111 1000 - 3
1642 * 1111 0110 - 4
1643 * 1111 0100 - 5
1644 * 1111 0010 - 6
1645 * 1111 0000 - 7
1646 * 1110 1111 - 8
1647 * 1100 1111 - 9
1648 * 1010 1111 - *
1649 * 1000 1111 - *
1650 * 0110 1111 - *
1651 * 0100 1111 - /
1652 * 0010 1111 - #
1653 * 0000 1111 - .
1654 *

```

```

1655 * ENTRY NONE
1656 *
1657 * TO CALLER WHEN A KEY IS HIT
1658 * (A) = 0 - 10*
1659 * 1 - 11*
1660 * 2 - 12*
1661 * 3 - 13*
1662 * 4 - 14*
1663 * 5 - 15*
1664 * 6 - 16*
1665 * 7 - 17*
1666 * 8 - 18*
1667 * 9 - 19*
1668 * 10 - 1A*
1669 * 11 - 1B*
1670 * 12 - 1C*
1671 * 13 - 1D*
1672 * 14 - 1E*
1673 *
1674 * USES A,F
1675 *

```

```

003.260 EQU
003.260 345 PUSH H
003.261 305 PUSH B
003.262 016 024 MVI C,400/20 WAIT 400 HS
003.264 041 026 040 LXI H,RCKA
003.267 333 360 IN IP,PAD INPUT PAD VALUE
003.271 107 MOV B,A (B) = VALUE
1676
1677 RCK EQU *
1678 PUSH H
1679 PUSH B
1680 MVI C,400/20 WAIT 400 HS
1681 LXI H,RCKA
1682
1683 RCK1 IN IP,PAD INPUT PAD VALUE
1684 MOV B,A (B) = VALUE

```

```

003.272 076 012 1685 MVI A,20/2
003.274 315 053 000 1686 CALL DLY
003.277 170 1687 MOV A,B
003.300 276 1688 CMP M
003.301 302 310 003 1689 JNE RCK2
003.304 015 1690 DCR C
003.305 302 267 003 1691 JNZ RCK1
1692 WAIT M CYCLES
1693 * HAVE KEY VALUE
1694
003.310 167 1695 RCK2 MOV M,A
003.311 356 376 1696 XRI 3760
003.313 017 1697 RRC
003.314 322 326 003 1698 JNC RCK3
003.317 017 1699 RRC
003.320 017 1700 RRC
003.321 017 1701 RRC
003.322 017 1702 RRC
003.323 322 267 003 1703 JNC
003.326 107 1704 RCK3 MOV 8,A
003.327 076 002 1705 A,4/2
003.331 315 140 002 1706 CALL HORN
003.334 170 1707 MOV A,8
003.335 346 017 1708 ANI 170
003.337 301 1709 POP B
003.340 341 1710 POP H
003.341 311 1711 RET
RETURN

```

DISPLAY SEGMENT CODING:

```

1715 **
1716 *
1717 *
1718 *
1719 *
1720 *
1721 *
1722 *
1723 *
1724 *

```

BYTE = 76 543 210

1  
6 2  
0  
5 3  
4  
7

REGISTER INDEX TO 7-SEGMENT PATTERN

```

003.342 244 230 DS 0
003.342 244 230 DM 10011000101001008 SP
003.344 220 234 DM 10011001001000008 AF
003.346 206 215 DM 10001101100001108 BC
003.350 302 214 DM 10001100110000108 DE
003.352 222 217 DM 1000111100100108 HL
003.354 230 316 DM 11001110100110008 PC

```

OCTAL TO 7-SEGMENT PATTERN

```

003.356 001 DS 0
003.356 001 DB 0000000018 0
003.357 163 DB 011100118 1
003.360 110 DB 010010008 2
003.361 140 DB 011000008 3
003.362 062 DB 001100108 4
003.363 044 DB 001001008 5
003.364 004 DB 000001008 6
003.365 161 DB 011100018 7
003.366 000 DB 000000008 8
003.367 040 DB 001000008 9

```

I/O ROUTINES TO BE COPIED INTO AND USED IN RAM.

```

1752 **
1753 *
1754 *
1755 *
1756 *
1757 *
1758 *
1759 *
1760 *
1761 *
1762 *

```

4000A-7

PRSRM EQU \*  
DB 1  
CTLFLG DB 0  
MFLAG DB 0

REFIND  
CTLFLG  
MFLAG

RAM8GO - H8 FRONT PANEL MONITOR #01.02.00. Unix HBASH V1.4.1 5-Jul-80 Page 42  
CONSTANTS AND TABLES. IORDM 16:53:23 11-SEP-80

Address	DB	DM.RR	DSPMOD	DISPLAY REGISTER	/PAM8GO	04MAR80/
003.374 002	08	0	DSPROY	REGI	Show	*SP#
003.375 000	08	0				/Ram8Go 2/
003.376 000	08	0				
003.377 311	08	MI.REY				
006.000	1767					
	1768					ERRNZ #-4000A

XINIT1 /RAM8GO JUN80/

XINIT1 - SIZE MEMORY

1772 \*\*  
1773 \*

1774 \* XINIT1 IS JUMPED TO DURING PAM8'S MEMORY SIZING  
1775 \* THIS ROUTINE DIFFERS FROM THE STANDARD PAM8 FUNCTION  
1776 \* IN THAT IT IS NON-DESTRUCTIVE TO WHAT MAY BE RAM BELOW  
1777 \* 040000A, AND IT WILL NOT WRAP-AROUND IN A 64K RAM SYSTEM  
1778 \*

1779 \* ENTRY JUMPED TO FROM OLD INIT1

1780 \* (DE) = SEARCH INCREMENT

1781 \* (HL) = FIRST RAM SEARCH LOCATION

1782 \* EXIT (HL) = FIRST LOCATION WHERE NO RAM FOUND

1783 \* (OR ZERO IF RAM THROUGH 64K)

1784 \* (E) = 0. AS REQUIRED

1785

004.000 176 XINIT1 MOV A,M GET THE VALUE OF THE CURRENT TRIAL ADDRESS  
004.001 065 DCR M ATTEMPT TO CHANGE IT  
004.002 276 CMP M COMPARE IT TO ITS OLD VALUE  
004.003 167 MOV M,A RESTORE OLD VALUE  
004.004 312 117 000 JZ INIT2 THERE WAS NO CHANGE => NO RAM  
004.007 031 DAD D INCREMENT THE SEARCH ADDRESS  
004.010 322 000 004 JNC XINIT1 HAS NOT WRAPPED AROUND  
004.013 303 117 000 JMP INIT2 BACK INTO INLINE CODE

```

1797 ** XINIT - EXTENDED INITIALIZATION /Ram8Go 2/
1798 *
1799 * DECIDE IF THERE IS RAM AT ZERO,
1800 * IF THERE IS, THEN COPY RAM FROM PANEL AND H17 ROM TO
1801 * APPROPRIATE POSITIONS
1802 * JUMP BACK TO INLINE INIT
1803 *
1804 * Modified to only do one move directly to RAM. /Ram8Go 2/
1805 *
1806 * ENTRY (DE) = RAM8GO /Ram8Go 2/
1807 *
1808 * EXIT (DE) = PRSRAM
1809 * (HL) = PRSRAM+PRSL-1
1810 * RAM AT ZERO SET UP IF PRESENT
1811 *
1812
1813 H17ROM EQU 030000A H17 Rom Address
1814 H17ROML EQU 2*1024 Length of H17 ROM
1815
1816 XINIT XRA A Initialize the flag
1817 STA CTFILG2
1818
1819 * Copy check routine to RAM
1820
1821 MVI C,XINAL
1822 LXI D,XINA
1823 LXI H,XINB
1824 XINI D LDAX D
1825 MOV M,A
1826 INX D
1827 INX H
1828 DCR C
1829 JNZ XINI
1830
1831 * Check for RAM at Zero
1832
1833 LXI H,RAM8GO
1834 LDA CTFILG2
1835 MOV B,A Save original in B
1836 ORI OP-CTL2 Turn on RAM at Zero
1837 LXI D,XIN2 DE = return address
1838 JMP XINB
1839 XIN2 JZ XIN5 No change with decrement
1840
1841 * Copy ROM to RAM
1842
1843 LXI B,RAM8GOL Length to Copy
1844 LXI D,RAM8GO
1845 XIN3 D Move RAM8GO into place
1846 STAX D
1847 INX D
1848 DCX B
1849 MOV A,B
1850 ORA C
1851 JNZ XIN3 Not all moved yet
1852
030.000
010.000
004.016 257
004.017 062 066 040
004.022 016 012
004.024 021 146 004
004.027 041 004 040
004.032 032
004.033 167
004.034 023
004.035 043
004.036 015
004.037 302 032 004
004.042 041 000 000
004.045 072 066 040
004.050 107
004.051 366 362
004.053 021 061 004
004.056 303 004 040
004.061 312 135 004
004.064 001 000 010
004.067 021 000 000
004.072 032
004.073 022
004.074 023
004.075 013
004.076 170
004.077 261
004.100 302 072 004
    
```

```

1853 * Copy H17 ROM to its final resting place (RIP)
1854
004.103 001 000 010 LXI 8,H17ROML
004.106 041 000 030 LXI H,H17ROM
004.111 032 1857 XIN4 Move H17 ROM into place
004.112 167 MOV M+A
004.113 023 INX D
004.114 043 INX H
004.115 013 DCX B
004.116 170 MOV A,B
004.117 261 ORA C
004.120 302 111 004 JNZ XIN4 Not all moved yet
1865
004.123 072 066 040 LDA CTLFLG2
004.126 366 040 ORI CBZ.ORG
004.130 062 066 040 STA CTLFLG2
004.133 323 362 OUT OP.CTL2 Turn on Ram at 0
1870
004.135 021 371 003 LXI D,PRSRROM RESTORE NORMAL VALUES
004.140 041 012 040 LXI H,PRSRROM+PRSL-1
1873
004.143 303 073 000 JMP INIT RETURN TO INLINE CODE
1875
004.146 323 362 OUT OP.CTL2 Select RAM
004.150 176 MOV A,M
004.151 065 DCR H
004.152 276 CMP M check for a change
004.153 170 MOV A,B
004.154 323 362 OUT OP.CTL2 Select ROM
1881
004.156 353 XCHG
1883
004.157 351 PCHL
1884 XINAL EQU *-XINA
000.012

```



1887	***	Extended Command Table
1888	*	
1889		
004.160	306 004	EXTCMD ADI 4
004.162	207	ADD A A = 2 * A
004.163	021 177 004	LXI D,EXTCMDA
004.166	157	MOV L,A
004.167	046 000	MVI H,0
004.171	031	DAD D
004.172	176	MOV A,H
004.173	043	INX H
004.174	146	MOV H,H
004.175	157	MOV L,A
004.176	351	PCHL
1901		
004.177	322 000	EXTCMDA DM ERROR
004.201	253 004	DM PRI800
004.203	236 004	DM SEC800
004.205	322 000	DM ERROR

1907	**	AUTOB - Auto Boot
1908	*	
1909	*	AUTOB performs an auto boot of the primary device.
1910	*	
1911	*	ENTRY: NONE
1912	*	
1913	*	EXIT: To PRI800
1914	*	
1915	*	USES: ALL
1916	*	
1917		
004.207	041 010 040	AUTOB LXI H,MFLAG
004.212	176	MOV A,H
004.213	346 275	ANI 3770-U0,DDU-U0,NFK
004.215	167	MOV M,A
004.216	043	INX H
000.000		ERRNZ GTFLG-MFLAG-1
004.217	066 360	MVI M,CB,SSI,CB,MTL+CB,CLI+CB,SPK
004.221	076 377	MVI A,-1
004.223	062 006 040	STA DSPROT
004.226	373	EI
004.227	052 035 040	LHLD REGPTR
004.232	371	SPHL
004.233	303 253 004	JMP PRI800

\*0\* Illegal  
 \*1\* -> Primary Boot  
 \*2\* -> Secondary Boot  
 \*3\* Illegal

HL = Processor Address  
 Enter Processor

Enable Display Updates, and Re-Fresh

All Periods OFF

doot.PRI800 device

```

1933 *** PRI800 - Primary Boot /Ram8Go 2/
1934 *
1935 *
1936 *
1937 *
1938 *
1939 *
1940 *
1941 *
1942 *
1943 *
1944 *
1945 SEC800 XRA A
1946 SEC800 STA AIO:UNI Zero Boot Unit
1947 LXI B,MSGSEC
1948 IN IP:CON
1949 CMA
1950 JMP 8001 Invert Primary Flag
1951 Boot Secondary Device
1952 PRI800 XRA A
1953 PRI800 STA AIO:UNI
1954 LXI B,MSGPRI
1955 IN IP:CON
1956
1957 8001 LXI SP,STACK Initialize the stack-pointer
1958 ANI CN:PRI
1959 IN IP:CON
1960 PUSH PSW
1961 JZ 8002 174 is the device to boot
1962
1963 * Boot Device is 170
1964
1965 MVI A,1700 Save Boot Device Address
1966 STA BDA
1967 POP PSM
1968 ANI CN:170H Mask Device Type
1969 JZ BERR No Device Installed at 170
1970 ERRNZ CND:NDI No-Device-Installed Flag
1971 RRC
1972 RRC Device Type converted to index
1973 JMP 8003
1974
1975 * Boot Device is 174
1976
1977 8002 MVI A,1740 Save Boot Device Address
1978 STA BDA
1979 POP PSM
1980 ANI CN:174H Mask out device type
1981
1982 * Initialize Vectors and Display
1983
1984 8003 PUSH PSW Save Device Index
1985 PUSH B
1986
1987 MVI A,CB:SSI+CB:CLI+CB:SPK Turn off monitor mode
1988 STA CTLFLG
    
```

```

1989
004.336 076 007 HVI A,7
004.340 041 037 040 LXI H,UIVEC
004.343 066 303 8004 M,MI.JMP Stuff Interrupt Vectors
004.345 043 INX H
004.346 066 002 M,#EIRET
004.350 043 INX H
004.351 066 007 HVI M,EIRET/256
004.353 043 INX H
004.354 075 DCR A
004.355 302 343 004 JNZ 8004
.....
004.360 257 XRA A
004.361 062 122 041 2002 STA TIMEOUT Zero Time-Out Counter
004.364 041 031 034 LXI H,ROMCLK M17 Rom Clock Routine
004.367 042 124 041 2004 SHLD USRCLK
004.372 041 221 005 LXI H,CLKINT
004.375 042 040 040 2006 SHLD UIVEC+1 Initialize Clock Interrupt Vector
.....
005.000 001 132 037 LXI B,800TA
005.003 021 110 040 LXI D,D.COM
005.006 315 151 007 2010 CALL SMOV
005.011 130 2011 DB 800TAL
.....
005.012 041 240 040 2012 LXI H,D-RAM
005.015 006 037 2014 MVI B,D-RAML
005.017 315 323 007 2015 CALL $ZERO Zero Memory
.....
005.022 072 010 040 2017 LDA .MFLAG
005.025 366 003 2018 ORI UO.CLK+UO.DDU Enable Clock Int. turn off Display Update
005.027 062 010 040 2019 STA .MFLAG
.....
005.032 301 2021 POP B
005.033 021 013 040 2022 LXI D,FPLEDS
005.036 315 151 007 2023 CALL SMOV
005.041 003 2024 DB MSGLEN
005.042 056 006 2025 MVI L,9-MSGLEN
005.044 076 377 2026 MVI A,-1
005.046 022 2027 8005 STAX D Blank some
005.047 023 2028 INX D
005.050 055 2029 DCR L
005.051 302 046 005 2030 JNZ 8005
.....
005.054 361 2031 POP PSM
005.055 021 101 005 2033 LXI D,8006
005.060 325 2034 PUSH D Force Boot to return to 8006
.....
005.061 062 121 041 2036 STA 80F Save Boot Device Flag
005.064 207 2037 ADD A A = 2 + A
005.065 157 2038 MOV L,A
005.066 046 000 2039 MVI H,0
005.070 021 125 005 2040 LXI D,800A
005.073 031 2041 DAD D
005.074 176 2042 MOV A,H
005.075 043 2043 INX H
005.076 146 2044 MOV H,M
    
```

```

005.077 157      MOV      L,P,A      HL = Device Processor Address
005.100 351      PCHL
.....
005.101 072 010 040 LDA      .MFLAG
005.104 346 375 ANI      3770-U0,DDU      Turn on Display Update
005.106 062 010 040 STA      .MFLAG      Restore original front panel mode
005.111 052 124 041 LHLD     USRCLK
005.114 042 040 040 SHLD     UIVEC+1      Clear Time-Out Vector to just user vector
005.117 332 322 000 JC       ERROR      Boot Routines return here
.....
005.122 303 200 042 JMP      USERFWA
.....

```

```

.....
2057 **      Device Processors
2058 *
2059
2060 800A EQU *
2061
2062 ERRNZ *-B00A/2-CND.H17
2063 DW      8H17
2064
2065 ERRNZ *-B00A/2-CND.H47
2066 DW      8H47
2067
2068 DW      BERR      Illegal Device
2069 DW      BERR
2070
2071
2072 MSGPRI DB      10011008,110111108,110111118 *Pri*
2073 MSGLEN EQU *--MSGPRI
2074
2075 MSGSEC DB      101001008,100011008,100011018 *SEC*
2076 ERRNZ *-MSGSEC-MSGLEN
.....

```

```

2080 ** BERR - Boot Error
2081 *
2082 * BERR handles boot errors.
2083 *
2084
005.143 072 010 040 BERR LDA .MFLAG
005.146 366 002 086 ORI UO.DDU Disable Display Update.
005.150 062 010 040 STA .MFLAG
2088
005.153 001 210 005 LXI B,BERRA
005.156 021 013 040 LXI D,FPLEDS
005.161 315 151 007 CALL SMOV Set up Error Message in LED's
005.164 011 2092 DB BERRAL
2093
005.165 001 000 000 LXI B,BERRB BC = Time-Out Count
005.170 013 2095 BERRI DCX B
005.171 170 2096 MOV A,B
005.172 261 2097 ORA C
005.173 312 322 000 JZ ERROR Done displaying message
2099
005.176 333 360 2100 IN IP.PAD
005.200 376 157 2101 CPI K.STAR *
005.202 312 322 000 JZ ERROR Cancel was hit
005.205 303 170 005 JMP BERRI
2104
005.210 206 2105 BERRA DB 3770-50-53-54-55-56 b
005.211 306 2106 DB 3770-50-53-54-55 o
005.212 306 2107 DB 3770-50-53-54-55 o
005.213 362 2108 DB 3770-50-52-53 t
005.214 377 2109 DB 3770 t
005.215 377 2110 DB 3770
005.216 214 2111 DB 3770-50-51-54-55-56 E
005.217 336 2112 DB 3770-50-55 F
005.220 336 2113 DB 3770-50-55 F
000.011 2114 BERRAL EQU *-BERRA
2115
000.000 2116 BERRB EQU 0 Time-Out Count (Full wrap)
    
```

```

2119 *** CLKINT - Clock Interrupt Processor
2120 *
2121 * CLKINT processes the clock interrupts by:
2122 *
2123 *   Checking for abort
2124 *   Checking for Time-Out
2125 *   Passing the Interrupts on to the user
2126 *
2127 *   This clock routine is only to be used at boot
2128 *   time.
2129 *
2130
2131 CLKINT   PUSH   PSM
2132 IN       IP-PAD
2133 CPI      K-STAR
2134 JZ       ERROR
2135
2136 LDA      TICCNT
2137 ANA     A
2138 JNZ     CKI3
2139
2140 LDA      TIMEOUT
2141 INR     A
2142 STA     TIMEOUT
2143 CPI     30
2144 JC      CKI3
2145
2146 *   Time-Out Error
2147
2148 LDA      BDF
2149 CPI     CMD.HI7
2150 JNZ     CKI1
2151
2152 *   Abort HI7
2153
2154 XRA     A
2155 STA     D-DLYMD
2156 LDA     D-DVCTL
2157 ANI     DF-MR
2158 STA     D-DVCTL
2159 OUT     DP-DC
2160 JMP     CKI2
2161
2162 *   Abort H47
2163
2164 CPI     CMD.H47
2165 JNZ     CKI2
2166 CALL    OBD.
2167 DB     M-RES,D-STAI
2168 ERRNZ  CKI2-*
2169
2170 *   Restore User Clock Vector
2171
2172 LHL    USRCLK
2173 SHLD  UIVEC+1
2174 EI
    
```

```

005.326 303 143 005 2175 JMP BERR boot Time-Out Error
                2176
005.331 361 2177 CKI3 POP PSM
005.332 345 2178 PUSH H
005.333 052 124 041 2179 LMLD USRCLK
005.336 343 2180 XTFL
005.337 311 2181 RET
Enter User's Clock Routine

```

RAM8CO - H8 FRONT PANEL MONITOR #01.02.00.  
H89 COM/DAT

/Ram8Go 2/

H89 COM/DAT

2184 \*\*\*

2185 \*

2186 \*

2187 \*

2188 \*

2189 \*

2190 .

2191 .

2192 .

2193 H89DAT

2194 JMP

2195 .

2196 .

2197 .

2198 H89COM

303 361 006

303 334 006

006.023

000.063

005.340

006.023

006.027

000.001

006.026

006.027

000.001

006.026

006.027

000.001

006.026

006.027

000.001

006.026

006.027

000.001

006.026

006.027

000.001

006.026

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006.027

000.001

006.026

006.027

000.001

006.026

006.027

000.001

006.026

006.027

000.001

006.026

006.027

000.001

006.026

H89COM and H89DAT are provided as common entry points  
between HIR-89 and RAM8CO.

SET 6023A

ERRMI .--

DS .--

H89DAT JMP DAT.

SET 6027A

ERRMI .--

DS .--

H89COM JMP COM.



```

2201 **      BH17 - Boot H17                               /Ram8Go 2/
2202 *
2203 *      BH17 boots the specified unit of an H-17 disk. The
2204 *      unit to boot is specified in AIO.UNI.
2205 *
2206 *      ENTRY: AIO.UNI = Unit of H-17 to boot.
2207 *      all H-17 Ram Vectors Initialized
2208 *
2209
2210 BH17      LXI      B,BH17A
2211          LXI      D,FPLEDS*3+2
2212          CALL    SMOV
2213          DB      BH17AL
2214
2215          XRA      A
2216          OUT    DP,DC      Turn off disk
2217
2218          LXI      H,R:SDP
2219          SHLD   D,SDP+1    Re-Vector set device parameter for SY2:
2220
2221          MVI      E,10
2222          CALL    BH174      Watch for 10 holes
2223          ANI      DF,HD      Watch inter-hole gap
2224          JZ      BH171
2225          CALL    BH174      Watch entire hole
2226          ANI      DF,HD
2227          JNZ    BH172
2228          DCR      E
2229          JNZ    BH171      Find another hole
2230
2231          CALL    D,ABORT
2232          LXI      D,USERFWA
2233          LXI      H,0
2234          CALL    D,READ
2235          JC      BH170      Error Reading Sectors, keep trying
2236
2237          RET
2238
2239
2240 BH174     LDA      AIO.UNI
2241          MOV      B,A
2242          INR      B
2243          XRA      A
2244          CALL    BITS      Select device
2245          ERNZ   DF,D50-2
2246          ERNZ   DF,D51-4
2247          ERNZ   DF,D52-8
2248          ORI    DF,HD
2249          OUT    DP,DC      Turn on motor and drive select
2250          IN     Op,DC      Look at the drive status
2251          RET
2252
2253 BH17A     DB      3770-S0-S2-S3-S5-S6  'H'
2254          DB      3770          'H'
2255          DB      3770-S2-S3    '1'
2256          DB      3770-S1-S2-S3 '7'
    
```



```

2260 **      BH47      - Boot H47
2261 *
2262 *      BH47 boots the specified unit of an H-47 disk. The
2263 *      unit to boot is specified in A10.UNI.
2264 *
2265 *      ENTRY: A10.UNI = Unit of H-47 to boot.
2266 *      all H-17 Ram Vectors initialized.
2267 *
2268
006.152 001 324 006      BH47      LXI      B,BH47A
006.155 021 020 040      LXI      D,FPLEDS+3+2
006.160 315 151 007      CALL     MOV
006.163 004
006.164 315 200 006      BH471     CALL     BH472
006.167 320
006.170 076 372
006.172 315 053 000      MVI      A,500/2
006.175 303 164 006      CALL     DLY
006.176 303 164 006      JMP      BH471
006.177
006.178
006.179
2270
2271
2272
2273
2274
2275
2276
2277
2278
2279
2280
2281 **      BH472
2282 *
2283
2284 *      Wait for Done
2285
2286 BH472     CALL     OSD.
2287 DB      M,RES,D,STAI
2288 CALL     MDN
2289 RC
2290
2291 *      Wait for Device Ready
2292
2293 BH473     CALL     RRDY
2294 RC
2295 CALL     RRDY      L = Ready Bits
2296 RC
2297
2298 LDA      A10.UNI
2299 MOV     B,A
2300 XRA     A
2301 CALL    BITS
2302 ANA     L
2303 JNZ     BH473
2304
2305 *      Boot the Device
2306
2307 CALL     COM
2308 DB      DD,LSC
2309 RC
2310 CALL    DAT
2311 DB      0
2312 RC
    
```

Output Load Sector Count Command  
 Output data

```

006.247 315 355 006 2313 CALL DAT Transfer count of 2
006.252 002 2314 DB 2
006.253 330 2315 RC
006.254 315 167 007 2316 CALL WDN
006.257 330 2317 RC Try again
006.260 315 330 006 2319 CALL COM Output Read Command
006.263 007 2320 DB DO-REAB
006.264 330 2321 RC
006.265 315 355 006 2322 CALL DAT Track Number
006.270 000 2323 DB 0
006.271 330 2324 RC
006.272 072 061 041 2325 LDA AIO.UNI
006.275 017 2326 RRC
006.276 017 2327 RRC
006.277 017 2328 RRC
000.000 ERRNZ UNT.M-01100000B Start at sector 1
006.300 366 001 2329 ORI 1
000.000 ERRNZ SEC.M-00011111B
006.302 315 361 006 2332 CALL DAT.
006.305 330 2333 RC
006.306 021 200 042 2334 LXI D,USERFHA
006.311 315 066 007 2335 CALL P1M BH474
006.314 332 167 007 2337 JC WDN Pre-Mature DONE means end, error set if S.ERR
006.317 022 2338 STAX D
006.320 023 2339 INX D
006.321 303 311 006 2340 JMP BH474 Get another byte
006.324 222 2341
006.325 377 2342 BH47A DB 3770-S0-S2-S3-S5-S6 'HV'
006.326 262 2343 DB 3770 DB 3770
006.327 361 2344 DB 3770-S0-S2-S3-S6 '4V'
000.004 2345 DB 3770-S2-S3-S1 '7'
000.004 2346 BH47AL EQU *-BH47A

```

RAM8GO - H8 FRONT PANEL MONITOR #01.02.00. Unix HBASM V1.4.1 5-Jul-80 Page 58  
 Subroutines COM 16:53:52 11-SEP-80 /Ram8Go 2/

```

2350 ** COM - Command
2351 *
2352 * COM output a command byte.
2353 *
2354 * ENTRY: *(RET+1)= Command byte
2355 *
2356 * EXIT: PSM = 'C' Set if ERROR
2357 *          'C' Clear if NO error
2358 *
2359 * USES: PSM,BC
2360 *
2361 *
2362 * XTHL
2363 * MOV A,M A = command byte
2364 * INX H
2365 * XTHL Restore return address
2366 *
2367 * COM.
2368 * CALL MDM PSM
2369 * JC COM1 Error
2370 * POP PSM
2371 * CALL '080 Output to data port
2372 * DB O-DATI
2373 * ANA A
2374 * RET
2375 *
2376 * COM1 INX SP Ignore saved PSM
2377 * INX SP
2378 * RET

2380 ** DAT - Data
2381 *
2382 * DAT outputs data to the boot H47 with a DFR handshake.
2383 *
2384 * ENTRY: *(RET+1)= data to output
2385 *
2386 * EXIT: To RET+1
2387 *
2388 * USES: PSM,BC
2389 *
2390 *
2391 * XTHL
2392 * MOV A,M A = Data
2393 * INX H
2394 * XTHL
2395 *
2396 * DAT.
2397 * CALL MTR PSM
2398 * JC DAT1 Error
2399 * POP PSM
2400 * CALL '080 Output to Data Port
2401 * DB O-DATI
2402 * ANA A

```

```

006.376 311      2403      RET
006.377 063      2404      INX      SP
007.000 063      2405      DAT1     Discard Saved Data
007.001 311      2406      INX      SP
007.002 373      2407      RET
    
```

```

007.003 311      2409      EIRET    - EI RETURN /Ram860 2/
007.004 311      2410      *
007.005 311      2411      * EIRET is a simple routine which Re-Enables Interrupts,
007.006 311      2412      * and executes a RETURN instruction.
007.007 311      2413      *
007.008 311      2414      *
007.009 311      2415      EIRET    EI
007.010 311      2416      RET
    
```

```

007.011 311      2418      * IBD - Input from Boot Device /Ram860 2/
007.012 311      2419      *
007.013 311      2420      * IBD inputs data from the Boot Port as saved at boot time.
007.014 311      2421      *
007.015 311      2422      * ENTRY: BDA = Boot Device Address
007.016 311      2423      * *(RET+1) = Port Index
007.017 311      2424      *
007.018 311      2425      * EXIT: A = Data Input from port
007.019 311      2426      * IOMRK destroyed
007.020 311      2427      *
007.021 311      2428      * USES: PSM
007.022 311      2429      *
007.023 311      2430      *
    
```

```

007.024 311      2431      IBD
007.025 311      2432      XTHL    PSM
007.026 311      2433      PUSH   D
007.027 311      2434      MOV    D,M      D = Port Index
007.028 311      2435      INX    H
007.029 311      2436      LDA    BDA
007.030 311      2437      ADD    D
007.031 311      2438      XCHG
007.032 311      2439      MOV    H,A      H = Actual Output Address
007.033 311      2440      MVI    L,MI+IN  L = MI+IN
007.034 311      2441      SHLD  IOMRK    Stuff Instruction and Port
007.035 311      2442      XCHG
007.036 311      2443      POP    D
007.037 311      2444      POP    PSM
007.038 311      2445      XTHL
007.039 311      2446      JNP    IOMRK    Do the actual input
    
```

```

2448 **      08D      - Output to Boot Device      /Ram8Go 2/
2449 *
2450 *      08D outputs the data to the indexed Boot Device.
2451 *
2452 *      ENTRY:  BDA      = Boot Device Address
2453 *              *(RET+1) = Port Address Index
2454 *
2455 *      EXIT:   IOWRK destroyed
2456 *              Data output to the port
2457 *
2458 *      USES:   PSM, IOWRK
2459 *
2460
2461 08D.      XTHL
2462 MOV      A,M      A = data byte to output
2463 INX      H
2464 XTHL
2465
2466 08D
2467 XTHL      XTHL
2468 PUSH     PSW
2469 MOV      D,M      D = Port Index
2470 INX      H
2471 LDA      BDA      A = Boot Device Address
2472 ADD      D
2473 XCHG
2474 MOV      M,A      H = Actual Device address
2475 MVI      L,MI.OUT L=MI.OUT
2476 SLD      IOWRK    Stuff Instruction and address
2477 XCHG
2478 POP      D
2479 POP      PSW
2480 XTHL
2481 JMP      IOWRK    Do the actual I/O
    
```

```

2483 **      PIN      - Port In      /Ram8Go 2/
2484 *
2485 *      PIN inputs a byte of data from the H-47 with
2486 *      a data-transfer-ready handshake.
2487 *
2488 *      ENTRY:  NONE
2489 *
2490 *      EXIT:   PSM      = 'C' Set if ERROR
2491 *              'C' Clear if NO error
2492 *              A      = data
2493 *
2494 *      USES:   PSM
2495 *
2496
2497 PIN      CALL     IBD
2498 DB
2499 ANI      S.DIR+S.DDM
2500 JZ       PIN      Not done, and not ready to transfer
    
```

```

2501 .....
007.077 346 040 ANI S.00N
007.101 067 STC
007.102 300 RNZ Error because done before DTR
2505 .....
007.103 315 004 007 CALL IBD
007.106 001 08 D.DATI
007.107 247 ANA A
007.110 311 RET

```

R.SDP - Set-Up Device Parameters /Ram8Go 2/

```

2511 ** R.SDP sets up arguments for the specific unit.
2512 *
2513 *
2514 *
2515 * D.DVCTL = Motor ON
2516 * D.TRKPT = Address of device track number
2517 *
2518 * Modified to access drive 3, or SY2:.
2519 *
2520 * ENTRY: AIO.UNI = Unit Number
2521 *
2522 * EXIT: HL = D.TRKPT
2523 *
2524 * USES: PSM,HL
2525 *
2526 *
2527 R.SDP

```

```

007.111 076 012 MVI A,ERTCNT
007.113 062 264 040 STA D.OECNT Set the max error count for the operation
007.116 072 061 041 LDA AIO.UNI
007.121 365 PUSH PSM
007.122 376 002 CPI 1+1
2532 JC R.SDP. Unit 0 or 1
007.124 332 073 036 JCN DF.DS0-2
000.000 ERRNZ DF.DS1-4
000.000 ERRNZ DF.DS1-4
2536 MVI A,3 Unit 2
007.127 076 003 ERRNZ DF.DS2-8
000.000 JMP R.SDP.
007.131 303 073 036

```

```

2541 ** RRDY - Read Ready /Ram8Go 2/
2542 *
2543 * RRDY checks to see if the drive specified in
2544 * AIO.UNI is ready.
2545 *
2546 * ENTRY: AIO.UNI = unit number
2547 *
2548 * EXIT: L = Ready Bits
2549 *
2550 * USES: PSM,L

```



```

2551 *
2552
007.134 315 330 006 RRDY CALL COM
007.137 020 2553 RRDY DB DD.RRDY
007.140 315 066 007 2554 CALL PIN
007.143 330 2555 RC
007.144 157 2556 L,A L=Ready Bits
007.145 315 167 007 2557 CALL WDN
007.150 311 2558 RET Unit return ERROR
2559
    
```

```

2561 ** SMOV - Short Move /Ram8Go 2/
2562 *
2563 * SMOV performs a short (<256) byte move)
2564 *
2565 * ENTRY: BC = source
2566 * DE = destination
2567 * RET = byte count
2568 *
2569 * EXIT: RET+1
2570 *
2571 * USES: PSM,BC,DE,L
2572 *
2573
    
```

```

007.151 343 XTHL
007.152 176 MOV A,M
007.153 043 INX H
007.154 343 XTHL
007.155 157 MOV L,A L = Byte Count
2578
2579
007.156 012 LDAX B
007.157 022 STAX D
007.160 003 INX B
007.161 023 INX D
007.162 055 DCR L
007.163 302 156 007 2584 JNZ SMOV. Move more bytes
2585
007.166 311 RET
2586
2587
    
```

```

2589 ** WDN - Wait for Done /Ram8Go 2/
2590 *
2591 * WDN waits for the done bit to be set. A time-out
2592 * is kept track of in order that the command may be
2593 * re-tried.
2594 *
2595 * ENTRY: NONE
2596 *
2597 * EXIT: PSM = %C set if there is an error or time-out
2598 * %C clear if no error
2599 *
2600 * USES: PSM,BC
    
```

```

2601 *
2602
007.167 001 000 175 2603 WDN LXI B,WDNA
007.172 013 2605 WDN1 DCX B
007.173 170 2606 MOV A,8
007.174 261 2607 ORA C
007.175 067 2608 STC
007.176 310 2609 RZ
007.177 315 004 007 2610 CALL IBD
007.202 000 2611 DB D,STAI
007.203 346 040 2613 ANI S,DDN
007.205 312 172 007 2614 JZ WDN1
007.210 315 004 007 2616 CALL IBD
007.213 000 2617 DB D,STAI
007.214 346 001 2618 ANI S,ERR
007.216 067 2619 STC
007.217 300 2620 RNZ
007.220 247 2621 ANA A
007.221 311 2622 RET
175.000 2624 EQU 32000
2625 WDNA EQU 32000
Time-Out Counter

```

```

2627 ** WTR - Wait for Transfer Request /RamGo 2/
2628 *
2629 * WTR waits for a transfer request. It checks for DONE
2630 * first, and if it is found, flags an error. The code
2631 * will also time-out waiting for $5.DIR$.
2632 * ENTRY: NONE
2633 *
2634 * EXIT: PSM = 'C' set if ERROR
2635 * 'C' clear if NO error
2636 *
2637 * USES: PSM,BC
2638 *
2639 *
2640
007.222 001 000 175 2641 WTR LXI B,WTRA
007.225 315 004 007 2643 WTRI CALL IBD
007.230 000 2644 DB D,STAI
007.231 346 040 2645 ANI S,DDN
007.233 067 2646 STC
007.234 300 2647 RNZ
007.235 013 2648 DCX B
007.236 170 2649 MOV A,8
007.237 261 2650 ORA C
007.240 067 2651 STC
007.241 310 2652 RZ
2653
Time-out ERROR

```

RAM80 - H8 FRONT PANEL MONITOR #01.02.00. Unix HBASH V1.4.1 5-Jul-80 Page 64  
Subroutines WTR 16:53:59 11-SEP-80

007.242	315	004	007	CALL	IBD	2654
007.245	000			DB	D-STAI	2655
007.246	346	Z00		ANI	S-DTR	2656
007.250	312	225	007	JZ	MTR1	2657
						2658
						2659
007.253	311			RET		2660
						2661
175.000				EQU		2662
				WTRA		32000
					Time-Out count	

```

2666 ** PATCH1 /Ram8Go 2/
2667 *
2668 * PATCH1 replaces code which initially only initialized
2669 * the Tape UART with code which also checks for Auto-Boot.
2670 * Since the return address is already on the stack, if
2671 * Auto-Boot is set, INIT exits to AUTO8 instead of ERROR.
2672 *
2673 *
2674 * ENTRY: NONE
2675 *
2676 * EXIT: HL = INIT exit address
2677 * Tape UART initialized
2678 *
2679 * USES: PSW,BC
2680 *
2681
007.254 PATCH1 EQU *
2682 *
2683 * Initialize LOAD/DUMP Uart
2684 *
2685
007.254 MVI A,UMI.L8+UMI.L6+UMI.L6X
007.256 OUT OP.TPC SET 8 BIT, NO PARITY, 1 STOP, X16
2688
2689 * Check for Auto-Boot
2690
007.260 LXI H,ERROR
007.263 IN OP.CTL2
007.265 ANI CN.A80
007.267 RZ No Auto-Boot
2695
007.270 LXI H,AUTO8
007.273 RET

```

```

2699 ** PATCH2 /Ram8Go 2/
2700 *
2701 * PATCH2 moves the MTR6 code out of its original place
2702 * in the ROM to permit providing for H89/H8 common PIN
2703 * routine.
2704 *
2705
007.274 PATCH2 JZ ERROR NOT ALLOWED TO ALTER STACKPOINTER
007.277 INX H
007.300 POP PSW RESTORE VALUE AND CARRY FLAG
007.301 JMP IOA INPUT OCTAL ADDRESS
2709

```

```

007.304      2712      XTEXT      BITS      /Ram8Go 2/
.....
2714X **      BITS      - BIT SET
2715X *
2716X *      BITS SETS THE SPECIFIED BIT IN THE ACCUMULATOR.
2717X *
2718X *      ENTRY: A      = ORIGINAL A
2719X *      B      = NUMBER OF BIT TO SET ( 7=HIGH,...,0=LOW )
2720X *
2721X *      EXIT: A      = ORIGINAL A WITH BIT(B) SET
2722X *
2723X *      USES: PSH
2724X *
2725X
007.304 305      2726X BITS      PUSH      B
.....
2727X
2728X      PUSH      PSH
007.305 365      2729X      MVI      A,10000000h
007.306 076 200      2730X      INR      B
007.310 004      2731X BITS1
007.311 007      2732X      DCR      B
007.312 005      2733X      JNZ      BITS1
007.313 302 311 007 2734X
.....
007.316 117      2735X      MOV      C,A
007.317 361      2736X      POP      PSH
007.320 261      2737X      ORA      C
2738X
007.321 301      2739X      POP      BC
007.322 311      2740X      RET
007.323      2741      XTEXT      ZERO      /Ram8Go 2/
.....
2743X **      $ZERO - ZERO MEMORY
2744X *
2745X *      $ZERO ZEROS A BLOCK OF MEMORY.
2746X *
2747X *      ENTRY (HL) = ADDRESS
2748X *      (B) = COUNT
2749X *      (A) = 0
2750X *      USES A9,B,F,H,L
2751X
2752X
007.323 257      2753X $ZERO      XRA      A
007.324 167      2754X      MOV      M,A
007.325 043      2755X      INX      H
007.326 005      2756X      DCR      B
007.327 302 324 007 2757X      JNZ      ZRUI      IF MORE
007.332 311      2758X      RET
.....

```



Address	Label	Value	Description
2781	**		THE FOLLOWING ARE CONTROL CELLS AND FLAGS USED BY THE KEYSET MONITOR.
040.000	ORG	40000A	8192
040.000	START	DS	DUMP STARTING ADDRESS
040.002	IOMRK	DS	IN OR OUT INSTRUCTION
040.004	XINB	EQU *	Transient Routine Area /Ram860 2/
040.004	PRSRAM	EQU *	FOLLOWING CELLS INITIALIZED FROM ROM
040.004		DS	RET
040.005	REGI	DS	INDEX OF REGISTER UNDER DISPLAY
040.006	DSPROT	DS	PERIOD FLAG BYTE
040.007	DSPMOD	DS	DISPLAY MODE
040.010	MFLAG	DS	USER FLAG OPTIONS
2797	*		SEE *UO.XXX* BITS DESCRIBED AT FRONT
2798			
040.011	CILFLG	DS	FRONT PANEL CONTROL BITS
040.012	REFIND	DS	REFRESH INDEX (0 TO 7)
000.007	PRSL	EQU *	END OF AREA INITIALIZED FROM ROM
040.013	FPLEDS	EQU *	FRONT PANEL LED PATTERNS
040.013	ALEDS	DS	ADDR 0
040.014		DS	ADDR 1
040.015		DS	ADDR 2
040.016		DS	ADDR 3
040.017		DS	ADDR 4
040.020		DS	ADDR 5
040.021	DLEDS	DS	DATA 0
040.022		DS	DATA 1
040.023		DS	DATA 2
040.024	ABUSS	DS	ADDRESS BUSS
040.026	RCKA	DS	RCK SAVE AREA
040.027	CRCSUM	DS	CRC-16 CHECKSUM
040.031	TPERRX	DS	TAPE ERROR EXIT ADDRESS
040.033	TICCNT	DS	CLOCK TIC COUNTER
040.035	REGPTR	DS	REGISETR CONTENTS POINTER
040.037	UIVEC	DS	USER INTERRUPT VECTORS
040.037		DS	JUMP TO CLOCK PROCESSOR
040.042		DS	JUMP TO SINGLE STEP PROCESSOR
040.045		DS	JUMP TO I/O 3
040.050		DS	JUMP TO I/O 4
040.053		DS	JUMP TO I/O 5
040.056		DS	JUMP TO I/O 6
040.061		DS	JUMP TO I/O 7
040.064	NMIRET	DS	Used by H-88/H-89 /Ram860 2/
040.066	CILFLG2	DS	Control byte for DPZ-CTL /Ram860 2/
2834			
2835			
2836			

```

041.120      2837      ORG      41120A
2838
041.120      2839      BDA      DS      1      Boot Device Address      /Ram8Go 2/
041.121      2840      BDF      DS      1      Boot Device Flag        /Ram8Go 2/
041.122      2841      TIMEOUT DS      1      Counter for Time-Out    /Ram8Go 2/
041.123      2842      DS      1
041.124      2843      USRCLK DS      2      Secondary User Clock for Boot /Ram8Go 2/
2844
041.126      2845      END

```

```

Assembly complete
2845 statements
0 errors detected
26126 bytes free

```





RAMSGD - H8 FRONT PANEL MONITOR #01.02.00.  
Cross Reference Table

CB2-ORG 000040	126E	1867			
CB2-SID 000100	127E				
CB2-SSI 000001	124E				
CKI1 005305	2150	2164L			
CKI2 005317	2160	2165	2168	2172L	
CKI3 005331	2138	2144	2177L		
CLK2 000234	751	753L			
CLK3 000237	747	756E			
CLK4 000313	780	796E			
CLKINT 005221	2005	2131L			
CLOCK 000201	563	564	727L		
CM-170M 000014	139E	1968			
CM-174M 000003	138E	1980			
CM-AB0 000200	143E	2693			
CM-8AU 000100	142E				
CM-HEM 000040	141E				
CM-PRI 000020	140E	1958			
CMD-H17 000000	145E	2062	2149		
CMD-H47 000001	147E	2065	2164		
CMD-MDI 000000	146E	1970			
COM 006330	2307	2319	2362L	2553	
COM 006334	2198	2367L			
COM1 006352	2369	2376L			
CRC 002347	1402L	1463			
CRC1 002356	1406L	1426			
CRC2 003004	1417	1424L			
CRC5UM 040027	1154	1192	1247	1347	1405
CRC 002172	1119	1246L	1427	1427	2818L
CTLFLG 040011	578	686	744	749	771
	1923	1988	776	823	1045
	1817	1834	1048	1057	1219
		1866	1868	1868	2834L
CTLFLG2 040066	703L	799			
CUI1 000165	304L	2231			
D-ABORT 040141	309L				
D-CDE 040160	233L	2009			
D-COM 040110	380E	2372	2401	2507	
D-DATI 000001	324L				
D-DLY 040235	263L				
D-DLYHS 040244	262L	2155			
D-DLYMO 040243	268L				
D-DRYTB 040251	310L				
D-DTS 040163	260L	2156	2158		
D-DVCTL 040242	279L				
D-E-CHK 040267	280L				
D-E-HCK 040270	278L				
D-E-HSY 040266	277L				
D-E-RDS 040265	282L				
D-E-TRK 040272	281L				
D-E-VOL 040271	276L				
D-ERR 040265	283L				
D-ERRL 040273	323L				
D-ERRT 040232	270L				
D-HECNT 040261	314L				
D-LPS 040177	312L				
D-MAI 040171	313L				
D-MAO 040174	302L				
D-MOUNT 040133	272L				
D-OECNT 040264		2528			

RAM8G0 - H8 FRONT PANEL MONITOR #01.02.00.  
Cross Reference Table

D.0PR	040273	287L			
D.0PM	040275	288L			
D.0RAM	040240	236L			
D.0RAML	000037	290E	255	290	2013
D.0RDB	040202	315L	2014		
D.0READ	040147	306L	2235		
D.0READR	040152	307L			
D.0SDP	040205	316L	2219		
D.0SDT	040166	311L			
D.0SEGMT	040262	271L			
D.0STAI	000000	379E	380	2167	2287 2498 2612 2617 2644 2656
D.0STS	040210	317L			
D.0STZ	040213	318L			
D.0SYDD	040130	301L			
D.0TRKPT	040245	265L			
D.0TS	040241	258L			
D.0TT	040240	257L			
D.0UDLY	040216	319L			
D.0VEC	040130	235L	299		
D.0VOLPT	040247	266L			
D.0MNB	040227	322L			
D.0WRITE	040155	308L			
D.0WSC	040221	320L			
D.0WSP	040224	321L			
D.0XIT	040144	305L			
D.0XOK	040136	303L			
DAT	006355	2310	2313	2322	2391L
DAT.	006361	2193	2332	2396L	
DAT1	006377	2398	2405L		
DD.0BOOT	000000	418L			
DD.0CPY	000013	429L			
DD.0DS	000202	453L			
DD.0FRM0	000014	430L			
DD.0FRM1	000015	431L			
DD.0FRM2	000016	432L			
DD.0FRM3	000017	433L			
DD.0LSC	000003	421L	2308		
DD.0RAD	000004	422L			
DD.0RAS	000002	420L			
DD.0RDL	000205	456L			
DD.0RDL	000203	454L			
DD.0REA	000005	423L			
DD.0REAB	000007	425L	2320		
DD.0RROD	000020	434L	2554		
DD.0RST	000001	419L			
DD.0SOC	000200	451L			
DD.0SFO	000020	440L			
DD.0SPF1	000021	441L			
DD.0SPF2	000022	442L			
DD.0SPF3	000023	443L			
DD.0SPF4	000024	444L			
DD.0SPF5	000025	445L			
DD.0ST	000201	452L			
DD.0MDLB	000210	459L			
DD.0WR8D	000012	428L			
DD.0MRD	000011	427L			
DD.0MRI	000006	424L			



RAM60 - HB FRONT PANEL MONITOR #01.02.00.  
Cross Reference Table

INT4	000040	595L			
INT5	000050	600L			
INT6	000060	614L			
INT7	000070	621L			
INTXIT	000172	710L	774	1050	
IOA	003062	1009	1492L	2709	
IOB	003066	903	1492	1507L	
IOB1	003070	1508L	1522		
IOWRK	040002	1024	1025	2441	2787L
IP.COM	000362	107E	1948	1955	1959
IP.PAD	000360	99E	797	1280	1309
IP.TPC	000371	103E	1311		
IP.TPD	000370	105E	1381		
K.OIVD	000117	174E			
K.DOT	000117	176E			
K.MINU	000217	172E			
K.NUMB	000057	175E			
K.PLUS	000257	171E			
K.STAR	000157	173E	2101	2133	
LAST	001150	886	983L		
LOA0	001272	1084L	1127		
LOA1	001342	1110L	1117		
LOAD	001267	1082E			
LRA	003047	919	1477L	1592	
LRA.	003052	785	1101	1171	1478L
LST2	001154	989L			
M.INI	242355	373E			
M.OUTI	243355	374E			
MEMM	001165	889	1002L		
MI.AMI	000346	207E	1270		
MI.HLT	000166	201E	791		
MI.IN	000333	203E	1018	2440	
MI.JMP	000303	204E	1992		
MI.LDA	000072	206E			
MI.LXID	000021	208E	1019		
MI.OUT	000323	205E	1020	2475	
MI.REI	000311	202E	1766		
MSGLEN	000003	2024	2025	2073E	2076
MSGPRI	005135	1954	2072L	2073	
MSGSEC	005140	1947	2075L	2076	
MTR	000344	834E	1060		
MTR1	000345	837	837L		
MTR4	001005	850	860L		
MTR5	001051	855	899L		
MTR6	001072	901	918L		
MTRA	001035	864	878E		
NEXT	001132	885	962L		
MMIRET	040064	2833L			
08D	007037	2371	2400	2466L	
08D.	007033	2166	2286	2461L	
OP.CTL	000360	100E	1047	1056	
OP.CTL2	000362	108E	1836	1869	1876
OP.DIG	000360	101E	758	1881	2692
OP.SEG	000361	102E	760		
OP.TPC	000371	104E	1145	1203	1294
OP.TPD	000370	106E	1462	1460	2687
OUT	001202	881	1020L		

RAM8GD - H8 FRONT PANEL MONITOR #01.02.00.  
Cross Reference Table

PA1CH1	007254	660	2682E				
PA1CH2	007274	921	2706L				
PIN	007066	916	2336	2497L	2500	2555	
PR1800	004253	1903	1930	1952L			
PR1800	004254	1953L	2768				
PRSL	000007	1872	2801E				
PRSKAM	040004	1872	2789E	2801			
PRSR0M	003371	1759E	1871				
R\$W	001126	888	953L				
R.SDP	007111	2218	2527L				
R.SOP	036073	155E	2533	2539			
RAM8GD	000000	548E	551	1833	1844	2776	
RAM8GD	010000	1843	2776E				
RCK	003260	847	938	1508	1677E		
RCK1	003267	1683L	1691	1703			
RCK2	003310	1689	1695L				
RCK3	003326	1698	1704L				
RCKA	040026	1681	2817L				
REFIND	040012	749	2800L				
REGI	040005	870	944	967	988	1477	2792L
REGM	001104	890	931L				
REGPTR	040035	693	825	1480	1928	2822L	
RMEM	001261	883	1066L				
RNB	002331	1110	1337	1362	1376L		
RNB1	002335	1378L	1380				
RNP	002325	1096	1106	1246	1348	1362L	
ROM800T	030000	228E					
ROMCLK	034031	156E	2003				
RRDY	007134	2293	2295	2553L			
RT.BD	000005	185E					
RT.BP	000002	182E					
RT.CT	000003	183E					
RT.MI	000001	181E	1083	1155			
RT.NB	000004	184E					
RT.PD	000006	186E					
S.DDM	000040	383E	2499	2502	2613	2645	
S.DTR	000200	385E	2499	2657			
S.ERR	000001	382E	2618				
S.GRT0	024000	224E					
S.GRT1	025000	225E					
S.GRT2	026000	226E					
S.IEM	000100	384E					
S.INT	040343	238L					
S.SOVR	041146	240L	242				
S.SW0	000002	387E					
S.SW1	000004	388E					
S.SW2	000010	389E					
S.SW3	000020	390E					
S.VAL	040277	237L					
S0	000001	160E	2105	2106	2107	2108	2113
S1	000002	161E	2111	2256	2345	2111	2112
S2	000004	162E	2108	2253	2255	2256	2253
S3	000010	163E	2105	2106	2107	2108	2113
S4	000020	164E	2105	2106	2107	2108	2113
S5	000040	165E	2105	2106	2107	2111	2112
S6	000100	166E	2105	2111	2253	2342	2342
S7	000200	167E	2105	2111	2253	2342	2344

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Cross Reference Table

SAE	001063	912L	963	984	1028
SAVALL	000132	561	576	677L	
SB*BT0	000001	404E			
SB*CR0	000010	401E			
SB*DL0	000040	399E			
SB*ILC	000002	403E			
SB*LTD	000004	402E			
SB*MR0	000020	400E			
SB*UMR	000200	397E			
SB*MPD	000100	398E			
SC*UART	000372	501E			
SEC*M	000037	480E	2331		
SEC800	004236	1904	1945L		
SEC800*	004237	1946L	2770		
SID*0	000000	473E	476		
SID*1	000200	474E	476		
SID*M	000200	476E			
SINCR	004000	642E	644		
SMOV	007151	2010	2023	2091	2212 2271 2574L
SMOV*	007156	2580L	2585		
SRS	002265	1084	1333E		
SRS1	002265	1334L	1342	1346	
SRS2	002271	1337L	1340		
SSIZ*M	004000	484E			
SST1	001235	618	1048L		
SSTEP	001225	882	1043E		
STACK	042200	244E	1957		
STACKL	001032	242E			
START	040000	645	1108	1157	2786L
STPRIN	001244	579	1054E		
SYDD	040130	234E			
TD*IN	000370	194E			
TD*OUT	000370	195E			
TER1	002220	1278L	1285		
TER3	002215	1271L	1282		
TFT	002133	1126	1202L	1266	
TICCNT	040033	727	729	764	1223 1283 2136 2820L
TIMEOUT	041122	2002	2140	2142	2841L
TPABT	002244	1066	1141	1293L	
TPERR	002205	1095	1264L		
TPERRX	040031	1067	1142	1313	2819L
TPXIT	002252	1279	1309L	1378	1456
TS*IN	000371	196E			
TS*OUT	000371	197E			
UCI*ER	000020	523E	1376	1459	
UCI*IE	000002	525E			
UCI*IR	000100	521E			
UCI*RE	000004	524E	1376		
UCI*RO	000040	522E	1376		
UCI*TE	000001	526E	1144	1459	
UDR	000000	498E			
UF*FCT	000100	358E			
UF*RDA	000001	355E			
UF*RR0	000002	356E			
UF*RPE	000004	357E			
UF*TRM	000200	359E			
UFD	003161	767	1573E		





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Cross Reference Table

XIMB	040004	1823	1838	2788E
XINIT	004016	552	1816L	
XINITI	004000	649	1786L	179Z
ZR01	007324	2754L	2757	

30454 bytes free

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