digital

Property of
K. T. Pogran

Computer Special Systems

IMP11-A
PDP-11 HOST TO IMP
FULL DUPLEX NPR INTERFACE

COMPUTER TYPE	DRAWING SET NO.
PDP-11	7010678-0-0
PROGRAM NO.	**DOCUMENT NO.**
DECSPEC-11-AYNADB	CSS-MO-F-3.3-20

DATE
FEBRUARY 1975

PRELIM[illegible]

DATE:_____

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SHIPPING LIST

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IMP 11-A

PDP-11 HOST TO IMP FULL DUPLEX NPR INTERFACE

1.1 GENERAL DESCRIPTION

The IMP[1]11-A Interface, manufactured by Digital, provides a direct connection between PDP-11 Computer Systems and the Interface Message Processor (IMP) used to connect Host Computers to the Advanced Research Projects Agency (ARPA) network. This UNIBUS option allows the user (with addition of appropriate software) to communicate via the network with other Host systems, and is supplied with level conversion modules to connect to either the Local or Distant Host interface of network IMP's.

The IMP 11-A (Figure 1-1) is supplied in a BA11-ES mounting box, complete with power supply, UNIBUS cable and Light Emitting Diode (LED) indicator panel, and includes all the logic elements required to implement the full duplex bit serial signal interchange defined for IMP to HOST connections. Diagnostic and exerciser software is also included to facilitate acceptance and maintenance procedures.

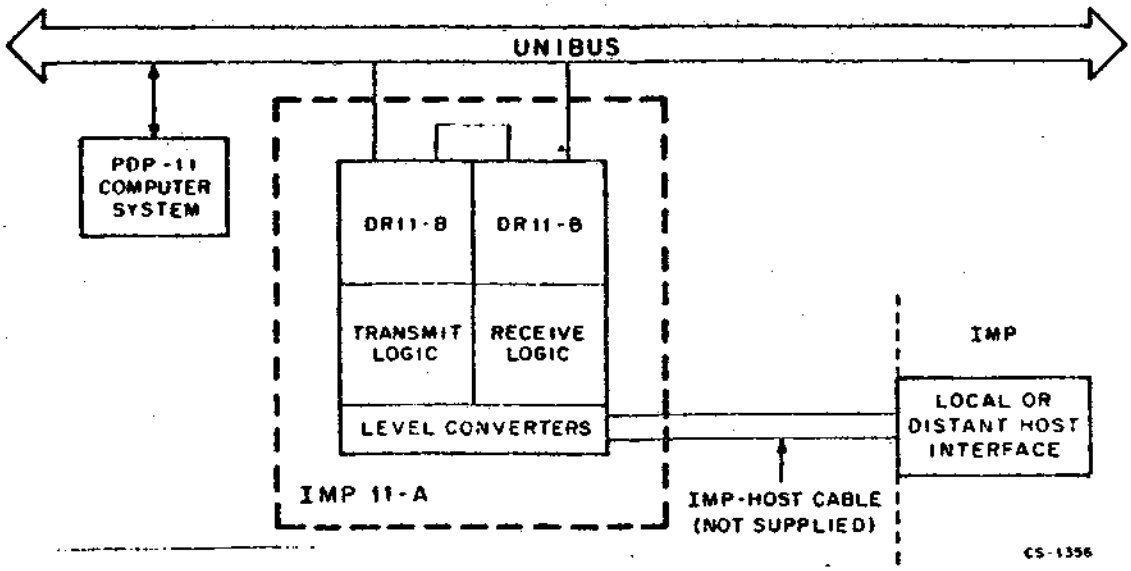


Figure 1-1 System Block Diagram

1.2 OPERATION

The IMP 11-A logic consists of two DR11-B general purpose NPR interfaces plus two specially wired BB11 System Unit mounting blocks containing standard Digital M-Series Modules. One DR11-B and its associated BB11 is dedicated to the transmit data and control signal path, and the other to the receive signals. When enabled for transmit, 16-bit words are loaded into a register where the IMP defined four way handshake signals shift one bit at a time out to the IMP. Each 16-bit word to be

shifted out of the IMP 11-A is input to the register by the DR11-B until the preset word count overflows. This overflow terminates the transmit sequence.

On receive, 16-bit words are assembled from the serial bit stream from the IMP and are transferred to system memory by the DR11-B. Either word count overflow or disconnection of the IMP terminates the transfer and appropriate status interrupts are generated.

1.3 SPECIFICATIONS*

a.	**Mechanical:**	
	Mounting Box	One, type BA11-ES
	Dimensions	10-1/2 in. h, x 19 in. w, x 24 in. d
	Weight	130 lbs
	Prerequisites	None
b.	**Electrical:**	
	Input Power	120 Vac ± 10%, 47-63 Hz
	Power Supply	One, type H720-E
	Logic	M-series modules, TTL levels
c.	**Operational:**	
	Capacity	One IMP host interface
	Transfer	Full duplex, NPR
	Unibus Loads	Two
	Data Rate	Nominal 100,000 bits/sec., full duplex
	Interrupt	Receive Section 1) Receipt of LAST BIT from IMP 2) Receive word count overflow Transmit Section 1) Word count overflow
	Output Levels	Local host - single ended 0 Vdc to 5 Vdc Distant host - differential ± 1.0 Vdc
	Signalling	Bit asynchronous with request/acknowledge handshake per bit
	Indicators	12 front panel Light Emitting Diodes displaying major IMP 11-A functions
	Cabling	Connector only supplied for terminating customer supplied IMP-HOST cable

1.4 AVAILABILITY

The IMP 11-A Interface is manufactured to meet the specifications of the March 1974 revision of BB & N report No. 1822, "Specifications for the interconnection of a host and an IMP".

*Specifications are subject to change without notice.

SECTION 2
INSTALLATION

2.1 SITE CONSIDERATIONS

The IMP-11A logic is contained in a BA11-ES mounting box. Power is derived from an H720E power supply which is also contained in the BA-11ES mounting box. No special environmental considerations exist, the IMP-11A operates in the same environment as the PDP-11/45.

2.2 CABLES

2.2.1 Unibus Cables

Connection between the IMP-11 and the PDP-11 Unibus is accomplished by means of standard PDP-11 Unibus Cables (BC11A). An M92Ø jumper card is provided for the Unibus connection between the two DR-11B's in the IMP-11. The input bus cable from the processor side is connected to slots ABØ1 in the DR-11B in the front of the mounting box and the output bus cable is connected to slots ABØ4 in the second DR-11B.

NOTE: It was not intended for any other logic to be housed in the BA-11ES mounting box with the IMP-11, therefore Unibus connections were not provided in the other two system units. If it is essential to mount another Unibus device in this box, a short length of bus cable must be used to connect it to the DR-11B's located in the front of the box.

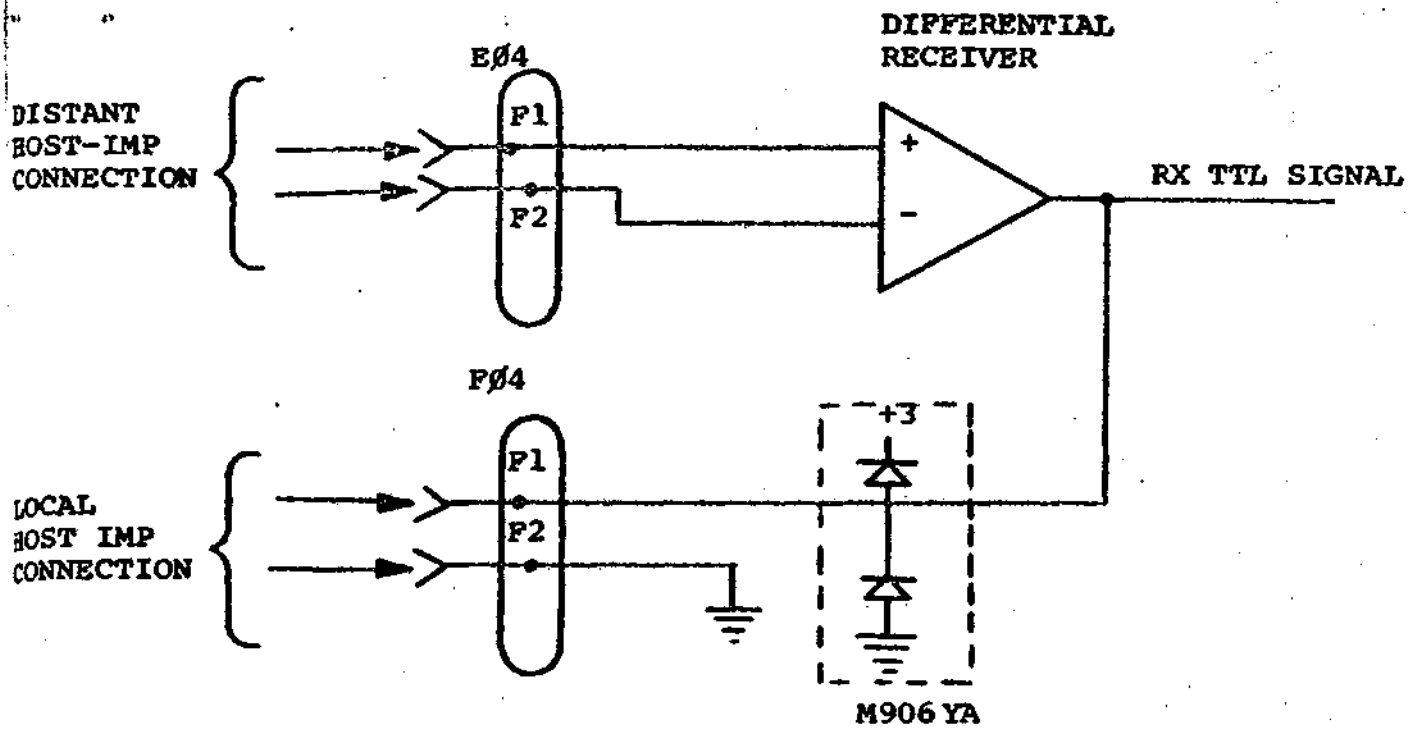
2.2.2 Signal Cable

A signal cable is not provided with the IMP-11, the user must provide a cable to connect the IMP-11 to the IMP. The end of this cable which is to attach to the IMP-11 should be connected to the M908 which is provided as follows:

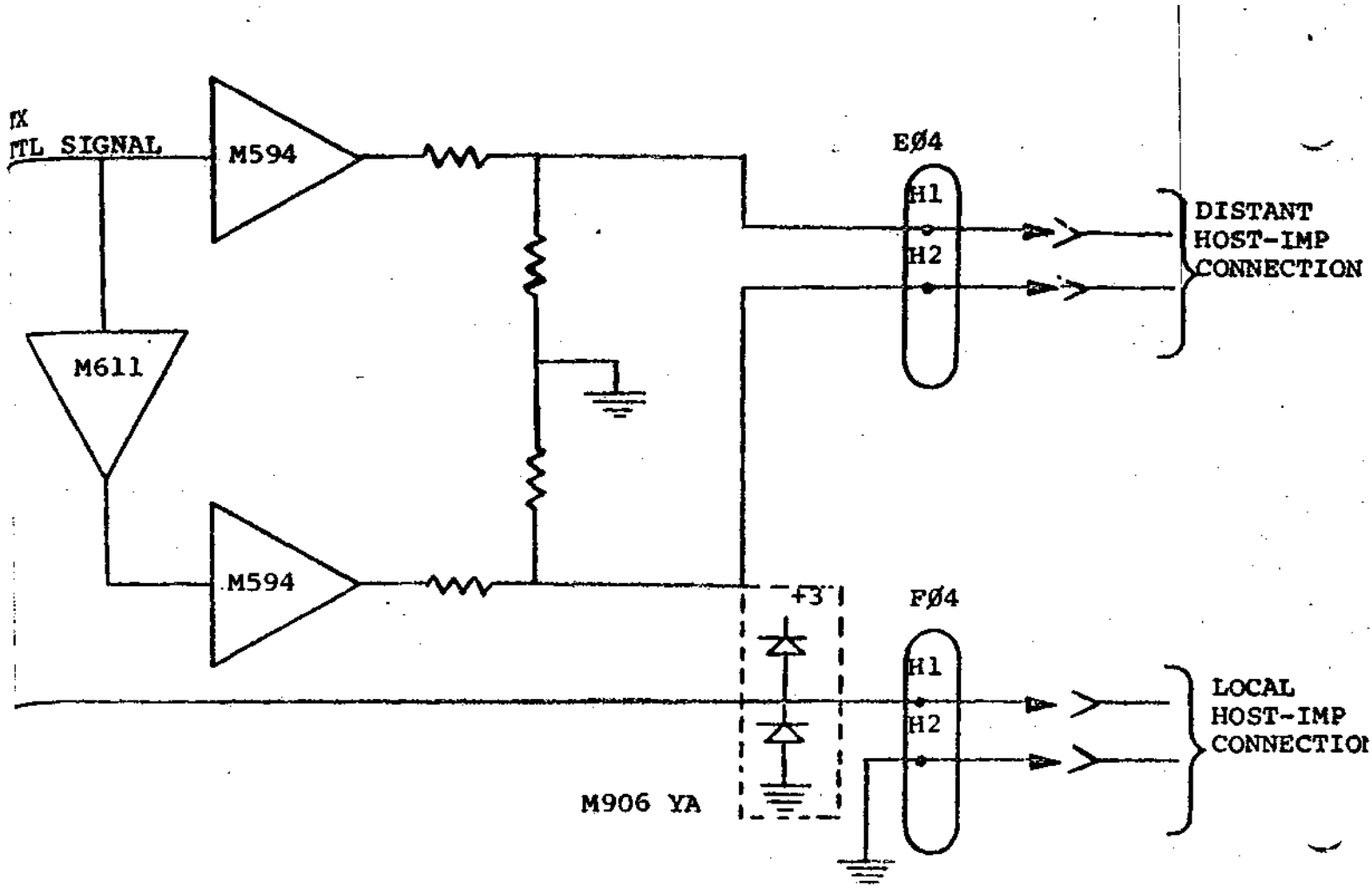
SIGNAL NAME**	SIGNAL PIN	SIGNAL GROUND PIN
Ready-for-next-host-bit (TX RFNB)	N1	N2
There's-your-host-bit (TX TYB)	P1	P2
Data: Host to Imp (TX Data)	S1	S2
Last Host bit (TX LB)	R1	R2
Ready-for-next-IMP-bit (RX RFNB)	H1	H2
There's-your-Imp-bit (RX TYB)	D1	D2
Data: Imp to host (RX Data)	F1	F2
Last IMP bit (RX LB)	E1	E2
IMP master ready	L1	
IMP Ready test	L2	
Host Master Ready	J1	
Host Ready test	J2	
Shield Ground	C2	

**The names shown correspond to the names used in BB+N Report #1822. Shown in parenthesis are the corresponding signal names in the IMP-11A.

The signal cable will be connected to slot FØ4 of the interface logic for local host operation and slot EØ4 for distant host operation. The two slots are pin compatible and no change in the signal cable should be required by the IMP-11 to convert from local host to distant host operation. Figire 2-1 shows a simplified schematic of a typical signal to illustrate the relationship of the two connector slots.



IMP TO HOST SIGNAL



HOST TO IMP SIGNAL
FIGURE 2-1
TYPICAL IMP-11 SIGNAL CONNECTIONS

Note that the distant and local transmit (host to IMP) signals do not interfere but that the distant and local receive signals will interfere in local host mode unless the M5007 differential receiver is removed. Therefore, to convert an IMP-11 from local to distant host operation, use slot EØ4 instead of FØ4 and remove the M5ØØ7 module.

Further specifications for construction of the interface cable can be found in Bolt, Beranek, and Newman report #1822, "Sepcifications for the Interconnection of a Host and an Imp".

2.2.3 Internal Cabling

A short length of ribbon cable is used to connect the LED indicators on the front panel to the indicator cable slot (DØ4) in the IMP-11 logic.

A short Unibus Cable (BC11A-Ø2) is used to connect the first DR-11B to the IMP-11A transmit logic. An M920 jumper is used to connect the second DR-11B to the receive logic.

2.3 GROUNDING

The IMP-11A should be grounded to the processor system ground with the ground strap provided.

2.4 INITIAL OPERATION

The following checkout and acceptance procedures are performed in-house prior to shipment of the IMP-11A. It is suggested that they be performed again at the customer's site, as an initial on site turn-on procedure.

2.4.1 Acceptance Test

A. Check out the DR-11B's on a stand-alone basis.
   Disconnect the IMP-11 interface logic from the DR-11B's by disconnecting the BC-11A Unibus Cable from slot CDØ4 of the first DR-11B and the M920 jumper from slot CDØ4 of the second DR-11B.

Move the M968, DR-11B test board, from AB02 to slot CD04 in each DR-11B. Run the DR-11B diagnostic (MAINDEC-11-DZDRBA) on each DR-11B. The test should be run for twenty minutes without error on each DR-11B. (See Section 3.1 for DR-11B addresses).
* Remove Jumper E03A1 - E03C2

B. Check out the IMP-11 in local host mode.

Reconnect the DR-11B's to the IMP-11 interface logic. Restore the DR-11B test board to slot AB02 in each DR-11B. Install the IMP-11 loop-back connector in slot F04 of the IMP-11 interface logic.

Remove the M5007 differential receiver. NOTE: The IMP-11 will malfunction in the local host mode if this module is not removed.

Run the IMP-11 exerciser (DECSPEC-11-AYNADB) for 45 minutes.

C. Checkout the IMP-11 in distant host mode.

Replace the M5007 differential receiver module in the IMP-11 logic and move the loop back connector from slot F04 to slot E04.

Repeat running the IMP-11 exerciser for 45 minutes.

NOTE: For factory acceptance, a long twisted pair cable will be used in this test in place of the loop back connector to more realistically test the differential level converters.

2.5 RELATED LITERATURE

a. Bolt, Beranek, and Newman Report #1822, "Specifications for Interconnection of a Host and an IMP".

b. DR-11B Option Description DEC-11-HDRA-D

c. Unibus Interface Manual

d. Logic Handbook

SECTION 3
OPERATION AND PROGRAMMING

All access to the IMP-11 logic by the program is through the two DR-11B's. The option appears and functions as two standard DR-11B's with the exception of the function and status bits, which are redefined for the IMP-11A. The reader is referred to the DR-11B manual which is provided with the IMP-11 for a more thorough description of the standard DR-11B functions.

3.1 HARDWARE REGISTERS

The following is a list of the hardware registers in the IMP-11A with their standard address assignments:

TXWCR	172410
TXBAR	172412
TXCSR	172414
TXDBR	172416
RXWCR	172430
RXBAR	172432
RXCSR	172434
RXDBR	172436

Standard vector addresses are

Transmit	124
Receive	114

3.1.1 Transmit word count register (TXWCR) - 172410

The TXWCR is a 16 bit read/write register. It is initially loaded with the 2's complement of the number of words to be transmitted and increments toward zero after each bus cycle. When the overflow occurs (all 1's to all Ø's) the READY bit of the TXCSR sets, bus

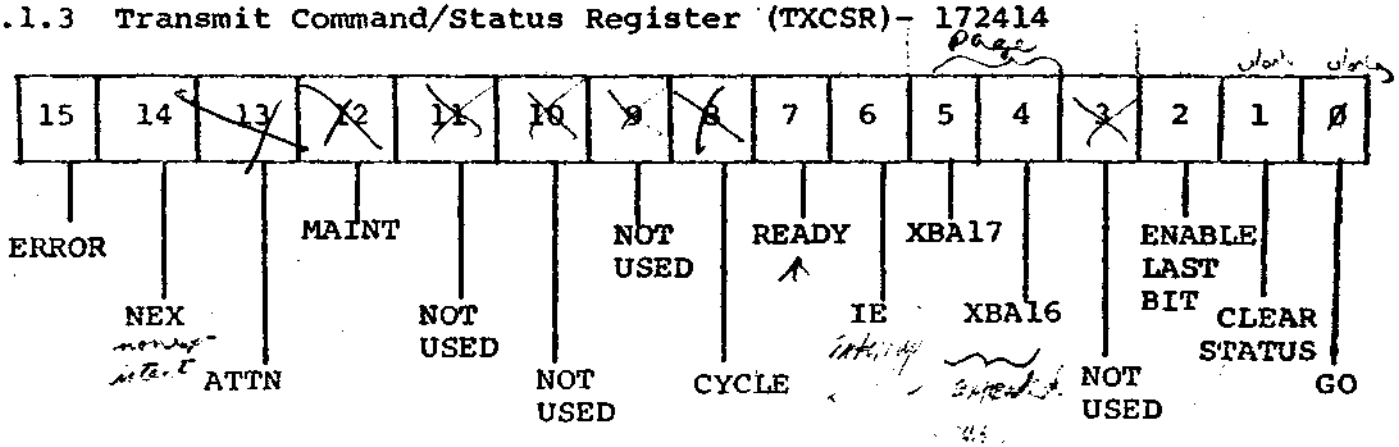
cycles cease ,and if the interrupt enable (bit Ø6 of the TXCSR) is set an interrupt is generated. TXWCR is cleared by bus INIT.

3.1.2 Transmit Bus Address Register (TXBAR)- 172412

The TXBAR is a 15 bit read/write register. Bit Ø, corresponding to address bit AØØ is set permanently to a zero. With the two extended memory bits in the TXCSR (XBA16 and XBA17) the TXBAR specifies BUS A <17 : Ø1> in direct bus access. The register is incremented by two following each bus cycle advancing the address to the next sequential word location in the UNIBUS address space. If the TXBAR overflows (all 1's to all Ø's) the error bit in the TXCSR sets. This error condition is cleared by loading the TXBAR or by bus INIT. NOTE: TXBAR is a word register; do not use byte instructions when loading the register.

The TXBAR is cleared by bus INIT. Overflow does not increment the extended address bits XBA16 and XBA17. Therefore the maximum block that can be transferred is 32K words and a block cannot be transmitted that overlaps a 32K boundary.

2.1.3 Transmit Command/Status Register (TXCSR)- 172414



3.1.3.1 ERROR (Bit-15) - The ERROR bit is read-only, and specifies an error condition when:

a. The DR11-B has attempted to address non-existent memory (also indicated by NEX Bit-14) or

b. ~~The test module is not inserted in slot AB02 or CD04 of the~~ DR11-B, ~~or~~

c. The bus address ~~register~~ ~~T:BAR~~ has overflowed by incrementing from all 1's to all 0's.

ERROR sets READY (Bit-7) and causes an interrupt if INTERRUPT ENABLE (Bit-6) is set.

The ERROR bit is cleared by removing the condition(s) that caused it to set:

e. NEX is cleared by loading Bit-14 with a zero.

f. ~~Insert~~ the test module in slot AB02 for normal operation ~~or CDØ4~~ for diagnostic tests.

g. Reload the bus address register DRBA.

3.1.3.2 NEX (Bit-14) - NEX is a read/write to 0 bit. The non-existent memory condition specifies that, as Unibus master, the DR-11B did not receive a SSYN response within a 20 microseconds following assertion of MSYN. NEX sets ERROR (Bit-15), READY (Bit-7), and causes an interrupt request if IE (Bit-6) has been set. This bit is cleared by INIT or by loading a zero, it cannot be loaded with a one.

3.1.3.3 ATTN (Bit 13) - The ATTN bit is pulsed by the transmit logic to set the READY BIT in the DR11B when TX CLEAR STATUS (Bit 2) is asserted. It will cause an interrupt if IE (Bit 6) is set. This is a READ ONLY Bit and should normally be zero.

3.1.3.4 MAINT (Bit-12) - The MAINT bit is read/write; it is used exclusively with diagnostic programs and is cleared by INIT (refer to Chapter Five in the DR11-B manual for further information).

3.1.3.5 Bits 9, 10, and 11 are not used in the transmit logic. They are read only bits.

3.1.3.6 CYCLE (Bit-8) - The cycle bit is not used in the IMP-11 logic and may be ignored.

3.1.3.7 READY (Bit-7) - The read-only READY bit specifies that the DR11-B is ready to accept a new command. When set, READY forces the DR11-B to release control of the Unibus and inhibits further DMA cycles. This bit is set by INIT, ERROR (Bit-15), or word count overflow and is cleared by GO (Bit-0). Note that READY must be cleared prior to initiating the block transfer. When set, causes an interrupt request if IE (Bit-6) has been set.

3.1.3.8 IE (Bit-6) - The read/write IE bit enables an interrupt to occur when either ERROR or READY is asserted. This bit is cleared by INIT.

3.1.3.9 XBA17, XBA16 (Bits 5 and 4) - These two read/write extended bus address bits (17 and 16) are used with TXBAR to specify A<17:01> in direct memory transfers. XBA17 and XBA16 do ~~not~~ increment when TXBAR overflows; ~~instead, ERROR is set.~~

3.1.3.10 Bit 3 is not used in the transmit logic.

3.1.3.11 ENABLE LAST BIT (BIT 2) When set, the IMP-11 will generate the LAST BIT signal to indicate the end of message when the word count overflows. The bit is cleared to stop the IMP-11 from signaling end of message when transmitting multiple buffers. This bit should be set when transmitting the last buffer in the message. If the message consists of only one buffer, the bit can be set before starting transmission (setting the go bit) ~~NOTE: The IMP-11 examines the state of this bit when the last word (word count overflow) has been received from the DR-11B.~~

3.1.3.12 TX Clear Status (Bit 1) This bit initializes the transmit logic. It should be set and cleared to initialize the transmit logic in the IMP-11. NOTE: Leaving this bit set will disable the transmit logic. Setting this bit will also cause the transmit DR-11B to abort any operation and set it's Ready bit. Will cause an interrupt if IE (Bit 6) is set.

3.1.3.13 GO (Bit-0) - The write-only GO bit causes a pulse to initiate the first DMA cycle in the block transfer. This bit always reads as a zero. When set, this bit clears ready (Bit 7).

3.1.4 Transmit Data Buffer Register (TXDBR) - 172416

The TXDBR serves as temporary storage register in the DR-11B to hold the word being transferred under program control. There should be no need for access to this register in the IMP-11A.

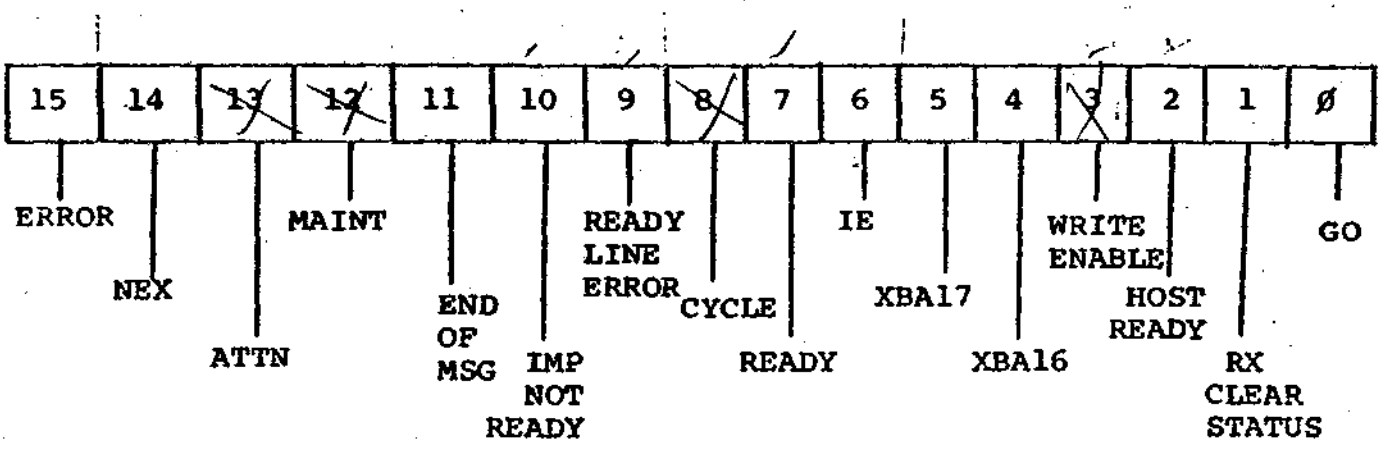
3.1.5 Receive Word Count Register (RXWCR) 172430

The function of the RXWCR is equivalent to the TXWCR (see section 3.1.1).

3.1.6 Receive Bus Address Register (RXBAR) - 172432

The function of the RXBAR is equivalent to the TXBAR (see section 3.1.2).

3.1.7 Receive Command/Status Register (RXCSR) 172434



3.1.7.1 ERROR (Bit-15) - The ERROR bit is read-only, and specifies an error condition when:

a. The DR11-B has attempted to address non-existent memory (also indicated by NEX Bit-14) or

b. The test module is not inserted in slot AB02 or CD04 of the DR11-B, or

c. The bus address register RXBAR has overflowed by incrementing from all 1's to all 0's.

ERROR sets READY (Bit-7) and causes an interrupt if INTERRUPT ENABLE (Bit-6) is set.

The ERROR bit is cleared by removing the condition(s) that caused it to set:

e. NEX is cleared by loading Bit-14 with a zero.

f. Insert the test module in slot AB02 for normal operation or DC04 for diagnostic tests.

g. Reload the bus address register RXBAR.

3.1.7.2 NEX (Bit-14) - NEX is a read/write to 0-bit. The non-existent memory condition specifies that, as Unibus master, the IMP11-A did not receive a SSYN response within a 20 microseconds following assertion of MSYN. NEX sets ERROR (Bit-15), READY (Bit-7), and causes an interrupt request if IE (Bit-6) has been set. This bit is cleared by INIT or by loading a zero, it cannot be loaded with a one.

3.1.7.3 ATTN (Bit 13) The ATTN bit is read only; it is pulsed by the IMP-11 when the last bit signal has been received from the IMP. This causes an interrupt if interrupt enable (Bit 6) is set. The error bit will not be set and end of MSG (Bit 11) will be set when the last bit has been received. The ATTN Bit is also pulsed by the receive logic to set the DR11B Ready Bit when RX clears status is asserted.

3.1.7.4 MAINT (Bit-12) - The MAINT bit is read/write; it is used exclusively with diagnostic programs and is cleared by INIT (refer to Chapter Five in the DR11-B manual for further information).

3.1.7.5 END OF MSG (Bit 11) - Indicates that the last bit signal has been received from the IMP signifying the end of a message. Cleared by RX CLEAR STATUS or GO (Bit Ø).

3.1.7.6 IMP NOT READY (Bit 10) - When set, indicates that the IMP is not ready.

3.1.7.7 READY LINE ERROR (Bit 9) When set, indicates that either HOST READY ~~is~~ was not set or IMP NOT READY ~~is~~ was set. (cleared by RCLEAR, RGO, RESET.)

3.1.7.8 CYCLE (Bit-8) - The cycle bit is not used in the IMP-11 and may be ignored.

3.1.7.9 READY (Bit-7) - The read-only READY bit specfies that the DR11-B is ready to accept a new command. When set, READY forces the DR11-B to release control of the Unibus and inhibits further DMA cycles. This bit is set by INIT, ERROR (Bit-15), or word count overflow and is cleared by GO (Bit-0). Note that READY must be cleared prior to initiating the block transfer. When set, causes an interrupt request if IE (Bit-6) has been set.

3.1.7.10 IE (Bit-6) - The read/write IE bit enables an interrupt to occur when either ERROR or READY is asserted. This bit is cleared by INIT.

3.1.7.11 XB17, XB16 (Bits 5 and 4) - These two read/write extended bus address bits (17 and 16) are used with TXBAR to specify A<17:01> in direct memory transfers. XBA17 and XBA16 ~~do~~ not increment when TXBAR overflows ~~instead~~, ERROR is set.

3.1.7.12 RX WRITE ENABLE (Bit 3) - Must be set for proper operation of the receive logic. If this bit is not set, the IMP-11 will effectively discard any data that is received although it will other wise appear to operate normally. (READ/WRITE)

3.1.7.13 HOST READY (Bit 2) - SET to INDICATE to the IMP that the host is on line and ready. Cleared by INIT. (READ/WRITE)

3.1.7.14 RX CLEAR STATUS (Bit 1) Initializes RECEIVE LOGIC. It should be set and then cleared to initialize the logic. NOTE: Leaving this bit set will disable the transmit logic. Setting this bit will cause the receive DR-11B to abort any operation and set it's ready bit. Will cause an interrupt it IE (Bit 6) is set.

3.1.7.15 GO (Bit-0) - The write-only GO bit causes a pulse to initiate the first DMA cycle in the block transfer. This bit always reads as a zero. When set, this bit clears READY (Bit-7).

3.1.8 Data Buffer Register (RXDBR) receive. - 172436

The RXDBR serves as a temporary storage register in the DR-11B to hold the work being transferred under program control. There should be no need to access this register in the IMP-11A.

3.2 INDICATORS

There are 12 indicators on the front of the IMP-11A. (See figure 3-1).

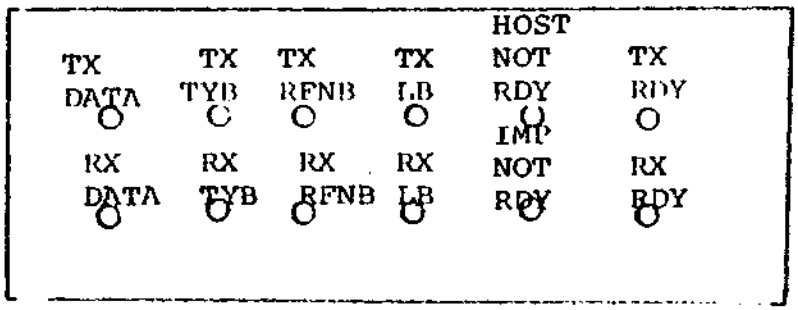


FIGURE 3-1 IMP-11 INDICATOR PANEL

The lights, DATA, RFNB, and TYB represent the current state of the Data, Ready-for-Next-Bit and There's-your-Bit signals respecively between the host and IMP.

The lights IMP NOT READY and HOST NOT READY reflect the state of the ready signals in the IMP and host. The normal condition of these lights is that both should be out. If either of these lights is lit it indicates an abnormal condition in either the host or the IMP.

The two ready lights reflect the state of the DR-11B ready signals. These lights will be out while DMA transfers are taking place and will be on when the respective DR-11B is idle.

3.3 PROGRAMMING EXAMPLE

The following example shows the programming steps necessary to transmit a block of 500 decimal words.

```
TRNSMT:  MOV  #TXBUF,TXBAR; Set up Bus Address
         MOV  #-500., TXWCR; Set up word count
         MOV  #2,TXCSR; TOGGLE TX CLEAR STATUS
         MOV  #4,TXCSR; Set Enable Last Bit
         BIS  #101,TXCSR; Set TX GO and INT Enable.
          .
          .
          .
TXBUF:   (500 words of data)
114:     Transmit Interrupt Service Address
116:     and Processor Status Word
```

The following shows the programming steps necessary to receive a 500 word (or less) message:

```
MOV   #RXBUF,RXBAR; Set RX Bus Address
MOV   #-500., RXWCR; Set RX Word Count
MOV   #16,RXCSR; Set host ready, write enable and clear status
BIC   #2,RXCSR; Drop Clear Status
BIS   #101,RXCSR; Set RX GO and Interrupt Enable
        •
        •
        •
124 ⎫ RX Interrupt Service routine address and Processor Status Word
126 ⎭
```

The above program for receiving will cause an interrupt whenever 500 words of data have been received and/or the last bit signal is received.

NOTE: The last bit signal is not recognized by the IMP-11 until the end of a word.

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

The IMP-11 is a PDP-11 family device for interfacing a PDP-11 to the Advanced Research Projects Agency Network (ARPANET). The IMP-11 is designed to connect to an Interface Message Processor (IMP) which is the communications processor in the ARPANET. The signalling scheme is in adherence with the specifications in Bolt, Beranek and Newman Report 1822, "Specifications for Interconnection of a Host and an IMP."

Figure 4.1 shows a simplified block diagram of the IMP-11 logic.

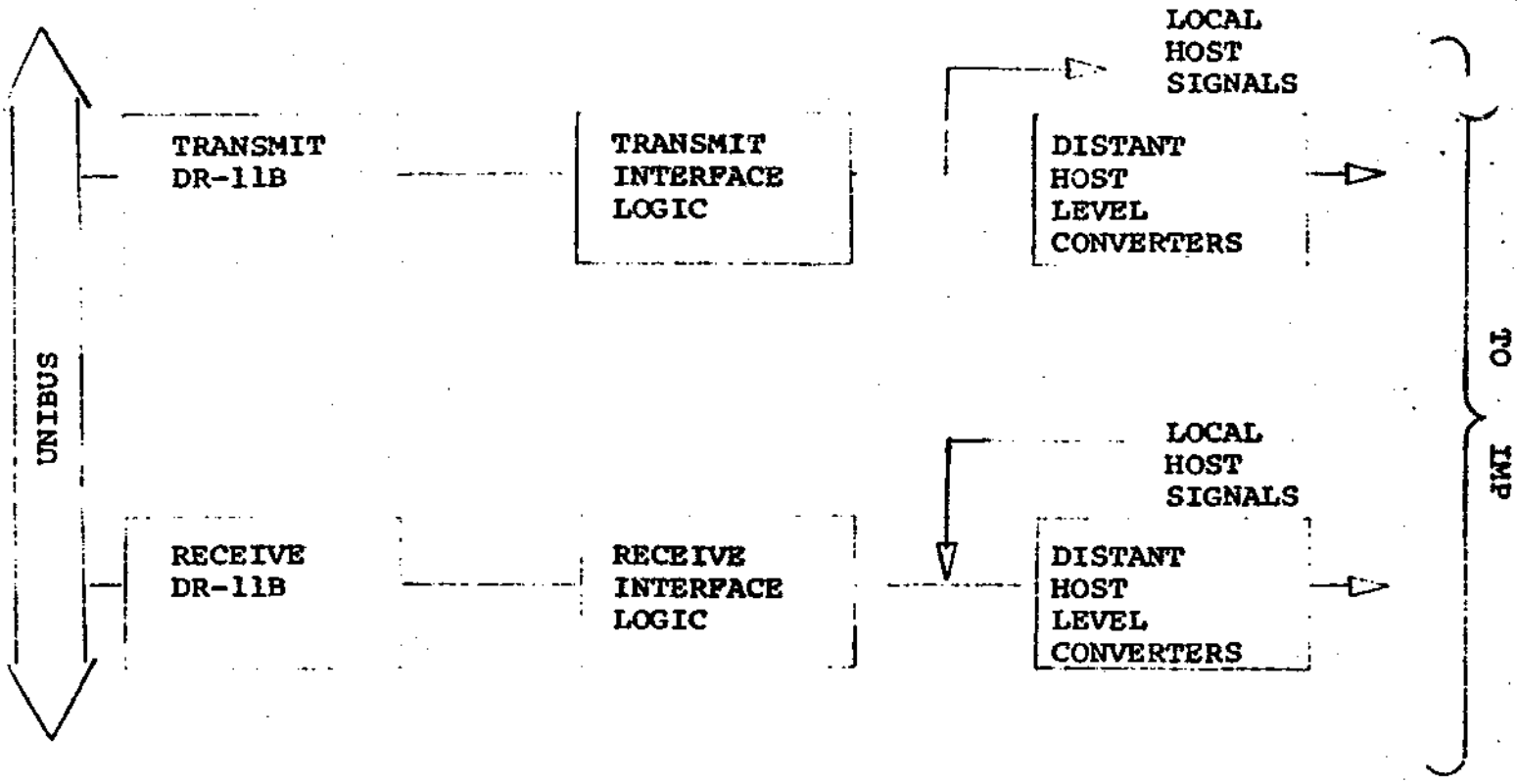


FIGURE 4.1

IMP-11 SIMPLIFIED LOGIC DIAGRAM

The interface to the UNIBUS is through 2 DR-11B's. Associated with this pair of DR11-B's is an interface logic assembly. This logic controls the DR11-B's, serializes and de-serializes the data, and generates the control signals required by the Host Interface in the IMP.

4.2 INTERFACE LEVELS

The IMP-11 is capable of operating in two modes, as either a local host or as a distant host. The local host signals out of the IMP are standard TTL levels of 0 and +3V to ground driven by high current drivers. The distant host signals are differential signals as follows:

	Logic 1	Logic Ø
Signal Line	+0.5V	-0.5V
Pair	-0.5V	+0.5V

4.3 TRANSMIT LOGIC

The transmit section of the interface logic assembly consists of a 16 bit shift register, a 4 bit counter, and a number of flip-flops for status and control bits.

The transmitting sequence is initiated when the GO bit is set and the DR-11B Ready signal goes low. This removes the reset from the transmit logic. This causes a pulse on TX READY FALL and a request is given to the DR-11B for the first word. The DR-11B does an NPR cycle, inputing the first word from computer memory and passing it to the transmit shift register of the interface logic assembly. The data is shifted out according to the four way hand shaking protocol of the Host Interface of the IMP. (see timing diagram print IMP-11-0-10).

The four way hand shaking sequence associated with each data bit proceeds as follows. The assertion of Ready-for-Next-Bit (RFNB) from the Host interface in the IMP is detected in the IMP11-A and the next data bit is shifted onto the data line. After a short delay, the IMP11-A asserts Theres-your-Bit. (TYB) The Host interface uses this signal to strobe the data bit in and then drops RFNB. The negation of RFNB at the IMP-11A results in the dropping of TYB. The interface logic in the IMP11-A starts on the next four-transition cycle when RFNB signal is re-asserted by the Host interface.

Figure 4-2 shows a simplified diagram of this sequence.

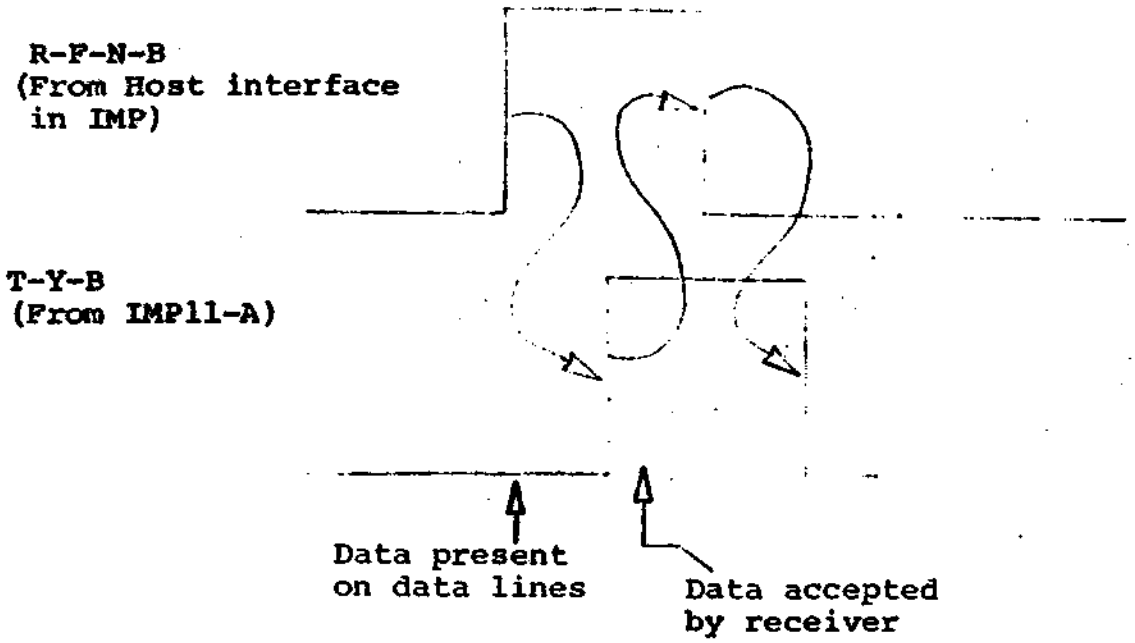


FIGURE 4.2

The 4 bit counter is incremented and the shift register is shifted during each cycle. When the counter overflows, (16 bits transmitted) a new word request is given to the DR-11B and further transfers are inhibited until the word has been received from the DR-11B and loaded into the shift register. Note that the counter is incremented to one as soon as the word is loaded since the first bit is present on the data lines at that time.

The TX Last Word flip flop is set as soon as the last word is being transmitted (indicated by the rise of the DR-11B ready signal. On the last bit of the last word, the Last Bit (LB) signal is transmitted along with the data if the Enable Last Bit was set in the DR-11B status register. The Last Word flip flop is cleared automatically following transmitting this bit so that it will be initialized for the next block of data. As soon as the Last Word signal is cleared, the Reset signal is asserted and the logic is disabled until the next block transfer.

4.4 RECEIVE LOGIC

The basic operation of the receive logic is very similar to the transmit logic. There are several minor differences and several additional features. One of the minor differences is the 4 bit counter starts at zero rather than one because the first bit must be shifted in before it is counted.

When the Last Bit signal has been recognized by the IMP-11 logic, it is not presented to the processor as an interrupt until the word has been transferred by the DR-11B. Therefore, if it is sent before all 16 bits have been received,the interrupt will not occur until all 16 bits have been received.

Print IMP-11-Ø-Ø9 shows a detailed drawing of the receive timing sequence.

A relay is included in the logic to signify to the IMP that the host PDP-11 is ready. The two sides of the relay contacts are brought out to the IMP as signal lines. The normal way to use these is to ground one side and sample the output of the other side. The other side will then be switched between an open circuit and ground depending on the state of the relay. The relay is set by setting the host ready bit in the RXCSR. Naturally, if power is lost to the IMP-11, the relay will open and indicate to the IMP that it is not ready.

A flip flop (Ready Line Error) has been included to store the fact that either HOST NOT READY or IMP NOT READY has been asserted.

4.5 DR-11B LOGIC

The DR-11B's are standard and have not been modified. Refer to the DR-11B option description for a thorough analysis of the DR-11B logic. Since some of the normal DR-11B signals have different names in the IMP-11, a table is presented here to show the correlation of the standard DR-11B signal names and the names given to the signals in the IMP-11 logic.

TABLE 4-1

IMP-11/DR11B SIGNAL NAMES

IMP-11 RECEIVE SECTION NAME	NAME IN RECEIVE DR11B
GROUND	CO CONTROL H
WRITE ENABLE	C1 CONTROL H
	CYCLE REQUEST AH
RX WORD READY	CYCLE REQUEST BH
+3V	WC INC ENB H
+3V	BA INC ENB H
GROUND	A00 H
RX END OF MESSAGE	DSTAT A H
IMP NOT READY	DSTAT B H
READY LINE ERROR	DSTAT C H
RX ATTN H	ATTN H
+3V	SINGLE CYCLE H
RX WRITE ENABLE	FNCT 3 H
HOST READY	FNCT 2 H
RX CLEAR STATUS	FNCT 1 H
RX INACTIVE	READY H
RX CYCLE BUSY	BUSY H
RX WORD ACCEPT	END CYCLE H
	GO H
	NO LOCK H
	INIT H

IMP-11 RECEIVE SECTION NAME	NAME IN RECEIVE DR-11B
RX BIT Ø8	DAT15 IN H
RX BIT Ø9	DAT14 IN H
RX BIT 1Ø	DAT13 IN H
RX BIT 11	DAT12 IN H
RX BIT 12	DAT11 IN H
RX BIT 13	DAT10 IN H
RX BIT 14	DAT09 IN H
RX BIT 15	DAT08 IN H
RX BIT 00	DAT07 IN H
RX BIT 01	DAT06 IN H
RX BIT 02	DAT05 IN H
RX BIT 03	DAT04 IN H
RX BIT 04	DAT03 IN H
RX BIT 05	DAT02 IN H
RX BIT 06	DAT01 IN H
RX BIT 07	DAT00 IN H
	DAT15 OUT H
	DAT14 OUT H
	DAT13 OUT H
	DAT12 OUT H
	DAT11 OUT H
	DAT10 OUT H
	DAT09 OUT H
	DAT08 OUT H
	DAT07 OUT H
	DAT06 OUT H

IMP-11 RECEIVE SECTION NAME	NAME IN RECEIVE DR-11B
	DAT05 OUT H
	DAT04 OUT H
	DAT03 OUT H
	DAT02 OUT H
	DAT01 OUT H
	DAT00 OUT H

IMP-11 TRANSMIT SECTION NAME	NAME IN TRANSMIT DR-11B
GROUND	CO CONTROL H
GROUND	C1 CONTROL H
WORD REQUEST	CYCLE REQUEST AH
	CYCLE REQUEST BH
+3V	WC INC ENB H
+3V	BA INC ENB H
GROUND	A00 H
	DSTAT A H
	DSTAT B H
	DSTAT C H
TX ATTN H	ATTN H
+3V	SINGLE CYCLE H
	FNCT 3 H
TX ENABLE LAST BIT	FNCT 2 H
TX CLEAR STATUS	FNCT 1 H
TX READY	READY H
TX CYCLE BUSY	BUSH H
TX WORD VALID	END CYCLE H
	GO H
	NO LOCK H
	INIT H

IMP-11 TRANSMIT SECTION NAME		NAME IN RECEIVE DR-11B
		DAT15 IN H
		DAT14 IN H
		DAT13 IN H
		DAT12 IN H
		DAT11 IN H
		DAT10 IN H
		DAT09 IN H
		DAT08 IN H
		DAT07 IN H
		DAT06 IN H
		DAT05 IN H
		DAT04 IN H
		DAT03 IN H
		DAT02 IN H
		DAT01 IN H
		DAT00 IN H
ΓX	BIT 8	DAT15 OUT H
	9	DAT14 OUT H
	10	DAT13 OUT H
	11	DAT12 OUT H
	12	DAT11 OUT H
	13	DAT10 OUT H
	14	DAT09 OUT H
	15	DAT08 OUT H
	0	DAT07 OUT H
	1	DAT06 OUT H
'X	BIT 2	DAT05 OUT H

TX	BIT 3	DAT04	OUT	H
	4	DAT03	OUT	H
	5	DAT02	OUT	H
TX	BIT 6	DAT01	OUT	H

SECTION 5
MAINTENANCE

5.1 SPECIAL TEST EQUIPMENT - NONE

5.2 SPECIAL TOOLS - NONE

5.3 PREVENTIVE MAINTENANCE

Clean fan filters to insure adequate ventilation is provided. This will facilitate proper cooling of power supplies and control logic.

5.4 CORRECTIVE MAINTENANCE

It is suggested that the acceptance and test procedure in Appendix A be repeated to locate and repair malfunctioning logic.

SECTION 6
SPARE PARTS

6.1 MODULES

Table 6.1 lists the IMP-11A module complement by Dec No., function, and quantity.

TABLE 6.1

IMP-11A MODULE COMPLEMENT

TYPE	FUNCTION	QTY.
G8000	+12V SUPPLY	1
K265	Relay Driver	1
M111	Inverter	2
M113	10-2 Input Nand Gate	2
M117	6-4 Input Nand Gate	1
M205	5 "D" Flip Flops	3
M238	Synchronous 4 bit UP/Down Counter	1
M245	4 Bit shift register	4
M310	Delay Line	1
M401	Variable clock	1
M594	EIA level converter	2
M611	High Speed Power Inverter	1
M5ØØ7	Differential Receivers	1
W964-YA	Resistor Network with -5V supply	1
M906YA	Terminator	1

APPENDIX A
DEVICE DIAGNOSTIC PROGRAM DESCRIPTION

A.1 ABSTRACT

The diagnostic program for the IMP is the IMP-11A Offline Exerciser (DECSPEC-11-AYNADA). An online diagnostic which checks the operation of both the IMP and the IMP-11 is available from Bolt, Beranek, and Newman. The On line diagnostic is not supported by DEC and any inquiries regarding it should be addressed directly to BB+N.

The offline exerciser tests the IMP-11 by looping the transmit side into the receive side by using the test connector provided.

The diagnostic transmits 500 words of random data through the IMP on each pass. It also checks the proper operation of all status and function bits and interrupts.

NOTE: The IMP-11 offline exerciser was not intended to be used in isolating problems in the DR-11B's. These problems can best be isolated by running the DR-11B diagnostic on each of the DR-11B's with them disconnected from the IMP-11A logic. Since the majority of the logic in the IMP-11 is in the DR-11B, it is suggested that the first step in isolating any problems that occur should be to verify the operation of the DR-11B's on a stand-alone basis.

A.2 REQUIREMENTS

The diagnostic can be run with 8K of core, any PDP-11 processor, and the IMP-11.

A.3 LOADING PROCEDURE

The program is normally furnished on paper tape. The normal procedure for loading binary tapes is followed for loading the tape into memory.

A.4 STARTING PROCEDURE

There are three starting addresses used in the program:

200 Normal Start and Initialization

204 Restart Address

210 Start program at this address to input any non-standard IMP-11 addresses.

A.5 ERRORS

When an error occurs, the diagnostic prints out the contents of the IMP-11 hardware registers (see section 3). If a data check error occurs, the diagnostic also prints out the number of the word in error and the transmitted and received words.

APPENDIX B
SHIPPING LIST

B.1 EQUIPMENT FURNISHED

The following documents and equipment are provided with an IMP-11A:

a. BA11ES mounting box with mounting hardware. (1 each)

b. H720E power supply with remote turn-on cable. (1 each)

c. DR-11B general purpose NPR interface (2 each)

d. IMP-11 interface logic with full module complement (see table 6.1)

e. Test connector for IMP-11 logic. (1 each)

f. Blank M908 for user signal cable. (1 each)

g. IMP-11 Option Description (CSS-MO-F-3.3-18A)

h. IMP-11 Offline Exerciser (DECSPEC-11-AYNADB)

i. IMP-11 Print Set.

j. DR-11B/DA-11B Manual.

k. DR-11B Print Set.

l. DR-11B/DA-11B Diagnostic. (MAINDEC-11-DZDRBA)