digital

DV11-Ø

Engineering Drawings

Digital Equipment Corporation

digital EQUIPMENT CORPORATION

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

SEQUENCE	
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BUS CONTROL & MUX	D-CS-M7807-0-1
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INTERNAL BUS CONN. M92Ø	C-CS-M920-0-1
DV11 DIST. PANEL (C.S.)	D-CS-5411153-0-1
MODEM I/O CABLE ASSY	C-UA-BCØ8R-0-0
H325 TEST CONNECTOR	D-CS-H325-0-1
H861 TEST CONNECTOR	D-CS-H861-0-1
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SEQUENCE	MFG. PRINT SET
DV11 MODULE TEST PROCEDURE	A-SP-DV11-0-2
DV11 TEST PROCEDURE	A-SP-DV11-0-3
ACCEPTANCE PROCEDURE	A-SP-DV11-0-4

THIS IS PRINT SET ☐☐☐☐

UNIT VARIATIONS

VAR	TITLE	PRINT SET 1
DV11-AA	COMM. MUX CONTROL UNIT	X
DV11-BA	MODULE SET & DIST. PANEL (SYNCH)	X
DV11-BB	MODULE SET & DIST.PANEL (ASYNCH)	X
DV11-BC	SYNCH/ASYNCH MODULE SET & DIST. PANEL	X

REVISIONS		
DATE	CHG. NO.	REV
5-76	DV11-4	D
REVISED & REDRAWN		
8-76	DV11-5	E
7-77	DV11-6	F
5-78	DV11-MK7	H
10-78	DV11-MK8	J
6-82	DV11-MKØØ9	K

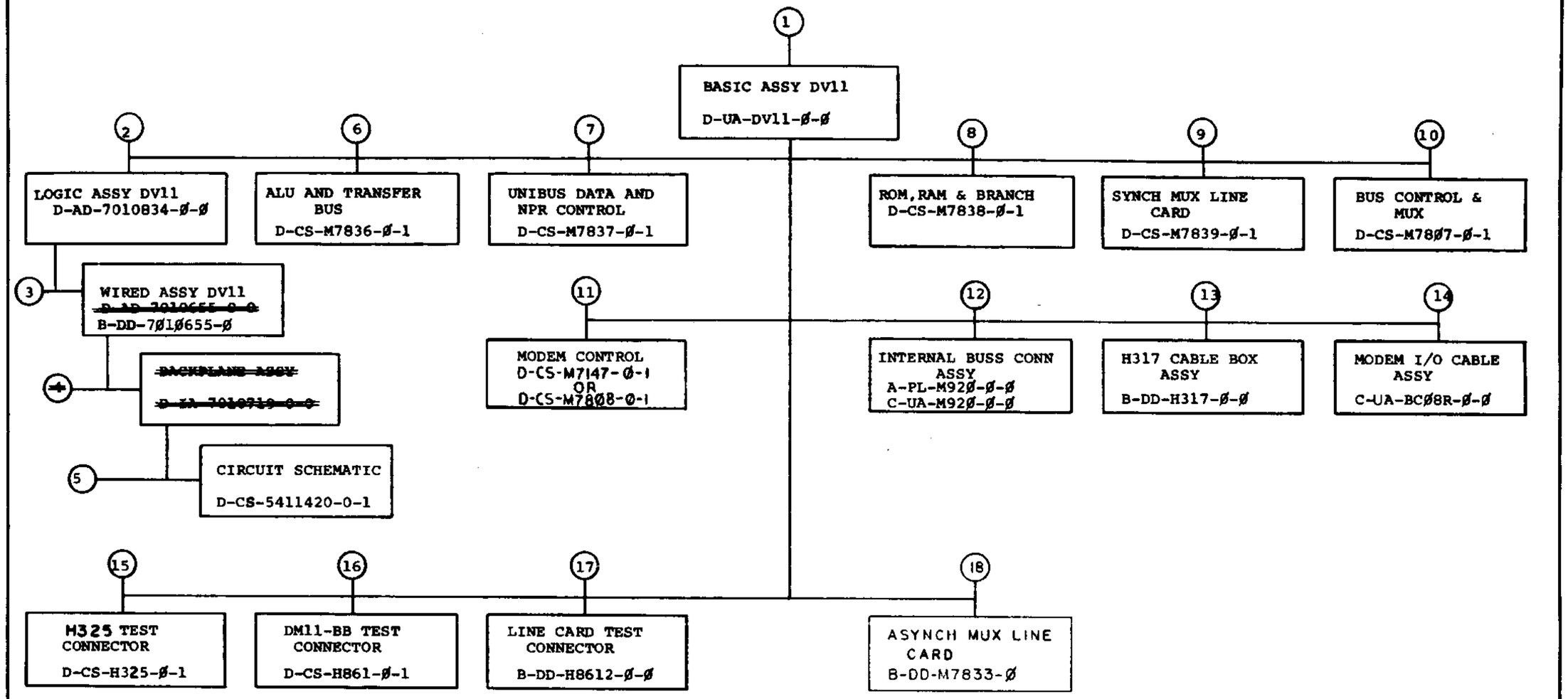
USED ON OPTION/MODEL	
DV11	

SHEET 1 OF 5

DRN. K. DAVIS	DATE 3-20-75	TITLE: BASIC ASSY (DV11)
CHK'D. S. ROBERTS	DATE 4-23-75	
PROJ ENG. J.E.McNAMARA	DATE 4-23-75	
PROD. R. WALL	DATE 4-23-75	SIZE B / CODE DD / NUMBER DV11-Ø / REV K
FIELD SERV. T. RITTER	DATE 4-25-75	DIST / MP-ØDV11-ØØ

EK-DV11-TM-001 (12-82-1283)

DRB 106



TITLE	SHEET	SIZE	CODE	NUMBER	REV
BASIC ASSY DV11	2 OF 5	B	DD	DV11-Ø	K

DRB 107
DEC 16-(325)-1062-3-N871

CUSTOMER PRINT SET				MFG. SET	ELECTRICAL						CUSTOMER PRINT SET				MFG SET	ELECTRICAL					
1					FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	1					FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X					1	D-UA-DV11-Ø-Ø	B	9	BASIC ASSY (DV11)		X					6	D-CS-M7836-Ø-1	#	10	ALU AND TRANSFER BUS	
X						A-SP-DV11-Ø-1	B	44	ENGINEERING SPEC								K-CO-M7836-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			X			A-SP-DV11-Ø-2	A	3	DV11 MODULE TEST PROCEDURE								D-AH-M7836-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			X			A-SP-DV11-Ø-3	B	19	DV11 TEST PROCEDURE								B-MH-M7836-Ø-6		1	MODULE ECO HISTORY	
X			X			A-SP-DV11-Ø-4	A	3	ACCEPTANCE PROCEDURE												
X						A-PL-DV11-Ø-5		1	SHIPPING LIST												
X						A-PL-DV11-Ø-6	A	1	SOFTWARE LIST												
X						D-BD-DV11-Ø-8	A	2	DV11 MODEM CONTROL		X					7	D-CS-M7837-Ø-1	#	11	UNIBUS DATA AND NPR CONTROL	
X						C-IC-DV11-Ø-9	A	1	INTERCONNECTION DV11								K-CO-M7837-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
X						D-BS-DV11-Ø-1Ø	A	8	LINE CARD Ø-3 (SYNCH)								D-AH-M7837-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
X						D-BS-DV11-Ø-11	A	8	LINE CARD 4-7 (SYNCH)								B-MH-M7837-Ø-6		1	MODULE ECO HISTORY	
X						D-BS-DV11-Ø-12	A	8	LINE CARD 8-11 (SYNCH)												
X						D-BS-DV11-Ø-13	A	8	LINE CARD 12-15 (SYNCH)												
C						K-CS-DV11-Ø-14	A	13	MICROPROGRAM LISTING												
X						D-BS-DV11-Ø-15		10	LINE CARD Ø-3 (ASYNCH)												
X						D-BS-DV11-Ø-16		10	LINE CARD 4-7 (ASYNCH)		X					8	D-CS-M7838-Ø-1	#	11	ROM, RAM & BRANCH	
X						D-BS-DV11-Ø-17		10	LINE CARD 8-11 (ASYNCH)								K-CO-M7838-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
X						D-BS-DV11-Ø-18		10	LINE CARD 12-15 (ASYNCH)								D-AH-M7838-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
																	B-MH-M7838-Ø-6		1	MODULE ECO HISTORY	
																	K-CS-M7838-Ø-8		9	23-A1Ø1A2 (ROM LIST)	
																	K-CS-M7838-Ø-9		9	23-A1Ø2A2 (ROM LIST)	
X					2	D-AD-7010834-0-0	#	1	LOGIC ASSY (DV11)								K-CS-M7838-Ø-1Ø		9	23-A1Ø3A2 (ROM LIST)	
X						D-IA-7010835-0-0	#	1	POWER HARNESS (DV11)								K-CS-M7838-Ø-11		9	23-A1Ø4A2 (ROM LIST)	
																	K-CS-M7838-Ø-12		9	23-A1Ø5A2 (ROM LIST)	
																	K-CS-M7838-Ø-13		9	23-A1Ø6A2 (ROM LIST)	
																	K-CS-M7838-Ø-14		9	23-A1Ø7A2 (ROM LIST)	
~~X~~	~~—~~	~~—~~	~~—~~	~~—~~	~~3~~	~~D-AD-7010655-0-0~~	~~#~~	~~1~~	~~WIRED ASSY (DV11)~~								K-CS-M7838-Ø-15		9	23-A1Ø8A2 (ROM LIST)	
~~C~~	~~—~~	~~—~~	~~—~~	~~—~~		~~K-WL-DV11-Ø-7~~	~~A~~	~~1~~	~~WIRE LIST~~												
						~~A-WT-7010655-0~~		~~1~~	~~AWT REVISION STATUS~~												
					3	B-DD-7010655-Ø	A	1	DRAWING DIRECTORY												
											X					9	D-CS-M7839-Ø-1	#	9	SYNCH MUX LINE CARD	
																	K-CO-M7839-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
~~X~~	~~—~~	~~—~~	~~—~~	~~—~~	~~4~~	~~D-IA-7010719-0-0~~	~~#~~	~~1~~	~~BACKPLANE ASSY~~								D-AH-M7839-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
																	B-MH-M7839-Ø-6		1	MODULE ECO HISTORY	
X					5	D-CS-5411420-0-1	#	1	CIRCUIT SCHEMATIC												
						K-CO-5411420-0-4		1	X-Y COORDINATE HOLE LOCATION												
						D-AH-5411420-0-5		1	ASSY/DRILLING HOLE LAYOUT												
						B-MH-5411420-0-6		1	MODULE ECO HISTORY												

CUSTOMER PRINT SET CODES

X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE		SIZE	CODE	NUMBER	REV
BASIC ASSY (DV11)	SHEET 3 OF 5	B	DO	DV11-Ø	K

DRB 108

OEC 14-(325)-1062-2B-R072

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CUSTOMER PRINT SET						ELECTRICAL						CUSTOMER PRINT SET						ELECTRICAL					
1					MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	1					MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X						10	D-CS-M78Ø7-Ø-1	#	7	BUS CONTROL & MUX		X						16	D-CS-H861-Ø-1	#	1	DM11-BB TEST CONNECTOR	
							K-CO-M78Ø7-Ø-4		1	X-Y COORDINATE HOLE LOCATION									K-CO-H861-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
							D-AH-M78Ø7-Ø-5		1	ASSY/DRILLING HOLE LAYOUT									D-AH-H861-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
							B-MH-M78Ø7-Ø-6		1	MODULE ECO HISTORY									B-MH-H861-Ø-6		1	MODULE ECO HISTORY	
X						11	D-CS-M7147-Ø-1	#	7	MODEM CONTROL								17	B-DD-H8612-Ø		2	LINE CARD TEST CONNECTOR	
							K-CO-M7147-Ø-4		1	X-Y COORDINATE HOLE LOCATION		X							C-UA-H8612-Ø-Ø	#	1	LINE CARD TEST CONNECTOR	
							D-AH-M7147-Ø-5		1	ASSY/DRILLING HOLE LAYOUT													
							B-MH-M7147-Ø-6		1	MODULE ECO HISTORY													
																		18	B-DD-M7833-Ø		1	ASYNCH MUX LINE CARD	
												X							D-UA-M7833-Ø-Ø		3	ASYNCH MUX LINE CARD	
						12	C-UA-M92Ø-Ø-Ø		1	INTERNAL BUS CONN. ASSY		X							B-PL-M7833-Ø-Ø		4	ASYNCH MUX LINE CARD	
							A-PL-M92Ø-Ø-Ø		1	INTERNAL BUS CONN. M92Ø		X							D-CS-M7833-Ø-1		10	ASYNCH MUX LINE CARD	
X							C-CS-M92Ø-Ø-1	*	1	INTERNAL BUS CONN. M92Ø									D-MD-5Ø12Ø25-Ø-Ø		3	DRILL AND ETCH DRAWING	
							K-CO-M92Ø-Ø-4		1	X-Y COORDINATE HOLE LOCATION									B-MH-M7833-Ø-6		1	ASYNCH MUX LINE CARD	
							D-AH-M92Ø-Ø-5		1	ASSY/DRILLING HOLE LAYOUT													
												X						11	D-CS-M78Ø8-Ø-1	#	7	MODEM CONTROL	
						13	B-DD-H317-Ø-Ø		3	H317 CABLE BOX ASSY									K-CO-M78Ø8-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
X							D-CS-5411153-0-1	#	3	DV11 DIST. PANEL (C.S.)									D-AH-M78Ø8-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
																			B-MH-M78Ø8-Ø-6		1	MODULE ECO HISTORY	
X						14	C-UA-BCØ8R-Ø-Ø	#	1	BCØ8R I/O CABLE													
X						15	D-CS-H325-Ø-1	#	1	H325 TEST CONNECTOR													
							K-CO-H325-Ø-4		1	X-Y COORDINATE HOLE LOCATION													
							C-AH-H325-Ø-5		1	ASSY/DRILLING HOLE LAYOUT													
							B-MH-H325-Ø-6		1	MODULE ECO HISTORY													

CUSTOMER PRINT SET CODES	TITLE	SHEET	OF	SIZE	CODE	NUMBER	REV
X = PRINT OF DOCUMENT INCLUDED IN PRINT SET C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED	BASIC ASSY (DV11)	4	5	B	DO	DV11-Ø	K

DRB 108

OEC 16-(325)-1062-20-R972

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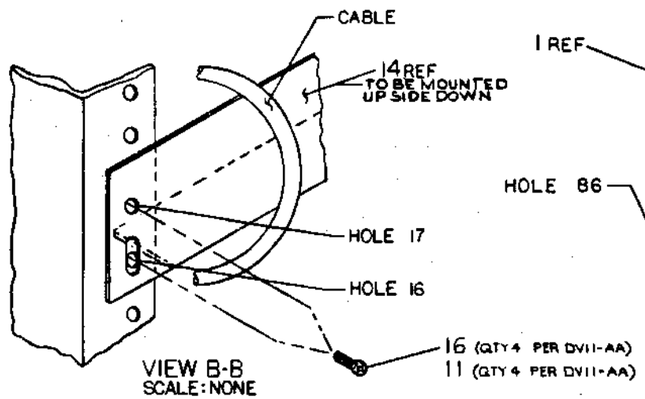
CUSTOMER PRINT SET	MFG. SET	MECHANICAL FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
1		1	D-UA-DV11-Ø-Ø	B	9	BASIC ASSY (DV11)	
			D-MD-7408510-0-0		1	CROSS BAR CABLE BRKT	
			C-IA-7408283-0-0		1	SIDE BAR SUPPORT	
			C-IA-7411632-0-0		1	STRAIN RELIEF	
			C-IA-7411633-0-0		1	CLAMP, STRAIN RELIEF	
		2	D-AD-7010834-0-0		1	LOGIC ASSY (DV11)	
			D-IA-7010835-0-0		1	POWER HARNESS (DV11)	
		3	B-DD-7010655-0		1	DV11 WIRED ASSY	
		4	~~D-IA-7010719-0-0~~		~~1~~	~~BACKPLANE ASSY~~	
		12	C-UA-M92Ø-Ø-Ø		1	INTERNAL BUS CONN ASSY	
			A-PL-M92Ø-Ø-Ø		1	INTERNAL BUS CONN. M92Ø	
			A-DC-7407806-0-0		1	DEC UNIBUS DECAL	
		13	B-DD-H317-Ø		3	H317 CABLE BOX ASSY	
		14	C-UA-BCØ8R-Ø-Ø		1	MODEM I/O CABLE ASSY	

CUSTOMER PRINT SET CODES	
	X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
	C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
	S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

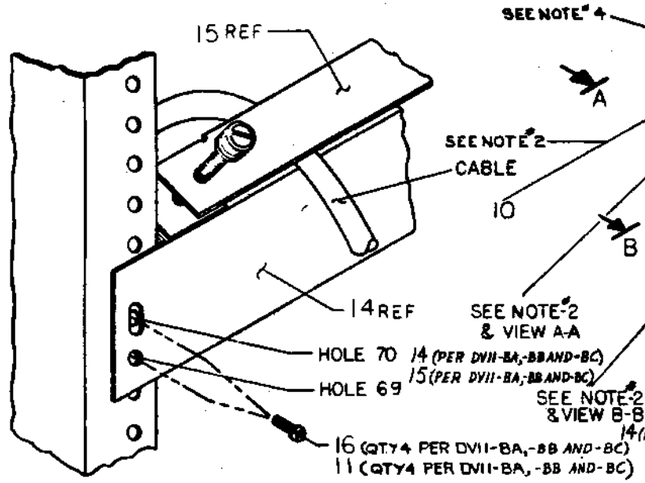
TITLE	SHEET	SIZE	CODE	NUMBER	REV
BASIC ASSY (DV11)	5 OF 5	B	DD	DV11-Ø	K

DRB 108

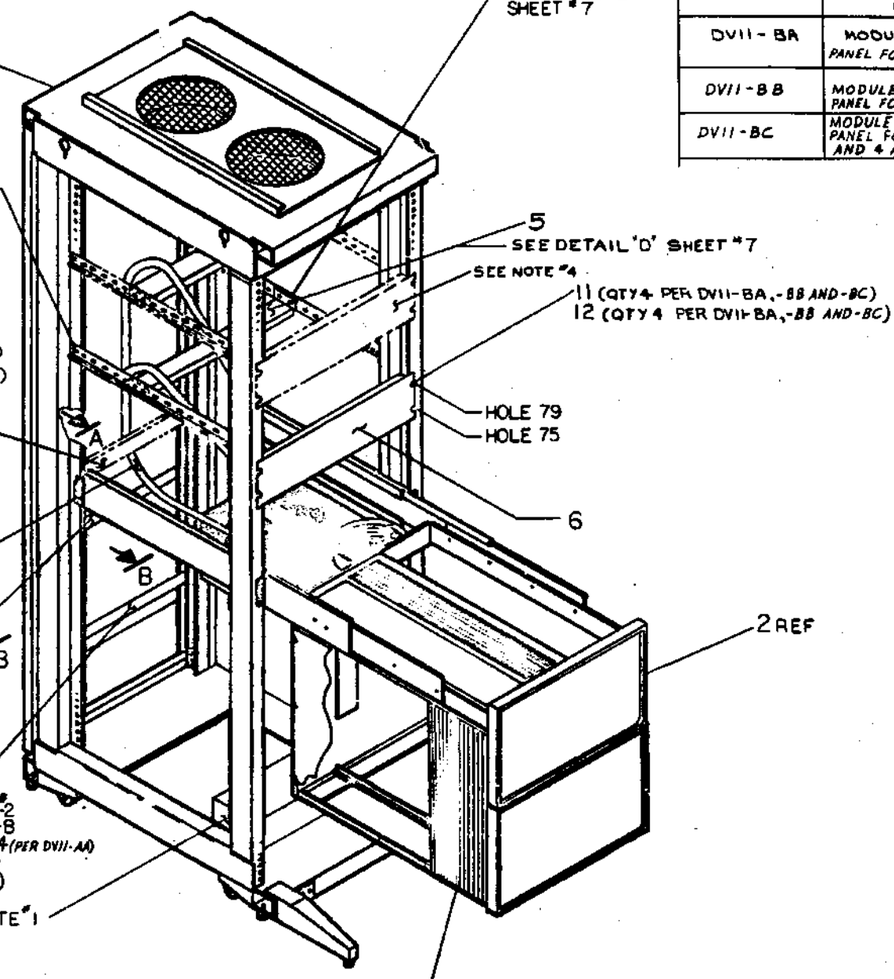
MK



VIEW B-B
SCALE: NONE



VIEW A-A



LEGEND	
NUMBER	VARIATION
DVII-AA	COMM MUX. CONTROL UNIT
DVII-BA	MODULE SET & DIST. PANEL FOR 8 SYNC LINES
DVII-BB	MODULE SET & DIST. PANEL FOR 8 ASYN LINES
DVII-BC	MODULE SET & DIST PANEL FOR 4 SYNC LINES AND 4 ASYN LINES

NOTES:

1. 861 POWER CONTROL MUST BE LOCATED AT FRONT OF CABINET TO ALLOW CABLES FROM ITEM ("6") TO SWEEP BEHIND AND UNDER ITEM "2
2. EACH H960 CONTAINING A DVII SHALL HAVE ONE STRAIN RELIEF (ITEM #4) AND CLAMP (ITEM 15) FOR BC08R CABLES AND ONE STRAIN RELIEF AT THE LOWER REAR OF CABINET, SEE VIEWS A-A AND B-B.
3. A CABINET THAT CONTAINS AN EXPANDER BOX CANNOT HAVE MORE THAN TWO CABLE BOX ASSEMBLIES, ITEM "6) FOR SYSTEMS WITH THREE OR MORE CABLE BOX ASSEMBLIES A SEPERATE CABINET MUST BE USED. UP TO FOUR (4) NELS CAN BE MOUNTED INTO CABINETS WITHOUT AN EXPANDER BOX.
4. 8 LINE SYSTEM IS SHOWN: TO MAKE UP 16 LINE SYSTEM ADD THE FOLLOWING EQUIPMENT (SHOWN WITH PHANTOM LINES): ONE H317-C (ITEM "6) USING MTG HOLES "57, 97, TWO SIDE BAR SUPPORTS (ITEM "8) USING MTG HOLE "99, ONE CROSS BAR CABLE BRKT (ITEM "5), ONE STRAIN RELIEF (ITEM "14), ONE CLAMP, STRAIN RELIEF (ITEM "15) AND NECESSARY MTG HARDWARE

DVII-BC	DVII-BB	DVII-BA	DVII-AA			
1	2	-	-	ASYNCH MUX LINE CARD	D-CS-M7833-0-1	27
1	1	1	-	H325 TEST CONNECTOR	D-CS-H325-0-1	26
-	-	-	1	H861 TEST CONNECTOR	D-CS-H861-0-1	25
2	2	2	-	LINE CARD TEST CONNECTOR	C-UA-H841-2-0-0	24
-	-	-	1	MODEM CONTROL	D-CS-M7147-0-1	23
1	-	2	-	SYNCH MUX LINE CARD	D-CS-M7839-0-1	22
-	-	-	1	ROM, RAM & BRANCH	D-CS-M7838-0-1	21
-	-	-	1	UNIBUS DATA AND NPR CONTROL	D-CS-M7837-0-1	20
-	-	-	1	ALU AND TRANSFER BUS	D-CS-M7836-0-1	19
-	-	-	1	BUS CONTROL & MUX	D-CS-M7567-0-1	18
-	-	-	1	INTERNAL BUS CONN M920	C-UA-M920-0-0	17
8	8	8	4	SCR PHL PAN HD 10-32 X 3/8 LG	9006071-1	16
1	1	1	-	CLAMP, STRAIN RELIEF	C-IA-7411633-00	15
1	1	1	1	STRAIN RELIEF	C-IA-7411632-00	14
-	-	-	4	SCR PHL PAN HD 8-32-1 LG	9006043-1	13
8	8	8	-	SCR PHL PAN HD 10-32-5/8 LG	9006074-1	12
8	8	8	4	NUT, TINNERMAN #10-32	9007786	11
4	4	4	-	I/O CABLE (BC08R)	C-UA-BC08R-12-0	10
-	-	-	1	PRIORITY JUMPER LEVEL #5	C-IA-5408788-00	9
2	2	2	-	SIDE BAR SUPPORT	C-IA-7408283-00	8
-	-	-	4	WASHER, LOCK #8 EXT TOOTH	9008078	7
1	1	1	-	H317-C CABLE BOX ASS'Y	D-UA-H317-C-0	6
1	1	1	-	CROSS BAR CABLE BRK'T.	D-MD-7408510-00	5
8	8	8	-	WASHER LOCK #10 EXT	9007651	4
-	-	-	1	LOGIC ASSY (DVII)	D-AD-7408834-00	3
REF	REF	REF	REF	MOUNTING BOX ASSY	D-UA-BAN-FC-0	2
REF	REF	REF	REF	H960 CABINET	D-UA-H960-CD-0	1
FIRST USED ON OPTION/MODEL		QTY	DESCRIPTION	PART NO.	ITEM NO.	
PDP 11			PARTS LIST			

REVISIONS			
DOC.	CHANGE NO.	REV.	
22	DVII-00004	A	
23	DVII-MK007	B	
24	DVII-MK008	C	

DRAWN	J. MCNAMARA	9-30-74
ENGR	DVII-MK007	10-7-74
ENGR	A. HARRINGTON	10-25-74
ENGR	DVII-MK008	11-27-74
ENGR	A. HARRINGTON	12-6-74

CHKD	Calvary	11-25-74
MFG	[illegible]	9-22-75
QUA	[illegible]	9-22-75
MFG	[illegible]	9-22-75
QUA	[illegible]	9-22-75

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES. TOLERANCES: DECIMALS .XX = ±.01, .XXX = ±.005, X = ±.1; ANGLES ±0° 30'. REMOVE BURRS AND BREAK SHARP CORNERS (UNLESS QUALITY). MATERIAL. FINISH.

NEXT HIGHER ASSY: B-DD-DVII-0

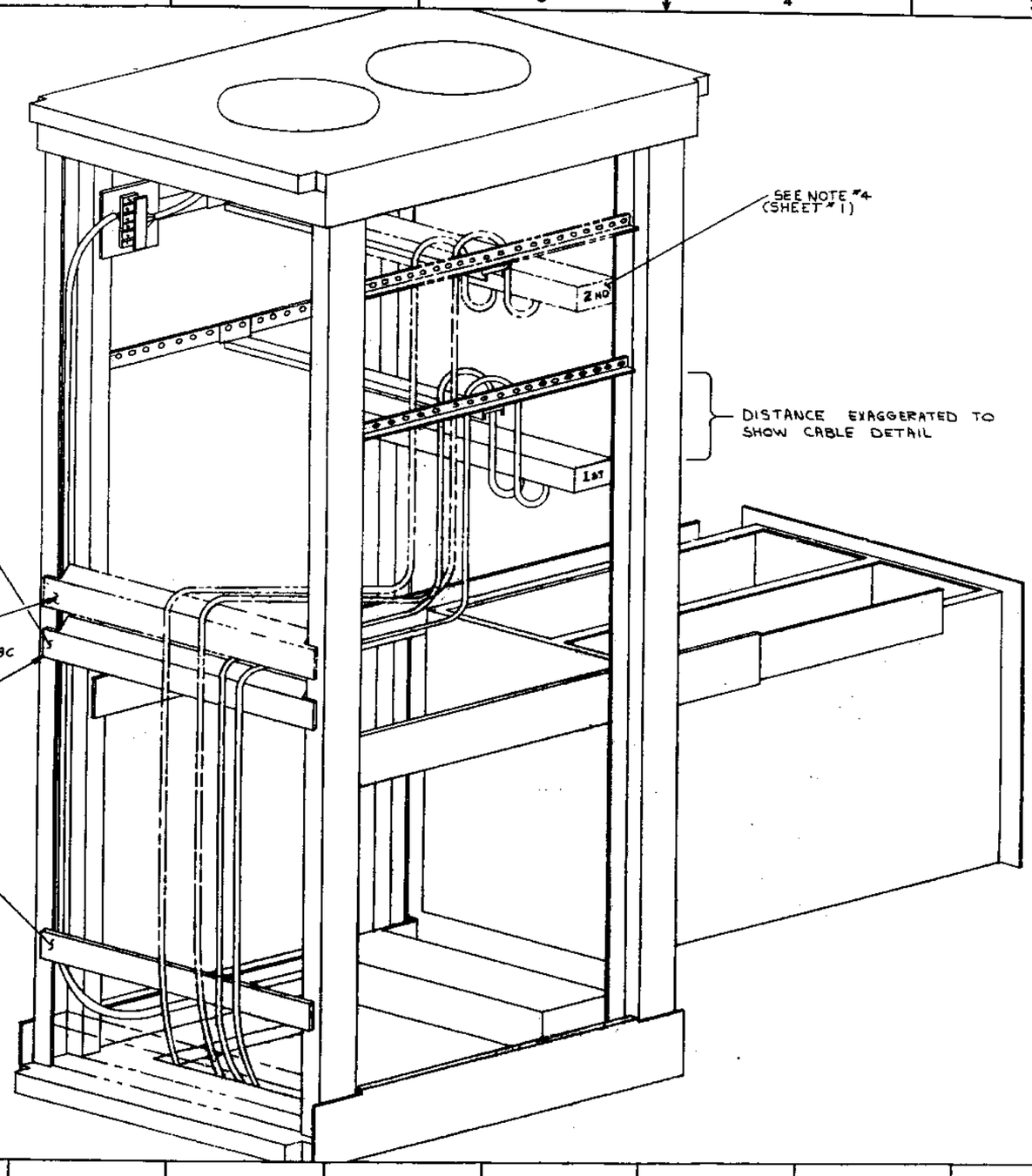
EQUIPMENT CORPORATION

TITLE: BASIC ASSY DVII

SIZE: D | CODE: UA | NUMBER: DVII-0-0 | REV: C

SCALE | SHEET 1 OF 9 | DIST.

DVII-0-0 C



NOTE:
FOR ROUTING BC05D CABLES FROM DISTRIBUTION PANELS TO MODEMS. SEE SHEET #3 FOR ROUTING BC05R CABLES.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	BASIC ASSY DVII		SIZE / CODE	NUMBER / REV.
SCALE NONE	SHEET 2 OF 9		D UA	DVII-Ø-Ø C
			DIST.	

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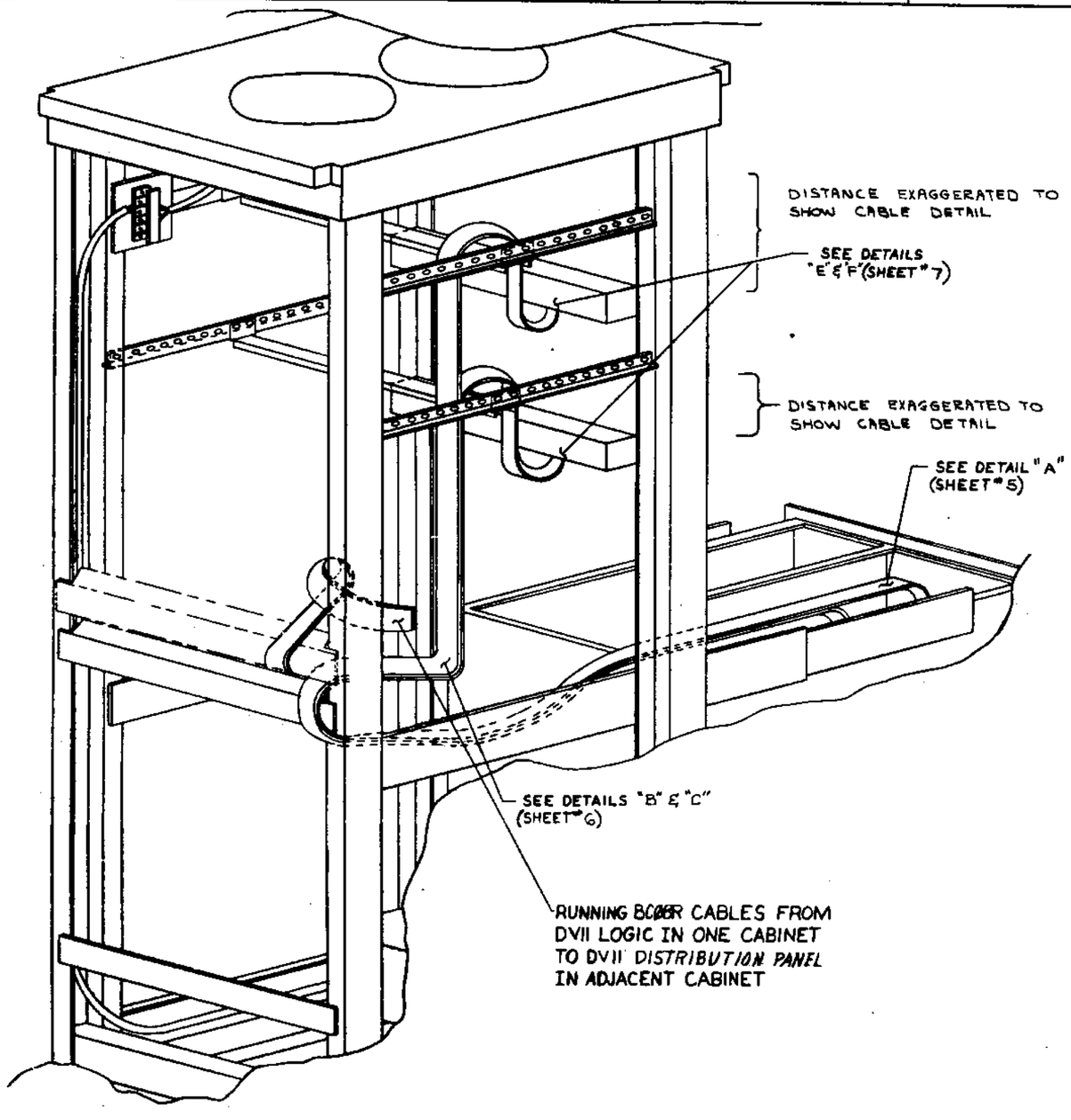


NOTE:
FOR ROUTING BCØ8R CABLES FROM DVII LOGIC & EXPANDER BOX TO DISTRIBUTION PANELS IN SAME CABINET OR ADJACENT CABINET. SEE SHEET # 2 FOR BCØ5D CABLE ROUTING.

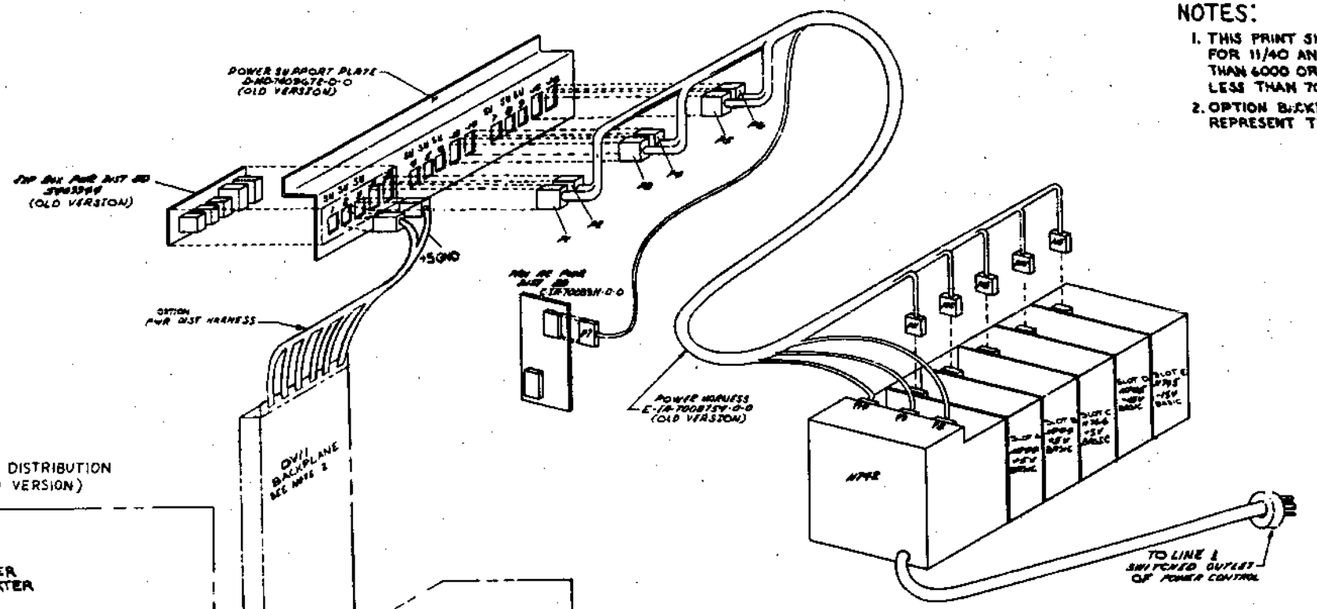
REVISIONS		
CHK	CHANGE NO.	REV.

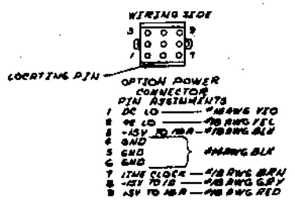
TITLE	BASIC ASSY. DV11		SIZE	CODE	NUMBER	REV.
SCALE	NONE	SHEET 3 OF 9	D	UA	DV11-Ø-Ø	C
			DIST.			

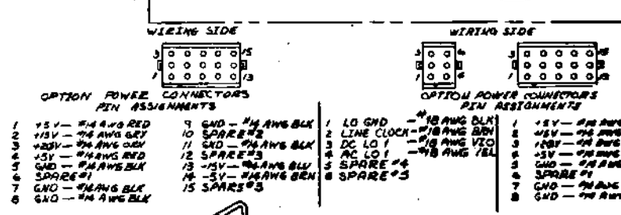
MK

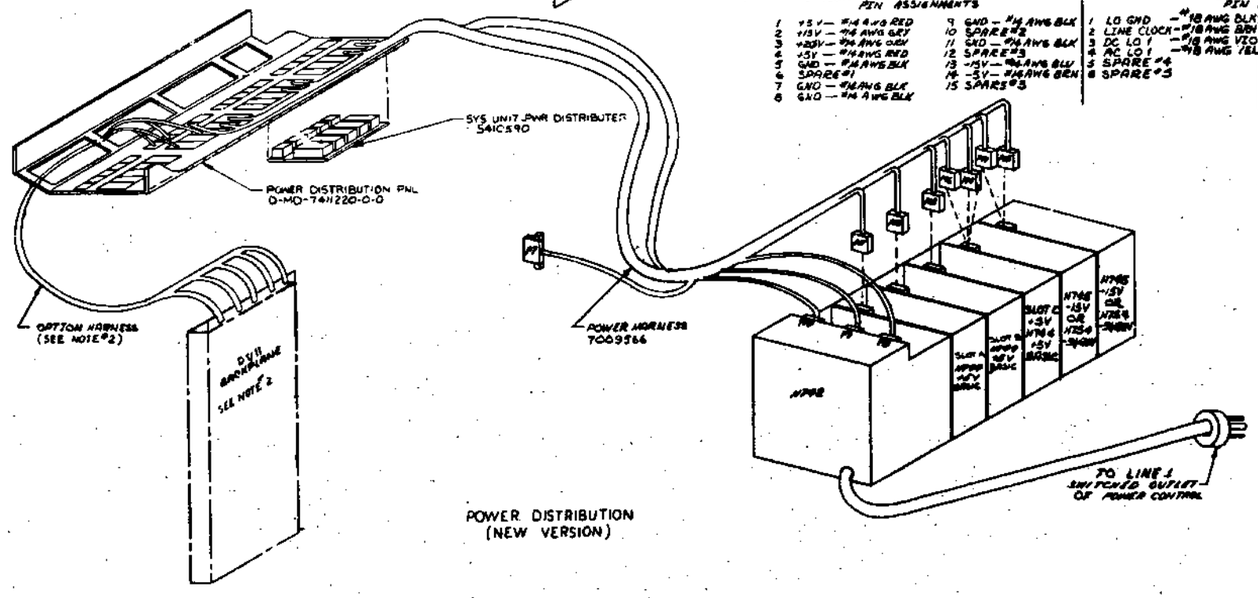
NOTES:
1. THIS PRINT SHOWS HARNESS ARRANGMENTS FOR 11/40 AND 11/35 WITH SERIAL NO. GREATER THAN 6000 OR H960-D,E WITH SERIAL NO. GREATER THAN 7000.
2. OPTION BACKPLANES AND HARNESSES REPRESENT TYPICAL INSTALLATION.

POWER DISTRIBUTION
(OLD VERSION)









POWER DISTRIBUTION
(NEW VERSION)

REVISIONS	REV
CHANGE NO	
CHK	

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
PDP11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES: DECIMALS, ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY √

DRN. C. Mooney DATE 11-19-74
CHK'D Earl Rowe DATE 4-23-75
ENG. DATE
PROJ. ENG. DATE 4-23-75
PROD. R. Will DATE 4-23-75

digital EQUIPMENT CORPORATION

TITLE: BASIC ASSY
DV11

MATERIAL
FINISH
NEXT HIGHER ASSY. B-DD-DV11-0
SCALE
SHEET 4 OF 4

SIZE D | CODE UA | NUMBER DV11-0-0 | REV. C
DIST.

MK

TO DETAIL "C" SHEET #6

TO DETAIL "C" SHEET #6

MODEM CONTROL LEADS FOR LINES 8-11 (UJ10)

MODEM CONTROL LEADS FOR LINES 12-15 (UJ12)

USE H861 (ITEM#25) FOR MODEM CONTROL CABLE, MAINTENANCE (SEE A-SP-DVII-0-3)

25

DATA AND CLOCK, LINES 12-15 (UJ11)

DATA AND CLOCK, LINES 8-11 (UJ9)

DATA AND CLOCK, LINES 4-7 (LJ11)

DATA AND CLOCK, LINES 0-3 (LJ9)

MODEM CONTROL LEADS FOR LINES 4-7 (LJ12)

MODEM CONTROL LEADS FOR LINES 0-3 (LJ10)

SHIELD SIDE

M7147 OR M7806

M7833 MODULES OR M7839 MODULES

M7807

H8612 CONNECTOR (ITEM#24) INSERTED IN PLACE OF CABLE FOR MAINTENANCE (SEE A-SP-DVII-0-3)

24

DETAIL "A"

ALL CABLES SHOWN ARE BC08R

FOR MODULE PLACEMENT INFORMATION, SEE SHEET#9

REVISIONS		
CHG	CHANGE NO.	REV.

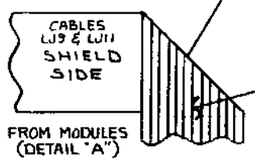
APPLICATION: DVII-AA,BA,BB,BC

TITLE: BASIC ASSY DVII		SIZE: D	CODE: UA	NUMBER: DVII-0-0
SCALE: NONE	SHEET 5 OF 9	DIST.		REV. C

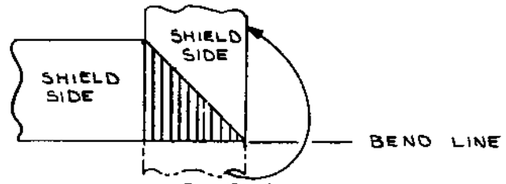
MK

FOLD LJ9 & LJ11 TOGETHER AS ONE CABLE

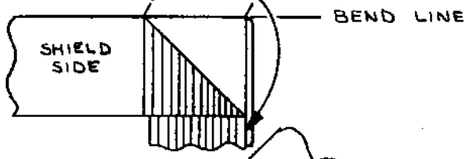
STEP #1



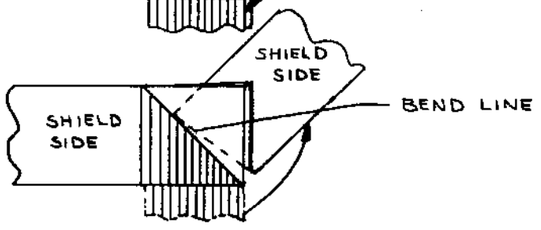
STEP #2



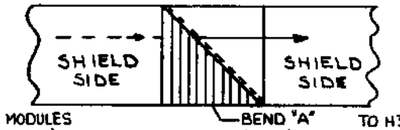
STEP #3



STEP #4

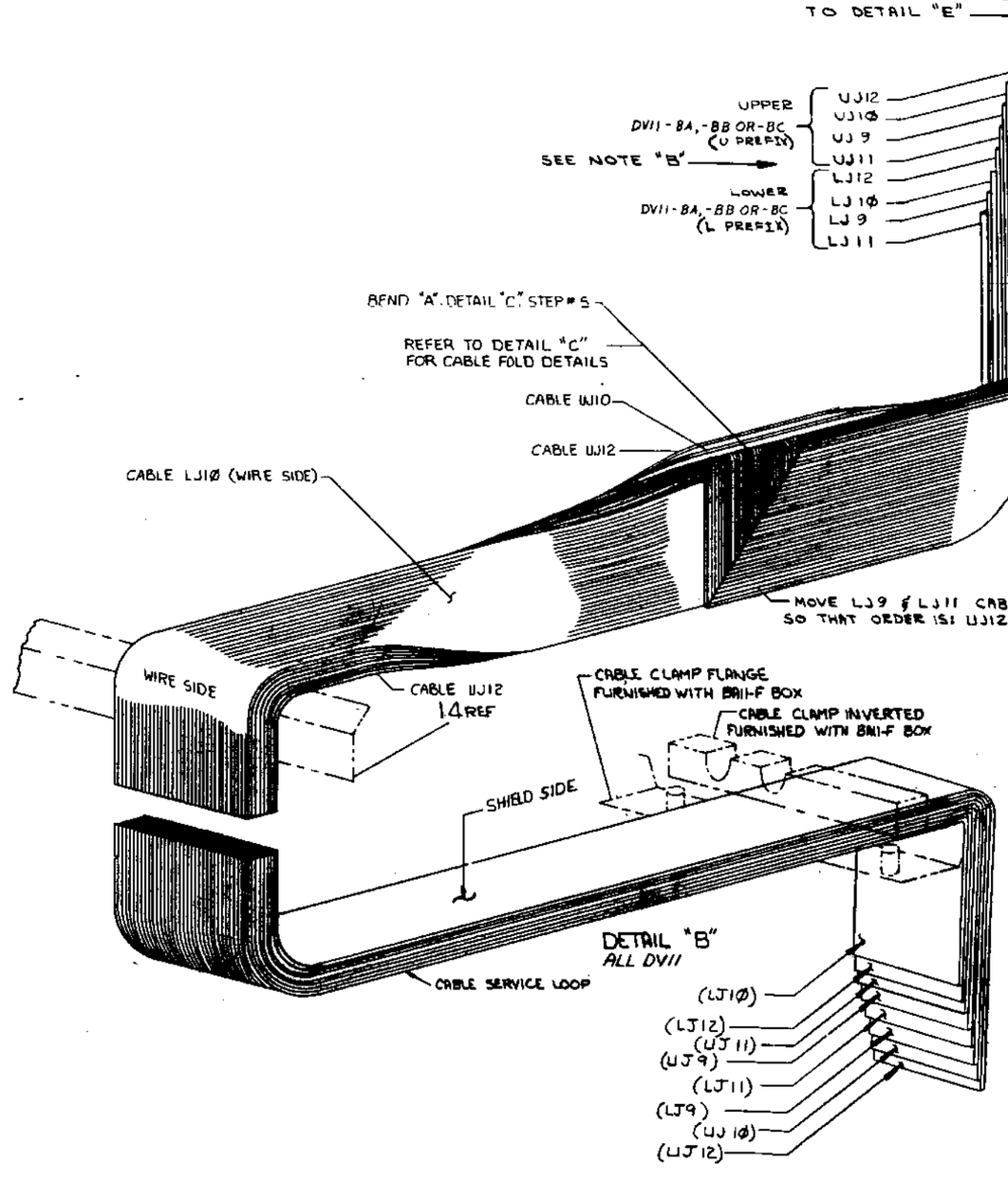


STEP #5



DETAIL "C"

NOTE THAT UJ9, UJ11, LJ12, LJ10 CABLES CAN PASS THROUGH THE FOLDED AREA AS SHOWN BY DOTTED ARROW AND SOLID ARROW. NOTE THAT FOLDED CABLE IS INSTALLED IN DETAIL "B" UPSIDE DOWN FROM VIEW SHOWN IN DETAIL "C" - REFER TO POSITION OF BEND "A".



DETAIL "B"
ALL DV11

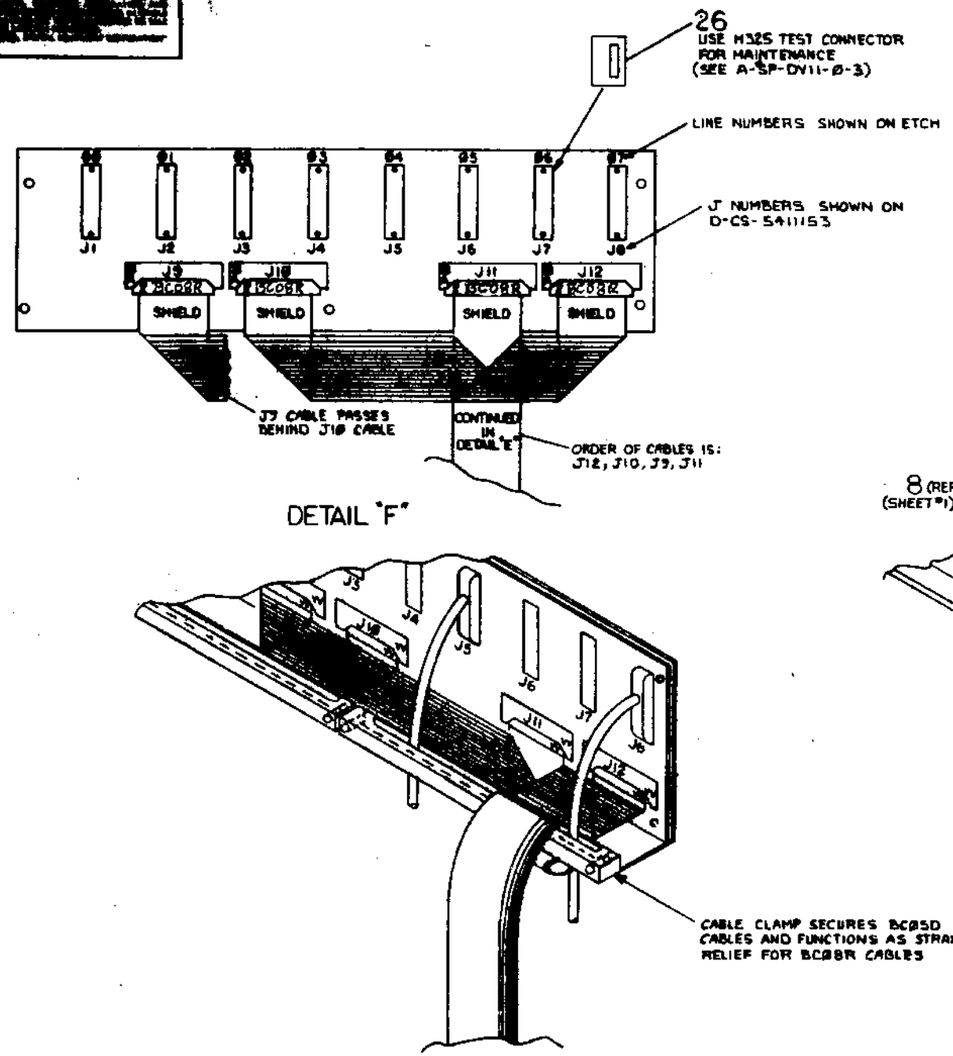
NOTES:
A. INSTALL VINYL FOAM BETWEEN UNIBUS & OTHER CABLES WHERE UNIBUS GOES THRU CABLE CLAMPS.
B. DV11 DISTRIBUTION PANEL (H317C) CONTAINING D-CS-5411153) REFER TO DETAILS "E" AND "F" ON SHEET # 7.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	BASIC ASSY. DV11		
SIZE	CODE	NUMBER	REV.
D	UA	DV11-0-0	C
SCALE	NONE	SHEET 6 OF 9	DIST.

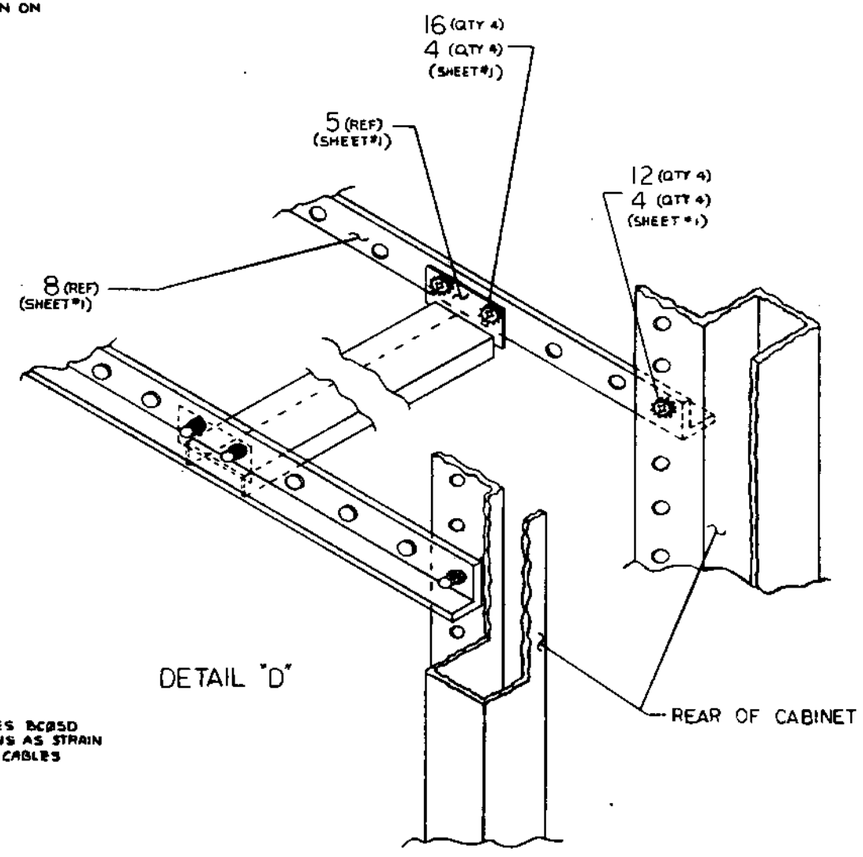
DLA DV11-0-0 C

MK



DETAIL "F"

DETAIL "E"
CONTINUED FROM DETAIL "F"



DETAIL "D"

REVISIONS		
DATE	CHANGE REQ.	REV.

TITLE	BASIC ASSY DV11	SIZE/CODE	D UA
SCALE	NONE	SHEET	7 OF 9
NUMBER	DV11-Ø-Ø	REV.	C
DIST.			

MK

VECTORS :

OCTAL TO SWITCH POSITION CONVERSIONS FOR M7887

	VECTORS 8	7	6	5	4	3	2	
300	ON	OFF	OFF	ON	ON	ON	*	*VECTOR BIT 2 IS CONTROLLED BY DV11 LOGIC
304	ON	OFF	OFF	ON	ON	ON	*	
310	ON	OFF	OFF	ON	ON	OFF	*	
314	ON	OFF	OFF	ON	ON	OFF	*	
320	ON	OFF	OFF	ON	OFF	ON	*	
324	ON	OFF	OFF	ON	OFF	ON	*	
330	ON	OFF	OFF	ON	OFF	OFF	*	
334	ON	OFF	OFF	ON	OFF	OFF	*	
340	ON	OFF	OFF	OFF	ON	ON	*	
344	ON	OFF	OFF	OFF	ON	ON	*	
350	ON	OFF	OFF	OFF	ON	OFF	*	
354	ON	OFF	OFF	OFF	ON	OFF	*	
360	ON	OFF	OFF	OFF	OFF	ON	*	
364	ON	OFF	OFF	OFF	OFF	ON	*	
370	ON	OFF	OFF	OFF	OFF	OFF	*	
374	ON	OFF	OFF	OFF	OFF	OFF	*	
400	OFF	ON	ON	ON	ON	ON	*	
410	OFF	ON	ON	ON	ON	OFF	*	
420	OFF	ON	ON	ON	OFF	ON	*	
430	OFF	ON	ON	ON	OFF	OFF	*	

OCTAL TO JUMPER CONVERSIONS FOR M7887

	VECTORS 8	7	6	5	4	3	2
300	OUT	IN	IN	OUT	OUT	OUT	OUT
304	OUT	IN	IN	OUT	OUT	OUT	IN
310	OUT	IN	IN	OUT	OUT	IN	OUT
314	OUT	IN	IN	OUT	OUT	IN	IN
320	OUT	IN	IN	OUT	IN	OUT	OUT
324	OUT	IN	IN	OUT	IN	OUT	IN

PDP 11 BIT TO OCTAL DIGIT CORRESPONDENCE

BIT	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EXAMPLE	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
OCTAL DIGIT	6TH			5TH			4TH			3RD			2ND			1ST		
EXAMPLE	7			7			5			0			0			0		

NOTE I/O DEVICE ADDRESS IN #11 LITERATURE ARE VARIOUSLY GIVEN AS 760 000 THRU 777 777 AND AS 160 000 THRU 177 777
THESE ARE EQUIVALENT IN MACHINES WITHOUT MEMORY MANAGEMENT. WHENEVER BITS 15,14, AND 13 ARE ALL "1" (16X XXX OR 17X XXX) THE PROCESSOR ALSO MARES BITS 17 AND 16 "1" (76X XXX OR 77X XXX) [ON MACHINES WITH MEMORY MANAGEMENT I/O DEVICE ADDRESSES ARE IN PHYSICAL MEMORY AT 760 000 THRU 777 777. THEY ARE ONLY AVAILABLE TO A PROGRAM IF SOME VIRTUAL ADDRESS AREA IS MAPPED INTO THIS PHYSICAL AREA]

JUMPERS AND MODIFICATIONS

BR LEVEL SELECT BOARD - M7837
BR PLUG SHOULD BE 5400778 (LEVEL #5)
(AS SUPPLIED STANDARD)

ADDRESSES:

M7838
DV11 DATA CONTROL ADDRESS OFF-1, ON-0
BITS 9,11,12 ARE OFF
BIT 10,15 ON

		8	7	6	5	4
775	000	ON	ON	ON	ON	ON
	040	ON	ON	ON	OFF	ON
	100	ON	ON	OFF	ON	ON
	140	ON	ON	OFF	OFF	ON

M7887
DV11 MODEM CONTROL ADDRESS OUT-1, IN-0
BITS 9,11,12 ARE OUT
BIT 10,15 IN

		8	7	6	5	4	3
775	020	IN	IN	IN	IN	OUT	IN
	060	IN	IN	IN	OUT	OUT	IN
	120	IN	IN	OUT	IN	OUT	IN
	160	IN	IN	OUT	OUT	OUT	IN

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
BASIC ASSY DV11	D	UA	DV11-0-0	C
SCALE — SHEET 5 OF 9	DIST.			

MK

VIEW FROM SLOT SIDE

NOTES:

1. IF END OF BUS REPLACE M92Ø WITH M93Ø.
2. IF LAST UNIT IN BASIC BOX REPLACE M92Ø WITH BC11A CABLE END WHEN EXPANDING TO PHERIPHERAL BOX.
3. IF FIRST UNIT IN EXPANDER BOX REPLACE M92Ø WITH BC11A CABLE END.
4. TWO LINE CARDS ITEM #22 OR #27 ARE LOCATED IN SLOTS 5&6 FOR THE FIRST LINE CARD VARIATION: FOR THE SECOND LINE CARD VARIATION LOCATE TWO MORE LINE CARDS IN SLOTS 7&8.
5. M7147 IS USED ON REVISION B OR LATER TO CURE FALSE REPORTING OF TRANSITIONS ON MODEM CONTROL LINES.

F	E	D	C	B	A		
M7147 OR M7808 MODEM CONTROL SCAN AND MUX (NOTE 5)				M92Ø UNIBUS CONNECTOR NOTE #1 & #2			23
M7833 ASYNC MUX LINE CARD	OR	M7839 SYNC MUX LINE CARD LINES 12-15				9	22,27 SEE NOTE #4
M7833 ASYNC MUX LINE CARD	OR	M7839 SYNC MUX LINE CARD LINES 8-11				8	22,27 SEE NOTE #4
M7833 ASYNC MUX LINE CARD	OR	M7839 SYNC MUX LINE CARD LINES 4-7				7	22,27 SEE NOTE #4
M7833 ASYNC MUX LINE CARD	OR	M7839 SYNC MUX LINE CARD LINES Ø-3				6	22,27 SEE NOTE #4
M7838 ROM RAM AND BRANCH						5	21
M7837 UNIBUS DATA AND NPR CONTROL						4	20
M7836 ALU AND TRANSFER BUS						3	19
M78Ø7 BUS CONTROL AND MUX				M92Ø UNIBUS CONNECTOR (NOTE #3)		2	
F	E	D	C	B	A	1	
			18		17		

REVISIONS		
CHG.	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
BASIC ASSY DV11	D	UA	DV11-Ø-Ø	C
SCALE — SHEET 9 OF 9	DIST.			

MK

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE May 17,1974

TITLE DV11 Communications Multiplexor

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	00001	J.McNAMARA	5-75		5/14/75
B	ECO CHANGE	00004	W.SMITH	4-76		5/28/76

ENG	APPD	SIZE	CODE	NUMBER	REV
5-23-74	5-23-74	A	SP	DV11-0-1	B

DEC 16-(392)-1079-N971
DRA 107

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DV11 Communications Multiplexor

General Description

The DV11 is a sixteen line multiplexor for the PDP-11 family of computers.

The DV11 is designed to achieve very high throughput (16 lines times 1200 characters per second times two directions equals 38,400 characters per second in DDCMP mode, 26,000 characters per second in character oriented protocols) by the use of NPR transfers on both transmission and reception. The use of control bytes stored in core tables makes the DV11 essentially a classical state machine and permits it to achieve hardware throughput capabilities without committing the hardware design to any specific protocol.

The DV11 is housed in a nine slot double system unit and includes a distribution panel for each eight line group and a complete sixteen line modem control similar to the DM11-BB modem control.

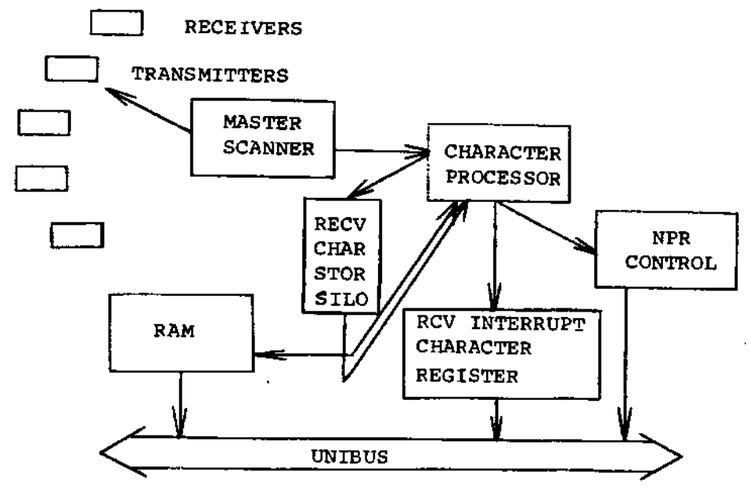


Figure 1: Block Diagram of DV11

SIZE	CODE	NUMBER	REV
A	SP	DV11-0-1	B

DEC FORM NO OEC 16-(381)-1022-N370
DRA 108

A DV11-AA is the option designation for the DV11 control logic and double system unit. No lines or distribution panels are implemented with this option. Three option designations are provided for ordering the line cards in eight line groups. Each group contains a distribution panel in addition to the selection type of line cards. Line cards for eight synchronous lines are designated a DV11-BA option. Line cards for eight asynchronous lines are designated a DV11-BB option. For four synchronous, four asynchronous line card mixture, DV11-BC is the option designation.

The basic elements of the DV11 are shown in figure 1.

The Receivers (16) assemble characters received from serial communications lines and assert a flag as each character is received. The Transmitters (16) disassemble characters and transmit them on serial communications lines and assert a flag whenever they can accept another character for transmission.

The Master Scanner sequentially checks the Receivers and Transmitters for each line to see if flags exist.

The Character Processor is a ROM controlled microprocessor which handles all characters received or transmitted by the DV11. It controls all non-Unibus data transfers and steps the Master Scanner. Except for those occasions where a Unibus instruction or NPR transfer involving the DV11 is taking place, the microprocessor never stops.

The Received Character Storage Silo is a first-in, first-out storage buffer. While most characters received by the DV11 will propagate through this buffer and be directly transferred to PDP-11 core by means of an NPR transfer, the occasion may arise when the attention of the PDP-11 program is required before this is done in the case of a particular character. To prevent the Receivers from experiencing data overruns during the interval that the DV11 is awaiting program attention, the microprogram will continue to load the received characters into the first-in first-out buffer, but the action of the Character Processor in withdrawing characters from the buffer will cease until the PDP-11 program responds to the interrupt caused by the special character at the bottom of the silo buffer.

The character which requires PDP-11 program attention is copied into the Next Received Character Register at the time the aforementioned interrupt is generated.

The RCV Interrupt Character Register is a Unibus addressable register used by the microprogram to show the PDP-11 program any received character, along with line number and error flags, for which the microprogram requires assistance in processing.

The NPR Control is the hardware which the microprogram uses to gain control of the Unibus in order to store received characters, obtain characters for transmission, and obtain control bytes that direct the character processing.

The RAM contains the current addresses and byte counts used in the aforementioned NPR transfers. The initial values are loaded by the PDP-11 program via the Unibus and these values are subsequently updated by the microprogram. The RAM also contains a line protocol byte for each line by which the PDP-11 program can specify what action is to be taken when the byte count reaches zero and what type of block check polynomial should be used. In addition, a line state byte is stored for each line providing a snapshot of what microprogram activity is in progress on a particular line.

Operation

The Master Scanner checks both Receivers and Transmitters for flags indicating that characters are to be read from them (receivers) or loaded into them (transmitters).

If the Master Scanner finds a receiver flag, the microprocessor performs a data transfer operation reading a character from that Receiver and loading it into the Received Character Storage Silo.

If the Master Scanner finds a transmitter flag, the microprocessor utilizes the NPR Control to obtain a character from core and to obtain a control byte from core. The control byte contains information regarding any special treatment the character is to receive during transmission.

After any such treatment, the microprocessor loads that character into that Transmitter for transmission.

In addition to servicing Receiver flags and Transmitter flags, the microprocessor also retrieves characters from the Received Character Storage Silo. As removed from the character storage silo, each character is accompanied by its line number and error flags.

If any of the error flags are set, the microprocessor places the character in the Receiver Interrupt Character Register and generates an interrupt. If there are no error flags set, the microprocessor appends "Mode bits*" to the high order end of the character and uses the resultant expanded character as an offset in a core table from which a control byte appropriate to that character and mode is retrieved. The control byte indicates whether or not an interrupt should be generated (i.e., special character), whether or not the character should be included in the block check character calculation, whether or not the character should be stored in the core message table for that line, and whether or not the "Mode bits" for that line should be changed. In those cases where the microprocessor deposits a character in the Receiver Interrupt Character Register (either because of error flags or as a result of information in the control byte), no further action** is taken by the microprocessor in retrieving characters from the Received Character Storage Silo until so directed by the setting of System Control Register bit Ø8 - Receiver Interrupt Response Complete.

The details of DV11 operation are best understood by reference to the register bit explanations which follow on sheets 6 to 36. Most bits are the same for synchronous and asynchronous applications, but where they differ, notes refer the reader to the appropriate information on sheets 37 to 44.

*Mode bits are always loaded into bits Ø8, Ø9, and 1Ø. Thus, the core tables containing the mode bytes always contain 256 bytes for each mode - i.e., all received characters are treated as 8-bit characters.
**If the program is too tardy in servicing the Receiver Interrupt Character Register, the silo will overflow - See System Control Register (address XØØ) bit 14.

System Control Register - Address XØØ

The System Control Register is a byte addressable register. The bit assignment is as follows:

Bit	Description
ØØ	Microprocessor GO This bit when set permits the DV11 to cycle the Microprocessor that controls the DV11. This is read/write, CLEARED by Initialize. System programs must set this bit for the DV11 to function.
Ø1	ROM Single Step (For Maintenance Use) This bit permits the PDP-11 program to execute one ROM cycle (only). This bit is read/write, cleared by Initialize. When the ROM cycle begins, this bit is automatically cleared.
Ø2	ROM Branch Disable (For Maintenance Use) This bit when set assures that the DV11 microcode will not branch if the ROM cycles to a branch instruction while this bit is set. This bit is read/write, cleared by Initialize.
Ø3	ROM Data Source Select (For Maintenance Use) This bit when set enables the ROM Data Register (a microprocessor register) to be loaded from the Unibus by doing a write into the Special Functions Register (address X12). This bit is read/write, cleared by Initialize.
Ø4-Ø5	Memory Extension The information stored in these bits becomes bits 16 and 17 respectively of any current address or control table base address loaded by the program into the RAM. These bits are read/write (cleared by Initialize) but when read, represent only the status of bits 4 and 5 of the System Control Register, not the status of address bits 16 and 17 of the selected line. See the Line Control Register for further information. This arrangement permits interrupt service routines to save the contents of the System Control Register accurately.

Ø6 Receiver Interrupt Enable

This bit, when set, permits the setting of bit 7 to generate an interrupt request. RW Init. clears.

Ø7 Receiver Interrupt (Vector A)

This bit, when set, indicates that the microprocessor has either (1) withdrawn a byte from a core control table indicating that an interrupt should be generated for the character presently being processed, or (2) the character presently being processed has one or more of its associated error flags set or (3) experienced a zero byte count, non-existant memory location, or memory parity error in processing this characater. The program should respond to this interrupt by setting SCRØ8. (The program might wish to alter the Control Byte Storage Register before setting SCRØ8.) This bit is read only except when SCRØ9 is set. It is cleared by Initialize.

Ø8 Receiver Interrupt Response

The setting of this bit clears SCRØ7 and allows the microprocessor to take action on the character in the RICR (according to the information stored in the Receiver Control Byte Storage Register) and to continue removing characters from the receive silo for processing.

Ø9 Bit 7 & 15 Write Enable (Maintenance)

This bit, when set, permits the program to write bits 7 and 15 of this register. This bit is read/write, cleared by Initialize. This register must be word addressed when and while this bit (SCRØ9) is set.

1Ø NPR Status Overflow Interrupt

This bit, when set, indicates that the DV11 hardware checked the NPR status register (a silo) and found that there was no room due to insufficient program attention to servicing this register. All DV11 transmitter action in performing NPR trasnfers will cease until this condition is corrected. This bit is read/write, cleared by Initialize.

11 Master Clear

This bit, when set, generates "Initialize" within the DV11 data handling sections (It does not affect the modem control.). The silos (both received character and NPR status*) are cleared. The secondary registers are not cleared. This bit is read/write and is self-clearing.

12 Storage Interrupt Enable

This bit, when set, permits the setting of bit 1Ø to generate an interrupt request. Read/write, cleared by Initialize.

13 NPR Status Interrupt Enable

This bit, when set, permits the setting of bit 15 to generate an interrupt request. This bit is read/write, cleared by Initialize.

14 Unused

15 NPR Status Interrupt (Vector B)

This bit is set whenever there is one or more entries in the NPR Status Register, which is a silo-type register. The reading of that read-once register clears this bit, but it resets again if a new entry moves down into the register to replace the previously read entry. This bit is read only except when **SCRØ9** is set, when it is read/write. This bit is cleared by Initialize

*The NPR Status Register Bit 15 ("Entry Present") is cleared by Initialize; the other bits are not.

Receiver Interrupt Character Register - Address XØ2

This register is read only, cleared by Initialize.

Bits	Description
ØØ-Ø7	Interrupting Character These bits contain the interrupting character, right justified. The least significant bit is bit ØØ. On parity-equipped characters, less than 8 bits, the parity bit will appear immediately to the left of the highest order bit in the character. See special note associated with Error Code 0101 below.
Ø8-11	Line Number The bits indicate the line number on which the interrupting character was received. Bit 8 is the least significant bit.
12-15	Error Code These bits indicate the reason that the character shown in bits ØØ-Ø7 generated an interrupt request. Refer to Chart.

Error Code Bit				Meaning
15	14	13	12	
0	0	0	0	SPECIAL CHARACTER The receipt of this character caused the seizure of a control byte which had bit ØØ (generate interrupt) set indicating that this is a special character.
0	0	0	1	PARITY ERROR This character was received with a parity sense opposite to that selected for this line by the parity sense switches on the line card.
0	0	1	0	OVERRUN The character(s) preceding this character on this line has (have) been lost due to failure of the DV11 receiver system to keep up with the incoming character rate on this line.

Error Code Bit				Meaning
15	14	13	12	
0	0	1	1	PARITY ERROR AND OVERRUN (SEE PREVIOUS LISTINGS) (FOR ASYNCHRONOUS USE, SEE SHEETS 42&43)
0	1	0	0	BYTE COUNT WARNING This character has been stored, but it is the last character that can be stored for this line as the byte count is now zero for reception on this line.
0	1	0	1	BLOCK CHECK COMPLETED A block of text or data and the associated block check characters have been received and the program should now check the accumulated receiver block check; the DV11 presents the OR of the high and low bytes of that register in bits ØØ-Ø7 of this register
0	1	1	0	UNDEFINED
0	1	1	1	UNDEFINED
1	0	0	0	BYTE COUNT ZERO This character was not stored, as the byte count for reception on this line is zero and thus there is no place to store this character.
1	0	0	1	UNDEFINED
1	0	1	0	UNDEFINED
1	0	1	1	UNDEFINED
1	1	0	0	PROCESSING ERROR ØØ A nonexistant memory time-out occurred when the DV11 attempted to store this character.
1	1	0	1	PROCESSING ERROR Ø1 A nonexistent memory time-out occurred when the DV11 attempted to obtain the control byte associated with this character.
1	1	1	0	PROCESSING ERROR 1Ø A memory parity error occurred when the DV11 attempted to store this character. (NOTE: this error should never occur, as the memory parity logic gives alarms only on DATO transfers).
1	1	1	1	PROCESSING ERROR 11 A memory parity error occurred when the DV11 attempted to obtain the control byte associated with this character.

In response to a receiver interrupt (SCRØ7), the PDP-11 Program should examine this register (Receiver Interrupt Character Register), make any desired changes in the Receiver Control Byte Storage Register, and then set SCRØ8.

Note: Line Control Register bit definitions for synchronous lines are shown on sheets 11 to 15. Line Control Register bit definitions for asynchronous lines are shown on sheets 38 to 42.

Line Control Register - Address Ø4

This register controls the maintenance features associated with each line in the DV11 and provides an opportunity for the PDP-11 program to read the extended address bits for each line.

The following bits are read only and may be read only after the appropriate bits in the Secondary Register Selection Register have been conditioned to select the appropriate secondary register for the appropriate line: Ø4, Ø5, and Ø7.

The following bits are read/write, but the read is only a read of the most recently written entry into this bit of this register, not a read of the status of this bit for this line (This is referred to as "write/limited read".). A write into one of these bits does not affect the selected line unless bit 15 is also set: Ø8, Ø9, 1Ø, 11, 12, 13, and 14. An example will clarify this. The PDP-11 program can read and write LPR 13 (Receiver Enable) at any time, but reading will only tell the program whether or not LPR 13 is set, not whether or not a particular line's receiver is enabled or not. In addition, the line specified in Secondary Register Selection Register bits ØØ-Ø3 will not be placed in Receiver Enable mode merely by the writing of bit 13 of the LPR. Rather, the line will be placed in Receiver Enable mode only when bit 15 is set in addition (or subsequent to) bit 13 being set.

The line number to which the maintenance information, search sync, or extended address applies is specified by bits ØØ-Ø3 of the Secondary Register Selection Register.

The bit functional assignments are as follows:

ØØ-Ø1 Reserved for Maintenance
(Caution: Various bits may appear here during normal DV11 operation.)

Ø2-Ø3 Unused

Ø4-Ø5 Extended Address Read (Read Only)

For the line number entered in bits ØØ-Ø3 of the Secondary Register Selection Register these bits represent the status of bits 16 and 17 of the secondary register specified by bits Ø8-11 of the Secondary Register Selection Register. This permits the PDP-11 program to read the Extended Address bits of the Current Address and Control Table Base Address entries in the RAM.

Ø6 Unused

Ø7 Maintenance Bit Window (Maintenance)

When in the maintenance mode Ø1 only, this bit can be used to monitor the input to the receiver logic of the selected line. The stimulus that creates the input could be either the maintenance Data bit or the serial output of the transmitter, depending on the state of the Transmitter Disable bit. Program read only. This bit does not represent the status of the selected line.

Ø8 Maintenance Clock Pulse (Maintenance) (See Bit 15)

This bit is used to simulate the Transmitter and Receiver Clock. It is used for diagnostic purposes only. With this bit, the diagnostic has the ability to single step the interface. Setting this bit causes the transmitter to transfer a bit from the internal shift register to the output of the transmitter and causes the receiver to transfer the input of the receiver into the internal shift register.

This bit is program write only and is self-clearing. It pulses all DV11 lines that are in maintenance mode Ø1.

Ø9 Transmitter Disable (Maintenance) (See Bit 15)

This bit, when set, disables the output of this line's Synchronous Transmitter. In this way data from the Maintenance Data bit may be entered into the receiver. This bit is used only for maintenance purposes and is write/limited read.

11 & 12 Maintenance Mode Select (See Bit 15)

These bits are used to select any one of the three maintenance modes:

	BIT SETTING 12	11
1. Internal Maintenance Mode	0	1
2. External Maintenance Mode	1	0
3. Internal Maintenance Mode for Systems Testing	1	1
4. Normal Operation	0	0

Internal Maintenance Mode (Ø1)

Internal Maintenance Mode clocking comes from the Maintenance Clock Pulse bit (bit Ø8) driven via the program. While using this mode, the following EIA level converters are disabled (This is done so that the majority of the logic can be diagnosed without disconnecting the modem cable.):

Receiver Clock
Transmitter Clock
Receiver Data
Transmitter Data

Transmitted data is looped to received data on a TTL basis.

External Maintenance Mode (1Ø)

When in the external maintenance mode, all lines connected to the data set must be removed at the data set interface. A special connector replaces the connector of the data set. The function of the special connector is to turn around specified signals after level conversion and bring them back to the DV11 as simulated inputs.

Clocking in this mode is under control of internal DV11 clocks in the same way as Internal Maintenance Mode 11.

Internal Maintenance Mode for Systems Testing (11)

With bits 12 and 11 both set to a one (mode 11), the internal maintenance mode provides internal clocking for the receiver and transmitter. The clocking rate is controlled by switches on the DV11 line cards. Mode 11 will be the same as mode Ø1 with respect to data set control leads and TTL data loopback. The only difference is that in mode 11 the receiver and transmitter clocking is derived from internal clocks.

Bits 11 and 12 are write/limited read.

NOTE: If bits 12 and 11 are zero, normal operating mode is assumed.

13 Receiver Enable (See bit 15)

When this bit is set by the program, a sync search is initiated on this line by the receiver logic. After an initialize, this bit must be set by the program before any reception can begin on this line - i.e., Receiver Active (See "Line State" secondary register) will not set unless this bit has been set.

A switch for each line determines whether the receiver searches for one sync character or for two in a row.

A successful sync search results in the setting of Receiver Active (Line State Bit ØØ) for this line.

This bit is write/limited read.

NOTE: Should it be desired to resynchronize during the course of reception, the program could accomplish this by setting "Receiver Resynchronize" (Line State Ø1). To shut down reception on a line, the program should clear Receiver Enable and then set Receiver Resynchronize.

14 Maintenance Data (Maintenance) (See Bit 15)

This bit is used only in the maintenance mode by the diagnostic program. In maintenance mode Ø1 this bit can be used to simulate data at the receiver input. When used as a simulated input to the receiver, the Transmitter Disable bit must be set to inhibit additional input from the transmitter. This bit should be cleared if it is not being used as the simulated input. If this bit were inadvertently set in maintenance mode and the transmitter Disable bit was clear, the receiver input would have two sources of input. This bit is write/limited read.

15 Maintenance Conditions Strobe (Maintenance)

The setting of this bit records the status of bits Ø8, Ø9, 1Ø, 11, 12, 13, and 14 into the status flip-flops associated with the line specified in bits ØØ-Ø3 of the Secondary Register Selection Register. This bit is self-clearing, hence write only. It may be set at the same time as the bits whose status it records, as its action is delayed until the conclusion of the instruction cycle which set it. This bit is necessary due to "Reads" in the PDP-11/20 being "read-write" cycles, and certain synchronization requirements associated with mode changes during clocking pulses.

CAUTION: After setting this bit, do not change bits ØØ-Ø3 of Secondary Register Selection Register until this bit has self cleared indicating conclusion of the strobe operation.

Secondary Register Selector - Address XØ6

The bits in this register provide a path for the program to access the various locations in the DV11 RAM. The program may read or write these locations. The various locations may be thought of as registers.

Interrupt service routines must save the contents of this register so that no changes occur between the setting of bits in this register and the reading or writing of the Secondary Register Access Register - Address X1Ø.

The bit assignments of the Secondary Register Selector Register are as follows:

Bit	Description
ØØ-Ø3	Line Selection For each type of register selected by bits Ø8-11, there are 16 registers - one per line. The setting of the Line Selection bits determines exactly which of these line registers is to be addressed.
Ø4-Ø7	Unused
Ø8-11	Register Selection These bits determine which type of register is addressed for the line number specified in bits ØØ-Ø3.

Bits

11	10	9	8	
0	0	0	0	Transmitter Primary Current Address
0	0	0	1	Transmitter Primary Byte Count
0	0	1	0	Transmitter Secondary Current Address
0	0	1	1	Transmitter Secondary Byte Count
0	1	0	0	Receiver Current Address
0	1	0	1	Receiver Byte Count
0	1	1	0	Transmitter Accumulated Block Check
0	1	1	1	Receiver Accumulated Block Check
1	0	0	0	Transmit Control Table Base Address

Bits

11	10	9	8	
1	0	0	1	Receiver Control Table Base Address
1	0	1	0	Line Protocol Parameters
1	0	1	1	Line State
1	1	0	0	Transmitter Mode Bits
1	1	0	1	Receiver Mode Bits
1	1	1	0	Line Progress
1	1	1	1	Receiver Control Byte Storage Register

Secondary Registers

These registers are selected by conditioning bits in the Secondary Register Selector Register (Address XØ6) and then reading or writing into the Secondary Register Access Register (Address X1Ø).

NOTE: The Secondary Registers are NOT cleared by Initialize.

0000 Transmitter Principal Current Address

The Transmitter Principal Current Address secondary register contains the 18-bit core memory address of the next character to be transmitted on the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State secondary register bit 07 set to zero).

0001 Transmitter Principal Byte Count

The transmitter Principal Byte Count secondary register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission based on reaching a zero byte count during transmisssion. When bit 15 is set to zero by the PDP-11 program, bits 13-15 of the Line Progress secondary register for this line will control the trans-

mission mode when the principal byte count reaches zero; also, the BCC will be transmitted if Line Progress bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00-02 of the Transmitter Mode Bits secondary register continue to control the line transmission mode. A byte count with bit 15 set to zero (at the time the byte count is loaded by the PDP-11 program) is referred to as a "marked" byte count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State 07 set to zero). When this register reaches zero, transmission continues using the transmitter alternate byte count for this line, if the Transmitter Go bit in the Line State secondary register is still set to one.

0010 Transmitter Alternate Current Address
The Transmitter Alternate Current Address register has exactly the same function as the Transmitter Principal Current Address register (0000). This register is incremented by one with each character transmitted by the DV11 on the associated line if the alternate message table is being used (line State secondary register bit 07 set to one).

0011 Transmitter Alternate Byte Count

The transmitter Alternate Byte Count secondary register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission based on reaching a zero byte count during transmission in the same fashion as described for Transmitter Principal Byte Count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the alternate message table is being used (line State secondary register bit 07 set to one). When this register reaches zero, transmission continues using the

transmitter principal byte count for this line if the Transmitter Go bit in the Line State secondary register is still set to one.

0100 Receiver Current Address

The Receiver Current Address register contains the 18-bit core memory address for storage of the next character to be received on the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. This register is incremented by one with each character received on the associated line by the DV11.

0101 Receiver Byte Count

The Receiver Byte Count secondary register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be received on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC anticipation based on reaching a zero byte count during reception. When bit 15 is set to zero by the PDP-11 program, bits 13-15 of the Line State secondary register for this line will control the reception mode when the byte count reaches zero; also, the BCC will be expected if Line State bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00-02 of the Receiver Mode Bits secondary register continue to control the line reception mode. When this register reaches zero, an interrupt code is set in the Receiver Interrupt Character register and the DV11 stops transferring received characters to core memory.

0110 Transmitter Accumulated Block Check Character

The Transmitter Accumulated Block Check secondary register contains the continuously computed block check character specified by the Line Protocol Parameters secondary register to enable destination stations to check integrity of transmission on the associated line. Characters to be included in the

block check calculation are specified by bit 03 of the transmitter control bytes for each character. The contents of this register are transmitted as two sequential bytes, low-order eight bits first, except when LRC-8 is the selected block check type, in which case a single byte is transmitted. The DV11 automatically clears this register to zero after transmitting its contents.

NOTE

The DV11 computes CRC-16 and CRC-CCITT on a byte at a time basis (parallel), thus the character length must be eight bits. LRC-8 may be selected for characters of 5, 6, 7, or 8 bits.

0111 Receiver Accumulated Block Check Character

The Receiver Accumulated Block Check secondary register contains the continuously computed block check character specified by the Line Protocol Parameters secondary register for checking integrity of data received on the associated line. Characters to be included in the block check calculation are specified by bit 03 of the receiver control byte for that character. The PDP-11 program should clear this register if the accumulated block check at the end of the message is non-zero.

1000 Transmitter Control Table Base Address

The transmitter Control Table Base Address secondary register contains the 18-bit address of the transmitter control table for the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. The contents of this register are used by the microprocessor in the computation of the control byte addresses for transmitted characters.

1001 Receiver Control Table Base Address

The Receiver Control Table Base Address secondary register contains the 18-bit address of the receiver control table for the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. The contents of this register are used by the microprocessor in the computation of the control byte addresses for the received characters.

1010 Line Protocol Parameters

The Line Protocol Parameters secondary register contains the transmitter Data Link Escape (DLE) character when required by the associated line protocol, plus control bits to implement protocol requirements and handling of synch characters. The PDP-11 program writes the data in this register for reference by the microprogram. Bit assignments are described in the following table:

LINE PROTOCOL PARAMETERS SECONDARY REGISTER BIT ASSIGNMENTS

Bit(s)	Designation
00	Idle Mark if both Byte Counts Zero
01	Strip Leading Syncs
02	Unused
03-04	Block Check Type 03 04 BCC Type 0 0 LRC-8 (XOR) 1 0 CRC-16 ($X^{16}+X^{15}+X^{2}+1$) 0 1 Unused-16 1 1 CRC-CCITT ($X^{16}+X^{12}+X^{5}+1$)
05	DDCMP Receive
06	DDCMP Transmit
07	Unused
08-15	DLE Character

1011 Line State

The Line State secondary register is used by the PDP-11 program and the microprocessor to control and monitor line activities in executing the selected protocol. This register is also used by the PDP-11 program to store mode change and BCC anticipation bits for reference by the microprocessor when a marked receiver byte count reaches zero.

LINE STATE SECONDARY REGISTER BIT ASSIGNMENTS

Bit(s)	Designation	Read/Write
00	Receiver Active	Read
01	Receiver Resynchronize	Write
02	Transmitter Go	Read or Write
03	Transmitter Underrun	Read or Write zero
04	Transmitter Non-existant Memory (NXM)	
05	Transmitter Memory Parity Error	
06	Sync Strip On	
07	Use Alternate Tables	
08-09	Unused	
10	Expect BCC	
11-12	Unused	
13-15	Next Receive Mode on Marked Byte Count = 0	

1100 Transmitter Mode Bits

The Transmitter Mode Bits secondary register contain the 3-bit mode selection field (in bits 00-02) which determines the transmitter control table to be used for controlling transmission on the associated line.

1101 Receiver Mode Bits

The Receiver Mode Bits secondary register contains the 3-bit mode selection field (in bits 00-02) which determines the receiver control table to be used for controlling reception on the associated line.

1110 Line Progress

The Line Progress secondary register contains bits set and referenced by the microprocessor to control and monitor activities on the associated line in executing the selected protocol (these bits are not intended for access by the PDP-11 program). This register also stores mode change and BCC transmission control bits, as set by the PDP-11 program, for use by the microprocessor when a marked transmitter byte count reaches zero.

LINE PROGRESS SECONDARY REGISTER BIT ASSIGNMENTS

Bit(s)	Designation
00	Send BCC1 Next
01	Send BCC2 Next
02	DLE Sending In Progress
03-04	Unused
05	Expect BCC1
06	Expect BCC2 Next

07	Resynchronization Flag Expected
08-09	Unused
10	Send BCC
11-12	Unused
13-15	Next Transmit Mode on Marked Byte Count = 0

1111 Receiver Control Byte Holding

The Receiver Control Byte Holding secondary register provides a location for the microprocessor to store the Receiver Control Byte in bits 00-07 during character processing. The PDP-11 program may set a control byte into this register while responding to a DV11 receiver special character interrupt. When the PDP-11 program signals the DV11 that its interrupt response is complete (SCR 08=1), the microprocessor uses the control byte in this register to control the disposition of the interrupting character in the Receiver Interrupt Character register.

The microprocessor may also use this register to write control bytes that specify character discard only, if an error condition or data block boundary condition caused the interrupt; the existing mode specified in the control byte is not altered. The PDP-11 program should not write this register except during initialization or interrupt response cycles.

Special Functions Register - Address X12

Reserved for maintenance. Various bits may appear here during normal operations. Word addressable.

NPR Status Register - Address X14

This register is a silo-type register in that it is read once, in that a new entry "falls" into the register if there are additional "entries" existing at the time that the read of this register is completed. This register is read only.

This register reports various interrupt-causing conditions associated with the transmitter NPR hardware. Interrupt conditions related to various transmitter NPR operations are stacked up in a first-in first-out storage buffer along with the line number being serviced when this condition occurred. As soon as the program has finished reading this register once, a new entry is cycled into the register in place of the former entry. The interrupt is SCR 15 (NPR Status Interrupt). This register is read only, not cleared by Initialize, except for bit 15 which is cleared by initialize.

Bits	Description
ØØ-Ø3	Line Number These bits indicate which line was being serviced when the interrupt condition developed. The format of these bits is the same as bits ØØ-Ø3 of the Secondary Register Selection Register (SRSR) so that the program can load these bits into the SRSR and read the appropriate current address of byte count.
Ø4-Ø7	Unused
Ø8-11	These bits indicate the type of interrupt condition which occurred. The hardware is designed so that simultaneous occurrences on the same line create separate entries (Example: non-existant memory and byte count zero both occur). NOTE that the condition codes are the addresses of the secondary registers which apply.

Code	Condition
ØØØØ	Transmitter Principal Current Address sent NPR hardware to a non-existant memory location (NXM).
ØØØ1	Transmitter Principal Byte Count = Ø.
ØØ1Ø	Transmitter Alternate Current Address sent NPR hardware to a non-existant memory location.
ØØ11	Transmitter Alternate Byte Count = Ø.
1ØØØ	Transmitter Control Table Base Address - fetching control byte produced NXM or a memory parity error, The program should examine the Line State secondary register for further details.
12-14	Unused
15	Entry Present When set, this bit indicates that bits ØØ-11 contain a valid entry. Reading the register or generating initialize clears this bit. It re-sets when another status report entry reaches the "bottom" of the silo and can be read in bits ØØ-11. Bits ØØ-11 are meaningless unless this bit (15) is set.

Reserved Register - Address X16

Bits	Function
ØØ-15	Reserved - word addressable

CONTROL BYTE FORMATS

The DV11 achieves its high througput and generalized operating capabilities by having both the transmitter and the receiver character handling apparatus perform NPR cycles to control byte tables in PDP-11 core to determine the next step to take with regard to the particular character being processed. The bit assignments in the control bytes are arranged such that the same control bytes may be used for both transmission and reception if the communications protocol being used progresses from

mode to mode in a symmetrical fashion on both transmit and receive and provided that the same characters would be included in the Block Check Character in both transmission and reception.

BITS	TRANSMITTER CONTROL BYTE FUNCTION	RECEIVER CONTROL BYTE FUNCTION
Ø5-Ø7	NEXT MODE Determines next transmission mode used on this line.	NEXT MODE Determines next reception mode used on this line
Ø4	RESERVED	STORE/DISCARD Determines whether this character is stored in message table or is discarded.
Ø3	INCLUDE IN BCC YES/NO Determines whether or not this character will be included in the BCC being accumulated for this line.	INCLUDE IN BCC YES/NO Determines whether or not this character will be included in the BCC being accumulated for this line.
Ø2	SEND BCC NEXT Tells Transmitter Logic to send the 16-bit BCC after the character presently being handled. (8-bit if LRC selected)	EXPECT BCC NEXT Tells receiver logic to expect the 16-bit BCC after the character presently being handled. (8-bit if LRC selected)
Ø1	SEND DATA LINK ESCAPE NEXT Tells transmitter logic to send Data Link Escape character from Secondary Register 1Ø1Ø before sending the character presently being handled. (8-bit if LRC selected).	RESERVED

ØØ	RESERVED	GENERATE AN INTERRUPT The setting of this bit causes the character presently being processed to generate an interrupt. The microprocessor moves that character to the Receiver Interrupt Character Register and generates an interrupt request.

SPECIFICATIONS

SYSTEM ADDRESSES

The DV11 uses the same address space as the DM11-A. The first DV11 in a system would be at 775ØØØ; the next at 775Ø4Ø; then 7751ØØ; and finally, 7751 4Ø. If there are DM11-A's in the system already, the first DV11 would be at 775Ø4Ø. The DV11 data handling and modem control use a total of ten registers.

INTERRUPT VECTORS

The DV11 requires three interrupt vectors - two for the data handling section and one for the modem control. The interrupt vectors are in the floating vector space that starts at 3ØØ. The DV11 modem control follows the DM11-BB which follows the DN11. The DV11 data handling section follows the DUP11 which in turn follows the DU11.

TIMING CONSIDERATIONS

The modem control timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan to either run free (SCAN EN) or to be sequentially stepped through the line counter line by line (STEP bit of CSR). The Read/Write cycles of the modem control scan logic force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's Read/Write cycles prevent halting the scan and changing the line number with one machine cycle.

Programs should not spin on flags in the DV11 secondary registers using loops less than 3Ø (octal) instructions; to do so may interfere with DV11 RAM microprocessor / Unibus access interlocks.

ORDER NUMBERS

DV11-AA	Double System unit contains all DV11 logic except the line cards and distribution panels. No lines are implemented.
DV11-BA	Line cards and distribution panel for eight synchronous lines. Requires 5-1/4 inches of cabinet space. Two DV11-BA's can be used with one DV11-AA. To configure an 8 line synchronous DV11, order 1 DV11-AA and 1 DV11-BA. To configure a 16 line synchronous DV11, order 1 DV11-AA and 2 DV11-BA's.
DV11-BB	Line cards and distribution panel for eight asynchronous lines. Requires 5-1/4 inches of cabinet space. Two DV11-BB's can be used with one DV11-AA. To configure an 8 line asynchronous DV11, order 1 DV11-AA and 1 DV11-BB. To configure a 16 line asynchronous DV11, order 1 DV11-AA and 2 DV11-BB's.
DV11-BC	Line cards and distribution panel for four synchronous and four asynchronous lines. Requires 5-1/4 inches of cabinet space.

BUS LOADS

Two bus loads.

POWER CONSUMPTION

A DV11 system with 16 synchronous lines takes:

17.5 Amps @ +5 Volts
1.Ø Amps @ -15 Volts
Ø.5 Amps @ +15 Volts

A DV11 system with 16 asynchronous lines takes:

2Ø.5 Amps @ +5 Volts
1.Ø Amps @ -15 Volts
Ø.6 Amps @ +15 Volts

A DV11 with 8 synchronous and 8 asynchronous lines takes:

19.Ø Amps @ +5 Volts
1.Ø Amps @ -15 Volts
Ø.55 Amps @ +15 Volts

ENVIRONMENTAL

+10 degrees to +50 degrees C with a relative humidity of 20% to 95%.

SPACE REQUIREMENTS

DV11-AA:	Two system units (SU's).
DV11-BA:	5-1/4 inches of cabinet space (SM PAN).
DV11-BB:	5-1/4 inches of cabinet space (SM PAN).
DV11-BC:	5-1/4 inches of cabinet space (SM PAN).

CABLES

Order BCØ5D-25 modem cables.

PROGRAMMABLE MODEM CONTROL DEVICE REGISTERS

The two programmable modem control device registers and their specific bit assignments are listed in the following paragraphs.

Control Status Register (CSR) (Address: 770XX0)

Bit	Status	Description
03:00	LINE #	The LINE # bits are the binary addresses for the modem control's 16 lines (0-15) as follows:

Bit 3	2	1	0	Line #
0	0	0	0	0
0	0	0	1	1
			:	:
1	1	1	1	15

If the Scan is cleared by INITIALIZE or CLR SCAN, the Line # Register will settle in 16μs $\pm$10%. When settled, the Line # Register will be set to Line #0(0000).

NOTE

When the Scan is enabled (or STEP) the next line to be tested will always be Line # +1. These bits are Read/Write and are cleared by INITIALIZE and by CLR SCAN.

04	BUSY	BUSY provides a program indicator that is set to 1 when the Scan is cycling. This bit is particularly useful to determine when a CLR SCAN (bit 11) has completed the task of cycling 0s into the Scanner's memory elements. In addition, this bit must be tested for 0 if SCAN ENABLE was turned off preparatory to changing the Line #. In Interrupt Mode, this procedure guarantees that detected transitions are serviced before the Line # is changed. (If functioning with interrupts OFF, then DONE should be tested after BUSY is found to be 0.)

Bit	Status	Description
05	SCAN EN	The SCAN ENABLE flip-flop allows the scan to "free run" -- testing all lines sequentially if the DONE flip-flop is cleared. When the SCAN EN flip-flop is set to 1 and DONE is 0, a ring counter is allowed to cycle in the following order (from Rest): a. Increment line counter. b. Store contents of memory (Line # Address) in the HOLD flip-flop. c. Write current modem status into memory. d. Compare HOLD and contents of memory for Interrupt conditions. The ring counter continues to cycle (a to d) if DONE remains 0 and SCAN EN is set. If the SCAN EN flip-flop is negated while the ring counter is cycling (i.e., DONE net set) the ring counter will come to rest in 1.2μs $\pm$10% (MAX). The line #Register must not be changed until BUSY (bit 04) is found to be 0. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
06	INTER EN	If set to 1, Interrupt Enable allows DONE to cause an interrupt on priority four (4). This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
07	DONE	The DONE flag, when set to 1, indicates that the hardware Scan has detected a transition on CARRIER, SEC RX, CS, or the RING Modem Status leads. Additionally, DONE freezes the Scan which makes available to the programmer: a. The Line # that caused the interrupt b. The state of the flags (4 bits) c. Modem status (8 bits)

This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.

08 STEP

STEP, when set to 1, causes the Scan to increment the Line # and test that line for interrupts causing transitions. STEP can be used in place of SCAN EN, but care should be exercised that the Scan rate is great enough (milliseconds) so that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1.2μs $\pm$10% to execute. This bit is Write 1s only.

09 MAINT MODE

When the MAINT MODE flip-flog is set to 1, it conditions the Scan Input (RING, CLEAR TO SEND, CARRIER, and SEC RX) to a 1 or ON state. Utilizing STEP or SCAN EN with MAINT MODE exercises 100 percent of the scan logic (not the data multiplexers). This includes the interrupt circuits (M7821) and the address selector (M105).

This mode provides a diagnostic feature, as well as an on-line test facility for the modem control's interaction with the Unibus. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.

10 CLEAR MUX

CLEAR MUX clears the REQUEST TO SEND, TERMINAL READY, SEC TX, and LINE EN flip-flops for all lines, when this bit is set to 1. This bit is Write 1s only.

11 CLR SCAN

CLEAR SCAN clears all active functions (Line #, SCAN EN, etc.) and the memory logic, when this bit is set to 1. The memory logic requires 18.8μs $\pm$10% to cycle a CLEAR through the memory locations. This function is especially useful if the programmer requires knowledge of the ON states of CARRIER, CLEAR TO SEND, RING and SEC RX. When the Scan is enabled (or STEP) following a CLR SCAN, an interrupt will occur for all ON states as they will appear (to the logic) as OFF to ON transitions.

12 DSR *

The DATA SET READY flag is 1 if an ON to OFF or an OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.

13 CS

The CLEAR TO SEND flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.

14 CO

The CARRIER flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.

15 RING

The RING flag is 1 if an OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.

* FOR ASYNCHRONOUS USE, REFERENCE SHEET 43.

Line Status Register (LSR) (Address: 770XX2)

Bit	Status	Description
00	LINE EN	The LINE ENABLE flip-flop, when asserted, enables RING, CO, CS, and SEC RX to be sampled (line status) by the program, and to be tested for transitions.

This bit is Read/Write and cleared by INITIALIZE and CLEAR MUX.

01 TERM RDY — Controls switching of the data communications equipment to the communication channel (via modem).

Auto-Dial and Manual Call origination: Maintains the established call.

Auto-Answer: Allows "handshaking" in response to a RING signal.

This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.

02 RS — When REQUEST TO SEND is set to 1, it conditions the modem for transmit if the communications channel has been established (switched network). This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.

03 NS * — The New Sync (201) flip-flop, when 1, presents a high to the New Sync lead. This bit is Read/Write and is cleared by INITIALIZE or CLEAR MUX.

04 DSR * — When the state of the modem's Data Set Ready lead is a high, this bit is a 1. The DSR bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

05 CS — This bit reflects the current state of the modem CLEAR TO SEND lead. An ON indicates that the modem is ready to transmit data. This lead is most often the result of the REQUEST TO SEND lead. The CS bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

* FOR ASYNCHRONOUS USE, REFERENCE SHEET 43.

06 CO — This bit reflects the current state of the modem carrier detect lead. An OFF indicates that the received signal is unsuitable for demodulation. The CO bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

07 RING — This bit reflects the current state of the modem's ring lead. The RING bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

NOTE

The Line Status Register bits 07:04 are inhibited when LINE EN is 0.

System Addresses

The DV11 modem control uses two address locations in the floating address area.

Interrupt Vectors

Each modem control requires one interrupt vector. The vector addresses are assigned upward from 300 to 777. The modem control falls in behind the DV11 in contiguous assignments from 300.

Timing Considerations

The modem control timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan to either run free (SCAN EN) or to be sequentially stepped through the line counter line by line (STEP bit of CSR). The Read/Write cycles of the modem control scan logic (Paragraph 4.4) force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's Read/Write cycles prevent halting the scan and changing the line number with one machine cycle.

General Description

The DV11 Asynchronous Line Card provides EIA communication capability for the DV11 multiplexor. Each ALC contains four double-buffered serial communication lines (UART'S) that are serviced by the DV11 character processor.

For Asynchronous reception, the UART assembles the serial communication line's character and presents a receiver flag to the character processor. Upon servicing of that receiver flag, the ALC presents the received character and associated error conditions to the character processor's Received Character Storage Silo for future processing. During Asynchronous transmission, the character processor checks the state of the line card's transmit flag to determine the need for servicing. If conditions exist so that transmission is required on that line, the character processor will send a parallel character to the transmitter register file for serial presentation to the communication line.

Each serial communication line of the ALC can operate with with individual programmable parameters.

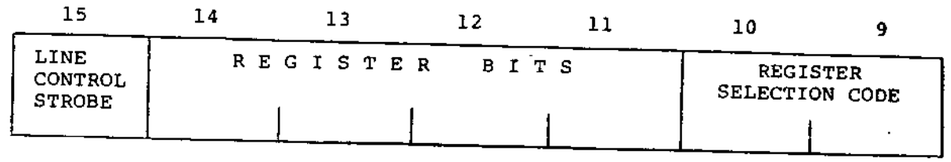
The parameters are:

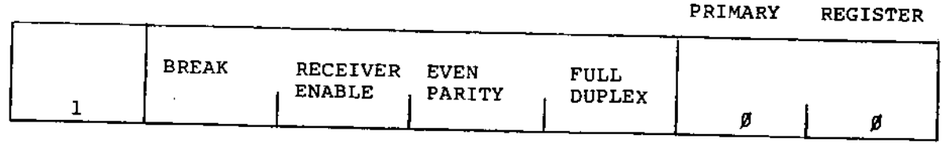
Character length:	5, 6, 7 or 8 bit.
Number of stop bits:	1 or 2 for 5, 6, 7, 8 bit characters.
Parity generation and detection:	Odd, Even or None.
Operating Mode:	Half Duplex or Full Duplex and Receiver Enable.
Transmitter/ Receiver Speed:	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 and 38,400.
Breaks:	Generaticn and Detection.

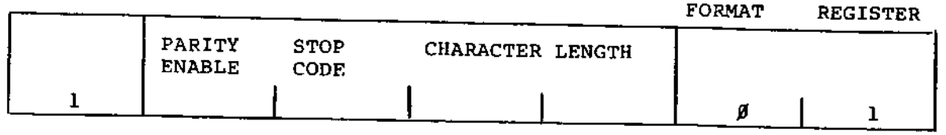
LINE CONTROL REGISTER (LCR) - ADDRESS X04

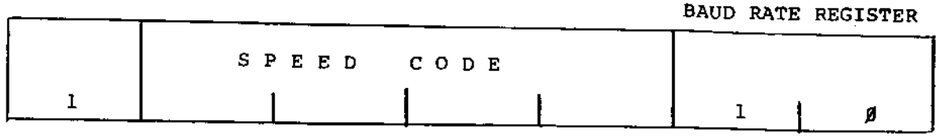
This register controls the features associated with each type of line card. The following LCR bit functions will pertain only to those lines associated with an asynchronous line card. For synchronous line card functions, refer to sheets 9 through 15 of this specification. Bits 00-03 of the Secondary Register Selection Register specify the line numbers to which the bits in the Line Control Register apply.

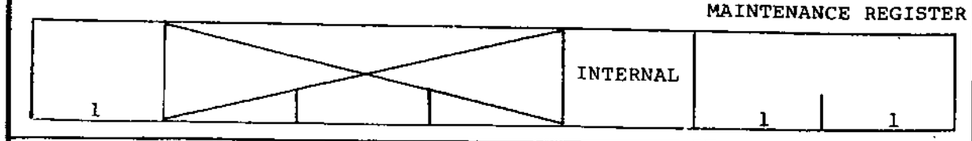
The bit assignments of the asynchronous line card are as follows:











BITS 09-10 REGISTER SELECTION CODE (See bit 15)

Each line has four associated registers that are determined by the states of these bits. These registers are four bits wide and are defined by bits 11 through 14.

Register	Bit Setting 10	9
1. Primary	0	0
2. Format	0	1
3. Baud Rate	1	0
4. Maintenance	1	1

BIT PRIMARY REGISTER

11 (Primary ØØ) Full-Duplex/Half Duplex (See bit 15)

The per line bit, when cleared, conditions the line to operate in full-duplex mode. If this bit is set, the line is conditioned to operate in half-duplex mode, where the selected receiver is blinded during transmission of a character.

12 (Primary ØØ) Even Parity (See bit 15)

This bit, when set, generates character with even parity on the line and expects received characters to have even parity. If this bit is cleared, characters of odd parity are generated on the line and received characters are expected to have odd parity.

The state of this bit is immaterial if the Parity Enable bit (Format Register - Bit 14) is not set. This bit must be conditioned prior to loading of the Format Register.

13 (Primary ØØ) Receiver Enable (See bit 15)

This bit must be set before the receiver logic can assemble characters from the serial input line. When this bit is set, Receiver Active (Line State Bit ØØ) will subsequently set. To shut down reception on a line, the program should first clear Receiver Enable and then set Receiver Resynchronize (Line State Bit Ø1). The program must wait one character interval after shutdown before restarting a line.

14 (Primary ØØ) Break (See bit 15)

This bit, when set, will force a space on that line's output causing a break condition. The break condition may be timed by sending characters during the break interval, since these characters never reach the EIA line.

All primary registers will be cleared following a Bus Initialize or DV11 Master Clear.

BIT FORMAT REGISTER

11-12 (Format Ø1) Character Length (see bit 15)

These bits are set to receive and transmit characters of the length (excluding parity) as shown below.

12	11	
0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

13 (Format Ø1) Two Stop Bits (See bit 15)

This bit, when set, conditions the line transmitting with 5, 6, 7 or 8 bit code to transmit characters having two stop bits. One stop bit is sent when this bit is cleared.

14 (Format Ø1) Parity Enable (See bit 15)

If this bit is set, characters transmitted on the line have an appropriate parity bit affixed; and characters received on the line have their parity checked. Parity sense is determined by the state of Primary Register bit 12.

BIT BAUD RATE

11-14 (Baud Rate 1Ø) Speed Code (See bit 15)

The state of these bits determine the operating speed for the transmitter and receiver of the selected line.

14	13	12	11	Baud Rate
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	38,400

Refer to DV11 Busy and Data Set Busy features for 38.4K baud operation.

BIT MAINTENANCE

11 (Maintenance 11) Maintenance Internal Mode (See bit 15)

This per line bit, when set, loops the transmitter's serial output lead to the receiver's serial input lead on a TTL basis. While operating in maintenance mode, the EIA transmit data leads, EIA received data leads, and the remote Data Set Busy features are disabled. Normal operating mode is assumed when this bit is cleared. All Maintenance Registers will be cleared following a Bus Initialize or DV11 Master Clear.

12-14 (Maintenance 11) Unused

BIT 15 LINE CONTROL STROBE

The setting of this bit records the status of bits Ø9, 1Ø, 11, 12, 13 and 14 into the registers associated for the line specified in bits ØØ-Ø3 of the Secondary Register Selection Register. This bit is self-clearing, hence write only. It may be set at the same time as the bits whose status it records, as its action is delayed until the conclusion of the instruction cycle which set it.

CAUTION: Reference the CAUTION NOTE located on sheet 15.

RECEIVER INTERRUPT CHARACTER REGISTER - ADDRESS XØ2

The RICR Register is a Unibus Addressable Register used by the microprogram to show the PDP-11 program any received character, along with line number and error flags, for which the microprogram requires assistance in processing.

Three individual error flags from an asynchronous line will be presented in the RICR register in the following manner:

Error Code Bit 15	14	13	12	Meaning
0	0	0	1	Parity Error This character was received with a parity sense opposite to that which was selected for this line.
0	0	1	0	Overrun Error The character(s) preceding this character on this line has (have) been lost due to failure of the DV11 receiver system to keep up with the incoming character rate on this line.
0	0	1	1	Framing Error These bits are set if the received character did not have a stop bit present at the proper time. These bits are usually interpreted as indicating the reception of a break.

Existing error codes not shown above are the same for both the synchronous and asynchronous line cards.

A priority encoding scheme is used by an asynchronous line to present a multiple error code condition. Any error flag combination that contains an overrun error will be presented as an Overrun Error (code 0010) in the RICR register. A framing error and parity error combination will be presented as a Framing Error (code 0011) in the RICR Register. A multiple error condition that displays a Parity Error (code 0001) does not exist. This priority scheme is used only by the Asynchronous Line Card. Existing error code bits that are generated on a synchronous line are not affected by this scheme.

PROGRAMMABLE MODEM CONTROL DEVICE REGISTERS

The Asynchronous Line Card uses the existing modem control unit, but with Secondary Receive and Secondary Transmit substituted for Data Set Ready and New Sync respectively. An asynchronous line requires the following changes to the programmable modem control device registers and bit assignments:

CONTROL STATUS REGISTER (CSR) (ADDRESS: 770XX0)

Bit	Status	Description
12	SEC Rx	The Secondary Receive Flag is a ONE if an ON to OFF or an OFF to ON transition has occurred on this modem lead. This bit is not legitimate if the Program has changed the Line # and the Scan has not cycled for one or more lines. This bit is READ only and shall present a ZERO when INITIALIZED or CLEAR SCAN.

LINE STATUS REGISTER (LSR) (ADDRESS: 770XX2)

3	SEC Tx	The Secondary Transmit (202) flip flop, when a ONE, presents a MARK to the Modems Secondary Transmit lead. This bit is READ/WRITE and is cleared by INITIALIZE or CLEAR MUX.
4	SEC Rx	The state of the modem's Secondary Receive Lead, when a ONE, is a MARKING state. The Sec Rx bit is inhibited when the Line Enable Flip Flop is a ZERO. This bit is READ only.

DV11 BUSY

DV11 Busy is a response that emanates from an asynchronous receiving line to indicate that the character servicing rate for that line isn't being sustained. To insure received data integrity, external hardware must interpret and implement this response in such a fashion as to provide a restraining feature on the remote transmitter.

The "ON" condition of DV11 Busy is indicated by a negative voltage in the 3 to 15 volt range. The "OFF" condition of DV11 Busy is indicated by a positive voltage in the 3 to 15 volt range. DV11 Busy will be in the off state following a Unibus Initialized, DV11 Master Clear or Receiver Enable being cleared (LCR Primary Register bit 13). The ON duration of this lead is dependent on the servicing rate of the DV11 Character Processor. Therefore, DV11 Busy can be of any minimal period. DV11 Busy will be asserted a maximum of 10/16th of a bit time following the reception of the first stop bit. For an operating speed of 38.4K baud, external hardware must implement the DV11 Busy feature.

DATA SET BUSY

Each asynchronous transmitting line has the capability of having continual transmission remotely started and stopped. This is the complementary feature of DV11 Busy. Data Set Busy must be implemented with external supporting hardware and must be used with an operating speed of 38.4K baud. Line card modification is required for implementing Data Set Busy at a baud rate other than 38.4K baud.

The "ON" condition of Data Set Busy will be interpreted by a negative voltage in the 3 to 15 volt range. The "OFF" condition of Data Set Busy will be interpreted by a positive voltage in the 3 to 15 volt range. Data Set Busy, when on, is defined as a remote stop request.

To inhibit continual character transmission, Data Set Busy must be received prior to 15/16th of the last stop bit interval. Data Set Busy is invalid when the line is being operated in either internal maintenance mode or at an operating speed less than 38.4K baud, assuming no line card modification was performed.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 22 April 75

TITLE DV11 Acceptance Procedure

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	E C O CHANGE	00004	W. SMITH	4-76	[illegible]	5-21-76

ENG	APPD	SIZE	CODE	NUMBER	REV
4-22-75 [illegible]		A	SP	DV11 - Ø - 4	A

DEC 16-(392)-1079-N971
DRA 107

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE DV11 Acceptance Procedure

I. Q.C. STATUS

Acceptance must ascertain that hte DV11-AA, DV11-BA, DV11-BB and DV11-BC have been through Q.C.

II. ECO STATUS

All hardware to be shipped with this option must have all current ECO's installed. Acceptance area will have on hand any and all information required to verify the ECO status of the option to be shipped.

III. Hardware Procedure

A. Requirements

1. DV11 logic tests DZDVA through DZDVF
2. PDP-11 with 8K of core and a console Teletype
3. An expander box suitable for the DV11; i.e. with space for hex modules and capable of supplying the following current requirements:

	@ +5 Volts	@ -15 Volts	@ +15 Volts
DV11-AA, 2 DV11-BA	17.5 Amps	1 Amp	Ø.5 Amps
DV11-AA, 2 DV11-BB	20.5 Amps	1 Amp	Ø.6 Amps
DV11-AA, DV11-BA, DV11-BB	19.0 Amps	1 Amp	Ø.55 Amps

B. Procedure

1. Check the module placement against sheet 9 of the Unit Assembly drawing (D-UA-DV11-Ø-Ø).
2. Place an H8612 test connector in the jack of each line card. Connect a total of four BC08R cables from each jack of the M7807 and M7809 modules to each jack (all are identical) of the H861 test connector. Connect the BC08R cables such that the smooth side is toward you and the ribbed side is toward the circuit board.
3. Load and run diagnostics DZDVA through DZDVF for four error-free passes* each. In the DZDVE diagnostic select the tests appropriate to H861. Refer to the diagnostic writeup for starting procedures. In particular, refer to the DZDVE writeup for manual input of parameters if other than standard addresses, etc. are being used.

*NOTE: RUN ALL DIAGNOSTICS WITH ITERATIONS ENABLED.

SIZE	CODE	NUMBER	REV
A	SP	DV11-Ø-4	A

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

4. Remove the H8612 and H861 test connectors and reconfigure the apparatus in accordance with Figure 1.
5. Load and run four error-free passes* of DZDVE, selecting the tests which utilize the H325 test connector. Note that the DZDVE test can be run with any number of H325's by using the introductory dialog of the DZDVE test to specify which lines are equipped with H325's and then moving the H325's until all lines have been tested.

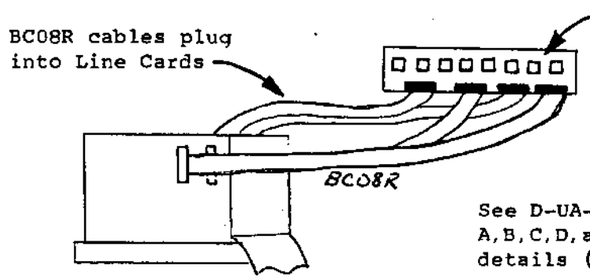


Figure 1- Test Configuration for Acceptance Procedure

Note for Figure 1: Only one H317C Distribution Panel is shown. This is sufficient to test two line cards simultaneously. If it is desired to test four at a time, a second H317C panel would be used and eight more H325 connectors.

*NOTE: RUN ALL DIAGNOSTICS WITH ITERATIONS ENABLED.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY John McNamara	CHECKED Bob Roberts	SECTION
DATE April 16, 1975	DATE 4-17-75	
ENG John P. McNamara	PROD R. Wall	ISSUED SECT.
DATE 4-17-75	DATE 4-17-75	

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DV11-AA
1.	MP-DV11-Ø	DV11 Customer Print Set #1	1
2.	ZJ192-RB	DV11 Diagnostic Kit	1
3.	EK-DV11-MM	DV11 Maintenance Manual	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
DV11 Shipping List		A	PL	DV11-Ø-5		
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16-(325)-1031-N870
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

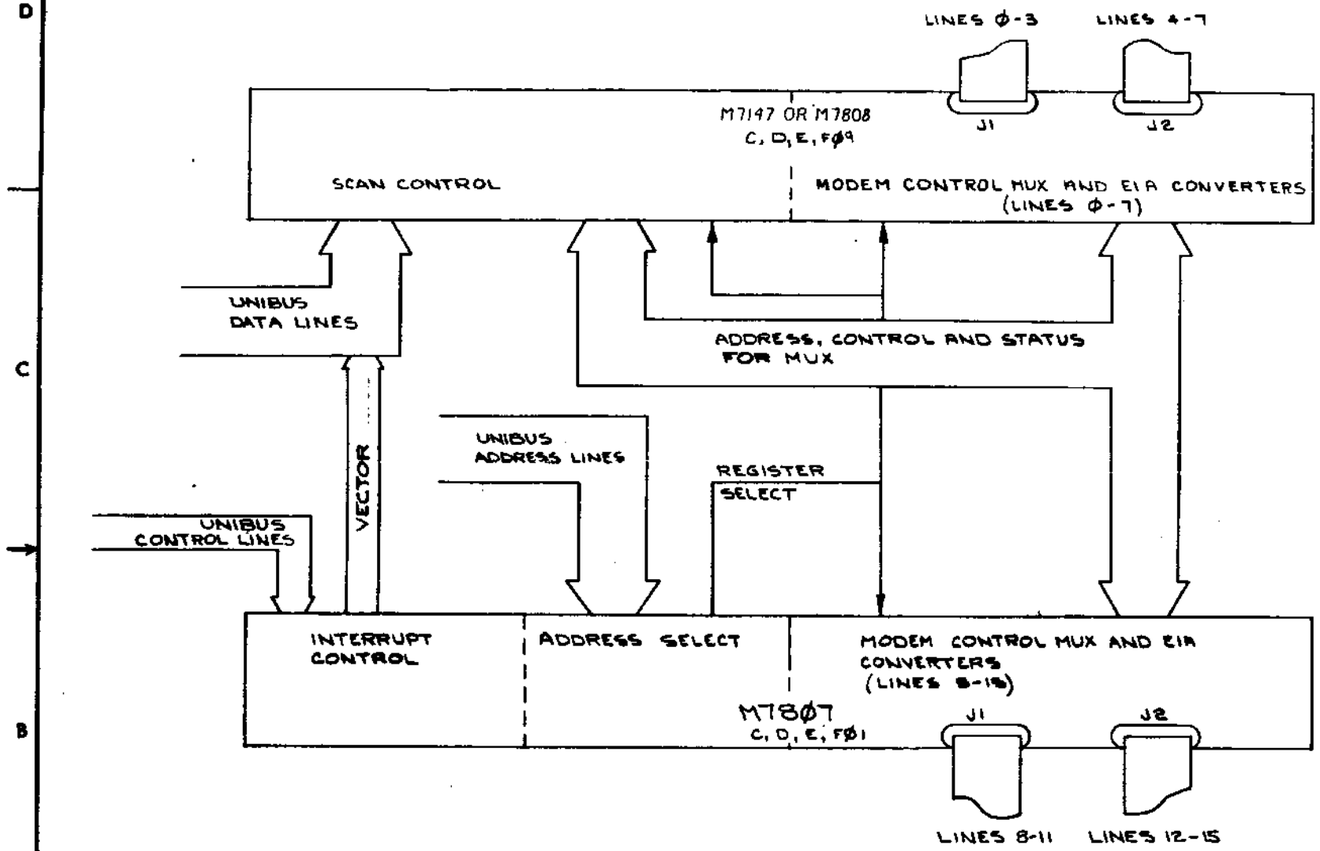
PARTS LIST

MADE BY John McNamara	CHECKED Ed Roberts	SECTION
DATE April 16, 1975	DATE 4-17-75	
ENG John E. McNamara	PROD R. Wall	ISSUED SECT.
DATE 4-17-75	DATE 4-17-75	

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DV11-AA
1	ZJ192-RB	DV11 Diagnostic Kit	1
		NOTE: The ZJ192-RB diagnostic kit includes,	
		but is not necessarily limited to, the	
		following diagnostics: Maindec-11-DZDVA,	
		Maindec-11-DZDVB, Maindec-11-DZDVC,	
		Maindec-11-DZDVD, MAINDEC-11-DZDVE,	
		AND MAINDEC-11-DZDVF.	

TITLE DV11 Software List	ASSY NO. -11-	SIZE A	CODE PL	NUMBER DV11-0-6	REV. A	ECO NO. DV11-00004
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16-(325)-1031-N870
DRA 110



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DVII		PARTS LIST		

DIMENSIONAL TOLERANCE
UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
X.XX ±0.13	.XXX ±.005	±0°30'
X.X ±0.5	.XX ±.02	
X ±1	.X ±.1	

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

MATERIAL

FINISH

		DATE
DRN	K. Smith	3-18-75
CHK	Sid Black	4-17-75
ENG		4-17-75
MFG		4-17-75
QA		4-17-75

NEXT HIGHER ASSY.: B-DD-DVII-Ø

SCALE

SHEET 1 OF 8

DIST.

TITLE: DVII MODEM CONTROL

SIZE	CODE	NUMBER	REV.
D	BD	DVII-Ø-8	B

MK

NOTES:
1. MODULE PINS, AS USED IN THIS PRINT, ARE AS PER SYSTEM UNIT BACK PANEL WIRES.
2. FOR ASYNCHRONOUS USE, MUX NEW SYNC L AND MUX DATA SET READY L ARE REDEFINED AS MUX SEC TX L AND MUX SEC RX L RESPECTIVELY.

MODEM CONTROL SCAN LINES Ø-15

SEE NOTE 2

INTERRUPT CONTROL M7897 C,D,E,F,Ø1

ADDRESS SELECT M7897 C,D,E,F,Ø1

M7197 OR M7808 C,D,E,F,Ø9 MUX LINES Ø-7

M7807 C,D,E,F,Ø1 MUX LINES 8-15

LINES Ø-3

LINES 4-7

LINES 8-11

LINES 12-15

FIRST USED ON OPTION/MODEL: DVII	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		

DIMENSIONAL TOLERANCE — UNLESS OTHERWISE SPECIFIED

DRAW.	DATE
K. Bums	3-18-75
CHKD. Richard Ribeiro	4-17-75
ENGR.	DATE 4-17-75
QUAL. ENGR.	DATE 4-17-75
PROD. R. Well	DATE 4-17-75

NEXT HIGHER ASSY. B-DD-DVII-Ø

MATERIAL —

FINISH —

SCALE —

SHEET 2 OF 2

digital

TITLE: DVII MODEM CONTROL

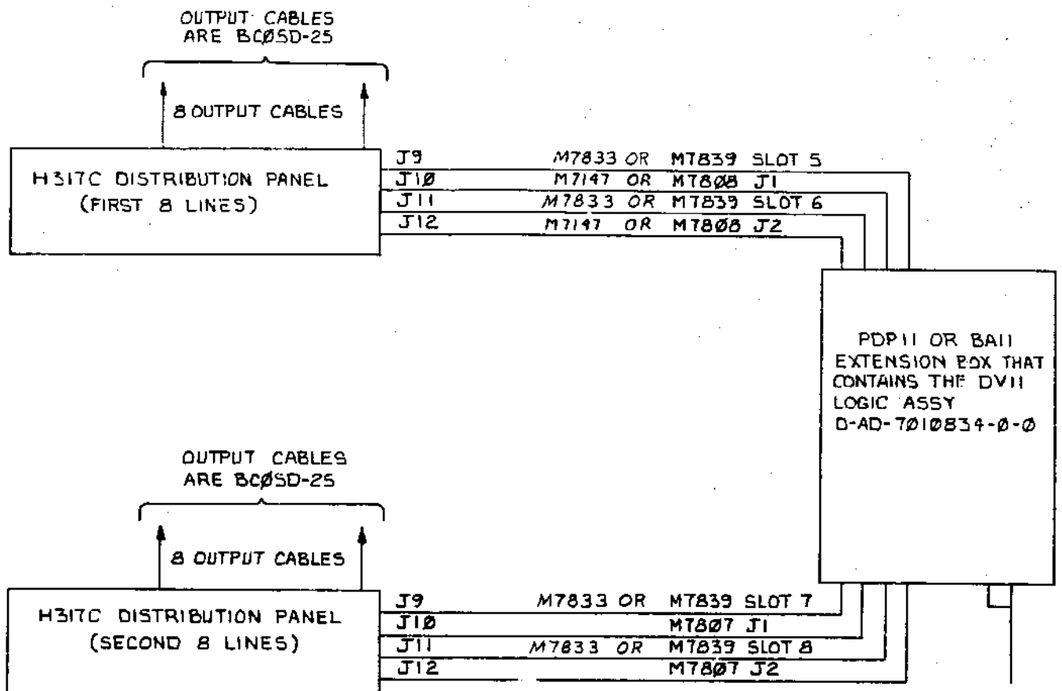
SIZE	CODE	NUMBER	REV.
D	BD	DVII-Ø-8	B

DIST.

MK

NOTES:

1. ON MT8ØT, M7147 OR M7808 MODULES J1 IS THE JACK NEAREST THE EDGE OF THE BOARD.
2. ON H31TC DISTRIBUTION PANEL (D-CS-5411153) J9 IS FAR LEFT JACK; J12 IS FAR RIGHT JACK.
3. INSERT CABLES FLAT SIDE TOWARD YOU; RIBBED SIDE AGAINST CIRCUIT BOARD.



REVISIONS	CHK	CHANGE NO.	REV.
	EY	DV11-00004	A
		J. MCNAMARA	
		DV11-MK008	B
		R. HARRINGTON	

FIRST USED ON OPTION/MODEL: DV11	QTY.	DESCRIPTION	PART NO. / ITEM NO.
		PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES: DECIMALS .xxx = .006, .xx = .02, .x = .1; ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY √
MATERIAL
FINISH

DRN. Robert Kapanol	DATE 3-28-75	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D. S. Roberts	DATE 4-17-75	
ENG.	DATE 4-17-75	
PROJ. ENG.	DATE 4-17-75	
PROD. K. Wall	DATE 4-17-75	

TITLE: INTERCONNECTION DV11

NEXT HIGHER ASSY.: B-DD-DV11-Ø
SCALE
SHEET 1 OF 1

SIZE	CODE	NUMBER	REV.
C	IC	DV11-Ø-9	B

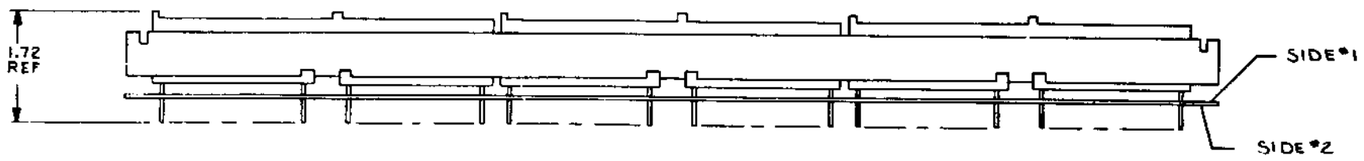
DIST.

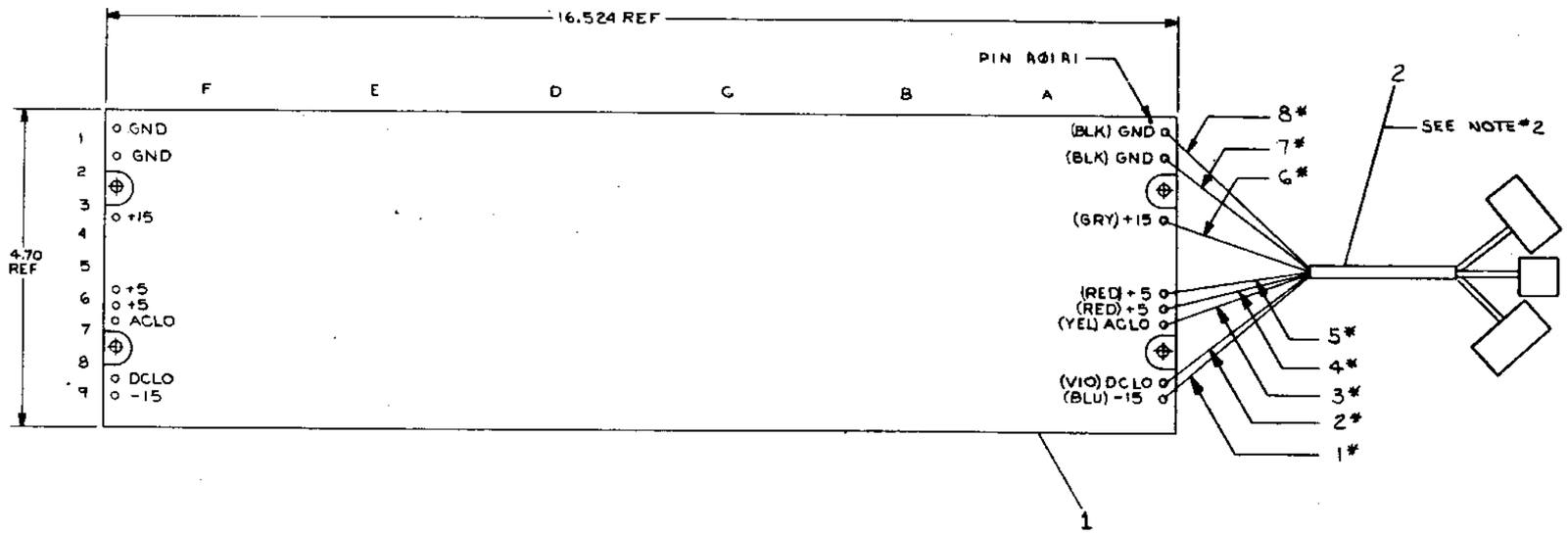
DEC FORM NO. DEC 100-B

SIZE C CODE 14220 NUMBER DV11-Ø-9 REV B

DO NOT SCALE DRAWING

NOTES:
1. # INDICATES POINT NO. ON ITEM#2 (POWER HARNESS).
2. ITEM#2 (POWER HARNESS) TO BE CONNECTED TO ITEM#1 (LOGIC ASSY) AS SHOWN USING SOLDER.





REF			
	AWT REVSTATUS	A-WT-7010834-0	3
1	POWER HARNESS (DVII)	0-IA-7010835-0-0	2
1	WIRED ASS'Y	0-IA-7010655-0-0	1
	DESCRIPTION	DWG/PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES					
		OVER 0 TO 0.6	OVER 0.6 TO 1.2	OVER 1.2 TO 3	OVER 3 TO 6	OVER 6 TO 12	OVER 12 TO 48
SURFACE QUALITY ∞	MEDIUM ☐	±.005	±.005	±.010	±.015	±.031	±.062
MICROINCHES	PREFERRED ☐	±.002	±.010	±.005	±.010	±.015	±.031

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL —

Finish —

DRN. — 1/17/75
CHK'D — 1-9-75
ENG. —
PROJ. —
PROD. — 1-9-75

FIRST USED ON: PDP11

TITLE: LOGIC ASS'Y (DVII)

NEXT HIGHER ASSY.: 0-UA-DVII-0-0

SIZE: D | CODE: AD | NUMBER: 7010834-0-0 | REV.:

SCALE 1/1

SHEET 1 OF 1 | DIST.

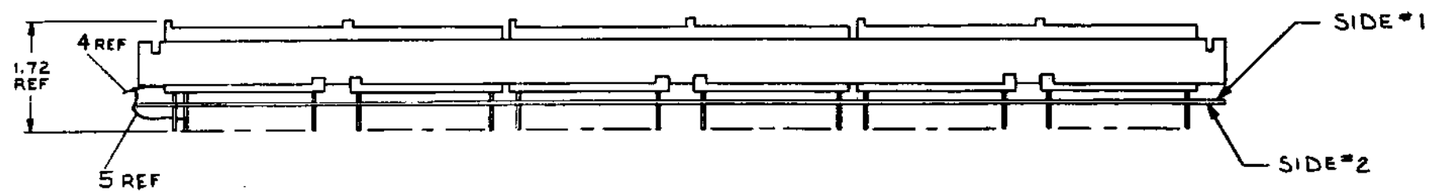
REVISIONS — REV. — CHANGE NO. — CHK.

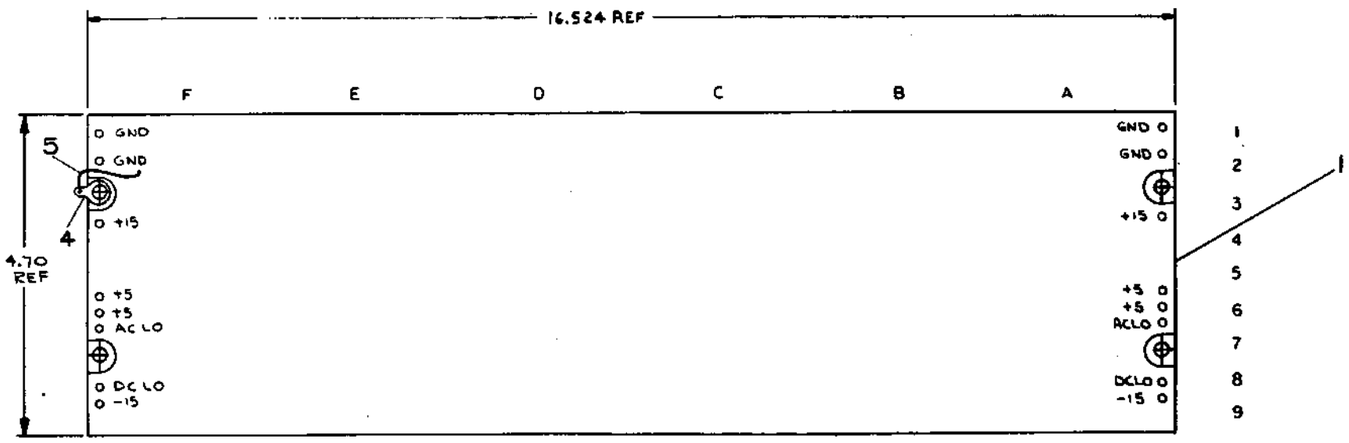
DEC FORM NO. 1005-C

DO NOT SCALE DRAWING

NOTES:

1. WIREWRAP ONE END OF ITEM #5 TO PIN POST1 AND SOLDER THE OTHER END TO ITEM #4 WHICH IS MOUNTED UNDER THE SYSTEM UNIT MOUNTING SCREW.





A/R	COMPRESS-O-CARTON	9905016-4	9
REF	PACKAGING INSTRUCTIONS	3700040-0-0	8
1	DECAL, LOGIC ASSY	7411881-01	7
REF	AWT REVISION STATUS	A-WT-7010655-0	6
A/R	WIRE #24 AWG SOLID BLK	9107488-00	5
1	TERMINAL LOCKING, SHAKEPROOF	9008150	4
REF	WIRE LIST	K-W-DVII-0-7	3
A/R	WIRE #30 AWG SOLID YEL	9105740-44	2
1	BACK PLANE ASSY	D-AD-7010834-0	1
QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: PDP 11

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS: .xxx = ±.005, .xx = ±.02, .x = ±.1
ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY 7
MATERIAL
FINISH

DRW. C. Hurley DATE 11-6-74
CHKD. S. Parker DATE 11-7-74
ENGR. [illegible] DATE 11-7-74
PROJ. [illegible] DATE 11-7-74
MGR. R. Wall DATE 11-8-74

NEXT HIGHER ASSY. D-AD-7010834-0-0

digital EQUIPMENT CORPORATION

TITLE: WIRED ASSY (DVII)

SIZE D CODE AD NUMBER 7010655-0-0 REV. A

SCALE — SHEET 1 OF 1

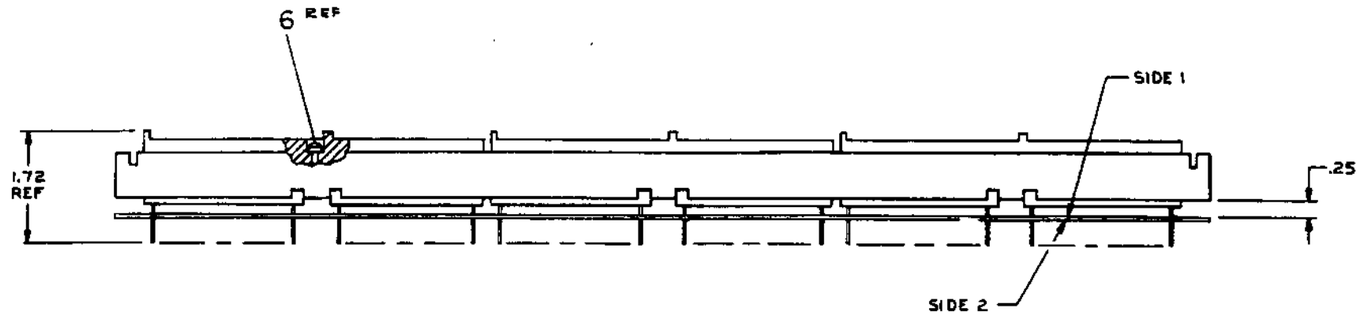
REVISIONS			
LTR	CHANGE NO		
A	DVII-00003	J MCNAMARA	11-7-74

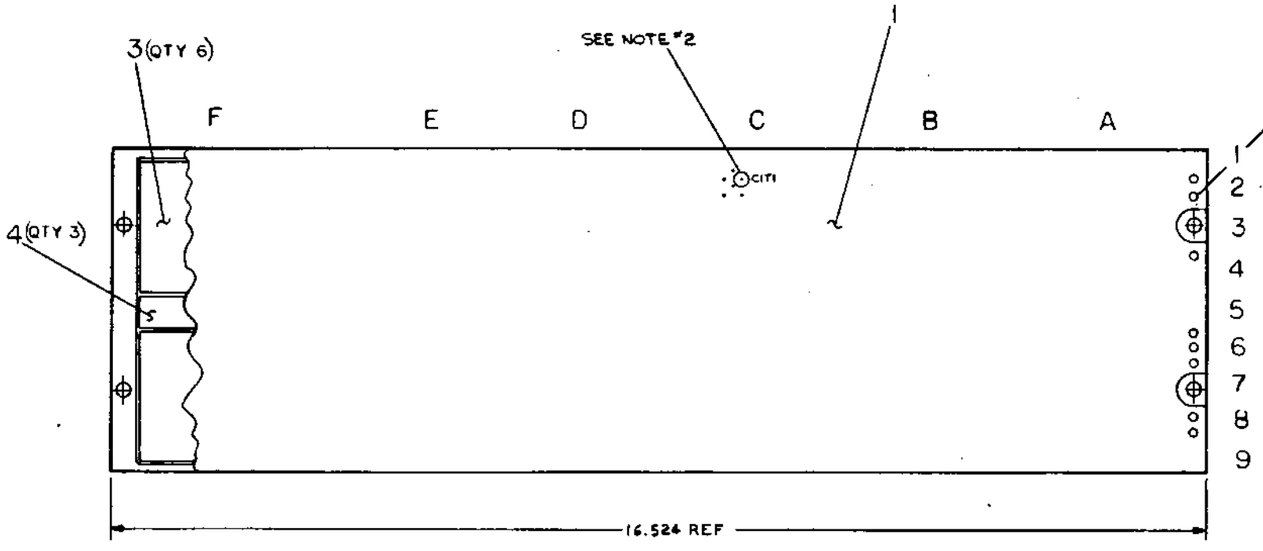
D AD 7010655-0-0 A

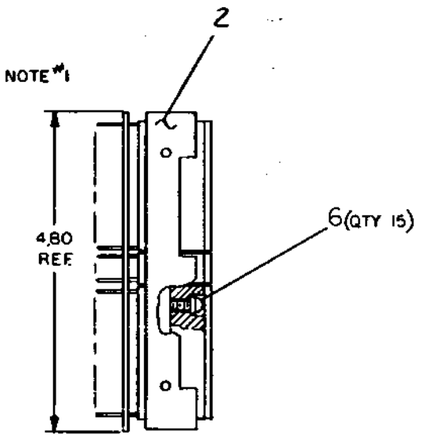
DO NOT SCALE DRAWING

D IA 7010719-0-0

NOTES:
1. INSERT EYELET (ITEM #5) FROM SIDE #2 OF ETCH BOARD.
2. REWORK ITEM #1 (ETCH BOARD), IF REV C, BY USING CIRCUIT BOARD REWORK DRILL (HOLLOW DRILL .04 ID, .125 OD) AT PIN CIT1 ALL THE WAY THROUGH. THIS WORK TO BE DONE AFTER ITEM #1 HAS BEEN INSTALLED ON ITEMS #3 & #4. NO REWORK REQUIRED IF ITEM #1 IS REV D OR LATER







REF	DESCRIPTION	PART NO.	ITEM NO.
	CIRCUIT SCHEMATIC	D-CS-5441420-0-1	7
15	SCR FIL HD POSI DR 8-32 X .62	9006120-6	6
16	EYELET	9009405	5
3	72 PIN CONN. BLOCK	12J1425-00	4
6	288 PIN BLOCK H863	12J0258	3
1	LOGIC FRAME	12J1439	2
1	ETCHED CIRCUIT BOARD	5011619	1

FIRST USED ON OPTION/MODEL: PDP 11

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS: .XXX ± .005; .XX ± .02; .X ± .1
ANGLES: ± 30'
REMOVE BURRS AND BREAK SHARP
FINISH: MATERIAL —; FINISH —

		DATE
DRN	C Hong	11-14-74
CHK	Ed Rich	4-9-75
ENG		4/9/75
MFG		4/9/75
QA		4/9/75
PROJ	K. Wall	4/9/75

NEXT HIGHER ASSY: D-AD-7010655-0-0
SCALE 1/1
SHEET 1 OF 1

digital EQUIPMENT CORPORATION

TITLE: BACK PLANE ASSY

SIZE D | CODE IA | NUMBER 7010719-0-0 | REV

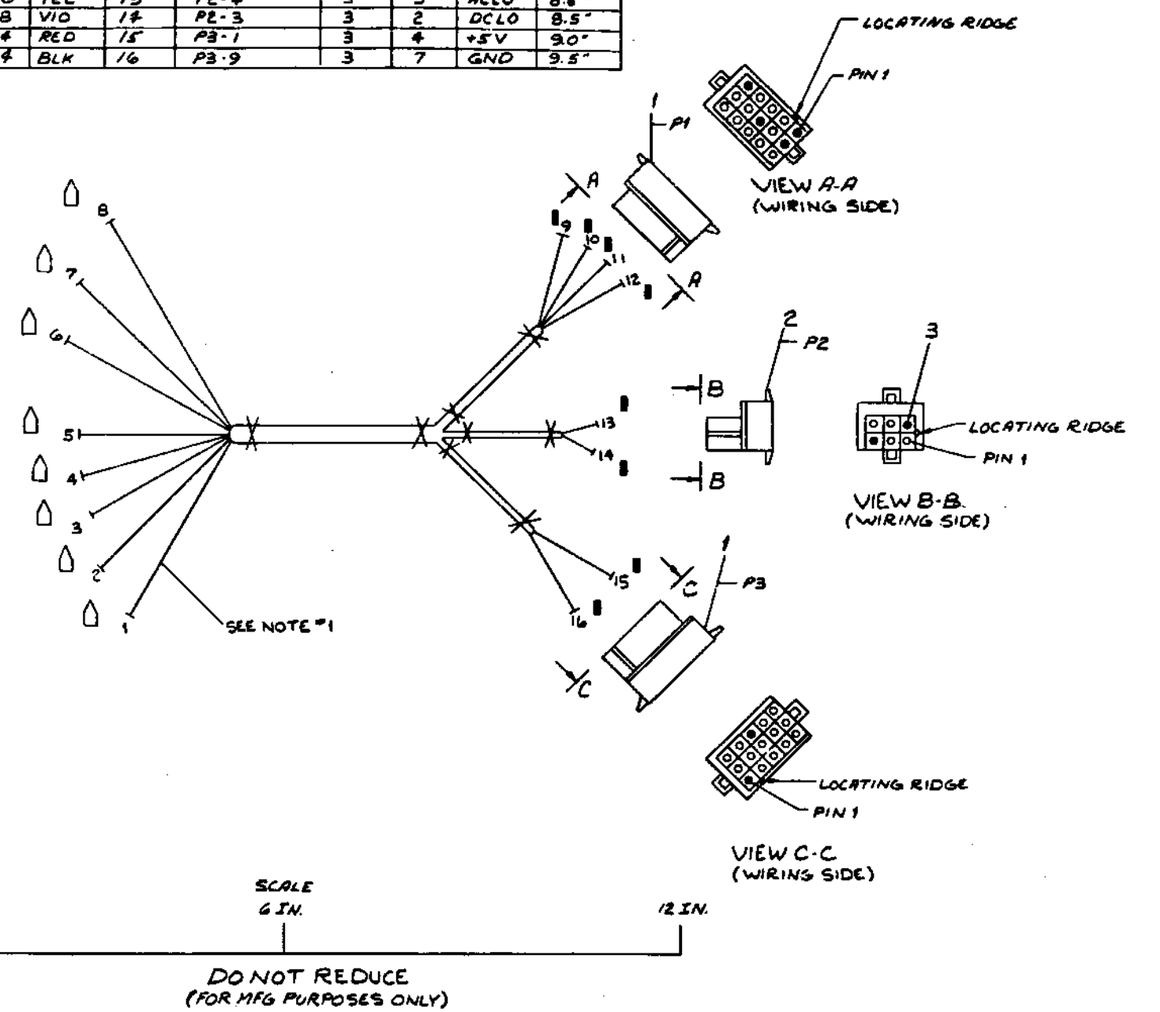
DIST.

REVISIONS: REV | CHANGE NO | CHK

WIRE TABLE

ITEM NO	DESCRIPTION AWG	DESCRIPTION COLOR	FROM POINT	FROM CONNECTION	FROM WITH	TO POINT	SIGNAL	WIRE LENGTHS
6	14	BLU	9	P1-13	3	1	-15V	10.0"
5	14	BLK	10	P1-8	3	8	GND	10.5"
4	14	RED	11	P1-1	3	5	+5V	9.0"
9	18	GRY	12	P1-2	3	6	+15V	9.5"
8	18	YEL	13	P2-4	3	3	ACLO	8.5"
7	18	VIO	14	P2-3	3	2	DCLO	8.5"
4	14	RED	15	P3-1	3	4	+5V	9.0"
5	14	BLK	16	P3-9	3	7	GND	9.5"

NOTES
1. INSULATION AT POINT 1 THRU 8 SHOULD BE STRIPPED BACK .18 INCHS AND WIRES SOLDER TINNED.



ITEM	QTY	DESCRIPTION	DWG./PART NO.
X	B	TIE WRAP	9007031
0	A/R	WIRE, #18 AWG (GRY)	9107360-88
0	A/R	WIRE, #18 AWG (YEL)	9107360-44
0	A/R	WIRE, #18 AWG (VIO)	9107360-77
0	A/R	WIRE, #14 AWG (BLU)	9107370-66
0	A/R	WIRE, #14 AWG (BLK)	9107370-00
0	A/R	WIRE, #14 AWG (RED)	9107370-22
8	8	PIN, MALE	1209378-01
	1	HOUSING, CONN, 6 PIN	1209351-06
	2	HOUSING, CONN 18 PIN	1209351-15

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES: 0 TO .12	.13 TO .24	.25 TO .48	.49 TO .72	.73 TO 1.20	1.21 TO 2.40	2.41 TO 4.80
SURFACE QUALITY 125 MICROINCHES	MEDIUM	±.005	±.005	±.010	±.015	±.020	±.030	±.045
	PREFERRED	±.010	±.010	±.015	±.020	±.030	±.045	±.060

QUANTITY B VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL: SEE PARTS LIST

FINISH

DRN: J.C. 1-20-75
CHK: 2-24-75
ENG: 2-24-75
PROJ. ENG: 2-24-75
PROD. 2-27-75
NEXT HIGHER ASSY.
D-AD-7010834-0-0
SCALE
SHEET 1 OF 1

FIRST USED ON: DV11

TITLE: POWER HARNESS (DV11)

SIZE D | CODE IA | NUMBER 7010835-0-0 | REV.

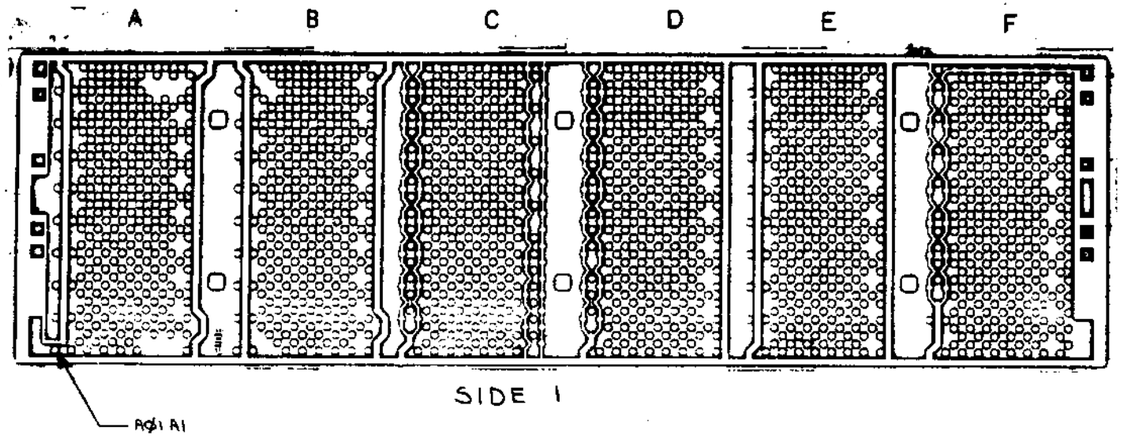
DIST.

REVISIONS REV.	CHANGE NO.	CHK.

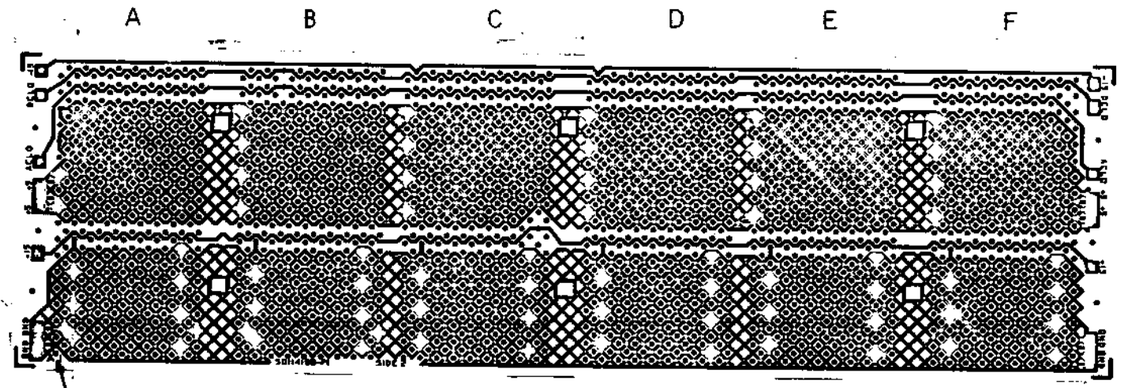
DEC FORM NO. 3159 1/66-C

7010835-0-0 D IA

NOTES:



SIDE 1



SIDE 2

IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF		MODULE ECO HISTORY	D-MM-5411420-0-4	4
REF		ASSY/DRILLING HOLE LAYOUT	D-MM-5411420-0-5	3
REF		X-Y COORDINATE HOLE LOCATION	D-CO-5411420-0-4	2
1		ETCHED CIRCUIT BOARD	5011419	1
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: PDP11

ETCH BOARD REV | DEPT

REV	CHANGE NO.	CHK	DATE
C	5411420-00002	J. McNAMARA	2-10-72
B	5411420-1	J. McNAMARA	1-24-72

REVISIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRAWN	DATE
J. McNAMARA	1-24-72
CHK	DATE
J. McNAMARA	1-24-72
ENGR	DATE
MFG	DATE

NEXT HIGHER ASSY: D-IA-7010719-0-0

SCALE: NONE

SHEET 1 OF 1

digital EQUIPMENT CORPORATION

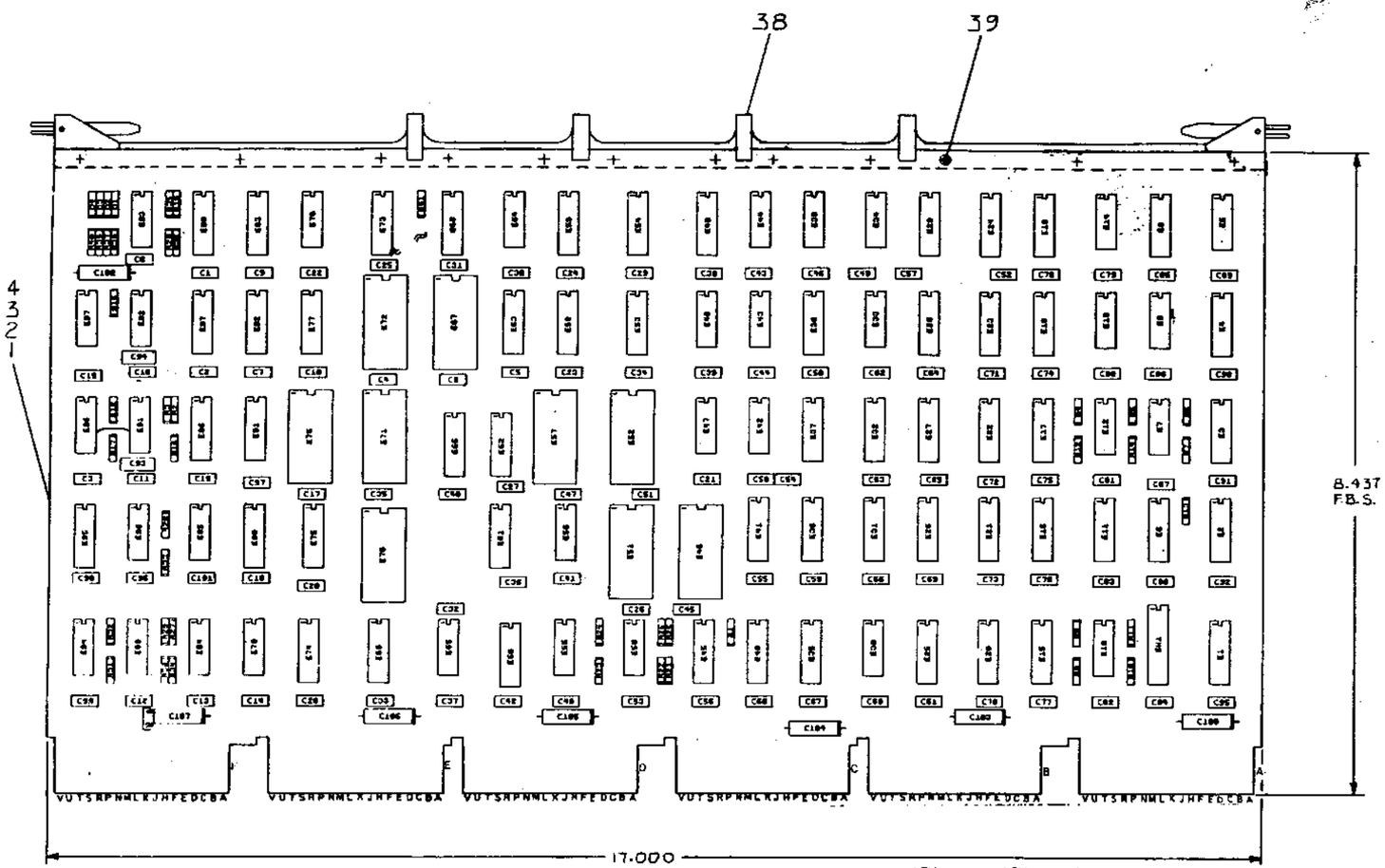
TITLE: CIRCUIT SCHEMATIC

SIZE: D | CODE | NUMBER: DCS 5411420-0-1 | REV: C

DIST.

DCS5411420-0-1 C

NOTES:



74155	8	16
74151	8	16
74153	8	16
74181	12	24
74150	12	24
74175	8	16
74174	8	16
8640	1	8
74157	8	16
8838	9	16
3341	8	16
IC TYPE	GND	+5V

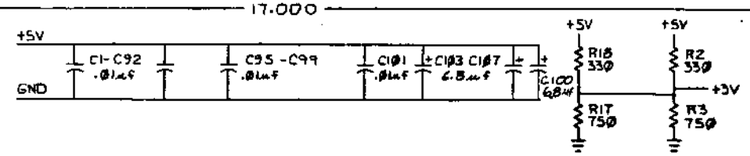
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

-12V: 1

AA2, BA2, CA2, DA2, EA2, FA2

AC2, AT1, BC2, BT1, CC2, CT1, DC2, DT1, EC2, ET1, FC2, FT1



REF				
REF		X-Y COORDINATE HOLE LOCATION	X-CO-M7836-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7836-0-5	2
REF		MODULE ECO HISTORY	B-MH-M7836-0-6	3
1		ETCHED CIRCUIT BOARD	5818878	4
1	C83	CAP 10 PF 100V 5% DM	1000008	5
1	C84	CAP 100 PF 100V 5% DM	1000016	6
98	C1 THRU C92, C95-C99, C101	CAP .01 UF 100V 20% CER	1001870-01	7
7	C100, C102 THRU C107	CAP 6.8 UF 35V 10% tant	1005306	8
4	D1-D4	DIODE D664	1100114	9
2	R2, R18	RES. 330 1/4W 5%	1300295	10
1	R1	RES. 470 1/4W 5%	1300316	11
1	R15	RES. 3K 1/4W 5%	1300432	12
12	R4-R14, R41	RES. 1K 1/4W 5%	1300305	13
2	R3, R17	RES. 750 1/4W 5%	1301481	14
1	R16	RES. 18K 1/4W 5%	1302405	15
4	E5, E85, E90, E97	IC 7474	1905941	16
1	E55	IC 7432	19M521	17
1	E78	IC 7420	1905577	18
1	E84	IC 7402	1908804	19
3	E14, 30, 65	IC 7404	1909688	20
1	E8	IC 8881	1909705	21
3	E7, 10, 12	IC 8242	1909712	22
4	E13, 50, 89, 93	IC 8640	1911469	23
4	E38, 49, 53, 54	IC 74153	1908837	24
5	E46, 52, 57, T0, T1	IC 74181	1908902	25
10	E33, 34, 39, 42, 43, 44, 47, 48, 56, 64	IC 7486	1910011	26
2	E79, 96	IC 7437	1910091	27
4	E51, 67, 72, 76	IC 74150	1910153	28
2	E91, 92	IC 74121	1910230	29
7	E4, 9, 19, 28, 82, 62, 31	IC 74175	1910651	30
13	E53, 59, 60, 61, 63, 66, 18, 23, 27, 41, 45, 35, 36	IC 74174	1910652	31
4	E1, 37, 40, 32	IC 74157	1910655	32
1	E35	IC 74155	1910656	33
4	E3, 15, 20, 25	IC 8838	1911117	34
1	E94	IC 7408	1910155	35
8	E24, 73, 81, 29, 83, 86, 88, 68	IC 3341	2111168	36
1	SW1	SWITCH 10 POS	12111184-06	37
1		HEX HANDLE ASSY	12108711 -2	38
12		EYELET	8006732	39
11	R19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39	RES. 180, 1/4W, 5%	1301322	40
11	R20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40	RES. 390, 1/4W, 5%	1300309	41
1		COVER SWITCH 10 POS	12112284-06	42
14	E2, 6, 11, 16, 17, 21, 22, 26, 69, 74, 75, 77, 80, 87	IC, 74151	1909936	43
A/R		WIRE #30 AWG INSULATED	9105740	44

QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO

PARTS LIST

FIRST USED ON OPTION MODEL: DV11-AA

ETCH BOARD REV: B

ORIGINATED	A
CHANGE NO.	
REVISIONS	
CHK	

DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

ORIG: D.L. Sm. DATE 5/1/75
CHKD: DATE 5/14/75
CHK: DATE 5/14/75
PROJ. ENG: DATE 5/14/75
PROD. ENG: DATE 5/16/75

NEXT HIGHER ASSY: B-DD-DV11-0

SCALE:

SHEET 1 OF 10

digital EQUIPMENT CORPORATION

TITLE: ALU AND TRANSFER BUS

SIZE: D | CODE: DCS | NUMBER: M7836-0-1 | REV: A

DIST.

DCS M7836-0-1 A

SUB DI-2 ALU A=B H
DI-1 COUT L

74181 E71
DI-2 REG A Ø7 H
DI-2 REG A Ø6 H
DI-2 REG A Ø5 H
DI-2 REG A Ø4 H
DI-2 BUF ROM DATA Ø3 H
DI-2 BUF ROM DATA Ø2 H
DI-2 BUF ROM DATA Ø1 H
DI-2 BUF ROM DATA ØØ H

74181 E7Ø
DI-2 REG A Ø3 H
DI-2 REG A Ø2 H
DI-2 REG A Ø1 H
DI-2 REG A ØØ H
DI-3 BUF ROM DATA Ø4 H
DI-3 BUF ROM DATA Ø5 H

+5V
R1 47Ø

74174 E16
DI-4 TRANSFER BUS 17 H (BA1)
DI-4 TRANSFER BUS 16 H (AL1)
DI-4 TRANSFER BUS 15 H (AV2)
DI-4 TRANSFER BUS 14 H (BF1)
DI-4 TRANSFER BUS 13 H (AS2)
DI-4 TRANSFER BUS 12 H (AP2)
DI-1 REG B 17 H
DI-1 REG B 16 H
DI-1 REG B 15 H
DI-1 REG B 14 H
DI-1 REG B 13 H
DI-1 REG B 12 H
CLR CLK

DI-3 T INIT DI L (ES2)

74174 E58
DI-4 TRANSFER BUS 11 H (BE2)
DI-4 TRANSFER BUS 1Ø H (EV2)
DI-4 TRANSFER BUS Ø9 H (ES1)
DI-4 TRANSFER BUS Ø8 (ER1)
DI-3 TRANSFER BUS Ø7 (EP1)
DI-3 TRANSFER BUS Ø6 (BD2)
DI-1 REG B Ø7 H
DI-1 REG B ØØ H
CLR CLK

74174 E6Ø
DI-3 TRANSFER BUS Ø5 H (EJ2)
DI-3 TRANSFER BUS Ø4 H (CE2)
DI-3 TRANSFER BUS Ø3 H (DR2)
DI-3 TRANSFER BUS Ø2 H (DN2)
DI-3 TRANSFER BUS Ø1 H (DP2)
DI-3 TRANSFER BUS ØØ H (DT2)
DI-1 REG B Ø5 H
DI-1 REG B Ø4 H
DI-1 REG B Ø3 H
DH REG B Ø2 H
DI-1 REG B Ø1 H
DI-1 REG B ØØ H
CLR CLK

DI-6 B REGISTER CLOCK L DU2
7404 E65

74174 E61
DI-1 ALU RESULT Ø6 H
DI-1 ALU RESULT Ø3 H
DI-1 ALU RESULT Ø4 H
DI-1 ALU RESULT Ø5 H
DI-1 ALU RESULT Ø6 H
DI-1 ALU RESULT Ø7 H
DM2
DL2
CE1
CLR CLK

DI-4 SET ALU Ø2 L
7474 E55
DI-1 ALU RESULT Ø2 H
DH2
DI-9 BUF INIT
7408 E94
DI-4 CLEAR ALU Ø2 L FP1
+3V
7474 E95
DI-1 ALU RESULT Ø1 H
FL1
DI-4 CLEAR ALU Ø1 L FT2
DI-2 ALU RESULT CLOCK H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE/CODE	NUMBER	REV.
ALU AND TRANSFER BUS (DI-1)	D DCS	M7836-Ø-1	A
SCALE	SHEET 2 OF 1C	DIST.	

D3-6 A REGISTER CLOCK L — EC1 — 7404 E65

74174 E23
DI-4 TRANSFER BUS 17 H (BA1) 3 — D0 — R0(1) 2 — DI-1 REG B 17 H
DI-4 TRANSFER BUS 16 H (AL1) 4 — D1 — R1(1) 5 — DI-1 REG B 16 H
DI-4 TRANSFER BUS 15 H (ANE) 6 — D2 — R2(1) 7
DI-4 TRANSFER BUS 14 H (BF1) 11 — D3 — R3(1) 10
DI-4 TRANSFER BUS 13 H (AS2) 13 — D4 — R4(1) 12
DI-4 TRANSFER BUS 12 H (AP2) 14 — D5 — R5(1) 15
CLR CLK

D3-7 INIT DI L — ES2

74174 E63
DI-4 TRANSFER BUS 11 H (BE2) 3 — D0 — R0(1) 2
DI-4 TRANSFER BUS 10 H (EV2) 4 — D1 — R1(1) 5
DI-4 TRANSFER BUS Ø9 H (EB1) 6 — D2 — R2(1) 7
DI-4 TRANSFER BUS Ø8 H (ER1) 11 — D3 — R3(1) 10
DI-3 TRANSFER BUS Ø7 H (EP1) 13 — D4 — R4(1) 12 — DI-2 REG A Ø7 H
DI-3 TRANSFER BUS Ø6 H (BD2) 14 — D5 — R5(1) 15 — DI-2 REG A Ø6 H
CLR CLK

74174 E66
DI-3 TRANSFER BUS Ø5 H (EJ2) 3 — D0 — R0(1) 2 — DI-2 REG A Ø5 H
DI-3 TRANSFER BUS Ø4 H (CE2) 4 — D1 — R1(1) 5 — DI-2 REG A Ø4 H
DI-3 TRANSFER BUS Ø3 H (DR2) 6 — D2 — R2(1) 7 — DI-2 REG A Ø3 H
DI-3 TRANSFER BUS Ø2 H (DM2) 11 — D3 — R3(1) 10 — DI-2 REG A Ø2 H
DI-3 TRANSFER BUS Ø1 H (DP2) 13 — D4 — R4(1) 12 — DI-2 REG A Ø1 H
DI-3 TRANSFER BUS ØØ H (DT2) 14 — D5 — R5(1) 15 — DI-2 REG A ØØ H
CLR CLK

74181 E52
DI-1 REG B 17 H — B3
DI-1 REG B 16 H — A3
B A2
B1 A1
B0 A0
S3 S2 S1 S0 M CIN
A=B COUT G P
F3 F2 F1 F0

DI-3 BUF ROM DATA Ø4 H

74181 E46
DI-1 REG B 15 H — B3
DI-1 REG B 14 H — A3
B2 A2
B1 A1
B0 A0
S3 S2 S1 S0 M CIN
A=B COUT G P
F3 F2 F1 F0

DI-1 REG B 13 H
DI-1 REG B 12 H

DI-1 ALU A=B H (CU2)

74181 E57
DI-1 REG B 11 H — B3
DI-1 REG B 10 H — A3
B2 A2
B1 A1
B0 A0
S3 S2 S1 S0 M CIN
A=B COUT G P
F3 F2 F1 F0

DI-1 REG B Ø9 H
DI-1 REG B Ø8 H

DI-1 COUT L

D3-2 ROM DATA Ø3 H — ES1 — 7437 E96
D3-2 ROM DATA Ø2 H — EY2 — 7437 E96
D3-2 ROM DATA Ø1 H — ER1 — 7437 E96
D3-2 ROM DATA ØØ H — EM1 — 7437 E96
+3V

74174 E41
DØ R0(1) — DI-2 ALU RESULT 17 H
DI R1(1) — DI-2 ALU RESULT 16 H
D2 R2(1) — CV2 — DI-2 ALU RESULT 15 H
D3 R3(1) — DI-2 ALU RESULT 14 H
D4 R4(1) — DI-2 ALU RESULT 13 H
D5 R5(1) — DI-2 ALU RESULT 12 H
CLR CLK

7432 E55 — 8 — DJ2 DI-2 ALU 13-12 H

74175 E62
DØ R0(1) R0(0) — DI-2 ALU RESULT 11 H
DI R1(1) R1(0) — DI-2 ALU RESULT 10 H
D2 R2(1) R2(0) — DI-2 ALU RESULT Ø9 H
D3 R3(1) R3(0) — DI-2 ALU RESULT Ø8 H
CLR CLK

DI-2 BUF ROM DATA Ø5 H
DI-2 BUF ROM DATA Ø2 H
DI-2 BUF ROM DATA Ø1 H
DI-2 BUF ROM DATA ØØ H

D3-2 ALU OPERATION L — FF2 — 7402 E84 — 4 — DI-2 ALU RESULT CLOCK H
D3-7 DATA STROBE L — FE1

DI-4 CLEAR ALU RESULT HIGH BYTE L — FS2 — 7408 E94 — 6
DI-9 BUF INIT L

REVISIONS		
ONE	CHANGE NO.	REV.

TITLE	ALU AND TRANSFER BUS (DI-2)	SIZE/CODE	D	CS	NUMBER M7836-Ø-1
SCALE		SHEET 3 OF 10	DIST.		REV. A

D5-2 TRANSFER SOURCE ENAB L — DXE

DI-1 REGISTER B 15 H
DI-9 NPR DATI 07 H
D3-11 RAM OUTPUT 07 H
DI-5 SILO OUT 07 H
D2-6 NPR DATO 07 H
DI-7 BCC 07 H
DI-1 ALU RESULT 07 H
D3-2 ROM DATA 04 H
EVI
+3V
DC1 DI-3 BUF ROM DATA 04 H
DI-3 TRANSFER BUS 07 H

DI-1 REGISTER B 14 H
DI-9 NPR DATI 06 H
D3-11 RAM OUTPUT 06 H
DI-5 SILO OUT 06 H
D2-6 NPR DATO 06 H
DI-7 BCC 06 H
DI-1 ALU RESULT 06 H
D3-2 ROM DATA 05 H
EI2
+3V
EM1 DI-3 BUF ROM DATA 05 H
BD2 DI-3 TRANSFER BUS 06 H

DI-1 REGISTER B 13 H
DI-9 NPR DATI 05 H
D3-11 RAM OUTPUT 05 H
DI-5 SILO OUT 05 H
D2-6 NPR DATO 05 H
DI-7 BCC 05 H
DI-1 ALU RESULT 05 H
D3-2 ROM DATA 06 H
EI3
+3V
DI-3 BUF ROM DATA 06 H
EJ2 DI-3 TRANSFER BUS 05 H

DI-1 REGISTER B 12 H
DI-9 NPR DATI 04 H
D3-11 RAM OUTPUT 04 H
DI-5 SILO OUT 04 H
D2-6 NPR DATO 04 H
DI-7 BCC 04 H
DI-1 ALU RESULT 04 H
CE2 DI-3 TRANSFER BUS 04 H

D3-4 MASTER SCAN 03 H
DI-2 ALU RESULT 11 H
DI-1 REGISTER B 11 H
DI-9 NPR DATI 03 H
D3-11 RAM OUTPUT 03 H
DI-5 SILO OUT 03 H
D2-6 NPR DATO 03 H
DI-7 BCC 03 H
DI-1 ALU RESULT 03 H
DR2 DI-3 TRANSFER BUS 03 H

D3-4 MASTER SCAN 02 H
DI-2 ALU RESULT 10 H
DI-1 ALU RESULT 07 H
DI-1 REGISTER B 10 H
DI-9 NPR DATI 02 H
D3-11 RAM OUTPUT 02 H
DI-5 SILO OUT 02 H
D2-6 NPR DATO 02 H
DI-7 BCC 02 H
DI-1 ALU RESULT 02 H
DN2 DI-3 TRANSFER BUS 02 H

D3-2 ROM DATA 07 H
DI-3 BUF ROM DATA 07 H

DI-3 SEL H

D3-4 MASTER SCAN 01 H
DI-2 ALU RESULT 09 H
DI-1 ALU RESULT 06 H
DI-1 REGISTER B 09 H
DI-9 NPR DATI 01 H
D3-11 RAM OUTPUT 01 H
DI-5 SILO OUT 01 H
D2-6 NPR DATO 01 H
DI-7 BCC 01 H
DI-1 ALU RESULT 01 H
DI-3 TRANSFER BUS 01 H

D3-4 MASTER SCAN 00 H
DI-2 ALU RESULT 08 H
DI-1 ALU RESULT 05 H
DI-1 REGISTER B 08 H
DI-9 NPR DATI 00 H
D3-11 RAM OUTPUT 00 H
DI-5 SILO OUT 00 H
D2-6 NPR DATO 00 H
DI-7 BCC 00 H
DI-1 ALU RESULT 00 H
DI-3 TRANSFER BUS 00 H

REVISIONS		
ENG	CHANGE NO.	REV.

TITLE ALU AND TRANSFER BUS (DI-3)
SCALE — SHEET 4 OF 10
SIZE D CODE CS NUMBER M7836-0-1 REV. A
DIST.

DI-2 ALU RESULT 17 H
D3-11 RAM OUTPUT 17 H AT2
D2-3 RIRR 05 H AR1
BAI
DI-4 TRANSFER BUS 17 H
STB 74151 E16

DI-2 ALU RESULT 13 H
DI-7 BCC 13 H
DI-9 NPR DATO 13 H
DI-5 SILO OUT 13 H
D3-11 RAM OUTPUT 13 H API
AS2 DI-4 TRANSFER BUS 13 H
STB 74151 E11

DI-3 SEL H
DI-2 ALU RESULT 10 H
DI-7 BCC 10 H
DI-9 NPR DATO 10 H
DI-5 SILO OUT 10 H
D3-11 RAM OUTPUT 10 H EPE
D3-11 RAM OUTPUT 02 H EU2
D2-3 RIRR 02 H ER2
EV2 DI-4 TRANSFER BUS 10 H
STB 74151 E80

DI-2 ALU RESULT 16 H
D3-11 RAM OUTPUT 16 H AL2
D2-3 RIRR 04 H AR2
AL1 DI-4 TRANSFER BUS 16 H
STB 74151 E2

DI-2 ALU RESULT 12 H
DI-7 BCC 12 H
DI-9 NPR DATO 12 H
DI-5 SILO OUT 12 H
D3-11 RAM OUTPUT 12 H AN1
AP2 DI-4 TRANSFER BUS 12 H
STB 74151 E6

DI-2 ALU RESULT 09 H
DI-7 BCC 09 H
DI-9 NPR DATO 09 H
DI-5 SILO OUT 09 H
D3-11 RAM OUTPUT 09 H EE2
D3-11 RAM OUTPUT 01 H EJ1
D2-3 RIRR 01 H EM2
ES1 DI-4 TRANSFER BUS 09 H
STB 74151 E75

DI-2 ALU RESULT 15 H (CY2)
DI-7 BCC 15 H
DI-9 NPR DATO 15 H
DI-5 SILO OUT 15 H
D3-11 RAM OUTPUT 15 H AR2
D2-3 RIRR 07 H AU2
AV2 DI-4 TRANSFER BUS 15 H
STB 74151 E17

DI-2 ALU RESULT 11 H
DI-7 BCC 11 H
DI-9 NPR DATO 11 H
DI-5 SILO OUT 11 H
D3-11 RAM OUTPUT 11 H FV1
D2-3 RIRR 03 H FD1
BE2 DI-4 TRANSFER BUS 11 H
STB 74151 E87

DI-2 ALU RESULT 08 H
DI-7 BCC 08 H
DI-9 NPR DATO 08 H
DI-5 SILO OUT 08 H
D3-11 RAM OUTPUT 08 H EL2
D3-11 RAM OUTPUT 00 H EDI
D2-3 RIRR 00 H EN1
ER1 DI-4 TRANSFER BUS 08 H
STB 74151 E77

DI-3 BUF ROM DATA 04 H
DI-3 BUF ROM DATA 05 H
DI-3 BUF ROM DATA 06 H

D3-2 TRANSFER SOURCE ENAB L DK2
DI-3 BUF ROM DATA 07 H
7432 E55

DI-2 ALU RESULT 14 H
DI-7 BCC 14 H
DI-9 NPR DATO 14 H
DI-5 SILO OUT 14 H
D3-11 RAM OUTPUT 14 H BC1
D2-3 RIRR 06 H BB1
BF1 DI-4 TRANSFER BUS 14 H
STB 74151 E22

D3-3 SET/CLEAR 04 L EU2
STB STA 74155 E45
FB3 DI-4 SET ALU 02 L
FB2 DI-4 CLEAR ALU 02 L
FB1 DI-4 CLEAR ALU 01 L
FB0 DI-4 CLEAR ALU RESULT HIGH BYTE L
FA3 DI-4 SET SILO OUT L
FA2 DI-4 SET SILO IN L
FA1 DI-4 CLEAR RECEIVED DATA ENABLE L
FA0 DI-4 SET RECEIVED DATA ENABLE L
DI-2 BUF ROM DATA 02 H
DI-2 BUF ROM DATA 01 H
DI-2 BUF ROM DATA 00 H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ALU AND TRANSFER BUS (DI-4)	D	DCS	M7836-0-1	A
SCALE	SHEET 5 OF 10		DIST.	

D1-5 RECEIVER FLAG WAITING H

D1-5 READY IN L

D1-4 SILO IN L

D1-4 SET RECEIVED DATA ENABLE L

D1-5 RECEIVED DATA ENABLE H

D1-4 CLEAR RECEIVED DATA ENABLE L

D2-3 SCR Ø7 H

D1-5 RECEIVED CHARACTER WAITING H

D1-5 SILO OUT 15 H

D1-5 SILO OUT 14 H

D1-5 SILO OUT 13 H

D1-5 SILO OUT 12 H

D3-7 INIT D1 L

D1-5 SILO OUT 11 H

D1-5 SILO OUT 10 H

D1-5 SILO OUT Ø9 H

D1-5 SILO OUT Ø8 H

D3-3 RESYNC PULSE L

D1-9 INIT H

D3-3 ADVANCE MASTER SCANNER L

D3-4 MASTER SCAN Ø3 H

D3-4 MASTER SCAN Ø2 H

D3-4 MASTER SCAN Ø1 H

D3-4 MASTER SCAN Ø0 H

MASTER OR L

MASTER PE L

RECV DATA Ø7 L

RECV DATA Ø6 L

RECV DATA Ø5 L

RECV DATA Ø4 L

RECV DATA Ø3 L

RECV DATA Ø2 L

RECV DATA Ø1 L

RECV DATA Ø0 L

D1-4 SET SILO OUT L

D1-5 SILO OUT Ø7 H

D1-5 SILO OUT Ø6 H

D1-5 SILO OUT Ø5 H

D1-5 SILO OUT Ø4 H

D1-5 SILO OUT Ø3 H

D1-5 SILO OUT Ø2 H

D1-5 SILO OUT Ø1 H

D1-5 SILO OUT Ø0 H

-15V FB2 D4 D3 D2 D1 D664 -12V (TO PIN 1 OF ALL 3341'S) C1Ø2 4.8 UFD

NC.

REVISIONS

CHK	CHANGE NO.	REV.

TITLE: ALU AND TRANSFER BUS (D1-5I)

SIZE D CODE DCS NUMBER M7836-Ø-1 REV. A

SCALE — SHEET 6 OF 10

DIST.

DI-2 REG A 0 H
DI-1 REG B 0 H → 7486 E56 → DI-6 LRC 00 H

DI-2 REG A 1 H
DI-1 REG B 1 H → 7486 E56 → DI-6 LRC 01 H

DI-2 REG A 2 H
DI-1 REG B 2 H → 7486 E56 → DI-6 LRC 02 H

DI-2 REG A 3 H
DI-1 REG B 3 H → 7486 E56 → DI-6 LRC 03 H

DI-2 REG A 4 H
DI-1 REG B 4 H → 7486 E64 → DI-6 LRC 04 H

DI-2 REG A 5 H
DI-1 REG B 5 H → 7486 E64 → DI-6 LRC 05 H

DI-2 REG A 6 H
DI-1 REG B 6 H → 7486 E64 → DI-6 LRC 06 H

DI-2 REG A 7 H
DI-1 REG B 7 H → 7486 E64 → DI-6 LRC 07 H

7486 E39 → DI-6 CRC16-06 H

7486 E39 → DI-6 CRC16-08 H

7486 E39 → DI-6 CRC16-09 H

7486 E34 → DI-6 CRC16-10 H

7486 E34 → DI-6 CRC16-11 H

7486 E34 → DI-6 CRC16-12 H

7486 E34 → DI-6 CRC16-13 H

7486 E44 → DI-6 CRC-CCITT 12 H

DI-1 REG B 8 H
7486 E44 → DI-6 CRC-CCITT 13 H

DI-1 REG B 9 H
7486 E44 → DI-6 CRC-CCITT 14 H

DI-1 REG B 10 H
7486 E44 → DI-6 CRC-CCITT 15 H

DI-1 REG B 11 H → 7486 E42 → DI-6 CRC16-07 H

7486 E42 → DI-6 CRC16-14 H

7486 E42 → DI-6 CRC16-15 H

DI-6 CRC16-13 H

7486 E47 → DI-6 CRC16-00 H

DI-1 REG B 12 H
7486 E43 → DI-6 CRC-CCITT 00 H

7486 E43 → DI-6 CRC-CCITT 01 H

7486 E43 → DI-6 CRC-CCITT 02 H

7486 E48 → DI-6 CRC-CCITT 03 H

DI-1 REG B 13 H
7486 E43 → DI-6 CRC-CCITT 07 H

7486 E47 → DI-6 CRC-CCITT 08 H

7486 E33 → DI-6 CRC-CCITT 09 H

7486 E33 → DI-6 CRC-CCITT 10 H

DI-1 REG B 14 H
7486 E48 → DI-6 CRC-CCITT 06 H

DI-1 REG B 15 H
7486 E48 → DI-6 CRC-CCITT 05 H

DI-1 REG B 12 H
7486 E48 → DI-6 CRC-CCITT 04 H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ALU AND TRANSFER BUS (DI-6)	D	CS	M7836-0-1	A
SCALE — SHEET 7 OF 10	DIST.			

DCS M7836-0-1 REV A

DI-6 CRC-CCITT Ø1 H
DI-6 REG B Ø9 H
DI-6 LRC Ø1 H
74153 E49 1/2 +1
DI-6 CRC-CCITT ØØ H
DI-6 CRC-16 ØØ H
DI-6 LRC ØØ H
74153 E49 1/2 +Ø
D3-11 RAM CO2 S OUTPUT Ø4H
74Ø4 E59
+3V
7437 E79

DI-6 CRC-CCITT Ø3 H
DI-6 REG B 11 H
DI-6 LRC Ø3 H
74153 E53 1/2 +1
DI-6 CRC-CCITT Ø2 H
DI-6 REG B 1Ø H
DI-6 LRC Ø2 H
74153 E53 1/2 +Ø

DI-6 CRC-CCITT Ø5 H
DI-6 REG B 13 H
DI-6 LRC Ø5 H
74153 E54 1/2 +1
DI-6 CRC-CCITT Ø4 H
DI-6 REG B 12 H
DI-6 LRC Ø4 H
74153 E54 1/2 +Ø

DI-6 CRC-CCITT Ø7 H
DI-6 CRC-16 Ø7 H
DI-6 LRC Ø7 H
74153 E38 1/2 +1
DI-6 CRC-CCITT Ø6 H
DI-6 CRC-16 Ø6 H
DI-6 LRC Ø6 H
74153 E38 1/2 +Ø

74174 E59
D0 R0(1) → DI-7 BCC Ø5 H
D1 R1(1) → DI-7 BCC Ø4 H
D2 R2(1) → DI-7 BCC Ø3 H
D3 R3(1) → DI-7 BCC Ø2 H
D4 R4(1) → DI-7 BCC Ø1 H
D5 R5(1) → DI-7 BCC ØØ H
CLR CLK

74157 E37
DI-6 CRC-16 Ø8 H
DI-6 CRC-CCITT Ø8 H
DI-6 CRC-16 Ø9 H
DI-6 CRC-CCITT Ø9 H
DI-6 CRC-16 1Ø H
DI-6 CRC-CCITT 1Ø H
DI-6 CRC-1611 H
DI-6 LRC Ø3 H
STB SØ

D3-11 RAM OUTPUT Ø3 L
74Ø4 E65

74157 E32
DI-6 CRC 16 12 H
DI-6 CRC-CCITT 12 H
DI-6 CRC 16 13 H
DI-6 CRC-CCITT 13 H
DI-6 CRC-16 14 H
DI-6 CRC-CCITT 14 H
DI-6 CRC-16 15 H
DI-6 CRC-CCITT 15 H
STB SØ

74174 E36
D5 R5(1) → DI-7 BCC Ø8 H
D4 R4(1) → DI-7 BCC Ø9 H
D3 R3(1) → DI-7 BCC 1Ø H
D2 R2(1) → DI-7 BCC 11 H
D1 R1(1) → DI-7 BCC 12 H
D0 R0(1) → DI-7 BCC 13 H
CLR CLK

74175 E31
D3 R3(1) → DI-7 BCC 14 H
D2 R2(1) → DI-7 BCC 15 H
D1 R1(1) → DI-7 BCC Ø6 H
D0 R0(1) → DI-7 BCC Ø7 H
CLR CLK

D3-7 INIT DI L (ES2)
D3-7 DATA STROBE L FE1
D3-2 BCC CALCULATION L FC1
74Ø2 E84

REVISIONS
CHR	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ALU AND TRANSFER BUS (DI-7)	D	CS	M7836-Ø-1	A
SCALE —	SHEET 8 OF 10	DIST.		

DCS M7836-Ø-1 A

D3-2 ROM DATA Ø9 H
D3-2 ROM DATA Ø8 H
DI-4 TRANSFER BUS 17 H
DI-4 TRANSFER BUS 16 H
DI-9 BUF INIT L
D3-6 NPR ADDRESS REGISTER CLOCK L
DI-4 TRANSFER BUS 15 H
DI-4 TRANSFER BUS 14 H
DI-4 TRANSFER BUS 13 H
DI-4 TRANSFER BUS 12 H
DI-4 TRANSFER BUS 11 H
DI-4 TRANSFER BUS 10 H
DI-4 TRANSFER BUS Ø9 H
DI-4 TRANSFER BUS Ø8 H
DI-3 TRANSFER BUS Ø7 H
DI-3 TRANSFER BUS Ø6 H
D3-7 INIT DI L
DI-3 TRANSFER BUS Ø5 H
DI-3 TRANSFER BUS Ø4 H
DI-3 TRANSFER BUS Ø3 H
DI-3 TRANSFER BUS Ø2 H
DI-3 TRANSFER BUS Ø1 H
DI-3 TRANSFER BUS Ø0 H

74175 E4
74175 E9
74174 E27
74174 E35
7404 E9Ø
7404 E35

D2-7 ADDRESS TO BUS L

8838 E3
8838 E2Ø
8838 E15
8838 E25

DI-8 C1 H
DI-8 BUS C1 L
DI-8 C0 H
DI-8 BUS C0 L
DI-8 A17 H
DI-8 BUS A17 L
DI-8 BUS A12 L
DI-8 BUS A11 L
DI-8 BUS A10 L
DI-8 BUS A09 L
DI-8 BUS A08 L
DI-8 BUS A07 L
DI-8 BUS A06 L
DI-8 BUS A05 L
DI-8 BUS A04 L
DI-8 BUS A03 L
DI-8 BUS A02 L
DI-8 BUS A01 L
DI-8 A00 H
DI-8 BUS A00 L
DI-8 A03 H
DI-8 BUS A02 L
DI-8 A02 H
DI-8 A01 H
DI-8 A00 H
DI-8 NPR ADDR00 H

DI-8 BUS A16 L
DI-8 BUS A15 L
DI-8 BUS A14 L
DI-8 BUS A13 L
DI-8 ADDRESS SELECTED H

8881 E8
8640 E13
8242 E7

S1-1 R6 1K
S1-2 R7 1K
S1-3 R8 1K
S1-4 R9 1K
S1-5 R10 1K
S1-6 R11 1K
S1-7 R12 1K
S1-8 R13 1K
S1-9 R14 1K
+5V

8242 E7
8242 E10
8242 E12

R4 1K

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ALU AND TRANSFER BUS (DI-8)	D	CS	M7836-Ø-1	A
SCALE	SHEET 9 OF 10	DIST.		

BUS PB L ANZ — 8640 E13 pin 16
BUS PA L AMI — 8640 E13 pin 2

7408 E94 pin 8 FP2 — DI-9 MEM PAR ERR H

74157 E1
D2-3 BUF DATAØØH AK2 — AØ
D2-3 BUF DATAØ8 H AJ2 — BØ
D2-3 BUF DATA Ø1 H AH2 — A1
D2-3 BUF DATAØ9H AF1 — B1
D2-3 BUF DATAØ2H AE2 — A2
D2-3 BUF DATA 1Ø H AF2 — B2
D2-3 BUF DATAØ3 H AH1 — A3
D2-3 BUF DATA 11 H AE1 — B3
STB SØ — pin 15
ØØ, Ø1, Ø2, Ø3

74175 E28
D3 R3(1) / R3(Ø) — DI-9 NPR DATI Ø2 H
D2 R2(1) / R2(Ø) — DI-9 NPR DATI Ø3 H
D1 R1(1) / R1(Ø)
DØ RØ(1) / RØ(Ø)
CLR CLK

DI-8 NPR ADDR ØØ H CH2

74157 E40
D2-3 BUF DATA Ø4 H CS2
D2-3 BUF DATA 12 H CR2
D2-3 BUF DATA Ø5 H CP2
D2-3 BUF DATA 13 H CN2
D2-3 BUF DATA ØG H CL2
D2-3 BUF DATA 14 H CK2
D2-3 BUF DATA Ø7 H CJ2
D2-3 BUF DATA 15 H CM2
STB SØ — pin 15
ØØ, Ø1, Ø2, Ø3

74174 E45
D4 R4(1) — DI-9 NPR DATI ØØ H
D1 R1(1) — DI-9 NPR DATI Ø1 H
D5 R5(1) — DI-9 NPR DATI Ø4 H
D3 R3(1) — DI-9 NPR DATI Ø5 H
D2 R2(1) — DI-9 NPR DATI Ø6 H
DØ RØ(1) — DI-9 NPR DATI Ø7 H
CLR CLK

D3-7 DATA STROBE H CT2 — T4Ø4 E14 — T4Ø2 E84 — DI-9 BUF INIT L
DI-9 INIT H

74175 E92
DI-4 TRANSFER BUS ØB H — DI-9 NPR DATO Ø8 H
DI-4 TRANSFER BUS Ø9 H — DI-9 NPR DATO Ø9 H
DI-4 TRANSFER BUS 1Ø H — DI-9 NPR DATO 1Ø H
DI-4 TRANSFER BUS 11 H — DI-9 NPR DATO 11 H
CLR CLK

74175 E19
DI-4 TRANSFER BUS 12 H — DI-9 NPR DATO 12 H
DI-4 TRANSFER BUS 13 H — DI-9 NPR DATO 13 H
DI-4 TRANSFER BUS 14 H — DI-9 NPR DATO 14 H
DI-4 TRANSFER BUS 15 H — DI-9 NPR DATO 15 H
CLR CLK

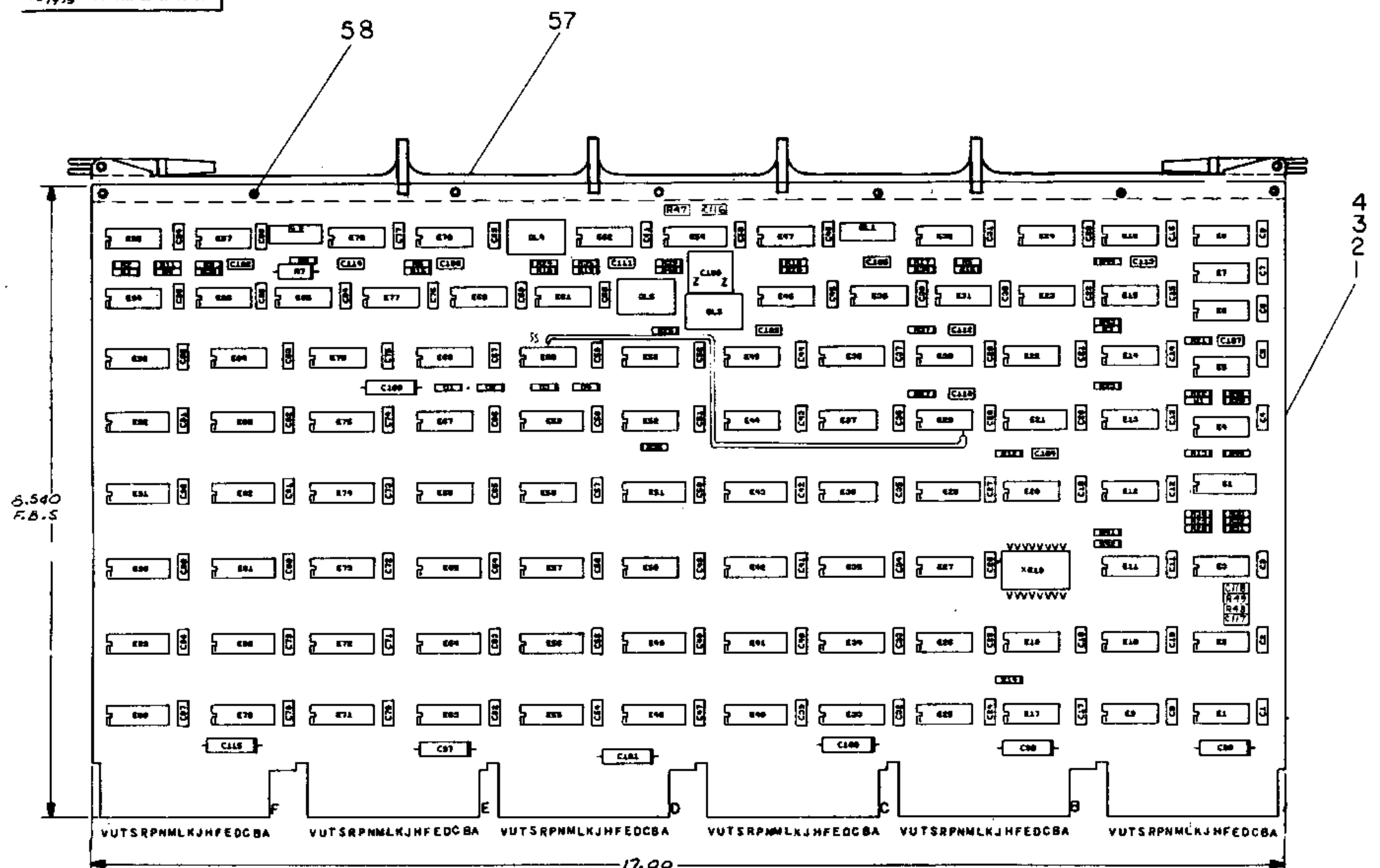
D3-7 INIT DI L ES2

D3-6 NPR DATO REGISTER CLOCK L AU1 — T4Ø4 E15

REVISIONS		
CHR	CHANGE NO.	REV.

TITLE	ALU AND TRANSFER BUS 101-91	SIZE D	CODE CS	NUMBER M7836-Ø-1
SCALE	—	SHEET 10 OF 10	DIST.	REV. A

NOTES: R47,R48,R49,C116,C117,C118 ARE ECO#2 ADDITIONS.



CAUTION: OFF SHEET PARTS LIST.
SEE K-PL-M7837-Ø-Ø.

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7837-Ø-Ø	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7837-Ø-Ø	2
REF		MODULE ECO HISTORY	B-MH-M7837-Ø-Ø	3
1		ETCHED CIRCUIT BOARD	5010977	4
3	C104,C110,C111	CAP 10 PF 100V 5%	1000006	5
5	C109,C106,C112,C102,C107	CAP 100 PF 100V 5%	1000016	6
3	C113,C117,C118	CAP 330 PF 100V 5%	1000023	7
2	C105,C116	CAP 470 PF 100V 5%	1000024	8
1	C103	CAP 1500 PF 100V 5%	1002478	9
94	C1 – C94	CAP .01 UF 100V 20%	1001610-01	10
7	C97–C101, C108, C115	CAP 6.8 UF 35V 10%	1005306	11
4	D1–D4	DIODE D664	1100114	12
9	E8, E12, E22, E53, E60, E66, E67, E77, E84.	I.C DEC 7474	1905547	13
3	E15, E69, E86	I.C DEC 7400	1905575	14
1	E68	I.C DEC 7410	1905576	15
6	E6, E13, E24, E31, E36, E94	I.C DEC 7402	1909004	16
1	E76	I.C DEC 74H55	1909063	17
7	E4, E7, E18, E25, E26, E27, E32	I.C DEC 8640	1911969	18
2	E61, E95	I.C DEC 74S74	1910544	19
3	E16, E44, E50	I.C DEC 7404	1909686	20
8	E1, E2, E3, E9, E10, E11, E14, E17	I.C DEC 8881	1909705	21
16	E71, E72, E73, E74, E75, E79, E80, E81, E82, E83, E88, E89, E90, E91, E92, E93	I.C DEC 74151	1909936	22
1	E38.	I.C DEC 7492	1910096	23
1	E51	I.C DEC 4015	1910087	24
2	E37, E58	I.C DEC 7437	1910091	25
4	E23, E47, E52, E85	I.C DEC 7408	1910155	26
9	E5, E20, E29, E30, E45, E62, E70, E78, E87	I.C DEC 74121	1910230	27
7	E28, E34, E40, E48, E56, E59, E63	I.C DEC 74175	1910651	28
3	E33, E64, E65	I.C DEC 74174	1910652	29
4	E35, E41, E42, E43	I.C DEC 74157	1910655	30
1	E49	I.C DEC 74155	1910656	31
1	E54	I.C DEC 74123	19104[illegible]	32
14	R28, R27, R30, R31, R32, R33, R35, R11, R14, R15, R18, R19, R22, R36	RES 1K 1/4W 5%	1300365	33
1	R37	RES 3K 1/4W 5%	1300432	34
1	R17	RES 3.3K 1/4W 5%	1300439	35
1	R34	RES 10K 1/4W 5%	1300479	36

PARTS LIST

ETCH BOARD REV. B

FIRST USED ON OPTION MODEL: DV11-AA

IC TYPE	GND	+5V
I.C DEC 74151	8	16
I.C DEC 7492	8	16
I.C DEC 4015	8	16
I.C DEC 74175	8	16
I.C DEC 74174	8	16
I.C DEC 74157	8	16
I.C DEC 74155	8	16
I.C DEC 74123	8	16

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

CHANGE NO.	REV.
W. SMITH 13-NOV-81	J
M7837-HK897	
R. HARRINGTON	H
M7837-00006	
J. MCNAMARA 12-SEP-77	F
M7837-00005	
J. MCNAMARA 3-NOV-76	E
ECO M7837-00004	
J.M. NAMARA	D
M7837-00003	
J. MCNAMARA	C
M7837-00002	
J. MCNAMARA	B
M7837-00001	
ORIGINATED	A

REVISIONS

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

DRN DATE 1/24/75
CHKD DATE 2/4/75
ENG DATE 3-4-75
PROJ. ENG. DATE 3-10-75
PROD. DATE 3-10-75

NEXT HIGHER ASSY B-DD-DV11-Ø

SCALE —
SHEET 1 OF 11

digital

TITLE UNIBUS DATA AND NPR CONTROL

SIZE D CODE CS NUMBER M7837-Ø-1 REV. J

MK

5	R45,R45,R44,R46,R43	RES 180Ω 1/4 W 5%	1301832	37
3	R42,R39,R42	RES 750Ω 1/4W 5%	1301901	38
3	R38, R13, R30	RES 390Ω 1/4 W 5%	1300909	39
1	R7	RES 2.21K, 1/2W, 1% RN60	1312404	40
1	R35	RES 18K 1/4 W 5%	1302469	41
2	R6, R9	RES 2.74K 1/4 W 1% RN55	1304068	42
1	R26	RES 9.1K 1/4 W 5%	1300847	43
3	R48,R48,R49	RES 820Ω 1/4W 5%	1300871	44
1	R16	RES 100Ω 1/4W 5%	1300829	45
5	R1, R40, R41, R5, R8	RES 330Ω 1/4W 5%	1300895	46
2	R27, R12	RES 6.8K 1/4W 5%	1301423	47
2	R4, R36	RES 470Ω 1/4W 5%	1300376	48
1	R10	RES 47K 1/4 W 5%	1302177	49
1	R21	RES 1.5K 1/4 W 5%	1300391	50
1		SWITCH RKR COVER, 8 POS	12111284-04	51
1	U19	SOCKET 16 PIN	12 09838	52
1	S1	SWITCH SOCKET DIP	12111164-04	53
2	DL1, DL2	DELAY LINE 30 NS	16055828-01	54
2	DL4, DL5	DELAY LINE 50 NS	16094228	55
1	DL3	DELAY LINE 100NS	16093594	56
1		HANDLE HEX	12107711-02	57
12		EYELET	90006732	58
1	W1	JUMPER INSULATED	9009185	59
1	U21	IC DEC 74193	12100018	60
2	E35, E37	I.C DEC 3341	21111128	61
1	C114	CAP, 68PF, 100V, 5%	10000014	62
2	E33,E46	IC. DEC 7432	1311521	63
AR		WIRE, #30 AWG INSULATED	9105740	64
1	R47	RES 15Kn 1/4W 5%	1300496	65

CAUTION:
OFF SHEET PARTS LIST.
SEE K-PL-M7837-Ø-2.

REVISIONS		
CAGE	CHANGE NO.	REV

TITLE	UNIBUS DATA AND NPR CONTROL	SIZE	CODE	NUMBER / REV.
SCALE	SHEET 2 OF 11	D	DCS	M7837-Ø-1 J
		DIST.		

1.MK

D2-1 DATA FOR BUS ØØ H
D2-4 SCR ØØ H
D2-9 RICR ØØ H
D3-2 BRANCH 9 L
D3-F SRS ØØH
D3-9 RAM UNIDATAØØ H
D3-2 ROM DATA ØØ H
D2-9 NPR STATUS ØØ H
D2-3 RIRR ØØ H
D1-B AØØ H CU2
7437 E37
D2-1 DATA SOURCE C L

D2-1 DATA FOR BUS Ø2 H
D2-4 SCR Ø2 H
D2-9 RICR Ø2 H
D3-8 SRS Ø2 H
D3-9 RAM UNIDATAØ2 H
D3-2 ROM DATA Ø2 H
D2-9 NPR STATUS Ø2 H
D2-3 RIRR Ø2 H
D1-B AØ1 H CN2
7437 E87
D2-1 DATA SOURCE A L

D2-1 DATA FOR BUS Ø1H
D2-4 SCR Ø1 H
D2-9 RICR Ø1 H
D3-2 BRANCH 8 L
D3-8 SRS Ø1H
D3-9 RAM UNIDATAØ1H
D3-2 ROM DATA Ø1 H
D2-9 NPR STATUS Ø1 H
D2-3 RIRR Ø1 H
D1-B AØ1 H CS1
7447 E97
D2-1 DATA SOURCE B L

D2-1 DATA FOR BUS Ø4 H
D2-4 SCR Ø4H
D2-9 RICR Ø4 H
D3-10 RAM UNIDATA 10 H
D3-9 RAM UNIDATAØ4 H
D3-2 ROM DATAØ4 H
D2-3 RIRR Ø4 H

D2-1 DATA BUS Ø4 H
D2-4 SCR Ø7H
D2-9 RICR Ø7 H
D2-3 LCR Ø7 H
D3-9 RAM UNIDATA Ø7 H
D3-2 ROM DATA Ø7H
D2-3 RIRR Ø7 H
D2-1 DATA FOR BUS Ø7 H

D2-1 DATA FOR BUS Ø5H
D2-4 SCR Ø5H
D2-9 RICR Ø5 H
D3-10 RAM UNI DATA 17 H
D3-9 RAM UNIDATA Ø5 H
D3-2 ROM DATA Ø5 H
D2-3 RIRR Ø5 H

D2-1 DATA FOR BUS Ø6 H
D2-4 SCR Ø6 H
D2-9 RICR Ø6 H
D3-9 RAM UNIDATA Ø6H
D3-2 ROM DATA Ø6H
D2-3 RIRR Ø6H

D2-1 DATA FOR BUS Ø9H
D2-4 SCR Ø9 H
D2-9 RICR Ø9 H
D2-3 LCR Ø9 H
D3-8 SRS Ø9H
D3-10 RAM UNI DATA Ø9 H
D3-2 ROM DATA Ø9 H
D2-9 NPR STATUS Ø9 H

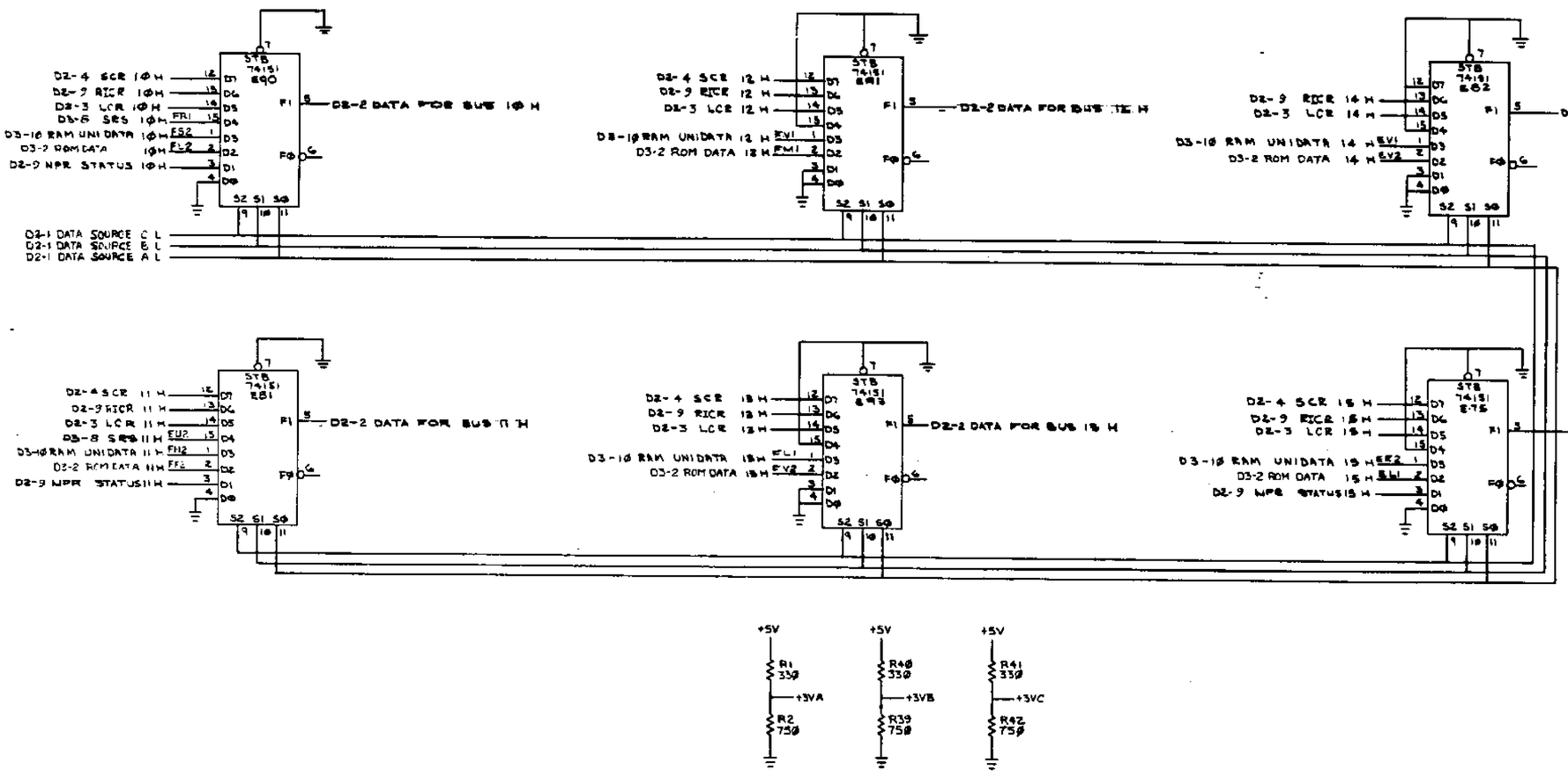
D2-1 DATA FOR BUS Ø8 H
D2-4 SCR Ø8H
D2-9 RICR Ø8 H
D2-3 LCR Ø8H
D3-8 SRS Ø8H
D3-9 RAM UNIDATA Ø8 H
D3-2 ROM DATA Ø8H
D2-9 NPR STATUS Ø8H

STB 74151 E70
STB 74151 E71
STB 74151 E53
STB 74151 E76
STB 74151 E83
STB 74151 E80
STB 74151 E92
STB 74151 E72
STB 74151 E84

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	UNIBUS DATA & NPR CONTROL (D2-1)	SIZE/CODE	NUMBER	REV.
SCALE	—	D CS	M7837-Ø-1	J
SHEET	3 OF 11	DIST.	MK	



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	UNIBUS DATA & NPR CONTROL (D2-2)	
SIZE/CODE	D CS M7837-Ø-1	REV. J
SCALE		SHEET 4 OF 11
DWG.	MK	

DCS M7837-Ø-1 J

D2-6 BUS DIS L
D2-6 BUS DI4 L
D2-9 A BUFFERED INIT D2 L
D2-6 BUS DI3 L
D2-6 BUS DI2 L
D2-6 BUS DI1 L
D2-6 BUS DIØ L
D2-6 BUS DI7 L
D2-6 BUS DI6 L
D2-5 LOAD LCR H
D3-5 2400 BAUD
D2-3 LCR 15 H
R26 4.7K +5V
DMI
D2-3 CONTCOL STROBE H
C199 100PF
74174 E33
CLZ D2-3 LCR 14 H
CEZ D2-3 LCR 13 H
SVI D2-3 LCR 12 H
CBI D2-3 LCR 11 H
CDZ D2-3 LCR 10 H
CJI D2-3 LCR Ø9 H
D2-3 LCR Ø8 H
D3-5 2Ø48 KB H
BR2 D2-3 BUF DATA 15 H
CF2 D2-3 BUF DATA 14 H
CEI D2-3 BUF DATA 13 H
CB2 D2-3 BUF DATA 12 H
BRI D2-3 BUF DATA 11 H
CDI D2-3 BUF DATA 10 H
CFI D2-3 BUF DATA Ø9 H
BSI D2-3 BUF DATA Ø8 H
74121 E45
74193 E21
BIT WINDOW L
BVI
D2-3 LCR Ø7 H
D2-6 BUS DØ7 L
D2-6 BUS DØ6 L
D2-6 BUS DØ5 L
D2-6 BUS DØ4 L
D2-6 BUS DØ3 L
D2-6 BUS DØ2 L
D2-6 BUS DØ1 L
D2-6 BUS DØØ L
D2-3 SET CLEAR Ø3 L
D3-2 ROM DATA Ø2 H
D3-2 ROM DATA Ø1 H
D3-2 ROM DATA ØØ H
74175 E69
D2-3 RIEE Ø7 H
D2-3 RIEE Ø6 H
D2-3 RIEE Ø5 H
D2-3 RIEE Ø4 H
D2-3 BUF DATA Ø4 H
D2-3 BUF DATA Ø5 H
D2-3 BUF DATA Ø6 H
D2-3 BUF DATA Ø7 H
D2-3 SET RECEIVER INTERRUPT L
D2-3 SET SCR 10 L
D2-3 SET RICE 14 L
D2-3 SET EICE 15 L
D2-3 CLEAR NXM L
D2-3 CLEAR SCR ØB L
D2-3 SET RICE 12 L
D2-3 SET EICE 13 L
D2-3 BUF DATA ØØ H
D2-3 BUF DATA Ø1 H
D2-3 BUF DATA Ø2 H
D2-3 BUF DATA Ø3 H
D2-3 RIEE Ø3 H
D2-3 RIEE Ø2 H
D2-3 RIEE Ø1 H
D2-3 RIEE ØØ H
D2-3 MAINTENANCE CLK PULSE H
D2-5 LOAD RIRR H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA AND NPR CONTROL (2-3)	D	DCS	M7837-Ø-1	J
SCALE	SHEET 5 OF 11	DIST.	MK	

D2-3 BUF DATA Ø3 H — 74175 E69 D3 — R3(1) — D2-4 SCR Ø3 H (SOURCE SELECT); R3(0) — D2-4 SCR Ø3 L
D2-3 BUF DATA Ø2 H — D2 — R2(1) — D2-4 SCR Ø2 H (BRANCH DISABLE); R2(0)
D2-3 BUF DATA Ø4 H — D1 — R1(1) — D2-4 SCR Ø4 H (MEMEX A16); R1(0)
D2-3 BUF DATA ØØ H — D0 — R0(1) — D2-4 SCR ØØ H (MICROPROCESSOR AC); R0(0)
CLR CLK
D2-9 B BUFFERED INIT D2 L
D2-3 BUF DATA Ø1 H — 7474 E66 — FP1 — D2-4 SCR Ø1 H (ROM SINGLE STEP)
D3-7 Ø1 L (B11) — 7400 E28
FN2 — D2-4 SCR Ø5 H (MEMEX A17)
D2-3 BUF DATA Ø5 H — 7474 E67
D2-3 BUF DATA Ø6 H — 7474 E67 — D2-4 SCR Ø6 H (RECV INTR ENAB)
D2-3 SET RECEIVER INTERRUPT L
D2-3 BUF DATA Ø7 H — 7474 E68 — DV1 — D2-4 SCR Ø7 H (RECV INTERRUPT)
D2-5 LOAD SCR LOW BYTE H — 7400 E23
D2-8 TEMPDEMY DISABLE L — 7410 E68
+3V
D2-3 BUF DATA Ø8 H — 7474 E12 — AV2 — D2-4 SCR Ø8 H (RECV INTERRUPT RESPONSE COMPLETE)
E44 220Ω; C113 330 PF
7400 E15
7400 E47
D2-3 SET SCR 10 L
D2-3 BUF DATA 10 H — 7474 E66 — D2-4 SCR 10 H (NPR STATUS OVERFLOW INTR)
R47 15K; C116 470 PF
D2-3 CLR SCR Ø8 L — E54 74123 3NS — +3
D2-3 BUF DATA 15 H — 7474 E12 — D2-4 SCR 15 H
D2-9 NPR STATUS AVAILABLE L — 7400 E15
7410 E28 — 7400 E29 — D2-4 B REQUEST H — 7404 E16 — D2-4 B REQUEST L
7410 E68 — 7404 E76 — D2-4 A REQUEST H
D2-4 A REQUEST L
74175 E28
D2-3 BUF DATA 11 H — D3 — R3(1) — BP2 — D2-4 SCR 11 H (MASTER CLEAR); R3(0)
D2-3 BUF DATA Ø9 H — D2 — R2(1) — D2-4 SCR Ø9 H (SCR'S WRITE ENABLE); R2(0)
D2-3 BUF DATA 13 H — D1 — R1(1) — D2-4 SCR 13 H (NPR STATUS INTR EN); R1(0)
D2-3 BUF DATA 12 H — D0 — R0(1) — D2-4 SCR 12 H (STORAGE INTR EN); R0(0)
CLK CLR
D2-5 LOAD SCR HIGH BYTE H — 7404 E16 — 7410 E29 — C114 10PF — +5V — R27 4.8K

REVISIONS		
CHR	CHANGE NO.	REV.

TITLE: UNIBUS DATA & NPR CONTROL (D2-4)
SIZE: D | CODE | NUMBER: DCS M7837-Ø-1 | REV: J
SCALE | SHEET 6 OF 11 | DIST. | MK

7442 E38

D3 – 7 INSTRUCTION DECODER ENABLE A L CJ2
D1-8 A03 H CU2
D1-8 A02 H CS1
D1-8 A01 H CNZ

D1-8 A00 H AM1
D1-8 C0 H AT2
D1-8 C1 H BH1

7404 E16 (×4)
7402 E24 (×3)
7432 E39 (×3)
7402 E31 (×3)
7432 E31
7432 E39
7432 E46
7402 E36
7402 E24 (×2)
7402 E31 (×2)
7432 E39
7437 E37
7402 E36

D2-5 LOAD LCR H
D2-5 UNIBUS RAM WRITE L
D2-5 LOAD SFR L
D2-5 LOAD XXX H
D2-5 LOAD SRS HIGH BYTE H
D2-5 LOAD SRS LOW BYTE H
D2-5 LOAD SCR HIGH BYTE H
D2-5 LOAD SCR LOW BYTE H
D2-5 READ REGISTER H
D2-5 DATA TO BUS H
D2-5 READ NPR STATUS H

D2-T NPR DATA TO BUS L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	UNIBUS DATA AND NPR CONTROL (D2-5)	SIZE/CODE	NUMBER / REV.
SCALE	NONE	SHEET 7 OF 17	D DCS M7837-0-1 J
DIST.			MK

DI-3 TRANSFER BUS 04 H
DI-3 TRANSFER BUS 03 H
DI-3 TRANSFER BUS 06 H
DI-3 TRANSFER BUS 07 H
DI-3 TRANSFER BUS 05 H
DI-3 TRANSFER BUS 01 H
DI-3 TRANSFER BUS 02 H
DI-3 TRANSFER BUS 00 H
D2-9 @ BUFFERED INIT D 2 L
D3-6 UPE DATO REG CLK L
D2-6 NPR DATO 07 H
D2-6 NPR DATO 06 H
D2-6 NPR DATO 05 H
D2-6 NPR DATO 04 H
D2-6 NPR DATO 03 H
D2-6 NPR DATO 02 H
D2-6 NPR DATO 01 H
D2-6 NPR DATO 00 H
DE-2 DATA FOR BUS 15 H
DE-2 DATA FOR BUS 14 H
DE-2 DATA FOR BUS 13 H
DE-2 DATA FOR BUS 12 H
DE-2 DATA FOR BUS 11 H
DE-2 DATA FOR BUS 10 H
D2-1 DATA FOR BUS 09 H
D2-1 DATA FOR BUS 08 H
DE-1 DATA FOR BUS 07 H
DE-1 DATA FOR BUS 06 H
DE-1 DATA FOR BUS 05 H
DE-1 DATA FOR BUS 04 H
DE-1 DATA FOR BUS 03 H
DE-1 DATA FOR BUS 02 H
DE-1 DATA FOR BUS 01 H
DE-1 DATA FOR BUS 00 H
DE-5 READ REGISTER H
DI-8 NPR ADDR 00 H
DE-7 NPR DATA TO BUS L
DE-5 DATA TO BUS H
DE-8 VECTOR TO BUS L
D2-8 VECTOR BIT 02 H
D2-6 BUS DI5 L
D2-6 BUS DI4 L
D2-6 BUS DI3 L
D2-6 BUS DI2 L
D2-6 BUS DI1 L
D2-6 BUS DI0 L
D2-6 BUS DØ9 L
D2-6 BUS DØ8 L
D2-6 BUS DØ7 L
D2-6 BUS DØ6 L
D2-6 BUS DØ5 L
D2-6 BUS DØ4 L
D2-6 BUS DØ3 L
D2-6 BUS DØ2 L
D2-6 BUS DØ1 L
D2-6 BUS DØØ L
D2-6 BUS INTR L

REVISIONS		
CHG	CHANGE NO.	REV.

TITLE	SIZE	NUMBER	REV.
UNIBUS DATA & NPR CONTROL (D2-6)	D	DCS M7837-Ø-1	J
SCALE —	SHEET 8 OF 11	DIST.	

+5V R5 330 DL1 30NS R4 470
8640 E32 7402 E94 DE-7 NO BBSY NO SSYN H
D3-7 BUS SSYN L BU1 R16 100 R17 3.3K R34 10K C105 470 PF
D2-7 SSYN H
7400 E86 7402 E94 74121 E78 200NS C106 100 PF R6 2.7K
DE-7 NPR DATA TO BUS L
D1-8 C1 H 14H65 E76
+5V R8 330 D3-2 NPR OPERATION L EK1 FJ2 DL2 30NS R38 470 D3-7 Ø2 L
74124 E78 C119 68PF R7 2.21K 1/2W, 1%
+3V 74174 E96 BG BUS
BF3 D2-T REQUEST BUS H 8881 E17 AE2 D2-T BUS NPR L
7400 E86 74174 E96 GRANT +5V E14 18Ø 8881 E17 BD1 D2-T BUS NPG OUT H
7400 E69
R45 +5V 18Ø BUS NPG IN H AU1 R13 390 8640 E4 7464 E44 R24 1K
DL4 50NS R19 1K 74174 E77 SACK 8881 E17 AP2 D2-T/D2-8 BUS BSY L
7400 E85 74174 E77 BSY 7402 E13
7400 E85 BHI D2-7 ADDRESS TO BUS L
R10 47K C103 1500PF 74128 E54 20MS
+3V
R9 2.7K +5V 74121 E87 MSYN WAIT 200NS C102 100PF
74174 E84 MSYN BE-6 ASSERT MSYN H
7404 E44 7400 E86 D2-9 B BUFFER1 OUT D2 L D2-3 CLEAR NXM L
7474 E86 CLR 7402 E94
74121 E28 DATA STROBE 1.0MS BF1 DE-7 DATA STROBE H C104 100PF R12 6.8K +5V
R25 1K DL3 100NS R11 1K 74174 E75 TIME OUT EK1 D2-7 NXM H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE UNIBUS DATA & NPR CONTROL (D2-7)
SCALE SHEET 9 OF 11
SIZE D CODE CS NUMBER M7837-Ø-1 REV. J
DIST. MX

* IN FOR 11/20 WITH KNIL OUT FOR ALL OTHERS.

D2-4 A REQUEST H
D2-4 B REQUEST H
D2-4 A REQUEST L
D2-4 A REQUEST H
D2-4 B REQUEST L
D2-4 B REQUEST H
D2-8 TEMPORARY DISABLE L
D2-9 INIT H
D2-7 SSYN H
D2-7 BUS VPR L
D2-8 VECTOR BIT 8RN
D2-8 VECTOR TO BUS L
D2-7/D2-8 BUS BSY L
D2-7/D2-8 BUS SACK L
D2-7 NO BSY NO SSYN H
BUS BG5 OUT H
BUS BG5 IN H
BUS BG6 OUT H
BUS BG6 IN H
BUS BR6 L
BUS BR5 L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA & NPR CONTROL (D2-8)	D	DCS	M7837-0-1	J
SCALE NONE	SHEET 10 OF 11			

D1-3 TRANSFER BUS Ø0H (CK2) 14
D1-3 TRANSFER BUS Ø1H (CK2) 13
D1-3 TRANSFER BUS Ø2H (CK1) 11
D1-3 TRANSFER BUS Ø3H (CL1) 6
D1-3 TRANSFER BUS Ø4H (CK2) 4
D1-3 TRANSFER BUS Ø5H (BN1) 3
74174 E64
D1-4 TRANSFER BUS 12 H DE1
8018 E61
D2-9 EICR Ø0H
D2-9 EICR Ø1H
D2-9 EICR Ø2H
D2-9 EICR Ø3H
D2-9 EICR Ø4H
D2-9 EICR Ø5H
D2-3 SET EICR 12 L
TRANSFER BUS 13 H DE2
D2-3 SET EICR 13 L
TRANSFER BUS 14 H DF2
D2-3 SET EICR 14 L
D1-4 TRANSFER BUS 15H DJ1
D2-3 SET EICR 15 L
D2-9 EICR 12H
D2-9 EICR 13H
D2-9 EICR 14H
D2-9 EICR 15H

D3-4 NPR STATUS REPORTING REGISTER CLK L
BPI
C112 100pf
R37 3K
+5V

D3-7 INIT D2 L DE2 13
7404 E58
D2-9 A BUFFERED INIT D2 L
D2-9 INIT H
D2-9 B BUFFERED INIT D2 L

R36 1K +5V

D3-4 MASTER SCAN Ø0H DE1
D3-4 MASTER SCAN Ø1H DP1
74174 E68
D1-3 TRANSFER BUS Ø6H (CP1) 14
D1-3 TRANSFER BUS Ø7H (CC2) 13
D1-4 TRANSFER BUS Ø8H EC1 11
D1-4 TRANSFER BUS Ø9H EB2 6
D1-4 TRANSFER BUS 10H EA2 4
D1-4 TRANSFER BUS 11H EE2 3
D2-9 EICR Ø6 H
D2-9 EICR Ø7 H
D2-9 EICR Ø8 H
D2-9 EICR Ø9 H
D2-9 EICR 10 H
D2-9 EICR 11 H
D3-4 MASTER SCAN Ø2 H DN1
D3-4 MASTER SCAN Ø3H DM1
8641 E65
D2-9 NPR STATUS Ø0H
D2-9 NPR STATUS Ø1H
D2-9 NPR STATUS Ø2H
D2-9 NPR STATUS Ø3H
D2-5 READ NPR STATUS H
D2-9 NPR STATUS 08H
D2-9 NPR STATUS 09H
D2-9 NPR STATUS 10H
D2-9 NPR STATUS 11 H

+3V
C111 100pf
R35 18K
+5V
D2-9 NPR STATUS 13 H
7474 E68 NPR STATUS
7408 E69
7408 E52
7408 E52
7408 E52
7408 E58
D2-9 NPR STATUS AVAILABLE L
DK2
D2-9 NPR FILO NOT AVAILABLE H

D2-2 ROM DATA Ø0H (DC1) 4
D2-2 ROM DATA Ø1 H (DD2) 5
D2-2 ROM DATA Ø2H (DM2) 12
D2-2 ROM DATA Ø3H (ET2) 15
74174 E56
DL1
D3-6 RAM OUT PUT DATA CLK H
D3-6 RICR CLOCK L DD1
7404 E50
8641 E57
C108 .68uf
-15V
D1 D2 D3 D4 0664
DB2
-15V

REVISIONS
ECN | CHANGE NO. | REV.

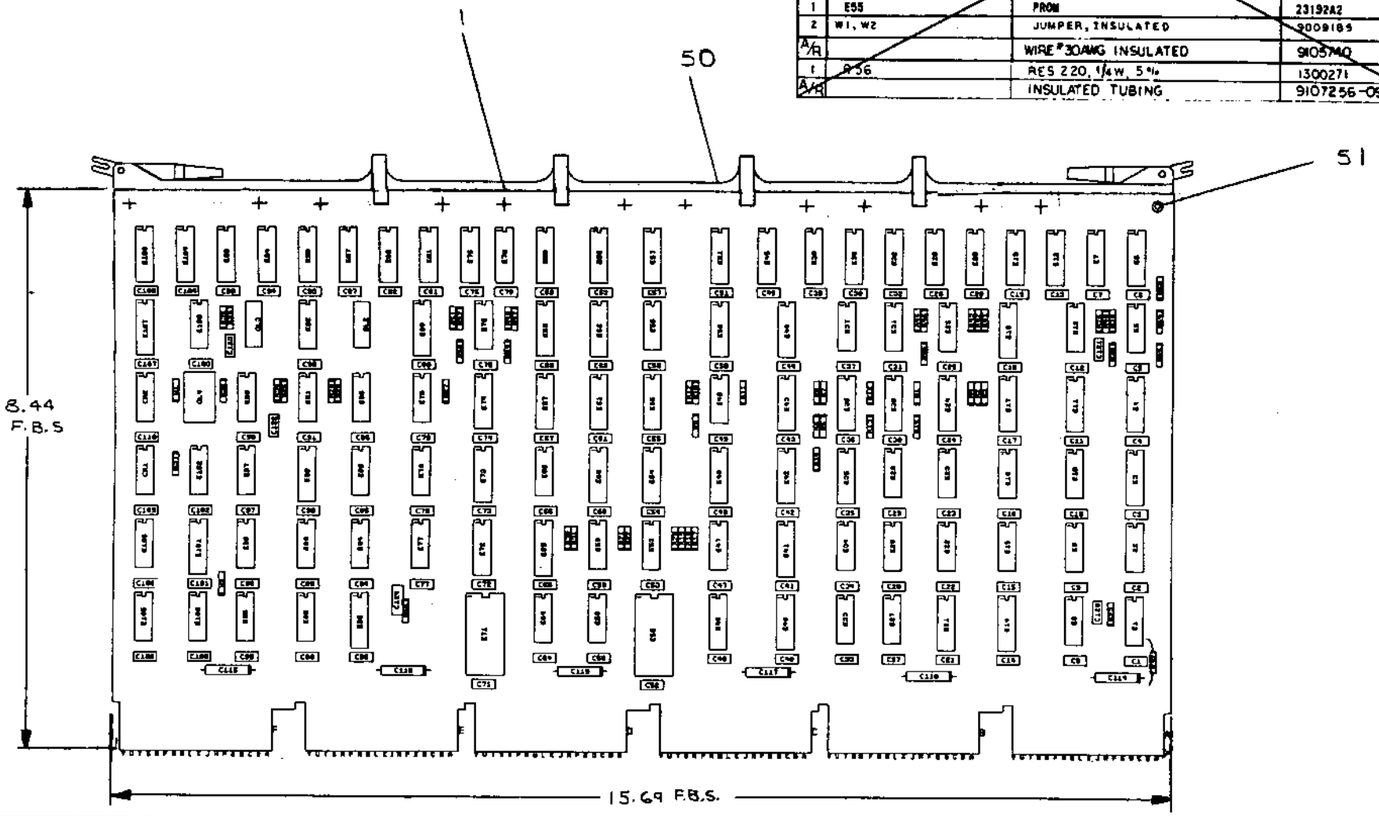
TITLE UNIBUS DATA AND NPR CONTROL (D2-9)
SIZE D | CODE DCS | NUMBER M7837-Ø-1 | REV. J
SCALE | SHEET 11 OF 11 | DIST.
MK

DCS M7837-Ø-1

NOTES:

1. FOR USE WITH ASYNCHRONOUS LINE CARDS M7833 THIS BOARD MUST BE CS REV E OR LATER.

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
1	E80	I.C. DEC 74S175	1910857	52
1		HANDLE ASSY.	12109711-2	53
12		EYELET, HANDLE	9006732	54
1	E4	PROM	23185A2	55
1	E11	PROM	23186A2	56
1	E17	PROM	23187A2	57
1	E24	PROM	23188A2	58
1	E30	PROM	23189A2	59
1	E38	PROM	23190A2	60
1	E43	PROM	23191A2	61
1	E55	PROM	23192A2	62
2	W1, W2	JUMPER, INSULATED	9009185	63
A/R		WIRE #30AWG INSULATED	9105740	64
1	R56	RES 220, 1/4W, 5%	1300271	65
A/R		INSULATED TUBING	9107256-09	66



AA2, BA2, CA2, DA2, EA2, FA2 — +5V

AC2, AT1, BC2, BT1, CC2, CT1, DC2, DT1, EC2, ET1, FC2, FT1 — GND

C114 .68UF, C115 .68UF, C116 .68UF, C117 .68UF, C118 .68UF, C119 .68UF, C1 .01UF, C1 THRU C110 .01UF

IC TYPE	GND	+5V
8640	1	8
7493	10	5
7492	10	5

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV	CHANGE NO.	DATE	APPROVED
A	M7838-00001	17-JUN-80	A. HARRINGTON
B	M7838-00002	7-JUL-80	R. HARRINGTON
C	M7838-00003	7-AUG-80	J. MCNAMARA
D	M7838-00004	7-SEP-80	J. MCNAMARA
E	M7838-00005	7-OCT-80	J. MCNAMARA
F	M7838-00006	7-NOV-80	J. MCNAMARA
G	M7838-00007	7-JAN-81	J. MCNAMARA
H	M7838-00008	7-MAR-81	R. HARRINGTON
J	M7838-00009	7-MAY-81	R. HARRINGTON
K	M7838-00010	7-JUN-81	A. HARRINGTON

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REF		DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	X-CO-M7838-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7838-0-5	2
REF		MODULE ECO HISTORY	B-MH-M7838-0-6	3
1		ETCHED CIRCUIT BOARD	5010978	4
1	C131	CAP 10PF 100V,5% DM	1000008	5
2	C120,C123	CAP 100PF 100V,5% DM	1000018	6
2	C122,C124	CAP 1000PF 100V,5%	1000842	7
110	C1-C113	CAP .01UF 100V, 20%	1001870-01	8
6	C114-C119	CAP 68UF 35V 10% TANT	1005808	9
3	R24,29,30	RES. 330 OHM, 1/4W, 5%	1300295	10
2	R25,28	RES. 470 OHM, 1/4W, 5%	1300318	11
37	R1-18,27,38-55,36,37,	RES. 1K, 1/4W, 5%	1300365	12
1	R34	RES. 3.3K, 1/4W, 5%	1300439	13
2	R23,57	RES. 4.7K, 1/4W, 5%	1300447	14
3	R19,20,22	RES. 390 OHM, 1/4W, 5%	1300309	15
1	R26	RES. 15K, 1/4W, 5%	1300496	16
3	R17,18,21	RES. 180 OHM, 1/4W, 5%	1301322	17
1	R31	RES. 750 OHM, 1/4W, 5%	1301401	18
1	R35	RES. 5.6K, 1/4W, 5%	1301874	19
2	DL2,DL3	DELAY LINE 30NS	1605928-01	20
1	DL4	DELAY LINE 100NS	1605559	21
1	CR1	20MHZ OSCILLATOR 14 PIN DIP	1811880-00	22
1	CR2	5.068 MHZ OSCILLATOR 14 PIN DIP	1811880-02	23
5	E50,15,22,23,26	I.C. DEC 7474	1905547	24
2	E47,70	I.C. DEC 7400	1905575	25
1	E2	I.C. DEC 7420	1909577	26
2	E97,102	I.C. DEC 7430	1905578	27
4	E31,37,49,58	I.C. DEC 7401	1905580	28
3	E85,91,1	I.C. DEC 7402	1909004	29
1	E105	I.C. DEC 7492	1908053	30
2	E100,106	I.C. DEC 7493	1909054	31
2	E59,96	I.C. DEC 74H00	1909056	32
1	E95	I.C. DEC 74H11	1909287	33
2	E33,53	I.C. DEC 8640	1911469	34
4	E84,88,89,16	I.C. DEC 74S74	1910544	35
5	E5,25,64,77,75	I.C. DEC 7404	1909686	36
1	E21	I.C. DEC 7442	1910046	37
1	E27	I.C. DEC 8881	1909705	38
3	E3,10,86	I.C. DEC 8815	1909713	39
5	E61,65,67,72,74	I.C. DEC 74193	1910018	40
1	E66	I.C. DEC 7437	1910091	41
2	E52,71	I.C. DEC 74150	1910153	42
3	E92,20,34	I.C. DEC 7408	1910155	43
4	E8,12,98,103	I.C. DEC 74121	1910230	44
1	E101	I.C. DEC 74161	1910650	45
10	E3,14,42,44,46,48,50,54,60,62	I.C. DEC 74175	1910651	46
1	E73	I.C. DEC 74174	1910652	47
9	E19,45,51,57,63,66,69,80,107	I.C. DEC 74157	1910655	48
4	E75,40,41,83	I.C. DEC 74155	1910656	49
19	E8,7,13,18,20,26,32,38,E39,78,76,81,82,87,93,94,E99,104,108	I.C. DEC 3100	1910818-02	50
1	E79	I.C. DEC 74H10	1909057	51
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: DV11-AA

ETCH BOARD REV: C

		DATE
DRN.	K. Davis	1-6-75
CHK.	D. Lee	1-14-75
ENG.	E. Lee	1-12-75
PROJ. ENG.	R. Lemon	1-12-75
PROD.	R. Wilk	2-12-75

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: ROM, RAM AND BRANCH

NEXT HIGHER ASSY: B-DD-DV11-Ø

SCALE: NONE

SHEET 1 OF 12

SIZE	CODE	NUMBER	REV.
D	CS	M7838-Ø-1	K

DIST.

DCSM7838-Ø-1 K

D2-3 BUF DATA Ø0 H — BM2 — 74Ø1 E37 — R16 1K
D2-3 BUF DATA Ø1 H — BP2 — 74Ø1 E37 — R15 1K
D2-3 BUF DATA Ø2 H — BU2 — 74Ø1 E37 — R14 1K
D2-3 BUF DATA Ø3 H — BN2 — 74Ø1 E37 — R13 1K
D2-3 BUF DATA Ø4 H — AK2 — 74Ø1 E31 — R4 1K
D2-3 BUF DATA Ø5 H — AJ2 — 74Ø1 E31 — R3 1K
D2-3 BUF DATA Ø6 H — AP2 — 74Ø1 E31 — R2 1K
D2-3 BUF DATA Ø7 H — AL2 — 74Ø1 E31 — R1 1K
D2-3 BUF DATA Ø8 H — FP2 — 74Ø1 E56 — R8 1K
D2-3 BUF DATA Ø9 H — CS2 — 74Ø1 E56 — R7 1K
D2-3 BUF DATA 1Ø H — EV1 — 74Ø1 E56 — R6 1K
D2-3 BUF DATA 11 H — FS2 — 74Ø1 E56 — R5 1K
D2-3 BUF DATA 12 H — EN1 — 74Ø1 E49 — R12 1K
D2-4 BUF DATA 13 H — CF2 — 74Ø1 E49 — R11 1K
D2-3 BUF DATA 14 H — CK1 — 74Ø1 E49 — R1Ø 1K
D2-3 BUF DATA 15 H — CL1 — 74Ø1 E49 — R9 1K
+5V

D2-4 SCR Ø3 L — DR2 — 7431 E66

74193 E74 (CRY, BRW, D3, D2, D1, DØ, CLR, LD, CUP, CDN; R3(1), R2(1), R1(1), RØ(1))
D3-2 ROM DATA 15 H

74193 E61
D3-2 ROM DATA Ø7 H
D3-2 ROM DATA Ø6 H
D3-2 ROM DATA Ø5 H
D3-2 ROM DATA Ø4 H

74193 E67
D3-2 ROM DATA Ø3 H
D3-2 ROM DATA Ø2 H
D3-2 ROM DATA Ø1 H
D3-2 ROM DATA ØØ H

74ØØ1 E77 — D3-7 INIT D3 L
D3-7 Ø1 H
+3V

D3-2 BRANCH POINT TRUE H
D3-7 Ø2 H
74HØØ E59

23-190 A2 MEI E36 (ME1, ME2, D, E, F, G, H; Y4, Y3, Y2, Y1; A, B, C)
23-189 A2 MEI E30
23-131 A2 MEI E43
23-192 A2 MEI E55

23-187 A2 MEI E17
D3-1 ROM Ø3 L
D3-1 ROM Ø2 L
D3-1 ROM Ø1 L
D3-1 ROM ØØ L

23-188 A2 MEI E24
D3-1 ROM Ø7 L
D3-1 ROM Ø6 L
D3-1 ROM Ø5 L
D3-1 ROM Ø4 L

23-186 A2 MEI E11
D3-1 ROM 11 L
D3-1 ROM 1Ø L
D3-1 ROM Ø9 L
D3-1 ROM Ø8 L

23-139 A2 MEI E4
D3-1 ROM 15 L
D3-1 ROM 14 L
D3-1 ROM 13 L
D3-1 ROM 12 L

74HØØ E39

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-1)	D	CS	M7838-Ø-1	K
SCALE —	SHEET 2 OF 12	DIST.	MK	

DCS M7838-0-1 K

NOTE PIN DV2 IS ASSIGNED PIN "I-2 ALU-8" BUT IS NOT USED ON THIS BOARD

D2-4 SCR Ø2 H EU1

74S08 E92 FB2 D3-2 TRANSFER SOURCE ENAB L

TRAN FLAG WAITING L CP2 R17 180Ω R18 390Ω 8640 E55

DB1 D3-2 BRANCH B L

74S08 E59

74S74 E68 D3-7 T SØ H D3-2 BRANCH POINT TRUE H

74S74 E58 FB3 D3-2 DATA TRANSFER L; FB2 D3-2 RAM OPERATION L; FB1 D3-2 ALU OPERATION L; FB0 EP2; 74155 E65 FB3 FA2 BU2 D3-2 BCC CALCULATION L; FA1 D3-2 SET/CLEAR OPERATION L; FA0 E72 D3-2 MPR OPERATION L; DB DA S1 SØ

MATCH DETECT L CR1 R20 390Ω R19 180Ω 8640 E55 +5V

DATA NOT AVAILABLE L CT2 R22 390Ω R21 180Ω 8640 E53 +5V

D2-6 WRITE INHIBIT H

D3-11 RAM OUTPUT Ø-14=Ø H

D3-11 RAM OUTPUT 15 H CM1

DI-9 MEM PRE ERR H CS1

D2-7 REQUEST BUS H

D3-11 RAM OUTPUT ØI H; D3-11 RAM OUTPUT Ø6 H; D3-11 RAM OUTPUT Ø5 H; D3-11 RAM OUTPUT Ø4 H; D3-11 RAM OUTPUT Ø3 H; D3-11 RAM OUTPUT Ø2 H; D3-11 RAM OUTPUT ØI H; D3-11 RAM OUTPUT ØØ H

ST8 74150 E52 DI5 DI4 DI3 DI2 DI1 DIØ DØ9 DØ8 DØ7 DØ6 DØ5 DØ4 DØ3 DØ2 DØ1 DØØ; S3 S2 S1 SØ

DI-5 READY IN L DL1; DI-1 ALU RESULT Ø4 H DS1; DI-1 ALU RESULT Ø3 H DS2; DI-1 ALU RESULT Ø2 H DT2; DI-1 ALU RESULT ØI H DV1; DI-1 ALU RESULT ØØ H DV2; DI-2 ALU 13-12 H EC1; D2-9 MPR SILO NOT AVAILABLE H EJ1; D2-7 NXM H EJ2; D2-6 SCR Ø3 H EK1; DI-5 RECEIVER FLAG WAITING EK2; DI-5 RECEIVED CHARACTER WAITING H EN2; +3V; DI-2 ALU RESULT 15 H EH1

ST8 74150 E71 DI5 DI4 DI3 DI2 DI1 DIØ DØ9 DØ8 DØ7 DØ6 DØ5 DØ4 DØ3 DØ2 DØ1 DØØ; S3 S2 S1 SØ

EH2 D3-2 BRANCH A L

74175 E64 D3-1 ROM 15 L D3 R3(1) R3(Ø); D3-1 ROM 14 L D2 R2(1) R2(Ø); D3-1 ROM 13 L D1 R1(1) R1(Ø); D3-1 ROM 12 L DØ RØ(1) RØ(Ø); CLR CLK; D3-7 INIT D3 L

EE2 D3-2 ROM DATA 15 H; ES1 D3-2 ROM DATA 14 H; ES2 D3-2 ROM DATA 13 H; EE2 D3-2 ROM DATA 12 H

74175 E54 D3-1 ROM 11 L D3 R3(1) R3(Ø); D3-1 ROM 10 L D2 R2(1) R2(Ø); D3-1 ROM Ø9 L D1 R1(1) R1(Ø); D3-1 ROM Ø8 L DØ RØ(1) RØ(Ø); CLR CLK

DB2 D3-2 ROM DATA 11 H; CU2 D3-2 ROM DATA 10 H; EA1 D3-2 ROM DATA Ø9 H; D3-2 ROM DATA Ø8 L; ED1 D3-2 ROM DATA Ø8 H

74175 E48 D3-1 ROM Ø7 L D3 R3(1) R3(Ø); D3-1 ROM Ø6 L D2 R2(1) R2(Ø); D3-1 ROM Ø5 L D1 R1(1) R1(Ø); D3-1 ROM Ø4 L DØ RØ(1) RØ(Ø); CLR CLK

CH2 D3-2 ROM DATA Ø7 H; CE1 D3-2 ROM DATA Ø6 H; CE1 D3-2 ROM DATA Ø5 H; CE2 D3-2 ROM DATA Ø4 H

74175 E42 D3-1 ROM Ø3 L D3 R3(1) R3(Ø); D3-1 ROM Ø2 L D2 R2(1) R2(Ø); D3-1 ROM ØI L D1 R1(1) R1(Ø); D3-1 ROM ØØ L DØ RØ(1) RØ(Ø); CLR CLK

BL1 D3-2 ROM DATA Ø3 H; D3-2 ROM DATA Ø2 L; BD1 D3-2 ROM DATA Ø2 H; D3-2 ROM DATA ØI L; E01 D3-2 ROM DATA ØI H; D3-2 ROM DATA ØØ L; BC1 D3-2 ROM DATA ØØ H

D3-7 Ø3 L; DH1; 74H08 E59; D2-5 LOAD SFR L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-2)	D	CS	M7838-Ø-1	K
SCALE	SHEET 3 OF 12	DIST.		

MK

D3-2 ROM DATA Ø5 H — 7400 E47 pin 1
D3-2 ROM DATA Ø4 H — 7400 E47 pin 5
D3-2 ROM DATA Ø7 H — 7400 E47 pin 9
D3-2 ROM DATA Ø3 H — 7400 E47 pin 13
D3-2 ROM DATA Ø6 H — 7400 E78 pin 13
D3-7 DATA STROBE L — 7402 E85 pin 3
D3-2 SET/CLEAR OPERATION L — 7402 E85 pin 2

7400 E47 pin 3 — 7415[4] E41 STBA
7400 E47 pin 6 — CNI — D3-3 SET/CLEAR ØØ L
7400 E47 pin 8 — 7415[4] E35 STBA
7400 E47 pin 11 — CDI — D3-3 SET/CLEAR Ø3 L
7400 E78 pin 11 — 7415[4] E40 STBA

D3-3 ROM DATA ØØ L — 7415[4] E41 DB
D3-2 ROM DATA Ø1 L — 7415[4] E41 S1
D3-2 ROM DATA Ø2 L — 7415[4] E41 SØ

7415[4] E41 DA
- FBØ — D3-3 SET RAM OUTPUT ØØ L
- FB1 — D3-3 CLEAR RAM OUTPUT ØØ L
- FB2 — D3-3 SET RAM OUTPUT Ø1 L
- FB3 — D3-3 CLEAR RAM OUTPUT Ø1 L
- FAØ — D3-3 SET RAM OUTPUT Ø2 L
- FA1 — D3-3 CLEAR RAM OUTPUT Ø2 L
- FA2 — D3-3 SET RAM OUTPUT Ø3 L
- FA3 — D3-3 CLEAR RAM OUTPUT Ø3 L

7415[4] E35 DB
- FBØ — D3-3 SET RAM OUTPUT Ø4 L
- FB1 — D3-3 CLEAR RAM OUTPUT Ø4 L
- FB2 — D3-3 SET RAM OUTPUT Ø5 L
- FB3 — D3-3 CLEAR RAM OUTPUT Ø5 L

7415[4] E35 DA
- FAØ — D3-3 SET RAM OUTPUT Ø6 L
- FA1 — D3-3 CLEAR RAM OUTPUT Ø6 L
- FA2 — D3-3 SET RAM OUTPUT Ø7 L
- FA3 — D3-3 CLEAR RAM OUTPUT Ø7 L

7415[5] E40 DB
- FBØ — D3-3 SET TRAN DATA Ø3 L
- FB1 — D3-3 CLEAR TRAN DATA Ø3 L
- FB2 — CD2 — D3-3 SET T MARK L
- FB3 — CA1 — D3-3 CLEAR T MARK L

7415[5] E40 DA
- FAØ — CE2 — D3-3 RESYNC PULSE L
- FA1 — DP2 — D3-3 ADVANCE MASTER SCANNER L
- FA2
- FA3

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-3)	D	CS	M7838-Ø-1	K
SCALE — SHEET 4 OF 12	DIST.	MK		

D3-3 TRANSFER BUS Ø0 H — CJ2 13 — 74175 E46 D3 R3 — 15 CH1 — D3-Ø TRAN DATA Ø0 H
D3-3 TRANSFER BUS Ø1 H — CK2 12 — D2 R2 — 10 CJ1 — D3-Ø TRAN DATA Ø1 H
D3-3 TRANSFER BUS Ø2 H — CMR 5 — D1 R1 — 7 CL2 — D3-Ø TRAN DATA Ø2 H
D3-3 TRANSFER BUS Ø3 H — CMA 4 — D0 R0 — 2 CN2 — D3-Ø TRAN DATA Ø3 H
CLR CLK — 1 — 9

D3-7 INIT D3 L

D3-6 TRANSMITTED DATA BUS CLOCK L — 7404 E64 (1, 2)

D3-3 SET TRAN DATA Ø8 L — 7474 E58 (4, 5, 2, 1, 3, 6) — DFZ — D3-Ø TRAN DATA Ø8 H
D3-5 INIT H
D3-3 CLEAR TRAN DATA Ø8 L

D3-3 TRANSFER BUS Ø4 H — AN4 13 — 74175 E14 D3 R3 — 15 AT2 — D3-Ø TRAN DATA Ø4 H
D3-3 TRANSFER BUS Ø5 H — AR1 12 — D2 R2 — 10 AS1 — D3-Ø TRAN DATA Ø5 H
D3-3 TRANSFER BUS Ø6 H — AU2 5 — D1 R1 — 7 AN2 — D3-Ø TRAN DATA Ø6 H
D3-3 TRANSFER BUS Ø7 H — AN 4 — D0 R0 — 2 AS2 — D3-Ø TRAN DATA Ø7 H
CLR CLK — 1 — 9

+3V — 10 — C120 100PF — E23 4.7K — +5V

3 4 5 — 74121 E6 — 11 9 6 1 — AM2 — D3-Ø TRANSMITTER STROBE H
6 7

74Ø4 E64 (5, 6) — DP1 — D3-Ø MASTER SCAN C H

74193 E72 — 12 13 CRY BRW — 9 D3 10 D2 1 D1 15 D0 — CLR LD CUP CDN — 14 11 5 4 — +3V
P3 7 NC; P2 6 NC; P1 2 NC; P0 3 DN1 — D3-Ø MASTER SCAN Ø3 H
74Ø4 E64 (3, 4) — DN2 — D3-Ø MASTER SCAN D H

74193 E65 — 12 13 CRY BRW — 9 D3 10 D2 1 D1 15 D0 — CLR LD CUP CDN — 14 11 5 4 — +3V
R3 7 DM2 — D3-Ø MASTER SCAN Ø2 H
R2 6 DL2 — D3-Ø MASTER SCAN Ø1 H
R1 2 FT2 — D3-Ø MASTER SCAN Ø0 H
R0 3 FU2 — D3-Ø MASTER SCAN T/R

D3-5 INIT H
D3-3 ADVANCE MASTER SCANNER L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-4)	D	CS	M7838-Ø-1	K
SCALE	SHEET 5 OF 12	DIST.		

DCSM7838-Ø-1 K

+5 V — W2 — (W2 REMOVED FOR AUTOMATED MODULE TEST) — D3-5 2Ø MHZ

7492 E1Ø5: R3(1) 8 FS1 D3-5 96ØØ BAUD; R2(1) 9 FR1 D3-5 192Ø0 BAUD; R1(1) 11 N/C; R0(1) 12 FL1 D3-5 48ØØ BAUD; CLKBC CLKB6

7493 E1ØØ: R3(1) 11 FR1 D3-5 6ØØ BAUD; R2(1) 8 FR2 D3-5 12ØØ BAUD; R1(1) 9 FR3 D3-5 24ØØ BAUD; R0(1) 12 N/C; CLR; CLKBC CLKB6; N/C

7404 E6Ø — D3-5 INIT H

7493 E1Ø6: R3(1) 11; R2(1) 8; R1(1) 9; R0(1) 12 FL2 D3-5 23Ø.4K8 H; CLR; CLKBC CLKB6

D3-7 INIT D3 L

+5V — W1 — (W1 REMOVED FOR AUTOMATED MODULE TEST)

74161 E1Ø1: MSB; LSB; CLR; LD; CLK; CNT EN; CRY EN C.O. 15; +3V

74H6Ø E9G

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-5)	D	CS	M7838-Ø-1	K
SCALE — SHEET 6 OF 12	DIST.			

MK

D3-6 WRITE INHIBIT H
D3-3 INIT H
7474 E58
D3-6 RAM OUTPUT DATA CLOCK L
7404 EG4
D3-6 RAM OUTPUT DATA CLOCK H
DH2
D2-5 UNIBUS RAM WRITE '
AH2
7412 E12
R26 1.5
C121 10 PF
+5V
R24 330
DL3
30 NS
R25 470
8815 E86
7402 E91
DL2
R29 330
R28 470
7408 E92
D3-6 RAM WRITE ENABLE B L
D3-6 RAM WRITE ENABLE A L
R30 330
R31 750
3106 E108
D3-8 RAM ADD Φ1 H
D3-8 RAM ADD Φ0 H
D3-8 RAM ADD Φ2 H
D3-8 RAM ADD Φ7 H
D3-8 RAM ADD Φ3 H
D3-8 RAM ADD Φ4 H
D3-8 RAM ADD Φ5 H
D3-8 RAM ADD Φ6 H
CS1
CS2
CS3
A0
A1
A2
A3
A4
A5
A6
A7
D OUT
WE DIN
D3-2 ROM DATA Φ8 L
D3-7 T5Φ L
R27 2K
D3-2 RAM OPERATION L
D3-7 Φ2 L
D3-2 ROM DATA Φ8 H
D3-7 INSTRUCTION DECODER ENABLE B L
D3-2 DATA TRANSFER L
7474 E21
D3-2 ROM DATA Φ2 H
D3-2 ROM DATA Φ1 H
D3-2 ROM DATA Φ0 H
D3
D2
D1
D0
D3-6 NPR STATUS REPORTING REGISTER CLOCK L
D3-6 RICR CLOCK L
D3-6 NPR DATO REGISTER CLOCK L
D3-6 RAR Ø-3 CLOCK L
D3-6 NPR ADDRESS REGISTER CLOCK L
D3-6 B REGISTER CLOCK L
D3-6 A REGISTER CLOCK L
D3-6 TRANSMITTED DATA BUS CLOCK L

REVISIONS
CHK | CHANGE NO. | REV.

TITLE: ROM, RAM & BRANCH (D3-6)
SIZE D | CODE CS | NUMBER M7838-Ø-1 | REV. K
SCALE: | SHEET 7 OF 12 | DIST.

D2-6 SCR 11 H EL1 — 7406 E78 — C122 1000 PF — R34 3.3K — +3V — 74121 E98 — 2.4 USEC

D2-6 ASSERT MSYN H — BP2 — 8881 E27 — 8W D3-7 BUS MSYN L — 8640 E33

D2-8 A17 H FE1 — D1-8 ADDRESS SELECTED H FE2 — 7430 E102 — 7430 E97 — D3-7 INSTRUCTION DECODER ENABLE B L

D2-6 LOAD LCR H FB1 — +5V R35 5.6K — 74121 E103 — C123 100 PF

BUS INIT L AN1 — 8640 E33 — 7402 E85 — 7404 E77 — +3V — 7437 E66 — EB2 D3-7 INIT D1 L

+3V — 7400 E78 — AV1 D3-7 INIT D2 L

7437 E66 — D3-7 INIT D3 L

DL4 100NS — R36 1K — R37 1K — +3V

7404 E77 — D3-7 BUS INIT L

7404 E77 — R56 220 — C124 1000PF — 8881 E27 — BV1 D3-7 BUS SSYN L

FB1 D3-7 INSTRUCTION DECODER ENABLE A L

SCR Ø1 H FF2 — 74H80 E96 — 74H00 E96 — SCR ØØ H FA1

7911 E93 — 7911 E95 — 74S74 E88 UNIBUS GO — 74S74 E84 MICRO CODE GO — ER1 D3-7 Ø1 L — D3-7 Ø1 H

74S74 E91 PHASE — D3-5 20 MHZ

7402 E55 — 13

74S175 E90 — D3 R3(0) — FC1 D3-7 DATA STROBE L

D2 R2(1) — R2(0)

D1 R1(1) — R1(0) — FD2 D3-7 Ø2 L — D3-7 Ø2 H

D0 R0(1) — R0(0) — D3-7 T SW H — D3-7 T SW L — CLR CLK

+3V — 74S74 E89 — D3-7 Ø3 H — D3-7 Ø3 L

74S74 E89 — 7250 — 13

RS7 4.7K — +5V — C1 H AN1 — 7402 E1 — CØ H BM1 — 7402 E1 — 74S38 DATIP E16

74S38 E8 MICRO WRITE CONTROL STORE CHIP

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ROM, RAM & BRANCH (D3-7)			
SIZE	CODE	NUMBER	REV.	
D	CS	M7838-Ø-1	K	
SCALE	SHEET 8 OF 12	DIST.		

MK

D3-7 INSTRUCTION DECODER ENABLE Ø L

INSTRUCTION DECODER ENABLE A L

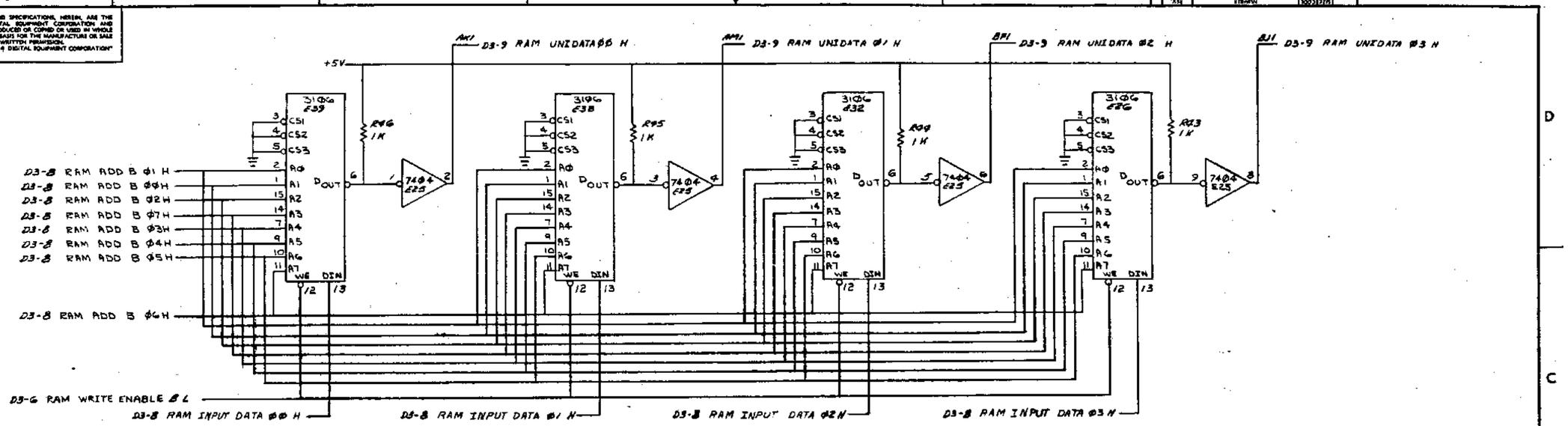
D2-5 LOAD SRS LOW BYTE H

D2-5 LOAD SRS HIGH BYTE H

D3-6 RAR Ø-3 CLOCK L

REVISIONS		
CHK	CHANGE NO.	REV.

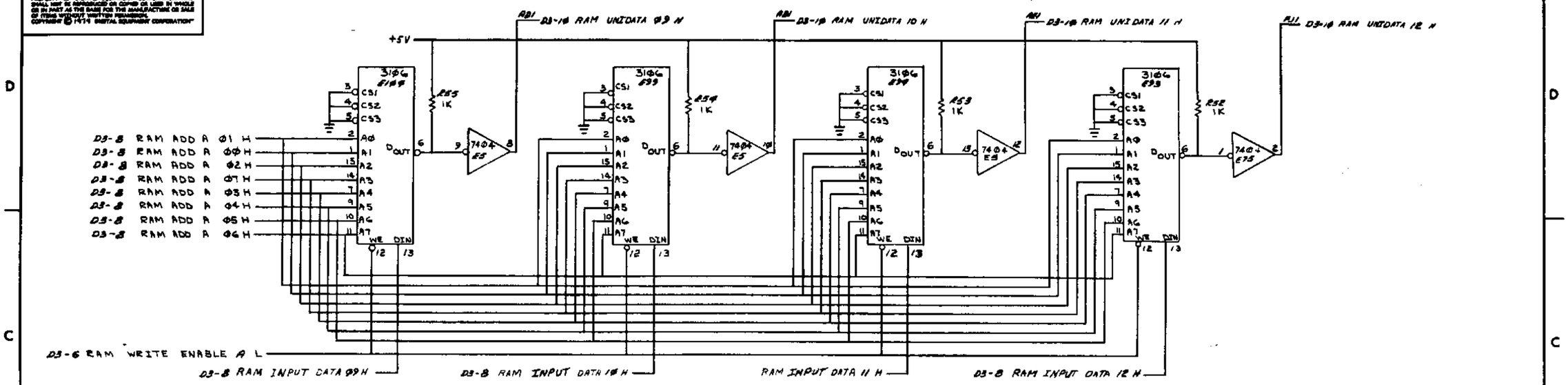
TITLE: ROM, RAM & BRANCH (D3-8)
SIZE: D CODE: CS NUMBER: M7838-Ø-1 REV: K
SCALE: SHEET 9 OF 12 DIST.



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-9)	D	CS	M7838-Ø-1	K
SCALE	SHEET 10 OF 12	DIST.		

MK



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-1Ø)	D	CS	M7838-Ø-1	K
SCALE —	SHEET 11 OF 12	DIST.		

MK

D3-3 SET RAM OUTPUT Ø6 L
D3-9 RAM UNIDATA Ø6 H
D3-6 RAM OUTPUT DATA CLOCK L
D3-3 CLEAR RAM OUTPUT Ø6 L
7437 E66
7408 E29
7474 E23
DA1
D3-11 RAM OUTPUT Ø6 H

D3-3 SET RAM OUTPUT Ø5 L
D3-9 RAM UNIDATA Ø5 H
D3-3 CLEAR RAM OUTPUT Ø5 L
7408 E29
7474 E23
DC1
D3-11 RAM OUTPUT Ø5 H

D3-3 SET RAM OUTPUT Ø4 L
D3-9 RAM UNIDATA Ø4 H
D3-3 CLEAR RAM OUTPUT Ø4 L
7408 E29
7474 E28
CU1
D3-11 RAM OUTPUT Ø4 H

D3-3 SET RAM OUTPUT Ø3 L
D3-9 RAM UNIDATA Ø3 H
D3-3 CLEAR RAM OUTPUT Ø3 L
7408 E29
7474 E28
CV2
D3-11 RAM OUTPUT Ø3 H
BK2
D3-11 RAM OUTPUT Ø3 L

D3-3 SET RAM OUTPUT Ø2 L
D3-9 RAM UNIDATA Ø2 H
D3-3 CLEAR RAM OUTPUT Ø2 L
7408 E34
7474 E22
CV1
D3-11 RAM OUTPUT Ø2 H

D3-3 SET RAM OUTPUT Ø1 L
D3-9 RAM UNIDATA Ø1 H
D3-3 CLEAR RAM OUTPUT Ø1 L
7408 E34
7474 E22
BA1
D3-11 RAM OUTPUT Ø1 H

D3-3 SET RAM OUTPUT Ø0 L
D3-9 RAM UNIDATA Ø0 H
D3-3 CLEAR RAM OUTPUT Ø0 L
7408 E34
7474 E15
AH2
D3-11 RAM OUTPUT Ø0 H

74174 E73
D3-10 RAM UNIDATA 12 H
D3-10 RAM UNIDATA 13 H
D3-10 RAM UNIDATA 14 H
D3-10 RAM UNIDATA 15 H
D3-10 RAM UNIDATA 16 H
D3-10 RAM UNIDATA 17 H
D3-7 INIT D3 L
EE1 D3-11 RAM OUTPUT 12 H
DR1 D3-11 RAM OUTPUT 13 H
ED2 D3-11 RAM OUTPUT 14 H
EB1 D3-11 RAM OUTPUT 15 H
EF2 D3-11 RAM OUTPUT 16 H
EF1 D3-11 RAM OUTPUT 17 H

8815 E10
D3-3 CLEAR RAM OUTPUT Ø5 L

8815 E10
74175 E3
D3-9 RAM UNIDATA Ø8 H
D3-10 RAM UNIDATA Ø9 H
D3-10 RAM UNIDATA 10 H
D3-10 RAM UNIDATA 11 H
D3-7 INIT D3 L
AE2 D3-11 RAM OUTPUT Ø8 H
AR2 D3-11 RAM OUTPUT Ø9 H
AD2 D3-11 RAM OUTPUT 10 H
AC1 D3-11 RAM OUTPUT 11 H

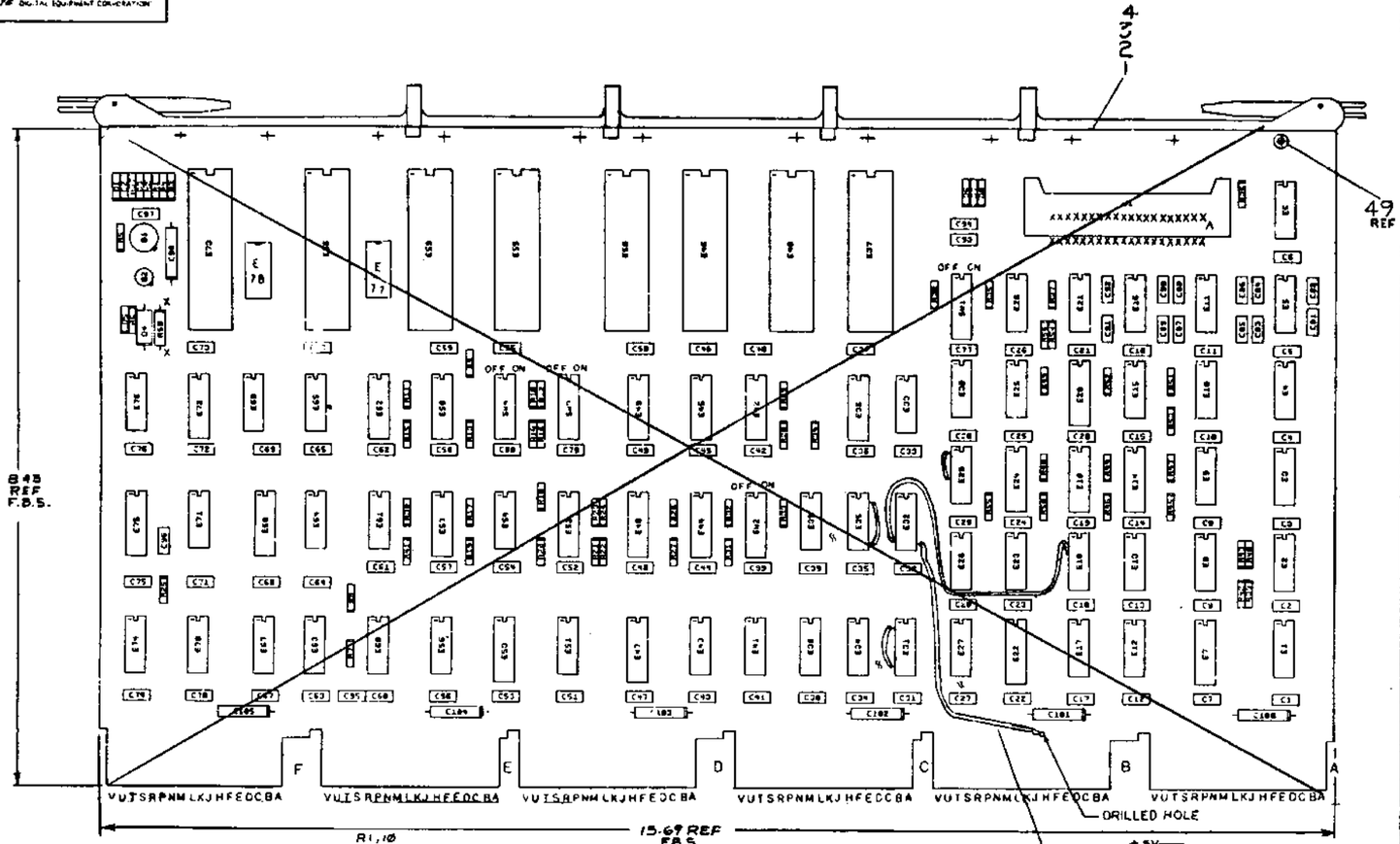
D3-3 SET RAM OUTPUT Ø7 L
D3-9 RAM UNIDATA Ø7 H
D3-3 CLEAR RAM OUTPUT Ø7 L
7474 E15
7408 E34
AL2 D3-11 RAM OUTPUT Ø7 H

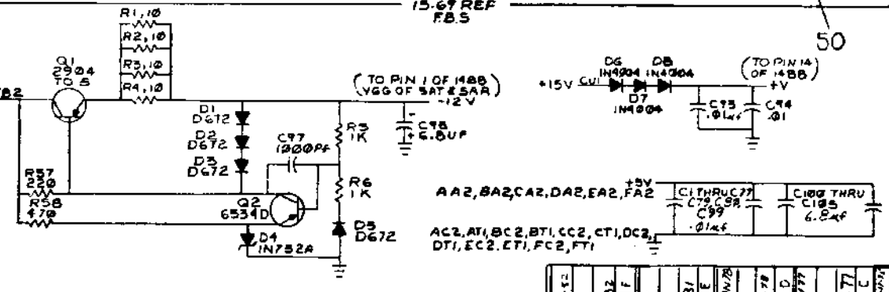
8815 E9
7428 E2
7404 E17
D3-7 BUF INIT L
D3-11 RAM OUTPUT Ø-14*Ø
D3-3 CLEAR RAM OUTPUT Ø6 L
7408 E34
8815 E9

REVISIONS
CHK | CHANGE NO. | REV.

TITLE: ROM, RAM & BRANCH (D3-11)
SIZE: D | CODE: | NUMBER: DCSM7838-Ø-1 | REV: K
SCALE: —/— | SHEET 12 OF 12 | DIST.
MK

NOTES:





CAUTION:
OFF SHEET PARTS LIST
SEE K-PL-M7839-0-0

DEC 74157	8	16	
DEC 74123	8	16	
DEC 74155	8	16	
DEC 74153	8	16	
DEC 74175	8	16	
PR14728 SAR	60	1	— 16
PT 14828 SAT	81	1	— 16
DEC 1488	7	—	14 1
IC TYPE	GND	+5V	+V -12

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV				
REF		X-Y COORDINATE HOLE LOCATION	X-CO-M7839-0-4	1
REF		ASST/HOLE DRILLING LAYOUT	D-AH-M7839-0-5	2
REF		MODULE ECO HISTORY	D-MH-M7839-0-6	3
1		ETCHED CIRCUIT BOARD	5010988	4
1	C98	CAP 68 PF, 100V, 5%	1000014	5
12	C81-92	CAP 470 PF, 100V, 5%	1000024	6
1	C87	CAP 1000PF, 100V, 5%	1000042	7
83	C93,94,96,C177,89,78,80	CAP .01 UF, 100V DISC	1001610-01	8
7	C88,100-C105	CAP 6.8 UF, 35V, 10%	1000306	9
1	D4	DIODE 1N752A	1102000	10
4	D1,2,3,5	DIODE D672	1105275	11
3	D6,7,8	DIODE 1N4004	1105788	12
1	J1	CONN, 40 PIN	1208961	13
4	SW1,SW2,SW3,SW4	DIPSWITCH 8-POS	1211184-04	14
4		DIPSWITCH COVER 8-POS	1211284-04	15
1	R57	RES. 220,1/4W, 5%	1300271	16
1	R7	RES. 330, 1/4W, 5%	1300345	17
1	R58	RES. 470, 1/2W, 5%	1300315	18
11	R5,8,30,38-44,26,27	RES. 1K, 1/4W, 5%	1300369	19
35	R9 THRU 25,28,29,36 THRU 34,45 THRU 56	RES. 10K,1/4W, 5%	1300478	20
4	R1 THRU R4	RES. 10, 1/4W, 5%	1301317	21
1	R6	RES. 750, 1/4W, 5%	1301401	22
4	R35 THRU 38	RES. 7.5K, 1/4W, 5%	1301422	23
1	Q1	TRANSISTOR 2904	1501742	24
1	Q2	TRANSISTOR 6534D	1503408	25
4	E21,33,17,23	DEC I.C. 7400	1905575	26
3	E64,8,9	DEC I.C. 7450	1905588	27
3	E1,12,3	DEC I.C. 7402	1909804	28
3	E39,25,34	DEC I.C. 74H11	1909767	29
10	E69,65,43,32,28,51,50,60,27,38	DEC I.C. 7474	1905547	30
3	E41,54,10	DEC I.C. 7404	1909688	31
4	E70,71,74,67	DEC I.C. 8881	1909705	32
1	E2	DEC I.C. 8242	1909712	33
3	E61,78,30	DEC I.C. 7417	1909929	34
2	E52,58	DEC I.C. 74157	1910655	35
9	E48,E36,44,40,42,82,45,49,22	DEC I.C. 74153	1909837	36
1	E83	DEC I.C. 7437	1910081	37
5	E18,35,29,31,19	DEC I.C. 7408	1910155	38
2	E20,0	DEC I.C. 1488	1910322	39
3	E5,16,11	DEC I.C. 1489	1910323	40
5	E14,19,20,24,75	DEC I.C. 74123	1910436	41
1	E7	DEC I.C. 74175	1910651	42
4	E47,57,53,72	DEC I.C. 74155	1910656	43
2	E15,1	DEC I.C. 7432	1911521	44
4	E59,37,46,66	DEC I.C. PR14728 SAR	2111556	45
4	E66,73,59,55	DEC I.C. PT14828 SAT	2111557-01	46
1		TRAN COVER	9008351-0	47
1		HANDLE ASSY	1210711-2	48
12		EYELET	9008732	49
A/R		WIRE 30 AWG GREEN	9105740-55	50

QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO

PARTS LIST

FIRST USED ON OPTION MODEL: DV11

ETCH BOARD REV: B

DEC NO.	EIA NO.
D672	1N3653
6534D	NONE
2904	2N1132

DEC NO. / EIA NO.

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO.	ORIGINATED
A	M7839-00001	6-12-78 R. HARRINGTON
B	M7839-00002	17-DEC-78 R. HARRINGTON
C	M7839-MK0023	27JUL81 J. MCNAMARA
D	M7839-MK0064	6-12-81 R. HARRINGTON
E	M7839-MK0085	27JUL81 J. MCNAMARA
F	M7839-MK0085	30-JUN-82 F. BACKES

CHK

DRN [illegible] DATE 1/10/78
CHKD [illegible] DATE 1/10/78
ENG [illegible] DATE 3/19/79
PROJ ENG [illegible] DATE 3/14/78
PROD [illegible] DATE 3/14/78

NEXT HIGHER ASSY: B-DD-DV11-0-0

SCALE: NONE
SHEET 1 OF 9

digital EQUIPMENT CORPORATION

TITLE: SYNC MUX LINE CARD

SIZE D | CODE DCS | NUMBER M7839-0-1 | REV F

DIST

DCS M7839-0-1

MK

BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR Ø0
C	GROUND
D	DCE SCR Ø1
E	GROUND
F	DCE SCR Ø2
H	GROUND
J	DCE SCR Ø3
K	GROUND
L	EIA RCV DATA Ø0
M	GROUND
N	EIA RCV DATA Ø1
P	GROUND
R	EIA XMIT DATA Ø0
S	GROUND
T	EIA XMIT DATA Ø1
U	GROUND
V	DTE SCTE Ø0
W	GROUND
X	DTE SCTE Ø1
Y	DTE SCTE Ø2
Z	GROUND
A A	DTE SCTE Ø3
B B	GROUND
C C	EIA XMIT DATA Ø2
D D	GROUND
E E	EIA XMIT DATA Ø3
F F	GROUND
H H	EIA RCV DATA Ø2
J J	GROUND
K K	EIA RCV DATA Ø3
L L	GROUND
M M	DCE SCT Ø3
N N	GROUND
P P	DCE SCT Ø2
R R	GROUND
S S	DCE SCT Ø1
T T	GROUND
U U	DCE SCT Ø0
V V	GROUND

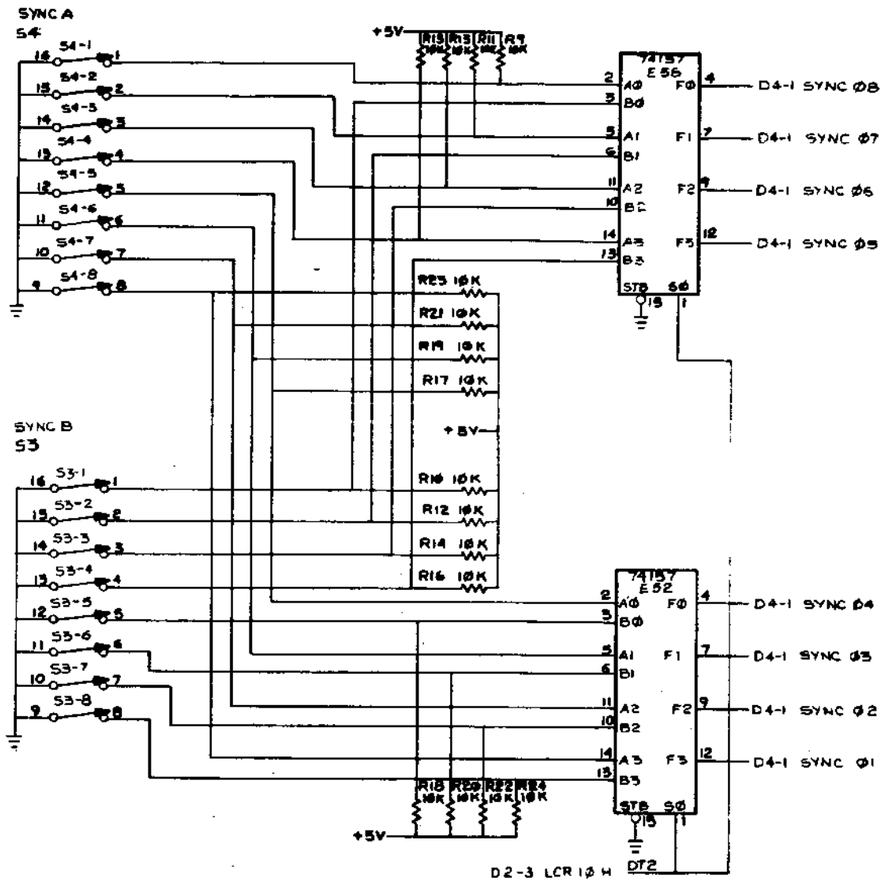
PARAMETER SWITCH SETTINGS

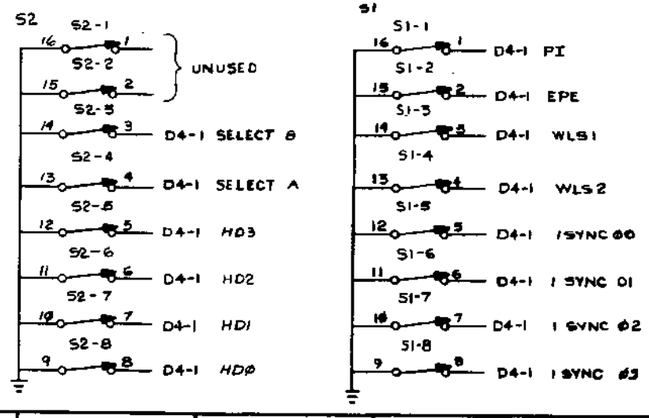
FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HD3	S2	5	ON		OFF	
	HD2	S2	6	ON		OFF	
	HD1	S2	7	ON		OFF	
	HDØ	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	ON	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC ØØ	S1	5	OFF		ON	
	1 SYNC Ø1	S1	6	OFF		ON	
	1 SYNC Ø2	S1	7	OFF		ON	
	1 SYNC Ø3	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1-8	OFF		ON	
LCR10=1	SYNC B	S3	1-8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1	GROUND
	CS2	GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1	GROUND
	MS2	NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1	NO CONNECTION
	RMS2	NO CONNECTION
	RMS3	NO CONNECTION

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN BR1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA ØR H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.





(CHARTS, SWITCHES AND SYNC SELECTOR)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	NUMBER	REV.
SYNC MUX LINE CARD (D4-1)	D	CS M7839-Ø-1	F
SCALE	SHEET 2 OF 3	DRW. MK	

DCS M7839-Ø-1 F

D4-2 CARD PARAMETER SELECT ØØ-Ø3 L DM2

D3-8 SRS Ø3 L DS2
D3-8 SRS Ø2 L DR2
D2-3 CONTROL STROBE H CS2
D4-2 BUF CONTROL STROBE L
D3-7 INIT DI L EN2
D4-2 RESET H
D4-2 RESET A L
D4-2 RESET B L
+3V
D4-2 STROBE Ø3 L
D4-2 STROBE Ø3 H
D4-2 STROBE Ø2 L
D4-2 STROBE Ø2 H
D4-2 STROBE Ø1 L
D4-2 STROBE Ø1 H
D4-2 STROBE ØØ L
D4-2 STROBE ØØ H
D3-8 SES Ø1 H BT2
D3-8 SES ØØ H BM2
D4-5 RCV IN Ø3 H
D4-5 RCV IN Ø2 H
D4-4 RCV IN Ø1 H
D4-4 RCV IN ØØ H
BIT WINDOW L PR1
D4-3 INTR MAINTENANCE ØØ-Ø3 H PE2

D3-4 TRAN DATA (P.I.) ERI (SEE NOTE 3 ON SHEET 2 OF 9)
D3-4 TRAN DATA Ø7 H EP1 — D4-2 TR8 H
D3-4 TRAN DATA Ø6 H EM2 — D4-2 TR7 H
D3-4 TRAN DATA Ø5 H FR2 — D4-2 TR6 H
D3-4 TRAN DATA Ø4 H FV2 — D4-2 TR5 H
D3-4 TRAN DATA Ø3 H FS2 — D4-2 TR4 H
D3-4 TRAN DATA Ø2 H FV1 — D4-2 TR3 H
D3-4 TRAN DATA Ø1 H FT2 — D4-2 TR2 H
D3-4 TRAN DATA ØØ H FU2 — D4-2 TR1 H

D4-2 CARD FLAG SELECT ØØ-Ø3 L DM2
D3-4 MASTER SCAN D H EU2
D3-4 MASTER SCAN C H EN2
D3-3 RESYNC PULSE L DF2
D4-2 RESYNC PULSE Ø3 L
D4-2 RESYNC PULSE Ø2 L
D4-2 RESYNC PULSE Ø1 L
D4-2 RESYNC PULSE ØØ L
D3-3 SET TMARK L CU2
D4-2 SET TMARK Ø3 L
D4-2 SET TMARK Ø2 L
D4-2 SET TMARK Ø1 L
D4-2 SET TMARK ØØ L
D1-5 RECEIVED DATA ENABLE H CN2
D4-2 DATA ENABLE Ø3-Ø3 H FK1
+5V
R25 10K
C96 68pf
R26 1K
R27 1K
D4-5 DR Ø3 H
D4-5 DR Ø2 H
D4-4 DR Ø1 H
D4-4 DR ØØ H
DATA NOT AVAILABLE L FC1
D4-7 MDET Ø3 H
D4-7 MDET Ø2 H
D4-6 MDET Ø1 H
D4-6 MDET ØØ H
MATCH DETECT L FE1

D4-2 BUF RDE Ø3 L
D4-2 BUF RDE Ø2 L
D4-2 BUF RDE Ø1 L
D4-2 BUF RDE ØØ L
D4-2 THRL Ø3 L
D4-2 THRL Ø2 L
D4-2 THRL Ø1 L
D4-2 THRL ØØ L
D3-4 TRANSMITTER STROBE H EM2
D3-4 MASTER SCAN Ø1 H EM1
D3-4 MASTER SCAN ØØ H EN1
D4-5 TRAN FLAG Ø3 H
D4-5 TRAN FLAG Ø2 H
D4-4 TRAN FLAG Ø1 H
D4-4 TRAN FLAG ØØ H
D4-7 REC FLAG Ø3 H
D4-7 REC FLAG Ø2 H
D4-6 REC FLAG Ø1 H
D4-6 REC FLAG ØØ H
TRAN FLAG WAITING L FL2
RECEIVER FLAG L FM2
D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D3-4 MASTER SCAN T/R CE2

(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD (D4-2)
DRAWING NUMBER: DCS M7839-Ø-1
REV: F
SCALE
SHEET 3 OF 9
CHKD. MK

NOTE:1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M7839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

REVISIONS		
ORIG	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD (D4-3)		SIZE: D	CODE: CS	NUMBER: M7839-Ø-1	REV: F
SCALE:	SHEET 4 OF 9	DIST:			

(CLOCK SOURCE AND SELECTION)

EIA REC DATA ØØ
EIA REC DATA Ø1
D2-3 LCR 14 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR ØJ H
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT ØØ-Ø3 L
D4-2 BUF CONTROL STROBE L
D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ (1) H
D4-4 MODE Ø1 (Ø) H
D4-4 MODE Ø1 (1) H
D4-3 INTR MAINTENANCE ØØ-Ø3 H
D4-4 TRANS DISABLE ØØ-Ø3 H
D4-4 INTR RCV DATA ØØ-Ø3 L
D4-4 RCV IN ØØ H
D4-4 RCV IN Ø1 H
D4-4 BUF MODE ØØ (Ø) H
D4-4 BUF MODE Ø1 (Ø) H
SERIAL OUT ØØ L
SERIAL OUT Ø1 L
ETCH CUTS FOR YC VARIATION ONLY
EIA XMIT DATA ØØ
EIA XMIT DATA Ø1
D4-3 TX CLOCK Ø1 H
74LS74
YC VARIATION ONLY
D4-8 TMARK ØØ L
D4-3 TX CLOCK ØØ H
D4-2 RESET H
D4-2 THRL ØØ L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE ØØ L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
D4-4 MODE ØØ (1) H
TCO ØØ H
EOC ØØ H
D4-4 DA ØØ H
D4-4 TRAN FLAG ØØ H
D4-3 TX CLOCK ØØ H
D4-2 RESET A L
YC VARIATION
D4-8 TMARK Ø1 L
D4-3 TX CLOCK Ø1 H
D4-2 RESET H
D4-2 THRL Ø1 L
TCO Ø1 H
EOC Ø1 H
D4-4 DA Ø1 H
D4-4 TRAN FLAG Ø1 H
(MODE SELECTION, TRANSMITTERS ØØ AND Ø1).

REVISIONS		
ECR	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD (D4-4)
DCSM7839-Ø-1
REV. F
SCALE
SHEET 5 OF 9
MK

EIA REC DATA Ø2 — J1 NN — 1Ø04 E11 — C88 470pf

D4-4 MODE ØØ (Ø) H — 9 — 7450 E9 — 8

D4-4 MODE ØØ (1) H — 13 — 1

D4-4 TRANS DISABLE ØØ-Ø3 H (AF2) — 2 — 7402 E12 — 1 — 3

9 — 7400 E25 — 8 — BK2 — D4-5 RCV IN Ø2 H

D4-4 INTR RCV DATA ØØ-Ø3 L — BC1

D4-4 BUF MODE ØØ(Ø)H — 5 — 8242 E2 — 4

+5V — R42 1K — 12 — 13 — 1488 E6 — 11 — J1 CC — EIA XMIT DATA Ø2

D4-4 MODE ØØ(1) H — 12 — CUT ETCH: YC VAR ONLY — 7402 E12 — 13 — 11

5 — 7404 E10 — 6 — AT2 — SERIAL OUT Ø2 L

EIA REC DATA Ø3 — J1 KK — 1Ø — 1489 E11 — 8 — C85 470Pf

D4-4 MODE ØØ(Ø) H — 2 — 3 — 7450 E9 — 6

D4-4 MODE ØØ(1) H — 4 — 5

6 — 7402 E5 — 4 — (AF2) — D4-4 TRANS DISABLE ØØ-Ø3 H

13 — 7400 E25 — 11 — BK1 — D4-5 RCV IN Ø3 H

D4-4 BUF MODE ØØ (Ø) H — +5V — R45 1K — J1 EE — EIA XMIT DATA Ø3

D4-4 MODE ØØ(1) H — 9 — 7402 E5 — 10 — 8 — 1 — 2 — 8292 E2 — 3 — 12 — 13 — 1488 E26 — 11

ETCH CUT FOR YC VARIATION ONLY

+5 — -12V — VSS 1 — VGG 16 — VDD 21

D4-8 TMARK Ø2 L EJ2 — 17 — CTS

D4-3 TX CLOCK Ø2 H — 5 — TRC

D4-2 RESET H — 18 — MR

10 — DAR

D4-2 THRL Ø2 L — 19 — THRL

D4-2 TR8 H — 38 — TR8

D4-2 TR7 H — 36 — TR7

D4-2 TR6 H — 34 — TR6

D4-2 TR5 H — 32 — TR5

D4-2 TR4 H — 30 — TR4

D4-2 TR3 H — 28 — TR3

D4-2 TR2 H — 26 — TR2

D4-2 TR1 H — 24 — TR1

D4-2 STROBE Ø2 L — 26 — FNRL

D4-1 SYNC Ø8 — 37 — FR8

D4-1 SYNC Ø7 — 35 — FR7

D4-1 SYNC Ø6 — 33 — FR6

D4-1 SYNC Ø5 — 31 — FR5

D4-1 SYNC Ø4 — 29 — FR4

D4-1 SYNC Ø3 — 27 — FR3

D4-1 SYNC Ø2 — 25 — FR2

D4-1 SYNC Ø1 — 23 — FR1

4 — CRL

22 — CD

SAT Ø2 E59

TRO — 15

TCO — 11 EJ2 — TCO Ø2 H

DD/EOC — 13 EK2 — EOC Ø2 H

DA — 12 — D4-5 DA Ø2 H

THRE — 14 — D4-5 TRAN FLAG Ø2 H

PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2

3 2 39 40 6 7 8 9

D4-1 PI

D4-1 EPE

D4-1 WLS1

D4-1 WLS2

+3V — 10 — 12 — D — 5 — Q — 9 — E77 — C — R — Q — 8 — 11 — 13 — 74LS74

D4-3 TXCLK Ø2 H

D4-2 RESET B L

YC VARIATION ONLY

+5 — -12V — VSS 1 — VGG 16 — VDD 21

D4-8 TMARK Ø2L EE2 — 17 — CTS

D4-3 TX CLOCK Ø3 H — 5 — TRC

D4-2 RESET H — 18 — MR

10 — DAR

D4-2 THR_ Ø3 L — 19 — THRL

D4-2 TR8 H — 38 — TR8

D4-2 TR7 H — 36 — TR7

D4-2 TR6H — 34 — TR6

D4-2 TR5H — 32 — TR5

D4-2 TR4 H — 30 — TR4

D4-2 TR3H — 28 — TR3

D4-2 TR2H — 26 — TR2

D4-2 TR1H — 24 — TR1

D4-2 STROBE Ø3 L — 26 — FNRL

D4-1 SYNC Ø8 — 37 — FR8

D4-1 SYNC Ø7 — 35 — FR7

D4-1 SYNC Ø6 — 33 — FR6

D4-1 SYNC Ø5 — 31 — FR5

D4-1 SYNC Ø4 — 29 — FR4

D4-1 SYNC Ø3 — 27 — FR3

D4-1 SYNC Ø2 — 25 — FR2

D4-1 SYNC Ø1 — 23 — FR1

4 — CRL

22 — CD

SAT Ø3 E58

TRO — 15 — 9 — 7404 E10 — 8 — AH2 — SERIAL OUT Ø3 L

ETCH CUT YC VARIATION ONLY

TCO — 11 ED2 — TCO Ø3 H

DD/EOC — 13 EF2 — EOC Ø3 H

DA — 12 — D4-5 DA Ø3 H

THRE — 14 — D4-5 TRAN FLAG Ø3 H

PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2

3 2 39 40 6 7 8 9

D4-1 PI

D4-1 EPE

D4-1 WLS1

D4-1 WLS2

+3V — 4 — 2 — D — 5 — Q — 6 — E77 — C — R — Q — 3 — 1 — 74LS74

D4-3 TXCLOCK Ø3 H

D4-2 RESET B L

YC VARIATION ONLY

(TRANSMITTERS Ø2 AND Ø3)

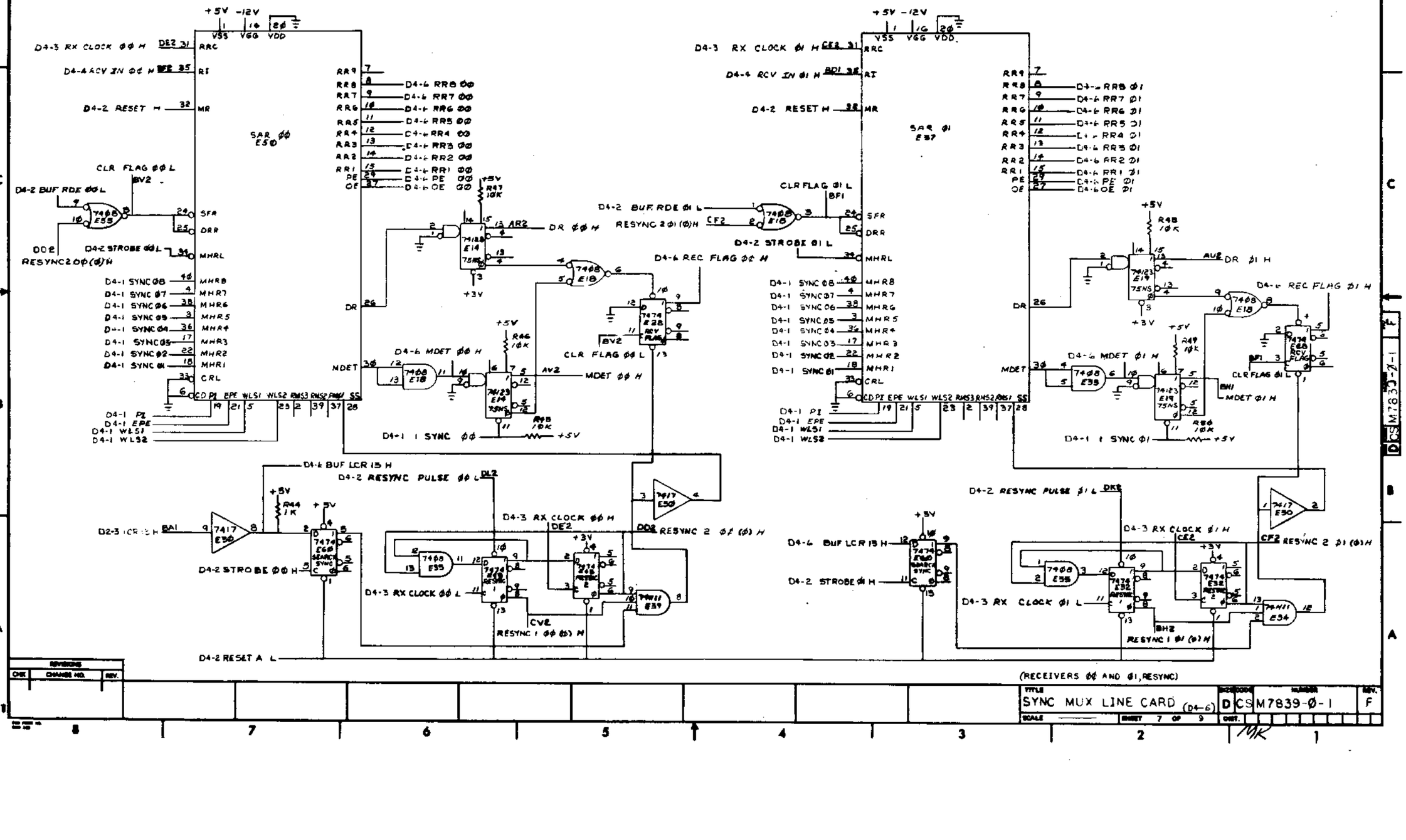
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD (D4-5)

SIZE: D — CS: M7839-Ø-1 — REV: F

SCALE — SHEET 6 OF 9

DCS M7839-Ø-1 F



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	DRAWING NO.	REV.
SYNC MUX LINE CARD (D4-6)	DCS M7839-Ø-1	F
SCALE	SHEET 7 OF 9	

D4-2 RX CLOCK Ø2 H
D4-2 RCV IN Ø2 H
D4-2 RESET H
SAR Ø2 E46
D4-2 BUF RDE Ø2 L
CLR FLAG Ø2 L
D4-2 STROBE Ø2 L
RESYNC 2 Ø2 (Ø) H
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
D4-7 RR8 Ø2
D4-7 RR7 Ø2
D4-7 RR6 Ø2
D4-7 RR5 Ø2
D4-7 RR4 Ø2
D4-7 RR3 Ø2
D4-7 RR2 Ø2
D4-7 RR1 Ø2
D4-7 PE Ø2
D4-7 OE Ø2
D4-7 REC FLAG Ø2 H
D4-7 MDET Ø2 H
MDET Ø2 H
D4-1 I SYNC Ø2
D4-2 RESYNC PULSE Ø2 L
D4-3 RX CLOCK Ø2 H
D4-3 RX CLOCK Ø2 L
D4-6 BUF LCR 13 H
RESYNC 1 Ø2 (Ø) H
D4-2 RESET B L

D4-3 RX CLOCK Ø3 H
D4-3 RCV IN Ø3 H
D4-2 RESET H
SAR Ø3 E40
D4-2 BUF RDE Ø3 L
CLR FLAG Ø3 L
D4-2 STROBE Ø3 L
RESYNC 2 Ø3 (Ø) H
D4-7 RR8 Ø3
D4-7 RR7 Ø3
D4-7 RR6 Ø3
D4-7 RR5 Ø3
D4-7 RR4 Ø3
D4-7 RR3 Ø3
D4-7 RR2 Ø3
D4-7 RR1 Ø3
D4-7 PE Ø3
D4-7 OE Ø3
D4-7 REC FLAG Ø3 H
D4-7 MDET Ø3 H
CLR FLAG Ø3 L
BP2
MDET Ø3 H
D4-1 I SYNC Ø3
D4-2 RESYNC PULSE Ø3 L
D4-3 RX CLOCK Ø3 H
D4-3 RX CLOCK Ø3 L
D4-6 BUF LCR 13 H
RESYNC 1 Ø3 (Ø) H

(RECEIVERS Ø2 AND Ø3, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD (D4-7)			SIZE: D	CODE: CS
SCALE:	SHEET: 8 OF 9		DIST.	NUMBER: M7839-Ø-1
				REV: F

D4-7 RR6 Ø5
D4-7 RR6 Ø2
D4-6 RR6 Ø1
D4-6 RR6 ØØ
D4-7 RR5 Ø5
D4-7 RR5 Ø2
D4-6 RR5 Ø1
D4-6 RR5 ØØ
5781 5780 74153 E42
8881 E74 FR1 RECV DATA Ø5 L
8881 E74 FS1 RECV DATA Ø4 L

D4-7 PE Ø5
D4-7 PE Ø2
D4-6 PE Ø1
D4-6 PE ØØ
D4-7 DE Ø5
D4-7 DE Ø2
D4-6 DE Ø1
D4-6 DE ØØ
5781 5780 74153 E44
8881 E76 FM1 MASTER PE L
8881 E78 FL1 MASTER OR L

D4-2 SET TMARK Ø5 L
D4-2 SET TMARK Ø2 L
D4-2 SET TMARK Ø1 L
D4-2 SET TMARK ØØ L
D4-2 RESET H
7474 EG3 TMARK Ø5 — EE2 D4-8 TMARK Ø5 L
7474 EG4 TMARK Ø2 — EL2 D4-9 TMARK Ø2 L
7474 EG5 TMARK Ø1 — CB2 D4-8 TMARK Ø1 L
7474 EG5 TMARK ØØ — CD2 D4-8 TMARK ØØ L

D4-7 RR4 Ø5
D4-7 RR4 Ø2
D4-6 RR4 Ø1
D4-6 RR4 ØØ
D4-7 RR3 Ø3
D4-7 RR3 Ø2
D4-6 RR3 Ø1
D4-6 RR3 ØØ
5781 5780 74153 E45
8881 E74 FN1 RECV DATA Ø5 L
8881 E74 FP1 RECV DATA Ø2 L

D3 3 CLEAR TMARK L FK2 19
5788 5784 74155 E78
FB3 FB2 FB1 FB0
FA3 FA2 FA1 FA0
DB DA

D4-2 CARD FLAG SELECT ØØ-Ø3 L DM2

D4-7 RR2 Ø3
D4-7 RR2 Ø2
D4-6 RR2 Ø1
D4-6 RR2 ØØ
D4-7 RR1 Ø3
D4-7 RR1 Ø2
D4-6 RR1 Ø1
D4-6 RR1 ØØ
5781 5780 74153 E49
8881 E71 FN2 RECV DATA Ø1 L
8881 E71 FP2 RECV DATA ØØ L

D4-7 RR8 Ø3
D4-7 RR8 Ø2
D4-6 RR8 Ø1
D4-6 RR8 ØØ
D4-7 RR7 Ø3
D4-7 RR7 Ø2
D4-6 RR7 Ø1
D4-6 RR7 ØØ
5781 5780 74153 E56
8881 E76 FH1 RECV DATA Ø7 L
8881 E78 FJ1 RECV DATA Ø6 L

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D4-2 DATA ENABLE ØØ-Ø3 H (FK1)

(RECV DATA MUX'S AND TMARK DECODER)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SYNC MUX LINE CARD (D4-8)	
SIZE	D	
CODE	CS	
NUMBER	M7839-Ø-1	
REV.	F	
SCALE		
SHEET	9 OF 9	
DIST.	MK	

DCS M7839-Ø-1 F

BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR Ø0
C	GROUND
D	DCE SCR Ø1
E	GROUND
F	DCE SCR Ø2
H	GROUND
J	DCE SCR Ø3
K	GROUND
L	EIA RCV DATA ØØ
M	GROUND
N	EIA RCV DATA Ø1
P	GROUND
R	EIA XMIT DATA ØØ
S	GROUND
T	EIA XMIT DATA Ø1
U	GROUND
V	DTE SCTE ØØ
W	GROUND
X	DTE SCTE Ø1
Y	DTE SCTE Ø2
Z	GROUND
A A	DTE SCTE Ø3
B B	GROUND
C C	EIA XMIT DATA Ø2
D D	GROUND
E E	EIA XMIT DATA Ø3
F F	GROUND
H H	EIA RCV DATA Ø2
J J	GROUND
K K	EIA RCV DATA Ø3
L L	GROUND
M M	DCE SCT Ø3
N N	GROUND
P P	DCE SCT Ø2
R R	GROUND
S S	DCE SCT Ø1
T T	GROUND
U U	DCE SCT ØØ
V V	GROUND

PARAMETER SWITCH SETTINGS

FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL/HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HDØ3	S2	5	ON		OFF	
	HDØ2	S2	6	ON		OFF	
	HDØ1	S2	7	ON		OFF	
	HDØØ	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC ØØ	S1	5	OFF		ON	
	1 SYNC Ø1	S1	6	OFF		ON	
	1 SYNC Ø2	S1	7	OFF		ON	
	1 SYNC Ø3	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1↕8	OFF		ON	
LCR10=1	SYNC B	S3	1↕8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1	GROUND
	CS2	GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1	GROUND
	MS2	NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1	NO CONNECTION
	RMS2	NO CONNECTION
	RMS3	NO CONNECTION

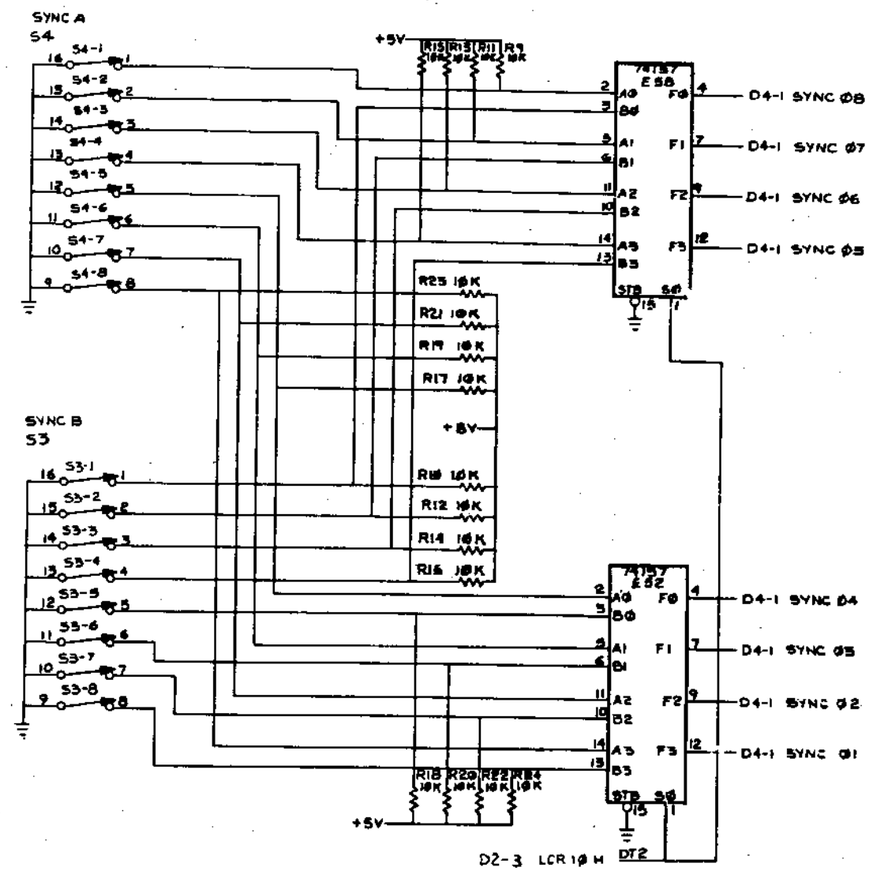
S2

S2-1 1 — S2-2 2 } UNUSED
S2-3 3 — D4-1 SELECT B
S2-4 4 — D4-1 SELECT A
S2-5 5 — D4-1 HD Ø3
S2-6 6 — D4-1 HD Ø2
S2-7 7 — D4-1 HD Ø1
S2-8 8 — D4-1 HD ØØ

S1

S1-1 1 — D4-1 PI
S1-2 2 — D4-1 EPE
S1-3 3 — D4-1 WLS1
S1-4 4 — D4-1 WLS2
S1-5 5 — D4-1 1SYNC ØØ
S1-6 6 — D4-1 1 SYNC Ø1
S1-7 7 — D4-1 1 SYNC Ø2
S1-8 8 — D4-1 1 SYNC Ø3

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA Ø8 H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KB H. NO M7839 CIRCUITRY IS CONNECTED TO IT.



D3-5 230.4 KB H BM1
(SEE NOTE 4)

(CHARTS SWITCHES AND SYNC SELECTOR)

REVISIONS		
CHR	CHANGE NO.	REV.
	DVII-00006	A

DRN.		4/8
CHK.		4/8/80
ENG.		
PROJ. ENG.		
PROD.		
NEXT HIGHER ASSY.	8-00-DVII-Ø	
SCALE		
SHEET 1 OF 8		

FIRST USED ON: DVII

TITLE: SYNC MUX LINE CARD LINES ØØ-Ø3 (94-1)

SIZE	CODE	NUMBER	REV.
D	85	DVII-Ø-10	A

DIST.

D4-2 CARD PARAMETER SELECT ØØ-Ø3 L DMZ

D3-8 SRS Ø3 L BS2
D3-8 SRS Ø2 L BE2
7400 E23

D2-3 CONTROL STROBE H CS2
7404 E41
D4-2 BUF CONTROL STROBE L

D3-7 INIT DI L EN2
7437 E63
D4-2 RESET H
D4-2 RESET A L
D4-2 RESET B L
+3V

D4-2 STROBE Ø3 L
D4-2 STROBE Ø2 L
D4-2 STROBE Ø1 L
D4-2 STROBE ØØ L
7404 E54
D4-2 STROBE Ø3 H
D4-2 STROBE Ø2 H
D4-2 STROBE Ø1 H
D4-2 STROBE ØØ H

D3-8 SES Ø1 H BT2
D3-8 SES ØØ H BM2

D4-5 RCV IN Ø3 H
D4-5 RCV IN Ø2 H
D4-4 RCV IN Ø1 H
D4-4 RCV IN ØØ H
74153 E22
8881 E67
FPI BIT WINDOW L
BE2
D4-3 INTR MAINTENANCE ØØ-Ø3 H

D3-4 TRAN DATA Ø8 H ERI (SEE NOTE 3 ON SHEET 1 OF 8)
D3-4 TRAN DATA Ø7 H EP1
7417 E61
D4-2 TRB H

D3-4 TRAN DATA Ø6 H EM2
7417 E61
D4-2 TRT H

D3-4 TRAN DATA Ø5 H FR2
7417 E76
D4-2 TRG H

D3-4 TRAN DATA Ø4 H FV2
7417 E76
D4-2 TRS H

D3-4 TRAN DATA Ø3 H FS2
7417 E76
D4-2 TR4 H

D3-4 TRAN DATA Ø2 H FV1
7417 E76
D4-2 TR3 H

D3-4 TRAN DATA Ø1 H FT2
7417 E76
D4-2 TR2 H

D3-4 TRAN DATA ØØ H FU2
7417 E76
D4-2 TR1 H

D3-4 MASTER SCAN Ø H BU2
D3-4 MASTER SCAN C H EN2
7437 E63
D4-2 CARD FLAG SELECT ØØ-Ø3 L DM2

D3-3 RESYNC PULSE L DF2
7404 E41
D4-2 RESYNC PULSE Ø3 L DH2
D4-2 RESYNC PULSE Ø2 L DJ2
D4-2 RESYNC PULSE Ø1 L DK2
D4-2 RESYNC PULSE ØØ L DL2

D3-3 SET TMARK L CU2
7404 E41
D4-2 SET TMARK Ø3 L
D4-2 SET TMARK Ø2 L
D4-2 SET TMARK Ø1 L
D4-2 SET TMARK ØØ L

D1-5 RECEIVED DATA ENABLE H CN2
74H11 E39
FXI
D4-2 DATA ENABLE ØØ-Ø3 H

+5V
225 1ØK
C96 68pf
74123 E75 RDE
FUI
2DE ØØ-Ø3 H
+3V

D3-4 TRANSMITTER STROBE H EM2

+5V
226 1K
D3-4 MASTER SCAN Ø1 H EM1
7417 E61

+5V
227 1K
D3-4 MASTER SCAN ØØ H EN1
7417 E61

D4-2 BUF RDE Ø3 L
D4-2 BUF RDE Ø2 L
D4-2 BUF RDE Ø1 L
D4-2 BUF RDE ØØ L
D4-2 THRL Ø3 L
D4-2 THRL Ø2 L
D4-2 THRL Ø1 L
D4-2 THRL ØØ L

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D3-4 MASTER SCAN T/R CRR
7404 E41

D4-5 DA Ø3 H
D4-5 DA Ø2 H
D4-4 DA Ø1 H
D4-4 DA ØØ H
D4-7 MDET Ø3 H
D4-7 MDET Ø2 H
D4-6 MDET Ø1 H
D4-6 MDET ØØ H
74153 E62
8881 E67
PCI DATA NOT AVAILABLE L
FEI MATCH DETECT L

D4-5 TRAN FLAG Ø3 H
D4-5 TRAN FLAG Ø2 H
D4-4 TRAN FLAG Ø1 H
D4-4 TRAN FLAG ØØ H
D4-7 REC FLAG Ø3 H
D4-7 REC FLAG Ø2 H
D4-6 REC FLAG Ø1 H
D4-6 REC FLAG ØØ H
74153 E48
8881 E71
FLZ TRAN FLAG WAITING L
FMZ RECEIVER FLAG L

(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-2)	SIZE	CODE	NUMBER / REV.
		D	BS	DVII-Ø-1Ø A
SCALE	SHEET 2 OF 8	DRWG.		

DVII-Ø-1Ø A

NOTE 1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M1839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.

D4-8 TMARK ØØ L — CD2 — R28 10K +5V — D4-1 HD ØØ — 7400 E33
DCE SCR ØØ — J1 B — 1489 E5 — 7432 E4 — CB1 470 pF
D4-3 RX CLOCK ØØ L — 74H11 E25 — 7404 E91 — DE2 — D4-3 RX CLOCK ØØ H

D4-8 TMARK Ø2 L — EL2 — R33 10K +5V — D4-1 HD Ø2 — 7400 E38
DCE SCR Ø2 — J1 F — 1489 E5 — 7432 E9 — CB3 470 pF
D4-3 RX CLOCK Ø2 L — 74H11 E39 — 7404 E54 — 12 DS2 — D4-3 RX CLOCK Ø2 H

DCE SCR Ø1 — J1 D — 1489 E5 — 7432 E4 — CB2 470 pF
D4-3 RX CLOCK Ø1 L — 74H11 E25 — 7404 E54 — 10 CE2 — D4-3 RX CLOCK Ø1 H
D4-8 TMARK Ø1 L — CB2 — R29 10K +5V — D4-1 HD Ø1 — 7400 E33

D4-3 RX CLOCK Ø3 L — 74H11 E25 — 7404 E91 — 8 CP2 — D4-3 RX CLOCK Ø3 H
DCE SCR Ø3 — J1 J — 1489 E5 — 7432 E4 — CB4 470 pF
D4-8 TMARK Ø3 L — EE2 — R24 10K +5V — D4-1 HD Ø3 — 7400 E32

DCE SCT ØØ — J1 44 — 1489 E16 — 7432 E15 — CB8 470 pF — 7400 E21 — D4-3 TX CLOCK ØØ H
DCE SCT Ø1 — J1 55 — 1489 E16 — 7432 E15 — CB9 470 pF — 7400 E21 — D4-3 TX CLOCK Ø1 H
DCE SCT Ø2 — J1 PP — 1489 E16 — 7432 E15 — CB10 470 pF — 7400 E21 — D4-3 TX CLOCK Ø2 H
DCE SCT Ø3 — J1 MM — 1489 E16 — 7432 E15 — CB9 470 pF — 7400 E21 — D4-3 TX CLOCK Ø3 H

J1 — DTE SCTE ØØ — R37 7.5K SEE NOTE 1 — 1488 E26 — V
DTE SCTE Ø1 — R36 7.5K SEE NOTE 1 — 1488 E6 — X
DTE SCTE Ø2 — R35 7.5K SEE NOTE 1 — 1488 E26 — Y
DTE SCTE Ø3 — R38 7.5K SEE NOTE 1 — 1488 E26 — AA

S1 S2 S3 S4 S5 S6 S7 S8 — 74LS32 E68
D3-5 9600 BAUD — FF2
D3-5 4800 BAUD — FE2
D3-5 2400 BAUD — FD2
D3-5 1200 BAUD — FD1
R31 10K +5V
R32 10K
D4-1 SELECT B
D4-1 SELECT A
F1 — ES2 — D4-3 MUX CLOCK ØØ-Ø3 H

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

D2-3 MAINTENANCE CLK PULSE H — ET2 — 7430 E64 — 8 BS1 — SOURCE CLOCK A ØØ-Ø3 L
D4-3 MUX CLOCK ØØ-Ø3 H (ES2) — D2-3 MAINTENANCE CLK PULSE H (ET2) — 7450 E64 — 6 — BN2 — SOURCE CLOCK B ØØ-Ø3 L
M32 — SYSTEM MODE ØØ-Ø3 H

D4-4 MODE ØØ (1) H — 7417 E61 — D4-4 MODE Ø1 (Ø) H — R30 1K +5V — 7408 E13 — BE2 — D4-3 INTR MAINTENANCE ØØ-Ø3 H

(CLOCK SOURCE AND SELECTION)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-3)
SIZE D | CODE BS | NUMBER DV11-Ø-10 | REV. A
SCALE | SHEET 3 OF 8 | DIST.

D4-4 MODE ØØ (0) H
D4-4 MODE ØØ (1) H
D4-4 RCV IN ØØ H
D4-4 INTR RCV DATA ØØ-Ø3 L
EIA REC DATA Ø1
D4-4 MODE Ø1 (0) H
D4-4 MODE Ø1 (1) H
D4-4 RCV IN Ø1 H
D4-4 TRANS DISABLE ØØ-Ø3 H
SERIAL OUT Ø1 L
D4-4 BUF MODE ØØ (0) H
EIA XMIT DATA Ø1
D2-3 LCR 14 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR Ø3 H
EIA REC DATA ØØ
D4-3 INTR MAINTENANCE ØØ-Ø3 H
D4-4 MODE Ø1 (1) H
D4-4 MODE Ø1 (0) H
D4-4 TRANS DISABLE ØØ-Ø3 H
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT ØØ-Ø3 L
D4-2 BUF CONTROL STROBE L
SERIAL OUT ØØ L
D4-4 BUF MODE ØØ (0) H
EIA XMIT DATA ØØ
D4-4 MODE ØØ (1) H
D4-8 TMARK ØØ L
D4-3 TX CLOCK ØØ H
D4-2 RESET H
D4-2 THRL ØØ L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE ØØ L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TCO ØØ H
EOC ØØ H
D4-4 DA ØØ H
D4-4 TRAN FLAG ØØ H
D4-8 TMARK Ø1 L
D4-3 TX CLOCK Ø1 H
D4-2 RESET H
D4-2 THRL Ø1 L
D4-2 STROBE Ø1 L
TCO Ø1 H
EOC Ø1 H
D4-4 DA Ø1 H
D4-4 TRAN FLAG Ø1 H
(MODE SELECTION, TRANSMITTERS ØØ AND Ø1)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-4)	D	BS	DV11-Ø-10	A

SCALE — SHEET 4 OF 8 — DWG.

EIA REC DATA Ø2 — J1 HH — 1488 E11 — CBB 47Øpf

D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7430 E9

D4-4 TRANS DISABLE ØØ-Ø3 H (AF2) — 7402 E12

7400 E23 — BK2 — D4-5 RCV IN Ø2 H

D4-4 INTR RCV DATA ØØ-Ø3 L — BC1

D4-4 BUF MODE ØØ(Ø)H — 8242 E2 — +5V R42 1K — 1488 E6 — J1 CC — EIA XMIT DATA Ø2

D4-4 MODE ØØ (1) H — 7402 E12 — 7404 E10 — AT2 — SERIAL OUT Ø2 L

EIA REC DATA Ø3 — J1 KK — 1488 E11 — CB5 47Øpf

D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7430 E9 — 7402 E3 — (AF2) — D4-4 TRANS DISABLE ØØ-Ø3 H

7400 E23 — BK1 — D4-5 RCV IN Ø3 H

D4-4 BUF MODE ØØ (Ø) H — +5V R45 1K — 8242 E2 — 1488 E26 — J1 E8 — EIA XMIT DATA Ø3

D4-4 MODE ØØ(1)H — 7402 E3 — SERIAL OUT Ø3 L — AH2

+5V -12V — VSS VGG VDD

SAT Ø2 E57

D4-8 TMARK Ø2 L — EE2 17 — CTS
D4-3 TX CLOCK Ø2 H — 5 — TRC
D4-2 RESET H — 18 — MR
10 — DAR
D4-2 THRL Ø2 L — 19 — THRL
D4-2 TR8 H — 38 — TR8
D4-2 TR7 H — 36 — TR7
D4-2 TR6 H — 34 — TR6
D4-2 TR5 H — 32 — TR5
D4-2 TR4 H — 30 — TR4
D4-2 TR3 H — 28 — TR3
D4-2 TR2 H — 26 — TR2
D4-2 TR1 H — 24 — TR1
D4-2 STROBE Ø2 L — 22 — FHRL
D4-1 SYNC Ø8 — 37 — FR8
D4-1 SYNC Ø7 — 35 — FR7
D4-1 SYNC Ø6 — 33 — FR6
D4-1 SYNC Ø5 — 31 — FR5
D4-1 SYNC Ø4 — 29 — FR4
D4-1 SYNC Ø3 — 27 — FR3
D4-1 SYNC Ø2 — 25 — FR2
D4-1 SYNC Ø1 — 23 — FR1
4 — CRL
ER — CO PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 — 3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO 15 — TCO 11 EJ2 — TCO Ø2 H — DD/EOC 13 EK2 — EOC Ø2 H — DA 12 — D4-5 DA Ø2 H — THRE 14 — D4-5 TRAN FLAG Ø2 H

SAT Ø3 E55

D4-8 TMARK Ø3 L — EE2 17 — CTS
D4-3 TX CLOCK Ø3 H — 5 — TRC
D4-2 RESET H — 18 — MR
16 — DAR
D4-2 THRL Ø3 L — 19 — THRL
D4-2 TR8 H — 38 — TR8
D4-2 TR7 H — 36 — TR7
D4-2 TR6 H — 34 — TR6
D4-2 TR5 H — 32 — TR5
D4-2 TR4 H — 30 — TR4
D4-2 TR3 H — 28 — TR3
D4-2 TR2 H — 26 — TR2
D4-2 TR1 H — 24 — TR1
D4-2 STROBE Ø3 L — 22 — FHRL
D4-1 SYNC Ø8 — 37 — FR8
D4-1 SYNC Ø7 — 35 — FR7
D4-1 SYNC Ø6 — 33 — FR6
D4-1 SYNC Ø5 — 31 — FR5
D4-1 SYNC Ø4 — 29 — FR4
D4-1 SYNC Ø3 — 27 — FR3
D4-1 SYNC Ø2 — 25 — FR2
D4-1 SYNC Ø1 — 23 — FR1
4 — CRL
22 — CO PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 — 3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO 15 — 7404 E16 — AH2 — SERIAL OUT Ø3 L

TCO 11 EDE — TCO Ø3 H — DD/EOC 13 EFE — EOC Ø3 H — DA 12 — D4-5 DA Ø3 H — THRE 14 — D4-5 TRAN FLAG Ø3 H

REVISIONS

CHK	CHANGE NO.	REV.

(TRANSMITTERS Ø2 AND Ø3)

TITLE SYNC MUX LINE CARD LINES ØØ-Ø3 (Ø4-5)

SIZE D — CODE BS — NUMBER DVII-Ø-1Ø — REV. A

SCALE — SHEET 5 OF 8 — DIST.

DVII-Ø-1Ø A

D4-3 RX CLOCK ØØ H
D4-4 RCV IN ØØ H
D4-2 RESET H
SAR ØØ E5Ø
CLR FLAG ØØ L
D4-2 BUF RDE ØØ L
CV2
RESYNC 1 ØØ (Ø) H
D4-2 STROBE ØØ L
D4-1 SYNC ØØ
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 P1
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
D4-6 RR8 ØØ
D4-6 RR7 ØØ
D4-6 RR6 ØØ
D4-6 RR5 ØØ
D4-6 RR4 ØØ
D4-6 RR3 ØØ
D4-6 RR2 ØØ
D4-6 RR1 ØØ
D4-6 PE ØØ
D4-6 OE ØØ
DR ØØ H
D4-6 MDET ØØ H
MDET ØØ H
CLR FLAG ØØ L
D4-1 1 SYNC ØØ
D4-6 REC FLAG ØØ H
D4-6 BUF LCR 13 H
D2-3 LCK 13 H
D4-2 STROBE ØØ H
D4-2 RESYNC PULSE ØØ L
D4-3 RX CLOCK ØØ H
D4-3 RX CLOCK ØØ L
RESYNC 2 ØØ (Ø) H
D4-2 RESET A L

D4-3 RX CLOCK Ø1 H
D4-4 RCV IN Ø1 H
D4-2 RESET H
SAR Ø1 E37
CLR FLAG Ø1 L
D4-2 BUF RDE Ø1 L
RESYNC 1 Ø1 (Ø) H
D4-2 STROBE Ø1 L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 P1
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
D4-6 RR8 Ø1
D4-6 RR7 Ø1
D4-6 RR6 Ø1
D4-6 RR5 Ø1
D4-6 RR4 Ø1
D4-6 RR3 Ø1
D4-6 RR2 Ø1
D4-6 RR1 Ø1
D4-6 PE Ø1
D4-6 OE Ø1
AUE DR Ø1 H
D4-6 REC FLAG Ø1 H
D4-6 MDET Ø1 H
MDET Ø1 H
CLR FLAG Ø1 L
D4-1 1 SYNC Ø1
D4-6 BUF LCR 13 H
D4-2 STROBE Ø1 H
D4-2 RESYNC PULSE Ø1 L
D4-3 RX CLOCK Ø1 L
CF2 RESYNC 2 Ø1 (Ø) H
RESYNC 1 Ø1 (Ø) H

(RECEIVERS ØØ AND Ø1, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-6)			
SIZE	CODE	NUMBER	REV.	
D	BS	DVII-Ø-1Ø	A	
SCALE		SHEET 6 OF 8	DIST.	

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø2 H DS2
D4-5 RCV IN Ø2 H BK2
D4-2 RESET H
SAR Ø2 E46
RRC RI MR SFR DRR MHRL MHR8 MHR7 MHR6 MHR5 MHR4 MHR3 MHR2 MHR1 CRL CD PI EPE WLS1 WLS2 RMS7 RMS6 RMS1 RMS0
RR9 RR8 RR7 RR6 RR5 RR4 RR3 RR2 RR1 PE OE
D4-7 RR8 Ø2 … D4-7 OE Ø2
D4-1 PI D4-1 EPE D4-1 WLS1 D4-1 WLS2
D4-2 BUF RDE Ø2 L
CLR FLAG Ø2 L BU2
7408 E29
DN2
RESYNC 1 Ø2 (Ø) H
D4-2 STROBE Ø2 L
D4-1 SYNC Ø8 … D4-1 SYNC Ø1
R51 1ØK +5V
DR Ø2 H BB1
7413 E20 7SNS
+3V
DR
MDET
D4-7 MDET Ø2 H
R52 1ØK
BU2
CLR FLAG Ø2 L
BJ2
MDET Ø2 H
D4-1 1 SYNC Ø2
R53 1ØK +5V
7474 E27 RCV FLAG
D4-7 REC FLAG Ø2 H
D4-2 RESYNC PULSE Ø2 L DJ2
D4-3 RX CLOCK Ø2 H DS2
D4-6 BUF LCR 13 H
D4-2 STROBE Ø2 H
D4-3 RX CLOCK Ø2 L
7417 E36
DR2
RESYNC 2 Ø2 (Ø) H
7474 E36 SEARCH SYNC
7474 E31 RESYNC
74H11 E34
DN2
RESYNC 1 Ø2 (Ø) H
D4-2 RESET B L

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø3 H CP2
D4-5 RCV IN Ø3 H BK1
D4-2 RESET H
SAR Ø3 E46
RRC RI MR SFR DRR MHRL MHR8 MHR7 MHR6 MHR5 MHR4 MHR3 MHR2 MHR1 CRL CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 RMS0
RR9 RR8 RR7 RR6 RR5 RR4 RR3 RR2 RR1 PE OE
D4-7 RR8 Ø3 … D4-7 OE Ø3
D4-1 PI D4-1 EPE D4-1 WLS1 D4-1 WLS2
CLR FLAG Ø3 L BV1
D4-2 BUF RDE Ø3 L
RESYNC 1 Ø3 (Ø) H BK2
7408 E31
D4-2 STROBE Ø3 L
D4-7 REC FLAG Ø2 H
D4-1 SYNC Ø8 … D4-1 SYNC Ø1
R54 1ØK +5V
DR Ø3 H BL2
7413 E24 7SNS
+3V
DR
MDET
D4-7 MDET Ø3 H
R55 1ØK
BV1
CLR FLAG Ø3 L
BP2
MDET Ø3 H
D4-1 1 SYNC Ø3
R56 1ØK +5V
7474 E27 RCV FLAG
D4-7 REC FLAG Ø3 H
D4-2 RESYNC PULSE Ø3 L DH2
D4-3 RX CLOCK Ø3 H CP2
D4-6 BUF LCR 13 H
D4-2 STROBE Ø3 H
D4-3 RX CLOCK Ø3 L
7417 E36
CR2
RESYNC 2 Ø3 (Ø) H
7474 E36 SEARCH SYNC
7474 E31 RESYNC
74H11 E34
CR2
RESYNC 1 Ø3 (Ø) H

(RECEIVERS Ø2 AND Ø3, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-7)
SIZE D CODE BS NUMBER DVII-Ø-10 REV A
SCALE SHEET 7 OF 8 DIST.

D4-7 RR6 Ø3
D4-7 RR6 Ø2
D4-6 RR6 Ø1
D4-6 RR6 ØØ
D4-7 RR5 Ø3
D4-7 RR5 Ø2
D4-6 RR5 Ø1
D4-6 RR5 ØØ
74153 E42
8881 E74
FR1 RECV DATA Ø5 L
FS1 RECV DATA Ø4 L

D4-7 PE Ø3
D4-7 PE Ø2
D4-6 PE Ø1
D4-6 PE ØØ
D4-7 OE Ø3
D4-7 OE Ø2
D4-6 OE Ø1
D4-6 OE ØØ
74153 E44
8881 E70
FM1 MASTER PE L
FL1 MASTER OR L

D4-7 RR4 Ø3
D4-7 RR4 Ø2
D4-6 RR4 Ø1
D4-6 RR4 ØØ
D4-7 RR3 Ø3
D4-7 RR3 Ø2
D4-6 RR3 Ø1
D4-6 RR3 ØØ
74153 E45
8881 E74
FN1 RECV DATA Ø3 L
FP1 RECV DATA Ø2 L

D3-3 CLEAR TMARK L FK2
74153 E76
FB3
FB2
FB1
FB0
FA3
FA2
FA1
FA0

D4-2 SET TMARK Ø3 L
D4-2 SET TMARK Ø2 L
D4-2 SET TMARK Ø1 L
D4-2 SET TMARK ØØ L
D4-2 RESET H
7474 E88 MARK Ø3
7474 E88 MARK Ø2
7474 E88 MARK Ø1
7474 E88 MARK ØØ
EB2 D4-8 TMARK Ø3 L
EL2 D4-8 TMARK Ø2 L
EB3 D4-8 TMARK Ø1 L
CD2 D4-8 TMARK ØØ L

D4-2 CARD FLAG SELECT ØØ-Ø3 L DM2

D4-7 RR2 Ø3
D4-7 RR2 Ø2
D4-6 RR2 Ø1
D4-6 RR2 ØØ
D4-7 RR1 Ø3
D4-7 RR1 Ø2
D4-6 RR1 Ø1
D4-6 RR1 ØØ
74153 E49
8881 E71
FN2 RECV DATA Ø1 L
FP2 RECV DATA ØØ L

D4-7 RR8 Ø7
D4-7 RR8 Ø2
D4-6 RR8 Ø1
D4-6 RR8 ØØ
D4-7 RR7 Ø3
D4-7 RR7 Ø2
D4-6 RR7 Ø1
D4-6 RR7 ØØ
74153 E36
8881 E78
FH1 RECV DATA Ø7 L
FJ1 RECV DATA Ø6 L

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D4-2 DATA ENABLE ØØ-Ø3 H (FK1)

(RECV DATA MUX S AND TMARK DECODER)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SYNC MUX LINE CARD LINES ØØ-Ø3 (04-8)	SIZE/CODE	NUMBER / REV.
		D BS	DVII-Ø-10 / A
SCALE	SHEET 8 OF 8	DIST.	

BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR Ø4
C	GROUND
D	DCE SCR Ø5
E	GROUND
F	DCE SCR Ø6
H	GROUND
J	DCE SCR Ø7
K	GROUND
L	EIA RCV DATA Ø1
M	GROUND
N	EIA RCV DATA Ø5
P	GROUND
R	EIA XMIT DATA Ø4
S	GROUND
T	EIA XMIT DATA Ø5
U	GROUND
V	DTE SCTE Ø4
W	GROUND
X	DTE SCTE Ø5
Y	DTE SCTE Ø6
Z	GROUND
A A	DTE SCTE Ø7
B B	GROUND
C C	EIA XMIT DATA Ø6
D D	GROUND
E E	EIA XMIT DATA Ø7
F F	GROUND
H H	EIA RCV DATA Ø6
J J	GROUND
K K	EIA RCV DATA Ø7
L L	GROUND
M M	DCE SCT Ø7
N N	GROUND
P P	DCE SCT Ø6
R R	GROUND
S S	DCE SCT Ø5
T T	GROUND
U U	DCE SCT Ø4
V V	GROUND

PARAMETER SWITCH SETTINGS

FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HDØ7	S2	5	ON		OFF	
	HDØ6	S2	6	ON		OFF	
	HDØ5	S2	7	ON		OFF	
	HDØ4	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY		EVEN PARITY
	PI	S1	1	OFF	ON		ON
	EPE	S1	2	OFF	ON		OFF
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC Ø4	S1	5	OFF		ON	
	1 SYNC Ø5	S1	6	OFF		ON	
	1 SYNC Ø6	S1	7	OFF		ON	
	1 SYNC Ø7	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1-8	OFF		ON	
LCR10=1	SYNC B	S3	1-8	OFF		ON	

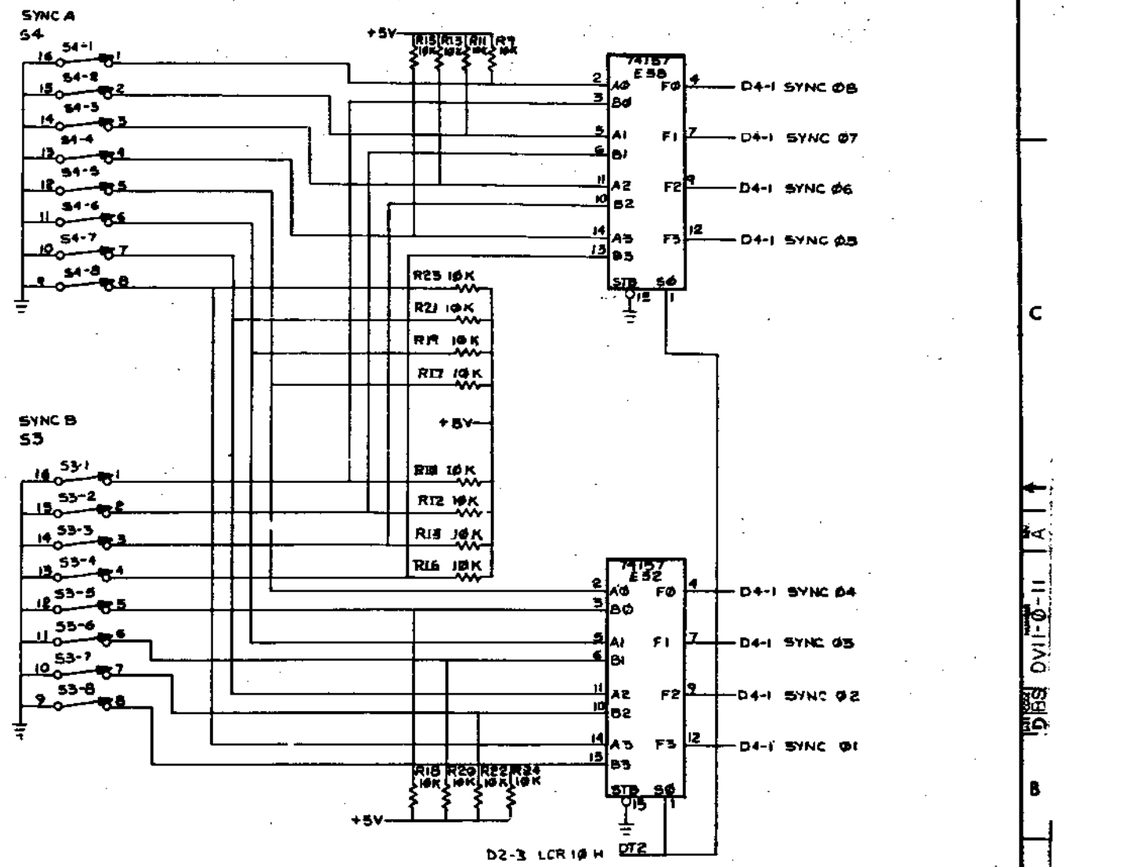
PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1 CS2	GROUND GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1 MS2	GROUND NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1 RMS2 RMS3	NO CONNECTION NO CONNECTION NO CONNECTION

S2
S2-1, S2-2 } UNUSED
S2-3 D4-1 SELECT B
S2-4 D4-1 SELECT A
S2-5 D4-1 HD Ø7
S2-6 D4-1 HD Ø6
S2-7 D4-1 HD Ø5
S2-8 D4-1 HD Ø4

S1
S1-1 D4-1 PI
S1-2 D4-1 EPE
S1-3 D4-1 WLS1
S1-4 D4-1 WLS2
S1-5 D4-1 1 SYNC Ø4
S1-6 D4-1 1 SYNC Ø5
S1-7 D4-1 1 SYNC Ø6
S1-8 D4-1 1 SYNC Ø7

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN BR1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA 08 H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.



REVISIONS		
CHK	CHANGE NO.	REV.
DC	DVII-00006	A
B Grasso 20 July 77	J McNAMARA	

(CHARTS SWITCHES AND SYNC SELECTOR)

DRN	4/77	FIRST USED ON: DVII
CHK	7/18/77	digital
ENG.		TITLE: SYNC MUX LINE CARD LINES Ø4 - Ø7 (D4-1)
PROJ. ENG.	4-17-78	
PROD.	4-17-78	
NEXT HIGHER ASSY.		B-DD-DVII-Ø
SCALE		SIZE D CODE 85 NUMBER DVII-Ø-11 REV. A
SHEET 1 OF 8		DIST.

DVII-Ø-11 A

D4-2 CARD PARAMETER SELECT Ø4-Ø7 L DM2

D3-8 SR5 Ø3 L BS2
D3-8 SR5 Ø2 H BE2
7486 E23

D2-3 CONTROL STROBE H CS2
7404 E41
D4-2 BUF CONTROL STROBE L

STB8 STB4 74153 E53

D4-2 STROBE Ø7 L
7404 E54
D4-2 STROBE Ø7 H

D4-2 STROBE Ø6 L
7404 E54
D4-2 STROBE Ø6 H

D4-2 STROBE Ø5 L
7404 E54
D4-2 STROBE Ø5 H

D4-2 STROBE Ø4 L
7404 E54
D4-2 STROBE Ø4 H

D3-7 INIT DI L EN2
7437 E63
D4-2 RESET H
7437 E63
D4-2 RESET A L
7437 E63
D4-2 RESET B L
+3V

D3-8 SR5 Ø1 H BT2
D3-8 SR5 Ø0 H BM2

D4-5 RCV IN Ø7 H
D4-5 RCV IN Ø6 H
D4-4 RCV IN Ø5 H
D4-4 RCV IN Ø4 H
74153 E22
8881 E67
FP1 BIT WINDOW L
BE2
D4-3 INTR MAINTENANCE Ø4-Ø7 H

D3-4 TRAN DATA Ø8 H ER1 (SEE NOTE 3 ON SHEET 1 OF 2)

D3-4 TRAN DATA Ø7 H EP1 7417 E61 D4-2 TR8 H
D3-4 TRAN DATA Ø6 H EM2 7417 E61 D4-2 TR7 H
D3-4 TRAN DATA Ø5 H FR2 7417 E76 D4-2 TR6 H
D3-4 TRAN DATA Ø4 H FV2 7417 E76 D4-2 TR5 H
D3-4 TRAN DATA Ø3 H FS2 7417 E76 D4-2 TR4 H
D3-4 TRAN DATA Ø2 H FV1 7417 E76 D4-2 TR3 H
D3-4 TRAN DATA Ø1 H FT2 7417 E76 D4-2 TR2 H
D3-4 TRAN DATA Ø0 H FU2 7417 E76 D4-2 TR1 H

D4-2 CARD FLAG SELECT Ø4-Ø7 L DM2

D3-4 MASTER SCAN D H EU2
D3-4 MASTER SCAN Ø2 H EN2
7437 E63
7404 E41
D3-3 RESYNC PULSE L DF2

STB8 STB4 74155 E47

D4-2 RESYNC PULSE Ø7 L
D4-2 RESYNC PULSE Ø6 L
D4-2 RESYNC PULSE Ø5 L
D4-2 RESYNC PULSE Ø4 L

D3-3 SET TMARK L CU2
7404 E41

D4-2 SET TMARK Ø7 L
D4-2 SET TMARK Ø6 L
D4-2 SET TMARK Ø5 L
D4-2 SET TMARK Ø4 L

D4-5 DA Ø7 H
D4-5 DA Ø6 H
D4-4 DA Ø5 H
D4-4 DA Ø4 H
D4-7 MDET Ø7 H
D4-7 MDET Ø6 H
D4-6 MDET Ø5 H
D4-6 MDET Ø4 H
74153 E62
8881 E67
FC1 DATA NOT AVAILABLE L
FE1 MATCH DETECT L

D1-5 RECEIVED DATA ENABLE H CN2
74H11 E39
FX1 D4-2 DATA ENABLE Ø4-Ø7 H

+5V
R25 10K
C96 68pf
7823 E75 RDE 3868MS
FU1 RDE Ø4-Ø7 H
+3V

STB8 STB4 74155 E57

D4-2 BUF RDE Ø7 L
D4-2 BUF RDE Ø6 L
D4-2 BUF RDE Ø5 L
D4-2 BUF RDE Ø4 L
D4-2 THRL Ø7 L
D4-2 THRL Ø6 L
D4-2 THRL Ø5 L
D4-2 THRL Ø4 L

D3-4 TRANSMITTER STROBE H EH2

D4-5 TRAN FLAG Ø7 H
D4-5 TRAN FLAG Ø6 H
D4-4 TRAN FLAG Ø5 H
D4-4 TRAN FLAG Ø4 H
D4-7 REC FLAG Ø7 H
D4-7 REC FLAG Ø6 H
D4-6 REC FLAG Ø5 H
D4-6 REC FLAG Ø4 H
74153 E48
8881 E71
FL2 TRAN FLAG WAITING L
FM2 RECEIVER FLAG L

+5V R26 1K
D3-4 MASTER SCAN Ø1 H EM1 V3 7417 E61
+5V R27 1K
D3-4 MASTER SCAN Ø0 H EN1 7417 E61

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN Ø0 H
D3-4 MASTER SCAN T/R CR2
7404 E41

(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SYNC MUX LINE CARD LINES Ø4-Ø7 (D4-2)	SIZE/CODE	NUMBER	REV.
		D BS	DVII-Ø-11	A
SCALE	SHEET 2 OF 8	DIST.		

DVII-Ø-11 DES A

NOTE 1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M7839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

REVISIONS		
CHK	CHANGE NO.	REV.

(CLOCK SOURCE AND SELECTION)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø4-Ø7 (D4-3)	D	BS	DV11-Ø-11	A
SCALE	SHEET 3 OF 8	DIST.		

D4-4 MODE Ø8 (8) H
D4-4 MODE Ø4(0) H
D4-3 ENTR MAINTENANCE Ø4-Ø1H
D4-4 MODE Ø1(1) H
D4-4 MODE Ø1(Ø) H
D4-4 TRANS DISABLE Ø4-Ø7 H
D4-4 BUF MODE Ø8(Ø) H
D4-4 RCV IN Ø4 H
D4-4 INTR RCV DATB Ø4-Ø7 L
EIA REC DATA Ø4
D2-3 LCR 14 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR Ø9 H
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT Ø4-Ø7 L
D4-2 BUF CONTROL STROBE L
AJ2 SERIAL OUT Ø4 L
D4-4 MODE Ø8 (1) H
EIA XMIT DATA Ø4
+5V -12V
D4-3 TMARK Ø4 L
D4-3 TX CLOCK Ø4 H
D4-2 RESET H
D4-2 THRL Ø4 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE Ø4 L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
SAT Ø4 E73
TCO Ø4 H
EOC Ø4 H
D4-4 DA Ø4 H
D4-4 TRAN FLAG Ø4 H
EIA REC DATA Ø5
D4-4 MODE Ø8 (0) H
D4-4 MODE Ø4 (1) H
D4-4 RCV IN Ø5 H
D4-4 TRANS DISABLE Ø4-Ø7 H
SERIAL OUT Ø5 L
D4-4 MODE Ø8Ø4 H
D4-4 BUF MODE Ø4(8) H
EIA XMIT DATA Ø5
D4-3 TX CLOCK Ø5 H
D4-2 THRL Ø5 L
D4-2 STROBE Ø5 L
D4-4 DA Ø5 H
D4-4 TRAN FLAG Ø5 H
SAT Ø5 E66
TCO Ø5 H
EOC Ø5 H
D4-4 DA Ø5 H
D4-4 TRAN FLAG Ø5 H

(MODE SELECTION, TRANSMITTERS Ø4 AND Ø5)

REVISIONS		
CHG	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD LINES Ø4 - Ø7 (D4-4)
SIZE D CODE BS NUMBER DV11-Ø-11 REV. A
SCALE — SHEET 4 OF 8 DIST.

EIA REC DATA Ø6 — J1 HH — 1489 E11 — C85 47Ø pf
D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9
D4-4 TRANS DISABLE Ø4-Ø7 H (AF2) — 7402 E12
7460 E23 — BK2 — D4-5 RCV IN Ø6 H
D4-4 INTR RCV DATA Ø4-Ø7 L — BC1
D4-4 BUF MODE ØØ (Ø) H — +5V R42 1K — 8242 E2 — 1488 E6 — J1 CC — EIA XMIT DATA Ø6
D4-4 MODE ØØ (1) H — 7402 E12 — 7404 E10 — AT2 — SERIAL OUT Ø6 L
EIA REC DATA Ø7 — J1 KK — 1489 E11 — C85 47Ø pf
D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9 — 7402 E3
7400 E23 — BK1 — D4-5 RCV IN Ø7 H
D4-4 BUF MODE ØØ (Ø) H — +5V R45 1K — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA Ø7
D4-4 MODE ØØ (1) H — 7402 E3
(AF2) D4-4 TRANS DISABLE Ø4-Ø7 H

+5V -12V — VSS VGG VDD — SAT Ø6 E59

D4-8 TMARK Ø6 L	EL2 17	CTS
D4-3 TX CLOCK Ø6 H	5	TRC
D4-2 RESET H	18	MR
	10	DAR
D4-2 THRL Ø6 L	19	THRL
D4-2 TR8 H	38	TR8
D4-2 TR7 H	36	TR7
D4-2 TR6 H	34	TR6
D4-2 TR5 H	32	TR5
D4-2 TR4 H	30	TR4
D4-2 TR3 H	28	TR3
D4-2 TR2 H	26	TR2
D4-2 TR1 H	24	TR1
D4-2 STROBE Ø6 L	22	FHRL
D4-1 SYNC Ø8	37	FR8
D4-1 SYNC Ø7	35	FR7
D4-1 SYNC Ø6	33	FR6
D4-1 SYNC Ø5	31	FR5
D4-1 SYNC Ø4	29	FR4
D4-1 SYNC Ø3	27	FR3
D4-1 SYNC Ø2	25	FR2
D4-1 SYNC Ø1	23	FR1
	4	CRL
	22	CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2

TRO	15	
TCO	11 EJ2	TCO Ø6 H
DD/ EOC	13 EK2	EOC Ø6 H
$\overline{DA}$	12	D4-5 $\overline{DA}$ Ø6 H
THRE	14	D4-5 TRAN FLAG Ø6 H

D4-1 PI, D4-1 EPE, D4-1 WLS1, D4-1 WLS2 — 3, 2, 39, 40

+5V -12V — VSS VGG VDD — SAT Ø7 E55

D4-8 TMARK Ø7 L	EE2 17	CTS
D4-3 TX CLOCK Ø7 H	5	TRC
D4-2 RESET H	18	MR
	10	DAR
D4-2 THRL Ø7 L	19	THRL
D4-2 TR8 H	38	TR8
D4-2 TR7 H	36	TR7
D4-2 TR6 H	34	TR6
D4-2 TR5 H	32	TR5
D4-2 TR4 H	30	TR4
D4-2 TR3 H	28	TR3
D4-2 TR2 H	26	TR2
D4-2 TR1 H	24	TR1
D4-2 STROBE Ø7 L	22	FHRL
D4-1 SYNC Ø8	37	FR8
D4-1 SYNC Ø7	35	FR7
D4-1 SYNC Ø6	33	FR6
D4-1 SYNC Ø5	31	FR5
D4-1 SYNC Ø4	29	FR4
D4-1 SYNC Ø3	27	FR3
D4-1 SYNC Ø2	25	FR2
D4-1 SYNC Ø1	23	FR1
	4	CRL
	22	CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2

TRO	15	
TCO	11 EDE	TCO Ø7 H
DD/ EOC	13 EFE	EOC Ø7 H
$\overline{DA}$	12	D4-5 $\overline{DA}$ Ø7 H
THRE	14	D4-5 TRAN FLAG Ø7 H

D4-1 PI, D4-1 EPE, D4-1 WLS1, D4-1 WLS2 — 3, 2, 39, 40

7404 E10 — AH2. — SERIAL OUT Ø7 L

REVISIONS		
CHK	CHANGE NO.	REV.

(TRANSMITTERS Ø6 AND Ø7)

TITLE	SYNC MUX LINE CARD LINES Ø4-Ø7 (D4-5)	SIZE/CODE	NUMBER
SCALE	SHEET 5 OF 8	D DBS	DVII-Ø-II
	DIST.		REV. A

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø4 H DE2 31 RRC
D4-4 RCV IN Ø4 H BE2 35 RI
D4-2 RESET H 32 MR
SAR Ø4 E50
RR9 7
RR8 8 D4-6 RR8 Ø4
RR7 9 D4-6 RR7 Ø4
RR6 10 D4-6 RR6 Ø4
RR5 11 D4-6 RR5 Ø4
RR4 12 D4-6 RR4 Ø4
RR3 13 D4-6 RR3 Ø4
RR2 14 D4-6 RR2 Ø4
RR1 15 D4-6 RR1 Ø4
PE 29 D4-6 PE Ø4
OE 27 D4-6 OE Ø4
CLR FLAG Ø4 L BV2
D4-2 BUF RDE Ø4 L
7408 E58
SFR 24
DRR 25
CV2
RESYNC 1 Ø: (Ø) H
D4-2 STROBE Ø4 L 39 MHRL
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
CRL 33
CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
+5V R47 10K
7408 E18
AR2
DR Ø4 H
7474 E28 RCV FLAG
CLR FLAG Ø4 L
D4-6 REC FLAG Ø4 H
DR 26
D4-6 MDET Ø4 H
MDET 30
7400 E18
4V2
MDET Ø4 H
74123 E19 74LS
R46 10K
D4-1 1 SYNC Ø4
D4-6 BUF LCR 15 H
D4-2 RESYNC PULSE Ø4 L DL2
D2-3 LCR 15 H BA1
7417 E30
R44 1K
D4-2 STROBE Ø4 H
7474 E68 SEARCH SYNC
D4-3 RX CLOCK Ø4 H DE2
DD2 RESYNC 2 Ø4 (Ø) H
D4-3 RX CLOCK Ø4 L
7474 E38 RESYNC
7411 E39
CV2
RESYNC 1 Ø4 (Ø) H
D4-2 RESET A L

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø5 H CE2 31 RRC
D4-4 RCV IN Ø5 H BD1 35 RI
D4-2 RESET H 32 MR
SAR Ø5 E37
RR9 7
RR8 8 D4-6 RR8 Ø5
RR7 9 D4-6 RR7 Ø5
RR6 10 D4-6 RR6 Ø5
RR5 11 D4-6 RR5 Ø5
RR4 12 D4-6 RR4 Ø5
RR3 13 D4-6 RR3 Ø5
RR2 14 D4-6 RR2 Ø5
RR1 15 D4-6 RR1 Ø5
PE 29 D4-6 PE Ø5
OE 27 D4-6 OE Ø5
CLR FLAG Ø5 L BF1
D4-2 BUF RDE Ø5 L
RESYNC 1 Ø5 (Ø) H BH2
7408 E18
SFR 24
DRR 25
D4-2 STROBE Ø5 L 39 MHRL
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
CRL 33
CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
+5V R48 10K
7408 E19
AU2
DR Ø5 H
DR 26
D4-6 REC FLAG Ø5 H
7474 E68 RCV FLAG
CLR FLAG Ø5 L
D4-6 MDET Ø5 H
MDET 30
7408 E35
74123 E19 74LS
R49 10K
BH1
MDET Ø5 H
D4-1 1 SYNC Ø5
D4-2 RESYNC PULSE Ø5 L DK2
D4-6 BUF LCR 15 H
D4-2 STROBE Ø5 H
7474 E68 SEARCH SYNC
D4-3 RX CLOCK Ø5 H CE2
CF2 RESYNC 2 Ø5 (Ø) H
D4-3 RX CLOCK Ø5 L
7474 E38 RESYNC
7411 E34
BH2
RESYNC 1 Ø5 (Ø) H

(RECEIVERS Ø4 AND Ø5, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES Ø4 - Ø7 (D4 - 6)		SIZE D	CODE BS	NUMBER DVII-Ø-11
SCALE	SHEET 6 OF 8	DIST.		REV. A

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø6 H DS2 31 RRC
D4-5 RCV IN Ø6 H BX2 35 RI
D4-2 RESET H 32 MR
SAR Ø6 E46
CLR FLAG Ø6 L BU2
D4-2 BUF RDE Ø6 L
7408 E29
SFR 24
DRR 25
DN2
D4-2 STROBE Ø6 L
RESYNC 1 Ø6 (Ø) H
MHRL 34
D4-1 SYNC Ø8 MHR8 40
D4-1 SYNC Ø7 MHR7 4
D4-1 SYNC Ø6 MHR6 38
D4-1 SYNC Ø5 MHR5 3
D4-1 SYNC Ø4 MHR4 36
D4-1 SYNC Ø3 MHR3 17
D4-1 SYNC Ø2 MHR2 22
D4-1 SYNC Ø1 MHR1 18
CRL 33
CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
RR9 7
RR8 8 D4-7 RR8 Ø6
RR7 9 D4-7 RR7 Ø6
RR6 10 D4-7 RR6 Ø6
RR5 11 D4-7 RR5 Ø6
RR4 12 D4-7 RR4 Ø6
RR3 13 D4-7 RR3 Ø6
RR2 14 D4-7 RR2 Ø6
RR1 15 D4-7 RR1 Ø6
PE 29 D4-7 PE Ø6
OE 27 D4-7 OE Ø6
DR 26
+5V
RSI 10K
7403 E28
7SNS
BB1
DR Ø6 H
+3V
7408 E29
D4-7 REC FLAG Ø6 H
7474 E27 RCV FLAG
CLR FLAG Ø6 L
D4-7 MDET Ø6 H
MDET 30
+5V
R52 10K
7408 E29
74123 E28 7SNS
BB2
MDET Ø6 H
R53 10K
+5V
D4-1 1 SYNC Ø6
D4-2 RESYNC PULSE Ø6 L DJ2
7417 E36
DR8
RESYNC 2 Ø6 (Ø) H
+3V
D4-6 BUF LCR 15H
D4-2 STROBE Ø6 H
7474 E56
D4-3 RX CLOCK Ø6 H DS2
7408 E29
7474 E51 RESYNC
D4-3 RX CLOCK Ø6 L
7474 E51 SYNC
7411 E54
DN2
RESYNC 1 Ø6 (Ø) H
D4-2 RESET B L

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK Ø7 H CP2 31 RRC
D4-5 RCV IN Ø7 H BX1 35 RI
D4-2 RESET H 32 MR
SAR Ø7 E40
CLR FLAG Ø7 L BV1
D4-2 BUF RDE Ø7 L
7408 E31
SFR 24
DRR 25
CK2
RESYNC 1 Ø7 (Ø) H
D4-2 STROBE Ø7 L
MHRL 34
D4-1 SYNC Ø8 MHR8 40
D4-1 SYNC Ø7 MHR7 4
D4-1 SYNC Ø6 MHR6 38
D4-1 SYNC Ø5 MHR5 3
D4-1 SYNC Ø4 MHR4 36
D4-1 SYNC Ø3 MHR3 17
D4-1 SYNC Ø2 MHR2 22
D4-1 SYNC Ø1 MHR1 18
CRL 33
CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
RR9 7
RR8 8 D4-7 RR8 Ø7
RR7 9 D4-7 RR7 Ø7
RR6 10 D4-7 RR6 Ø7
RR5 11 D4-7 RR5 Ø7
RR4 12 D4-7 RR4 Ø7
RR3 13 D4-7 RR3 Ø7
RR2 14 D4-7 RR2 Ø7
RR1 15 D4-7 RR1 Ø7
PE 29 D4-7 PE Ø7
OE 27 D4-7 OE Ø7
DR 26
+5V
R54 10K
7403 E24
7SNS
BL2
DR Ø7 H
+3V
7408 E31
D4-7 REC FLAG Ø7 H
7474 E27 RCV FLAG
BV1
CLR FLAG Ø7 L
D4-7 MDET Ø7 H
MDET 30
7408 E31
74123 E24 7SNS
BP2
MDET Ø7 H
R56 10K
+5V
D4-1 1 SYNC Ø7
D4-2 RESYNC PULSE Ø7 L DH2
7417 E36
CK2
RESYNC 2 Ø7 (Ø) H
+3V
D4-6 BUF LCR 15H
D4-2 STROBE Ø7 H
7474 E56
D4-3 RX CLOCK Ø7 H CP2
7408 E31
7474 E58 RESYNC
D4-3 RX CLOCK Ø7 L
7474 E58 SYNC
7411 E54
CK2
RESYNC 1 Ø7 (Ø) H

REVISIONS		
CHK	CHANGE NO.	REV.

(RECEIVERS Ø6 AND Ø7, RESYNC)

TITLE: SYNC MUX LINE CARD LINES Ø4-Ø7 (D4-7)	SIZE D	CODE BS	NUMBER DVII-Ø-11	REV. A
SCALE	SHEET 7 OF 8	DIST.		

D4-7 RR6 Ø7
D4-7 RR6 Ø6
D4-6 RR6 Ø5
D4-6 RR6 Ø4
D4-7 RR5 Ø7
D4-7 RR5 Ø6
D4-6 RR5 Ø5
D4-6 RR5 Ø4
74153 E42
8881 E74 → FR1 RECV DATA Ø5 L
8881 E74 → FS1 RECV DATA Ø4 L

D4-7 PE Ø7
D4-7 PE Ø6
D4-6 PE Ø5
D4-6 PE Ø4
D4-7 OE Ø7
D4-7 OE Ø6
D4-6 OE Ø5
D4-6 OE Ø4
74153 E44
8881 E78 → FM1 MASTER PE L
8881 E78 → FL1 MASTER OR L

D4-7 RR4 Ø7
D4-7 RR4 Ø6
D4-6 RR4 Ø5
D4-6 RR4 Ø4
D4-7 RR3 Ø7
D4-7 RR3 Ø6
D4-6 RR3 Ø5
D4-6 RR3 Ø4
74153 E45
8881 E74 → FN1 RECV DATA Ø3 L
8881 E74 → FP1 RECV DATA Ø2 L

D3-3 CLEAR TMARK L FK2 15
74155 E76 FB3 FB2 FB1 FB0 FA3 FA2 FA1 FA0
D4-2 SET TMARK Ø7 L
D4-2 SET TMARK Ø6 L
D4-2 SET TMARK Ø5 L
D4-2 SET TMARK Ø4 L
D4-2 RESET H
7474 E69 MARK Ø7 → EE2 D4-8 TMARK Ø7 L
7474 E69 MARK Ø6 → EL2 D4-8 TMARK Ø6 L
7474 E65 MARK Ø5 → CB2 D4-8 TMARK Ø5 L
7474 E65 MARK Ø4 → CD2 D4-8 TMARK Ø4 L

D4-2 CARD FLAG SELECT Ø4-Ø7 L DM2
D4-7 RR2 Ø7
D4-7 RR2 Ø6
D4-6 RR2 Ø5
D4-6 RR2 Ø4
D4-7 RR1 Ø7
D4-7 RR1 Ø6
D4-6 RR1 Ø5
D4-6 RR1 Ø4
74153 E49
8881 E71 → FN2 RECV DATA Ø1 L
8881 E71 → FP2 RECV DATA Ø0 L

D4-7 RR8 Ø7
D4-7 RR8 Ø6
D4-6 RR8 Ø5
D4-6 RR8 Ø4
D4-7 RR7 Ø7
D4-7 RR7 Ø6
D4-6 RR7 Ø5
D4-6 RR7 Ø4
74153 E36
8881 E78 → FH1 RECV DATA Ø7 L
8881 E78 → FJ1 RECV DATA Ø6 L

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D4-2 DATA ENABLE Ø4 Ø7 H (FK1)

REVISIONS
CHK | CHANGE NO. | REV.

(RECV DATA MUX S AND TMARK DECODER)

TITLE SYNC MUX LINE CARD LINES Ø4 - Ø7 D4 - 8
SIZE D | CODE BS | NUMBER DVII-Ø-11 | REV. A
SCALE | SHEET 8 OF 8 | DIST

DVII-Ø-11 A

BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR Ø8
C	GROUND
D	DCE SCR Ø9
E	GROUND
F	DCE SCR 1Ø
H	GROUND
J	DCE SCR 11
K	GROUND
L	EIA RCV DATA Ø8
M	GROUND
N	EIA RCV DATA Ø9
P	GROUND
R	EIA XMIT DATA Ø8
S	GROUND
T	EIA XMIT DATA Ø9
U	GROUND
V	DTE SCTE Ø8
W	GROUND
X	DTE SCTE Ø9
Y	DTE SCTE 1Ø
Z	GROUND
A A	DTE SCTE 11
B B	GROUND
C C	EIA XMIT DATA 1Ø
D D	GROUND
E E	EIA XMIT DATA 11
F F	GROUND
H H	EIA RCV DATA 1Ø
J J	GROUND
K K	EIA RCV DATA 11
L L	GROUND
M M	DCE SCT 11
N N	GROUND
P P	DCE SCT 1Ø
R R	GROUND
S S	DCE SCT Ø9
T T	GROUND
U U	DCE SCT Ø8
V V	GROUND

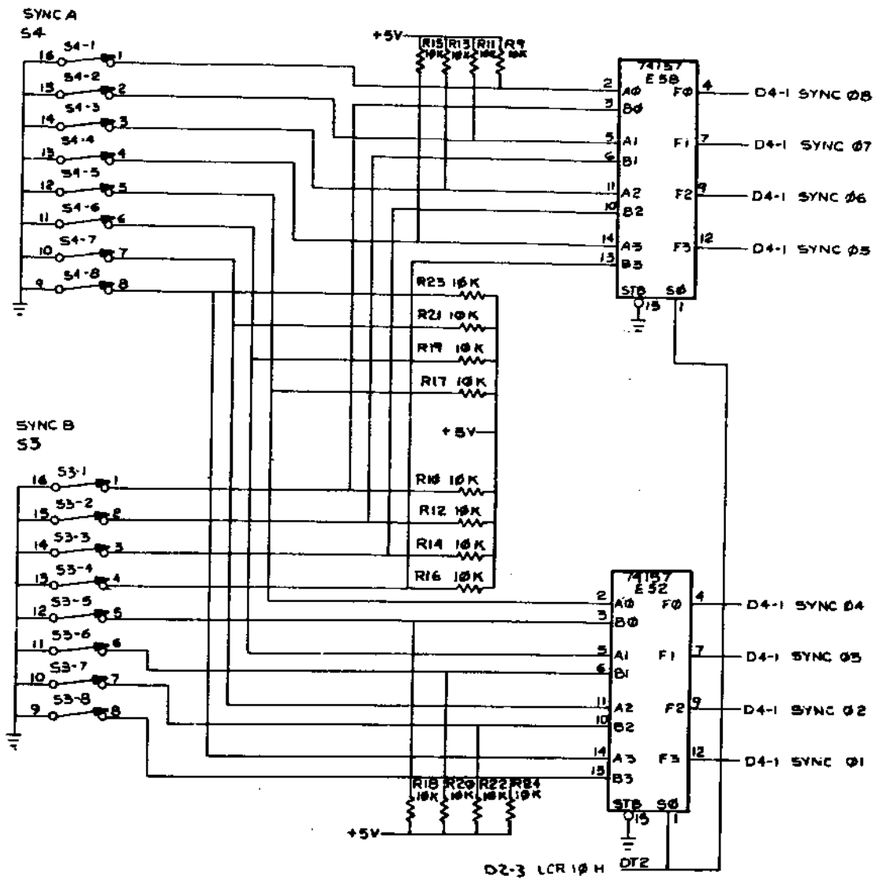
PARAMETER SWITCH SETTINGS

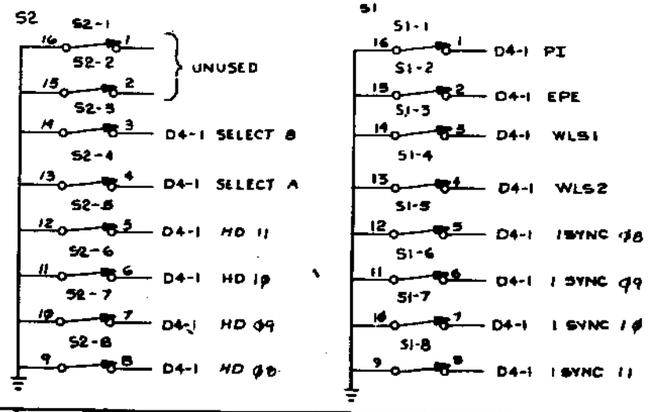
FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HDX1	S2	5	ON		OFF	
	HDØ2	S2	6	ON		OFF	
	HDØ9	S2	7	ON		OFF	
	HDØ8	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC Ø8	S1	5	OFF		ON	
	1 SYNC Ø9	S1	6	OFF		ON	
	1 SYNC 1Ø	S1	7	OFF		ON	
	1 SYNC 11	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1 thru 8	OFF		ON	
LCR10=1	SYNC B	S3	1 thru 8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1	GROUND
	CS2	GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1	GROUND
	MS2	NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1	NO CONNECTION
	RMS2	NO CONNECTION
	RMS3	NO CONNECTION

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL. TRAN DATA Ø8 H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.





D3-5 230.4 KB H BM1
(SEE NOTE 4)

(CHARTS, SWITCHES AND SYNC SELECTOR)

REVISIONS		
CHK	CHANGE NO.	REV.
J M	DVII-00006	A
J MCNAMARA		

DRW		FIRST USED ON: DVII
CHK		digital
ENG.		TITLE: SYNC MUX LINE CARD LINES Ø8 -11
PROJ. ENG.		
PROD.		
NEXT HIGHER ASSY.	B-DD-DVII-Ø	SIZE: D CODE: BS NUMBER: DVII-Ø-12 REV: A
SCALE		
SHEET 1 OF 8		DIST.

DVII-Ø-12 A

D4-2 CARD PARAMETER SELECT Ø8-11 L DM2

D3-8 SRS Ø3 H BS2 — 74Ø4 B25
D3-8 SRS Ø2 L BR2

D2-3 CONTROL STROBE H CS2 11 — 7404 E41 — D4-2 BUF CONTROL STROBE L

D3-7 INIT DI L BN2 9 — 7437 E43
D4-2 RESET H
7437 E43 — D4-2 RESET A L
7437 E43 — D4-2 RESET B L
+3V

D4-2 STROBE 11 L
D4-2 STROBE 1Ø L
D4-2 STROBE Ø9 L
D4-2 STROBE Ø8 L
7404 E54 — D4-2 STROBE 11 H
7404 E54 — D4-2 STROBE 1Ø H
7404 E54 — D4-2 STROBE Ø9 H
7404 E54 — D4-2 STROBE Ø8 H

D3-8 SRS Ø1 H BT2
D3-8 SRS Ø4 H BM2

D4-5 RCV IN 11 H
D4-5 RCV IN 1Ø H
D4-4 RCV IN Ø9 H
D4-4 RCV IN Ø8 H
74153 E32 — 8881 E47 — FR1 — BIT WINDOW L
BE2
D4-3 INTR MAINTENANCE Ø8-11 H

D3-4 TRAN DATA Ø8 H ER1 (SEE NOTE 3 ON SHEET 1 OF 8)

D3-4 TRAN DATA Ø7 H EM1 — 7417 E61 — D4-2 TR8 H
D3-4 TRAN DATA Ø6 H EM2 — 7417 E61 — D4-2 TR7 H
D3-4 TRAN DATA Ø5 H FR2 13 — 7417 E76 — D4-2 TR6 H
D3-4 TRAN DATA Ø4 H FV2 — 7417 E76 — D4-2 TR5 H
D3-4 TRAN DATA Ø3 H FS2 11 — 7417 E76 — D4-2 TR4 H
D3-4 TRAN DATA Ø2 H FV1 — 7417 E76 — D4-2 TR3 H
D3-4 TRAN DATA Ø1 H FT2 9 — 7417 E76 — D4-2 TR2 H
D3-4 TRAN DATA Ø0 H FU2 — 7417 E76 — D4-2 TR1 H

D4-2 CARD FLAG SELECT Ø8-11 L DM2

D3-4 MASTER SCAN Ø3 H BU2 12 — 7437 E43
D3-4 MASTER SCAN C H BN2 13

D3-3 RESYNC PULSE L DF2 — 7404 E41
D4-2 RESYNC PULSE 11 L
D4-2 RESYNC PULSE 1Ø L
D4-2 RESYNC PULSE Ø9 L
D4-2 RESYNC PULSE Ø8 L

D3-3 SET TMARK L CU2 — 7404 E41
D4-2 SET TMARK 11 L
D4-2 SET TMARK 1Ø L
D4-2 SET TMARK Ø9 L
D4-2 SET TMARK Ø8 L

D4-5 DA 11 H
D4-5 DA 1Ø H
D4-4 DA Ø9 H
D4-4 DA Ø8 H
74153 E62 — 8881 E47 — FC1 — DATA NOT AVAILABLE L

D4-7 MDET 11 H
D4-7 MDET 1Ø H
D4-6 MDET Ø9 H
D4-6 MDET Ø8 H
74153 E62 — 8881 E47 — FR1 — MATCH DETECT L

D1-5 RECEIVED DATA ENABLE H CN2 — 74H11 E34 — FK1 — D4-2 DATA ENABLE Ø8-11 H
+5V — R25 1ØK — C96 68pf — 74123 E75 — FU1 — EDE Ø8-11 H — +5V

D3-9 TRANSMITTER STROBE H EH2

D4-2 BUF RDE 11 L
D4-2 BUF RDE 1Ø L
D4-2 BUF RDE Ø9 L
D4-2 BUF RDE Ø8 L
D4-2 TMRL 11 L
D4-2 TMRL 1Ø L
D4-2 TMRL Ø9 L
D4-2 TMRL Ø8 L

D4-5 TRAN FLAG 11 H
D4-5 TRAN FLAG 1Ø H
D4-4 TRAN FLAG Ø9 H
D4-4 TRAN FLAG Ø8 H
D4-7 REC FLAG 11 H
D4-7 REC FLAG 1Ø H
D4-6 REC FLAG Ø9 H
D4-6 REC FLAG Ø8 H
74153 E40 — 8881 E71 — FL2 — TRAN FLAG WAITING L
8881 E71 — FM2 — RECEIVER FLAG L

+5V — R26 1K — D3-9 MASTER SCAN Ø1 H EM1 — 7417 E61
+5V — R27 1K — D3-9 MASTER SCAN Ø0 H EM1 — 7417 E61

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN Ø0 H
D3-4 MASTER SCAN T/R CR2 13 — 7404 E41 — 12

(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES Ø8-11 (D4-2)
SIZE D | CODE BS | NUMBER DV11-Ø-12 | REV. A
SCALE | SHEET 2 OF 8 | DWG.

DIGITAL DBS DV11-Ø-12 A

NOTE 1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M7839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

(CLOCK SOURCE AND SELECTION)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES Ø8-11 (04-3) | SIZE D | CODE BS | NUMBER DV11-Ø-12 | REV. A | SCALE | SHEET 3 OF 8 | DIST.

D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ(1) H
D4-4 RCV IN ØØ H
D4-4 INTR RCV DATA ØØ-11 L
D4-3 INTR MAINTENANCE Ø8-11 H
D4-4 MODE Ø1(Ø) H
D4-4 MODE Ø1(1) H
D4-4 TRANS DISABLE Ø8-11 H
D4-4 BUF MODE ØØ(Ø) H
D4-4 BUF MODE ØØ(1) H
EIA XMIT DATA Ø8
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT Ø8-11 L
D4-2 BUF CONTROL STROBE L
AJ2 SERIAL OUT Ø8 L
D4-4 MODE Ø0 (1) H
SAT Ø8 E73
D4-8 TMARK Ø8 L
D4-3 TX CLOCK Ø8 H
D4-2 RESET H
D4-2 THRL Ø8 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE Ø8 L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TCO Ø8 H
EOC Ø8 H
D4-4 SA Ø8 H
D4-4 TRAN FLAG Ø8 H
EIA REC DATA Ø9
D4-4 TRANS DISABLE Ø8-11 H
SERIAL OUT Ø9 L
D4-4 MODE ØØ(Ø) H
D4-4 BUF MODE ØØ(1) H
EIA XMIT DATA Ø9
SAT Ø9 E66
D4-8 TMARK Ø9 L
D4-3 TX CLOCK Ø9 H
D4-2 RESET H
D4-2 THRL Ø9 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE Ø9 L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TCO Ø9 H
EOC Ø9 H
D4-4 SA Ø9 H
D4-4 TRAN FLAG Ø9 H
BD1 D4-4 RCV EN Ø9 H

REVISIONS
CHK | CHANGE NO. | REV.

(MODE SELECTION, TRANSMITTERS Ø8 AND Ø9)

TITLE SYNC MUX LINE CARD LINES Ø8-11 (D4-4)
SIZE D | CODE 85 | NUMBER DVII-Ø-12 | REV. A
SCALE | SHEET 4 OF 8 | DIST.

DVII-Ø-12

EIA REC DATA /Ø — J1 MM — 1488 E11 — C88 47Ø pf

D4-4 MODE ØØ (Ø) H — 9 — 1Ø
D4-4 MODE ØØ (1) H — 13 — 1
7450 E29 — 8
7400 E25 — 8 — BK2 — D4-5 RCV IN /Ø H

D4-4 TRANS DISABLE ØB-11 H (AF2) — 8 — 7402 E12 — 1 — 3

D4-4 INTR RCV DATA ØB-11 L — BC1
+5V — R42 1K
D4-4 BUF MODE ØØ(Ø)H — 5 — 6 — 8242 E2 — 4 — 12 — 13 — 1488 E6 — 11 — J1 CC — EIA XMIT DATA /Ø
D4-4 MODE ØØ (1) H — 12 — 11 — 7402 E12 — 13
7400 E10 — 5 — 6 — AT2 — SERIAL OUT /Ø L

EIA REC DATA // — J1 KK — 1488 E11 — C85 47Ø pf — 8
D4-4 MODE ØØ (Ø) H — 2 — 3
D4-4 MODE ØØ (1) H — 4 — 7450 E9 — 6
7400 E23 — 13 — 12 — 11 — BK1 — D4-5 RCV IN // H
7402 E5 — 6 — 5 — 4 — (AF2) — D4-4 TRANS DISABLE ØB-11 H
D4-4 MODE ØØ(1)H — 9 — 8 — 7402 E3 — Ø
D4-4 BUF MODE ØØ (Ø) H — 1 — 2 — 8242 E2 — 3 — +5V R43 1K — 12 — 13 — 1488 E26 — 11 — J1 EE — EIA XMIT DATA //

+5 / -12V — 1 — 16 — 21 — VSS VGG VDD

D4-8 TMARK /Ø L — EE2 17 — CTS
D4-3 TX CLOCK /ØH — 5 — TRC
D4-2 RESET H — 18 — MR
10 — DAR
D4-2 THRL /Ø L — 19 — THRL
D4-2 TRB H — 38 — TRB
D4-2 TR7 H — 36 — TR7
D4-2 TR6 H — 34 — TR6
D4-2 TR5 H — 32 — TR5
D4-2 TR4 H — 30 — TR4
D4-2 TR3 H — 28 — TR3
D4-2 TR2 H — 26 — TR2
D4-2 TR1 H — 24 — TR1
D4-2 STROBE /Ø L — 20 — FHRL
D4-1 SYNC ØB — 37 — FR8
D4-1 SYNC Ø7 — 35 — FR7
D4-1 SYNC Ø6 — 33 — FR6
D4-1 SYNC Ø5 — 31 — FR5
D4-1 SYNC Ø4 — 29 — FR4
D4-1 SYNC Ø3 — 27 — FR3
D4-1 SYNC Ø2 — 25 — FR2
D4-1 SYNC Ø1 — 23 — FR1
4 — CRL
22 — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO — 15 — TCO /Ø H
11 EJ2 — TCO /Ø H
DD/ EOC — 13 EK2 — EOC /Ø H
OA — 12 — D4-5 OA /Ø H
THRE — 14 — D4-5 TRAN FLAG /Ø H

+5V -12V — 1 — 16 — 21 — VSS VGG VDD

D4-8 TMARK // L — EE2 17 — CTS
D4-3 TX CLOCK // H — 5 — TRC
D4-2 RESET H — 18 — MR
10 — DAR
D4-2 THRL // L — 19 — THRL
D4-2 TRB H — 38 — TRB
D4-2 TR7 H — 36 — TR7
D4-2 TR6 H — 34 — TR6
D4-2 TR5 H — 32 — TR5
D4-2 TR4 H — 30 — TR4
D4-2 TR3 H — 28 — TR3
D4-2 TR2 H — 26 — TR2
D4-2 TR1 H — 24 — TR1
D4-2 STROBE // L — 20 — FHRL
D4-1 SYNC ØB — 37 — FR8
D4-1 SYNC Ø7 — 35 — FR7
D4-1 SYNC Ø6 — 33 — FR6
D4-1 SYNC Ø5 — 31 — FR5
D4-1 SYNC Ø4 — 29 — FR4
D4-1 SYNC Ø3 — 27 — FR3
D4-1 SYNC Ø2 — 25 — FR2
D4-1 SYNC Ø1 — 23 — FR1
4 — CRL
22 — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO — 15 — 7404 E10Ø — 8 — AN2 — SERIAL OUT // L
TCO — 11 EDZ — TCO // H
DD/EOC — 13 EF2 — EOC // H
OA — 12 — D4-5 OA // H
THRE — 14 — D4-5 TRAN FLAG // H

(TRANSMITTERS /Ø AND //)

REVISIONS		
CHG	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES ØB-11 (U4-5)	D	BS	DV11-Ø-12	A
SCALE	SHEET 5 OF 8		DWG.	

DBS DV11-Ø-12 A

+5V -12V VSS VGG VDD

D4-3 RX CLOCK Ø8 H — CE2 31 — RRC
D4-4 RCV IN Ø8 H — DE2 35 — RI
D4-2 RESET H — 32 — MR
SAR Ø8 E50

CLR FLAG Ø8 L — BV2
D4-2 BUF RDE Ø8 L — 74Ø8 E5B — 24 SFR, 25 DRR
CVE — D4-2 STROBE Ø8 L — 34 MHRL
RESYNC 1 Ø8 (Ø) H

D4-1 SYNC Ø8 — 46 MHR8
D4-1 SYNC Ø7 — 4 MHR7
D4-1 SYNC Ø6 — 38 MHR6
D4-1 SYNC Ø5 — 3 MHR5
D4-1 SYNC Ø4 — 36 MHR4
D4-1 SYNC Ø3 — 17 MHR3
D4-1 SYNC Ø2 — 22 MHR2
D4-1 SYNC Ø1 — 18 MHR1
33 CRL
6 CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
D4-1 PI — 19
D4-1 EPE — 21
D4-1 WLS1 — 5
D4-1 WLS2 — 23

RR9 7
RR8 8 — D4-6 RR8 Ø8
RR7 9 — D4-6 RR7 Ø8
RR6 10 — D4-6 RR6 Ø8
RR5 11 — D4-6 RR5 Ø8
RR4 12 — D4-6 RR4 Ø8
RR3 13 — D4-6 RR3 Ø8
RR2 14 — D4-6 RR2 Ø8
RR1 15 — D4-6 RR1 Ø8
PE 29 — D4-6 PE Ø8
OE 37 — D4-6 OE Ø8
DR 26

+5V R47 1K
D4-2 BUF LCR 13 H — BAI — 7417 E3B — 8
+5V R44 1K
D4-2 STROBE Ø8 H — 5 — 7474 E6B SEARCH SYNC
D4-2 RESYNC PULSE Ø8 L — DL2
D4-3 RX CLOCK Ø8 H — DE2
D4-3 RX CLOCK Ø8 L — 7408 E3B — 7474 E2B RESYNC — 7411 E3B — 8
CVE RESYNC 1 Ø8 (Ø) H
7417 E3B — DDR RESYNC 2 Ø8 (Ø) H

DR Ø8 H — AR2 — 74123 E14 75NS — R97 10K +5V
MDET — 30 — 7408 E18 — R46 10K +5V — AV2 — MDET Ø8 H
D4-1 I SYNC Ø8 — R98 10K +5V
D4-6 MDET Ø8 H
D4-6 REC FLAG Ø8 H
7474 E2B REV FLAG — BV2 — CLR FLAG Ø8 L

D4-2 RESET A L

+5V -12V VSS VGG VDD

D4-3 RX CLOCK Ø9 H — CE2 31 — RRC
D4-4 RCV IN Ø9 H — DE1 35 — RI
D4-2 RESET H — 32 — MR
SAR Ø9 E37

CLR FLAG Ø9 L — BF1
D4-2 BUF RDE Ø9 L — 74Ø8 E1B — 24 SFR, 25 DRR
RESYNC 1 Ø9 (Ø) H — BH2 — D4-2 STROBE Ø9 L — 34 MHRL

D4-1 SYNC Ø8 — 46 MHR8
D4-1 SYNC Ø7 — 4 MHR7
D4-1 SYNC Ø6 — 38 MHR6
D4-1 SYNC Ø5 — 3 MHR5
D4-1 SYNC Ø4 — 36 MHR4
D4-1 SYNC Ø3 — 17 MHR3
D4-1 SYNC Ø2 — 22 MHR2
D4-1 SYNC Ø1 — 18 MHR1
33 CRL
6 CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
D4-1 PI — 19
D4-1 EPE — 21
D4-1 WLS1 — 5
D4-1 WLS2 — 23

RR9 7
RR8 8 — D4-6 RR8 Ø9
RR7 9 — D4-6 RR7 Ø9
RR6 10 — D4-6 RR6 Ø9
RR5 11 — D4-6 RR5 Ø9
RR4 12 — D4-6 RR4 Ø9
RR3 13 — D4-6 RR3 Ø9
RR2 14 — D4-6 RR2 Ø9
RR1 15 — D4-6 RR1 Ø9
PE 29 — D4-6 PE Ø9
OE 37 — D4-6 OE Ø9
DR 26

+5V R46 1K
DR Ø9 H — AU2 — 74123 E19 75NS — R47 10K +5V
MDET — 30 — 7408 E3B — 7474 E2B REV FLAG — BF1 — CLR FLAG Ø9 L
BH1 — MDET Ø9 H
D4-1 I SYNC Ø9 — R86 10K +5V
D4-6 MDET Ø9 H
D4-6 REC FLAG Ø9 H

D4-6 BUF LCR 13 H — 7474 E6B SEARCH SYNC
D4-2 STROBE Ø9 H — 15
D4-2 RESYNC PULSE Ø9 L — DK2
D4-3 RX CLOCK Ø9 H — CE2
D4-3 RX CLOCK Ø9 L — 7408 E3B — 7474 E2B RESYNC — 7411 E3B — 12
BH2 RESYNC 1 Ø9 (Ø) H
7417 E3B — CE2 RESYNC 2 Ø9 (Ø) H

REVISIONS		
CHK	CHANGE NO.	REV.

(RECEIVERS Ø8 AND Ø9, RESYNC)

TITLE SYNC MUX LINE CARD LINES Ø8 12 (D4-6)				
SCALE	SHEET 6 OF 8	SIZE D	CODE BS	NUMBER DVII-Ø-12 REV. A
		DIST		

DIGITAL EQUIPMENT CORP. MAYNARD, MASS.

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK 10 H DS2 31
D4-5 RCV IN 10 H BK1 35
D4-2 RESET H 32
SAR 10 E46
RRC RI MR
RR9 RR8 RR7 RR6 RR5 RR4 RR3 RR2 RR1 PE OE
D4-7 RR8 10 … D4-7 RR1 10
D4-7 PE 10
D4-7 OE 10
CLR FLAG 10 L
D4-2 BUF RDE 10 L
BU2
7408 E29
SFR DRR MHRL
DN2
D4-2 STROBE 10 L
RESYNC 1 10 (Ø) H
D4-1 SYNC Ø8 … Ø1
MHR8 MHR7 MHR6 MHR5 MHR4 MHR3 MHR2 MHR1
CRL
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
CCDPI EPE WLS1 WLS2 RMS1 RMS2 RMS4 RMS8 SS
R51 1ØK +5V
7413 E29 7545
DR 10 H
DR 26
BB1
+3V
7408 E29
10
BU2
7474 E27 RCV FLAG
CLR FLAG 10 L
MDET 30
D4-7 MDET 10 H
R52 10K +5V
BJ2
MDET 10 H
D4-1 1 SYNC 10
R55 10K +5V
D4-2 RESYNC PULSE 10 L DJ2
7417 E36
DR2 RESYNC 2 10 (Ø) H
D4-6 BUF LCR 15 H
D4-2 STROBE 10 H
7474 E56 SEARCH SYNC
D4-3 RX CLOCK 10 H DS2
7408 E29
7474 E51 RESYNC
D4-3 RX CLOCK 10 L
7474 E51 BUFFER
7411 E54
DN2
RESYNC 1 10 (Ø) H
D4-2 RESET BL

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK 11 H CP2 31
D4-5 RCV IN 11 H BK1 35
D4-2 RESET H 38
SAR 11 E46
RRC RI MR
RR9 RR8 RR7 RR6 RR5 RR4 RR3 RR2 RR1 PE OE
D4-7 RR8 11 … D4-7 RR1 11
D4-7 PE 11
D4-7 OE 11
CLR FLAG 11 L
BV1
D4-2 BUF RDE 11 L
7408 E31
SFR DRR MHRL
RESYNC 1 11 (Ø) H CK2
D4-2 STROBE 11 L
D4-7 REC FLAG 10 H
D4-1 SYNC Ø8 … Ø1
MHR8 MHR7 MHR6 MHR5 MHR4 MHR3 MHR2 MHR1
CRL
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
CCDPI EPE WLS1 WLS2 RMS1 RMS2 RMS4 RMS8 SS
R54 10K +5V
7413 E24 7545
DR 11 H
BK2
DR 26
+3V
D4-7 REC FLAG 11 H
7408 E31
7474 E27 RCV FLAG
BV1
CLR FLAG 11 L
BJ2
MDET 11 H
MDET 30
D4-7 MDET 11 H
R55 10K +5V
D4-1 1 SYNC 11
R56 10K +5V
D4-2 RESYNC PULSE 11 L DH2
7417 E36
CK2 RESYNC 2 11 (Ø) H
D4-6 BUF LCR 15 H
D4-2 STROBE 11 H
7474 E56 SEARCH SYNC
D4-3 RX CLOCK 11 H CK2
7408 E31
7474 E56 RESYNC
D4-3 RX CLOCK 11 L
7474 E56 BUFFER
7411 E34
CK2
RESYNC 1 11 (Ø) H

REVISIONS		
CHK	CHANGE NO.	REV.

(RECEIVERS 10 AND 11, RESYNC)

TITLE SYNC MUX LINE CARD LINES Ø8 -11 (D4-7)
SIZE D CODE BS NUMBER DV11-Ø-12 REV. A
SCALE — SHEET 7 OF 8 DIST.

D4-7 RR6 11
D4-7 RR6 10
D4-6 RR6 09
D4-6 RR6 08
D4-7 RR5 11
D4-7 RR5 10
D4-6 RR5 09
D4-6 RR5 08
8881 E74 — FRI — RECV DATA 05 L
8881 E74 — FRI — RECV DATA 04 L

D4-7 PE 11
D4-7 PE 10
D4-6 PE 09
D4-6 PE 08
D4-7 OE 11
D4-7 OE 10
D4-6 OE 09
D4-6 OE 08
8881 E70 — FMI — MASTER PE L
8881 E70 — FLI — MASTER OR L

D4-7 RR4 11
D4-7 RR4 10
D4-6 RR4 09
D4-6 RR4 08
D4-7 RR3 11
D4-7 RR3 10
D4-6 RR3 09
D4-6 RR3 08
8881 E74 — FNI — RECV DATA 05 L
8881 E74 — 10 FPI — RECV DATA 02 L

D3-3 CLEAR TMARK L — FK2 15

D4-2 SET TMARK 11 L
D4-2 SET TMARK 10 L
D4-2 SET TMARK 09 L
D4-2 SET TMARK 08 L
D4-2 RESET H

7474 E68 — EEE — D4-8 TMARK 11 L
7474 E68 — EL2 — D4-8 TMARK 10 L
7474 E68 — CBB — D4-8 TMARK 09 L
7474 E68 — CD2 — D4-8 TMARK 08 L

D4-2CARD FLAG SELECT 08-11 L — DM2

D4-7 RR2 11
D4-7 RR2 10
D4-6 RR2 09
D4-6 RR2 08
D4-7 RR1 11
D4-7 RR1 10
D4-6 RR1 09
D4-6 RR1 08
8881 E71 — FN2 — RECV DATA 01 L
8881 E71 — FP2 — RECV DATA 00 L

D4-7 RR8 11
D4-7 RR8 10
D4-6 RR8 09
D4-6 RR8 08
D4-7 RR7 11
D4-7 RR7 10
D4-6 RR7 09
D4-6 RR7 08
8881 E70 — FHI — RECV DATA 07 L
8881 E70 — 10 FYI — RECV DATA 06 L

D4-2 BUF MASTER SCAN 01 H
D4-2 BUF MASTER SCAN 00 H
D4-2 DATA ENABLE 08-11 H — (FK1)

REVISIONS		
CHK	CHANGE NO.	REV.

(RECV DATA MUX S AND TMARK DECODER)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES 08-11 (04-8)	D	BS	DV11-0-12	A
SCALE	SHEET 8 OF 8		DIST.	

BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR 12
C	GROUND
D	DCE SCR 13
E	GROUND
F	DCE SCR 14
H	GROUND
J	DCE SCR 15
K	GROUND
L	EIA RCV DATA 12
M	GROUND
N	EIA RCV DATA 13
P	GROUND
R	EIA XMIT DATA 12
S	GROUND
T	EIA XMIT DATA 13
U	GROUND
V	DTE SCTE 12
W	GROUND
X	DTE SCTE 13
Y	DTE SCTE 14
Z	GROUND
A A	DTE SCTE 15
B B	GROUND
C C	EIA XMIT DATA 14
D D	GROUND
E E	EIA XMIT DATA 15
F F	GROUND
H H	EIA RCV DATA 14
J J	GROUND
K K	EIA RCV DATA 15
L L	GROUND
M M	DCE SCT 15
N N	GROUND
P P	DCE SCT 14
R R	GROUND
S S	DCE SCT 13
T T	GROUND
U U	DCE SCT 12
V V	GROUND

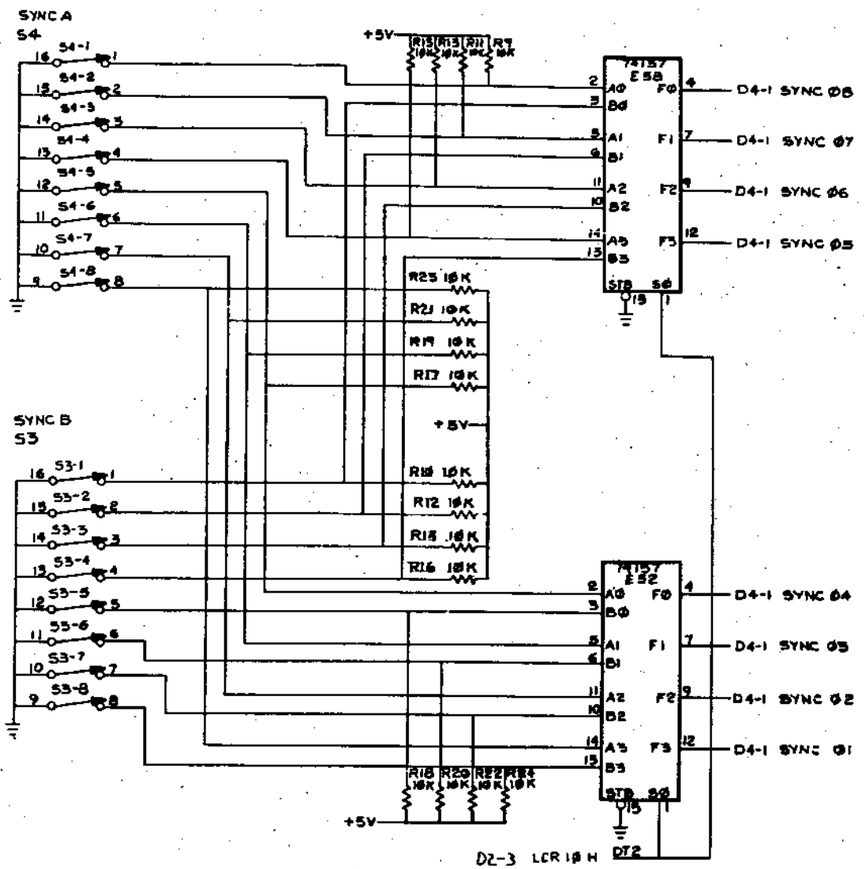
PARAMETER SWITCH SETTINGS

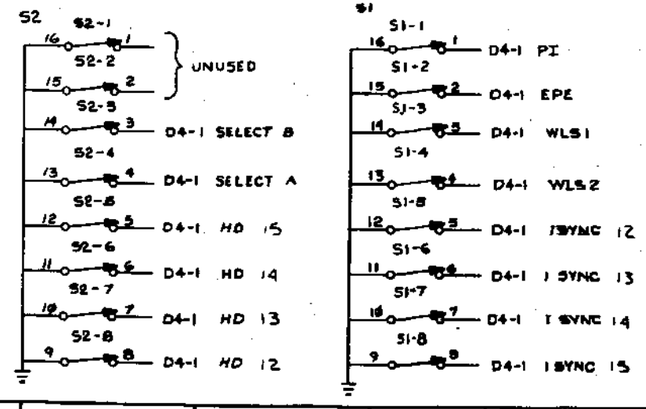
FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B / SELECT A	S2 / S2	3 / 4	ON / ON	ON / OFF	OFF / ON	OFF / OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HD 15	S2	5	ON		OFF	
	HD 14	S2	6	ON		OFF	
	HD 13	S2	7	ON		OFF	
	HD 12	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI / EPE	S1 / S1	1 / 2	OFF / OFF	ON / ON	ON / OFF	
CHARACTER LENGTH				5 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	8 BITS/CHAR
	WLS1 / WLS2	S1 / S1	3 / 4	OFF / OFF	ON / ON	OFF / ON	ON / ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC 12	S1	5	OFF		ON	
	1 SYNC 13	S1	6	OFF		ON	
	1 SYNC 14	S1	7	OFF		ON	
	1 SYNC 15	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=0	SYNC A	S4	1 thru 8	OFF		ON	
LCR10=1	SYNC B	S3	1 thru 8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1 / CS2	GROUND / GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1 / MS2	GROUND / NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1 / RMS2 / RMS3	NO CONNECTION / NO CONNECTION / NO CONNECTION

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA 08 H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KB H. NO M7839 CIRCUITRY IS CONNECTED TO IT.





D3-5 230.4 KB H BM1
(SEE NOTE 4)

REVISIONS		
CHK	CHANGE NO.	REV.
	DVII-00006	A
J. McNAMARA	20 July 77	

(CHARTS, SWITCHES, AND SYNC SELECTOR)

DRN		FIRST USED ON: DVII
CHK'D		digital
ENG.		TITLE: SYNC MUX LINE CARD LINES 12 - 15 (D4-1)
PROJ. ENG.		
PROD.	4-12-13	
NEXT HIGHER ASSY.		
B DD-DVII-0		SIZE D / CODE BS / NUMBER DVII-0-13 / REV. A
SCALE		
SHEET 1 OF 8		DIST.

DBS DVII-0-13 REV A

D4-2 CARD PARAMETER SELECT 12 - 15 L DM2

D3-8 SRS ϕ3 H BS2 — 74S64 E83 — D3-8 SRS ϕ2 H BE3

D2-3 CONTROL STROBE H CS2 — 7404 E41 — D4-2 BUF CONTROL STROBE L

D3-7 INIT 01 L IN2 — 7437 E63 — D4-2 RESET H

7437 E63 — D4-2 RESET A L

7437 E63 — D4-2 RESET B L

+3V

5788 5784 74153 E55 — DB, DA, S1, SØ; FB3 FB2 FB1 FBØ; FA3 FA2 FA1 FAØ

D4-2 STROBE 15 L

7404 E54 — D4-2 STROBE 15 H

D4-2 STROBE 14 L

7404 E54 — D4-2 STROBE 14 H

D4-2 STROBE 13 L

7404 E54 — D4-2 STROBE 13 H

D4-2 STROBE 12 L

7404 E54 — D4-2 STROBE 12 H

D3-8 SES 01 H BTZ

D3-8 SRS ϕϕ H BM2

5788 5784 74153 E22 — D4-5 RCV IN 15 H; D4-5 RCV IN 14 H; D4-4 RCV IN 13 H; D4-4 RCV IN 12 H

8881 E47 — FFI BIT WINDOW L

BE2 — D4-3 INTR MAINTENANCE 12 - 15 H

D3-4 TRAN DATA ϕ8 H ER1 (SEE NOTE 3 ON SHEET 1 OF 5)

D3-4 TRAN DATA ϕ7 H EP1 — 7417 E61 — D4-2 TR8 H

D3-4 TRAN DATA ϕ6 H EM2 — 7417 E61 — D4-2 TR7 H

D3-4 TRAN DATA ϕ5 H FB2 — 7417 E76 — D4-2 TR6 H

D3-4 TRAN DATA ϕ4 H FV2 — 7417 E76 — D4-2 TR5 H

D3-4 TRAN DATA ϕ3 H FS2 — 7417 E76 — D4-2 TR4 H

D3-4 TRAN DATA ϕ2 H FV1 — 7417 E76 — D4-2 TR3 H

D3-4 TRAN DATA ϕ1 H FT2 — 7417 E76 — D4-2 TR2 H

D3-4 TRAN DATA ϕϕ H FU2 — 7417 E76 — D4-2 TR1 H

D4-2 CARD FLAG SELECT 12 - 15 L DM2

D3-4 MASTER SCAN ϕ3 H EN2 — 7437 E69

D3-4 MASTER SCAN ϕ2 H EN2 — 7437 E69

7404 E41 — D3-3 RESYNC PULSE L DF2

7404 E41 — D3-3 SET TMARK L CU2

74H11 E3A — D1-5 RECEIVED DATA ENABLE H CN2 — FK1 — D4-2 DATA ENABLE 12-15 H

+5V; R25 10K; C96 68pf; 7413 E75 RDE 368NS; FU1 — RDE 12-15 H; +3V

D3-4 TRANSMITTER STROBE H EH2

+5V; R26 1K — 7417 E61 — D3-4 MASTER SCAN ϕ1 H EM1

+5V; R27 1K — 7417 E61 — D3-4 MASTER SCAN ϕϕ H EN1

5788 5784 74153 E47 — DB, DA, S1, SØ; FB3 FB2 FB1 FBØ; FA3 FA2 FA1 FAØ

D4-2 RESYNC PULSE 15 L (12 DM2)

D4-2 RESYNC PULSE 14 L (11 DS2)

D4-2 RESYNC PULSE 13 L (10 DK2)

D4-2 RESYNC PULSE 12 L (9 DL2)

D4-2 SET TMARK 15 L

D4-2 SET TMARK 14 L

D4-2 SET TMARK 13 L

D4-2 SET TMARK 12 L

5788 5784 74153 E57 — DB, DA, S1, SØ; FB3 FB2 FB1 FBØ; FA3 FA2 FA1 FAØ

D4-2 BUF RDE 15 L

D4-2 BUF RDE 14 L

D4-2 BUF RDE 13 L

D4-2 BUF RDE 12 L

D4-2 THRL 15 L

D4-2 THRL 14 L

D4-2 THRL 13 L

D4-2 THRL 12 L

5788 5784 74153 E22 — D4-5 DA 15 H; D4-5 DA 14 H; D4-4 DA 13 H; D4-4 DA 12 H; D4-7 MDET 15 H; D4-7 MDET 14 H; D4-6 MDET 13 H; D4-6 MDET 12 H

8881 E47 — FCI DATA NOT AVAILABLE L

8881 E47 — FBI MATCH DETECT L

5788 5784 74153 E45 — D4-5 TRAN FLAG 15 H; D4-5 TRAN FLAG 14 H; D4-4 TRAN FLAG 13 H; D4-4 TRAN FLAG 12 H; D4-7 REC FLAG 15 H; D4-7 REC FLAG 14 H; D4-6 REC FLAG 13 H; D4-6 REC FLAG 12 H

8881 E71 — FLZ TRAN FLAG WAITING L

8881 E71 — FNE RECEIVER FLAG L

D4-2 BUF MASTER SCAN ϕ1 H

D4-2 BUF MASTER SCAN ϕϕ H

D3-4 MASTER SCAN TIR CRE — 7404 E41

(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SYNC MUX LINE CARD LINES 12 - 15 (D4-2)	SIZE/CODE	D 85
SCALE		SHEET 2 OF 8	DIST.
NUMBER	DV11-Ø-13	REV.	A

DV11-Ø-13 D 85 A

NOTE: 1) A JUMPER WIRE MAY BE SOLDERED ACROSS THE RESISTOR IF THE CUSTOMER SO REQUESTS. HOWEVER, ALL M7839 MODULES WILL BE SHIPPED WITH THE RESISTOR NOT JUMPERED TO INSURE PROPER OPERATION WITH BELL SYSTEM 201A AND 201B MODEMS.

D4-8 TMARK 12 L — CD2 — R28 10K +5V — D4-1 HD 12 — 7466 E33
DCE SCR 12 — J1 P — 1489 E5 — C81 470 pF — 7432 E4 — 74H11 E25 — 7466 E41 — DE2 — D4-3 RX CLOCK 12 H
D4-3 RX CLOCK 12 L

D4-8 TMARK 14 L — EL2 — R33 10K +5V — D4-1 HD 14 — 7466 E38
DCE SCR 14 — J1 F — 1489 E5 — C83 470 pF — 7432 E4 — 74H11 E39 — 7466 E54 — DS2 — D4-3 RX CLOCK 14 H
D4-3 RX CLOCK 14 L

DCE SCR 13 — J1 D — 1489 E5 — C82 470 pF — 7432 E9 — 74H11 E25 — 7466 E54 — CE2 — D4-3 RX CLOCK 13 H
D4-3 RX CLOCK 13 L
D4-8 TMARK 13 L — CB2 — R29 10K +5V — D4-1 HD 13 — 7466 E33

DCE SCR 15 — J1 J — 1489 E5 — C84 470 pF — 7432 E4 — 74H11 E26 — 7466 E41 — 8 CP2 — D4-3 RX CLOCK 15 H
D4-3 RX CLOCK 15 L
D4-8 TMARK 15 L — EE2 — R34 10K +5V — D4-1 HD 15 — 7466 E33

DCE SCT 12 — J1 U — 1489 E16 — C92 470 pF — 7432 E15 — 7466 E21 — D4-3 TX CLOCK 12 H
DCE SCT 13 — J1 S — 1489 E16 — C91 470 pF — 7432 E15 — 7466 E21 — D4-3 TX CLOCK 13 H
DCE SCT 14 — J1 P — 1489 E16 — C90 470 pF — 7432 E15 — 7466 E21 — D4-3 TX CLOCK 14 H
DCE SCT 15 — J1 MM — 1489 E16 — C89 470 pF — 7432 E15 — 7466 E21 — D4-3 TX CLOCK 15 H

J1 — 1488 E26 — R37 7.5K SEE NOTE 1 — V — DTE SCTE 12
1488 E26 — R36 7.5K SEE NOTE 1 — X — DTE SCTE 13
1488 E26 — R35 7.5K SEE NOTE 1 — Y — DTE SCTE 14
1488 E26 — R38 7.5K SEE NOTE 1 — AA — DTE SCTE 15

D3-5 9600 BAUD
D3-5 4800 BAUD
D3-5 2400 BAUD
D3-5 1200 BAUD
74153 E68 — STB1 STB0 — D1 C1 B1 A1 — FF2 FE2 FD2 FD1 — D0 C0 B0 A0 — F1 F0 — ES2 — D4-3 MUX CLOCK 12-15 H
R31 10K +5V — R32 10K — D4-1 SELECT B — D4-1 SELECT A

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

D2-3 MAINTENANCE CLK PULSE H — ET2 — 7456 E64 — BB1 — SOURCE CLOCK A 12-15 L
D4-3 MUX CLOCK 12-15 H (ES2) — 7456 E64 — BB2 — SOURCE CLOCK B 12-15 L
D2-3 MAINTENANCE CLK PULSE H (ET2)
D4-4 MODE Ø1 (1) H — 7411 E61 — 7408 E13 — BB2 — D4-3 SYSTEM MODE 12-15 H
D4-4 MODE Ø0 (1) H
R30 1K +5V — 7408 E13 — BE2 — D4-3 INTR MAINTENANCE 12-15 H
D4-4 MODE Ø1 (Ø) H

(CLOCK SOURCE AND SELECTION)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SYNC MUX LINE CARD LINES 12—15 (D4-3)	SIZE/CODE	NUMBER / REV.
SCALE	SHEET 3 OF 8	D BS	DVII-Ø-13 A
		DIST.	

DES DVII-Ø-13 A

D4-4 MODE ϕϕ (0) H
D4-4 MODE ϕϕ (1) H
D4-4 RCV IN 12 H
D4-4 INTR RCV DATA 12-15 L
D4-3 INTR MAINTENANCE 12-15 H
D4-4 MODE ϕ1(0) H
D4-4 MODE ϕ1(1) H
D2-3 LCR 14 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR 09 H
EIA REC DATA 12
D4-4 TRANS DISABLE 12-15 H
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT 2-15 L
D4-2 BUF CONTROL STROBE L
D4-4 BUF MODE ϕϕ (0) H
SERIAL OUT 12 L
EIA XMIT DATA 12
D4-4 MODE ϕ1 (0) H
D4-8 TMARK 12 L
D4-3 TX CLOCK 12 H
D4-2 RESET H
D4-2 THRL 12 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE 12 L
D4-1 SYNC ϕ8
D4-1 SYNC ϕ7
D4-1 SYNC ϕ6
D4-1 SYNC ϕ5
D4-1 SYNC ϕ4
D4-1 SYNC ϕ3
D4-1 SYNC ϕ2
D4-1 SYNC ϕ1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
SAT 12 E73
TCO 12 H
ECC 12 H
D4-4 DA 12 H
D4-4 TRAN FLAG 12 H
D4-4 RCV IN 13 H
D4-4 INTR RCV DATA 12-15 L
D4-4 TRANS DISABLE 12-15 H
SERIAL OUT 13 L
D4-4 BUF MODE ϕϕ (0) H
EIA XMIT DATA 13
D4-8 TMARK 13 L
D4-3 TX CLOCK 13 H
D4-2 RESET H
D4-2 THRL 13 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE 13 L
D4-1 SYNC ϕ8
D4-1 SYNC ϕ7
D4-1 SYNC ϕ6
D4-1 SYNC ϕ5
D4-1 SYNC ϕ4
D4-1 SYNC ϕ3
D4-1 SYNC ϕ2
D4-1 SYNC ϕ1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
SAT 13 E66
TCO 13 H
EOC 13 H
D4-4 DA 13 H
D4-4 TRAN FLAG 13 H
D4-4 RCV IN 13 H
D4-4 MODE ϕϕ (1) H
D4-4 MODE ϕ1 (0) H
D4-4 BUF MODE ϕ1 (0) H
+5V
+5V -12V
R41 1K
R40 1K
R39 1K
C87 .47MF
C86 .47MF

(MODE SELECTION, TRANSMITTERS 12 AND 13)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES 12 – 15 (04-4)	D	BS	DVII-Ø-13	A

SCALE — SHEET 4 OF 8 — DIST.

DVII-Ø-13 A

EIA REC DATA 14 — J1 HH — 1489 E11 — C88 470pf

D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ (1) H
7450 E9 — 7400 E23 — BK2 — D4-5 RCV IN 14 H

D4-4 TRANS DISABLE 12-15 H (AF2) — 7402 E12

D4-4 INTR RCV DATA 12-15 L BC1

D4-4 BUF MODE ØØ (Ø) H — +5V — R42 1K — 8242 E2 — 1488 E6 — J1 CC — EIA XMIT DATA 14

D4-4 MODE ØØ (1) H — 7402 E12 — 7404 E10 — AT2 — SERIAL OUT 14 L

EIA REC DATA 15 — J1 KK — 1489 E11 — C85 470pf

D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ (1) H
7450 E9 — 7400 E23 — BK1 — D4-5 RCV IN 15 H

D4-4 BUF MODE ØØ (Ø) H — +5V — R43 1K — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA 15

D4-4 MODE ØØ (1) H — 7402 E3 — 7402 E3 — (AF2) — D4-4 TRANS DISABLE 12-15 H

+5V -12V — VSS VGG VDD — SAT 14 E59

D4-8 TMARK 14 L EL2 17 — CTS
D4-3 TX CLOCK 14 H 5 — TRC
D4-2 RESET H 18 — MR
10 — DAR
D4-2 THRL 14 L 19 — THRL
D4-2 TR8 H 38 — TR8
D4-2 TR7 H 36 — TR7
D4-2 TR6 H 34 — TR6
D4-2 TR5 H 32 — TR5
D4-2 TR4 H 30 — TR4
D4-2 TR3 H 28 — TR3
D4-2 TR2 H 26 — TR2
D4-2 TR1 H 24 — TR1
D4-2 STROBE 14 L 26 — FHRL
D4-1 SYNC Ø8 37 — FR8
D4-1 SYNC Ø7 35 — FR7
D4-1 SYNC Ø6 33 — FR6
D4-1 SYNC Ø5 31 — FR5
D4-1 SYNC Ø4 29 — FR4
D4-1 SYNC Ø3 27 — FR3
D4-1 SYNC Ø2 25 — FR2
D4-1 SYNC Ø1 23 — FR1
4 — CRL
22 — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO 15 — TCO 11 EJ2 — TCO 14 H
DD/EOC 13 EK2 — EOC 14 H
DA 12 — D4-5 DA 14 H
THRE 16 — D4-5 TRAN FLAG 14 H

+5V -12V — VSS VGG VDD — SAT 15 E55

D4-8 TMARK 15 L EE2 17 — CTS
D4-3 TX CLOCK 15 H 5 — TRC
D4-2 RESET H 18 — MR
16 — DAR
D4-2 THRL 15 L 19 — THRL
D4-2 TR8 H 38 — TR8
D4-2 TR7 H 36 — TR7
D4-2 TR6 H 34 — TR6
D4-2 TR5 H 32 — TR5
D4-2 TR4 H 30 — TR4
D4-2 TR3 H 28 — TR3
D4-2 TR2 H 26 — TR2
D4-2 TR1 H 24 — TR1
D4-2 STROBE 15 L 26 — FHRL
D4-1 SYNC Ø8 37 — FR8
D4-1 SYNC Ø7 35 — FR7
D4-1 SYNC Ø6 33 — FR6
D4-1 SYNC Ø5 31 — FR5
D4-1 SYNC Ø4 29 — FR4
D4-1 SYNC Ø3 27 — FR3
D4-1 SYNC Ø2 25 — FR2
D4-1 SYNC Ø1 23 — FR1
4 — CRL
22 — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO 15 — 7404 E10 — AH2 — SERIAL OUT 15 L
TCO 11 EDE — TCO 15 H
DD/EOC 13 EFE — EOC 15 H
DA 12 — D4-5 DA 15 H
THRE 16 — D4-5 TRAN FLAG 15 H

REVISIONS

CHK	CHANGE NO.	REV.

(TRANSMITTERS 14 AND 15)

TITLE SYNC MUX LINE CARD LINES 12 - 15 (D4-5)
SIZE D | CODE BS | NUMBER DVII-0-13 | REV. A
SCALE | SHEET 5 OF 8 | DIST.

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK 12 H DE2 31
D4-4 RCV IN 12 H BF8 35
D4-2 RESET H 38
RRC RI MR
SAR 12 E50
CLR FLAG 12 L
BV2
D4-2 BUF RDE 12 L
7408 E5B
SFR DRR
CV2
D4-2 STROBE 12 L 34
RESYNC 1 12 (Ø) H
MHRL
D4-1 SYNC Ø8 46 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
CRL
CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
RR9 7
RR8 8 D4-6 RR8 12
RR7 9 D4-6 RR7 12
RR6 10 D4-6 RR6 12
RR5 11 D4-6 RR5 12
RR4 12 D4-6 RR4 12
RR3 13 D4-6 RR3 12
RR2 14 D4-6 RR2 12
RR1 15 D4-6 RR1 12
PE 29 D4-6 PE 12
OE 27 D4-6 OE 12
DR 26
+5V R47 10K
74123 E14 75M5
AR2 DR 12 H
+3V
7408 E18
D4-6 REC FLAG 12 H
7474 E28 REC FLAG
CLR FLAG 12 L
+5V R46 10K
MDET 30
D4-6 MDET 12 H
7408 E18
74123 E19 75M5
AV2 MDET 12 H
R45 10K
D4-1 1 SYNC 12 +5V
D4-6 BUF LCR 15 H
D4-2 RESYNC PULSE 12 L DL2
+5V R44 1K +3V
D2-3 LCR 13 H BA1
7417 E36
7474 E6B SEARCH SYNC
D4-2 STROBE 12 H
7408 E35
D4-3 RX CLOCK 12 L
7474 E5B RESYNC
CV2
RESYNC 1 12 (Ø) H
DE2
+3V
DD2 RESYNC 2 12 (Ø) H
7417 E30
7411 E34
D4-2 RESET A L

+5V -12V
VSS VGG VDD
D4-3 RX CLOCK 13 H CE2 31
D4-4 RCV IN 13 H BD1 38
D4-2 RESET H 38
RRC RI MR
SAR 13 E67
CLR FLAG 13 L
BF1
D4-2 BUF RDE 13 L
7408 E1B
SFR DRR
RESYNC 1 13 (Ø) H BH2
D4-2 STROBE 13 L 34
MHRL
D4-1 SYNC Ø8 46 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
CRL
CD PI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
RR9 7
RR8 8 D4-6 RR8 13
RR7 9 D4-6 RR7 13
RR6 10 D4-6 RR6 13
RR5 11 D4-6 RR5 13
RR4 12 D4-6 RR4 13
RR3 13 D4-6 RR3 13
RR2 14 D4-6 RR2 13
RR1 15 D4-6 RR1 13
PE 29 D4-6 PE 13
OE 27 D4-6 OE 13
DR 26
+5V 24B 10K
74123 E19 75M5
AU2 DR 13 H
+3V
7408 E18
D4-6 REC FLAG 13 H
7474 E28 REC FLAG
CLR FLAG 13 L
+5V R49 10K
MDET 30
D4-6 MDET 13 H
7408 E39
74123 E19 75M5
BH1 MDET 13 H
R86 10K
D4-1 1 SYNC 13 +5V
D4-2 RESYNC PULSE 13 L DR2
+5V
D4-6 BUF LCR 15 H
7474 E6B SEARCH SYNC
D4-2 STROBE 13 H
D4-3 RX CLOCK 13 H CE2
+3V
7408 E38
7474 E38 RESYNC
D4-3 RX CLOCK 13 L
BH2 RESYNC 1 13 (Ø) H
7417 E30
CF2 RESYNC 2 13 (Ø) H
7411 E34

REVISIONS
CHR | CHANGE NO. | REV.

(RECEIVERS 12 AND 13, RESYNC)

TITLE SYNC MUX LINE CARD
LINES 12 - 15 (D4-6)
SIZE D CODE BS NUMBER DVII-0-13 REV. A
SCALE — SHEET 6 OF 8 DIST.

DVII-0-13 A
8 7 6 5 4 3 2 1

D4-3 RX CLOCK 14 H DS2 31 — RRC
D4-5 RCV IN 14 H BK2 35 — RI
D4-2 RESET H 32 — MR
+5V -12V 1 16 2Ø — VSS VGG VDD
SAR 14 E46
RR9 7
RR8 8 — D4-7 RR8 14
RR7 9 — D4-7 RR7 14
RR6 10 — D4-7 RR6 14
RR5 11 — D4-7 RR5 14
RR4 12 — D4-7 RR4 14
RR3 13 — D4-7 RR3 14
RR2 14 — D4-7 RR2 14
RR1 15 — D4-7 RR1 14
PE 29 — D4-7 PE 14
OE 27 — D4-7 OE 14
RSI +5V 10K
CLR FLAG 14 L BU2
D4-2 BUF RDE 14 L — 7408 E29
D4-2 STROBE 14 L — MHRL 34
DN2
RESYNC 1 14 (Ø) H
SFR 24
DRR 25
DR 26
7433 E28 75NS — DR 14 H BB1
7408 E29
+3V
D4-1 SYNC Ø8 40 — MHR8
D4-1 SYNC Ø7 4 — MHR7
D4-1 SYNC Ø6 38 — MHR6
D4-1 SYNC Ø5 3 — MHR5
D4-1 SYNC Ø4 36 — MHR4
D4-1 SYNC Ø3 17 — MHR3
D4-1 SYNC Ø2 22 — MHR2
D4-1 SYNC Ø1 18 — MHR1
CRL 33
CDPI EPE WLS1 WLS2 RHS3 RHS2 RHS1 SS 6 19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
D4-7 MDET 14 H
MDET 30 12 — 7408 E29
R52 10K +5V
7414 E27 RCV FLAG 8 9 11 13
BU2 CLR FLAG 14 L
7433 E28 75NS — BJ2 MDET 14 H
R53 10K +5V
D4-1 1 SYNC 14
D4-2 RESYNC PULSE 14 L DJ2
7417 E36 5 6 — DR2 RESYNC 2 14 (Ø) H
D4-6 BUF LCR 15 H 2 4 5 6 — 7474 E56 SYNC
D4-2 STROBE 14 H 3 8
D4-3 RX CLOCK 14 H DS2
7408 E29 1 2 3 12 18
7474 E51 RESYNC 1 9 11 13
D4-3 RX CLOCK 14 L
+3V 4 2 5 6 — 7474 E51 RESYNC 2 1 3
74H11 E54 3 4 5 6
DN2
RESYNC 1 14 (Ø) H
D4-2 RESET 8 L

D4-3 RX CLOCK 15 H CP2 31 — RRC
D4-5 RCV IN 15 H BK1 35 — RI
D4-2 RESET H 32 — MR
+5V -12V 1 16 2Ø — VSS VGG VDD
SAR 15 E40
RR9 7
RR8 8 — D4-7 RR8 15
RR7 9 — D4-7 RR7 15
RR6 10 — D4-7 RR6 15
RR5 11 — D4-7 RR5 15
RR4 12 — D4-7 RR4 15
RR3 13 — D4-7 RR3 15
RR2 14 — D4-7 RR2 15
RR1 15 — D4-7 RR1 15
PE 29 — D4-7 PE 15
OE 27 — D4-7 OE 15
CLR FLAG 15 L BV1
D4-2 BUF RDE 15 L — 7408 E31
RESYNC 1 15 (Ø) H — CK2
D4-2 STROBE 15 L — MHRL 34
SFR 24
DRR 25
DR 26
D4-7 REC FLAG 14 H
D4-1 SYNC Ø8 40 — MHR8
D4-1 SYNC Ø7 4 — MHR7
D4-1 SYNC Ø6 38 — MHR6
D4-1 SYNC Ø5 3 — MHR5
D4-1 SYNC Ø4 36 — MHR4
D4-1 SYNC Ø3 17 — MHR3
D4-1 SYNC Ø2 22 — MHR2
D4-1 SYNC Ø1 18 — MHR1
CRL 33
CDPI EPE WLS1 WLS2 RHS3 RHS2 RHS1 SS 6 19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
+5V R54 10K
7433 E24 75NS — BL2 DR 15 H
7408 E31
+3V
D4-7 REC FLAG 15 H
+5V R55 10K
D4-7 MDET 15 H
MDET 30 9 10 — 7408 E31
7433 E24 75NS — BP2 MDET 15 H
R56 10K +5V
D4-1 1 SYNC 15
BV1 3 — 7474 E27 RCV FLAG 5 6
CLR FLAG 15 L
D4-2 RESYNC PULSE 15 L DH2
7417 E36 11 10 — CK2 RESYNC 2 15 (Ø) H
D4-6 BUF LCR 15 H 12 9 — 7474 E56 SYNC
D4-2 STROBE 15 H 11 15
D4-3 RX CLOCK 15 H CP2
7408 E31 1 2 3 12 18
7474 E56 RESYNC 9 11 13
D4-3 RX CLOCK 15 L
+3V 4 2 5 6 — 7474 E56 RESYNC 2 1 3
74H11 E54 9 10 11 8
CK2
RESYNC 1 15 (Ø) H

REVISIONS
CHK | CHANGE NO. | REV.

(RECEIVERS 14 AND 15, RESYNC)
TITLE SYNC MUX LINE CARD LINES 12 - 15 (D4-7)
SIZE D | CODE BS | NUMBER DVII-Ø-13 | REV. A
SCALE | SHEET 7 OF 8 | DIST.

D4-7 RR6 15
D4-7 RR6 14
D4-6 RR6 13
D4-6 RR6 12
D4-7 RR5 15
D4-7 RR5 14
D4-6 RR5 13
D4-6 RR5 12
8881 E74 FRI RECV DATA Ø5 L
8881 E74 FSI RECV DATA Ø4 L

D4-7 PE 15
D4-7 PE 14
D4-6 PE 13
D4-6 PE 12
D4-7 OE 15
D4-7 OE 14
D4-6 OE 13
D4-6 OE 12
8881 E78 FMI MASTER PE L
8881 E78 FLI MASTER OR L

D4-2 SET TMARK 15 L
D4-2 SET TMARK 14 L
D4-2 SET TMARK 13 L
D4-2 SET TMARK 12 L
D4-2 RESET H
EEE D4-8 TMARK 15 L
EEE D4-8 TMARK 14 L
CBE D4-8 TMARK 13 L
CD2 D4-8 TMARK 12 L

D4-7 RR4 15
D4-7 RR4 14
D4-6 RR4 13
D4-6 RR4 12
D4-7 RR3 15
D4-7 RR3 14
D4-6 RR3 13
D4-6 RR3 12
8881 E74 FNI RECV DATA Ø5 L
8881 E74 FPI RECV DATA Ø2 L

D3-3 CLEAR TMARK L FKZ 15

D4-2 CARD FLAG SELECT 12-15 L DM2

D4-7 RR2 15
D4-7 RR2 14
D4-6 RR2 13
D4-6 RR2 12
D4-7 RR1 15
D4-7 RR1 14
D4-6 RR1 13
D4-6 RR1 12
8881 E71 FN2 RECV DATA Ø1 L
8881 E71 FP2 RECV DATA ØØ L

D4-7 RR8 15
D4-7 RR8 14
D4-6 RR8 13
D4-6 RR8 12
D4-7 RR7 15
D4-7 RR7 14
D4-6 RR7 13
D4-6 RR7 12
8881 E70 FHI RECV DATA Ø7 L
8881 E70 FJI RECV DATA Ø6 L

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D4-2 DATA ENABLE 12-15 H (FKI)

REVISIONS
CHK | CHANGE NO. | REV.

(RECV DATA MUXS AND TMARK DECODER)

TITLE SYNC MUX LINE CARD
LINES 12 - 15 (D4-8)
SIZE D | CODE BS | NUMBER DVII-Ø-13 | REV. A
SCALE | SHEET 8 OF 8 | DIST.

DIGITAL EQUIPMENT CORPORATION

REV.	NUMBER	CODE	SIZE
A	DV11-0-14	CS	K

This microprogram listing lists the 9 bit binary address of each micro instructions, followed by the 16 bit micro instruction as it would appear in the ROM DATA REGISTER (D3-2), followed by an explanation of the micro instruction. Contents of the ROM DATA REGISTER are the complement of the ROM chip outputs. Odd addresses reference one set of 4 ROM chips, even addresses reference the other set of 4 ROM chips.

BITS	ADDRESSES	PART NUMBER	ROM LIST
15-12	even	23-192A2	K-CS-M7838-0-15
11-8	even	23-191A2	K-CS-M7838-0-14
7-4	even	23-189A2	K-CS-M7838-0-12
3-0	even	23-190A2	K-CS-M7838-0-13
15-12	odd	23-185A2	K-CS-M7838-0-8
11-8	odd	23-186A2	K-CS-M7838-0-9
7-4	odd	23-188A2	K-CS-M7838-0-11
3-0	odd	23-187A2	K-CS-M7838-0-10

Diagnostic DZDVC Test #1 compares ROM DATA REGISTER contents with this listing. Use the above table to determine which ROM is faulty. Bit 15 is at left end of word Bit 0 at right end.

REVISIONS	REV.	CHANGE NO.	CHK
	A	DV11-00002	

DEC FORM NO. DRB 109

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DV11		PARTS LIST		

DRN. Robert Kopperud	DATE 3-31-75	
CHK'D. Carl Roberts	DATE 4-17-75	
ENG. Lieut. R. Hansen	DATE 4-17-75	
PROJ. ENG. Lieut. R. Hansen	DATE 4-17-75	
PROD. R. Lavalle	DATE 4-17-75	
NEXT HIGHER ASSEMBLY B-DD-DV11-0		
SCALE —		
SHEET 1 OF 13		

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
MICROPROGRAM LISTING

SIZE	CODE	NUMBER	REV.
K	CS	DV11-0-14	A

DIST.

```
                                    ;IDLE LOOP

00 0000 0000  0101 0000 0100 0010   ILOOP  S/C     6,2      ;INCREMENT SCANNER
00 0000 0001  0011 0000 0101 0100           XFR     ,5,4     ;MOVE MASTER SCAN TO RAM ADDRESS
00 0000 0010  0000 0010 1110 0100           BRA     2,TSERV  ;TEST FOR TRANSMIT FLAG WAITING, IF YES BRANCH TO TRANSMIT SERVICE
00 0000 0011  0000 0100 0000 1010           BRA     4,RSERV  ;TEST FOR RECEIVER FLAG WAITING, IF YES BRANCH TO RECEIVE FLAG SERV
00 0000 0100  0000 0011 0100 0011           BRA     3,SSERV  ;TEST FOR RECEIVED CHARACTER WAITING, IF YES BRANCH TO RECEIVED CHA
00 0000 0101  0010 0000 0000 1011   ILOP2  RAM     0,0,13   ;OBTAIN LINE STATE
00 0000 0110  0111 0001 0010 1110           BRB     1,RSYNC  ;TEST RAM OUTPUT 01 (RESYNC), IF YES BRANCH TO RESYNCHRONIZE
00 0000 0111  0111 0010 0011 1010           BRB     2,TMARK  ;TEST RAM OUTPUT 02 (XMIT GO), IF YES BRANCH TO CLEAR TMARK
00 0001 0000  0000 0101 0010 1001   ILOP5  BRA     5,ISERV  ;TEST FOR CHARACTER DISPATCH PROCEED, (SCM 08) IF YES BRANCH T
00 0001 0001  0000 0001 0000 0000           BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP


                                    ;RECEIVE FLAG SERVICE  (LINE STATE IS IN RAM OUTPUT)

00 0001 0010  0010 0000 0000 1011   RSERV  RAM     0,0,13   ;OBTAIN LINE STATE
00 0001 0011  0111 0000 0001 1110           BRB     0,TESTX  ;TEST RAM OUTPUT 00 (RECEIVER ACTIVE), IF YES BRANCH TO TESTX
00 0001 0100  0111 1101 0000 1111           BRB     15,S/ACT         ;TEST MATCH DETECT, IF YES BRANCH TO SET ACTIVE
00 0001 0101  0101 0000 0100 0110           S/C     6,6      ;SET RESYNC PULSE,
00 0001 0110  0000 0001 0000 0000           BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO ILOOP
00 0001 0111  0010 0000 0000 1010   S/ACT  RAM     0,0,12   ;OBTAIN DLE/PROTOCOL
00 0010 0000  0111 0001 0001 1000           BRB     1,SACT2  ;TEST RAM 01 (STRIP LEADING SYNC), IF YES BRANCH TO SACT2
00 0010 0001  0010 0000 0000 1011   SACT1  RAM     0,0,13   ;OBTAIN LINE STATE
00 0010 0010  0101 0000 0010 0111           S/C     5,7      ;SET RAM OUTPUT 00 (RECEIVER ACTIVE)
00 0010 0011  0010 0001 1011 1011           RAM     1,13,13  ;WRITE NEW LINE STATE
00 0010 0100  0111 1111 0200 1001           BRB     16,SACT1         ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO SACT 1
00 0010 0101  0101 0000 0001 0011   CLRRF  S/C     4,3      ;SET RECEIVE DATA ENABLE
00 0010 0110  0101 0000 0001 0010           S/C     4,2      ;CLEAR RECEIVE DATA ENABLE AND DATA AVAILABLE (FLAG WAITING)
00 0010 0111  0000 0001 0000 0000           BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP
00 0011 0000  0010 0000 0000 1011   SACT2  RAM     0,0,13   ;OBTAIN LINE STATE
00 0011 0001  0101 0000 0010 0111           S/C     5,7      ;SET RAM OUTPUT 00 (RECEIVER ACTIVE)
00 0011 0010  0101 0000 1000 0110           S/C     7,6      ;SET RAM OUTPUT 06 (STRIP SYNC ON)
00 0011 0011  0010 0001 1011 1011           RAM     1,13,13  ;WRITE NEW LINE STATE
00 0011 0100  0111 1111 0000 1100           BRB     16,SACT2         ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO SACT 2
00 0011 0101  0000 0001 0001 0101           BRA     1,CLRRF  ;TEST FOR SURE TRUE, IF YES BRANCH TO CLRRF


00 0011 0110  0010 0000 0000 1011   TESTX  RAM     0,0,13   ;OBTAIN LINE STATE
00 0011 0111  0111 0110 0001 0001           BRB     6,TMD    ;TEST RAM OUTPUT 06 (STRIP SYNC ON), IF YES BRANCH TO TMD
00 0100 0000  0000 0001 0010 0101           BRA     1,S/RDE  ;TEST FOR SURE TRUE, IF YES BRANCH TO S/RDE
00 0100 0001  0111 1101 0001 0101   TMD    BRB     15,CLRRF         ;TEST MATCH DETECT, IF YES BRANCH TO CLRRF
00 0100 0010  0101 0000 0100 0010           S/C     7,2      ;CLEAR RAM OUTPUT 06 (STRIP SYNC ON)
00 0100 0011  0010 0001 1011 1011           RAM     1,13,13  ;WRITE NEW LINE STATE
00 0100 0100  0111 1111 0000 1010           BRB     16,RSERV         ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO RSERV
00 0100 0101  0101 0000 0001 0011   S/RDE  S/C     4,3      ;SET RECEIVE DATA ENABLE
00 0100 0110  0101 0000 0001 0001           S/C     4,1      ;SET SILO IN
00 0100 0111  0101 0000 0001 0010           S/C     4,2      ;CLEAR RECEIVE DATA ENABLE AND DATA AVAILABLE (FLAG WAITING)
00 0101 0000  0000 0001 0000 0000           BRA     1,ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO ILOOP

                                    ;RECEIVE INTERRUPT RESPONSE SERVICE

00 0101 0001  0011 0000 1100 0001   ISERV  XFR     ,14,1    ;MOVE SILO OUT TO A REGISTER
00 0101 0010  0001 0000 0001 1111           ALU     37       ;LET ALU RESULT = A REGISTER
00 0101 0011  0011 0000 0110 0100           XFR     ,6,4     ;MOVE ALU RESULT 08-11 TO RAM ADDRESS REGISTER 00-03
00 0101 0100  0101 0000 0000 1110           S/C     3,6      ;CLEAR SCR08
00 0101 0101  0000 0001 0110 0010           BRA     1,CTEST  ;TEST FOR SURE TRUE, IF YES BRANCH TO CTEST
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                                    ;RESYNCHRONIZE (MASTER SCAN IS IN RAM AR, LINE STATE IS IN RAM OUTPUT)

0001101110  0010000000001011    RSYNC  RAM     0,0,13  ;OBTAIN LINE STATE
0001101111  0101000000100011           S/C     5,3     ;CLEAR RAM OUTPUT 00 (RECEIVER ACTIVE)
0001110000  0101000000100001           S/C     5,1     ;CLEAR RAM OUTPUT 01 (RESYNCHRONIZE)
0001110001  0010000110111011           RAM     1,13,13 ;WRITE NEW LINE STATE
0001110010  0111111000101110           BRB     16,RSYNC        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0001110011  0010000000001110    PSI    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0001110100  0101000001000010           S/C     7,4     ;SET RAM OUTPUT 07
0001110101  0010000110111110           RAM     1,13,16 ;WRITE NEW LINE PROTOCOL
0001110110  0111111000110011           BRB     16,PSI  ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0001110111  0101000001000110           S/C     6,6     ;SET RESYNC PULSE
0001111000  0101000000100001           S/C     4,1     ;SET SILO IN
0001111001  0000000100000101           BRA     1,ILOP2 ;TEST FOR SURE TRUE, IF YES BRANCH TO ILOP2 (ILOOP +2)

                                    ;CLEAR TMARK

0001111010  0101000001000001    TMARK  S/C     6,1     ;CLEAR TMARK
0001111011  0000000100001000           BRA     1,ILOP5 ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP +5

                                    ;TEST FOR RESYNC FLAG (LINE NUMBER IN RAM AR, CHARACTER IN ALU RESULT)

0001111100  0000000000111110    TFRF   BRA     0,CRAM7 ;TEST BIT IS OF ALU RESULT, IF YES BRANCH TO HERE +2
0001111101  0000000110000011           BRA     1,DISC  ;TEST FOR SURE TRUE, IF YES BRANCH TO DISCARD RECEIVED CHARACTER
0001111110  0010000000001110    CRAM7  RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0001111111  0101000010000040           S/C     7,0     ;CLEAR RAM OUTPUT 07 (RESYNCH FLAG NOT FOUND)
0010000000  0010000110111110           RAM     1,13,16 ;WRITE NEW LINE PROTOCOL
0010000001  0111111000111110           BRB     16,CRAM7        ;TEST FOR WRITE INHIBIT,IF YES BRANCH BACK
0010000010  0000000110000011           BRA     1,DISC  ;TEST FOR SURE TRUE, IF YES BRANCH TO DISCARD RECEIVED CHARACTER

                                    ;RECEIVED CHARACTER SILO SERVICE

0010000011  0000010100101041    SSERV  BRA     5,ISERV ;TEST FOR SCR08 (COULD HAVE SET BETWEEN 7 AND 9 INST OF ILOOP)
0010000100  0001100001100001           XFR     ,10,1   ;MOVE SILO OUT TO A REGISTER
0010000101  0001000000011111           ALU     3       ;LET ALU RESULT = A REGISTER
0010000110  0011000001100140           XFR     ,0,4    ;MOVE ALU RESULT 08-11 TO RAM ADDRESS REGISTER 00-03
0010000111  0010000000001011           RAM     0,0,13  ;OBTAIN LINE STATE
0010001000  0111000110000011           BRB     1,DISC  ;TEST RAM OUTPUT 01 (RESYNC), IF YES BRANCH TO DISCARD
0010001001  0010000000001110           RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0010001010  0111011100111140           BRB     7,TFRF  ;TEST RAM OUTPUT 07, IF YES BRANCH TO TEST FOR RESYNC FLAG
0010001011  1000100001011001           BRA     14,POER ;TEST BITS  13, 14 OF ALU RESULTS, IF YES BRANCH TO PARITY/OVERRUN
0010001100  0111011010111010           BRB     6,T8C2  ;TEST RAM OUTPUT 06, IF YES BRANCH TO THIS IS BCC 2
0010001101  0111010110100141           BRB     5,T8C1  ;TEST RAM OUTPUT 05, IF YES BRANCH TO THIS IS BCC 1
0010001110  0001000000001101           RAM     0,0,5   ;OBTAIN RECEIVER BYTE COUNT
0010001111  0111110310001140           BRB     14,CR8C0        ;TEST RAM OUTPUT 8-14=0, IF YES BRANCH TO CHARACTER RECEIVED WHILE
0010010000  0010000000001010           RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL IT
0010010001  0111010101111110           BRB     5,DDCMR ;TEST RAM OUTPUT 05, IF YES BRANCH TO DDCMP RECV
0010010010  0010000000001101           RAM     0,0,15  ;OBTAIN RECEIVER MODE BITS
0010010011  0001000010100010    ZETA   XFR     ,12,2   ;MOVE RAM OUTPUT DATA TRANSLATED 8-2/8-10 TO B REGISTER
0010010100  0101000000010111           S/C     0,7     ;CLEAR ALU RESULT UPPER BYTE
0010010101  0011000011110041           XFR     ,17,1   ;MOVE ALU RESULT TO A REGISTER
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0010010110  0001000000010110           ALU     20      ;LET ALU RESULTS = A PLUS B
0010010111  0010000111100010           XFR     ,17,2   ;MOVE ALU RESULTS TO B REGISTER
0010011000  0000000000001001           RAM     0,0,11  ;OBTAIN RECEIVER CONTROL TABLE BASE ADDRESS
0010011001  0011000010110041           XFR     ,13,1   ;MOVE RAM OUTPUT DATA TO A REGISTER (BASE ADDRESS)
0010011010  0000100000010110           ALU     20      ;LET ALU RESULTS = A PLUS B (EFFECTIVE ADDRESS)
0010011011  0011000011110011           XFR     I,17,3  ;MOVE ALU RESULTS TO NPR ADDRESS REGISTER
0010011100  0100000000000040           NPR             ;00 NPR TO GET CONTROL BYTE
0010011101  0111110010111101    RBUS1  BRB     11,RBUS1        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
0010011110  0000011011011010           BRA     6,RNXMC ;TEST NXM, IF YES, BRANCH TO RECEIVER NXM / CONTROL BYTE
0010011111  0111110101101011           BRB     14,RMPEC        ;TEST MEM PAR ERR, IF YES, BRANCH TO RECEIVER MPE/CONTROL BYTE
0011000000  0010000000001111           RAM     0,0,17  ;OBTAIN CONTROL BYTE STORAGE REGISTER (TO CLEAR INTERLOCK)
0011000001  0010000110011111           RAM     1,11,17 ;MOVE DATI REGISTER TO RAM AND WRITE CONTROL BYTE STORAGE REGISTER

                                    ;CONTROL BYTE TESTS BEGIN (CHARACTER IS IN SILO OUT, CONTROL BYTE IS IN RAM 17)

0011000010  0010000000001111    CTEST  RAM     0,0,17  ;OBTAIN CONTROL BYTE STORAGE REGISTER
0011000011  0011000010110010           XFR     ,13,2   ;MOVE RAM OUTPUT TO B REGISTER
0011000100  0000100000000141           ALU     5       ;LET ALU RESULT = B REGISTER
0011000101  0010000101111141           RAM     1,7,15  ;MOVE ALU RESULTS TRANSLATED 5-7/8-2 TO RAM (AND WRITE NEW MODE BITS
0011000110  1000101010101011           BRA     14,CBINT        ;TEST BIT 8 OF ALU RESULT, IF YES BRANCH TO CONTROL BYTE INTERRUPT
0011000111  0000110010011011           BRA     14,EBCC ;TEST BIT 02 OF ALU RESULT, IF YES BRANCH TO SET EXPECT BCC 1 NEXT
0011001000  0000110110000141    EPSIL  BRA     15,RBCC ;TEST BIT 03 OF ALU RESULT, IF YES, BRANCH TO CALCULATE RECV B

                                    ;RETURN FROM RECV BCC  (CONTROL BYTE IS STILL IN ALU RESULT)

0011001001  0000111010000011    RRBCC  BRA     10,DISC ;TEST BIT 4 OF ALU RESULT, IF YES, BRANCH TO (BIT 4 SET = DISC
0011001010  0010000000000140           RAM     0,0,4   ;OBTAIN RECEIVER CURRENT ADDRESS
0011001011  0011001111010011           XFR     0,13,3  ;MOVE RAM OUTPUT TO NPR ADDRESS REGISTER
0011001100  0011000011000141           XFR     ,14,5   ;MOVE SILO OUT TO DATO REGISTER (FOR USE IF NEXT CHARACTER WILL HAVE
0011001101  0100000000000040           NPR             ;00 NPR TO STORE RECEIVED CHARACTER
0011001110  0111110010101110    RBUS2  BRB     11,RBUS2        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
0011001111  0000011011100040           BRA     6,RNXM  ;TEST NXM, IF YES, BRANCH TO RECEIVER NXM
0011010000  0010000000001010    DRBC   RAM     0,0,5   ;OBTAIN RECEIVER BYTE COUNT
0011010001  0011000010110041           XFR     ,13,1   ;MOVE RAM OUTPUT TO REGISTER A
0011010010  0001000000111111           ALU     77      ;LET ALU RESULTS = A+1
0011010011  0010000111110141           RAM     1,17,5  ;MOVE ALU RESULTS TO RAM INPUT (AND WRITE NEW BYTE COUNT)
0011010100  0111111000110040           BRB     16,DRBC ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO  HERE -4
0011010101  0010000000001140    DRC-   RAM     0,0,4   ;OBTAIN RECEIVER CURRENT ADDRESS
0011010110  0011000010110041           XFR     ,13,1   ;MOVE RAM OUTPUT DATA TO REGISTER A
0011010111  0001000000111111           ALU     77      ;LET ALU RESULTS = A+1
0011011000  0010000111110140           RAM     1,17,4  ;MOVE ALU RESULTS TO RAM INPUT (AND WRITE NEW ADDRESS)
0011011001  0111111001110141           BRB     16,DRCA ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
0011011010  0010000000000141           RAM     0,0,5   ;OBTAIN RECEIVER BYTE COUNT
0011011011  0111110010001111           BRB     14,NBC0 ;TEST RAM OUTPUT 8-14=0, IF YES, BRANCH TO NEXT CHARACTER WILL HAVE
0011011100  0101000000010040           S/C     4,0     ;SET SILO OUT
0011011101  0000000100000240           BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                    ;DDCMP RECEPTION

0011011110  0010000000001141    DDCMR  RAM     0,0,15  ;OBTAIN RECEIVER MODE BITS
0011011111  0111110010000041           BRB     14,DDCM2        ;TEST RAM OUTPUT 8-14=0, IF YES BRANCH TO DDCM2
0100000000  0000000101010011           BRA     1,ZETA  ;TEST FOR SURE TRUE, IF YES BRANCH TO ZETA
0100000001  0001000000001140    DDCM2  ALU     14      ;LET ALU RESULT = 0
0100000010  0000000110000141           BRA     1,RBCC  ;TEST FOR SURE TRUE, IF YES BRANCH TO CALCULATE RECV BCC
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                        ;DISCARD RECEIVED CHARACTER

0100000011  0101000000001000W0  DISC    S/C     4,0     ;SET SILO OUT
0100000100  0000000010000000W0          BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                        ;CALCULATE RECV BCC (ASSUME RECEIVED CHARACTER IN SILO OUT)

0100000101  0011000011000001    RBCC    XFR     ,14,1   ;MOVE SILO OUT REGISTER TO A REGISTER
0100000110  0011000000000111            RAM     0,0,7   ;OBTAIN RECV BCC CALCULATED TO DATE
0100000111  0011000010110010            XFR     ,13,2   ;MOVE RAM OUTPUT DATA TO B REGISTER
0100001000  0010000000001010            RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0100001001  0110000000000000            BCC             ;PERFORM SPECIFIED BCC CALCULATION
0100001010  0011000011110111            RAM     1,16,7  ;MOVE BCC TO RAM INPUT AND WRITE NEW RECEIVER BCC
0100001011  0000000101101001            BRA     1,RRBCC ;TEST FOR SURE TRUE, IF YES, BRANCH TO RETURN FROM RECV BCC

                        ;CHARACTER RECEIVED WHILE RECV BC=0

0100001100  0011000011000110    CRBC0   XFR     ,14,6   ;MOVE SILO OUT REGISTER TO RICR
0100001101  0101000000001000            S/C     3,0     ;SET RICR 15 (TO INDICATE RECEPTION WHILE BC=0)
0100001110  1000000110110010            BRA     1,CNAC0 ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY

                        ;NEXT CHARACTER WILL HAVE BC=0  (SILO OUT HAS BEEN SET, RECEIVER BYTE COUNT IS 1

0100001111  0011000011010110    NBC0    XFR     ,15,6   ;MOVE NPR DATO REGISTER TO RICR
0100010000  0101000000001001            S/C     3,1     ;SET RICR 14 (TO INDICATE RECEPTION OF NEXT CHARACTER WILL BE BC=0)
0100010001  0111101110010011            BR8     15,MCBCX        ;TEST RAM OUTPUT 15, IF TRUE BRANCH TO MODE CHANGE / BCC EXPECT
0100010010  1000000110110010            BRA     1,CNAC8 ;TEST FOR SURE TRUE, IF YES BRANCH TO  CREATE NULL ACTION CONTROL B

                        ;MODE CHANGE AND BCC EXPECT

0100010011  0010000000001010    MCBCX   RAM     0,0,13  ;OBTAIN LINE STATE
0100010100  0011000010000010            XFR     ,13,2   ;MOVE RAM OUTPUT TO B REGISTER
0100010101  0011000010000010            XFR     ,10,2   ;MOVE B REGISTER 8-15 TO B REGISTER 0-7
0100010110  0001000000000101            ALU     5       ;LET ALU RESULT = B REGISTER
0100010111  0010000010111111            RAM     1,7,15  ;MOVE ALU RESULTS TRANSLATED TO RAM AND WRITE NEW  RECV MODE BITS
0100011000  0010000011111111            RAM     1,17,17 ;WRITE CONTROL BYTE STORAGE FROM ALU RESULT
0100011001  0000110010100000            BRA     14,EBCN ;TEST ALU RESULT 02, IF YES BRANCH TO EXPECT BCC NEXT BECAUSE OF BC
0100011010  1000000110110010            BRA     1,CNAC8 ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY

                        ;EXPECT BCC NEXT BECAUSE OF CONTROL BYTE

0100011011  0010000000001110    EBCC    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100011100  0101000010000101            S/C     7,5     ;SET RAM OUTPUT 05 (EXPECT BCC 1 NEXT)
0100011101  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL FROM RAM OUTPUT
0100011110  0111111010011011            BR8     10,EBCC ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100011111  0000000101101000            BRA     1,EPSIL ;TEST FOR SURE TRUE, IF YES BRANCH TO EPSIL

                        ;EXPECT BCC NEXT BECAUSE OF BC = 0

0100100000  0010000000001110    EBCN    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100100001  0101000010000101            S/C     7,5     ;SET RAM OUTPUT 05 (EXPECT BCC1 NEXT)
0100100010  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL FROM RAM OUTPUT
0100100011  0111111010100000            BR8     10,EBCN ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO EBCN
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0100100100  0010000011000011            BRA     1,DISC  ;TEST FOR SURE TRUE, IF YES BRANCH TO DISCARD

                        ;THIS IS BCC 1

0100100101  0010000000001110    TBC1    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100100110  0101000010000001            S/C     7,1     ;CLEAR RAM OUTPUT 05 (EXPECT BCC 1 NEXT)
0100100111  0101000010000110            S/C     7,6     ;SET RAM OUTPUT 00 (EXPECT BCC 2 NEXT)
0100101000  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL FROM RAM
0100101001  0111111010010011            BR8     10,TBC1 ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100101010  0011000011000001            XFR     ,14,1   ;MOVE SILO OUT REGISTER TO A REGISTER
0100101011  0010000000000111            RAM     0,0,7   ;OBTAIN RECV BCC CALCULATED TO DATE
0100101100  0011000010110010            XFR     ,13,2   ;MOVE RAM OUTPUT DATA TO B REGISTER
0100101101  0010000000001010            RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0100101110  0110000000000000            BCC             ;PERFORM SPECIFIED BCC CALCULATION
0100101111  0010000011110011            RAM     1,16,7  ;MOVE BCC TO RAM INPUT AND WRITE NEW RECEIVER BCC
0100110000  0010000000001010            RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II (TO LOOK FOR LRC)
0100110001  0111010110110000            BNB     3,TBC1X ;TEST RAM OUTPUT 03
0100110010  0111010010110000            BRB     4,TBC1X ;TEST RAM OUTPUT 04
0100110011  0010000000001110    MRTMA   RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100110100  0101000010000010            S/C     7,2     ;CLEAR RAM OUTPUT 06 (EXPECT BCC2 NEXT)
0100110101  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL
0100110110  0111111010110011            BRB     10,MRTMA        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100110111  0000000110001100            BRA     1,BCCCK ;TEST FOR SURE TRUE, IF YES BRANCH  TO BCC CHECK COMPLETE
0100111000  0101000000010000    TBC1X   S/C     4,0     ;SET SILO OUT
0100111001  0000000100000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                        ;THIS IS BCC 2

0100111010  0010000000001110    TBC2    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100111011  0101000010000010            S/C     7,2     ;CLEAR RAM OUTPUT 06
0100111100  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL
0100111101  0111111010111010            BRB     10,TBC2 ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100111110  0011000011000001            XFR     ,14,1   ;MOVE SILO OUT REGISTER TO A REGISTER
0100111111  0010000000000111            RAM     0,0,7   ;OBTAIN RECV BCC CALCULATED TO DATE
0101000000  0011000010110010            XFR     ,13,2   ;MOVE RAM OUTPUT DATA TO B REGISTER
0101000001  0010000000001010            RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0101000010  0110000000000000            BCC             ;PERFORM SPECIFIED BCC CALCULATION
0101000011  0010000011110011            RAM     1,16,7  ;MOVE BCC TO RAM INPUT AND WRITE NEW RECEIVER BCC
0101000100  0010000000001111    BCCCK   ALU     36      ;LET ALU RESULT = MINUS 1
0101000101  0101000000001111            S/C     4,7     ;CLEAR ALU RESULT UPPER BYTE
0101000110  0011000011110001            XFR     ,17,1   ;MOVE ALU RESULT TO A REGISTER
0101000111  0011000011000010            XFR     ,14,2   ;MOVE SILO OUT TO B REGISTER
0101001000  0000000000001101            ALU     15      ;LET ALU RESULT = AND OF A COMPLEMENT AND B
0101001001  0011000011110010            XFR     ,17,2   ;MOVE ALU RESULT TO B REGISTER
0101001010  0011000011100001            XFR     ,16,1   ;MOVE BCC TO A REGISTER
0101001011  0000000000011111            ALU     37      ;LET ALU RESULT = A
0101001100  0101000000010111            S/C     4,7     ;CLEAR ALU RESULT UPPER BYTE
0101001101  0011000011110001            XFR     ,17,1   ;MOVE ALU RESULT TO A REGISTER
0101001110  0000000000011110            ALU     34      ;LET ALU RESULT= A OR B
0101001111  0010000011110001            XFR     ,17,1   ;MOVE ALU RESULT TO A REGISTER
0101010000  0011000011000010            XFR     ,16,2   ;MOVE BCC TO B REGISTER
0101010001  0011000010000010            XFR     ,10,2   ;MOVE B REGISTER 8-15 TO B REGISTER 0-7 (UPPER BYTE OF BCC)
0101010010  0000000000011110            ALU     34      ;LET ALU RESULT = A OR B
0101010011  0010000011110110            XFR     ,17,6   ;MOVE ALU RESULT TO RICR REGISTER
0101010100  0101000000001101            S/C     3,5     ;SET RICR 12
0101010101  0101000000010001            S/C     3,1     ;SET RICR 14
0101010110  1000000110110010            BRA     1,CNAC8 ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY.
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                        ;RECEIVER MPE / CONTROL BYTE

0|10|0111  0011000011000110  RMPEC  XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
0|10|1000  0101000000011000          S/C     3,4     ;SET RICR 13
0|10|1001  0000000111011011          BRA     1,GAMMA ;TEST FOR SURE TRUE, IF YES BRANCH TO RECEIVER NXM / CONTROL BYTE +

                        ;RECEIVER NXM / CONTROL BYTE

0|10|1010  0011000011000110  RNXMC  XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
0|10|1011  0101000000001101  GAMMA  S/C     3,5     ;SET RICR 12
0|10|1100  0101000000010001  BETA   S/C     3,1     ;SET RICR 14
0|10|1101  0101000000001000          S/C     3,0     ;SET RICR 15
0|10|1110  0101000000001111          S/C     3,7     ;CLEAR NXM
0|10|1111  1000000110110010          BRA     1,CNACB ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY

                        ;RECEIVER NXM (WE GOT HERE FROM RECEIVED CHARACTER SILO SERVICE)

0|11|0000  0011000011000110  RNXM   XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
0|11|0001  0000000111011100          BRA     1,BETA  ;TEST FOR SURE TRUE, IF YES BRANCH TO RECEIVER NXM / CONTROL BYTE +

                        ;NPR SILO OVERFLOW

0|11|0010  0101000000001010  NPRSO  S/C     3,2     ;SET SCR 10 INDICATING NPR SILO OVERFLOW
0|11|0011  0000000100000000          BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                        ;TRANSMIT SERVICE

                        ;CHECK FOR BCC TRANSMISSION

0|11|0100  0010000000001110  TSERV  RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0|11|0101  0011000010110001          XFR     ,13,1   ;MOVE RAM OUTPUT DATA TO A REGISTER
0|11|0110  0000100000011111          ALU     37      ;LET ALU RESULT=A REGISTER
0|11|0111  1000101010010110          BRA     14,SBC1 ;TEST BIT 0 OF ALU RESULT, IF YES BRANCH TO SEND BCC 1
0|11|1000  1000101110100010          BRA     13,SBC2 ;TEST BIT 1 OF ALU RESULT, IF YES BRANCH TO SEND BCC 2
0|11|1001  0000011111100010          BRA     7,NPRSD ;TEST FOR NPR SILO NOT AVAILABLE, IF YES,BRANCH TO NPR SILO OVERFLO

                        ;PRINCIPAL/ALTERNATE SELECTION

0|11|1010  0010000000001011          RAM     0,0,13  ;OBTAIN LINE STATE
0|11|1011  0111001011101101          BRB     2,SIGMA ;TEST BIT 02 OF RAM, IF YES, BRANCH TO HERE +2 (TESTING TRANSMIT GO
0|11|1100  1000000101100100          BRA     1,ITYPE ;TEST FOR SURE TRUE, IF YES BRANCH TO SELECT TYPE OF IDLING
0|11|1101  0111011111110010  SIGMA  BRB     7,USCA  ;TEST RAM OUTPUT 07, IF YES BRANCH TO USE ALTERNATE CA
0|11|1110  0010000000000001          RAM     0,0,1   ;OBTAIN PRINCIPAL BC (GE TEST)
0|11|1111  1111110001000000          BRB     14,XPBCB        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO XMIT PBCO
0|11|0000  0010000000000000          RAM     0,0,0   ;OBTAIN PRINCIPAL CURRENT ADDRESS
0|11|0001  0000000111110101          BRA     1,OXCB  ;TEST FOR SURE TRUE, IF YES BRANCH TO OBTAIN XMIT CONTROL BYTE

                        ;USE ALTERNATE CA

0|11|0010  0010000000000011  USCA   RAM     0,0,3   ;OBTAIN ALTERNATE BC. (GE TEST)
0|11|0011  1111110001010000          BRB     14,XSBCB        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO XMIT SBCO
0|11|0100  0010000000000010          RAM     0,0,2   ;OBTAIN ALTERNATE CURRENT ADDRESS
                        ;OBTAIN XMIT CONTROL BYTE
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0|11|0101  0010000000000011          RAM     0,0,3   ;OBTAIN LINE STATE
0|11|0110  0000000000000000          BRB     2,SIGMA ;TEST BIT 02 OF RAM, IF YES, BRANCH TO HERE +2 (TESTING TRANSMIT GO
0|11|0111  0111001111110111          BRA     1,ITYPE ;TEST FOR SURE TRUE, IF YES BRANCH TO SELECT TYPE OF IDLING
0|11|1000  1000000100001111  SIGMA  BRB     7,USCA  ;TEST RAM OUTPUT 07, IF YES BRANCH TO USE ALTERNATE CA
0|11|1001  0010000000000001          RAM     0,0,1   ;OBTAIN PRINCIPAL BC (GE TEST)
0|11|1010  0000000000000000          BRB     14,XPBCB        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO XMIT PBCO
0|11|1011  0000000000000000          RAM     0,0,0   ;OBTAIN PRINCIPAL CURRENT ADDRESS
0|11|1100  0000000000000000          BRA     1,OXCB  ;TEST FOR SURE TRUE, IF YES BRANCH TO OBTAIN XMIT CONTROL BYTE

                        ;USE ALTERNATE CA

0|11|1101  0010000000000011  USCA   RAM     0,0,3   ;OBTAIN ALTERNATE BC. (GE TEST)
0|11|1110  1111110001010000          BRB     14,XSBCB        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO XMIT SBCO
0|11|1111  0010000000000010          RAM     0,0,2   ;OBTAIN ALTERNATE CURRENT ADDRESS
                        ;OBTAIN XMIT CONTROL BYTE

0|11|0000  0010000000000011  OXCB   XFR     1,13,3  ;MOVE DATA FROM RAM OUTPUT TO NPR ADDRESS REGISTER
0|11|0001  0000000000000000          NPR             ;DO NPR TO GET CHARACTER
0|11|0010  0000000000000000  RBUS3  BRB     11,RBUS3        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
0|11|0011  0000000000000000          BRA     6,TNXMC ;TEST NXM, IF YES, BRANCH TO TRANSMIT NXM/CHARACTER
0|11|0100  0000000000000000          BRB     14,TMPEC        ;TEST MEM PAR ERR, IF YES, BRANCH TO TRANSMIT MPE/CHARACTER
0|11|0101  0000000000000000          XFR     ,11,1   ;MOVE DATA FROM CDC/DATI REGISTER TO A REGISTER
0|11|0110  0000000000000000          ALU     37      ;LET ALU RESULT = A REGISTER
0|11|0111  0000000000000000          XFR     ,17,5   ;MOVE DATA FROM ALU RESULT TO DATO REGISTER (FOR BCC AND TRANSMITTER
0|11|1000  0000000000000000          RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0|11|1001  0000000000000000          BRB     6,ODCMX ;TEST RAM OUTPUT 06, IF YES BRANCH TO ODCMP XMIT (CALCULATE BCC)
0|11|1010  0000000000000000          RAM     0,0,14  ;OBTAIN MODE BITS
0|11|1011  0000000000000000  PI     XFR     ,12,2   ;MOVE RAM OUTPUT DATA TRANSLATED 0-2/8-10 TO B REGISTER
0|11|1100  0000000000000000          ALU     26      ;LET ALU RESULTS = A PLUS B
0|11|1101  0000000000000000          XFR     ,17,2   ;MOVE ALU RESULTS TO B REGISTER
0|11|1110  0000000000000000          RAM     0,0,10  ;OBTAIN CONTROL TABLE BASE ADDRESS
0|11|1111  0000000000000000          XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
0|11|0000  0000000000000000          ALU     20      ;LET ALU RESULT = A PLUS B ((CHAR+MODE)+BASE ADDR)
0|11|0001  0000000000000000          XFR     1,17,3  ;MOVE ALU RESULTS TO NPR ADDRESS REGISTER
0|11|0010  0000000000000000          NPR             ;DO NPR TO GET CONTROL BYTE
0|11|0011  0000000000000000  RBUS4  BRB     11,RBUS4        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
0|11|0100  0000000000000000          BRA     6,TNXMC ;TEST NXM, IF YES, BRANCH TO TRANSMIT NXM/CONTROL BYTE
0|11|0101  0000000000000000          BRB     14,TMPEC        ;TEST MEM PAR ERR, IF YES, BRANCH TO TRANSMIT MPE/CONTROL BYTE
0|11|0110  0000000000000000          XFR     ,11,2   ;MOVE DATI REGISTER TO B REGISTER
0|11|0111  0000000000000000          ALU     5       ;LET ALU RESULT = B REGISTER
0|11|1000  0000000000000000          BRA     13,SDLE ;TEST BIT 1 OF ALU RESULT, IF YES BRANCH TO SEND DLE FIRST.

                        ;RETURN FROM DLE SENDING

1|00|0111  0010000101111100  RDLE   RAM     1,7,14  ;MOVE ALU RESULT TRANSLATED 5-7/0-2 TO RAM (AND WRITE NEW MODE B
1|00|1000  1000110010000010          BRA     14,SSBN ;TEST BIT 2 OF ALU RESULT, IF YES BRANCH TO SET SEND BCC NEXT

                        ;RETURN FROM SSBCNXT

1|00|1001  1000110110001111  RSSBN  BRA     15,XBCC ;TEST BIT 3 OF ALU RESULT, IF YES BRANCH TO CALCULATE TRANS BC

                        ;RETURN FROM XMIT BCC

1|00|1010  1111110000110100  RXBCC  BRB     10,SIDLE        ;TEST FOR DNA FLAG, IF YES BRANCH TO SENT IDLE
1|00|1011  0011000011010000  ALPHA  XFR     ,15,0   ;MOVE DATO REGISTER TO TRANSMITTED DATA BUS
1|00|1100  0010000000001011          RAM     0,0,13  ;OBTAIN LINE STATE
1|00|1101  1111011100100011          BRB     7,USBC  ;TEST BIT 7 OF RAM OUTPUT, IF YES BRANCH TO USE ALTERNATE BC

                        ;USE PRINCIPAL, BC

1|00|1110  0010000000000001  UPBC   RAM     0,0,1   ;OBTAIN PRINCIPAL BYTE COUNT
1|00|1111  1111110001000000          BRB     14,XPBCM        ;TEST RAM 0-14=0
1|00|0000  0011000010110001          XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1|00|0001  0000100000011111          ALU     7       ;LET ALU RESULTS = A PLUS 1
1|00|0010  0010000000000001          RAM     1,17,1  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW PRINCIPAL BYTE COUNT
1|00|0011  0010000000000000          BRB     10,UPBC ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1|00|0100  0011000010110001  OPCA   RAM     0,0,2   ;OBTAIN PRINCIPAL CURRENT ADDRESS
1|00|0101  0000100000011111          XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1|00|0110  0000000000000000          ALU     7       ;LET ALU RESULT = A PLUS 1
1|00|0111  0010000111110000          RAM     1,17,0  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW PRINCIPAL CURRENT ADDRES
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1Ø0011111  1111111000011011        BRB     1Ø,OPCA ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0100000  0010000030000001        RAM     0;0,; ;OBTAIN PRINCIPAL BYTE COUNT
1Ø0100001  1111110001000001        BRB     14,XP8C0        ;TEST RAM 0-14-0, IF YES, BRANCH TO XMIT P8CO
1Ø0100010  0000000100000000        BRA     1;ILOOP ;TEST FOR SURE TRUE AND BRANCH TO IDLE LOOP

                                ;USE ALTERNATE BC

1Ø0100011  0010000000000011    USBC    RAM     0;0,3   ;OBTAIN ALTERNATE BYTE COUNT
1Ø0100100  1111110001010000            BRB     14,XS8C0        ;TEST RAM 0-14=0
1Ø0100101  0011000010110001            XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1Ø0100110  0001000000111111            ALU     7?      ;LET ALU RESULTS = A PLUS 1
1Ø0100111  0010000111110011            RAM     1;17,3  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW ALTERNATE BYTE COUNT
1Ø0101000  1111111000010011            BRB     1Ø,USBC ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0101001  0010000000000010    OSCA    RAM     0;0,2   ;OBTAIN ALTERNATE CURRENT ADDRESS
1Ø0101010  0011000010110001            XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1Ø0101011  0001000000111111            ALU     7/      ;LET ALU RESULT = A PLUS 1
1Ø0101100  0010000111110010            RAM     1;17,2  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW ALTERNATE CURRENT ADDRES
1Ø0101101  1111111000101001            BRB     1Ø,OSCA ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0101110  0010000000000011            RAM     0;0,3   ;OBTAIN ALTERNATE BYTE COUNT
1Ø0101111  1111110001000000            BRB     14,XS8C0        ;TEST RAM 0-14-0, IF YES, BRANCH TO XMIT S8C0
1Ø0110000  0000000100000000            BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;TRANSMIT NXM/CHARACTER  (CURRENT ADDRESS REGISTER ADDRESS IS IN RAM AR)

                                ;TRANSMIT NXM/CONTROL BYTE  (CONTROL TABLE BASE ADDRESS REGISTER ADDRESS IS IN R

1Ø0110001  0011000000000111    TNXMC   XFR     ,Ø,7    ;MOVE  TO NPR STATUS REPORT REG.
1Ø0110010  0010000000001011    IOTA    RAM     0;0,13  ;OBTAIN LINE STATE
1Ø0110011  0101000010000111            S/C     7;7     ;SET RAM 04 (TRANSMITTER NXM)
1Ø0110100  0101000000001111            S/C     3;7     ;CLEAR NXM
1Ø0110101  0101000000100010            S/C     5;2     ;CLEAR RAM 02 (TRANSMITTER GO)
1Ø0110110  0010000110111011            RAM     1;13,13 ;WRITE NEW LINE STATE
1Ø0110111  1111111000110010            BRB     1Ø,IOTA ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO IOTA
1Ø0111000  0000000100000000            BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;TRANSMIT MPE/CHARACTER   (CURRENT ADDRESS REGISTER ADDRESS IS IN RAM AR)

                                ;TRANSMIT MPE/CONTROL BYTE  (CONTROL TABLE BASE ADDRESS REGISTER ADDRESS IS IN R

1Ø0111001  0011000000000111    TMPEC   XFR     ,Ø,7    ;MOV.  TO NPR STATUS REPORT REG.
1Ø0111010  0010000000001011    OMEGA   RAM     0;0,13  ;OBTAIN LINE STATE
1Ø0111011  0101000010000101            S/C     7;5     ;SET RAM 05 (TRANSMIT MPE)
1Ø0111100  0101000000100010            S/C     5;2     ;CLEAR RAM 02 (TRANSMITTER GO)
1Ø0111101  0010000110111011            RAM     1;13,13 ;WRITE NEW LINE STATE
1Ø0111110  1111111000111010            BRB     1Ø,OMEGA        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0111111  0000000100000000            BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES, BRANCH TO IDLE LOOP

                                ;XMIT PBCØ

1Ø1000000  0010000000001011    XPBC0   RAM     0;0,13  ;OBTAIN LINE STATE
1Ø1000001  0101000010000100            S/C     7;4     ;SET RAM OUTPUT BIT 7 (GO TO ALTERNATE)
1Ø1000010  0010000110111011            RAM     1;13,13 ;MOVE RAM OUTPUT TO RAM (AND WRITE NEW LINE STATE)
1Ø1000011  1111111001000000            BRB     1Ø,XPBC0        ;TEST FOR WRITE INHIBT, IF YES BRANCH TO HERE -3
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1Ø1000100  0010000000000001            RAM     0;0,1   ;OBTAIN PRINCIPAL BYTE COUNT
1Ø1000101  0[illegible]0000000111      XFR     ,Ø,7    ;MAKE NPR SILO ENTRY
1Ø1000110  1111101101001000            BRB     15,RED  ;TEST RAM OUTPUT BIT 15, IF YES BRANCH TO HERE +2
1Ø1000111  1000000010101011            BRA     1;CBC0  ;TEST FOR SURE TRUE, IF YES BRANCH TO CHECK FOR BOTH BC=0
1Ø1001000  0010000100000001    RED     RAM     1;0,1   ;ZERO PRINCIPAL BYTE COUNT
1Ø1001001  0010000000001110    OTMB    RAM     0;0,16  ;OBTAIN  LINE PROTOCOL
1Ø1001010  0011000010110010            XFR     ,13,2   ;MOVE RAM OUTPUT TO REGISTER B
1Ø1001011  0011000010000010            XFR     ,10,2   ;MOVE REGISTER B8-15 TO REGISTER B 0-7
1Ø1001100  0001000000000101            ALU     5       ;LET ALU RESULT = B
1Ø1001101  0010000101111100            RAM     1;7,14  ;MOVE ALU RESULTS TRANSLATED  TO RAM AND WRITE NEW MODE BITS
1Ø1001110  1000110010000111            BRA     14,BCBSB        ;TEST  ALU RESULT B2, IF YES BRANCH TO BC0 SEND BCC
1Ø1001111  1000000101010111            BRA     1;CBC0  ;TEST FOR SURE TRUE, IF YES BRANCH TO CHECK FOR BOTH BC=0

                                ;XMIT S8CO

:Ø1010000  0011000000001011    XS8C0   RAM     0;0,13  ;OBTAIN LINE STATE
1Ø1010001  0101000010000100            S/C     7;0     ;CLEAR RAM OUTPUT BIT 7 (GO TO PRINCIPAL)
1Ø1010010  0010000110111011            RAM     1;13,13 ;MOVE RAM OUTPUT TO RAM (AND WRITE NEW LINE STATE)
1Ø1010011  1111111001010000            BRB     1Ø,XS8C0        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -3
1Ø1010100  0010000000000011            RAM     0;0,3   ;OBTAIN ALTERNATE BYTE COUNT
1Ø1010101  0011000000000111            XFR     ,Ø,7    ;MAKE NPR SILO ENTRY
1Ø1010110  1111101101011001            BRB     15,ES8  ;TEST RAM OUTPUT 15, IF YES, BRANCH TO CLEAR ALTERNATE BYTE COUNT

                                ;CHECK FOR BOTH BC=0

1Ø1010111  0010000000000001    CBC0    RAM     0;0,1   ;OBTAIN PRINCIPAL BYTE COUNT
1Ø1011000  1111110001011010            BRB     14,DELTA        ;TEST RAM OUTPUT 0-14-0, IF YES, BRANCH TO HERE +2
1Ø1011001  0000000100000000            BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES, BRANCH TO IDLE LOOP
1Ø1011010  0010000000000011    DELTA   RAM     0;0,3   ;OBTAIN ALTERNATE BYTE COUNT
1Ø1011011  1111110001011111            BRB     14,C/GO ;TEST RAM OUTPUT 0-14-0, IF YES, BRANCH TO CLEAR GO
1Ø1011100  0000000100000000            BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;CLEAR ALTERNATE BYTE COUNT

1Ø1011101  0010000100000011    ES8     RAM     1;0,3   ;ZERO ALTERNATE BYTE COUNT
1Ø1011110  1000000101001001            BRA     1;OTMB  ;TEST FOR SURE TRUE, BRANCH TO OTMB

                                ;CLEAR GO

1Ø1011111  0010000000001011    C/GO    RAM     0;0,13  ;OBTAIN LINE STATE
1Ø1100000  0101000000100010            S/C     5;2     ;CLEAR RAM B2 (TRANSMITTER GO)
1Ø1100001  0010000110111011            RAM     1;13,13 ;WRITE NEW LINE STATE
1Ø1100010  1111111001011111            BRB     1Ø,C/GO ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -3
1Ø1100011  0000000100000000            BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;SELECT TYPE OF IDLE

1Ø1100100  0010000000001010    ITYPE   RAM     0;0,12  ;OBTAIN TRANSMITTER DLE/PROTOCOL II
1Ø1100101  1111000001100111            BRB     0;BCBCC ;TEST RAM OUTPUT B8, IF YES BRANCH TO BCBCC
1Ø1100110  0000000100000000            BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP
1Ø1100111  0101000000100101    BCBCC   S/C     6;5     ;SET TMARK
1Ø1101000  0C0000001000000Ø            BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;SENT IDLE  (LINE STATE IS IN RAM OUTPUT)

1Ø1101001  0010000000001011    SIDLE   RAM     0;0,13  ;OBTAIN LINE STATE
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1Ø1101010  0101000000100100        S/C     5,4     ;SET RAM Ø3 (TRANSMITTER UNDERRUN)
1Ø1101011  0010000110111011        RAM     1,13,13 ;MOVE RAM OUTPUT TO RAM (AND WRITE NEW LINE STATE)
1Ø1101100  1111111001101001        BRB     1Ø,SIDLE        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -3
1Ø1101101  1000000100010010        BRA     1,ALPHA ;TEST FOR SURE TRUE, IF YES, BRANCH TO RETURN FROM XMIT BCC +3

                                   ;SENT IDLE/DLE

1Ø1101110  0010000000001011        MU      RAM     Ø,Ø,13  ;OBTAIN LINE STATE
1Ø1101111  0101000000100100        S/C     5,4     ;SET Ø3 (UNDERRUN)
1Ø1110000  0010000110111011        RAM     1,13,13 ;WRITE LINE STATE
1Ø1110001  1111111001101110        BRB     1Ø,MU   ;TEST FOR INHIBIT
1Ø1110010  1000000101111011        BRA     1,NU    ;GO BACK TO SEND IDLE

                                   ;SEND DLE FIRST

                                   ;(WE GOT HERE FROM TRANSMIT SERVICE.  THE CONTROL BYTE IS
                                   ;IN ALU RESULT AND B REGISTER.  MASTER SCAN POSITION IS IN
                                   ;RAM ADDRESS REGISTER Ø-3).

1Ø1110011  0010000000001110        SDLE    RAM     Ø,Ø,16  ;OBTAIN LINE PROTOCOL
1Ø1110100  1111001001111101        BRB     2,CRAM2 ;TEST RAM OUTPUT Ø2, IF YES BRANCH TO CLEAR RAM Ø2
1Ø1110101  0101000000100110        S/C     5,6     ;SET RAM Ø2
1Ø1110110  0010000110111110        RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT AND WRITE NEW LINE PROTOCOL
1Ø1110111  1111111001110011        BRB     1Ø,SDLE ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
1Ø1111000  0010000000001010        RAM     Ø,Ø,12  ;OBTAIN TRANSMITTER DLE / LINE PROTOCOL II
1Ø1111001  0011000010110010        XFR     ,13,2   ;MOVE RAM OUTPUT TO REGISTER B
1Ø1111010  1111100001101110        BRB     1Ø,MU   ;TEST FOR DMA FLAG, IF YES BRANCH TO SENT IDLE/DLE
1Ø1111011  0011000010000000        NU      XFR     ,1Ø,Ø   ;MOVE REGISTER B 15-8 TRANSMITTED DATA BUS
1Ø1111100  0000000100000000        BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                   ;CLEAR RAM Ø2 (RAM Ø2 IS DLE SENDING IN PROGRESS)

1Ø1111101  0010000000001110        CRAM2   RAM     Ø,Ø,16  ;OBTAIN LINE PROTOCOL
1Ø1111110  0101000000100010        S/C     5,2     ;CLEAR RAM OUTPUT Ø2
1Ø1111111  0010000110111110        RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT DATA AND WRITE NEW LINE PROTOCOL
11ØØØØØØØ  1111111001111101        BRB     1Ø,CRAM2        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11ØØØØØØ1  1000000100001110        BRA     1,RDLE  ;TEST FOR SURE TRUE, IF YES BRANCH TO RETURN FROM DLE SENDING

                                   ;SET SEND BCC NEXT

11ØØØØØ1Ø  0010000000001110        SSBN    RAM     Ø,Ø,16  ;OBTAIN LINE PROTOCOL
11ØØØØØ11  0101000000100111        S/C     5,7     ;SET RAM OUTPUT BIT Ø
11ØØØØ1ØØ  0010000110111110        RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT AND WRITE NEW LINE PROTOCOL
11ØØØØ1Ø1  1111111001000010        BRB     1Ø,SSBN ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11ØØØØ110  1000000100010000        BRA     1,RSSBN ;TEST FOR SURE TRUE, IF YES BRANCH TO RETURN FROM SSBCCNXT

                                   ;BCC SEND BCC

11ØØØØ111  0010000000001110        BCCSB   RAM     Ø,Ø,16  ;OBTAIN LINE PROTOCOL
11ØØØ1ØØØ  0101000000100111        S/C     5,7     ;SET RAM OUTPUT BIT Ø
11ØØØ1ØØ1  0010000110111110        RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT AND WRITE NEW LINE PROTOCOL
11ØØØ1Ø1Ø  1111111010000111        BRB     1Ø,BCCSB        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11ØØØ1Ø11  1000000101010111        BRA     1,CBCC  ;TEST FOR SURE TRUE, IF YES BRANCH TO CBCC
```
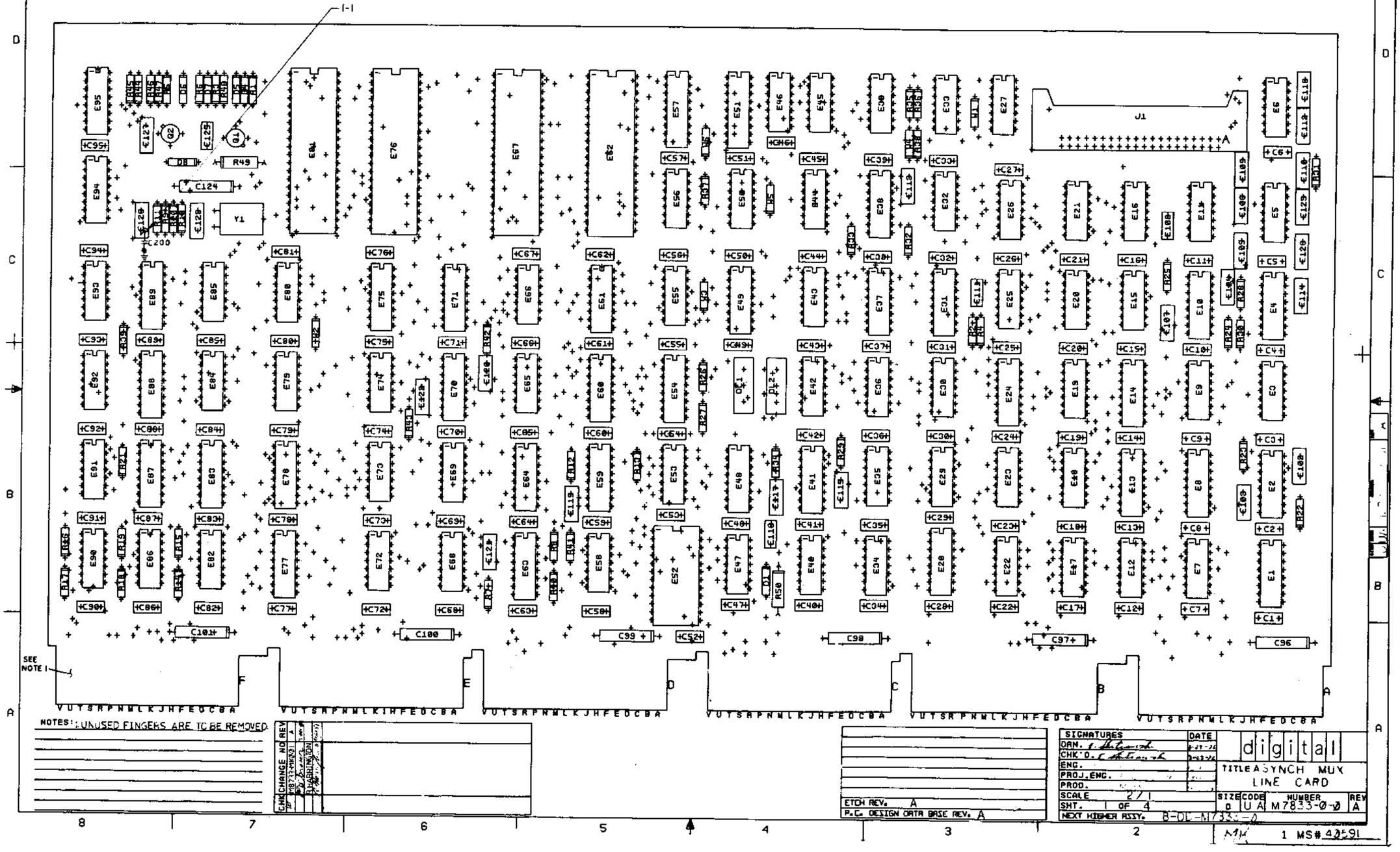



```
                                   ;DDCMP TRANSMIT

11ØØØ1100  ...*000000001100        DDCMX   RAM     Ø,Ø,14  ;OBTAIN TRANSMITTER MODE BITS
11ØØØ1101  1111110010001111        BRB     14,XBCC ;TEST RAM Ø-14=Ø, IF YES BRANCH TO XBCC
11ØØØ1110  1000000100000000        BRA     1,PI    ;TEST FOR SURE TRUE, IF YES BRANCH TO PI

                                   ;CALCULATE TRANSMITTER BCC

11ØØØ1111  0011000011010001        XBCC    XFR     ,15,1   ;MOVE DATO REGISTER TO A REGISTER
11ØØ1ØØØØ  0010000000000110        RAM     Ø,Ø,6   ;OBTAIN TRANSMITTER BCC CALCULATED TO DATE
11ØØ1ØØØ1  0011000010110010        XFR     ,13,2   ;MOVE RAM DATA TO REGISTER B
11ØØ1ØØ1Ø  0010000000001010        RAM     Ø,Ø,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
11ØØ1ØØ11  0110000000000000        BCC             ;PERFORM SPECIFIED BCC CALCULATION
11ØØ1Ø1ØØ  0010000111100110        RAM     1,16,6  ;MOVE BCC TO RAM INPUT AND WRITE NEW TRANSMITTER BCC
11ØØ1Ø1Ø1  1000000100010001        BRA     1,RXBCC ;TEST FOR SURE TRUE, IF YES, BRANCH TO RETURN FROM XMIT BCC

                                   ;SEND BCC 1

                                   ;(WE GOT HERE FROM TRANSMIT SERVICE.  THE MASTER SCAN POSITION
                                   ;IS IN THE RAM ADDRESS REGISTER Ø-3.  THE LINE PROTOCOL IS IN
                                   ;THE A REGISTER AND THE ALU RESULT REGISTER.)

11ØØ1Ø110  0010000000001110        SBC1    RAM     Ø,Ø,16  ;OBTAIN LINE PROTOCOL
11ØØ1Ø111  0011000011010001        XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
11ØØ11ØØØ  0001000000111111        ALU     7/      ;LET ALU RESULT = A PLUS 1
11ØØ11ØØ1  0010000111111110        RAM     1,17,16 ;MOVE ALU RESULT TO RAM INPUT DATA AND WRITE NEW LINE PROTOCOL
11ØØ11Ø1Ø  1111111010010110        BRB     1Ø,SBC1 ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11ØØ11Ø11  0010000000000110        RAM     Ø,Ø,6   ;OBTAIN TRANSMITTER BCC
11ØØ111ØØ  0011000010110000        XFR     ,13,Ø   ;MOVE RAM OUTPUT DATA TO TRANSMITTED DATA BUS (HIGH ORDER BITS GO INT
11ØØ111Ø1  0010000000001010        RAM     Ø,Ø,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II (TO LOOK FOR LRC)
11ØØ111Ø1  1111001112100001        BRB     3,GOIDL ;TEST RAM OUTPUT Ø3, IF YES BRANCH TO HERE +4
11ØØ11111  1111010012100001        BRB     4,GOIDL ;TEST RAM OUTPUT Ø4, IF YES BRANCH TO HERE +3
11Ø1ØØØØØ  1000000110100101        BRA     1,C/LU1 ;TEST FOR SURE TRUE, IF YES BRANCH TO SEND BCC 2 + 6
11Ø1ØØØØ1  0000000100000000        GOIDL   BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                   ;SEND BCC2

                                   ;(WE GOT HERE FROM TRANSMIT SERVICE.  THE MASTER SCAN POSITION
                                   ;IS IN THE RAM ADDRESS REGISTER Ø-3.  THE LINE PROTOCOL IS IN
                                   ;THE A REGISTER AND IN THE ALU RESULT REGISTER.)

11Ø1ØØØ1Ø  0010000000000110        SBC2    RAM     Ø,Ø,6   ;OBTAIN TRANSMITTER BCC
11Ø1ØØ011  0011000010110010        XFR     ,13,2   ;MOVE RAM OUTPUT DATA TO REGISTER B
11Ø1ØØ1ØØ  0011000010000000        XFR     ,1Ø,Ø   ;MOVE REGISTER B 8-15/Ø-7 TO TRANSMITTED DATA BUS

11Ø1ØØ101  0010000100000110        C/LU1   RAM     1,Ø,6   ;MOVE ZERO TO RAM INPUT DATA AND WRITE ZERO TRANSMITTER BCC
11Ø1ØØ11Ø  0010000000001110        RAM     Ø,Ø,16  ;OBTAIN LINE PROTOCOL
11Ø1ØØ111  0101000000100001        S/C     5,1     ;CLEAR RAM BIT Ø1 (SEND BCC 2)
11Ø1Ø1ØØØ  0010000110111110        RAM     1,13,16 ;MOVE RAM INPUT TO RAM INPUT DATA AND WRITE NEW LINE PROTOCOL
11Ø1Ø1ØØ1  1111111010010101        BRB     1Ø,C/LU1        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø1Ø1Ø1Ø  0000000100000000        BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP
```

```
                                        ;RECEIVED ERRORS

                                        ;CONTROL BYTE INTERRUPT

1 1 0 1 0 1 0 1 1   0 0 1 0 0 0 0 0 0 0 0 0 0 1 1 1 1   CBINT  RAM     0,0,17  ;READ CONTROL BYTE HOLDING REGISTER
1 1 0 1 0 1 1 0 0   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 1 1           S/C     5,3     ;CLEAR RAM 00 (GENERATE INTERRUPT)
1 1 0 1 0 1 1 0 1   0 0 1 0 0 0 0 0 1 1 0 1 1 1 1 1 1           RAM     1,13,17 ;WRITE CONTROL BYTE HOLDING REGISTER
1 1 0 1 0 1 1 1 0   0 0 1 1 0 0 0 0 0 1 1 0 0 0 1 1 0           XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
1 1 0 1 0 1 1 1 1   0 1 0 1 0 0 0 0 0 0 0 0 1 0 1 1 1           S/C     3,3     ;SET SCR07 (RECEIVER INTERRUPT)
1 1 0 1 1 0 0 0 0   0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0           BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                        ;PARITY AND OVERRUN ERRORS

1 1 0 1 1 0 0 0 1   0 0 1 1 0 0 0 0 1 1 0 0 0 1 1 0         POER    XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER

                                        ;CREATE NULL ACTION CONTROL BYTE (MODE IS PRESERVED)

1 1 0 1 1 0 0 1 0   0 0 1 0 0 0 0 0 0 0 0 0 0 1 1 1 1   CNACB  RAM     0,0,17  ;READ CONTROL BYTE HOLDING REGISTER
1 1 0 1 1 0 0 1 1   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 1 1           S/C     5,3     ;CLEAR RAM 00
1 1 0 1 1 0 1 0 0   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 0 1           S/C     5,1     ;CLEAR RAM 01
1 1 0 1 1 0 1 0 1   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 1 0           S/C     5,2     ;CLEAR RAM 02
1 1 0 1 1 0 1 1 0   0 1 0 1 0 0 0 0 0 0 0 1 0 0 0 0 0           S/C     5,0     ;CLEAR RAM 03
1 1 0 1 1 0 1 1 1   0 1 0 1 0 0 0 0 0 0 1 0 0 0 1 1 1           S/C     7,7     ;SET RAM OUTPUT 04 (DISCARD)
1 1 0 1 1 1 0 0 0   0 0 1 0 0 0 0 0 1 1 0 1 1 1 1 1 1           RAM     1,13,17 ;WRITE CONTROL BYTE HOLDING REGISTER FROM RAM OUTPUT
1 1 0 1 1 1 0 0 1   0 1 0 1 0 0 0 0 0 0 0 0 1 0 1 1 1           S/C     3,3     ;SET SCR 07 (RECEIVER INTERRUPT)
1 1 0 1 1 1 0 1 0   0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0           BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                        ;END
```

COMPONENT SIDE VIEW



NOTES: 1. UNUSED FINGERS ARE TO BE REMOVED.

CHK	CHANGE NO	REV
	V8713-HW001	A

ETCH REV. A
P.C. DESIGN DATA BASE REV. A

SIGNATURES	DATE
DRN.	
CHK'D.	
ENG.	
PROJ.ENG.	
PROD.	
SCALE 2/1	
SHT. 1 OF 4	
NEXT HIGHER ASSY. B-DC-M7833-0	

digital

TITLE ASYNCH MUX LINE CARD

SIZE	CODE	NUMBER	REV
D	UA	M7833-0-0	A

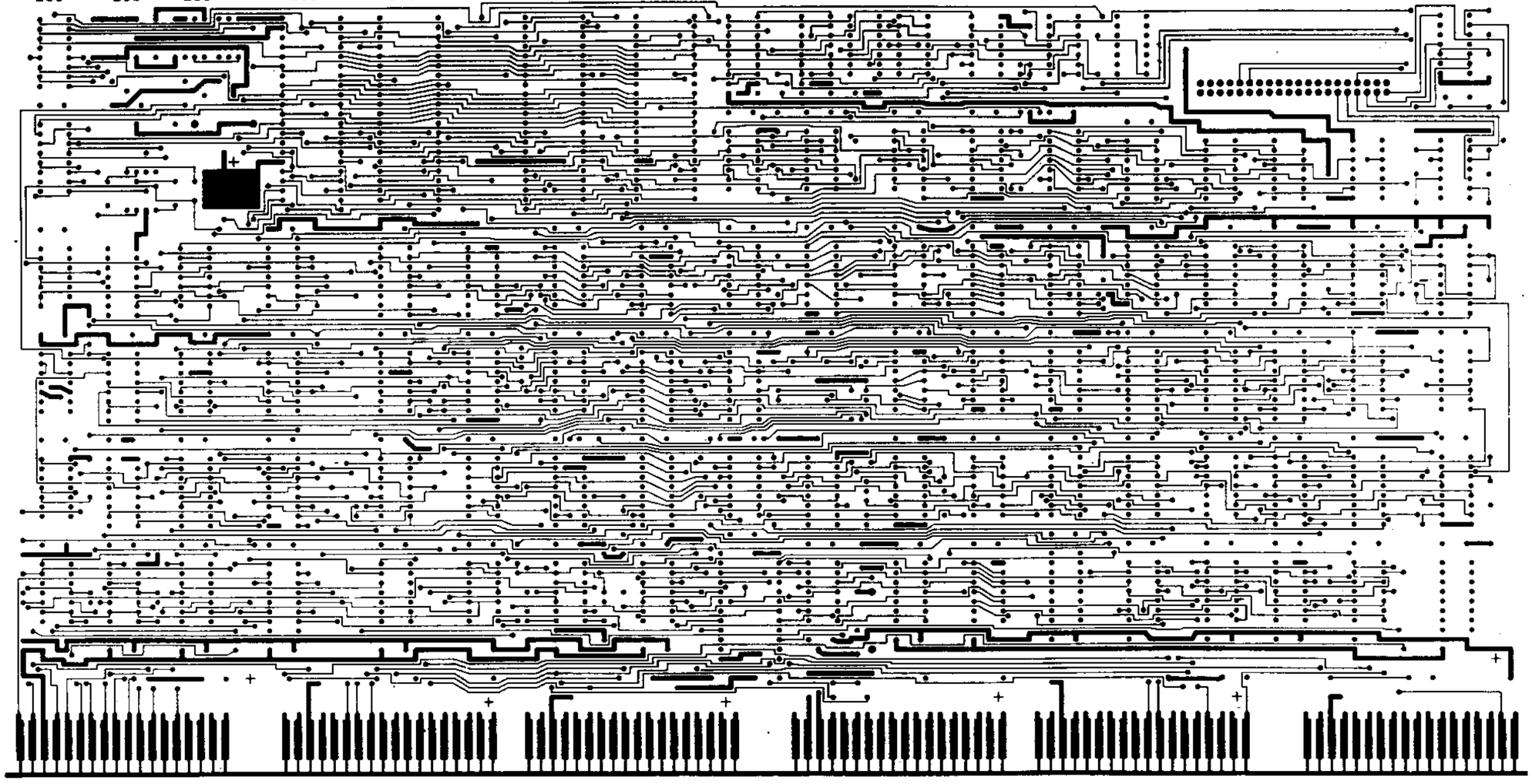
1 MS# 40591

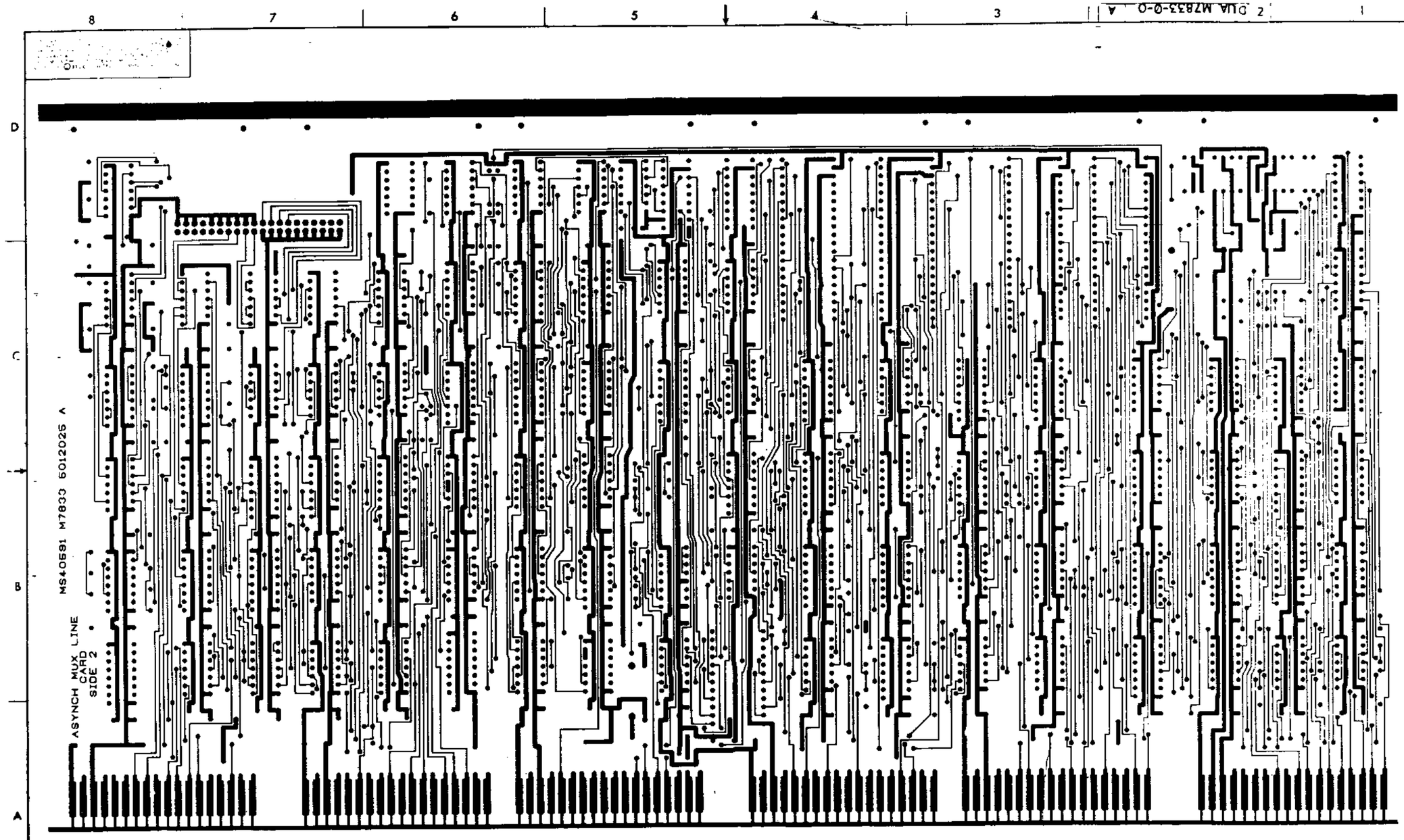
CS*ABCDEFHJKLMNPRS

SIDE 1

digital

E95 E89 E86 E81 E76 E67 E62 E57 E51 E48 E45 E39 E33 E27 E21 E16 E11 E6





REVISIONS		
CHK	CHANGE NO	REV

TITLE: ASYNCH MUX LINE CARD DUA M7833-0-0 A

SCALE: 2/1 SHEET 3 OF 4

DUA M7833-0-0 A

REWORK INSTRUCTIONS

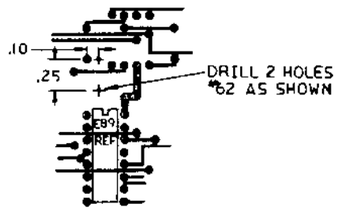


FIG 1
COMPONENT SIDE VIEW
SCALE-NONE

ECO* M7833-MK00J

1-1 DRILL TWO HOLES #62 AS SHOWN IN FIGURE 1. INSERT C200 IN HOLES. BEND AND SOLDER TOP LEAD TO ETCH CONNECTING C126 TO R11. BEND AND SOLDER BOTTOM LEAD TO GROUND ETCH FROM E89 PIN 8, AS SHOWN IN FIGURE 2.

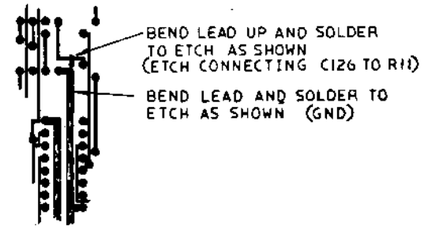


FIG. 2
SOLDER SIDE VIEW
SCALE - NONE

REVISIONS
CHK | CHANGE NO. | REV.

TITLE: ASYNCH MUX LINE CARD
SIZE: D | CODE: DUA | NUMBER: M7833-0-0 | REV: A
SCALE: NONE | SHEET 4 OF 4 | DIST.
MK

REV. A
DUA M7833-0-0

AUTOMATED BY PRTLST.3P(44)

P A R T S L I S T

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
1	1	D-MD-5012025-0-0	5012025-00	M7833-ETCH BD	1	
2	2		1002427-00	15.0 MMF 100V 5%200PPM MICA	2	C115,C122
3	3		1005820-00	22.0 MMF 100V 5%200PPM MICA	3	C123,C126,C200
4	4		1001739-00	27.0 MMF 100V 5%200PPM MICA	5	C102,C103,C104,C107,C121
5	5		1000012-00	56.0 MMF 100V 5%200PPM MICA	1	C120
6	6		1000006-00	10.0 MMF 100V 5%200PPM MICA	1	C114
7	7		1000019-00	150.0 MMF 100V 5%200PPM MICA	1	C113
8	8		1000020-00	180.0 MMF 100V 5%200PPM MICA	1	C117
9	9		1000024-00	470.0 MMF 100V 5%200PPM MICA	8	C105,C106,C109,C110,C112,C118,
10	10		1000042-00	1000.0 MMF 100V 5%200PPM MICA	1	CONT C128,C129 C127
11	11		1001610-01	.01 MFD50/100V +80-20% DISC	99	C1-C95,C111,C125,C108,C116
12	12		1005306-00	6.8MFD 35V 10% S.TANT	7	C96-C101,C124
13	13		1000016-00	100.0 MMF 100V 5%200PPM MICA	1	C119
14	14		1102808-00	1N 752A VZ= 5.6 5% .40W	1	D8
15	15		1105275-00	D 672 TR= 15NS PIV= 60V SI	4	D4-D7
16	16		1110836-00	1N 759A VZ= 12.0 5% .40W	1	D1
17	17		1209941-02	HEADER 100 40POS RT ANGLE	1	J1
18	18		1216988-02	HANDLE,MODULE,HEX TWO EJECTORS	1	
19	19		1301317-00	10.0 .25 W 5.0 % CC	4	R44-R47
20	20		1300271-00	220.0 .25 W 5.0 % CC	1	R48
21	21		1300295-00	330.0 .25 W 5.0 % CC	2	R1,R2
22	22		1300309-00	390.0 .25 W 5.0 % CC	2	R26,R39
23	23		1300316-00	470.0 .25 W 5.0 % CC	2	R27,R40
24	24		1300315-00	470.0 .50 W 5.0 % CC	1	R49
25	25		1301401-00	750.0 .25 W 5.0 % CC	2	R3,R4
26	26		1300365-00	1.0 K .25 W 5.0 % CC	18	R5,R6,R11-R21,R31,R35-R38
27	27		1300479-00	10.0 K .25 W 5.0 % CC	17	R7-R10,R22-R25,R28-R30,R32-R34,
28	28		1302336-00	39.0 .50 W 5.0 % CC	1	CONT R41-R43 R50

REVISION HISTORY			BASIC PART NO: M7833
ENG	ECO NUMBER	REV	SECTION A OF A
RH	M8733-MK001	A	SECTION.VARIATION INDEX [A] 00 [B] [C] [D] [E] [F] [H] [J] [K] [L] [M] [N]

DRN: B.FRASER	DATE: 15-DEC-80	D I G I T A L
CHK'D: J.FALKOWSKI	DATE: 15-DEC-80	TITLE: PARTS LIST ASYN MUX LINE CARD
DES.ENG: W.SMITH	DATE: 15-DEC-80	
RESP.ENG.: R.HARRINGTON (R. Harrington 6 MAR 81)	DATE: 15-DEC-80	DOCUMENT NUMBER
MFG.ENG.: R.WALL	DATE: 15-DEC-80	SIZE: K / CODE: PL / NUMBER: M7833-0-0 / REV: A
ASSEMBLY NUMBER: D-UA-M7833-0-0	TOP DOCUMENT NUMBER: #B-DD-M7833-0	FILE NAME: MK0296.PLS / EDIT #: 3

MK

AUTOMATED BY PRTLST.3P(44) P A R T S L I S T SHEET A2 OF A2

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY PER VARIATION 00	REFERENCE DESIGNATOR
29	29		1501742-00	DEC2904 PNP 600MW SI 40 40 P	1	Q1
30	30		1503409-00	DEC6534D PNP 310MW SI 40 90	1	Q2
31	31		1605528-00	DELAY= 30NS,0TAPS DL5184	2	DL1,DL2
32	32		1811660-02	OSCILLATOR, XTAL 5.0688 MHZ	1	E27
33	33		1812396-00	XTAL 2.4576 MHZ	1	Y1
34	34		1909701-00	74154 1 OF 16,BINA	1	E52
35	35		1910436-00	DEC 74123 ONE SHOT-DUAL,RETRIG	8	E2,E4,E10,E38,E41,E59,E63,E70
36	36		1905575-00	7400 NAND GATE-QUAD 2IN	1	E68
37	37		1909686-00	7404 INVERTER GATE-HEX 1I	7	E7,E47,E53,E58,E66,E73,E80
38	38		1910091-00	DEC 7437 AND GATE-QUAD 2IN,BU	3	E12,E40,E46
39	39		1910651-00	DEC 74175 FF-D QUAD	6	E8,E13,E14,E24,E49,E88
40	40		1905547-00	7474 FF-D DUAL,EDGE TRIGG	13	E15,E23,E25,E26,E29,E34-E36,E44,
					CONT	E45,E55,E74,E84
41	41		1909937-00	74153 MUX 1 OF 4 (DUAL)	4	E37,E71,E75,E83
42	42		1910656-00	74155 DECODER-2 OF 4(DUAL)	4	E31,E60,E61,E89
43	43		1911521-00	7432 OR GATE-QUAD 2IN, PO	3	E3,E22,E72.
44	44		1909705-00	DEC 8881 NAND GATE-QUAD 2IN O	4	E82,E86,E90,E91
45	45		2112623-00	DUAL BAUD RATE GEN/PROG DIVIDER,	2	E51,E57
46	46		1905577-00	7420 NAND GATE-DUAL 4INPU	1	E39
47	47		1910390-00	DEC 7380 NOR GATE-QUAD 2IN,FA	1	E93
48	48		1910837-00	8093 BUFFER CATE-QUAD 2IN	2	E18,E50
49	49		1912666-00	BUFFER GATE-QUAD 2IN	2	E17,E56
50	50		1909054-00	7493 COUNTER,ASYNCH UP,BI	1	E92
51	51		1910655-00	74157 MUX 2 TO 1 QUAD	1	E64
52	52		1909267-00	DEC 74H11 AND GATE-TRIPLE 3INP	2	E33,E69
53	53		1910738-00	DEC 74170 MEMORY READ/WRITE	5	E54,E77,E78,E94,E95
54	54		1910155-00	DEC 7408 AND GATE,POS.QUAD 2I	7	E9,E19,E20,E30,E32,E42,E85
55	55		1910454-00	DEC 9318 ENCODER, 8 INPUT PRI	2	E48,E87
56	56		1910322-00	DEC 1488L DRIVER,LINE,QUAD,EI	2	E11,E16
57	57		1909004-00	DEC 7402 NOR GATE-QUAD 2IN	2	E21,E43
58	58		1910323-00	DEC 1489L RECEIVER,LINE,QUAD,	2	E5,E6
59	59		1909713-00	DEC 8815 NOR GATE-DUAL 4IN	2	E65,E79
60	60		2111450-00	UART 40K BAUD VARIATION OF 19-10	4	E62,E67,E76,E81
61	61		9008351-00	CAP,TRANSISTOR .320 ID	1	
62	62		9009185-00	JUMPER, WIRE, INSULATED, BLACK B	6	W1-W6
63	63		9000024-01	EYELET, ROLLED FLANGE, .121 OD X	12	

D	I	G	I	T	A	L	TITLE	SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							ASYN MUX LINE CARD		K	PL	M7833-0-0	A

MK

BERG CONNECTOR

J1

- A — DATA SET BUSY ØØ
- B — DATA SET BUSY Ø1
- D — DATA SET BUSY Ø2
- E — ASYN H
- F — DATA SET BUSY Ø3
- H — EIA RCV DATA ØØ
- J — EIA RCV DATA Ø1
- X — EIA XMIT DATA ØØ
- L — EIA XMIT DATA Ø1
- M — DVII BUSY ØØ
- N — DVII BUSY Ø1
- P — DVII BUSY Ø2
- R — DVII BUSY Ø3
- S — EIA XMIT DATA Ø2
- T — EIA XMIT DATA Ø3
- U — EIA RCV DATA Ø2
- V — EIA RCV DATA Ø3
- W — GND
- AA — GND
- BB — GND
- CC — GND
- DD — GND
- EE — GND
- FF — GND
- HH — GND
- JJ — GND
- KK — GND
- LL — GND
- MM — GND
- NN — GND
- PP — GND
- RR — GND
- SS — GND
- TT — GND
- UU — GND
- VV — GND

+5V — R1 330 — +3VA — C125 .Ø1 µfd — R3 75Ø

+5V — R2 33Ø — +3VB — C111 Ø1.µfd — R4 75Ø

+15V — CU1 — R5Ø 39 1/2W — D4-1 +12V (TO PIN 9 OF 5Ø16) (TO PIN 14 OF 1488) — D1 IN759A — C116 Ø1.µfd — C1Ø8 .Ø1µfd

-15V — FB2 — Q1 2N2Ø4 — R44 1Ø — R45 1Ø — R46 1Ø — R47 1Ø — D4 D672 — D5 D672 — D6 D672 — R48 22Ø — R49 47Ø 1/2W — C127 1ØØØPF — R5 1K — C124 6.8 µfd — D4-1 -12V (TO PIN 1 OF 1488) (TO PIN 2 OF UART) — Q2 6534D — R6 1K — D8 IN752A — D7 D672

+5V — C1-C95 .Ø1 µfd — C96-C1Ø1 6.8 µfd — GND

CLOCK GENERATION CHART

CLOCK ADDRESS DCBA	BAUD RATE	PERIOD (USEC)
ØØØØ	50	1250.00
ØØØ1	75	833.33
ØØ1Ø	110	568.18
ØØ11	134.5	464.68
Ø1ØØ	150	416.67
Ø1Ø1	300	208.33
Ø11Ø	600	104.17
Ø111	1200	52.08
1ØØØ	1800	34.72
1ØØ1	2000	31.25
1Ø1Ø	2400	26.04
1Ø11	3600	17.36
11ØØ	4800	13.02
11Ø1	7200	8.68
111Ø	9600	6.51
1111	38400	1.63

(CHART, REGULATORS)

REVISIONS			
	CHANGE NO.		REV.
DRN	M7833-MØØØ1		A
CHK			
ENG			
PROJ ENG			
PROD	R. HARRINGTON		

DRN R Raymond	1-13-76	FIRST USED ON DVII
CHK		TITLE ASYNCH MUX LINE CARD (D4-1)
ENG		
PROJ ENG		
PROD R. Wall		
NEXT HIGHER ASSY. D-UA-M7833-Ø-Ø		SIZE D CODE CS NUMBER M7833-Ø-1 REV. A
SCALE		
SHEET OF 1Ø		DIST.

MK

D3-7 INIT D1 L — EV2 — 7404 E7 — D4-2 RESET H — 7437 E40 — D4-2 RESET L

+3VB

7474 E35 — D4-2 MAINT Ø3 H / D4-2 MAINT Ø3 L
7474 E35 — D4-2 MAINT Ø2 H / D4-2 MAINT Ø2 L
7474 E34 — D4-2 MAINT Ø1 H / D4-2 MAINT Ø1 L
7474 E34 — D4-2 MAINT ØØ H / D4-2 MAINT ØØ L

7404 E47 — 7404 E47 — 7404 E47 — 7404 E47 — 7404 E47 — 7404 E47

7404 E47 — D4-2 BRG STROBE Ø3 H
7404 E47 — D4-2 BRG STROBE Ø2 H
7404 E58 — D4-2 BRG STROBE Ø1 H
7404 E58 — D4-2 BRG STROBE ØØ H
7404 E58 — D4-2 UART STROBE Ø3 H
7404 E58 — D4-2 UART STROBE Ø2 H
7404 E58 — D4-2 UART STROBE Ø1 H
7404 E58 — D4-2 UART STROBE ØØ H

74154 E52 — Ø15 Ø14 Ø13 Ø12 Ø11 Ø10 Ø9 Ø8 Ø7 Ø6 Ø5 Ø4 Ø3 Ø2 Ø1 ØØ — STB1 STBØ

D2-3 LCR 1Ø — DT2 — D3
D2-3 LCR Ø9 — AP2 — D2
D3-8 SRS Ø1 — BT2 — D1
D3-8 SRS ØØ — BM2 — DØ

+5V — R41 1ØK — C119 1ØØ PF

D2-3 CONTROL STROBE H — CS2
D3-8 SRS Ø3 L — BS2
D3-8 SRS Ø2 L — BR2
7400 E68
74123 E55 — 400NS

DJ2 — D4-2 CARD PARAMETER SELECT ØØ-Ø3 L

+3VA

D4-2 PEN L

D2-3 LCR 14 H — AL2 — 7404 E7 — 7437 E12 — D4-2 BUF LCR 14 H
D2-3 LCR 13 H — BA1 — 7404 E7 — 7437 E12 — D4-2 BUF LCR 13 H
D2-3 LCR 12 H — AM2 — 7404 E7 — 7437 E12 — D4-2 BUF LCR 12 H
D2-3 LCR 11 H — AN2 — 7404 E7 — 7437 E12 — D4-2 BUF LCR 11 H

74175 E24 — D4-2 BREAK Ø3 (Ø) H / D4-2 RCV ENBL Ø3 (1) H / D4-2 PEV Ø3 H / D4-2 HALF DUPLEX Ø3 H
74175 E13 — D4-2 BREAK Ø2 (Ø) H / D4-2 RCV ENBL Ø2 (1) H / D4-2 PEV Ø2 H / D4-2 HALF DUPLEX Ø2 H
74175 E8 — D4-2 BREAK Ø1 (Ø) H / D4-2 RCV ENBL Ø1 (1) H / D4-2 PEV Ø1 H / D4-2 HALF DUPLEX Ø1 H
74175 E14 — D4-2 BREAK ØØ (Ø) H / D4-2 RCV ENBL ØØ (1) H / D4-2 PEV ØØ H / D4-2 HALF DUPLEX ØØ H

(CARD SELECTION, REGISTERS, STROBES, INIT)

REVISIONS

CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (D4-2)	D	CS	M7833-Ø-1	A
SCALE —	SHEET 2 OF 1Ø		UNIT	

MK

D3-4 MASTER SCAN D H
D3-4 MASTER SCAN C H
DM2 D4-3 CARD FLAG SELECT ØØ-Ø3 L
D3-3 RESYNC PULSE L
D4-3 RESYNC PULSE Ø3 L
D4-3 RESYNC PULSE Ø2 L
D4-3 RESYNC PULSE Ø1 L
D4-3 RESYNC PULSE ØØ L
D3-4 TRANSMITTER STROBE H
D4-3 TRAN FLAG CLK Ø3 L
D4-3 TRAN FLAG CLK Ø2 L
D4-3 TRAN FLAG CLK Ø1 L
D4-3 TRAN FLAG CLK ØØ L
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
D4-6 RCV FLAG Ø3 H
D4-6 RCV FLAG Ø2 H
D4-6 RCV FLAG Ø1 H
D4-6 RCV FLAG ØØ H
D4-5 MATCH Ø3 (1) H
D4-5 MATCH Ø2 (1) H
D4-5 MATCH Ø1 (1) H
D4-5 MATCH ØØ (1) H
FM2 RECEIVER FLAG L
FE1 MATCH DETECT L
+5V
R8 10K
D1-5 RECEIVED DATA ENABLE H
FD1 D4-3 RDE ØØ-Ø3
+3VB
FK1 D4-3 DATA ENABLE ØØ-Ø3 H
D4-3 MATCH H
D4-2 RESET L
D4-3 CLR RCV FLAG Ø3 L
D4-3 CLR RCV FLAG Ø2 L
D4-3 CLR RCV FLAG Ø1 L
D4-3 CLR RCV FLAG ØØ L
D4-3 CLR MATCH Ø3 L
D4-3 CLR MATCH Ø2 L
D4-3 CLR MATCH Ø1 L
D4-3 CLR MATCH ØØ L
D3-4 MASTER SCAN Ø1 H
D3-4 MASTER SCAN ØØ H
D4-8 TRAN FLAG Ø3 H
D4-8 TRAN FLAG Ø2 H
D4-8 TRAN FLAG Ø1 H
D4-8 TRAN FLAG ØØ H
FL2 TRAN FLAG WAITING
D3-4 MASTER SCAN T/R
(SCAN SELECTION, FLAGS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (D4-3)	D	DCS	M7833-Ø-1	A
SCALE —	SHEET 3 OF 10	DIST.	MK	

M7833-Ø-1 A

R9 10K
R10 10K
C126 22PF
C123 22PF
7380 E93
7380 E93
Y1 2.457G MHZ
R11 1K
C200 22PF
7404 E80
W2 (W2 REMOVED FOR AUTOMATED MODULE TEST)
D4-2 RESET H
7493 E92
R3Ø
R2Ø
R1Ø
RØØ
CLR
CLKØ CLKBC
BN2
D4-4 SOURCE CLOCK B ØØ-Ø3 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
COM 5Ø16 E51
TD TC TB TA STT EXT2 EXT1 RD RC RB RA STR 4T 4R
D4-1 +12V
BJ1 D4-4 SOURCE CLOCK A ØØ-Ø3 L
5Ø.ØØ8 MHZ E27
+5V
W1 (W1 REMOVED FOR AUTOMATED MODULE TEST)
7437 E46
7437 E46
COM 5Ø16 E57
D4-1 +12V
+3VA
D4-2 BRG STROBE Ø3 H
D4-2 BRG STROBE Ø2 H
D4-2 BRG STROBE Ø1 H
D4-2 BRG STROBE ØØ H
D4-2 RESET L
7420 E39
7474 E45
7474 E45
7474 E55
7474 E55
D4-4 SPEED 17Ø3 H
D4-4 SPEED 17Ø2 H
D4-4 SPEED 17Ø1 H
D4-4 SPEED 17ØØ H
8Ø34 E56
8Ø93 E5Ø
CP2 D4-4 CLOCK Ø3 H
DØ2 D4-4 CLOCK Ø2 H
CE2 D4-4 CLOCK Ø1 H
DE2 D4-4 CLOCK ØØ H

REVISIONS
CHK | CHANGE NO | REV.

(CRYSTAL, CLOCK GENERATION)

TITLE ASYNCH MUX LINE CARD (04-4)
SCALE
SHEET 4 OF 10
SIZE D | CODE DCS | NUMBER M7833-Ø-1 | REV. A
DIST.
MK

D4-6 ENBL ERROR FLAGS L

D4-1Ø OR Ø3
D4-1Ø OR Ø2
D4-9 OR Ø1
D4-9 OR ØØ
D4-1Ø PE Ø3
D4-1Ø PE Ø2
D4-9 PE Ø1
D4-9 PE ØØ

D4-1Ø FE Ø3
D4-1Ø FE Ø2
D4-9 FE Ø1
D4-9 FE ØØ

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-3 BUF MSCAN ØØ L
D4-3 BUF MSCAN Ø1 L
D4-3 CARD FLAG SELECT ØØ-Ø3 L
D4-6 RCV FILE LOAD L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE ADDRS ØØ L
D4-3 DATA ENABLE ØØ-Ø3 H

MASTER OR L
MASTER PE L
RECV DATA Ø7 L
RECV DATA Ø6 L
RECV DATA Ø5 L
RECV DATA Ø4 L
RECV DATA Ø3 L
RECV DATA Ø2 L
RECV DATA Ø1 L
RECV DATA ØØ L

D4-2 RCV ENBL Ø3 (1) H
D4-3 CLR MATCH Ø3 L
D4-3 RESYNC PULSE Ø3 L
D4-5 MATCH Ø3 (1) H
D4-5 ACTIVE Ø3 H
D4-5 ACTIVE Ø3 L

D4-2 RCV ENBL Ø2 (1) H
D4-3 CLR MATCH Ø2 L
D4-3 RESYNC PULSE Ø2 L
D4-5 MATCH Ø2 (1) H
D4-5 ACTIVE Ø2 H
D4-5 ACTIVE Ø2 L

D4-2 RCV ENBL Ø1 (1) H
D4-3 CLR MATCH Ø1 L
D4-3 RESYNC PULSE Ø1 L
D4-5 MATCH Ø1 (1) H
D4-5 ACTIVE Ø1 H
D4-5 ACTIVE Ø1 L

D4-2 RCV ENBL ØØ (1) H
D4-3 CLR MATCH ØØ L
D4-3 RESYNC PULSE ØØ L
D4-5 MATCH ØØ (1) H
D4-5 ACTIVE ØØ H
D4-5 ACTIVE ØØ L

(RCV FILE... DATA, MATCH LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (D4-5)	D	DCS	M7833-Ø-1	A
SCALE —	SHEET 5 OF 1Ø	DIST.	MK	

D4-6 RDE Ø3 L
D4-6 RDE Ø2 L
D4-6 RDE Ø1 L
D4-6 RDE ØØ L
D4-6 RESET DA Ø3 L
D4-6 RESET DA Ø2 L
D4-6 RESET DA Ø1 L
D4-6 RESET DA ØØ L

D4-3 CLR RCV FLAG Ø3 L
D4-5 ACTIVE Ø3 H
D4-3 CLR RCV FLAG Ø2 L
D4-5 ACTIVE Ø2 H
D4-3 CLR RCV FLAG Ø1 L
D4-5 ACTIVE Ø1 H
D4-3 CLR RCV FLAG ØØ L
D4-5 ACTIVE ØØ H

D4-1Ø DA Ø3 L
D4-6 RCV FLAG Ø3 H
D4-1Ø DA Ø2 L
D4-6 RCV FLAG Ø2 H
D4-9 DA Ø1 L
D4-6 RCV FLAG Ø1 H
D4-9 DA ØØ L
D4-6 RCV FLAG ØØ H

DV11 BUSY Ø3
DV11 BUSY Ø2
DV11 BUSY Ø1
DV11 BUSY ØØ
ASYN H

D4-6 ENBL ERROR FLAGS L
D4-6 RCV FILE ADDRS ØØ L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RECEIVER SAMPLE CLOCK H
D4-6 RCV FILE LOAD L
D4-2 RESET L

RDE
RDE DLY
LOAD FILE
WAIT DLY
SAMPLE CLK
SAMPLE DELAY
RESET DA

(RECEIVER FLAG SERVICE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ASYNCH MUX LINE CARD (D4-6)			
SIZE	CODE	NUMBER	REV.	
D	CS	M7833-Ø-1	A	
SCALE	SHEET 6 OF 1Ø	DIST.		

MK

D4-10 SERIAL OUT Ø3 H — AH2 — 74Ø8 E9 pin 3
D4-2 BREAK Ø3 (Ø) H — 74Ø8 E9 pin 2
74Ø8 E9 pin 3 → 1488 E11 pin 2 → 1488 E11 pin 3 → J1 EE
EIA XMIT DATA Ø3 ← J1 EE
EIA RCV DATA Ø3 → J1 KK → 1489 E5 pin 1 → 1489 E5 pin 3
C1Ø6 47ØPF
D4-2 MAINT Ø3 H → 8Ø94 E17 pin 2 → 8Ø94 E17 pin 3
8Ø94 E17 pin 1 → 8Ø93 E18 pin 1
1489 E5 pin 3 → 7432 E3 pin 1 → 7432 E3 pin 3 → 8Ø93 E18 pin 2 → 8Ø93 E18 pin 3
D4-5 ACTIVE Ø3 L → 7432 E22 pin 2 → 7432 E22 pin 3 BK1 → D4-7 SERIAL IN Ø3 H
D4-2 HALF DUPLEX Ø3 H — 74Ø8 E19 pin 1
D4-1Ø EOC Ø3 L — (EF2) — 74Ø8 E19 pin 2 → 74Ø8 E19 pin 3 → 7432 E3 pin 2

D4-10 SERIAL OUT Ø2 H — AT2 — 74Ø8 E9 pin 4
D4-2 BREAK Ø2 (Ø) H — 74Ø8 E9 pin 5
74Ø8 E9 pin 6 → 1488 E11 pin 5 → 1488 E11 pin 6 → J1 CC
EIA XMIT DATA Ø2 ← J1 CC
EIA RCV DATA Ø2 → J1 HH → 1489 E5 pin 4 → 1489 E5 pin 6
C1Ø5 47ØPF
D4-2 MAINT Ø2 H → 8Ø94 E17 pin 5 → 8Ø94 E17 pin 6
8Ø94 E17 pin 4 → 8Ø93 E18 pin 4
1489 E5 pin 6 → 7432 E3 pin 4 → 7432 E3 pin 6 → 8Ø93 E18 pin 5 → 8Ø93 E18 pin 6
D4-5 ACTIVE Ø2 L → 7432 E22 pin 5 → 7432 E22 pin 6 BK2 → D4-7 SERIAL IN Ø2 H
D4-2 HALF DUPLEX Ø2 H — 74Ø8 E19 pin 4
D4-1Ø EOC Ø2 L — (EK2) — 74Ø8 E19 pin 5 → 74Ø8 E19 pin 6 → 7432 E3 pin 5

D4-9 SERIAL OUT Ø1 H — AB1 — 74Ø8 E9 pin 9
D4-2 BREAK Ø1 (Ø) H — 74Ø8 E9 pin 1Ø
74Ø8 E9 pin 8 → 1488 E11 pin 9 → 1488 E11 pin 8 → J1 T
EIA XMIT DATA Ø1 ← J1 T
EIA RCV DATA Ø1 → J1 N → 1489 E5 pin 1Ø → 1489 E5 pin 8
C128 47ØPF
D4-2 MAINT Ø1 H → 8Ø94 E17 pin 9 → 8Ø94 E17 pin 8
8Ø94 E17 pin 1Ø → 8Ø93 E18 pin 1Ø
1489 E5 pin 8 → 7432 E3 pin 9 → 7432 E3 pin 8 → 8Ø93 E18 pin 9 → 8Ø93 E18 pin 8
D4-5 ACTIVE Ø1 L → 7432 E22 pin 1Ø → 7432 E22 pin 8 BD1 → D4-7 SERIAL IN Ø1 H
D4-2 HALF DUPLEX Ø1 H — 74Ø8 E19 pin 9
D4-9 EOC Ø1 L — (ER2) 1Ø — 74Ø8 E19 pin 1Ø → 74Ø8 E19 pin 8 → 7432 E3 pin 1Ø

D4-9 SERIAL OUT ØØ H — AJ2 — 74Ø8 E9 pin 12
D4-2 BREAK ØØ (Ø) H — 74Ø8 E9 pin 13
74Ø8 E9 pin 11 → 1488 E11 pin 12 → 1488 E11 pin 11 → J1 R
EIA XMIT DATA ØØ ← J1 R
EIA RCV DATA ØØ → J1 L → 1489 E5 pin 13 → 1489 E5 pin 11
C129 47Ø PF
D4-2 MAINT ØØ H → 8Ø94 E17 pin 12 → 8Ø94 E17 pin 11
8Ø94 E17 pin 13 → 8Ø93 E18 pin 13
1489 E5 pin 11 → 7432 E3 pin 12 → 7432 E3 pin 11 → 8Ø93 E18 pin 12 → 8Ø93 E18 pin 11
D4-5 ACTIVE ØØ L → 7432 E22 pin 13 → 7432 E22 pin 11 BF2 → D4-7 SERIAL IN ØØ H
D4-2 HALF DUPLEX ØØ H — 74Ø8 E19 pin 12
D4-9 EOC ØØ L — (FJ2) 13 — 74Ø8 E19 pin 13 → 74Ø8 E19 pin 11 → 7432 E3 pin 13

(EIA IN & OUT, HALF DUPLEX, BREAK, MAINT LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (D4-7)	D	CS	M7833-Ø-1	A
SCALE —	SHEET 7 OF 1Ø	DIST.		

NOTES:

. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FEATURE AT 9600 BAUD OR LESS.

DATA SET BUSY Ø3 — J1 F — 1489 E6 — C118 47ØPF — D4-4 SPEED 17Ø3 H — * W6 — R38 1K +5V — T4H11 E33 — D4-2 MAINT Ø3 L — 8815 E65 — D4-1Ø EOC Ø3 L (EF2) — D4-1Ø TBMT Ø3 L

DATA SET BUSY Ø2 — J1 D — 1489 E6 — C109 47ØPF — D4-4 SPEED 17Ø2 H — * W5 — R37 1K +5V — T4H11 E33 — D4-2 MAINT Ø2 L — 8815 E65 — D4-1Ø EOC Ø2 L (EK2) — D4-1Ø TBMT Ø2 L

DATA SET BUSY Ø1 — J1 B — 1489 E6 — C112 47ØPF — D4-4 SPEED 17Ø1 H — * W4 — R36 1K +5V — T4H11 E33 — D4-2 MAINT Ø1 L — 8815 E79 — D4-9 EOC Ø1 L (ER2) — D4-9 TBMT Ø1 L

DATA SET BUSY ØØ — J1 9 — 1489 E6 — C110 47ØPF — D4-4 SPEED 17ØØ H — * W3 — R35 1K +5V — T4H11 E69 — D4-2 MAINT ØØ L — 8815 E79 — D4-9 EOC ØØ L (FJ2) — D4-9 TBMT ØØ L

D4-2 RESET L — T4ØØ E42 — +5V — R39 39Ø — 5ØNS DL2 — R4Ø 47Ø — C121 27PF — RT 1ØK — T4123 EG3 — 175 NS — +3VB

T9175 E88 — D5 R3(1) — D2 R2(1) R2(Ø) — D1 R1(1) R1(Ø) — DØ RØ(1) RØ(Ø) — CLR CLK

3318 E87 — A0 A1 A2 — E0 G9 — E1 — +3VA

+5V — R42 1ØK — C120 56PF — T4123 E7Ø — 25Ø NS — +3VA

ST88 ST8A — DB DA — SØ S1 — 74155 E89 — ØB0 ØB1 ØB2 ØB3 — ØA0 ØA1 ØA2 ØA3

+5V — R43 1ØK — C122 15PF — T4123 E7Ø — 125 NS

D4-2 RESET L — D4-8 THRL Ø3 L — D4-3 TRAN FLAG CLK Ø3 L — T4ØØ E85 — T7474 ET4 — +3VA — D4-8 TRAN FLAG Ø3 H

D4-8 THRL Ø2 L — D4-3 TRAN FLAG CLK Ø2 L — T4ØØ E85 — T7474 ET4 — +3VA — D4-8 TRAN FLAG Ø2 H

D4-8 THRL Ø1 L — D4-3 TRAN FLAG CLK Ø1 L — T4ØØ E85 — T7474 E84 — +3VA — D4-8 TRAN FLAG Ø1 H

D4-8 THRL ØØ L — D4-3 TRAN FLAG CLK ØØ L — T4ØØ E85 — T7474 E84 — +3VA — D4-8 TRAN FLAG ØØ H

D3-4 TRAN DATA Ø7 H — EP1 — D4-8 DB5
D3-4 TRAN DATA Ø6 H — EM2 — D4-8 DB7
D3-4 TRAN DATA Ø5 H — FR2 — D4-8 DB6
D3-4 TRAN DATA Ø4 H — FV2 — D4-8 DB5

D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L

T74175 E88 — RD RA1 RAØ — D3 D2 D1 DØ — R3(1) R2(1) R2(Ø) R1(1) RØ(1) RØ(Ø) — WR WA1 WAØ

D3-4 TRAN DATA Ø3 H — FS2 — D4-8 DB4
D3-4 TRAN DATA Ø2 H — FV1 — D4-8 DB3
D3-4 TRAN DATA Ø1 H — FT2 — D4-8 DB2
D3-4 TRAN DATA ØØ H — FU2 — D4-8 DB1

(TRANSMIT FLAG SERVICING)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ASYNCH MUX LINE CARD (Ø4-8)	SIZE	CODE	NUMBER / REV.
SCALE	SHEET 8 OF 1Ø	D	DCS	M7833-Ø-1 / A
		DIST.		

MK

M7833-Ø-1 REV. A

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-7 SERIAL IN ØØ H BF2 20 SERIAL IN
D4-6 RESET DA ØØ L 18 CLR R DONE
D4-6 RDE ØØ L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK ØØ H (DE2) 4Ø X CLK
UART ØØ ETG
D4-8 THRL ØØ L 23 LD XD
33 XD7
32 XD6
31 XD5
3Ø XD4
29 XD3
28 XD2
27 XD1
26 XDØ
CLR NB1 NB2 2SB NP EP LDC
21 38 37 36 35 32 34

R DONE 19
OR ERR 15 D4-9 OR ØØ
FR ERR 14 D4-9 FE ØØ
P ERR 13 D4-9 PE ØØ
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 AJ2 D4-9 SERIAL OUT ØØ H
XRDY 22 11 T4Ø4 E73 1Ø D4-9 TBMT ØØ L
EOC 24
9 T4Ø4 E8Ø 8 FJ2 D4-9 EOC ØØ L
1 T4Ø4 E8Ø 2 D4-9 DA ØØ L

D4-7 SERIAL IN Ø1 H (BD1) 2Ø SERIAL IN
D4-6 RESET DA Ø1 L 18 CLR R DONE
D4-6 RDE Ø1 L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø1 H (CE2) 4Ø X CLK
UART Ø1 EB1
D4-8 THRL Ø1 L 23 LD XD
33 XD7
32 XD6
31 XD5
3Ø XD4
29 XD3
28 XD2
27 XD1
26 XDØ
CLR NB1 NB2 2SB NP EP LDC
21 38 37 36 35 39 34

R DONE 17
OR ERR 15 D4-9 OR Ø1
FR ERR 14 D4-9 FE Ø1
P ERR 13 D4-9 PE Ø1
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 AB1 D4-9 SERIAL OUT Ø1 H
XRDY 22 11 T4Ø4 E8Ø Ø D4-9 TBMT Ø1 L
EOC 24
13 T4Ø4 E8Ø :2 ER2 D4-9 EOC Ø1 L
3 T4Ø4 E8Ø 4 D4-9 DA Ø1 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV ØØ H
D4-2 UART STROBE ØØ H
D4-2 PEV Ø1 H
D4-2 UART STROBE Ø1 H

(UARTS ØØ & Ø1)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (D4-9)	D	CS	M7833-Ø-1	A
SCALE — SHEET 9 OF 1Ø	DIST.			

MK

M7833-Ø-1

D4-9 RDB
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-7 SERIAL IN Ø2 H (BK2) 20
D4-6 RESET DA Ø2 L 18
D4-6 RDE Ø2 L 4
STB STATUS 16
R CLK 17
D4-4 CLOCK Ø2 H (DS2) 40
X CLK
D4-8 THRL Ø2 L 23
LD XD 33
XD7 32
XD6 31
XD5 30
XD4 29
XD3 28
XD2 27
XD1 26
XDØ
CLR NBI NB2 2SB NP EP LDC 21 38 37 36 35 39 34

UART Ø2
E67

SERIAL IN
CLR R DONE
STB RD
STB STATUS
R CLK
X CLK
LD XD
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XDØ
CLR NBI NB2 2SB NP EP LDC

R DONE 19
OR ERR 15 — D4-1Ø OR Ø2
FR ERR 14 — D4-1Ø FE Ø2
P ERR 13 — D4-1Ø PE Ø2
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12
SERIAL OUT 25 — AT2 — D4-1Ø SERIAL OUT Ø2 H
XRDY 22 — 5 — 74Ø4 E66 — 6 — D4-1Ø TBMT Ø2 L
EOC 24 — 9 — 74Ø4 E66 — 8 EK2 — D4-1Ø EOC Ø2 L

1 — 74Ø4 E66 — 2 — D4-1Ø DA Ø2 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV Ø2 H
D4-2 UART STROBE Ø2 H
D4-2 PEV Ø3 H
D4-2 UART STROBE Ø3 H

D4-7 SERIAL IN Ø3 H (BK1) 20
D4-6 RESET DA Ø3 L 18
D4-6 RDE Ø3 L 4
STB STATUS 16
R CLK 17
D4-4 CLOCK Ø3 H (CP2) 40
X CLK
D4-8 THRL Ø3 L 23
LD XD 33
XD7 32
XD6 31
XD5 30
XD4 29
XD3 28
XD2 27
XD1 26
XDØ
CLR NBI NB2 2SB NP EP LDC 21 38 37 36 35 39 34

UART Ø3
E62

SERIAL IN
CLR R DONE
STB RD
STB STATUS
R CLK
X CLK
LD XD
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XDØ
CLR NBI NB2 2SB NP EP LDC

R DONE 19
OR ERR 15 — D4-1Ø OR Ø3
FR ERR 14 — D4-1Ø FE Ø3
P ERR 13 — D4-1Ø PE Ø3
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12
SERIAL OUT 25 — AH2 — D4-1Ø SERIAL OUT Ø3 H
XRDY 22 — 11 — 74Ø4 E66 — 10 — D4-1Ø TBMT Ø3 L
EOC 24 — 13 — 74Ø4 E66 — 12 EF2 — D4-1Ø EOC Ø3 L

3 — 74Ø4 E66 — 4 — D4-1Ø DA Ø3 L

(UARTS Ø2 & Ø3)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD (D4-1Ø)	D	CS	M7833-Ø-1	A
SCALE — SHEET 1Ø OF 1Ø	CHST.			

MK

DCS M7833-Ø-1 REV A

BERG CONNECTOR

J1

- A — DATA SET BUSY ØØ
- B — DATA SET BUSY Ø1
- C — DATA SET BUSY Ø2
- D — ASYN H
- E — DATA SET BUSY Ø3
- F — EIA RCV DATA ØØ
- H — EIA RCV DATA Ø1
- J — EIA XMIT DATA ØØ
- K — EIA XMIT DATA Ø1
- L — DVII BUSY ØØ
- M — DVII BUSY Ø1
- N — DVII BUSY Ø2
- P — DVII BUSY Ø3
- R — EIA XMIT DATA Ø2
- S — EIA XMIT DATA Ø3
- T — EIA RCV DATA Ø2
- U — EIA RCV DATA Ø3
- V, W, X, Y, Z, AA, BB, CC, DD, EE, FF, HH, JJ, KK, LL, MM, NN, PP, RR, SS, TT, UU, VV

+5V — R1 330 — +3VA; C125 .Ø1 µfd; R3 750

+5V — R2 330 — +3VB; C111 .Ø1 µfd; R4 750

+15V — CU1 — R50 39 1/2W — D4-12V (TO PIN 9 OF 5Ø1Ø) (TO PIN 14 OF 1488); D1 IN759A; C116 .Ø1 µfd; C1Ø8 .Ø1 µfd

-15V FB2 — Q1 2N2584 — R44 1Ø; R45 1Ø; R46 1Ø; R47 1Ø; D4 D672; D5 D672; D6 D672; R48 27Ø; R49 47Ø 1/2W; C127 1ØØØPF; Q2 65340; D8 IN752A; D7 D672; R5 1K; R6 1K; C124 6.8 µfd; D4-1 -12V (TO PIN 1 OF 1488) (TO PIN 2 OF UART)

+5V — C1-C95 .Ø1 µfd; C96-C101 6.8 µfd — GND

CLOCK GENERATION CHART

CLOCK ADDRESS DCBA	BAUD RATE	PERIOD (USEC)
ØØØØ	50	1250.00
ØØØ1	75	833.33
ØØ1Ø	110	568.18
ØØ11	134.5	464.68
Ø1ØØ	150	416.67
Ø1Ø1	300	208.33
Ø11Ø	600	104.17
Ø111	1200	52.08
1ØØØ	1800	34.72
1ØØ1	2000	31.25
1Ø1Ø	2400	26.04
1Ø11	3600	17.36
11ØØ	4800	13.02
1101	7200	8.68
111Ø	9600	6.51
1111	38400	1.63

(CHART, REGULATORS)

DRN		1-13-76
CHK		4-15-76
ENG		4-15-76
PROJ. ENG.		4-15-76
PROD. E		4-15-76
NEXT HIGHER ASSY.		
B-DD-DVII-Ø		
SCALE		
SHEET	OF 1Ø	

FIRST USED ON: DVII

TITLE: ASYNCH MUX LINE CARD, LINES ØØ-Ø3 (D4-1)

SIZE D | CODE BS | NUMBER DVII-Ø-15 | REV. *

DIST.

REVISIONS		
ZONE	CHANGE NO.	REV.

D3-7 INIT D1 L
EV2
7404 E7
D4-2 RESET H
7437 E40
D4-2 RESET L
+3VB
7474 E35
D4-2 MAINT Ø3 H
D4-2 MAINT Ø3 L
7474 E35
D4-2 MAINT Ø2 H
D4-2 MAINT Ø2 L
7474 E34
D4-2 MAINT Ø1 H
D4-2 MAINT Ø1 L
7474 E34
D4-2 MAINT ØØ H
D4-2 MAINT ØØ L
7404 E47
7404 E47
7404 E47
7404 E47
7404 E47
D4-2 BRG STROBE Ø3 H
7404 E47
D4-2 BRG STROBE Ø2 H
7404 E58
D4-2 BRG STROBE Ø1 H
7404 E58
D4-2 BRG STROBE ØØ H
7404 E58
D4-2 UART STROBE Ø3 H
7404 E58
D4-2 UART STROBE Ø2 H
7404 E58
D4-2 UART STROBE Ø1 H
7404 E58
D4-2 UART STROBE ØØ H
7404 E53
7404 E53
7404 E53
7404 E53
74154 E52
Ø15
Ø14
Ø13
Ø12
Ø11
Ø10
Ø9
Ø8
Ø7
Ø6
Ø5
Ø4
Ø3
Ø2
Ø1
Ø0
D2-3 LCR 1Ø
DT2
D3
D2-3 LCR Ø9
AP2
D2
D3-8 SRS Ø1
BT2
D1
D3-8 SRS ØØ
BM2
DØ
STB1
STBØ
+5V
R41 1Ø k
C119 1ØØ PF
D2-3 CONTROL STROBE H
CS2
D3-8 SRS Ø3 L
BS2
D3-8 SRS Ø2 L
BR2
7400 E68
74123 E53
+3VA
DJ2
D4-2 CARD PARAMETER SELECT ØØ-Ø3 L
D2-3 LCR 14 H
AL2
7404 E7
D4-2 PEN L
7437 E12
D4-2 BUF LCR 14 H
D2-3 LCR 13 H
BA1
7404 E7
7437 E12
D4-2 BUF LCR 13 H
D2-3 LCR 12 H
AM2
7404 E7
7437 E12
D4-2 BUF LCR 12 H
D2-3 LCR 11 H
AN2
7404 E7
7437 E12
D4-2 BUF LCR-11 H
74175 E24
D3 R3(1) R3(Ø)
D4-2 BREAK Ø3 (Ø H
D2 R2(1) R2(Ø)
D4-2 RCV ENBL Ø3 (1 H
D1 R1(1) R1(Ø)
D4-2 PEV Ø3 H
DØ RØ(1) RØ(Ø)
D4-2 HALF DUPLEX Ø3 H
CLR CLK
74175 E13
D4-2 BREAK Ø2 (Ø H
D4-2 RCV ENBL Ø2 (1 H
D4-2 PEV Ø2 H
D4-2 HALF DUPLEX Ø2 H
74175 E8
D4-2 BREAK Ø1 (Ø H
D4-2 RCV ENBL Ø1 (1 H
D4-2 PEV Ø1 H
D4-2 HALF DUPLEX Ø1 H
74175 E14
D4-2 BREAK ØØ (Ø H
D4-2 RCV ENBL ØØ (1 H
D4-2 PEV ØØ H
D4-2 HALF DUPLEX ØØ H

(CARD SELECTION, REGISTERS, STROBES, INIT)

REVISIONS
CHR | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINES ØØ-03 (04-2)
SIZE D CODE BS NUMBER DVII-Ø-15 REV. *
SCALE — SHEET 2 OF 1Ø DIST.

D3-4 MASTER SCAN D H
D3-4 MASTER SCAN C H
EU2
EN2
T400 E68
DM2
D4-3 CARD FLAG SELECT Ø0-Ø3 L
T404 E73
D3-5 RESYNC PULSE L
DF2
D3-4 TRANSMITTER STROBE H
EH2
T400 E48
T404 E53
D4-3 TRAN FILE LOAD L
74155 E60
STØB STØA
DB
DA
SI
SØ
ØBØ D4-3 RESYNC PULSE Ø3 L
ØB1 D4-3 RESYNC PULSE Ø2 L
ØB2 D4-3 RESYNC PULSE Ø1 L
ØB3 D4-3 RESYNC PULSE Ø0 L
ØAØ D4-3 TRAN FLAG CLK Ø3 L
ØA1 D4-3 TRAN FLAG CLK Ø2 L
ØA2 D4-3 TRAN FLAG CLK Ø1 L
ØA3 D4-3 TRAN FLAG CLK Ø0 L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN Ø0 L
D4-6 RCV FLAG Ø3 H
D4-6 RCV FLAG Ø2 H
D4-6 RCV FLAG Ø1 H
D4-6 RCV FLAG Ø0 H
D4-5 MATCH Ø3 (1) H
D4-5 MATCH Ø2 (1) H
D4-5 MATCH Ø1 (1) H
D4-5 MATCH Ø0 (1) H
74153 E37
STØØ STØ1
AI BI CI DI
AØ BØ CØ DØ
SI SØ
1Ø 11 12 13 6 5 4 3
9 7
T432 E72
8881 E82
FM2 RECEIVER FLAG L
FE1 MATCH DETECT L
+5V
R8 10K
D4-5 RECEIVED DATA ENABLE H
CN2
T400 E68
74123 E63
FU1
D4-3 RDE Ø0-Ø3
+3V8
FK1
D4-3 DATA ENABLE Ø0-Ø3 H
74LS74 E36
D4-3 MATCH H
D4-2 RESET L
T437 E90
74155 E31
STØ6 STØA
ØBØ D4-3 CLR RCV FLAG Ø3 L
ØB1 D4-3 CLR RCV FLAG Ø2 L
ØB2 D4-3 CLR RCV FLAG Ø1 L
ØB3 D4-3 CLR RCV FLAG Ø0 L
ØAØ D4-3 CLR MATCH Ø3 L
ØA1 D4-3 CLR MATCH Ø2 L
ØA2 D4-3 CLR MATCH Ø1 L
ØA3 D4-3 CLR MATCH Ø0 L
D3-4 MASTER SCAN Ø1 H
EM1
T404 E73
D3-4 MASTER SCAN Ø0 H
EN1
T404 E73
74153 E83
STØ1 STØØ
D4-8 TRAN FLAG Ø3 H
D4-8 TRAN FLAG Ø2 H
D4-8 TRAN FLAG Ø1 H
D4-8 TRAN FLAG Ø0 H
8881 E82
FL2 TRAN FLAG WAITING L
D3-4 MASTER SCAN T/R
CR2
T404 E73

(SCAN SELECTION, FLAGS)

REVISIONS		
CHR	CHANGE NO	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø0-Ø3 (D4-3)	D	85	DVII-Ø-15	*
SCALE	SHEET 3 OF 10	DIST.		

D 85 DVII-Ø-15

R9 10K
R10 10K
C126 22PF
C123 22PF
7380 E93
7380 E93
Y1 2.4576 MHZ
C200 22PF
R11 1K
7404 E80
W2 (W2 REMOVED FOR AUTOMATED MODULE TEST)
7493 E92
D4-2 RESET H
R3(1) R2(1) R1(1) R0(1) CLK0 CLKBC CLR
BN2
D4-4 SOURCE CLOCK B Ø0-Ø3 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
TD TC TB TA STT EXT2 EXT1 RD RC RB RA STR
COM 5Ø16 E51
ST SR
D4-1 +12V
5Ø86 E27
MHZ
+5V
W1 (W1 REMOVED FOR AUTOMATED MODULE TEST)
BJ1 D4-4 SOURCE CLOCK A Ø0-Ø3 L
7437 E46
7437 E46
COM 5Ø16 E57
7420 E37
D4-2 BRG STROBE Ø3 H
D4-2 BRG STROBE Ø2 H
D4-2 BRG STROBE Ø1 H
D4-2 BRG STROBE Ø0 H
D4-2 RESET L
+3VA
D 7474 E45
D 7474 E55
D4-4 SPEED 17Ø3 H
D4-4 SPEED 17Ø2 H
D4-4 SPEED 17Ø1 H
D4-4 SPEED 17Ø0 H
8094 E56
8093 E50
CP2 D4-4 CLOCK Ø3 H
DS2 D4-4 CLOCK Ø2 H
CE2 D4-4 CLOCK Ø1 H
DE2 D4-4 CLOCK Ø0 H

(CRYSTAL CLOCK GENERATION)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø0-Ø3 (D4-4)	D	BS	DVII-Ø-15	*
SCALE	SHEET 4 OF 10		DIST.	

D4-6 ENBL ERROR FLAGS L

D4-1Ø OR Ø3
D4-1Ø OR Ø2
D4-9 OR Ø1
D4-9 OR ØØ

D4-1Ø PE Ø3
D4-1Ø PE Ø2
D4-9 PE Ø1
D4-9 PE ØØ

D4-1Ø FE Ø3
D4-1Ø FE Ø2
D4-9 FE Ø1
D4-9 FE ØØ

74153 E71 — 74153 E75 — T04 E53 — H11 E69 — H11 E69

S Ø | F
L | A
H | B

74157 E64

+3VB

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5

D4-3 BUF MSCAN ØØ L
D4-3 BUF MSCAN Ø1 L
D4-3 CARD FLAG SELECT ØØ-Ø3 L

D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-6 RCV FILE LOAD L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE ADDRS ØØ L
D4-3 DATA ENABLE ØØ-Ø3 H

74170 E54 — 74170 E35 — 74170 E59

8881 E86 — FL1 — MASTER OR L
8881 E86 — FM1 — MASTER PE L
8881 E86 — 1Ø FH1 — RECV DATA Ø7 L
8881 E86 — 13 FJ1 — RECV DATA Ø6 L
8881 E9Ø — FR1 — RECV DATA Ø5 L
8881 E9Ø — FS1 — RECV DATA Ø4 L
8881 E9Ø — 1Ø FN1 — RECV DATA Ø3 L
8881 E9Ø — 13 FP1 — RECV DATA Ø2 L
8881 E91 — FN2 — RECV DATA Ø1 L
8881 E91 — FP2 — RECV DATA ØØ L

R12 R13 R14 R15 R16 R17 R18 R19 R2Ø R21 — 1K — +5V

R22 — 1ØK — +5V — C1Ø2 27 PF
D4-2 RCV ENBL Ø3 (1) H
74123 E2 — 74174 E23 — 74174 E27
D4-5 MATCH Ø3 (1) H
D4-5 ACTIVE Ø3 H
D4-5 ACTIVE Ø3 L
D4-3 CLR MATCH Ø3 L
7408 E3Ø
D4-3 RESYNC PULSE Ø3 L
D4-2 RCV ENBL Ø3 (1) H

R23 — 1ØK — +5V — C1Ø3 27PF
D4-2 RCV ENBL Ø2 (1) H
74123 E2 — 74174 E23 — 74174 E27
D4-5 MATCH Ø2 (1) H
D4-5 ACTIVE Ø2 H
D4-5 ACTIVE Ø2 L
D4-3 CLR MATCH Ø2 L
7408 E3Ø
D4-3 RESYNC PULSE Ø2 L
D4-2 RCV ENBL Ø2 (1) H

R24 — 1ØK — +5V — C1Ø4 27 PF
D4-2 RCV ENBL Ø1 (1) H
74123 E1Ø — 74174 E25 — 74174 E27
D4-5 MATCH Ø1 (1) H
D4-5 ACTIVE Ø1 H
D4-5 ACTIVE Ø1 L
D4-3 CLR MATCH Ø1 L
7408 E2Ø
D4-3 RESYNC PULSE Ø1 L
D4-2 RCV ENBL Ø1 (1) H

R25 — 1ØK — +5V — C1Ø7 27 PF
D4-2 RCV ENBL ØØ (1) H
74123 E1Ø — 74174 E15 — 74174 E27
D4-5 MATCH ØØ (1) H
D4-5 ACTIVE ØØ H
D4-5 ACTIVE ØØ L
D4-3 CLR MATCH ØØ L
7408 E2Ø
D4-3 RESYNC PULSE ØØ L
D4-2 RCV ENBL ØØ (1) H

(RCV FILES, RCV DATA, MATCH LOGIC)

REVISIONS | CHR | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINES ØØ-Ø3 (D4-5)
SIZE D | CODE 8S | NUMBER DV11-Ø-15 | REV. *
SCALE — | SHEET 5 OF 1Ø | DIST.

+5VA
+3VA
+3VB
+5V

D4-6 RDE Ø3 L
D4-6 RDE Ø2 L
D4-6 RDE Ø1 L
D4-6 RDE ØØ L

D4-6 RESET DA Ø3 L
D4-6 RESET DA Ø2 L
D4-6 RESET DA Ø1 L
D4-6 RESET DA ØØ L

D4-3 CLR RCV FLAG Ø3 L
D4-5 ACTIVE Ø3 H
D4-3 CLR RCV FLAG Ø2 L
D4-5 ACTIVE Ø2 H
D4-3 CLR RCV FLAG Ø1 L
D4-5 ACTIVE Ø1 H
D4-3 CLR RCV FLAG ØØ L
D4-5 ACTIVE ØØ H

D4-Ø DA Ø3 L
D4-6 RCV FLAG Ø3 H
D4-Ø DA Ø2 L
D4-6 RCV FLAG Ø2 H
D4-9 DA Ø1 L
D4-6 RCV FLAG Ø1 H
D4-9 DA ØØ L
D4-6 RCV FLAG ØØ H

DVII BUSY Ø3
DVII BUSY Ø2
DVII BUSY Ø1
DVII BUSY ØØ
ASYN H

D4-6 ENBL ERROR FLAGS L
D4-6 RCV FILE ADDRS ØØ L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE LOAD L
D4-6 RECEIVER SAMPLE CLOCK H
D4-2 RESET L

RDE
RDE DLY
LOAD FILE
WAIT DLY
RESET DA
SAMPLE CLK
SAMPLE DELAY

R23 10K
R26 330
R27 470
R28 10K
R29 10K
R30 10K
R31 1K
R32 10K
R33 10K
R34 10K
C113 150 PF
C114 100PF
C115 15PF
C117 180PF

(RECEIVER FLAG SERVICE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ASYNCH MUX LINE CARD LINES CC-Ø3(04-6)
SIZE D | CODE BS | NUMBER DV11-Ø-15 | REV. *
SCALE | SHEET 6 OF 10

D4-10 SERIAL OUT Ø3 H — AH2 1 — T4Ø8 E9 3
D4-2 BREAK Ø3 (Ø) H — 2
2 — 1488 E11 3 — J1 EE — EIA XMIT DATA Ø3
EIA RCV DATA Ø3 — J1 KK — 1 — 1489 E5 3
C1Ø6 47ØPF — 2
D4-2 MAINT Ø3 H — 2 — 8094 E17 3 — 1
D4-2 HALF DUPLEX Ø3 H — 1 — T4Ø8 E19 3
D4-1Ø EOC Ø3 L — (EF2) 2
1 — 7432 E3 3 — 2 — 8093 E18 3 — 1
D4-5 ACTIVE Ø3 L — 1 — 7432 E22 3 — BK1 — D4-7 SERIAL IN Ø3 H

D4-10 SERIAL OUT Ø2 H — AT2 4 — T4Ø8 E9 6
D4-2 BREAK Ø2 (Ø) H — 5
4 — 1488 E11 6 — J1 CC — EIA XMIT DATA Ø2
EIA RCV DATA Ø2 — J1 HH — 4 — 1489 E5 6
C1Ø5 47ØPF — 5
D4-2 MAINT Ø2 H — 5 — 8094 E17 6 — 4
D4-2 HALF DUPLEX Ø2 H — 4 — T4Ø8 E19 6
D4-1Ø EOC Ø2 L — (EK2) 5
4 — 7432 E3 6 — 5 — 8093 E18 6 — 4
D4-5 ACTIVE Ø2 L — 4 — 7432 E22 6 — BK2 — D4-7 SERIAL IN Ø2 H

D4-9 SERIAL OUT Ø1 H — AB1 9 — T4Ø8 E9 8
D4-2 BREAK Ø1 (Ø) H — 1Ø
9 — 1488 E11 8 — J1 T — EIA XMIT DATA Ø1
EIA RCV DATA Ø1 — J1 N — 1Ø — 1489 E5 8
C12Ø 47ØPF — 9
D4-2 MAINT Ø1 H — 9 — 8094 E17 8 — 1Ø
D4-2 HALF DUPLEX Ø1 H — 9 — T4Ø8 E19 8
D4-9 EOC Ø1 L — (ER2) 1Ø
1Ø — 7432 E3 8 — 9 — 8093 E18 8 — 1Ø
D4-5 ACTIVE Ø1 L — 9 — 7432 E22 8 — BD1 — D4-7 SERIAL IN Ø1 H

D4-9 SERIAL OUT ØØ H — AJ2 12 — T4Ø8 E9 11
D4-2 BREAK ØØ (Ø) H — 13
12 — 1488 E11 11 — J1 R — EIA XMIT DATA ØØ
EIA RCV DATA ØØ — J1 L — 13 — 1489 E5 11
C129 47ØPF — 12
D4-2 MAINT ØØ H — 12 — 8094 E17 11 — 13
D4-2 HALF DUPLEX ØØ H — 12 — T4Ø8 E19 11
D4-9 EOC ØØ L — (RJ2) 13
12 — 7432 E3 11 — 12 — 8093 E18 11 — 13
D4-5 ACTIVE ØØ L — 12 — 7432 E22 11 — BF2 — D4-7 SERIAL IN ØØ H

(EIA IN & OUT, HALF DUPLEX, BREAK, MAINT LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES ØØ-03 (Ø4-7)	D	BS	DVII-Ø-15	*

SCALE — SHEET 7 OF 1Ø — DIST.

DVII-Ø-15 BS D

NOTES:
1. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FEATURE AT 9600 BAUD OR LESS.

DATA SET BUSY Ø3 — M89 E6 — D4-2 MAINT Ø3 L — T4H11 E33 — R38 1K — C118 47ØPF — D4-4 SPEED 17Ø3 H — *W6 — +5V
D4-1Ø EOC Ø3 L (EF2) — D4-1Ø TBMT Ø3 L — 8815 E65

DATA SET BUSY Ø2 — M89 E6 — D4-2 MAINT Ø2 L — T4H11 E33 — R37 1K — C109 47ØPF — D4-4 SPEED 17Ø2 H — *W5 — +5V
D4-1Ø EOC Ø2 L (EK2) — D4-1Ø TBMT Ø2 L — 8815 E65

DATA SET BUSY Ø1 — M89 E6 — D4-2 MAINT Ø1 L — T4H11 E33 — R36 1K — C112 47ØPF — D4-4 SPEED 17Ø1 H — *W4 — +5V
D4-9 EOC Ø1 L (ER2) — D4-9 TBMT Ø1 L — 8815 E79

DATA SET BUSY ØØ — M89 E6 — D4-2 MAINT ØØ L — T4H11 E69 — R35 1K — C110 47ØPF — D4-4 SPEED 17ØØ H — *W3 — +5V
D4-9 EOC ØØ L (FJ2) — D4-9 TBMT ØØ L — 8815 E79

D4-2 RESET L — 74ØØ E42 — R39 35Ø — +5V — 3ØNS DL2 — R40 47Ø — C121 27PF — 175 NS — 74123 E63 — +3VB — RT 1ØK — +5V
D4-2 RESET L — 74ØØ E42 — C120 56PF — 25Ø NS — 74123 E7Ø — +3VA — R42 1ØK — +5V
C122 15PF — 125 NS — 74123 E7Ø — R43 1ØK — +5V

T9175 E88 (D3 R3(Ø) R3(1) D2 R2(Ø) R2(1) D1 R1(Ø) R1(1) DØ RØ(Ø) RØ(1) CLR CLK)
T9318 E87 (AØ A1 A2 EO G9 E1)
T4155 E89 (STBØ STB1 DB DA SØ S1 FBØ FB1 FB2 FB3 FAØ FA1 FA2 FA3)

D4-2 RESET L
D4-8 TWRL Ø5 L — +3VA — T474 E74 — D4-3 TRAN FLAG CLK Ø5 L — T4ØØ E85 — D4-8 TRAN FLAG Ø5 H
D4-8 TWRL Ø2 L — +3VA — T474 E74 — D4-3 TRAN FLAG CLK Ø2 L — T4ØØ E85 — D4-8 TRAN FLAG Ø2 H
D4-8 TWRL Ø1 L — +3VA — T474 E84 — D4-3 TRAN FLAG CLK Ø1 L — T4ØØ E85 — D4-8 TRAN FLAG Ø1 H
D4-8 TWRL ØØ L — +3VA — T474 E84 — D4-3 TRAN FLAG CLK ØØ L — T4ØØ E85 — D4-8 TRAN FLAG ØØ H

D3-4 TRAN DATA Ø7 H — EP1
D3-4 TRAN DATA Ø6 H — EM2
D3-4 TRAN DATA Ø5 H — FR2
D3-4 TRAN DATA Ø4 H — FY2
D3-4 TRAN FILE LOAD L
D3-3 BUF MSCAN Ø1 L
D3-3 BUF MSCAN ØØ L
T7417Ø E78 (D3 D2 D1 DØ RD RA1 RAØ WR WA1 WAØ R3(1) R2(1) R1(1) RØ(1)) — D4-8 DB8 DB7 DB6 DB5

D3-4 TRAN DATA Ø3 H — FS2
D3-4 TRAN DATA Ø2 H — FV1
D3-4 TRAN DATA Ø1 H — FT2
D3-4 TRAN DATA ØØ H — FU2
T7417Ø E77 (D3 D2 D1 DØ RD RA1 RAØ WR WA1 WAØ R3(1) R2(1) R1(1) RØ(1)) — D4-8 DB4 DB3 DB2 DB1

(TRANSMIT FLAG SERVICING)

REVISIONS		
CHR	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES ØØØ3(Ø4-8)	D	BS	DV11-Ø-15	*
SCALE —	SHEET 8 OF 1Ø		DIST.	

DBS DV11-Ø-15

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-7 SERIAL IN ØØ H (BF2) 20 — SERIAL IN
D4-6 RESET DA ØØ L 18 — CLR R DONE
D4-6 RDE ØØ L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK ØØ H (DE2) 40 — X CLK
UART ØØ E76
D4-8 THRL ØØ L 23 — LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ
CLR NB1 NB2 2SB NP EP LDC
R DONE 19
OR ERR 15 — D4-9 OR ØØ
FR ERR 14 — D4-9 FE ØØ
P ERR 13 — D4-9 PE ØØ
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12
SERIAL OUT 25 — AJ2 — D4-9 SERIAL OUT ØØ H
XRDY 22 — 11 T4Ø4 E7J 10 — D4-9 TBMT ØØ L
EOC 24 — 9 T4Ø4 E8Ø 8 FJ2 — D4-9 EOC ØØ L
21 38 37 36 35 33 34
1 T4Ø4 E8Ø 2 — D4-9 DA ØØ L

D4-7 SERIAL IN Ø1 H (BD1) 20 — SERIAL IN
D4-6 RESET DA Ø1 L 18 — CLR R DONE
D4-6 RDE Ø1 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK Ø1 H (EE2) 40 — X CLK
UART Ø1 E81
D4-8 THRL Ø1 L 23 — LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ
CLR NB1 NB2 2SB NP EP LDC
R DONE 19
OR ERR 15 — D4-9 OR Ø1
FR ERR 14 — D4-9 FE Ø1
P ERR 13 — D4-9 PE Ø1
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12
SERIAL OUT 25 — AB1 — D4-9 SERIAL OUT Ø1 H
XRDY 22 — 11 T4Ø4 E8Ø 10 — D4-9 TBMT Ø1 L
EOC 24 — 13 T4Ø4 E8Ø 12 ER2 — D4-9 EOC Ø1 L
21 38 37 36 35 33 34
3 T4Ø4 E8Ø 4 — D4-9 DA Ø1 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV ØØ H
D4-2 UART STROBE ØØ H
D4-2 PEV Ø1 H
D4-2 UART STROBE Ø1 H

(UARTS ØØ & Ø1)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINESØØ-Ø3 (D4-9)
SIZE D | CODE BS | NUMBER DVII-Ø-15 | REV. *
SCALE | SHEET 9 OF Ø | DIST.

DBS DVII-Ø-15

D4-9 RDB
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-7 SERIAL IN Ø2 H (BX2) 20 — SERIAL IN
D4-6 RESET DA Ø2 L 18 — CLR R DONE
D4-6 RDE Ø2 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK Ø2 H (DS2) 40 — X CLK
UART Ø2 E67
D4-2 THRL Ø2 L 23 — LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ
CLR NBI NB2 2SB NP EP LDC
21 38 37 36 35 39 34

R DONE 19 — 1 74Ø4 E66 2 — D4-1Ø DA Ø2 L
OR ERR 15 — D4-1Ø OR Ø2
FR ERR 14 — D4-1Ø FE Ø2
P ERR 13 — D4-1Ø PE Ø2
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 — AT2 IM-1Ø SERIAL OUT Ø2 H
XRDY 22 — 5 74Ø4 E66 6 — D4-1Ø TSMT Ø2 L
EOC 24 — 9 74Ø4 E66 8 EK2 — D4-1Ø EOC Ø2 L

D4-7 SERIAL IN Ø3 H (BK1) 20 — SERIAL IN
D4-6 RESET DA Ø3 L 18 — CLR R DONE
D4-6 RDE Ø3 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK Ø3 H (CP2) 40 — X CLK
UART Ø3 E62
D4-8 THRL Ø3 L 23 — LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ
CLR NBI NB2 2SB NP EP LDC
21 38 37 36 35 39 34

R DONE 19 — 3 74Ø4 E66 4 — D4-1Ø DA Ø3 L
OR ERR 15 — D4-1Ø OR Ø3
FR ERR 14 — D4-1Ø FE Ø3
P ERR 13 — D4-1Ø PE Ø3
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 — AH2 D4-1Ø SERIAL OUT Ø3 H
XRDY 22 — 11 74Ø4 E66 1Ø — D4-1Ø TSMT Ø3 L
EOC 24 — 13 74Ø4 E66 12 EF2 — D4-1Ø EOC Ø3 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
IM-2 PEV Ø2 H
IM-2 UART STROBE Ø2 H
D4-2 PEV Ø3 H
D4-2 UART STROBE Ø3 H

(UARTS Ø2 & Ø3)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINESØØ-Ø3 (D4-1Ø)
SIZE D | CODE BS | NUMBER DV11-Ø-15 | REV. *
SCALE — | SHEET Ø OF 1Ø | DIST.

D BS DV11-Ø-15

BERG CONNECTOR

J1

- A
- B — DATA SET BUSY Ø4
- C
- D — DATA SET BUSY Ø5
- E
- F — DATA SET BUSY Ø6
- H — ASYN H
- J — DATA SET BUSY Ø7
- K
- L — EIA RCV DATA Ø4
- M
- N
- P — EIA RCV DATA Ø5
- R
- S — EIA XMIT DATA Ø4
- T
- U — EIA XMIT DATA Ø5
- V
- W — DV11 BUSY Ø4
- X
- Y — DV11 BUSY Ø5
- Z — DV11 BUSY Ø6
- AA
- BB — DV11 BUSY Ø7
- CC
- DD — EIA XMIT DATA Ø6
- EE
- FF — EIA XMIT DATA Ø7
- HH
- JJ — EIA RCV DATA Ø6
- KK — EIA RCV DATA Ø7
- LL
- MM
- NN
- PP
- RR
- SS
- TT
- UU
- VV

+5V — R1 330 — +3VA; C125 .01 µfd; R3 750

+5V — R2 330 — +3VB; C111 .01 µfd; R4 750

+15V — R50 3.9 1/2W — D1-12V (TO PIN 9 OF 1488) (TO PIN 14 OF 1488); D1 IN759A; C116 .01 µfd; C108 .01 µfd

-15V — FB2 — Q1 2N2904 — R44 10 — R45 10 — R46 10 — R47 10 — D4 D672 — D5 D672 — D6 D672 — D4-1-12V (TO PIN 1 OF 1488) (TO PIN 2 OF UART); R48 220; R49 470 1/2W; C127 1000PF; Q2 6534D; R5 1K; C124 6.8 µfd; R6 1K; D8 IN752A; D7 D672

+5V — C1-C95 .01 µfd; C96-C101 6.8 µfd — GND

CLOCK GENERATION CHART

CLOCK ADDRESS DCBA	BAUD RATE	PERIOD (USEC)
0000	50	1250.00
0001	75	833.33
0010	110	568.18
0011	134.5	464.68
0100	150	416.67
0101	300	208.33
0110	600	104.17
0111	1200	52.08
1000	1800	34.72
1001	2000	31.25
1010	2400	26.04
1011	3600	17.36
1100	4800	13.02
1101	7200	8.68
1110	9600	6.51
1111	38400	1.63

(CHART, REGULATORS)

DRN	1-13-76	FIRST USED ON: DV11
CHK	1-15-76	digital
ENG	1-15-76	TITLE: ASYNCH MUX LINE CARD LINES Ø4-Ø7 (D4-1)
PROJ. ENG	1-15-76	
PROD	1-16-76	
NEXT HIGHER ASSY.		
B-DD-DV11-Ø		SIZE D; CODE 85; NUMBER DV11-Ø-16; REV. *
SCALE		
SHEET OF 10		DIST

REVISIONS — REV. — CHANGE NO. — CHK

D4-2 RESET H
D3-7 INIT D1 L
EV2
7404 E7
7437 E40
D4-2 RESET L
+3VB
7474 E35
D4-2 MAINT Ø7 H
D4-2 MAINT Ø7 L
7474 E35
D4-2 MAINT Ø6 H
D4-2 MAINT Ø6 L
7474 E34
D4-2 MAINT Ø5H
D4-2 MAINT Ø5L
7474 E34
D4-2 MAINT Ø4 H
D4-2 MAINT Ø4 L
7404 E47
7404 E47
7404 E47
7404 E47
7404 E47
D4-2 BRG STROBE Ø7 H
D4-2 BRG STROBE Ø6 H
D4-2 BRG STROBE Ø5 H
D4-2 BRG STROBE Ø4 H
7404 E58
7424 E58
D4-2 UART STROBE Ø7 H
7404 E58
D4-2 UART STROBE Ø6 H
7404 E58
D4-2 UART STROBE Ø5 H
7404 E58
D4-2 UART STROBE Ø4 H
7404 E53
7404 E53
7404 E53
7404 E53
74154 E52
D2-3 LCR 1Ø
D2-3 LCR Ø9
D3-8 SR9 Ø1
D3-8 SR3 ØØ
DT2
AP2
BT2
BM2
+5V
R41 1ØK
C119 1ØØPF
D3-8 CONTROL STROBE H
CS2
D3-8 SR9 Ø3 L
D3-8 SR9 Ø2 H
AS2
BR2
7400 E62
74123 E53 400NS
STB1 STBØ
D12
D4-2 CARD PARAMETER SELECT Ø4 Ø7 L
+3VA
D2-3 LCR 14 H
D2-3 LCR 13 H
D2-3 LCR 12 H
D2-3 LCR 11 H
AL2
BA1
AM2
AN2
7404 E7
D4-2 PEN L
7437 E12
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
74175 E24
D4-2 BREAK Ø7 (Ø) H
D4-2 RCV ENBL Ø7 (Ø) H
D4-2 PEV Ø7 H
D4-2 HALF DUPLEX Ø7 H
74175 E13
D4-2 BREAK Ø6 (Ø) H
D4-2 RCV ENBL Ø6 (Ø) H
D4-2 PEV Ø6 H
D4-2 HALF DUPLEX Ø6 H
74175 E8
D4-2 BREAK Ø5 (Ø) H
D4-2 RCV ENBL Ø5 (Ø) H
D4-2 PEV Ø5 H
D4-2 HALF DUPLEX Ø5 H
74175 E14
D4-2 BREAK Ø4 (Ø) H
D4-2 RCV ENBL Ø4 (Ø) H
D4-2 PEV Ø4 H
D4-2 HALF DUPLEX Ø4 H
CLR CLK

(CARD SELECTION, REGISTERS, STROBES, INIT)

REVISIONS		
CHR	CHANGE NO.	REV.

TITLE	ASYNCH MUX LINE CARD LINES Ø4-Ø7(04-2)			
SIZE	CODE	NUMBER		REV.
D	BS	DV11-Ø-16		*
SCALE		SHEET 2 OF 10		DIST.

MADE IN U.S.A.

D3-4 MASTER SCAN D H
D3-4 MASTER SCAN Ø2 H
EU2 12
EN2 13
7400 E68
11
DM2 D4-3 CARD FLAG SELECT Ø4-Ø7 L
7404 ET3

D3-3 RESYNC PULSE L
DF2 15
74155 E60
STBB STBA
DB
SI
SØ
9 D4-3 RESYNC PULSE Ø7 L
10 D4-3 RESYNC PULSE Ø6 L
11 D4-3 RESYNC PULSE Ø5 L
12 D4-3 RESYNC PULSE Ø4 L
7 D4-3 TRAN FLAG CLK Ø7 L
6 D4-3 TRAN FLAG CLK Ø6 L
5 D4-3 TRAN FLAG CLK Ø5 L
4 D4-3 TRAN FLAG CLK Ø4 L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L

D3-4 TRANSMITTER STROBE H
EH2 4
5
7400 E68
6
3
7404 E53
4
D4-3 TRAN FILE LOAD L

D4-6 RCV FLAG Ø7 H
D4-6 RCV FLAG Ø6 H
D4-6 RCV FLAG Ø5 H
D4-6 RCV FLAG Ø4 H
D4-5 MATCH Ø7 (1) H
D4-5 MATCH Ø6 (1) H
D4-5 MATCH Ø5 (1) H
D4-5 MATCH Ø4 (1) H
74155 E37
STBØ STB1
AI
BI
CI
DI
AØ
BØ
CØ
DØ
SI
SØ
9
7
7432 ET2
8881 E82
FM2 RECEIVER FLAG L
FE1 MATCH DETECT L

+5V
RB 10K
D1-5 RECEIVED DATA ENABLE H
CN2 9
10
7400 E68
8
2
14
15
13
FJJ1 D4-3 RDE Ø4-Ø7
74123 E63
TS
NS
+3VB
FK1 D4-3 DATA ENABLE Ø4-Ø7 H
D4-3 MATCH H
7474 E36
7437 E40
D4-2 RESET L

D3-4 MASTER SCAN Ø1 H
EM1 5
7404 E73
6
D3-4 MASTER SCAN ØØ H
EN1 9
7404 E73
8

D4-8 TRAN FLAG Ø7 H
D4-8 TRAN FLAG Ø6 H
D4-8 TRAN FLAG Ø5 H
D4-8 TRAN FLAG Ø4 H
74155 E83
STBI STBØ
AI
BI
CI
DI
AØ
BØ
CØ
DØ
SI
SØ
9
7
8881 E82
FL2 TRAN FLAG WAITING L

D3-4 MASTER SCAN T/R
CR2 3
7404 ET3
4

74155 E31
STBB STBA
DB
DA
SI
SØ
9 D4-3 CLR RCV FLAG Ø7 L
10 D4-3 CLR RCV FLAG Ø6 L
11 D4-3 CLR RCV FLAG Ø5 L
12 D4-3 CLR RCV FLAG Ø4 L
7 D4-3 CLR MATCH Ø7 L
6 D4-3 CLR MATCH Ø6 L
5 D4-3 CLR MATCH Ø5 L
4 D4-3 CLR MATCH Ø4 L

(SCAN SELECTION. FLAGS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES Ø4-Ø7(04-3)
SIZE D CODE BS NUMBER DV11-Ø-16 REV. *
SCALE — SHEET 3 OF 10 DIST.

DBS DV11-Ø-16

R9 10K
R10 10K
C126 22PF
C123 22PF
7380 E93
7380 E93
Y1 2.4576 MHZ
R11 1K
C200 22PF
7404 E80
W2 (W2 REMOVED FOR AUTOMATED MODULE TEST)
D4-2 RESET H
7493 E92
R3(1) R2(1) R1(1) R0(1) CLK0 CLKBC CLR
BN2 D4-4 SOURCE CLOCK B Ø4-Ø7 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
COM 5016 E51
TD TC TB TA STT EXT2 EXT1 RD RC RB RA STR 6T 4R
D4-1 +12V
BJ1 D4-4 SOURCE CLOCK A Ø4-Ø7 L
5.0688 MHZ E27
+5V
W1 (W1 REMOVED FOR AUTOMATED MODULE TEST)
7437 E46
7437 E46
COM 5016 E57
D4-1 +12V
+3VA
D4-2 BRG STROBE Ø7 H
D4-2 BRG STROBE Ø6 H
D4-2 BRG STROBE Ø5H
D4-2 BRG STROBE Ø4 H
D4-2 RESET L
7420 E39
7474 E45
7474 E45
7474 E55
7474 E55
D4-4 SPEED 17Ø7 H
D4-4 SPEED 17Ø6 H
D4-4 SPEED 17Ø5 H
D4-4 SPEED 17Ø4 H
8Ø34 E56
8Ø93 E5Ø
CP2 D4-4 CLOCK Ø7 H
DS2 D4-4 CLOCK Ø6 H
CE2 D4-4 CLOCK Ø5 H
DE2 D4-4 CLOCK Ø4 H

(CRYSTAL CLOCK GENERATION)

REVISIONS		
CHG	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES Ø4-Ø7 (D4-4)
SIZE D CODE BS NUMBER DV11-Ø-16 REV. *
SCALE — SHEET 4 OF 1Ø DIST.

DV11-Ø-16 BS D 8

D4-6 ENBL ERROR FLAGS L

D4-10 OR Ø⁻
D4-10 OR Ø₀
D4-9 OR Ø₅
D4-9 OR Ø₄

D4-10 PE Ø7
D4-10 PE Ø6
D4-9 PE Ø5
D4-9 PE Ø4

D4-10 FE Ø7
D4-10 FE Ø6
D4-9 FE Ø5
D4-9 FE Ø4

74153 E71
74153 E75
74153 E64
74H11 E69
74Ø4 E53
74170 E54
74170 E55
74170 E56

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-3 BUF MSCAN ØØ L
D4-3 BUF MSCAN Ø1 L
D4-3 CARD FLAG SELECT Ø4-Ø7 L

D4-6 RCV FILE LOAD L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE ADDRS ØØ L
D4-3 DATA ENABLE Ø4-Ø7 H

8881 E86 — FL1 — MASTER OR L
8881 E86 — FM1 — MASTER PE L
8881 E86 — FH1 — RECV DATA Ø7 L
8881 E86 — FJ1 — RECV DATA Ø6 L
8881 E9Ø — FR1 — RECV DATA Ø5 L
8881 E9Ø — FS1 — RECV DATA Ø4 L
8881 E9Ø — FN1 — RECV DATA Ø3 L
8881 E9Ø — FP1 — RECV DATA Ø2 L
8881 E91 — FN2 — RECV DATA Ø1 L
8881 E91 — FR2 — RECV DATA ØØ L

R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 — 1K / 10K — +5V

D4-2 RCV ENBL Ø7 (1) H
C1Ø2 27 PF
74123 E2 — 74Ø8 E3Ø — 7474 E23 — 7474 E25
D4-3 CLR MATCH Ø7 L
D4-3 RESYNC PULSE Ø7 L
D4-2 RCV ENBL Ø7(1)H
D4-5 MATCH Ø7(1)H
D4-5 ACTIVE Ø7 H
D4-5 ACTIVE Ø7 L

D4-2 RCV ENBL Ø6(1)H
C1Ø3 27PF
D4-3 CLR MATCH Ø6 L
D4-3 RESYNC PULSE Ø6 L
D4-2 RCV ENBL Ø6(1) H
D4-5 MATCH Ø6(1)H
D4-5 ACTIVE Ø6 H
D4-5 ACTIVE Ø6 L

D4-2 RCV ENBL Ø5(1) H
C1Ø4 27PF
74123 E1Ø — 74Ø8 E2Ø — 7474 E25
D4-3 CLR MATCH Ø5 L
D4-3 RESYNC PULSE Ø5 L
D4-2 RCV ENBL Ø5(1) H
D4-5 MATCH Ø5(1) H
D4-5 ACTIVE Ø5 H
D4-5 ACTIVE Ø5 L

D4-2 RCV ENBL Ø4 (1) H
C1Ø7 27 PF
74123 E1Ø — 74Ø8 E2Ø — 7474 E15
D4-3 CLR MATCH Ø4 L
D4-3 RESYNC PULSE Ø4 L
D4-2 RCV ENBL Ø4 (1) H
D4-5 MATCH Ø4 (1) H
D4-5 ACTIVE Ø4 H
D4-5 ACTIVE Ø4 L

(RCV FILES, RCV DATA, MATCH LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø4-Ø7(04-5)	D	8S	DV11-Ø-16	*
SCALE —	SHEET 5 OF 1Ø		DIST.	

+3VA
+3VB
+5V
D4-10 DA Ø7 L
D4-10 DA Ø6 L
D4-9 DA Ø5 L
D4-9 DA Ø4 L
D4-6 RCV FLAG Ø7 H
D4-6 RCV FLAG Ø6 H
D4-6 RCV FLAG Ø5 H
D4-6 RCV FLAG Ø4 H
D4-3 CLR RCV FLAG Ø7 L
D4-5 ACTIVE Ø7 H
D4-3 CLR RCV FLAG Ø6 L
D4-5 ACTIVE Ø6 H
D4-3 CLR RCV FLAG Ø5 L
D4-5 ACTIVE Ø5 H
D4-3 CLR RCV FLAG Ø4 L
D4-5 ACTIVE Ø4 H
D4-6 RESET DA Ø7 L
D4-6 RESET DA Ø6 L
D4-6 RESET DA Ø5 L
D4-6 RESET DA Ø4 L
D4-6 RDE Ø7 L
D4-6 RDE Ø6 L
D4-6 RDE Ø5 L
D4-6 RDE Ø4 L
DV11 BUSY Ø7
DV11 BUSY Ø6
DV11 BUSY Ø5
DV11 BUSY Ø4
ASYN H
D4-6 ENBL ERROR FLAGS L
D4-6 RCV FILE ADDRS Ø0 L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RECEIVER SAMPLE CLOCK H
D4-6 RCV FILE LOAD L
D4-2 RESET L
RDE
RDE DLY
LOAD FILE
WAIT DLY
SAMPLE CLK
SAMPLE DELAY
RESET DA
(RECEIVER FLAG SERVICE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES Ø4-07(04-6)
SIZE D | CODE 85 | NUMBER DV11-Ø-16 | REV. *
SCALE — | SHEET 6 OF 10 | DWG. | DV11-Ø-16

D4-10 SERIAL OUT Ø7 H
D4-2 BREAK Ø7 (Ø) H
AH2
7408 E9
1488 E11
J1 EE
EIA XMIT DATA Ø7
EIA RCV DATA Ø7
KK
1489 E5
C106 470PF
8094 E17
D4-2 MAINT Ø 7H
8093 E18
7432 E3
D4-2 HALF DUPLEX Ø 7 H
D4-10 EOC Ø7 L
(EF2) 2
7408 E19
D4-5 ACTIVE Ø7 L
7432 E22
8K1
D4-7 SERIAL IN Ø7 H

D4-10 SERIAL OUT Ø6 H
D4-2 BREAK Ø6 (Ø) H
AT2
7408 E9
1488 E11
J1 CC
EIA XMIT DATA Ø6
EIA RCV DATA Ø6
HH
1489 E5
C105 470PF
8094 E17
D4-2 MAINT Ø 6H
8093 E18
7432 E3
D4-2 HALF DUPLEX Ø6 H
D4-10 EOC Ø6 L
(EK2) 5
7408 E19
D4-5 ACTIVE Ø6 L
7432 E22
8K2
D4-7 SERIAL IN Ø6 H

D4-9 SERIAL OUT Ø5 H
D4-2 BREAK Ø5(Ø)H
A81
7408 E9
1488 E11
J1 T
EIA XMIT DATA Ø5
EIA RCV DATA Ø5
N
1489 E5
C128 470PF
8094 E17
D4-2 MAINT Ø5 H
8093 E18
7432 E3
D4-2 HALF DUPLEX Ø5 H
D4-9 EOC Ø5 L
(ER2) 10
7408 E19
D4-5 ACTIVE Ø5 L
7432 E22
8D1
D4-7 SERIAL IN Ø5 H

D4-9 SERIAL OUT Ø4 H
D4-2 BREAK Ø4 (Ø) H
AJ2
7408 E9
1488 E11
J1 R
EIA XMIT DATA Ø4
EIA RCV DATA Ø4
L
1489 E5
C129 470 PF
8094 E17
D4-2 MAINT Ø4 H
8093 E18
7432 E3
D4-2 HALF DUPLEX Ø4 H
D4-9 EOC Ø4 L
(KJ2) 13
7408 E19
D4-5 ACTIVE Ø4 L
7432 E22
BF2
D4-7 SERIAL IN Ø4 H

(EIA IN & OUT. HALF DUPLEX. BREAK. MAINT LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø4-Ø7 (D4-7)	D	8S	DV11-Ø16	*

SCALE — SHEET 7 OF 10 — DIST.

D8SDV11-Ø-16

NOTES:

1. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FEATURE AT 9600 BAUD OR LESS.

DATA SET BUSY Ø7 — M89 E66 — C118 47ØPF — D4-2 MAINT Ø7 L — T4H11 E33 — R38 1K — D4-4 SPEED 1TØ7 H — * W6 — +5V

DATA SET BUSY Ø6 — M89 E66 — C109 47ØPF — D4-2 MAINT Ø6 L — T4H11 E33 — R37 1K — D4-4 SPEED 1TØ6 H — * W5 — +5V

DATA SET BUSY Ø5 — M89 E66 — C112 47ØPF — D4-2 MAINT Ø6 L — T4H11 E33 — R36 1K — D4-4 SPEED 1TØ5 H — * W4 — +5V

DATA SET BUSY Ø4 — M89 E66 — C110 47ØPF — D4-2 MAINT Ø4 L — T4H11 E69 — R35 1K — D4-4 SPEED 1TØ4 H — * W3 — +5V

D4-1Ø EOC Ø7 L (EF2) — D4-1Ø TBMT Ø7 L — 8815 E65
D4-1Ø EOC Ø6 L (EK2) — D4-1Ø TBMT Ø6 L — 8815 E65
D4-9 EOC Ø5 L (ER2) — D4-9 TBMT Ø5 L — 8815 E79
D4-9 EOC Ø4 L (FJ2) — D4-9 TBMT Ø4 L — 8815 E79

D4-2 RESET L

D4-8 THRL Ø7 L — +3VA — T474 E74 — D4-3 TRAN FLAG CLK Ø7 L — T4Ø8 E85 — D4-8 TRAN FLAG Ø7 H
D4-8 THRL Ø6 L — +3VA — T474 E74 — D4-3 TRAN FLAG CLK Ø6 L — T4Ø8 E85 — D4-8 TRAN FLAG Ø6 H
D4-8 THRL Ø5 L — +3VA — T474 E84 — D4-3 TRAN FLAG CLK Ø5 L — T4Ø8 E85 — D4-8 TRAN FLAG Ø5H
D4-8 THRL Ø4 L — +3VA — T474 E84 — D4-3 TRAN FLAG CLK Ø4 L — T4Ø8 E85 — D4-8 TRAN FLAG Ø4 H

T9175 E88 — DS R3(1) R3(Ø) — D2 R2(1) R2(Ø) — D1 R1(1) R1(Ø) — DØ RØ(1) RØ(Ø) — CLR CLK

3318 E87 — A Ø 1 2 — E Ø G Ø — E1

STBB STBA — DB — T4155 E89 — DA — SØ S1 — FBØ FB1 FB2 FB3 — 4AØ 4A1 4A2 4A3

D3-4 TRAN DATA Ø7 H — EP1 — D4-8 DB8
D3-4 TRAN DATA Ø6 H — EM2 — D4-8 DB7
D3-4 TRAN DATA Ø5 H — FR2 — D4-8 DB6
D3-4 TRAN DATA Ø4 H — FY2 — D4-8 DB5

T4174 E74 — RD RA1 RAØ — D3 D2 D1 DØ — R3(1) R2(1) R1(1) RØ(1) — WR WA1 WAØ

D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L

D3-4 TRAN DATA Ø3 H — FS2 — D4-8 DB4
D3-4 TRAN DATA Ø2 H — FV1 — D4-8 DB3
D3-4 TRAN DATA Ø1 H — FT2 — D4-8 DB2
D3-4 TRAN DATA ØØ H — FU2 — D4-8 DB1

T4174 E77

M4Ø8 E42 — +5V — R39 33Ø — 3ØNS DL2 — R4Ø 47Ø — C121 27PF — R7 1ØK — T4123 E63 — 175 NS — +3VB

C120 56PF — R92 1ØK — T4123 E7Ø — 25Ø NS

C122 15PF — R93 1ØK — T4123 E7Ø — 125 NS

(TRANSMIT FLAG SERVICING)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø4-Ø7(Ø4-8)	D	BS	DV11-Ø-16	*
SCALE —	SHEET 8 OF 1Ø	DIST.		

DBS DV11-Ø-16

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

1 T4Ø4 E8Ø 2 — D4-9 DA Ø4 L

D4-7 SERIAL IN Ø4 H (BF2) 20 SERIAL IN
D4-6 RESET DA Ø4 L 18 CLR R DONE
D4-6 RDE Ø4 L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø4 H (DE2) 40 X CLK

UART Ø4 E76

D4-8 THRL Ø4 L 23 LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ

R DONE 19
OR ERR 15 — D4-9 OR Ø4
FR ERR 14 — D4-9 FE Ø4
P ERR 13 — D4-9 PE Ø4
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12

A12 — D4-9 SERIAL OUT Ø4 H
SERIAL OUT 25
XRDY 22 — 11 T4Ø4 E73 10 — D4-9 TBMT Ø4 L
EOC 24 — 9 T4Ø4 E8Ø 8 FJ2 — D4-9 EOC Ø4 L

CLR NB1 NB2 PSB NP EP LDC
21 38 37 36 35 33 34

3 T4Ø4 E8Ø 4 — D4-9 DA Ø5 L

D4-7 SERIAL IN Ø5 H (BD1) 20 SERIAL IN
D4-6 RESET DA Ø5 L 18 CLR R DONE
D4-6 RDE Ø5 L 4 STB RD
16 STB STATUS
17 R CLK
D4-4 CLOCK Ø5 H (CE2) 40 X CLK

UART Ø5 E81

D4-8 THRL Ø5 L 23 LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XDØ

R DONE 13
OR ERR 15 — D4-9 OR Ø5
FR ERR 14 — D4-9 FE Ø5
P ERR 13 — D4-9 PE Ø5
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12

AB1 — D4-9 SERIAL OUT Ø5H
SERIAL OUT 25
XRDY 22 — 11 T4Ø4 E8Ø 10 — D4-9 TBMT Ø5 L
EOC 24 — 13 T4Ø4 E8Ø 12 ER2 — D4-9 EOC Ø5L

CLR NB1 NB2 PSB NP EP LDC
21 38 37 36 35 33 34

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV Ø4 H
D4-2 UART STROBE Ø4 H
D4-2 PEV Ø5 H
D4-2 UART STROBE Ø5 H

(UARTS Ø4 & Ø5)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø4Ø7 (04-9)	D	BS	DVII-Ø-16	*
SCALE	SHEET 9 OF 10		DWG.	

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-7 SERIAL IN Ø6 H (BK2) 20 — SERIAL IN
D4-6 RESET DA Ø6 L 18 — CLR R DONE
D4-6 RDE Ø6 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK Ø6 H (DS2) 40 — X CLK
UART Ø6 E67
D4-8 THRL Ø6 L 23 — LD XD
33 — XDT
32 — XD6
31 — XD5
30 — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ
CLR NPI MR2 2:8 NP EP LDC
21 38 37 36 35 39 34

R DONE 19 → 74Ø4 E66 1→2 → D4-1Ø DA Ø6 L
OR ERR 15 → D4-1Ø OR Ø6
FR ERR 14 → D4-1Ø FE Ø6
P ERR 13 → D4-1Ø PE Ø6
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 → AT2 D4-1Ø SERIAL OUT Ø6 H
XRDY 22 → 74Ø4 E66 5→6 → D4-1Ø TBMT Ø6 L
EOC 24 → 74Ø4 E66 9→8 EX2 → D4-1Ø EOC Ø6 L

D4-7 SERIAL IN Ø7 H (BK1) 20 — SERIAL IN
D4-6 RESET DA Ø7 L 18 — CLR R DONE
D4-6 RDE Ø7 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK Ø7 H (CP2) 40 — X CLK
UART Ø7 E62
D4-8 THRL Ø7 L 23 — LD XD
33 — XDT
32 — XD6
31 — XD5
30 — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ
CLR NPI MR2 2:6 NP EP LDC
21 38 37 36 35 39 34

R DONE 19 → 74Ø4 E66 3→4 → D4-1Ø DA Ø7 L
OR ERR 15 → D4-1Ø OR Ø7
FR ERR 14 → D4-1Ø FE Ø7
P ERR 13 → D4-1Ø PE Ø7
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 → AH2 D4-1Ø SERIAL OUT Ø7 H
XRDY 22 → 74Ø4 E66 11→1Ø → D4-1Ø TBMT Ø7 L
EOC 24 → 74Ø4 E66 13→12 EFZ → D4-1Ø EOC Ø7 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV Ø6 H
D4-2 UART STROBE Ø6 H
D4-2 PEV Ø7 H
D4-2 UART STROBE Ø7 H

(UARTS Ø6 & Ø7)

REVISIONS
CHR. | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINES Ø4-Ø7 (Ø4-1Ø)
SIZE D | CODE BS | NUMBER DV11-Ø-16 | REV. *
SCALE — | SHEET Ø OF 1Ø | CHST.

D BS DV11-Ø-16

BERG CONNECTOR

J1

- A — DATA SET BUSY Ø8
- B — DATA SET BUSY Ø9
- C — DATA SET BUSY 1Ø
- D — ASYN H
- E — DATA SET BUSY 11
- F — EIA RCV DATA Ø8
- H — EIA RCV DATA Ø9
- J — EIA XMIT DATA Ø8
- K — EIA XMIT DATA Ø9
- L — DV11 BUSY Ø8
- M — DV11 BUSY Ø9
- N — DV11 BUSY 1Ø
- P — DV11 BUSY 11
- R — EIA XMIT DATA 1Ø
- S — EIA XMIT DATA 11
- T — EIA RCV DATA 1Ø
- U — EIA RCV DATA 11
- V, W, X, Y, Z, AA, BB, CC, DD, EE, FF, HH, JJ, KK, LL, MM, NN, PP, RR, SS, TT, UU, VV — (no connection)

+5V — R1 330 — +3VA; C125 .Ø1 µfd; R3 75Ø

+5V — R2 330 — +3VB; C111 .Ø1 µfd; R4 75Ø

+15V — CU1 — RSØ 3.9 1/2W — D1-1+12V (TO PIN 9 OF 5Ø1Ø) (TO PIN 14 OF 1488); D1 IN759A; C116 .Ø1 µfd; C1Ø8 .Ø1 µfd

-15V — FB2 — Q1 2N2Ø4 — R44 1Ø; R45 1Ø; R46 1Ø; R47 1Ø; D4 D672; D5 D672; D6 D672; R48 22Ø; R49 47Ø 1/2W; C12T 1ØØØ PF; Q2 65340; R5 1K; R6 1K; D8 IN752A; D7 D672; C124 6.8 µfd; D4-1 -12V (TO PIN 1 OF 1488) (TO PIN 2 OF UART)

+5V — C1-C95 .Ø1 µfd; C96-C1Ø1 6.8 µfd — GND

CLOCK GENERATION CHART

CLOCK ADDRESS DCBA	BAUD RATE	PERIOD (USEC)
ØØØØ	50	1250.00
ØØØ1	75	833.33
ØØ1Ø	110	568.18
ØØ11	134.5	464.68
Ø1ØØ	150	416.67
Ø1Ø1	300	208.33
Ø11Ø	600	104.17
Ø111	1200	52.08
1ØØØ	1800	34.72
1ØØ1	2000	31.25
1Ø1Ø	2400	26.04
1Ø11	3600	17.36
11ØØ	4800	13.02
11Ø1	7200	8.68
111Ø	9600	6.51
1111	38400	1.63

(CHART: REGULATORS)

DRN		4-13-76
CHK		4-15-76
ENG		4-15-76
PROJ. ENG.		4-15-76
PROD.		4-16-76
NEXT HIGHER ASSY.	B-DD-DV11-Ø	
SCALE		
SHEET	OF 1Ø	

FIRST USED ON: DV11

TITLE: ASYNCH MUX LINE CARD LINES Ø8-11 (D4-1)

SIZE D — CODE 8S — NUMBER DV11-Ø-17 — REV *

DIST.

REVISIONS — LTR — CHANGE NO.

DV11-Ø-17

D3-7 INIT D1 L — EV2 — 7404 E7 — D4-2 RESET H — D4-2 RESET L

7437 E40

+3VB

7474 E35 — D4-2 MAINT 11 H / D4-2 MAINT 11 L

7474 E35 — D4-2 MAINT 10 H / D4-2 MAINT 10 L

7474 E34 — D4-2 MAINT 09 H / D4-2 MAINT 09 L

7474 E34 — D4-2 MAINT 08 H / D4-2 MAINT 08 L

7404 E47

74154 E52 — D2-3 LCR 10 — DT2 — D3; D2-3 LCR 09 — AP2 — D2; D3-8 SRS 01 — BT2 — D1; D3-8 SRS 00 — BM2 — D0

7404 E47 — D4-2 BRG STROBE 11 H

7404 E47 — D4-2 BRG STROBE 10 H

7404 E58 — D4-2 BRG STROBE 09 H

7404 E58 — D4-2 BRG STROBE 08 H

7404 E58 — D4-2 UART STROBE 11 H

7404 E58 — D4-2 UART STROBE 10 H

7404 E58 — D4-2 UART STROBE 04 H

7404 E58 — D4-2 UART STROBE 00 H

7404 E53

7404 E53

7404 E53

+5V — R41 10K — C119 100 PF

D2-3 CONTROL STROBE H — CS2 — D3-8 SRS 03 H — BA2 — D3-8 SRS 02 L — BR2 — 7400 E68 — 74123 E59 — DJ2 — D4-2 CARD PARAMETER SELECT 08-11 L

+3VA

D4-2 PEN L

D2-3 LCR 14 H — AL2 — 7404 E7 — 7437 E12 — D4-2 BUF LCR 14 H

D2-3 LCR 13 H — BA1 — 7404 E7 — 7437 E12 — D4-2 BUF LCR 13 H

D2-3 LCR 12 H — AM2 — 7404 E7 — 7437 E12 — D4-2 BUF LCR 12 H

D2-3 LCR 11 H — AN2 — 7404 E7 — 7437 E12 — D4-2 BUF LCR 11 H

74175 E24 — D4-2 BREAK 11 (00) H; D4-2 RCV ENBL 11 (01) H; D4-2 PEV 11 H; D4-2 HALF DUPLEX 11 H

74175 E13 — D4-2 BREAK 10 (01) H; D4-2 RCV ENBL 10 (01) H; D4-2 PEV 10 H; D4-2 HALF DUPLEX 10 H

74175 E8 — D4-2 BREAK 09 (02) H; D4-2 RCV ENBL 09 (01) H; D4-2 PEV 09 H; D4-2 HALF DUPLEX 09 H

74175 E14 — D4-2 BREAK 08 (03) H; D4-2 RCV ENBL 08 (01) H; D4-2 PEV 08 H; D4-2 HALF DUPLEX 08 H

(CARD SELECTION, REGISTERS, STROBES, INIT)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ASYNCH MUX LINE CARD LINES 08-11 (D4-2)
SIZE: D — CODE: BS — NUMBER: DV11-0-17 — REV: *
SCALE — SHEET 2 OF 10 — D-ST.

DBS DV11-0-17

D3-4 MASTER SCAN Ø3 H
Ø3-4 MASTER SCAN C H
EU2
EN2
T4ØØ E68
DM2
D4-3 CARD FLAG SELECT Ø8-11 L
T4Ø4 ET3
STBB STBA
D3-3 RESYNC PULSE L
DF2
DB
T4155 E6Ø
ΦBØ
ΦB1
ΦB2
ΦB3
D4-3 RESYNC PULSE 11 L
D4-3 RESYNC PULSE 1Ø L
D4-3 RESYNC PULSE Ø9 L
D4-3 RESYNC PULSE Ø8 L
D3-4 TRANSMITTER STROBE H
EH2
T4ØØ E68
T4Ø4 ES3
ΦAØ
ΦA1
ΦA2
ΦA3
DA
D4-3 TRAN FLAG CLK 11 L
D4-3 TRAN FLAG CLK 1Ø L
D4-3 TRAN FLAG CLK Ø9 L
D4-3 TRAN FLAG CLK Ø8 L
D4-3 TRAN FILE LOAD L
SI
SØ
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
STBØ STB1
D4-6 RCV FLAG 11 H
D4-6 RCV FLAG 1Ø H
D4-6 RCV FLAG Ø9 H
D4-6 RCV FLAG Ø8 H
AI
BI
CI
DI
T4153 E37
D4-5 MATCH 11 (1) H
D4-5 MATCH 1Ø (1) H
D4-5 MATCH Ø9 (1) H
D4-5 MATCH Ø8 (1) H
AØ
BØ
CØ
DØ
FØ
T4132 ET2
8881 E82
FM2
RECEIVER FLAG L
+5V
R8 1Ø K
D1-5 RECEIVED DATA ENABLE H
CN2
FU1
D4-3 RDE Ø8-11
T4123 E63
T4 N3 Ø
FK1
D4-3 DATA ENABLE Ø8-11 H
+3V8
D4-3 MATCH H
T474 E36
T4Ø3T E4Ø
D4-2 RESET L
FE1
MATCH DETECT L
STBB STBA
D4-3 CLR RCV FLAG 11 L
D4-3 CLR RCV FLAG 1Ø L
D4-3 CLR RCV FLAG Ø9 L
D4-3 CLR RCV FLAG Ø8 L
T4155 E31
ΦBØ
ΦB1
ΦB2
ΦB3
DB
DA
ΦAØ
ΦA1
ΦA2
ΦA3
D4-3 CLR MATCH 11 L
D4-3 CLR MATCH 1Ø L
D4-3 CLR MATCH Ø1 L
D4-3 CLR MATCH Ø8 L
SI
SØ
D3-4 MASTER SCAN Ø1 H
EM1
T4Ø4 ET3
D3-4 MASTER SCAN Ø8 H
EN1
STBI STBØ
D4-8 TRAN FLAG 11 H
D4-8 TRAN FLAG 1Ø H
D4-8 TRAN FLAG Ø1 H
D4-8 TRAN FLAG ØØ H
T4153 E83
AI
BI
CI
DI
AØ
BØ
CØ
DØ
FI
FØ
SI
SØ
D3-4 MASTER SCAN T/R
CR2
FL2
TRAN FLAG WAITING L
(SCAN SELECTION. FLAGS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES Ø8-11 (D4-3)
SIZE D | CODE 8S | NUMBER DV11-Ø-17 | REV. *
SCALE | SHEET 3 OF 1Ø | DIST.

DV11-Ø-17 D 8S

R9 10K
R10 10K
C126 22PF
C123 22PF
7380 E93
7380 E95
Y1 2.4576 MHZ
R11 1K
C200 22PF
7404 E80
W2
(W2 REMOVED FOR AUTOMATED MODULE TEST)
7493 E92
D4-2 RESET H
CLR
R3(1)
R2(1)
R1(2)
R0(1)
CLK0 CLK1
BN2
D4-4 SOURCE CLOCK B Ø8-11 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
COM 5016 E51
COM 5016 E57
D4-1 +12V
BJ1
D4-4 SOURCE CLOCK A Ø8-11 L
5MHZ E27
+5V
W1
(W1 REMOVED FOR AUTOMATED MODULE TEST)
7437 E46
7420 E39
D4-2 BRG STROBE 11 H
D4-2 BRG STROBE Ø H
D4-2 BRG STROBE Ø9 H
D4-2 BRG STROBE Ø8 H
D4-2 RESET L
+3VA
7474 E45
7474 E55
D4-4 SPEED 17Ø3 H
D4-4 SPEED 17Ø2 H
D4-4 SPEED 17Ø1 H
D4-4 SPEED 17Ø0 H
8034 E56
8033 E50
CP2 D4-4 CLOCK 11 H
DS2 D4-4 CLOCK 10 H
CE2 D4-4 CLOCK Ø9 H
DE2 D4-4 CLOCK Ø8 H

REVISIONS		
CHK	CHANGE NO.	REV.

(CRYSTAL. CLOCK GENERATION)

TITLE ASYNCH MUX LINE CARD LINES Ø8-11 (D4-4)
SIZE D CODE BS NUMBER DV11-Ø-17 REV. *
SCALE — SHEET 4 OF 10 DIST.

D4-6 ENBL ERROR FLAGS L

D4-Ø OR 11
D4-1Ø OR 1Ø
D4-9 OR Ø9
D4-9 OR Ø8

D4-Ø PE 11
D4-1Ø PE 1Ø
D4-9 PE Ø9
D4-9 PE Ø8

D4-Ø FE 11
D4-1Ø FE 1Ø
D4-9 FE Ø9
D4-9 FE Ø8

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5

D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-3 BUF MSCAN ØØ L
D4-3 BUF MSCAN Ø1 L
D4-3 CARD FLAG SELECT Ø2 L

D4-6 RCV FILE LOAD L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE ADDRS ØØ L
D4-3 DATA ENABLE Ø8-11 H

MASTER OR L
MASTER PE L
RECV DATA Ø7 L
RECV DATA Ø6 L
RECV DATA Ø5 L
RECV DATA Ø4 L
RECV DATA Ø3 L
RECV DATA Ø2 L
RECV DATA Ø1 L
RECV DATA ØØ L

D4-2 RCV ENBL 11 (1) H
D4-3 CLR MATCH 11 L
D4-3 RESYNC PULSE 11 L
D4-2 RCV ENBL 11 (1) H
D4-5 MATCH 11 . 01) H
D4-5 ACTIVE 11 H
D4-5 ACTIVE 11 L

D4-2 RCV ENBL 1Ø (1) H
D4-3 CLR MATCH 1Ø L
D4-3 RESYNC PULSE 1Ø L
D4-2 RCV ENBL 1Ø (1) H
D4-5 MATCH 1Ø (1) H
D4-5 ACTIVE 1Ø H
D4-5 ACTIVE 1Ø L

D4-2 RCV ENBL Ø9 (1) H
D4-3 CLR MATCH Ø9L
D4-3 RESYNC PULSE Ø9 L
D4-2 RCV ENBL Ø9 (1) H
D4-5 MATCH Ø9 (1) H
D4-5 ACTIVE Ø9 H
D4-5 ACTIVE Ø9 L

D4-2 RCV ENBL Ø8 (1) H
D4-3 CLR MATCH Ø8L
D4-3 RESYNC PULSE Ø8 L
D4-2 RCV ENBL Ø8 (1) H
D4-5 MATCH Ø8 (1) H
D4-5 ACTIVE Ø8 H
D4-5 ACTIVE Ø8 L

(RCV FILES, RCV DATA, MATCH LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ASYNCH MUX LINE CARD LINES Ø8-11 (04-5)			
SIZE	CODE	NUMBER	REV.	
D	BS	DV11-Ø-17	*	
SCALE		SHEET 5 OF 10	DIST.	

+3VA
+3VB
+5V
D4-1Ø DA 11 L
D4-6 RCV FLAG 11 H
D4-3 CLR RCV FLAG 11 L
D4-5 ACTIVE 11 H
D4-6 RESET DA 11 L
D4-1Ø DA 1Ø L
D4-6 RCV FLAG 1Ø H
D4-3 CLR RCV FLAG 1Ø L
D4-5 ACTIVE 1Ø H
D4-9 DA Ø9 L
D4-6 RCV FLAG Ø9 H
D4-3 CLR RCV FLAG Ø9 L
D4-5 ACTIVE Ø9 H
D4-8 DA Ø8 L
D4-6 RCV FLAG Ø8 H
D4-3 CLR RCV FLAG Ø8 L
D4-5 ACTIVE Ø8 H
D4-6 RDE 11 L
D4-6 RDE 1Ø L
D4-6 RDE Ø9 L
D4-6 RDE Ø8 L
D4-6 RESET DA 1Ø L
D4-6 RESET DA Ø9 L
D4-6 RESET DA Ø8 L
J1
DV11 BUSY 11
DV11 BUSY 1Ø
DV11 BUSY Ø9
DV11 BUSY Ø8
ASYN H
R31 1K
D4-6 ENBL ERROR FLAGS L
D4-6 RCV FILE ADDRS ØØ L
D4-6 RCV FILE ADDRS Ø1 L
R32 1ØK
R33 1ØK
R34 1ØK
C113 15ØPF
C115 15PF
C114 1ØPF
C117 18ØPF
RDE
RDE DLY
LOAD FILE
WAIT DLY
RESET DA
SAMPLE CLK
SAMPLE DELAY
D4-6 RECEIVER SAMPLE CLOCK H
D4-6 RCV FILE LOAD L
D4-2 RESET L
R27 1ØK
R28 1ØK
R30 1ØK
R26 33Ø
R27 47Ø
3ØNS DL1
(RECEIVER FLAG SERVICE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES Ø8-11 (D4-8)
SIZE D CODE RS NUMBER DV11-Ø-17 REV. *
SCALE — SHEET 6 OF 1Ø DIST.

D4-10 SERIAL OUT 11 H
D4-2 BREAK 11 (Ø) H
AH2
T4Ø8 E9
1488 E11
EIA RCV DATA 11
J1 Ee KK
EIA XMIT DATA 11
1489 E5
C1Ø6 47ØPF
D4-2 MAINT 11 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX 11 H
D4-1Ø EOC 11 L
(EF2)
T4Ø8 E19
7432 E3
D4-5 ACTIVE 11 L
7432 E22
BK1
D4-7 SERIAL IN 11 H

D4-10 SERIAL OUT 1Ø H
D4-2 BREAK 1Ø (Ø) H
AT2
T4Ø8 E9
1488 E11
EIA RCV DATA 1Ø
J1 CC HH
EIA XMIT DATA 1Ø
1489 E5
C1Ø5 47ØPF
D4-2 MAINT 1Ø H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX 1Ø H
D4-1Ø EOC 1Ø L
(EK2)
T4Ø8 E19
7432 E3
D4-5 ACTIVE 1Ø L
7432 E22
BK2
D4-7 SERIAL IN 1Ø H

D4-9 SERIAL OUT Ø9 H
D4-2 BREAK Ø9 (Ø) H
AB1
T4Ø8 E9
1488 E11
EIA RCV DATA Ø9
J1 T N
EIA XMIT DATA Ø9
1489 E5
C128 47ØPF
D4-2 MAINT Ø9 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX Ø9 H
D4-9 EOC Ø9 L
(ER2)
T4Ø8 E19
7432 E3
D4-5 ACTIVE Ø9 L
7432 E22
BD1
D4-7 SERIAL IN Ø9 H

D4-9 SERIAL OUT Ø8 H
D4-2 BREAK Ø8 (Ø) H
AJ2
T4Ø8 E9
1488 E11
EIA RCV DATA Ø8
J1 R L
EIA XMIT DATA Ø8
1489 E5
C129 47ØPF
D4-2 MAINT Ø8 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX Ø8 H
D4-9 EOC Ø8 L
(NJ2)
T4Ø8 E19
7432 E3
D4-5 ACTIVE Ø8 L
7432 E22
BF2
D4-7 SERIAL IN Ø8 H

(EIA IN & OUT. HALF DUPLEX, BREAK, MAINT LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø8-11 (D4-7)	D	BS	DV11-Ø-17	*

SCALE — SHEET 7 OF 1Ø

DBS DV11-Ø-17

NOTES:

1. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FEATURE AT 9600 BAUD OR LESS.

DATA SET BUSY 11 — J — 1489 E66 — C118 47ØPF — D4-2 MAINT 11 L — 74H11 E33 — R38 1K — D4-4 SPEED 1713 H — *W6 — +5V
D4-1Ø EOC 11 L (EF2) — D4-1Ø TBMT 11 L — 8815 E65
D4-2 RESET L — D4-3 TRAN FLAG CLK 11 L — 7474 ET4 — D4-8 TRAN FLAG 11 H — D4-8 TXRL 11 L — 74Ø8 E85 — +3VA

DATA SET BUSY 1Ø — F — 1489 E66 — C1Ø9 47ØPF — D4-2 MAINT 1Ø L — 74H11 E33 — R37 1K — D4-4 SPEED 1712 H — *W5 — +5V
D4-1Ø EOC 1Ø L (EK2) — D4-1Ø TBMT 1Ø L — 8815 E65
D4-3 TRAN FLAG CLK 1Ø L — 7474 ET4 — D4-8 TRAN FLAG 1Ø H — D4-8 TXRL 1Ø L — 74Ø8 E85 — +3VA

DATA SET BUSY Ø9 — D — 1489 E66 — C112 47ØPF — D4-2 MAINT Ø9 L — 74H11 E33 — R36 1K — D4-4 SPEED 1711 H — *W4 — +5V
D4-9 EOC Ø9 L (ER2) — D4-9 TBMT Ø9 L — 8815 E79
D4-3 TRAN FLAG CLK Ø9 L — 7474 E84 — D4-8 TRAN FLAG Ø9 H — D4-8 TXRL Ø9 L — 74Ø8 E85 — +3VA

DATA SET BUSY Ø8 — B — 1489 E66 — C11Ø 47ØPF — D4-2 MAINT Ø8 L — 74H11 E67 — R35 1K — D4-4 SPEED 1710 H — *W3 — +5V
D4-9 EOC Ø8 L (FJ2) — D4-9 TBMT Ø8 L — 8815 E79
D4-3 TRAN FLAG CLK Ø8 L — 7474 E84 — D4-8 TRAN FLAG Ø8 H — D4-8 TXRL Ø8 L — 74Ø8 E85 — +3VA

74175 EBB — D5 R3(1) R3(Ø) — D2 R2(1) R2(Ø) — D1 R1(1) R1(Ø) — DØ RØ(1) RØ(Ø) — CLR CLK
3318 EB7 — A0 A1 A2 — E0 G5 — E1
STB8 STBA — 74155 EB9 — DB DA — SØ S1 — 4B0 4B1 4B2 4B3 — 4A0 4A1 4A2 4A3

D4-2 RESET L — 74Ø8 E42 — +5V — RT 10K — R39 39Ø — 30NS DL2 — R4Ø 47Ø — C121 27PF — 74123 EG3 — 175 NS — +3V8
R42 10K — C12Ø 56PF — 74123 ET0 — 25Ø NS — +3VA
R43 10K — C122 15PF — 74123 ET0 — 125 NS

D3-4 TRAN DATA ØT H — EP1 — D3-4 TRAN DATA Ø6 H — EM2 — D3-4 TRAN DATA Ø5 H — FR2 — D3-4 TRAN DATA Ø4 H — FV2
D3-4 TRAN FILE LOAD L
D3-3 BUF MSCAN Ø1 L
D3-3 BUF MSCAN ØØ L
7417Ø ET8 — RD RA1 RAØ — D3 D2 D1 DØ — R3(1) R2(1) R1(1) RØ(1) — WR WA1 WAØ — D4-8 DB8 DB7 DB6 DB5
D3-4 TRAN DATA Ø3 H — FS2 — D3-4 TRAN DATA Ø2 H — FV1 — D3-4 TRAN DATA Ø1 H — FT2 — D3-4 TRAN DATA ØØ H — FU2
7417Ø ET7 — D4-8 DB4 DB3 DB2 DB1

(TRANSMIT FLAG SERVICING)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES Ø8-11 (04-Ø)	D	BS	DV11-Ø-17	*
SCALE	SHEET 8 OF 1Ø	DIST.		

DV11-Ø-17

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

T4Ø4 E8Ø — D4-9 DA Ø8 L

D4-7 SERIAL IN Ø8 H (BF2) 2Ø
D4-6 RESET DA Ø8 L 18
D4-6 RDE Ø8 L 4
16
17
D4-4 CLOCK Ø8 H (DE2) 9Ø

UART Ø8 ET6

SERIAL IN
CLR R DONE
STB RD
STB STATUS
R CLK
X CLK
LD XD
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XDØ
CLR NB1 NB2 PB NP EP LOC

R DONE 19
OR ERR 15 — D4-9 OR Ø8
FR ERR 14 — D4-9 FE Ø8
P ERR 13 — D4-9 PE Ø8
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 — AJ2 — D4-9 SERIAL OUT Ø8 H
XRDY 22 — T4Ø4 E73 — 1Ø — D4-9 TBMT Ø8 L
EOC 24 — T4Ø4 EBØ — 8 FJ2 — D4-9 EOC Ø8 L

D4-8 THRL Ø8 L 23
33
32
31
3Ø
29
28
27
26
21 38 37 36 35 39 34

T4Ø4 E8Ø — D4-9 DA Ø9L

D4-7 SERIAL IN Ø9 H (BD1) 2Ø
D4-6 RESET DA Ø9 L 18
D4-6 RDE Ø9 L 4
16
17
D4-4 CLOCK Ø9 H (CE2) 9Ø

UART Ø9 E81

SERIAL IN
CLR R DONE
STB RD
STB STATUS
R CLK
X CLK
LD XD
XD7
XD6
XD5
XD4
XD3
XD2
XD1
XDØ
CLR NB1 NB2 PB NP EP LOC

R DONE 19
OR ERR 15 — D4-9 OR Ø9
FR ERR 14 — D4-9 FE Ø9
P ERR 13 — D4-9 PE Ø9
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 1Ø
RD1 11
RDØ 12
SERIAL OUT 25 — AB1 — D4-9 SERIAL OUT Ø9 H
XRDY 22 — T4Ø4 E8Ø — 9Ø — D4-9 TBMT Ø9 L
EOC 24 — T4Ø9 EBØ — 13 — 12 ER2 — D4-9 EOC Ø9 L

D4-8 THRL Ø9 L 23
33
32
31
3Ø
29
28
27
26
21 38 37 36 35 39 34

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV Ø8 H
D4-2 UART STROBE Ø8 H
D4-2 PEV Ø9 H
D4-2 UART STROBE Ø9 H

(UARTS Ø8 & Ø9)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINES Ø8-11 (D4-9)
SIZE D | CODE 8S | NUMBER DVII-Ø-17 | REV. *
SCALE | SHEET 9 OF 1Ø | DIST.

DVII-Ø-17

D4-9 RDB
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-8 DR8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV 10 H
D4-2 UART STROBE 10 H
D4-2 PEV 11 H
D4-2 UART STROBE 11 H

UART 10 E67

D4-7 SERIAL IN 10 H (BX2) 20 — SERIAL IN
D4-6 RESET DA 10 L 18 — CLR R DONE
D4-6 RDE 10 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK 10 H (DS2) 40 — X CLK
D4-8 THRL 10 L 23 — LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XD0
CLR NR1 NB2 2SB NP EP LDC
21 38 37 36 35 39 34

R DONE 19 — 1 T404 E66 2 — D4-10 DA 10 L
OR ERR 15 — D4-10 OR 10
FR ERR 14 — D4-10 FE 10
P ERR 13 — D4-10 PE 10
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RD0 12
SERIAL OUT 25 — ATZ — D4-10 SERIAL OUT 10 H
XRDY 22 — 5 T404 E66 6 — D4-10 TBMT 10 L
EOC 24 — 9 T404 E66 8 EK2 — D4-10 EOC 10 L

UART 11 E62

D4-7 SERIAL IN 11 H (BK1) 20 — SERIAL IN
D4-6 RESET DA 11 L 18 — CLR R DONE
D4-6 RDE 11 L 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK 11 H (CP2) 40 — X CLK
D4-8 THRL 11 L 23 — LD XD
33 XD7
32 XD6
31 XD5
30 XD4
29 XD3
28 XD2
27 XD1
26 XD0
CLR NR1 NB2 2SB NP EP LDC
21 38 37 36 35 39 34

R DONE 19 — 3 T404 E66 4 — D4-10 DA 11 L
OR ERR 15 — D4-10 OR 11
FR ERR 14 — D4-10 FE 11
P ERR 13 — D4-10 PE 11
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RD0 12
SERIAL OUT 25 — AH2 — D4-10 SERIAL OUT 11 H
XRDY 22 — 11 T404 E66 10 — D4-10 TBMT 11 L
EOC 24 — 13 T404 E66 12 EF2 — D4-10 EOC 11 L

(UARTS 10 & 11)

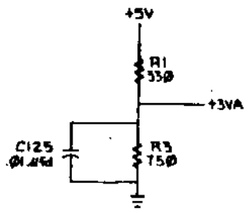
REVISIONS		
CHK	CHANGE NO.	REV.

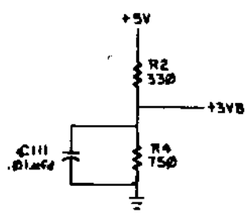
TITLE: ASYNCH MUX LINE CARD LINES Ø8-11 (04-10)
SIZE D CODE 8S NUMBER DV11-Ø-17 REV. *
SCALE — SHEET 10 OF 10 DIST.

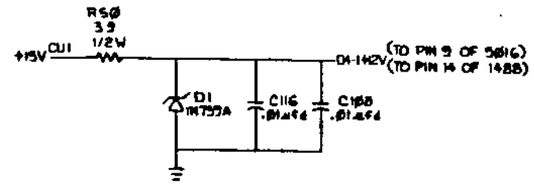
BERG CONNECTOR

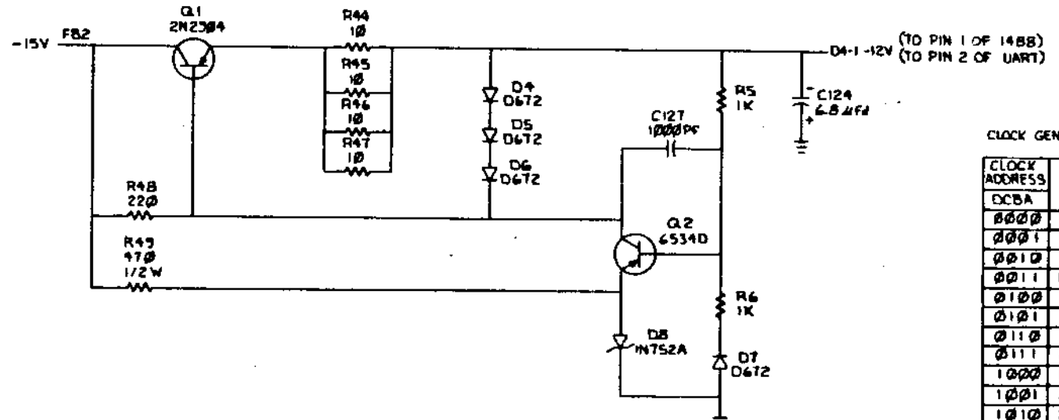
J1

DATA SET BUSY 12
DATA SET BUSY 13
DATA SET BUSY 14
ASYN H
DATA SET BUSY 15
EIA RCV DATA 12
EIA RCV DATA 13
EIA XMIT DATA 12
EIA XMIT DATA 13
DVII BUSY 12
DVII BUSY 13
DVII BUSY 14
DVII BUSY 15
EIA XMIT DATA 14
EIA XMIT DATA 15
EIA RCV DATA 14
EIA RCV DATA 15



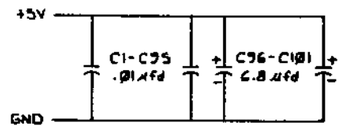






CLOCK GENERATION CHART

CLOCK ADDRESS OCBA	BAUD RATE	PERIOD (USEC)
ØØØØ	50	1250.00
ØØØ1	75	833.33
ØØ1Ø	110	568.18
ØØ11	134.5	464.68
Ø1ØØ	150	416.67
Ø1Ø1	300	208.33
Ø11Ø	600	104.17
Ø111	1200	52.08
1ØØØ	1800	34.72
1ØØ1	2000	31.25
1Ø1Ø	2400	26.04
1Ø11	3600	17.36
11ØØ	4800	13.02
11Ø1	7200	8.68
111Ø	9600	6.51
1111	38400	1.63



(CHART, REGULATORS)

DRN		
CHK		
ENG		
PROJ. ENG.		
PROD. E.		
NEXT HIGHER ASSY.		
B-DD-DVII-Ø		
SCALE		
SHEET	OF 1Ø	

FIRST USED ON: DVII

TITLE: ASYNCH MUX LINE CARD LINES 12-15 (D4-1)

SIZE	CODE	NUMBER	REV.
D	85	DVII-Ø-18	*

DIST.

REVISIONS		
REV.	CHANGE NO.	DATE

D 85 DVII-Ø-18

D3-7 INIT D1 L — EV2 13 — 7404 E7 — 12 — 12 — 7437 E40 — 11 — D4-2 RESET L
D4-2 RESET H — 13 — 7404 E47 — 12

+3VB

7474 E35 — 10 — 12 — 9 — D4-2 MAINT 15 H / D4-2 MAINT 15 L — 11 — C — 13
7474 E35 — 4 — 2 — 5 — D4-2 MAINT 14 H / D4-2 MAINT 14 L — 3 — C — 1
7474 E34 — 10 — 12 — 9 — D4-2 MAINT 13 H / D4-2 MAINT 13 L — 11 — C — 13
7474 E34 — 4 — 2 — 5 — D4-2 MAINT 12 H / D4-2 MAINT 12 L — 3 — C — 1

7404 E47 — 11 — 10
7404 E47 — 9 — 8
7404 E47 — 1 — 2
7404 E47 — 3 — 4 — D4-2 BRG STROBE 15 H
7404 E47 — 5 — 6 — D4-2 BRG STROBE 14 H
7404 E58 — 13 — 12 — D4-2 BRG STROBE 13 H
7404 E58 — 11 — 10 — D4-2 BRG STROBE 12 H
7404 E58 — 9 — 8 — D4-2 UART STROBE 15 H
7404 E58 — 1 — 2 — D4-2 UART STROBE 14 H
7404 E58 — 3 — 4 — D4-2 UART STROBE 13 H
7404 E58 — 5 — 6 — D4-2 UART STROBE 12 H
7404 E53 — 13 — 12
7404 E53 — 11 — 10
7404 E53 — 9 — 8
7404 E53 — 1 — 2

74154 E52 — Ø15 17, Ø14 16, Ø13 15, Ø12 14, Ø11 13, Ø10 11, Ø9 10, Ø8 9, Ø7 8, Ø6 7, Ø5 6, Ø4 5, Ø3 4, Ø2 3, Ø1 2, Ø0 1

D2-3 LCR 10 — DT2 — 20 — D3
D2-3 LCR 09 — AP2 — 21 — D2
D3-8 SRS 01 — BT2 — 22 — D1
D3-8 SRS 00 — BM2 — 23 — D0
+5V
R41 10K
C119 100 PF
STB1 18, STB0 19

D2-3 CONTROL STROBE H — CS2 — 10 — 9
D3-8 SRS 03 H — RS2 — 2
D3-8 SRS 02 H — BR2 — 1
7402 E68 — 3
74123 E57 — 6, 7, 5, 12, 4, 13, 11
+3VA
D12 — D4-2 CARD PARAMETER SELECT 12-15 L

D4-2 PEN L
D2-3 LCR 14 H — AL2 — 11 — 7404 E7 — 10 — 13, 12 — 7437 E12 — 11 — D4-2 BUF LCR 14 H
D2-3 LCR 13 H — BA1 — 9 — 7404 E7 — 8 — 9, 10 — 7437 E12 — 8 — D4-2 BUF LCR 13 H
D2-3 LCR 12 H — AM2 — 1 — 7404 E7 — 2 — 5, 4 — 7437 E12 — 6 — D4-2 BUF LCR 12 H
D2-3 LCR 11 H — AN2 — 3 — 7404 E7 — 4 — 1, 2 — 7437 E12 — 3 — D4-2 BUF LCR 11 H

74175 E24 — D3 R3(1) 15, R3(0) 14 — D4-2 BREAK 15 (0) H
D2 R2(1) 10, R2(0) 11 — D4-2 RCV ENBL 15 (1) H
D1 R1(1) 7, R1(0) 6 — D4-2 PEV 15 H
D0 R0(1) 2, R0(0) 3 — D4-2 HALF DUPLEX 15 H
CLR 1, CLK 9

74175 E13 — D4-2 BREAK 14 (0) H / D4-2 RCV ENBL 14 (1) H / D4-2 PEV 14 H / D4-2 HALF DUPLEX 14 H
74175 E8 — D4-2 BREAK 13 (0) H / D4-2 RCV ENBL 13 (1) H / D4-2 PEV 13 H / D4-2 HALF DUPLEX 13 H
74175 E14 — D4-2 BREAK 12 (0) H / D4-2 RCV ENBL 12 (1) H / D4-2 PEV 12 H / D4-2 HALF DUPLEX 12 H

(CARD SELECTION, REGISTERS, STROBES, INIT)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ASYNCH MUX LINE CARD LINES 12-15 (04-2)
SIZE: D | CODE: BS | NUMBER: DV11-0-18 | REV: *
SCALE | SHEET 2 OF 10 | DIST.

D3-4 MASTER SCAN Ø3 H
D3-4 MASTER SCAN Ø2 H
EU2
EN2
7400 E68
DM2
D4-3 CARD FLAG SELECT 12-15 L
7404 E73
D3-3 RESYNC PULSE L
DF2
74155 E60
STB0 STBA
DB
DA
S1 S0
GB0 D4-3 RESYNC PULSE 15 L
GB1 D4-3 RESYNC PULSE 14 L
GB2 D4-3 RESYNC PULSE 13 L
GB3 D4-3 RESYNC PULSE 12 L
GA0 D4-3 TRAN FLAG CLK 15 L
GA1 D4-3 TRAN FLAG CLK 14 L
GA2 D4-3 TRAN FLAG CLK 13 L
GA3 D4-3 TRAN FLAG CLK 12 L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
D3-4 TRANSMITTER STROBE H
EH2
7400 E68
7404 E53
D4-3 TRAN FILE LOAD L
D4-6 RCV FLAG 15 H
D4-6 RCV FLAG 14 H
D4-6 RCV FLAG 13 H
D4-6 RCV FLAG 12 H
D4-5 MATCH 15 (1) H
D4-5 MATCH 14 (1) H
D4-5 MATCH 13 (1) H
D4-5 MATCH 12 (1) H
STB0 STB1
A1 B1 C1 D1
A0 B0 C0 D0
S1 S0
74153 E37
7432 E72
8881 E82
FM2 RECEIVER FLAG L
FE1 MATCH DETECT L
+5V
R8 10K
D1-5 RECEIVED DATA ENABLE H
CN2
7400 E68
FU1 D4-3 RDE 12-15
74123 E63
+3VB
FK1 D4-3 DATA ENABLE 12-15 H
D4-3 MATCH H
7474 E36
7437 E40
D4-2 RESET L
STB3 STBA
GB0 D4-3 CLR RCV FLAG 15 L
GB1 D4-3 CLR RCV FLAG 14 L
GB2 D4-3 CLR RCV FLAG 13 L
GB3 D4-3 CLR RCV FLAG 12 L
GA0 D4-3 CLR MATCH 15 L
GA1 D4-3 CLR MATCH 14 L
GA2 D4-3 CLR MATCH 13 L
GA3 D4-3 CLR MATCH 12 L
74155 E31
D3-4 MASTER SCAN Ø1 H
EM1
D3-4 MASTER SCAN ØØ H
EN1
D4-8 TRAN FLAG 15 H
D4-8 TRAN FLAG 14 H
D4-8 TRAN FLAG 13 H
D4-8 TRAN FLAG 12 H
STB1 STB0
74153 E83
8881 E82
FL2 TRAN FLAG WAITING L
D3-4 MASTER SCAN T/R
CR2
(SCAN SELECTION, FLAGS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ASYNCH MUX LINE CARD LINES 12-15 (D4-3)
SIZE D | CODE BS | NUMBER DV11-Ø-18 | REV. *
SCALE — | SHEET 3 OF 10 | DIST.

DIGITAL DBS DV11-Ø-18

R9 10K
R10 10K
C126 22PF
C123 22PF
7380 E93
7380 E95
Y1 2.457G MHZ
C208 22PF
R11 1K
7404 E80
W2 (W2 REMOVED FOR AUTOMATED MODULE TEST)
D4-2 RESET H
7493 E92
R3(1) R2(1) R1(1) R0(1) CLR CLK0 CLK8C
BN2 D4-4 SOURCE CLOCK B 12-15 L
D4-2 BUF LCR 14 H
D4-2 BUF LCR 13 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 11 H
COM 5016 E51
TD TC TB TA STT EXT2 EXT1 RD RC RB RA STR ST SR
D4-1 +12V
5MHZ E27 +5V
W1 (W1 REMOVED FOR AUTOMATED MODULE TEST)
BJ1 D4-4 SOURCE CLOCK A 12-15 L
7437 E46
7437 E46
COM 5016 E57
D4-1 +12V
+3VA
7474 E45
7474 E45
7474 E55
7474 E55
7420 E39
D4-2 BRG STROBE 15 H
D4-2 BRG STROBE 14 H
D4-2 BRG STROBE 13 H
D4-2 BRG STROBE 12 H
D4-2 RESET L
D4-4 SPEED 1717 H
D4-4 SPEED 1716 H
D4-4 SPEED 1715 H
D4-4 SPEED 1714 H
8094 E56
8093 E50
CP2 D4-4 CLOCK 15 H
DS2 D4-4 CLOCK 14 H
CE2 D4-4 CLOCK 13 H
DE2 D4-4 CLOCK 12 H

REVISIONS		
CHG	CHANGE NO.	REV.

(CRYSTAL. CLOCK GENERATION)

TITLE	SIZE	CODE	NUMBER	REV.
ASYNCH MUX LINE CARD LINES 12 - 15 (D4-4)	D	BS	DV11-Ø-18	*
SCALE	SHEET 4 OF 10	DIST.		

D4-6 ENBL ERROR FLAGS L

D4-10 OR 15
D4-10 OR 14
D4-9 OR 13
D4-9 OR 12
D4-10 PE 15
D4-10 PE 14
D4-9 PE 13
D4-9 PE 12

D4-10 FE 15
D4-10 FE 14
D4-9 FE 13
D4-9 FE 12

74153 E71
74153 E75
74H11 E69
7404 E53
T915T E64

+3VB

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

T9170 E95
T9170 E94

D4-3 BUF MSCAN Ø0 L
D4-3 BUF MSCAN Ø1 L
D4-3 CARD FLAG SELECT 12-15 L

D4-6 RCV FILE LOAD L
D4-6 RCV FILE ADDRS Ø1 L
D4-6 RCV FILE ADDRS Ø0 L
D4-3 DATA ENABLE 12-15 H

8881 E86 — FL1 — MASTER OR L
8881 E86 — FM1 — MASTER PE L
8881 E86 — FH1 — RECV DATA Ø7 L
8881 E86 — FJ1 — RECV DATA Ø6 L
8881 E9Ø — FR1 — RECV DATA Ø5 L
8881 E9Ø — FS1 — RECV DATA Ø4 L
8881 E9Ø — FN1 — RECV DATA Ø3 L
8881 E9Ø — FP1 — RECV DATA Ø2 L
8881 E91 — FN2 — RECV DATA Ø1 L
8881 E91 — FP2 — RECV DATA Ø0 L

R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 — 1K / 10K — +5V

C1Ø2 27 PF
C1Ø3 27 PF
C1Ø4 27 PF
C1Ø7 27 PF

D4-2 RCV ENBL 15 (1) H
D4-2 RCV ENBL 14 (1) H
D4-2 RCV ENBL 13 (1) H
D4-2 RCV ENBL 12 (1) H

74123 E2
74123 E10
74123 E15
74174 E23
74174 E25
74174 E15

D4-3 CLR MATCH 15 L
D4-3 CLR MATCH 14 L
D4-3 CLR MATCH 13 L
D4-3 CLR MATCH 12 L

D4-3 RESYNC PULSE 15 L
D4-3 RESYNC PULSE 14 L
D4-3 RESYNC PULSE 13 L
D4-3 RESYNC PULSE 12 L

7408 E3Ø
7408 E2Ø

D4-5 MATCH 15 (1) H
D4-5 MATCH 14 (1) H
D4-5 MATCH 13 (1) H
D4-5 MATCH 12 (1) H

D4-5 ACTIVE 15 H
D4-5 ACTIVE 15 L
D4-5 ACTIVE 14 H
D4-5 ACTIVE 14 L
D4-5 ACTIVE 13 H
D4-5 ACTIVE 13 L
D4-5 ACTIVE 12 H
D4-5 ACTIVE 12 L

(RCV FILES, RCV DATA, MATCH LOGIC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	ASYNCH MUX LINE CARD LINES 12-15 (D4-5)	SIZE/CODE	NUMBER / REV.
		D	BS DV11-Ø-18 *
SCALE	SHEET 5 OF 10	DIST.	

+3VA
+3VB
+5V
D4-1Ø DA 15 L
D4-6 RCV FLAG 15 H
D4-3 CLR RCV FLAG 15 L
D4-5 ACTIVE 15 H
D4-6 RESET DA 15 L
D4-6 RESET DA 14 L
D4-6 RESET DA 13 L
D4-6 RESET DA 12 L
D4-1Ø DA 14 L
D4-6 RCV FLAG 14 H
D4-3 CLR RCV FLAG 14 L
D4-5 ACTIVE 14 H
D4-9 DA 13 L
D4-6 RCV FLAG 13 H
D4-3 CLR RCV FLAG 13 L
D4-5 ACTIVE 13 H
D4-9 DA 12 L
D4-6 RCV FLAG 12 H
D4-3 CLR RCV FLAG 12 L
D4-5 ACTIVE 12 H
D4-6 RDE 15 L
D4-6 RDE 14 L
D4-6 RDE 13 L
D4-6 RDE 12 L
DV11 BUSY 15
DV11 BUSY 14
DV11 BUSY 13
DV11 BUSY 12
ASYN H
R31 1K
D4-6 ENBL ERROR FLAGS L
D4-6 RCV FILE ADDRS ØØ L
D4-6 RCV FILE ADDRS Ø1 L
R32 1ØK
R33 1ØK
R34 1ØK
C113 15ØPF
C117 15ØPF
RDE
RDE DLY
LOAD FILE
D4-6 RCV FILE LOAD L
RESET DA
R29 1ØK
C115 15PF
WAIT DLY
R26 33Ø
3Ø NS
DL1
R27 47Ø
C114 1ØPF
R28 1ØK
R3Ø 1ØK
SAMPLE CLK
SAMPLE DELAY
D4-6 RECEIVER SAMPLE CLOCK H
D4-2 RESET L
(RECEIVER FLAG SERVICE)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES 12-15 (D4-6)
SIZE D | CODE BS | NUMBER DVII-Ø-18 | REV. *
SCALE | SHEET 6 OF 1Ø | DIST.

D4-10 SERIAL OUT 15 H
D4-2 BREAK 15 (Ø) H
AH2
T4Ø8 E9
1488 E11
J1 EE
EIA XMIT DATA 15
EIA RCV DATA 15
J1 KK
1489 E5
C1Ø6 47ØPf
D4-2 MAINT 15 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX 15 H
D4-1Ø EOC 15 L
(EF2)
T4Ø8 E13
7432 E3
7432 E22
D4-5 ACTIVE 15 L
BK1
D4-7 SERIAL IN 15 H

D4-10 SERIAL OUT 14 H
D4-2 BREAK 14 (Ø) H
AT2
T4Ø8 E9
1488 E11
J1 CC
EIA XMIT DATA 14
EIA RCV DATA 14
J1 HH
1489 E5
C1Ø5 47ØPf
D4-2 MAINT 14 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX 14 H
D4-1Ø EOC 14 L
(EK2)
T4Ø8 E19
7432 E3
7432 E22
D4-5 ACTIVE 14 L
BK2
D4-7 SERIAL IN 14 H

D4-9 SERIAL OUT 13 H
D4-2 BREAK 13 (Ø) H
AB1
T4Ø8 E9
1488 E11
J1 T
EIA XMIT DATA 13
EIA RCV DATA 13
J1 N
1489 E5
C128 47ØPf
D4-2 MAINT 13 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX 13 H
D4-9 EOC 13 L
(ER2)
T4Ø8 E19
7432 E3
7432 E22
D4-5 ACTIVE 13 L
BD1
D4-7 SERIAL IN 13 H

D4-9 SERIAL OUT 12 H
D4-2 BREAK 12 (Ø) H
AJ2
T4Ø8 E9
1488 E11
J1 R
EIA XMIT DATA 12
EIA RCV DATA 12
J1 L
1489 E5
C129 47ØPf
D4-2 MAINT 12 H
8Ø94 E17
8Ø93 E18
D4-2 HALF DUPLEX 12 H
D4-9 EOC 12 L
(KJ2)
T4Ø8 E19
7432 E3
7432 E22
D4-5 ACTIVE 12 L
BF2
D4-7 SERIAL IN 12 H

(EIA IN & OUT. HALF DUPLEX, BREAK, MAINT LOGIC)

REVISIONS		
ECR	CHANGE NO.	REV.

TITLE ASYNCH MUX LINE CARD LINES 12-15 (D4-7)	SIZE D	CODE BS	NUMBER DV11-Ø-18	REV. *
SCALE —/—	SHEET 1 OF 1Ø		CUST.	

DBS DV11-Ø-18

NOTES:
1. * JUMPER MUST BE REMOVED TO IMPLEMENT DATA SET BUSY FEATURE AT 9600 BAUD OR LESS.

DATA SET BUSY 15 — J1 L — 1489 E6 — C118 470 PF — D4-4 SPEED 1717 H — * W6 — R38 1K — +5V
D4-2 MAINT 15 L — T4H11 E33
D4-1Ø EOC 15 L (EF2) — 8815 E65
D4-1Ø TBMT 15 L

DATA SET BUSY 14 — F — 1489 E6 — C1Ø9 470 PF — D4-4 SPEED 1716 H — * W5 — R37 1K — +5V
D4-2 MAINT 14 L — T4H11 E33
D4-1Ø EOC 14 L (EK2) — 8815 E65
D4-1Ø TBMT 14 L

DATA SET BUSY 13 — D — 1489 E6 — C112 470 PF — D4-4 SPEED 1715 H — * W4 — R36 1K — +5V
D4-2 MAINT 13 L — T4H11 E33
D4-9 EOC 13 L (ER2) — 8815 E79
D4-9 TBMT 13 L

DATA SET BUSY 12 — B — 1489 E6 — C11Ø 470 PF — D4-4 SPEED 1714 H — * W3 — R35 1K — +5V
D4-2 MAINT 12 L — T4H11 E69
D4-9 EOC 12 L (FJ2) — 8815 E79
D4-9 TBMT 12 L

D4-2 RESET L — T74Ø8 E42 — R39 39Ø — +5V — 3ØNS DL2 — R4Ø 47Ø — C121 27PF — 175 NS — 74123 EG3 — +5VB
T9175 E88 (D3 R3(1) R3(Ø); D2 R2(1) R2(Ø); D1 R1(1) R1(Ø); DØ RØ(1) RØ(Ø); CLR CLK)
3318 E87 (A2 A1 AØ; EO G5; E1)
+3VA
ST88 ST8A (DB; FBØ FB1 FB2 FB3; T4155 E89; DA; FAØ FA1 FA2 FA3; SØ S1)
+5V — R7 1ØK — C12Ø 56PF — 25Ø NS — 74123 ET1Ø
+5V — R42 1ØK — C122 15PF — 125 NS — 74123 ET7Ø
+5V — R43 1ØK

D4-2 RESET L
D4-8 THRL 15 L — +3VA — T74 ET4 — D4-3 TRAN FLAG CLK 15 L — T4Ø8 E85 — D4-8 TRAN FLAG 15 H
D4-8 THRL 14 L — +3VA — T74 ET9 — D4-3 TRAN FLAG CLK 14 L — T4Ø8 E85 — D4-8 TRAN FLAG 14 H
D4-8 THRL 13 L — +3VA — T74 E84 — D4-3 TRAN FLAG CLK 13 L — T4Ø8 E85 — D4-8 TRAN FLAG 13 H
D4-8 THRL 12 L — +3VA — T74 E84 — D4-3 TRAN FLAG CLK 12 L — T4Ø8 E85 — D4-8 TRAN FLAG 12 H

T7170 ET8 (RD RA1 RAØ; D3 D2 D1 DØ; R3(1) R2(1) R1(1) R0(1); WR WA1 WAØ)
D3-4 TRAN DATA Ø7 H — EP1 — D4-8 DB5
D3-4 TRAN DATA Ø6 H — EM2 — D4-8 DB7
D3-4 TRAN DATA Ø5 H — FR2 — D4-8 DB6
D3-4 TRAN DATA Ø4 H — FY2 — D4-8 DB5
D4-3 TRAN FILE LOAD L
D4-3 BUF MSCAN Ø1 L
D4-3 BUF MSCAN ØØ L
T7170 ET7 (RD RA1 RAØ; D3 D2 D1 DØ; R3(1) R2(1) R1(1) R0(1); WR WA1 WAØ)
D3-4 TRAN DATA Ø3 H — FS2 — D4-8 DB4
D3-4 TRAN DATA Ø2 H — FV1 — D4-8 DB3
D3-4 TRAN DATA Ø1 H — FT2 — D4-8 DB2
D3-4 TRAN DATA ØØ H — FU2 — D4-8 DB1

(TRANSMIT FLAG SERVICING)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ASYNCH MUX LINE CARD LINES 12-15(04-8)
SIZE D | CODE 8S | NUMBER DV11-Ø-18 | REV. *
SCALE | SHEET 8 OF 1Ø | DIST.

D4-9 RD8
D4-9 RD7
D4-9 RD6
D4-9 RD5
D4-9 RD4
D4-9 RD3
D4-9 RD2
D4-9 RD1

D4-7 SERIAL IN 12 H — BF2 20 — SERIAL IN
D4-6 RESET DA 12 L — 18 — CLR R DONE
D4-6 RDE 12 L — 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-4 CLOCK 12 H — (DE2) 40 — X CLK

UART 12
ET6

D4-8 THRL 12 L — 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
30 — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ

CLR NB1 NB2 2SB NP EP LDC
21 38 37 36 35 33 34

R DONE 19 — 1 T4Ø4 E8Ø 2 — D4-9 DA 12 L
OR ERR 15 — D4-9 OR 12
FR ERR 14 — D4-9 FE 12
P ERR 13 — D4-9 PE 12
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12

SERIAL OUT 25 — AJ2 — D4-9 SERIAL OUT 12 H
XRDY 22 — 11 T4Ø4 ET3 10 — D4-9 TBMT 12 L
EOC 29 — 9 T4Ø4 E8Ø 8 — FJ2 — D4-9 EOC 12 L

D4-7 SERIAL IN 13 H — (BD1) 20 — SERIAL IN
D4-6 RESET DA 13 L — 18 — CLR R DONE
D4-6 RDE 13 L — 4 — STB RD
16 — STB STATUS
17 — R CLK
D4-9 CLOCK 13 H — (CE2) 40 — X CLK

UART 13
E81

D4-8 THRL 13 L — 23 — LD XD
33 — XD7
32 — XD6
31 — XD5
30 — XD4
29 — XD3
28 — XD2
27 — XD1
26 — XDØ

CLR NB1 NB2 2SB NP EP LDC
21 38 37 36 35 33 34

R DONE 19 — 3 T4Ø4 E8Ø 4 — D4-9 DA 13 L
OR ERR 15 — D4-9 OR 13
FR ERR 14 — D4-9 FE 13
P ERR 13 — D4-9 PE 13
RD7 5
RD6 6
RD5 7
RD4 8
RD3 9
RD2 10
RD1 11
RDØ 12

SERIAL OUT 25 — AB1 — D4-9 SERIAL OUT 13 H
XRDY 22 — 11 T4Ø4 E8Ø 10 — D4-9 TBMT 13 L
EOC 24 — 13 T4Ø4 E8Ø 12 — ER2 — D4-9 EOC 13 L

D4-8 DB8
D4-8 DB7
D4-8 DB6
D4-8 DB5
D4-8 DB4
D4-8 DB3
D4-8 DB2
D4-8 DB1

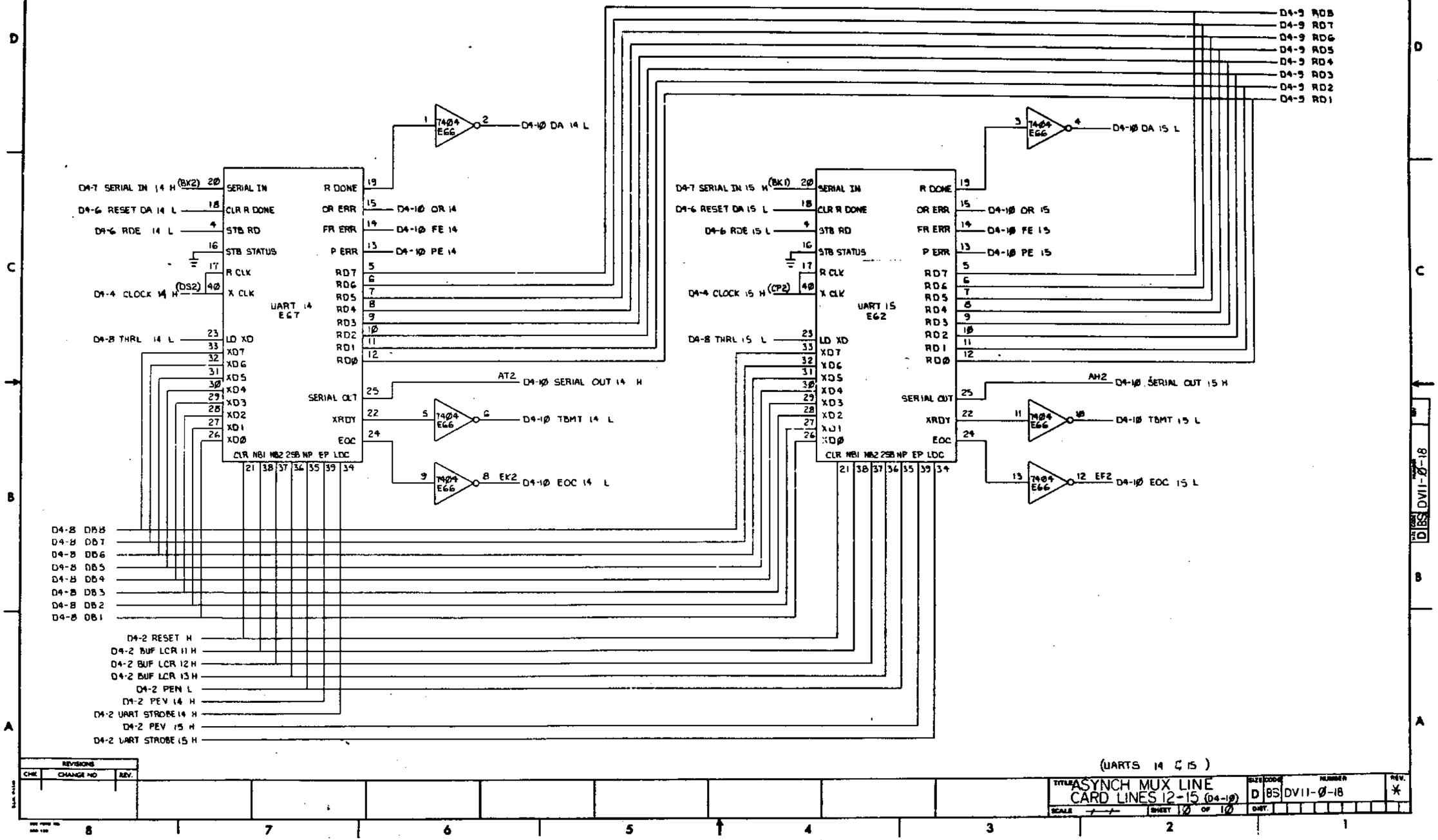
D4-2 RESET H
D4-2 BUF LCR 11 H
D4-2 BUF LCR 12 H
D4-2 BUF LCR 13 H
D4-2 PEN L
D4-2 PEV 12 H
D4-2 UART STROBE 12 H
D4-2 PEV 13 H
D4-2 UART STROBE 13 H

(UARTS 12 & 13)

REVISIONS
CHK | CHANGE NO. | REV.

TITLE ASYNCH MUX LINE CARD LINES 12-15 (D4-9)
SIZE D | CODE BS | NUMBER DV11-Ø-18 | REV. *
SCALE | SHEET 9 OF 10 | DIST

DEC DWG DBS DV11-Ø-18

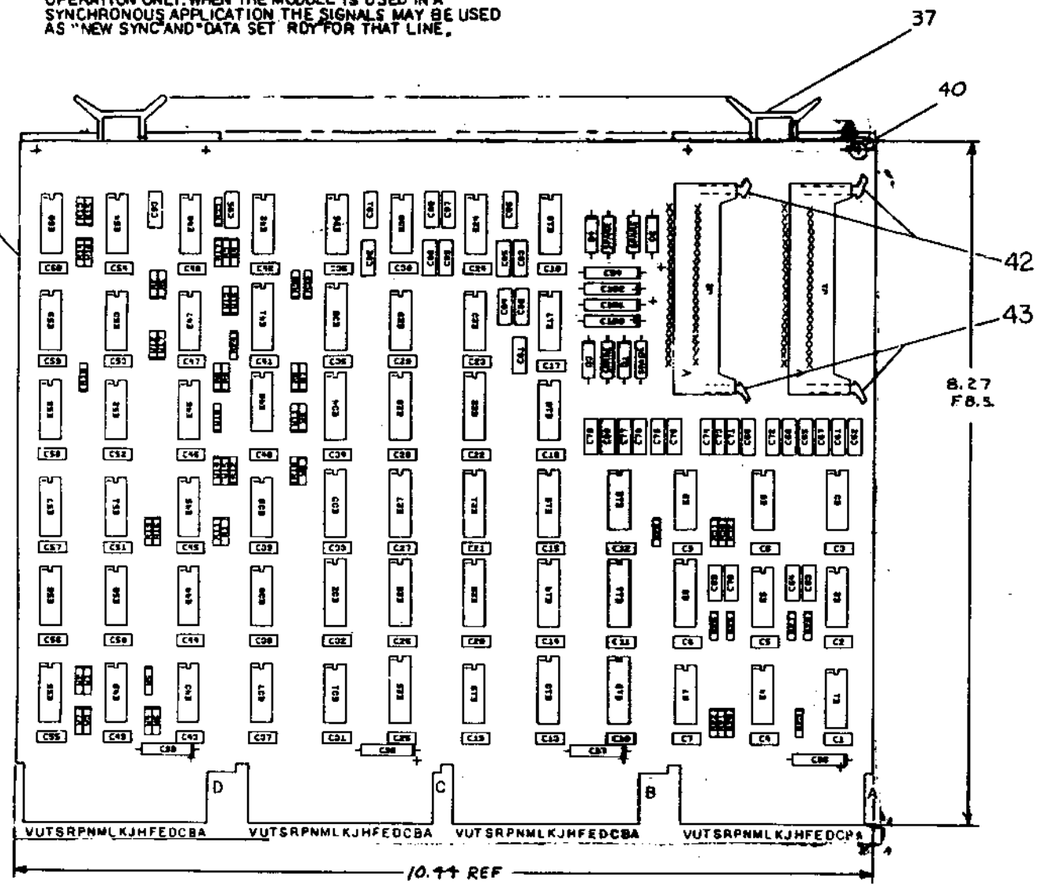


REVISIONS		
CHK	CHANGE NO	REV.

TITLE: ASYNCH MUX LINE CARD LINES 12-15 (D4-1Ø)
SIZE D | CODE 85 | NUMBER DV11-Ø-18 | REV. *
SCALE — | SHEET 1Ø OF 1Ø | DWG.

NOTES:

1. ALL UNUSED PINS ON J1, J2 GO TO GND
2. THE SIGNALS 'SEC TX' AND 'SEC RX' REFER TO ASYNCHRONOUS OPERATION ONLY. WHEN THE MODULE IS USED IN A SYNCHRONOUS APPLICATION THE SIGNALS MAY BE USED AS "NEW SYNC" AND "DATA SET RDY" FOR THAT LINE.



JUMPER TABLE		
JUMPER	BIT	
W1	D00	JUMPER REMOVED INTERRUPT VECTOR = 0
W2	D02	
W3	D03	
W4	D06	
W5	D07	
W6	D05	
W7	D04	
W8	A12	JUMPER REMOVED DEVICE SELECT = 1
W9	A09	
W10	A08	
W11	A10	
W12	A04	
W13	A05	
W14	A11	
W15	A03	
W16	A06	
W17	A07	

DEC 8640	1	8
DEC IC 7442	8	16
DEC IC 74175	8	16
DEC IC 74151	8	16
IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

+5V

A A2, B A2, C A2, D A2 — C1 – C68 .01 μF; C96 – C99 6.8 μF

A C 2, A T1; B C 2, B T1
C C 2, C T1; D C 2, D T1

REF			
		X-Y COORDINATE HOLE LOCATION	E-CO-M7907-0-4
REF		ASSY/DRILLING HOLE LAYOUT	D-MA-M7907-0-5
REF		MODULE ECO HISTORY	D-MA-M7907-0-6
1		ETCHED CIRCUIT BOARD	8019863
6	C84, C86—C102	CAP 6.8 UF 35V 10%	1005306
80	C1-C80	CAP .01 UF 100V 20%	1001810-04
33	C81—C93	CAP 470 UUF 100V 5%	1000824
1	C99	CAP 330 PF 100V 5%	1000823
4	D1,D2 D3, D4	DIODE 1N4733A	1109245
16	R1-R13, R15, R17, R18,	RES 1K 1/4W 5%	1300365
1	R14	RES 100 1/4W 5%	1300220
1	R33	RES 47 1/4W 5%	1300202
1	R16	RES 100 1/4W 5%	1301322
5	R26-R23, R39	RES 750 1/4W 5%	1301481
8	R25-R32	RES 33K 1/4W 10%	1300510
1	R19	RES 390 1/4W 5%	1300369
[illegible]	[illegible]	[illegible]	[illegible]
1	E52	I.C. DEC 7400	1910130
1	E6	I.C. DEC 7417	1909929
8	E16, E18, E23, E25, E36, E42	I.C. DEC 1408L	1910322
8	E3,5,8,8,12,17,24,38	I.C. DEC 1409L	1910323
8	E8,11,14,15,20,21,22,26	I.C. DEC 74151	1909936
6	E10,13,25,28,32,33,34,35	I.C. DEC 74175	1910831
1	E19	I.C. DEC 7419	1909576
1	E27	I.C. DEC 7442	1910840
6	E6,E7,E40,E51,E55,E60	I.C. DEC 8881	1909795
2	E58, E59	I.C. DEC 7400	1909575
7	E31,E37, E43,E45, E46 E53, E54	I C DEC 8646	1911469
1	E50	I.C. DEC 7474	1909847
1	E2	I.C. DEC 74H04	1909831
1	E44	I.C. DEC 74H00	1909858
3	E39, E40, E47	I.C. DEC 8242	1909712
1	E41	I.C. DEC 74123	1910438
1	E48	I.C. DEC 74H74	1909887
1	E35	I.C. DEC 8815	1909713
2	E50 E57	I.C. DEC 7402	1909004
4		HANDLE FLIP CHIP	9000337-6
2	J1,J2	40 PIN HEADER	1209941
18	W1-W18	JUMPER (INSULATED)	9000499
8		EYELET HANDLE	9006732
1	R38	RES 33Ω 1/4W 5%	1300295
2		LEFT LATCH	1209941-03
2		RIGHT LATCH	1209941-04
1	R24	RES. 10K, 1/4W, 5%	1300479

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

ETCH BOARD REV D

FIRST USED ON OPTION MODEL

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REV	DWG CHANGE NO.	ORIGINATED	REVISIONS
H	M7807-00004	J.C. HARRINGTON 11 JAN 78	
F	M7807-00003	J.M. NAMARA 6-4-76	
E	M7807-00002	J. McINTYRE 4-30-76	
D	M7807-00001	W. RUNDLOCK 2-3-75	

DRN J. Harrington 12/4/78
DSGN J. Harrington 11/4/78
ENGR J. McIntyre 4-30-76
MFG J. McIntyre 5-10-76
QA J. McIntyre 5-10-76
NEXT HIGHER ASSY
SCALE —/—
SHEET 1 OF 7

digital EQUIPMENT CORPORATION

TITLE BUS CONTROL & MUX

DCS M7807-0-1 H

BUS MSYN L — CE1 — 8640 E37
BUS AI7 L — CD1 — 8640 E37
BUS AI6 L — CE2 — 8640 E37
BUS AI5 L — CD2 — 8640 E37
BUS AI4 L — CK1 — 8640 E37
BUS AI3 L — CK2 — 8640 E37
BUS AI2 L — CC1 — 8640 E37
BUS AI1 L — CL1 — 8640 E45
BUS AI0 L — CP1 — 8640 E45
BUS AØ9 L — CR1 — 8640 E45
BUS AØ8 L — CN2 — 8640 E45
BUS AØ7 L — CP2 — 8640 E46
BUS AØ6 L — CU1 — 8640 E46
BUS AØ5 L — CV1 — 8640 E46
BUS AØ4 L — CU2 — 8640 E46
BUS AØ3 L — CV2 — 8640 E43
BUS AØ2 L — CF1 — 8640 E43
BUS AØ1 L — CH1 — 8640 E43
BUS AØØ L — CH2 — 8640 E31
BUS C1 L — CF2 — 8640 E43
BUS CØ L — CJ2 — 8640 E31

R11 1K
R12 1K
R16 1K
R9 1K
R8 1K
R7 1K
R6 1K
R5 1K
R4 1K
R3 1K
R2 1K
R1 1K
+5V

W8 — 8242 E39
W14 — 8242 E40
W11 — 8242 E40
W9 — 8242 E40
W10 — 8242 E40
W17 — 8242 E47
W16 — 8242 E47
W13 — 8242 E47
W12 — 8242 E47
W15 — 8242 E39
EXT GND CAN

R13 1K
R14 100
C93 .330 MFD
74H00 E44 — 8881 E50 — 8881 E62
EXT CAN CAI
CJ2 BUS SSYN Ø L
CL2 DI TEST POINT

8815 E38 — CS2 DI SELECT Ø N
8815 E38 — CT2 DI SELECT 2 N

74H00 E44
CM1 DI IN HIGH H
7402 E58 — CN1 DI OUT LOW H

REVISIONS		
CHK	CHANGE NO	REV

TITLE	BUS CONTROL & MUX (D1)	SIZE	CODE	NUMBER / REV.
		D	CS	M7807-0-1 H
SCALE 1/1	SHEET 2 OF 7	DIST.		

M7807-0-1 D CS H

D7 INT A H DK2
D7 INT ENB A H DH2
D2 INTR DONE B H DS1
BUS NPR L DJ1
BUS B BG IN H DE1
BUS BSY L DD1
BUS SSYN L DC1
D2 MASTER B L DS2
D2 MASTER B L DR2 DP2
DP1 BUS B BR L
DA1 BUS B BG OUT H
DT2 BUS SACK L
D7 INT A H DD2
DM2 DEZ BUS DØ2 L
DM3 DL1 BUS DØ3 L
DM7 DM2 BUS DØ4 L
DM6 DF1 BUS DØ5 L
DM1 BUS INTR L
DM4 DF2 BUS DØ6 L
DM5 DM1 BUS DØ7 L
DM1 DK1 BUS DØ8 L
DM2 INTR DONE B H

REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (02)	D	CS	M7807-0-1	H
SCALE —/— SHEET 3 OF 7	DIST.			

D7 SELECT 2 H
+5V
R24 10K
+3V
R39 750Ω
R38 330Ω
+5V
74LS10 E41
D7 OUT LAN H
D7 GROUP 8-15 H
74H10 E19
(INTR STATUS H)
D5 MUX LINE EN H
D8 CLEAR CYCLE L
D7 GROUP 8-15 H
BS1
AU1
7410 E19
74H04 E2
D5 EN MUX H
74151 C8 RING SELECTOR
D6 RING 8 L
D6 RING 9 L
D6 RING 10 L
D6 RING 11 L
D6 RING 12 L
D6 RING 13 L
D6 RING 14 L
D6 RING 15 L
8881 E7
BF2
D5 MUX RING L
D7 LINE CNT MSB H
D7 LINE CNT + H
D7 LINE CNT LSB H
7417 E4
7417 E4
7417 E9
R22 750Ω
R21 750Ω
R20 750Ω
7442 BCD LINE DECOR
D3 CLOCK 15 L
D3 CLOCK 14 L
D3 CLOCK 13 L
D3 CLOCK 12 L
D3 CLOCK 11 L
D3 CLOCK 10 L
D3 CLOCK 9 L
D3 CLOCK 8 L
D3 A LINE CNT MSB H
D3 A LINE CNT + H
D3 A LINE CNT LSB H

J1
1488 E42
D3 SEC TX 8 H *
1488 E41
D3 TERM RDY 8 H
1488 E41
D3 RQ TO SEND 8 H
74175 E32 LINES 8
D7 000 H
D7 001 H
D7 002 H
D7 003 H
D3 LINE EN 8 L
D3 SEC TX 8 L *
D3 TERM RDY 8 L
D3 RQ TO SEND 8 L
D3 INI L

J1
1488 E18
D3 SEC TX 9 H *
1488 E18
D3 TERM RDY 9 H
1488 E18
D3 RQ TO SEND 9 H
74175 E25 LINES 9
D3 LINE EN 9 L
D3 SEC TX 9 L *
D3 TERM RDY 9 L
D3 RQ TO SEND 9 L
D3 INI L

J1
1488 E29
D3 SEC TX 10 H *
1488 E29
D3 TERM RDY 10 H
1488 E29
D3 RQ TO SEND 10 H
74175 E33 LINES 10
D3 LINE EN 10 L
D3 SEC TX 10 L *
D3 TERM RDY 10 L
D3 RQ TO SEND 10 L
D3 INI L

J1
1488 E42
D3 SEC TX 11 H *
1488 E18
D3 TERM RDY 11 H
1488 E29
D3 RQ TO SEND 11 H
74175 E28 LINES 11
D3 LINE EN 11 L
D3 SEC TX 11 L *
D3 TERM RDY 11 L
D3 RQ TO SEND 11 L
D3 INI L

* SEE NOTE 2.

7417 E4
R23 750Ω
+5V
D7 CLEAR MUX L
BJ1
7413 E4
D3 INI L

TO PIN 1 OF E16, E23, E29 1488 IC'S
AB2 BB2
D1 IN4733A
-15V
-10V A
C138 6.8 MFD

TO PIN 14 OF E16, E23, E29 1488 IC'S
D2 IN4733A
+15V
AU1
+10V A
C101 6.8 MFD

TO PIN 1 OF E18, E36, E42 1488 IC'S
AB2 BB2
D3 IN4733A
-15V
-10V B
C102 6.8 MFD

TO PIN 14 OF E18, E38, E42
D4 IN4733A
+15V
AU1
+10V B
C99 6.8 MFD

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (03)	D	CS	M7807-9-1	H
SCALE / / SHEET 4 OF 7	DIST.			

D3 EN MUX H

D6 CARRIER 8 L
D6 CARRIER 9 L
D6 CARRIER 10 L
D6 CARRIER 11 L
D6 CARRIER 12 L
D6 CARRIER 13 L
D6 CARRIER 14 L
D6 CARRIER 15 L

578 74151 E22 CARRIER SELECTOR

8881 E7

D4 MUX CARRIER L

D6 CLEAR TO SEND 8 L
D6 CLEAR TO SEND 9 L
D6 CLEAR TO SEND 10 L
D6 CLEAR TO SEND 11 L
D6 CLEAR TO SEND 12 L
D6 CLEAR TO SEND 13 L
D6 CLEAR TO SEND 14 L
D6 CLEAR TO SEND 15 L

578 74151 E15 CLEAR TO SEND SELECTOR

8881 E7

D4 MUX CLEAR TO SEND L

*

D6 SEC RX 8 L
D6 SEC RX 9 L
D6 SEC RX 10 L
D6 SEC RX 11 L
D6 SEC RX 12 L
D6 SEC RX 13 L
D6 SEC RX 14 L
D6 SEC RX 15 L

578 74151 E21 SEC RX SELECTOR

8881 E7

D4 MUX SEC RX L

D3 B LINE CNT LSB H
D3 B LINE CNT * H
D3 B LINE CNT MSB H

J2

1488 E16

D4 SEC TX 12 H *
D4 TERM RDY 12 H
D4 RQ TO SEND 12 H

74175 E34 LINES 12

D4 LINE EN 12 L
D4 SEC TX 12 L *
D4 TERM RDY 12 L
D4 RQ TO SEND 12 L

D3 INI L
D3 CLOCK 12 L

1488 E36

D4 SEC TX 13 H *
D4 TERM RDY 13 H
D4 RQ TO SEND 13 H

74175 E35 LINES 13

D4 LINE EN 13 L
D4 SEC TX 13 L *
D4 TERM RDY 13 L
D4 RQ TO SEND 13 L

D3 INI L
D3 CLOCK 13 L

1488 E23

D4 SEC TX 14 H *
D4 TERM RDY 14 H
D4 RQ TO SEND 14 H

74175 E18 LINES 14

D4 LINE EN 14 L
D4 SEC TX 14 L *
D4 TERM RDY 14 L
D4 RQ TO SEND 14 L

D3 INI L
D3 CLOCK 14 L

D7 000 H (BN1)
D7 003 H (BYTE)
D7 001 H (B.D.)
D7 002 H (BME)

* SEE NOTE 2

DCS M7807-2-1 H

REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (D4)	D	CS	M7807-01	H
SCALE 1=1 SHEET 5 OF 7	DIST.			

D3 LINE EN 8 L
D3 LINE EN 9 L
D3 LINE EN 10 L
D3 LINE EN 11 L
D4 LINE EN 12 L
D4 LINE EN 13 L
D4 LINE EN 14 L
LINE EN 15 L

D3 SEC TX 8 L
D3 SEC TX 9 L
D3 SEC TX 10 L
D3 SEC TX 11 L
D4 SEC TX 12 L
D4 SEC TX 13 L
D4 SEC TX 14 L
SEC TX 15 L *

D3 TERM RDY 8 L
D3 TERM RDY 9 L
D3 TERM RDY 10 L
D3 TERM RDY 11 L
D4 TERM RDY 12 L
D4 TERM RDY 13 L
D4 TERM RDY 14 L
TERM RDY 15 L

D3 RQ TO SEND 8 L
D3 RQ TO SEND 9 L
D3 RQ TO SEND 10 L
D3 RQ TO SEND 11 L
D4 RQ TO SEND 12 L
D4 RQ TO SEND 13 L
D4 RQ TO SEND 14 L
RQ TO SEND 15 L

D7 000 H
D7 001 H
D7 010 H
D7 002 H
D3 INIT L
D3 CLOCK 15 L

D3 8 LINE CNT MSB H
D3 8 LINE CNT + H
D3 8 LINE CNT LSB H
(R/W STATUS) D7 GROUP 8-15-H

D5 SEC TX 15 H
D5 TERM RDY 15 H
D5 RQ TO SEND 15 H

D5 MUX LINE EN L
D5 MUX LINE EN H
D5 MUX SEC TX L *
D5 MUX TERM RDY L
D5 MUX RQ TO SEND L
D5 EN RHT H

*SEE NOTE 2

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (D5)	D	CS	M7807-0-1	H
SCALE	SHEET 6 OF 7	DIST.		

J1 E5 — RING 8 H (1) → DG RING 8 L (3); C78 .47μf; R25 33K; −15V
AA RING 9 H (4) → DG RING 9 L (6); C69 .47μf; R26 33K
L RING 10 H (13) → DG RING 10 L (11); C64 .47μf; R27 33K
BB RING 11 H (10) → DG RING 11 L (8); C63 .47μf; R28 33K

J2 E9 — K RING 12 H (1) → DG RING 12 L (3); C76 .47μf; R29 33K
AA RING 13 H (4) → DG RING 13 L (6); C75 .47μf; R30 33K
L RING 14 H (13) → DG RING 14 L (11); C74 .47μf; R31 33K
BB RING 15 H (10) → DG RING 15 L (8); C73 .47μf; R32 33K

J1 E6 — U CARRIER 8 H (1) → DG CARRIER 8 L (3); C68 .47μf
KK CARRIER 9 H (4) → DG CARRIER 9 L (6); C71 .47μf
V CARRIER 10 H (13) → DG CARRIER 10 L (11); C72 .47μf
LL CARRIER 11 H (10) → DG CARRIER 11 L (8); C66 .47μf

J2 E30 — U CARRIER 12 H (1) → DG CARRIER 12 L (3); C91 .47μf
KK CARRIER 13 H (4) → DG CARRIER 13 L (6); C92 .47μf
V CARRIER 14 H (13) → DG CARRIER 14 L (11); C90 .47μf
LL CARRIER 15 H (10) → DG CARRIER 15 L (8); C88 .47μf

J1 E10 — S CLEAR TO SEND 8 H (1) → DG CLEAR TO SEND 8 L (3); C80 .47μf
NN CLEAR TO SEND 9 H (4) → DG CLEAR TO SEND 9 L (6); C79 .47μf
T CLEAR TO SEND 10 H (13) → DG CLEAR TO SEND 10 L (11); C77 .47μf
WW CLEAR TO SEND 11 H (10) → DG CLEAR TO SEND 11 L (8); C78 .47μf

J2 E17 — S CLEAR TO SEND 12 H (1) → DG CLEAR TO SEND 12 L (3); C84 .47μf
NN CLEAR TO SEND 13 H (4) → DG CLEAR TO SEND 13 L (6); C83 .47μf
T CLEAR TO SEND 14 H (13) → DG CLEAR TO SEND 14 L (11); C82 .47μf
WW CLEAR TO SEND 15 H (10) → DG CLEAR TO SEND 15 L (8); C81 .47μf

J1 E8 — Y SEC RX 8 H * (1) → DG SEC RX 8 L * (3); C67 .47μf
SS SEC RX 9 H * (4) → DG SEC RX 9 L * (6); C65 .47μf
E SEC RX 10 H * (13) → DG SEC RX 10 L * (11); C61 .47μf
VV SEC RX 11 H * (10) → DG SEC RX 11 L * (8); C62 .47μf

J2 E22 — Y SEC RX 12 H * (1) → DG SEC RX 12 L * (3); C87 .47μf
SS SEC RX 13 H * (4) → DG SEC RX 13 L * (6); C89 .47μf
E SEC RX 14 H * (13) → DG SEC RX 14 L * (11); C86 .47μf
VV SEC RX 15 H * (10) → DG SEC RX 15 L * (8); C85 .47μf

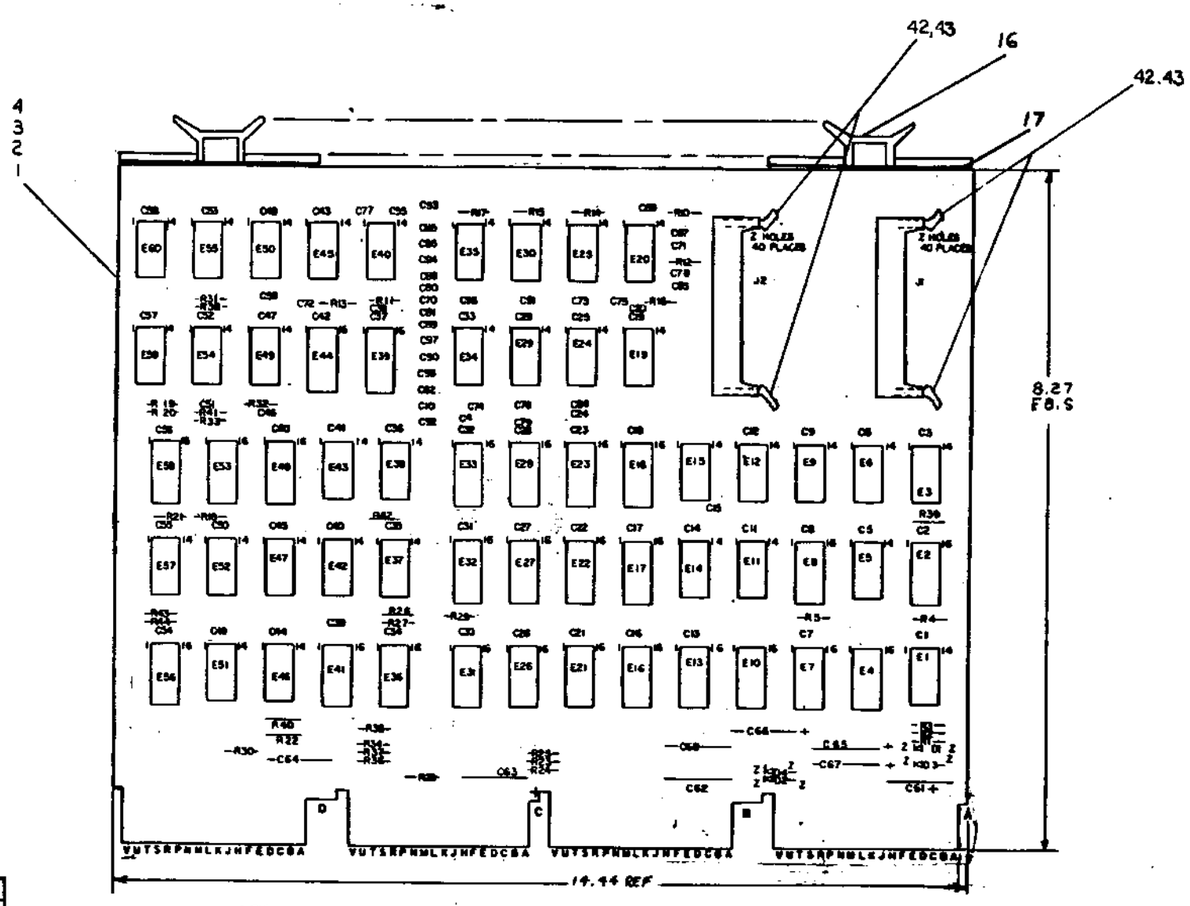
* SEE NOTE 2.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (D6)	D	CS	M7807-0-1	H
SCALE —	SHEET 7 OF 7	DIST.		

NOTES:

1. FOR −15V TO −10V AND +15V TO +10V SEE SHEET 7 OF 7
2. THE SIGNALS "SEC TX" AND "SEC Rx" REFER TO ASYNCHRONOUS OPERATION ONLY. WHEN THE MODULE IS USED IN A SYNCHRONOUS APPLICATION THE SIGNALS MAY BE USED AS "NEW SYNC" AND "DATA SET RDY" FOR THAT LINE.



DEC 4015	8	16
DEC 8271	8	16
DEC 7489	8	16
DEC 8640	1	8
DEC 8266	8	16
DEC 74123	8	16
DEC 7442	8	16
DEC 74175	8	16
DEC 74151	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

+5V BACKPLANE DISTRIBUTION
DC0, DT1
DC1, DT1
DC2, DT1

C61 0.1 μF | C62 0.1 μF | C63 0.1 μF | C1 THRU C3 .01 μF | C5 THRU C9 .01 μF | C11 THRU C58 .01 μF

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO
REF		X-Y COORDINATE HOLE LOCATION	X-CO-M7800-0-4	1
REF		ASSY/DRILL HOLE LAYOUT	D-AD-M7800-0-5	2
REF		MODULE ECO HISTORY	D-EH-M7800-0-0	3
1		ETCHED CIRCUIT BOARD	5010804	4
56	C1-3,5-9,11-56	CAP .01 MF, 100V, Z 20%	1001010-00	5
33	C4,10,58,59-60	CAP 470 PF, 100V, ± 5%	1000824	6
1	C60	CAP 82 PF, 100V, ± 5%	1000815	7
0	C61 THRU C64	CAP 0.1 MF, 25V, + 10%	1001300	8
4	Q1,2,3,4	DIODE 1N4733A ZENER	1150043	9
2	J1,J2	CONNECTOR 40 PIN	1200641	10
20	R1-4,10-20,32-38,40-43	RES. 750 1/4W 5%	1301401	11
1	R31	RES. 220 1/4W 5%	1300271	12
8	R18-17	RES. 330 1/4W 10%	1300510	13
0	R5,6,7,8	RES. 300Ω ±2% 1/4W 5%	1300300	14
1	R44	RES. 330 1/4W 5%	1300295	15
4		HANDLE FLIP CHIP	9000337-00	16
8		EYELET	9000722	17
1	E60	I.C. DEC 7474	1000643	18
8	E10,20,24,25,29,30,34,35	I.C. DEC 14009	1010323	19
8	E17,18,22,23,27,28,32,33	I.C. DEC 74151	1000836	20
8	E4,7,12,13,18,21,26,31	I.C. DEC 74175	1010651	21
8	E5,8,9,11,12,15	I.C. DEC 1489	1010322	22
2	E14,40	I.C. DEC 7410	1000675	23
1	E2	I.C. DEC 7442	1010640	24
2	E1,42	I.C. DEC 7417	1000329	25
1	E3	I.C. DEC 74123	1010436	26
4	E3,38,54,60	I.C. DEC 8881	1000700	27
2	E36,53	I.C. DEC 8266	1000634	28
2	E41,44	I.C. DEC 8830	1011117	29
1	E45	I.C. DEC 8640	1001409	30
1	E51	I.C. DEC 7418	1000828	31
1	E55	I.C. DEC 7400	1010300	32
1	E37	I.C. DEC 74197	1010836	33
2	E48,47	I.C. DEC 7400	1000673	34
1	E52	I.C. DEC 7408	1010195	35
2	E55,57	I.C. DEC 8015	1000713	36
2	E40,43	I.C. DEC 7404	1000600	37
1	E48	I.C. DEC 8271	1000615	38
2	E39,58	I.C. DEC 4015	1010007	39
1	E50	I.C. DEC 7408	1010011	40
2	R9,39	RES. 10K,1/4W,5%	7300479	41
2		LEFT LATCH	1209941-03	42
2		RIGHT LATCH	1209941-04	43
A/R		WIRE 30 AWG	9105740-55	44

PARTS LIST

FIRST USED ON OPTION MODEL

ETCH BOARD REV D

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

REVISIONS	DWN	CHANGE NO.	DATE
M7800-00002	J.McINTYRE		4-19-74
M7800-00003	J.McINTYRE		4-22-74
M7800-00004	J.McNAMARA		5-21-74
M7800-00005	R.HARRINGTON		6-13-74
ORIGINATED	W.FANDRICK		10-30-73

NEXT HIGHER ASSY

SCALE NONE
SHEET 1 OF 7

digital EQUIPMENT CORPORATION

TITLE: MODEM CONTROL

SIZE D | CODE DCS | NUMBER M7800-0-1 | REV J

NOTE:

* REMOVE WIRE TO INHIBIT INTERUPTS FROM TRANSITIONS.

* SEE NOTE 2.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
MODEM CONTROL (D7)	D	CS	M7808-0-1	J
SCALE	SHEET 2 OF 7		DWG.	

+3V

D7 LINE CNT +H
D7 LINE CNT MSB H
D7 GROOP 8-15 H
D7 LINE CUNT LSB H
8815 E57
7410 E46
D7 CLEAR SCAN L
DR1 DB CLEAR CYCLE (0) L

+5V D7 LD HOLD H DV1
7404 E48

+5V
R23 750Ω R24 750Ω R25 750Ω R22 750Ω
R18 750Ω R19 750Ω R20 750Ω R21 750Ω

D7 MAINT MODE(1) H
7416 E51
7410 E51
CD1 D4,D10 MUX CLEAR TO SEND L
7416 E51
CA1 D4,D10 MUX CARRIER L
7416 E51
CC1 D3,D9 MUX RING L

D4,D10 MUX SEC RC L CB1

7489 E66
WR ENB
D0 M0(1)
D1 M1(1)
D2 M2(1)
D3 M3(1)
A3 A2 A1 A0

D7 GROOP 8-15 H DV2
D7 LINE CNT MSB H DU2
D7 LINE CNT +H DU1
D7 LINE CNT LSB H DS1

7486 E59
7404 E48
4015 E58
D3 R3(1)
D2 R2(1)
D1 R1(1)
D0 R0(1)
OSET3
OSET2
OSET1
OSET0
CLR CLK
+3V

D7 LD HOLD H DP1

D7 RD SCAN STATUS H
8881 E60
DR2 DB BUS DATA 12 L
DR1 DB BUS DATA 13 L
DSC DB BUS DATA 14 L
DPC DB BUS DATA 15 L
8816 E55
+3V
7486 E59
DB TRANSITION DET H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
MODEM CONTROL (08)	D	CS	M7808-0-1	U
SCALE	SHEET 3 OF 7		DIST.	

D1 SELECT 2H — 8T2 — 74153 E8 — D1 OUT LOW H BUS 7 / D9 GROUP 0-7 H BUS 15 — 7416 E10 — 12

+5V — R5 10K — 7

+5V — R44 330Ω — R43 75Ω

+5V — R3 75Ω — R2 75Ω — R1 75Ω

D7 LINE CNT MSB H — 8K2 — 13 — 7417 E1 — 12

D7 LINE CNT + H — BL2 — 11 — 7417 E1 — 10

D7 LINE CNT LSB H — BM2 — 9 — 7417 E1 — 8

7442 E2: D3 ← 12, D2 ← 13, D1 ← 14, D0 ← 15; F9 → 11, F8 → 10, F7 → D9 CLOCK 7 L, F6 → D9 CLOCK 6 L, F5 → D9 CLOCK 5 L, F4 → D9 CLOCK 4 L, F3 → D9 CLOCK 3L, F2 → D9 CLOCK 2L, F1 → D9 CLOCK 1L, F0 → D9 CLOCK 0L

D9 SW MUX LINE EN H — BS1 4 — 7416 E10 — 9
D11 GROUP 0-7 H — BC8 11
D8 CLEAR CYCLE L — BC9 10

9 → 7404 E9B → 13 → D9 ENA MUX H

74151 E18: D0 ← D12 RING 0 L, D1 ← D12 RING 1 L, D2 ← D12 RING 2 L, D3 ← D12 RING 3 L, D4 ← D12 RING 4 L, D5 ← D12 RING 5 L, D6 ← D12 RING 6 L, D7 ← D12 RING 7 L; S2 S1 S0 ← 9 10 11; F → 6 → 12 → 8881 E13 → 13 → BF2 → D9 MUX RING L; F1 → 5

D9 B LINE CNT MSB H
D9 B LINE CNT + H
D9 B LINE CNT LSB H

J1

1488 E6: 4,5 → 6 W → D9 SEC TX Ø H *; 12,13 → 11 M → D9 TERM RDY Ø H; 9,10 → 8 P → D9 RQ TO SEND Ø H

1488 E5: 4,5 → 6 UU → D9 SEC TX 1 H *; 12,13 → 11 CC → D9 TERM RDY 1 H; 9,10 → 8 EE → D9 RQ TO SEND 1 H

1488 E7: 4,5 → 6 L → D9 SEC TX 2 H *; 12,13 → 11 H → D9 TERM RDY 2 H; 9,10 → 8 K → D9 RQ TO SEND 2 H

1488 E4: 2,3 → 6 TT → D9 SEC TX 3 H *; 12,13 → 11 DD → D9 TERM RDY 3 H; 9,10 → 8 FF → D9 RQ TO SEND 3 H

74175 E4 LINE Ø: D7 D00 H — BN1 — 4 D0; D7 D03 H — BJ2 — 5 D1; D7 D01 H — BP1 — 12 D2; D7 D02 H — BH2 — 13 D3; R0(1) → 8 → D9 LINE EN Ø L; R0(0) → 3 → D9 SEC TX Ø L *; R1(1) → 7 → D9 TERM RDY Ø L; R1(0) → 6 → D9 RQ TO SEND Ø L; CLR ← D9 INI L ← 1; CLK ← 9

74175 E7 LINE 1: D0 ← 4; D1 ← 5; D2 ← 12; D3 ← 13; R0(1) → 2 → D9 LINE EN 1 L; R0(0) → 3 → D9 SEC TX 1 L *; R1(1) → 7 → D9 TERM RDY 1 L; R1(0) → 6 → D9 RQ TO SEND 1 L; CLR ← D9 INI L ← 1; CLK ← 9

74175 E10 LINE 2: D0 ← 4; D1 ← 5; D2 ← 12; D3 ← 13; R0(1) → 2 → D9 LINE EN 2 L; R0(0) → 3 → D9 SEC TX 2 L *; R1(1) → 7 → D9 TERM RDY 2 L; R1(0) → 6 → D9 RQ TO SEND 2 L; CLR ← D9 INI L ← 1; CLK ← 9

74175 E13 LINE 3: D0 ← 4; D1 ← 5; D2 ← 12; D3 ← 13; R0(1) → 2 → D9 LINE EN 3 L; R0(0) → 3 → D9 SEC TX 3 L *; R1(1) → 7 → D9 TERM RDY 3 L; R1(0) → 6 → D9 RQ TO SEND 3 L; CLR ← D9 INI L ← 1; CLK ← 9

D7 CLEAR MUX L — BJ1 — 5 — 7417 E1 — 6 — D9 INI L; 1 — 7417 E1 — 2 — R4 75Ω — +5V

D1 IN4733A (TO PIN 3 OF 3 1488 IC'S): −15V — AB2 BB2 — C65 6.8μF — −10V

D2 IN4733A (TO PIN 14 OF 3 1488 IC'S): +15V — AU1 — C66 6.8μF — +10V

*SEE NOTE 2.

REVISIONS		
CHK	CHANGE NO	REV

(MUX)
TITLE: MODEM CONTROL (D9)
SIZE D | CODE CS | NUMBER M78Ø8-Ø-1 | REV J
SCALE | SHEET 4 OF 7 | DIST.

D9 EN MUX H

DIZ CARRIER Ø L
DIZ CARRIER 1 L
DIZ CARRIER 2 L
DIZ CARRIER 3 L
DIZ CARRIER 4 L
DIZ CARRIER 5 L
DIZ CARRIER 6 L
DIZ CARRIER 7 L
→ 8T78 74151 E23 CARRIER SELECTOR → 8881 E3 → D10 MUX CARRIER L

DIZ CLEAR TO SEND Ø L
DIZ CLEAR TO SEND 1 L
DIZ CLEAR TO SEND 2 L
DIZ CLEAR TO SEND 3 L
DIZ CLEAR TO SEND 4 L
DIZ CLEAR TO SEND 5 L
DIZ CLEAR TO SEND 6 L
DIZ CLEAR TO SEND 7 L
→ 8T78 74151 E28 CLEAR TO SEND SELECTOR → 8881 E3 → 4 BC1 → D10 MUX CLEAR TO SEND L

*DIZ SEC RX Ø L
DIZ SEC RX 1 L
DIZ SEC RX 2 L
DIZ SEC RX 3 L
DIZ SEC RX 4 L
DIZ SEC RX 5 L
DIZ SEC RX 6 L
DIZ SEC RX 7 L
→ 8T78 74151 E33 SEC RX SELECTOR → 8881 E3 → 6 BA1 → D10 MUX SEC RX L *

D9 LINE CNT LSB H
D9 LINE CNT + H
D9 LINE CNT MSB H

J2

1488 E12 → D10 SEC TX 4 H *
1488 E12 → D10 TERM RDY 4 H
1488 E12 → D10 RQ TO SEND 4 H

74175 E16 LINE 4
LINE EN 4 L
SEC TX 4 L *
TERM RDY 4 L
RQ TO SEND 4 L
D9 INI L
D9 CLOCK 4 L

1488 E11 → D10 SEC TX 5 H *
1488 E11 → D10 TERM RDY 5 H
1488 E11 → D10 RQ TO SEND 5 H

74175 E21 LINE 5
LINE EN 5 L
SEC TX 5 L
TERM RDY 5 L
RQ TO SEND 5 L
D9 INI L
D9 CLOCK 5 L

1488 E15 → D10 SEC TX 6 H *
1488 E15 → D10 TERM RDY 6 H
1488 E15 → D10 RQ TO SEND 6 H

74175 E26 LINE 6
LINE EN 6 L
SEC TX 6 L *
TERM RDY 6 L
RQ TO SEND 6 L
D9 INT L
D9 CLOCK 6 L

D0Ø H
D0Ø3 H
D0Ø1 H
D0Ø2 H

D3 IN4733A (TO PIN 1 OF 3 1488 IC'S)
-15V A82 B82 → C67 6.8µF → -10V

D9 IN4733A (TO PIN 14 OF 3 1488 IC'S)
+15V A11 → C68 6.8µF → +10V

* SEE NOTE 2.

REVISIONS

CHK	CHANGE NO	REV

(MUX)
TITLE: MODEM CONTROL (D10)
SIZE: D | CODE: CS | NUMBER: M78Ø8-Ø-1 | REV: J
SCALE | SHEET 5 OF 7 | DIST

D7 6P08P 6-7 H
852

D9 LINE END L
D9 LINE EN 1 L
D9 LINE EN 2 L
D9 LINE EN 3 L
D10 LINE EN 4 L
D10 LINE EN 5 L
D10 LINE EN 6 L
LINE EN 7 L

D9 SEC TX Ø L
D9 SEC TX 1 L
D9 SEC TX 2 L
D9 SEC TX 3 L
D10 SEC TX 4 L
D10 SEC TX 5 L
D10 SEC TX 6 L
* SEC TX 7 L

D9 TERM RDYØ L
D9 TERM RDY 1 L
D9 TERM RDY 2 L
D9 TERM RDY 3 L
D10 TERM RDY 4 L
D10 TERM RDY 5 L
D10 TERM RDY 6 L
TERM RDY 7 L

D9 RQ TO SEND Ø L
D9 RQ TO SEND 1 L
D9 RQ TO SEND 2 L
D9 RQ TO SEND 3 L
D10 RQ TO SEND 4 L
D10 RQ TO SEND 5 L
D10 RQ TO SEND 6 L
RQ TO SEND 7 L

D9 LINE CNT MSB H
D9 LINE CNT + H
D9 LINE CNT LSB H

D7, DØØ H
D7, DØ1 H
D7, DØ2 H
D7, DØ3 H
D9 INT L
D9 CLOCK 7 L

D11 SEC TX 7 H
D11 TERM RDY 7 H *
D11 RQ TO SEND 7 H

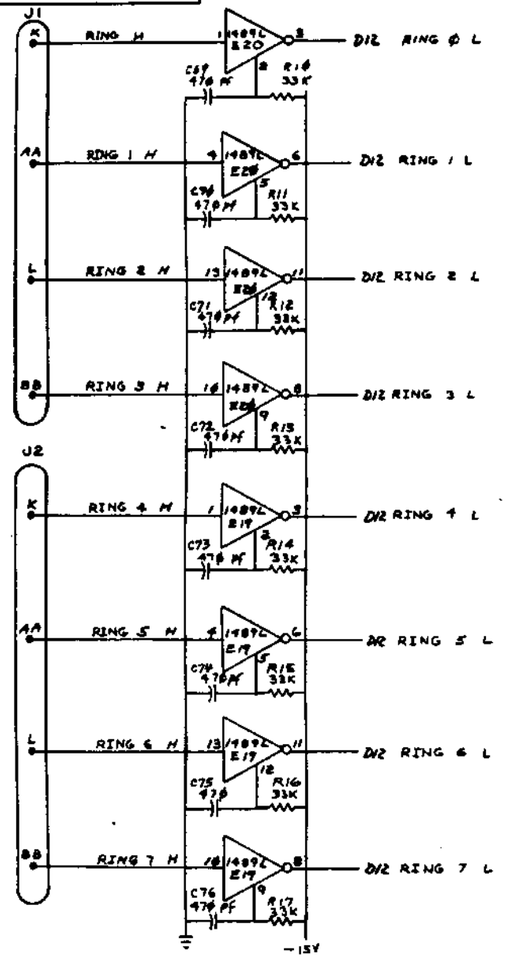
D11 MUX LINE EN L
D11 MUX LINE EN H
D11 * MUX SEC TX L
D11 MUX TERM RDY L
D11 MUX RQ TO SEND L

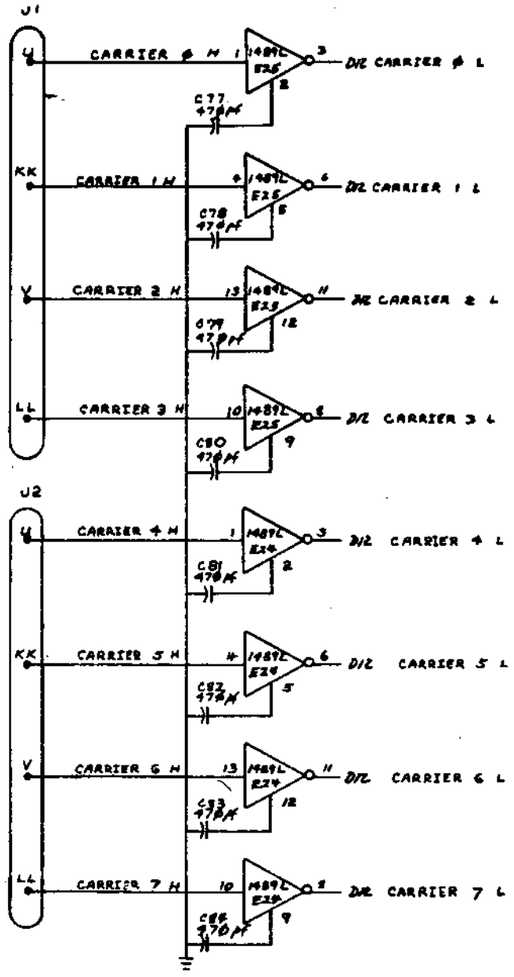
BK1 BV2 BL1 BF1 BH1

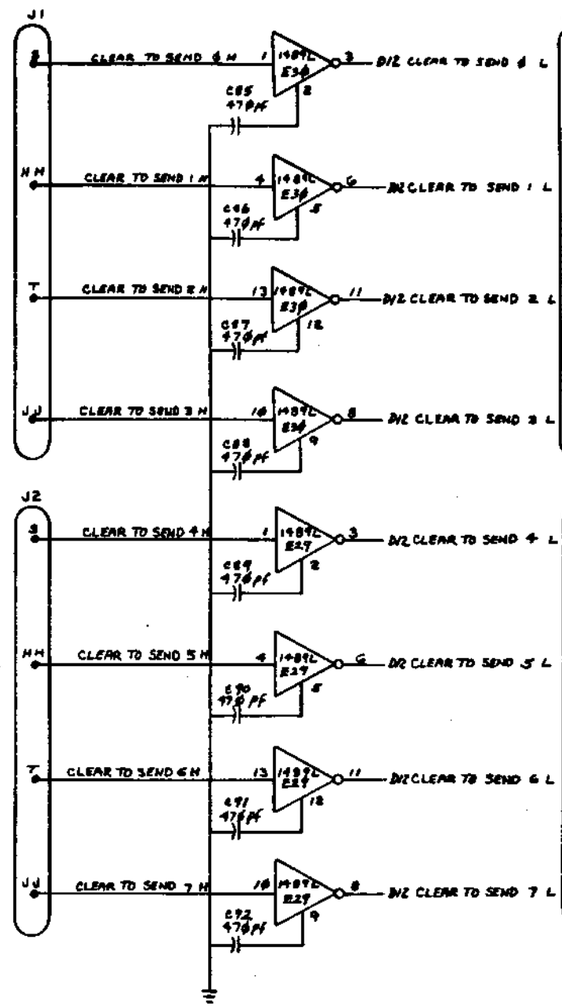
* SEE NOTE 2.

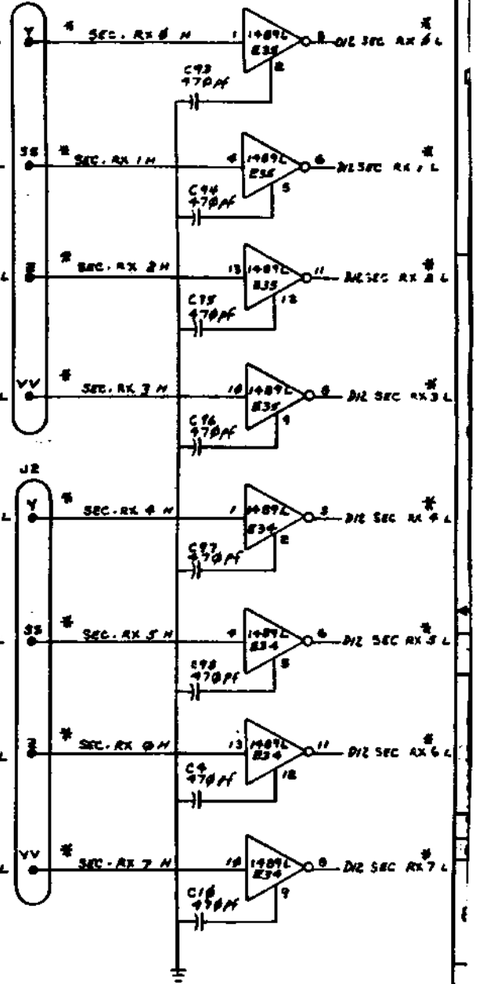
REVISIONS		
CHR	CHANGE NO	REV

TITLE	MODEM CONTROL (011)		
SIZE	CODE	NUMBER	REV.
D	CS	M7808-0-1	J
SCALE	SHEET 6 OF 7	DRV.	









* SEE NOTE 2

REVISIONS		
CHK	CHANGE NO	REV

(EIA LEVEL CONVERTERS)

TITLE	SIZE	CODE	NUMBER	REV.
MODEM CONTROL (DI2)	D		CS M7808-Ø-1	J
SCALE	SHEET 7 OF 7		DIST.	