ELECTRICAL

CUSTOMER PRINT SET 1	MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X		1	D-UA-DV11-Ø-Ø		9	BASIC ASSY (DV11)	
X			A-SP-DV11-Ø-1	A	36	ENGINEERING SPEC	
	X		A-SP-DV11-Ø-2		3	DV11 MODULE TEST PROCEDURE	
	X		A-SP-DV11-Ø-3	A	19	DV11 TEST PROCEDURE	
X	X		A-SP-DV11-Ø-4		3	ACCEPTANCE PROCEDURE	
X			A-PL-DV11-Ø-5		1	SHIPPING LIST	
X			A-PL-DV11-Ø-6		1	SOFTWARE LIST	
X			D-BD-DV11-Ø-8		2	DV11 MODEM CONTROL	
X			C-IC-DV11-Ø-9		1	INTERCONNECTION DV11	
X			D-BS-DV11-Ø-1Ø		9	LINE CARD Ø-3	
X			D-BS-DV11-Ø-11		9	LINE CARD 4-7	
X			D-BS-DV11-Ø-12		9	LINE CARD 8-11	
X			D-BS-DV11-Ø-13		9	LINE CARD 12-15	
C			K-CS-DV11-Ø-14	A	13	MICROPROGRAM LISTING	
X		2	D-AD-7010834-0-0	#	1	LOGIC ASSY (DV11)	
			A-WT-7010834-0		1	AWT REV STATUS	
X			D-IA-7010835-0-0	#	1	POWER HARNESS (DV11)	
X		3	D-AD-7010655-0-0	#	1	WIRED ASSY (DV11)	
C			K-WL-DV11-Ø-7		1	WIRE LIST	
X		4	D-IA-7010719-0-0	#	1	BACKPLANE ASSY	
X		5	D-CS-5411420-0-1	#	1	CIRCUIT SCHEMATIC	
			K-CO-5411420-0-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-5411420-0-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-5411420-0-6		1	MODULE ECO HISTORY	

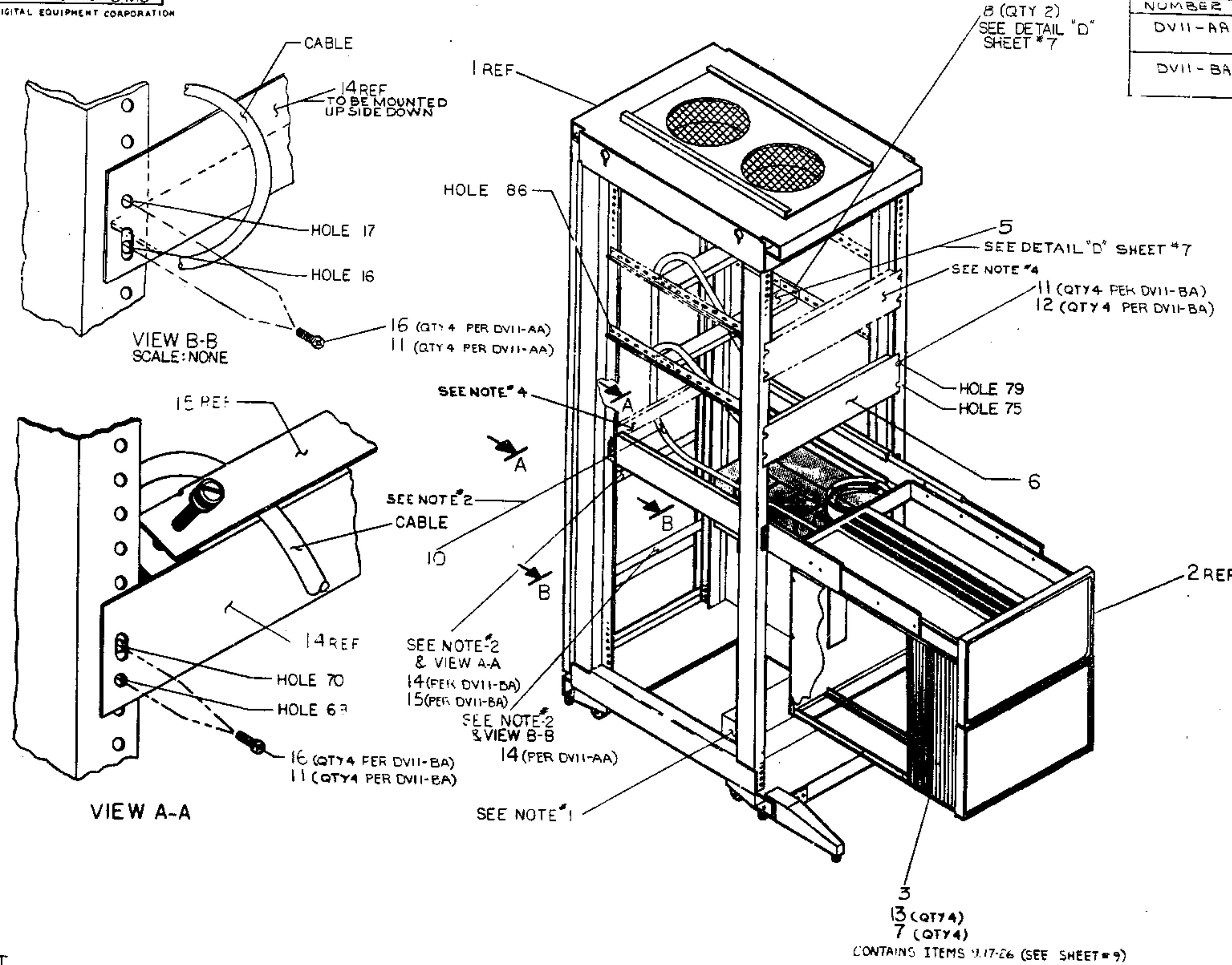
ELECTRICAL

CUSTOMER PRINT SET 1	MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X		6	D-CS-M7836-Ø-1	#	10	ALU AND TRANSFER BUS	
			K-CO-M7836-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-M7836-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-M7836-Ø-6		1	MODULE ECO HISTORY	
X		7	D-CS-M7837-Ø-1	#	11	UNIBUS DATA AND NPR CONTROL	
			K-CO-M7837-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-M7837-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-M7837-Ø-6		1	MODULE ECO HISTORY	
X		8	D-CS-M7838-Ø-1	#	11	ROM, RAM & BRANCH	
			K-CO-M7838-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-M7838-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-M7838-Ø-6		1	MODULE ECO HISTORY	
			K-CS-M7838-Ø-8		9	23-A1Ø1A2 (ROM LIST)	
			K-CS-M7838-Ø-9		9	23-A1Ø2A2 (ROM LIST)	
			K-CS-M7838-Ø-1Ø		9	23-A1Ø3A2 (ROM LIST)	
			K-CS-M7838-Ø-11		9	23-A1Ø4A2 (ROM LIST)	
			K-CS-M7838-Ø-12		9	23-A1Ø5A2 (ROM LIST)	
			K-CS-M7838-Ø-13		9	23-A1Ø6A2 (ROM LIST)	
			K-CS-M7838-Ø-14		9	23-A1Ø7A2 (ROM LIST)	
			K-CS-M7838-Ø-15		9	23-A1Ø8A2 (ROM LIST)	
X		9	D-CS-M7839-Ø-1	#	9	SYNCH MUX LINE CARD	
			K-CO-M7839-Ø-4		1	X-Y COORDINATE HOLE LOCATION	
			D-AH-M7839-Ø-5		1	ASSY/DRILLING HOLE LAYOUT	
			B-MH-M7839-Ø-6		1	MODULE ECO HISTORY	

CUSTOMER PRINT SET CODES

X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE	SHEET	SIZE	CODE	NUMBER	REV
BASIC ASSY (DV11)	3 OF 5	B	OD	DV11-Ø	B



LEGEND	
NUMBER	VARIATION
DV11-AA	SYNCH MUX CONTROL UNIT
DV11-BA	MODULE SET & DIST. PANEL

NOTES:

1. 861 POWER CONTROL MUST BE LOCATED AT FRONT OF CABINET TO ALLOW CABLES FROM ITEM (#6) TO SWEEP BEHIND AND UNDER ITEM #2
2. EACH H960 CONTAINING A DV11 SHALL HAVE ONE STRAIN RELIEF (ITEM 14) AND CLAMP (ITEM 15) FOR BC08R CABLES AND ONE STRAIN RELIEF AT THE LOWER REAR OF CABINET. SEE VIEWS A-A AND B-B.
3. A CABINET THAT CONTAINS AN EXPANDER BOX CANNOT HAVE MORE THAN TWO CABLE BOX ASSEMBLIES ITEM #6. FOR SYSTEMS WITH THREE OR MORE CABLE BOX ASSEMBLIES A SEPERATE CABINET MUST BE USED. UP TO FOUR (4) PANELS CAN BE MOUNTED INTO CABINETS WITHOUT AN EXPANDER BOX.
4. 8 LINE SYSTEM IS SHOWN; TO MAKE UP 16 LINE SYSTEM ADD THE FOLLOWING EQUIPMENT (SHOWN WITH PHANTOM LINES): ONE H317-C (ITEM #6) USING MTG HOLES 95 & 97, TWO SIDE BAR SUPPORTS (ITEM #8) USING MTG HOLE #99, ONE CROSS BAR CABLE BRKT (ITEM #5), ONE STRAIN RELIEF (ITEM #14), ONE CLAMP STRAIN RELIEF (ITEM #15) AND NECESSARY MTG HARDWARE

QTY DV11-BA	QTY DV11-AA	DESCRIPTION	PART NO.	ITEM NO.
1	-	H325 TEST CONNECTOR	D-CS-H325-0-1	26
-	1	H861 TEST CONNECTOR	D-CS-H861-0-1	25
2	-	LINE CARD TEST CONNECTOR	C-UA-H8612-0-0	24
-	1	MODEM CONTROL	D-CS-M7868-0-1	23
2	-	SYNCH MUX LINE CARD	D-CS-M763 -0-1	22
-	1	ROM, RAM & BRANCH	D-CS-M7838-0-1	[illegible]
-	1	N BUS [illegible] AND [illegible] CONTROL	D-CS-M7837-0-1	[illegible]
-	1	ALU AND TRANSFER BUS	D-CS-M7836-0-1	19
-	1	BUS CONTROL & MUX	D-CS-M7867-0-1	[illegible]
-	1	INTERNAL BUS CONN M920	[illegible] M920-0-0	[illegible]
8	4	SCR, PHL PAN HD 10-32 X 3/8 LG	9006071-1	[illegible]
1	-	CLAMP, STRAIN RELIEF	C-IA-7411633-0-0	15
1	1	STRAIN RELIEF	C-IA-7411632-0-0	14
-	4	SCR PHL PAN HD #8-32-1 LG	9006043-1	13
8	-	SCR PHL PAN HD #10-32-5/8 LG	9006074-1	12
8	4	NUT, TINNERMAN #10-32	9007786	[illegible]
4	-	I/O CABLE (BC08R)	C-UA-BC08R-12-0	[illegible]
-	1	PRIORITY JUMPER LEVEL #5	C-IA-5408778-0-0	9
2	-	SIDE BAR SUPPORT	C-IA-7408285-0-0	8
-	4	WASHER, LOCK #8 EXT TOOTH	9008072	7
1	-	H517-C CABLE BOX ASS'Y	D-UA-H517-C-0	6
1	-	CROSS BAR CABLE BRK'T.	D-MD-7408510-0-0	5
8	-	WASHER LOCK #10 EXT	9007651	4
-	1	LOGIC ASSY (DV11)	D-AD-7010834-00	3
REF	REF	MOUNTING BOX ASSY	D-UA-BA11-FC-0	2
REF	REF	H960 CABINET	D-UA-H960-CD-0	1

PARTS LIST

FIRST USED ON OPTION/MODEL	PDP 11
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES	DECIMALS .XXX ± .005 .XX ± .02 .X ± .1; ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY	✓
MATERIAL	—
FINISH	—
DRN	DATE 11-25-74
CHKD	DATE 4-23-75
ENG	DATE 4-23-75
PROD	DATE 4-23-75
APPD R. Wall	DATE 4-27-75
NEXT HIGHER ASSY.	B-DD-DV11-0
SCALE	—
SHEET	1 OF 9

DIGITAL EQUIPMENT CORPORATION

TITLE: BASIC ASSY DV11

SIZE	CODE	NUMBER	REV.
D	UA	DV11-0-0	

DIST.

CUSTOMER PRINT SET 1	MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
			MECHANICAL				
		1	D-UA-DV11-Ø-Ø		9	BASIC ASSY (DV11)	
			D-MD-7408510-0-0		1	CROSS BAR CABLE BRKT	
			C-IA-7408283-0-0		1	SIDE BAR SUPPORT	
			C-IA-7411632-0-0		1	STRAIN RELIEF	
			C-IA-7411633-0-0		1	CLAMP, STRAIN RELIEF	
		2	D-AD-7010834-0-0		1	LOGIC ASSY (DV11)	
			D-IA-7010835-0-0		1	POWER HARNESS (DV11)	
		3	D-AD-7010655-0-0		1	WIRED ASSY (DV11)	
		4	D-IA-7010719-0-0		1	BACKPLANE ASSY	
		12	C-UA-M92Ø-Ø-Ø		1	INTERNAL BUS CONN ASSY	
			A-PL-M92Ø-Ø-Ø		1	INTERNAL BUS CONN. M92Ø	
			A-DC-7407806-0-0		1	DEC UNIBUS DECAL	
		13	B-DD-H317-Ø		3	H317 CABLE BOX ASSY	
		14	C-IA-BCØ8R-Ø-Ø		1	MODEM I/O CABLE ASSY	

CUSTOMER PRINT SET	MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
			MECHANICAL				

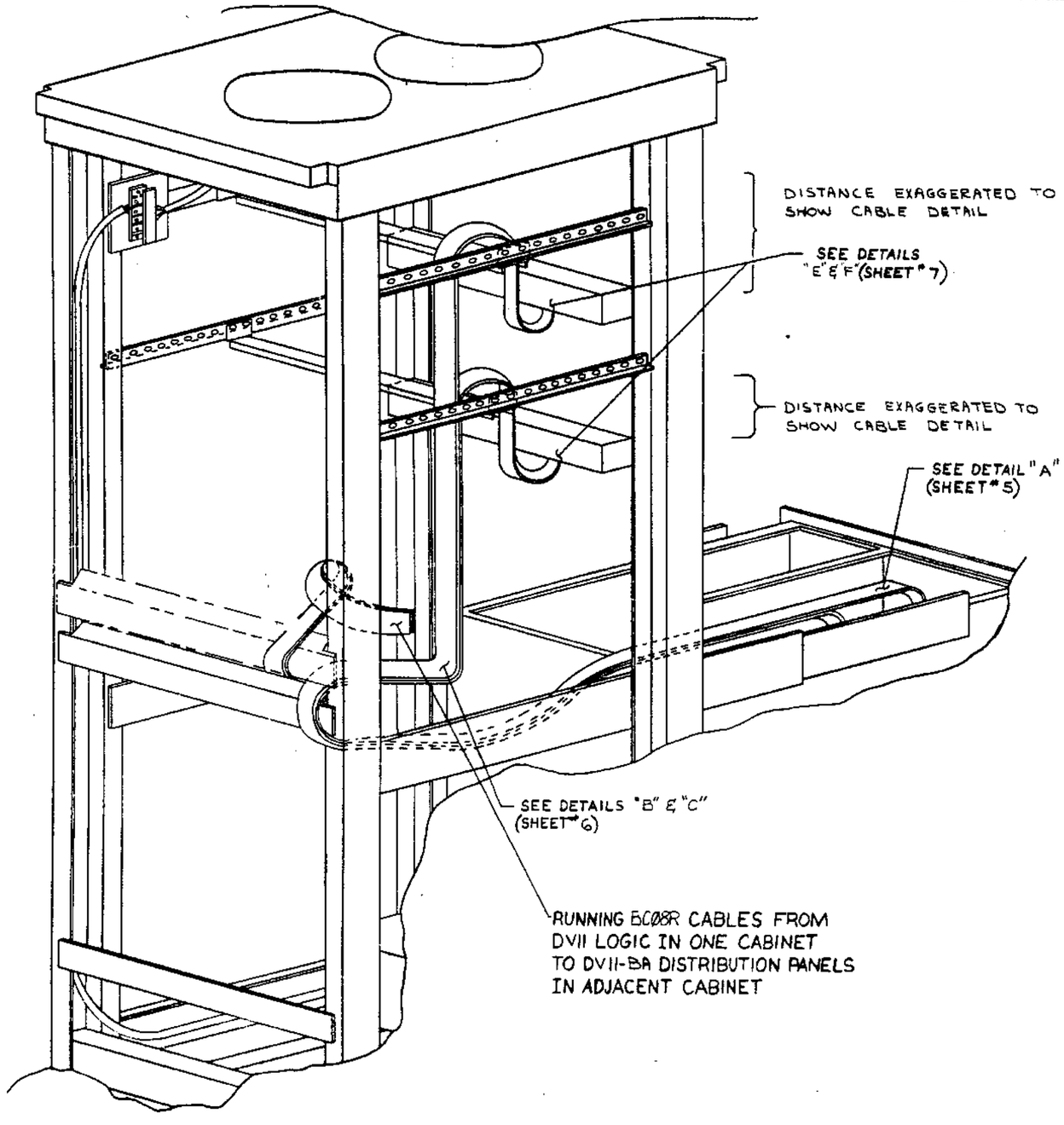
CUSTOMER PRINT SET CODES

X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE	SHEET	OF	SIZE	CODE	NUMBER	REV
BASIC ASSY (DV11)	5	5	B	DD	DV11-Ø	B

DRB 108

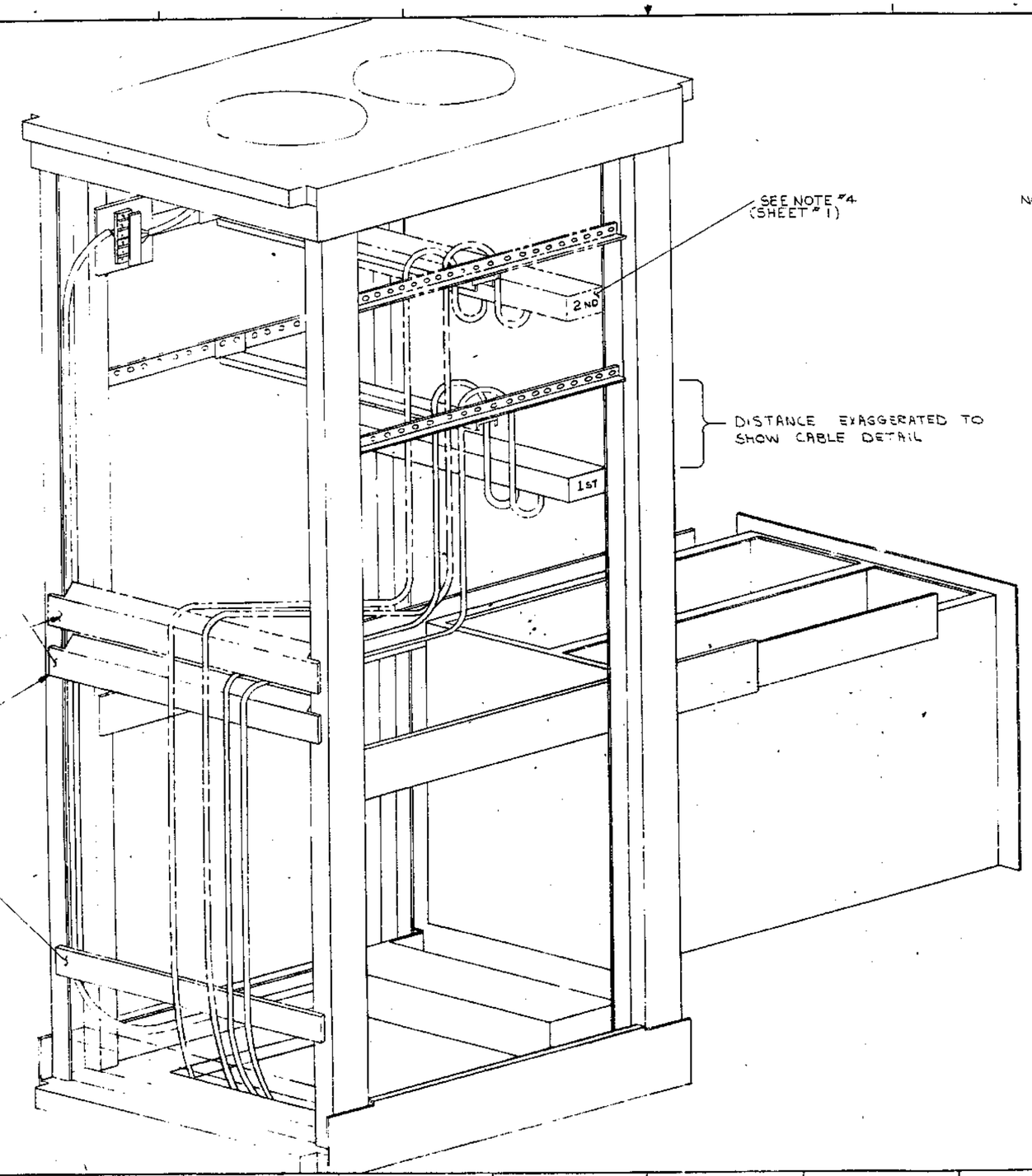
DEC 16-(325)-1062-2B-R972



NOTE:
FOR ROUTING BCØ5R CABLES FROM DVII LOGIC & EXPANDER BOX TO DISTRIBUTION PANELS IN SAME CABINET OR ADJACENT CABINET. SEE SHEET # 2 FOR BCØ5D CABLE ROUTING.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: BASIC ASSY. DVII		SIZE: D	CODE: UA	NUMBER: DVII-Ø-Ø
SCALE: NONE	SHEET 3 OF 9	DIST.		REV.



NOTE:
FOR ROUTING BC05D CABLES FROM DISTRIBUTION PANELS TO MODEMS. SEE SHEET #3 FOR ROUTING BC05R CABLES.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	BASIC ASSY DV11	SIZE	CODE	NUMBER / REV.
SCALE NONE	SHEET 2 OF 9	D	04	DV11-D-0
		DIST.		

TO DETAIL "C" SHEET #6

TO DETAIL "C" SHEET #6

MODEM CONTROL LEADS FOR LINES 8-11 (UJ10)

MODEM CONTROL LEADS FOR LINES 12-15 (UJ12)

USE H861 (ITEM #25) FOR MODEM CONTROL CABLE MAINTENANCE (SEE A-SP-DVII-0-0)

25

DATA AND CLOCK, LINES 12-15 (UJ11)

DATA AND CLOCK, LINES 8-11 (UJ9)

DATA AND CLOCK, LINES 4-7 (LJ11)

DATA AND CLOCK, LINES 0-3 (LJ9)

MODEM CONTROL LEADS FOR LINES 4-7 (LJ12)

MODEM CONTROL LEADS FOR LINES 0-3 (LJ10)

SHIELD SIDE

SHIELD SIDE

M7808

M7809 MODULES

9 8 7 6

H8612 CONNECTOR (ITEM #24) INSERTED IN PLACE OF CABLE FOR MAINTENANCE (SEE A-SP-DVII-0-0)

24

SHIELD SIDE

SHIELD SIDE

M7807

4 3 2 1

A B C D E

DETAIL "A"

ALL CABLES SHOWN ARE BC08R
FOR MODULE PLACEMENT INFORMATION SEE SHEET #9

REVISIONS		
CHK	CHANGE NO	REV

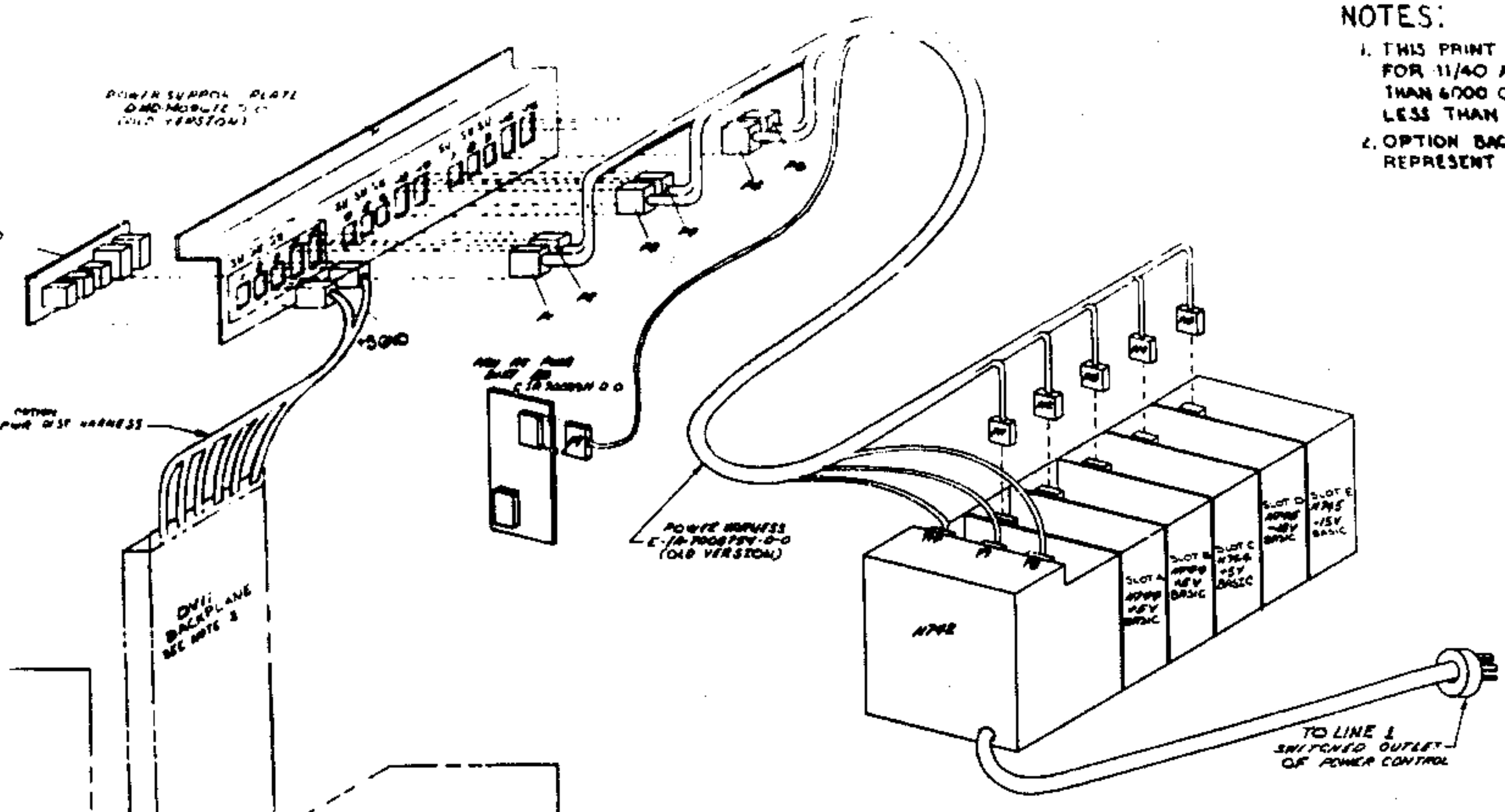
APPLICATION: DVII-AA,BA

TITLE	SIZE	CODE	NUMBER	REV.
BASIC ASSY DVII	D	UA	DVII-0-0	

SCALE NONE SHEET 5 OF 9 DIST

NOTES:

1. THIS PRINT SHOWS HARNESS ARRANGMENTS FOR 11/40 AND 11/35 WITH SERIAL NO. LESS THAN 6000 OR H960-D,E WITH SERIAL NO. LESS THAN 7000.
2. OPTION BACKPLANES AND HARNESSES REPRESENT TYPICAL INSTALLATION.



WIRING SIDE

LOCATING PIN

OPTION POWER CONNECTOR PIN ASSIGNMENTS

1. DC LO — #18 AWG VIO
2. AC LO — #18 AWG YEL
3. -15V TO 18A — #18 AWG BLU
4. GND
5. GND } #18 AWG BLK
6. GND
7. LINE CLOCK — #18 AWG BRN
8. +15V TO 1A — #18 AWG GRY
9. +5V TO 18A — #18 AWG RED

POWER DISTRIBUTION
(OLD VERSION)

NOTES:

1. THIS PRINT SHOWS HARNESS ARRANGMENTS FOR 11/40 AND 11/35 WITH SERIAL NO. GREATER THAN 6000 OR H960-D,E WITH SERIAL NO. GREATER THAN 7000.
2. OPTION BACKPLANES AND HARNESSES REPRESENT TYPICAL INSTALLATION.

WIRING SIDE

OPTION POWER CONNECTORS PIN ASSIGNMENTS

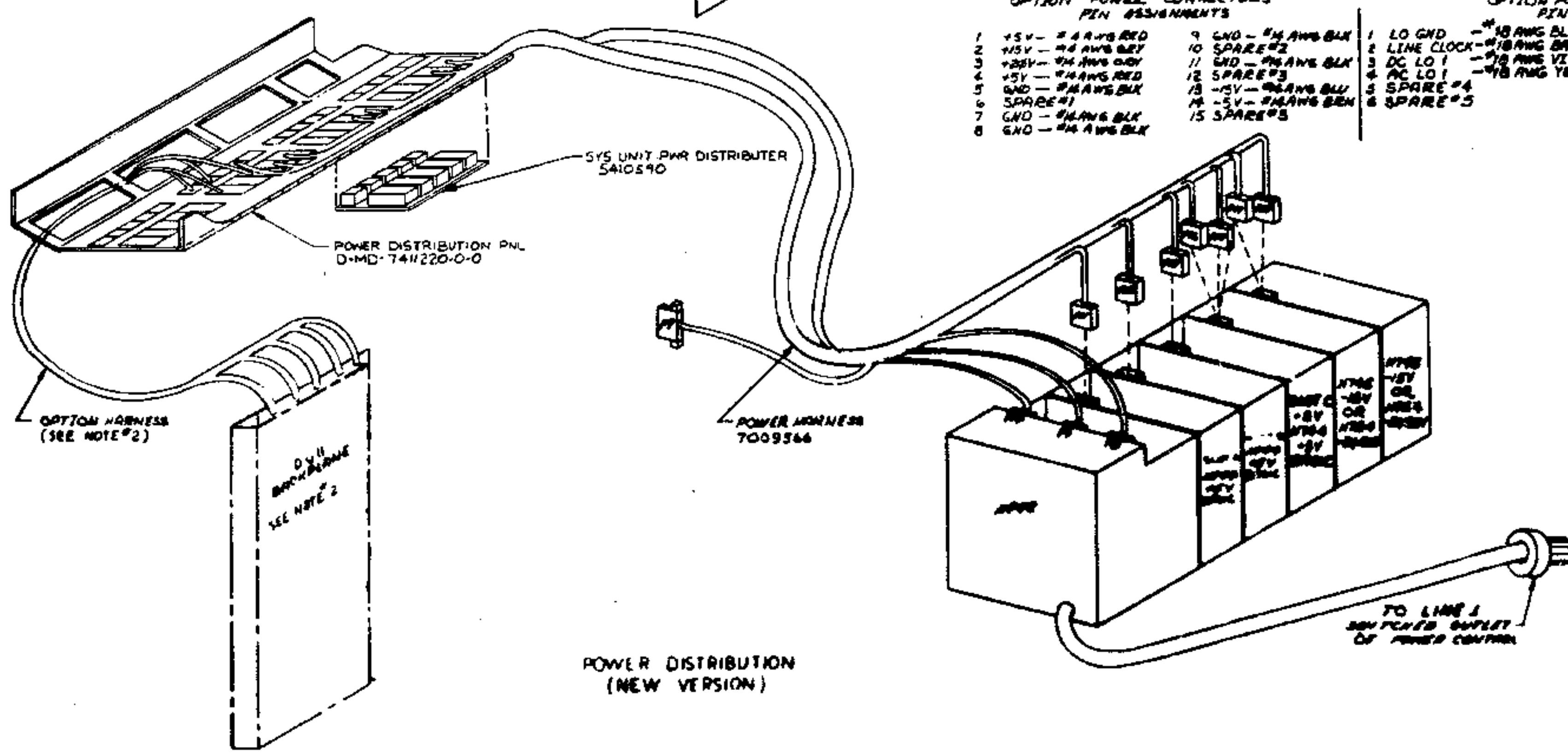
1	+5V — #14 AWG RED	9	GND — #14 AWG BLK
2	+15V — #14 AWG GRY	10	SPARE #2
3	+20V — #14 AWG ORN	11	GND — #14 AWG BLK
4	+5V — #14 AWG RED	12	SPARE #3
5	GND — #14 AWG BLK	13	-15V — #14 AWG BLU
6	SPARE #1	14	-5V — #14 AWG BRN
7	GND — #14 AWG BLK	15	SPARE #5
8	GND — #14 AWG BLK		

1	LO GND — #18 AWG BLK
2	LINE CLOCK — #18 AWG BRN
3	DC LO 1 — #18 AWG VIO
4	AC LO 1 — #18 AWG YEL
5	SPARE #4
6	SPARE #5

WIRING SIDE

OPTION POWER CONNECTORS PIN ASSIGNMENTS

1	+5V — #14 AWG RED	9	GND — #14 AWG BLK
2	+15V — #14 AWG GRY	10	SPARE #2
3	+20V — #14 AWG ORN	11	GND — #14 AWG BLK
4	+5V — #14 AWG RED	12	SPARE #3
5	GND — #14 AWG BLK	13	-15V — #14 AWG BLU
6	SPARE #1	14	-5V — #14 AWG BRN
7	GND — #14 AWG BLK	15	SPARE #3
8	GND — #14 AWG BLK		



POWER DISTRIBUTION
(NEW VERSION)

FIRST USED ON OPTION/MODEL	QTY	DESCRIPTION	PART NO.	ITEM NO.
PDP11	PARTS LIST			

UNLESS OTHERWISE SPECIFIED DIMENSIONS IN INCHES
TOLERANCES: DECIMALS .XXX ± .005, .XX ± .02, .X ± .1; ANGLES ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY
MATERIAL —
FINISH —

DRN / CHK'D / ENG / PROJ ENG / PROD — DATE 4-23-75

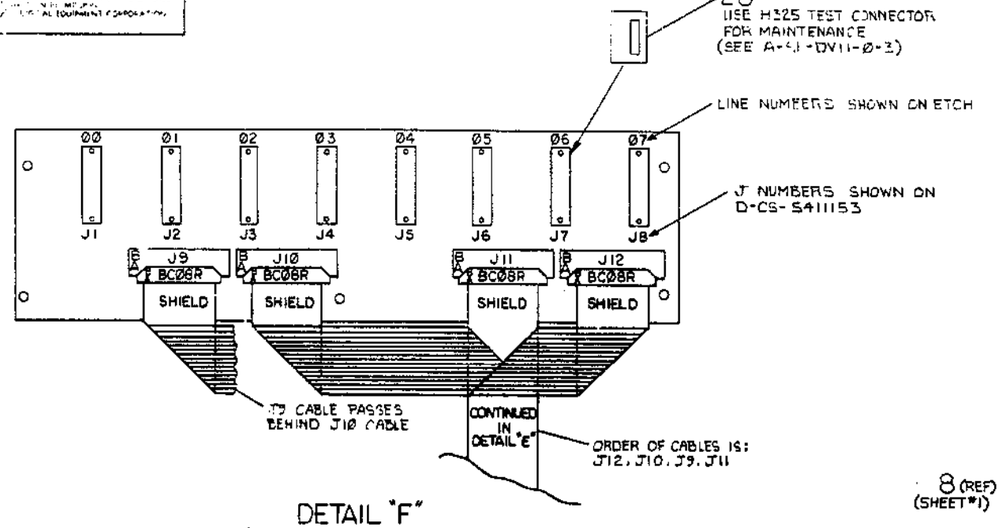
NEXT HIGHER ASSY: B-DD-DV11-Ø

SCALE —
SHEET 4 OF 4

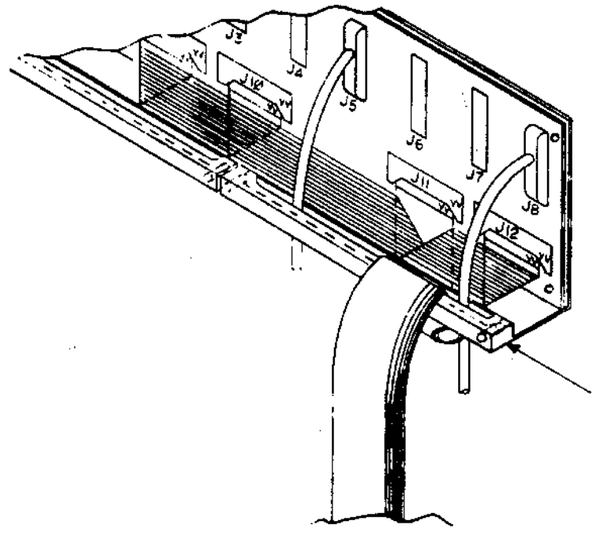
digital EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: **BASIC ASSY DV11**

SIZE D | CODE UA | NUMBER DV11-Ø-Ø | REV.



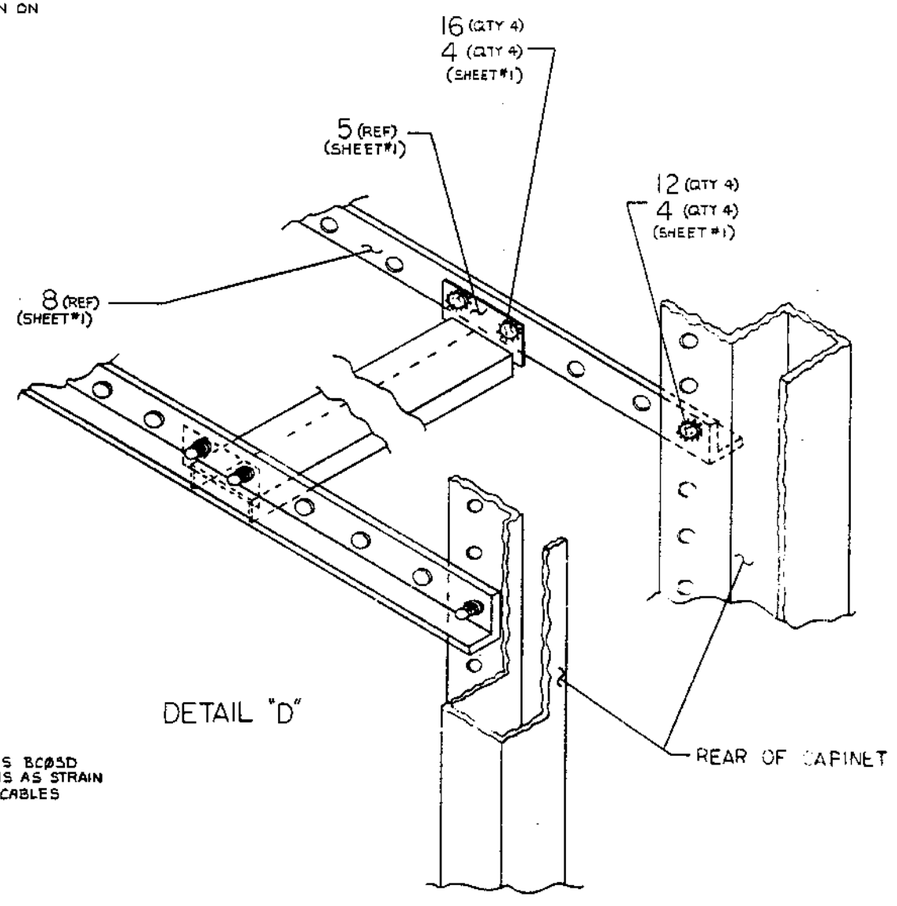
DETAIL "F"



CABLE CLAMP SECURES BC03D CABLES AND FUNCTIONS AS STRAIN RELIEF FOR BC08R CABLES

DETAIL "E"

(CONTINUED FROM DETAIL "F")



DETAIL "D"

REVISIONS

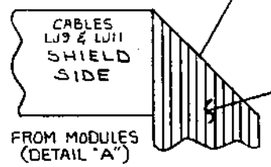
CHK	CHANGE NO.	REV

TITLE	BASIC ASSY DV11	SIZE D	CODE UA	NUMBER DV11-0-0
SCALE	NONE	SHEET 7 OF 9	DIST	REV.

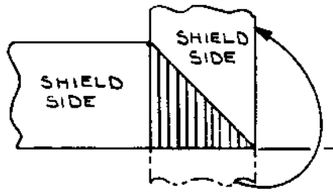
DUA DV11-0-0

FOLD LJ9 & LJ11 TOGETHER AS ONE CABLE

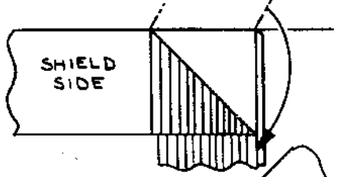
STEP #1



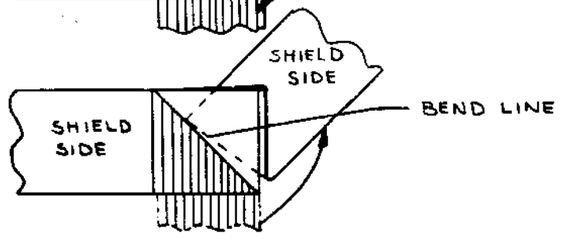
STEP #2



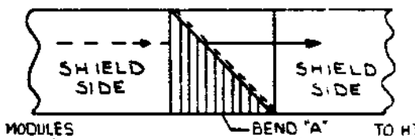
STEP #3



STEP #4

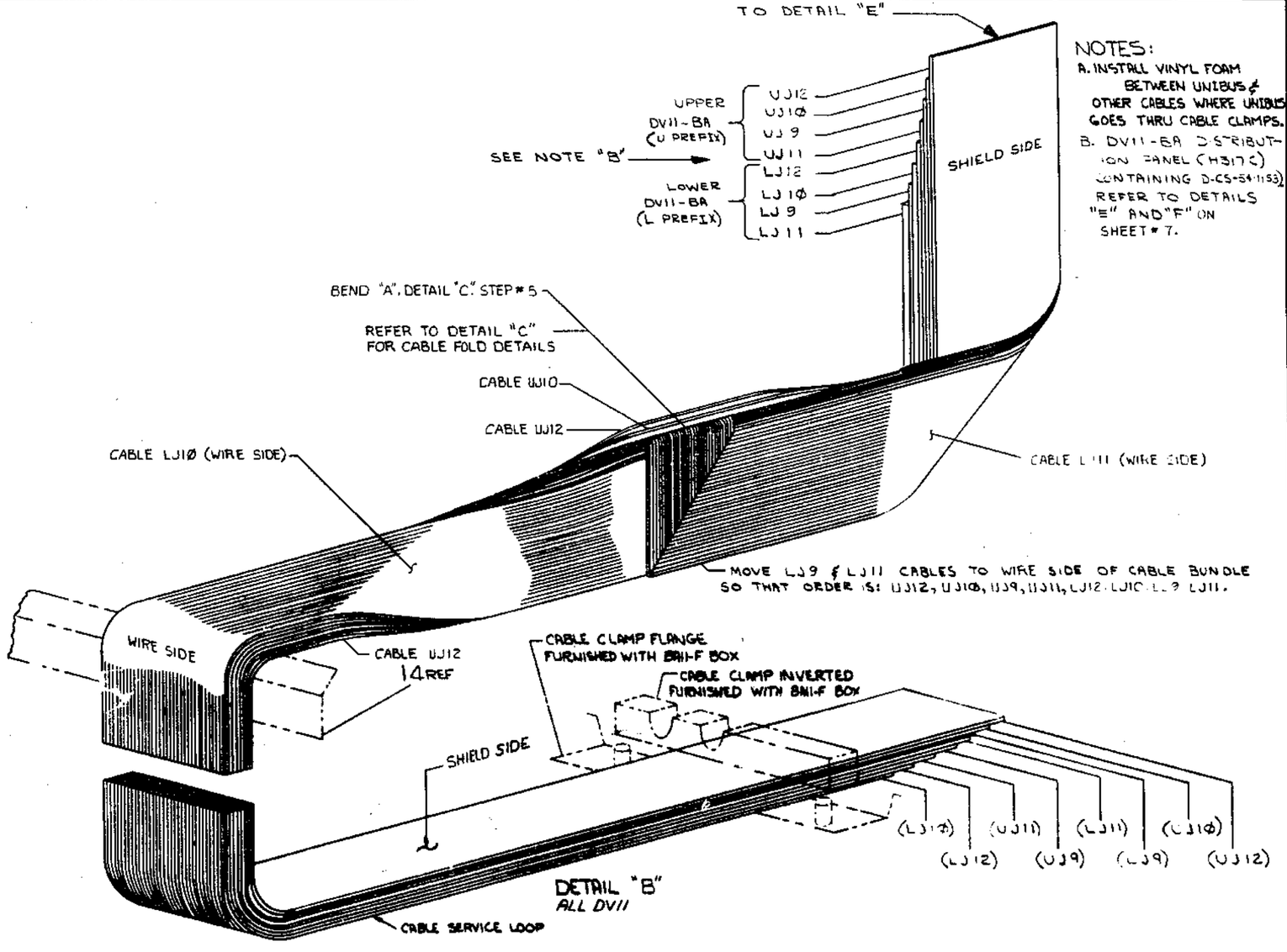


STEP #5



DETAIL "C"

NOTE THAT UJ9, UJ11, LJ12, LJ10 CABLES CAN PASS THROUGH THE FOLDED AREA AS SHOWN BY DOTTED ARROW AND SOLID ARROW. NOTE THAT FOLDED CABLE IS INSTALLED IN DETAIL "B" UPSIDE DOWN FROM VIEW SHOWN IN DETAIL "C" - REFER TO POSITION OF BEND "A".



DETAIL "B"
ALL DV11

NOTES:

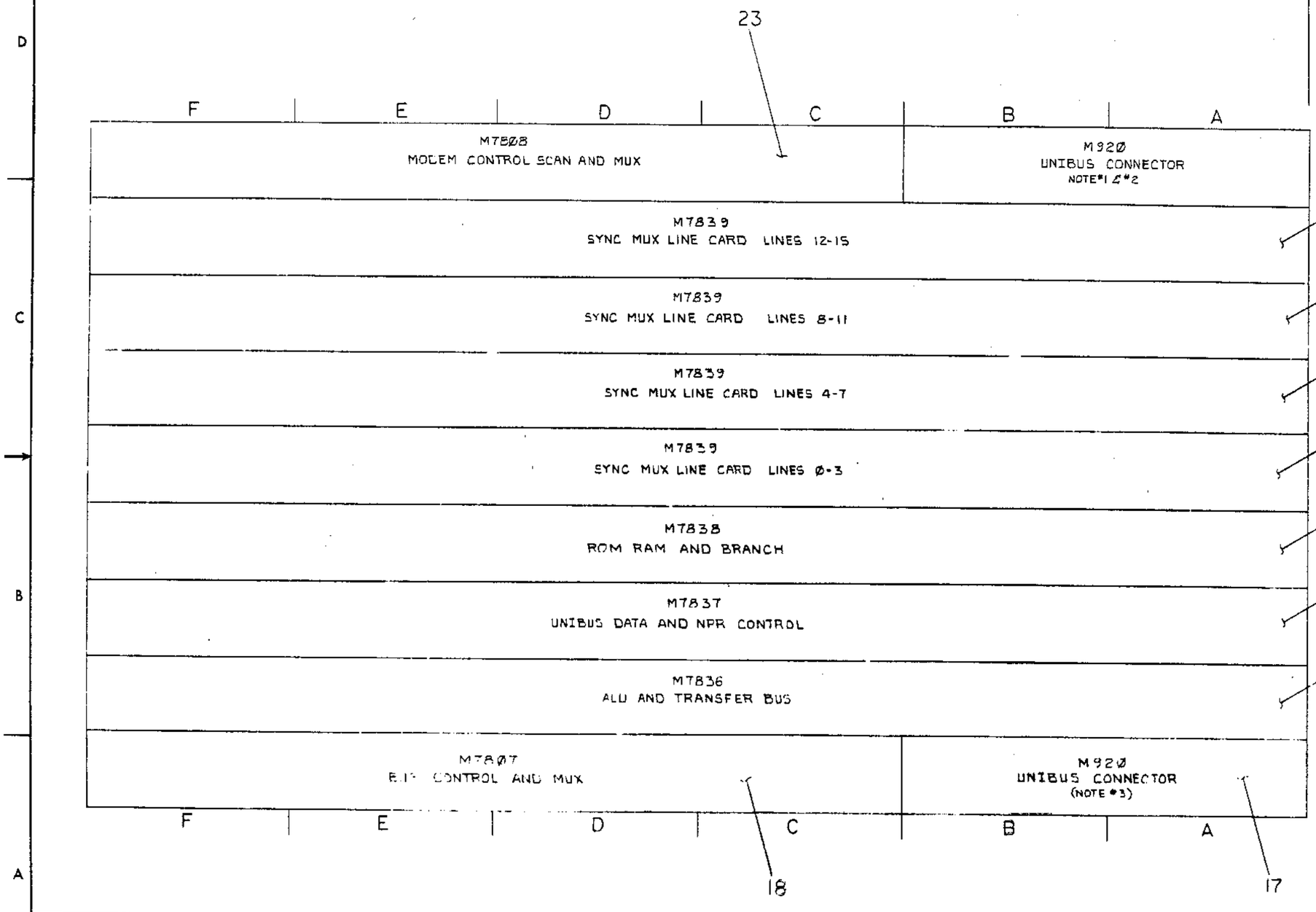
A. INSTALL VINYL FOAM BETWEEN UNIBUS & OTHER CABLES WHERE UNIBUS GOES THRU CABLE CLAMPS.

B. DV11-BA DISTRIBUTION PANEL (H317C) CONTAINING D-CS-54-11153) REFER TO DETAILS "E" AND "F" ON SHEET # 7.

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	BASIC ASSY. DV11	SIZE	CODE	NUMBER	REV.
SCALE NONE	SHEET 6 OF 9	D	UA	DV11-Ø-Ø	
		DIST.			

VIEW FROM SLOT SIDE



NOTES:

1. IF END OF BOX REPLACE M920 WITH M930.
2. IF LAST UNIT IN BASIC BOX REPLACE M920 WITH BC11A CABLE END WHEN EXPANDING TO PHERIPHERAL BOX.
3. IF FIRST UNIT IN EXPANDER BOX REPLACE M920 WITH BC11A CABLE END.
4. TWO M7839 CARDS ITEM# 22 ARE LOCATED IN SLOTS 5 & 6 FOR FIRST DV11-BA; FOR SECOND DV11-BA LOCATE TWO MORE M7839 CARDS TO SLOTS 7 & 8.

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV.
BASIC ASSY DV11	D	UA	DV11-0-0	
SCALE —	SHEET 9 OF 9	DIST.		

VECTORS:

OCTAL TO SWITCH POSITION CONVERSION - M7837

VECTORS

	8	7	6	5	4	3	2	
	1	2	3					
300	ON	OFF	OFF	ON	ON	ON	3	*VECTOR BIT 2 IS CONTROLLED BY DV11 LOGIC
304	ON	OFF	OFF	ON	ON	ON	4	
310	ON	OFF	OFF	ON	ON	OFF	*	
314	ON	OFF	OFF	ON	ON	OFF	*	
320	ON	OFF	OFF	ON	OFF	ON	*	
324	ON	OFF	OFF	ON	OFF	ON	*	
330	ON	OFF	OFF	ON	OFF	OFF	*	
334	ON	OFF	OFF	ON	OFF	OFF	*	
340	ON	OFF	OFF	OFF	ON	ON	*	
350	ON	OFF	OFF	OFF	ON	OFF	*	
364	ON	OFF	OFF	OFF	OFF	ON	*	
370	ON	OFF	OFF	OFF	OFF	OFF	*	
400	OFF	ON	ON	ON	ON	ON	*	
410	OFF	ON	ON	ON	ON	OFF	*	
420	OFF	ON	ON	ON	OFF	ON	*	
430	OFF	ON	ON	ON	OFF	OFF	*	

OCTAL TO JUMPER CONVERSIONS FOR M7807

VECTORS

	8	7	6	5	4	3	2
	1	5	4	6	7	3	7
300	OUT	IN	IN	OUT	OUT	OUT	OUT
304	OUT	IN	IN	OUT	OUT	OUT	IN
310	OUT	IN	IN	OUT	OUT	IN	OUT
314	OUT	IN	IN	OUT	OUT	IN	IN
320	OUT	IN	IN	OUT	IN	OUT	OUT
324	OUT	IN	IN	OUT	IN	OUT	IN

330 OUT [illegible]

410 IN OUT OUT OUT IN OUT

ADDRESSES.

M7836

DV11 DATA CONTROL ADDRESS OFF-1, ON-0

BITS 9,11,12 ARE OFF

BIT 10 IS ON

		8	7	6	5	4
775	000	ON	ON	ON	ON	ON
	040	ON	ON	ON	OFF	ON
	100	ON	ON	OFF	ON	ON
	140	ON	ON	OFF	OFF	ON

M7807

DV11 MODEM CONTROL ADDRESS OUT-1, IN-0

BITS 9,11,12 ARE OUT

BIT 10 IS IN

		8	7	6	5	4	3
775	020	IN	IN	IN	IN	OUT	IN
	060	IN	IN	IN	OUT	OUT	IN
	120	IN	IN	OUT	IN	OUT	IN
	160	IN	IN	OUT	OUT	OUT	IN

PDP 11 BIT TO OCTAL DIGIT CORRESPONDANCE

BIT	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EXAMPLE	1	1	1	1	1	1	1	0	1	0	0	0	1	0	0	0	0	0
OCTAL DIGIT	6TH			5TH			4TH			3RD			2ND			1ST		
EXAMPLE	7			7			5			0			0			0		

NOTE I/O DEVICE ADDRESS IN #11 LITERATURE ARE VARIOUSLY GIVEN AS 760 000 THRU 777 777 AND AS 160 000 THRU 177 777 THESE ARE EQUIVALENT IN MACHINES WITHOUT MEMORY MANAGEMENT. WHENEVER BITS 15,14, AND 13 ARE ALL "1" (16X XXX OR 17X XXX) THE PROCESSOR ALSO MAKES BITS 17 AND 16 "1" (76X XXX OR 77X XXX) [ON MACHINES WITH MEMORY MANAGEMENT I/O DEVICE ADDRESSES ARE IN PHYSICAL MEMORY AT 760 000 THRU 777 777. THEY ARE ONLY AVAILABLE TO A PROGRAM IF SOME VIRTUAL ADDRESS AREA IS MAPPED INTO THIS PHYSICAL AREA]

JUMPERS AND MODIFICATIONS

BR LEVEL SELECT BOARD - M7837

BR PLUG SHOULD BE 5400778 (LEVEL #5)

(AS SUPPLIED STANDARD)

OUT 126

REVISIONS		
CHK	CHANGE NO	REV

TITLE [illegible]

SIZE D | CODE | NUMBER DUA11-K-X | REV.

SCALE - | SHEET 5 OF 5 | DIST

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE May 17,1974

TITLE DV11 Communications Multiplexor

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A	ECO CHANGE	00001	J.McNAMARA	5-75		

ENG	APPD	SIZE	CODE	NUMBER	REV
	5-23	A	SP	DV11-0-1	A

DEC 16-(392)-1079-N971
DRA 107

General Description

The DV11 is a sixteen line synchronous multiplexor for the PDP-11 family of computers.

The DV11 is designed to achieve very high throughput (16 lines times 1200 characters per second times two directions equals 38,400 characters per second) by use of NPR transfers on both transmission and reception. The use of control bytes stored in core tables makes the DV11 essentially a classical state machine and permits it to achieve hardware throughput capabilities without committing the hardware design to any specific protocol.

The DV11 is housed in a nine slot double system unit and includes a distribution panel for each eight line group and a complete sixteen line modem control identical to the DM11-BB modem control, but with Data Set Ready and New Sync substituted for Secondary Receive and Secondary Transmit respectively.

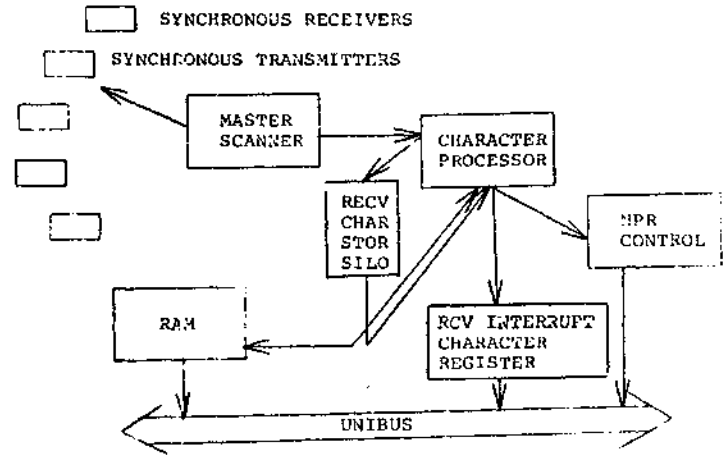


Figure 1: Block Diagram of DV11

The basic elements of the DV11 are shown in figure 1.

The Synchronous Receivers (16) assemble characters received from serial communications lines and assert a flag as each character is received. The Synchronous Transmitters (16) disassemble characters and transmit them on serial communications lines and assert a flag whenever they can accept another character for transmission.

The Master Scanner sequentially checks the Synchronous Receivers and Synchronous Transmitters for each line to see if flags exist.

The Character Processor is a ROM controlled microprocessor which handles all characters received or transmitted by the DV11. It controls all non-Unibus data transfers and steps the Master Scanner. Except for those occasions where a Unibus instruction or NPR transfer involving the DV11 is taking place, the microprocessor never stops.

The Received Character Storage Silo is a first-in, first-out storage buffer. While most characters received by the DV11 will propagate through this buffer and be directly transferred to PDP-11 core by means of an NPR transfer, the occasion may arise when the attention of the PDP-11 program is required before this is done in the case of a particular character. To prevent the Synchronous Receivers from experiencing data overruns during the interval that the DV11 is awaiting program attention, the microprogram will continue to load the received characters into the first-in first-out buffer, but the action of the Character Processor in withdrawing characters from the buffer will cease until the PDP-11 program responds to the interrupt caused by the special character at the bottom of the silo buffer. The character which requires PDP-11 program attention is copied into the Next Received Character Register at the time the aforementioned interrupt is generated.

The Next Received Character Register is a Unibus addressable register used by the microprogram to show the PDP-11 program any received character, along with line number and error flags, for which the microprogram requires assistance in processing.

The NPR Control is the hardware which the microprogram uses to gain control of the Unibus in order to store received characters, obtain characters for transmission, and obtain control bytes that direct the character processing.

The RAM contains the current addresses and byte counts used in the aforementioned NPR transfers. The initial values are loaded by the PDP-11 program via the Unibus and these values are subsequently updated by the microprogram. The RAM also contains a line protocol byte for each line by which the PDP-11 program can specify what action is to be taken when the byte count reaches zero and what type of block check polynomial should be used. In addition, a line state byte is stored for each line providing a snapshot of what microprogram activity is in progress on a particular line.

Operation

The Master Scanner checks both Synchronous Receivers and Synchronous Transmitters for flags indicating that characters are to be read from them (receivers) or loaded into them (transmitters).

If the Master Scanner finds a receiver flag, the microprocessor performs a data transfer operation reading a character from that Synchronous Receiver and loading it into the Received Character Storage Silo.

If the Master Scanner finds a transmitter flag, the microprocessor utilizes the NPR Control to obtain a character from core and to obtain a control byte from core. The control byte contains information regarding any special treatment the character is to receive during transmission. After any such treatment, the microprocessor loads that character into that Synchronous Transmitter for transmission.

In addition to servicing Synchronous Receiver flags and Synchronous Transmitter flags, the microprocessor also retrieves characters from the Received Character Storage Silo. As removed from the character storage silo, each character is accompanied by its line number and error flags.

If any of the error flags are set, the microprocessor places the character in the Receiver Interrupt Character Register and generates an interrupt. If there are no error flags set, the microprocessor appends "Mode bits*" to the high order end of the character and uses the resultant expanded character as an offset in a core table from which a control byte appropriate to that character and mode is retrieved. The control byte indicates whether or not an interrupt should be generated (i.e., special character), whether or not the character should be included in the block check character calculation, whether or not the character should be stored in the core message table for that line, and whether or not the "mode bits" for that line should be changed. In those cases where the microprocessor deposits a character in the Receiver Interrupt Character Register (either because of error flags or as a result of information in the control byte), no further action** is taken by the microprocessor in retrieving characters from the received character storage silo until so directed by the setting of System Control Register bit Ø8 - Receiver Interrupt Response Complete.

The details of DV11 operation are best understood by reference to the register bit explanations which follow.

*Mode bits are always loaded into bits Ø8, Ø9, and 1Ø. Thus, the core tables containing the mode bytes always contain 256 bytes for each mode - i.e., all received characters are treated as 8-bit characters.

**If the program is too tardy in servicing the Receiver Interrupt Character Register, the silo will overflow - See System Control Register (address XØØ) bit 14.

System Control Register - Address XØØ

The System Control Register is a byte addressable register. The bit assignment is as follows:

Bit	Description

ØØ Microprocessor

This bit when set permits the DV11 to cycle the Microprocessor that controls the DV11. This is read/write, CLEARED by Initialize. System programs must set this bit for the DV11 to function.

Ø1 ROM Single Step (For Maintenance Use)

This bit permits the PDP-11 program to execute one ROM cycle (only). This bit is read/write, cleared by Initialize. When the ROM cycle begins, this bit is automatically cleared.

Ø2 ROM Branch Disable (For Maintenance Use)

This bit when set assures that the DV11 microcode will not branch if the ROM cycles to a branch instruction while this bit is set. This bit is read/write, cleared by Initialize.

Ø3 ROM Data Source Select (For Maintenance Use)

This bit when set enables the ROM Data Register (a microprocessor register) to be loaded from the Unibus by doing a write into the Special Functions Register (address X12). This bit is read/write, cleared by Initialize.

Ø4-Ø5 Memory Extension

The information stored in these bits becomes bits 16 and 17 respectively of any current address or control table base address loaded by the program into the RAM. These bits are read/write (cleared by Initialize) but when read, represent only the status of bits 4 and 5 of the System Control Register, not the status of address bits 16 and 17 of the selected line. See the Line Control Register for further information. This arrangement permits interrupt service routines to save the contents of the System Control Register accurately.

Ø6 Receiver Interrupt Enable

This bit, when set, permits the setting of bit 7 to generate an interrupt request. RW Init. clears.

Ø7 Receiver Interrupt (Vector A)

This bit, when set, indicates that the microprocessor has either (1) withdrawn a byte from a core control table indicating that an interrupt should be generated for the character presently being processed, or (2) the character presently being processed has one or more of its associated error flags set or (3) experienced a zero byte count, non-existant memory location, or memory parity error in processing this characater. The program should respond to this interrupt by setting SCRØ8. (The program might wish to alter the Control Byte Storage Register before setting SCRØ8.) This bit is read only except when SCRØ9 is set. It is cleared by Initialize.

Ø8 Receiver Interrupt Response

The setting of this bit clears SCRØ7 and allows the microprocessor to take action on the character in the RICR (according to the information stored in the Receiver Control Byte Storage Register) and to continue removing characters from the receive silo for processing.

Ø9 Bit 7 & 15 Write Enable (Maintenance)

This bit, when set, permits the program to write bits 7 and 15 of this register. This bit is read/write, cleared by Initialize. This register must be word addressed when and while this bit (SCRØ9) is set.

1Ø NPR Status Overflow Interrupt

This bit, when set, indicates that the DV11 hardware checked the NPR status register (a silo) and found that there was no room due to insufficient program attention to servicing this register. All DV11 transmitter action in performing NPR trasnfers will cease until this condition is corrected. This bit is read/write, cleared by Initialize.

11 Master Clear

This bit, when set, generates "Initialize" within the DV11 data handling sections (It does not affect the modem control.). The silos (both received character and NPR status*) are cleared. The secondary registers are not cleared. This bit is read/write and is self-clearing.

12 Storage Interrupt Enable

This bit, when set, permits the setting of bit 1Ø to generate an interrupt request. Read/write, cleared by Initialize.

13 NPR Status Interrupt Enable

This bit, when set, permits the setting of bit 15 to generate an interrupt request. This bit is read/write, cleared by Initialize.

14 Unused

15 NPR Status Interrupt (Vector B)

This bit is set whenever there is one or more entries in the NPR Status Register, which is a silo-type register. The reading of that read-once register clears this bit, but it resets again if a new entry moves down into the register to replace the previously read entry. This bit is read only except when SCRØ9 is set, when it is read/write. This bit is cleared by Initialize

*The NPR Status Register Bit 15 ("Entry Present") is cleared by Initialize; the other bits are not.

Receiver Interrupt Character Register - Address X∅2

This register is read only, cleared by Initialize.

Bits	Description
∅∅-∅7	Interrupting Character These bits contain the interrupting character, right justified. The least significant bit is bit ∅∅. On parity-equipped characters, less than 8 bits, the parity bit will appear immediately to the left of the highest order bit in the character. See special note associated with Error Code 0101 below.
∅8-11	Line Number The bits indicate the line number on which the interrupting character was received. Bit 8 is the least significant bit.
12-15	Error Code These bits indicate the reason that the character shown in bits ∅∅-∅7 generated an interrupt request. Refer to Chart.

Error Code Bit				Meaning
15	14	13	12	
0	0	0	0	SPECIAL CHARACTER The receipt of this character caused the seizure of a control byte which had bit ∅∅ (generate interrupt) set indicating that this is a special character.
0	0	0	1	PARITY ERROR This character was received with a parity sense opposite to that selected for this line by the parity sense switches on the line card.
0	0	1	0	OVERRUN The character(s) preceding this character on this line has (have) been lost due to failure of the DV11 receiver system to keep up with the incoming character rate on this line.

Error Code Bit				Meaning
15	14	13	12	
0	0	1	1	PARITY ERROR AND OVERRUN (see previous listings)
0	1	0	0	BYTE COUNT WARNING This character has been stored, but it is the last character that can be stored for this line as the byte count is now zero for reception on this line.
0	1	0	1	BLOCK CHECK COMPLETED A block of text or data and the associated block check characters have been received and the program should now check the accumulated receiver block check; the DV11 presents the OR of the high and low bytes of that register in bits ∅∅-∅7 of this register.
0	1	1	0	UNDEFINED
0	1	1	1	UNDEFINED
1	0	0	0	BYTE COUNT ZERO This character was not stored, as the byte count for reception on this line is zero and thus there is no place to store this character.
1	0	0	1	UNDEFINED
1	0	1	0	UNDEFINED
1	0	1	1	UNDEFINED
1	1	0	0	PROCESSING ERROR ∅∅ A nonexistant memory time-out occurred when the DV11 attempted to store this character.
1	1	0	1	PROCESSING ERROR ∅1 A nonexistent memory time-out occurred when the DV11 attempted to obtain the control byte associated with this character.
1	1	1	0	PROCESSING ERROR 1∅ A memory parity error occurred when the DV11 attempted to store this character. (NOTE: this error should never occur, as the memory parity logic gives alarms only on DATO transfers).
1	1	1	1	PROCESSING ERROR 11 A memory parity error occurred when the DV11 attempted to obtain the control byte associated with this character.

In response to a receiver interrupt (SCR∅7), the PDP-11 Program should examine this register (Receiver Interrupt Character Register), make any desired changes in the Receiver Control Byte Storage Register, and then set SCR∅8.

Line Control Register - Address ∅4

This register controls the maintenance features associated with each line in the DV11 and provides an opportunity for the PDP-11 program to read the extended address bits for each line.

The following bits are read only and may be read only after the appropriate bits in the Secondary Register Selection Register have been conditioned to select the appropriate secondary register for the appropriate line: ∅4, ∅5, and ∅7.

The following bits are read/write, but the read is only a read of the most recently written entry into this bit of this register, not a read of the status of this bit for this line (This is referred to as "write/limited read".). A write into one of these bits does not affect the selected line unless bit 15 is also set: ∅8, ∅9, 1∅, 11, 12, 13, and 14. An example will clarify this. The PDP-11 program can read and write LPR 13 (Receiver Enable) at any time, but reading will only tell the program whether or not LPR 13 is set, not whether or not a particular line's receiver is enabled or not. In addition, the line specified in Secondary Register Selection Register bits ∅∅-∅3 will not be placed in Receiver Enable mode merely by the writing of bit 13 of the LPR. Rather, the line will be placed in Receiver Enable mode only when bit 15 is set in addition (or subsequent to) bit 13 being set.

The line number to which the maintenance information, search sync, or extended address applies is specified by bits ∅∅-∅3 of the Secondary Register Selection Register.

The bit functional assignments are as follows:

∅∅-∅1 Reserved for Maintenance
(Caution: Various bits may appear here during normal DV11 operation.)

∅2-∅3 Unused

∅4 ∅5 Extended Address Read (Read Only)

For the line number entered in bits ∅∅-∅3 of the Secondary Register Selection Register these bits represent the status of bits 16 and 17 of the secondary register specified by bits ∅8-11 of the Secondary Register Selection Register. This permits the PDP-11 program to read the Extended Address bits of the Current Address and Control Table Base Address entries in the RAM.

∅6 Unused

∅7 Maintenance Bit Window (Maintenance)

When in the maintenance mode ∅1 only, this bit can be used to monitor the input to the receiver logic of the selected line. The stimulus that creates the input could be either the maintenance Data bit or the serial output of the transmitter, depending on the state of the Transmitter Disable bit. Program read only. This bit does not represent the status of the selected line.

∅8 Maintenance Clock Pulse (Maintenance) (See Bit 15)

This bit is used to simulate the Transmitter and Receiver Clock. It is used for diagnostic purposes only. With this bit, the diagnostic has the ability to single step the interface. Setting this bit causes the transmitter to transfer a bit from the internal shift register to the output of the transmitter and causes the receiver to transfer the input of the receiver into the internal shift register.

This bit is program write only and is self-clearing. It pulses all DV11 lines that are in maintenance mode ∅1.

∅9 Transmitter Disable (Maintenance) (See Bit 15)

This bit, when set, disables the output of this line's Synchronous Transmitter. In this way data from the Maintenance Data bit may be entered into the receiver. This bit is used only for maintenance purposes and is write/limited read.

11 & 12 Maintenance Mode Select (See Bit 15)

These bits are used to select any one of the three maintenance modes:

	BIT SETTING 12	11
1. Internal Maintenance Mode	0	1
2. External Maintenance Mode	1	0
3. Internal Maintenance Mode for Systems Testing	1	1
4. Normal Operation	0	0

Internal Maintenance Mode (Ø1)

Internal Maintenance Mode clocking comes from the Maintenance Clock Pulse bit (bit Ø8) driven via the program. While using this mode, the following EIA level converters are disabled (This is done so that the majority of the logic can be diagnosed without disconnecting the modem cable.):

Receiver Clock
Transmitter Clock
Receiver Data
Transmitter Data

Transmitted data is looped to received data on a TTL basis.

External Maintenance Mode (1Ø)

When in the external maintenance mode, all lines connected to the data set must be removed at the data set interface. A special connector replaces the connector of the data set. The function of the special connector is to turn around specified signals after level conversion and bring them back to the DV11 as simulated inputs.

Clocking in this mode is under control of internal DV11 clocks in the same way as Internal Maintenance Mode 11.

Internal Maintenance Mode for Systems Testing (11)

With bits 12 and 11 both set to a one (mode 11), the internal maintenance mode provides internal clocking for the receiver and transmitter. The clocking rate is controlled by switches on the DV11 line cards. Mode 11 will be the same as mode Ø1 with respect to data set control leads and TTL data loopback. The only difference is that in mode 11 the receiver and transmitter clocking is derived from internal clocks.

Bits 11 and 12 are write/limited read.

NOTE: If bits 12 and 11 are zero, normal operating mode is assumed.

13 Receiver Enable (See bit 15)

When this bit is set by the program, a sync search is initiated on this line by the receiver logic. After an initialize, this bit must be set by the program before any reception can begin on this line - i.e., Receiver Active (See "Line State" secondary register) will not set unless this bit has been set.

A switch for each line determines whether the receiver searches for one sync character or for two in a row.

A successful sync search results in the setting of Receiver Active (Line State Bit ØØ) for this line.

This bit is write/limited read.

NOTE: Should it be desired to resynchronize during the course of reception, the program could accomplish this by setting "Receiver Resynchronize" (Line State Ø1). To shut down reception on a line, the program should clear Receiver Enable and then set Receiver Resynchronize.

14 Maintenance Data (Maintenance) (See Bit 15)

This bit is used only in the maintenance mode by the diagnostic program. In maintenance mode Ø1 this bit can be used to simulate data at the receiver input. When used as a simulated input to the receiver, the Transmitter Disable bit must be set to inhibit additional input from the transmitter. This bit should be cleared if it is not being used as the simulated input. If this bit were inadvertently set in maintenance mode and the transmitter Disable bit was clear, the receiver input would have two sources of input. This bit is write/limited read.

15 Maintenance Conditions Strobe (Maintenance)

The setting of this bit records the status of bits Ø8, Ø9, 1Ø, 11, 12, 13, and 14 into the status flip-flops associated with the line specified in bits ØØ-Ø3 of the Secondary Register Selection Register. This bit is self-clearing, hence write only. It may be set at the same time as the bits whose status it records, as its action is delayed until the conclusion of the instruction cycle which set it. This bit is necessary due to "Reads" in the PDP-11/20 being "read-write" cycles, and certain synchronization requirements associated with mode changes during clocking pulses.

[illegible]condary Register Selector - Address XØ6

The bits in this register provide a path for the program to access the various locations in the DV11 RAM. The program may read or write these locations. The various locations may be thought of as registers.

Interrupt service routines must save the contents of this register so that no changes occur between the setting of bits in this register and the reading or writing of the Secondary Register Access Register - Address X1Ø.

The bit assignments of the Secondary Register Selector Register are as follows:

Bit	Description
ØØ-Ø3	Line Selection For each type of register selected by bits Ø8-11, there are 16 registers - one per line. The setting of the Line Selection bits determines exactly which of these line registers is to be addressed.
Ø4-Ø7	Unused
Ø8-11	Register Selection These bits determine which type of register is addressed for the line number specified in bits ØØ-Ø3.

Bits

11	10	9	8	
0	0	0	0	Transmitter Primary Current Address
0	0	0	1	Transmitter Primary Byte Count
0	0	1	0	Transmitter Secondary Current Address
0	0	1	1	Transmitter Secondary Byte Count
0	1	0	0	Receiver Current Address
0	1	0	1	Receiver Byte Count
0	1	1	0	Transmitter Accumulated Block Check
0	1	1	1	Receiver Accumulated Block Check
1	0	0	0	Transmit Control Table Base Address

Bits

11	10	9	8	
1	0	0	1	Receiver Control Table Base Address
1	0	1	0	Line Protocol Parameters
1	0	1	1	Line State
1	1	0	0	Transmitter Mode Bits
1	1	0	1	Receiver Mode Bits
1	1	1	0	Line Progress
1	1	1	1	Receiver Control Byte Storage Register

Secondary Registers

These registers are selected by conditioning bits in the Secondary Register Selector Register (Address XØ6) and then reading or writing into the Secondary Register Access Register (Address X1Ø).

NOTE: The Secondary Registers are NOT cleared by Initialize.

0000 Transmitter Principal Current Address

The Transmitter Principal Current Address secondary register contains the 18-bit core memory address of the next character to be transmitted on the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State secondary register bit 07 set to zero).

0001 Transmitter Principal Byte Count

The transmitter Principal Byte Count secondary register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission based on reaching a zero byte count during transmission. When bit 15 is set to zero by the PDP-11 program, bits 13-15 of the Line Progress secondary register for this line will control the transmission mode when the principal byte count reaches zero; also, the BCC will be transmitted if Line Progress bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00-02 of the Transmitter Mode Bits secondary register continue to control the line transmission mode. A byte count with bit 15 set to zero (at the time the byte count is loaded by the PDP-11 program) is referred to as a "marked" byte count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State 07 set to zero). When this register reaches zero, transmission continues using the transmitter alternate byte count for this line, if the Transmitter Go bit in the Line State secondary register is still set to one.

0010 Transmitter Alternate Current Address

The Transmitter Alternate Current Address register has exactly the same function as the Transmitter Principal Current Address register (0000). This register is incremented by one with each character transmitted by the DV11 on the associated line if the alternate message table is being used (line State secondary register bit 07 set to one).

0011 Transmitter Alternate Byte Count

The transmitter Alternate Byte Count secondary register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission based on reaching a zero byte count during transmission in the same fashion as described for Transmitter Principal Byte Count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the alternate message table is being used (line State secondary register bit 07 set to one). When this register reaches zero, transmission continues using the

transmitter principal byte count for this line if the Transmitter Go bit in the Line State secondary register is still set to one.

0100 Receiver Current Address

The Receiver Current Address register contains the 18-bit core memory address for storage of the next character to be received on the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. This register is incremented by one with each character received on the associated line by the DV11.

0101 Receiver Byte Count

The Receiver Byte Count secondary register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be received on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC anticipation based on reaching a zero byte count during reception. When bit 15 is set to zero by the PDP-11 program, bits 13-15 of the Line State secondary register for this line will control the reception mode when the byte count reaches zero; also, the BCC will be expected if Line State bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00-02 of the Receiver Mode Bits secondary register continue to control the line reception mode. When this register reaches zero, an interrupt code is set in the Receiver Interrupt Character register and the DV11 stops transferring received characters to core memory.

0110 Transmitter Accumulated Block Check Character

The Transmitter Accumulated Block Check secondary register contains the continuously computed block check character specified by the Line Protocol Parameters secondary register to enable destination stations to check integrity of transmission on the associated line. Characters to be included in the

block check calculation are specified by bit 03 of the transmitter control bytes for each character. The contents of this register are transmitted as two sequential bytes, low-order eight bits first, except when LRC-8 is the selected block check type, in which case a single byte is transmitted. The DV11 automatically clears this register to zero after transmitting its contents.

NOTE

The DV11 computes CRC-16 and CRC-CCITT on a byte at a time basis (parallel), thus the character length must be eight bits. LRC-8 may be selected for characters of 5, 6, 7, or 8 bits.

0111 Receiver Accumulated Block Check Character

The Receiver Accumulated Block Check secondary register contains the continuously computed block check character specified by the Line Protocol Parameters secondary register for checking integrity of data received on the associated line. Characters to be included in the block check calculation are specified by bit 03 of the receiver control byte for that character. The PDP-11 program should clear this register if the accumulated block check at the end of the message is non-zero.

1000 Transmitter Control Table Base Address

The transmitter Control Table Base Address secondary register contains the 18-bit address of the transmitter control table for the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. The contents of this register are used by the microprocessor in the computation of the control byte addresses for transmitted characters.

1001 Receiver Control Table Base Address

The Receiver Control Table Base Address secondary register contains the 18-bit address of the receiver control table for the associated line. The extended address bits are initially loaded from SCR 04-05 to provide the 18-bit address capability. The contents of this register are used by the microprocessor in the computation of the control byte addresses for the received characters.

1010 Line Protocol Parameters

The Line Protocol Parameters secondary register contains the transmitter Data Link Escape (DLE) character when required by the associated line protocol, plus control bits to implement protocol requirements and handling of synch characters. The PDP-11 program writes the data in this register for reference by the microprogram. Bit assignments are described in the following table:

LINE PROTOCOL PARAMETERS SECONDARY REGISTER BIT ASSIGNMENTS

Bit(s)	Designation
00	Idle Mark if both Byte Counts Zero
01	Strip Leading Syncs
02	Unused
03-04	Block Check Type

03	04	BCC Type
0	0	LRC-8 (XOR)
1	0	CRC-16 ($X^{16}+X^{15}+X^2+1$)
0	1	Unused-16
1	1	CRC-CCITT ($X^{16}+X^{12}+X^5+1$)

05	DDCMP Receive
06	DDCMP Transmit
07	Unused
08-15	DLE Character

1011 Line State

The Line State secondary register is used by the PDP-11 program and the microprocessor to control and monitor line activities in executing the selected protocol. This register is also used by the PDP-11 program to store mode change and BCC anticipation bits for reference by the microprocessor when a marked receiver byte count reaches zero.

LINE STATE SECONDARY REGISTER BIT ASSIGNMENTS

Bit(s)	Designation	Read/Write
00	Receiver Active	Read
01	Receiver Resynchronize	Write
02	Transmitter Go	Read or Write
03	Transmitter Underrun	Read or Write zero
04	Transmitter Non-existant Memory (NXM)	
05	Transmitter Memory Parity Error	
06	Sync Strip On	
07	Use Alternate Tables	
08-09	Unused	
10	Expect BCC	
11-12	Unused	
13-15	Next Receive Mode on Marked Byte Count = 0	

1100 Transmitter Mode Bits

The Transmitter Mode Bits secondary register contain the 3-bit mode selection field (in bits 00-02) which determines the transmitter control table to be used for controlling transmission on the associated line.

1101 Receiver Mode Bits

The Receiver Mode Bits secondary register contains the 3-bit mode selection field (in bits 00-02) which determines the receiver control table to be used for controlling reception on the associated line.

1110 Line Progress

The Line Progress secondary register contains bits set and referenced by the microprocessor to control and monitor activities on the associated line in executing the selected protocol (these bits are not intended for access by the PDP-11 program). This register also stores mode change and BCC transmission control bits, as set by the PDP-11 program, for use by the microprocessor when a marked transmitter byte count reaches zero.

LINE PROGRESS SECONDARY REGISTER BIT ASSIGNMENTS

Bit(s)	Designation
00	Send BCC1 Next
01	Send BCC2 Next
02	DLE Sending In Progress
03-04	Unused
05	Expect BCC1
06	Expect BCC2 Next

07	Resynchronization Flag Expected
08-09	Unused
10	Send BCC
11-12	Unused
13-15	Next Transmit Mode on Marked Byte Count = 0

1111 Receiver Control Byte Holding

The Receiver Control Byte Holding secondary register provides a location for the microprocessor to store the Receiver Control Byte in bits 00-07 during character processing. The PDP-11 program may set a control byte into this register while responding to a DV11 receiver special character interrupt. When the PDP-11 program signals the DV11 that its interrupt response is complete (SCR 08=1), the microprocessor uses the control byte in this register to control the disposition of the interrupting character in the Receiver Interrupt Character register.

The microprocessor may also use this register to write control bytes that specify character discard only, if an error condition or data block boundary condition caused the interrupt; the existing mode specified in the control byte is not altered. The PDP-11 program should not write this register except during initialization or interrupt response cycles.

Special Functions Register - Address X12

Reserved for maintenance. Various bits may appear here during normal operations. Word addressable.

NPR Status Register - Address X14

This register is a silo-type register in that it is read once, in that a new entry "falls" into the register if there are additional "entries" existing at the time that the read of this register is completed. This register is read only.

This register reports various interrupt-causing conditions associated with the transmitter NPR hardware. Interrupt conditions related to various transmitter NPR operations are stacked up in a first-in first-out storage buffer along with the line number being serviced when this condition occurred. As soon as the program has finished reading this register once, a new entry is cycled into the register in place of the former entry. The interrupt is SCR 15 (NPR Status Interrupt). This register is read only, not cleared by Initialize, except for bit 15 which is cleared by initialize.

Bits	Description
ØØ-Ø3	Line Number These bits indicate which line was being serviced when the interrupt condition developed. The format of these bits is the same as bits ØØ-Ø3 of the Secondary Register Selection Register (SRSR) so that the program can load these bits into the SRSR and read the appropriate current address of byte count.
Ø4-Ø7	Unused
Ø8-11	These bits indicate the type of interrupt condition which occurred. The hardware is designed so that simultaneous occurrences on the same line create separate entries (Example: non-existant memory and byte count zero both occur). NOTE that the condition codes are the addresses of the secondary registers which apply.

Code	Condition
ØØØØ	Transmitter Principal Current Address sent NPR hardware to a non-existant memory location (NXM).
ØØØ1	Transmitter Principal Byte Count = Ø.
ØØ1Ø	Transmitter Alternate Current Address sent NPR hardware to a non-existant memory location.
ØØ11	Transmitter Alternate Byte Count = Ø.
1ØØØ	Transmitter Control Table Base Address - fetching control byte produced NXM or a memory parity error. The program should examine the Line State secondary register for further details.

12-14 Unused

15 Entry Present

When set, this bit indicates that bits ØØ-11 contain a valid entry. Reading the register or generating initialize clears this bit. It re-sets when another status report entry reaches the "bottom" of the silo and can be read in bits ØØ-11. Bits ØØ-11 are meaningless unless this bit (15) is set.

Reserved Register - Address X16

Bits	Function
ØØ-15	Reserved - word addressable

CONTROL BYTE FORMATS

The DV11 achieves its high througput and generalized operating capabilities by having both the transmitter and the receiver character handling apparatus perform NPR cycles to control by tables in PDP-11 core to determine the next step to take with regard to the particular character being processed. The bit assignments in the control bytes are arranged such that the same control bytes may be used for both transmission and reception if the communications protocol being used progresses fr-

mode to mode in a symmetrical fashion on both transmit and receive and provided that the same characters would be included in the Block Check Character in both transmission and reception.

BITS	TRANSMITTER CONTROL BYTE FUNCTION	RECEIVER CONTROL BYTE FUNCTION
Ø5-Ø7	NEXT MODE Determines next transmission mode used on this line.	NEXT MODE Determines next reception mode used on this line
Ø4	RESERVED	STORE/DISCARD Determines whether this character is stored in message table or is discarded.
Ø3	INCLUDE IN BCC YES/NO Determines whether or not this character will be included in the BCC being accumulated for this line.	INCLUDE IN BCC YES/NO Determines whether or not this character will be included in the BCC being accumulated for this line.
Ø2	SEND BCC NEXT Tells Transmitter Logic to send the 16-bit BCC after the character presently being handled. (8-bit if LRC selected)	EXPECT BCC NEXT Tells receiver logic to expect the 16-bit BCC after the character presently being handled. (8-bit if LRC selected)
Ø1	SEND DATA LINK ESCAPE NEXT Tells transmitter logic to send Data Link Escape character from Secondary Register 1Ø1Ø before sending the character presently being handled. (8-bit if LRC selected).	RESERVED
ØØ	RESERVED	GENERATE AN INTERRUPT The setting of this bit causes the character presently being processed to generate an interrupt. The microprocessor moves that character to the Receiver Interrupt Character Register and generates an interrupt request.

SPECIFICATIONS

SYSTEM ADDRESSES

The DV11 uses the same address space as the DM11-A. The first DV11 in a system would be at 775ØØØ; the next at 775Ø4Ø; then 7751ØØ; and finally, 7751ØØ. If there are DM11-A's in the system already, the first DV11 would be at 7750ØØ. The DV11 data handling and modem control use a total of ten registers.

INTERRUPT VECTORS

The DV11 requires three interrupt vectors - two for the data handling section and one for the modem control. The interrupt vectors are in the floating vector space that starts at 3ØØ. The DV11 modem control follows the DM11-BB which follows the DN11. The DV11 data handling section follows the DUP11 which in turn follows the DU11.

TIMING CONSIDERATIONS

The modem control timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan to either run free (SCAN EN) or to be sequentially stepped through the line counter line by line (STEP bit of CSR). The Read/Write cycles of the modem control scan logic force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's Read/Write cycles prevent halting the scan and changing the line number with one machine cycle.

Programs should not spin on flags in the DV11 secondary registers using loops less than 3Ø (octal) instructions; to do so may interfere with DV11 RAM microprocessor / UNIBUS access interlocks.

ORDER NUMBERS

DV11-AA	Double System unit contains all DV11 logic except the line cards and distribution panels. No lines are implemented.
DV11-BA	Line cards and distribution panel for eight lines. Requires 5-1/4 inches of cabinet space. Two DV11-BA's can be used with one DV11-AA. To configure an 8 line DV11, order 1 DV11-AA and 1 DV11-BA. To configure a 16 line DV11, order 1 DV11-AA and 2 DV11-BA's.

BUS LOADS

Two bus loads.

POWER CONSUMPTION

15 Amps @ +5 Volts

1 Amp @ -15 Volts

Ø.5 Amps @ +15 Volts

ENVIRONMENTAL

+ 10 degrees to + 50 degrees C with a relative humidity of 20% to 95%.

SPACE REQUIREMENTS

DV11-AA: Two system units (SU's).

DV11-BA: 5-1/4 inches of cabinet space (SM PAR).

CABLES

Order BCØSD-25 modem cables.

PROGRAMMABLE MODEM CONTROL DEVICE REGISTERS

The two programmable modem control device registers and their specific bit assignments are listed in the following paragraphs.

Control Status Register (CSR) (Address: 770XX0)

Bit	Status	Description
03:00	LINE #	The LINE # bits are the binary addresses for the modem control's 16 lines (0-15) as follows: Bit 3 2 1 0 — Line # 0 0 0 0 — 0 0 0 0 1 — 1 . . . . 1 1 1 1 — 15 If the Scan is cleared by INITIALIZE or CLR SCAN, the Line # Register will settle in 16μs ±10%. When settled, the Line # Register will be set to Line #0(0000). NOTE When the Scan is enabled (or STEP) the next line to be tested will always be Line # +1. These bits are Read/Write and are cleared by INITIALIZE and by CLR SCAN.
04	BUSY	BUSY provides a program indicator that is set to 1 when the Scan is cycling. This bit is particularly useful to determine when a CLR SCAN (bit 11) has completed the task of cycling Øs into the Scanner's memory elements. In addition, this bit must be tested for 0 if SCAN ENABLE was turned off preparatory to changing the Line #. In Interrupt Mode, this procedure guarantees that detected transitions are serviced before the Line # is changed. (If functioning with interrupts OFF, then DONE should be tested after BUSY is found to be 0.)

Bit	Status	Description
05	SCAN EN	The SCAN ENABLE flip-flop allows the scan to "free run" -- testing all lines sequentially if the DONE flip-flop is cleared. When the SCAN EN flip-flop is set to 1 and DONE is 0, a ring counter is allowed to cycle in the following order (from Rest): a. Increment Line counter. b. Store contents of memory (Line # Address) in the HOLD flip-flop. c. Write current modem status into memory. d. Compare HOLD and contents of memory for Interrupt conditions. The ring counter continues to cycle (a to d) if DONE remains 0 and SCAN EN is set. If the SCAN EN flip-flop is negated while the ring counter is cycling (i.e., DONE not set) the ring counter will come to rest in 1.2μs ±10% (MAX). The line #Register must not be changed until BUSY (bit 04) is found to be 0. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
06	INTER EN	If set to 1, Interrupt Enable allows DONE to cause an interrupt on priority four (4). This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
07	DONE	The DONE flag, when set to 1, indicates that the hardware Scan has detected a transition on CARRIER, SEC RX, CS, or the RING Modem Status leads. Additionally, DONE freezes the Scan which makes available to the programmer: a. The Line # that caused the interrupt. b. The state of the flags (4 bits) c. Modem status (8 bits)

This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.

08 STEP — STEP, when set to 1, causes the Scan to increment the Line # and test that line for interrupts causing transitions. STEP can be used in place of SCAN EN, but care should be exercised that the Scan rate is great enough (milliseconds) so that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1.2 μs ±10% to execute. This bit is Write 1s only.

09 MAINT MODE — When the MAINT MODE flip-flog is set to 1, it conditions the Scan Input (RING, CLEAR TO SEND, CARRIER, and SEC RX) to a 1 or ON state. Utilizing STEP or SCAN EN with MAINT MODE exercises 100 percent of the scan logic (not the data multiplexers). This includes the interrupt circuits (M7821) and the address selector (M105).

This mode provides a diagnostic feature, as well as an on-line test facility for the modem control's interaction with the Unibus. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.

10 CLEAR MUX — CLEAR MUX clears the REQUEST TO SEND, TERMINAL READY, SEC TX, and LINE EN flip-flops for all lines, when this bit is set to 1. This bit is Write 1s only.

11 CLR SCAN — CLEAR SCAN clears all active functions (Line #, SCAN EN, etc., and the memory logic, when this bit is set to 1. The memory logic requires 18.8 μs ±10% to cycle a CLEAR through the memory locations. This function is especially useful if the programmer requires knowledge of the ON states of CARRIER, CLEAR TO SEND, RING and SEC RX. When the Scan is enabled (or STEP) following a CLR SCAN, an interrupt will occur for all ON states as they will appear (to the logic) as OFF to ON transitions.

12 DSR — The DATA SET READY flag is 1 if an ON to OFF or an OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.

13 CS — The CLEAR TO SEND flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.

14 CO — The CARRIER flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.

15 RING — The RING flag is 1 if an OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.

Line Status Register (LSR) (Address: 770XX2)

Bit	Status	Description
00	LINE EN	The LINE ENABLE flip-flop, when asserted, enables RING, CO, CS, and SEC RX to be sampled (line status) by the program, and to be tested for transitions.

This bit is Read/Write and cleared by INITIALIZE and CLEAR MUX.

01 TERM RDY — Controls switching of the data communications equipment to the communication channel (via modem).

Auto-Dial and Manual Call origination: Maintains the established call.

Auto-Answer: Allows "handshaking" in response to a RING signal.

This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.

02 RS — When REQUEST TO SEND is set to 1, it conditions the modem for transmit if the communications channel has been established (switched network). This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.

03 NS — The New Sync (201) flip-flop, when 1, presents a high to the New Sync lead. This bit is Read/Write and is cleared by INITIALIZE or CLEAR MUX.

04 DSR — When the state of the modem's Data Set Ready lead is a high, this bit is a 1. The DSR bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

05 CS — This bit reflects the current state of the modem CLEAR TO SEND lead. An ON indicates that the modem is ready to transmit data. This lead is most often the result of the REQUEST TO SEND lead. The CS bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

06 CO — This bit reflects the current state of the modem carrier detect lead. An OFF indicates that the received signal is unsuitable for demodulation. The CO bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

07 RING — This bit reflects the current state of the modem's ring lead. The RING bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.

NOTE

The Line Status Register bits 07:00 are inhibited when LINE EN is 0.

System Addresses

The DV11 modem control uses two address locations in the floating address area.

Interrupt Vectors

Each modem control requires one interrupt vector. The vector addresses are assigned upward from 300 to 777. The modem control falls in behind the DV11 in contiguous assignments from 300.

Timing Considerations

The modem control timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan to either run free (SCAN EN) or to be sequentially stepped through the line counter line by line (STEP bit of CSR). The Read/Write cycles of the modem control scan logic (Paragraph 4.4) force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's Read/Write cycles prevent halting the scan and changing the line number with one machine cycle.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY John McNamara	CHECKED Ed Roberts	SECTION
DATE April 16, 1975	DATE 4-17-75	
ENG John E. McNamara	PROD R. Wall	ISSUED SECT.
DATE 4-17-75	DATE 4-17-75	

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DV11-AA
1	ZJ192-RB	DV11 Diagnostic Kit	1
		NOTE: The ZJ192-RB diagnostic kit includes, but is not necessarily limited to, the following diagnostics: **Maindec-11-DZDVA**, Maindec-11-DZDVB, Maindec-11-DZDVC, Maindec-11-DZDVD, and Maindec-11-DZDVE.	

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
DV11 Software List	--	A	PL	DV11-Ø-6		
	SHEET 1 OF 1	DIST.				

DEC FORM DEC 16 (325) 1031 N870
DRA 110

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MADE BY John McNamara	CHECKED Ed Roberts	SECTION
DATE April 16, 1975	DATE 4-17-75	
ENG John E. McNamara	PROD R. Wall	ISSUED SECT.
DATE 4-17-75	DATE 4-17-75	

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION DV11-AA
1.	MP-DV11-Ø	DV11 Customer Print Set #1	1
2.	ZJ192-RB	DV11 Diagnostic Kit	1
3.	EK-DV11-MM	DV11 Maintenance Manual	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
DV11 Shipping List	SHEET 1 OF 1	A	PL	DV11-Ø-5		
		DIST.				

DEC FORM DEC 16-(325)-1031 N870
DRA 110

DIGITAL EQUIPMENT CORPORATION

REV.	NUMBER	CODE	SIZE
7-0-1	DV11	WL	K

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DV11		PARTS LIST		

DRN. Robert Koppenal	DATE 4-9-75	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. Sid Roberts	DATE 4-17-75	
ENG. John E. McNamara	DATE 4-17-75	TITLE WIRE LIST
PROJ. ENG. John E. McNamara	DATE 4-17-75	
PROD. R. Wall	DATE 4-17-75	
NEXT HIGHER ASSEMBLY B-DD-DV11-0		SIZE K / CODE WL / NUMBER DV11-0-7 / REV.
SCALE		
SHEET 1 OF 1		DIST.

REVISIONS

REV.	CHANGE NO.	CHK

DEC FORM NO DPB 109

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
01 L		B03J1		1-01				M7837			1				1
01 L		E04R1		1-02				M7838							1
01 L				1									11-0/8		1
02 L		F03J2		1-01				M7837			1				2
02 L		F04D2		1-02				M7838							2
02 L				1									3-0/8		2
1200 BAUD		F04K2		1-01				M7838			1				3
1200 BAUD		F05D1		1-02				M7839			2				3
1200 BAUD		F06D1		1-03				M7839			1				3
1200 BAUD		F07D1		1-04				M7839			2				3
1200 BAUD		F08D1		1-05				M7839							3
1200 BAUD				1									11-4/8		3
19200 BAUD		F04R1						M7838						1-PIN RUN	4
230,4 KB H		B08M1		1-01				M7839			1				5
230,4 KB H		B07M1		1-02				M7839			2				5
230,4 KB H		B06M1		1-03				M7839			1				5
230,4 KB H		B05M1		1-04				M7839			2				5
230,4 KB H		B03M1		1-05				M7837			1				5
230,4 KB H		F04L2		1-06				M7838							5
230,4 KB H				1									24-4/8		5
2400 BAUD		F04J2		1-01				M7838			1				6
2400 BAUD		F05D2		1-02				M7839			2				6
2400 BAUD		F06D2		1-03				M7839			1				6
2400 BAUD		F07D2		1-04				M7839			2				6
2400 BAUD		F08D2		1-05				M7839							6
2400 BAUD				1									11-2/8		6
4800 BAUD		F04L1		1-01				M7838			1				7
4800 BAUD		F05E2		1-02				M7839			2				7
4800 BAUD		F06E2		1-03				M7839			1				7
4800 BAUD		F07E2		1-04				M7839			2				7
4800 BAUD		F08E2		1-05				M7839							7
4800 BAUD				1									11-4/8		7
600 BAUD		F04H2						M7838						1-PIN RUN	8

	9600 BAUD		DM3S1	1-01		M7837	1					9
	9600 BAUD		FM8F2	1-02		M7839	2					9
	9600 BAUD		FM7F2	1-03		M7839	1					9
	9600 BAUD		FM6F2	1-04		M7839	2					9
	9600 BAUD		FM5F2	1-05		M7839	1					9
	9600 BAUD		FM4S1	1-06		M7838						9
	9600 BAUD			1						19-6/8		9
	A REGISTER CLOCK L		BM4M2	1-01		M7838	1					10
	A REGISTER CLOCK L		EM2C1	1-02		M7836						10
	A REGISTER CLOCK L			1						10-2/8		10
	A00 H		AM3M1	1-01		M7837	1					11
	A00 H		M72V1	1-02		M7836						11
	A00 H			1						6-2/8		11
	A01 H		CM2A1	1-01		M7836	1					12
	A01 H		CM3U2	1-02		M7837						12
	A01 H			1						4-0/8		12
	A02 H		BM2U1	1-01		M7836	1					13
	A02 H		CM3S1	1-02		M7837						13
	A02 H			1						4-6/8		13
	A03 H		BM2F2	1-01		M7836	1					14
	A03 H		CM3U2	1-02		M7837						14
	A03 H			1						6-4/8		14
	A17 H		AM2K1	1-01		M7836	1					15
	A17 H		FM4E1	1-02		M7838						15
	A17 H			1						15-4/8		15
	ADDRESS SELECTED H		AM2S1	1-01		M7836	1					16
	ADDRESS SELECTED H		FM4E2	1-02		M7838						16
	ADDRESS SELECTED H			1						15-0/8		16
	ADDRESS TO BUS L		AM2V1	1-01		M7836	1					17
	ADDRESS TO BUS L		EC3H1	1-02		M7837						17
	ADDRESS TO BUS L			1						11-6/8		17
	ADVANCE MASTER SCAN L		A02D2	1-01		M7836	1					18
	ADVANCE MASTER SCAN L		DM4P2	1-02		M7838						18
	ADVANCE MASTER SCAN L			1						11-6/8		18
	ALU 13-12 H		DM2J2	1-01		M7836	1					19
	ALU 13-12 H		EM4C1	1-02		M7838						19
	ALU 13-12 H			1						4-4/8		19

	ALU A=B H		CM2D2	1-01		M7836	1					20
	ALU A=B H		DM4V2	1-02		M7838						20
	ALU A=B H			1						5-6/8		20
	ALU OPERATION L		EM4P2	1-01		M7838	1					21
	ALU OPERATION L		FM2E2	1-02		M7836						21
	ALU OPERATION L			1						4-4/8		21
	ALU RESULT 00 H		DM2M2	1-01		M7836	1					22
	ALU RESULT 00 H		DM4U2	1-02		M7838						22
	ALU RESULT 00 H			1						3-6/8		22
	ALU RESULT 01 H		DM4U1	1-01		M7838	1					23
	ALU RESULT 01 H		FM2L1	1-02		M7836						23
	ALU RESULT 01 H			1						7-0/8		23
	ALU RESULT 02 H		DM2M2	1-01		M7836	1					24
	ALU RESULT 02 H		DM4T2	1-02		M7838						24
	ALU RESULT 02 H			1						4-0/8		24
	ALU RESULT 03 H		DM2L2	1-01		M7836	1					25
	ALU RESULT 03 H		DM4S2	1-02		M7838						25
	ALU RESULT 03 H			1						3-4/8		25
	ALU RESULT 04 H		CM2E1	1-01		M7836	1					26
	ALU RESULT 04 H		DM4S1	1-02		M7838						26
	ALU RESULT 04 H			1						6-6/8		26
	ALU RESULT 15 H		CM2V2	1-01		M7836	1					27
	ALU RESULT 15 H		EM4H1	1-02		M7838						27
	ALU RESULT 15 H			1						6-4/8		27
	ASSERT MSYN H		BM4P2	1-01		M7838	1					28
	ASSERT MSYN H		FM3J1	1-02		M7837						28
	ASSERT MSYN H			1						9-6/8		28
	B REGISTER CLOCK L		BM4F2	1-01		M7838	1					29
	B REGISTER CLOCK L		DM2U2	1-02		M7836						29
	B REGISTER CLOCK L			1						9-4/8		29
	BCC CALCULATION L		EM4U2	1-01		M7838	1					30
	BCC CALCULATION L		FM2C1	1-02		M7836						30
	BCC CALCULATION L			1						4-0/8		30

A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
	AP3V1		1-01					M7837		1				31
	F05F1		1-02					M7839		2				31
	F06F1		1-03					M7839		1				31
	FW7F1		1-04					M7839		2				31
	F08F1		1-05					M7839						31
			1									22-6/8		31
	E04H2		1-01					M7838		1				32
	F03D1		1-02					M7837						32
			1									5-0/8		32
	D04B1		1-01					M7838		1				33
	F03P2		1-02					M7837						33
			1									9-2/8		33
	A02K2		1-01					M7836		2				34
	B04M2		1-02					M7838		1				34
	E03F2		1-03					M7837						34
			1									15-4/8		34
	A02H2		1-01					M7836		2				35
	BW4R2		1-02					M7838		1				35
	EW3H2		1-03					M7837						35
			1									16-0/8		35
	AP2E2		1-01					M7836		1				36
	B03N1		1-02					M7837		2				36
	B04U2		1-03					M7838						36
			1									9-4/8		36
	AP2H1		1-01					M7836		1				37
	B03E1		1-02					M7837		2				37
	B04N2		1-03					M7838						37
			1									8-4/8		37
	A04K2		1-01					M7838		1				38
	C02S2		1-02					M7836		2				38
	E03D1		1-03					M7837						38
			1									15-2/8		38
	A04J2		1-01					M7838		1				39
	B03V2		1-02					M7837		2				39
	C02P2		1-03					M7836						39
			1									11-0/8		39

A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
	A04P2		1-01					M7838		1				40
	B03T2		1-02					M7837		2				40
	C02L2		1-03					M7836						40
			1									10-0/8		40
	304L2		1-01					M7838		2				41
	B03G2		1-02					M7837		1				41
	C02J2		1-03					M7836						41
			1									7-4/8		41
	A02J2		1-01					M7836		2				42
	B03S1		1-02					M7837		1				42
	FW4P2		1-03					M7838						42
			1									19-0/8		42
	A02F1		1-01					M7836		1				43
	C03F1		1-02					M7837		2				43
	C04S2		1-03					M7838						43
			1									11-4/8		43
	A02F2		1-01					M7836		2				44
	CW3D1		1-02					M7837		1				44
	FW4V1		1-03					M7838						44
			1									17-0/8		44
	A02E1		1-01					M7836		2				45
	B03K1		1-02					M7837		1				45
	FW4S2		1-03					M7838						45
			1									19-6/8		45
	CW3B2		1-01					M7837		2				46
	C02R2		1-02					M7836		1				46
	EW4N1		1-03					M7838						46
			1									11-6/8		46
	C02N2		1-01					M7836		2				47
	C03E1		1-02					M7837		1				47
	CW4F2		1-03					M7838						47
			1									6-4/8		47
	C02K2		1-01					M7836		2				48
	C04K1		1-02					M7838		1				48
	C03F2		1-03					M7837						48
			1									5-6/8		48

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
BUF DATA 15 H		BA3F2		1-01					M7837		1				49
BUF DATA 15 H		CA4L1		1-02					M7838		2				49
BUF DATA 15 H		CA2M2		1-03					M7836						49
BUF DATA 15 H				1									7-6/8		49
BUF ROM DATA 04 H		DA2C1							M7836					1-PIN RUN	50
BUF ROM DATA 05 H		EA2A1							M7836					1-PIN RUN	51
BUS A00 L		BA9A2		1-01					UNIB		1				52
BUS A00 L		BA2A2		1-02					M7836		2				52
BUS A00 L		BA1A2		1-03					UNIB		1				52
BUS A00 L		EA1A2		1-04					DM11						52
BUS A00 L				1									18-4/8		52
BUS A01 L		BA9A1		1-01					UNIB		1				53
BUS A01 L		BA2A1		1-02					M7836		2				53
BUS A01 L		BA1A1		1-03					UNIB		1				53
BUS A01 L		EA1A1		1-04					DM11						53
BUS A01 L				1									18-4/8		53
BUS A02 L		BA9J2		1-01					UNIB		1				54
BUS A02 L		BA2J2		1-02					M7836		2				54
BUS A02 L		BA1J2		1-03					UNIB		1				54
BUS A02 L		EA1F1		1-04					DM11						54
BUS A02 L				1									18-4/8		54
BUS A03 L		BA9J1		1-01					UNIB		1				55
BUS A03 L		BA2J1		1-02					M7836		2				55
BUS A03 L		BA1J1		1-03					UNIB		1				55
BUS A03 L		EA1V2		1-04					DM11						55
BUS A03 L				1									20-0/8		55
BUS A04 L		BA9K2		1-01					UNIB		1				56
BUS A04 L		BA2K2		1-02					M7836		2				56
BUS A04 L		BA1K2		1-03					UNIB		1				56
BUS A04 L		EA1U2		1-04					DM11						56
BUS A04 L				1									19-4/8		56
BUS A05 L		BA9K1		1-01					UNIB		1				57
BUS A05 L		BA2K1		1-02					M7836		2				57
BUS A05 L		BA1K1		1-03					UNIB		1				57
BUS A05 L		EA1V1		1-04					DM11						57
BUS A05 L				1									19-6/8		57

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
BUS A06 L		BA9L2		1-01					UNIB		1				58
BUS A06 L		BA2L2		1-02					M7836		2				58
BUS A06 L		BA1L2		1-03					UNIB		1				58
BUS A06 L		EA1U1		1-04					DM11						58
BUS A06 L				1									19-6/8		58
BUS A07 L		BA9L1		1-01					UNIB		1				59
BUS A07 L		BA2L1		1-02					M7836		2				59
BUS A07 L		BA1L1		1-03					UNIB		1				59
BUS A07 L		EA1P2		1-04					DM11						59
BUS A07 L				1									19-0/8		59
BUS A08 L		BA9M2		1-01					UNIB		1				60
BUS A08 L		BA2M2		1-02					M7836		2				60
BUS A08 L		BA1M2		1-03					UNIB		1				60
BUS A08 L		EA1N2		1-04					DM11						60
BUS A08 L				1									18-6/8		60
BUS A09 L		BA9M1		1-01					UNIB		1				61
BUS A09 L		BA2M1		1-02					M7836		2				61
BUS A09 L		BA1M1		1-03					UNIB		1				61
BUS A09 L		EA1P1		1-04					DM11						61
BUS A09 L				1									19-0/8		61
BUS A10 L		BA9N2		1-01					UNIB		1				62
BUS A10 L		BA2N2		1-02					M7836		2				62
BUS A10 L		BA1N2		1-03					UNIB		1				62
BUS A10 L		EA1P1		1-04					DM11						62
BUS A10 L				1									19-0/8		62
BUS A11 L		BA9N1		1-01					UNIB		1				63
BUS A11 L		BA2N1		1-02					M7836		2				63
BUS A11 L		BA1N1		1-03					UNIB		1				63
BUS A11 L		EA1L1		1-04					DM11						63
BUS A11 L				1									18-2/8		63
BUS A12 L		BA9P2		1-01					UNIB		1				64
BUS A12 L		BA2P2		1-02					M7836		2				64
BUS A12 L		BA1P2		1-03					UNIB		1				64
BUS A12 L		EA1C1		1-04					DM11						64
BUS A12 L				1									17-4/8		64
BUS A13 L		BA9P1		1-01					UNIB		1				65
BUS A13 L		BA2P1		1-02					M7836		2				65
BUS A13 L		BA1P1		1-03					UNIB		1				65
BUS A13 L		EA1K2		1-04					DM11						65
BUS A13 L				1									18-2/8		65

RUN NAME	A/P	PIN NAME	ORDER PIN	PAY = ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
BUS A14 L		BV9R2		1-01					UNIB	1					66
BUS A14 L		BG2R2		1-02					M7836	2					66
BUS A14 L		B01R2		1-03					UNIB	1					66
BUS A14 L		E01K1		1-04					DM11						66
BUS A14 L				1									18-2/8		66
BUS A15 L		B09R1		1-01					UNIB	1					67
BUS A15 L		BV2R1		1-02					M7836	2					67
BUS A15 L		B01R1		1-03					UNIB	1					67
BUS A15 L		EV1D2		1-04					DM11						67
BUS A15 L				1									17-4/8		67
BUS A16 L		BV9S2		1-01					UNIB	1					68
BUS A16 L		BV2S2		1-02					M7836	2					68
BUS A16 L		B01S2		1-03					UNIB	1					68
BUS A16 L		EV1F2		1-04					DM11						68
BUS A16 L				1									17-2/8		68
BUS A17 L		BV9S1		1-01					UNIB	1					69
BUS A17 L		BV2S1		1-02					M7836	2					69
BUS A17 L		BV1S1		1-03					UNIB	1					69
BUS A17 L		EV1D1		1-04					DM11						69
BUS A17 L				1									17-2/8		69
BUS ACLO L		BV1F1		1-01					UNIB	1					70
BUS ACLO L		BV9F1		1-02					UNIB						70
BUS ACLO L				1									6-2/8		70
BUS B BG IN H		B01E2		1-01					UNIB	1					71
BUS B BG IN H		FV1E1		1-02					DM11	2					71
BUS B BG IN H		E09L2		1-03					DM11						71
BUS B BG IN H				1									20-6/8		71
BUS B BG OUT H		BV9E2		1-01					UNIB	1					72
BUS B BG OUT H		EV9K2		1-02					DM11	2					72
BUS B BG OUT H		FV1A1		1-03					DM11						72
BUS B BG OUT H				1									17-6/8		72
BUS BBSY L		AV9P2		1-01					UNIB	1					73
BUS BBSY L		AV3P2		1-02					M7837	2					73
BUS BBSY L		AV1P2		1-03					UNIB	1					73
BUS BBSY L		FV1D1		1-04					DM11						73
BUS BBSY L				1									23-0/8		73
BUS BG5 IN H		B01B1		1-01					UNIB	1					74
BUS BG5 IN H		B03B1		1-02					M7837						74
BUS BG5 IN H				1									3-2/8		74

RUN NAME	A/P	PIN NAME	ORDER PIN	PAY = ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
BUS BG5 OUT H		BP3E2		1-01					M7837	1					75
BUS BG5 OUT H		B0981		1-02					UNIB						75
BUS BG5 OUT H				1									5-4/8		75
BUS BG6 IN H		B01A1		1-01					UNIB	1					76
BUS BG6 IN H		BV3A1		1-02					M7837						76
BUS BG6 IN H				1									3-2/8		76
BUS BG6 OUT H		BV3B2		1-01					M7837	1					77
BUS BG6 OUT H		BV9A1		1-02					UNIB						77
BUS BG6 OUT H				1									5-0/8		77
BUS BG7 H		AV1V1		1-01					UNIB	1					78
BUS BG7 H		AV9V1		1-02					UNIB						78
BUS BG7 H				1									6-2/8		78
BUS BR4 L		B09D2		1-01					UNIB	2					79
BUS BR4 L		BV1D2		1-02					UNIB	1					79
BUS BR4 L		FV1P1		1-03					DM11						79
BUS BR4 L				1									20-4/8		79
BUS BR5 L		B01C1		1-01					UNIB	2					80
BUS BR5 L		B03C1		1-02					M7837	1					80
BUS BR5 L		B09C1		1-03					UNIB						80
BUS BR5 L				1									8-4/8		80
BUS BR6 L		AV1U2		1-01					UNIB	2					81
BUS BR6 L		AV3U2		1-02					M7837	1					81
BUS BR6 L		A09U2		1-03					UNIB						81
BUS BR6 L				1									8-4/8		81
BUS BR7 L		AP1T2		1-01					UNIB	1					82
BUS BR7 L		A09T2		1-02					UNIB						82
BUS BR7 L				1									6-2/8		82
BUS C0 L		BV9U2		1-01					UNIB	1					83
BUS C0 L		BV2U2		1-02					M7836	2					83
BUS C0 L		BP1U2		1-03					UNIB	1					83
BUS C0 L		EV1J2		1-04					DM11						83
BUS C0 L				1									17-4/8		83
BUS C1 L		BV9T2		1-01					UNIB	1					84
BUS C1 L		BV2I2		1-02					M7836	2					84
BUS C1 L		BV1T2		1-03					UNIB	1					84
BUS C1 L		E01F2		1-04					DM11						84
BUS C1 L				1									17-2/8		84

A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
BUS D00 L	A01C1		1-01					UNIB		1				85
BUS D00 L	A03C1		1-02					M7837		2				85
BUS D00 L	A09C1		1-03					UNIB		1				85
BUS D00 L	E09E1		1-04					DM11						85
BUS D00 L			1									21-4/8		85
BUS D01 L	A01D2		1-01					UNIB		1				86
BUS D01 L	A03D2		1-02					M7837		2				86
BUS D01 L	A09D2		1-03					UNIB		1				86
BUS D01 L	E09K1		1-04					DM11						86
BUS D01 L			1									22-2/8		86
BUS D02 L	A01D1		1-01					UNIB		1				87
BUS D02 L	A03D1		1-02					M7837		2				87
BUS D02 L	A09D1		1-03					UNIB		1				87
BUS D02 L	E09B2		1-04					DM11		2				87
BUS D02 L	F01E2		1-05					DM11						87
BUS D02 L			1									29-0/8		87
BUS D03 L	A01E2		1-01					UNIB		1				88
BUS D03 L	A03E2		1-02					M7837		2				88
BUS D03 L	A09E2		1-03					UNIB		1				88
BUS D03 L	E09J1		1-04					DM11		2				88
BUS D03 L	F01G1		1-05					DM11						88
BUS D03 L			1									29-2/8		88
BUS D04 L	A01E1		1-01					UNIB		1				89
BUS D04 L	A03E1		1-02					M7837		2				89
BUS D04 L	A09E1		1-03					UNIB		1				89
BUS D04 L	F09B1		1-04					DM11		2				89
BUS D04 L	F01N2		1-05					DM11						89
BUS D04 L			1									30-4/8		89
BUS D05 L	A01F2		1-01					UNIB		1				90
BUS D05 L	A03F2		1-02					M7837		2				90
BUS D05 L	A09F2		1-03					UNIB		1				90
BUS D05 L	E09V1		1-04					DM11		2				90
BUS D05 L	F01F1		1-05					DM11						90
BUS D05 L			1									30-0/8		90
BUS D06 L	A01F1		1-01					UNIB		1				91
BUS D06 L	A03F1		1-02					M7837		2				91
BUS D06 L	A09F1		1-03					UNIB		1				91
BUS D06 L	F09A1		1-04					DM11		2				91
BUS D06 L	F01F2		1-05					DM11						91
BUS D06 L			1									29-6/8		91

A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
BUS D07 L	A01H2		1-01					UNIB		1				92
BUS D07 L	A03H2		1-02					M7837		2				92
BUS D07 L	A09H2		1-03					UNIB		1				92
BUS D07 L	E09R1		1-04					DM11		2				92
BUS D07 L	F01H1		1-05					DM11						92
BUS D07 L			1									29-4/8		92
BUS D08 L	A01H1		1-01					UNIB		1				93
BUS D08 L	A03H1		1-02					M7837		2				93
BUS D08 L	A09H1		1-03					UNIB		1				93
BUS D08 L	F09E1		1-04					DM11		2				93
BUS D08 L	F01K1		1-05					DM11						93
BUS D08 L			1									30-2/8		93
BUS D09 L	A01J2		1-01					UNIB		1				94
BUS D09 L	A03J2		1-02					M7837		2				94
BUS D09 L	A09J2		1-03					UNIB		1				94
BUS D09 L	E09V2		1-04					DM11						94
BUS D09 L			1									22-4/8		94
BUS D10 L	A01J1		1-01					UNIB		1				95
BUS D10 L	A03J1		1-02					M7837		2				95
BUS D10 L	A09J1		1-03					UNIB		1				95
BUS D10 L	F09F1		1-04					DM11						95
BUS D10 L			1									23-6/8		95
BUS D11 L	A01K2		1-01					UNIB		1				96
BUS D11 L	A03K2		1-02					M7837		2				96
BUS D11 L	A09K2		1-03					UNIB		1				96
BUS D11 L	F09C1		1-04					DM11						96
BUS D11 L			1									23-4/8		96
BUS D12 L	A01K1		1-01					UNIB		1				97
BUS D12 L	A03K1		1-02					M7837		2				97
BUS D12 L	A09K1		1-03					UNIB		1				97
BUS D12 L	F09R2		1-04					DM11						97
BUS D12 L			1									25-0/8		97
BUS D13 L	A01L2		1-01					UNIB		1				98
BUS D13 L	A03L2		1-02					M7837		2				98
BUS D13 L	A09L2		1-03					UNIB		1				98
BUS D13 L	F09T2		1-04					DM11						98
BUS D13 L			1									24-6/8		98

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
BUS D14 L		AP1L1		1-P1					UNIB		1				99
BUS D14 L		A03L1		1-02					M7837		2				99
BUS D14 L		A09L1		1-03					UNIB		1				99
BUS D14 L		F09S2		1-04					DM11						99
BUS D14 L				1									24-6/8		99
BUS D15 L		AP1M2		1-01					UNIB		1				100
BUS D15 L		A03M2		1-02					M7837		2				100
BUS D15 L		A09M2		1-03					UNIB		1				100
BUS D15 L		F09P2		1-04					DM11						100
BUS D15 L				1									24-2/8		100
BUS DCLO L		BP1F2		1-01					UNIB		1				101
BUS DCLO L		B09F2		1-02					UNIB						101
BUS DCLO L				1									6-2/8		101
BUS INIT L		AP1A1		1-P1 *					UNIB		2				102
BUS INIT L		A04A1		1-02 *					M7838		1				102
BUS INIT L		A09A1		1-03 *					UNIB		2				102
BUS INIT L		A07S1		1-04 *					M7839		1				102
BUS INIT L		E07V1		1-05 *					M7839		2				102
BUS INIT L		F09D1		1-06 *					DM11						102
BUS INIT L				1									30-0/8		102
BUS INTR L		A09B1		1-P1					UNIB		1				103
BUS INTR L		A03B1		1-02					M7837		2				103
BUS INTR L		AP1H1		1-03					UNIB		1				103
BUS INTR L		F01M1		1-04					DM11						103
BUS INTR L				1									25-2/8		103
BUS MSYN L		B09V1		1-P1					UNIB		1				104
BUS MSYN L		B04V1		1-02					M7838		2				104
BUS MSYN L		BP1V1		1-03					UNIB		1				104
BUS MSYN L		E01E1		1-04					DM11						104
BUS MSYN L				1									17-0/8		104
BUS NPG IN H		AP1U1		1-P1					UNIB		1				105
BUS NPG IN H		A03U1		1-02					M7837						105
BUS NPG IN H				1									3-2/8		105
BUS NPG OUT H		AP9U1		1-P1					UNIB		1				106
BUS NPG OUT H		B03D1		1-02					M7837						106
BUS NPG OUT H				1									5-6/8		106

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RU NUM
BUS NPR L		A09S2		1-01					UNIB		1				1
BUS NPR L		A03S2		1-02					M7837		2				1
BUS NPR L		A21S2		1-03					UNIB		1				1
BUS NPR L		F01J1		1-04					DM11						1
BUS NPR L				1									23-2/8		1
BUS PA L		A01M1		1-21					UNIB		2				1
BUS PA L		A02M1		1-02					M7836		1				1
BUS PA L		A09M1		1-03					UNIB						1
BUS PA L				1									8-4/8		1
BUS PB L		AP1N2		1-01					UNIB		2				1
BUS PB L		AP2N2		1-02					M7836		1				1
BUS PB L		A09N2		1-03					UNIB						1
BUS PB L				1									8-4/8		1
BUS SACK L		A09R2		1-01					UNIB		1				1
BUS SACK L		A03R2		1-02					M7837		2				1
BUS SACK L		A01R2		1-03					UNIB		1				1
BUS SACK L		F01I2		1-04					DM11						1
BUS SACK L				1									24-2/8		1
BUS SSYN L		B09U1		1-01					UNIB		2				1
BUS SSYN L		B04U1		1-02					M7838		1				1
BUS SSYN L		B03U1		1-03					M7837		2				1
BUS SSYN L		B01U1		1-04					UNIB		1				1
BUS SSYN L		E01J1		1-05					DM11		2				1
BUS SSYN L		F01C1		1-06					DM11						1
BUS SSYN L				1									24-2/8		1
C0 H		A02J1		1-01					M7836		1				1
C0 H		A03T2		1-02					M7837						1
C0 H				1									3-6/8		1
C1 H		A02D1		1-01					M7836		1				1
C1 H		B03N1		1-02					M7837						1
C1 H				1									6-2/8		1
CARD FLAG SEL 00-03 L		D05M2							M7839					1-PIN RUN	1
CARD FLAG SEL 04-07 L		D06M2							M7839					1-PIN RUN	1
CARD FLAG SEL 08-11 L		D07M2							M7839					1-PIN RUN	1
CARD FLAG SEL 12-15 L		D08M2							M7839					1-PIN RUN	1

RUN NAME	A/P	PIN .NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
CARD PAR SEL 00-03 L		D05U2							M7839					1-PIN RUN	118
CARD PAR SEL 04-07 L		D06U2							M7839					1-PIN RUN	119
CARD PAR SEL 08-11 L		D07U2							M7839					1-PIN RUN	120
CARD PAR SEL 12-15 L		D08U2							M7839					1-PIN RUN	121
CLEAR ALU 01 L		F02T2							M7836					1-PIN RUN	122
CLEAR ALU 02 L		F02P1							M7836					1-PIN RUN	123
CLEAR CYCLE L		D01P2		1-01					DM11	2					124
CLEAR CYCLE L		D09P2		1-02					DM11	1					124
CLEAR CYCLE L		F09R1		1-03					DM11						124
CLEAR CYCLE L				1									14-0/8		124
CLEAR MUX L		D01J1		1-01					DM11	2					125
CLEAR MUX L		D09J1		1-02					DM11	1					125
CLEAR MUX L		F09M2		1-03					DM11						125
CLEAR MUX L				1									14-2/8		125
CLEAR TMARK L		C04A1		1-01					M7838	1					126
CLEAR TMARK L		F05K2		1-02					M7839	2					126
CLEAR TMARK L		F06K2		1-03					M7839	1					126
CLEAR TMARK L		F07K2		1-04					M7839	2					126
CLEAR TMARK L		F08K2		1-05					M7839						126
CLEAR TMARK L				1									20-0/8		126
CLR ALU RESLT HI BYT L		F02S2							M7836					1-PIN RUN	127
CLR FLAG 00 L		B05V2							M7839					1-PIN RUN	128
CLR FLAG 01 L		B05F1							M7839					1-PIN RUN	129
CLR FLAG 02 L		B05U2							M7839					1-PIN RUN	130
CLR FLAG 03 L		B05V1							M7839					1-PIN RUN	131
CLR FLAG 04 L		B06V2							M7839					1-PIN RUN	132
CLR FLAG 05 L		B06F1							M7839					1-PIN RUN	133
CLR FLAG 06 L		B06U2							M7839					1-PIN RUN	134
CLR FLAG 07 L		B06V1							M7839					1-PIN RUN	135

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
CLR FLAG 08 L		B07V2							M7839					1-PIN RUN	136
CLR FLAG 09 L		B07F1							M7839					1-PIN RUN	137
CLR FLAG 10 L		B07U2							M7839					1-PIN RUN	138
CLR FLAG 11 L		B07V1							M7839					1-PIN RUN	139
CLR FLAG 12 L		B08V2							M7839					1-PIN RUN	140
CLR FLAG 13 L		B08F1							M7839					1-PIN RUN	141
CLR FLAG 14 L		B08U2							M7839					1-PIN RUN	142
CLR FLAG 15 L		B08V1							M7839					1-PIN RU	143
CONTROL STROBE H		C08S2		1-01					M7839	2					144
CONTROL STROBE H		C07S2		1-02					M7839	1					144
CONTROL STROBE H		C06S2		1-03					M7839	2					144
CONTROL STROBE H		C05S2		1-04					M7839	1					144
CONTROL STROBE H		D03H1		1-05					M7837						144
CONTROL STROBE H				1									13-0/8		144
D 00 H		D01N1		1-01					DM11	1					145
D 00 H		D09N1		1-02					DM11	2					145
D 00 H		E09F2		1-03					DM11						145
D 00 H				1									10-4/8		145
D 01 H		D01P1		1-01					DM11	1					146
D 01 H		D09P1		1-02					DM11	2					146
D 01 H		E09E2		1-03					DM11						146
D 01 H				1									10-2/8		146
D 02 H		D01H2		1-01					DM11	1					147
D 02 H		D09H2		1-02					DM11	2					147
D 02 H		E09H2		1-03					DM11						147
D 02 H				1									11-0/8		147
D 03 H		D01J2		1-01					DM11	1					148
D 03 H		D09J2		1-02					DM11	2					148
D 03 H		E09D2		1-03					DM11						148
D 03 H				1									10-4/8		148
DATA ENAB 00-03 H		F05K1							M7839					-PIN RUN	149
DATA ENAB 04-07 H		F06K1							M7839					1-PIN RUN	150

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
DATA ENAB 08-11 H		F07K1							M7839					1-PIN RUN	151
DATA ENAB 12-15 H		F08K1							M7839					1-PIN RUN	152
DATA NOT AVAILABLE L		C04T2		1-01					M7838	1					153
DATA NOT AVAILABLE L		F05C1		1-02					M7839	2					153
DATA NOT AVAILABLE L		F06C1		1-03					M7839	1					153
DATA NOT AVAILABLE L		F07C1		1-04					M7839	2					153
DATA NOT AVAILABLE L		F08C1		1-05					M7839						153
DATA NOT AVAILABLE L				1									17-0/8		153
DATA STROBE H		B03F1		1-01					M7837	1					154
DATA STROBE H		C02T2		1-02					M7836						154
DATA STROBE H				1									6-2/8		154
DATA STROBE L		F02E1		1-01					M7836	1					155
DATA STROBE L		F04C1		1-02					M7838						155
DATA STROBE L				1									3-4/8		155
DR 00 H		A05R2							M7839					1-PIN RUN	156
DR 01 H		A05U2							M7839					1-PIN RUN	157
DR 02 H		B05R1							M7839					1-PIN RUN	158
DR 03 H		B05U2							M7839					1-PIN RUN	159
DR 04 H		A06R2							M7839					1-PIN RUN	160
DR 05 H		A06U2							M7839					1-PIN RUN	161
DR 06 H		B06R1							M7839					1-PIN RUN	162
DR 07 H		B06U2							M7839					1-PIN RUN	163
DR 08 H		A07R2							M7839					1-PIN RUN	164
DR 09 H		A07U2							M7839					1-PIN RUN	165
DR 10 H		B07B1							M7839					1-PIN RUN	166
DR 11 H		B07U2							M7839					1-PIN RUN	167
DR 12 H		A08R2							M7839					1-PIN RUN	168
DR 13 H		A08U2							M7839					1-PIN RUN	169

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
DR 14 H		B08B1							M7839					1-PIN RUN	172
DR 15 H		B08U2							M7839					1-PIN RUN	171
EOC 00 H		F05J2							M7839					1-PIN RUN	172
EOC 01 H		E05R2							M7839					1-PIN RUN	173
EOC 02 H		E05K2							M7839					1-PIN RUN	174
EOC 03 H		E05F2							M7839					1-PIN RUN	175
EOC 04 H		F06J2							M7839					1-PIN RUN	176
EOC 05 H		E06R2							M7839					1-PIN RUN	177
EOC 06 H		E06K2							M7839					1-PIN RUN	178
EOC 07 H		E06F2							M7839					1-PIN RUN	179
EOC 08 H		F07J2							M7839					1-PIN RUN	180
EOC 09 H		E07R2							M7839					1-PIN RUN	181
EOC 10 H		E07K2							M7839					1-PIN RUN	182
EOC 11 H		E07F2							M7839					1-PIN RUN	183
EOC 12 H		F08J2							M7839					1-PIN RUN	184
EOC 13 H		E08R2							M7839					1-PIN RUN	185
EOC 14 H		E08K2							M7839					1-PIN RUN	186
EOC 15 H		E08F2							M7839					1-PIN RUN	187
EXT CLOCK		F09K2							DM11					1-PIN RUN	188
GROUND 01		F01C2		1-01					DM11	1					189
GROUND 01		F01J2		1-02					DM11						189
GROUND 01				1									3-0/8		189
GROUND 02		E01A1		1-01					DM11	1					190
GROUND 02		E01C2		1-02					DM11						190
GROUND 02				1									2-6/8		190

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
GROUND 09		F09B2		1-01					DM11		1				191
GROUND 09		F09C2		1-02					DM11						191
GROUND 09				1									2-4/8		191
GROUP 0-7 H		D09R2		1-01					DM11		1				192
GROUP 0-7 H		D09S2		1-02					DM11		2				192
GROUP 0-7 H		D09U1		1-03					DM11		1				192
GROUP 0-7 H		D09V1		1-04					DM11		2				192
GROUP 0-7 H		E09P1		1-05					DM11						192
GROUP 0-7 H				1									12-0/8		192
GROUP 8-15 H		D01R2		1-01					DM11		1				193
GROUP 8-15 H		D01S2		1-02					DM11		2				193
GROUP 8-15 H		D01U1		1-03					DM11		1				193
GROUP 8-15 H		D01V1		1-04					DM11		2				193
GROUP 8-15 H		E09F1		1-05					DM11		1				193
GROUP 8-15 H		F09V2		1-06					DM11						193
GROUP 8-15 H				1									21-2/8		193
IN HIGH		E01M1		1-01					DM11		1				194
IN HIGH		E09E2		1-02					DM11						194
IN HIGH				1									7-4/8		194
INH CLK L		F09H2							DM11					1-PIN RUN	195
INIT 01 L		E04B2		1-01					M7838		2				196
INIT 01 L		E02S2		1-02					M7836		1				196
INIT 01 L		E05V2		1-03					M7839		2				196
INIT 01 L		E06V2		1-04					M7839		1				196
INIT 01 L		E07V2		1-05					M7839		2				196
INIT 01 L		E08V2		1-06					M7839						196
INIT 01 L				1									17-0/8		196
INIT 02 L		A04V1		1-01					M7838		1				197
INIT 02 L		D03E2		1-02					M7837						197
INIT 02 L				1									9-0/8		197
INST DECODER ENAB A L		C03J2		1-01					M7837		1				198
INST DECODER ENAB A L		F04B1		1-02					M7838						198
INST DECODER ENAB A L				1									9-6/8		198
INT A H		F01D2		1-01					DM11		2				199
INT A H		F01H2		1-02					DM11		1				199
INT A H		F01K2		1-03					DM11		2				199
INT A H		F09N2		1-04					DM11						199
INT A H				1									12-0/8		199

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
INTR DONE B H		F01N2		1-01					DM11		1				200
INTR DONE B H		F01S1		1-02					DM11						200
INTR DONE B H				1									3-0/8		200
INTR MAINT 00-03 H		B05E2							M7839					1-PIN RUN	201
INTR MAINT 04-07 H		B06E2							M7839					1-PIN RUN	202
INTR MAINT 08-11 H		B07E2							M7839					1-PIN RUN	203
INTR MAINT 12-15 H		B06E2							M7839					1-PIN RUN	204
INTR RCV DATA 00-03 L		B05C1							M7839					1-PIN RUN	205
INTR RCV DATA 04-07 L		B06C1							M7839					1-PIN RUN	206
INTR RCV DATA 08-11 L		B07C1							M7839					1-PIN RUN	207
INTR RCV DATA 12-15 L		B08C1							M7839					1-PIN RUN	208
INTR TEST H		F09M1							DM11					1-PIN RUN	209
LCR 00 H		A08P2		1-01					M7839		2				210
LCR 00 H		A07P2		1-02					M7839		1				210
LCR 00 H		A06P2		1-03					M7839		2				210
LCR 00 H		A05P2		1-04					M7839		1				210
LCR 00 H		C03J1		1-05					M7837						210
LCR 00 H				1									15-6/8		210
LCR 10 H		C03D2		1-01					M7837		1				211
LCR 10 H		D05T2		1-02					M7839		2				211
LCR 10 H		D06T2		1-03					M7839		1				211
LCR 10 H		D07T2		1-04					M7839		2				211
LCR 10 H		D08T2		1-05					M7839						211
LCR 10 H				1									15-2/8		211
LCR 11 H		A05N2		1-01					M7839		2				212
LCR 11 H		A06N2		1-02					M7839		1				212
LCR 11 H		A07N2		1-03					M7839		2				212
LCR 11 H		A08N2		1-04					M7839		1				212
LCR 11 H		C03H1		1-05					M7837						212
LCR 11 H				1									15-6/8		212

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
LCR 12 H		A06M2		1-01					M7839		2				213
LCR 12 H		A07M2		1-02					M7839		1				213
LCR 12 H		A06M2		1-03					M7839		2				213
LCR 12 H		A05M2		1-04					M7839		1				213
LCR 12 H		B03V1		1-05					M7837						213
LCR 12 H				1									14-6/8		213
LCR 13 H		B08A1		1-01					M7839		2				214
LCR 13 H		B07A1		1-02					M7839		1				214
LCR 13 H		B06A1		1-03					M7839		2				214
LCR 13 H		B05A1		1-04					M7839		1				214
LCR 13 H		C03E2		1-05					M7837						214
LCR 13 H				1									14-0/8		214
LCR 14 H		A08L2		1-01					M7839		2				215
LCR 14 H		A07L2		1-02					M7839		1				215
LCR 14 H		A06L2		1-03					M7839		2				215
LCR 14 H		A05L2		1-04					M7839		1				215
LCR 14 H		C03L2		1-05					M7837						215
LCR 14 H				1									16-2/8		215
LD HOLD H		F09P1		1-01					DM11		1				216
LD HOLD H		F09V1		1-02					DM11						216
LD HOLD H				1									3-0/8		216
LINE CNT + H		D01L2		1-01					DM11		1				217
LINE CNT + H		D09L2		1-02					DM11		2				217
LINE CNT + H		E09L1		1-03					DM11		1				217
LINE CNT + H		F09U1		1-04					DM11						217
LINE CNT + H				1									17-2/8		217
LINE CNT LSB H		D01M2		1-01					DM11		1				218
LINE CNT LSB H		D09M2		1-02					DM11		2				218
LINE CNT LSB H		E09M1		1-03					DM11		1				218
LINE CNT LSB H		F09S1		1-04					DM11						218
LINE CNT LSB H				1									16-6/8		218
LINE CNT MSB H		D01K2		1-01					DM11		1				219
LINE CNT MSB H		D09K2		1-02					DM11		2				219
LINE CNT MSB H		E09N1		1-03					DM11		1				219
LINE CNT MSB H		F09U2		1-04					DM11						219
LINE CNT MSB H				1									17-2/8		219
LINE INCR H		F09N1							DM11					1-PIN RUN	220

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
LOAD LCR H		C03A1		1-01					M7837		1				221
LOAD LCR H		F04P1		1-02					M7838						221
LOAD LCR H				1									12-0/8		221
LOAD SFR L		D03F1		1-01					M7837		1				222
LOAD SFR L		D04H1		1-02					M7838						222
LOAD SFR L				1									2-6/8		222
LOAD SRS HIGH BYTE H		B03L1		1-01					M7837		1				223
LOAD SRS HIGH BYTE H		D04D2		1-02					M7838						223
LOAD SRS HIGH BYTE H				1									7-2/8		223
LOAD SRS LOW BYTE H		B03K1		1-01					M7837		1				224
LOAD SRS LOW BYTE H		C04B1		1-02					M7838						224
LOAD SRS LOW BYTE H				1									4-2/8		224
MAINT CLOCK PULSE H		B03D2		1-01					M7837		1				225
MAINT CLOCK PULSE H		E05T2		1-02					M7839		2				225
MAINT CLOCK PULSE H		E06T2		1-03					M7839		1				225
MAINT CLOCK PULSE H		E07T2		1-04					M7839		2				225
MAINT CLOCK PULSE H		E08T2		1-05					M7839						225
MAINT CLOCK PULSE H				1									20-2/8		225
MASTER B L		F01P2		1-01					DM11		2				226
MASTER B L		F01R2		1-02					DM11		1				226
MASTER B L		F01S2		1-03					DM11						226
MASTER B L				1									5-0/8		226
MASTER OR L		D02A1		1-01					M7836		1				227
MASTER OR L		F05L1		1-02					M7839		2				227
MASTER OR L		F06L1		1-03					M7839		1				227
MASTER OR L		F07L1		1-04					M7839		2				227
MASTER OR L		F08L1		1-05					M7839						227
MASTER OR L				1									17-6/8		227
MASTER PE L		D02E1		1-01					M7836		1				228
MASTER PE L		F05M1		1-02					M7839		2				228
MASTER PE L		F06M1		1-03					M7839		1				228
MASTER PE L		F07M1		1-04					M7839		2				228
MASTER PE L		F08M1		1-05					M7839						228
MASTER PE L				1									17-2/8		228

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	11153 EXCEPTIONS	RUN NUMBER
MASTER SCAN 00 H		D03R1		1-01					M7837		1				229
MASTER SCAN 00 H		E08N1		1-02					M7839		2				229
MASTER SCAN 00 H		E07N1		1-03					M7839		1				229
MASTER SCAN 00 H		E06N1		1-04					M7839		2				229
MASTER SCAN 00 H		E05N1		1-05					M7839		1				229
MASTER SCAN 00 H		F02D2		1-06					M7836		2				229
MASTER SCAN 00 H		F04T2		1-07					M7838						229
MASTER SCAN 00 H				1									23-0/8		229
MASTER SCAN 01 H		D03P1		1-01					M7837		2				230
MASTER SCAN 01 H		D04L2		1-02					M7838		1				230
MASTER SCAN 01 H		E05M1		1-03					M7839		2				230
MASTER SCAN 01 H		E06M1		1-04					M7839		1				230
MASTER SCAN 01 H		E08M1		1-05					M7839		2				230
MASTER SCAN 01 H		E07M1		1-06					M7839		1				230
MASTER SCAN 01 H		F02F2		1-07					M7836						230
MASTER SCAN 01 H				1									22-6/8		230
MASTER SCAN 02 H		D02E2		1-01					M7836		1				231
MASTER SCAN 02 H		D04N2		1-02					M7838		2				231
MASTER SCAN 02 H		D03N1		1-03					M7837		1				231
MASTER SCAN 02 H		E08N2		1-04					M7839		2				231
MASTER SCAN 02 H		E06N2		1-05					M7839						231
MASTER SCAN 02 H				1									16-2/8		231
MASTER SCAN 03 H		D04N1		1-01					M7838		2				232
MASTER SCAN 03 H		D03M1		1-02					M7837		1				232
MASTER SCAN 03 H		E08U2		1-03					M7839		2				232
MASTER SCAN 03 H		E07U2		1-04					M7839		1				232
MASTER SCAN 03 H		F02H1		1-05					M7836						232
MASTER SCAN 03 H				1									10-2/8		232
MASTER SCAN 04 H		D04P1		1-01					M7838		1				233
MASTER SCAN 04 H		E05N2		1-02					M7839		2				233
MASTER SCAN 04 H		E07N2		1-03					M7839						233
MASTER SCAN 04 H				1									8-2/8		233
MASTER SCAN 05 H		D04N2		1-01					M7838		1				234
MASTER SCAN 05 H		E05U2		1-02					M7839		2				234
MASTER SCAN 05 H		E06U2		1-03					M7839						234
MASTER SCAN 05 H				1									8-4/8		234

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	11153 EXCEPTIONS	RUN NUMBER
MASTER SCAN I/R		C08R2		1-01					M7839		2				235
MASTER SCAN I/R		C07R2		1-02					M7839		1				235
MASTER SCAN I/R		C06R2		1-03					M7839		2				235
MASTER SCAN I/R		C05R2		1-04					M7839		1				235
MASTER SCAN I/R		F04U2		1-05					M7838						235
MASTER SCAN I/R				1									19-2/8		235
MATCH DETECT L		C04R1		1-01					M7838		1				236
MATCH DETECT L		F05E1		1-02					M7839		2				236
MATCH DETECT L		F06E1		1-03					M7839		1				236
MATCH DETECT L		F07E1		1-04					M7839		2				236
MATCH DETECT L		F08E1		1-05					M7839						236
MATCH DETECT L				1									17-6/8		236
MDET 00 H		A05V2							M7839					1-PIN RUN	237
MDET 01 H		B05H1							M7839					1-PIN RUN	238
MDET 02 H		B05J2							M7839					1-PIN RUN	239
MDET 03 H		B05P2							M7839					1-PIN RUN	240
MDET 04 H		A06V2							M7839					1-PIN RUN	241
MDET 05 H		B06H1							M7839					1-PIN RUN	242
MDET 06 H		B06J2							M7839					1-PIN RUN	243
MDET 07 H		B06P2							M7839					1-PIN RUN	244
MDET 08 H		A07V2							M7839					1-PIN RUN	245
MDET 09 H		B07H1							M7839					1-PIN RUN	246
MDET 10 H		B07J2							M7839					1-PIN RUN	247
MDET 11 H		B07P2							M7839					1-PIN RUN	248
MDET 12 H		A08V2							M7839					1-PIN RUN	249
MDET 13 H		B08H1							M7839					1-PIN RUN	250
MDET 14 H		B08J2							M7839					1-PIN RUN	251
MDET 15 H		B08P2							M7839					1-PIN RUN	252

A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
	MEM PAR ERR H		CR4P1		1-01			M7838		1				253
	MEM PAR ERR H		FV2P2		1-02			M7838						253
	MEM PAR ERR H				1									253
												10-6/8		
	MUX 0-7 EN H		DV9N2		1-01			DM11		2				254
	MUX 0-7 EN H		D09S1		1-02			DM11		1				254
	MUX 0-7 EN H		DV9V2		1-03			DM11						254
	MUX 0-7 EN H				1									254
												6-0/8		
	MUX 8-15 EN H		DV1N2		1-01			DM11		2				255
	MUX 8-15 EN H		D01S1		1-02			DM11		1				255
	MUX 8-15 EN H		D01V2		1-03			DM11						255
	MUX 8-15 EN H				1									255
												6-0/8		
	MUX CARRIER L		D0181		1-01			DM11		1				256
	MUX CARRIER L		D0981		1-02			DM11		2				256
	MUX CARRIER L		EV9A1		1-03			DM11						256
	MUX CARRIER L				1									256
												11-0/8		
	MUX CLOCK 00-03 H		E05S2					M7839					1-PIN RUN	257
	MUX CLOCK 04-07 H		EV6S2					M7839					1-PIN RUN	258
	MUX CLOCK 08-11 H		EV7S2					M7839					1-PIN RUN	259
	MUX CLOCK 12-15 H		FV8S2					M7839					1-PIN RUN	260
	MUX CLR TO SEND L		DV1C1		1-01			DM11		1				261
	MUX CLR TO SEND L		DV9C1		1-02			DM11		2				261
	MUX CLR TO SEND L		EV9D1		1-03			DM11						261
	MUX CLR TO SEND L				1									261
												11-2/8		
	MUX DATA SET READY L		DV1A1		1-01			DM11		1				262
	MUX DATA SET READY L		D09A1		1-02			DM11		2				262
	MUX DATA SET READY L		E09B1		1-03			DM11						262
	MUX DATA SET READY L				1									262
												11-2/8		
	MUX DATA TERM READY L		DV1F1		1-01			DM11		1				263
	MUX DATA TERM READY L		DV9F1		1-02			DM11		2				263
	MUX DATA TERM READY L		EV9S2		1-03			DM11						263
	MUX DATA TERM READY L				1									263
												12-2/8		
	MUX LINE EN L		DV1K1		1-01			DM11		1				264
	MUX LINE EN L		DV9K1		1-02			DM11		2				264
	MUX LINE EN L		EV9P2		1-03			DM11						264
	MUX LINE EN L				1									264
												11-6/8		

A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
	MUX NEW SYNC L		D01L1		1-01			DM11		1				26
	MUX NEW SYNC L		D09L1		1-02			DM11		2				26
	MUX NEW SYNC L		E09R2		1-03			DM11						26
	MUX NEW SYNC L				1									26
												11-6/8		
	MUX RING L		D01F2		1-01			DM11		1				26
	MUX RING L		DV9F2		1-02			DM11		2				26
	MUX RING L		EV9C1		1-03			DM11						26
	MUX RING L				1									26
												11-0/8		
	MUX RQ TO SEND L		DV1H1		1-01			DM11		1				26
	MUX RQ TO SEND L		D09H1		1-02			DM11		2				26
	MUX RQ TO SEND L		E09N2		1-03			DM11						26
	MUX RQ TO SEND L				1									26
												12-0/8		
	NPR ADDR 00 H		CV2H2		1-01			M7836		1				26
	NPR ADDR 00 H		CV3C1		1-02			M7837						26
	NPR ADDR 00 H				1									26
												3-0/8		
	NPR ADDRESS REG CLK L		B14J2		1-01			M7838		1				26
	NPR ADDRESS REG CLK L		CV2B1		1-02			M7836						26
	NPR ADDRESS REG CLK L				1									26
												4-6/8		
	NPR DATO 00 H		CV3V1		1-01			M7837		1				27
	NPR DATO 00 H		E02K1		1-02			M7836						27
	NPR DATO 00 H				1									27
												6-6/8		
	NPR DATO 01 H		CV3P2		1-01			M7837		1				271
	NPR DATO 01 H		E02D2		1-02			M7836						271
	NPR DATO 01 H				1									271
												6-6/8		
	NPR DATO 02 H		CV3B1		1-01			M7837		1				272
	NPR DATO 02 H		DV2F2		1-02			M7836						272
	NPR DATO 02 H				1									272
												5-0/8		
	NPR DATO 03 H		CV3R1		1-01			M7837		1				273
	NPR DATO 03 H		EV2F2		1-02			M7836						273
	NPR DATO 03 H				1									273
												6-6/8		
	NPR DATO 04 H		CV2F2		1-01			M7836		1				274
	NPR DATO 04 H		CV3T2		1-02			M7837						274
	NPR DATO 04 H				1									274
												3-6/8		
	NPR DATO 05 H		CV3M2		1-01			M7837		1				275
	NPR DATO 05 H		E02H2		1-02			M7836						275
	NPR DATO 05 H				1									275
												7-2/8		

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
NPR DATO 06 H		A02F1		1-01				M7836		1				276
NPR DATO 06 H		C03M1		1-02				M7837						276
NPR DATO 06 H				1								5-6/8		276
NPR DATO 07 H		C03U1		1-01				M7837		1				277
NPR DATO 07 H		F02N2		1-02				M7836						277
NPR DATO 07 H				1								7-0/8		277
NPR DATO REG CLK L		A02U1		1-01				M7836		2				278
NPR DATO REG CLK L		H04E1		1-02				M7838		1				278
NPR DATO REG CLK L		D03J2		1-03				M7837						278
NPR DATO REG CLK L				1								12-0/8		278
NPR OPERATION L		E03T2		1-01				M7838		1				279
NPR OPERATION L		F03K1		1-02				M7837						279
NPR OPERATION L				1								4-4/8		279
NPR SILO NOT AVAIL H		D03K2		1-01				M7837		1				280
NPR SILO NOT AVAIL H		F04J1		1-02				M7838						280
NPR SILO NOT AVAIL H				1								5-0/8		280
NPR STAT REP REG CLK L		H03P1		1-01				M7837		1				281
NPR STAT REP REG CLK L		H04R1		1-02				M7838						281
NPR STAT REP REG CLK L				1								4-0/8		281
NXM H		F03K1		1-01				M7837		1				282
NXM H		F04J2		1-02				M7838						282
NXM H				1								3-2/8		282
OUT LOW H		E01N1		1-01				DM11		2				283
OUT LOW H		D01U2		1-02				DM11		1				283
OUT LOW H		D09U2		1-03				DM11		2				283
OUT LOW H		F09J2		1-04				DM11						283
OUT LOW H				1								17-0/8		283
RAM OUTPUT 00 H		A04H2		1-01				M7838		1				284
RAM OUTPUT 00 H		F02D1		1-02				M7836						284
RAM OUTPUT 00 H				1								13-0/8		284
RAM OUTPUT 01 H		B04A1		1-01				M7838		1				285
RAM OUTPUT 01 H		E02J1		1-02				M7836						285
RAM OUTPUT 01 H				1								11-2/8		285
RAM OUTPUT 02 H		C04V1		1-01				M7838		1				286
RAM OUTPUT 02 H		E02U2		1-02				M7836						286
RAM OUTPUT 02 H				1								7-6/8		286

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
RAM OUTPUT 03 H		C04V2		1-01				M7838		1				287
RAM OUTPUT 03 H		E02L1		1-02				M7836						287
RAM OUTPUT 03 H				1								7-2/8		287
RAM OUTPUT 03 L		B04K2		1-01				M7838		1				288
RAM OUTPUT 03 L		D02V2		1-02				M7836						288
RAM OUTPUT 03 L				1								9-0/8		288
RAM OUTPUT 04 H		C02D2		1-01				M7836		1				289
RAM OUTPUT 04 H		C04U1		1-02				M7838						289
RAM OUTPUT 04 H				1								4-2/8		289
RAM OUTPUT 05 H		D04C1		1-01				M7838		1				290
RAM OUTPUT 05 H		E02E1		1-02				M7836						290
RAM OUTPUT 05 H				1								5-4/8		290
RAM OUTPUT 06 H		B02D1		1-01				M7836		1				291
RAM OUTPUT 06 H		D04A1		1-02				M7838						291
RAM OUTPUT 06 H				1								7-4/8		291
RAM OUTPUT 07 H		A04L2		1-01				M7838		1				292
RAM OUTPUT 07 H		E02K2		1-02				M7836						292
RAM OUTPUT 07 H				1								13-2/8		292
RAM OUTPUT 08 H		A04E2		1-01				M7838		1				293
RAM OUTPUT 08 H		E02L2		1-02				M7836						293
RAM OUTPUT 08 H				1								13-6/8		293
RAM OUTPUT 09 H		A04R2		1-01				M7838		1				294
RAM OUTPUT 09 H		E02E2		1-02				M7836						294
RAM OUTPUT 09 H				1								12-2/8		294
RAM OUTPUT 10 H		A04D2		1-01				M7838		1				295
RAM OUTPUT 10 H		E02P2		1-02				M7836						295
RAM OUTPUT 10 H				1								14-4/8		295
RAM OUTPUT 11 H		A04C1		1-01				M7838		1				296
RAM OUTPUT 11 H		F02V1		1-02				M7836						296
RAM OUTPUT 11 H				1								17-6/8		296
RAM OUTPUT 12 H		A02N1		1-01				M7836		1				297
RAM OUTPUT 12 H		E04F1		1-02				M7838						297
RAM OUTPUT 12 H				1								12-2/8		297
RAM OUTPUT 13 H		A02P1		1-01				M7836		1				298
RAM OUTPUT 13 H		D04R1		1-02				M7838						298
RAM OUTPUT 13 H				1								11-0/8		298

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
RAM OUTPUT 14 H		B02C1		1-01				M7836			1				299
RAM OUTPUT 14 H		E04D2		1-02				M7838							299
RAM OUTPUT 14 H				1									10-6/8		299
RAM OUTPUT 15 H		A02R2		1-01				M7836			1				300
RAM OUTPUT 15 H		E04B1		1-02				M7838							300
RAM OUTPUT 15 H				1									11-6/8		300
RAM OUTPUT 16 H		A02L2		1-01				M7836			1				301
RAM OUTPUT 16 H		E04F2		1-02				M7838							301
RAM OUTPUT 16 H				1									12-6/8		301
RAM OUTPUT 17 H		A02T2		1-01				M7836			1				302
RAM OUTPUT 17 H		E04F1		1-02				M7838							302
RAM OUTPUT 17 H				1									12-0/8		302
RAM OUTPUT DATA CLK H		D03L1		1-01				M7837			1				303
RAM OUTPUT DATA CLK H		D04H2		1-02				M7838							303
RAM OUTPUT DATA CLK H				1									3-2/8		303
RAM UNIDATA 00 H		A04K1		1-01				M7838			1				304
RAM UNIDATA 00 H		F03F1		1-02				M7837							304
RAM UNIDATA 00 H				1									15-4/8		304
RAM UNIDATA 01 H		A04H1		1-01				M7838			1				305
RAM UNIDATA 01 H		F03U2		1-02				M7837							305
RAM UNIDATA 01 H				1									16-4/8		305
RAM UNIDATA 02 H		B04F1		1-01				M7838			1				306
RAM UNIDATA 02 H		E03S1		1-02				M7837							306
RAM UNIDATA 02 H				1									11-4/8		306
RAM UNIDATA 03 H		B04J1		1-01				M7838			1				307
RAM UNIDATA 03 H		E03U1		1-02				M7837							307
RAM UNIDATA 03 H				1									11-4/8		307
RAM UNIDATA 04 H		A04P1		1-01				M7838			1				308
RAM UNIDATA 04 H		F03H1		1-02				M7837							308
RAM UNIDATA 04 H				1									15-0/8		308
RAM UNIDATA 05 H		A04L1		1-01				M7838			1				309
RAM UNIDATA 05 H		F03U1		1-02				M7837							309
RAM UNIDATA 05 H				1									16-6/8		309
RAM UNIDATA 06 H		A04F1		1-01				M7838			1				310
RAM UNIDATA 06 H		F03C1		1-02				M7837							310
RAM UNIDATA 06 H				1									15-4/8		310

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
RAM UNIDATA 07 H		A04J1		1-01				M7838			1				311
RAM UNIDATA 07 H		F03J1		1-02				M7837							311
RAM UNIDATA 07 H				1									15-6/8		311
RAM UNIDATA 08 H		A04H1		1-01				M7838			1				312
RAM UNIDATA 08 H		E03P1		1-02				M7837							312
RAM UNIDATA 08 H				1									13-6/8		312
RAM UNIDATA 09 H		A04D1		1-01				M7838			1				313
RAM UNIDATA 09 H		E03P2		1-02				M7837							313
RAM UNIDATA 09 H				1									14-2/8		313
RAM UNIDATA 10 H		A04B1		1-01				M7838			1				314
RAM UNIDATA 10 H		F03S2		1-02				M7837							314
RAM UNIDATA 10 H				1									17-4/8		314
RAM UNIDATA 11 H		A04E1		1-01				M7838			1				315
RAM UNIDATA 11 H		F03H2		1-02				M7837							315
RAM UNIDATA 11 H				1									16-0/8		315
RAM UNIDATA 12 H		F03V1		1-01				M7837			1				316
RAM UNIDATA 12 H		F04J1		1-02				M7838							316
RAM UNIDATA 12 H				1									3-6/8		316
RAM UNIDATA 13 H		F03L1		1-01				M7837			1				317
RAM UNIDATA 13 H		F04H1		1-02				M7838							317
RAM UNIDATA 13 H				1									3-0/8		317
RAM UNIDATA 14 H		E03V1		1-01				M7837			1				318
RAM UNIDATA 14 H		F04F1		1-02				M7838							318
RAM UNIDATA 14 H				1									3-6/8		318
RAM UNIDATA 15 H		E03R2		1-01				M7837			1				319
RAM UNIDATA 15 H		F04R1		1-02				M7838							319
RAM UNIDATA 15 H				1									4-6/8		319
RAM UNIDATA 16 H		F03B1		1-01				M7837			1				320
RAM UNIDATA 16 H		F04M1		1-02				M7838							320
RAM UNIDATA 16 H				1									3-6/8		320
RAM UNIDATA 17 H		F03R2		1-01				M7837			1				321
RAM UNIDATA 17 H		F04U1		1-02				M7838							321
RAM UNIDATA 17 H				1									2-6/8		321
RCV IN 00 H		B05F2						M7839						1-PIN RUN	322

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
RCV IN 01 H		B05D1						M7839						1-PIN RUN	323
RCV IN 02 H		B05K2						M7839						1-PIN RUN	324
RCV IN 03 H		B05K1						M7839						1-PIN RUN	325
RCV IN 04 H		B06F2						M7839						1-PIN RUN	326
RCV IN 05 H		B06D1						M7839						1-PIN RUN	327
RCV IN 06 H		B06K2						M7839						1-PIN RUN	328
RCV IN 07 H		B06K1						M7839						1-PIN RUN	329
RCV IN 08 H		B07F2						M7839						1-PIN RUN	330
RCV IN 09 H		B07D1						M7839						1-PIN RUN	331
RCV IN 10 H		B07K2						M7839						1-PIN RUN	332
RCV IN 11 H		B07K1						M7839						1-PIN RUN	333
RCV IN 12 H		B08F2						M7839						1-PIN RUN	334
RCV IN 13 H		B08D1						M7839						1-PIN RUN	335
RCV IN 14 H		B08K2						M7839						1-PIN RUN	336
RCV IN 15 H		B08K1						M7839						1-PIN RUN	337
RCVR CHAR WAITING H		E04N2	1-01					M7838	1						338
RCVD CHAR WAITING H		F02A1	1-02					M7836							338
RCVD CHAR WAITING H			1									4-2/8			338
RDE 20-23 H		F05U1						M7839						1-PIN RUN	339
RDE 24-27 H		F06U1						M7839						1-PIN RUN	340
RDE 30-33 H		F07U1						M7839						1-PIN RUN	341
RDE 32-35 H		F08U1						M7839						1-PIN RUN	342
READY IN L		D04L1	1-01					M7838	1						343
READY IN L		F02K2	1-02					M7836							343
READY IN L			1									7-6/8			343

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
RECEIVED DATA ENABLE H		C08N2	1-01					M7839			2				344
RECEIVED DATA ENABLE H		C07N2	1-02					M7839			1				344
RECEIVED DATA ENABLE H		C06N2	1-03					M7839			2				344
RECEIVED DATA ENABLE H		C05N2	1-04					M7839			1				344
RECEIVED DATA ENABLE H		F02R2	1-05					M7836							344
RECEIVED DATA ENABLE H			1									19-4/8			344
RECEIVER FLAG L		F02K1	1-01					M7836			1				345
RECEIVER FLAG L		F05M2	1-02					M7839			2				345
RECEIVER FLAG L		F06M2	1-03					M7839			1				345
RECEIVER FLAG L		F07M2	1-04					M7839			2				345
RECEIVER FLAG L		F08M2	1-05					M7839							345
RECEIVER FLAG L			1									12-4/8			345
RECEIVER FLAG WAITING		E04K2	1-01					M7838	1						346
RECEIVER FLAG WAITING		F02J2	1-02					M7836							346
RECEIVER FLAG WAITING			1									5-2/8			346
RECV DATA 00 L		F02N2	1-01					M7836			1				347
RECV DATA 00 L		F05P2	1-02					M7839			2				347
RECV DATA 00 L		F06P2	1-03					M7839			1				347
RECV DATA 00 L		F07P2	1-04					M7839			2				347
RECV DATA 00 L		F08P2	1-05					M7839							347
RECV DATA 00 L			1									12-0/8			347
RECV DATA 01 L		F02N1	1-01					M7836			1				348
RECV DATA 01 L		F05N2	1-02					M7839			2				348
RECV DATA 01 L		F06N2	1-03					M7839			1				348
RECV DATA 01 L		F07N2	1-04					M7839			2				348
RECV DATA 01 L		F08N2	1-05					M7839							348
RECV DATA 01 L			1									12-2/8			348
RECV DATA 02 L		F02J1	1-01					M7836			1				349
RECV DATA 02 L		F05P1	1-02					M7839			2				349
RECV DATA 02 L		F06P1	1-03					M7839			1				349
RECV DATA 02 L		F07P1	1-04					M7839			2				349
RECV DATA 02 L		F08P1	1-05					M7839							349
RECV DATA 02 L			1									12-2/8			349
RECV DATA 03 L		F02F1	1-01					M7836			1				350
RECV DATA 03 L		F05F1	1-02					M7839			2				350
RECV DATA 03 L		F06F1	1-03					M7839			1				350
RECV DATA 03 L		F07F1	1-04					M7839			2				350
RECV DATA 03 L		F08F1	1-05					M7839							350
RECV DATA 03 L			1									12-4/8			350

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
RECV DATA 04 L		F02L2		1-01				M7836		1					351
RECV DATA 04 L		F05S1		1-02				M7839		2					351
RECV DATA 04 L		F06S1		1-03				M7839		1					351
RECV DATA 04 L		F07S1		1-04				M7839		2					351
RECV DATA 04 L		F08S1		1-05				M7839							351
RECV DATA 04 L				1									12-0/8		351
RECV DATA 05 L		F02M2		1-01				M7836		1					352
RECV DATA 05 L		F05R1		1-02				M7839		2					352
RECV DATA 05 L		F06R1		1-03				M7839		1					352
RECV DATA 05 L		F07R1		1-04				M7839		2					352
RECV DATA 05 L		F08R1		1-05				M7839							352
RECV DATA 05 L				1									12-2/8		352
RECV DATA 06 L		F02H2		1-01				M7836		1					353
RECV DATA 06 L		F05J1		1-02				M7839		2					353
RECV DATA 06 L		F06J1		1-03				M7839		1					353
RECV DATA 06 L		F07J1		1-04				M7839		2					353
RECV DATA 06 L		F08J1		1-05				M7839							353
RECV DATA 06 L				1									12-0/8		353
RECV DATA 07 L		D02D2		1-01				M7836		1					354
RECV DATA 07 L		F05H1		1-02				M7839		2					354
RECV DATA 07 L		F06H1		1-03				M7839		1					354
RECV DATA 07 L		F07H1		1-04				M7839		2					354
RECV DATA 07 L		F08H1		1-05				M7839							354
RECV DATA 07 L				1									16-6/8		354
REQUEST BUS H		B03F2		1-01				M7837		1					355
REQUEST BUS H		C04S1		1-02				M7838							355
REQUEST BUS H				1									6-0/8		355
RESYNC 1 00(0) H		C05V2						M7839						1-PIN RUN	356
RESYNC 1 01(0) H		B05H2						M7839						1-PIN RUN	357
RESYNC 1 02(0) H		D05N2						M7839						1-PIN RUN	358
RESYNC 1 03(0) H		C05K2						M7839						1-PIN RUN	359
RESYNC 1 04(0) H		C06V2						M7839						1-PIN RUN	360
RESYNC 1 05(0) H		B06H2						M7839						1-PIN RUN	361
RESYNC 1 06(0) H		D06N2						M7839						1-PIN RUN	362

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
RESYNC 1 07(0) H		C06K2						M7839						1-PIN RUN	363
RESYNC 1 08(0) H		C07V2						M7839						1-PIN RUN	364
RESYNC 1 09(0) H		B07H2						M7839						1-PIN RUN	365
RESYNC 1 10(0) H		D07N2						M7839						1-PIN RUN	366
RESYNC 1 11(0) H		C07K2						M7839						1-PIN RUN	367
RESYNC 1 12(0) H		C08V2						M7839						1-PIN RUN	368
RESYNC 1 13(0) H		B08N2						M7839						1-PIN RUN	369
RESYNC 1 14(0) H		D08N2						M7839						1-PIN RUN	370
RESYNC 1 15(0) H		C08K2						M7839						1-PIN RUN	371
RESYNC 2 00(0) H		D05D2						M7839						1-PIN RUN	372
RESYNC 2 01(0) H		C05F2						M7839						1-PIN RUN	373
RESYNC 2 02(0) H		D05R2						M7839						1-PIN RUN	374
RESYNC 2 03(0) H		C05M2						M7839						1-PIN RUN	375
RESYNC 2 04(0) H		D06D2						M7839						1-PIN RUN	376
RESYNC 2 05(0) H		C06F2						M7839						1-PIN RUN	377
RESYNC 2 06(0) H		D06R2						M7839						1-PIN RUN	378
RESYNC 2 07(0) H		C06M2						M7839						1-PIN RUN	379
RESYNC 2 08(0) H		D07D2						M7839						1-PIN RUN	380
RESYNC 2 09(0) H		C07F2						M7839						1-PIN RUN	381
RESYNC 2 10(0) H		D07R2						M7839						1-PIN RUN	382
RESYNC 2 11(0) H		C07M2						M7839						1-PIN RUN	383
RESYNC 2 12(0) H		D08D2						M7839						1-PIN RUN	384
RESYNC 2 13(0) H		C08F2						M7839						1-PIN RUN	385

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
RESYNC 2 14(0) H		D08R2							M7839					1=PIN RUN	386
RESYNC 2 15(0) H		C08P2							M7839					1=PIN RUN	387
RESYNC PULSE 00 L		D05L2							M7839					1=PIN RUN	388
RESYNC PULSE 01 L		D05K2							M7839					1=PIN RUN	389
RESYNC PULSE 02 L		D05J2							M7839					1=PIN RUN	390
RESYNC PULSE 03 L		D05H2							M7839					1=PIN RUN	391
RESYNC PULSE 04 L		D06L2							M7839					1=PIN RUN	392
RESYNC PULSE 05 L		D06K2							M7839					1=PIN RUN	393
RESYNC PULSE 06 H		D06J2							M7839					1=PIN RUN	394
RESYNC PULSE 07 L		D06H2							M7839					1=PIN RUN	395
RESYNC PULSE 08 L		D07L2							M7839					1=PIN RUN	396
RESYNC PULSE 09 L		D07K2							M7839					1=PIN RUN	397
RESYNC PULSE 10 L		D07J2							M7839					1=PIN RUN	398
RESYNC PULSE 11 L		D07H2							M7839					1=PIN RUN	399
RESYNC PULSE 12 L		D08L2							M7839					1=PIN RUN	400
RESYNC PULSE 13 L		D08K2							M7839					1=PIN RUN	401
RESYNC PULSE 14 L		D08J2							M7839					1=PIN RUN	402
RESYNC PULSE 15 L		D08H2							M7839					1=PIN RUN	403
															404
RESYNC PULSE L		A02C1		1-01					M7836	1					404
RESYNC PULSE L		C04E2		1-02					M7838	2					404
RESYNC PULSE L		D05F2		1-03					M7839	1					404
RESYNC PULSE L		D06F2		1-04					M7839	2					404
RESYNC PULSE L		D07F2		1-05					M7839	1					404
RESYNC PULSE L		D08F2		1-06					M7839						404
RESYNC PULSE L				1									22-2/8		404
															405
RICR CLOCK L		B04E2		1-01					M7838	1					405
RICR CLOCK L		D03D1		1-02					M7837						405
RICR CLOCK L				1									7-6/8		405

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
															406
RIRR 00 H		E02N1		1-01					M7836	1					406
RIRR 00 H		F03D2		1-02					M7837						406
RIRR 00 H				1									4-4/8		406
															407
RIRR 01 H		D03H1		1-01					M7837	1					407
RIRR 01 H		E02M2		1-02					M7836						407
RIRR 01 H				1									6-2/8		407
															408
RIRR 02 H		D03A1		1-01					M7837	1					408
RIRR 02 H		E02R2		1-02					M7836						408
RIRR 02 H				1									6-4/8		408
															409
RIRR 03 H		D03E1		1-01					M7837	1					409
RIRR 03 H		E02D1		1-02					M7836						409
RIRR 03 H				1									7-6/8		409
															410
RIRR 04 H		A02M2		1-01					M7836	1					410
RIRR 04 H		F03B2		1-02					M7837						410
RIRR 04 H				1									14-6/8		410
															411
RIRR 05 H		A02R1		1-01					M7836	1					411
RIRR 05 H		F03N1		1-02					M7837						411
RIRR 05 H				1									15-4/8		411
															412
RIRR 06 H		F02R1		1-01					M7836	1					412
RIRR 06 H		D03H1		1-02					M7837						412
RIRR 06 H				1									9-6/8		412
															413
RIRR 07 H		A02U2		1-01					M7836	1					413
RIRR 07 H		F03K2		1-02					M7837						413
RIRR 07 H				1									14-6/8		413
															414
ROM DATA 00 H		B04C1		1-01					M7838	2					414
ROM DATA 00 H		D03C1		1-02					M7837	1					414
ROM DATA 00 H		F02M1		1-03					M7836						414
ROM DATA 00 H				1									16-4/8		414
															415
ROM DATA 01 H		B04D1		1-01					M7838	2					415
ROM DATA 01 H		D03D2		1-02					M7837	1					415
ROM DATA 01 H		F02R1		1-03					M7836						415
ROM DATA 01 H				1									17-0/8		415
															416
ROM DATA 02 H		B04D2		1-01					M7838	1					416
ROM DATA 02 H		D03M2		1-02					M7837	2					416
ROM DATA 02 H		F02V2		1-03					M7836						416
ROM DATA 02 H				1									17-4/8		416

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
ROM DATA 03 H		R04L1		1-01					M7838		1				417
ROM DATA 03 H		E03T2		1-02					M7837		2				417
ROM DATA 03 H		F02S1		1-03					M7836						417
ROM DATA 03 H				1									16-2/8		417
ROM DATA 04 H		C04R2		1-01					M7838		1				418
ROM DATA 04 H		E02V1		1-02					M7836		2				418
ROM DATA 04 H		F03E2		1-03					M7837						418
ROM DATA 04 H				1									12-4/8		418
ROM DATA 05 H		C04E1		1-01					M7838		1				419
ROM DATA 05 H		F02T2		1-02					M7836		2				419
ROM DATA 05 H		F03S1		1-03					M7837						419
ROM DATA 05 H				1									14-2/8		419
ROM DATA 06 H		C04F1		1-01					M7838		1				420
ROM DATA 06 H		E02U1		1-02					M7836		2				420
ROM DATA 06 H		F03A1		1-03					M7837						420
ROM DATA 06 H				1									12-6/8		420
ROM DATA 07 H		C04H2		1-01					M7838		2				421
ROM DATA 07 H		D02S2		1-02					M7836		1				421
ROM DATA 07 H		F03M2		1-03					M7837						421
ROM DATA 07 H				1									13-6/8		421
ROM DATA 08 H		A02A1		1-01					M7836		1				422
ROM DATA 08 H		E04D1		1-02					M7838		2				422
ROM DATA 08 H		E03K2		1-03					M7837						422
ROM DATA 08 H				1									17-0/8		422
ROM DATA 09 H		A02B1		1-01					M7836		1				423
ROM DATA 09 H		E04A1		1-02					M7838		2				423
ROM DATA 09 H		F03M2		1-03					M7837						423
ROM DATA 09 H				1									16-6/8		423
ROM DATA 10 H		C04U2		1-01					M7838		1				424
ROM DATA 10 H		F03L2		1-02					M7837						424
ROM DATA 10 H				1									9-6/8		424
ROM DATA 11 H		D04B2		1-01					M7838		1				425
ROM DATA 11 H		F03F2		1-02					M7837						425
ROM DATA 11 H				1									8-2/8		425
ROM DATA 12 H		E04R2		1-01					M7838		1				426
ROM DATA 12 H		F03M1		1-02					M7837						426
ROM DATA 12 H				1									5-0/8		426

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
ROM DATA 13 H		E04S2		1-01					M7838		1				427
ROM DATA 13 H		F03V2		1-02					M7837						427
ROM DATA 13 H				1									5-6/8		427
ROM DATA 14 H		E03V2		1-01					M7837		1				428
ROM DATA 14 H		E04S1		1-02					M7838						428
ROM DATA 14 H				1									2-6/8		428
ROM DATA 15 H		E03L1		1-01					M7837		1				429
ROM DATA 15 H		F04E2		1-02					M7838						429
ROM DATA 15 H				1									3-2/8		429
RX CLOCK 00 H		D05E2							M7839				1-PIN RUN		430
RX CLOCK 01 H		C05E2							M7839				1-PIN RUN		431
RX CLOCK 02 H		D05S2							M7839				1-PIN RUN		432
RX CLOCK 03 H		C05P2							M7839				1-PIN RUN		433
RX CLOCK 04 H		D06E2							M7839				1-PIN RUN		434
RX CLOCK 05 H		C06B2							M7839				1-PIN RUN		435
RX CLOCK 06 H		D06S2							M7839				1-PIN RUN		436
RX CLOCK 07 H		C06P2							M7839				1-PIN RUN		437
RX CLOCK 08 H		D07E2							M7839				1-PIN RUN		438
RX CLOCK 09 H		C07B2							M7839				1-PIN RUN		439
RX CLOCK 10 H		D07S2							M7839				1-PIN RUN		440
RX CLOCK 11 H		C07P2							M7839				1-PIN RUN		441
RX CLOCK 12 H		D08E2							M7839				1-PIN RUN		442
RX CLOCK 13 H		C08E2							M7839				1-PIN RUN		443
RX CLOCK 14 H		D08S2							M7839				1-PIN RUN		444
RX CLOCK 15 H		C08P2							M7839				1-PIN RUN		445
SCR 00 H		E03F1		1-01					M7837		1				446
SCR 00 H		F04A1		1-02					M7838						446
SCR 00 H				1									4-6/8		446

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
SCR 01 H		F03P1		1-01					M7837	1					447
SCR 01 H		F04F2		1-02					M7838						447
SCR 01 H				Y									3-4/8		447
SCR 02 H		E03H1		1-01					M7837	1					448
SCR 02 H		E04U1		1-02					M7838						448
SCR 02 H				1									4-4/8		448
SCR 03 L		DP4K2		1-01					M7838	1					449
SCR 03 L		E03E1		1-02					M7837						449
SCR 03 L				1									4-0/8		449
SCR 04 H		D04J1		1-01					M7838	1					450
SCR 04 H		E03A1		1-02					M7837						450
SCR 04 H				1									4-2/8		450
SCR 05 H		D04K1		1-01					M7838	1					451
SCR 05 H		F03N2		1-02					M7837						451
SCR 05 H				1									8-0/8		451
SCR 07 H		D03V1		1-01					M7837	1					452
SCR 07 H		F02B1		1-02					M7836						452
SCR 07 H				1									5-6/8		452
SCR 08 H		A03V2		1-01					M7837	1					453
SCR 08 H		E04K1		1-02					M7838						453
SCR 08 H				1									11-6/8		454
SCR 11 H		B03P2		1-01					M7837	1					454
SCR 11 H		E04L1		1-02					M7838						454
SCR 11 H				1									10-0/8		454
SELECT 2 H		E01S2		1-01					DM11	1					455
SELECT 2 H		F09F2		1-02					DM11						455
SELECT 2 H				1									7-2/8		455
SELECT 2 H		E01T2		1-01					DM11	2					456
SELECT 2 H		D01T2		1-02					DM11	1					456
SELECT 2 H		D09T2		1-03					DM11	2					456
SELECT 2 H		F09L2		1-04					DM11						456
SELECT 2 H				1									17-6/8		456
SERIAL OUT 00 L		AM5J2							M7839					1-PIN RUN	457
SERIAL OUT 01 L		AM5B1							M7839					1-PIN RUN	458

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
SERIAL OUT 02 L		AM5T2							M7839					1-PIN RUN	459
SERIAL OUT 03 L		AM5H2							M7839					1-PIN RUN	460
SERIAL OUT 04 L		AM6J2							M7839					1-PIN RUN	461
SERIAL OUT 05 L		AM6B1							M7839					1-PIN RUN	462
SERIAL OUT 06 L		AM6T2							M7839					1-PIN RUN	463
SERIAL OUT 07 L		AM6H2							M7839					1-PIN RUN	464
SERIAL OUT 10 L		AM7J2							M7839					1-PIN RUN	465
SERIAL OUT 09 L		A07B1							M7839					1-PIN RUN	466
SERIAL OUT 10 L		AM7T2							M7839					1-PIN RUN	467
SERIAL OUT 11 L		AM7H2							M7839					1-PIN RUN	468
SERIAL OUT 12 L		A08J2							M7839					1-PIN RUN	469
SERIAL OUT 13 L		A08H1							M7839					1-PIN RUN	470
SERIAL OUT 14 L		A08T2							M7839					1-PIN RUN	471
SERIAL OUT 15 L		A08H2							M7839					1-PIN RUN	472
SET TMARK L		C04D2		1-01					M7838	1					473
SET TMARK L		C05U2		1-02					M7839	2					473
SET TMARK L		C06U2		1-03					M7839	1					473
SET TMARK L		C07U2		1-04					M7839	2					473
SET TMARK L		C08U2		1-05					M7839						473
SET TMARK L				1									12-4/8		473
SET/CLEAR 03 L		C04D1		1-01					M7838	1					474
SET/CLEAR 03 L		D03H2		1-02					M7837						474
SET/CLEAR 03 L				1									5-6/8		474
SET/CLEAR 04 L		C04N1		1-01					M7838	1					475
SET/CLEAR 04 L		F02U2		1-02					M7836						475
SET/CLEAR 04 L				1									11-2/8		475
SOURCE CLK A 00-07 L		BP5J1							M7839					1-PIN RUN	476
SOURCE CLK A 04-07 L		BM6J1							M7839					1-PIN RUN	477

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
SOURCE CLK A 08-11 L		AA7J1							M7839					1-PIN RUN	478
SOURCE CLK A 12-15 L		AARJ1							M7839					1-PIN RUN	479
SOURCE CLK B 00-03 L		BC5N2							M7839					1-PIN RUN	480
SOURCE CLK B 04-07 L		BB6N2							M7839					1-PIN RUN	481
SOURCE CLK B 08-11 L		BA7N2							M7839					1-PIN RUN	482
SOURCE CLK B 12-15 L		BA8N2							M7839					1-PIN RUN	483
SRS 00 H		BAAM2		1-01					M7839	1					484
SRS 00 H		BA7M2		1-02					M7839	2					484
SRS 00 H		BA6M2		1-03					M7839	1					484
SRS 00 H		BA5M2		1-04					M7839	2					484
SRS 00 H		C04B2		1-05					M7838	1					484
SRS 00 H		F03E1		1-06					M7837						484
SRS 00 H				1									23-2/8		484
SRS 01 H		AA8T2		1-01					M7839	1					485
SRS 01 H		AA7T2		1-02					M7839	2					485
SRS 01 H		BA6T2		1-03					M7839	1					485
SRS 01 H		BA5T2		1-04					M7839	2					485
SRS 01 H		BA4M1		1-05					M7838	1					485
SRS 01 H		F03T2		1-06					M7837						485
SRS 01 H				1									25-2/9		485
SRS 02 H		BAAR2		1-01					M7839	1					486
SRS 02 H		BA6R2		1-02					M7839	2					486
SRS 02 H		B04T2		1-03					M7838	1					486
SRS 02 H		E03R1		1-04					M7837						486
SRS 02 H				1									17-0/8		486
SRS 03 H		BA8S2		1-01					M7839	1					487
SRS 03 H		BA7S2		1-02					M7839	2					487
SRS 03 H		BA4S2		1-03					M7838	1					487
SRS 03 H		E03S2		1-04					M7837						487
SRS 03 H				1									7-0/8		487
SRS 03 H		BA8S2		1-01					M7839	1					488
SRS 03 H		BA7S2		1-02					M7839	2					488
SRS 03 H		BA4S2		1-03					M7838	1					488
SRS 03 H		E03S2		1-04					M7837						488
SRS 03 H				1									16-6/8		488

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
SRS 03 L		BA4V2		1-01					M7838	1					489
SRS 03 L		BA5S2		1-02					M7839	2					489
SRS 03 L		BA6S2		1-03					M7839						489
SRS 03 L				1									5-6/8		489
SRS 04 H		D04E2		1-01					M7838	1					490
SRS 04 H		E03A2		1-02					M7837						490
SRS 04 H				1									6-0/8		490
SRS 09 H		D04M1		1-01					M7838	1					491
SRS 09 H		E03M1		1-02					M7837						491
SRS 09 H				1									9-0/8		491
SRS 10 H		D04V1		1-01					M7838	1					492
SRS 10 H		E03R1		1-02					M7837						492
SRS 10 H				1									7-2/8		492
SRS 11 H		D04F1		1-01					M7838	1					493
SRS 11 H		E03U2		1-02					M7837						493
SRS 11 H				1									6-4/8		493
SYSTEM MODE 00-03 H		AA5S2							M7839					1-PIN RUN	494
SYSTEM MODE 04-07 H		AA6S2							M7839					1-PIN RUN	495
SYSTEM MODE 08-11 H		A07S2							M7839					1-PIN RUN	496
SYSTEM MODE 12-15 H		AA8S2							M7839					1-PIN RUN	497
TCO 00 H		F05H2							M7839					1-PIN RUN	498
TCO 01 H		E05P2							M7839					1-PIN RUN	499
TCO 02 H		E05J2							M7839					1-PIN RUN	500
TCO 03 H		E05D2							M7839					1-PIN RUN	501
TCO 04 H		F06H2							M7839					1-PIN RUN	502
TCO 05 H		E06P2							M7839					1-PIN RUN	503
TCO 06 H		E06J2							M7839					1-PIN RUN	504
TCO 07 H		E06D2							M7839					1-PIN RUN	505
TCO 08 H		F07H2							M7839					1-PIN RUN	506

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RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW RV PG Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
TCO 09 H		F07P2				M7839					1-PIN RUN	507
TCO 10 H		F07J2				M7839					1-PIN RUN	508
TCO 11 H		E07D2				M7839					1-PIN RUN	509
TCO 12 H		F08H2				M7839					1-PIN RUN	510
TCO 13 H		E06P2				M7839					1-PIN RUN	511
TCO 14 H		F08J2				M7839					1-PIN RUN	512
TCO 15 H		E08D2				M7839					1-PIN RUN	513
TMARK 00 L		C05D2				M7839					1-PIN RUN	514
TMARK 01 L		C05B2				M7839					1-PIN RUN	515
TMARK 02 L		F05L2				M7839					1-PIN RUN	516
TMARK 03 L		F05E2				M7839					1-PIN RUN	517
TMARK 04 L		C06D2				M7839					1-PIN RUN	518
TMARK 05 L		C06B2				M7839					1-PIN RUN	519
TMARK 06 L		E06L2				M7839					1-PIN RUN	520
TMARK 07 L		E06E2				M7839					1-PIN RUN	521
TMARK 08 L		C07D2				M7839					1-PIN RUN	522
TMARK 09 L		C07B2				M7839					1-PIN RUN	523
TMARK 10 L		E07L2				M7839					1-PIN RUN	524
TMARK 11 L		E07E2				M7839					1-PIN RUN	525
TMARK 12 L		C08D2				M7839					1-PIN RUN	526
TMARK 13 L		C08B2				M7839					1-PIN RUN	527
TMARK 14 L		E08L2				M7839					1-PIN RUN	528
TMARK 15 L		F08E2				M7839					1-PIN RUN	529

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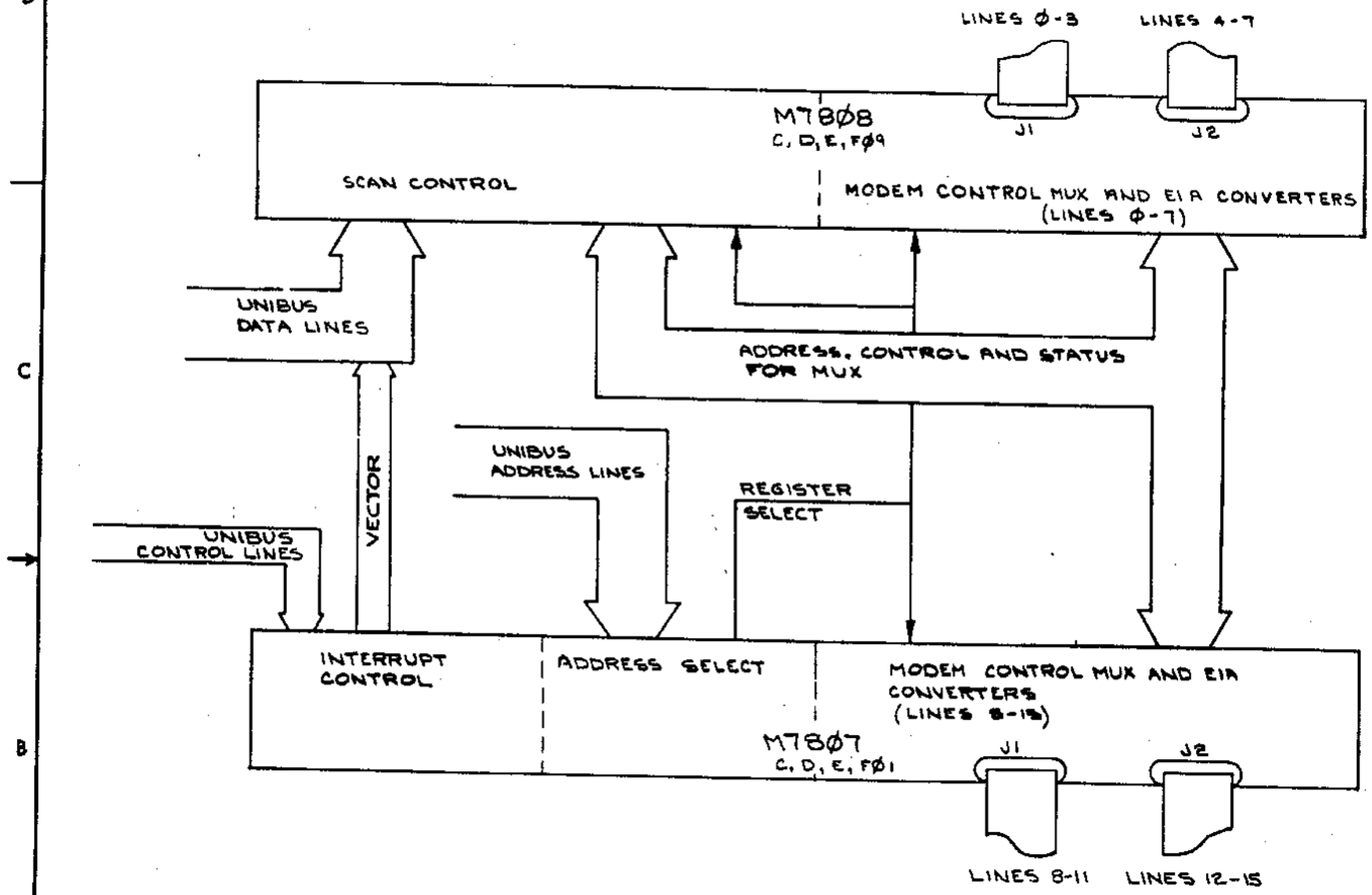
RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW RV PG Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
TP CL2		C01L2				DM11					1-PIN RUN	530
TP EXT CAP		E01B1				DM11					1-PIN RUN	531
TP FL1		F09L1				DM11					1-PIN RUN	532
TRAN DATA 00 H		C04H1		1-01		M7838		1				533
TRAN DATA 00 H		F05U2		1-02		M7839		2				533
TRAN DATA 00 H		F06U2		1-03		M7839		1				533
TRAN DATA 00 H		F07J2		1-04		M7839		2				533
TRAN DATA 00 H		F08U2		1-05		M7839						533
TRAN DATA 00 H				1						20-2/8		533
TRAN DATA 01 H		C04J1		1-01		M7838		1				534
TRAN DATA 01 H		F05T2		1-02		M7839		2				534
TRAN DATA 01 H		F06T2		1-03		M7839		1				534
TRAN DATA 01 H		F07T2		1-04		M7839		2				534
TRAN DATA 01 H		F08T2		1-05		M7839						534
TRAN DATA 01 H				1						20-0/8		534
TRAN DATA 02 H		C04L2		1-01		M7838		1				535
TRAN DATA 02 H		F05V1		1-02		M7839		2				535
TRAN DATA 02 H		F06V1		1-03		M7839		1				535
TRAN DATA 02 H		F07V1		1-04		M7839		2				535
TRAN DATA 02 H		F08V1		1-05		M7839						535
TRAN DATA 02 H				1						19-6/8		535
TRAN DATA 03 H		C04N2		1-01		M7838		1				536
TRAN DATA 03 H		F05S2		1-02		M7839		2				536
TRAN DATA 03 H		F06S2		1-03		M7839		1				536
TRAN DATA 03 H		F07S2		1-04		M7839		2				536
TRAN DATA 03 H		F08S2		1-05		M7839						536
TRAN DATA 03 H				1						19-2/8		536
TRAN DATA 04 H		A04T2		1-01		M7838		1				537
TRAN DATA 04 H		F05V2		1-02		M7839		2				537
TRAN DATA 04 H		F06V2		1-03		M7839		1				537
TRAN DATA 04 H		F07V2		1-04		M7839		2				537
TRAN DATA 04 H		F08V2		1-05		M7839						537
TRAN DATA 04 H				1						24-2/8		537
TRAN DATA 05 H		A04S1		1-01		M7838		1				538
TRAN DATA 05 H		F05R2		1-02		M7839		2				538
TRAN DATA 05 H		F06P2		1-03		M7839		1				538
TRAN DATA 05 H		F07P2		1-04		M7839		2				538
TRAN DATA 05 H		F08R2		1-05		M7839						538
TRAN DATA 05 H				1						24-0/8		538

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
TRAN DATA 06 H		AP4V2		1-01				M7838	1					539
TRAN DATA 06 H		EW5W2		1-02				M7839	2					539
TRAN DATA 06 H		EW6W2		1-03				M7839	1					539
TRAN DATA 06 H		FW7W2		1-04				M7839	2					539
TRAN DATA 06 H		EW8W2		1-05				M7839						539
TRAN DATA 06 H				1								20-4/8		539
TRAN DATA 07 H		AW4S2		1-01				M7838	1					540
TRAN DATA 07 H		EW5P1		1-02				M7839	2					540
TRAN DATA 07 H		EW6P1		1-03				M7839	1					540
TRAN DATA 07 H		EW7P1		1-04				M7839	2					540
TRAN DATA 07 H		EW8P1		1-05				M7839						540
TRAN DATA 07 H				1								21-0/8		540
TRAN DATA 08 H		DW4F2		1-01				M7838	1					541
TRAN DATA 08 H		EW5R1		1-02				M7839	2					541
TRAN DATA 08 H		EW6R1		1-03				M7839	1					541
TRAN DATA 08 H		FW7R1		1-04				M7839	2					541
TRAN DATA 08 H		EW8R1		1-05				M7839						541
TRAN DATA 08 H				1								14-2/8		541
TRAN FLAG WAITING L		CW4P2		1-01				M7838	1					542
TRAN FLAG WAITING L		FW5L2		1-02				M7839	2					542
TRAN FLAG WAITING L		FW6L2		1-03				M7839	1					542
TRAN FLAG WAITING L		FW7L2		1-04				M7839	2					542
TRAN FLAG WAITING L		FW8L2		1-05				M7839						542
TRAN FLAG WAITING L				1								18-4/8		542
TRANS DISABLE 00-03 H		AW5F2						M7839					1-PIN RUN	543
TRANS DISABLE 04-07 H		AW6F2						M7839					1-PIN RUN	544
TRANS DISABLE 08-11 H		AW7F2						M7839					1-PIN RUN	545
TRANS DISABLE 12-15 H		AW8F2						M7839					1-PIN RUN	546
TRANSFER BUS 00 H		CW4J2		1-01				M7838	2					547
TRANSFER BUS 00 H		CW3M2		1-02				M7837	1					547
TRANSFER BUS 00 H		DW2T2		1-03				M7836						547
TRANSFER BUS 00 H				1								9-4/8		547
TRANSFER BUS 01 H		CW4K2		1-01				M7838	2					548
TRANSFER BUS 01 H		CW3K2		1-02				M7837	1					548
TRANSFER BUS 01 H		DW2P2		1-03				M7836						548
TRANSFER BUS 01 H				1								8-4/8		548

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
TRANSFER BUS 02 H		CW4M2		1-01				M7838	2					549
TRANSFER BUS 02 H		CW3K1		1-02				M7837	1					549
TRANSFER BUS 02 H		DW2Y2		1-03				M7836						549
TRANSFER BUS 02 H				1								8-6/8		549
TRANSFER BUS 03 H		CW4N1		1-01				M7838	1					550
TRANSFER BUS 03 H		CW3L1		1-02				M7837	2					550
TRANSFER BUS 03 H		DW2R2		1-03				M7836						550
TRANSFER BUS 03 H				1								8-4/8		550
TRANSFER BUS 04 H		AW4W2		1-01				M7838	1					551
TRANSFER BUS 04 H		CW2E2		1-02				M7836	2					551
TRANSFER BUS 04 H		CW3R2		1-03				M7837						551
TRANSFER BUS 04 H				1								11-0/8		551
TRANSFER BUS 05 H		AW4P1		1-01				M7838	1					552
TRANSFER BUS 05 H		CW3N1		1-02				M7837	2					552
TRANSFER BUS 05 H		FW2J2		1-03				M7836						552
TRANSFER BUS 05 H				1								14-6/8		552
TRANSFER BUS 06 H		AW4U2		1-01				M7838	2					553
TRANSFER BUS 06 H		BW2U2		1-02				M7836	1					553
TRANSFER BUS 06 H		CW3P1		1-03				M7837						553
TRANSFER BUS 06 H				1								9-6/8		553
TRANSFER BUS 07 H		AW4U1		1-01				M7838	2					554
TRANSFER BUS 07 H		CW3S2		1-02				M7837	1					554
TRANSFER BUS 07 H		EW2P1		1-03				M7836						554
TRANSFER BUS 07 H				1								15-2/8		554
TRANSFER BUS 08 H		EW3C1		1-01				M7837	2					555
TRANSFER BUS 08 H		EW2R1		1-02				M7836	1					555
TRANSFER BUS 08 H		FW4P2		1-03				M7838						555
TRANSFER BUS 08 H				1								9-6/8		555
TRANSFER BUS 09 H		EW3B2		1-01				M7837	2					556
TRANSFER BUS 09 H		EW2S1		1-02				M7836	1					556
TRANSFER BUS 09 H		FW4M2		1-03				M7838						556
TRANSFER BUS 09 H				1								9-4/8		556
TRANSFER BUS 10 H		EW3D2		1-01				M7837	2					557
TRANSFER BUS 10 H		EW2V2		1-02				M7836	1					557
TRANSFER BUS 10 H		FW4N2		1-03				M7838						557
TRANSFER BUS 10 H				1								9-0/8		557

RUN NAME	A/P	PIN NAME	ORDER PIN	BAY - ORDER	Q	DRAW	RV	PG	Y	X	Z	REMARKS	LENGTH	EXCEPTIONS	RUN NUMBER
TRANSFER BUS 11 H		B02E2		1-01					M7836		1				558
TRANSFER BUS 11 H		E03E2		1-02					M7837		2				558
TRANSFER BUS 11 H		F04V1		1-03					M7838						558
TRANSFER BUS 11 H				1									17-2/8		558
TRANSFER BUS 12 H		A02P2		1-01					M7836		1				559
TRANSFER BUS 12 H		D03K1		1-02					M7837		2				559
TRANSFER BUS 12 H		E04M1		1-03					M7838						559
TRANSFER BUS 12 H				1									15-2/8		559
TRANSFER BUS 13 H		A02S2		1-01					M7836		1				560
TRANSFER BUS 13 H		D03L2		1-02					M7837		2				560
TRANSFER BUS 13 H		E04L2		1-03					M7838						560
TRANSFER BUS 13 H				1									15-0/8		560
TRANSFER BUS 14 H		B02F1		1-01					M7836		1				561
TRANSFER BUS 14 H		D03F2		1-02					M7837		2				561
TRANSFER BUS 14 H		E04M2		1-03					M7838						561
TRANSFER BUS 14 H				1									13-6/8		561
TRANSFER BUS 15 H		A02V2		1-01					M7836		1				562
TRANSFER BUS 15 H		D03J1		1-02					M7837		2				562
TRANSFER BUS 15 H		F04P1		1-03					M7838						562
TRANSFER BUS 15 H				1									15-0/8		562
TRANSFER BUS 16 H		A02L1		1-01					M7836		1				563
TRANSFER BUS 16 H		D04J2		1-02					M7838						563
TRANSFER BUS 16 H				1									10-6/8		563
TRANSFER BUS 17 H		B02A1		1-01					M7836		1				564
TRANSFER BUS 17 H		C04K2		1-02					M7838						564
TRANSFER BUS 17 H				1									9-2/8		564
TRANSFER SOURCE ENAB L		D02K2		1-01					M7836		1				565
TRANSFER SOURCE ENAB L		F04B2		1-02					M7838						565
TRANSFER SOURCE ENAB L				1									7-2/8		565
TRANSMITTER STROBE H		A04M2		1-01					M7838		1				566
TRANSMITTER STROBE H		E05H2		1-02					M7839		2				566
TRANSMITTER STROBE H		E06H2		1-03					M7839		1				566
TRANSMITTER STROBE H		E07H2		1-04					M7839		2				566
TRANSMITTER STROBE H		E08H2		1-05					M7839						566
TRANSMITTER STROBE H				1									20-6/8		566
UNIBUS PA: WRITE L		A04F2		1-01					M7838		1				567
UNIBUS PA: WRITE L		B03U2		1-02					M7837						567
UNIBUS PA: WRITE L				1									6-6/8		567

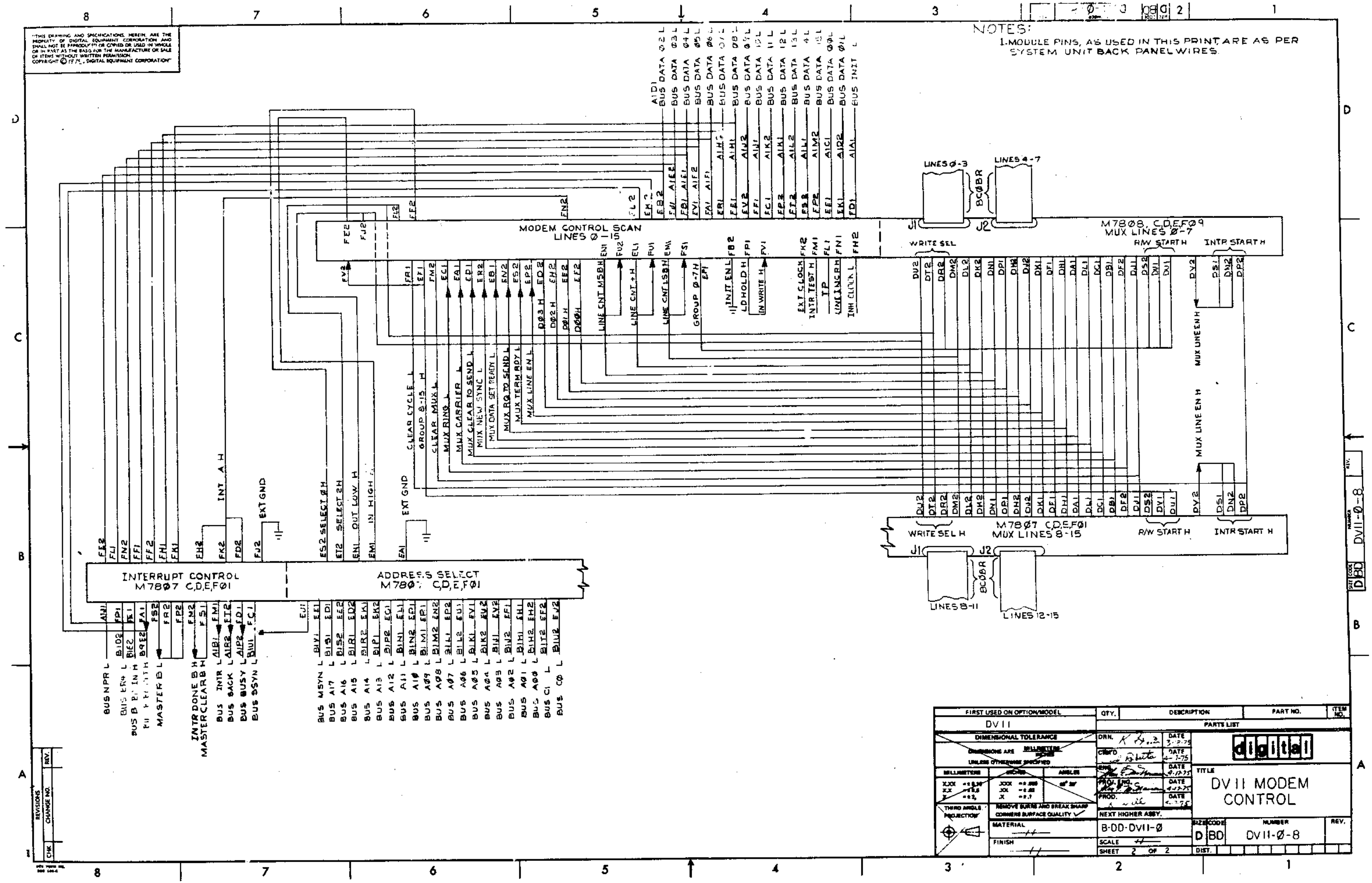


FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DVII		PARTS LIST		

DIMENSIONAL TOLERANCE	DRN K. Swab	DATE 3-18-75	digital
DIMENSIONS ARE MILLIMETERS / INCHES UNLESS OTHERWISE SPECIFIED	CHK'D Ed Roberts	DATE 4-17-75	TITLE: DVII MODEM CONTROL
MILLIMETERS: X.XX ±0.13, X.X ±0.5, X ±2.5 — INCHES: .XXX ±.005, .XX ±.02, .X ±.1 — ANGLES ±30'	ENGR	DATE 4-17-75	
THIRD ANGLE PROJECTION	PROJ. ENGR	DATE 4-17-75	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	MFG	DATE 5-7-75	
MATERIAL	NEXT HIGHER ASSY. B-DD-DVII-Ø		SIZE D · CODE 8D · NUMBER DVII-Ø-8 · REV.
FINISH	SCALE 1/1		
	SHEET 1 OF 2		DIST.

REVISIONS	REV.	CHANGE NO.	CHK

DVII-Ø-8



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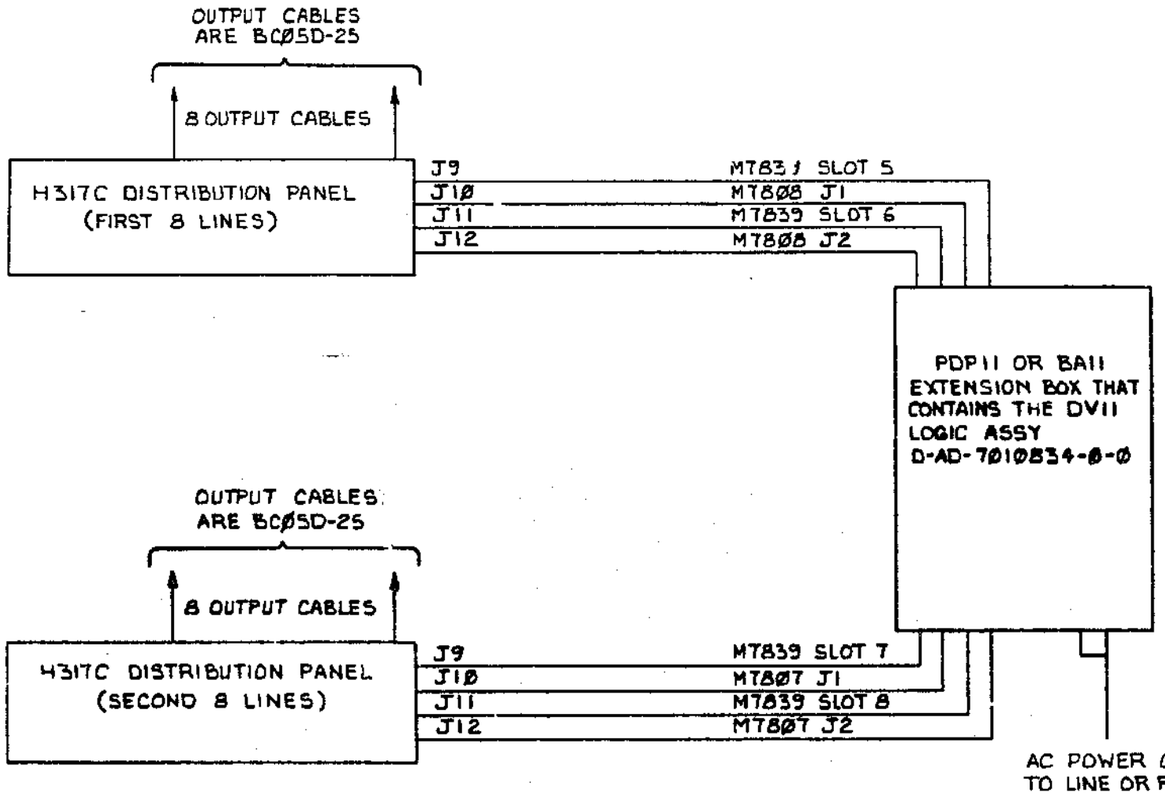
NOTES:
1. MODULE PINS, AS USED IN THIS PRINT, ARE AS PER SYSTEM UNIT BACK PANEL WIRES.
MODEM CONTROL SCAN LINES Ø-15
M7808 C,D,E,FØ9 MUX LINES Ø-7
M7807 C,D,E,FØ1 MUX LINES 8-15
INTERRUPT CONTROL M7807 C,D,E,FØ1
ADDRESS SELECT M7807 C,D,E,FØ1
LINES Ø-3
LINES 4-7
LINES 8-11
LINES 12-15
BCØ8R
WRITE SEL
WRITE SEL H
R/W START H
INTR START H
MUX LINE EN H
EXT GND
INT A H
CLEAR CYCLE L
GROUP 8-15 H
CLEAR MUX L
MUX RING L
MUX CARRIER L
MUX CLEAR TO SEND L
MUX NEW SYNC L
MUX DATA SET READY L
MUX RQ TO SEND L
MUX TERM RDY L
MUX LINE EN L
LINE CNT MSB H
LINE CNT + H
LINE CNT LSB H
GROUP Ø-7 H
INIT EN L
LD HOLD H
IN WRITE H
EXT CLOCK
INTR TEST H
TP
LINE INCR H
INH CLOCK L
ES2 SELECT ØH
SELECT 2H
OUT LOW H
IN HIGH
BUS DATA Ø2 L
BUS DATA Ø3 L
BUS DATA Ø4 L
BUS DATA Ø5 L
BUS DATA Ø6 L
BUS DATA Ø7 L
BUS DATA Ø8 L
BUS DATA Ø9 L
BUS DATA 1Ø L
BUS DATA 11 L
BUS DATA 12 L
BUS DATA 13 L
BUS DATA 14 L
BUS DATA 15 L
BUS DATA ØØ L
BUS DATA Ø1 L
BUS INIT L
BUS NPR L
MASTER B L
INTR DONE B H
MASTER CLEAR B H
BUS INTR L
BUS BACK L
BUS BUSY L
BUS SSYN L
BUS MSYN L
BUS A17 L
BUS A16 L
BUS A15 L
BUS A14 L
BUS A13 L
BUS A12 L
BUS A11 L
BUS A1Ø L
BUS AØ9 L
BUS AØ8 L
BUS AØ7 L
BUS AØ6 L
BUS AØ5 L
BUS AØ4 L
BUS AØ3 L
BUS AØ2 L
BUS AØ1 L
BUS AØØ L
BUS C1 L
BUS CØ L
FIRST USED ON OPTION/MODEL: DV11
NEXT HIGHER ASSY.: B-DD-DV11-Ø
TITLE: DV11 MODEM CONTROL
digital
SIZE: D
CODE: BD
NUMBER: DV11-Ø-8
SHEET 2 OF 2

NOTES:

1. ON M7807 & M7808 MODULES J1 IS THE JACK NEAREST THE EDGE OF THE BOARD.
2. ON H317C DISTRIBUTION PANEL (D-CS-5411153) J9 IS FAR LEFT JACK; J12 IS FAR RIGHT JACK.
3. INSERT CABLES FLAT SIDE TOWARD YOU; RIBBED SIDE AGAINST CIRCUIT BOARD.



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DV11		PARTS LIST		

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS: .xxx = .006; .xx = .02; .x = .1
ANGLES: ±0° 30'
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY √

MATERIAL —

FINISH —

DRN. Robert Kopparud	DATE 3-28-75	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D. Earl Roberts	DATE 4-17-75	
ENG. John E. Manson	DATE 4-17-75	
PROJ. ENG. John P. M. Manson	DATE 4-17-75	
PROD. R Wall	DATE 4-17-75	

TITLE: INTERCONNECTION DV11

NEXT HIGHER ASSY.: B-DD-DV11-Ø

SCALE —

SHEET | OF

SIZE	CODE	NUMBER	REV.
C	IC	DV11-Ø-9	

DIST.

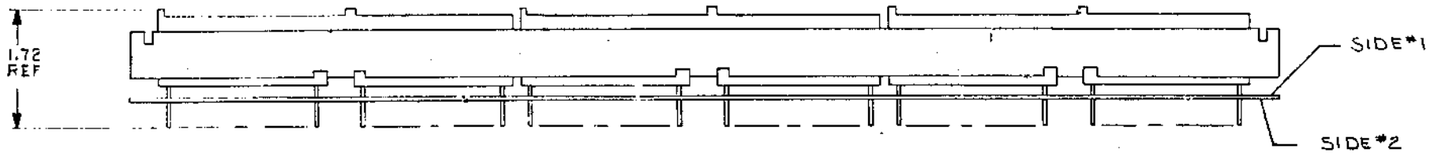
REVISIONS: REV. | CHANGE NO. | CHK

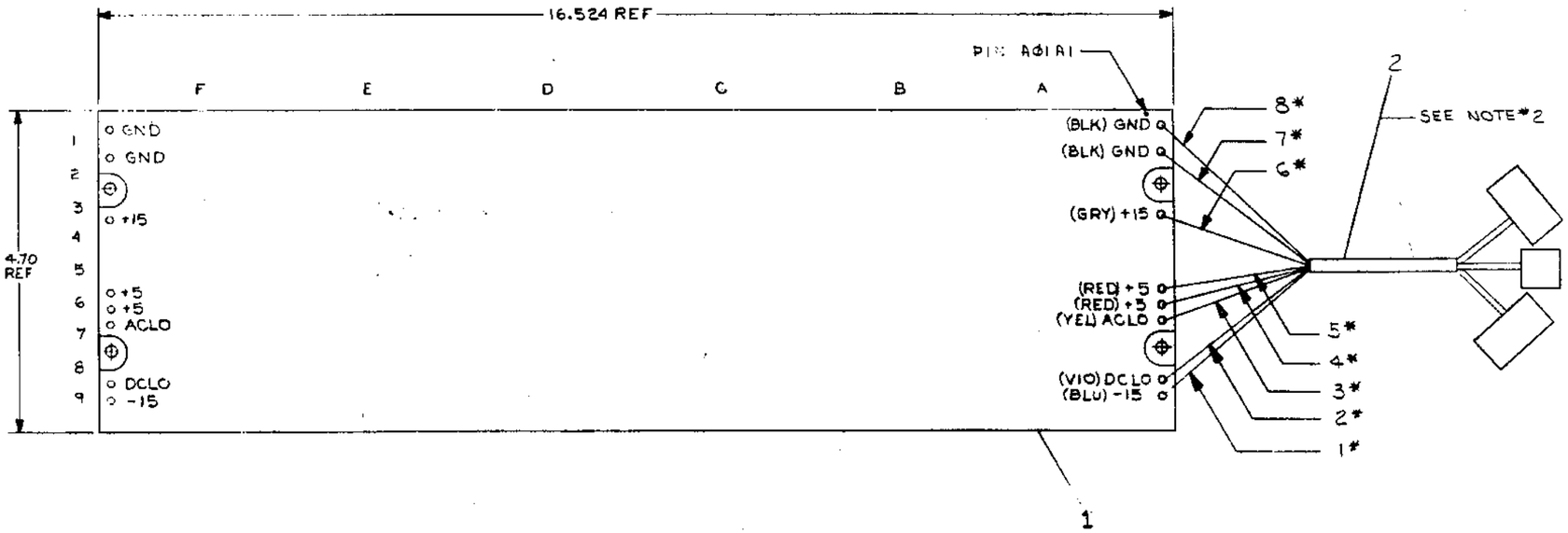
DEC FORM NO. DRC 100-B

4 3 2 1

DO NOT SCALE DRAWING

NOTES:
1. * INDICATES POINT NO. ON ITEM#2 (POWER HARNESS).
2. ITEM#2 (POWER HARNESS) TO BE CONNECTED TO ITEM#1 (LOGIC ASSY) AS SHOWN USING SOLDER.





ITEM NO.	DESCRIPTION	DWG./PART NO.	QTY
-EF	AWT REVSTATUS	A-WT-7010834-0	3
2	POWER HARNESS (DVII)	D-IA-7010835-0-0	2
1	WIRED ASS'Y	D-IA-7010655-0-0	1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ±0° 30'
CLASS OF ACCURACY (CHECK ONE)
SURFACE QUALITY IN MICRONICHES
MEDIUM
PREFERRED

NOMINAL DIMENSION RANGE INCHES	OVER 0 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 40.0	OVER 40.0 TO 80.0
MEDIUM	±.004	±.008	±.012	±.016	±.024	±.04
PREFERRED	±.002	±.010	±.020	±.04	±.060	±0.1

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL ##

FINISH ##

DRN. 1/17/75
CHK'D 4.9.75
ENG. 4/4/75
PROJ. MGR. 4/4/75
PROD. 4/21/75

NEXT HIGHER ASSY. D-UA-DVII-0-0

SCALE 1/1

SHEET 1 OF 1

FIRST USED ON PDP11

digital

TITLE
LOGIC ASS'Y
(DVII)

SIZE D | CODE AD | NUMBER 7010834-0-0 | REV.

DIST.

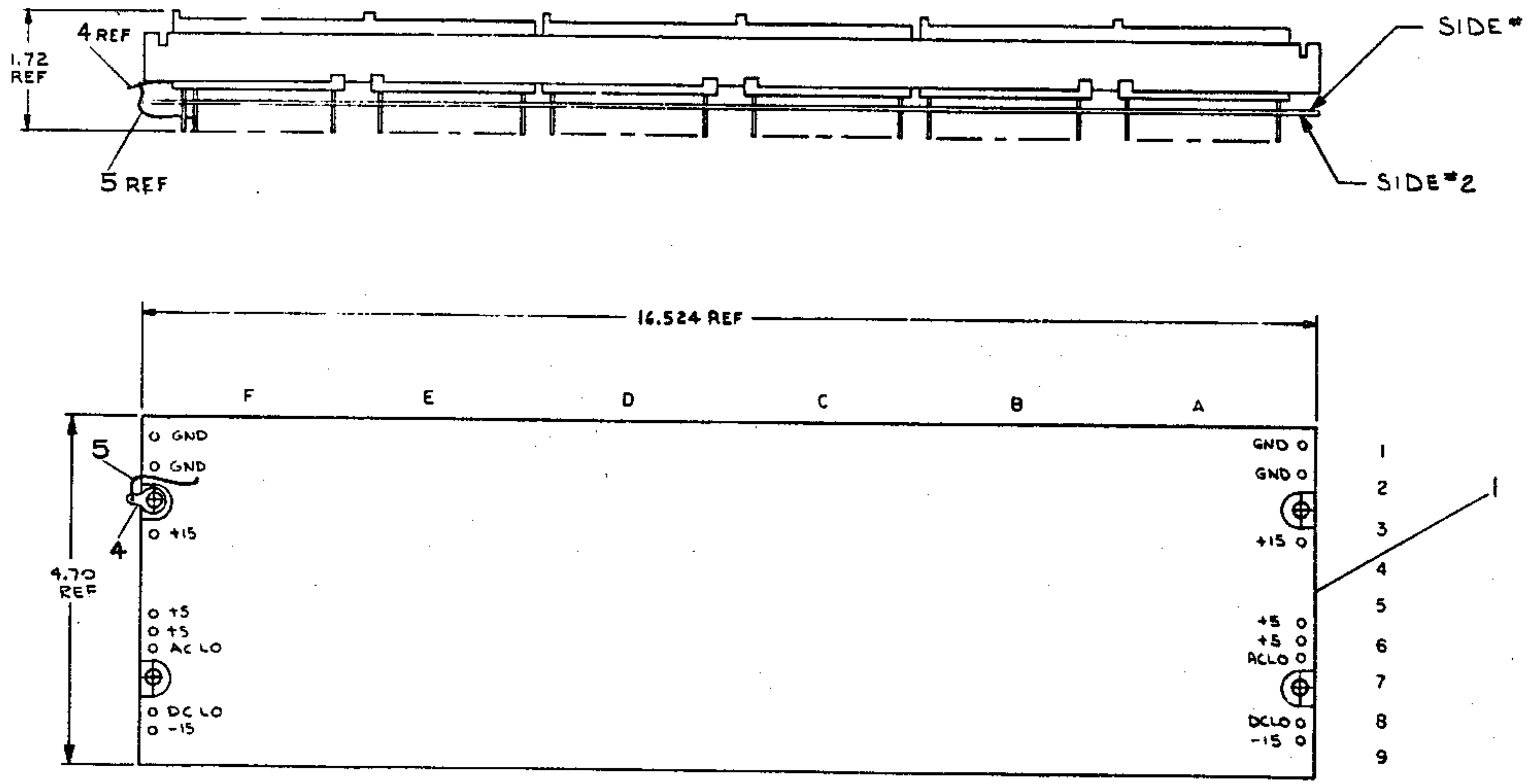
REVISIONS
REV. | CHANGE NO. | CHK.

DEC FORM NO. DRD 100-C

DO NOT SCALE DRAWING

NOTES:

1. WIREWRAP ONE END OF ITEM #5 TO PIN F02T1 AND SOLDER THE OTHER END TO ITEM #4 WHICH IS MOUNTED UNDER THE SYSTEM UNIT MOUNTING SCREW.



QTY.	DESCRIPTION		PART NO.	ITEM NO.
A/R	WIRE #24 AWG SOLID	BLK	9107688-00	5
1	TERMINAL LOCKING, SHAKEPROOF		9006766	4
REF	WIRE LIST		K-WL-DV11-0-7	3
A/R	WIRE #30 AWG SOLID YEL		9105740-44	2
1	BACK PLANE ASSY		D-AD-7010719-0-0	1

PARTS LIST

FIRST USED ON OPTION-MODEL: PDP 11

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES

TOLERANCES

DECIMALS	ANGLES
.xxx ± .005 .xx ± .02 .x ± .1	± 0° 30'

REMOVE BURRS AND BREAK SHARP CORNERS. SURFACE QUALITY ✓

MATERIAL: —/—/—

FINISH: —/—/—

DRN. DATE
CHKD. DATE 4-9-75
ENG. DATE
PROJ. ENG. DATE
PROD. DATE

NEXT HIGHER ASSY. D-AD7010834-0-0

SCALE —/—/—

SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

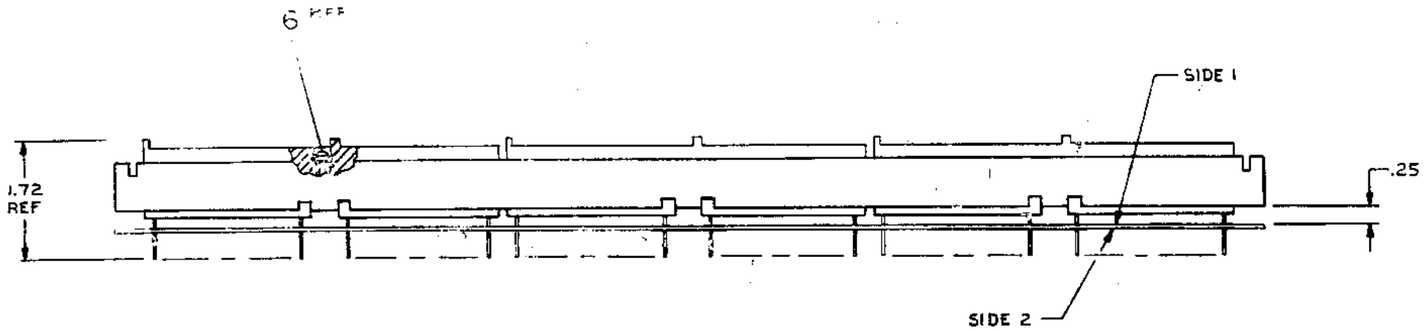
TITLE: WIRED ASSY (DV11)

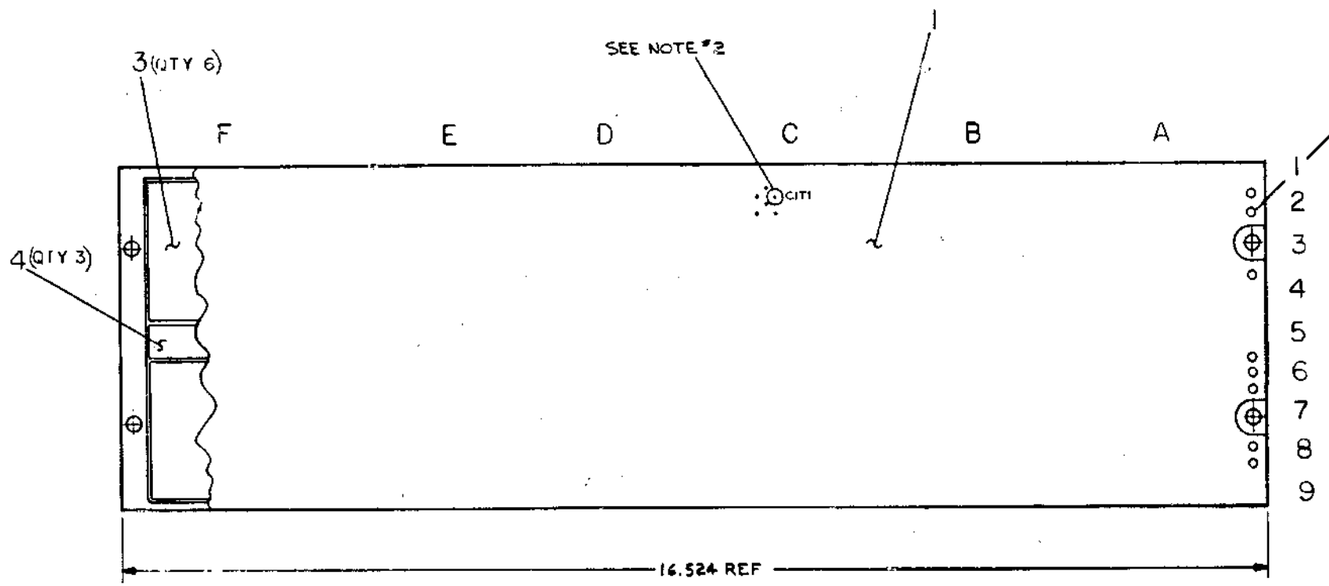
SIZE	CODE	NUMBER	REV.
D	AD	7010655-0-0	

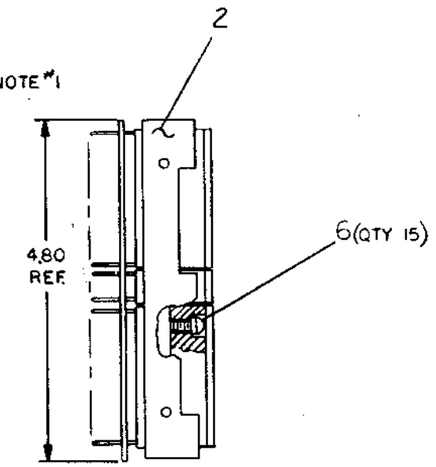
DIST.

DO NOT SCALE DRAWING

NOTES:
1. INSERT EYELET (ITEM*5) FROM SIDE *2 OF ETCH BOARD.
2. REWORK ITEM*1 (ETCH BOARD), IF REV C, BY USING CIRCUIT BOARD REWORK DRILL (HOLLOW DRILL .04 ID, .125 OD) AT PIN CITI ALL THE WAY THROUGH. THIS WORK TO BE DONE AFTER ITEM*1 HAS BEEN INSTALLED ON ITEMS *3 & *4. NO REWORK REQUIRED IF ITEM*1 IS REV D OR LATER







REF	CIRCUIT SCHEMATIC	D-CS-5411420-0-1	7
15	[illegible]	9006120-6	6
16	EYELET	9009605	5
3	72 PIN CONN. BLOCK	1211425-00	4
6	288 PIN BLOCK H863	1210258	3
1	LOGIC FRAME	12 11439	2
1	ETCHED CIRCUIT BOARD	5011413	1
QTY	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION MODEL: PDP 11

UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES
TOLERANCES
DECIMALS: .XXX ± .005, .XX ± .02, .X ± .1
ANGLES: ± 30
REMOVE BURRS AND BREAK SHARP CORNERS .005/.015 RADIUS

MATERIAL
FINISH

DRN. [illegible] DATE 11-14-74
CHKD [illegible] DATE 12-13
ENGR [illegible] DATE 12/4/75
PROJ. [illegible] DATE 12/4/75
PROD. K. Wall DATE 12/4/75

NEXT HIGHER ASSY. D-AD-7010655-0

SCALE 1/1
SHEET 1 OF 1

digital EQUIPMENT CORPORATION

TITLE: BACK PLANE ASSY

SIZE D | CODE IA | NUMBER 7010719-0-0 | REV

DIST.

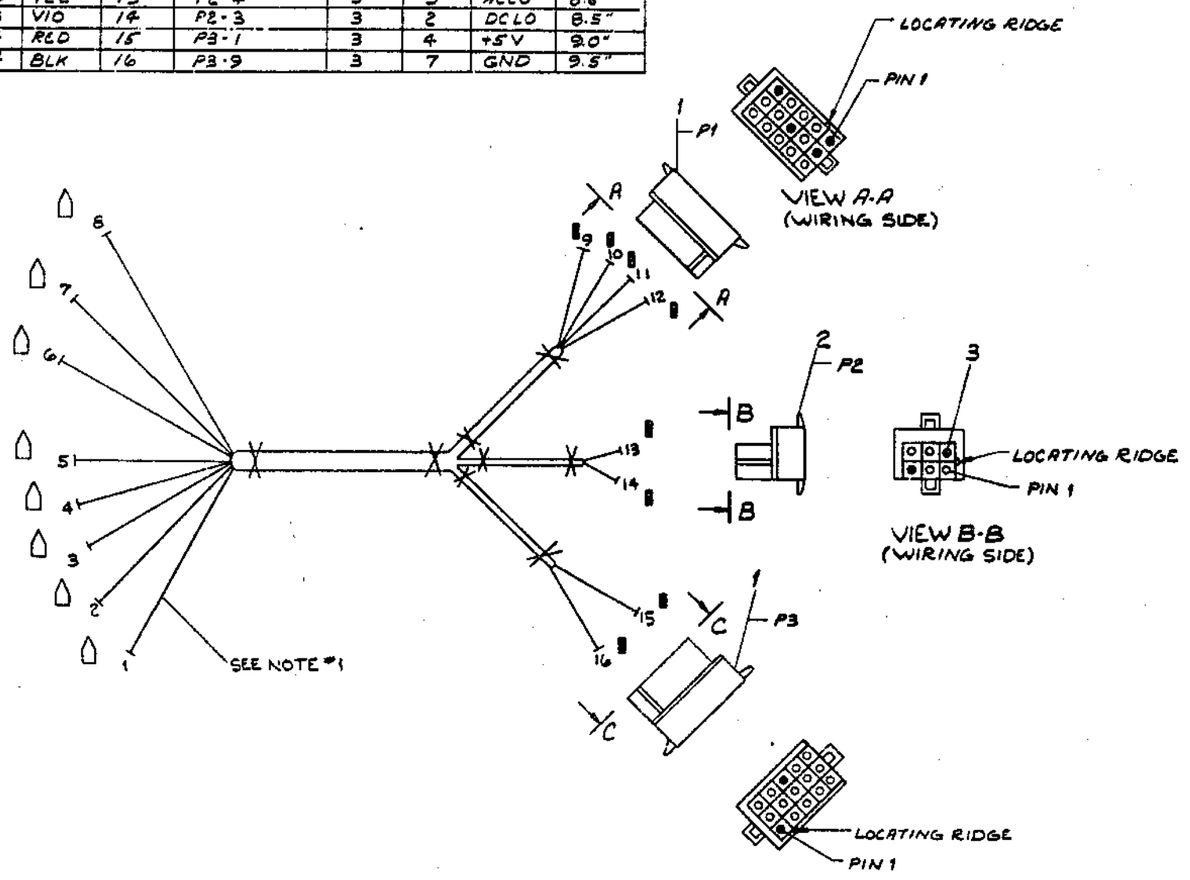
REVISIONS

REV	CHANGE NO	CHK

WIRE TABLE

ITEM NO	DESCRIPTION AWG	COLOR	FROM POINT	FROM CONNECTION	WITH	TO POINT	SIGNAL	WIRE LENGTHS
6	14	BLU	9	P1-13	3	1	-15V	10.0"
5	14	BLK	10	P1-8	3	8	GND	10.5"
4	14	RED	11	P1-1	3	5	+5V	9.0"
9	18	GRY	12	P1-2	3	6	+15V	9.5"
8	18	YEL	13	P2-4	3	3	ACLO	8.5"
7	18	VIO	14	P2-3	3	2	DCLO	8.5"
4	14	RED	15	P3-1	3	4	+5V	9.0"
5	14	BLK	16	P3-9	3	7	GND	9.5"

NOTES
1. INSULATION AT POINT 1 THRU 8 SHOULD BE STRIPPED BACK .18 INCHS AND WIRES SOLDER TINNED.



X	B	TIE WRAP	3007031	10
△	A/R	WIRE, #18 AWG (GRY)	9107360-88	9
△	A/R	WIRE, #18 AWG (YEL)	9107360-44	8
△	A/R	WIRE, #18 AWG (VIO)	9107360-77	7
△	A/R	WIRE, #14 AWG (BLU)	9107370-66	6
△	A/R	WIRE, #14 AWG (BLK)	9107370-00	5
△	A/R	WIRE, #14 AWG (RED)	9107370-22	4
■	8	PIN, MALE	1209378-01	3
	1	HOUSING, CONN. 6 PIN	1209351-06	2
	2	HOUSING, CONN 15 PIN	1209351-15	1

SYM	DESCRIPTION	DWG PART NO.	ITEM NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES ±0° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES: OVER 0 TO 0.3	OVER 0.3 TO 1.2	OVER 1.2 TO 4.0	OVER 4.0 TO 12.0	OVER 12.0 TO 48.0	OVER 48.0 TO 80.0
SURFACE QUALITY IN ✓ MICROINCHES	MEDIUM ☐	±.004	±.008	±.012	±.015	±.024	±.06
	PREFERRED ☐	±.012	±.016	±.020	±.03	±.062	±0.1

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL: SEE PARTS LIST

FINISH

DRN. J.C. Wiley 4-2078
CHK. [illegible] 5-31-75
ENG. [illegible] 4-3-75
PROJ. ENG. [illegible] 5-31-75
PROD. P. Li. [illegible] 7-31-75
NEXT HIGHER ASSY. D-AD-7010834-0-0
SCALE
SHEET 1 OF 1

FIRST USED ON: DV11

TITLE: POWER HARNESS (DV11)

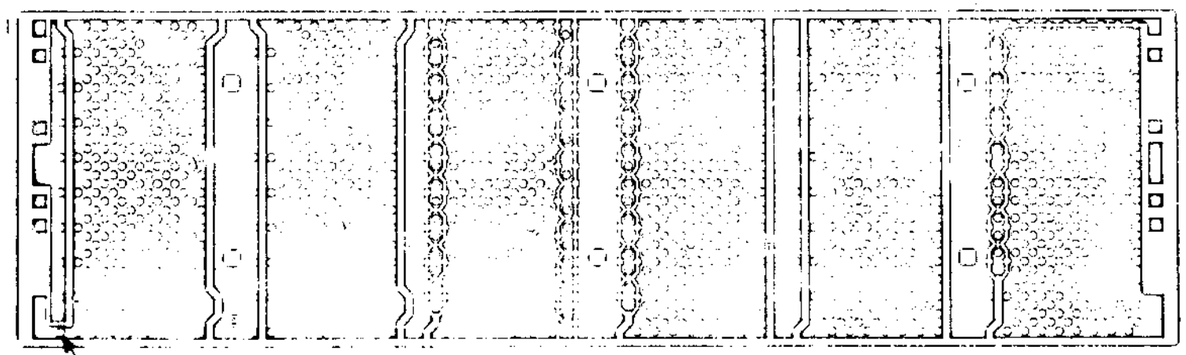
SIZE	CODE	NUMBER	REV.
D	IA	7010835-0-0	

DIST.

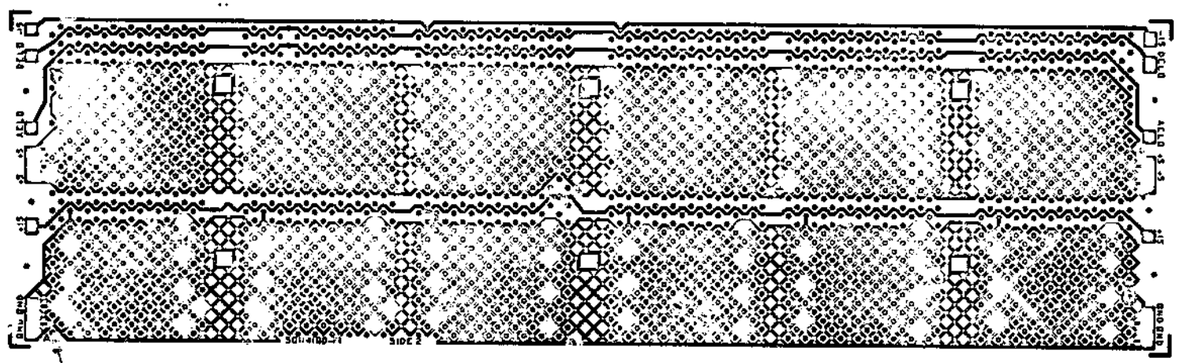
REVISIONS: REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 100-C

NOTES:



SIDE 1



SIDE 2

IC TYPE	GND	+ 5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF		MODULE ECO HISTORY	B-BIH-5411420-0-0	4
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-5411420-0-5	3
REF		X-Y COORDINATE HOLE LOCATION	K-CO-54.420-0-4	2
1		ETCHED CIRCUIT BOARD	5011419	1
QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO

PARTS LIST

FIRST USED ON OPTION MODEL: PDP11

ETCH BOARD REV: D-P1

REV	CHANGE NO	CHK	DATE
B	5411420-1	J.McNAMARA	1-28-75
C	5411420-0000	J.McNAMARA	2-6-75

DEC NO	EIA NO	DEC NO.	EIA NO

SEMICONDUCTOR CONVERSION CHART

DRN A.DAVIS 1-15-75
CHK'D 1-16-75
ENG 1-16-75
PROJ ENG 1-16-75
PGD C.Weld 1-16-75

NEXT HIGHER ASSY: D-IA-7010719-0-0

SCALE: NONE

SHEET 1 OF 1

digital EQUIPMENT CORPORATION

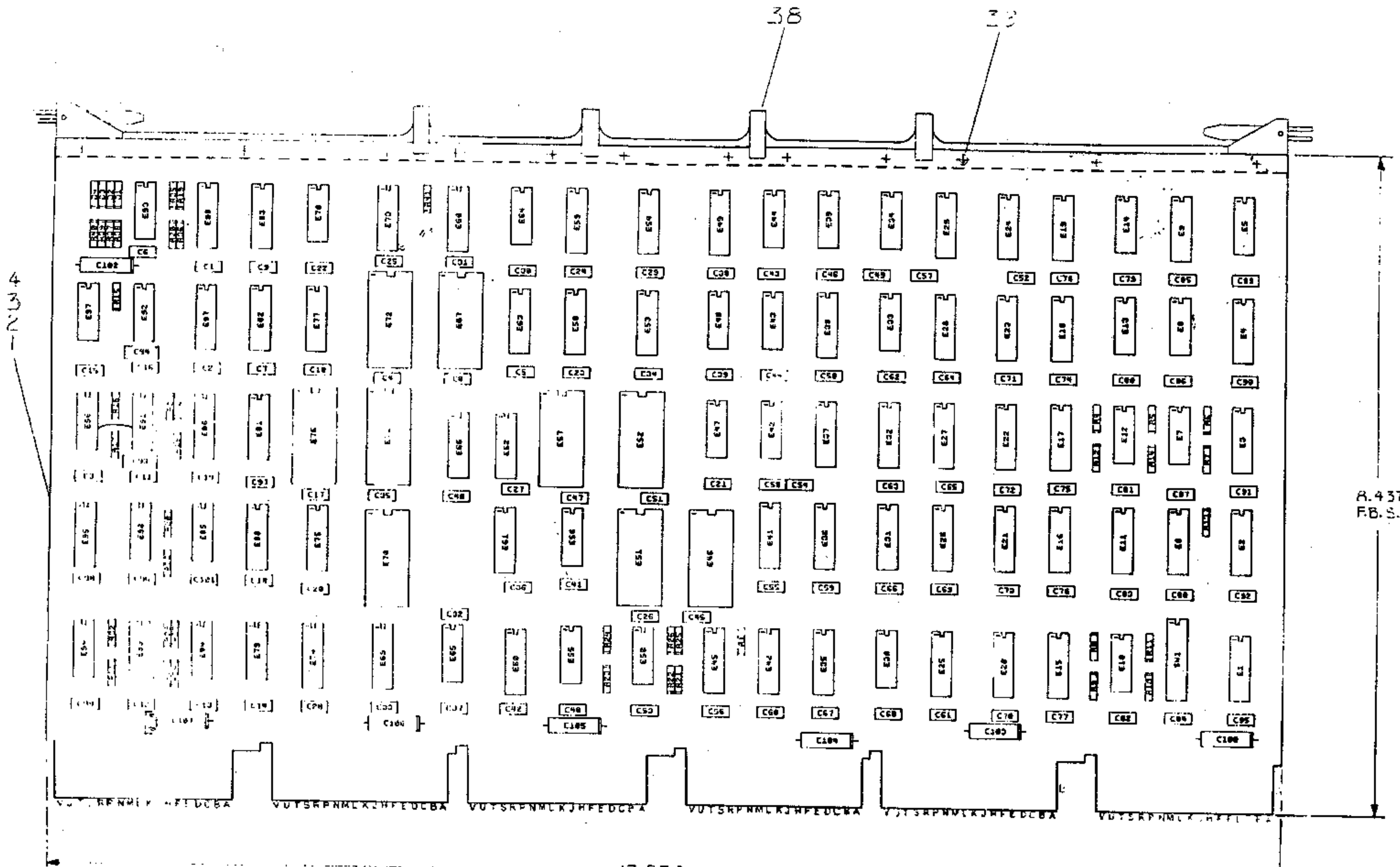
TITLE: CIRCUIT SCHEMATIC

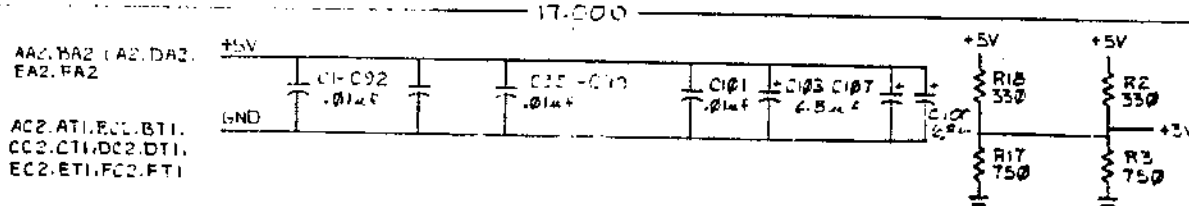
SIZE	CODE	NUMBER	REV
D	CS	5411420-0-1	C

DIST.

DCS-5411420-0-1, C

NOTES:





74..	8	16
74..	8	16
74153	8	16
74181	12	24
74150	12	24
74175	8	16
74174	8	16
8640	1	8
74157	8	16
8838	8	16
3341	8	16	1
IC TYPE	GND	+5V	-12V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

PARTS LIST

QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7836-0-4	1
REF		ASSY DRILLING HOLE LAYOUT	D-AH-M7836-0-5	2
REF		MODULE ECO HISTORY	B-MH-M7836-0-6	3
1		ETCHED CIRCUIT BOARD	5010976	4
1	C93	CAP 10 PF 100V 5% DM	1000006	5
1	C94	CAP 100 PF 100V 5% DM	1000016	6
98	C1 THRU C92, C95-C97, C101	CAP .01 UF 100V 20% CER	1001610-01	7
7	C100, C102 THRU C107	CAP 6.8 UF 35V 10% tant	1005306	8
4	D1-D4	DIODE D664	1103114	9
2	R2, R18	RES. 330 1 4W 5%	1300295	10
1	R1	RES. 470 1 4W 5%	1300316	11
1	R15	RES. 3K 1 4W 5%	1300432	12
12	R4-R14, R41	RES. 1K 1 4W 5%	1300365	13
2	R3, R17	RES 750 1 4W 5%	1301401	14
1	R16	RES. 18K 1 4W 5%	1302465	15
4	E5, E55, E90, E11	IC 7474	1905547	16
1	E55	IC 7442	19[illegible]	17
1	E78	IC 7420	1905577	18
1	E84	IC 7402	1909004	19
3	E14, 30, 65	IC 7404	1909686	20
1	E9	IC 8881	1909705	21
3	E7, 10, 12	IC 8242	1909712	22
4	E13, 50, 89, 97	IC 8640	19114[illegible]	23
4	E38, 41, 53, 54	IC 74153	1909937	24
5	E46, 52, 57, 70, 71	IC 74181	1909982	25
10	E33, 34, 39, 42, 43, 44, 47, 48, 56, 64	IC 7486	1910011	26
2	E79, 96	IC 7437	1910091	27
4	E51, 67, 72, 76	IC 74150	1910153	28
2	E91, 92	IC 74121	1910230	29
7	E4, 9, 19, 28, 82, 62, [illegible]	IC 74175	1910651	30
13	E53, 59, 60, 61, 63, 66, 18, 23, 27, 31, 45, 35, 36	IC 74174	1910652	31
4	E1, 37, 40, 32	IC 74157	1910655	32
1	E35	IC 74155	1910656	33
4	E3, 15, 20, [illegible]	IC 8838	1911117	34
1	E94	IC 7408	1910159	35
8	E24, 73, 81, 29, 83, 86, 85, 68	IC 3341	2111188	36
1	SW1	SWITCH 10 POS	1211164-06	37
1		HEX HANDLE ASSY	1210711-2	38
12		EYELET	9006732	39
11	R19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39	RES. 180, 1/4W, 5%	1301322	40
11	R20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40	RES. 330, 1/4W, 5%	1300309	41
1		COVER SWITCH 10 POS	1211084-06	42
14	E2, 6, 11, 16, 17, 21, 22, 26, 69, 74, 75, 77, 80, 87	IC 74151	1909936	43
A/R		WIRE #30 AWG INSULATED	4105740	44

FIRST USED ON OPTION MODEL: DV11-AA

ETCH BOARD REV: A

REV: A

CHANGE NO

REVISIONS

ORIGINATED

CHK

DEC NO	EIA NO	DEC NO	EIA NO

SEMICONDUCTOR CONVERSION CHART

DRN / CHKD / ENG / PROJ. ENG / PROD

NEXT HIGHER ASSY: B-DD-DV11-0

SCALE

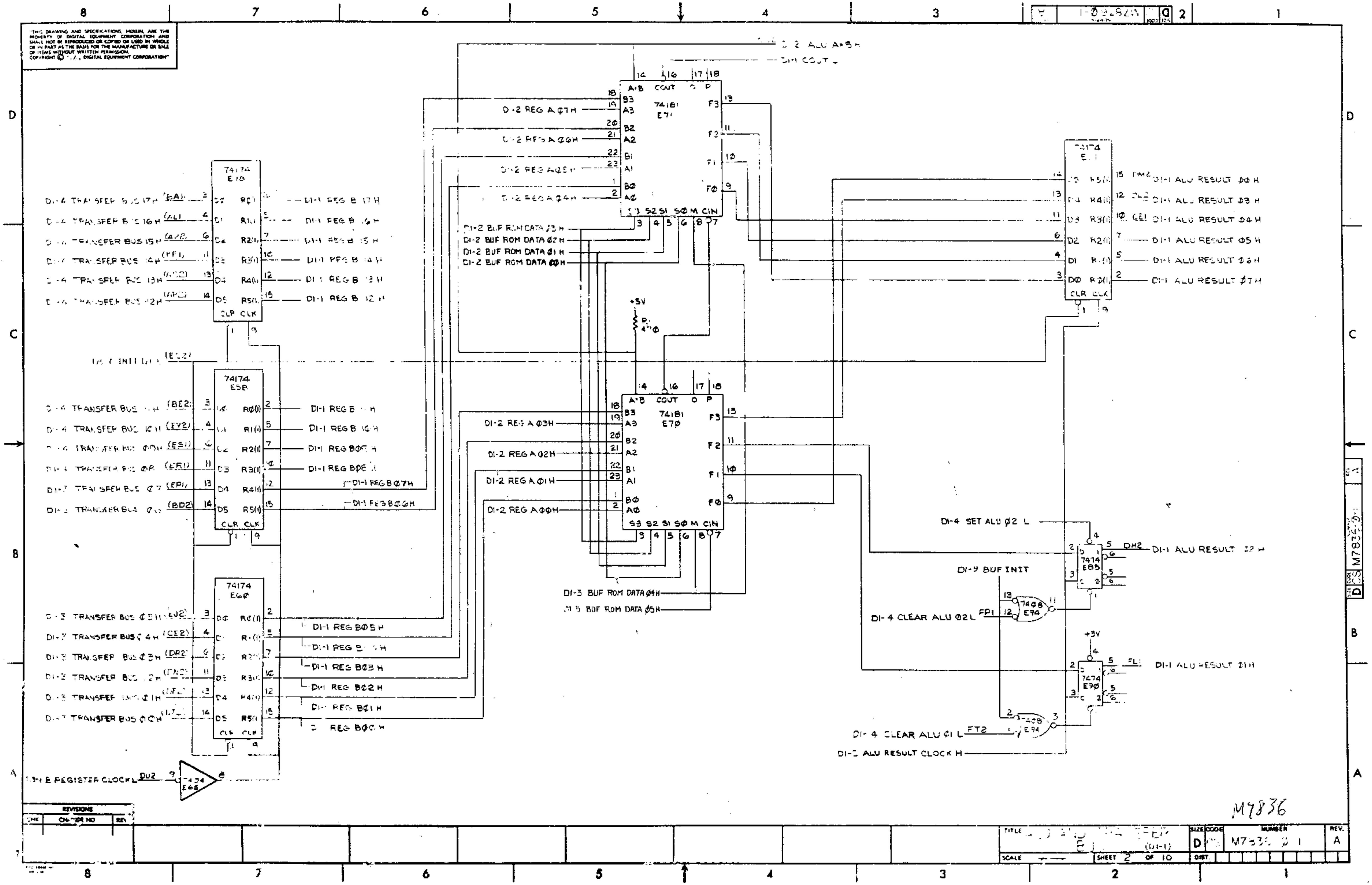
SHEET 1 OF 10

DIST

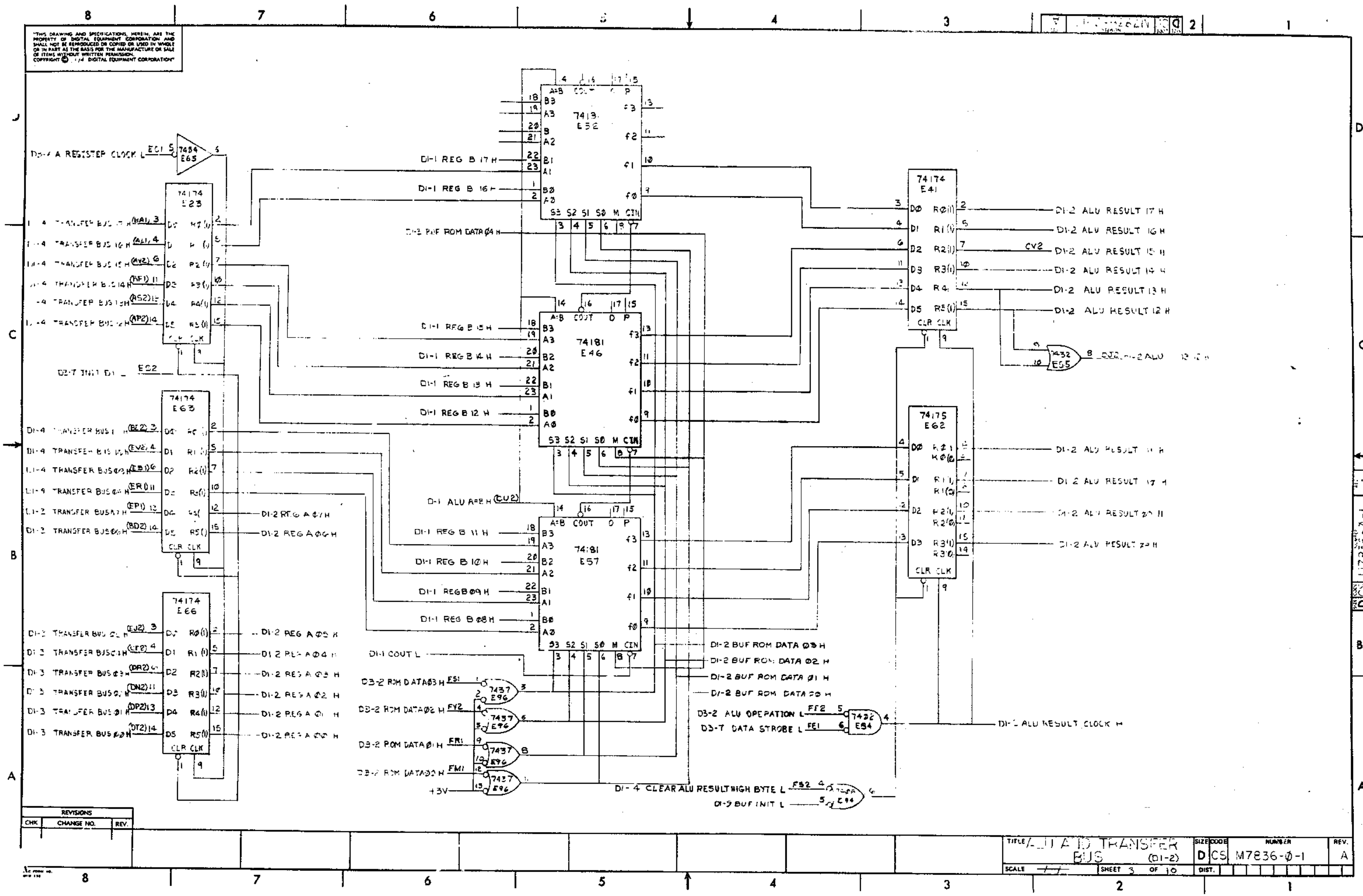
digital EQUIPMENT CORPORATION

TITLE: ALU AND TRANSFER BUS

SIZE: D CODE: CS NUMBER: M7836-0-1 REV: A



74174
E18
74174
E58
74174
E60
74181
E71
74181
E70
74174
7474
E85
7474
E30
7408
E94
7404
E65
DI-2 REG A Ø7H
DI-2 REG A Ø6H
DI-2 REG A Ø5H
DI-2 REG A Ø4H
DI-2 REG A Ø3H
DI-2 REG A Ø2H
DI-2 REG A Ø1H
DI-2 REG A ØØH
DI-2 BUF ROM DATA Ø2H
DI-2 BUF ROM DATA Ø1H
DI-2 BUF ROM DATA ØØH
DI-3 BUF ROM DATA Ø4H
DI-1 ALU RESULT ØØ H
DI-1 ALU RESULT Ø3 H
DI-1 ALU RESULT Ø4 H
DI-1 ALU RESULT Ø5 H
DI-1 ALU RESULT Ø6 H
DI-1 ALU RESULT Ø7 H
DI-4 SET ALU Ø2 L
DI-9 BUF INIT
DI-4 CLEAR ALU Ø2 L
DI-4 CLEAR ALU Ø1 L
DI-1 REG BØ7H
DI-1 REG BØ5 H
DI-1 REG BØ3 H
DI-1 REG BØ2 H
DI-1 REG BØ1 H
DI-4 TRANSFER BUS 16 H
DI-4 TRANSFER BUS 15 H
DI-4 TRANSFER BUS 14 H
DI-4 TRANSFER BUS 13 H
DI-4 TRANSFER BUS 12 H
DI-3 TRANSFER BUS Ø5 H
DI-3 TRANSFER BUS Ø4 H
DI-3 TRANSFER BUS Ø3 H
DI-3 TRANSFER BUS ØØ H
+5V
A•B
COUT
CIN
M7836



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74174 E23
74174 E63
74174 E66
74181 E52
74181 E46
74181 E57
74174 E41
74175 E62
7404 E65
7432 E55
7437 E96
7432 E54
DI-1 REG B 17 H
DI-1 REG B 16 H
DI-3 BUF ROM DATA Ø4 H
DI-1 REG B 15 H
DI-1 REG B 14 H
DI-1 REG B 13 H
DI-1 REG B 12 H
DI-1 ALU A=B H
DI-1 REG B 11 H
DI-1 REG B 10 H
DI-1 REG B Ø9 H
DI-1 REG B Ø8 H
DI-1 COUT L
D3-2 ROM DATA Ø3 H
D3-2 ROM DATA Ø2 H
D3-2 ROM DATA Ø1 H
D3-2 ROM DATA ØØ H
+3V
DI-2 BUF ROM DATA Ø3 H
DI-2 BUF ROM DATA Ø2 H
DI-2 BUF ROM DATA Ø1 H
DI-2 BUF ROM DATA ØØ H
D3-2 ALU OPERATION L
D3-7 DATA STROBE L
DI-2 ALU RESULT CLOCK H
DI-4 CLEAR ALU RESULT HIGH BYTE L
DI-9 BUF INIT L
DI-2 ALU RESULT 17 H
DI-2 ALU RESULT 16 H
DI-2 ALU RESULT 15 H
DI-2 ALU RESULT 14 H
DI-2 ALU RESULT 13 H
DI-2 ALU RESULT 12 H
DI-2 ALU RESULT 11 H
DI-2 ALU RESULT 10 H
DI-2 ALU RESULT Ø9 H
DI-2 ALU RESULT Ø8 H
DI-2 REG A Ø7 H
DI-2 REG A Ø6 H
DI-2 REG A Ø5 H
DI-2 REG A Ø4 H
DI-2 REG A Ø3 H
DI-2 REG A Ø2 H
DI-2 REG A Ø1 H
DI-2 REG A ØØ H
D2-7 INIT DI L
DI-4 TRANSFER BUS 17 H
DI-4 TRANSFER BUS 16 H
DI-4 TRANSFER BUS 15 H
DI-4 TRANSFER BUS 14 H
DI-4 TRANSFER BUS 13 H
DI-4 TRANSFER BUS 12 H
DI-4 TRANSFER BUS Ø7 H
DI-3 TRANSFER BUS Ø6 H
REVISIONS
CHK | CHANGE NO. | REV.
TITLE ALU AND TRANSFER BUS (DI-2)
SIZE D CODE CS NUMBER M7836-Ø-1 REV. A
SCALE
SHEET 3 OF 10
DIST.

D3-2 TRANSFER SOURCE ENAB L DK2

DI-1 REGISTER B 15 H
DI-9 NPR DATI Ø7 H
D3-11 RAM OUTPUT Ø7 H
DI-5 SILO OUT Ø7 H
D2-6 NPR DATO Ø7 H
DI-7 BCC Ø7 H
DI-1 ALU RESULT Ø7 H
EK2 EN2
STB 74151 E74 — f1 → EP1 DI-3 TRANSFER BUS Ø7 H; f0
D3-2 ROM DATA Ø4 H EV1 — 7437 E79 — +3V
S2 S1 S0 — OC1 DI-3 BUF ROM DATA Ø4 H

DI-1 REGISTER B 14 H
DI-9 NPR DATI Ø6 H
D3-11 RAM OUTPUT Ø6 H
DI-5 SILO OUT Ø6 H
D2-6 NPR DATO Ø6 H
DI-7 BCC Ø6 H
DI-1 ALU RESULT Ø6 H
BD1 BE1
STB 74151 E21 — f1 → BD2 DI-3 TRANSFER BUS Ø6 H; f0
D3-2 ROM DATA Ø5 H ET2 — 7437 E79 — +3V
S2 S1 S0 — EM1 DI-3 BUF ROM DATA Ø5 H

DI-1 REGISTER B 13 H
DI-9 NPR DATI Ø5 H
D3-11 RAM OUTPUT Ø5 H
DI-5 SILO OUT Ø5 H
D2-6 NPR DATO Ø5 H
DI-7 BCC Ø5 H
DI-1 ALU RESULT Ø5 H
EE1 EH2
STB 74151 E69 — f1 → EJ2 DI-3 TRANSFER BUS Ø5 H; f0
D3-2 ROM DATA Ø6 H FJ1 — 7437 E79 — +3V
S2 S1 S0 — DI-3 BUF ROM DATA Ø6 H

DI-1 REGISTER B 12 H
DI-9 NPR DATI Ø4 H
D3-11 RAM OUTPUT Ø4 H
DI-5 SILO OUT Ø4 H
D2-6 NPR DATO Ø4 H
DI-7 BCC Ø4 H
DI-1 ALU RESULT Ø4 H
CD2 CF2 (CE1)
STB 74151 E26 — f1 → CE2 DI-3 TRANSFER BUS Ø4 H; f0
S2 S1 S0

D3-4 MASTER SCAN Ø3 H
DI-2 ALU RESULT 11 H
DI-1 REGISTER B 11 H
DI-9 NPR DATI Ø3 H
D3-11 RAM OUTPUT Ø3 H
DI-5 SILO OUT Ø3 H
D2-6 NPR DATO Ø3 H
DI-7 BCC Ø3 H
DI-1 ALU RESULT Ø3 H
EH1 ELI EF2 (DL2)
STB 74150 E72 — f → 7404 E65 → DR2 DI-3 TRANSFER BUS Ø3 H
S3 S2 S1 S0

D3-4 MASTER SCAN Ø2 H
DI-2 ALU RESULT 10 H
DI-1 ALU RESULT Ø7 H
DI-1 REGISTER B 10 H
DI-9 NPR DATI Ø2 H
D3-11 RAM OUTPUT Ø2 H
DI-5 SILO OUT Ø2 H
D2-6 NPR DATO Ø2 H
DI-7 BCC Ø2 H
DI-1 ALU RESULT Ø2 H
DE2 EU2 DF2 (DH2)
STB 74150 E51 — f → 7404 E35 → DN2 DI-3 TRANSFER BUS Ø2 H
S3 S2 S1 S0

D3-2 ROM DATA Ø7 H DS2 — 7404 E65 → DI-3 BUF ROM DATA Ø7 H

D3-4 MASTER SCAN Ø1 H
DI-2 ALU RESULT 39 H
DI-1 ALU RESULT 35 H
DI-1 REGISTER B 09 H
DI-9 NPR DATI Ø1 H
D3-11 RAM OUTPUT Ø1 H
DI-5 SILO OUT Ø1 H
D2-6 NPR DATO Ø1 H
DI-7 BCC Ø1 H
DI-1 ALU RESULT Ø1 H
EF2 EJ1 ED2 (FL1)
STB 74150 E67 — f → 7404 E30 → EP2 DI-3 TRANSFER BUS Ø1 H
S3 S2 S1 S0

D3-4 MASTER SCAN Ø0 H
DI-2 ALU RESULT Ø8 H
DI-1 ALU RESULT 35 H
DI-1 REGISTER B Ø8 H
DI-9 NPR DATI Ø0 H
D3-11 RAM OUTPUT Ø0 H
DI-5 SILO OUT Ø0 H
D2-6 NPR DATO Ø0 H
DI-7 BCC Ø0 H
DI-1 ALU RESULT Ø0 H
FD2 ED1 EK1 (DH2)
STB 74152 E76 — f → 7404 E65 → DT2 DI-3 TRANSFER BUS Ø0 H
S3 S2 S1 S0

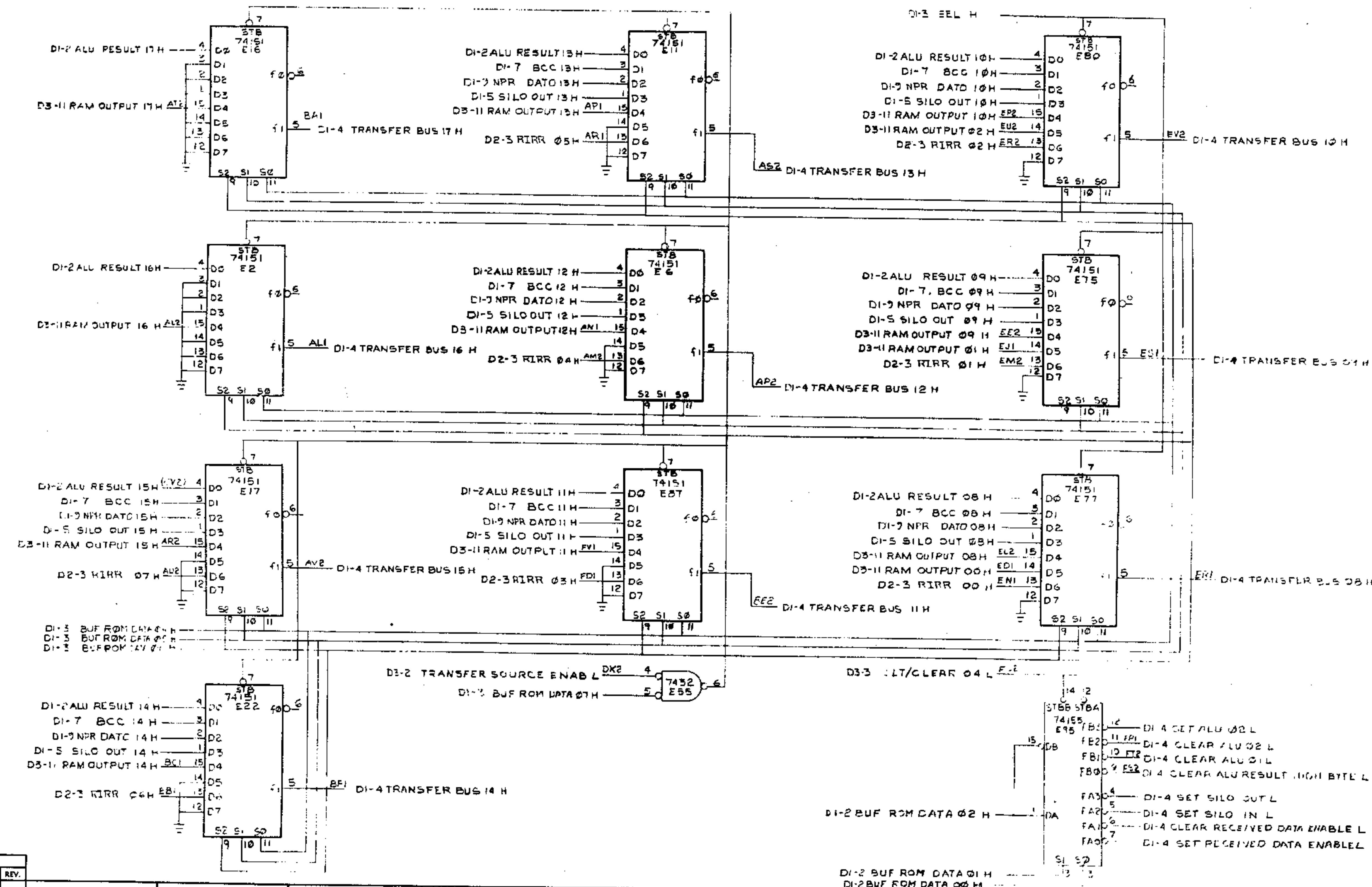
D3-4 MASTER SCAN Ø0 H
DI-2 ALU RESULT Ø8 H
DI-1 ALU RESULT 35 H
DI-1 REGISTER B Ø8 H
DI-9 NPR DATI Ø0 H
D3-11 RAM OUTPUT Ø0 H
DI-5 SILO OUT Ø0 H
D2-6 NPR DATO Ø0 H
DI-7 BCC Ø0 H
DI-1 ALU RESULT Ø0 H
FD2 ED1 EK1 (DH2)
STB 74152 E76 — f → 7404 E65 → DT2 DI-3 TRANSFER BUS Ø0 H
S3 S2 S1 S0

7432 E55 → DI-3 SEL H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ALU AND TRANSFER BUS (DI-3)
SIZE D CODE CS NUMBER M7836-Ø-1 REV. A
SCALE — SHEET 4 OF 13 DIST.

DCS M7836-Ø-1 REV. A

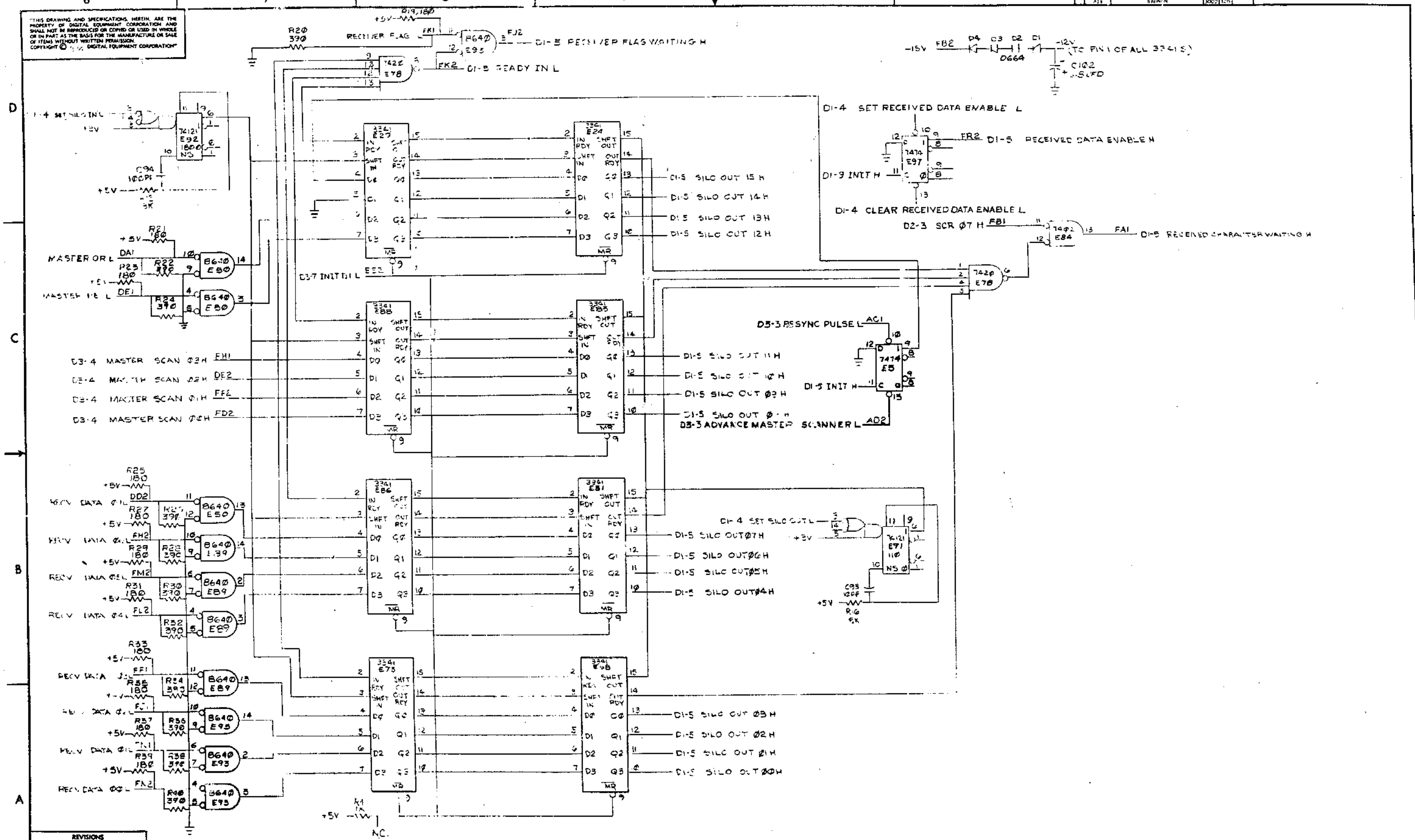


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ALU AND TRANSFER BUS (DI 4)

SIZE D | CODE CS | NUMBER M7836-Ø-1 | REV. A

SHEET 5 OF 10



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: SILO AND TRANSFER BUS (D1-5)

SIZE: D | CODE: CS | NUMBER: M7836-Ø-1 | REV. A

SHEET 6 OF 10

DI-2 REG A Ø H
DI-1 REG B Ø H — 7486 E56 — DI-6 LRC ØØ H

DI-2 REG A 1 H
DI-1 REG B 1 H — 7486 E56 — DI-6 LRC Ø1 H

DI-2 REG A 2 H
DI-1 REG B 2 H — 7486 E56 — DI-6 LRC Ø2 H

DI-2 REG A 3 H
DI-1 REG B 3 H — 7486 E56 — DI-6 LRC Ø3 H

DI-2 REG A 4 H
DI-1 REG B 4 H — 7486 E64 — DI-6 LRC Ø4 H

DI-2 REG A 5 H
DI-1 REG B 5 H — 7486 E64 — DI-6 LRC Ø5 H

DI-2 REG A 6 H
DI-1 REG B 6 H — 7486 E64 — DI-6 LRC Ø6 H

DI-2 REG A 7 H
DI-1 REG B 7 H — 7486 E64 — DI-6 LRC Ø7 H

DI-1 REG B 11 H — 7486 E42 — DI-6 CRC-CCITT 12 H

DI-1 REG B 14 H — 7486 E48 — DI-6 CRC-CCITT Ø6 H

DI-6 CRC16-Ø6 H
DI-6 CRC16-Ø5 H
DI-6 CRC16-Ø8 H
DI-6 CRC16-Ø9 H
DI-6 CRC16-1Ø H
DI-6 CRC16-11 H
DI-6 CRC16-12 H
DI-6 CRC-CCITT 13 H
DI-6 CRC CCITT 14 H
DI-6 CRC-CCITT 15 H

DI-1 REG B 8 H
DI-1 REG B 9 H
DI-1 REG B 1Ø H
DI-1 REG B 12 H
DI-1 REG B 15 H
DI-1 REG B 13 H

DI-6 CRC16-14 H
DI-6 CRC16-15 H
DI-6 CRC16-13 H
DI-6 CRC CCITT ØØ H
DI-6 CRC CCITT Ø1 H
DI-6 CRC-CCITT Ø2 H
DI-6 CRC-CCITT Ø7 H
DI-6 CRC-CCITT Ø8 H
DI-6 CRC-CCITT Ø9 H
DI-6 CRC-CCITT 1Ø H
DI-6 CRC-CCITT Ø5 H
DI-6 CRC-CCITT Ø4 H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ALU AND TRANSFER BUS (DI-6)	D	CS	M7836-Ø-1	A
SCALE —	SHEET 7 OF 10	DIST.		

DEC M7836-Ø-1

DI-6 CRC-CCITT Ø1 H
DI-6 REG B Ø9 H
DI-6 LRC Ø1 H
74153 E49 1/2

DI-6 CRC-CCITT ØØ H
DI-6 CRC-16 ØØ H
DI-6 LRC ØØ H
74153 E49 1/2

DI-6 CRC-CCITT Ø3 H
DI-6 REG B 11 H
DI-6 LRC Ø3 H
74153 E53 1/2

DI-6 CRC-CCITT Ø2 H
DI-6 REG B 10 H
DI-6 LRC Ø2 H
74153 E53 1/2

DI-6 CRC-CCITT Ø5 H
DI-6 REG B 13 H
DI-6 LRC Ø5 H
74153 E54 1/2

DI-6 CRC-CCITT Ø4 H
DI-6 REG B 12 H
DI-6 LRC Ø4 H
74153 E54 1/2

DI-6 CRC-CCITT Ø7 H
DI-6 CRC-16 Ø7 H
DI-6 LRC Ø7 H
74153 E38 1/2

DI-6 CRC-CCITT ØG H
DI-6 CRC-16 ØG H
DI-6 LRC ØG H
74153 E38 1/2

L3-11 RAM CLK 3
OUTPUT Ø4H
74Ø4 E56
+3V
74Ø7 E79

74174 E59
D0 R0(1) — DI-7 BCC Ø5 H
D1 R1(1) — DI-7 BCC Ø4 H
D2 R2(1) — DI-7 BCC Ø3 H
D3 R3(1) — DI-7 BCC Ø2 H
D4 R4(1) — DI-7 BCC Ø1 H
D5 R5(1) — DI-7 BCC ØØ H
CLR CLK

DI-6 CRC-16 Ø8 H
DI-6 CRC-CCITT Ø8 H
DI-6 CRC-16 Ø9 H
DI-6 CRC-CCITT Ø9 H
DI-6 CRC-16 1Ø H
DI-6 CRC-CCITT 1Ø H
DI-6 CRC-1611 H
DI-6 LRC Ø3 H
74157 E37
STB SØ

74174 E36
D5 R5(1) — DI-7 BCC Ø8 H
D4 R4(1) — DI-7 BCC Ø9 H
D3 R3(1) — DI-7 BCC 1Ø H
D2 R2(1) — DI-7 BCC 11 H
D1 R1(1) — DI-7 BCC 12 H
D0 R0(1) — DI-7 BCC 13 H
CLR CLK

D3-11 RAM OUTPUT Ø3 L
74Ø4 E65

DI-6 CRC-16 12 H
DI-6 CRC-CCITT 12 H
DI-6 CRC-16 13 H
DI-6 CRC-CCITT 13 H
DI-6 CRC-16 14 H
DI-6 CRC-CCITT 14 H
DI-6 CRC-16 15 H
DI-6 CRC-CCITT 15 H
74157 E32
STB SØ

74175 E31
D3 R3(1) — DI-7 BCC 14 H
D2 R2(1) — DI-7 BCC 15 H
D1 R1(1) — DI-7 BCC ZS H
D0 R0(1) — DI-7 BCC Ø7 H
CLR CLK

D3-7 INIT DI L (ES2)
D3-7 DATA STROBE L FE1
D3-2 BCC CALCULATION L FC1
74Ø2 E84

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE ALU AND TRANSFER BUS (DI-7)
SIZE D CODE CS NUMBER M7836-Ø-1 REV A
SCALE — SHEET 8 OF 10 DIST.

D3-2 ROM DATA Ø9 H
D3-2 ROM DATA Ø8 H
DI-4 TRANSFER BUS 17 H
DI-4 TRANSFER BUS 16 H
DI-9 BUF INIT L
D3-6 NPR ADDRESS REGISTER CLOCK L
DI-4 TRANSFER BUS 15 H
DI-4 TRANSFER BUS 14 H
DI-4 TRANSFER BUS 13 H
DI-4 TRANSFER BUS 12 H
DI-4 TRANSFER BUS 11 H
DI-4 TRANSFER BUS 10 H
DI-4 TRANSFER BUS Ø9 H
DI-4 TRANSFER BUS Ø8 H
DI-3 TRANSFER BUS Ø7 H
DI-3 TRANSFER BUS Ø6 H
D3-7 INIT DI L
DI-3 TRANSFER BUS Ø5 H
DI-3 TRANSFER BUS Ø4 H
DI-3 TRANSFER BUS Ø3 H
DI-3 TRANSFER BUS Ø2 H
DI-3 TRANSFER BUS Ø1 H
DI-3 TRANSFER BUS ØØ H

74175 E4
74175 E9
74174 E27
74174 E25
7404 E3Ø
8838 E3
8838 E2Ø
8838 E15
8838 E25
8881 E8
8240 E13
8242 E7
8242 E10
8242 E12

D2-7 ADDRESS TO BUS L
DI-8 C1 H
DI-8 BUS C1 L
DI-8 C0 H
DI-8 BUS C0 L
DI-8 A17 H
DI-8 BUS A17 L
DI-8 BUS A12 L
DI-8 BUS A11 L
DI-8 BUS A10 L
DI-8 BUS A09 L
DI-8 BUS A08 L
DI-8 BUS A07 L
DI-8 BUS A06 L
DI-8 BUS A05 L
DI-8 BUS A04 L
DI-8 BUS A03 L
DI-8 A03 H
DI-8 BUS A02 L
DI-8 A02 H
DI-8 BUS A01 L
DI-8 A01 H
DI-8 BUS A00 L
DI-8 A00 H
DI-8 NPR ADDR ØC H
DI-8 BUS A16 L
DI-8 BUS A15 L
DI-8 BUS A14 L
DI-8 BUS A13 L
DI-8 ADDRESS SELECTED H

S1-1 R6 1K
S1-2 R7 1K
S1-3 R8 1K
S1-4 R9 1K
S1-5 R10 1K
S1-6 R11 1K
S1-7 R12 1K
S1-8 R13 1K
S1-9 R14 1K
+5V
R4 1K
R5 1K

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ALU AND TRANSFER BUS (CPU)	D	CS	M7836-Ø-1	A
SCALE	SHEET 3 OF 10	DIST.		

BUS PB L ANZ — 8640 E13 — BUS PA L AM1 — 8640 E13

7408 E94 — DI-9 MEM PAR ERR H

D2-3 BUF DATAØ4 H AK2 — D2-3 BUF DATAØ6 H AJ2 — 74157 E1 — ST8 SØ
D2-3 BUF DATAØ1 H AH2 — D2-3 BUF DATAØ9 H AF1
D2-3 BUF DATAØ2 H AE2 — D2-3 BUF DATA 10 H AF2
D2-3 BUF DATAØ3 H AH1 — D2-3 BUF DATA 11 H AE1

DI-8 NPR ADDR ØØ H CH2

74175 E28 — CLR CLK
D3 R3(1) — R3(Ø)
D2 R2(1) — R2(Ø)
D1 R1(1) — R1(Ø) — DI-9 NPR DATI Ø2 H
DØ RØ(1) — RØ(Ø) — DI-9 NPR DATI Ø3 H

74175 E52 — CLR CLK
DI-4 TRANSFER BUS ØØ H — DI-9 NPR DATO ØØ H
DI-4 TRANSFER BUS Ø9 H — DI-9 NPR DATO Ø9 H
DI-4 TRANSFER BUS 1Ø H — DI-9 NPR DATO 1Ø H
DI-4 TRANSFER BUS 11 H — DI-9 NPR DATO 11 H

D2-3 BUF DATA Ø4 H CS2 — D2-3 BUF DATA 12 H CR2 — 74157 E48 — ST8 SØ
D2-3 BUF DATA Ø5 H CP2 — D2-3 BUF DATA 13 H CN2
D2-3 BUF DATA Ø6 H CL2 — D2-3 BUF DATA 14 H CK2
D2-3 BUF DATA Ø7 H CJ2 — D2-3 BUF DATA 15 H CM2

74174 E45 — CLR CLK
D4 R4(1) — DI-9 NPR DATI ØØ H
D1 R1(1) — DI-9 NPR DATI Ø1 H
D5 R5(1) — DI-9 NPR DATI Ø4 H
D3 R3(1) — DI-9 NPR DATI Ø5 H
D2 R2(1) — DI-9 NPR DATI Ø6 H
DØ RØ(1) — DI-9 NPR DATI Ø7 H

74175 E19 — CLR CLK
DI-4 TRANSFER BUS 12 H — DI-9 NPR DATO 12 H
DI-4 TRANSFER BUS 13 H — DI-9 NPR DATO 13 H
DI-4 TRANSFER BUS 14 H — DI-9 NPR DATO 14 H
DI-4 TRANSFER BUS 15 H — DI-9 NPR DATO 15 H

D3-7 DATA STROBE H CT2 — 7404 E14 — 7402 E84 — DI-9 BUF INIT L
DI-9 INIT H

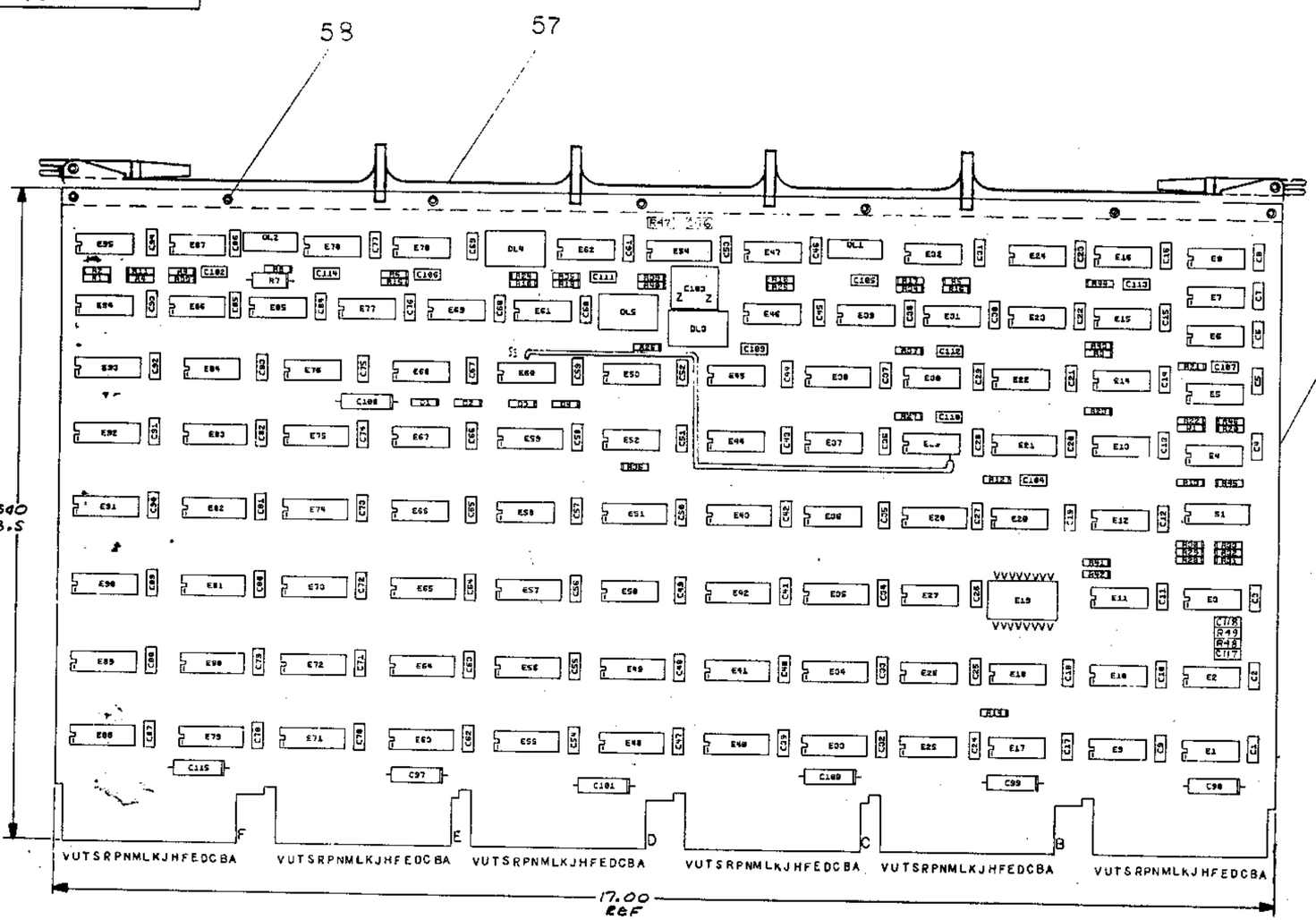
D3-7 INIT DI L ES2

D3-6 NPR DATO REGISTER CLOCK L AU1 — 7404 E14

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ADD END TRANSFER BUS (01-9)	D	CS	M7836-Ø-1	A
SCALE —	SHEET 10 OF 10	DIST.		

NOTES: R47, R48, R49, C116, C117, C118 ARE ECO #8 ADDITIONS.



REF			
REF		X-COORDINATE HOLE LOCATION	K-CO-M7837-04	1
REF		ASS'B/DRILLING HOLE LAYOUT	D-AH-M7837-0-5	2
REF		MODULE ECO HISTORY	B-MH-M7837-0-6	3
1		ETCHED CIRCUIT BOARD	5010-177	4
3	C104 C110, C111	CAP 10 PF 100V 5%	1000006	5
5	C109, C106, C112 C102, C107	CAP 100 PF 100V 5%	1000016	6
3	C113, C117, C118	CAP 330 PF 100V 5%	1000023	7
2	C105, C116	CAP 470 PF 100V 5%	1000024	8
1	C103	CAP 1500 PF 100V 5%	1002428	9
94	C1 – C96	CAP .01 UF 100V 20%	1001610-01	10
7	C97-C101, C108, C115	CAP 6.8 UF 35V 10%	1005306	11
4	D1-D4	DIODE D664	1100114	12
10	E8, E12, E22, E53, E60, E66 E67, E77 E84, E95	I.C DEC 7474	1905547	13
3	E15, E69, E86	I.C DEC 7400	1905575	14
1	E68	I.C DEC 7410	1905576	15
6	E6, E13, E24, E31, E36, E94	I.C DEC 7402	1909004	16
1	E76	I.C DEC 74H55	1909063	17
7	E4, E7, E18, E25, E26, E27, E32	I.C DEC 8640	1911969	18
1	E61	I.C DEC 74H74	1909667	19
3	E16, E44, E50	I.C DEC 7404	1909686	20
8	E1, E2, E3, E9, E10, E11 E14, E17	I.C DEC 8881	1909705	21
16	E71, E72, E73, E74, E75 E79, E80, E81, E82, E83 E88, E89, E90, E91, E92, E93	I.C DEC 74151	1909936	22
1	E38,	I.C DEC 7442	1910046	23
1	E51	I.C DEC 9015	1910087	24
2	E37, E58	I.C DEC 7437	1910091	25
4	E23, E47, E52, E85	I.C DEC 7408	1910155	26
9	E5, E20, E29, E30, E45 E62, E70, E78, E87	I.C DEC 74121	1910230	27
7	E28, E34, E40, E48, E56, E59, E63	I.C DEC 74175	1910651	28
3	E33, E64, E65	I.C DEC 74174	1910652	29
4	E35, E81, E42, E43	I.C DEC 74157	1910655	30
1	E49	I.C DEC 74155	1910656	31
1	E54	I.C DEC 74123	1910936	32
14	R28, R29, R30, R31, R32, R33, R35 R11, R26, R15, R16, R19, R42, R36	RES 1K 1/8W 5%	1300365	33
1	R37	RES 2K 1/8W 5%	1300432	34
1	R17	RES 3.8K 1/8W 5%	1300459	35
1	R34	RES 10K 1/8W 5%	1300479	36
QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

ETCH BOARD REV. 8

FIRST USED ON OPTION MODEL: DV11-AA

I.C DEC 74151	8	16
I.C DEC 7442	8	16
I.C DEC 9015	8	16
I.C DEC 74175	8	16
I.C DEC 74174	8	16
I.C DEC 74157	8	16
I.C DEC 74155	8	16
I.C DEC 74123	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV.	CHANGE NO.	CHK	DESIGNATED
A			
B			
C	M7837-00002		J MCNAMARA 6-Nov-75
D	M7837-00001		J MCNAMARA 6-2-75

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN. George Snyder	DATE	11/24/75
CHK'D.	DATE	12/6/75
ENG.	DATE	3-28-75
PROJ. ENG.	DATE	3-10-75
PROD.	DATE	2-13-75

NEXT HIGHER ASSY: B-DD-DV11-0

SCALE: 1/1

SHEET 1 OF 11

digital

TITLE: UNIBUS DATA AND NPR CONTPROL

SIZE	CODE	NUMBER	REV.
D	CS	M7837-0-1	C

DIST.

SIZE D CODE CS NUMBER M7837-0-1 REV. C

[illegible]	[illegible]	RES [illegible] 1/4 W 5%	[illegible]32	[illegible]
3	R2, R3? R42	RES 750Ω 1/4W 5%	1301401	[illegible]
3	R43, R13, R20	RES 390Ω 1/4 W 5%	1300309	39
1	R7	RES 2.21K 1/2W 1% RN6Ø	1312431	40
[illegible]	R35	RES 18K 1/4 W 5%	1302965	41
2	R6, R7	RES 2.74K 1/4 W 1% RN55	1304868	42
1	R26	RES 4.7K 1/4 W 5%	1300447	43
3	R44, R48, R49	RES 220Ω 1/4 W 5%	1300271	44
1	R16	RES 100 Ω 1/4 W 5%	1300229	45
5	R1, R40, R41, R5, R8	RES 330Ω 1/4 W 5%	1300295	46
2	R27, R12	RES 6.8K 1/4 W 5%	1301423	47
2	R4, R38	RES 470Ω 1/4 W 5%	1300316	48
1	R10	RES 47K 1/4 W 5%	1302177	49
1	R21	RES 1.5K 1/4 W 5%	1300591	50
1		SWITCH [illegible] 8 POS	1211264-[illegible]	51
1	E19	SOCKET GLASS	12 09838	52
1	S1	SWITCH ROCKER DIP	1211164-[illegible]	53
2	DL1, DL2	DELAY LINE 30 NS	1605528	54
2	DL4, DL5	DELAY LINE 50 NS	1609426	55
1	DL3	DELAY LINE 100NS	1609559	56
1		HANDLE HEX	1215711-[illegible]	57
12		EYELET	9006732	58
1	W1	JUMPER INSULATED	9009185	59
1	E21	IC DEC 74193	1910018	60
2	E55, E57	I.C DEC 3341	2111188	61
1	C114	CAP, 68PF, 100V, 5%	1000014	62
2	E39, E46	I.C. DEC 7432	1911521	63
A/R		WIRE, #30 AWG INSULATED	9105740	64
1	R47	RES 15KΩ 1/4W 5%	1300496	65

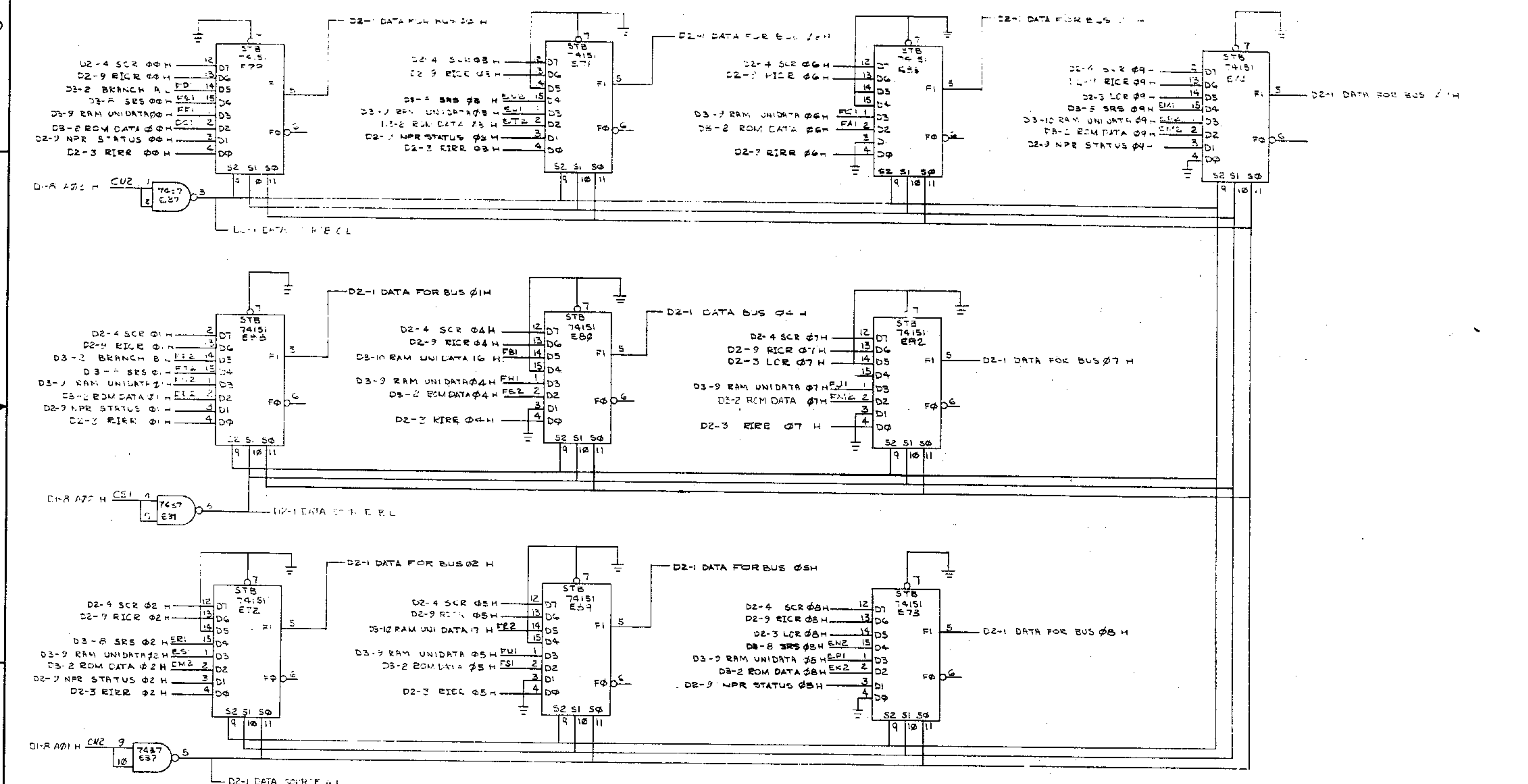
REVISIONS

CHK	CHANGE NO	REV

TITLE UNIBUS DATA AND NPR CONTROL

SIZE D CODE CS NUMBER M7837-Ø-1 REV. C

SCALE — SHEET 2 OF 11

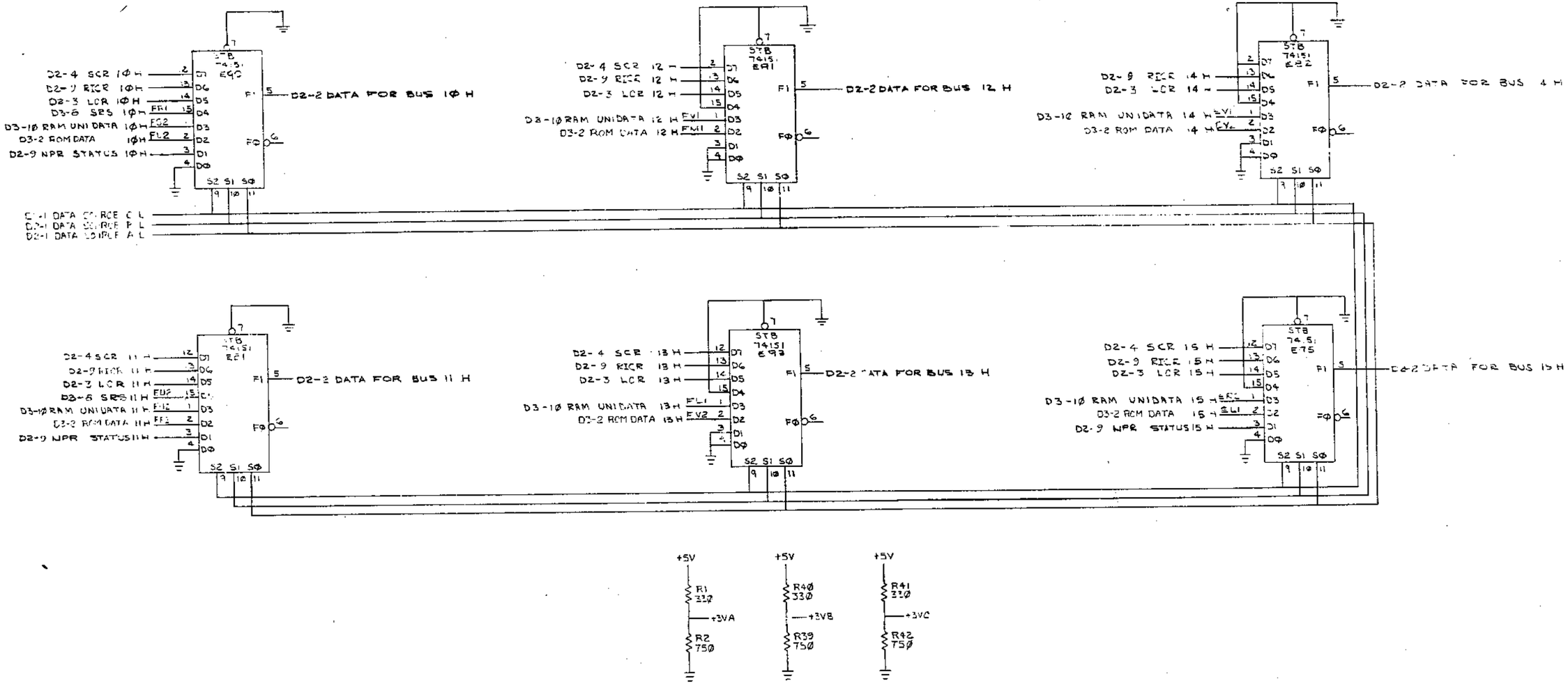


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE UNIBUS DATA & NPR CONTROL (D2-1)

SIZE D CODE CS NUMBER M7837-Ø-1 REV. C

SCALE — SHEET 3 OF 11



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE UNIBUS DATA & NPR CONTROL (D2-2)	SIZE D	CODE DCS	NUMBER M7837-Ø-1 REV. C
SCALE	SHEET 4 OF 11	DIST.	

D2-6 BUS DI5 L
D2-5 LOAD LCR H
D2-6 BUS DI4 L
D2-9A BUFFERED INIT D2 L
D2-6 BUS DI3 L
D2-6 BUS DI2 L
D2-6 BUS DI1 L
D2-6 BUS DI0 L
D2-6 BUS DI9 L
D2-6 BUS DI8 L
D3-5 9600 BAUD
D2-3 LCR 15 H
R26 4.7K +5V
DH1
C109 100PF
D2-3 CONTROL STROBE H
D2-3 LCR 14 H
D2-3 LCR 13 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR 10 H
D2-3 LCR 09 H
D2-3 LCR 08 H
D3-5 2304 KB H
BM1
D2-3 MAINTENANCE CLK PULSE H
D2-3 BUF DATA 15 H
D2-3 BUF DATA 14 H
D2-3 BUF DATA 13 H
D2-3 BUF DATA 12 H
D2-3 BUF DATA 11 H
D2-3 BUF DATA 10 H
D2-3 BUF DATA 09 H
D2-3 BUF DATA 08 H
BIT WINDOW L AV1
D2-3 LCR 07 H
D2-6 BUS DI7 L
D2-6 BUS DI6 L
D2-6 BUS DI5 L
D2-6 BUS DI4 L
D3-2 SET CLEAR 03 L
D2-6 BUS DI3 L
D3-2 ROM DATA 02 H
D3-2 ROM DATA 01 H
D3-2 ROM DATA 00 H
D2-6 BUS DI2 L
D2-6 BUS DI1 L
D2-6 BUS DI0 L
D2-5 LOAD RIRR H
D2-3 RIEE 07 H
D2-3 RIEE 06 H
D2-3 RIEE 05 H
D2-3 RIEE 04 H
D2-3 BUF DATA 04 H
D2-3 BUF DATA 05 H
D2-3 BUF DATA 06 H
D2-3 BUF DATA 07 H
D2-3 SET RECEIVER INTERRUPT L
D2-3 SET SCR 10 L
D2-3 SET RICE 14 L
D2-3 SET RICE 15 L
D2-3 CLEAR NXM L
D2-3 CLEAR SCE 03 L
D2-3 SET RICE 12 L
D2-3 SET RICE 13 L
D2-3 BUF DATA 00 H
D2-3 BUF DATA 01 H
D2-3 BUF DATA 02 H
D2-3 BUF DATA 03 H
D2-3 RIEE 03 H
D2-3 RIEE 02 H
D2-3 RIEE 01 H
D2-3 RIEE 00 H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE UNIBUS DATA AND NPR CONTROL (D2-3)		SIZE D	CODE DCS	NUMBER M7837-0-1	REV. C
SCALE	SHEET 5 OF 11	DIST.		

D2-3 BUF DATA Ø3 H
D2-3 BUF DATA Ø2 H
D2-3 BUF DATA Ø4 H
D2-3 BUF DATA ØØ H
D2-9 B BUFFERED INIT D2 L
D2-3 BUF DATA Ø1 H
D3-7 Ø1 L
D2-3 BUF DATA Ø5 H
D2-3 BUF DATA Ø6 H
D2-3 SET RECEIVER INTERRUPT L
D2-3 BUF DATA Ø7 H
D2-5 LOAD SCR LOW BYTE H
D2-4 SCR Ø3 H (CYCLE STEAL)
D2-4 SCR Ø3 L
D2-4 SCR Ø2 H (BRANCH ENABLE)
D2-4 SCR Ø4 H (MEM MGMT X A16)
D2-4 SCR ØØ H (MICROPROCESSOR INT)
D2-4 SCR Ø1 H (ROM SINGLE STEP)
D2-4 SCR Ø5 H (MEMEX A17)
D2-4 SCR Ø6 H (RECV INTR ENAB)
D2-4 SCR Ø7 H (RECV INTERRUPT)
D2-8 TEMPORARY DISABLE L
D2-3 BUF DATA Ø8 H
D2-3 SET SCR 1Ø L
D2-3 BUF DATA 1Ø H
D2-3 CLR SCR Ø8 L
D2-3 BUF DATA 15 H
D2-3 BUF DATA 11 H
D2-3 BUF DATA 14 H
D2-3 BUF DATA 13 H
D2-3 BUF DATA 12 H
D2-5 LOAD SCR HIGH BYTE H
D2-4 SCR 1Ø H (NPR STATUS OVERFLOW INTR)
D2-4 B REQUEST H
D2-4 B REQUEST L
D2-9 NPR STATUS AVAILABLE L
D2-4 SCR 15 H
D2-4 A REQUEST H
D2-4 A REQUEST L
D2-4 SCR 11 H (MASTER CLEAR)
D2-4 SCR Ø9 H (SCR15 WRITE ENABLE)
D2-4 SCR 13 H (NPR STATUS INTR EN)
D2-4 SCR 12 H (STORAGE INTR EN)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA & NPR CONTROL (D2-4)	D	DCS	M7837-Ø-1	C

SCALE — SHEET 6 OF 11 — DIST.

D8-7 INSTRUCTION DECODER ENABLE A L CJ2
D1-8 AØ3 H CU2
D1-8 AØ2 H CS1
D1-8 AØ1 H CN2
7442 E38 D3 D2 D1 D0 → f9 f8 f7 f6 f5 f4 f3 f2 f1 f0

D1-8 AØØ H AM1
D1-8 CØ H ATZ
D1-8 C1 H BH1
7404 E16
7402 E24
7432 E39
7402 E31

D2-5 LOAD LCR H (CA1)
D2-5 UNIBUS RAM WRITE L (BU2)
D2-5 LOAD SFR L (DF1)
D2-5 LOAD ERR H
D2-5 LOAD SRS HIGH BYTE H (BL1)
D2-5 LOAD SRS LOW BYTE H (BC1)
D2-5 LOAD SCR HIGH BYTE H
D2-5 LOAD SCR LOW BYTE H
D2-5 READ REGISTER H
D2-5 DATA TO BUS H
D2-T NPR DATA TO BUS L
7437 E37
D2-5 READ NPR STATUS H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA AND NPR CONTROL (D2-5)	D	CS	M7837-Ø-1	C
SCALE NONE	SHEET 7 OF 11	DIST.		

D2-3 TRANSFER BUS Ø6 H
D2-3 TRANSFER BUS Ø5 H
D2-3 TRANSFER BUS Ø4 H
D2-3 TRANSFER BUS Ø3 H
D2-3 TRANSFER BUS ØØ H
D2-3 TRANSFER BUS Ø1 H
D2-3 TRANSFER BUS Ø2 H
D2-3 TRANSFER BUS Ø7 H
D2-9 B BUFFERED INIT L
D2-6 LPB DATO REG CLK L
D2-6 NPR DATO Ø7 H
D2-6 NPR DATO Ø6 H
D2-6 NPR DATO Ø5 H
D2-6 NPR DATO Ø4 H
D2-6 NPR DATO Ø3 H
D2-6 NPR DATO Ø2 H
D2-6 NPR DATO Ø1 H
D2-6 NPR DATO ØØ H
D2-2 DATA FOR BUS 15 H
D2-2 DATA FOR BUS 14 H
D2-2 DATA FOR BUS 13 H
D2-2 DATA FOR BUS 12 H
D2-2 DATA FOR BUS 11 H
D2-2 DATA FOR BUS 10 H
D2-2 DATA FOR BUS Ø9 H
D2-2 DATA FOR BUS Ø8 H
D2-1 DATA FOR BUS Ø7 H
D2-1 DATA FOR BUS Ø6 H
D2-1 DATA FOR BUS Ø5 H
D2-1 DATA FOR BUS Ø4 H
D2-1 DATA FOR BUS Ø3 H
D2-1 DATA FOR BUS Ø2 H
D2-1 DATA FOR BUS Ø1 H
D2-1 DATA FOR BUS ØØ H
D2-5 READ REGISTER H
D1-8 NPR ADDR ØØ H CC1
D2-7 NPR DATA TO BUS L
D2-8 VECTOR TO BUS
D2-3 DATA TO BUS H
D2-6 BUS DI5 L
D2-6 BUS DI4 L
D2-6 BUS DI3 L
D2-6 BUS DI2 L
D2-6 BUS DI1 L
D2-6 BUS DIØ L
D2-6 BUS DØ9 L
D2-6 BUS DØ8 L
D2-6 BUS DØ7 L
D2-6 BUS DØ6 L
D2-6 BUS DØ5 L
D2-6 BUS DØ4 L
D2-6 BUS DØ3 L
D2-6 BUS DØ2 L
D2-6 BUS DØ1 L
D2-6 BUS DØØ L
D2-8 VECTOR BIT Ø2 H
D2-6 BUS INTR L
+5V R28 1K
+5V R29 1K
+5V R30 1K
+5V R31 1K
+5V R32 1K
+5V R33 1K
S1

REVISIONS		
CHK	CHANGE NO.	DEV.

TITLE UNIBUS ADAPTER NPR CONTROL (D2-6)
SIZE D | CODE DS | NUMBER M7837-Ø-1 | REV. C
SCALE — | SHEET 8 OF 11 | DIST.

D2 T NO BBSY NO SSYN H

D3-T BUS SSYN L

D2-T SSYN H

D2-2 NPR OPERATION L

D3-7 Ø2 L

D2-7 REQUEST IN H

AS2 D2-7 BUS NPR L

D2-7 NPR DATA TO BUS L

BD1 D2-7 BUS NPG OUT H

D1-8 C1 H

BUS NPG IN H

AR2 D2-7/D2-8 BUS SACK L

AP2 D2-7/D2-8 BUS BBSY L

EH1 D2-7 ADDRESS TO BUS L

D2-9 E BUFFERED INIT D2 L

D2-3 CLEAR NXM L

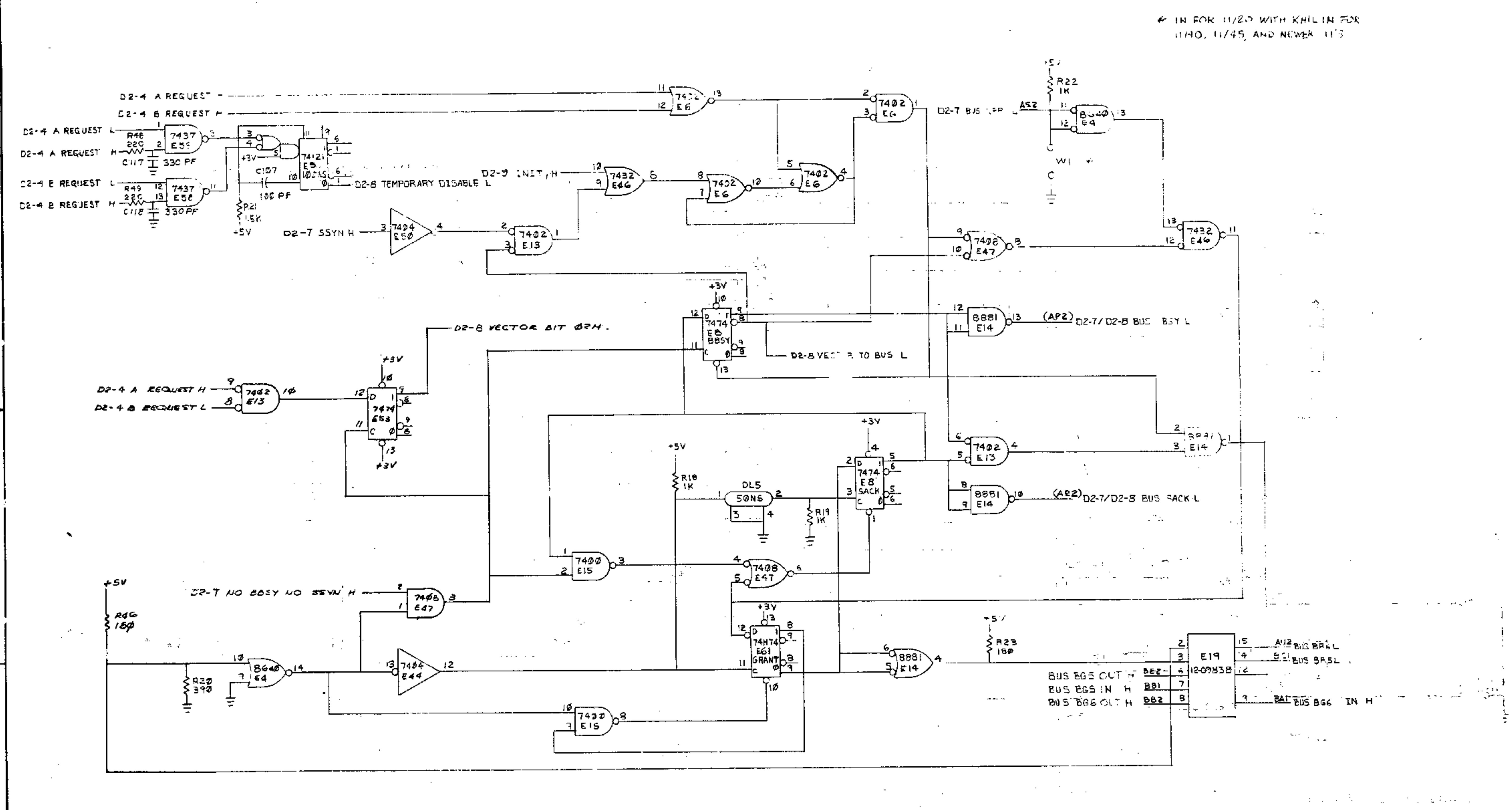
BF1 D2-7 DATA STROBE H

EK1 D2-7 NXM H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA & NPR CONTROL (D2-7)	D	CS	M7837-Ø-1	

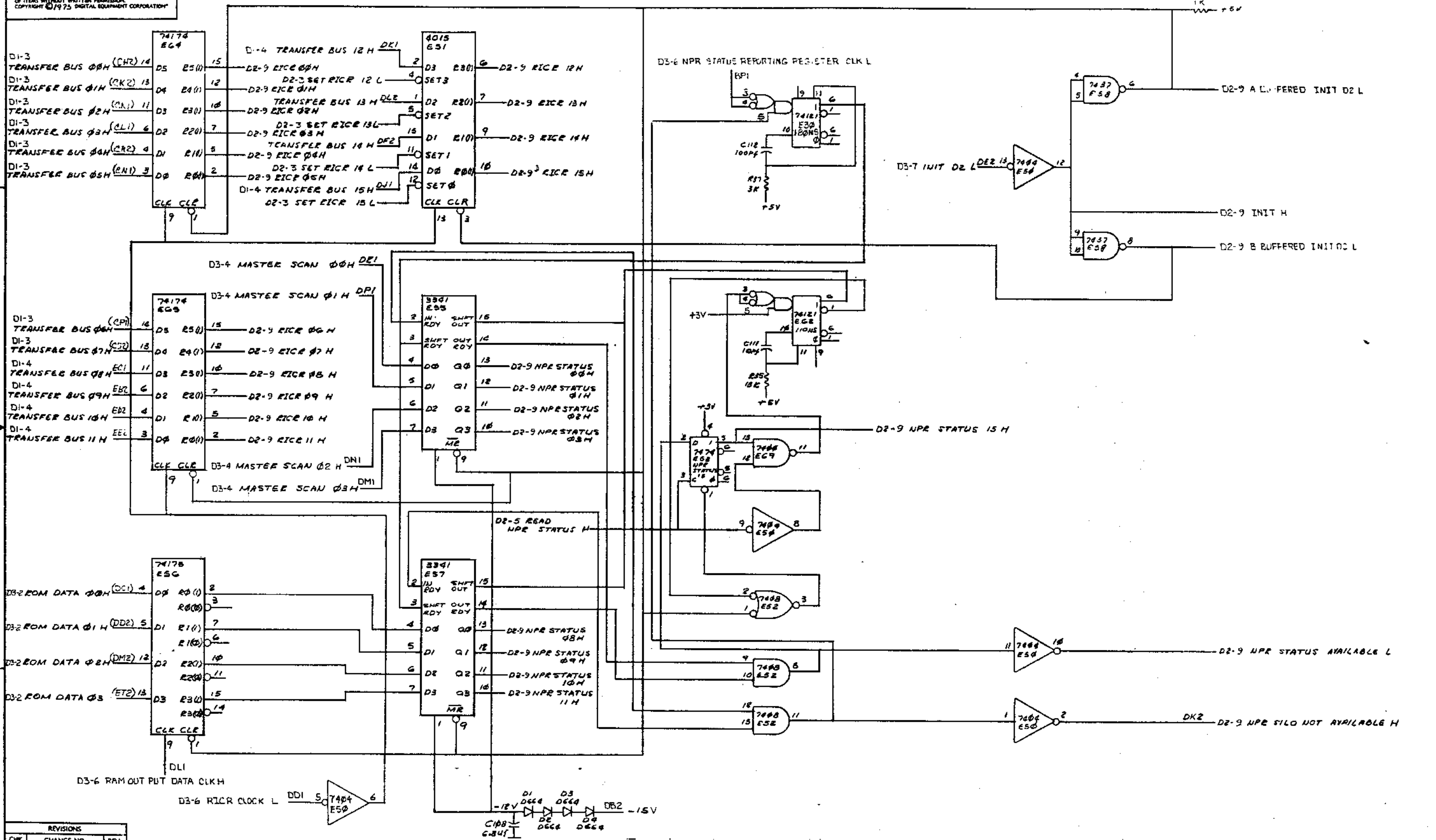
SCALE — SHEET 9 OF 11 — DIST.



TITLE	SIZE	CODE	NUMBER	REV.
UNIBUS DATA & NPR CONTROL (D2-8)	D	CS	M7837-Ø-1	C

SCALE NONE SHEET 10 OF 11

REVISIONS — CHK | CHANGE NO. | REV.



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: UNIBUS DATA AND NPR CONTROL (D2-9)

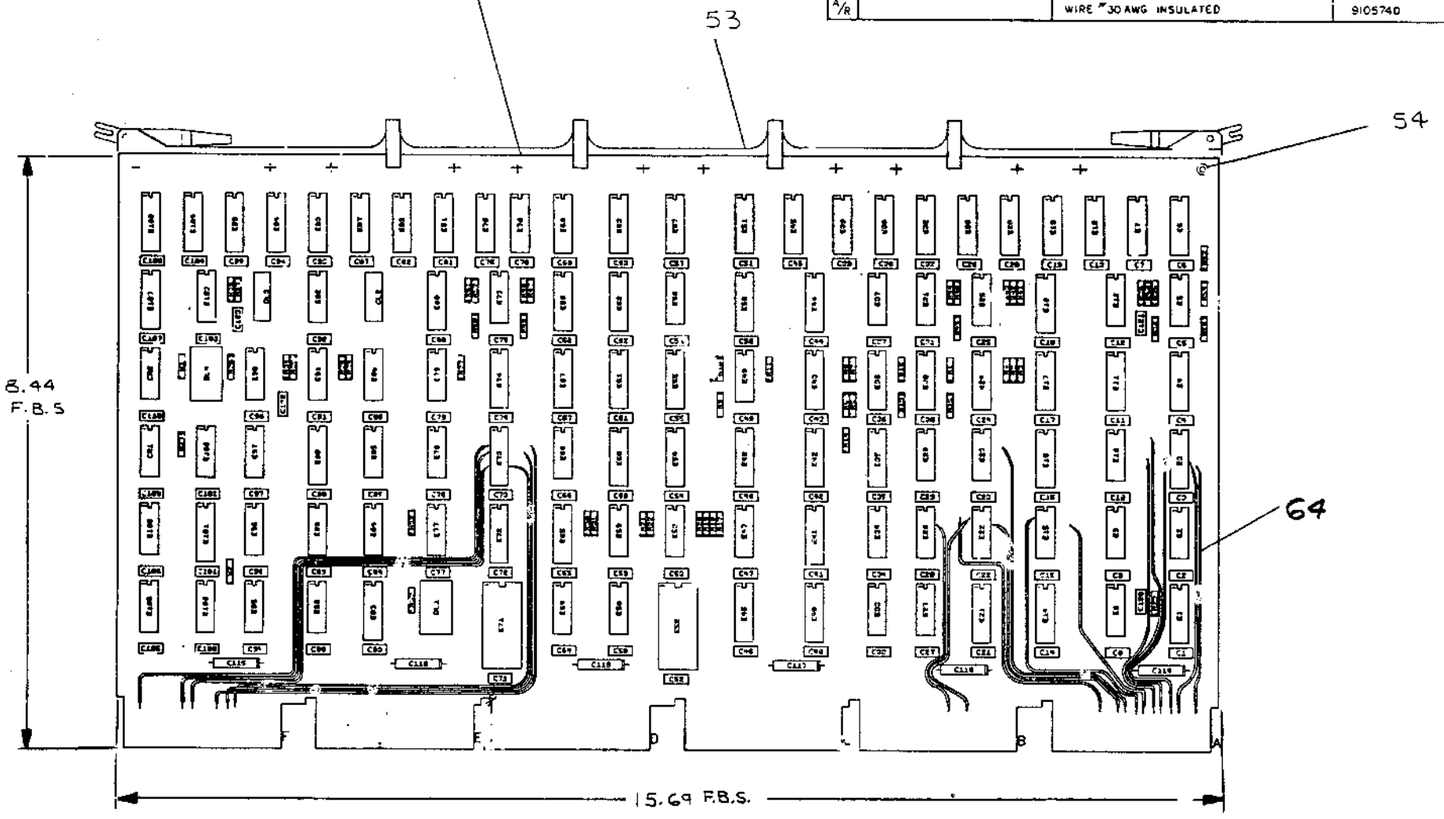
SIZE: D — CODE: CS — NUMBER: M7837-0-1 — REV.: C

SCALE: — SHEET 11 OF 11 — DIST.

D CS M7837-0-1 C

NOTES:
1 LOCATION E44 E16 ARE SPARES

QTY	REF		PART NO	ITEM NO
1	E90	I.C. DEC 74S175	1910957	52
1		HANDLE ASSY.	1210711-2	53
12		EYELET, HANDLE	9006702	54
1	E4	PROM	23188A2	55
1	E11	PROM	23186A2	56
1	E17	PROM	23187A2	57
1	E24	PROM	23188A2	58
1	E30	PROM	23189A2	59
1	E36	PROM	23190A2	60
1	E43	PROM	23191A2	61
1	E55	PROM	23192A2	62
2	W1, W2	JUMPER, INSULATED	9009185	63
A/R		WIRE #30 AWG INSULATED	9105740	64



QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO
REF		X & Y COORDINATE HOLE LOCATION	K CO-M7838-0-4	1
REF		ASSY DRILLING HOLE LAYOUT	D-AH-M7838-0-5	2
REF		MODULE ECO HISTORY	B-MH-M7838-0-5	3
1		ETCHED CIRCUIT BOARD	5010978	4
1	C121	CAP 10PF 100V 5% CER	1000806	5
2	C120,C123	CAP 100PF 100V 5% DM	1000815	6
1	C122	CAP 1000PF 100V 5%	1000842	7
110	C1-C118	CAP .01UF 100V 20%	1001610-01	8
6	C114-C119	CAP 6.8UF 35V 10% TANT	1005306	9
3	R24,29,30	RES. 330 OHM, 1/4W 5%	1300295	10
2	R25,28	RES. 470 OHM, 1/4W 5%	1300316	11
39	R1-16,27,32,35,36,37 38-55	RES. 1K, 1/4W, 5%	1300365	12
1	R34	RES. 3.3K, 1/4W, 5%	1300439	13
1	R23	RES. 4.7K, 1/4W, 5%	1300447	14
3	R18,20,22	RES. 390 OHM, 1/4W, 5%	1300309	15
1	R26	RES. 15K, 1/4W, 5%	1300496	16
3	R17,19,21	RES. 180 OHM, 1/4W, 5%	1301322	17
1	R31	RES. 750 OHM, 1/4W, 5%	1301401	18
1	R35	RES. 5.6K, 1/4W, 5%	1301874	19
2	DL2,DL3	DELAY LINE 30NS	1605528	20
2	DL1,DL4	DELAY LINE 100NS	1609559	21
1	CR1	20MHZ OSCILLATOR 14 PIN DIP	1811660-00	22
1	CR2	5.068 MHZ OSCILLATOR 14 PIN DIP	1811660-02	23
5	E58,15,22,23,26	I.C. DEC 7474	1905547	24
2	E47,78	I.C. DEC 7400	1905575	25
1	E2	I.C. DEC 7420	1905577	26
2	E97,102	I.C. DEC 7430	1905578	27
4	E31,37,49,56	I.C. DEC 7401	1905590	28
2	E85,91	I.C. DEC 7402	1909004	29
1	E105	I.C. DEC 7492	1909053	30
2	E100,106	I.C. DEC 7493	1909054	31
2	E59,96	I.C. DEC 74H00	1909056	32
1	E95	I.C. DEC 74H11	1909267	33
2	E33,53	I.C. DEC 8640	1911469	34
3	E84,88,89	I.C. DEC 74S74	1910544	35
5	E5,25,54,77,75	I.C. DEC 7404	1909888	36
1	E21	I.C. DEC 7442	1910046	37
1	E27	I.C. DEC 8881	1909705	38
3	E9,10,86	I.C. DEC 8815	1909713	39
5	E81,65,67,72,74	I.C. DEC 74193	1910018	40
1	E66	I.C. DEC 7437	1910091	41
2	E52,71	I.C. DEC 74150	1910153	42
3	E92,29,34	I.C. DEC 7408	1910155	43
4	E8,12,98,103	I.C. DEC 74121	1910230	44
1	E101	I.C. DEC 74181	1910850	45
10	E3,14,42,44,46,48 50,54, 60,82	I.C. DEC 74175	1910851	46
1	E73	I.C. DEC 74174	1910852	47
9	E18,45,51,57,63,68 69,80, 107	I.C. DEC 74157	1910855	48
4	E35,40,41,83	I.C. DEC 74155	1910856	49
19	E6,7,13,19,20,26,32,38, E39,70,76,81,82,87,93,94, E99,104,108	I.C. DEC 9106	1910816-02	50
1	E79	I.C. DEC 74H10	1909057	51

PARTS LIST

8640	1	8
7493	10	4
7492	10	5
IC TYPE	GND	+ 5.

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

AA2, BA2, CA2, DA2, EA2, FA2 — +5V

AC2, AT1, BC2, BT1, CC2, CT1, DC2, DT1, EC2, ET1, FC2, FT1 — GND

C114 6.8UF, C115 6.8UF, C116 6.8UF, C117 6.8UF, C118 6.8UF, C119 6.8UF, C1 THRU C110 .01UF, C110 .01UF

FIRST USED ON OPTION MODEL: DV11-AA

ETCH BOARD REV: B

REV	CHANGE NO	CHK	DATE
A	UNCONTROLLED	J. McNAMARA	7-23-75
B	M7838-00001	W. Brunnell	7-23-75

DEC NO	EIA NO	DEC NO	EIA NO

SEMICONDUCTOR CONVERSION CHART

DRN. K. Davis DATE 1-6-75
CHK. DATE 1-16-75
ENG. DATE 3-7-75
PROJ. LDR. DATE 7-15-75
PROD. DATE 7-21-75

NEXT HIGHER ASSY: B-DD-DV11-0
SCALE: NONE
SHEET 1 OF 12

digital EQUIPMENT CORPORATION

TITLE: ROM, RAM AND BRANCH

SIZE D | CODE | NUMBER: DCSM7838-0-1 | REV: B

DIST.

DCSM7838-0-1 B

D2-3 BUF DATA Ø0 H — 74Ø1 E37 — R16 1K
D2-3 BUF DATA Ø1 H — 74Ø1 E37 — R15 1K
D2-3 BUF DATA Ø2 H — 74Ø1 E37 — R14 1K
D2-3 BUF DATA Ø3 H — 74Ø1 E37 — R13 1K
D2-3 BUF DATA Ø4 H — 74Ø1 E31 — R4 1K
D2-3 BUF DATA Ø5 H — 74Ø1 E31 — R3 1K
D2-3 BUF DATA Ø6 H — 74Ø1 E31 — R2 1K
D2-3 BUF DATA Ø7 H — 74Ø1 E31 — R1 1K
D2-3 BUF DATA Ø8 H — 74Ø1 E56 — R8 1K
D2-3 BUF DATA Ø9 H — 74Ø1 E56 — R7 1K
D2-3 BUF DATA 10 H — 74Ø1 E56 — R6 1K
D2-3 BUF DATA 11 H — 74Ø1 E56 — R5 1K
D2-3 BUF DATA 12 H — 74Ø1 E49 — R12 1K
D2-3 BUF DATA 13 H — 74Ø1 E49 — R11 1K
D2-3 BUF DATA 14 H — 74Ø1 E49 — R10 1K
D2-3 BUF DATA 15 H — 74Ø1 E49 — R9 1K
+5V

D2-4 SCR Ø3 L — 7437 E46
D3-2 ROM DATA 15 H — 74193 E74
D3-2 ROM DATA Ø7 H
D3-2 ROM DATA Ø6 H
D3-2 ROM DATA Ø5 H
D3-2 ROM DATA Ø4 H — 74193 E61
D3-2 ROM DATA Ø3 H
D3-2 ROM DATA Ø2 H
D3-2 ROM DATA Ø1 H
D3-2 ROM DATA ØØ H — 74193 E67
D3-7 INIT D3 L — 7404 E77
D3-7 Ø1 H
4.3 V
D3-2 BRANCH POINT TRUE H
D3-7 Ø2 H — 74H00 E59

23-190 A2 MEI E36
23-189 A2 MEI E30
23-191 A2 MEI E43
23-192 A2 MEI E55
23-187 A2 MEI E17
23-188 A2 MEI E24
23-186 A2 MEI E11
23-185 A2 MEI E4

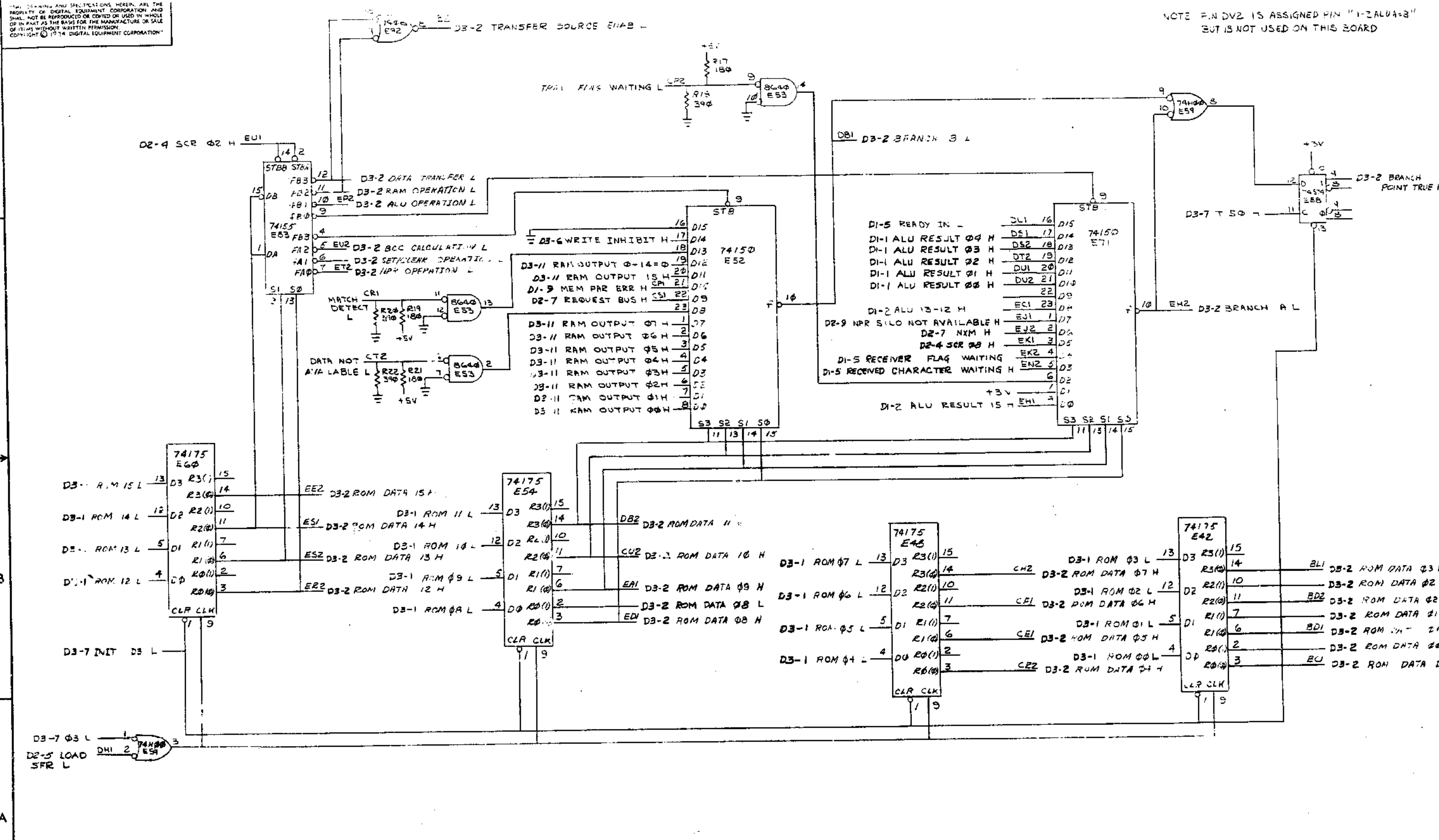
D3-1 ROM Ø3 L
D3-1 ROM Ø2 L
D3-1 ROM Ø1 L
D3-1 ROM ØØ L
D3-1 ROM Ø7 L
D3-1 ROM Ø6 L
D3-1 ROM Ø5 L
D3-1 ROM Ø4 L
D3-1 ROM 11 L
D3-1 ROM 10 L
D3-1 ROM Ø9 L
D3-1 ROM Ø8 L
D3-1 ROM 15 L
D3-1 ROM 14 L
D3-1 ROM 13 L
D3- ROM 12 L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-1)	D	CS	M7838-Ø-1	B
SCALE —	SHEET 2 OF 12	DIST.		

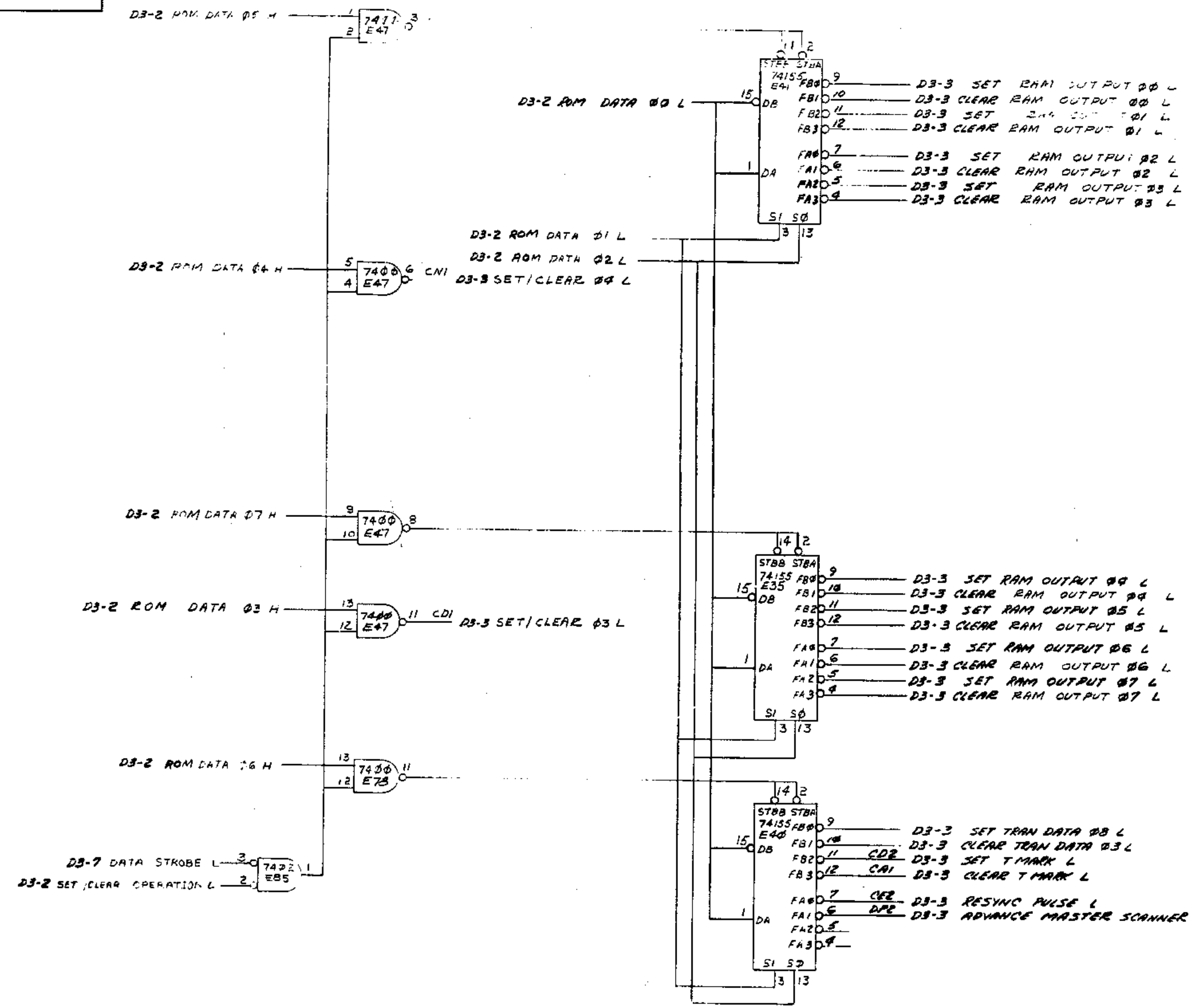
DEC M7838-Ø-1

NOTE: PIN DV2 IS ASSIGNED PIN "1-2ALUA=B" BUT IS NOT USED ON THIS BOARD



TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-2)	D	CS	M7838-Ø-1	B

SCALE — SHEET 3 OF 12



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ROM, RAM & BRANCH (D3-3)

SIZE	CODE	NUMBER	REV.
D	CS	M7838-Ø-1	B

SCALE — SHEET 4 OF 12

D3-3 TRANSFER BUS Ø0 H — CJ2 13 — 74175 E46 D3 R3 15 CM1 — D3-Ø TRAN DATA Ø0 H
D3-3 TRANSFER BUS Ø1 H — CK2 12 — D2 R2 10 CJ1 — D3-Ø TRAN DATA Ø1 H
D3-3 TRANSFER BUS Ø2 H — CM2 5 — D1 R1 7 CL2 — D3-Ø TRAN DATA Ø2 H
D3-3 TRANSFER BUS Ø3 H — CM1 4 — D0 R0 2 CN2 — D3-Ø TRAN DATA Ø3 H
CLR CLK — 1 — 9
D3-7 INIT D3 L
D3-6 TRANSMITTED DATA BUS CLOCK L — 74Ø4 E64 — 1 — 2

D3-3 TRANSFER BUS Ø4 H — AN2 13 — 74175 E4 D3 R3 15 AT2 — D3-Ø TRAN DATA Ø4 H
D3-3 TRANSFER BUS Ø5 H — AR1 12 — D2 R2 10 AS1 — D3-Ø TRAN DATA Ø5 H
D3-3 TRANSFER BUS Ø6 H — AU2 5 — D1 R1 7 AN2 — D3-Ø TRAN DATA Ø6 H
D3-3 TRANSFER BUS Ø7 H — AW1 4 — D0 R0 2 AS2 — D3-Ø TRAN DATA Ø7 H
CLR CLK — 1 — 9

D3-3 SET TRAN DATA Ø8 L — 7474 E58 — DF2 — D3-Ø TRAN DATA Ø8 H
D3-5 INIT H
D3-3 CLEAR TRAN DATA Ø8 L

+3V — 3 — 74121 E5 330Ω — 11 — 6 — AM2 — D3-Ø TRANSMITTER STROBE H
10 — C.2Ø 10VDC
223 4.7K
+5V

74Ø4 E64 — 5 — 6 — DP1 — D3-Ø MASTER SCAN C H

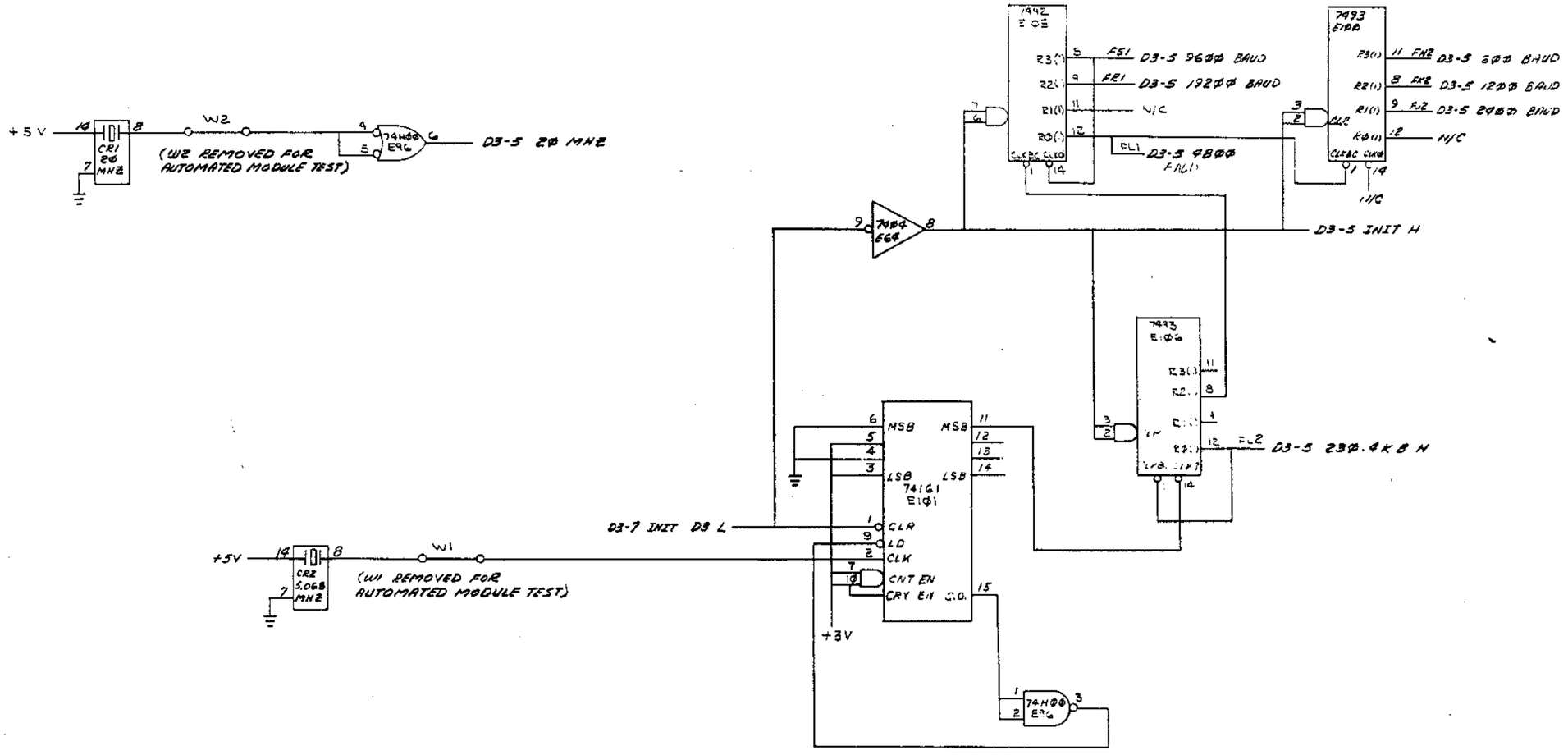
74193 E72 — CRY BRW — D3 D2 D1 D0 — 9 10 1 15 — RP3 RP2 RP1 RP0 — 7 6 2 3 — NC NC NC — DN1 — D3-Ø MASTER SCAN Ø3 H
CLR LD UP CDN — 14 11 5 4 — +3V
74Ø2 E64 — 3 — DN2 — D3-Ø MASTER SCAN D H

D3-5 INIT H

74193 E65 — CRY BRW — D3 D2 D1 D0 — 9 10 1 15 — RP3 RP2 RP1 RP0 — 7 6 2 3 — DM2 DL2 DK2 DJ2 — D3-Ø MASTER SCAN Ø2 H, Ø1 H, Ø0 H, /2
CLR LD UP CDN — 14 11 5 4 — +3V
D3-3 ADVANCE MASTER SCANNER L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ROM, RAM & BRANCH (D3-4)
SIZE: D | CODE: CS | NUMBER: M7836-Ø-1 | REV: B
SCALE | SHEET 5 OF 12 | DIST.



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-5)	D	CS	M7838-0-1	B
SCALE	SHEET 6 OF 12	DIST.		

DCSM,33--0-1

D3-6 WRITE INHIBIT H
D3-5 INIT H
D3-6 RAM OUTPUT DATA CLOCK L
D3-6 RAM OUTPUT DATA CLOCK H
D3-6 RAM WRITE ENABLE B L
D3-6 RAM WRITE ENABLE A L
D2-5 UNIBUS RAM WRITE L
D3-8 RAM ADD Φ1 H
D3-8 RAM ADD Φ0 H
D3-8 RAM ADD Φ2 H
D3-8 RAM ADD Φ7 H
D3-8 RAM ADD Φ3 H
D3-8 RAM ADD Φ4 H
D3-8 RAM ADD Φ5 H
D3-8 RAM ADD Φ6 H
D3-2 RAM DATA Φ8 L
D3-7 T5Φ L
D3-2 RAM OPERATION L
D3-7 Q2 L
D3-2 ROM DATA Φ8 H
D3-7 INSTRUCTION DECODER ENABLE B L
D3-2 DATA TRANSFER L
D3-2 ROM DATA Φ2 H
D3-2 ROM DATA Φ1 H
D3-2 ROM DATA Φ0 H
D3-6 NPR STATUS REPORTING REGISTER CLOCK L
D3-6 RICR CLOCK L
D3-6 NPR DATA REGISTER CLOCK L
D3-6 RAR Ø-3 CLOCK L
D3-6 NPR ADDRESS REGISTER CLOCK L
D3-6 B REGISTER CLOCK L
D3-6 A REGISTER CLOCK L
D3-6 TRANSMITTED DATA BUS CLOCK L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ROM, RAM & BRANCH (D3-6)	SIZE: D	CODE:	NUMBER: M7638-D-1	REV: B
SCALE:	SHEET 7 OF 12	DIST.		

D2-4 SCR 11 H
BVI D3-7 BUS MSYN L
D2-6 ACCEPT MSYN L
D1-8 A17 H
D1-8 ADDRESS SELECTED H
D2-5 LOAD LCR H
BUS INIT L
D3-7 INSTRUCTION DECODER ENABLE B L
D3-7 INSTRUCTION DECODER ENABLE A L
D3-7 BUS SSYN L
D3-7 INIT D1 L
D3-7 INIT D2 L
D3-7 INIT D3 L
D3-7 BUF INIT L
SCR Ø1 H
SCR ØØ H
D3-5 2Ø MHZ
D3-7 Ø1 N
D3-7 DATA STROBE L
D3-7 Ø2 N
D3-7 Ø2 L
D3-7 T5Ø N
D3-7 T5Ø L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
RCM, RAM & BRANCH (D3-7)	D	CS	M7838-Ø-1	B
SCALE	SHEET 8 OF 12		DIST.	

D3-7 INSTRUCTION DECODER ENABLE B L

D3-7 INSTRUCTION DECODER ENABLE A L

D3-6 RAM B-S CLOCK L

D2-5 LOAD SRS LOW BYTE H

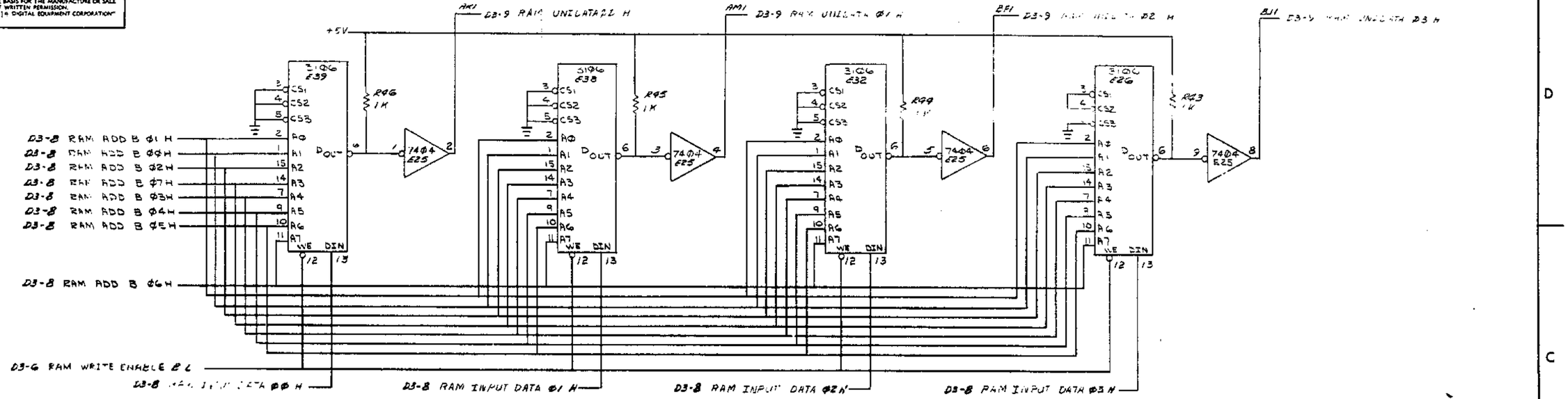
D2-5 LOAD SRS HIGH BYTE H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: ROM, RAM & BRANCH (D3-8)

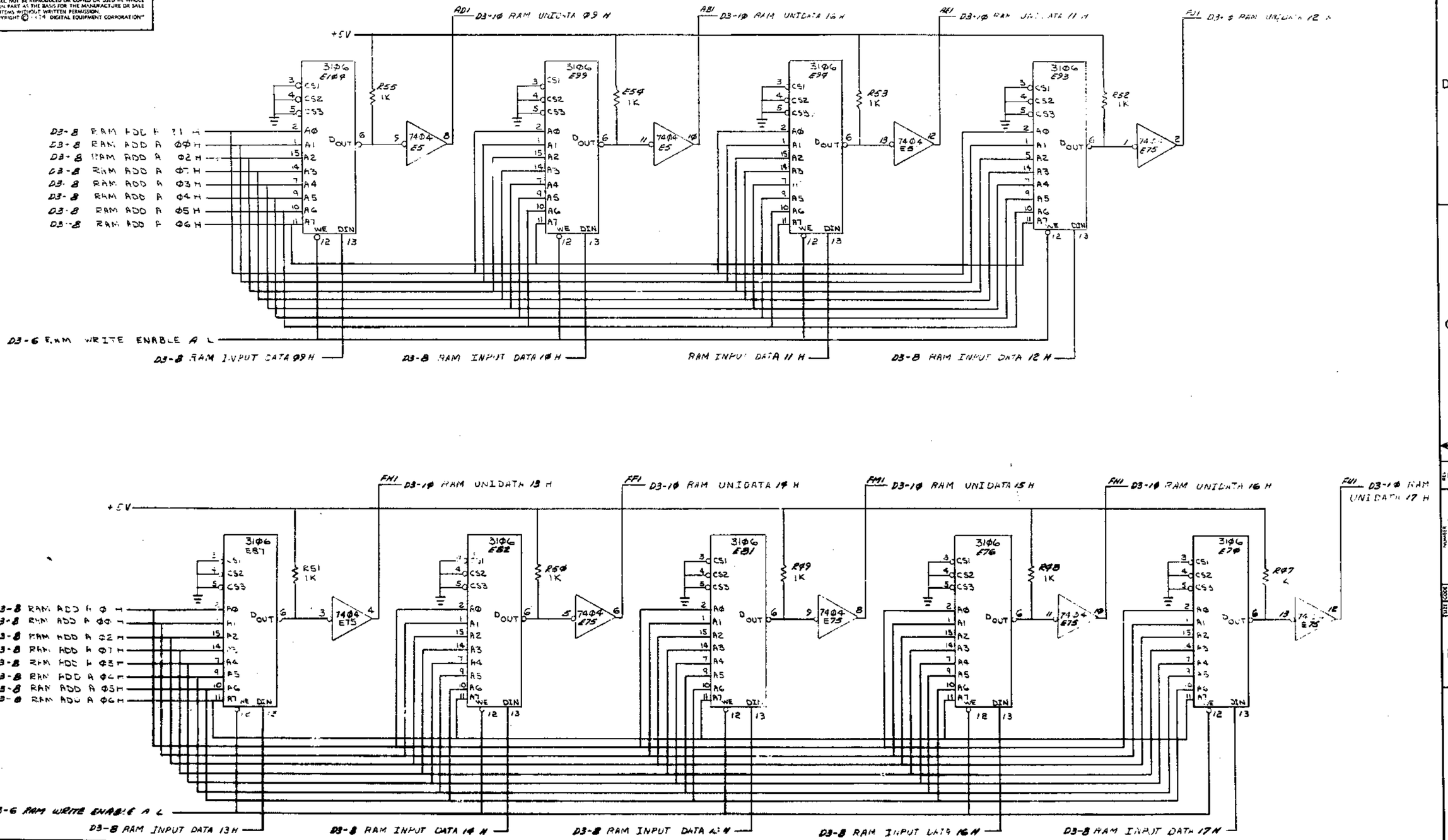
SIZE D | CS | NUMBER M7838-0-1 | REV B

SCALE | SHEET 9 OF 12



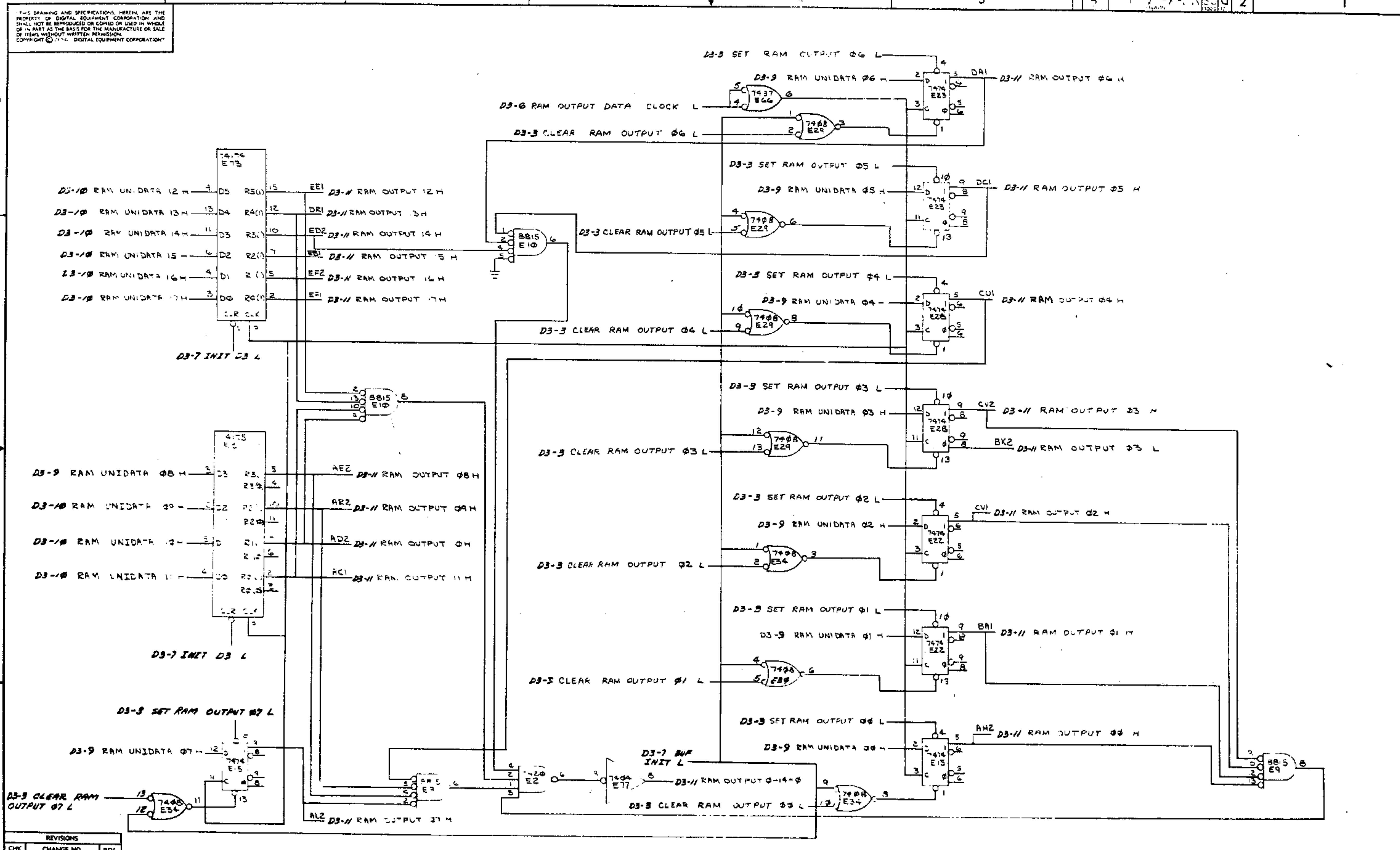
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-9)	D	CS	M7838-Ø-1	B
SCALE	SHEET 10 OF 12	DIST.		



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
ROM, RAM & BRANCH (D3-1Ø)	D	CS	M7838-Ø-1	B
SCALE	SHEET 11 OF 12		DIST.	



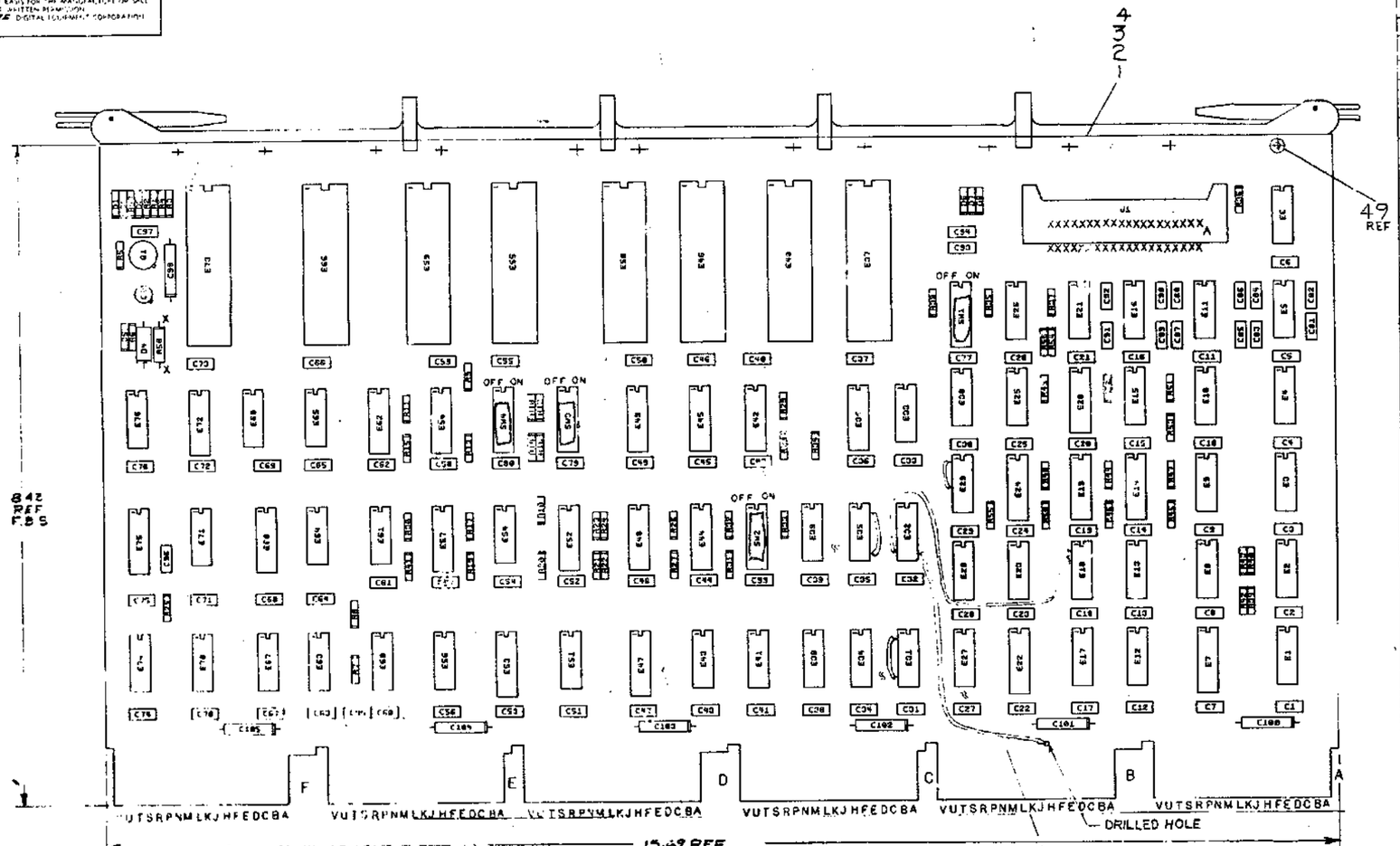
REVISIONS		
CHK	CHANGE NO.	REV.

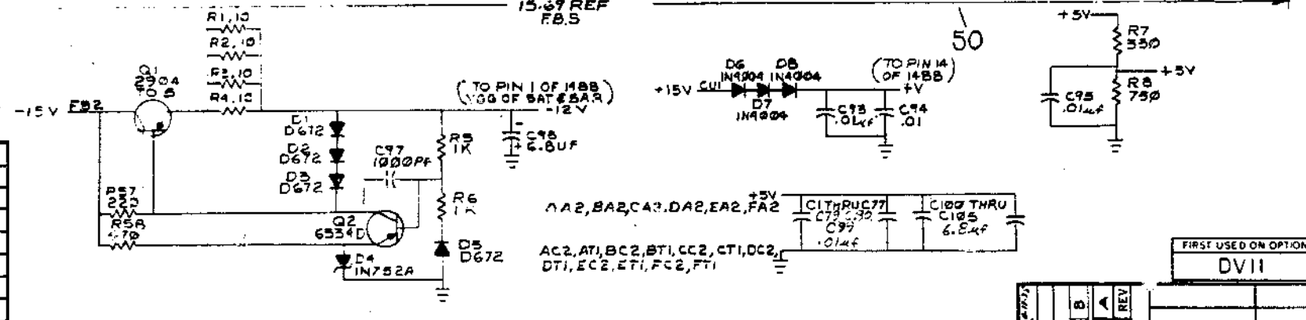
TITLE: ROM, RAM & BRANCH (D3-11)

SIZE	CODE	NUMBER	REV.
D	CS	M7838-Ø-1	B

SCALE: — SHEET 12 OF 12

NOTES:





REF					
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M7839-0-4	1
REF		ASSY-HOLE DRILLING LAYOUT	D-AH-M7839-0-5	2
REF		MODULE ECO HISTORY	B-MH-M7839-0-6	3
1		ETCHED CIRCUIT BOARD	5010983	4
1	C96	CAP 68 PF, 100V,5%	1000014	5
12	C81-92	CAP 470 PF, 100V, 5%	1000024	6
1	C97	CAP 1000PF, 100V, 5%	1000042	7
83	C93,94,95,C1-77,99,79,80	CAP .01 UF, 100V DISC	1001610-01	8
7	C98,100-C105	CAP 6.8 UF, 35V, 10%	1005306	9
1	D4	DIODE IN752A	1102808	10
4	D1,2,3,5	DIODE D672	1105275	11
3	D6,7,8	DIODE IN4004	1105796	12
1	J1	CONN, 40 PIN	1209941	13
4	SW1,SW2,SW3,SW4	DIPSWITCH 8-POS	1211164-04	14
4		DIPSWITCH COVER 8-POS	1211284-04	15
1	R57	RES. 220,1/4W, 5%	1300271	16
1	R7	RES. 330, 1/4W, 5%	1300295	17
1	R58	RES. 470, 1/2W, 5%	1300315	18
11	R5,6,30,38-44,26,27	RES. 1K, 1/4W, 5%	1300365	19
35	R8-THRU 25,28,29,31 THRU 34,45 THRU 56	RES. 10K,1/4W, 5%	1300479	20
4	R1 THRU R4	RES. 10, 1/4W, 5%	1301317	21
1	R8	RES. 750, 1/4W, 5%	1301401	22
4	R35 THRU 38	RES. 7.5K, 1/4W, 5%	1301422	23
1	Q1	TRANSISTOR 2904	1501742	24
1	Q2	TRANSISTOR 6534D	1503409	25
4	E21,33,17,23	DEC I.C. 7400	1905575	26
3	E64,8,9	DEC I.C. 7450	1905580	27
3	E1,12,3	DEC I.C. 7402	1909004	28
3	E39,25,34	DEC I.C. 74H11	1909267	29
10	E68,65,43,32,28,51,58,60,27,38	DEC I.C. 7474	1905547	30
3	E41,54,10	DEC I.C. 7404	1909686	31
4	E70,71,74,67	DEC I.C. 8881	1909705	32
1	E2	DEC I.C. 8242	1909712	33
3	E61,78,30	DEC I.C. 7417	1909929	34
2	E52,58	DEC I.C. 74157	1910655	35
9	E66,E36,44,46,42,62,45,49,22,	DEC I.C. 74153	1909937	36
1	E63	DEC I.C. 7437	1910081	37
5	E18,35,29,31,13	DEC I.C. 7408	1910155	38
2	E26,6	DEC I.C. 1488	1910322	39
3	E5,16,11	DEC I.C. 1489	1910323	40
5	E14,19,20,24,75	DEC I.C. 74123	1910436	41
1	E7	DEC I.C. 74175	1910651	42
4	E47,57,53,72	DEC I.C. 74155	1910656	43
2	E15,4	DEC I.C. 7432	1911521	44
4	E50,37,48,40	DEC I.C. PR1472B SAR	2111558	45
4	E88,73,59,55	DEC I.C. PT1482B SAT	2111557	46
1		TRAN COVER	9008351-0	47
1		HANDLE ASSY	1210711-2	48
12		EYELET	8006732	49
A/R		WIRE #30 AWG GREEN	9105740-55	50
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DEC 74157	8	16			
DEC 74123	8	16			
DEC 74155	8	16			
DEC 74153	8	16			
DEC 74175	8	16			
PR1472B SAR	20	1	—	16	
PT1482B SAT	21	1	—	16	
DEC 1488	7	—	14	1	
IC TYPE	GND	+5V	+V	-12	

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

DEC NO	EIA NO
D672	1N3653
6534D	NONE
2904	2N1132

SEMICONDUCTOR CONVERSION CHART

FIRST USED ON OPTION MODEL: DVII

ETCH BOARD REV: B

REV	CHANGE NO	ORIGINATED	CHK
A		J MCNAMARA 6-2-74	
B	M7839-00001		

DRN — DATE 11/15/74
CHK'D — DATE 5/6/75
ENG — DATE 7/11/75
PROJ ENG — DATE 3/14/75
PROD — DATE 3/14/75

NEXT HIGHER ASSY: B-DD-DVII-0-0

SCALE: NONE

SHEET 1 OF 9

digital EQUIPMENT CORPORATION

TITLE: SYNC MUX LINE CARD

SIZE/CODE: D | NUMBER: CS M7839-0-1 | REV: B

DIST.

DCS M7839-0-1 B

BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR Ø0
C	GROUND
D	DCE SCR Ø1
E	GROUND
F	DCE SCR Ø2
H	GROUND
J	DCE SCR Ø3
K	GROUND
L	EIA RCV DATA Ø0
M	GROUND
N	EIA RCV DATA Ø1
P	GROUND
R	EIA XMIT DATA Ø0
S	GROUND
T	EIA XMIT DATA Ø1
U	GROUND
V	DTE SCTE Ø0
W	GROUND
X	DTE SCTE Ø1
Y	DTE SCTE Ø2
Z	GROUND
A A	DTE SCTE Ø3
B B	GROUND
C C	EIA XMIT DATA Ø2
D D	GROUND
E E	EIA XMIT DATA Ø3
F F	GROUND
H H	EIA RCV DATA Ø2
J J	GROUND
K K	EIA RCV DATA Ø3
L L	GROUND
M M	DCE SCT Ø3
N N	GROUND
P P	DCE SCT Ø2
R R	GROUND
S S	DCE SCT Ø1
T T	GROUND
U U	DCE SCT Ø0
V V	GROUND

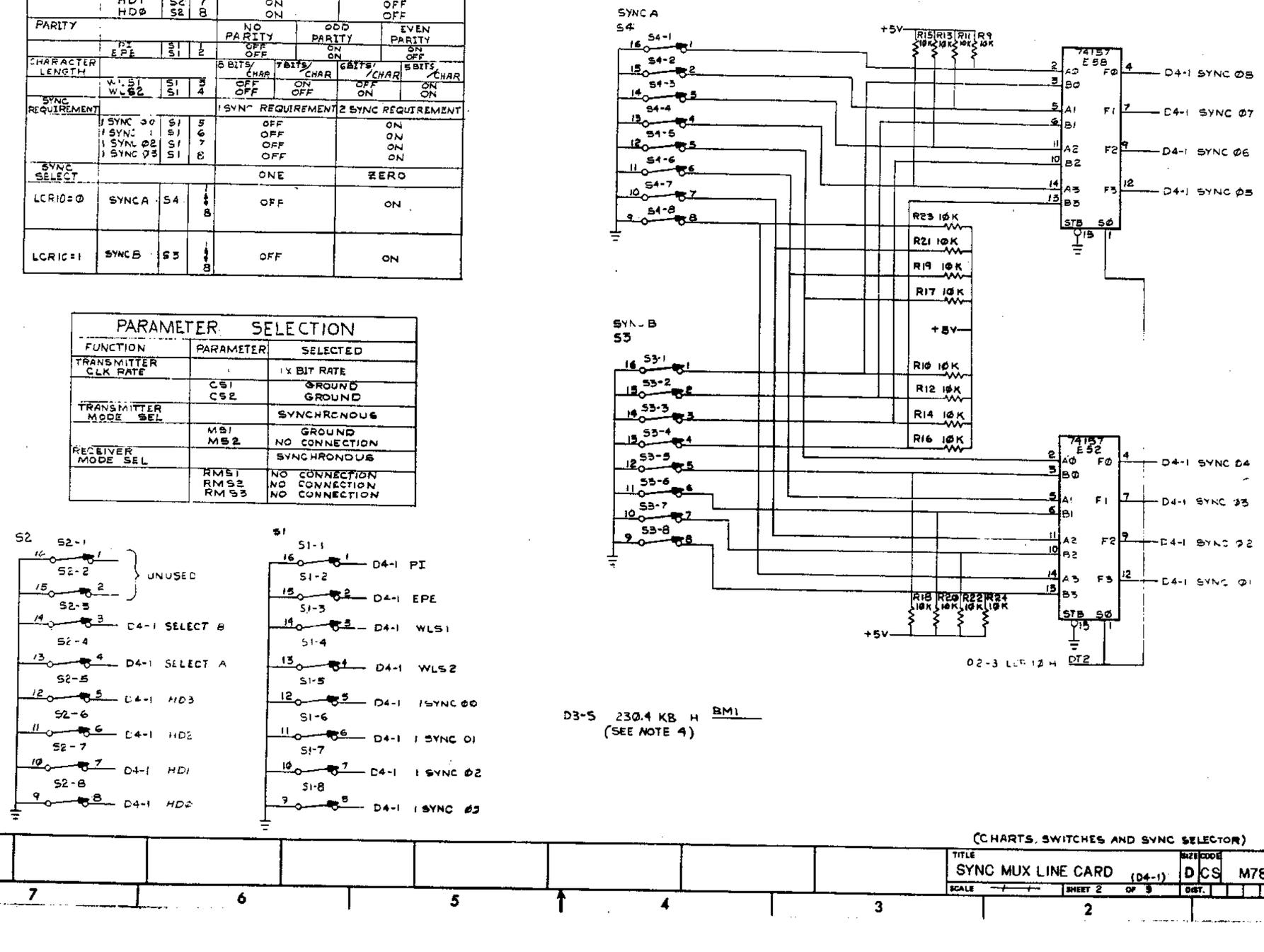
PARAMETER SWITCH SETTINGS

FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HD3	S2	5	ON		OFF	
	HD2	S2	6	ON		OFF	
	HD1	S2	7	ON		OFF	
	HDØ	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC ØØ	S1	5	OFF		ON	
	1 SYNC Ø1	S1	6	OFF		ON	
	1 SYNC Ø2	S1	7	OFF		ON	
	1 SYNC Ø3	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1↕8	OFF		ON	
LCR10=1	SYNC B	S3	1↕8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1	GROUND
	CS2	GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1	GROUND
	MS2	NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1	NO CONNECTION
	RMS2	NO CONNECTION
	RMS3	NO CONNECTION

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA AT H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN 3M1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.

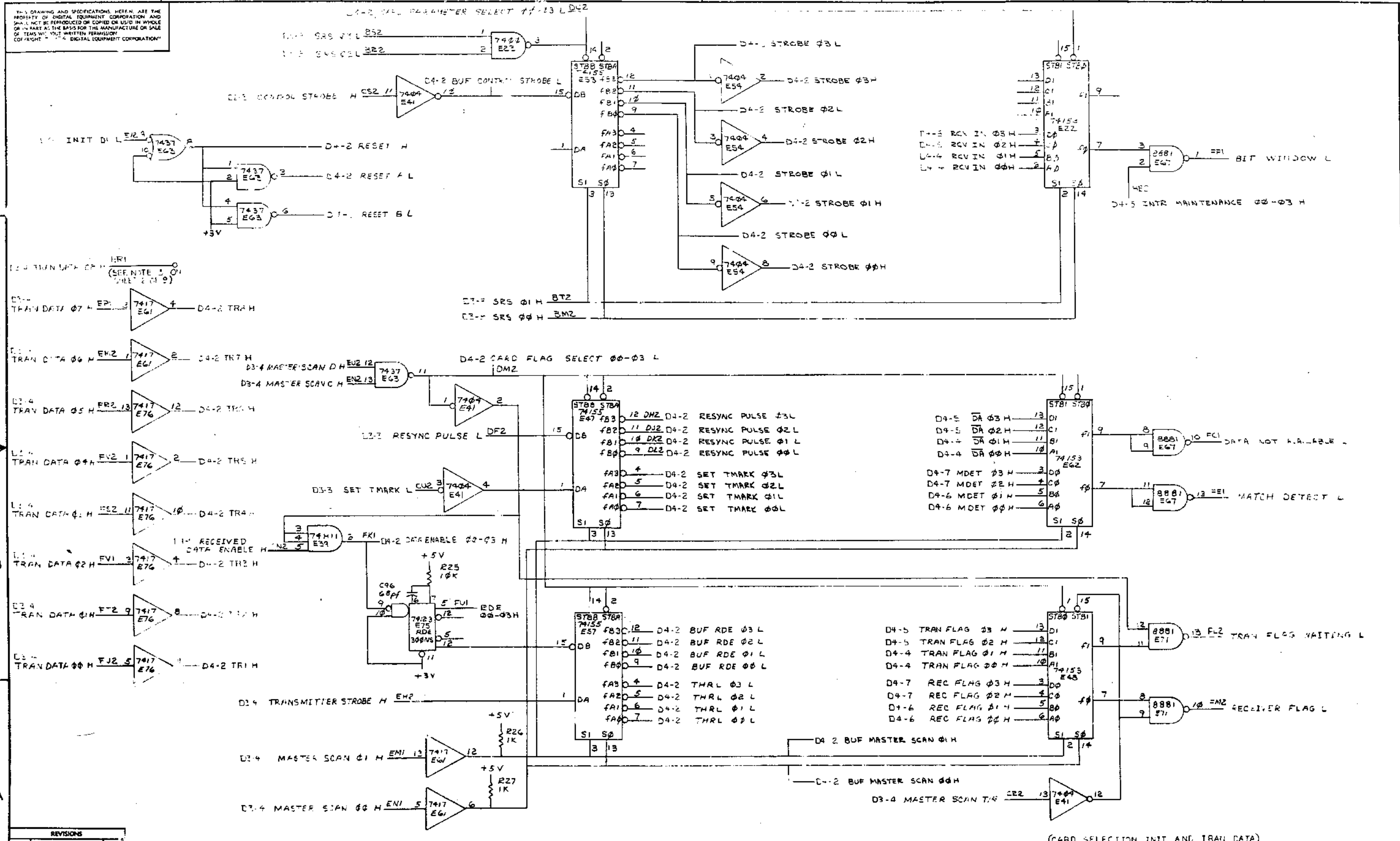


D3-5 230.4 KB H BM1
(SEE NOTE 4)

REVISIONS		
D.R.	CHANGE NO.	REV.

(CHARTS, SWITCHES AND SYNC SELECTOR)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD (D4-1)	D	CS	M7839-Ø-1	B
SCALE	SHEET 2 OF 5	DIST.		



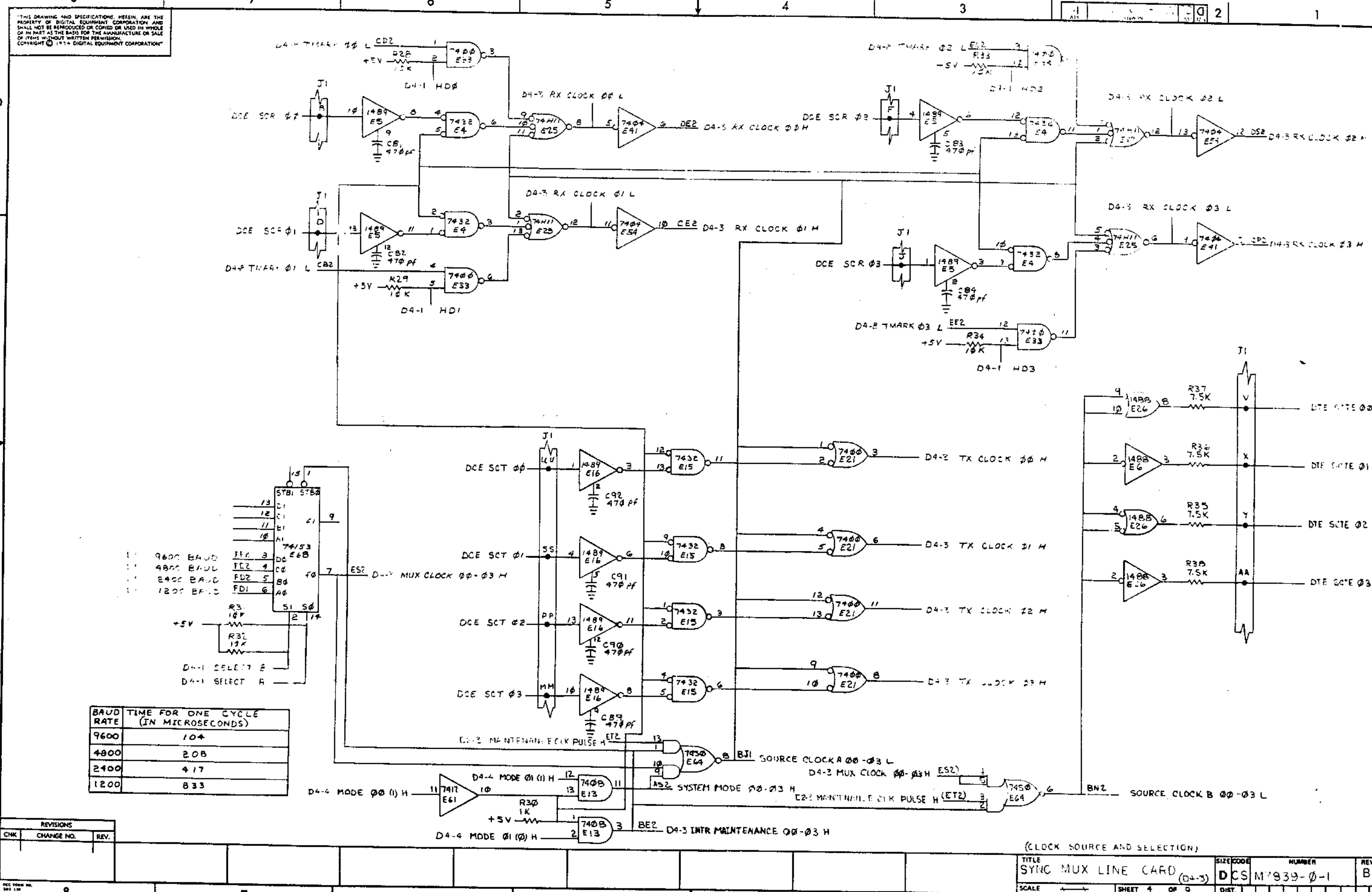
(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: SYNC MUX LINE CARD (D4-2)

SIZE: D | CODE: CS | NUMBER: M7839-Ø-1 | REV.: B

SCALE | SHEET 3 OF 9

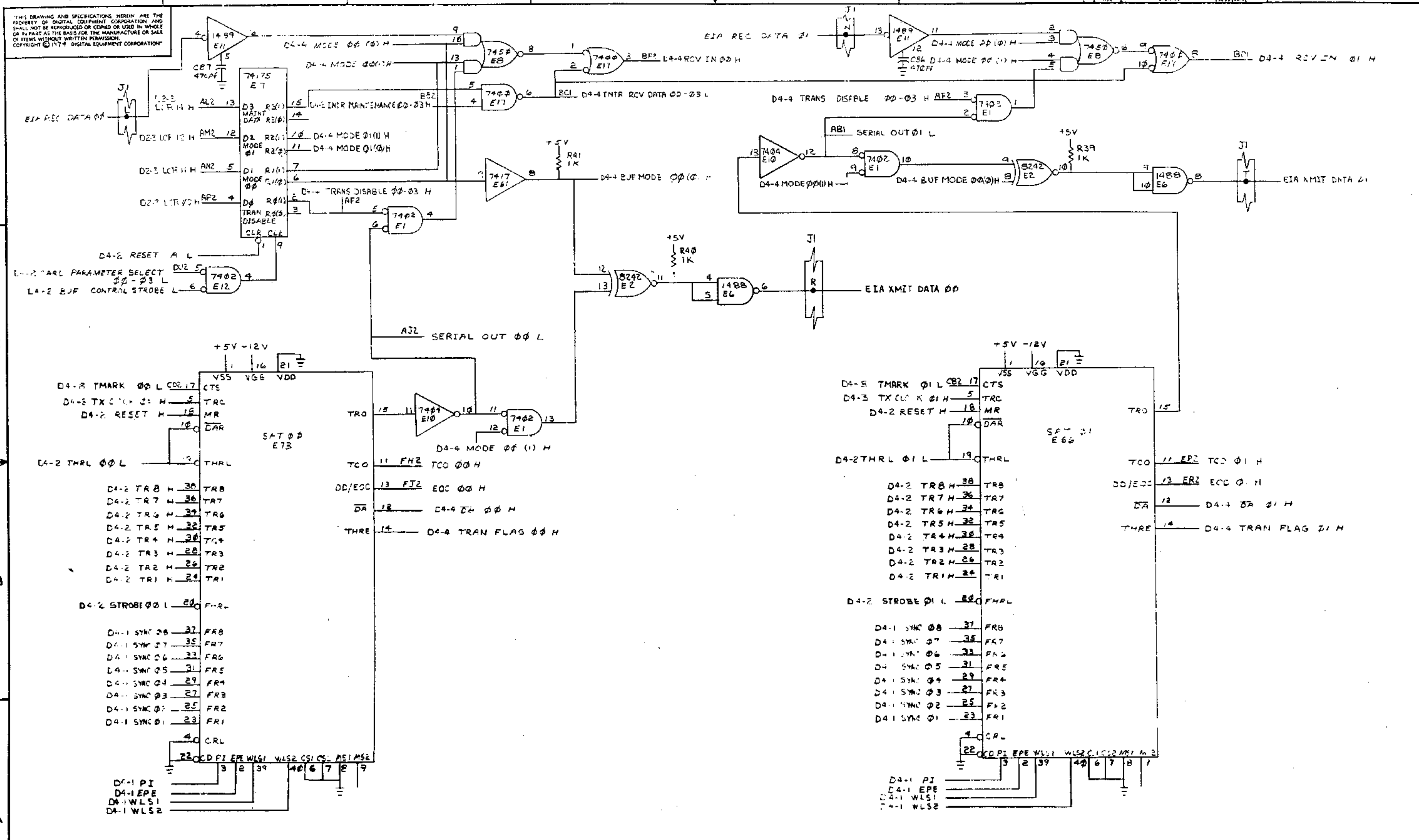


BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

TITLE: SYNC MUX LINE CARD (D4-3)

SIZE D | CODE CS | NUMBER M7839-Ø-1 | REV. B

SHEET 4 OF 9



(MODE SELECTION, TRANSMITTERS ØØ AND Ø1)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD (D4-4)	D	CS	M7839-Ø-1	B

SHEET 5 OF 9

J1 HH — EIA REC DATA Ø2 — 1489 E11 — CBB 470 pf

D4-4 MODE ØØ (Ø) H — D4-4 MODE ØØ (1) H — 74SØ E9 — 74ØØ E23 — BK2 — D4-5 RCV IN Ø2 H

D4-4 TRANS DISABLE ØØ-Ø3 H (AF2) — 7413 E12

D4-4 INTR RCV DATA ØØ-Ø3 L — BC1

D4-4 BUF MODE ØØ (Ø) H — +5V — R42 1K — 8242 E2 — 1488 E6 — J1 CC — EIA XMIT DATA Ø2

D4-4 MODE ØØ (1) H — 1402 E12 — 7404 E1Ø — AT2 — SERIAL OUT Ø2 L

J1 KK — EIA REC DATA Ø3 — 1489 E11 — CBS 470 pf

D4-4 MODE ØØ (Ø) H — D4-4 MODE ØØ (1) H — 74SØ E9 — 7402 E5 — 7400 E23 — BK1 — D4-5 RCV IN Ø3 H

D4-4 MODE ØØ (1) H — 74Ø2 E8 — +5V — R45 1K — D4-4 BUF MODE ØØ (Ø) H — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA Ø3

(AF2) D4-4 TRANS DISABLE ØØ-Ø3 H

+5 -12V — VSS VGG VDD

D4-2 TMARK Ø2 L EL2 17 — CTS
D4-2 TX CLOCK Ø2 H 5 — TRC
D4-2 RESET H 18 — MR
10 — DAR
D4-2 THRL Ø2 L 19 — THRL
D4-2 TR8 H 38 — TR8
D4-2 TR7 H 36 — TR7
D4-2 TR6 H 34 — TR6
D4-2 TR5 H 32 — TR5
D4-2 TR4 H 3Ø — TR4
D4-2 TR3 H 28 — TR3
D4-2 TR2 H 26 — TR2
D4-2 TR1 H 24 — TR1
D4-2 STROBE Ø2 L 26 — FHRL
D4-1 SYNC Ø8 37 — FR8
D4-1 SYNC Ø7 35 — FR7
D4-1 SYNC Ø6 33 — FR6
D4-1 SYNC Ø5 31 — FR5
D4-1 SYNC Ø4 29 — FR4
D4-1 SYNC Ø3 27 — FR3
D4-1 SYNC Ø2 25 — FR2
D4-1 SYNC Ø1 23 — FR1
4 — CRL
22 — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
D4-1 PI 3
D4-1 EPE 2
D4-1 WLS1 39
D4-1 WLS2 40
6 7 8 9

SAT Ø2 E59

TRD 15
TCO 11 EJ2 — TCO Ø2 H
DD/EOC 13 EK2 — EOC Ø2 H
DA 12 — D4-5 DA Ø2 H
THRE 14 — D4-5 TRAN FLAG Ø2 H

+5 -12V — VSS VGG VDD

D4-3 TMARK Ø2 L EE2 17 — CTS
D4-3 TX CLOCK Ø3 H 5 — TRC
D4-2 RESET H 18 — MR
10 — DAR
D4-2 THRL Ø3 L 19 — THRL
D4-2 TR8 H 38 — TR8
D4-2 TR7 H 36 — TR7
D4-2 TR6 H 34 — TR6
D4-2 TR5 H 32 — TR5
D4-2 TR4 H 3Ø — TR4
D4-2 TR3 H 28 — TR3
D4-2 TR2 H 26 — TR2
D4-2 TR1 H 24 — TR1
D4-2 STROBE Ø3 L 26 — FHRL
D4-1 SYNC Ø8 37 — FR8
D4-1 SYNC Ø7 35 — FR7
D4-1 SYNC Ø6 33 — FR6
D4-1 SYNC Ø5 31 — FR5
D4-1 SYNC Ø4 29 — FR4
D4-1 SYNC Ø3 27 — FR3
D4-1 SYNC Ø2 25 — FR2
D4-1 SYNC Ø1 23 — FR1
4 — CRL
22 — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
D4-1 PI 3
D4-1 EPE 2
D4-1 WLS1 39
D4-1 WLS2 40
6 7 8 9

SAT Ø3 E55

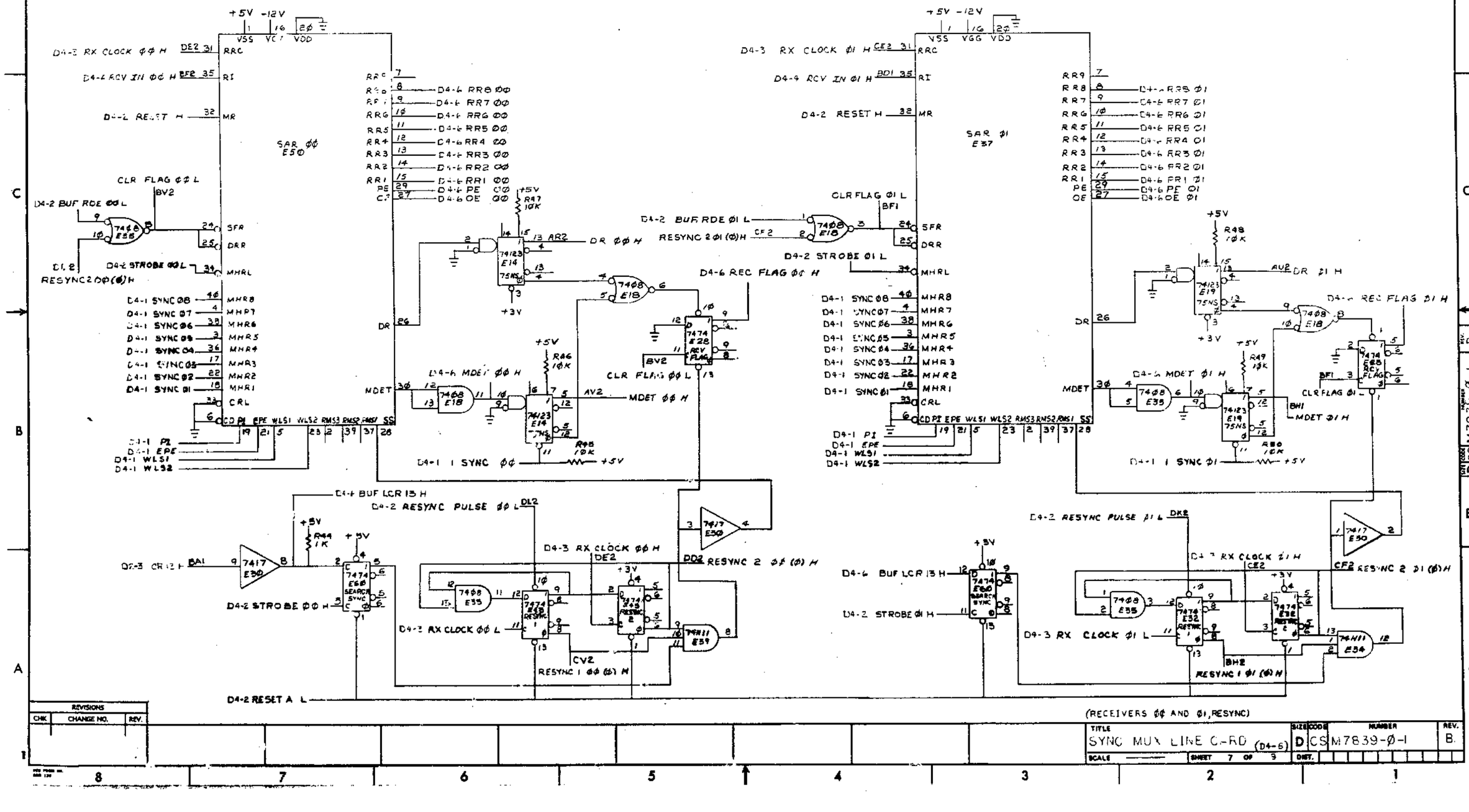
TRD 15 — 7432 E1Ø — AH2 — SERIAL OUT Ø3 L
TCO 11 ED2 — TCO Ø3 H
DD/EOC 13 EF2 — EOC Ø3 H
DA 12 — D4-5 DA Ø3 H
THRE 14 — D4-5 TRAN FLAG Ø3 H

REVISIONS

CHK	CHANGE NO.	REV.

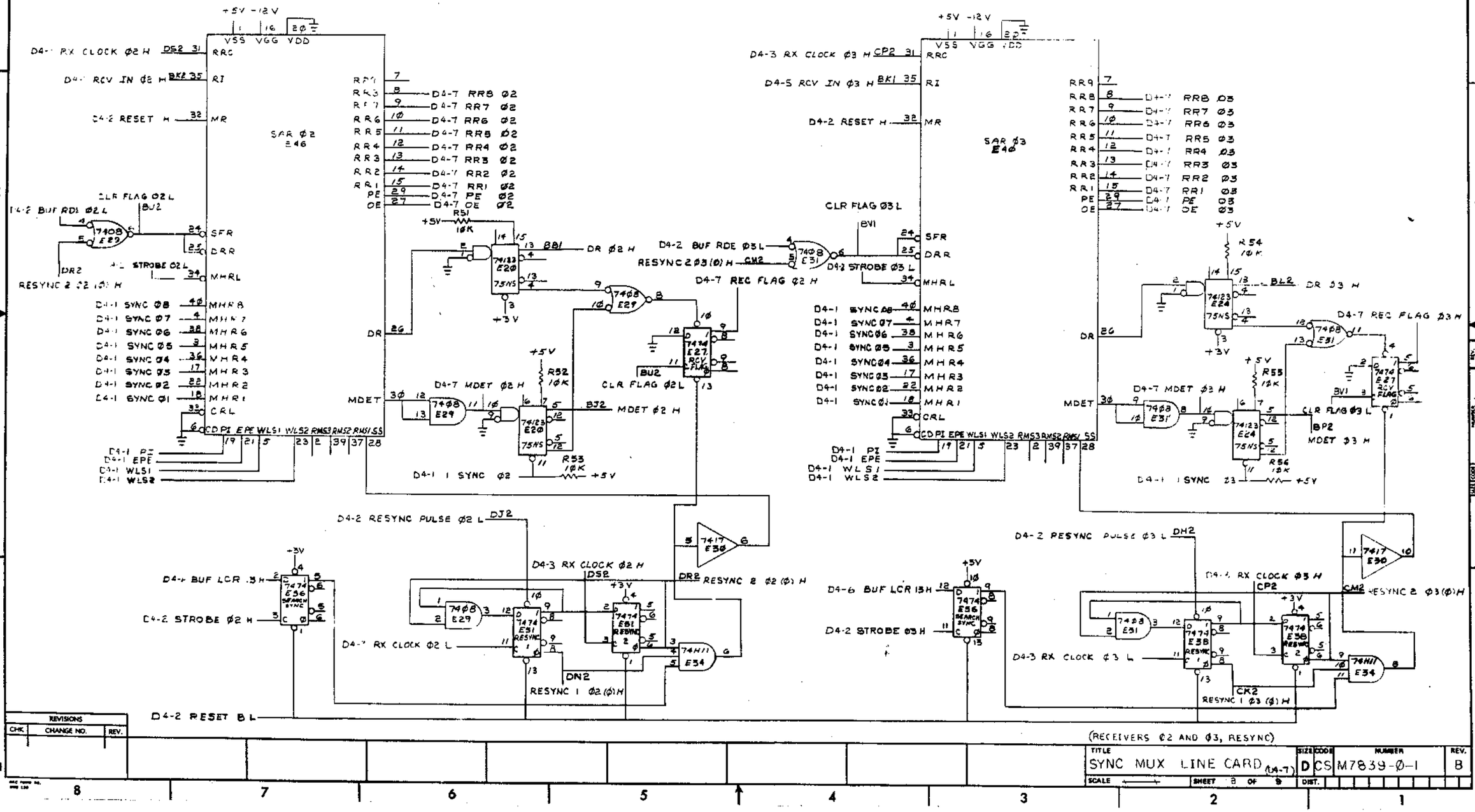
(TRANSMITTERS Ø2 AND Ø3)

TITLE: SYNC MUX LINE CARD (D4-5)
SIZE: D — CODE: CS — NUMBER: M7839-Ø-1 — REV: B
SCALE — SHEET 6 OF 9 — DIST.



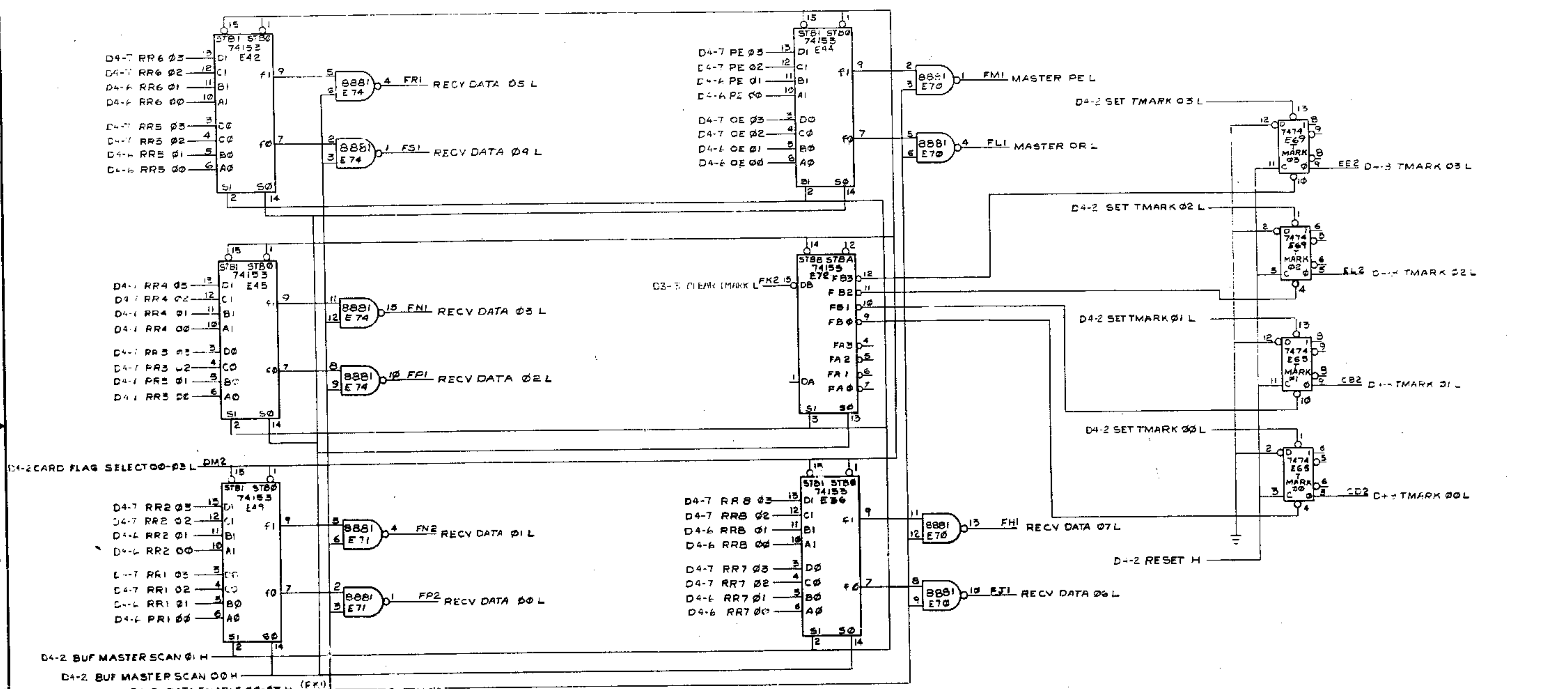
REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE C-RD (D4-6)	D	CS	M7839-Ø-1	B.
SCALE	SHEET 7 OF 9		DIST.	



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD (D4-7)	D	CS	M7839-Ø-1	B
SCALE	SHEET 8 OF 9	DIST.		



(RECV DATA MUX S AND TMARK DECODER)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD (04-8)	D	CS	M7839-Ø-1	B
SCALE	SHEET 9 OF 9			

REVISIONS		
CHK	CHANGE NO.	REV.

BERG PINNING CHART

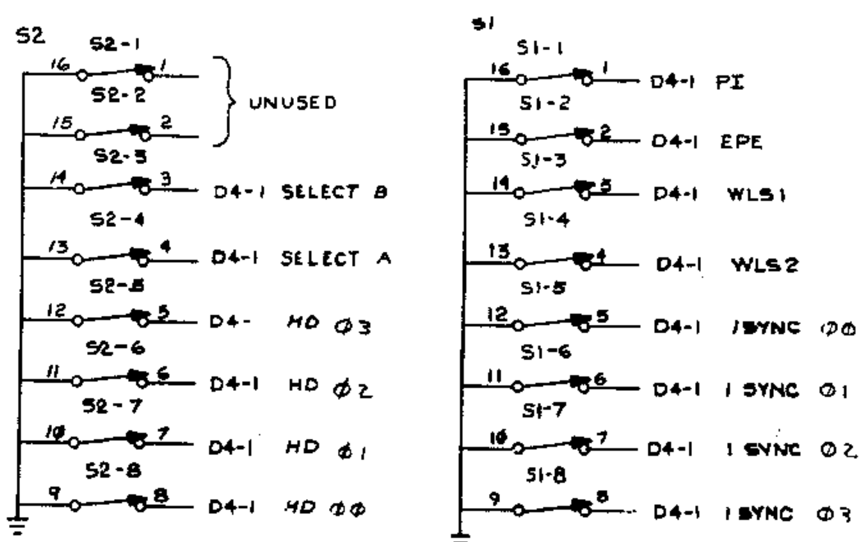
J1	SIGNAL
A	GROUND
B	DCE SCR ØØ
C	GROUND
D	DCE SCR Ø1
E	GROUND
F	DCE SCR Ø2
H	GROUND
J	DCE SCR Ø3
K	GROUND
L	EIA RCV DATA ØØ
M	GROUND
N	EIA RCV DATA Ø1
P	GROUND
R	EIA XMIT DATA ØØ
S	GROUND
T	EIA XMIT DATA Ø1
U	GROUND
V	DTE SCTE ØØ
W	GROUND
X	DTE SCTE Ø1
Y	DTE SCTE Ø2
Z	GROUND
AA	DTE SCTE Ø3
BB	GROUND
CC	EIA XMIT DATA Ø2
DD	GROUND
EE	EIA XMIT DATA Ø3
FF	GROUND
HH	EIA RCV DATA Ø2
JJ	GROUND
KK	EIA RCV DATA Ø3
LL	GROUND
MM	DCE SCT Ø3
NN	GROUND
PP	DCE SCT Ø2
PR	GROUND
SS	DCE SCT Ø1
TT	GROUND
UU	DCE SCT ØØ
VV	GROUND

PARAMETER SWITCH SETTINGS

FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/ SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B SELECT A	S2 S2	3 4	ON ON	ON OFF	OFF ON	OFF OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HD Ø3 HD Ø2 HD Ø1 HD ØØ	S2 S2 S2 S2	5 6 7 8	ON ON ON ON		OFF OFF OFF OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI EPE	S1 S1	1 2	OFF OFF	ON ON	ON OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1 WLS2	S1 S1	3 4	OFF OFF	ON OFF	OFF ON	ON ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC ØØ 1 SYNC Ø1 1 SYNC Ø2 1 SYNC Ø3	S1 S1 S1 S1	5 6 7 8	OFF OFF OFF OFF		ON ON ON ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1 – 8	OFF		ON	
LCR10=1	SYNC B	S3	1 – 8	OFF		ON	

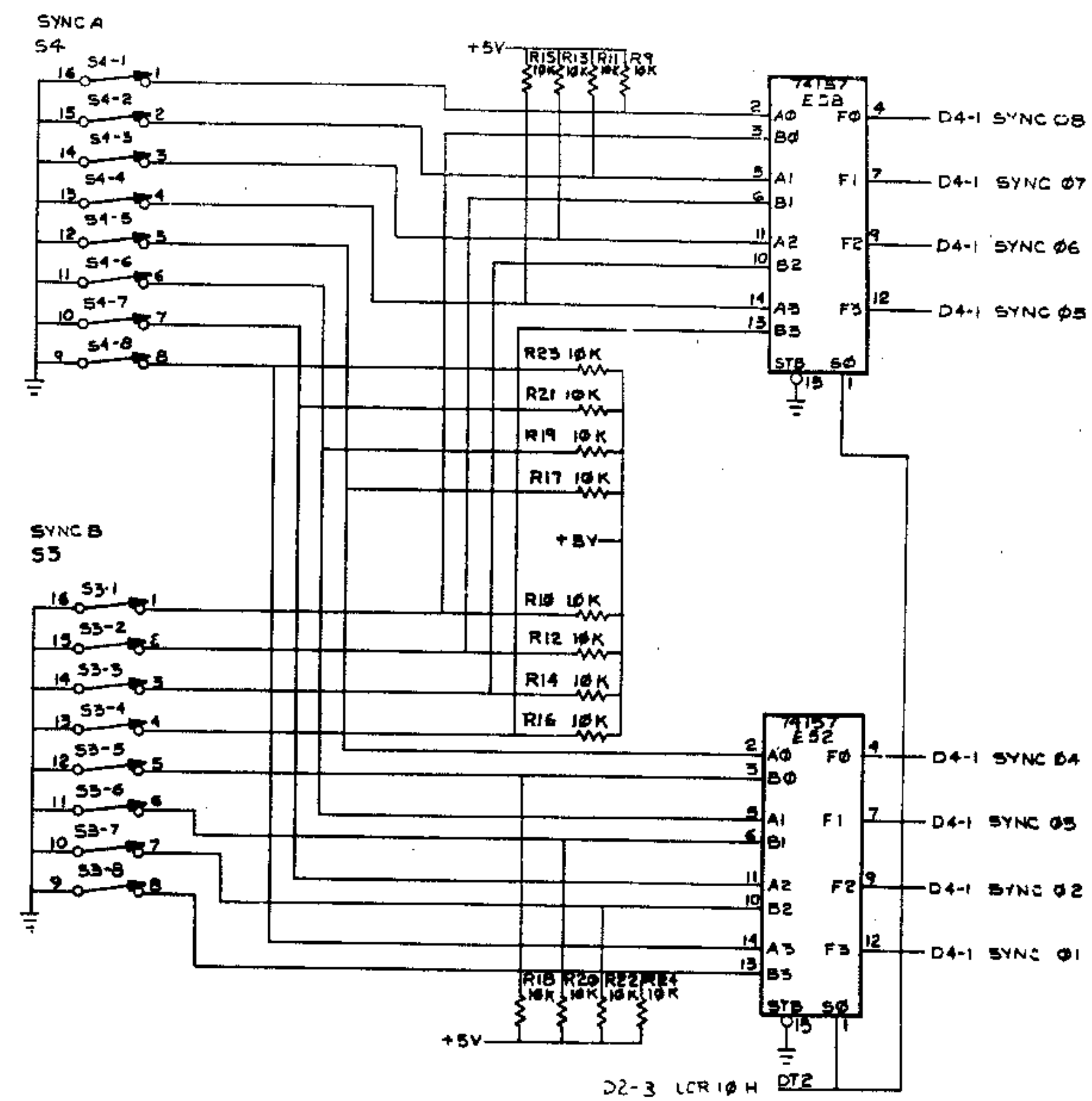
PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1 CS2	GROUND GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1 MS2	GROUND NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1 RMS2 RMS3	NO CONNECTION NO CONNECTION NO CONNECTION



NOTES:

1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA Ø8 H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 23Ø.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.



D3-5 23Ø.4 KB H BM1
(SEE NOTE 4)

(CHARTS SWITCHES AND SYNC SELECTOR)

DRN.	9/[illegible]
CHK'D	4/[illegible]
ENG.	
PROJ. ENG.	
PROD. R W[illegible]	
NEXT HIGHER ASSY.	B DD-DV11-Ø
SCALE	—
SHEET 1 OF 8	

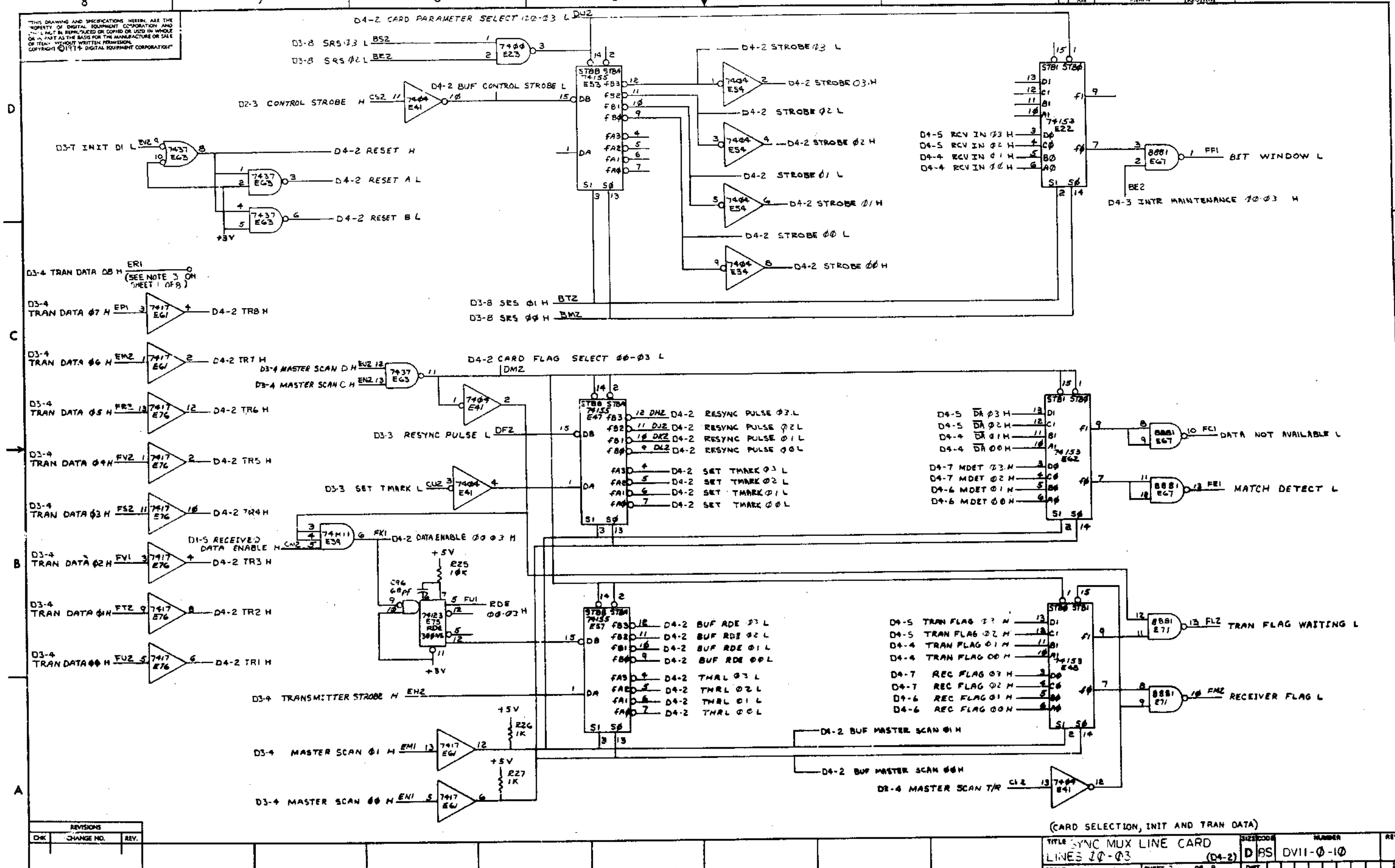
FIRST USED ON: DV11

digital

TITLE: SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-1)

SIZE	CODE	NUMBER	REV.
D	BS	DV11 Ø 10	

DIST.



(CARD SELECTION, INIT AND TRAN DATA)

TITLE SYNC MUX LINE CARD LINES 10-03 (D4-2)

SIZE D | CODE BS | NUMBER DV11-0-10

SHEET 2 OF 8

D4-8 TMARK ØØ L — CD2 — 74ØØ E33 — R28 10K +5V — D4-1 HD ØØ

DCE SCR ØØ — J1 B — 1489 E5 — CB1 47ØpF — 7432 E4 — D4-3 RX CLOCK ØØ L — 74H11 E25 — 7404 E41 — DE2 — D4-3 RX CLOCK ØØ H

D4-8 TMARK Ø2 L — EL2 — 74ØØ E33 — R33 10K +5V — D4-1 HD Ø2

DCE SCR Ø2 — J1 F — 1489 E5 — C83 47ØpF — 7432 E4 — D4-3 RX CLOCK Ø2 L — 74H11 E29 — 7404 E54 — DS2 — D4-3 RX CLOCK Ø2 H

DCE SCR Ø1 — J1 D — 1489 E5 — CB2 47ØpF — 7432 E4 — D4-3 RX CLOCK Ø1 L — 74H11 E25 — 7404 E54 — CE2 — D4-3 RX CLOCK Ø1 H

D4-8 TMARK Ø1 L — CB2 — 74Ø8 E33 — R29 10K +5V — D4-1 HD Ø1

DCE SCR Ø3 — J1 J — 1489 E5 — C84 47ØpF — 7432 E4 — D4-3 RX CLOCK Ø3 L — 74H11 E25 — 7404 E41 — CP2 — D4-3 RX CLOCK Ø3 H

D4-8 TMARK Ø3 L — EE2 — 74Ø5 E33 — R34 10K +5V — D4-1 HD Ø3

J1 — R37 7.5K — DTE SCTE ØØ

R36 7.5K — DTE SCTE Ø1

R35 7.5K — DTE SCTE Ø2

R38 7.5K — DTE SCTE Ø3

DCE SCT ØØ — J1 U — 1489 E16 — C92 47ØpF — 7432 E15 — D4-3 TX CLOCK ØØ H

DCE SCT Ø1 — J1 SS — 1489 E16 — C91 47ØpF — 7432 E15 — D4-3 TX CLOCK Ø1 H

DCE SCT Ø2 — J1 PP — 1489 E16 — C90 47ØpF — 7432 E15 — D4-3 TX CLOCK Ø2 H

DCE SCT Ø3 — J1 MM — 1489 E16 — C89 47ØpF — 7432 E15 — D4-3 TX CLOCK Ø3 H

D3-5 9600 BAUD — FF2
D3-5 4800 BAUD — FE2
D3-5 2400 BAUD — FD2
D3-5 1200 BAUD — FD1

74LS3 E68 — STB1 STB2 — D1 C1 B1 A1 — D6 C6 B6 A6 — S1 S6 — F1 F6 — ES2 — D4-3 MUX CLOCK ØØ-Ø3 H

R31 10K +5V — R32 10K — D4-1 SELECT B — D4-1 SELECT A

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

D2-3 MAINTENANCE CLK PULSE H — ET2 — 74S8 E64 — BS1 — SOURCE CLOCK A ØØ-Ø3 L

D4-3 MUX CLOCK ØØ-Ø3 H (ES2) — D2-3 MAINTENANCE CLK PULSE H (ET2) — 74S8 E64 — BN2 — SOURCE CLOCK B ØØ-Ø3 L

D4-4 MODE Ø1 (1) H — 74S8 E13 — BM2 — SYSTEM MODE ØØ-Ø3 H

D4-4 MODE ØØ (1) H — 74LS11 E61 — R3Ø 1K +5V

D4-4 MODE Ø1 (5) H — 74Ø8 E13 — BE2 — D4-3 INTR MAINTENANCE ØØ-Ø3 H

(CLOCK SOURCE AND SELECTION)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES ØØ-Ø3 (Ø4-3)
SIZE D CODE BS NUMBER DV11-Ø-10 REV.
SCALE — SHEET 3 OF 8 DIST.

D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ(1)H
D4-3 INTR MAINTENANCE ØØ-Ø3 H
D4-4 MODE Ø1(Ø) H
D4-4 MODE Ø1(1)H
D4-4 TRANS DISABLE ØØ-Ø3 H
D4-4 BUF MODE ØØ (Ø) H
D4-4 MODE ØØ (1) H
D4-4 RCV IN ØØ H
D4-4 INTR RCV DATA ØØ-Ø3 L
EIA REC DATA ØØ
D2-3 LCR 14 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR Ø9 H
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT ØØ-Ø3 L
D4-2 BUF CONTROL STROBE L
SERIAL OUT ØØ L
EIA XMIT DATA ØØ

EIA REC DATA Ø1
D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ (1) H
D4-4 TRANS DISABLE ØØ-Ø3 H
SERIAL OUT Ø1 L
D4-4 MODE ØØ(Ø)H
D4-4 BUF MODE ØØ(Ø)H
D4-4 RCV IN Ø1 H
EIA XMIT DATA Ø1

D4-2 TMARK ØØ L
D4-3 TX CLOCK ØØ H
D4-2 RESET H
D4-2 THRL ØØ L
D4-2 TRB H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE ØØ L
D4-1 SYNC ØØ
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
CRL
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TRO
TCO FH2 TCO ØØ H
DD/EOC FJ2 EOC ØØ H
DA D4-4 DA ØØ H
THRE D4-4 TRAN FLAG ØØ H

D4-2 TMARK Ø1 L
D4-3 TX CLOCK Ø1 H
D4-2 RESET H
D4-2 THRL Ø1 L
TCO EP2 TCO Ø1 H
DD/EOC EA2 EOC Ø1 H
DA D4-4 DA Ø1 H
THRE D4-4 TRAN FLAG Ø1 H

(MODE SELECTION, TRANSMITTERS ØØ AND Ø1)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES ØØ-Ø3 (04-4)
SIZE D CODE DBS NUMBER DV11-Ø-10 REV.
SCALE SHEET 4 OF 8 DIST.

EIA REC DATA A2 — J1 HH — 1489 E11 — CBB 47Øpf

D4-4 MODE ØØ (Ø) H — 9, 10
D4-4 MODE ØØ (1) H — 13, 1
7450 E9 — 8 — 7460 E23 — 8 — BK2 — D4-5 RCV IN Ø2 H

D4-4 TRANS DISABLE ØØ-Ø3 H (AF2) — 2, 3 — 7402 E12 — 1

D4-4 INTR RCV DATA ØØ-Ø3 L — BC1

D4-4 MODE ØØ (1) H — 12, 11 — 1402 E12 — 13
D4-4 BUF MODE ØØ (Ø) H — 5, 6 — 8242 E2 — 4
+5V — R42 1K — 12, 13 — 1488 E6 — 11 — J1 CC — EIA XMIT DATA Ø2

5 — 7404 E10 — 6 — AT2 — SERIAL OUT Ø2 L

EIA REC DATA Ø3 — J1 KK — 10 — 1489 E11 — 8 — CB5 47Øpf

D4-4 MODE ØØ (Ø) H — 2, 3
D4-4 MODE ØØ (1) H — 4, 5
7450 E9 — 6 — 13 — 7460 E23 — 11 — BK1 — D4-5 RCV IN Ø3 H

6, 5 — 7402 E3 — 4 — (AF2) — D4-4 TRANS DISABLE ØØ-Ø3 H

D4-4 MODE ØØ (1) H — 9, 8 — 7402 E3 — 10
D4-4 BUF MODE ØØ (Ø) H — 1, 2 — 8242 E2 — 3
+5V — R43 1K — 12, 13 — 1488 E26 — 11 — J1 EE — EIA XMIT DATA Ø3

+5V -12V — 1, 16 — VSS VGG — 21 VDD

SAT Ø2 E59

D4-8 TMARK Ø2 L — EL2 17 — CTS
D4-3 TX CLOCK Ø2 H — 5 — TRC
D4-2 RESET H — 18 — MR
10 — DAR
D4-2 THRL Ø2 L — 19 — HR
TRO — 15
TCO — 11 EJ2 — TCO Ø2 H
DD/EOC — 13 EK2 — EOC Ø2 H
DA — 12 — D4-5 DA Ø2 H
THRE — 14 — D4-5 TRAN FLAG Ø2 H

D4-2 TR8 H — 38 — TR8
D4-2 TR7 H — 36 — TR7
D4-2 TR6 H — 34 — TR6
D4-2 TR5 H — 32 — TR5
D4-2 TR4 H — 30 — TR4
D4-2 TR3 H — 28 — TR3
D4-2 TR2 H — 26 — TR2
D4-2 TR1 H — 24 — TR1

D4-2 STROBE Ø2 L — 22 — FHRL

D4-1 SYNC Ø8 — 37 — FR8
D4-1 SYNC Ø7 — 35 — FR7
D4-1 SYNC Ø6 — 33 — FR6
D4-1 SYNC Ø5 — 31 — FR5
D4-1 SYNC Ø4 — 29 — FR4
D4-1 SYNC Ø3 — 27 — FR3
D4-1 SYNC Ø2 — 25 — FR2
D4-1 SYNC Ø1 — 23 — FR1
4 — CRL
CC — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 — 3 2 39 40 6 7 8 9

D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

+5V -12V — 1, 16 — VSS VGG — 21 VDD

SAT Ø3 E55

D4-8 TMARK Ø3 L — EE2 17 — CTS
D4-3 TX CLOCK Ø3 H — 5 — TRC
D4-2 RESET H — 18 — MR
10 — DAR
D4-2 THRL Ø3 L — 19 — THRL
TRO — 15 — 7404 E10 — 8 — AH2 — SERIAL OUT Ø3 L
TCO — 11 ED2 — TCO Ø3 H
DD/EOC — 13 EF2 — EOC Ø3 H
DA — 12 — D4-5 DA Ø3 H
THRE — 14 — D4-5 TRAN FLAG Ø3 H

D4-2 TR8 H — 38 — TR8
D4-2 TR7 H — 36 — TR7
D4-2 TR6 H — 34 — TR6
D4-2 TR5 H — 32 — TR5
D4-2 TR4 H — 30 — TR4
D4-2 TR3 H — 28 — TR3
D4-2 TR2 H — 26 — TR2
D4-2 TR1 H — 24 — TR1

D4-2 STROBE Ø3 L — 22 — FHRL

D4-1 SYNC Ø8 — 37 — FR8
D4-1 SYNC Ø7 — 35 — FR7
D4-1 SYNC Ø6 — 33 — FR6
D4-1 SYNC Ø5 — 31 — FR5
D4-1 SYNC Ø4 — 29 — FR4
D4-1 SYNC Ø3 — 27 — FR3
D4-1 SYNC Ø2 — 25 — FR2
D4-1 SYNC Ø1 — 23 — FR1
4 — CRL
22 — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 — 3 2 39 40 6 7 8 9

D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

REVISIONS

CHK	CHANGE NO.	REV.

(TRANSMITTERS Ø2 AND Ø3)

TITLE SYNC MUX LINE CARD LINES ØØ-Ø3 (D4-5)
SIZE D — CODE BS — NUMBER DV11-Ø-1Ø — REV.
SCALE — SHEET 5 OF 8 — DIST.

D4-3 RX CLOCK ØØ H — DE2 31 — RRC
D4-4 RCV IN ØØ H — BF2 35 — RI
D4-2 RESET H — 32 — MR
SAR ØØ E5Ø
+5V -12V — VSS 1 — VGG 16 — VDD 2Ø
CLR FLAG ØØ L — BV2
D4-2 BUF RDE ØØ L — 74Ø8 E5Ø
CVE RESYNC 1 ØØ (Ø) H
D4-2 STROBE ØØ L — 34 — MHRL
SFR 24 — DRR 25
D4-1 SYNC ØØ 40 — MHR8
D4-1 SYNC Ø7 4 — MHR7
D4-1 SYNC Ø6 38 — MHR6
D4-1 SYNC Ø5 3 — MHR5
D4-1 SYNC Ø4 36 — MHR4
D4-1 SYNC Ø3 17 — MHR3
D4-1 SYNC Ø2 22 — MHR2
D4-1 SYNC Ø1 18 — MHR1
33 — CRL
6 — CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7
RR8 8 — D4-6 RR8 ØØ
RR7 9 — D4-6 RR7 ØØ
RR6 1Ø — D4-6 RR6 ØØ
RR5 11 — D4-6 RR5 ØØ
RR4 12 — D4-6 RR4 ØØ
RR3 13 — D4-6 RR3 ØØ
RR2 14 — D4-6 RR2 ØØ
RR1 15 — D4-6 RR1 ØØ
PE 29 — D4-6 PE ØØ
OE 27 — D4-6 OE ØØ

+5V — R47 1ØK
74123 E14 75NS — AR2 — DR ØØ H
DR 26
74Ø8 E18
+3V
D4-6 MDET ØØ H — MDET 3Ø
74Ø8 E18
74123 E14 75NS — AV2 — MDET ØØ H
+5V — R46 1ØK
D4-1 1 SYNC ØØ — R45 1ØK — +5V
7474 E28 RCV FLAG — BV2 — CLR FLAG ØØ L
D4-6 REC FLAG ØØ H

D4-6 BUF LCR 13 H — BA1
D4-2 RESYNC PULSE ØØ L — DL2
+5V — R44 1K — +3V
7417 E3Ø
7474 E6Ø SEARCH SYNC — D4-2 STROBE ØØ H
D4-3 RX CLOCK ØØ H — DE2
7474 E45 RESYNC 2
7417 E3Ø — DD2 RESYNC 2 ØØ (Ø) H
74Ø8 E35
D4-3 RX CLOCK ØØ L
74H11 E39
CV2 RESYNC 1 ØØ (Ø) H
D4-2 RESET A L

D4-3 RX CLOCK Ø1 H — CE2 31 — RRC
D4-4 RCV IN Ø1 H — BD1 35 — RI
D4-2 RESET H — 32 — MR
SAR Ø1 E37
+5V -12V — VSS 1 — VGG 16 — VDD 2Ø
CLR FLAG Ø1 L — BF1
D4-2 BUF RDE Ø1 L — 74Ø8 E18
RESYNC 1 Ø1 (Ø) H — BH2
D4-2 STROBE Ø1 L — 34 — MHRL
SFR 24 — DRR 25
D4-1 SYNC Ø8 40 — MHR8
D4-1 SYNC Ø7 4 — MHR7
D4-1 SYNC Ø6 38 — MHR6
D4-1 SYNC Ø5 3 — MHR5
D4-1 SYNC Ø4 36 — MHR4
D4-1 SYNC Ø3 17 — MHR3
D4-1 SYNC Ø2 22 — MHR2
D4-1 SYNC Ø1 18 — MHR1
33 — CRL
6 — CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

RR9 7
RR8 8 — D4-6 RR8 Ø1
RR7 9 — D4-6 RR7 Ø1
RR6 1Ø — D4-6 RR6 Ø1
RR5 11 — D4-6 RR5 Ø1
RR4 12 — D4-6 RR4 Ø1
RR3 13 — D4-6 RR3 Ø1
RR2 14 — D4-6 RR2 Ø1
RR1 15 — D4-6 RR1 Ø1
PE 29 — D4-6 PE Ø1
OE 27 — D4-6 OE Ø1

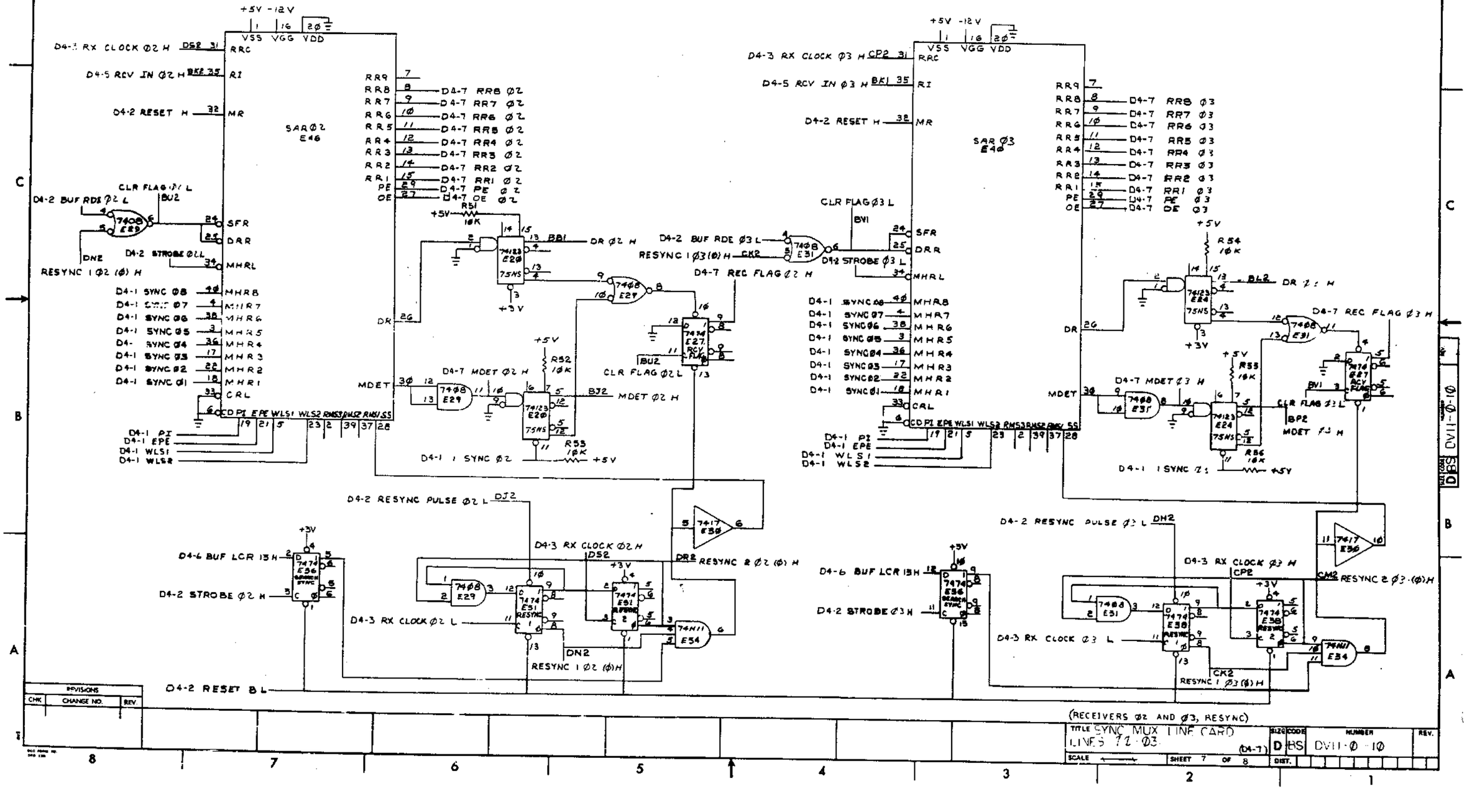
+5V — R48 1ØK
74123 E19 75NS — AU2 — DR Ø1 H
DR 26
74Ø8 E18
+3V
D4-6 REC FLAG Ø1 H
D4-6 MDET Ø1 H — MDET 3Ø
74Ø8 E35
74123 E19 75NS — BH1 — MDET Ø1 H
+5V — R49 1ØK
D4-1 1 SYNC Ø1 — R86 1ØK — +5V
7474 E28 RCV FLAG — BF1 — CLR FLAG Ø1 L

D4-6 BUF LCR 13 H
D4-2 RESYNC PULSE Ø1 L — DK2
+3V
7474 E6Ø SEARCH SYNC
D4-2 STROBE Ø1 H
D4-3 RX CLOCK Ø1 H — CE2
7474 E32 RESYNC 2
7417 E5Ø — CF2 RESYNC 2 Ø1 (Ø) H
74Ø8 E35
D4-3 RX CLOCK Ø1 L
74H11 E54
BH2 RESYNC 1 Ø1 (Ø) H

(RECEIVERS ØØ AND Ø1, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES 00-03 (D4-6)	D	BS	DV11-Ø-1Ø	
SCALE —	SHEET 6 OF 8		DWG.	



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø2 · Ø3 (D4-7)	D	BS	DV11-Ø-10	
SCALE	SHEET 7 OF 8		DIST.	

D4-7 RR6 Ø3
D4-7 RR6 Ø2
D4-6 RR6 Ø1
D4-6 RR6 ØØ
D4-7 RR5 Ø3
D4-7 RR5 Ø2
D4-6 RR5 Ø1
D4-6 RR5 ØØ
STB1 STBØ 74153 D1 E42 C1 B1 A1 DØ CØ BØ AØ SI SØ F1 FØ
8881 E74 → FR1 RECV DATA Ø5 L
8881 E74 → FS1 RECV DATA Ø4 L

D4-7 PE Ø3
D4-7 PE Ø2
D4-6 PE Ø1
D4-6 PE ØØ
D4-7 OE Ø3
D4-7 OE Ø2
D4-6 OE Ø1
D4-6 OE ØØ
STB1 STBØ 74153 D1 E44 C1 B1 A1 DØ CØ BØ AØ SI SØ F1 FØ
8881 E70 → FM1 MASTER PE L
8881 E70 → FL1 MASTER OR L

D4-7 RR4 Ø3
D4-7 RR4 Ø2
D4-6 RR4 Ø1
D4-6 RR4 ØØ
D4-7 RR3 Ø3
D4-7 RR3 Ø2
D4-6 RR3 Ø1
D4-6 RR3 ØØ
STB1 STBØ 74153 D1 E45 C1 B1 A1 DØ CØ BØ AØ SI SØ F1 FØ
8881 E74 → FN1 RECV DATA Ø3 L
8881 E74 → FP1 RECV DATA Ø2 L

D3-3 CLEAR TMARK L FK2
STB8 STBA 74153 E72 DB DA F B3 F B2 F B1 F B0 F A3 F A2 F A1 F A0 SI SØ
D4-2 SET TMARK Ø3 L
D4-2 SET TMARK Ø2 L
D4-2 SET TMARK Ø1 L
D4-2 SET TMARK ØØ L
7474 E69 T MARK Ø3 → EE2 D4-8 TMARK Ø3 L
7474 E69 T MARK Ø2 → EL2 D4-8 TMARK Ø2 L
7474 E65 T MARK Ø1 → CB2 D4-8 TMARK Ø1 L
7474 E65 T MARK ØØ → CD2 D4-8 TMARK ØØ L
D4-2 RESET H

D4-2 CARD FLAG SELECT ØØ-Ø3 L DM2
D4-7 RR2 Ø3
D4-7 RR2 Ø2
D4-6 RR2 Ø1
D4-6 RR2 ØØ
D4-7 RR1 Ø3
D4-7 RR1 Ø2
D4-6 RR1 Ø1
D4-6 RR1 ØØ
STB1 STBØ 74153 D1 E49 C1 B1 A1 DØ CØ BØ AØ SI SØ F1 FØ
8881 E71 → FN2 RECV DATA Ø1 L
8881 E71 → FP2 RECV DATA ØØ L

D4-7 RR8 Ø3
D4-7 RR8 Ø2
D4-6 RR8 Ø1
D4-6 RR8 ØØ
D4-7 RR7 Ø3
D4-7 RR7 Ø2
D4-6 RR7 Ø1
D4-6 RR7 ØØ
STB1 STBØ 74153 D1 E36 C1 B1 A1 DØ CØ BØ AØ SI SØ F1 FØ
3881 E70 → FH1 RECV DATA Ø7 L
8881 E70 → FJ1 RECV DATA Ø6 L

D4-2 BUF MASTER SCAN Ø1 H
D4-2 BUF MASTER SCAN ØØ H
D4-2 DATA ENABLE ØØ-Ø3 H (FK1)

REVISIONS
CHK | CHANGE NO. | REV.

(RECV DATA MUXS AND TMARK DECODER)

TITLE SYNC MUX LINE CARD LINES ØØ-Ø3 (24-8)
SIZE D | CODE 8S | NUMBER DVII Ø-10 | REV.
SCALE | SHEET 8 OF 8 | DIST.

BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR Ø9
C	GROUND
D	DCE SCR Ø5
E	GROUND
F	DCE SCR Ø6
H	GROUND
J	DCE SCR Ø7
K	GROUND
L	EIA RCV DATA Ø9
M	GROUND
N	EIA RCV DATA Ø5
P	GROUND
R	EIA XMIT DATA 14
S	GROUND
T	EIA XMIT DATA Ø5
U	GROUND
V	DTE SCTE Ø4
W	GROUND
X	DTE SCTE Ø5
Y	DTE SCTE Ø6
Z	GROUND
A A	DTE SCTE Ø7
B B	GROUND
C C	EIA XMIT DATA Ø6
D D	GROUND
E E	EIA XMIT DATA Ø7
F F	GROUND
H H	EIA RCV DATA Ø8
J J	GROUND
K K	EIA RCV DATA Ø7
L L	GROUND
M M	DCE SCT Ø7
N N	GROUND
P P	DCE SCT Ø8
R R	GROUND
S S	DCE SCT Ø5
T T	GROUND
U U	DCE SCT Ø4
V V	GROUND

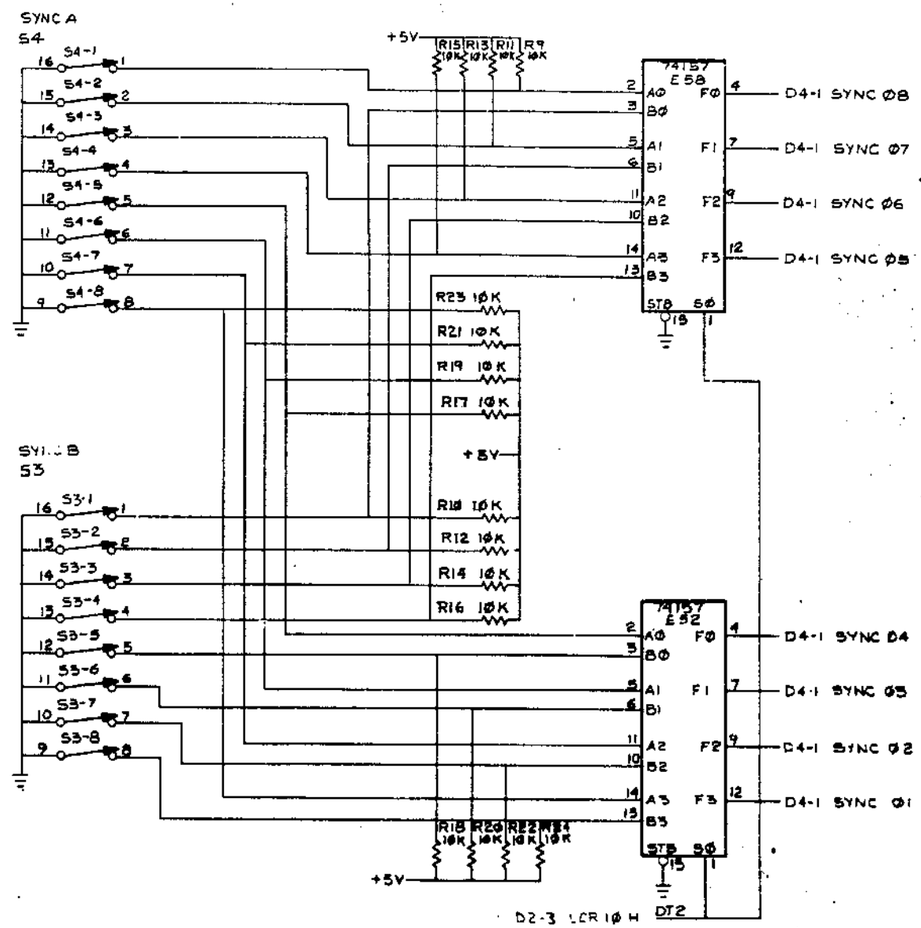
PARAMETER SWITCH SETTINGS

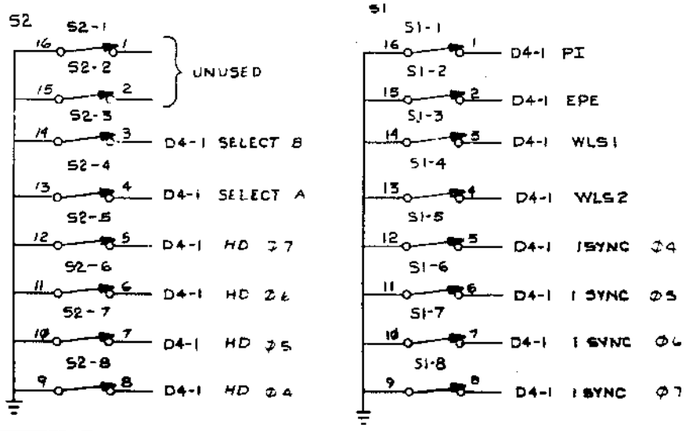
FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B	S2	3	ON	ON	OFF	OFF
	SELECT A	S2	4	ON	OFF	ON	OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HD Ø7	S2	5	ON		OFF	
	HD Ø6	S2	6	ON		OFF	
	HD Ø5	S2	7	ON		OFF	
	HD Ø4	S2	8	ON		OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI	S1	1	OFF	ON	ON	
	EPE	S1	2	OFF	ON	OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1	S1	3	OFF	ON	OFF	ON
	WLS2	S1	4	OFF	OFF	ON	ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC Ø4	S1	5	OFF		ON	
	1 SYNC Ø5	S1	6	OFF		ON	
	1 SYNC Ø6	S1	7	OFF		ON	
	1 SYNC Ø7	S1	8	OFF		ON	
SYNC SELECT				ONE		ZERO	
LCR10=Ø	SYNC A	S4	1-8	OFF		ON	
LCR10=1	SYNC B	S3	1-8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1	GROUND
	CS2	GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1	GROUND
	MS2	NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1	NO CONNECTION
	RMS2	NO CONNECTION
	RMS3	NO CONNECTION

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA Ø8 H. NO M7839 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.



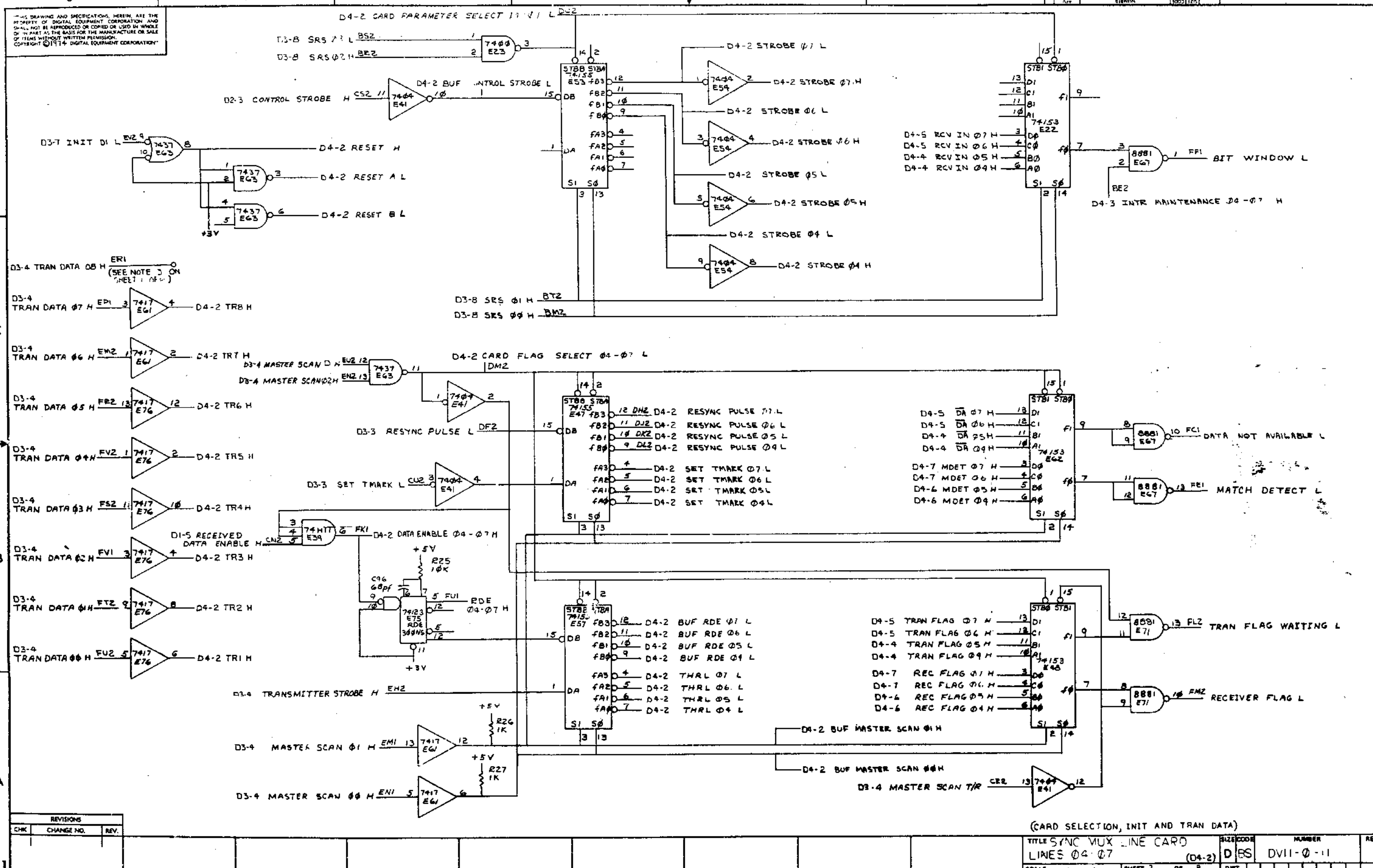


D3-5 230.4 KB H BM1
(SEE NOTE 4)

REVISIONS		
CHK	CHANGE NO.	REV.

(CHARTS SWITCHES AND SYNC SELECTOR)

DRN	4/77	FIRST USED ON: DV11
CHK	4/77	digital
ENG.		TITLE: SYNC MUX LINE CARD LINES Ø4 - Ø7 (D4-1)
PROJ. ENG.		
PROD.		
NEXT HIGHER ASSY		SIZE D, CODE BS, NUMBER DV11-Ø-11, REV.
M-DD DV11-Ø		DIST.
SCALE		
SHEET 1 OF 8		



REVISIONS

(CARD SELECTION, INIT AND TRAN DATA)

TITLE SYNC MUX LINE CARD LINES Ø4-Ø7 (D4-2)

SIZE D CODE BS NUMBER DV11-Ø-11

SHEET 2 OF 8

D4-8 TMARK Ø4 L — CD2 — R28 10K — +5V — D4-1 HD Ø4

D4-8 TMARK Ø6 L — EL2 — R33 10K — -5V — D4-1 HD Ø6

D4-8 TMARK Ø5 L — CB2 — R29 10K — +5V — D4-1 HD Ø5

D4-8 TMARK Ø7 L — EE2 — R34 10K — +5V — D4-1 HD Ø7

J1 — DCE SCR Ø4 — 1489 E5 — C81 470 pf — 7432 E4 — 74H11 E25 — D4-3 RX CLOCK Ø4 L — 7404 E41 — DE2 — D4-3 RX CLOCK Ø4 H

J1 — DCE SCR Ø6 — 1489 E5 — C83 470 pf — 7432 E4 — 74H11 E37 — D4-3 RX CLOCK Ø6 L — 7404 E54 — DS2 — D4-3 RX CLOCK Ø6 H

J1 — DCE SCR Ø5 — 1489 E5 — C82 470 pf — 7432 E4 — 74H11 E25 — D4-3 RX CLOCK Ø5 L — 7404 E54 — CE2 — D4-3 RX CLOCK Ø5 H

J1 — DCE SCR Ø7 — 1489 E5 — C84 470 pf — 7432 E4 — 74H11 E25 — D4-3 RX CLOCK Ø7 L — 7404 E41 — CP2 — D4-3 RX CLOCK Ø7 H

J1 — DCE SCT Ø4 — 1489 E16 — C92 470 pf — 7432 E15 — 7400 E21 — D4-3 TX CLOCK Ø4 H

J1 — DCE SCT Ø5 — 1489 E16 — C91 470 pf — 7432 E15 — 7400 E21 — D4-3 TX CLOCK Ø5 H

J1 — DCE SCT Ø6 — 1489 E16 — C90 470 pf — 7432 E15 — 7400 E21 — D4-3 TX CLOCK Ø6 H

J1 — DCE SCT Ø7 — 1489 E16 — C89 470 pf — 7432 E15 — 7400 E21 — D4-3 TX CLOCK Ø7 H

J1 — 1488 E26 — R37 7.5K — V — DTE SCTE Ø4

1488 E26 — R36 7.5K — X — DTE SCTE Ø5

1488 E26 — R35 7.5K — Y — DTE SCTE Ø6

1488 E26 — R38 7.5K — AA — DTE SCTE Ø7

74153 E48 — ST8I ST84 — D3-5 9600 BAUD — FF2 — D3-5 4800 BAUD — FE2 — D3-5 2400 BAUD — FD2 — D3-5 1200 BAUD — FD1 — R31 10K — R32 10K — +5V — D4-1 SELECT B — D4-1 SELECT A — ES2 — D4-3 MUX CLOCK Ø4-Ø7 H

BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

D2-3 MAINTENANCE CLK PULSE H — ET2 — 7450 E64 — BJ1 — SOURCE CLOCK A Ø4-Ø7 L

D4-3 MUX CLOCK Ø4-Ø7 H (ES2) — D2-3 MAINTENANCE CLK PULSE H (ET2) — 7450 E64 — BN2 — SOURCE CLOCK B Ø4-Ø7 L

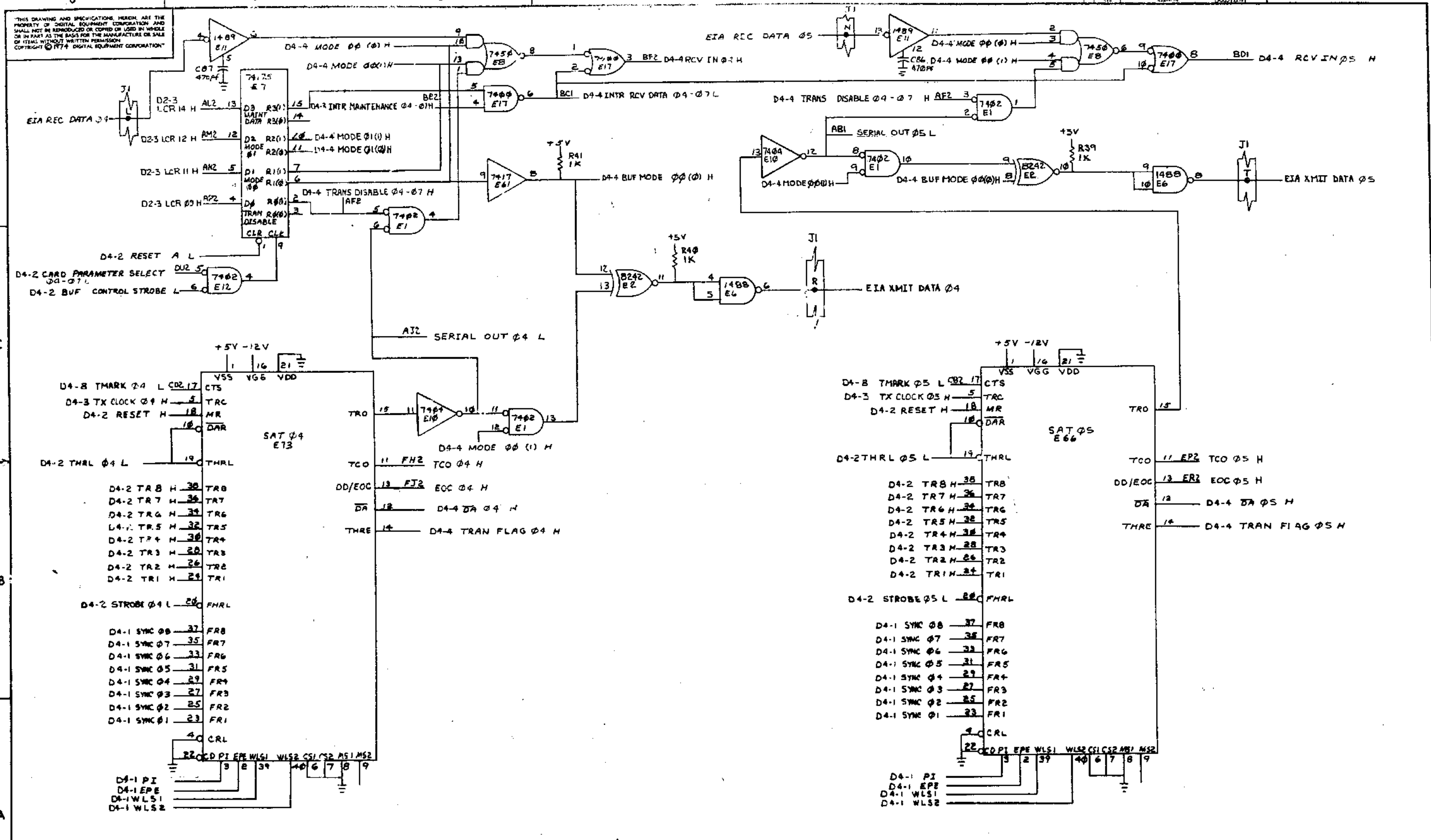
D4-4 MODE Ø0 (1) H — 74IT E61 — D4-4 MODE Ø1 (1) H — 7408 E13 — R30 1K — +5V — D4-4 MODE Ø1 (Ø) H — 7408 E13 — BE2 — D4-3 INTR MAINTENANCE Ø4-Ø7 H

M52 — SYSTEM MODE Ø4-Ø7 H

REVISIONS		
CHK	CHANGE NO.	REV.

(CLOCK SOURCE AND SELECTION)

TITLE SYNC MUX LINE CARD LINES Ø4 Ø7 (D4-3)
SIZE D CODE BS NUMBER DV11-Ø-11 REV.
SCALE — SHEET 3 OF 8 DIST.



REVISIONS

CHK	CHANGE NO.	REV.

(MODE SELECTION, TRANSMITTERS Ø4 AND Ø5)

TITLE SYNC MUX LINE CARD LINES Ø4 - Ø7 (D4-4)

SIZE D CODE BS NUMBER DV11-Ø-11 REV.

SCALE — SHEET 4 OF 8

EIA REC DATA Ø6 — J1 HH — 1489 E11 — CBB 470pf

D4-4 MODE ØØ (Ø) H — 7450 E9

D4-4 MODE ØØ (1) H — 7450 E9

D4-4 TRANS DISABLE Ø4-Ø7 H (AF2) — 7402 E12

7460 E23 — BK2 — D4-5 RCV IN Ø6 H

D4-4 INTR RCV DATA Ø4-Ø7 L — BC1

D4-4 BUF MODE ØØ (Ø) H — +5V — R42 1K

D4-4 MODE ØØ (1) H — 7402 E12 — 8242 E2 — 1488 E6 — J1 CC — EIA XMIT DATA Ø6

7404 E10 — AT2 — SERIAL OUT Ø6 L

EIA REC DATA Ø7 — J1 KK — 1489 E11 — CB5 470pf

D4-4 MODE ØØ (Ø) H — 7450 E9

D4-4 MODE ØØ (1) H — 7402 E3

7460 E23 — BK1 — D4-5 RCV IN Ø7 H

D4-4 MODE ØØ (1) H — 7402 E3

D4-4 BUF MODE ØØ (Ø) H — +5V — R43 1K — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA Ø7

(AF2) D4-4 TRANS DISABLE Ø4-Ø7 H

+5V -12V — VSS 1 — VGG 16 — VDD 21

SAT Ø6 E59

D4-8 TMARK Ø6 L EE2 17 — CTS
D4-3 TX CLOCK Ø6 H 5 — TRC
D4-2 RESET H 18 — MR
10 — DAR
D4-2 THRL Ø6 L 19 — THRL
D4-2 TRB H 38 — TRB
D4-2 TR7 H 36 — TR7
D4-2 TR6 H 34 — TR6
D4-2 TR5 H 32 — TR5
D4-2 TR4 H 30 — TR4
D4-2 TR3 H 28 — TR3
D4-2 TR2 H 26 — TR2
D4-2 TR1 H 24 — TR1
D4-2 STROBE Ø6 L 20 — FHRL
D4-1 SYNC Ø8 37 — FR8
D4-1 SYNC Ø7 35 — FR7
D4-1 SYNC Ø6 33 — FR6
D4-1 SYNC Ø5 31 — FR5
D4-1 SYNC Ø4 29 — FR4
D4-1 SYNC Ø3 27 — FR3
D4-1 SYNC Ø2 25 — FR2
D4-1 SYNC Ø1 23 — FR1
4 — CRL
22 — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO 15 — D4-8 TMARK Ø6 L EE2 17
TCO 11 EJ2 — TCO Ø6 H
DD/EOC 13 EK2 — EOC Ø6 H
DA 12 — D4-5 DA Ø6 H
THRE 14 — D4-5 TRAN FLAG Ø6 H

+5V -12V — VSS 1 — VGG 16 — VDD 21

SAT Ø7 E58

D4-8 TMARK Ø7 L EE2 17 — CTS
D4-3 TX CLOCK Ø7 H 5 — TRC
D4-2 RESET H 18 — MR
10 — DAR
D4-2 THRL Ø7 L 19 — THRL
D4-2 TRB H 38 — TRB
D4-2 TR7 H 36 — TR7
D4-2 TR6 H 34 — TR6
D4-2 TR5 H 32 — TR5
D4-2 TR4 H 30 — TR4
D4-2 TR3 H 28 — TR3
D4-2 TR2 H 26 — TR2
D4-2 TR1 H 24 — TR1
D4-2 STROBE Ø7 L 20 — FHRL
D4-1 SYNC Ø8 37 — FR8
D4-1 SYNC Ø7 35 — FR7
D4-1 SYNC Ø6 33 — FR6
D4-1 SYNC Ø5 31 — FR5
D4-1 SYNC Ø4 29 — FR4
D4-1 SYNC Ø3 27 — FR3
D4-1 SYNC Ø2 25 — FR2
D4-1 SYNC Ø1 23 — FR1
4 — CRL
22 — CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
3 2 39 46 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO 15 — 7404 E10 — AH2 — SERIAL OUT Ø7 L
TCO 11 ED2 — TCO Ø7 H
DD/EOC 13 EF2 — EOC Ø7 H
DA 12 — D4-5 DA Ø7 H
THRE 14 — D4-5 TRAN FLAG Ø7 H

REVISIONS

CHK	CHANGE NO.	REV.

(TRANSMITTERS Ø6 AND Ø7)

TITLE SYNC MUX LINE CARD LINES Ø4-Ø7 (D4-5)

SIZE D — CODE BS — NUMBER DVII-Ø-II — REV.

SCALE — SHEET 5 OF 8 — DIST.

DBS DVII-Ø-II

+5V -12V VSS VGG VDD 2Ø

D4-3 RX CLOCK Ø4 H DE2 31 RRC
D4-4 RCV IN Ø4 H DF2 35 RI
D4-2 RESET H 32 MR
SAR Ø4 E50

RR9 7
RR8 8 D4-6 RR8 Ø4
RR7 9 D4-6 RR7 Ø4
RR6 10 D4-6 RR6 Ø4
RR5 11 D4-6 RR5 Ø4
RR4 12 D4-6 RR4 Ø4
RR3 13 D4-6 RR3 Ø4
RR2 14 D4-6 RR2 Ø4
RR1 15 D4-6 RR1 Ø4
PE 29 D4-6 PE Ø4
OE 27 D4-6 OE Ø4

CLR FLAG Ø4 L BV2
D4-2 BUF RDE Ø4 L
74ØB E35
24 SFR
25 DRR
CV2
RESYNC 1 Ø4 (Ø) H
D4-2 STROBE Ø4 L 34 MHRL
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
33 CRL
6 CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

+5V R47 10K
74123 E14 75NS
AR2 DR Ø4 H
DR 26
+3V
74ØB E18
MDET 30
D4-6 MDET Ø4 H
+5V R46 10K
AV2 MDET Ø4 H
D4-1 1 SYNC Ø4
R45 10K +5V
74174 E28 RCV FLAG
BV2 CLR FLAG Ø4 L

D4-6 BUF LCR 13 H
D4-2 RESYNC PULSE Ø4 L DL2
+5V R44 1K +3V
D2-3 LCR 13 H BA1
7417 E30
74174 E60 SEARCH SYNC
D4-2 STROBE Ø4 H
D4-3 RX CLOCK Ø4 H DE2
74ØB E35
74174 E48 RESYNC
D4-3 RX CLOCK Ø4 L
CV2 RESYNC 1 Ø4 (Ø) H
74H11 E39
DD2 RESYNC 2 Ø4 (Ø) H
D4-2 RESET A L

+5V -12V VSS VGG VDD 2Ø

D4-3 RX CLOCK Ø5 H CE2 31 RRC
D4-4 RCV IN Ø5 H BD1 35 RI
D4-2 RESET H 38 MR
SAR Ø5 E37

RR9 7
RR8 8 D4-6 RR8 Ø5
RR7 9 D4-6 RR7 Ø5
RR6 10 D4-6 RR6 Ø5
RR5 11 D4-6 RR5 Ø5
RR4 12 D4-6 RR4 Ø5
RR3 13 D4-6 RR3 Ø5
RR2 14 D4-6 RR2 Ø5
RR1 15 D4-6 RR1 Ø5
PE 29 D4-5 PE Ø5
OE 27 D4-6 OE Ø5

CLR FLAG Ø5 L BF1
D4-2 BUF RDE Ø5 L
74ØB E18
RESYNC 1 Ø5 (Ø) H BH2
24 SFR
25 DRR
D4-2 STROBE Ø5 L 34 MHRL
D4-6 REC FLAG Ø4 H
D4-1 SYNC Ø8 40 MHR8
D4-1 SYNC Ø7 4 MHR7
D4-1 SYNC Ø6 38 MHR6
D4-1 SYNC Ø5 3 MHR5
D4-1 SYNC Ø4 36 MHR4
D4-1 SYNC Ø3 17 MHR3
D4-1 SYNC Ø2 22 MHR2
D4-1 SYNC Ø1 18 MHR1
33 CRL
6 CDPI EPE WLS1 WLS2 RMS3 RMS2 RMS1 SS
19 21 5 23 2 39 37 28
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

+5V R48 10K
74123 E19 75NS
AV2 DR Ø5 H
DR 26
+3V
74ØB E18
D4-6 REC FLAG Ø5 H
+5V R49 10K
MDET 30
D4-6 MDET Ø5 H
74ØB E35
74123 E19 75NS
BN1 MDET Ø5 H
BF1 3
CLR FLAG Ø5 L
74174 E68 RCV FLAG
D4-1 1 SYNC Ø5
R86 10K +5V

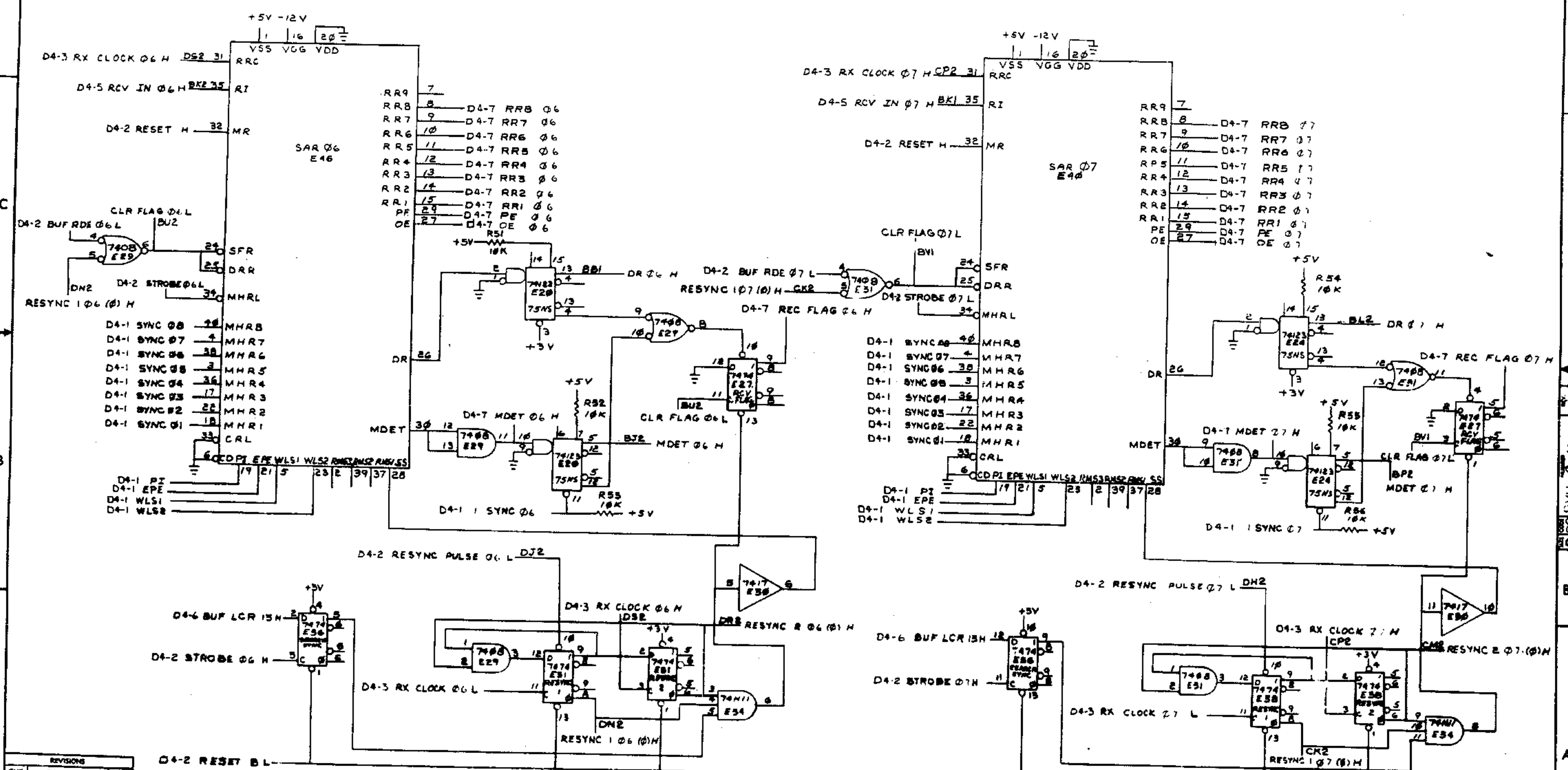
D4-6 BUF LCR 13 H
D4-2 STROBE Ø5 H
74174 E60 SEARCH SYNC
D4-2 RESYNC PULSE Ø5 L DK2
+5V
D4-3 RX CLOCK Ø5 H CE2
74ØB E35
74174 E52 RESYNC
D4-3 RX CLOCK Ø5 L
BH2 RESYNC 1 Ø5 (Ø) H
7417 E30
CF2 RESYNC 2 Ø5 (Ø) H
74H11 E34

(RECEIVERS Ø4 AND Ø5, RESYNC)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø4 - Ø7 (Ø4-6)	D	BS	DV11-Ø-11	
SCALE	SHEET 6 OF 8		DWG.	

CUSTOMER DHS

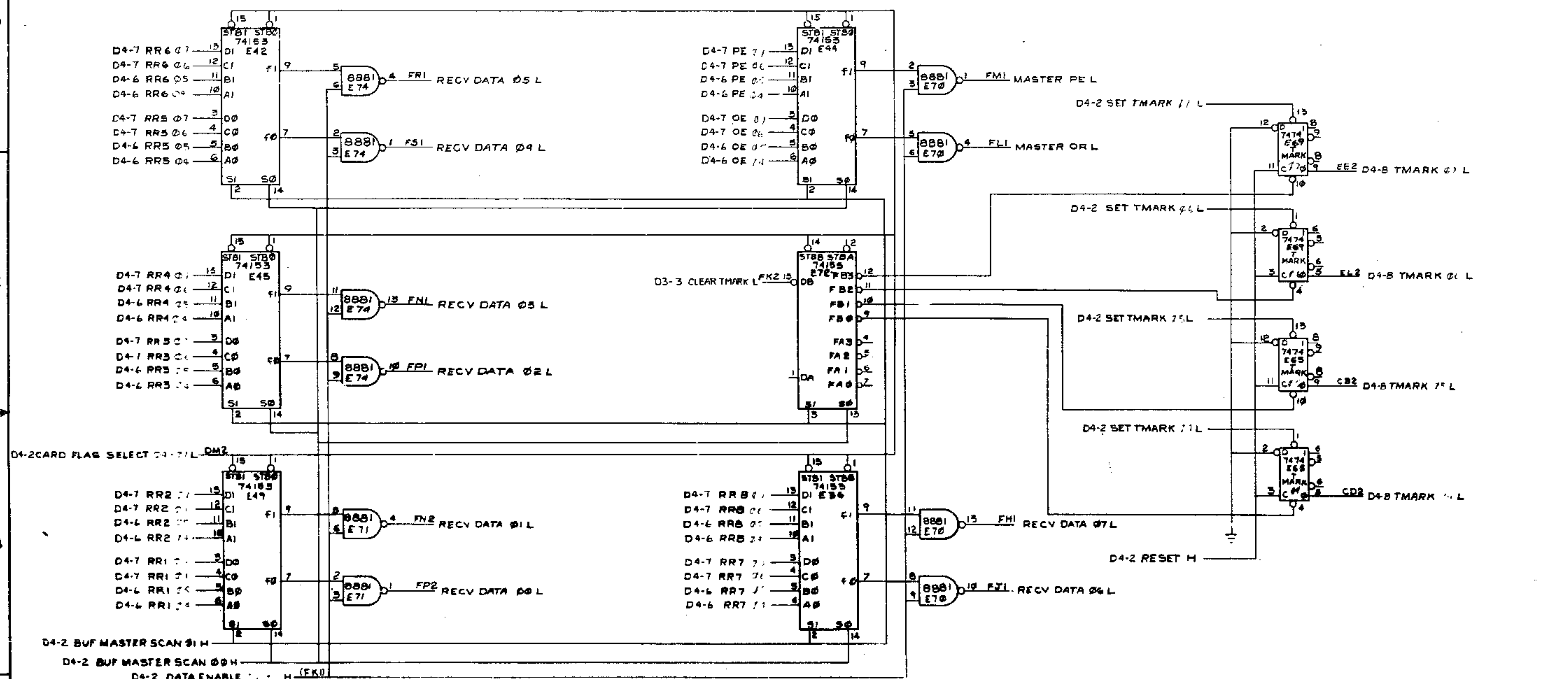


(RECEIVERS Ø6 AND Ø7, RESYNC)

TITLE SYNC MUX LINE CARD LINES Ø6-Ø7 (D4-7)

SIZE D CODE BS NUMBER DV11-Ø-11

SHEET 7 OF 8



(RECV DATA MUXS AND TMARK DECODER)

TITLE SYNC MUX LINE CARD LINES 24-27	SIZE D	CODE BS	NUMBER DV11-Ø-11
SCALE	SHEET 6 OF 6		

REVISIONS: CHK | CHANGE NO. | REV.

BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR 08
C	GROUND
D	DCE SCR 09
E	GROUND
F	DCE SCR 10
H	GROUND
J	DCE SCR 11
K	GROUND
L	EIA RCV DATA 08
M	GROUND
N	EIA RCV DATA 09
P	GROUND
R	EIA XMIT DATA 08
S	GROUND
T	EIA XMIT DATA 09
U	GROUND
V	DTE SCTE 09
W	GROUND
X	DTE SCTE 09
Y	DTE SCTE 10
Z	GROUND
A A	DTE SCTE 11
B B	GROUND
C C	EIA XMIT DATA 10
D D	GROUND
E E	EIA XMIT DATA 11
F F	GROUND
H H	EIA RCV DATA 10
J J	GROUND
K K	EIA RCV DATA 11
L L	GROUND
M M	DCE SCT 11
N N	GROUND
P P	DCE SCT 10
R R	GROUND
S S	DCE SCT 09
T T	GROUND
U U	DCE SCT 08
V V	GROUND

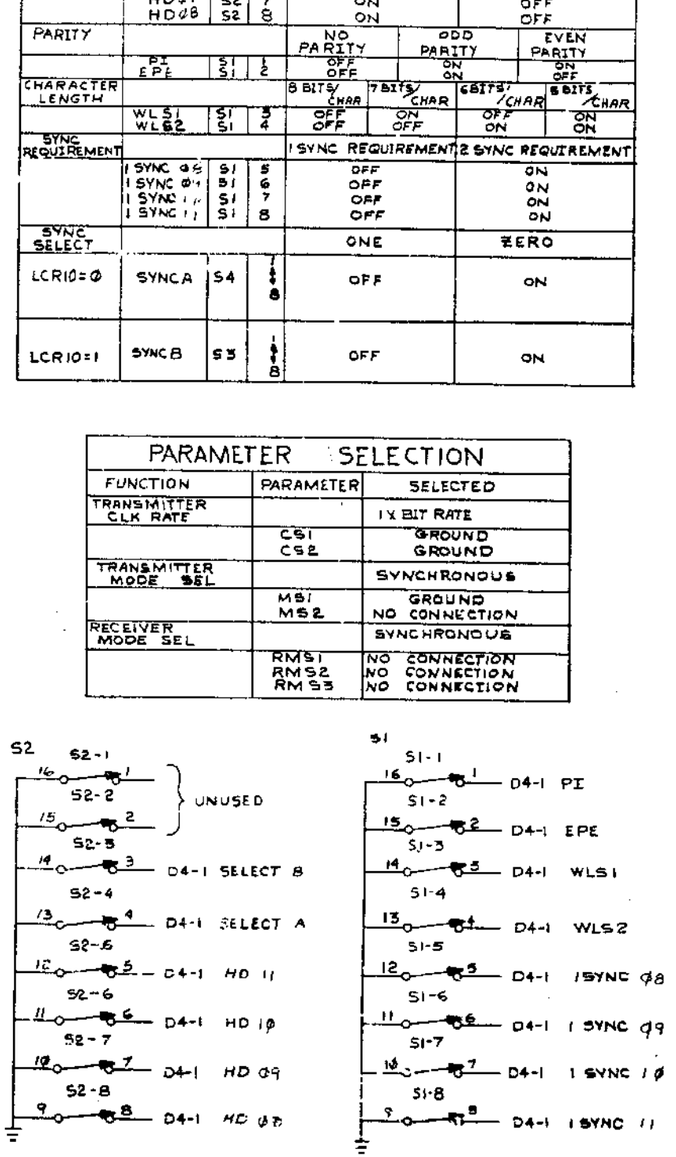
PARAMETER SWITCH SETTINGS

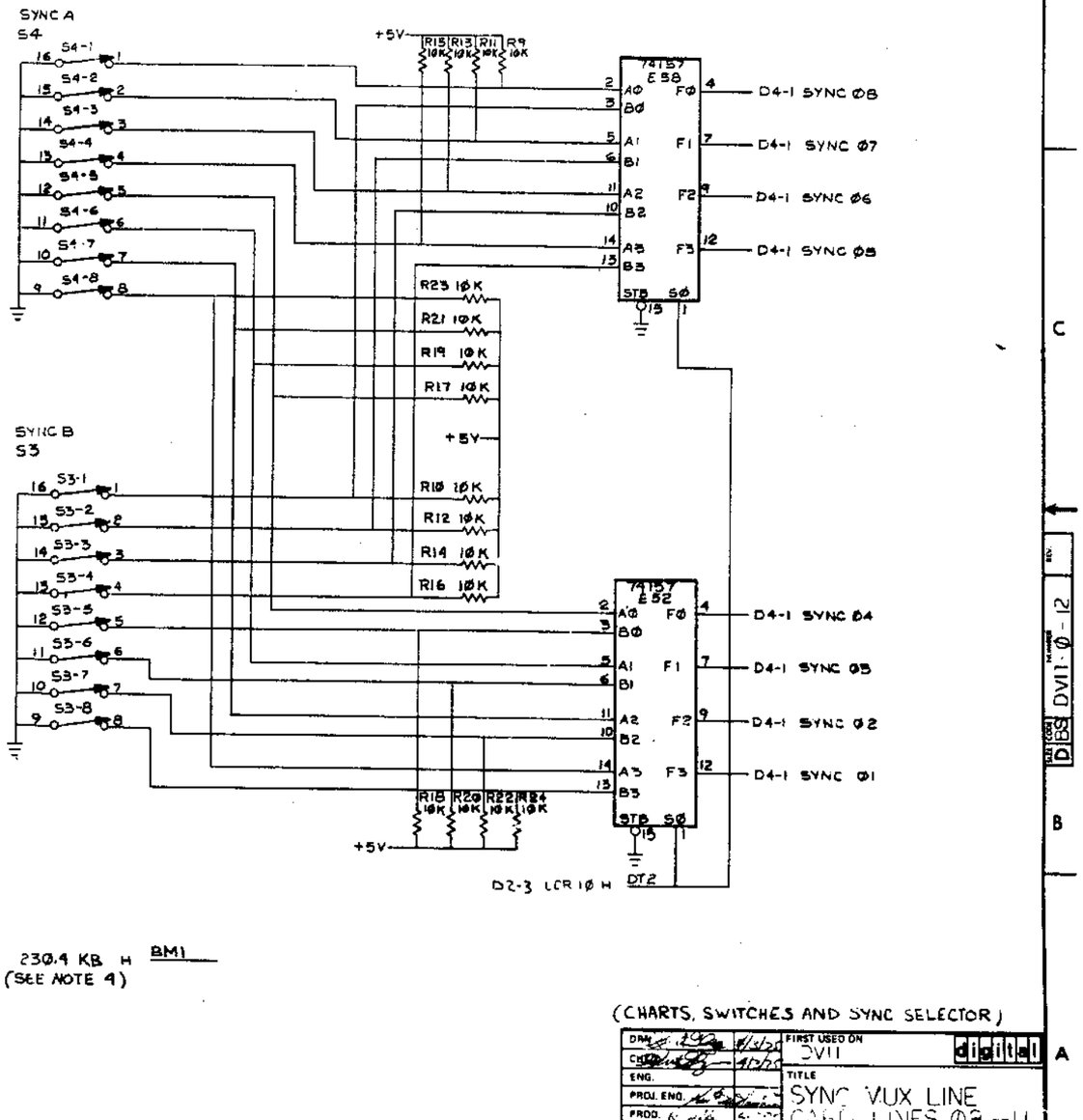
FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B SELECT A	S2 S2	3 4	ON ON	ON OFF	OFF ON	OFF OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HD HD10 HD09 HD08	S2 S2 S2 S2	5 6 7 8	ON ON ON ON		OFF OFF OFF OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI EPE	S1 S1	1 2	OFF OFF	ON ON	ON OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1 WLS2	S1 S1	3 4	OFF OFF	ON OFF	OFF ON	ON ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC 08 1 SYNC 09 1 SYNC 10 1 SYNC 11	S1 S1 S1 S1	5 6 7 8	OFF OFF OFF OFF		ON ON ON ON	
SYNC SELECT				ONE		ZERO	
LCR10=0	SYNC A	S4	1 ↕ 8	OFF		ON	
LCR10=1	SYNC B	S3	1 ↕ 8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1 CS2	GROUND GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1 MS2	GROUND NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1 RMS2 RMS3	NO CONNECTION NO CONNECTION NO CONNECTION

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA 08 H. NO M7813 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.





(CHARTS, SWITCHES AND SYNC SELECTOR)

REVISIONS		
CHK	CHANGE NO.	REV.

DRN		
CHK		
ENG.		
PROJ. ENG.		
PROD.		
NEXT HIGHER ASSY.		
R-DD-DVII-0		
SCALE		
SHEET 1 OF 8		

FIRST USED ON: DVII

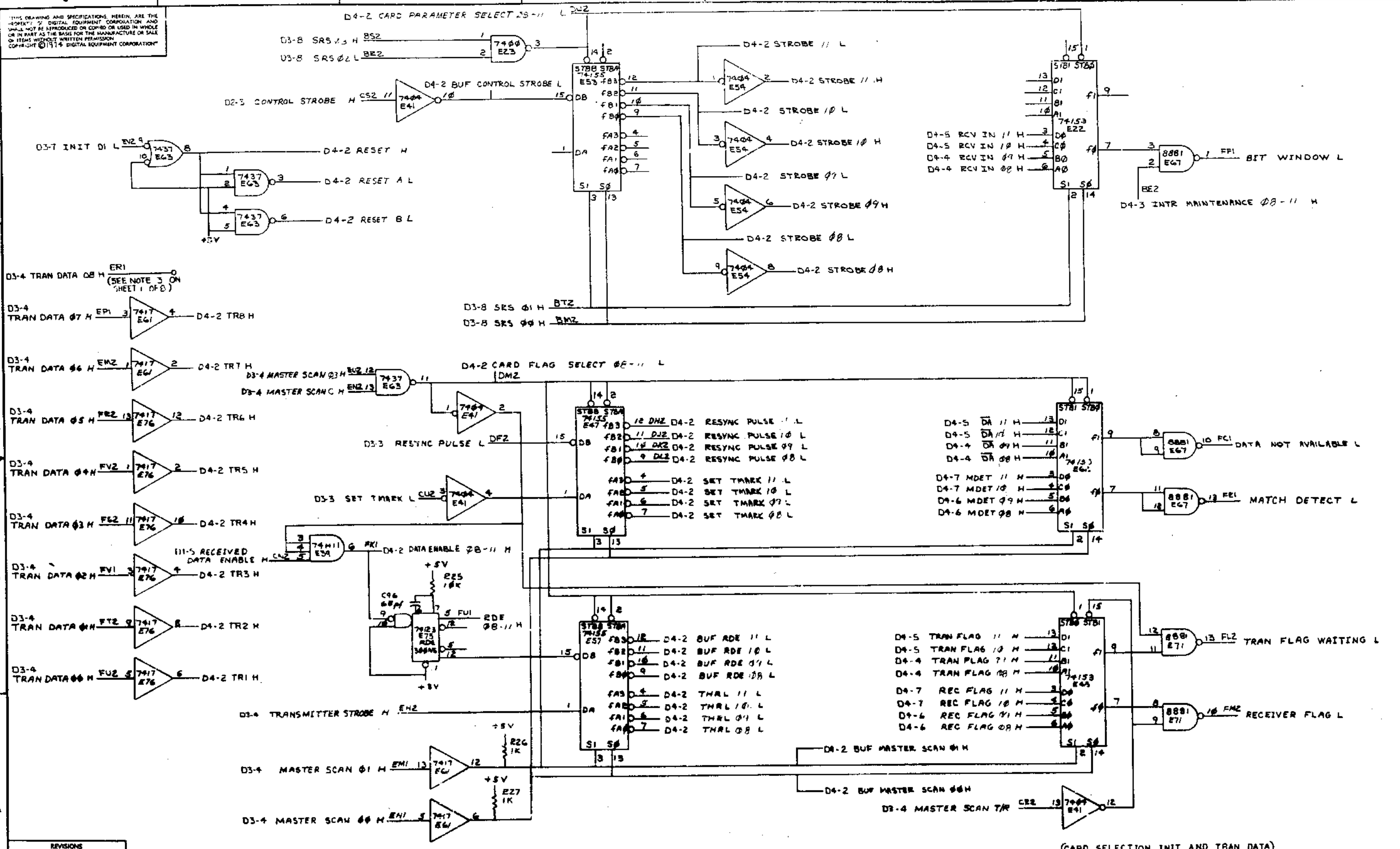
digital

TITLE: SYNC VUX LINE CARD LINES 08 -- 11 (D4-1)

SIZE	CODE	NUMBER	REV.
D	BS	DVII-0-12	

DIST.

DBS DVII-0-12



(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE SYNC MUX LINE CARD LINES Ø8-11 (D4-2)

SIZE D | CODE HS | NUMBER DV11-Ø-12 | REV.

SCALE | SHEET 2 OF 8

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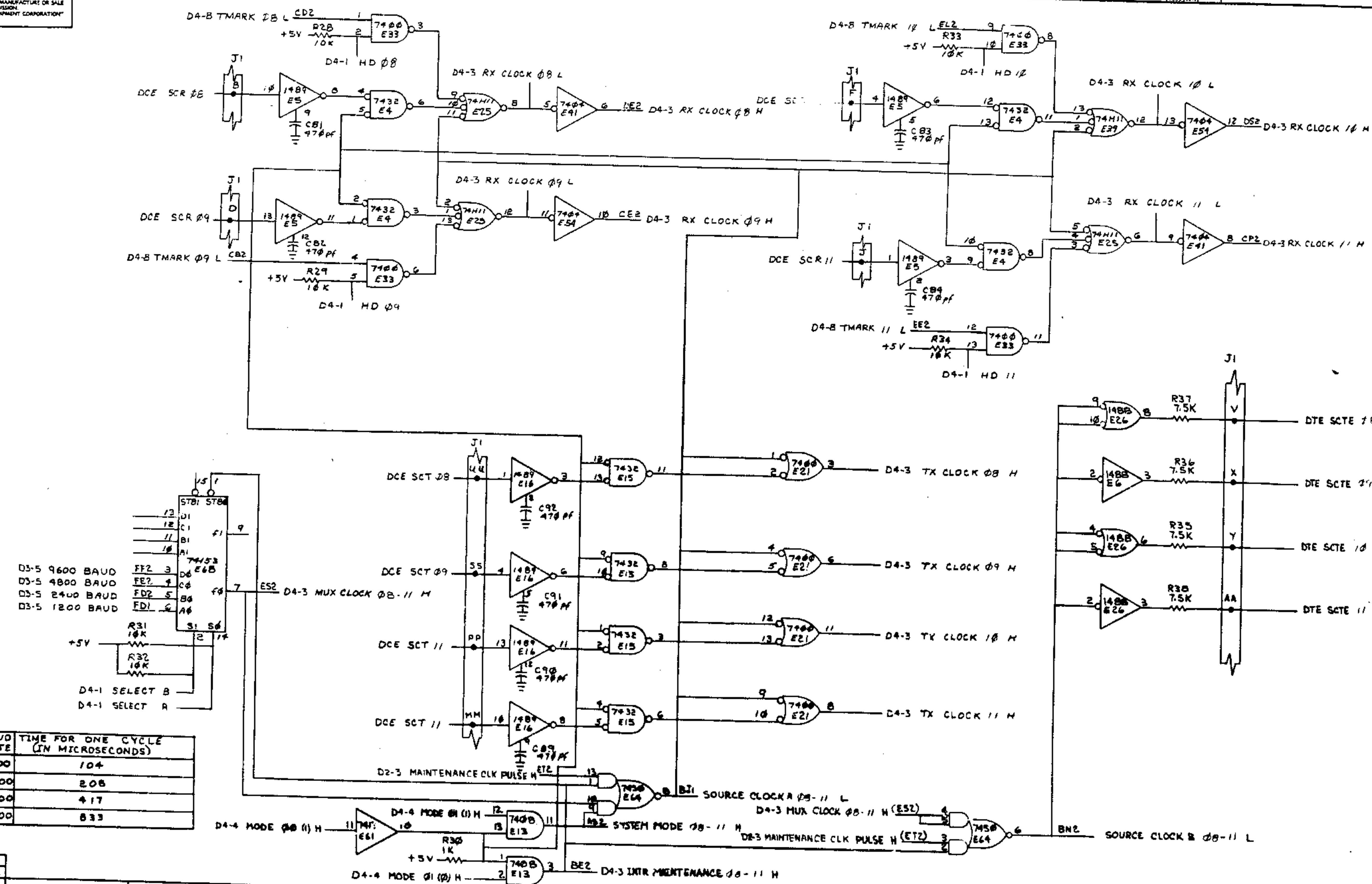


BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

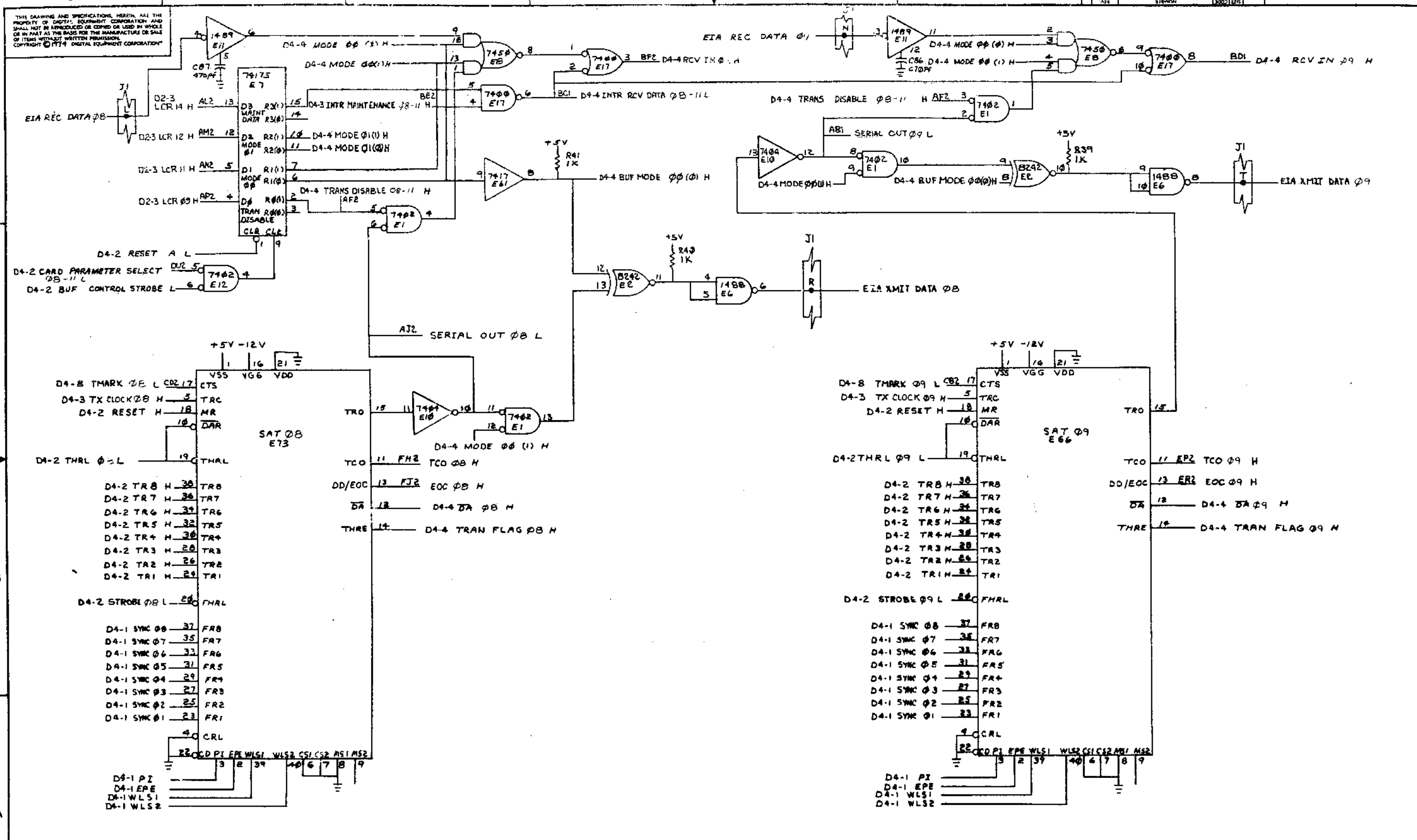
REVISIONS		
CHK	CHANGE NO.	REV.

(CLOCK SOURCE AND SELECTION)

TITLE SYNC MUX LINE CARD LINES Ø8-11 (D4-3)

SIZE D CODE BS NUMBER DV11-Ø-12 REV.

SCALE — SHEET 3 OF 8



(MODE SELECTION, TRANSMITTERS Ø8 AND Ø9)

TITLE SYNC MUX LINE CARD LINES Ø8-11 (D4-4)

SIZE D CODE ES NUMBER DV11-Ø-12

SHEET 4 OF 8

EIA REC DATA Ø — J1 HH — 1489 E11 — C85 47Øpf

D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9 — 7400 E23 — BK2 — D4-5 RCV IN Ø H

D4-4 TRANS DISABLE ØB-11 H (AF2) — 7402 E12

D4-4 INTR RCV DATA ØB-11 L — BC1

D4-4 BUF MODE ØØ (Ø) H — +5V R42 1K — 8242 E2 — 1488 E6 — J1 CC — EIA XMIT DATA Ø

D4-4 MODE ØØ (1) H — 7402 E12 — 7404 E10 — AT2 — SERIAL OUT Ø L

EIA REC DATA 1 — J1 KK — 1489 E11 — C85 47Øpf

D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9 — 7400 E23 — BK1 — D4-5 RCV IN 1 H

D4-4 BUF MODE ØØ (Ø) H — +5V R43 1K — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA 1

D4-4 MODE ØØ (1) H — 7402 E8 — (AF2) D4-4 TRANS DISABLE ØB-11 H

+5V -12V — VSS VGG VDD — SAT Ø E59

D4-8 TMARK Ø L EL2 17 CTS
D4-3 TX CLOCK Ø H 5 TRC
D4-2 RESET H 18 MR
10 DAR
D4-2 THRL Ø L 19 THRL
D4-2 TRB H 38 TR8
D4-2 TR7 H 36 TR7
D4-2 TR6 H 34 TR6
D4-2 TR5 H 32 TR5
D4-2 TR4 H 30 TR4
D4-2 TR3 H 28 TR3
D4-2 TR2 H 26 TR2
D4-2 TR1 H 24 TR1
D4-2 STROBE Ø L EL6 FHRL
D4-1 SYNC Ø8 37 FR8
D4-1 SYNC Ø7 35 FR7
D4-1 SYNC Ø6 33 FR6
D4-1 SYNC Ø5 31 FR5
D4-1 SYNC Ø4 29 FR4
D4-1 SYNC Ø3 27 FR3
D4-1 SYNC Ø2 25 FR2
D4-1 SYNC Ø1 23 FR1
4 CRL
EE CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

TRO 15
TCO 11 EJ2 TCO Ø H
DD/EOC 13 EK2 EOC Ø H
DA 12 D4-5 DA Ø H
THRE 14 D4-5 TRAN FLAG Ø H

+5V -12V — VSS VGG VDD — SAT 1 E58

D4-8 TMARK 11 L EE2 17 CTS
D4-3 TX CLOCK 11 H 5 TRC
D4-2 RESET H 18 MR
10 DAR
D4-2 THRL 11 L 19 THRL
D4-2 TR8 H 38 TR8
D4-2 TR7 H 36 TR7
D4-2 TR6 H 34 TR6
D4-2 TR5 H 32 TR5
D4-2 TR4 H 30 TR4
D4-2 TR3 H 28 TR3
D4-2 TR2 H 26 TR2
D4-2 TR1 H 24 TR1
D4-2 STROBE 11 L EE6 FHRL
D4-1 SYNC Ø8 37 FR8
D4-1 SYNC Ø7 35 FR7
D4-1 SYNC Ø6 33 FR6
D4-1 SYNC Ø5 31 FR5
D4-1 SYNC Ø4 29 FR4
D4-1 SYNC Ø3 27 FR3
D4-1 SYNC Ø2 25 FR2
D4-1 SYNC Ø1 23 FR1
4 CRL
EE CD PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2
3 2 39 40 6 7 8 9
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2

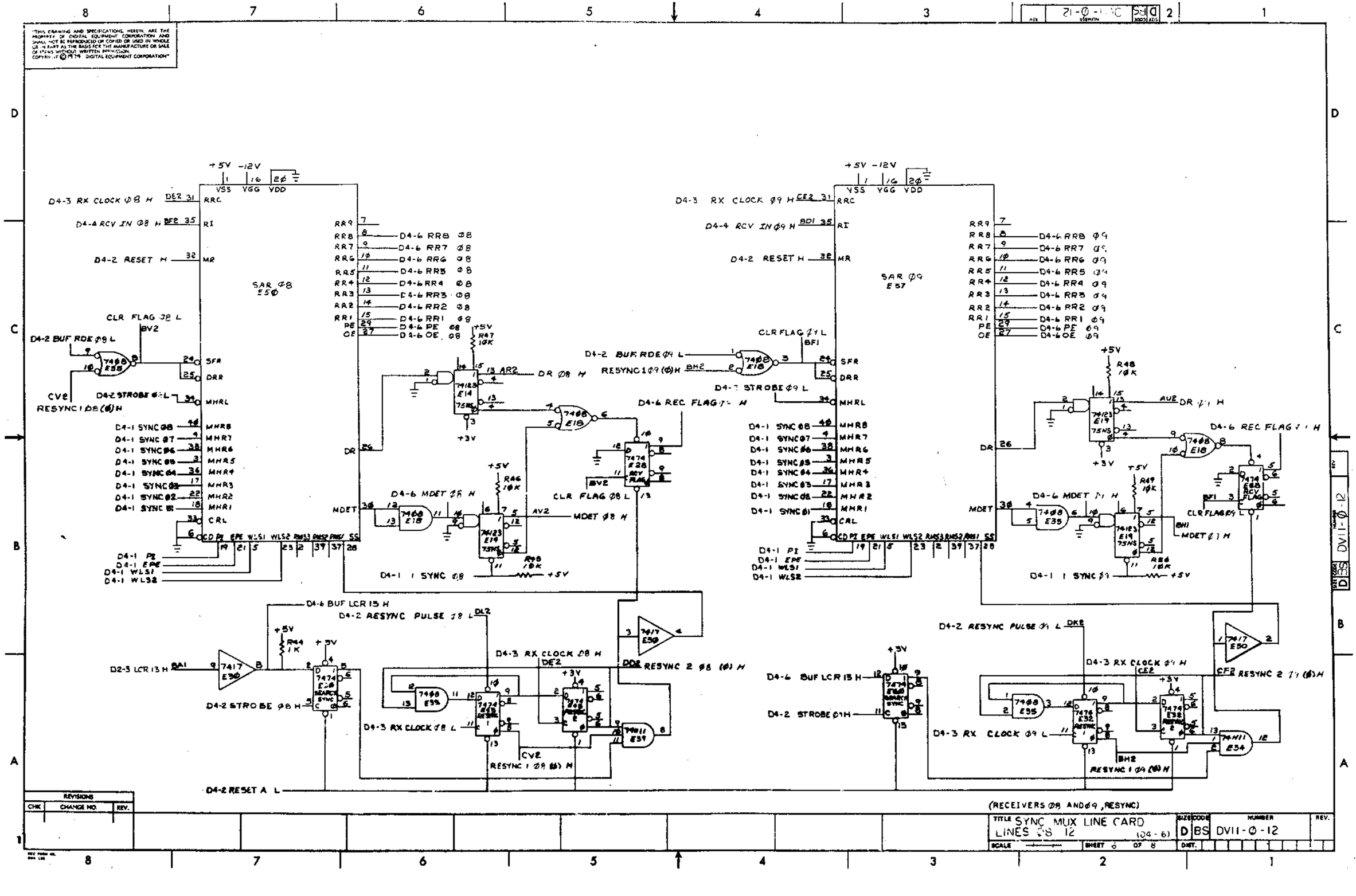
TRO 15 — 7404 E10 — 8 AH2 — SERIAL OUT 11 L
TCO 11 ED2 TCO 11 H
DD/EOC 13 EF2 EOC 11 H
DA 12 D4-5 DA 11 H
THRE 14 D4-5 TRAN FLAG 11 H

REVISIONS

CHK	CHANGE NO.	REV.

(TRANSMITTERS Ø AND 1)

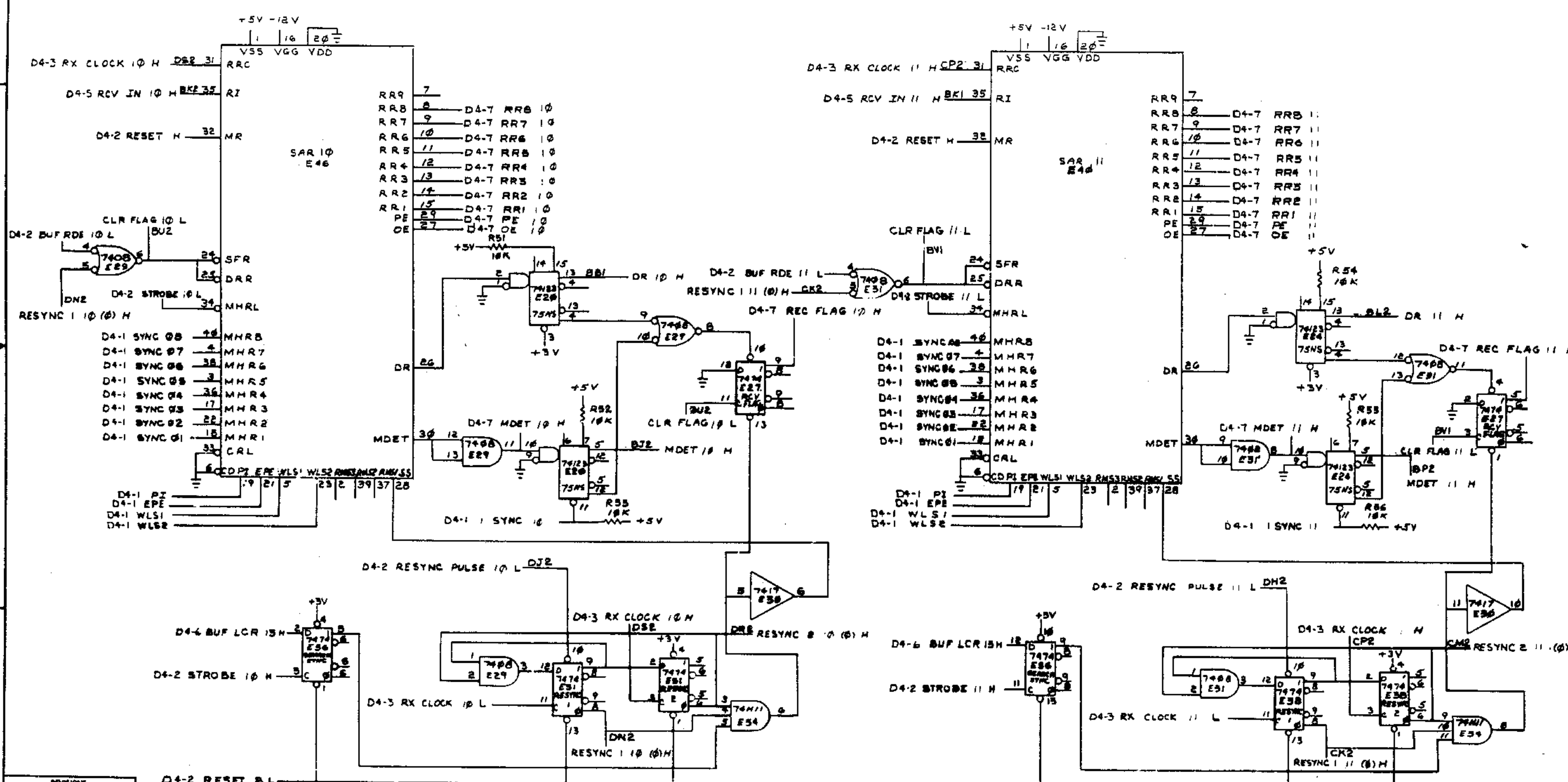
TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø8-11 (D4-5)	D	BS	DV11-Ø-12	
SCALE	SHEET 5 OF 8		DIST.	



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES Ø8 12 (Ø4-6)	D	BS	DV11-Ø-12	
SCALE	SHEET 6 OF 8		DWG.	

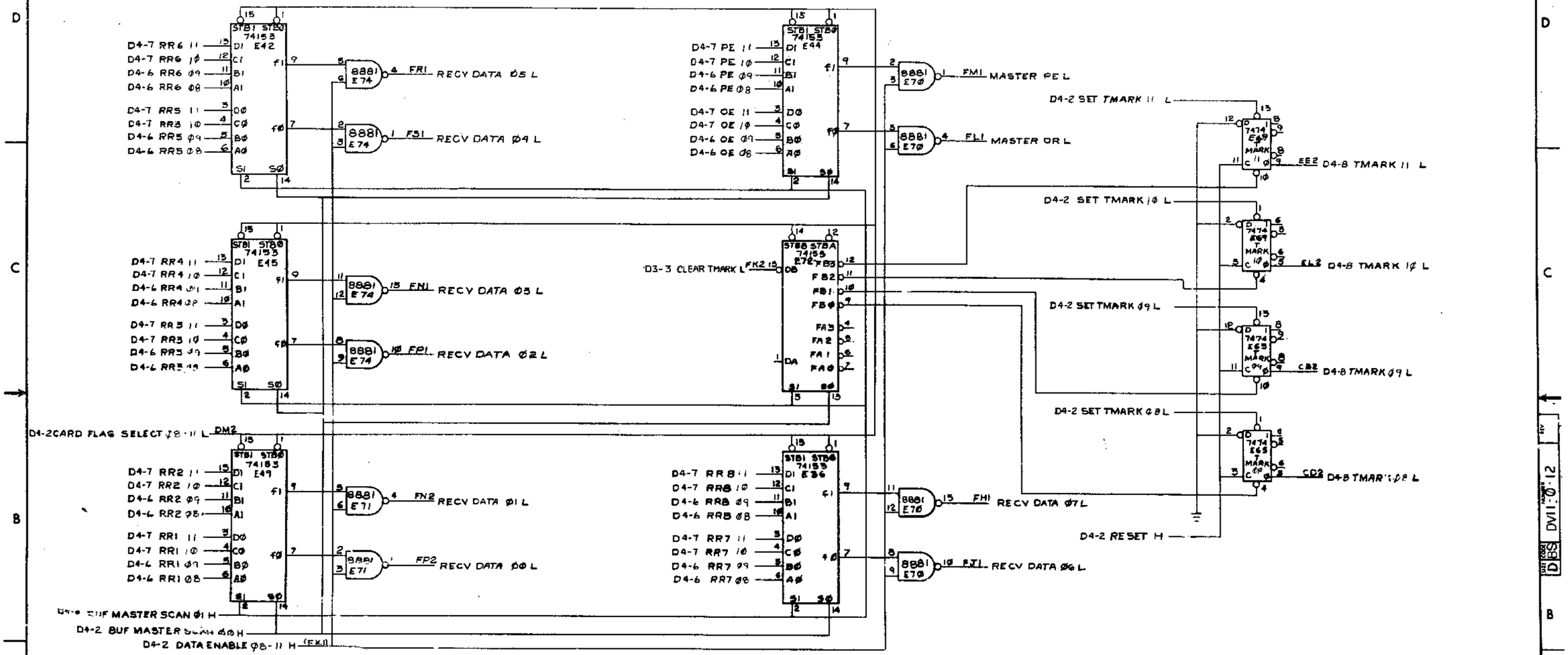
DES DV11-Ø-12



(RECEIVERS 10 AND 11, RESYNC)

TITLE	SYNC MUX LINE CARD LINES 08-11 (D4-7)
SIZE	D
CODE	BS
NUMBER	DV11-Ø-12
REV.	
SCALE	
SHEET	7 OF 8

REVISIONS		
CHK	CHANGE NO.	REV.



REVISIONS

CHK	CHANGE NO.	REV.

(RECV DATA MUX S AND TMARK DECODER)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES 2-11 (D4-8)	D	BS	DV11-0-12	

SCALE — SHEET 8 OF 8 — DIST.

BERG PINNING CHART

J1	SIGNAL
A	GROUND
B	DCE SCR 12
C	GROUND
D	DCE SCR 13
E	GROUND
F	DCE SCR 14
H	GROUND
J	DCE SCR 15
K	GROUND
L	EIA RCV DATA 2
M	GROUND
N	EIA RCV DATA 13
P	GROUND
R	EIA XMIT DATA 12
S	GROUND
T	EIA XMIT DATA 13
U	GROUND
V	DTE SCTE 12
W	GROUND
X	DTE SCTE 13
Y	DTE SCTE 14
Z	GROUND
A A	DTE SCTE 15
B B	GROUND
C C	EIA XMIT DATA 14
D D	GROUND
E E	EIA XMIT DATA 15
F F	GROUND
H H	EIA RCV DATA 14
J J	GROUND
K K	EIA RCV DATA 15
L L	GROUND
M M	DCE SCT 15
N N	GROUND
P P	DCE SCT 14
R R	GROUND
S S	DCE SCT 13
T T	GROUND
U U	DCE SCT 12
V V	GROUND

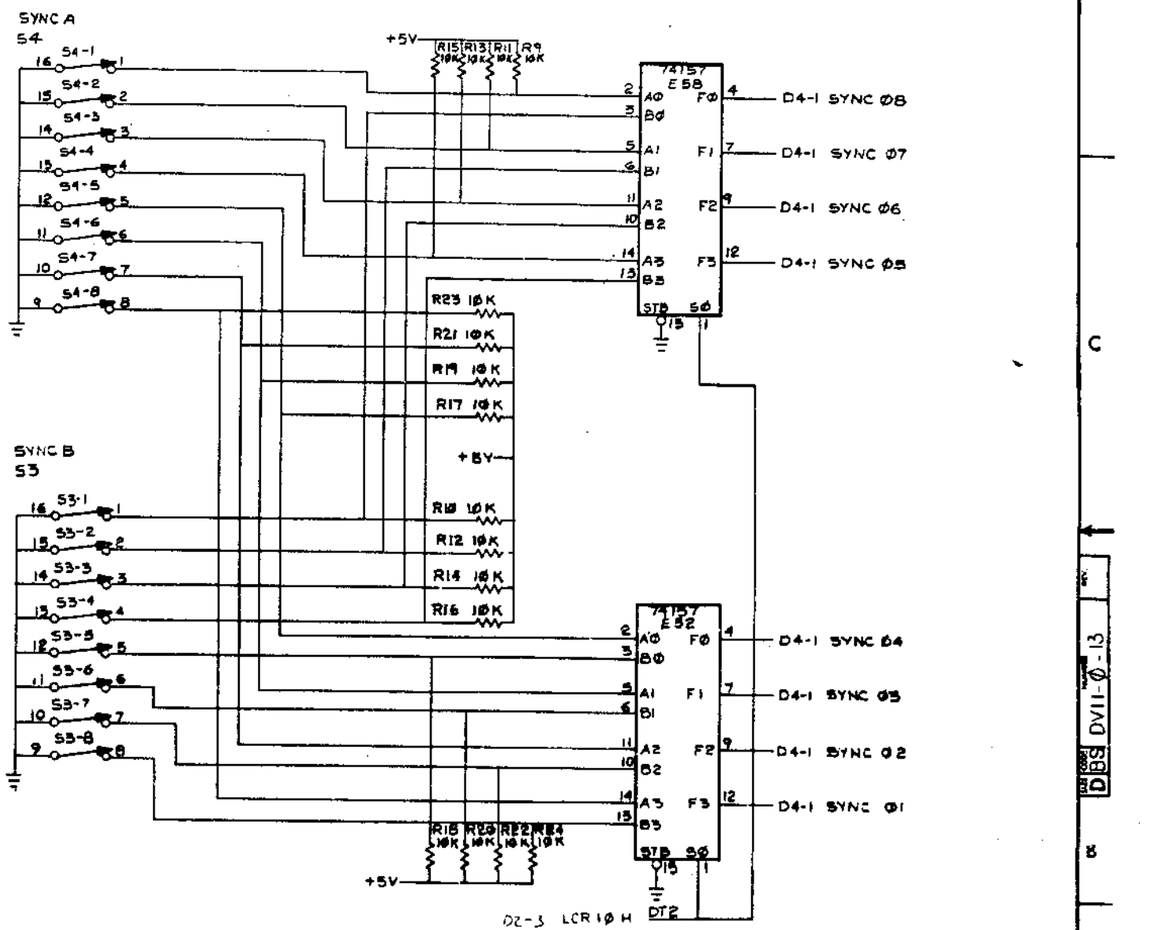
PARAMETER SWITCH SETTINGS

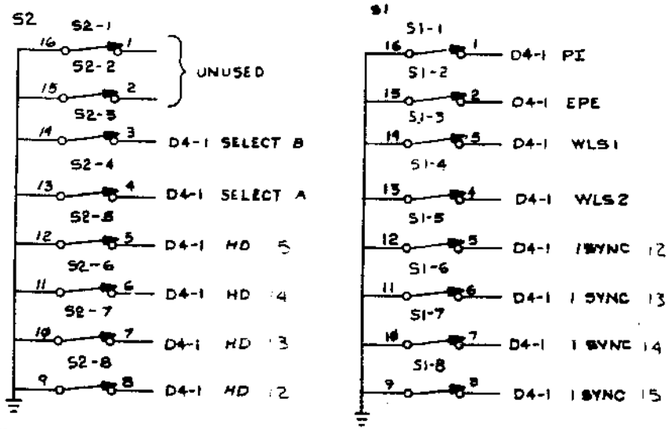
FUNCTION	SWITCH NAME	SW PACK	SW NO	PARAMETER/SETTING			
INTERNAL BAUD RATE				1200 BAUD	2400 BAUD	4800 BAUD	9600 BAUD
	SELECT B SELECT A	S2 S2	3 4	ON ON	ON OFF	OFF ON	OFF OFF
FULL / HALF DUPLEX				FULL DUPLEX		HALF DUPLEX	
	HD 15 HD 14 HD 13 HD 12	S2 S2 S2 S2	5 6 7 8	ON ON ON ON		OFF OFF OFF OFF	
PARITY				NO PARITY	ODD PARITY	EVEN PARITY	
	PI EPE	S1 S1	1 2	OFF OFF	ON ON	ON OFF	
CHARACTER LENGTH				8 BITS/CHAR	7 BITS/CHAR	6 BITS/CHAR	5 BITS/CHAR
	WLS1 WLS2	S1 S1	3 4	OFF OFF	ON OFF	OFF ON	ON ON
SYNC REQUIREMENT				1 SYNC REQUIREMENT		2 SYNC REQUIREMENT	
	1 SYNC 12 1 SYNC 13 1 SYNC 14 1 SYNC 15	S1 S1 S1 S1	5 6 7 8	OFF OFF OFF OFF		ON ON ON ON	
SYNC SELECT				ONE		ZERO	
LCR10=0	SYNC A	S4	1 ↕ 8	OFF		ON	
LCR10=1	SYNC B	S3	1 ↕ 8	OFF		ON	

PARAMETER SELECTION

FUNCTION	PARAMETER	SELECTED
TRANSMITTER CLK RATE		1X BIT RATE
	CS1 CS2	GROUND GROUND
TRANSMITTER MODE SEL		SYNCHRONOUS
	MS1 MS2	GROUND NO CONNECTION
RECEIVER MODE SEL		SYNCHRONOUS
	RMS1 RMS2 RMS3	NO CONNECTION NO CONNECTION NO CONNECTION

NOTES:
1. SWITCHES ARE MOUNTED FOR "OFF" TO THE LEFT AND "ON" TO THE RIGHT
2. FOR SYNC A OR SYNC B SELECTION S4-1 AND S3-1 RESPECTIVELY ARE THE MOST SIGNIFICANT BITS
3. PIN ER1 IS AN ASSIGNED BACKPLANE SIGNAL, TRAN DATA Ø8 H. NO M7820 CIRCUITRY IS CONNECTED TO IT.
4. PIN BM1 IS AN ASSIGNED BACKPLANE SIGNAL, 230.4KBH. NO M7839 CIRCUITRY IS CONNECTED TO IT.





REVISIONS		
CHK	CHANGE NO.	REV.

(CHARTS, SWITCHES AND SYNC SELECTOR)

DRN	FIRST USED ON: DV11
CHK'D	digital
ENG.	TITLE: SYNC MUX LINE CARD LINES 12 - 15
PROJ ENG.	(D4-1)
PROD	
NEXT HIGHER ASSY.	
E DD DV11 Ø	SIZE D, CODE BS, NUMBER DV11-Ø-13, REV.
SCALE	
SHEET 1 OF 8	DIST.

D4-2 CARD PARAMETER SELECT 12 - 15 L DU2

D3-8 SRS Ø3 H BS2 — 7400 E23

D3-8 SRS Ø2 H BE2

D2-3 CONTROL STROBE H CS2 — 7404 E41 — D4-2 BUF CONTROL STROBE L

STBB STBA 74155 E53 — FB3 FB2 FB1 FB0 — FA3 FA2 FA1 FA0 — S1 SØ — DA DB

D4-2 STROBE 15 L — 7404 E59 — D4-2 STROBE 15 H

D4-2 STROBE 14 L — 7404 E54 — D4-2 STROBE 14 H

D4-2 STROBE 13 L — 7404 E54 — D4-2 STROBE 13 H

D4-2 STROBE 12 L — 7404 E54 — D4-2 STROBE 12 H

D3-8 SRS Ø1 H BT2

D3-8 SRS ØØ H BM2

D3-7 INIT DI L EV2 — 7437 E63 — D4-2 RESET H

7437 E63 — D4-2 RESET A L

7437 E63 — D4-2 RESET B L

+3V

STBI STBØ 74153 E22 — D1 C1 B1 A1 — DØ CØ BØ AØ — S1 SØ — FI FØ

D4-5 RCV IN 15 H
D4-5 RCV IN 14 H
D4-4 RCV IN 13 H
D4-4 RCV IN 12 H

8881 E61 — FFI — BIT WINDOW L

BE2 — D4-3 INTR MAINTENANCE 12-15 H

D3-4 TRAN DATA ØB H ERI (SEE NOTE 3 ON SHEET 1 OF 5)

D3-4 TRAN DATA Ø7 H EP1 — 7417 E61 — D4-2 TR8 H

D3-4 TRAN DATA Ø6 H EM2 — 7417 E61 — D4-2 TR7 H

D3-4 TRAN DATA Ø5 H FR2 — 7417 E76 — D4-2 TR6 H

D3-4 TRAN DATA Ø4 H FV2 — 7417 E76 — D4-2 TR5 H

D3-4 TRAN DATA Ø3 H FS2 — 7417 E76 — D4-2 TR4 H

D3-4 TRAN DATA Ø2 H FV1 — 7417 E76 — D4-2 TR3 H

D3-4 TRAN DATA Ø1 H FT2 — 7417 E76 — D4-2 TR2 H

D3-4 TRAN DATA ØØ H FU2 — 7417 E76 — D4-2 TR1 H

D4-2 CARD FLAG SELECT 12 - 15 L DM2

D3-4 MASTER SCAN Ø3 H EU2
D3-4 MASTER SCAN Ø2 H EN2 — 7437 E63

7404 E41 — D3-3 RESYNC PULSE L DF2

STBB STBA 74155 E47 — FB3 FB2 FB1 FB0 — FA3 FA2 FA1 FA0 — S1 SØ — DA DB

18 DM2 D4-2 RESYNC PULSE 15 L
11 DJ2 D4-2 RESYNC PULSE 14 L
16 DK2 D4-2 RESYNC PULSE 13 L
9 DL2 D4-2 RESYNC PULSE 12 L

D4-2 SET TMARK 15 L
D4-2 SET TMARK 14 L
D4-2 SET TMARK 13 L
D4-2 SET TMARK 12 L

D3-3 SET TMARK L CU2 — 7404 E41

74H11 E39 — CN2 — FK1 — D4-2 DATA ENABLE 12-15 H

D1-5 RECEIVED DATA ENABLE H

+5V — R25 10K — C96 68pf

74123 E75 RDE 3885NS — FU1 — RDE 12-15 H

+3V

D3-4 TRANSMITTER STROBE H EH2

+5V — R26 1K — D3-4 MASTER SCAN Ø1 H EM1 — 7417 E61

+5V — R27 1K — D3-4 MASTER SCAN ØØ H EN1 — 7417 E61

STBI STBØ 74153 E62 — D1 C1 B1 A1 — DØ CØ BØ AØ — S1 SØ — FI FØ

D4-5 DA 15 H
D4-5 DA 14 H
D4-4 DA 13 H
D4-4 DA 12 H

8881 E67 — FCI — DATA NOT AVAILABLE L

D4-7 MDET 15 H
D4-7 MDET 14 H
D4-6 MDET 13 H
D4-6 MDET 12 H

8881 E67 — FEI — MATCH DETECT L

STBB STBA 74155 E57 — FB3 FB2 FB1 FB0 — FA3 FA2 FA1 FA0 — S1 SØ — DA DB

D4-2 BUF RDE 15 L
D4-2 BUF RDE 14 L
D4-2 BUF RDE 13 L
D4-2 BUF RDE 12 L

D4-2 THRL 15 L
D4-2 THRL 14 L
D4-2 THRL 13 L
D4-2 THRL 12 L

STBI STBØ 74153 E48 — D1 C1 B1 A1 — DØ CØ BØ AØ — S1 SØ — FI FØ

D4-5 TRAN FLAG 15 H
D4-5 TRAN FLAG 14 H
D4-4 TRAN FLAG 13 H
D4-4 TRAN FLAG 12 H

8881 E71 — FLZ — TRAN FLAG WAITING L

D4-7 REC FLAG 15 H
D4-7 REC FLAG 14 H
D4-6 REC FLAG 13 H
D4-6 REC FLAG 12 H

8881 E71 — FMZ — RECEIVER FLAG L

D4-2 BUF MASTER SCAN Ø1 H

D4-2 BUF MASTER SCAN ØØ H

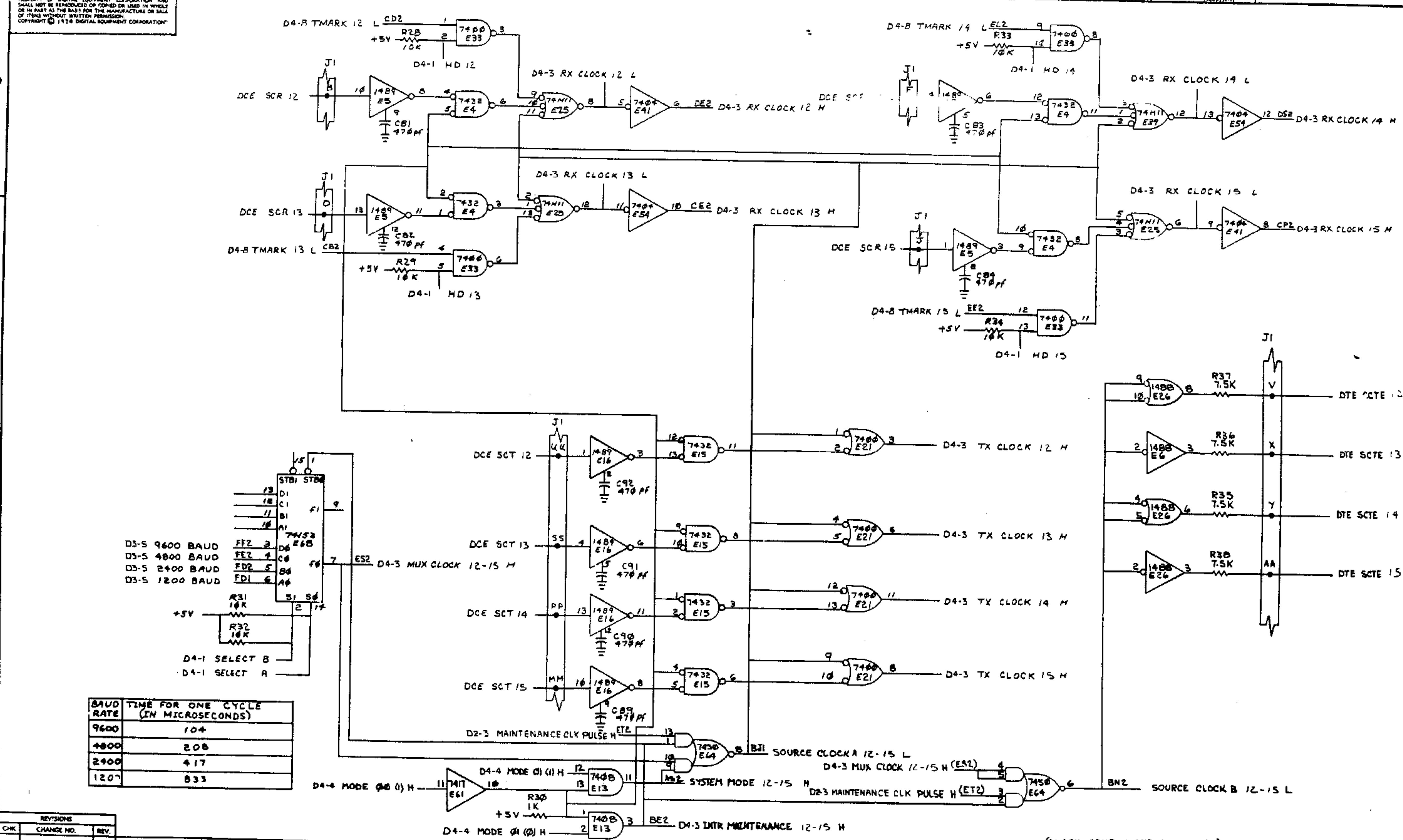
D3-4 MASTER SCAN T/R CR2 — 7404 E41

(CARD SELECTION, INIT AND TRAN DATA)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES 12 15 (D4-2)	D	BS	DV11-Ø-13	

SCALE — SHEET 2 OF 8 — DWG.



BAUD RATE	TIME FOR ONE CYCLE (IN MICROSECONDS)
9600	104
4800	208
2400	417
1200	833

(CLOCK SOURCE AND SELECTION)

TITLE SYNC MUX LINE CARD LINES 12 — 15 (D4-3)

SIZE D CODE BS NUMBER DV11-Ø-13

SHEET 3 OF 8

D4-4 MODE ØØ (Ø) H
D4-4 MODE ØØ (1) H
D4-4 RCV IN 12 H
BE2
BC1
D4-4 INTR RCV DATA 12-15 L
D4-3 INTR MAINTENANCE 12-15 H
D4-4 MODE Ø1(1) H
D4-4 MODE Ø1(Ø) H
D4-4 TRANS DISABLE 12-15 H
D4-4 BUF MODE ØØ (Ø) H
EIA REC DATA 12
EIA XMIT DATA 12
D2-3 LCR 10 H
D2-3 LCR 12 H
D2-3 LCR 11 H
D2-3 LCR Ø9 H
D4-2 RESET A L
D4-2 CARD PARAMETER SELECT 2-15 L
D4-2 BUF CONTROL STROBE L
SERIAL OUT 12 L
+5V -12V
D4-8 TMARK 12 L
D4-3 TX CLOCK 12 H
D4-2 RESET H
D4-2 THRL 12 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE 12 L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
D4-4 MODE ØØ (1) H
TCO 12 H
D4-4 DA 12 H
D4-4 TRAN FLAG 12 H
SAT 12 E73
D4-4 TRANS DISABLE 12-15 H
D4-4 MODE ØØ(Ø)H
D4-4 BUF MODE ØØ(Ø)H
EIA XMIT DATA 13
D4-8 TMARK 13 L
D4-3 TX CLOCK 13 H
D4-2 RESET H
D4-2 THRL 13 L
D4-2 TR8 H
D4-2 TR7 H
D4-2 TR6 H
D4-2 TR5 H
D4-2 TR4 H
D4-2 TR3 H
D4-2 TR2 H
D4-2 TR1 H
D4-2 STROBE 13 L
D4-1 SYNC Ø8
D4-1 SYNC Ø7
D4-1 SYNC Ø6
D4-1 SYNC Ø5
D4-1 SYNC Ø4
D4-1 SYNC Ø3
D4-1 SYNC Ø2
D4-1 SYNC Ø1
D4-1 PI
D4-1 EPE
D4-1 WLS1
D4-1 WLS2
TCO 13 H
EOC 13 H
D4-4 DA 13 H
D4-4 TRAN FLAG 13 H
SAT 13 E66

REVISIONS		
CHK	CHANGE NO.	REV.

(MODE SELECTION, TRANSMITTERS 12 AND 13)

TITLE SYNC MUX LINE CARD LINES 12 - 15 (D4-4)
SIZE D CODE E'S NUMBER DV11-Ø-13 REV.
SCALE SHEET 1 OF 8 DIST.

DV11-Ø-13

EIA REC DATA 14 — J1 HH — 1489 E11 — CB8 470pf

D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9

D4-4 TRANS DISABLE 12-15 H (AF2) — 7402 E12

7400 E23 — BK2 — D4-5 RCV IN 14 H

D4-4 INTR RCV DATA 12-15 L — BC1

D4-4 BUF MODE ØØ (Ø) H, +5V, R42 1K — 8242 E2 — 1488 E6 — J1 CC — EIA XMIT DATA 14

7400 E10 — AT2 — SERIAL OUT 14 L

EIA REC DATA 15 — J1 KK — 1489 E11 — CB5 470pf

D4-4 MODE ØØ (Ø) H, D4-4 MODE ØØ (1) H — 7450 E9 — 7402 E3

(AF2) D4-4 TRANS DISABLE 12-15 H

7400 E23 — BK1 — D4-5 RCV IN 15 H

D4-4 BUF MODE ØØ (Ø) H, +5V, R43 1K — 8242 E2 — 1488 E26 — J1 EE — EIA XMIT DATA 15

D4-4 MODE ØØ (1) H — 7402 E3

+5V -12V — VSS 1, VGG 16, VDD 21

SAT 14 E59

D4-8 TMARK 14 L (EJ2 17) — CTS
D4-3 TX CLOCK 14 H (5) — TRC
D4-2 RESET H (18) — MR
(10) — DAR
D4-2 THRL 14 L (19) — THRL
D4-2 TR8 H (38) — TR8
D4-2 TR7 H (36) — TR7
D4-2 TR6 H (34) — TR6
D4-2 TR5 H (32) — TR5
D4-2 TR4 H (30) — TR4
D4-2 TR3 H (28) — TR3
D4-2 TR2 H (26) — TR2
D4-2 TR1 H (24) — TR1
D4-2 STROBE 14 L (26) — FHRL
D4-1 SYNC Ø8 (37) — FR8
D4-1 SYNC Ø7 (35) — FR7
D4-1 SYNC Ø6 (33) — FR6
D4-1 SYNC Ø5 (31) — FR5
D4-1 SYNC Ø4 (29) — FR4
D4-1 SYNC Ø3 (27) — FR3
D4-1 SYNC Ø2 (25) — FR2
D4-1 SYNC Ø1 (23) — FR1
(4) — CRL
(22) — CO PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 (3 2 39 40 6 7 8 9)
D4-1 PI, D4-1 EPE, D4-1 WLS1, D4-1 WLS2

TRO (15) — TCO (11 EJ2) — TCO 14 H
DD/EOC (13 EK2) — EOC 14 H
DA (12) — D4-5 DA 14 H
THRE (14) — D4-5 TRAN FLAG 14 H

SAT 15 E55

D4-8 TMARK 15 L (EE2 17) — CTS
D4-3 TX CLOCK 15 H (5) — TRC
D4-2 RESET H (18) — MR
(10) — DAR
D4-2 THRL 15 L (19) — THRL
D4-2 TR8 H (38) — TR8
D4-2 TR7 H (36) — TR7
D4-2 TR6 H (34) — TR6
D4-2 TR5 H (32) — TR5
D4-2 TR4 H (30) — TR4
D4-2 TR3 H (28) — TR3
D4-2 TR2 H (26) — TR2
D4-2 TR1 H (24) — TR1
D4-2 STROBE 15 L (26) — FHRL
D4-1 SYNC Ø8 (37) — FR8
D4-1 SYNC Ø7 (35) — FR7
D4-1 SYNC Ø6 (33) — FR6
D4-1 SYNC Ø5 (31) — FR5
D4-1 SYNC Ø4 (29) — FR4
D4-1 SYNC Ø3 (27) — FR3
D4-1 SYNC Ø2 (25) — FR2
D4-1 SYNC Ø1 (23) — FR1
(4) — CRL
(22) — CO PI EPE WLS1 WLS2 CS1 CS2 MS1 MS2 (3 2 39 40 6 7 8 9)
D4-1 PI, D4-1 EPE, D4-1 WLS1, D4-1 WLS2

TRO (15) — 7404 E10 — AH2. — SERIAL OUT 15 L
TCO (11 EO2) — TCO 15 H
DD/EOC (13 EF2) — EOC 15 H
DA (12) — D4-5 DA 15 H
THRE (14) — D4-5 TRAN FLAG 15 H

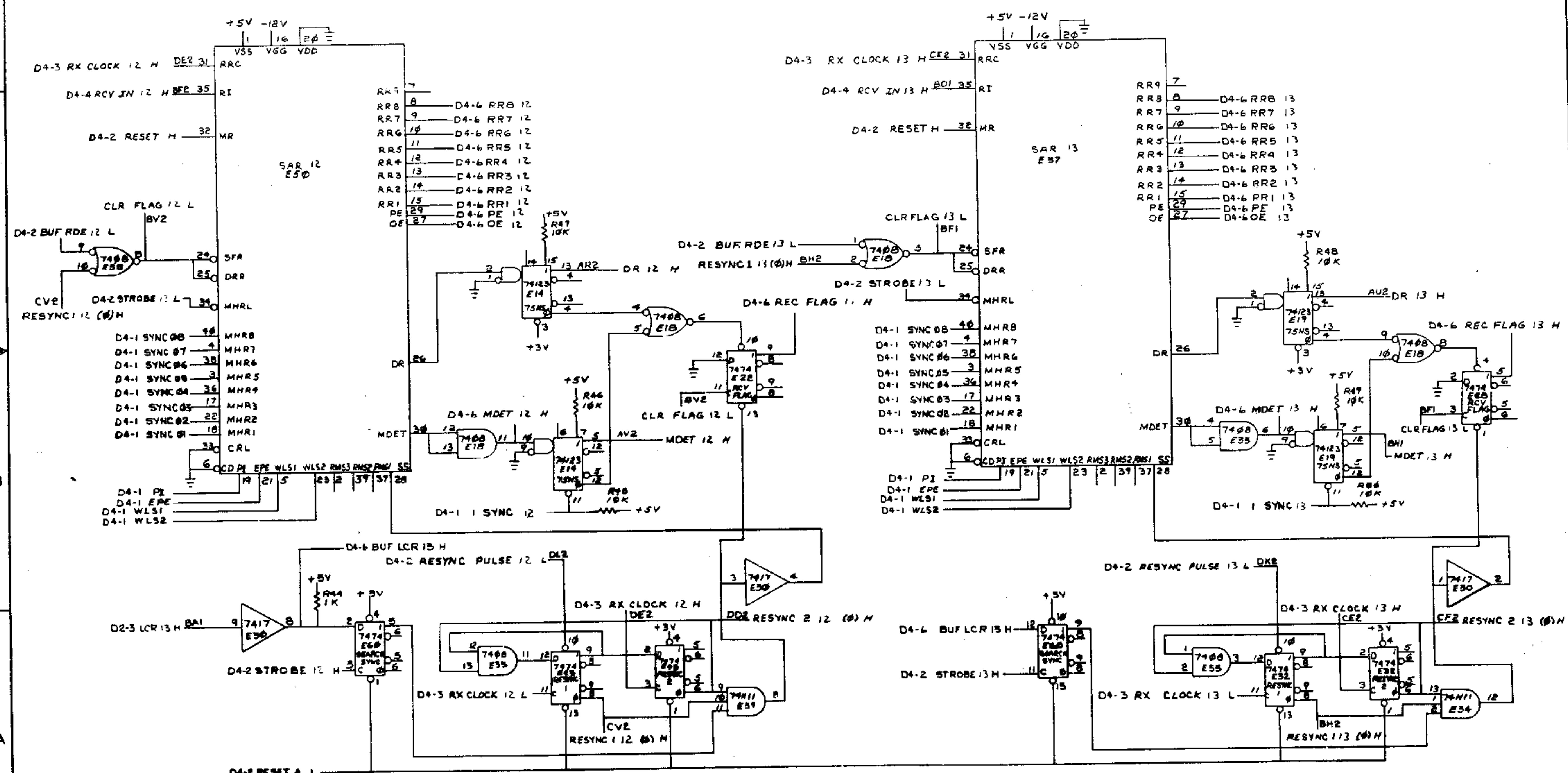
REVISIONS

CHK	CHANGE NO.	REV.

(TRANSMITTERS 14 AND 15)

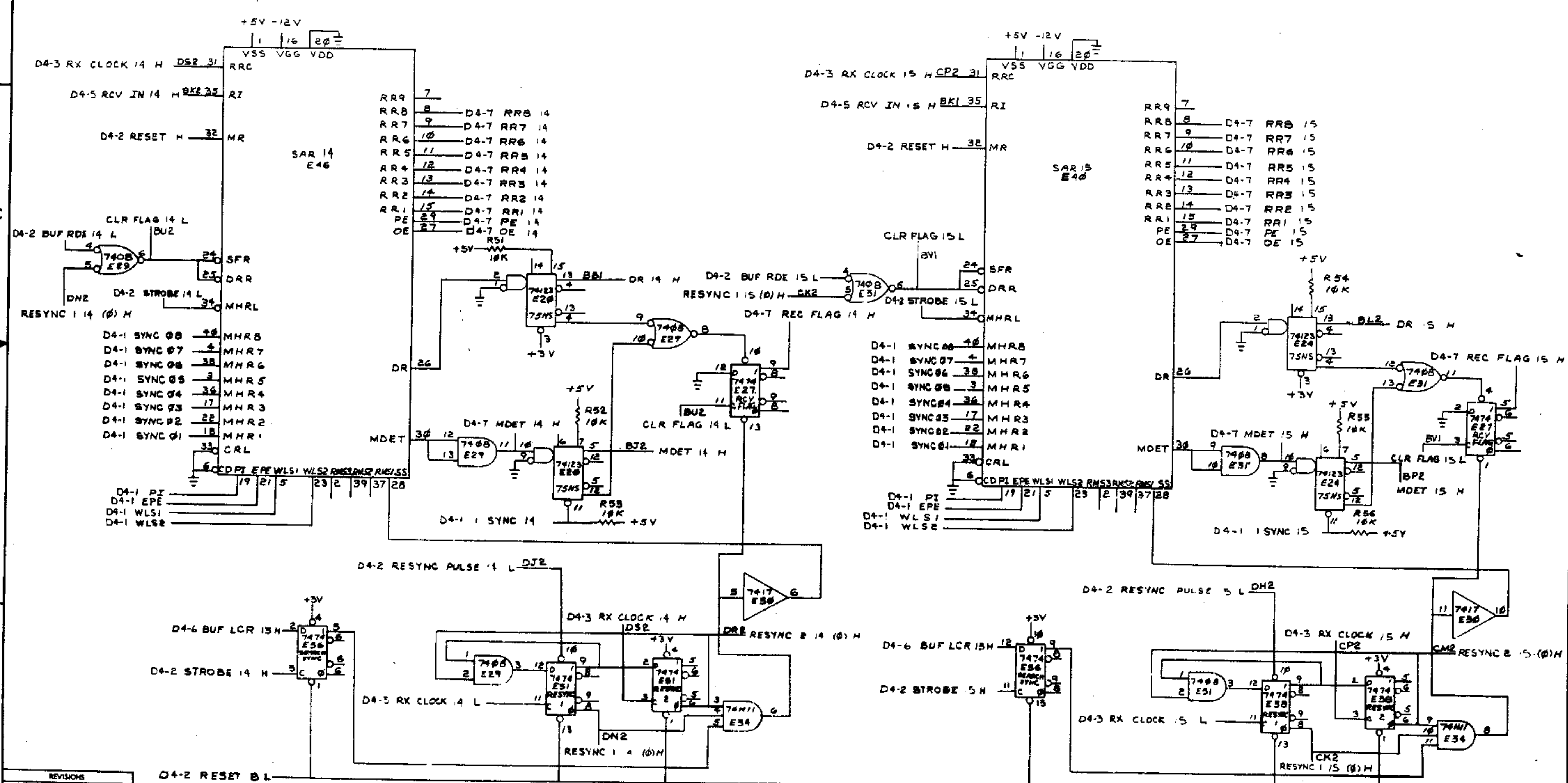
TITLE SYNC MUX LINE CARD LINES 12 - 15 (D4-5)
SIZE D | CODE | DFS | NUMBER DV11-Ø-13 | REV.
SCALE | SHEET 5 OF 8 | DIST.

DFS DV11-Ø-13 REV.



(RECEIVERS 12 AND 13, RESYNC)

TITLE	SYNC MUX LINE CARD LINES 12 - 15 (D4-6)
SIZE	D
CODE	BS
NUMBER	DV11-Ø-13
SHEET	6 OF 8

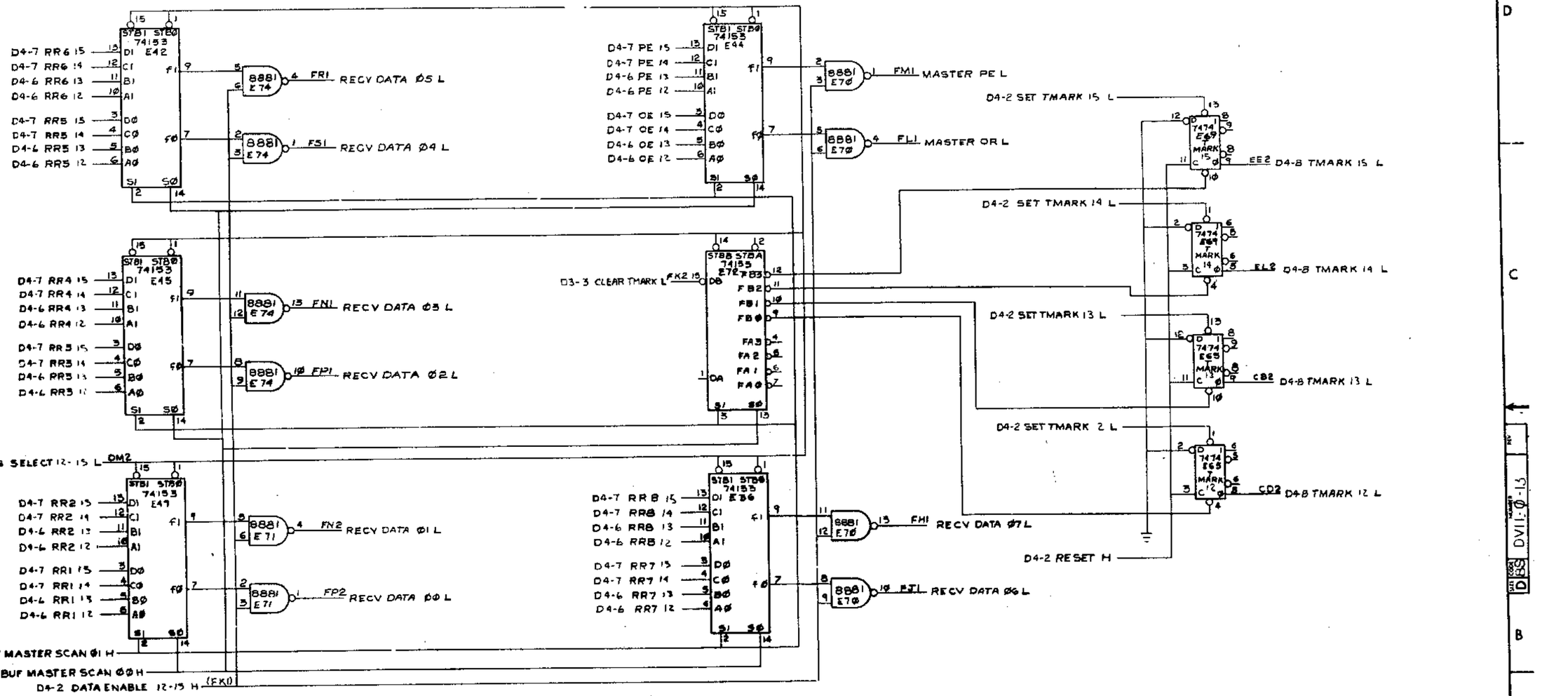


(RECEIVERS 14 AND 15, RESYNC)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES 12 - 15 (D4-7)	D	BS	DV11-Ø-13	

SCALE — SHEET 7 OF 8

REVISIONS		
CHK	CHANGE NO.	REV.



REVISIONS		
CHK	CHANGE NO.	REV.

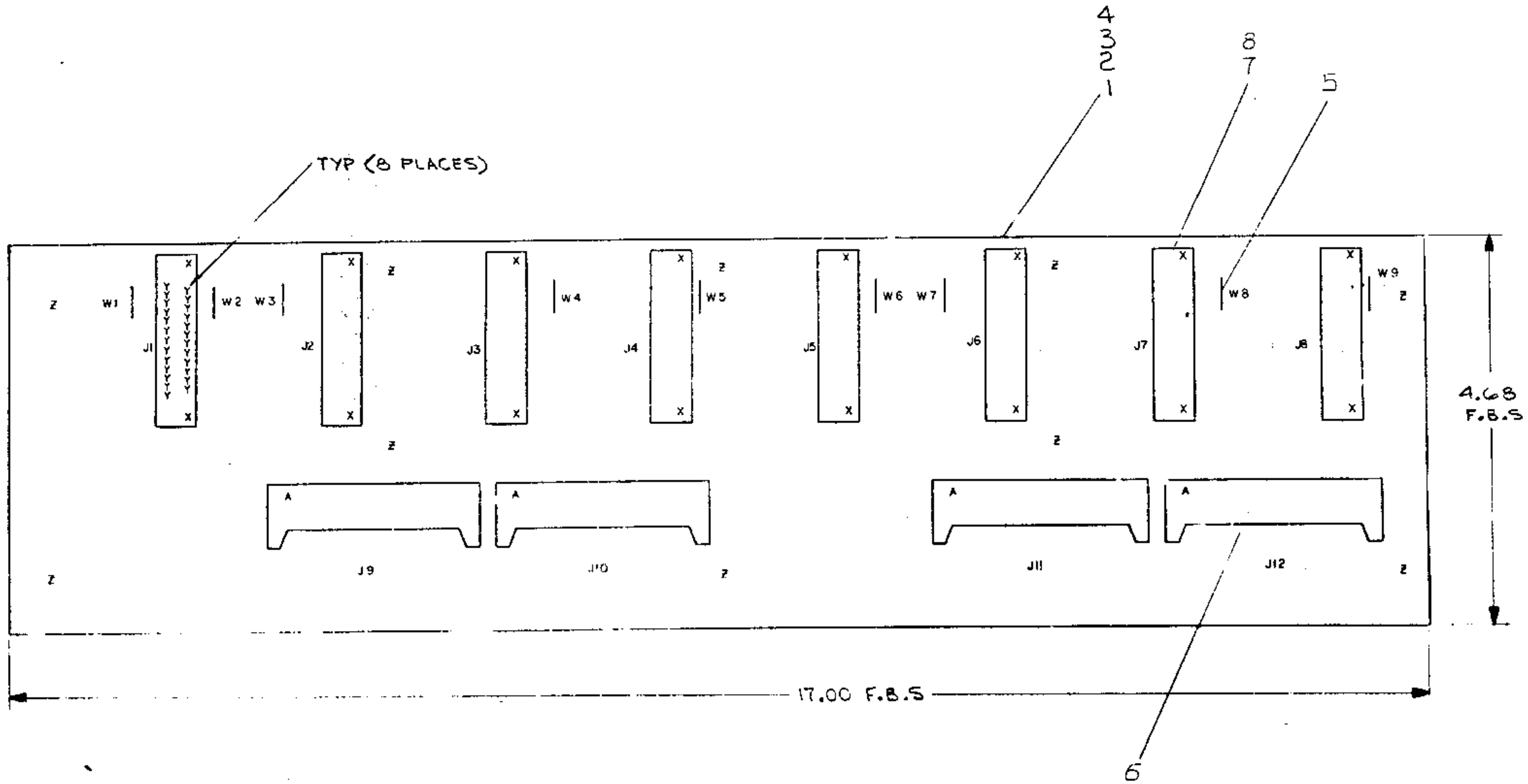
(RECV DATA MUXS AND TMARK DECODER)

TITLE	SIZE	CODE	NUMBER	REV.
SYNC MUX LINE CARD LINES 12-15 (D4-8)	D	BS	DV11-Ø-13	

SCALE — SHEET 8 OF 8 — DIST.

NOTES:

1. INSERT ALL JUMPERS



QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-5411153-0-4	1
REF		ASSY DRILLING HOLE LAYOUT	D-AH-5411153-0-5	2
REF		MODULE ECO HISTORY	B-UH-5411153-0-6	3
1		ETCHED CIRCUIT BOARD	5011152	4
5	W1-W9	JUMPER REEL	9107760-01	5
4	J9-J12	CONN 40 PIN	1209941	6
8	J1-J8	CONN EIA	1205386-01	7
16		SCREW LOCK ASSY	9008451	8

PARTS LIST

IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

FIRST USED ON OPTION MODEL: H317C

ETCH BOARD REV. A

SEMICONDUCTOR CONVERSION CHART

DEC NO.	EIA NO.	DEC NO.	EIA NO.

REV. A — ORIGINATED

DRN. George Dayton DATE 9-3-74
CHK'D. DATE
ENG. DATE
PROJ. ENG. DATE
PROD. DATE

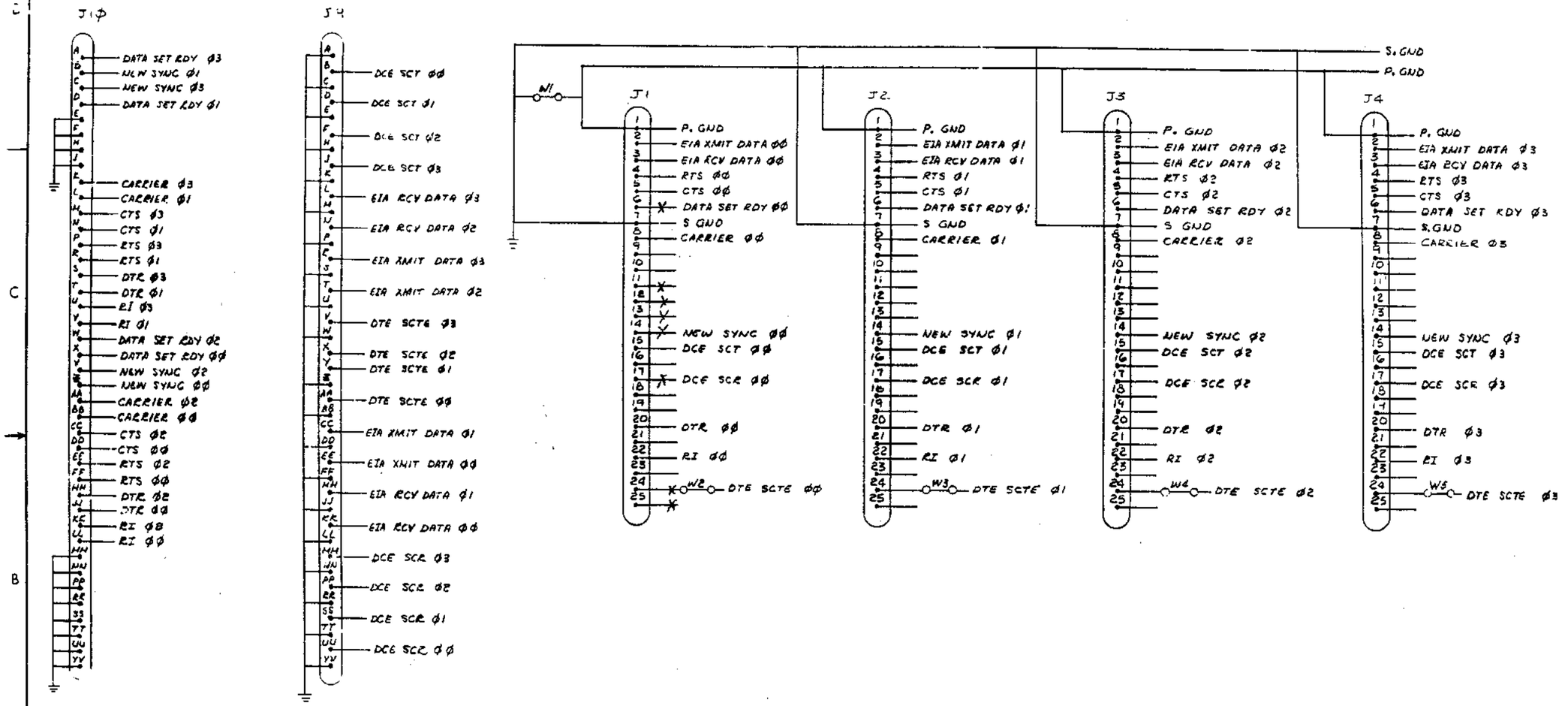
NEXT HIGHER ASSY D-UA-H317-Ø-Ø

digital

TITLE DV11 DISTRIBUTION PANEL

SIZE D CODE CS NUMBER 5411153-Ø-1 REV. *

SCALE —
SHEET 1 OF 5



REVISIONS		
CHK	CHANGE NO	REV

TITLE: J/11 DISTRIBUTION PANEL	SIZE: D	CODE: DCS	NUMBER: 5411153-0-1
SCALE: —	SHEET 2 OF 3	DIST 1	REV: —

DCS 5411153-0-1

DIGITAL EQUIPMENT CORPORATION

This microprogram listing lists the 9 bit binary address of each micro instructions, followed by the 16 bit micro instruction as it would appear in the ROM DATA REGISTER (D3-2), followed by an explanation of the micro instruction. Contents of the ROM DATA REGISTER are the complement of the ROM chip outputs. Odd addresses reference one set of 4 ROM chips, even addresses reference the other set of 4 ROM chips.

BITS	ADDRESSES	PART NUMBER	ROM LIST
15-12	even	23-192A2	K-CS-M7838-Ø-15
11-8	even	23-191A2	K-CS-M7838-Ø-14
7-4	even	23-189A2	K-CS-M7838-Ø-12
3-0	even	23-190A2	K-CS-M7838-Ø-13
15-12	odd	23-185A2	K-CS-M7838-Ø-8
11-8	odd	23-186A2	K-CS-M7838-Ø-9
7-4	odd	23-188A2	K-CS-M7838-Ø-11
3-0	odd	23-187A2	K-CS-M7838-Ø-1Ø

Diagnostic DZDVC Test #1 compares ROM DATA REGISTER contents with this listing. Use the above table to determine which ROM is faulty. Bit 15 is at left end of word Bit Ø at right end

REVISIONS		
REV.	CHANGE NO.	CHK
A	DV11-00002	

FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
DV11		PARTS LIST		

DRN. Robert Kopperal	DATE 3-31-75	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D Sid Roberts	DATE 4-17-75	
ENG. Robert E. Hansen	DATE 4-17-75	TITLE MICROPROGRAM LISTING
PROJ. ENG. Robert E. Hansen	DATE 4-17-75	
PROD. R. Wall	DATE 4-17-75	
NEXT HIGHER ASSEMBLY B-DD-DV11-Ø		SIZE K, CODE CS, NUMBER DV11-Ø-14, REV. A
SCALE		DIST.
SHEET 1 OF 13		

DEC FORM NO. DRB 109

```
                                        ;IDLE LOOP

0000000000  0101000001000010    ILOOP  S/C     6,2     ;INCREMENT SCANNER
0000000001  0011000001010100            XFR     ,5,4    ;MOVE MASTER SCAN TO RAM ADDRESS
0000000010  0000001011100100            BRA     2,TSERV ;TEST FOR TRANSMIT FLAG WAITING, IF YES BRANCH TO TRANSMIT SERVICE
0000000011  0000010000001010            BRA     4,RSERV ;TEST FOR RECEIVER FLAG WAITING, IF YES BRANCH TO RECEIVE FLAG SERV
0000000100  0000001101000011            BRA     3,SSERV ;TEST FOR RECEIVED CHARACTER WAITING, IF YES BRANCH TO RECEIVED CHA
0000000101  0010000000001011    ILOP2  RAM     0,0,13  ;OBTAIN LINE STATE
0000000110  0111000100101110            BRB     1,RSYNC ;TEST RAM OUTPUT 01 (RESYNC), IF YES BRANCH TO RESYNCHRONIZE
0000000111  0111001000111010            BRB     2,TMARK ;TEST RAM OUTPUT 02 (XMIT GO), IF YES BRANCH TO CLEAR TMARK
0000001000  0000010100101001    ILOP5  BRA     5,ISERV ;TEST FOR CHARACTER DISPATCH PROCEED, (SCN 08) IF YES BRANCH T
0000001001  0000000010000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP


                                        ;RECEIVE FLAG SERVICE  (LINE STATE IS IN RAM OUTPUT)

0000001010  0010000000001011    RSERV  RAM     0,0,13  ;OBTAIN LINE STATE
0000001011  0111000000011110            BRB     0,TESTX ;TEST RAM OUTPUT 00 (RECEIVER ACTIVE), IF YES BRANCH TO TESTX
0000001100  0111110100001111            BRB     15,S/ACT        ;TEST MATCH DETECT, IF YES BRANCH TO SET ACTIVE
0000001101  0101000001000110            S/C     6,6     ;SET RESYNC PULSE;
0000001110  0000000100000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO ILOOP
0000001111  0010000000001010    S/ACT  RAM     0,0,12  ;OBTAIN DLE/PROTOCOL
0000010000  0111000100011000            BRB     1,SACT2 ;TEST RAM 01 (STRIP LEADING SYNC), IF YES BRANCH TO SACT2
0000010001  0010000000001011    SACT1  RAM     0,0,13  ;OBTAIN LINE STATE
0000010010  0101000000100111            S/C     5,7     ;SET RAM OUTPUT 00 (RECEIVER ACTIVE)
0000010011  0010000110111011            RAM     1,13,13 ;WRITE NEW LINE STATE
0000010100  0111111000010001            BRB     16,SACT1        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO SACT 1
0000010101  0101000000100011    CLRRF  S/C     4,3     ;SET RECEIVE DATA ENABLE
0000010110  0101000000010010            S/C     4,2     ;CLEAR RECEIVE DATA ENABLE AND DATA AVAILABLE (FLAG WAITING)
0000010111  0000000100000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP
0000011000  0010000000011011    SACT2  RAM     0,0,13  ;OBTAIN LINE STATE
0000011001  0101000000100111            S/C     5,7     ;SET RAM OUTPUT 00 (RECEIVER ACTIVE)
0000011010  0101000000001110            S/C     7,6     ;SET RAM OUTPUT 06 (STRIP SYNC ON)
0000011011  0010000110111011            RAM     1,13,13 ;WRITE NEW LINE STATE
0000011100  0111111000011000            BRB     16,SACT2        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO SACT 2
0000011101  0000000100010101            BRA     1,CLRRF ;TEST FOR SURE TRUE, IF YES BRANCH TO CLRRF


0000011110  0010000000001011    TESTX  RAM     0,0,13  ;OBTAIN LINE STATE
0000011111  0111011000120001            BRB     6,TMD   ;TEST RAM OUTPUT 06 (STRIP SYNC ON), IF YES BRANCH TO TMD
0000100000  0000000100010001            BRA     1,S/RDE ;TEST FOR SURE TRUE, IF YES BRANCH TO S/RDE
0000100001  0111111010001011    TMD    BRB     15,CLRRF        ;TEST MATCH DETECT, IF YES BRANCH TO CLRRF
0000100010  0101000010000010            S/C     7,2     ;CLEAR RAM OUTPUT 06 (STRIP SYNC ON)
0000100011  0010000110111011            RAM     1,13,13 ;WRITE NEW LINE STATE
0000100100  0111111000001010            BRB     16,RSERV        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO RSERV
0000100101  0101000000010011    S/RDE  S/C     4,3     ;SET RECEIVE DATA ENABLE
0000100110  0101000000010001            S/C     4,1     ;SET SILO IN
0000100111  0101000000010010            S/C     4,2     ;CLEAR RECEIVE DATA ENABLE AND DATA AVAILABLE (FLAG WAITING)
0000101000  0000000100000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO ILOOP

                                        ;RECEIVE INTERRUPT RESPONSE SERVICE

0000101001  0011000011000001    ISERV  XFR     ,14,1   ;MOVE SILO OUT TO A REGISTER
0000101010  0000100000011111            ALU     37      ;LET ALU RESULT = A REGISTER
0000101011  0011000001100100            XFR     ,6,4    ;MOVE ALU RESULT 08-11 TO RAM ADDRESS REGISTER 00-03
0000101100  0101000000001110            S/C     3,6     ;CLEAR SCR08
0000101101  0000000101100010            BRA     1,CTEST ;TEST FOR SURE TRUE, IF YES BRANCH TO CTEST
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                                    ;RESYNCHRONIZE (MASTER SCAN IS IN RAM AR, LINE STATE IS IN RAM OUTPUT)

00 0101110  0010000000001011    RSYNC  RAM    0;0,13   ;OBTAIN LINE STATE
00 0101111  0101000000100011           S/C    5;3      ;CLEAR RAM OUTPUT 00 (RECEIVER ACTIVE)
00 0110000  0101000000100001           S/C    5;1      ;CLEAR RAM OUTPUT 01 (RESYNCHRONIZE)
00 0110001  0010000110111011           RAM    1;13,13  ;WRITE NEW LINE STATE
00 0110010  0111111000101110           BRB    16,RSYNC        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
00 0110011  0010000000001110    PSI    RAM    0;0,16   ;OBTAIN LINE PROTUCOL
00 0110100  0101000010000100           S/C    7;4      ;SET RAM OUTPUT 07
00 0110101  0010000110111110           RAM    1;13,16  ;WRITE NEW LINE PROTOCOL
00 0110110  0111111000110011           BRB    16,PSI   ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
00 0110111  0101000001000110           S/C    4;6      ;SET RESYNC PULSE
00 0111000  0101000000010001           S/C    4;1      ;SET SILO IN
00 0111001  0000000100000101           BRA    1;ILOP2  ;TEST FOR SURE TRUE, IF YES BRANCH TO ILOP2 (ILOOP +2)


                                    ;CLEAR TMARK

00 0111010  0101000010000001    TMARK  S/C    6;1      ;CLEAR TMARK
00 0111011  0000000100001000           BRA    1;ILOP5  ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP +5


                                    ;TEST FOR RESYNC FLAG (LINE NUMBER IN RAM AR, CHARACTER IN ALU RESULT)

00 0111100  0000000000111110    TFRF   BRA    0;CRAM7  ;TEST BIT 15 OF ALU RESULT, IF YES BRANCH TO HERE +2
00 0111101  0000000110000011           BRA    1;DISC   ;TEST FOR SURE TRUE, IF YES BRANCH TO DISCARD RECEIVED CHARACTER
00 0111110  0010000000001110    CRAM7  RAM    0;0,16   ;OBTAIN LINE PROTUCOL
00 0111111  0101000010000000           S/C    7;0      ;CLEAR RAM OUTPUT 07 (RESYNCH FLAG NOT FOUND)
00 1000000  0010000110111110           RAM    1;13,16  ;WRITE NEW LINE PROTOCOL
00 1000001  0111111000111110           BRB    16,CRAM7        ;TEST FOR WRITE INHIBIT,IF YES BRANCH BACK
00 1000010  0000000110000011           BRA    1;DISC   ;TEST FOR SURE TRUE, IF YES BRANCH TO DISCARD RECEIVED CHARACTER

                                    ;RECEIVED CHARACTER SILO SERVICE

00 1000011  0000010100101001    SSERV  BRA    5;ISERV  ;TEST FOR SCR08 (COULD HAVE SET BETWEEN 7 AND 9 INST OF ILOOP)
00 1000100  0011000011000001           XFR    ,14,1    ;MOVE SILO OUT TO A REGISTER
00 1000101  0001000000011111           ALU    31       ;LET ALU RESULT = A REGISTER
00 1000110  0011000001100100           XFR    ,6,4     ;MOVE ALU RESULT 08-11 TO RAM ADDRESS REGISTER 00-03
00 1000111  0010000000001011           RAM    0;0,13   ;OBTAIN LINE STATE
00 1001000  0111000110000011           BRB    1;DISC   ;TEST RAM OUTPUT 01 (RESYNC), IF YES BRANCH TO DISCARD
00 1001001  0010000000001110           RAM    0;0,16   ;OBTAIN LINE PROTUCOL
00 1001010  0111011100111100           BRB    7;TFRF   ;TEST RAM OUTPUT 07, IF YES BRANCH TO TEST FOR RESYNC FLAG
00 1001011  1000100010110001           BRA    16,POER  ;TEST BITS  13, 14 OF ALU RESULTS, IF YES BRANCH TO PARITY/OVERRUN
00 1001100  0111011010111010           BRB    6;T8C2   ;TEST RAM OUTPUT 06, IF YES BRANCH TO THIS IS BCC 2
00 1001101  0111010110100101           BRB    5;T8C1   ;TEST RAM OUTPUT 05, IF YES BRANCH TO THIS IS BCC 1
00 1001110  0010000000000101           RAM    0;0,5    ;OBTAIN RECEIVER BYTE COUNT
00 1001111  0111111001000100           BRB    14,CRBC0        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO CHARACTER RECEIVED WHILE
00 1010000  0010000000001010           RAM    0;0,12   ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
00 1010001  0111010101111110           BRB    5;ODCMR  ;TEST RAM OUTPUT 05, IF YES BRANCH TO ODCMP RECV
00 1010010  0010000000001101           RAM    0;0,15   ;OBTAIN RECEIVER MODE BITS
00 1010011  0011000010100010    ZETA   XFR    ,12,2    ;MOVE RAM OUTPUT DATA TRANSLATED 0-2/8-10 TO B REGISTER
00 1010100  0101000000010111           S/C    4;7      ;CLEAR ALU RESULT UPPER BYTE
00 1010101  0011000011110001           XFR    ,17,1    ;MOVE ALU RESULT TO A REGISTER
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00 1010110  0001000000010110           ALU    26       ;LET ALU RESULTS = A PLUS B
00 1010111  0011000011110010           XFR    ,17,2    ;MOVE ALU RESULTS TO B REGISTER
00 1011000  0010000000000101           RAM    0;0,11   ;OBTAIN RECEIVER CONTROL TABLE BASE ADDRESS
00 1011001  0011000010110001           XFR    ,13,1    ;MOVE RAM OUTPUT DATA TO A REGISTER (BASE ADDRESS)
00 1011010  0001000000010110           ALU    26       ;LET ALU RESULTS = A PLUS B (EFFECTIVE ADDRESS)
00 1011011  0011000011110011           XFR    1;17,3   ;MOVE ALU RESULTS TO NPR ADDRESS REGISTER
00 1011100  0100000000000000           NPR             ;DO NPR TO GET CONTROL BYTE
00 1011101  0111100101011101    RBUS1  BRB    11,RBUS1        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
00 1011110  0000011010111010           BRA    6;RNXMC  ;TEST NXM, IF YES, BRANCH TO RECEIVER NXM / CONTROL BYTE
00 1011111  0111101011010111           BRB    12,RMPEC        ;TEST MEM PAR ERR, IF YES, BRANCH TO RECEIVER MPE/CONTROL BYTE
00 1100000  0010000000001111           RAM    0;0,17   ;OBTAIN CONTROL BYTE STORAGE REGISTER (TO CLEAR INTERLOCK)
00 1100001  0010000110011111           RAM    1;11,17  ;MOVE DATI REGISTER TO RAM AND WRITE CONTROL BYTE STORAGE REGISTER


                                    ;CONTROL BYTE TESTS BEGIN (CHARACTER IS IN SILO OUT, CONTROL BYTE IS IN RAM 17)

00 1100010  0010000000001111    CTEST  RAM    0;0,17   ;OBTAIN CONTROL BYTE STORAGE REGISTER
00 1100011  0011000010110010           XFR    ,13,2    ;MOVE RAM OUTPUT TO B REGISTER
00 1100100  0001000000000001           ALU    5        ;LET ALU RESULT = B REGISTER
00 1100101  0010000101111101           RAM    1;7,15   ;MOVE ALU RESULTS TRANSLATED 5-7/0-2 TO RAM (AND WRITE NEW MODE BITS
00 1100110  1000101010101011           BRA    16,CBINT        ;TEST BIT 0 OF ALU RESULT, IF YES BRANCH TO CONTROL BYTE INTERPRT
00 1100111  0000110010011011           BRA    14,EBCC  ;TEST BIT 02 OF ALU RESULT, IF YES BRANCH TO SET EXPECT BCC 1 NEXT
00 1101000  0000110110000101    EPSIL  BRA    15,RBCC  ;TEST BIT 03 OF ALU RESULT, IF YES, BRANCH TO CALCULATE RECV B


                                    ;RETURN FROM RECV BCC  (CONTROL BYTE IS STILL IN ALU RESULT)

00 1101001  0000011210000011    RRBCC  BRA    10,DISC  ;TEST BIT 4 OF ALU RESULT, IF YES, BRANCH TO (BIT 4 SET = DISC
00 1101010  0010000000000100           RAM    0;0,4    ;OBTAIN RECEIVER CURRENT ADDRESS
00 1101011  0011001110110011           XFR    0;13,3   ;MOVE RAM OUTPUT TO NPR ADDRESS REGISTER
00 1101100  0011000011000101           XFR    ,14,5    ;MOVE SILO OUT TO DATO REGISTER (FOR USE IF NEXT CHARACTER WILL HAVE
00 1101101  0100000000000000           NPR             ;DO NPR TO STORE RECEIVED CHARACTER
00 1101110  0111100101101110    RBUS2  BRB    11,RBUS2        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
00 1101111  0000011011100000           BRA    6;RNXM   ;TEST NXM, IF YES, BRANCH TO RECEIVER NXM
00 1110000  0010000000000101    ORBC   RAM    0;0,5    ;OBTAIN RECEIVER BYTE COUNT
00 1110001  0011000010110001           XFR    ,13,1    ;MOVE RAM OUTPUT TO REGISTER A
00 1110010  0001000000011111           ALU    77       ;LET ALU RESULTS = A+1
00 1110011  0010000111110101           RAM    1;17,5   ;MOVE ALU RESULTS TO RAM INPUT (AND WRITE NEW BYTE COUNT)
00 1110100  0111111001110000           BRB    16,ORBC  ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO  HERE -4
00 1110101  0010000000000100    ORCA   RAM    0;0,4    ;OBTAIN RECEIVER CURRENT ADDRESS
00 1110110  0011000010110001           XFR    ,13,1    ;MOVE RAM OUTPUT DATA TO REGISTER A
00 1110111  0001000000111111           ALU    77       ;LET ALU RESULTS = A+1
00 1111000  0010000111110100           RAM    1;17,4   ;MOVE ALU RESULTS TO RAM INPUT (AND WRITE NEW ADDRESS)
00 1111001  0111111001110101           BRB    16,ORCA  ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
00 1111010  0010000000000101           RAM    0;0,5    ;OBTAIN RECEIVER BYTE COUNT
00 1111011  0111111210001111           BRB    14,NBC0  ;TEST RAM OUTPUT 0-14=0, IF YES, BRANCH TO NEXT CHARACTER WILL HAVE
00 1111100  0101000000010000           S/C    4;0      ;SET SILO OUT
00 1111101  0000000100000000           BRA    1;ILOOP  ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP


                                    ;DDCMP RECEPTION

00 1111110  0010000000001101    DDCMR  RAM    0;0,15   ;OBTAIN RECEIVER MODE BITS
00 1111111  0111111001000001           BRB    14,DDCM2        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO DDCM2
01 0000000  0000000101010011           BRA    1;ZETA   ;TEST FOR SURE TRUE, IF YES BRANCH TO ZETA
01 0000001  0001000000001100    DDCM2  ALU    14       ;LET ALU RESULT = 0
01 0000010  0000000110000101           BRA    1;RBCC   ;TEST FOR SURE TRUE, IF YES BRANCH TO CALCULATE RECV BCC
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                                    ;DISCARD RECEIVED CHARACTER

0100000011  0101000000014000    DISC    S/C     4,0     ;SET SILO OUT
0100001000  0000000100000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP


                                    ;CALCULATE RECV BCC (ASSUME RECEIVED CHARACTER IN SILO OUT)

0100001010  0011000011000001    RBCC    XFR     ,14,1   ;MOVE SILO OUT REGISTER TO A REGISTER
0100001110  0010000000000111            RAM     0,0,7   ;OBTAIN RECV BCC CALCULATED TO DATE
0100002111  0011000010110010            XFR     ,13,2   ;MOVE RAM OUTPUT DATA TO B REGISTER
0100001000  0010000000001010            RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0100001001  0110000000000000            BCC             ;PERFORM SPECIFIED BCC CALCULATION
0100011010  0010000111100111            RAM     1,16,7  ;MOVE BCC TO RAM INPUT AND WRITE NEW RECEIVER BCC
0100001011  0000000101101001            BRA     1,RRBCC ;TEST FOR SURE TRUE, IF YES, BRANCH TO RETURN FROM RECV BCC


                                    ;CHARACTER RECEIVED WHILE RECV BC=0

0100001100  0011000011000110    CRBC0   XFR     ,14,6   ;MOVE SILO OUT REGISTER TO RICR
0100001101  0101000000001000            S/C     3,0     ;SET RICR 15 (TO INDICATE RECEPTION WHILE BC=0)
0100001110  1000000110110010            BRA     1,CNACB ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY

                                    ;NEXT CHARACTER WILL HAVE BC=0  (SILO OUT HAS BEEN SET, RECEIVER BYTE COUNT IS 1

0100001111  0011000011010110    NBC0    XFR     ,15,6   ;MOVE NPR DATO REGISTER TO RICR
0100010000  0101000000201001            S/C     3,1     ;SET RICR 14 (TO INDICATE RECEPTION OF NEXT CHARACTER WILL BE BC=0)
0100010001  0111101110010011            BRB     15,MCBCX        ;TEST RAM OUTPUT 15, IF TRUE BRANCH TO MODE CHANGE / BCC EXPECT
0100010010  1000000110110010            BRA     1,CNACB ;TEST FOR SURE TRUE, IF YES BRANCH TO  CREATE NULL ACTION CONTROL B


                                    ;MODE CHANGE AND BCC EXPECT

0100010011  0010000200001011    MCBCX   RAM     0,0,13  ;OBTAIN LINE STATE
0100010100  0011000010110010            XFR     ,13,2   ;MOVE RAM OUTPUT TO B REGISTER
0100010101  0011000010000010            XFR     ,10,2   ;MOVE B REGISTER 8-15 TO B REGISTER 0-7
0100010110  0001000003000101            ALU     5       ;LET ALU RESULT = B REGISTER
0100010111  0010000101111101            RAM     1,7,15  ;MOVE ALU RESULTS TRANSLATED TO RAM AND WRITE NEW  RECV MODE BITS
0100011000  0010000111111111            RAM     1,17,17 ;WRITE CONTROL BYTE STORAGE FROM ALU RESULT
0100011001  0000011001010000            BRA     14,EBCN ;TEST ALU RESULT 02, IF YES BRANCH TO EXPECT BCC NEXT BECAUSE OF BC
0100011010  1000000110110010            BRA     1,CNACB ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY


                                    ;EXPECT BCC NEXT BECAUSE OF CONTROL BYTE

0100011011  0010000000001110    EBCC    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100011100  0101000010000101            S/C     7,5     ;SET RAM OUTPUT 05 (EXPECT BCC 1 NEXT)
0100011101  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL FROM RAM OUTPUT
0100011110  0111111010011011            BRB     16,EBCC ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100011111  0000000101101000            BRA     1,EPSIL ;TEST FOR SURE TRUE, IF YES BRANCH TO EPSIL


                                    ;EXPECT BCC NEXT BECAUSE OF BC = 0

0100100000  0010000000001110    EBCN    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100100001  0101000010000101            S/C     7,5     ;SET RAM OUTPUT 05 (EXPECT BCC1 NEXT)
0100100010  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL FROM RAM OUTPUT
0100100011  0111111010100000            BRB     16,EBCN ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO EBCN
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0100100100  0000000110000011            BRA     1,DISC  ;TEST FOR SURE TRUE, IF YES BRANCH TO DISCARD


                                    ;THIS IS BCC 1

0100100101  0010000000001110    TBC1    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100100110  0101000010000001            S/C     7,1     ;CLEAR RAM OUTPUT 01 (EXPECT BCC 1 NEXT)
0100100111  0101000010000110            S/C     7,6     ;SET RAM OUTPUT 06 (EXPECT BCC 2 NEXT)
0100101000  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL FROM RAM
0100101001  0111111010100101            BRB     16,TBC1 ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100101010  0011000011000001            XFR     ,14,1   ;MOVE SILO OUT REGISTER TO A REGISTER
0100101011  0010000000000111            RAM     0,0,7   ;OBTAIN RECV BCC CALCULATED TO DATE
0100101100  0011000010110010            XFR     ,13,2   ;MOVE RAM OUTPUT DATA TO B REGISTER
0100101101  0010000000001010            RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0100101110  0110000000000000            BCC             ;PERFORM SPECIFIED BCC CALCULATION
0100101111  0010000111100111            RAM     1,16,7  ;MOVE BCC TO RAM INPUT AND WRITE NEW RECEIVER BCC
0100110000  0010000000001010            RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II (TO LOOK FOR LRC)
0100110001  0111101110111000            BRB     3,TBC1X ;TEST RAM OUTPUT 03
0100110010  0111010010111000            BRB     4,TBC1X ;TEST RAM OUTPUT 04
0100110011  0010000200001110    MRTHA   RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100110100  0101000010000010            S/C     7,2     ;CLEAR RAM OUTPUT 06 (EXPECT BCC2 NEXT)
0100110101  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL
0100110110  0111111010110011            BRB     16,MRTHA        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100110111  0000000111000100            BRA     1,BCCCK ;TEST FOR SURE TRUE, IF YES BRANCH  TO BCC CHECK COMPLETE
0100111000  0101000020001300    TBC1X   S/C     4,0     ;SET SILO OUT
0100111001  0000000130000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP


                                    ;THIS IS BCC 2

0100111010  0010000000001110    TBC2    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0100111011  0101000010000010            S/C     7,2     ;CLEAR RAM OUTPUT 06
0100111100  0010000110111110            RAM     1,13,16 ;WRITE LINE PROTOCOL
0100111101  0111111010111011            BRB     16,TBC2 ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
0100111110  0011000011000001            XFR     ,14,1   ;MOVE SILO OUT REGISTER TO A REGISTER
0100111111  0010000000000111            RAM     0,0,7   ;OBTAIN RECV BCC CALCULATED TO DATE
0101000000  0011000010110010            XFR     ,13,2   ;MOVE RAM OUTPUT DATA TO B REGISTER
0101000001  0010000000001010            RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0101000010  0110000000000000            BCC             ;PERFORM SPECIFIED BCC CALCULATION
0101000011  0010000111100111            RAM     1,16,7  ;MOVE BCC TO RAM INPUT AND WRITE NEW RECEIVER BCC
0101000100  0001000000011100    BCCCK   ALU     34      ;LET ALU RESULT = MINUS 1
0101000101  0101000000010111            S/C     4,7     ;CLEAR ALU RESULT UPPER BYTE
0101000110  0011000011110001            XFR     ,17,1   ;MOVE ALU RESULT TO A REGISTER
0101000111  0011000011000010            XFR     ,14,2   ;MOVE SILO OUT TO B REGISTER
0101001000  0001000000011101            ALU     15      ;LET ALU RESULT = AND OF A COMPLEMENT AND B
0101001001  0011000011110010            XFR     ,17,2   ;MOVE ALU RESULT TO B REGISTER
0101001010  0011000011100001            XFR     ,16,1   ;MOVE BCC TO A REGISTER
0101001011  0001000000011111            ALU     31      ;LET ALU RESULT = A
0101001100  0101000000010111            S/C     4,7     ;CLEAR ALU RESULT UPPER BYTE
0101001101  0011000011110001            XFR     ,17,1   ;MOVE ALU RESULT TO A REGISTER
0101001110  0001000000011110            ALU     30      ;LET ALU RESULT= A OR B
0101001111  0011000011110001            XFR     ,17,1   ;MOVE ALU RESULT TO A REGISTER
0101010000  0011000011100010            XFR     ,16,2   ;MOVE BCC TO B REGISTER
0101010001  0011000010000010            XFR     ,12,2   ;MOVE B REGISTER 8-15 TO B REGISTER 0-7 (UPPER BYTE OF BCC)
0101010010  0001000000011110            ALU     30      ;LET ALU RESULT = A OR B
0101010011  0011000011110110            XFR     ,17,6   ;MOVE ALU RESULT TO RICR REGISTER
0101010100  0101000000001101            S/C     3,5     ;SET RICR 12
0101010101  0101000000001001            S/C     3,1     ;SET RICR 14
0101010110  1000000110110010            BRA     1,CNACB ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY
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                                ;RECEIVER NPE / CONTROL BYTE

0|10010111  0011000011000110    RNPEC  XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
0|1011000   0101000000000110    ⁰      S/C     3,4     ;SET RICR 13
0|1011001   0000000111011011    ⁰      BRA     1,GAMMA ;TEST FOR SURE TRUE, IF YES BRANCH TO RECEIVER NXM / CONTROL BYTE +

                                ;NECEIVER NXM / CONTROL BYTE

0|1011010   0011000011000110    RNXMC  XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
0|1011011   0101000000000110    GAMMA  S/C     3,5     ;SET RICR 12
0|1011100   0101000000000101    BETA   S/C     3,1     ;SET RICR 14
0|1011101   0101000000000100    ⁰      S/C     3,0     ;SET RICR 15
0|1011110   0101000000001111    ⁰      S/C     3,7     ;CLEAR NXM
0|1011111   1000000110110010    ⁰      BRA     1,CNACB ;TEST FOR SURE TRUE, IF YES BRANCH TO CREATE NULL ACTION CONTROL BY

                                ;RECEIVER NXM (WE GOT HERE FROM RECEIVED CHARACTER SILO SERVICE)

0|1100000   0011000011000110    RNXM   XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
0|1100001   0000000111011100    ⁰      BRA     1,BETA  ;TEST FOR SURE TRUE, IF YES BRANCH TO RECEIVER NXM / CONTROL BYTE +

                                ;NPR SILO OVERFLOW

0|1100010   0101000000001010    NPRSO  S/C     3,2     ;SET SCR 10 INDICATING NPR SILO OVERFLOW
0|1100011   0000000100000000    ⁰      BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;TRANSMIT SERVICE

                                ;CHECK FOR BCC TRANSMISSION

0|1100100   0010000000001110    TSERV  RAM     0,0,16  ;OBTAIN LINE PROTOCOL
0|1100101   0011000010110001    ⁰      XFR     ,13,1   ;MOVE RAM OUTPUT DATA TO A REGISTER
0|1100110   0001000000011111    ⁰      ALU     3/      ;LET ALU RESULT=A REGISTER
0|1100111   1000101010011110    ⁰      BRA     12,SBC1 ;TEST BIT 0 OF ALU RESULT, IF YES BRANCH TO SEND BCC 1
0|1101000   1000101110100010    ⁰      BRA     13,SBC2 ;TEST BIT 1 OF ALU RESULT, IF YES BRANCH TO SEND BCC 2
0|1101001   0000011111100010    ⁰      BRA     7,NPRSO ;TEST FOR NPR SILO NOT AVAILABLE, IF YES, BRANCH TO NPR SILO OVERFLO

                                ;PRINCIPAL/ALTERNATE SELECTION

0|1101010   0010000000001011            RAM     0,0,13  ;OBTAIN LINE STATE
0|1101011   0111001011101101            BRB     2,SIGMA ;TEST BIT 02 OF RAM, IF YES, BRANCH TO HERE +2 (TESTING TRANSMIT GO
0|1101100   1000000101100100            BRA     1,ITYPE ;TEST FOR SURE TRUE, IF YES BRANCH TO SELECT TYPE OF IDLING
0|1101101   0111011111110010    SIGMA   BRB     7,USCA  ;TEST RAM OUTPUT 07, IF YES BRANCH TO USE ALTERNATE CA
0|1101110   0010000000000001            RAM     0,0,1   ;OBTAIN PRINCIPAL BC (GE TEST)
0|1101111   1111110001000000            BRB     14,XPBC0        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO XMIT PBCO
0|1110000   0010000000000000            RAM     0,0,0   ;OBTAIN PRINCIPAL CURRENT ADDRESS
0|1110001   0000000111110101            BRA     1,OXCB  ;TEST FOR SURE TRUE, IF YES BRANCH TO OBTAIN XMIT CONTROL BYTE

                                ;USE ALTERNATE CA

0|1110010   0010000000000011    USCA    RAM     0,0,3   ;OBTAIN ALTERNATE BC, (GE TEST)
0|1110011   1111110001010000            BRB     14,XSBC0        ;TEST RAM OUTPUT 0-14=0, IF YES BRANCH TO XMIT SBCO
0|1110100   0010000000000010            RAM     0,0,2   ;OBTAIN ALTERNATE CURRENT ADDRESS
                                ;OBTAIN XMIT CONTROL BYTE
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0|1110101   0011000010110011    OXCB    XFR     I,13,3  ;MOVE DATA FROM RAM OUTPUT TO NPR ADDRESS REGISTER
0|1110110   0100000000000000            NPR             ;DO NPR TO GET CHARACTER
0|1110111   0111100111110111    RBUS3   BRB     11,RBUS3        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
0|1111000   1000011000110001            BRA     6,TNXMC ;TEST NXM, IF YES, BRANCH TO TRANSMIT NXM/CHARACTER
0|1111001   1111101000111001            BRB     12,TMPEC        ;TEST MEM PAR ERR, IF YES, BRANCH TO TRANSMIT MPE/CHARACTER
0|1111010   0011000010010001            XFR     ,11,1   ;MOVE DATA FROM CVC/DATI REGISTER TO A REGISTER
0|1111011   0001000000011111            ALU     3/      ;LET ALU RESULT = A REGISTER
0|1111100   0011000011110101            XFR     ,17,5   ;MOVE DATA FROM ALU RESULT TO DATO REGISTER (FOR BCC AND TRANSMITTER
0|1111101   0010000000001010            RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
0|1111110   1111011010001100            BRB     6,ODCMX ;TEST RAM OUTPUT 06, IF YES BRANCH TO ODCMP XMIT (CALCUL - F BCC)
0|1111111   0010000000001100            RAM     0,0,14  ;OBTAIN MODE BITS
1|0000000   0011000010100012    PI      XFR     ,12,2   ;MOVE RAM OUTPUT DATA TRANSLATED 0-2/8-10 TO B REGISTER
 0000001    0001000000010110        ⁰   ALU     26      ;LET ALU RESULTS = A PLUS B
1|0000010   0011000011110010        ⁰   XFR     ,17,2   ;MOVE ALU RESULTS TO B REGISTER
1|0000011   0010000000001000        ⁰   RAM     0,0,10  ;OBTAIN CONTROL TABLE BASE ADDRESS
1|0000100   0011000019110001        ⁰   XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1|0000101   0001000000010110        ⁰   ALU     26      ;LET ALU RESULT = A PLUS B ((CHAR+MODE)+BASE ADDR)
1|0000110   0011000011110011        ⁰   XFR     I,17,3  ;MOVE ALU RESULTS TO NPR ADDRESS REGISTER
1|0000111   0100000000000000        ⁰   NPR             ;DO NPR TO GET CONTROL BYTE
1|0001000   1111100100001000    RBUS4   BRB     11,RBUS4        ;TEST REQUEST BUS, IF YES, BRANCH TO HERE
1|0001001   1000011000110001            BRA     6,TNXMC ;TEST NXM, IF YES, BRANCH TO TRANSMIT NXM/CONTROL BYTE
1|0001010   1111101000111001            BRB     12,TMPEC        ;TEST MEM PAR ERR, IF YES, BRANCH TO TRANSMIT MPE/CONTROL BYT
1|0001011   0011000010010010            XFR     ,11,2   ;MOVE DATI REGISTER TO B REGISTER
1|0001100   0001000000000101            ALU     5       ;LET ALU RESULT = B REGISTER
1|0001101   1000101101110011            BRA     14,SDLE ;TEST BIT 1 OF ALU RESULT, IF YES BRANCH TO SEND DLE FIRST

                                ;RETURN FROM DLE SENDING

1|0001110   0010000101111100    RDLE    RAM     1,7,14  ;MOVE ALU RESULT TRANSLATED 5-7/0-2 TO RAM (AND WRITE NEW MODE P
1|0001111   1000110010000010            BRA     14,SSBN ;TEST BIT 2 OF ALU RESULT, IF YES BRANCH TO SET SEND BCC NEXT

                                ;RETURN FROM SSBCNXT

1|0010000   1000110110001111    RSSBN   BRA     15,XBCC ;TEST BIT 3 OF ALU RESULT, IF YES BRANCH TO CALCULATE TRANS BC

                                ;RETURN FROM XMIT BCC

1|0010001   1111130001101001    RXBCC   BRB     10,SIDLE        ;TEST FOR DNA FLAG, IF YES BRANCH TO SEND IDLE
1|0010010   0011000011010000    ALPHA   XFR     ,15,0   ;MOVE DATO REGISTER TO TRANSMITTED DATA BUS
1|0010011   0010000000001011            RAM     0,0,13  ;OBTAIN LINE STATE
1|0010100   1111011100100011            BRB     7,USBC  ;TEST BIT 7 OF RAM OUTPUT, IF YES BRANCH TO USE ALTERNATE BC

                                ;USE PRINCIPAL BC

1|0010101   0010000000000001    UPBC    RAM     0,0,1   ;OBTAIN PRINCIPAL BYTE COUNT
1|0010110   1111110001000000            BRB     14,XPBC0        ;TEST RAM 0-14=0
1|0010111   0011000010110001            XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1|0011000   0001000000011111            ALU     27      ;LET ALU RESULTS = A PLUS 1
1|0011001   0011000011110001            RAM     1,17,1  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW PRINCIPAL BYTE COUNT
1|0011010   1111111000010101            BRB     10,UPBC ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE =4
1|0011011   0010000000000000    OPCA    RAM     0,0,0   ;OBTAIN PRINCIPAL CURRENT ADDRESS
1|0011100   0011000010110001            XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1|0011101   0001000000011111            ALU     27      ;LET ALU RESULT = A PLUS 1
1|0011110   0010000111110000            RAM     1,17,0  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW PRINCIPAL CURR - ADDRES
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1Ø0011111  1111111000011011        BRB     1Ø,OPCA ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0100000  0010000000000001        RAM     0;0,1   ;OBTAIN PRINCIPAL BYTE COUNT
1Ø0100001  1111110001000000        BRB     14,XPBC0        ;TEST RAM 0-14-0, IF YES, BRANCH TO XMIT PBC0
1Ø0100010  0000000100000000        BRA     1;ILOOP ;TEST FOR SURE TRUE AND BRANCH TO IDLE LOOP

                                ;USE ALTERNATE BC

1Ø0100011  0010000000000011  USBC  RAM     0;0,3   ;OBTAIN ALTERNATE BYTE COUNT
1Ø0100100  1111111000101000        BRB     14,XSBC0        ;TEST RAM 0-14=0
1Ø0100101  0011000010110001        XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1Ø0100110  0001000000111111        ALU     7?      ;LET ALU RESULTS = A PLUS 1
1Ø0100111  0010000000111011        RAM     1;17,3  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW ALTERNATE BYTE COUNT
1Ø0101000  1111111000100011        BRB     1Ø,USBC ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0101001  0010000000000010  OSCA  RAM     0;0,2   ;OBTAIN ALTERNATE CURRENT ADDRESS
1Ø0101010  0011000010110001        XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
1Ø0101011  0001000000111011        ALU     7?      ;LET ALU RESULT = A PLUS 1
1Ø0101100  0010000111110010        RAM     1;17,2  ;MOVE ALU RESULT TO RAM INPUT AND WRITE NEW ALTERNATE CURRENT ADDRES
1Ø0101101  1111111000101001        BRB     1Ø,OSCA ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0101110  0010000000000011        RAM     0;0,3   ;OBTAIN ALTERNATE BYTE COUNT
1Ø0101111  1111110001010000        BRB     14,XSBC0        ;TEST RAM 0-14-0, IF YES, BRANCH TO XMIT SBC0
1Ø0110000  0000000100000000        BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;TRANSMIT NXM/CHARACTER  (CURRENT ADDRESS REGISTER ADDRESS IS IN RAM AR)

                                ;TRANSMIT NXM/CONTROL BYTE  (CONTROL TABLE BASE ADDRESS REGISTER ADDRESS IS IN R

1Ø0110001  0011000000000111  TNXMC XFR     ,Ø,7    ;MOVE  TO NPR STATUS REPORT REG.
1Ø0110010  0010000000001011  IOTA  RAM     0;0,13  ;OBTAIN LINE STATE
1Ø0110011  0101000010000111        S/C     7;7     ;SET RAM 04 (TRANSMITTER NXM)
1Ø0110100  0101000000001111        S/C     3;7     ;CLEAR NXM
1Ø0110101  0101000000100010        S/C     5;2     ;CLEAR RAM 02 (TRANSMITTER GO)
1Ø0110110  0010000110111011        RAM     1;13,13 ;WRITE NEW LINE STATE
1Ø0110111  1111111000110010        BRB     1Ø,IOTA ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO IOTA
1Ø0111000  0000000100000000        BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;TRANSMIT MPE/CHARACTER   (CURRENT ADDRESS REGISTER ADDRESS IS IN RAM AR)

                                ;TRANSMIT MPE/CONTROL BYTE  (CONTROL TABLE BASE ADDRESS REGISTER ADDRESS IS IN R

1Ø0111001  0011000000000111  TMPEC XFR     ,Ø,7    ;MOV  TO NPR STATUS REPORT REG.
1Ø0111010  0010000000001011  OMEGA RAM     0;0,13  ;OBTAIN LINE STATE
1Ø0111011  0101000010000101        S/C     7;5     ;SET RAM 05 (TRANSMIT MPE)
1Ø0111100  0101000000100010        S/C     5;2     ;CLEAR RAM 02 (TRANSMITTER GO)
1Ø0111101  0010000110111011        RAM     1;13,13 ;WRITE NEW LINE STATE
1Ø0111110  1111111000111010        BRB     1Ø,OMEGA        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -4
1Ø0111111  0000000100000000        BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES, BRANCH TO IDLE LOOP

                                ;XMIT PBC0

1Ø1000000  0010000000001011  XPBC0 RAM     0;0,13  ;OBTAIN LINE STATE
1Ø1000001  0101000010000100        S/C     7;4     ;SET RAM OUTPUT BIT 7 (GO TO ALTERNATE)
1Ø1000010  0010000110111011        RAM     1;13,13 ;MOVE RAM OUTPUT TO RAM (AND WRITE NEW LINE STATE)
1Ø1000011  1111111001000000        BRB     1Ø,XPBC0        ;TEST FOR WRITE INHIBT, IF YES BRANCH TO HERE -3
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1Ø1000100  0010000000000001        RAM     0;0,1   ;OBTAIN PRINCIPAL BYTE COUNT
1Ø1000101  0011000000000111        XFR     ,Ø,7    ;MAKE NPR SILO ENTRY
1Ø1000110  1111101101001000        BRB     13,RED  ;TEST RAM OUTPUT BIT 15, IF YES BRANCH TO HERE +2
1Ø1000111  1000000101010111        BRA     1;CBC0  ;TEST FOR SURE TRUE, IF YES BRANCH TO CHECK FOR BOTH BC=0
1Ø1001000  0010000000000001  RED   RAM     1;0,1   ;ZERO PRINCIPAL BYTE COUNT
1Ø1001001  0011000000001110  DTMB  RAM     0;0,16  ;OBTAIN  LINE PROTOCOL
1Ø1001010  0011000010110010        XFR     ,13,2   ;MOVE RAM OUTPUT TO REGISTER B
1Ø1001011  0011000010000010        XFR     ,10,2   ;MOVE REGISTER B8-15 TO REGISTER B 0-7
1Ø1001100  0001000000001001        ALU     5       ;LET ALU RESULT = B
1Ø1001101  0010000010111100        RAM     1;7,14  ;MOVE ALU RESULTS TRANSLATED  TO RAM AND WRITE NEW MODE [illegible]
1Ø1001110  1000110010000111        BRA     14,BC0SB        ;TEST  ALU RESULT 02, IF YES BRANCH TO BC0 SEND NOW
1Ø1001111  1000000101010111        BRA     1;CBC0  ;TEST FOR SURE TRUE, IF YES BRANCH TO CHECK FOR BOTH BC=0

                                ;XMIT SBC0

1Ø1010000  0010000000001011  XSBC0 RAM     0;0,13  ;OBTAIN LINE STATE
1Ø1010001  0101000010000000        S/C     7;0     ;CLEAR RAM OUTPUT BIT 7 (GO TO PRINCIPAL)
1Ø1010010  0010000110111011        RAM     1;13,13 ;MOVE RAM OUTPUT TO RAM (AND WRITE NEW LINE STATE)
1Ø1010011  1111111001000010        BRB     1Ø,XSBC0        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -3
1Ø1010100  0010000000000011        RAM     0;0,3   ;OBTAIN ALTERNATE BYTE COUNT
1Ø1010101  0011000000000111        XFR     ,Ø,7    ;MAKE NPR SILO ENTRY
1Ø1010110  1111101101011001        BRB     13,ESS  ;TEST RAM OUTPUT 15, IF YES, BRANCH TO CLEAR ALTERNATE BYTE COUNT

                                ;CHECK FOR BOTH BC=0

1Ø1010111  0010000000000001  CBC0  RAM     0;0,1   ;OBTAIN PRINCIPAL BYTE COUNT
1Ø1011000  1111110001011010        BRB     14,DELTA        ;TEST RAM OUTPUT 0-14-0, IF YES, BRANCH TO HERE +2
1Ø1011001  0000000100000010        BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES, BRANCH TO IDLE LOOP
1Ø1011010  0010000000000011  DELTA RAM     0;0,3   ;OBTAIN ALTERNATE BYTE COUNT
1Ø1011011  1111110001011111        BRB     14,C/GO ;TEST RAM OUTPUT 0-14-0, IF YES, BRANCH TO CLEAR GO
1Ø1011100  0000000100000010        BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;CLEAR ALTERNATE BYTE COUNT

1Ø1011101  0010000000000011  ESS   RAM     1;0,3   ;ZERO ALTERNATE BYTE COUNT
1Ø1011110  1000000101001001        BRA     1;DTMB  ;TEST FOR SURE TRUE, BRANCH TO DTMB

                                ;CLEAR GO

1Ø1011111  0010000000001011  C/GO  RAM     0;0,13  ;OBTAIN LINE STATE
1Ø1100000  0101000000100010        S/C     5;2     ;CLEAR RAM 02 (TRANSMITTER GO)
1Ø1100001  0010000110111011        RAM     1;13,13 ;WRITE NEW LINE STATE
1Ø1100010  1111111001000011        BRB     1Ø,C/GO ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -3
1Ø1100011  0000000100000010        BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;SELECT TYPE OF IDLE

1Ø1100100  0010000000001010  ITYPE RAM     0;0,12  ;OBTAIN TRANSMITTER DLE/PROTOCOL II
1Ø1100101  1111000000100111        BRB     0;BC0CG ;TEST RAM OUTPUT 00, IF YES BRANCH TO BC0CG
1Ø1100110  0000000100000000        BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP
1Ø1100111  0101000000100101  BC0CG S/C     6;5     ;SET TMARK
1Ø1101000  0000000100000000        BRA     1;ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                ;SENT IDLE  (LINE STATE IS IN RAM OUTPUT)

1Ø1101001  0010000000001011  SIDLE RAM     0;0,13  ;OBTAIN LINE STATE
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1Ø1101010  0101000000010Ø1ØØ        S/C     5,4      ;SET RAM Ø3 (TRANSMITTER UNDERRUN)
1Ø1101011  0010000110111011        RAM     1,13,13 ;MOVE RAM OUTPUT TO RAM (AND WRITE NEW LINE STATE)
1Ø1101100  1111111100110ØØ1        BRB     1Ø,8IDLE        ;TEST FOR WRITE INHIBIT, IF YES BRANCH TO HERE -3
1Ø1101101  1000000100010010        BRA     1,ALPHA ;TEST FOR SURE TRUE, IF YES, BRANCH TO RETURN FROM XMIT BCC +3

                                   ;SENT IDLE/DLE

1Ø1101110  0010000000001011        MU      RAM     0,0,13  ;OBTAIN LINE STATE
1Ø1101111  0101000000100100        S/C     5,4     ;SET Ø3 (UNDERRUN)
1Ø1110000  0010000110111011        RAM     1,13,13 ;WRITE LINE STATE
1Ø1110001  1111111001101110        BRB     1Ø,MU   ;TEST FOR INHIBIT
1Ø1110010  1000000101111011        BRA     1,NU    ;GO BACK TO SEND IDLE

                                   ;SEND DLE FIRST

                                   ;(WE GOT HERE FROM TRANSMIT SERVICE.  THE CONTROL BYTE IS
                                   ;IN ALU RESULT AND B REGISTER.  MASTER SCAN POSITION IS IN
                                   ;RAM ADDRESS REGISTER 0-3).

1Ø1110011  0010000000001110        SDLE    RAM     0,0,10  ;OBTAIN LINE PROTOCOL
1Ø1110100  1111001001111100        BRB     2,CRAM2 ;TEST RAM OUTPUT Ø2, IF YES BRANCH TO CLEAR RAM Ø2
1Ø1110101  0101000000100110        S/C     5,6     ;SET RAM Ø2
1Ø1110110  2010000110111110        RAM     1,13,10 ;MOVE RAM OUTPUT TO RAM INPUT AND WRITE NEW LINE PROTOCOL
1Ø1110111  1111111001110011        BRB     1Ø,SDLE ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
1Ø1111000  0010000000001010        RAM     0,0,12  ;OBTAIN TRANSMITTER DLE / LINE PROTOCOL II
1Ø1111001  0011000010110010        XFR     ,13,2   ;MOVE RAM OUTPUT TO REGISTER B
1Ø1111010  1111100001101110        BRB     1Ø,MU   ;TEST FOR DNA FLAG, IF YES BRANCH TO SENT IDLE/DLE
1Ø1111011  0011000010000ØØØ        NU      XFR     ,10,0   ;MOVE REGISTER B 15-8 TRANSMITTED DATA BUS
1Ø1111100  0000000100000000        BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                   ;CLEAR RAM Ø2 (RAM Ø2 IS DLE SENDING IN PROGRESS)

1Ø1111101  0010000000001110        CRAM2   RAM     0,0,16  ;OBTAIN LINE PROTOCOL
1Ø1111110  0101000000100010        S/C     5,2     ;CLEAR RAM OUTPUT Ø2
1Ø1111111  0010000110111110        RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT DATA AND WRITE NEW LINE PROTOCOL
11Ø000000  1111111001111ØØ1        BRB     1Ø,CRAM2        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø000001  1000000100001110        BRA     1,RDLE  ;TEST FOR SURE TRUE, IF YES BRANCH TO RETURN FROM DLE SENDING

                                   ;SET SEND BCC NEXT

11Ø000010  0010000000001110        SSBN    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
11Ø000011  0101000000100111        S/C     5,7     ;SET RAM OUTPUT BIT Ø
11Ø000100  0010000110111110        RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT AND WRITE NEW LINE PROTOCOL
11Ø000101  1111111010000010        BRB     1Ø,SSBN ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø000110  1000000100010000        BRA     1,RSSBN ;TEST FOR SURE TRUE, IF YES BRANCH TO RETURN FROM SSBCCNXT

                                   ;BCØ SEND BCC

11Ø000111  0010000000001110        BCØSB   RAM     0,0,16  ;OBTAIN LINE PROTOCOL
11Ø001000  0101000000100111        S/C     5,7     ;SET RAM OUTPUT BIT Ø
11Ø001001  0010000110111110        RAM     1,13,16 ;MOVE RAM OUTPUT TO RAM INPUT AND WRITE NEW LINE PROTOCOL
11Ø001010  1111111010000111        BRB     1Ø,BCØSB        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø001011  1000000101010111        BRA     1,CBCØ  ;TEST FOR SURE TRUE, IF YES BRANCH TO CBCØ
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                                   ;ODDMP TRANSMIT

11Ø001100  0010000000001100        ODDMX   RAM     0,0,14  ;OBTAIN TRANSMITTER MODE BITS
11Ø001101  1111110010001111        BRB     14,XBCC ;TEST RAM 0-14=0, IF YES BRANCH TO XBCC
11Ø001110  1000000100000000        BRA     1,PI    ;TEST FOR SURE TRUE, IF YES BRANCH TO PI

                                   ;CALCULATE TRANSMITTER BCC

11Ø001111  0011000011010001        XBCC    XFR     ,15,1   ;MOVE DATO REGISTER TO A REGISTER
11Ø010000  0010000000000110        RAM     0,0,6   ;OBTAIN TRANSMITTER BCC CALCULATED TO DATE
11Ø010001  0011000010110010        XFR     ,13,2   ;MOVE RAM DATA TO REGISTER B
11Ø010010  0010000000001010        RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II
11Ø010011  0110000000000000        BCC             ;PERFORM SPECIFIED BCC CALCULATION
11Ø010100  0010000111100110        RAM     1,16,6  ;MOVE BCC TO RAM INPUT AND WRITE NEW TRANSMITTER BCC
11Ø010101  1000000100010001        BRA     1,RXBCC ;TEST FOR SURE TRUE, IF YES, BRANCH TO RETURN FROM XMIT BCC

                                   ;SEND BCC 1

                                   ;(WE GOT HERE FROM TRANSMIT SERVICE.  THE MASTER SCAN POSITION
                                   ;IS IN THE RAM ADDRESS REGISTER 0-3.  THE LINE PROTOCOL IS IN
                                   ;THE A REGISTER AND THE ALU RESULT REGISTER.)

11ØØ10110  0010000000001110        SBC1    RAM     0,0,16  ;OBTAIN LINE PROTOCOL
11Ø010111  0011000010110001        XFR     ,13,1   ;MOVE RAM OUTPUT TO A REGISTER
11Ø011000  0001000000111111        ALU     77      ;LET ALU RESULT = A PLUS 1
11Ø011001  0010000111111110        RAM     1,17,16 ;MOVE ALU RESULT TO RAM INPUT DATA AND WRITE NEW LINE PROTOCOL
11Ø011010  1111111010010110        BRB     1Ø,SBC1 ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø011011  0010000000001110        RAM     0,0,6   ;OBTAIN TRANSMITTER BCC
11Ø011100  0011000010110000        XFR     ,13,0   ;MOVE RAM OUTPUT DATA TO TRANSMITTED DATA BUS (HIGH ORDER BITS GO INT
11Ø011101  0010000000010010        RAM     0,0,12  ;OBTAIN TRANSMITTER DLE/LINE PROTOCOL II (TO LOOK FOR LRC)
11Ø011110  1111001110100001        BRB     3,GOIDL ;TEST RAM OUTPUT Ø3, IF YES BRANCH TO HERE +Ø
11Ø011111  1111010010100001        BRB     4,GOIDL ;TEST RAM OUTPUT Ø4, IF YES BRANCH TO HERE +3
11Ø100000  1000000110100101        BRA     1,C/LU1 ;TEST FOR SURE TRUE, IF YES BRANCH TO SEND BCC 2 + 6
11Ø100001  0000000100000000        GOIDL   BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                   ;SEND BCC2

                                   ;(WE GOT HERE FROM TRANSMIT SERVICE.  THE MASTER SCAN POSITION
                                   ;IS IN THE RAM ADDRESS REGISTER 0-3.  THE LINE PROTOCOL IS IN
                                   ;THE A REGISTER AND IN THE ALU RESULT REGISTER.)

11Ø100010  0010000000000110        SBC2    RAM     0,0,6   ;OBTAIN TRANSMITTER BCC
11Ø100011  0011000010110010        XFR     ,13,2   ;MOVE RAM OUTPUT DATA TO REGISTER B
11Ø100100  0011000010000000        XFR     ,10,0   ;MOVE REGISTER B 0-15/0-7 TO TRANSMITTED DATA BUS

11Ø100101  0010000100000110        C/LU1   RAM     1,0,6   ;MOVE ZERO TO RAM INPUT DATA AND WRITE ZERO TRANSMITTER BCC
11Ø100110  0010000000001110        RAM     0,0,16  ;OBTAIN LINE PROTOCOL
11Ø100111  0101000000100001        S/C     5,1     ;CLEAR RAM BIT Ø1 (SEND BCC 2)
11Ø101000  0010000110111110        RAM     1,13,16 ;MOVE RAM INPUT TO RAM INPUT DATA AND WRITE NEW LINE PROTOCOL
11Ø101001  1111111010010101        BRB     1Ø,C/LU1        ;TEST FOR WRITE INHIBIT, IF YES BRANCH BACK
11Ø101010  0000000100000000        BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP
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                                        ;RECEIVED ERRORS

                                        ;CONTROL BYTE INTERRUPT

1101010111  0010000000001111    CBINT   RAM     0,0,17  ;READ CONTROL BYTE HOLDING REGISTER
1101011001  0101000000100011            S/C     5,3     ;CLEAR RAM 00 (GENERATE INTERRUPT)
1101011011  0010000111011111            RAM     1,13,17 ;WRITE CONTROL BYTE HOLDING REGISTER
1101011100  0011000011000110            XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER
1101011110  0101000000001011            S/C     3,3     ;SET SCR07 (RECEIVER INTERRUPT)
1101100000  0220000100000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP

                                        ;PARITY AND OVERRUN ERRORS

1101100001  0011000011000110    POER    XFR     ,14,6   ;MOVE SILO OUT TO RICR REGISTER

                                        ;CREATE NULL ACTION CONTROL BYTE (MODE IS PRESERVED)

1101100010  0010000000001111    CNACB   RAM     0,0,17  ;READ CONTROL BYTE HOLDING REGISTER
1101100011  0101000000100011            S/C     5,3     ;CLEAR RAM 00
1101100100  0101000000100001            S/C     5,1     ;CLEAR RAM 01
1101100101  0101000000102010            S/C     5,2     ;CLEAR RAM 02
1101100110  0101000000100000            S/C     5,0     ;CLEAR RAM 03
1101100111  0101000010000111            S/C     7,7     ;SET RAM OUTPUT 04 (DISCARD)
1101101000  0010000111011111            RAM     1,13,17 ;WRITE CONTROL BYTE HOLDING REGISTER FROM RAM OUTPUT
1101101001  0101000000601011            S/C     3,3     ;SET SCR 07 (RECEIVER INTERRUPT)
1101101010  0000000100000000            BRA     1,ILOOP ;TEST FOR SURE TRUE, IF YES BRANCH TO IDLE LOOP


                                        ;END
```
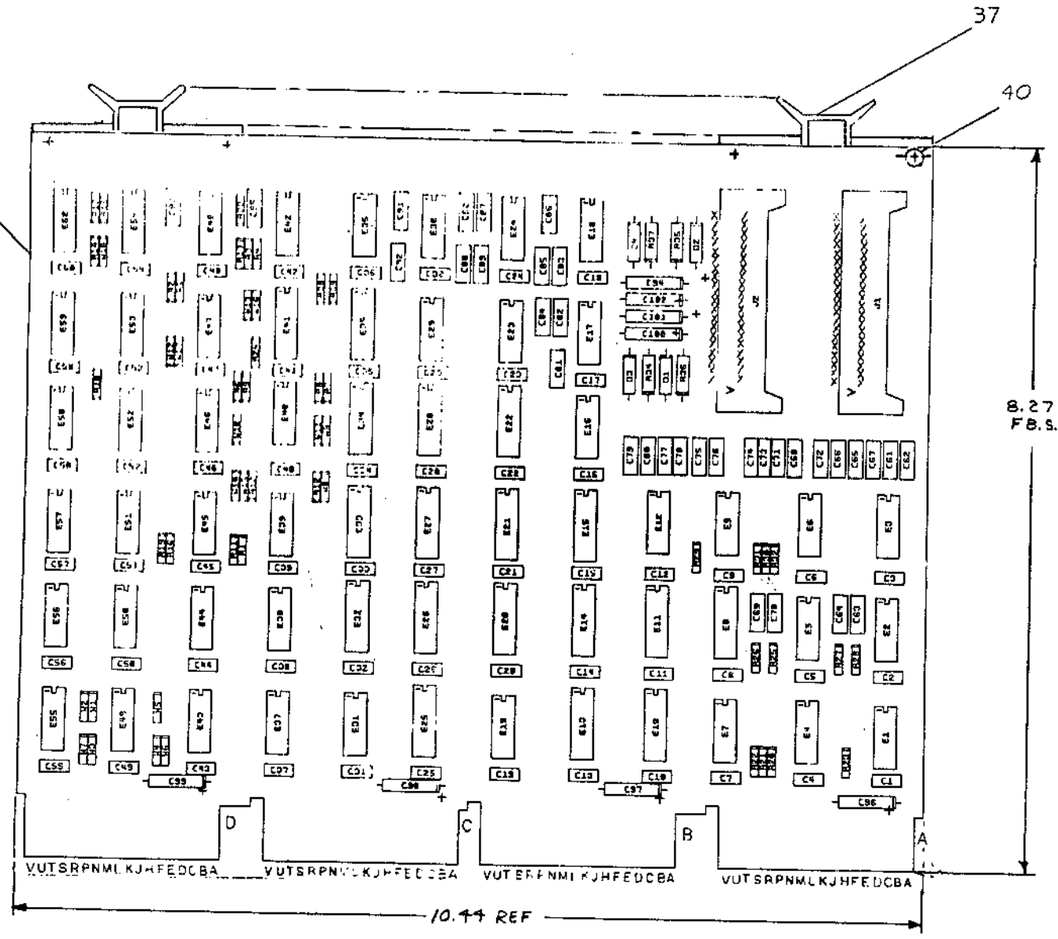

NOTES:

1. ALL UNUSED PINS ON J1, J2 GO TO GND



JUMPER TABLE

JUMPER	BIT	
W1	D00	JUMPER REMOVED INTERRUPT VECTOR = 0
W2	D02	
W3	D03	
W4	D06	
W5	D07	
W6	D05	
W7	D04	
W8	A12	JUMPER REMOVED DEVICE SELECT = 1
W9	A09	
W10	A08	
W11	A10	
W12	A04	
W13	A05	
W14	A11	
W15	A03	
W16	A06	
W17	A07	

REF			
		X-Y COORDINATE HOLE LOCATION	K-CO-M7807-0-4
REF		ASSY DRILLING HOLE LAYOUT	D-AH-M7807-0-5
REF		MODULE ECO HISTORY	B-MH-M7807-0-6
1		ETCHED CIRCUIT BOARD	5010883
8	C94,C96—C102	CAP 6.8 UF 35V 10%	1005306
60	C1-C60	CAP .01 UF 100V 20%	1001610-00
33	C61—C93	CAP 470 MMF 100V 5%	1000024
1	C95	CAP 330 PF 100V 5%	1000023
4	D1,D2 D3, D4	DIODE IN4733A	1109543
17	R1-R13,R15,R17,R18, R24	RES 1K 1/4W 5%	1300365
1	R14	RES 100 1/4W 5%	1300229
1	R33	RES 47 1/4W 5%	1300202
1	R19	RES 180 1/4W 5%	1301322
5	R20-R23, R39	RES 750 1/4W 5%	1301481
8	R25-R32	RES 33K 1/4W 10%	1300510
1	R16	RES 390 1/4W 5%	1300303
4	R34,R35 R36, R37	RES 330 1/2W 5%	1300224
1	E52	I.C. DEC 7408	1910155
1	E4	I.C. DEC 7417	1909929
8	E12,E18 E23,E29,E36,E42	I.C. DEC 1489L	1910022
8	E3,5,6,8,12,17,24,30	I.C. DEC 1489L	1910023
8	E9,11,14,15,20,21,22,28	I.C. DEC 74151	1909936
8	E10,13,25,28,32,33,34,35	I.C. DEC 74175	1910651
1	E19	I.C. DEC 7410	1905576
1	E27	I.C. DEC 7442	1910046
6	E1,E7,E43,E51,E55,E60	I.C. DEC 8881	1909705
2	E56, E59	I.C. DEC 7400	1905575
7	E31,E37, E41,E45,E46 E53, E54	I.C. DEC 7440	1910469
1	E58	I.C. DEC 7474	1905547
1	E2	I.C. DEC 74H04	1909931
1	E44	I.C. DEC 74H00	1909956
3	E39, E40, E47	I.C. DEC 8242	1909710
1	E61	I.C. DEC 74123	1910436
1	E48	I.C. DEC 74H74	1909867
1	E38	I.C. DEC 8815	1909713
2	E50 E57	I.C. DEC 7402	1909004
4		HANDLE FLIP CHIP	9008337-8
2	J1,J2	40 PIN HEADER	1209841
18	W1-W18	JUMPER (INSULATED)	9009185
4		EYELET HANDLE	SCC6732
1	R38	RES 33Ω 1/4W 5%	1100255

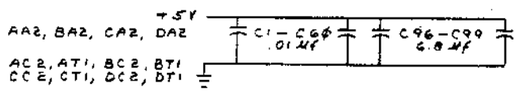
QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO

PARTS LIST

DEC 8641	1	8
DEC IC 7442	8	16
DEC IC 74175	8	16
DEC IC 74151	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS



DEC NO	EIA NO	DEC NO	EIA NO

SEMICONDUCTOR CONVERSION CHART

REV	CHANGE NO	CHK
D		
C		

REVISIONS

W. FANAZICK
M7807-0000I
PINNATE

DRN. — DATE 12/3/74
CHK'D — DATE 3/4/74
ENG. — DATE 3/4/74
PROJ ENG. — DATE 3-20-74
PROD. — DATE 3-20-74
NEXT HIGHER ASSY
SCALE
SHEET 1 OF 7

digital EQUIPMENT CORPORATION

TITLE: BUS CONTROL & MUX

SIZE	CODE	NUMBER	REV.
D	CS	M7807-0-	D

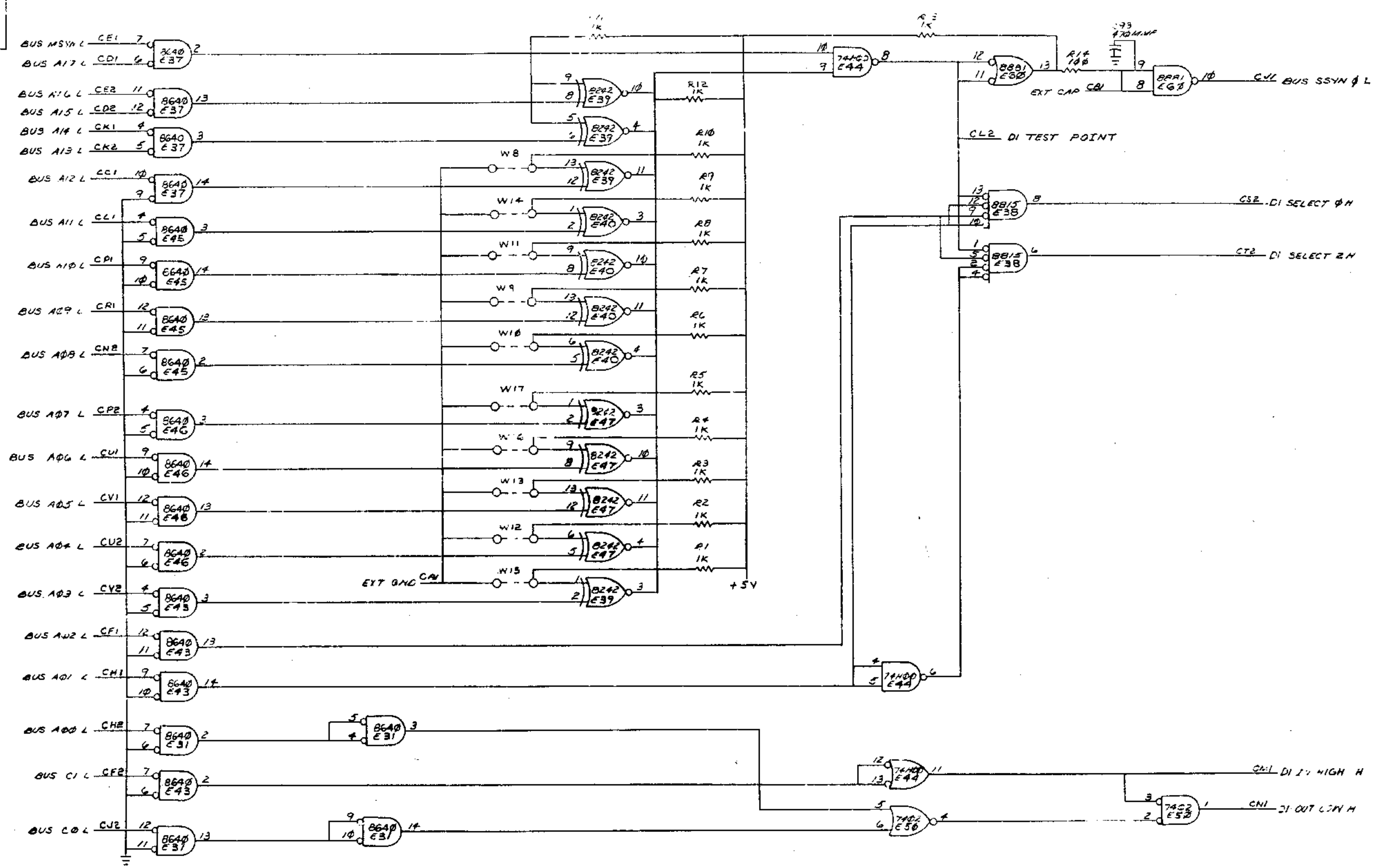
DIST.

DEC/M7807-0-

*INST USED ON OPTION MODEL

ETCH BOARD REV D

310



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE BUS CONTROL & MUX (D1)

SIZE D CODE CS NUMBER M7807-0-1 REV. D

SCALE — SHEET 1 OF 7

D CS M7807-0-1 D

D7 INT A H DR2 — 7406 E56 — 7402 E57 — 7402 E57 — 7402 E57 — DR1 BUS B AK L

D7 INT ENB A H DR1 — 7406 E56 — 7402 E57

D2 INTR DONE B H DS1 — 7402 E57

WIB — R15 1K — +5V

BUS NPR L DC1 — 8640 E54 — 8640 E54

BUS B BG IN H DE1 — R16 390 — 8640 E54 — 7400 E59 — 7400 E59

74H04 E2

74H74 E48 — 7400 E59

+5V R18 1K — 8881 E60 — 74S74 E58 SACK — 7403 E57

+5V R17 1K — A33 47 — C95 33PF — 8881 E60 — 74HC4 E2 — 74H04 E2

7474 E56 — 7408 E52

74S74 E58 BBSY — 7400 E59 — 8881 E51 — DS2 D2 MASTER B L

8881 E51 — DR1 BUS B AK L

+5V R19 1K — 8881 E51 — DA1 BUS A BG IN H

8881 E51 — IDT2 BUS SACK L

D7 INT A H DD2 — 8881 E55 — IN2 BUS IDT2 L

8881 E55 — IN3 BUS DR1 L

8881 E55 — IN7 SYNC BUS CON L

8881 E55 — IN6 DF1 BUS CDS L

8881 E49 — CAN BUS INTR L

8881 E49 — IN4 DF2 BUS CDG L

8881 E49 — IN5 DM1 BUS DG7 L

8881 E49 — IN1 DM1 BUS DG8 L

7402 E58 — DM2 ENTR DONE B H

BUS BBSY L DD1 — 8640 E53 — 8640 E53 — 7408 E52

BUS SSYN L DC1 — 8640 E53 — 7402 E58

D2 MASTER B L — DR2 DP2 — 74H00 E44

REVISIONS		
CHK	CHANGE NO	REV.

TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (D2)	D	CS	M7807-0-1	D
SCALE —	SHEET 3 OF 7	DIST.		

DCS-M7807-2-1

D1 SELECT 2 H BF2 — R24 1K — +5V — R39 75Ø — R38 33Ø — 74123 E41 — D1 OUT LOW H BR2 — D1 GROUP 8-15 H BR2 — 7410 E19

(INTR STATUS H) { D5 MUX LINE EN H, D8 CLEAR CYCLE L, D7 GROUP 8-15 H } BF2 — 7410 E19 — 74H24 E2 — D3 EN MUX H

D7 LINE CNT MSB H BK2 — 7417 E4 — R22 75Ø
D7 LINE CNT 4 H BL2 — 7417 E4 — R21 75Ø
D7 LINE CNT LSB H BM2 — 7417 E4 — R20 75Ø

74LS C27 LINE DOOR (D3) — D3 CLOCK 15 L … D3 CLOCK 8 L

74151 E8 RING SELECTOR — D6 RING 8 L … D6 RING 15 L — 7 — 10 — 11 — 6 — 5

1488 E7 — BF2 — D3 MUX RING L

D3 B LINE CNT MSB H
D3 M LINE CNT 4 H
D3 F LINE CNT LSB H

J1

1488 E42 — D3 SEC TX 8 H — D3 TERM RDY 8 H — D3 RQ TO SEND 8 H

1488 E18 — D3 SEC TX 9 H — D3 TERM RDY 9 H — D3 RQ TO SEND 9 H

1488 E29 — D3 SEC TX 10 H — D3 TERM RDY 10 H — D3 RQ TO SEND 10 H

1488 E42 — D3 SEC TX 11 H — D3 TERM RDY 11 H — D3 RQ TO SEND 11 H

D7 CØØ H BN1 — D7 CØ1 H BP1 — D7 CØ2 H BK2 — D7 CØ3 H BM2

74175 E32 LINES 8 — D3 LINE EN 8 L — D3 SEC TX 8 L — D3 TERM RDY 8 L — D3 RQ TO SEND 8 L — D3 INI L

74175 E25 LINES 9 — D3 LINE EN 9 L — D3 SEC TX 9 L — D3 TERM RDY 9 L — D3 RQ TO SEND 9 L — D3 INI L

74175 E33 LINES 10 — D3 LINE EN 10 L — D3 SEC TX 10 L — D3 TERM RDY 10 L — D3 RQ TO SEND 10 L — D3 INI L

74175 E28 LINES 11 — D3 LINE EN 11 L — D3 SEC TX 11 L — D3 TERM RDY 11 L — D3 RQ TO SEND 11 L — D3 INI L

DT CLEAR MUX L — BJ1 — 7417 E4 — R23 75Ø — +5V — D3 INI L

TO PIN 1 OF E16, E23, E27 488 IC'S — AB2 BB2 — D1 IN4733A — -15V — C10Ø 6.8 MFD — R34 33Ø — -10V A

TO PIN 14 OF E16, E23, E29 1488 IC'S — AU1 — D2 IN4733A — +15V — C101 6.8 MFD — R35 33Ø — +10V A

TO PIN 1 OF E18, E36, E42 1488 IC'S — AB2 BB2 — D3 IN4733A — -15V — C102 6.8 MFD — R36 33Ø — -10V B

TO PIN 14 OF E18, E33 E42 — AU1 — D4 IN4733A — +15V — C103 6.8 MFD — R37 33Ø — +10V B

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
BUS CONTROL & MUX (D3)	D	CS	M7827-2-	D
SCALE 1/1 — SHEET 4 OF 7 — DIST.				

D CS M7827-2-1 D

D3 EN MUX H

D3 B LINE CNT LSB H
D3 B LINE CNT * H
D3 B LINE CNT MSB H

D6 CARRIER 8 L
D6 CARRIER 9 L
D6 CARRIER 10 L
D6 CARRIER 11 L
D6 CARRIER 12 L
D6 CARRIER 13 L
D6 CARRIER 14 L
D6 CARRIER 15 L

57B 74151 E22 CARRIER SELECTOR f0

8881 E7

B81

D4 MUX CARRIER L

D6 CLEAR TO SEND 8 L
D6 CLEAR TO SEND 9 L
D6 CLEAR TC SEND 10 L
D6 CLEAR TO SEND 11 L
D6 CLEAR TO SEND 12 L
D6 CLEAR TO SEND 13 L
D6 CLEAR TO SEND 14 L
D6 CLEAR TO SEND 15 L

57B 74151 E15 CLEAR TO SEND SELECTOR f0

8881 E7

B81

D4 MUX CLEAR TO SEND L

D5 SEC RX 8 L
D6 SEC RX 9 L
D6 SEC RX 10 L
D6 SEC RX 11 L
D6 SEC RX 12 L
D6 SEC RX 13 L
D6 SEC RX 14 L
D6 SEC RX 15 L

57A 74151 E21 SEC RX SELECTOR f0

8881 E7

B81

D4 MUX SEC RX L

1488 E16

D4 SEC TX 12 H
D4 TERM RDY 12 H
D4 RQ TO SEND 12 H

74175 E24 LINES 12

D4 LINE EN 12 L
D4 SEC TX 12 L
D4 TERM RDY 12 L
D4 RQ TO SEND 12 L

D3 INI L
D3 CLOCK 12 L

1488 E36

D4 SEC TX 13 H
D4 TERM RDY 13 H
D4 RQ TO SEND 13 H

74175 E35 LINES 13

D4 LINE EN 13 L
D4 SEC TX 13 L
D4 TERM RDY 13 L
D4 RQ TO SEND 13 L

D3 INI L
D3 CLOCK 13 L

1488 E23

D4 SEC TX 14 H
D4 TERM RDY 14 H
D4 RQ TO SEND 14 H

74175 E18 LINES 14

D4 LINE EN 14 L
D4 SEC TX 14 L
D4 TERM RDY 14 L
D4 RQ TO SEND 14 L

D3 INI L
D3 CLOCK 14 L

D7 D06 H (BN1)
D7 D03 H (B7)
D7 D01 H (B P1)
D7 D02 H (B M2)

J2

REVISIONS

CHK	CHANGE NO	REV.

TITLE BUS CONTROL 1/2 MUX (D4)
SIZE D CODE CS NUMBER M7807-0-1 REV. D
SCALE 1/1 SHEET 5 OF 7 DIST.

M7807-2-1 D

D3 LINE EN 8 L
D3 LINE EN 9 L
D3 LINE EN 10 L
D3 LINE EN 11 L
D4 LINE EN 12 L
D4 LINE EN 13 L
D4 LINE EN 14 L
LINE EN 15 L

S7B 74151 E14 LINE EN SELECTOR

D5 MUX LINE EN L
D5 MUX LINE EN H

D3 SEC TX 8 L
D3 SEC TX 9 L
D3 SEC TX 10 L
D3 SEC TX 11 L
D4 SEC TX 12 L
D4 SEC TX 13 L
D4 SEC TX 14 L
SEC TX 15 L

S7B 74151 E11 SEC TX SELECTOR

D5 MUX SEC TX L

J2
D5 SEC TX 15 H
D5 TERM RDY 15 H
D5 RQ TO SEND 15 H

1488 E16
1488 E36
1488 E23

74175 E13 LINES 15

D7 D00 H
D7 D03 H
D7 D01 H
D7 D02 H
D3 INIT L
D3 CLOCK 15 L

TERM RDY 15 L

D3 TERM RDY 8 L
D3 TERM RDY 9 L
D3 TERM RDY 10 L
D3 TERM RDY 11 L
D4 TERM RDY 12 L
D4 TERM RDY 13 L
D4 TERM RDY 14 L

S7B 74151 E26 TERM RDY SELECTOR

D5 MUX TERM RDY L

D3 RQ TO SEND 8 L
D3 RQ TO SEND 9 L
D3 RQ TO SEND 10 L
D3 RQ TO SEND 11 L
D4 RQ TO SEND 12 L
D4 RQ TO SEND 13 L
D4 RQ TO SEND 14 L
RQ TO SEND 15 L

S7B 74151 E39 RQ TO SEND SELECTOR

D5 MUX RQ TO SEND L

D3 B LINE CNT MSB H
D3 B LINE CNT + H
D3 B LINE CNT LSB H

(R/W STATUS) D7 GROUP 8-15 - H

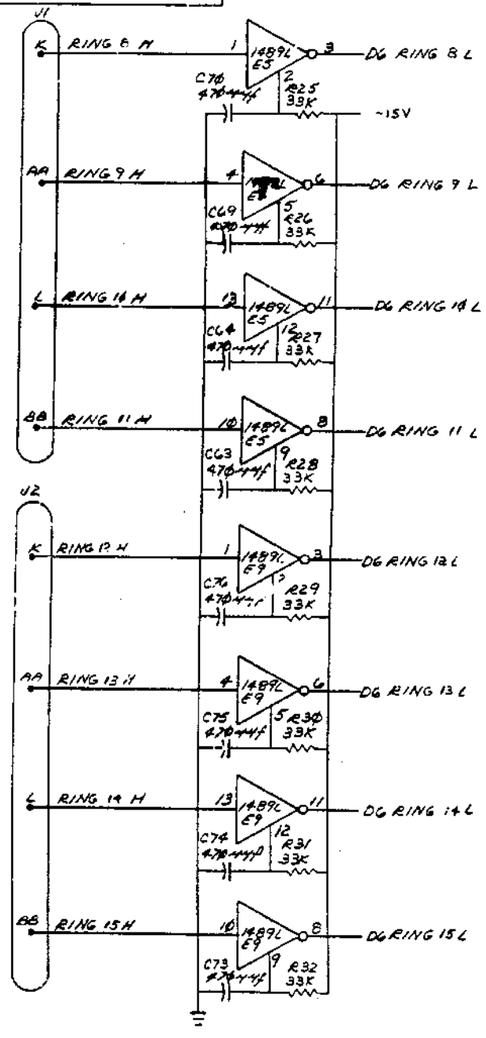
74100 E19
74H04 E2

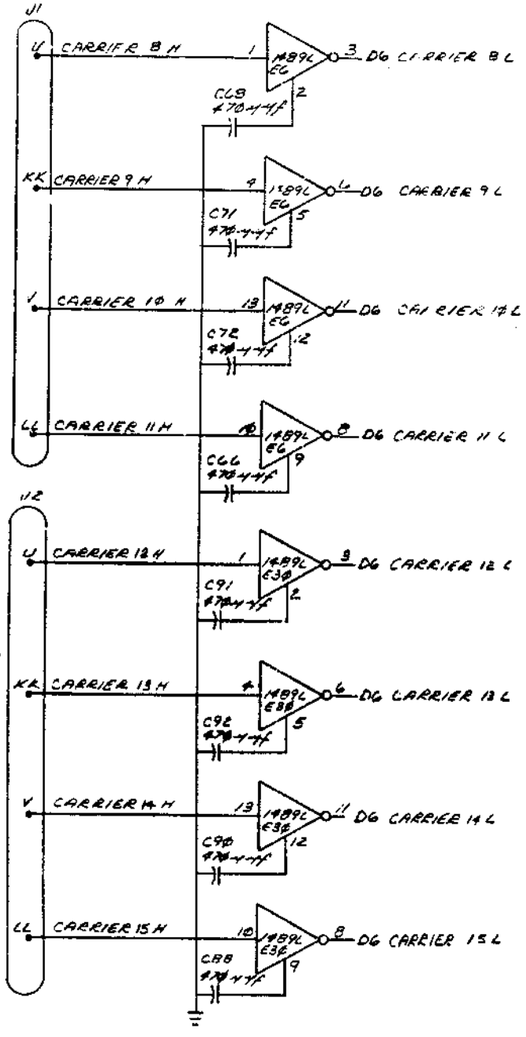
D5 EN RHT H

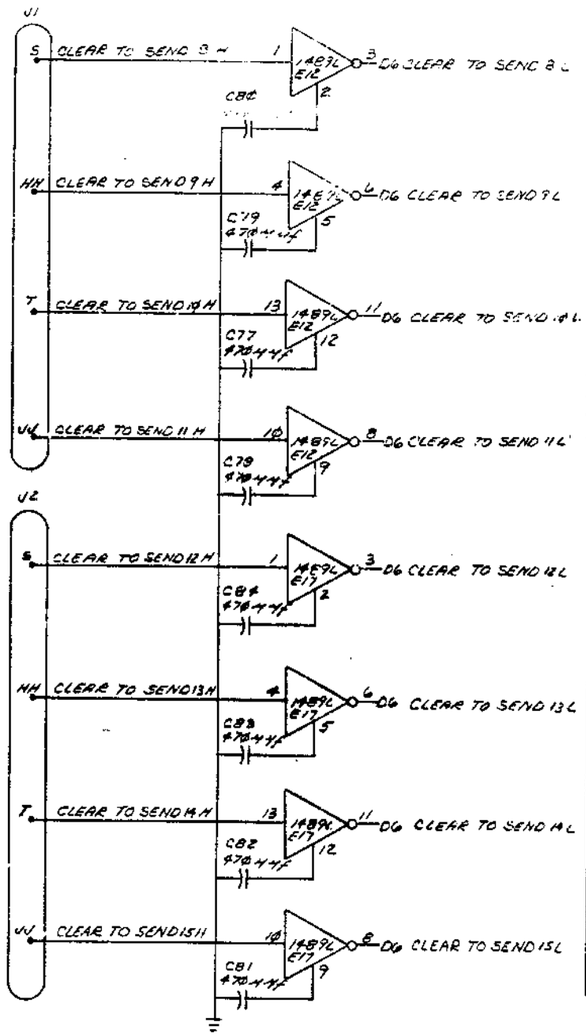
8881 E1

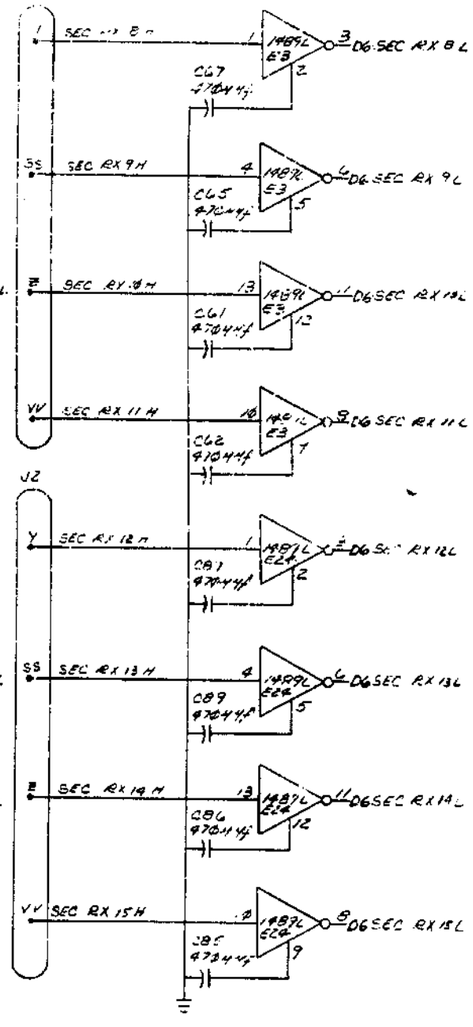
REVISIONS		
CHK	CHANGE NO	REV.

TITLE: BUS CONTROL & MUX (05)
SIZE: D | CODE: CS | NUMBER: M7807-0- | REV: D
SCALE | SHEET 6 OF 7 | DIST.









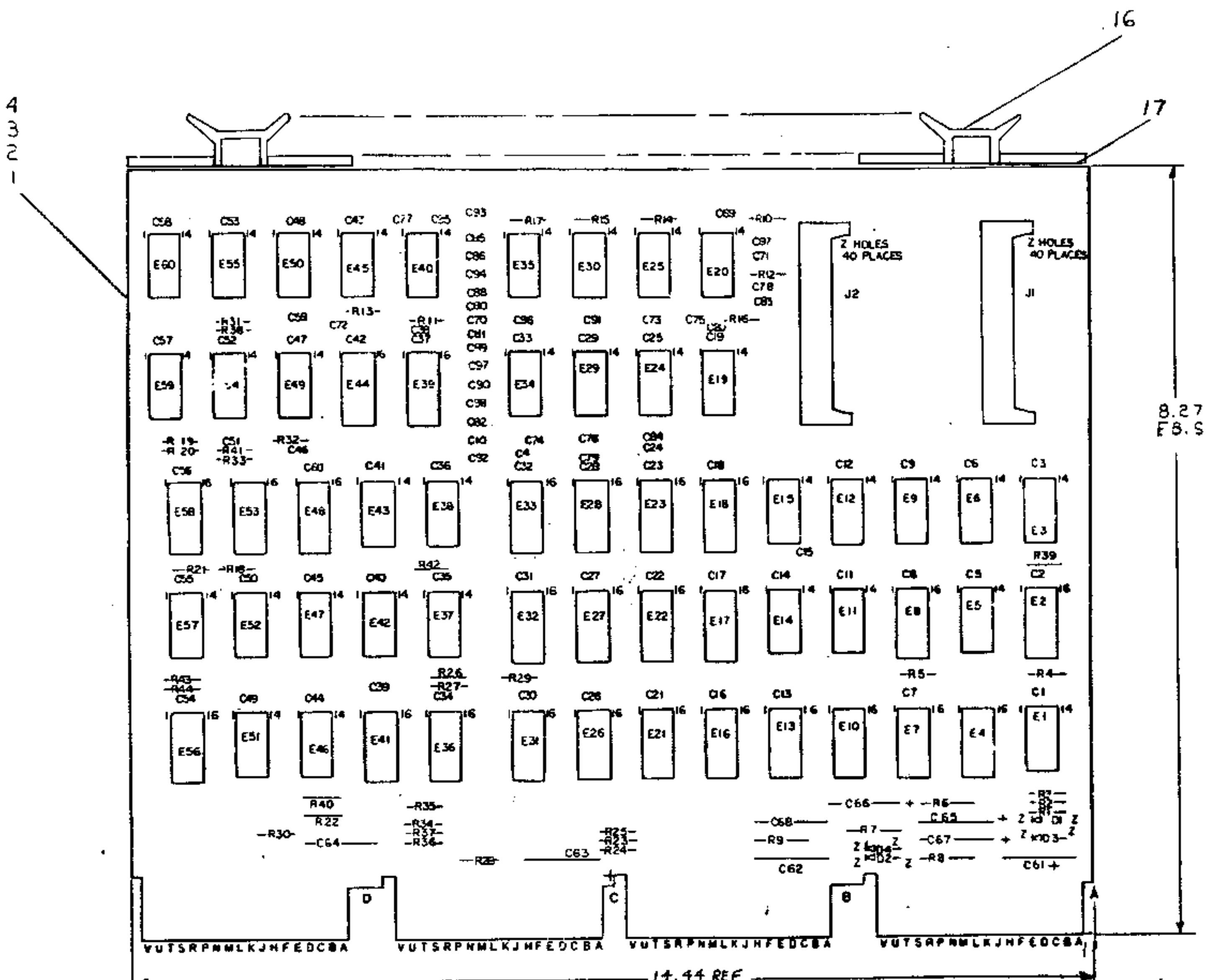
REVISIONS		
CHK	CHANGE NO.	REV

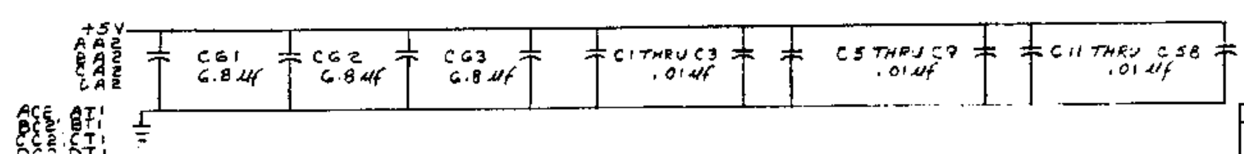
TITLE	SIZE	CODE	NUMBER	REV.
BUS CONTROL & MUX (DE)	D	CS	M7807-0-1	D
SCALE	SHEET 7 OF 7	DIST.		

CS M7807-0-1 D

NOTES:

1. FOR -15V TO -10V AND +15V TO +10V SEE SHEET 7 OF 7





QTY	REF DESIGNATION	DESCRIPTION	PART NO	ITEM NO
		X-Y COORDINATE HOLE LOCATION	K-CO-M7808-Ø-4	1
		ASSY. DRILL HOLE LAYOUT	D-AH-M7808-Ø-5	2
		MODULE ECO HISTORY	B-MH-M7808-Ø-6	3
1		ETCHED CIRCUIT BOARD	5010884	4
56	C1-3,5-9,11-58	CAP .01 UF, 100V, ± 20%	1001610-00	5
33	C4,10,59,69-98	CAP 470 PF, 100V, ± 5%	1000024	6
1	C60	CAP 82 PF, 100V, ± 5%	1000015	7
8	C61 THRU C68	CAP 6.8 UF, 35V, ± 10%	1005306	8
4	D1,2,3,4	DIODE 1N4733A ZENER	1109943	9
2	J1,J2	CONNECTOR 40 PIN	1209941	10
[illegible]	R1-4,18-30,32-[illegible]	RES. 750 1/4W 5%	1301401	11
1	R31	RES. 220 1/4W 5%	1300271	12
8	R10-17	RES. 33K 1/4W 10%	1300510	13
4	R6,7,8,9	RES. 330 1/2W 5%	1300296	14
1	R44	RES. 330 1/4W 5%	1300295	15
4		HANDLE FLIP CHIP	9008337-08	16
8		EYELET	9006732	17
1	E50	I.C. DEC 7474	1905547	18
8	E19,20,24,25,29,30,34,35	I.C. DEC 1489L	1910323	19
8	E17,18,22,23,27,28,32,33	I.C. DEC 74151	1909936	20
8	E4,7,10,13,16,21,26,31	I.C. DEC 74175	1910651	21
6	E5,6,9,11,12,15	I.C. DEC 1488	1910322	22
2	E14,49	I.C. DEC 7410	1905576	23
1	E2	I.C. DEC 7442	1910046	24
2	E1,42	I.C. DEC 7417	1909929	25
1	E8	I.C. DEC 74123	1910436	26
4	E3,38,54,60	I.C. DEC 8881	1909705	27
2	E36,53	I.C. DEC 8266	1909934	28
2	E41,44	I.C. DEC 8838	1911117	29
1	E46	I.C. DEC 8640	1911469	30
1	E51	I.C. DEC 7416	1909928	31
1	E56	I.C. DEC 7489	1910398	32
1	E37	I.C. DEC 74197	1910035	33
2	E45,47	I.C. DEC 7400	1905575	34
1	E52	I.C. DEC 7408	1910155	35
2	E55,57	I.C. DEC 8815	1909713	36
2	E40,43	I.C. DEC 7404	1909686	37
1	E48	I.C. DEC 8271	1909615	38
2	E39,58	I.C. DEC 4015	1910087	39
1	E59	I.C. DEC 7486	1910011	40
2	R5,39	[illegible] 1/4W, 5%	[illegible]	41

PARTS LIST

ETCH BOARD REV D

FIRST USED ON OPTION MODEL

IC TYPE	GND	+5V
DEC 4015	8	16
DEC 8271	8	16
DEC 7489	8	16
DEC 8640	1	8
DEC 8266	8	16
DEC 74123	8	16
DEC 7442	8	16
DEC 74175	8	16
DEC 74151	8	16

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

DEC NO	EIA NO	DEC NO	EIA NO

SEMICONDUCTOR CONVERSION CHART

REVISIONS: REV D — CHANGE NO M7808-00001 — ORIG

DRN. E. Wilson DATE 7/13/74
CHK'D DATE
ENG. W. L. Fanazick DATE
PROJ. ENG. W. L. Fanazick DATE
PROD. DATE 7-25-74
NEXT HIGHER ASSY

digital EQUIPMENT CORPORATION

TITLE: MODEM CONTROL

SIZE D, CODE C, NUMBER M7808-Ø-1, REV. D

SCALE NONE — SHEET 1 OF 7

DIST

NOTE:

* REMOVE WIRE TO INHIBIT INTERUPTS FROM TRANSITIONS.

DI1 D5 MUX SEC TX L CR2
DI1 D5 MUX RQ TO SEND L CN2
DI1 D5 MUX TERM RDY L CS2
DI1 D5 MUX LINE EN L CP2
DI SELECT 2 H DL2
DI IN HIGH H DE2
DI SELECT Ø H DF2
DI OUT LOW H DN2
BUS INITIALIZE L DD1
INT EN L DB2
DB MUX CLEAR TO SEND L
DB MUX RING L
DB MUX CARRIER L
DB MUX SEC RX L

BUS DATA Ø3 L (CJ1)
BUS DATA Ø2 L (CB2)
BUS DATA Ø1 L (CK1)
BUS DATA ØØ L (CE1)
BUS DATA Ø4 L
BUS DATA 11 L
BUS DATA Ø5 L (CV1)
BUS DATA Ø6 L (DA1)
BUS DATA Ø7 L (CR1)
BUS DATA Ø9 L (CV2)
BUS DATA ØØ L
BUS DATA Ø8 L

D7 RD SCAN STATUS H
D7 INT A H
D7 MAINT MODE (1) H
D7 CLEAR SCAN L
DONE (1) H
INTR EN (1) H
SCAN EN (1) H
LINE INCR H (DN1)
D7 LD HOLD H (DP1)
DB CLR CYCLE (Ø) L
INH CLK L (DH2)
EXT CLOCK L (DK2)
DB TRANS DET H
INTR TEST H (DM1)
OUT WRITE H (CL1)
DII MUX LINE EN L (CP2)

D7 DØØ H (CF2)
D7 DØ1 H (CE2)
D7 DØ2 H (CH2)
D7 DØ3 H (CD2)
D7 GROUP Ø-7 H (CP1)
D7 GROUP 8-15 H (CF1)
D7 LINE CNT MSB H (CN1)
D7 LINE CNT +H (CL1)
D7 LINE CNT LSB H (CM1)
D7 CLEAR SCAN L
DM2 D7 CLEAR MUX L

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
MODEM CONTROL (D7)	D	CS	M78Ø8-Ø-1	D
SCALE	SHEET 2 OF 7	DIST.		

DCS M7808-0-1 D

+3V

D7 LINE CNT +H
D7 LINE CNT MSB H
D7 GROOP 8-15 H
D7 LINE CUNT LSB H
8815 E27
7412 E49
D7 CLEAR SCAN L
DR1 D8 CLEAR CYCLE (Ø) L

+5V D7 LD HOLD H DV1
7404 E40
+5V

R23 R24 R25 R22 750Ø
R18 R19 R22 R21 750Ø

D7 MAINT MODE(1) H
7416 E51
D4,DIØ MUX CLEAR TO SEND L (CD1)
D4,DIØ MUX CARRIER L (CA1)
D3,D9 MUX RING L (CC1)

D4,DIØ MUX SEL RC L (CB1)
7489 E50
W E
A3 A2 A1 AØ
D7 GROOP 8-15 H DV2
D7 LINE CNT MBS H DU2
D7 LINE CNT +H DU1
D7 LINE CNT LSB H DS1

4Ø15 E58
SET 3 SET 2 SET 1 SET Ø
CLR CLK
+3V

D7 LD HOLD H DP1

7486 E59
7408 E52
7404 E40

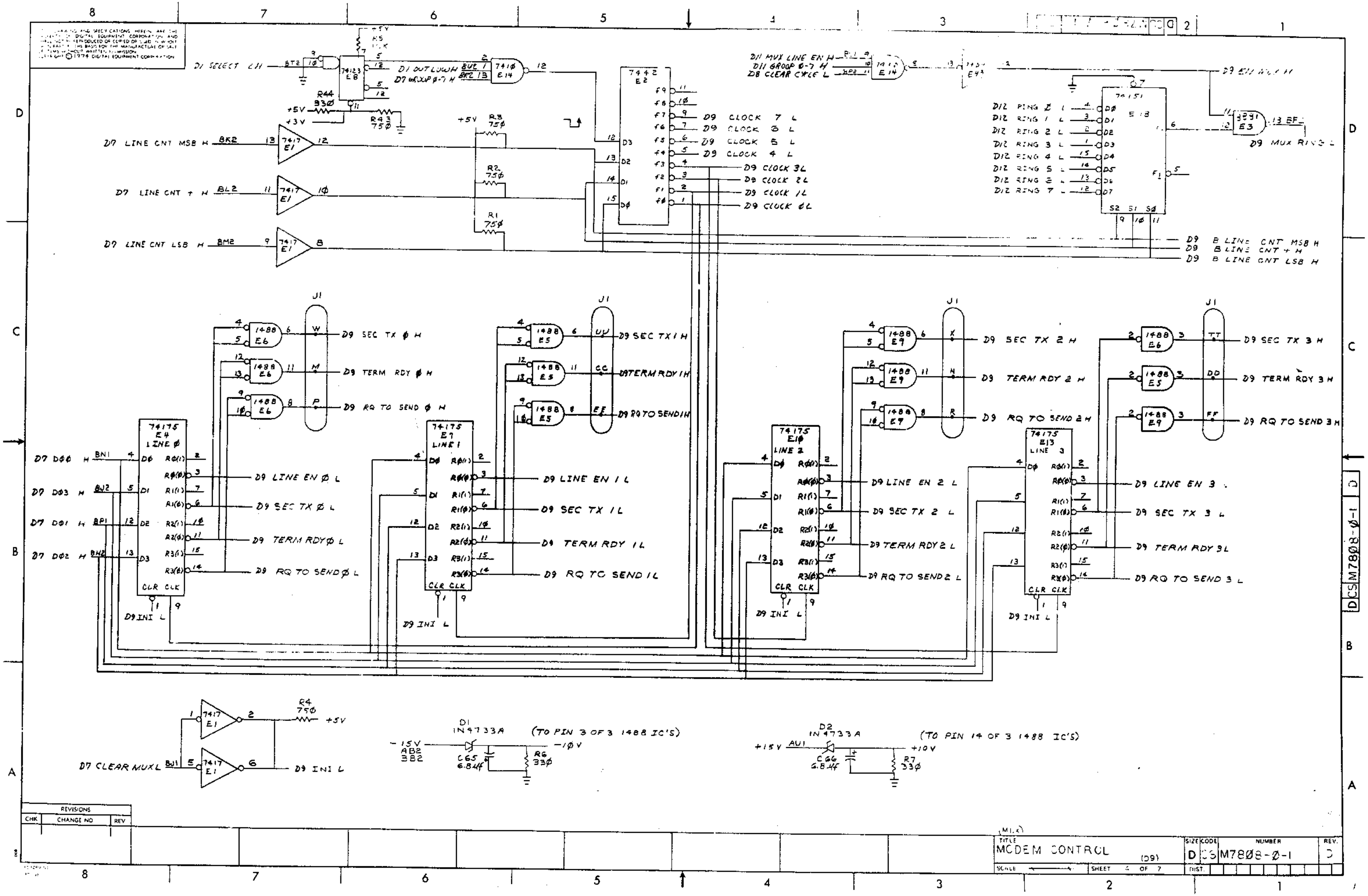
D7 RD SCAN STATUS H
8881 EGØ
8815 E55
+3V
7486 E59

DR2 D8 BUS DATA 12 L
DT2 D8 BUS DATA 13 L
DS2 D8 BUS DATA 14 L
DP2 D8 BUS DATA 15 L
D8 TRANSITION DET H

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
VCCEM CONTROL (D8)	D	CS	M7808-Ø-1	D
SCALE	SHEET 3 OF 7	DIST.		

DCS M7808-Ø-1 REV D


D1 SELECT L H
74123 E8
R5 1K
R44 330
R43 750
D1 OUT LOW H
D7 GROUP 0-7 H
7410 E14
7442 E2
D7 LINE CNT MSB H
D7 LINE CNT + H
D7 LINE CNT LSB H
7417 E1
R3 750
R2 750
R1 750
D9 CLOCK 7 L
D9 CLOCK 6 L
D9 CLOCK 5 L
D9 CLOCK 4 L
D9 CLOCK 3 L
D9 CLOCK 2 L
D9 CLOCK 1 L
D9 CLOCK 0 L
D11 MUX LINE EN H
D11 GROUP 0-7 H
D8 CLEAR CYCLE L
74151 E18
D12 RING 0 L
D12 RING 1 L
D12 RING 2 L
D12 RING 3 L
D12 RING 4 L
D12 RING 5 L
D12 RING 6 L
D12 RING 7 L
D9 MUX RING L
D9 B LINE CNT MSB H
D9 B LINE CNT + H
D9 B LINE CNT LSB H
J1
1488 E6
1488 E5
1488 E9
D9 SEC TX 0 H
D9 TERM RDY 0 H
D9 RQ TO SEND 0 H
D9 SEC TX 1 H
D9 TERM RDY 1 H
D9 RQ TO SEND 1 H
D9 SEC TX 2 H
D9 TERM RDY 2 H
D9 RQ TO SEND 2 H
D9 SEC TX 3 H
D9 TERM RDY 3 H
D9 RQ TO SEND 3 H
74175 E4 LINE 0
74175 E7 LINE 1
74175 E10 LINE 2
74175 E13 LINE 3
D7 D00 H
D7 D03 H
D7 D01 H
D7 D02 H
D9 LINE EN 0 L
D9 SEC TX 0 L
D9 TERM RDY 0 L
D9 RQ TO SEND 0 L
D9 LINE EN 1 L
D9 SEC TX 1 L
D9 TERM RDY 1 L
D9 RQ TO SEND 1 L
D9 LINE EN 2 L
D9 SEC TX 2 L
D9 TERM RDY 2 L
D9 RQ TO SEND 2 L
D9 LINE EN 3 L
D9 SEC TX 3 L
D9 TERM RDY 3 L
D9 RQ TO SEND 3 L
D9 INI L
R4 750
+5V
D7 CLEAR MUX L
D9 INI L
D1 1N4733A
-15V
C65 6.8µF
R6 330
-10V
(TO PIN 3 OF 3 1488 IC'S)
D2 1N4733A
+15V
C66 6.8µF
R7 330
+10V
(TO PIN 14 OF 3 1488 IC'S)
REVISIONS
CHK
CHANGE NO
REV
TITLE
MODEM CONTROL (D9)
SIZE D
CODE CS
NUMBER M7808-0-1
REV. D
SHEET 4 OF 7
D CS M7808-0-1

D9 EN MUX H

CARRIER SELECTOR (E23)

DI2 CARRIER Ø L
DI2 CARRIER 1 L
DI2 CARRIER 2 L
DI2 CARRIER 3 L
DI2 CARRIER 4 L
DI2 CARRIER 5 L
DI2 CARRIER 6 L
DI2 CARRIER 7 L

74151 E23 — S2 S1 SØ

8881 E3 → 1 BB1 DIØ MUX CARRIER L

CLEAR TO SEND SELECTOR (E28)

DI2 CLEAR TO SEND Ø L
DI2 CLEAR TO SEND 1 L
DI2 CLEAR TO SEND 2 L
DI2 CLEAR TO SEND 3 L
DI2 CLEAR TO SEND 4 L
DI2 CLEAR TO SEND 5 L
DI2 CLEAR TO SEND 6 L
DI2 CLEAR TO SEND 7 L

74151 E28 — S2 S1 SØ

8881 E3 → 4 BC1 DIØ MUX CLEAR TO SEND L

SEC RX SELECTOR (E33)

DI2 SEC RX Ø L
DI2 SEC RX 1 L
DI2 SEC RX 2 L
DI2 SEC RX 3 L
DI2 SEC RX 4 L
DI2 SEC RX 5 L
DI2 SEC RX 6 L
DI2 SEC RX 7 L

74151 E33 — S2 S1 SØ

8881 E3 → 4 BA1 DIØ MUX SEC RX L

D9 LINE CNT LSB H
D9 LINE CNT + H
D9 LINE CNT MSB H

LINE + (E16)

74175 E16 — D9 INI L, D9 CLOCK 4 L

LINE EN 4 L
SEC TX 4 L
TERM RDY 4 L
RQ TO SEND 4 L

LINE 5 (E21)

74175 E21 — D9 INI L, D9 CLOCK 5 L

LINE EN 5 L
SEC TX 5 L
TERM RDY 5 L
RQ TO SEND 5 L

LINE 6 (E26)

74175 E26 — D9 INT L, D9 CLOCK 6 L

LINE EN 6 L
SEC TX 6 L
TERM RDY 6 L
RQ TO SEND 6 L

D2Ø H
D2Ø3 H
D2Ø1 H
D2Ø2 H

J2

1488 E12 → DIØ SEC TX 4 H
1488 E12 → DIØ TERM RDY 4 H
1488 E12 → DIØ RQ TO SEND 4 H

1488 E11 → DIØ SEC TX 5 H
1488 E11 → DIØ TERM RDY 5 H
1488 E11 → DIØ RQ TO SEND 5 H

1488 E15 → DIØ SEC TX 6 H
1488 E15 → DIØ TERM RDY 6 H
1488 E15 → DIØ RQ TO SEND 6 H

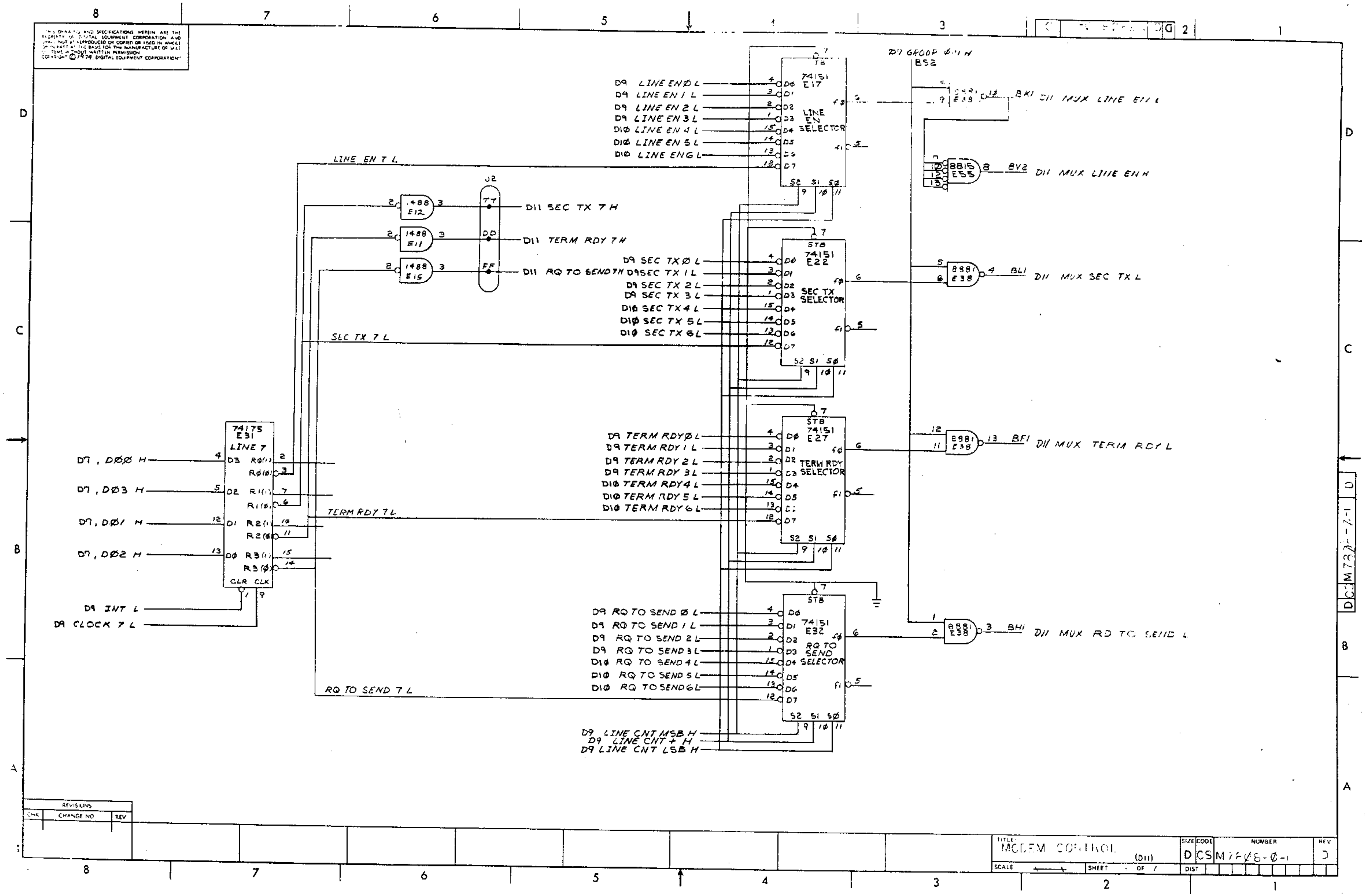
D3 IN4733A — (TO PIN 1 OF 3 1488 IC'S)
-15V ABZ 882 — C67 6.8µF — -10V R8 330

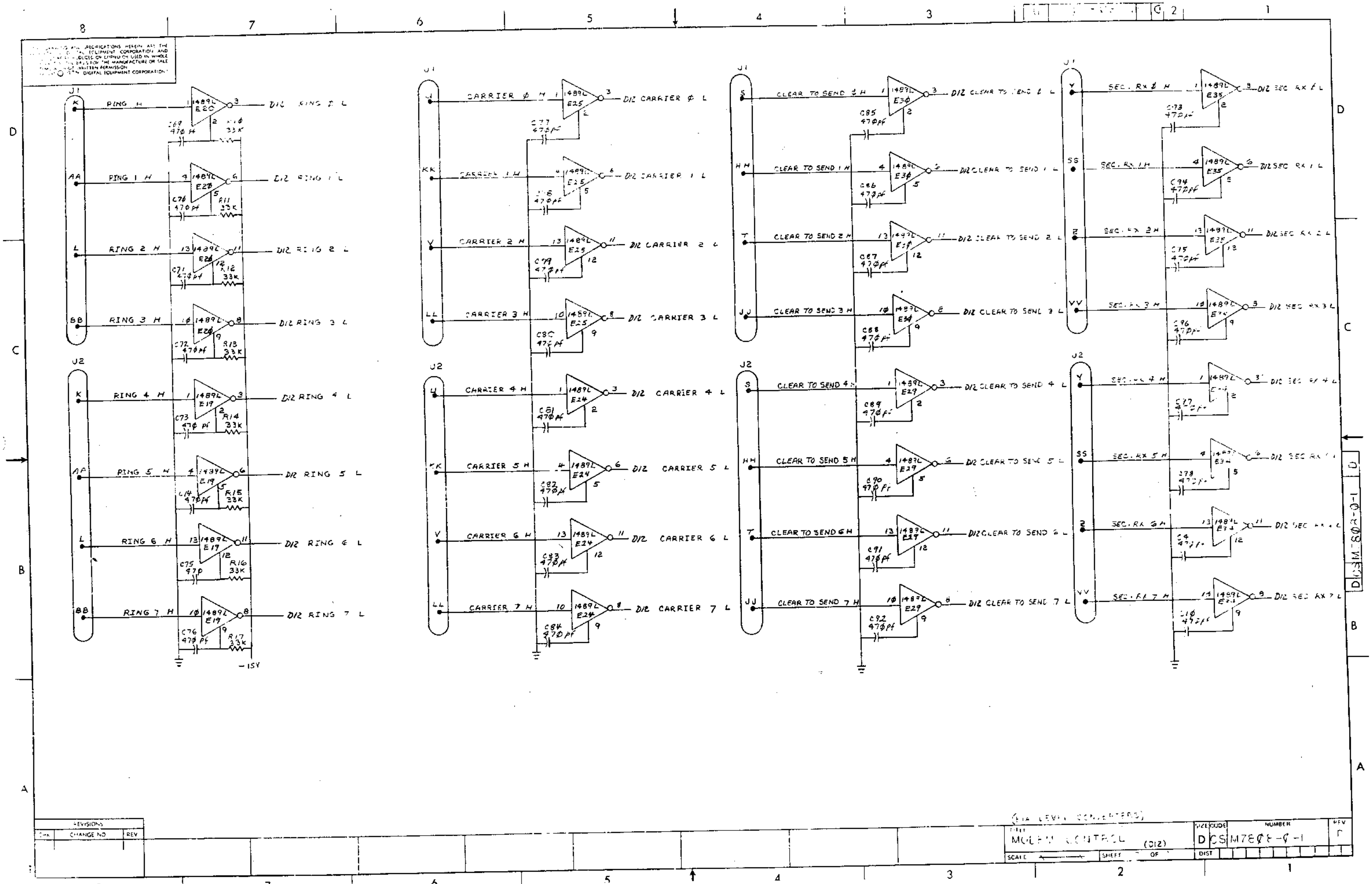
D4 IN4733A — (TO PIN 14 OF 3 1488 IC'S)
+15V AU1 — C68 6.8µF — +10V R9 330

REVISIONS		
CHK	CHANGE NO	REV

TITLE: MODEM CONTRO_ (DIØ) (MUX)
SIZE D | CODE | NUMBER: DCSM7803-Ø-1 | REV D
SCALE | SHEET _ OF | DIST

DCSM7803-Ø-1 D


74151 E17
LINE EN SELECTOR
D9 LINE ENØ L
D9 LINE EN 1 L
D9 LINE EN 2 L
D9 LINE EN 3 L
D1Ø LINE EN 4 L
D1Ø LINE EN 5 L
D1Ø LINE EN 6 L
LINE EN 7 L
D11 MUX LINE EN L
8815 E55
D11 MUX LINE EN H
1488 E12
1488 E11
1488 E15
D11 SEC TX 7 H
D11 TERM RDY 7 H
D11 RQ TO SEND 7 H
74151 E22
SEC TX SELECTOR
D9 SEC TX Ø L
D9 SEC TX 1 L
D9 SEC TX 2 L
D9 SEC TX 3 L
D1Ø SEC TX 4 L
D1Ø SEC TX 5 L
D1Ø SEC TX 6 L
SEC TX 7 L
8881 E38
D11 MUX SEC TX L
74175 E31
LINE 7
D7, DØØ H
D7, DØ3 H
D7, DØ1 H
D7, DØ2 H
D9 INT L
D9 CLOCK 7 L
74151 E27
TERM RDY SELECTOR
D9 TERM RDY Ø L
D9 TERM RDY 1 L
D9 TERM RDY 2 L
D9 TERM RDY 3 L
D1Ø TERM RDY 4 L
D1Ø TERM RDY 5 L
D1Ø TERM RDY 6 L
TERM RDY 7 L
D11 MUX TERM RDY L
74151 E32
RQ TO SEND SELECTOR
D9 RQ TO SEND Ø L
D9 RQ TO SEND 1 L
D9 RQ TO SEND 2 L
D9 RQ TO SEND 3 L
D1Ø RQ TO SEND 4 L
D1Ø RQ TO SEND 5 L
D1Ø RQ TO SEND 6 L
RQ TO SEND 7 L
D11 MUX RQ TO SEND L
D9 LINE CNT MSB H
D9 LINE CNT + H
D9 LINE CNT LSB H
MODEM CONTROL (D11)
D CS M7808-0-1

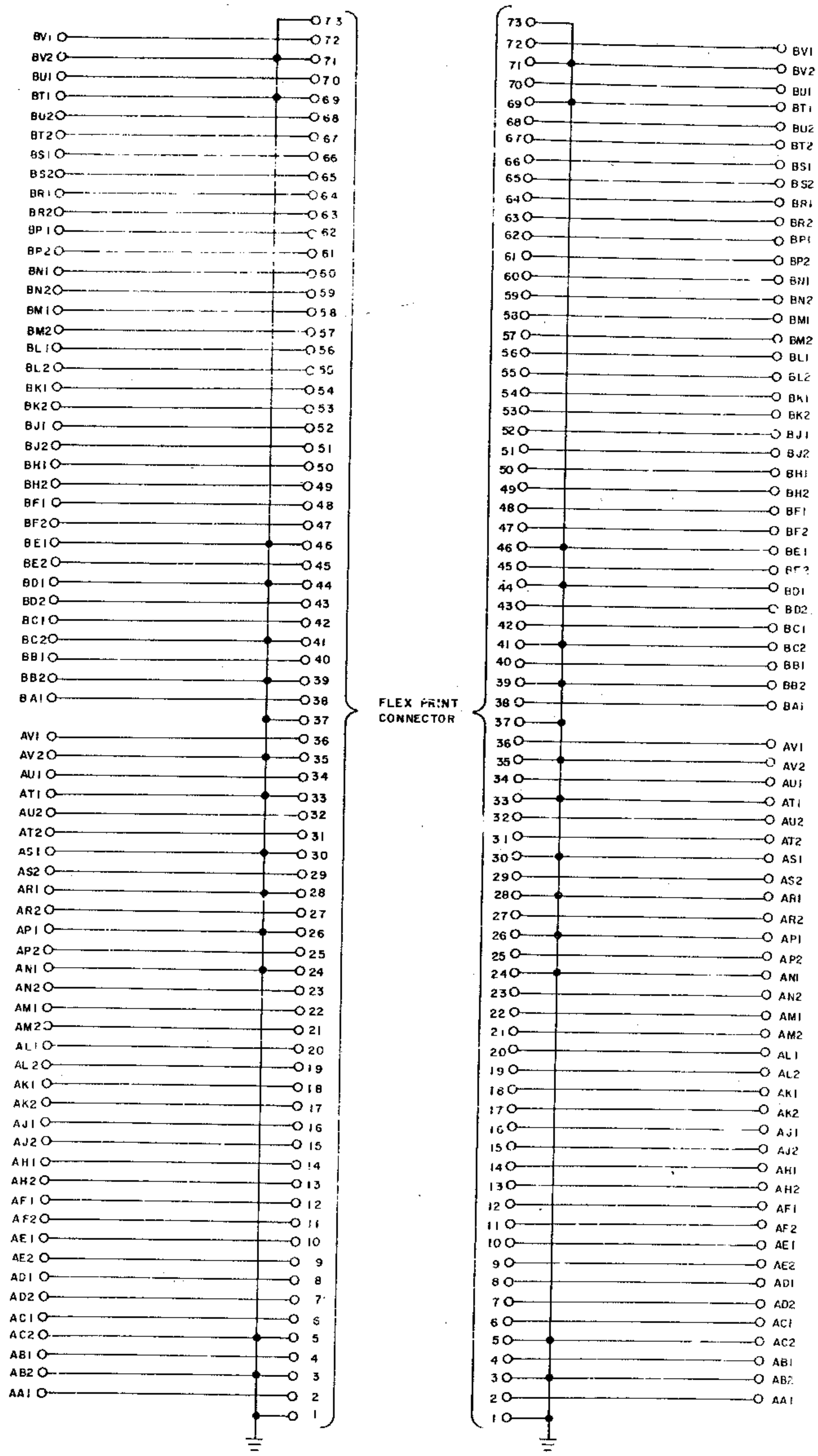


(EIA LEVEL CONVERTERS)

MODEM CONTROL (D12)

SIZE	CODE	NUMBER	REV
D	CS	M7808-Ø-1	F

REVISIONS		
CHK	CHG NO	REV.
	00001	A
	00002	B
	00004	C



TRANSISTOR & DIODE CONVERSION CHART

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

INTERNAL BUS CONNECTOR M920

SIZE	CODE	NUMBER	REV.
C	CS	M920-0-1	C

PRINTED CIRCUIT REV. B

DEC FORM NO. DRG-102