EK-ODH11-OP-002

DH11 asynchronous 16-line multiplexer user's manual

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CONTENTS

ILLUSTRATIONS

INTRODUCTION

This manual provides the user with information concerning the installation, operation, and programming of the DH11 Asynchronous 16-Line Programmable Multiplexer.

Although signals are transferred between the DH11 and the PDP-11 Unibus, this manual does not provide detailed information on the operation of the Unibus. A detailed discussion of the Unibus is contained in the *PDP-11 Peripherals Handbook.*

Three chapters comprise this manual:

Chapter 1 – General Description

Chapter 2 – Installation

Chapter 3 – Programming

CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DH11 Asynchronous 16-Line Programmable Multiplexer connects the PDP-11 with 16 asynchronous serial communications lines operating with individually programmable parameters. These parameters are:

Character Length: 5, 6, 7, or 8 bit

Number of Stop Bits: 1 or 2 for 6, 7, 8 bit characters
1 or 1.5 for 5 bit characters

Parity Generation and Detection: odd, even, or none

Operating Mode: half duplex or full duplex

Transmitter Speed and Receiver Speed: 0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800 or 9600 Baud plus Ext A, Ext B

Breaks: May be detected or generated on each line.

The DH11 multiplexer uses 16 double-buffered MOS/LSI receivers to assemble the incoming characters. An automatic scanner takes each received character and line number, and deposits that information in a first-in, first-out buffer memory referred to as the *silo*. The bottom of the silo is a register which is addressable from the Unibus.

The transmitter in the DH11 also uses double-buffered MOS/LSI units. They are loaded directly from message tables in the PDP-11 memory by means of single-cycle direct memory transfers (NPR). The current addresses and byte counts for each line's message table are stored in semiconductor memories located in the DH11. This reduces the Unibus time taken for the NPR transfers to one NPR cycle per character transmitted. The NPR cycle used is lengthened slightly.

As many as 16 DH11s may be placed on a single PDP-11 processor, creating a total capacity of 256 lines. Figure 1-1 shows some typical DH11 system applications.

1.1.1 DH11-AA and -AC Line Interfaces

Four DM11-DAs are connected to a DH11-AA or AC. Each DM11-DA provides line conditioning for four serial communications devices using 20 mA current loops. Such devices include a Teletype®, LA36 or VT05A or B.

Four DM11-DBs are connected to a DH11-AA or AC. Each DM11-DB provides line conditioning for four EIA/CCITT devices not requiring modem control.

® Teletype is a registered trademark of Teletype Corporation.

Four DM11-DCs are connected to a DM11-BB Modem Control which in turn is connected to a DH11-AA or AC. Each DM11-DC provides line conditioning for four EIA/CCITT devices equipped with data set control.

1.1.2 DH11-AB Line Interfaces

A DC08 Telegraph Line Interface is used with two DH11-ABs to provide line conditioning for 32 telegraph lines.

1.1.3 DH11-AD and -AE Line Interfaces

The DH11-AD and -AE use the H317-B distribution panel which provides 16 EIA/CCITT lines for devices with or without data set control.

1.2 PHYSICAL DESCRIPTION

1.2.1 Configurations

The DH11-AA multiplexer is available in four variations as shown in Figure 1-2:

The DH11-AA consists of a double system unit, all modules necessary to implement a 16-line asynchronous multiplexer, a 5-1/4 inch level conversion and distribution panel with its own power supply, and a data cable between the logic in the double system unit and the level conversion/distribution panel. The modules for level conversion are not included, so that the type and quantity of lines may be customized to the customer's requirements. The power supply for the distribution panel is also 5-1/4 inches high. Generally, it can be mounted on the rear of the rack in a position opposite the distribution panel, which is usually mounted on the front of the rack.

The DH11-AB is the same as the DH11-AA, but does not include the level conversion/distribution panel or its associated power supply. Instead of a data cable to a distribution panel, a data cable to the DC08CS Telegraph Converter Panel is supplied.

The DH11-AC is the same as the DH11-AA, except that the power supply on the level conversion/distribution panel is arranged for 240 V, 50 Hz operation. (There is no need for a 50 Hz version of the DH11-AB because it is a processor-powered option).

All of the above versions of the DH11 include pre-wired slots in the double system unit for the insertion of a DM11-BB Modem Control option.

The DH11-AD consists of a double system unit, all modules necessary to implement a 16-line asynchronous multiplexer, EIA level conversion for the data lines, modem control with EIA conversion, and a 16-line EIA distribution panel.

The DH11-AE is the same as the DH11-AD except the modem control is not included.

CAUTION

The DH11 uses hex modules and thus cannot be mounted in a BA11 CS or ES Expander Box. The 11/35, 11/40, 11/45 type boxes must be used (BA11-B, D, F series).

1.2.2 Multiplexer Distribution Panel and Power Supply

The DH11-AA and AC provide a panel for level converters and cables for the individual lines. The panel uses a standard H911 style rack, but only 6 connector blocks are used.

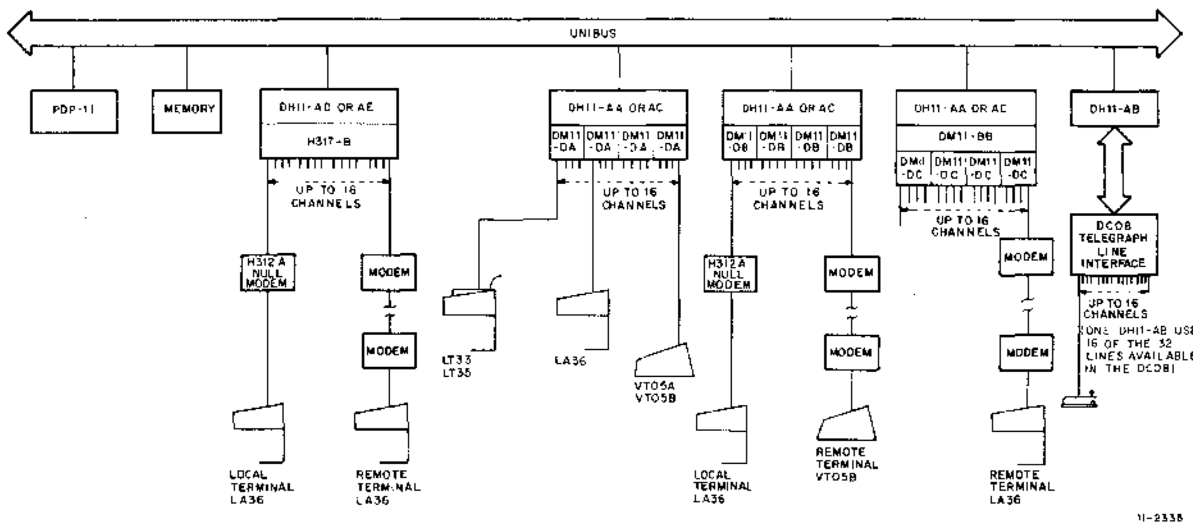


Figure 1-1 DH11 System Applications

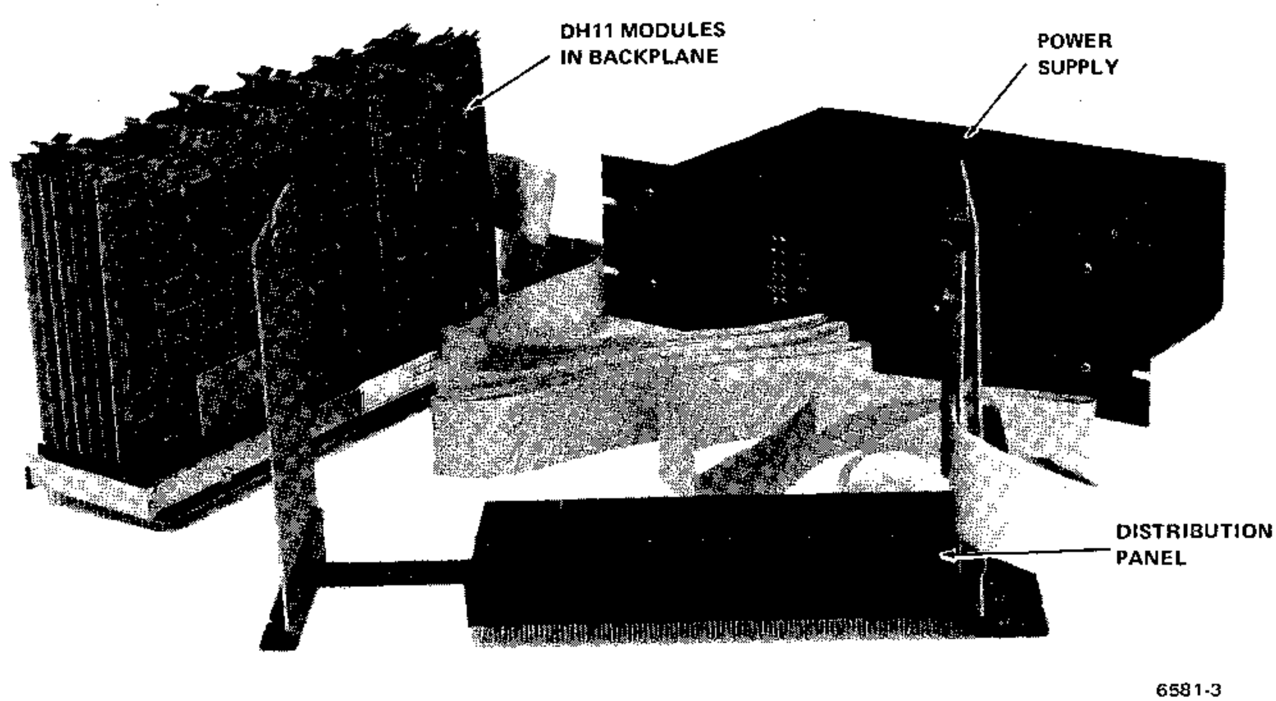
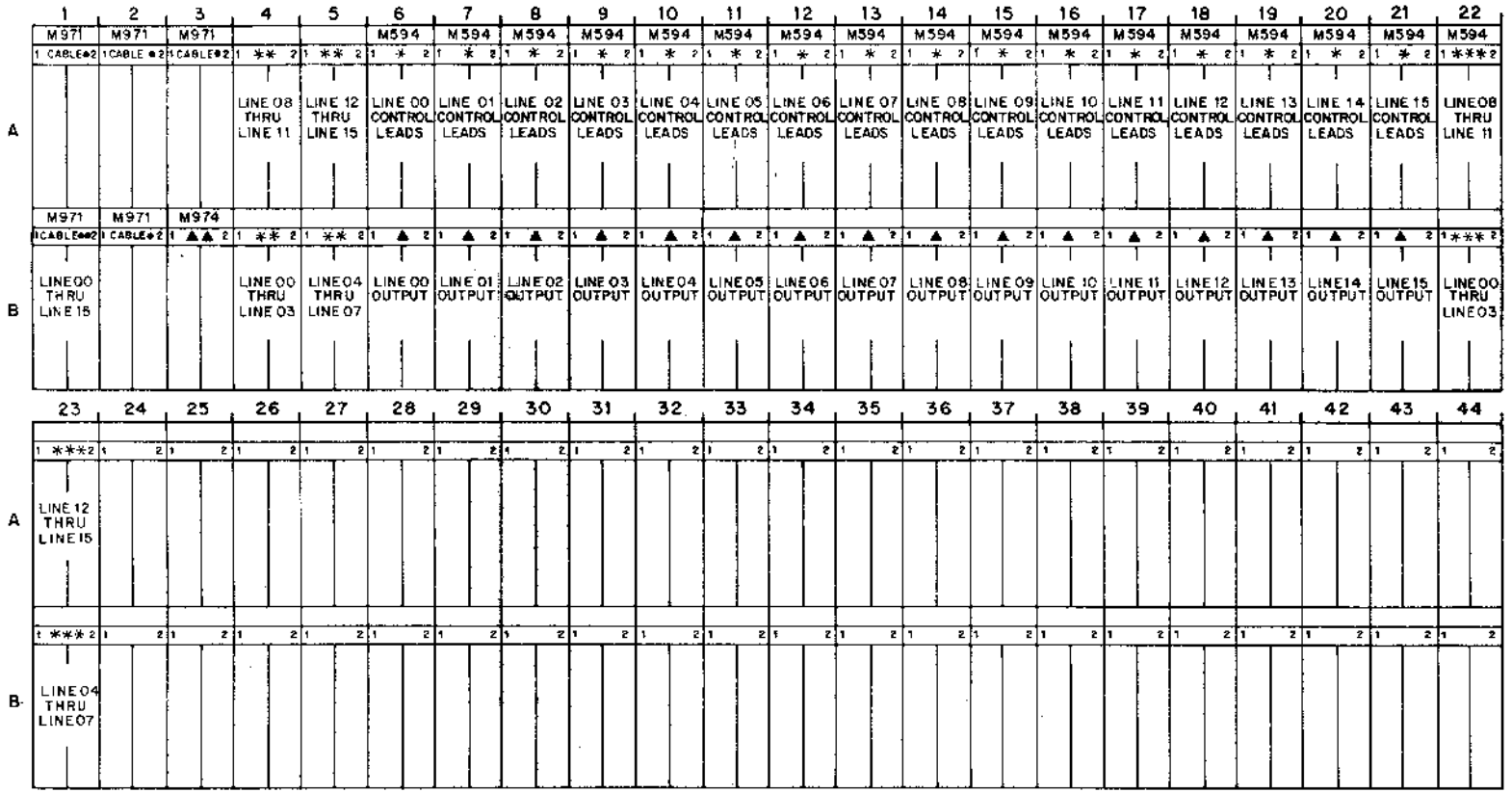


Figure 1-2 DH11 Multiplexer



* LEVEL CONVERSION OF CONTROL LEADS. ONE SLOT PER LINE. USE M594 ONLY WHEN DM11-BB IS IMPLEMENTED. IF DM11-DB IS USED REPLACE M594 WITH W404-A (SUPPLIED WITH DM11-DB). IF DM11-DA IS USED LEAVE BLANK.

** USE M594 FOR DM11-DB

*** USE M596 FOR DM11-DA

• USE ONLY IF DM11-BB IS IMPLEMENTED

•• DATA CABLE FROM DH11-AA CONTROL LOGIC

▲ 16 CABLE SLOTS ONE PER LINE FOR DM11-DA USE M973, FOR DM11-DB USE BC01R-25

▲▲ JUMPER CARD USED FOR DIAGNOSTIC PROGRAMS ONLY, REMOVE FOR NORMAL OPERATION

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Figure 1-3 Distribution Panel Module Utilization Diagram

The slot assignments follow the DF11 format which is the standard level conversion and cable slot for PDP-11 Communications Products (Figure 1-3). Slots A06 through A21 are used for level conversion modules. Slots B06 through B21 are used for cable termination. Other slots provide inputs or special purpose outputs. The distribution panel mounts on a standard 19-inch cabinet and connects to the DH11 logic by means of a BC08-S Data Cable.

Power for the distribution panel is provided by the H758 Power Supply mounted on the rear of the cabinet. Some units in the field use H739 or H751 supplies which are generally equivalent to an H758 supply. The H758 provides the voltages listed below:

+15 V @ 2 A
-15 V @ 2 A
+5 V @ 4 A

Power drain of the distribution panel depends on the type of level conversion used. The maximum drain on the +15 V and -15 V occurs when DF11-BB modems are used, at which time the full rated output of a 2 A is used. The maximum +5 V drain occurs when all lines are arranged for full modem control (four DM11-DC options); the current used is then 1.7 A.

The level conversion types can be mixed on a 4-line basis by using different converters on slots A4, A5, B4, and B5. Also, level converters can be mixed on a single line basis by using slots A6 through A21 for level conversion on a single line basis. Consult Figure 1-3 for specific details.

The DH11-AD and AE options use a 16-line EIA distribution panel. This panel requires no power of its own. It mounts in a standard 19 inch cabinet and connects to the DH11-AD and AE logic by means of two BC08S data cables and four BC08R modem control cables.

BC05D-25 cables may be ordered separately to connect from the EIA distribution panel to the modem.

1.2.3 General Specifications

Environmental:
Temperature: +50° F to +110° F
Humidity: 0 to 95 percent non condensing

Power Consumption:
The power consumption of the DH11-AA, AB, and AC logic (excluding the level conversion modules, which run off the level conversion/distribution panel power supply) is:

+5 V:	8.4 A (DH11 alone)**
	11.2 A (DH11 plus DM11-BB Modem Control)**
-15 V:	240 mA

The power consumption of the DH11-AD and AE is:

DH11-AD

+5 V:	10.8 A**
+15 V:	400 mA
-15 V:	645 mA

**Add 0.2 A if this is the last option on the Unibus.
(The Unibus terminator consumes 0.2 A)

DH11-AE

+5 V:	8.6 A**
+15 V:	100 mA
-15 V:	340 mA

**Add 0.2 A if this is the last option on the Unibus.
(The Unibus terminator consumes 0.2 A)

Receivers:

The DH11 receiver units provide serial to parallel conversion of 5, 6, 7, or 8 bit code with one start bit and at least one stop bit. An extra data bit is added when parity operation is selected. The allowable input distortion is 43.75 percent assuming no speed distortion. The maximum allowable speed distortion is 4.8 percent for 8-bit characters.

The DH11 transmitter units provide parallel to serial conversion of 5, 6, 7, or 8 bit code with one start bit and one, one and a half (5 bit only), or two (6, 7, or 8 bit only) stop units. An extra data bit is added if parity operation is selected.

The number of bits per character, the number of stop marks, and parity mode are selectable on a per-line basis, but must be the same as the corresponding receiver. The serial data rate is determined by a crystal clock and is program controllable on a per-line basis. The transmitter speeds may be program controlled independently of the receiver speeds. Output distortion is less than 2 percent.

Interface:

Interface to and from the control section. There are 16 output data lines and 16 input data lines at TTL levels using negative logic (mark = 0).

The input leads from the level conversion/distribution panel are equipped with pull up resistors which place lines not equipped with level conversion in a permanently spacing condition. Logic in the DH11 receivers prevents this condition from assembling null characters on a continuous basis, however.

Bus Loading:

The DH11 presents two bus loads to the Unibus. If a Modem Control is added, an additional bus load is added.

1.3 FUNCTIONAL DESCRIPTION

1.3.1 Receiver Operation

Reception on each line is by means of Universal Asynchronous Receiver/Transmitters (UARTs). These are 40-pin MOS/LSI devices that perform all the necessary functions for double-buffered asynchronous character assembly.

The receiver section of the UART samples the line at 16 times the bit rate of the signals to be received on that line. Upon detection of a mark-to-space transition, the UART counts 8 clock pulses and checks the state of the line again. This sampling occurs in the center of a normal start bit. If that sample is a mark, the receiver returns to its idling state, ready to detect another mark-to-space transition. If the sample is a space, the receiver enters the data entry condition and samples the state of the line at subsequent sample points spaced at multiples of 16 clock ticks from the center of the start bit. The number of samples taken is determined by the character length information entered into the UART via the Line Parameter Register. If parity checking has been enabled for this line, the receiver computes the parity of the character just received and compares it with the parity sense specified for reception on that line. If the parity sense differs, the parity error bit is set.

The character length, parity sense, number of stop bits, etc., that are used by the UART to perform the above operations, are stored within each UART in a Control Bits Holding Register. The Control Bits Holding Registers of each UART are addressable, on a write-only basis, from the Unibus, by first setting the line selection bits of the System Control Register and then loading the desired line parameters into the Line Parameter Register, from which they are automatically transferred to the Control Bits Holding Register of the designated UART. It is important that no interrupt handling routine intervene and change the contents of the System Control Register during the above operation.

1.3.2 Silo Operation

The silo is an MOS/LSI digital storage buffer that is 16 bits wide and 64 words deep. A 16-bit word is entered at the top and automatically bubbles down to the lowest location that does not already contain an entry. The bottom of the silo is the Next Received Character Register (NRC).

There are three registers associated with the silo. One is the Next Received Character Register. It is a read-once register because it is the bottom of the silo, and reading it extracts that character from the silo and causes all other entries to bubble down one more position.

The other two registers are byte-size registers and are contained within the Silo Status Register. One is the high byte, which is read-only and contains the status of an up-down counter, giving the actual fill level of the silo. The second register, the low byte, is read/write and is used by the program to specify that silo fill level beyond which the program wishes to receive interrupt notification.

1.3.3 Transmitter Operation

In the transmit mode, the program picks the desired line and selects the transmitter operating parameters. The program then loads the Current Address Register (CAR) with the memory address of the first character to be transmitted on the selected line. It also loads the Byte Count Register (BC) with the number of characters in the message and sets the bit of the Buffer Active Register (BAR) associated with the selected line. When the transmitter scanner finds a Transmitter Buffer Empty (TBMT) flag high for the selected line, it stops and a character is transferred from memory to the UART for transmission.

Transmission on each line is by means of UARTs that perform all the necessary functions for double-buffered asynchronous character transmission. The transmitter section of the UART holds the serial output line at a marking state when idle. When the transmitter loading leads have been conditioned with the character to be transmitted and the data strobe lead has been brought high (these functions are performed by the NPR control), the UART commences generation of a start space within one sixteenth of a bit time. The start space and all subsequent data bits are a full bit time each. The start space is followed by M data bits, where M is 5, 6, 7, or 8, as determined by the

Control Bits Holding Register. The data bits are presented to the line least significant bit first. The parity bit, if parity generation is enabled, is calculated by the transmitter and affixed after the last data bit, but before the stop marks.

The stop bit or bits depend in quantity upon the setting of the control word. If the transmission of 6, 7, or 8 bits has been selected, the program may select either one or two stop bits. If the transmission of 5 bit code has been selected, the program may select either one or one and a half stop bits.

If the transmitter's holding register has been loaded while a character was being transmitted, the second character has its start bit commence immediately at the end of the preceding character's stop bit(s).

1.3.4 Auto-Echo Operation

The DH11 contains provision for the hardware to echo received characters without software intervention. The feature may be enabled on any line by conditioning the line selection bits in the System Control Register and then setting the appropriate bits in the Line Parameter Register, including bit 15 (Auto Echo Enable).

The auto-echo hardware is part of the receiver scanner and operates as follows:

a. If the receiver scanner finds a received character for a line upon which auto-echo is not enabled, it simply dumps that character into the silo and resumes scanning.

b. If the receiver scanner finds a received character for a line upon which auto-echo is enabled, it examines the error flags associated with that character.

    1. If a framing error is detected, the remote terminal is trying to gain the attention of the processor by sending a break. In this case, the auto-echo hardware dumps the received character and associated flag into the silo so that the system software is alerted. The break is not echoed to the remote terminal.

    2. If an overrun error is detected, the remote terminal is trying to gain the attention of the processor by typing characters. This case is treated identically to b.1., above.

c. If the receiver scanner finds a received character from a line upon which auto-echo is enabled and there are no error flags of the type mentioned above, the receiver scanner and auto-echo logic attempts to echo the character. First, however, certain tests of internal logic conditions must be made.

    1. The UART transmitters are all loaded from a common internal data bus. Therefore, the auto-echo hardware must first check to see that no NPR cycles are in progress, loading a UART transmitter from that bus. If a conflict is indicated, the receiver scanner is restarted and the process is tried again on the scanner's next rotation.

    2. If the above test indicates no problem, the one remaining check is to see if the Transmitter Holding Register for the line upon which the character was received is available. If it is not, the scanner is restarted. If it is available, auto-echo commences.

    It is not advisable to transmit messages on a line and auto-echo characters received on that line simultaneously. It is not possible to receive characters on a line at 30 characters per second, echo them back by auto-echo at 30 characters per second, and transmit an independent message at 30 characters per second, all on the same line. The auto-echo hardware will interlock these functions to some degree, but if more than two characters are received on a line while the scanner is waiting for the transmitter holding buffer to become available, a data overrun occurs and characters are lost. Auto-echo and software-driven transmission should not be attempted on the same line simultaneously, if input from that line is expected.

1.3.5 Interrupts

1.3.5.1 Receiver Interrupts – There are two kinds of receiver interrupts; they are enabled by bits 6 and 12 of the System Control Register.

Receiver Interrupt (System Control Register bit 7) – This interrupt, when enabled, occurs whenever the number of entries in the silo exceeds the silo status alarm level that the program has stored in the low byte of the Silo Status Register and SCR bit 6 is set. (The program can examine actual silo fill at any time by examining the high byte of the Silo Status Register.)

Storage Overflow Interrupt (System Control Register bit 14) – This interrupt, when enabled, occurs when the character storage silo is full and the DH11 hardware needs to store an additional character and SCR bit 12 is set. Should this situation occur, it does not necessarily mean that data has been lost.

1.3.5.2 Transmitter Interrupts – There are two kinds of transmitter interrupt; both are enabled by bit 13 of the System Control Register.

Transmitter Interrupt (System Control Register bit 15) – This interrupt, if enabled, occurs whenever one or more lines have finished the transmission of a complete string of characters. Specifically, it occurs after the NPR cycle that loaded the last character to be transmitted (and hence incremented the byte count to 0).

Non-Existent Memory Interrupts (System Control Register bit 10) – This interrupt, when enabled, occurs whenever the DH11 addresses non-existent memory. Specifically, this interrupt occurs if the DH11 enters an NPR cycle, places an address on the Unibus, and fails to receive a slave sync response for the location addressed within 20 μs.

CHAPTER 2
INSTALLATION

This chapter provides information for installing and testing a DH11. The information is given in procedural steps.

1. After unpacking, check that all parts are present for the particular configuration listed below.

List A

1	7009180 Wired Backplane Assembly
1	7009561 Power Harness
1	G727 Grant Continuity Card
2	BR 5 Jumpers (5408778)
2	M7821 Interrupt Control Modules
1	M796 Unibus Master Control Module
1	M4540 Crystal Clock Module
1	M7277 Current Address and Address Selection Module
1	M7278 Registers and Byte Control Module
1	M7279 FIFO Buffer Module
2	M7280 Multiple UART Cards
1	M7288 Line Parameter Control Module
1	M7289 System Control and Receiver Scanner Module

List B

2	M971 Cable Card (type BC08R)
1	BC08S Cable
1	7008456 Distribution Panel (7008443 Logic with End Panels)
1	7008493 Power Harness
1	H758A or H739A Power Supply

List C

2	BC08S Cables
2	H8611 Test Connectors
1	H315 Test Connector
1	M5906 Priority and EIA Conversion Module
1	H317B EIA Distribution Panel (5410260 EIA Distribution Panel, 7410667-2 Cover, two 7410668 Cable Clamps, and a 7410666 Mounting Plate)

DH11-AA: The items in lists A and B, one G7360 Priority Selector Card, and one M974 Maintenance Board.

DH11-AB: The items in list A, one G7360 Priority Selector Card, one M974 Maintenance Board, and a 7008423 (M972 to dual W077) Cable.

DH11-AC: The items listed for the DH11-AA, but with an H758B or H739B (220 V) Power Supply substituted for the H758A or H739A Power Supply shown in list B. The DH11-AC is the 220 V version of the DH11-AA.

DH11-AD: The items in lists A and C, one M7807 Mux and Bus Control Module, one M7808 Mux and Scan Control Module, and a H861 Test Connector (Modem Control).

DH11-AE: The items in lists A and C.

2. In addition to the material mentioned above, the following items should be included.

   For each DM11DA ordered:

   1 M596 TTL to 20 mA Level Converter
   4 M973 Mate-N-Lok Cards

   For each DM11DB ordered:

   1 M594 TTL to EIA Level Converter
   4 BC01R Cable Assembly
   4 W404 DTR Jumper Card

   For each DM11DC ordered:

   4 M594 TTL to EIA Level Converter
   4 BC01R Cable Assembly

3. Refer to the unit assembly drawing (D-UA-DH11-0-0) in the DH11 Print Set. Install the DH11 9-slot double system unit containing the wired logic in a convenient spot in the expander box or processor box. With all power off, install the 7009561 Power Harness, being very careful to install the Faston connectors on their respective tabs without catching against or cutting any of the nearby backplane wiring. In early units, the long axis of the tabs is in line with the long axis of the double system unit. In this case, the power tabs must be bent so that they clear both the pins of the wired logic and the power supply regulators. The proper connections are listed on the backplane etch and their relative positions are shown in Figure 2-1. The DH11 interconnection diagrams are shown in Figures 2-2 and 2-3. When using the backplane with tabs whose long axis is perpendicular to the long axis of the system unit, the 7009561 Power Harness is used without alteration.

   Secure the ground wire from F02T1 to one of the mounting screws. Do not plug in the white connector of the 7009561 until step 9.

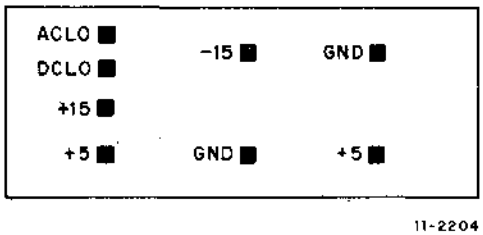


Figure 2-1 Backplane to 7009561 Cable Interconnection

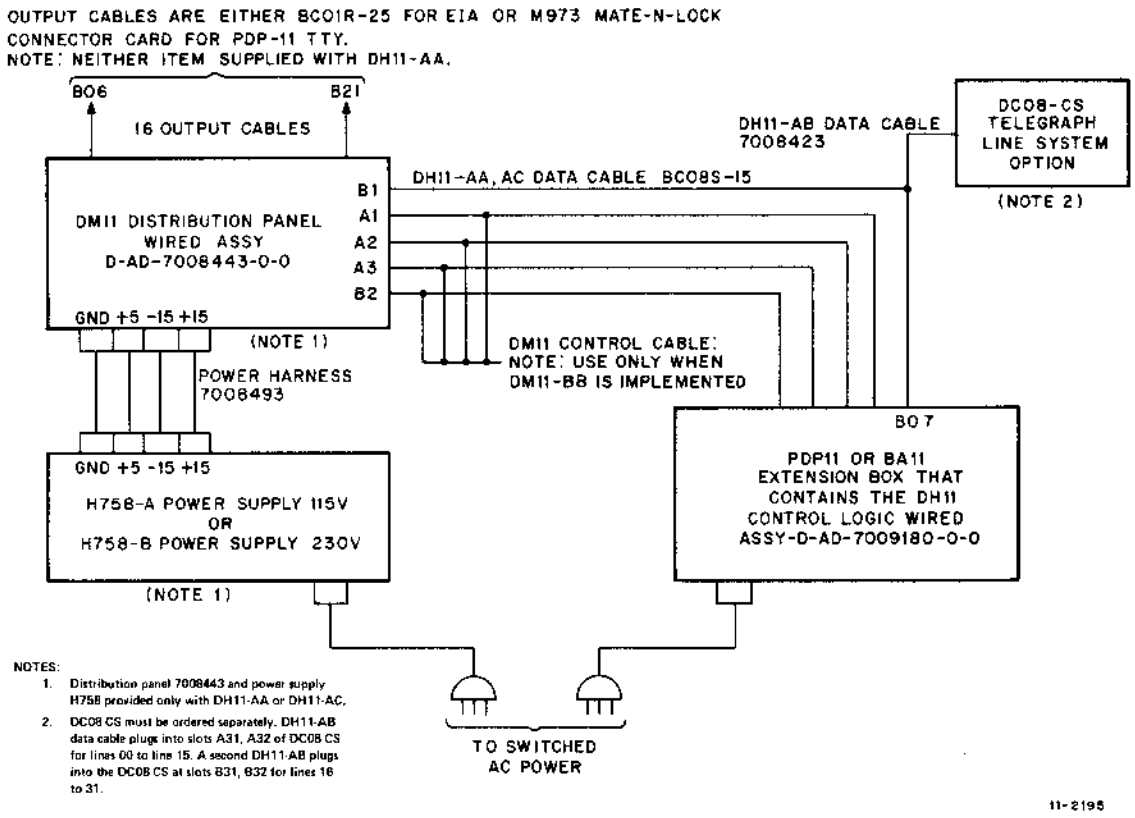


Figure 2-2 DH11-AA, AB, and AC Interconnection Diagram

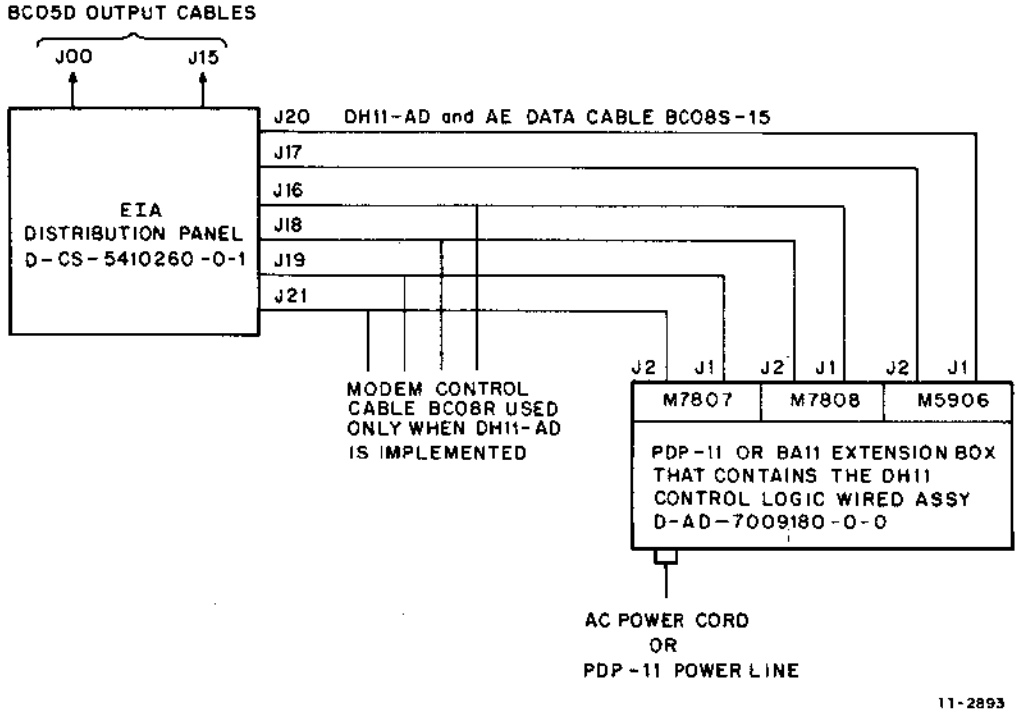


Figure 2-3 DH11-AD and AE Interconnection Diagram

4. Install the modules in their proper locations according to the module utilization list (D-MU-DH11-3-0). Figure 2-4 is the module utilization diagram. It is helpful to place the Unibus connectors, Unibus terminator (if used as last unit), and any modules with cables attached first. Beware of the tendency of hex modules to bow in the middle and for hex module extractor handles to catch on adjacent conventional handles.

5. Be sure that the G7360 or M5906 card has both priority plugs in place. BR5 is standard for the DH11.

6. The DH11 uses floating addresses and is located after the DJ11s in the floating address space that begins at location 160010. Because the DH11 has eight registers, it must be assigned an address that is a multiple of 20 (octal). All DH11s in a system should have consecutive addresses.

   Example 1: A system with no DJ11s, but two DH11s:

   160010 Cannot use for DH11s because not multiple of 20
   160020 First DH11
   160040 Second DH11
   160060 DH11 Gap (indicates that there are no more DH11s).

   Example 2: A system with one DJ11, two DH11s:

   160010 First DJ11
   160020 DJ11 Gap (indicates that there are no more DJ11s).
   160030 Cannot use for DH11s because not a multiple of 20.
   160040 First DH11
   160060 Second DH11
   160100 DH11 Gap (indicates that there are no more DH11s).

   The DH11 vectors (2) follow those of the DJ11 in the floating vector space that starts at address 300. The vectors starting at 300 are used in the following order: DC11; KL11/DL11-A,B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Readers; PA611 Punches; DT11; DX11; DL11-C,D,E; DJ11; DH11.

   Of the two vectors, the receiver vector is the lower numbered vector. The priority of the receiver and transmitter interrupts are individually selectable by means of two standard PDP-11 priority jumper plugs. If both are the same, the receiver has interrupt priority because it is electrically closer to the processor.

   If one or more DM11-BB options are ordered with the DH11s in a system, the DM11-BBs and associated DM11-DCs should be installed in the DH11s that have the lowest addresses (i.e., DH11-AA and ACs).

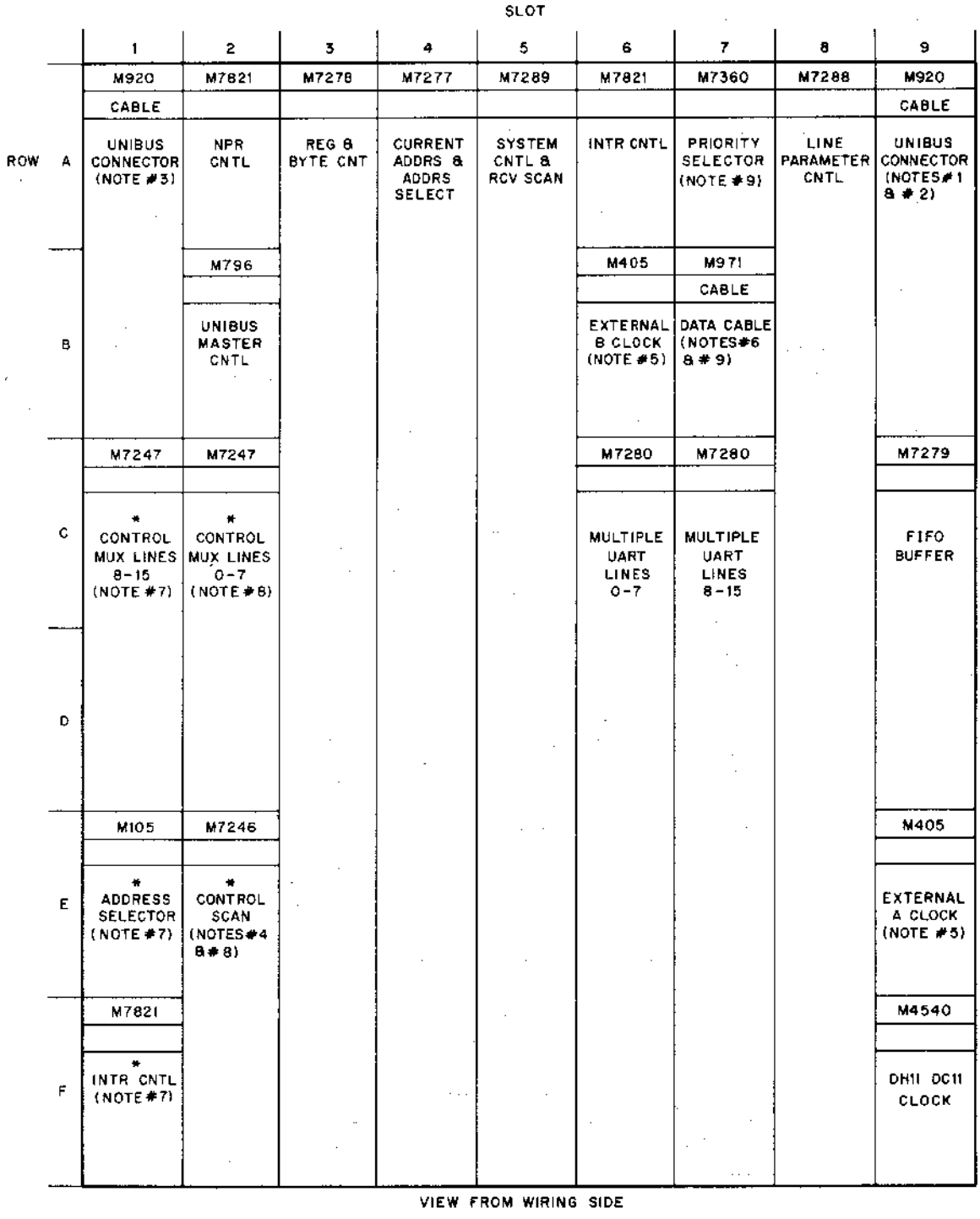
   The DH11s should be in order of increasing address as follows:

   1. DH11s with DM11-BB and full complement of DM11-DCs

   2. DH11-ADs

   3. DH11s with DM11-BB and a partial complement of DM11-DCs

   4. DH11s without modem control, but EIA conversion for data lines only (DM11-BBs or DH11-AEs)



NOTES:

1. If end of bus, replace M920 with M930.
2. If last unit in basic box, replace M920 with BC11A cable when expanding to peripheral box.
3. If first unit in expander box, replace M920 with BC11A cable.
4. E02 must be G727 grant continuity if modem control module set is not installed. * denotes DM11-BB modem control option, with DH11-AA or AC.
5. Module slots provide for additional clock rates.
6. For diagnostic checkout of DH11-AA, AB, or AC, replaces M971 with M974.
7. This slot contains Modem Control Module M7807 with DH11-AD.
8. This slot contains Modem Control Module M7808 with DH11-AD.
9. This slot contains EIA Converter and Priority Module M5906 for DH11-AD or AE.

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Figure 2-4 DH11 Module Utilization Diagram

5. DH11s with EIA and 20 mA mixed

6. DH11s with 20 mA only

The above order is preferred for RSTS systems. If the customer has other desires, he is the final authority.

7. The DH11 requires two M7821 modules. One of these modules (A06) is used to generate interrupts and must have its vector bit jumpers cut to provide the selected vector address.

Both sections of the M7821 are set to the same priority level (BR5) and each one generates an interrupt. Section A is used for receiver interrupts which assert the vector addresses of the form XX0, Section B is used for transmitter interrupts which assert vector addresses of the form XX4. To accomplish this, the bit 2 jumper must be left in. (If a DM11-BB is installed, its M7821 module (slot F01) must have the bit 2 jumper cut.) The other jumpers (bits 3–8) are cut as shown below to select the desired vector address. The jumper for vector bit 2 (W2) on the M7807 module must be out.

Jumper						Vector Address
8	7	6	5	4	3	
X			X	X	X	300
X			X	X		310
X			X		X	320
X			X			330
X				X	X	340
X				X		350
X					X	360
X						370
	X	X	X	X	X	400
	X	X	X	X		410
	X	X	X		X	420
	X	X	X			430
	X	X		X	X	440
	X	X		X		450
	X	X			X	460
	X	X				470
	X		X	X	X	500
	X		X	X		510
	X		X		X	520
	X		X			530
	X			X	X	540
	X			X		550
	X				X	560
	X					570

NOTES: 1. X means remove jumper (cut)
2. Cut only the jumpers shown. Leave the NPR jumper installed.

8. The M7277 module, located in slot 04, contains the address selection logic. The following jumper cut table indicates which jumpers should be cut to get the addresses indicated.

Jumper					Device Address
8	7	6	5	4	
		None			160000
				X	160020
			X		160040
			X	X	160060
		X			160100
		X		X	160120
		X	X		160140
		X	X	X	160160
	X				160200
	X			X	160220
	X		X		160240
	X		X	X	160260
	X	X			160300
	X	X		X	160320
	X	X	X		160340
	X	X	X	X	160360
X					160400
X				X	160420
X			X		160440
X			X	X	160460
X		X			160500
X		X		X	160520
X		X	X		160540
X		X	X	X	160560
X	X				160600
X	X			X	160620
X	X		X		160640
X	X		X	X	160660
X	X	X			160700
X	X	X		X	160720
X	X	X	X		160740
X	X	X	X	X	160760
					. . .

NOTE: X means remove jumper (cut).

The numbers identifying the jumpers are located on the M7277 etch right underneath the jumpers. In the set of five jumpers located near the center of the board, the order from top to bottom is: 8-11-12-10-9. In the set of four jumpers located near the edge of the board, the order from top to bottom is: 7-4-5-6.

9. Measure the resistance between the following pins on the backplane with the white plugs of the 7009561 cable hanging free (not plugged in):

   +5 V to GND must be 0.4 ohm to 10 ohms
   -15 V to GND must be 50 ohms to 500 ohms
   +15 V to GND must be 50 ohms to 500 ohms

   If the resistance is less than the lower limit indicated, check for a short. If the resistance exceeds the high limit, it may indicate an open circuit. Measure the resistance using the X1 scale. For the first measurement, place the red (+) probe on the +5 V terminal and the (-) lead on the GND terminal. In the second measurement, place the red (+) probe on the -15 V terminal and the black (-) lead on the GND terminal. For the third measurement, place the red (+) probe on the +15 V terminal and the black (-) lead on the GND terminal. If the above resistances are OK, connect the white plugs in accordance with D-UA-DH11-0-0.

10. Install the 7008456 Distribution Panel as indicated in D-UA-DH11-0-0 for the DH11-AA or AC. Be sure to install the module restraining bar across the back to hold the modules in case of cable strain. If installing a DH11-AD or AE panel, go to step 14.

11. Install the H758 or H739 Power Supply as shown in D-UA-DH11-0-0. Make sure the toggle switch is in the OFF position. Check the fuse with an ohmmeter. Plug the power plug into the receptacle strip on the cabinet or other processor switched outlet. Position the 7008493 Power Harness by running it up to the top of the cabinet, forward, then down to the distribution panel terminals. It is necessary to gain side access to do this. Mount the H758 on the rack. Do not mount the H758 on the door; you will be unable to close the door. The H739 can be mounted on the door. Be careful that the Faston tabs on the end of the distribution panel do not touch the frame.

12. Install an M971 cable module at each end of the BC08S cable and install the M971s thus equipped in the locations indicated in the D-MU-DH11-0-3 module utilization for the basic logic and in the D-MU-DM11-A-3 module utilization for the distribution panel. These are locations B07 in the DH11 and B01 in the distribution panel.

13. Install the M974 Maintenance Card in location B03 of the distribution panel. Be sure to remove it before starting the on-line tests. If installing the DH11-AA, AB, or AC, go to step 19.

14. For DH11-AD and AEs, install the H317-B EIA distribution panel assembly as indicated in D-UA-DH11-0-0.

15. For DH11-AD or AE installation, refer to Figure 2-3 for cable interconnections and to Figure 2-5 for proper insertion of the BC08S cables. These cables connect the data lines to the distribution panel and should not be installed until after all the off-line tests have run. The M5906 module should have H8611 test connectors in plugs J1 and J2.

CAUTION

Cables are neither marked nor keyed and if improperly connected can damage equipment. On the H317, the rib side of the cable must be away from the board. On the M5906 the smooth side of the cable must be away from the board.

16. The H317-B EIA Distribution Panel provides for several jumper selections (Figures 2-6 and 2-7). The DTR and REQUEST TO SEND leads (Figure 2-6) are normally strapped to a positive ON voltage for the DH11-AE. This strapping must be removed for lines that use a full modem control arrangement in which the modem control signals are combined with the data signals on the distribution panel. This is the case when modem control is used with the DH11-AD.

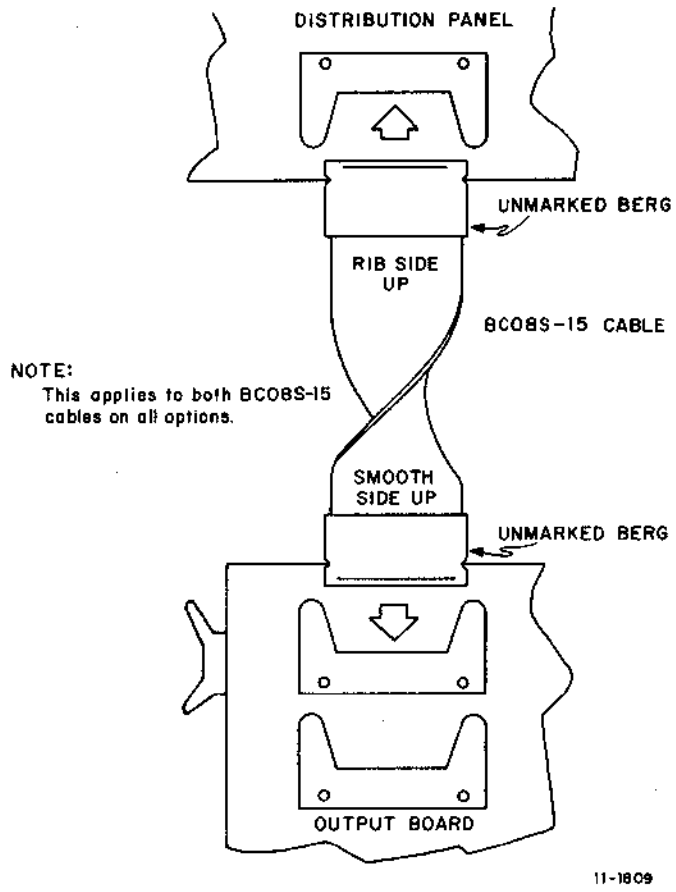


Figure 2-5 BC08S-15 Cable Polarization Diagram

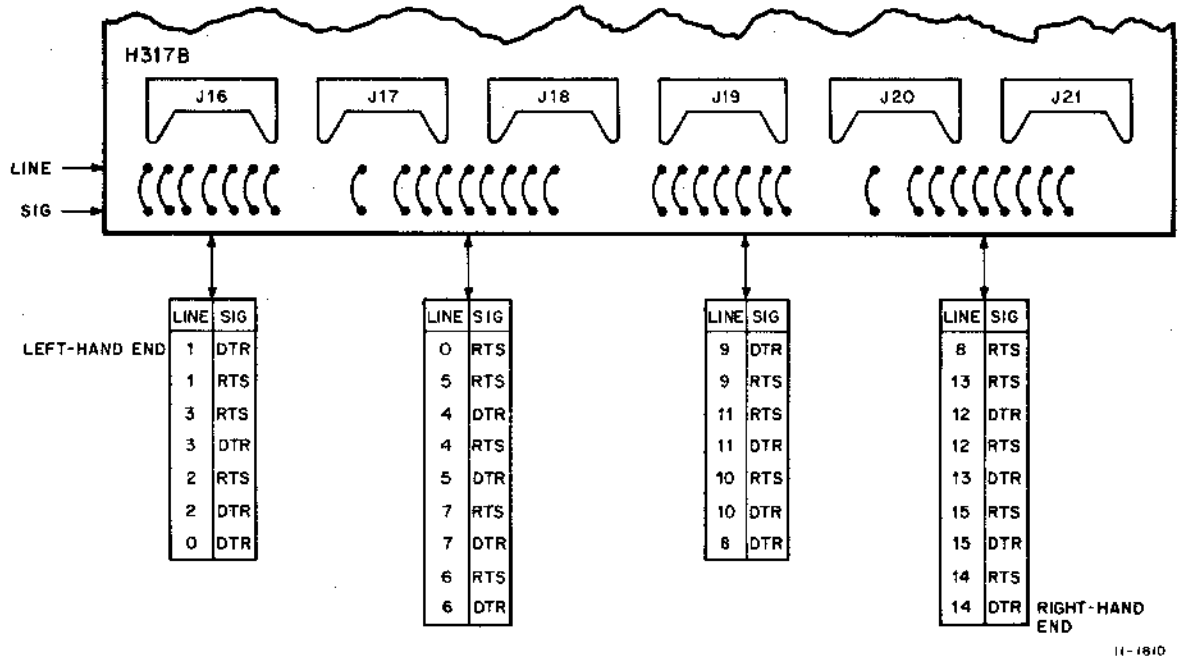
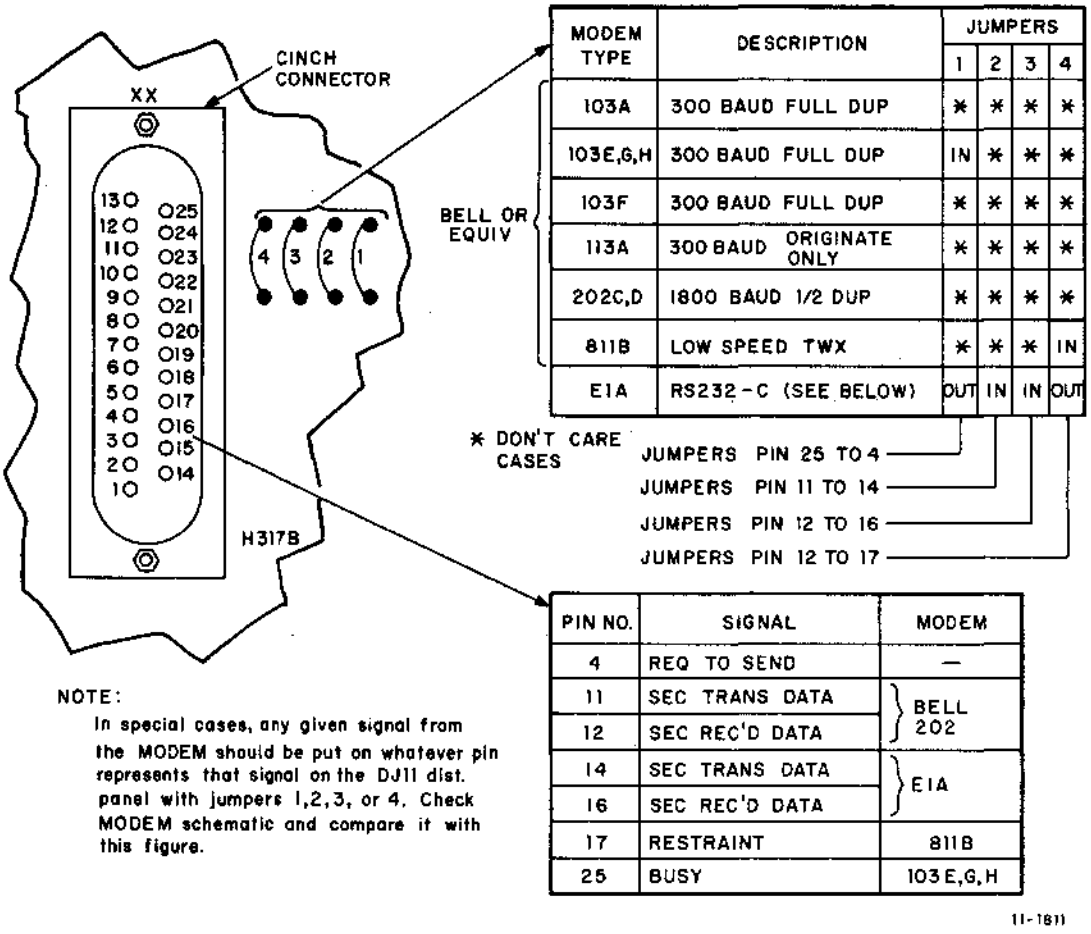


Figure 2-6 Strapping on H317B Distribution Panel



MODEM TYPE	DESCRIPTION	JUMPERS 1	2	3	4
103A	300 BAUD FULL DUP	*	*	*	*
103E,G,H	300 BAUD FULL DUP	IN	*	*	*
103F	300 BAUD FULL DUP	*	*	*	*
113A	300 BAUD ORIGINATE ONLY	*	*	*	*
202C,D	1800 BAUD 1/2 DUP	*	*	*	*
811B	LOW SPEED TWX	*	*	*	IN
EIA	RS232-C (SEE BELOW)	OUT	IN	IN	OUT

PIN NO.	SIGNAL	MODEM
4	REQ TO SEND	—
11	SEC TRANS DATA	BELL 202
12	SEC REC'D DATA	
14	SEC TRANS DATA	EIA
16	SEC REC'D DATA	
17	RESTRAINT	811B
25	BUSY	103E,G,H

Figure 2-7 Cinch-Connector Strapping on H317B Distribution Panel

17. The customer may implement the following options when installing the modem control into the DH11-AD.

    a. A null modem (H312A) may be connected to a line.

    b. Bus initialization of the modem control modules (M7807 and M7808) can be inhibited by removing DH11 backpanel wire F02B2 to ground.

    c. Interrupts for all lines may be inhibited for CARRIER, RING, SEC RX, or CLEAR TO SEND by removing the wires listed below:

Status	DH11 Wire Removed
CARRIER	E02A1 to D02B1
RING	E02C1 to D02F2
SEC RX	E02B1 to D02A1
CLEAR TO SEND	E02D1 to D02C1

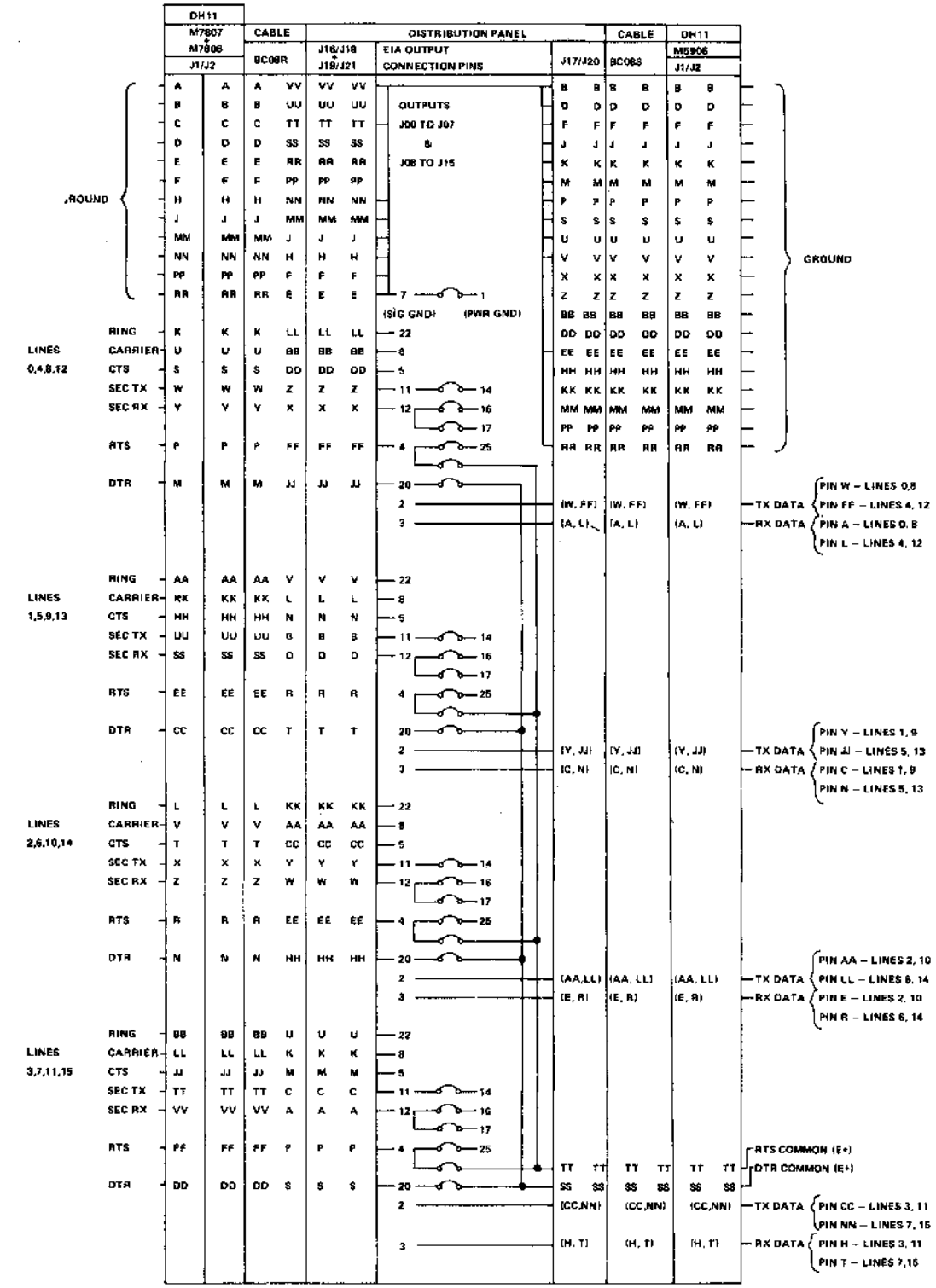
18. Figure 2-8 is a wire location diagram for the DH11-AD, AE to assist in the troubleshooting of individual lines up to the outputs on the distribution panel.

19. Turn on the power. Toggle in the Bootstrap and load the Absolute Loader, if not already done. The addresses and contents of the Bootstrap Loader are listed below.

	Address	Contents
NOTE	–744	016 701
Memory size determines the first three digits	–746	000 026
	–750	012 702
017 for 4K	–752	000 352
037 for 8K	–754	005 211
057 for 12K	–756	105 711
077 for 16K	–760	100 376
117 for 20K	–762	116 162
137 for 24K	–764	000 002
157 for 28K	–766	– 400
	–770	005 267
	–772	177 756
	–774	000 765
	–776	177 560 (keyboard)
		or
		177 550 (high speed reader)

20. Run the diagnostics in accordance with the instructions contained therein. Helpful information may be found in the DH11 Module Test Procedure, A-SP-DH11-0-11. One course of action not mentioned in the procedure is worthy of attention: if a diagnostic does not run, try a couple of other diagnostics before assuming that the diagnostic tape is no good. If both DZDHG and DZDHH run, the DH11 is operational; however, all diagnostics are important and should be run.

21. Run the On-Line Test, DZDHJ, in accordance with the instructions therein. Be sure to remove the M974 from the distribution panel.



NOTES:
1. M7807 – LINES 8 TO 15: J1–8 TO 11; J2–12 TO 15
2. M7808 – LINES 0 TO 7: J1–0 TO 3; J2–4 TO 7
3. DISTRIBUTION PANEL (16 LINES) J16–0 TO 3, J19–8 TO 11, J18–4 TO 7, J21–12 TO 15 } CONTROL; J17–0 TO 7, J20–8 TO 15 – DATA
4. M5906 (16 DATA LINES) J1–8 TO 15; J2–0 TO 7

11-2922

Figure 2-8 DH11-AD, AE Wire Location Diagram

CHAPTER 3
PROGRAMMING

3.1 INTRODUCTION

This chapter contains general DH11 programming information. It is divided into two sections; one lists the bit assignments and functions of the eight registers and the other discusses several DH11 operational features and programming constraints.

3.2 REGISTER BIT ASSIGNMENTS

3.2.1 System Control Register

The System Control Register is a byte-addressable register. The register format is shown in Figure 3-1.

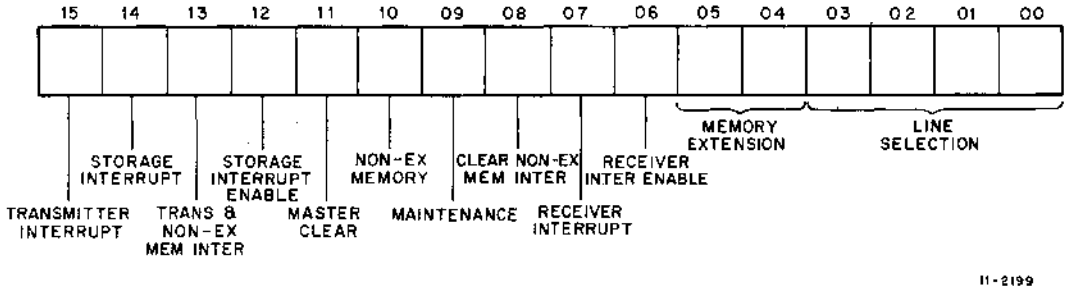


Figure 3-1 System Control Register Format

Bit	Function
00, 01, 02, 03	Line Selection – Each of the 16 lines served by the DH11 has its own storage for line parameter information, current address, and byte count. These storage locations are loaded by the program via the Line Parameter Register, Current Address Register, and Byte Count Register, but the hardware must first be told which line is to have its line parameters, current address, or byte count changed. This routine is accomplished by setting the line selection bits. These bits are read/write.

Bit	Function
04, 05	Memory Extension – The information stored in these bits becomes bits 16 and 17, respectively, of any current address loaded by the program into the Current Address Register. These bits are read/write, but when read, represent only the status of bits 4 and 5 of the System Control Register, not the status of the 16th and 17th address bits of the selected line. (See Paragraph 3.2.8 for further information.) The reason for this arrangement is to permit interrupt service routines to save the contents of the System Control Register accurately.
06	Receiver Interrupt Enable – This bit, when set, enables receiver interrupts (bit 07).
07	Receiver Interrupt – This bit, when set, indicates that the number of characters stored in the silo exceeds the alarm level specified by the low byte of the Silo Status Register. This bit is read only, except in maintenance mode, when it is read/write. When set, this bit generates an interrupt if bit 06 is also set.
08	Clear Non-Existent Memory Interrupt – This bit, when set, clears the non-existent memory interrupt flip-flop (bit 10) and clears itself. This bit is read/write.
09	Maintenance (Read/Write) – This bit, when set, places the DH11 in maintenance mode.
10	Non-Existent Memory – This bit is set whenever the NPR hardware within the DH11 addresses a memory location from which no slave sync signal is received within 20 μs. This indicates that the addressed location or device does not exist. This bit causes an interrupt if bit 13 is set also. This bit is read-only, unless in maintenance mode, at which time it is read/write.
11	Master Clear – This bit, when set, generates the initialize condition within the DH11, clearing the silo, UARTs, and registers. This bit is read/write.
12	Storage Interrupt Enable – This bit, when set, permits the setting of bit 14 to generate an interrupt. This bit is read/write.
13	Transmit and Non-Ex-Mem Interrupt Enable - This bit, when set, permits the setting of bit 10 or 15 to generate an interrupt. This bit is read/write.
14	Storage Interrupt - This bit is set whenever the receiver scanner has found a receiver holding buffer with a character in it and desires to store that character in the silo but cannot do so at this time because of a lack of space. When set, this bit causes an interrupt if bit 12 is set. This bit is read-only, except in maintenance mode, at which time it is read/write.

Bit	Function
15	Transmitter Interrupt – This bit is set whenever the DH11 concludes an NPR cycle that incremented a byte count to 0, indicating the loading of the last character in a message buffer into a UART transmitter holding register. This bit, when set, causes an interrupt if bit 13 is set. This bit is read/write. It is set during an NPR cycle so no hardware/software synchronizing problems occur.

3.2.2 Next Received Character Register

The Next Received Character Register is read-only and is word addressable. The register format is shown in Figure 3-2.

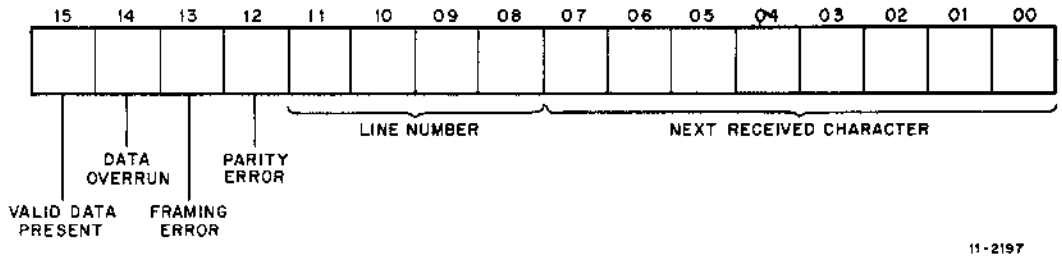


Figure 3-2 Next Received Character Register Format

Bit		Function
00 – 07	00 – 07	These bits contain the next received character, right justified. The least significant bit is bit 00. Unused bits are 0. The parity bit is not shown.
	08 – 11	These bits contain the line number upon which the character was received. Bit 08 is the least significant.
	12	Parity Error – This bit is set if the sense of the parity of the received character does not agree with that designated for that line.
	13	Framing Error – This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.
	14	Data Overrun – This bit is set if the received character is preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer.
	15	Valid Data Present – This bit indicates that the data presented in bits 14 – 00 is valid. It permits the use of a character handling program that takes characters from the silo until there are no more available. This is done by reading this register and checking bit 15 until one obtains a word for which bit 15 is 0.

3.2.3 Line Parameter Register

This register should be loaded only after the System Control Register has had its line selection bits arranged to select the line to which these line parameters are to apply. The register format is shown in Figure 3-3. This register is write-only.

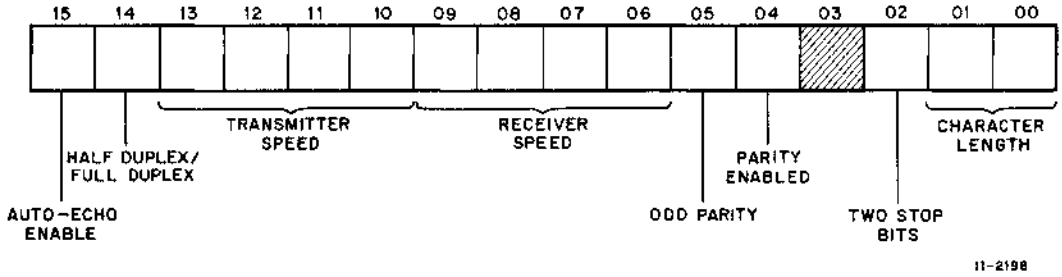


Figure 3-3 Line Parameter Register Format

Bit	Function
00 – 01	Character Length – These bits are set to receive and transmit characters of the length (excluding parity) shown below.

01	00	Bit
0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

02	Two Stop Bits – This bit, when set, conditions a line transmitting with 6, 7, or 8 bit code to transmit characters having two stop marks. If the line is transmitting 5 bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop marks. If this bit is not asserted, 1 stop mark is sent.
03	Reserved (Not used)
04	Parity Enabled – If this bit is set, characters transmitted on the line have an appropriate parity bit affixed, and characters received on the line have their parity checked.
05	Odd Parity – If this bit and bit 4 are set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit 4 is set, characters of even parity are generated on the line and incoming characters are expected to have even parity. If bit 4 is not set, the setting of this bit is immaterial.

Bit	Function
06 – 09	Receiver Speed – The state of these bits determines the operating speed for the receiver of the selected line. The speed table below is applicable.
10 – 13	Transmitter Speed – The state of these bits determines the operating speed for the transmitter of the selected line. The speed table below is applicable.

Speed Table for Receiver and Transmitter Speeds

9 13	8 12	7 11	6 10	(Receiver bits) (Transmitter bits)
0	0	0	0	Zero Baud
0	0	0	1	50 Baud
0	0	1	0	75 Baud
0	0	1	1	110 Baud
0	1	0	0	134.5 Baud
0	1	0	1	150 Baud
0	1	1	0	200 Baud
0	1	1	1	300 Baud
1	0	0	0	600 Baud
1	0	0	1	1200 Baud
1	0	1	0	1800 Baud
1	0	1	1	2400 Baud
1	1	0	0	4800 Baud
1	1	0	1	9600 Baud
1	1	1	0	External Input A
1	1	1	1	External Input B

14	Half Duplex/Full Duplex – If this bit is set, the line is conditioned to operate in half-duplex mode. If this bit is clear, the line is conditioned to operate in full-duplex mode. In this application half duplex means that the DH11 receiver is blinded during transmission of a character.
15	Auto-Echo Enable – When this bit is set, characters received on the line are to be hardware echoed.

3.2.4 Current Address Register

This register should be loaded only after the System Control Register has had the appropriate bits set to select the line number to which this current address is to apply. When this register is loaded, address bits 00 – 15 are transferred into semiconductor memories in the DH11 from bits 00 – 15, respectively, of this register. Address bits 16 – 17 are transferred into semiconductor memories in the DH11 from bits 4 – 5 of the System Control Register.

When this register is read, it indicates the current address of the line selected by the System Control Register. Bits 16 and 17 appear in the Silo Status Register.

3.2.5 Byte Count Register

In the same fashion as the Line Parameter and Current Address Registers, this register should not be loaded or read without first selecting a line number by means of the lower order four bits of the System Control Register. This register should be loaded with the 2's complement of the number of characters (bytes) to be transmitted on that line. The Byte Count Register is read/write.

3.2.6 Buffer Active Register

This register contains one bit for each line. The bits are set individually, using BIS instructions. Setting a bit initiates transmission on the associated line. The bit is cleared by the hardware when the last character to be transmitted on that line is loaded into the transmitter Data Holding Register of the UART for that line. It should be noted that while the clearing of a BAR bit does indicate that a new message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters are sent after the BAR bit clears. These are the last two characters of the message; one of them is starting when the BAR is cleared, and one is the final character loaded into the holding register, thus clearing the BAR bit. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request To Send. Clearly, Request To Send should not be dropped until at least two character times after the BAR bit for a given line clears.

Clearing a BAR bit should not be used to abort transmission on a line. Rather, the byte count for that line should be sent to 0. In this way, a transmitter interrupt is generated. The Buffer Active Register bits are read/write.

3.2.7 Break Control Register

This register contains one bit for each line. Setting a bit in this register immediately generates a break condition on the line corresponding to that bit number; clearing the bit terminates the break condition. The break condition may be timed by sending characters during the break interval, since these characters never actually reach the line.

3.2.8 Silo Status Register

This register is actually two byte-sized registers. The register format is shown in Figure 3-4.

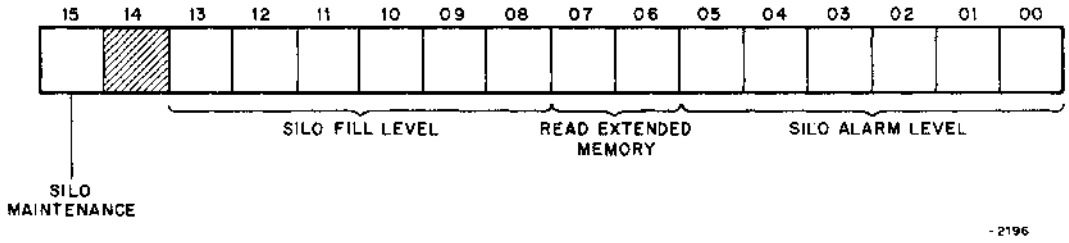


Figure 3-4 Silo Status Register Format

Bit	Function
00 – 05	Silo Alarm Level – The program writes a number corresponding to the desired silo alarm level into this location (see Paragraph 3.3.4, Silo, for programming considerations). When the number of characters stored in the silo exceeds that number, an interrupt (System Control Register bit 7) is generated, if enabled (System Control Register bit 6 is 1). These bits are read/write.

Bit	Function
06 – 07	Read Extended Memory – These bits are read-only and contain the A16 and A17 bits of the current address for the line to which the line selection bits of the System Control Register are pointing.
08 – 13	Silo Fill Level – These bits represent an up-down counter that indicates the actual number of characters in the silo. It should be noted that there are six binary digits; hence numbers between 0 and 63_{10} can be represented. A full silo has 64_{10} entries and appears as 00000, but one may easily tell the difference between an empty silo (00000) and a full silo (00000) by checking the storage overflow bit (bit 14 of the System Control Register). These bits are read-only.
14	Reserved
15	Silo Maintenance – Each time this bit is set, a fixed binary pattern (1010101010101010) is sent to the silo once for checking during maintenance. Clearing and setting loads another copy of the pattern.

3.3 OPERATIONAL FEATURES WITH PROGRAMMING SIGNIFICANCE

3.3.1 Introduction

This section includes the discussion of several operational features of the DH11 that have programming significance. The discussion covers the DH11 device and vector address requirements, the double-buffered feature of the UARTs, operation of the silo, use of break signals, and the function of the maintenance bits.

3.3.2 Floating Device and Vector Addresses

The DH11 uses floating device addresses that are located after the DJ11s in the floating address space that begins at location 160010. Because the DH11 has eight registers, it must be assigned an address that is a multiple of 20 (octal). All DH11s in a system should have consecutive addresses.

Example 1: A system with no DJ11s, but two DH11s:

160010 Cannot use for DH11s because not multiple of 20.
160020 First DH11
160040 Second DH11
160060 DH11 gap (indicates that there are no more DH11s).

Example 2: A system with one DJ11, two DH11s:

160010 First DJ11
160020 DJ11 gap (indicates that there are no more DJ11s).
160030 Cannot use for DH11s because not multiple of 20.
160040 First DH11
160060 Second DH11
160100 DH11 gap (indicates that there are no more DH11s).

The DH11 requires two vector addresses which follow those of the DJ11 in the floating vector space that starts at address 300. The vectors starting at 300 are used in the following order: DC11; KL11/DL11-A,B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Readers; PA611 Punches; DT11; DX11; DL11-C,D,E; DJ11; DH11.

Of the two DH11 vectors, the receiver vector is the lower numbered vector. The priority of the receiver and transmitter interrupts are individually selectable by means of two standard PDP-11 priority jumper plugs.

3.3.3 Double-Buffered Receivers and Transmitters

The receiver and transmitter sections of the UART are double-buffered; that is, each section contains a Shift Register and a Holding Register. For the receiver, the serial input character goes to the Shift Register which performs a serial-to-parallel conversion and transfers the character in parallel to the Holding Register. At this point, the DA (Received Data Available) flag goes high. In the DH11, the DA flags of the 16 UARTs are sampled by the receiver scanner. If the scanner finds a high DA flag, it copies the data from the receiver Holding Register into the silo, if space is available. If space is not available, the Storage Interrupt bit in the CSR is set and a receiver interrupt is generated, if enabled. This does not mean that the data has been lost. Rather, it indicates that the data in this or any other receiver Holding Register will be lost if the scanner cannot move the data to the silo before an additional character arrives on the line. Actual data loss is apparent to the program when characters are received with the DATA OVERRUN bit set.

For the transmitter, the Holding Register can be loaded in parallel with a character to be transmitted when the TBMT (Transmitter Buffer Empty) flag goes high. The character is automatically transferred to the Shift Register when this register becomes empty. The desired start, stop, and parity bits are added to the character and serial transmission begins. At the end of a character transmission, the EOC (End of Character) flag goes high and remains in this state until transmission of a new character begins.

3.3.4 Silo

The silo, actually more similar in design to a granary, is a first-in, first-out buffer store. A parallel loaded 16-bit word (see Paragraph 3.2.2 for the format) automatically propagates downward into the first location not already containing a word. When the silo is empty, the word propagates directly into the Next Received Character Register. The propagation time from the top of the silo to the bottom may be as much as 32 μs. For this reason, the hardware is arranged such that the receiver interrupt is not generated until the number of characters in the silo exceeds the silo alarm level and there is at least one character in the bottom of the silo. This arrangement is necessary because the up-down counter that indicates the number of characters in the silo indicates exactly that: the number of characters in the silo, which includes those resting in the bottom and those propagating downward.

While the hardware arrangement protects the case where the silo is empty and the alarm level is zero, the number of characters in the silo and the number actually available to be serviced may differ due to the propagation time. If having at least one character in the bottom of the silo was not made a condition in the interrupt generation, the program would receive an interrupt while the single character in the silo was propagating downward. For this reason, character handling programs should not assume there are some particular number of characters in the silo when servicing begins. Rather, the program should extract a character, check the valid data present bit (bit 15) and handle the character; then the program should extract the next character and repeat the process until bit 15 no longer tests as a 1. At that time, the silo may be assumed to be empty (although there may be another character propagating downward) and the character handling routine may be terminated until another receiver interrupt is received.

On very fast processors, such as the PDP-11/45, the program should avoid reading the Next Received Character Register more often than once per μs, as it takes 1 μs for characters in the silo to shift downward one position. Since the typical program checks bit 15 and moves the character to some location, it is anticipated that this speed requirement will not pose a problem.

The silo alarm level can be set to any number from 0 through 63. However, care should be taken that an appropriate alarm level be chosen to suit software/hardware timing and system throughput requirements. At any silo alarm level, once the program enters the receive interrupt routine it is best to read all words from the NRC, checking bit 15 of each one, until a word is encountered with bit 15 equal to a zero. This implies that the silo is empty, and will maximize the usefulness of the silo alarm feature.

The programmer must be aware that new characters may enter the silo as it is being emptied, so that the silo alarm level is not meant to indicate the exact silo fill level except at the moment it interrupts. It is recommended that the receiver interrupt service routine which reads the NRC be run at a priority level equal to or higher than that of the DH11. If the receiver is able to interrupt its own service routine while the silo is being emptied, extra interrupts will be generated due to interaction of incoming data, the silo fill level, and the silo alarm level.

3.3.5 Zero Baud

A speed selection of 0 Baud is provided so that the program may turn off any line. This is useful should excessive circuit noise on an unused line cause the receipt of annoying quantities of bogus characters.

3.3.6 Break Signals

When the Break Control Register has been conditioned to transmit a break signal on a particular line, DH11 logic immediately forces the output on that line to the space (0) condition.

The generation of a transmitter interrupt occurs when the last character of a message has been loaded into a UART transmitter from a message table in the PDP-11 memory. It is thus appropriate at that time for the program to set up a new message in memory and to load the appropriate current address and byte count so that the new message can begin when the old one is finished.

It is important to note that the former message is not finished when the transmitter interrupt is given; rather, the use of the memory table is finished. In terms of the actual serial communications line, there are two more characters left to go. One of these characters is in the UART transmitter's Shift Register; the other is in the UART transmitter's Holding Register.

The consequence of the above condition is that to send a break signal, one should load two nulls (all 1s) and wait for a transmitter interrupt before setting the appropriate bit in the Break Control Register. In this way, generation of a break does not interrupt the transmission of any printing characters. In like manner, when using characters to time the transmission of a break signal, nulls should be used so that when the break condition is terminated by clearing the bit in the Break Control Register, no printing characters are produced from the UART Shift and Holding Registers.

3.3.7 Initialize Signal

The Initialize signal clears the silo, UARTs, and all registers except the Current Address and Byte Count Registers. All scanners are forced to line 00 but continue operation from there.

3.3.8 Maintenance Bits SCR 09 and SSR 15

Setting bit SCR 09 (Maintenance) causes the following action:

> Enables the ability of the program to write SCR 07 (Receiver Interrupt), SCR 10 (Non-Existent Memory Interrupt), and SCR 14 (Storage Overflow Interrupt) bits. This write capability is normally not enabled as it can produce hardware/software synchronization problems unless carefully done.

The following precaution must be observed in the maintenance mode. If the program reads bit 7 of the SCR and finds that it is a 1, the program must perform a Bit Clear instruction on bit 7 before reading the NRC. This is required because in the maintenance mode, bit 7 is an OR function of the output of a program-controlled flip-flop and a signal from the silo alarm circuit. If SCR bit 7 is read, and is found to be a 1, and the Bit Clear instruction is not performed, the flip-flop is set during the restore portion of the Unibus read cycle. Because of the OR function, the flip-flop masks the transitions of the silo alarm circuit that occurs when the NRC is read. These transitions are required for proper operation of the M7821 Interrupt Module.

Loops the transmitted data leads (serial out line 00 – 15) to the received data leads (serial in line 00 – 15).

Setting bit SSR 15 (Silo Maintenance) causes the inputs of the silo to be set to a 1010101010101010 bit pattern, and a single 16-bit character made up of this pattern to be loaded into the silo. Successive clears and sets of SSR 15 repeat this procedure. All receiver speeds should be set to 0 Baud and the silo emptied before this is done, so that no data from the incoming serial lines is placed in the silo while it is under test.

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