

digital

RX01

Engineering Drawings

Digital Equipment Corporation

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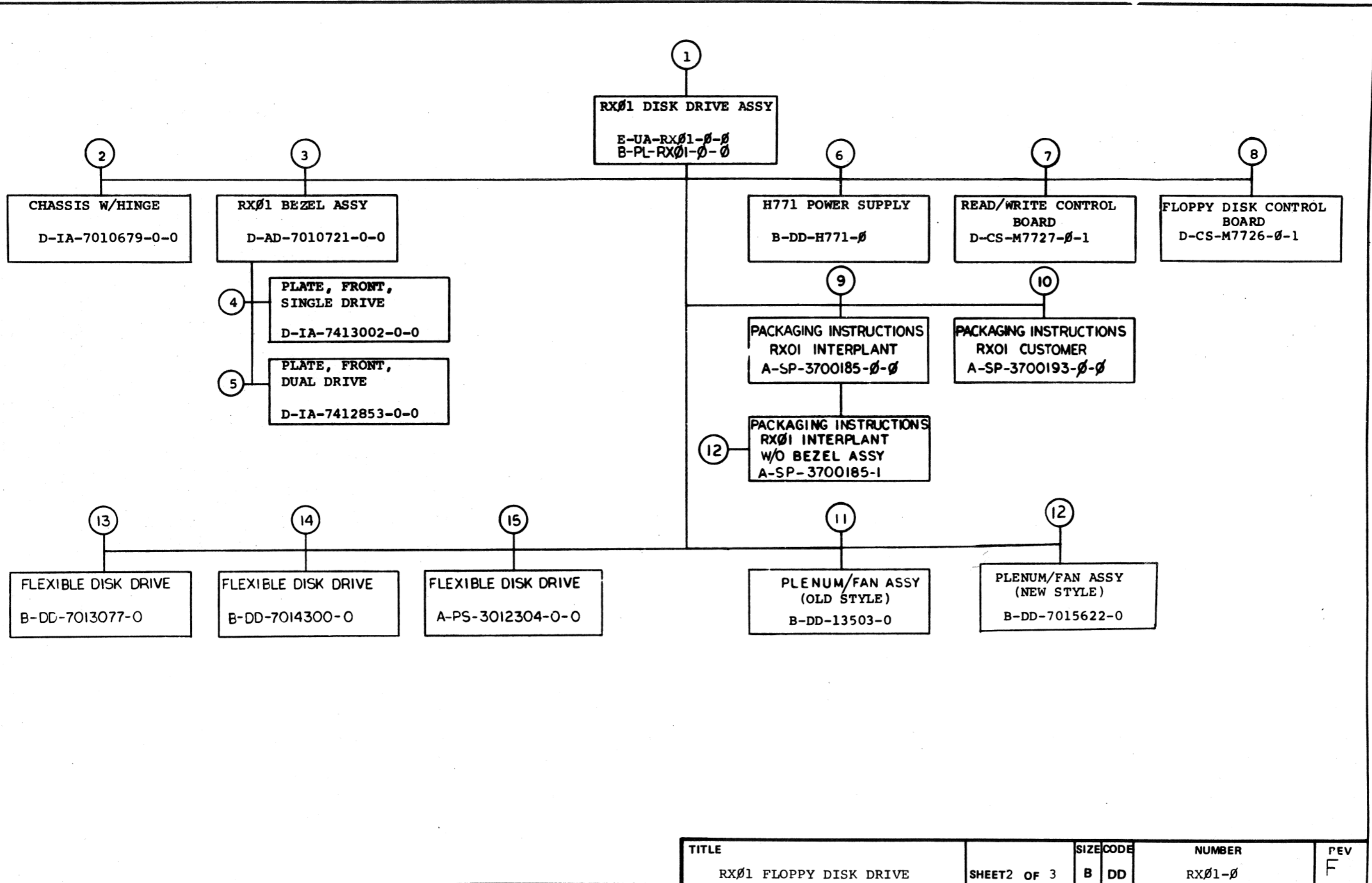
1956

1957

1958

1959

1960



TITLE	SIZE CODE	NUMBER	REV
RX01 FLOPPY DISK DRIVE	B DD	RX01-0	F

SHEET 2 OF 3

ML

CUSTOMER PRINT SET					MECHANICAL					CUSTOMER PRINT SET					ELECTRICAL				
MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FR. DATE	MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FR. DATE						
	1	E-UA-RX01-0-0		5	RX01 FLOPPY DISK DRIVE ASSY		X				3	RX01 FLOPPY DISK DRIVE							
		E-PL-RX01-0-0			RX01 FLOPPY DISK DRIVE ASSY (PI)														
		E-IA-7412666-0-0		1	COVER, TOP														
		D-IA-7010640-0-0		1	CABLE, EXTENSION, RX01														
		C-IA-7008612-0-0		1	CABLE, KEYCARD						34	RX01 ENGINEERING SPECIFICATION							
		D-UA-RC05L-0-0		1	CABLE, JUMPER		C						RX01 FIRMWARE LISTING						
		D-IA-7010696-0-0		1	HARNASS, VOLTAGE VARIATION														
				1	BRACKET SHIPPING RX01														
		C-MD-7409479-0-0		1	PLATE, PRESSURE					12		A SP 3700185-1	PACK INSTR W/O BEZEL						
		C-MD-5509081-0-0		1	PANEL, LIGHT (RX01)							A-PS-9905183	LAMINATED BUILDUP						
												A-PS-9905710-0-0	REGULAR SLOTTED CARTON						
												A-PS-9905712-0-0	PLYWOOD SUPPORT FIXTURE						
												A-PS-9905713-0-0	SCORED SHEET						
												A-PS 9905729-0-0	CARTON SEALING TAPE						
	2	D-IA-7010679-0-0		1	CHASSIS W/HINGE														
		E-IA-7412665-0-0		1	CHASSIS, FLEXIBLE DISK DRIVE														
		C-MD-7413236-0-0		1	HINGE, LOGIC														
	3	D-AD-7010721-0-0		1	RX01 BEZEL ASSY		X			7		D-CS-M7727-0-1	READ/WRITE CONTROL BOARD						
		E-MD-7412664-0-0		1	BEZEL, RX01							D-IA-5011370-0-0	ETCHED CIRCUIT BOARD (M7727)						
		A-PS-3612317-0-0		1	LOGO, RX01														
	4	D-IA-7413002-0-0		1	PLATE, FRONT, SINGLE DRIVE														
		C-SS-7413002-0-1		1	SILK SCREEN, SINGLE DRIVE		X			8		D-CS-M7726-0-1	FLOPPY DISK CONTROL BOARD						
												A-SP-M7726-0-7	ACCEPTANCE TEST PROCEDURE						
	5	D-IA-7412853-0-0		1	PLATE, FRONT, DUAL DRIVES														
		C-SS-7412853-0-1		1	SILK SCREEN, DUAL DRIVE							9	A-SP-3700185-0-0	PACKAGING INST. INTERPLANT					
													A-PS-9905710-0-0	REGULAR SLOTTED CARTON					
													A-PS-9905711-0-0	ONE PIECE FOLDER					
C	6	B-DD-H771-0		3	H771 POWER SUPPLY								A-PS-9905712-0-0	PLYWOOD SUPPORT FIXTURE					
		C-MD-7413350-0-0											A-PS-9905713-0-0	SCORED SHEET					
													A-PS-9905729-0-0	CARTON SEALING TAPE					
X	11	B-DD-7013503-0-0		3	PLENUM/FAN ASSY (OLD STYLE)							10	A-SP-3700193-0-0	PACKAGING INST. CUSTOMER					
													A-PS-9905741-0-0	FULL TELESCOPE CAP					
	13	B-DD-7013077-0		3	FLEXIBLE DISK DRIVE								A-PS-9905740-0-0	FOAM PAD					
													A-PS-9905739-0-0	LAMINATED BUILDUP					
	14	B-DD-7014300-0		3	FLEXIBLE DISK DRIVE								A-PS-9905734-0-0	PLASTIC STRAPPING					
	15	A-PS-3012704-0-0		14	FLEXIBLE DISK DRIVE														
	16	B-DD-7015622-0-0		2	PLENUM/FAN ASSY NEW STYLE														

CUSTOMER PRINT SET CODES
X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE
RX01 FLOPPY DISK DRIVE
SHEET 3 OF 3
SIZE CODE
B DD
NUMBER
RX01-0
REV
F

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PARTS LIST

Table with 5 columns: QTY, REF DESIGNATION, DESCRIPTION, PART NO., ITEM. Lists various electronic components like resistors, capacitors, diodes, and ICs.

Table with 3 columns: CHK, CHANGE NO, REV. For tracking revisions.

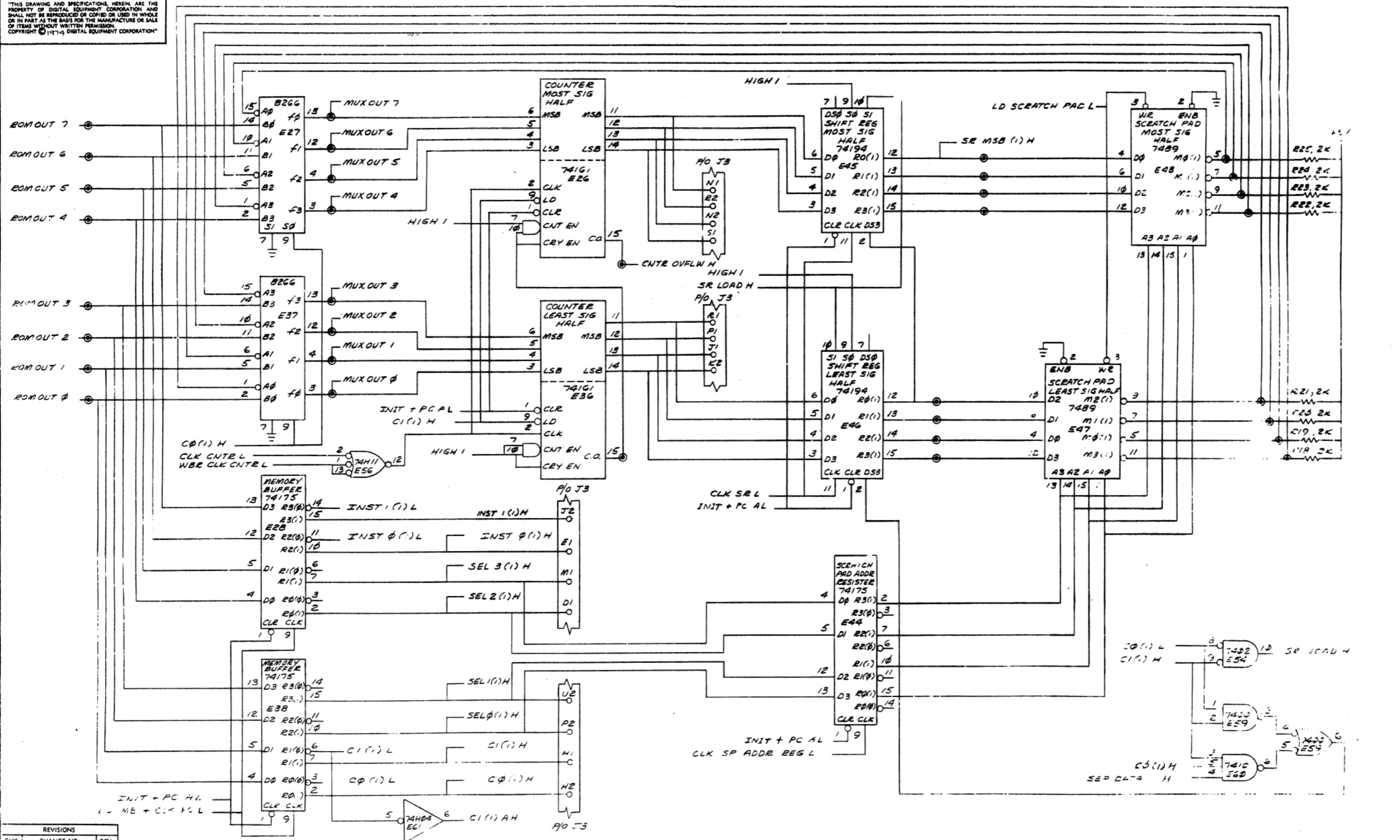
PARTS LIST

Table with 5 columns: QTY, REF DESIGNATION, DESCRIPTION, PART NO., ITEM. Continuation of parts list with various ICs and connectors.

Table with 4 columns: TYPE, LOCATION, PINS, DESCRIPTION. Lists spare IC gates and their pin configurations.

Table with 5 columns: TYPE, ITEM #, P.N., TYPE, P.N. Lists allowable substitutions for components.

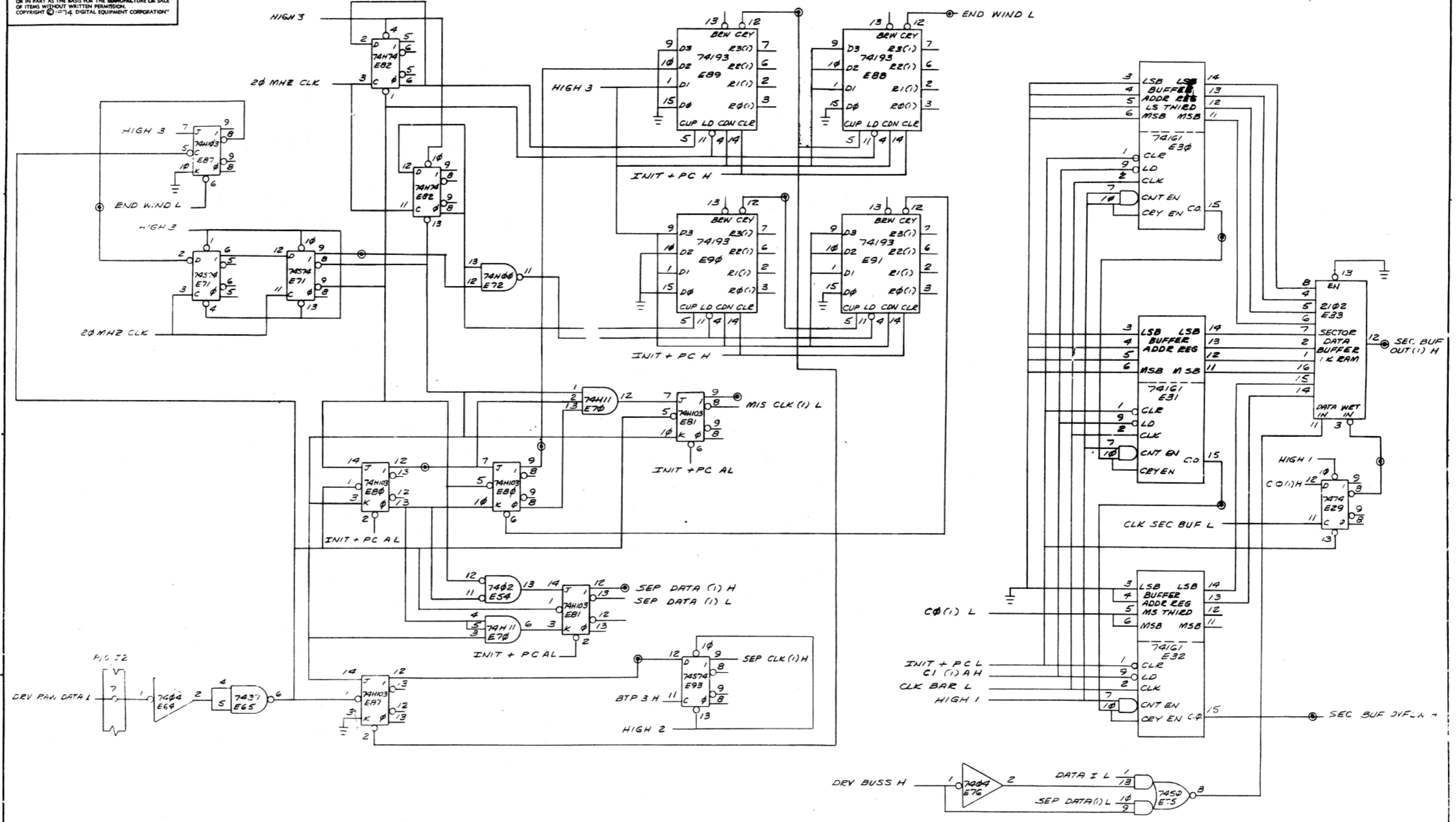
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REVISIONS		
CHK	CHANGE NO.	REV

TITLE	DISK CONTROLLER (3)	SIZE CODE	NUMBER	REV
SCALE	SHEET 3 OF 9	DIST.	DWG 47726	

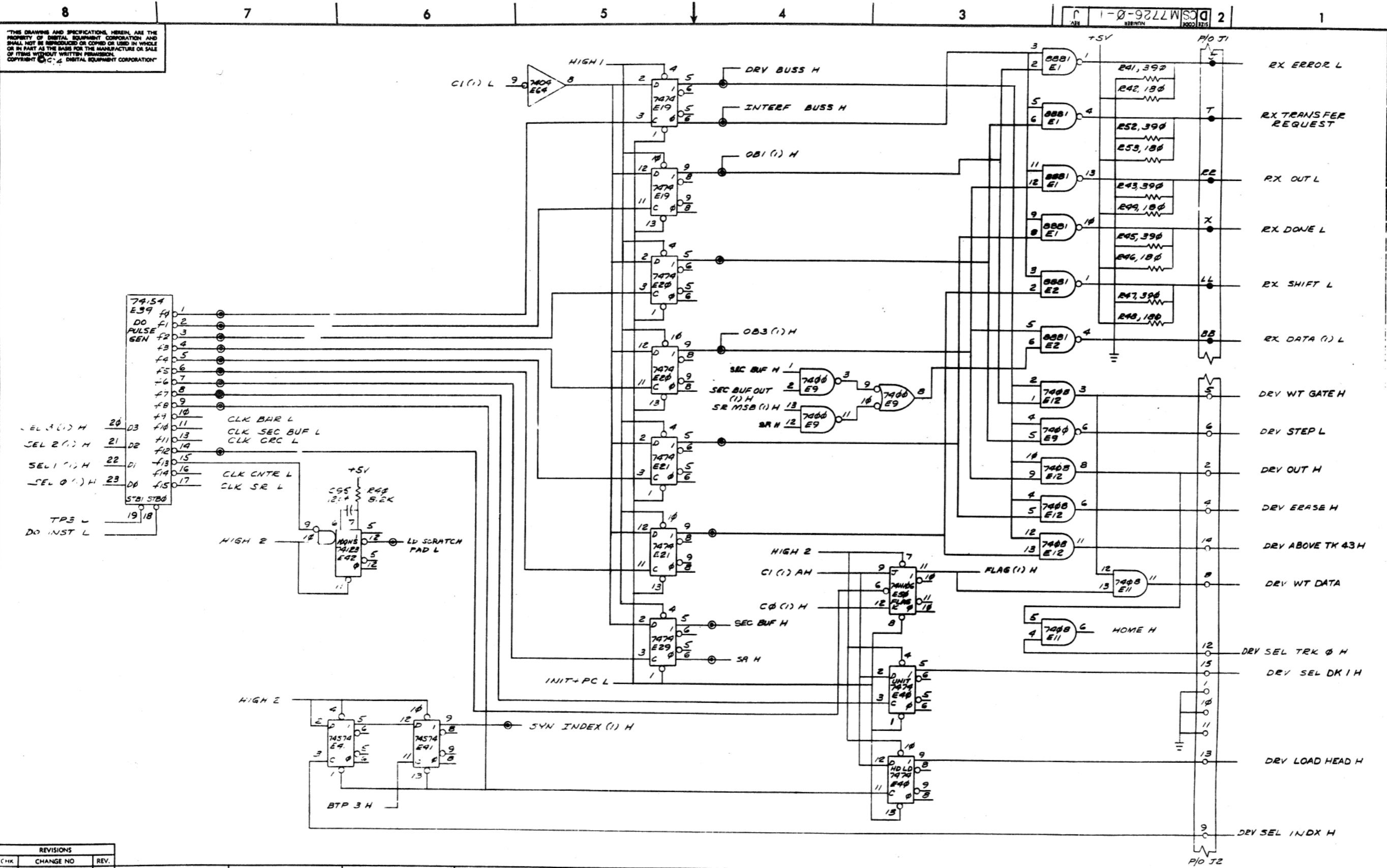
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REVISIONS		
CHK	CHANGE NO	REV.

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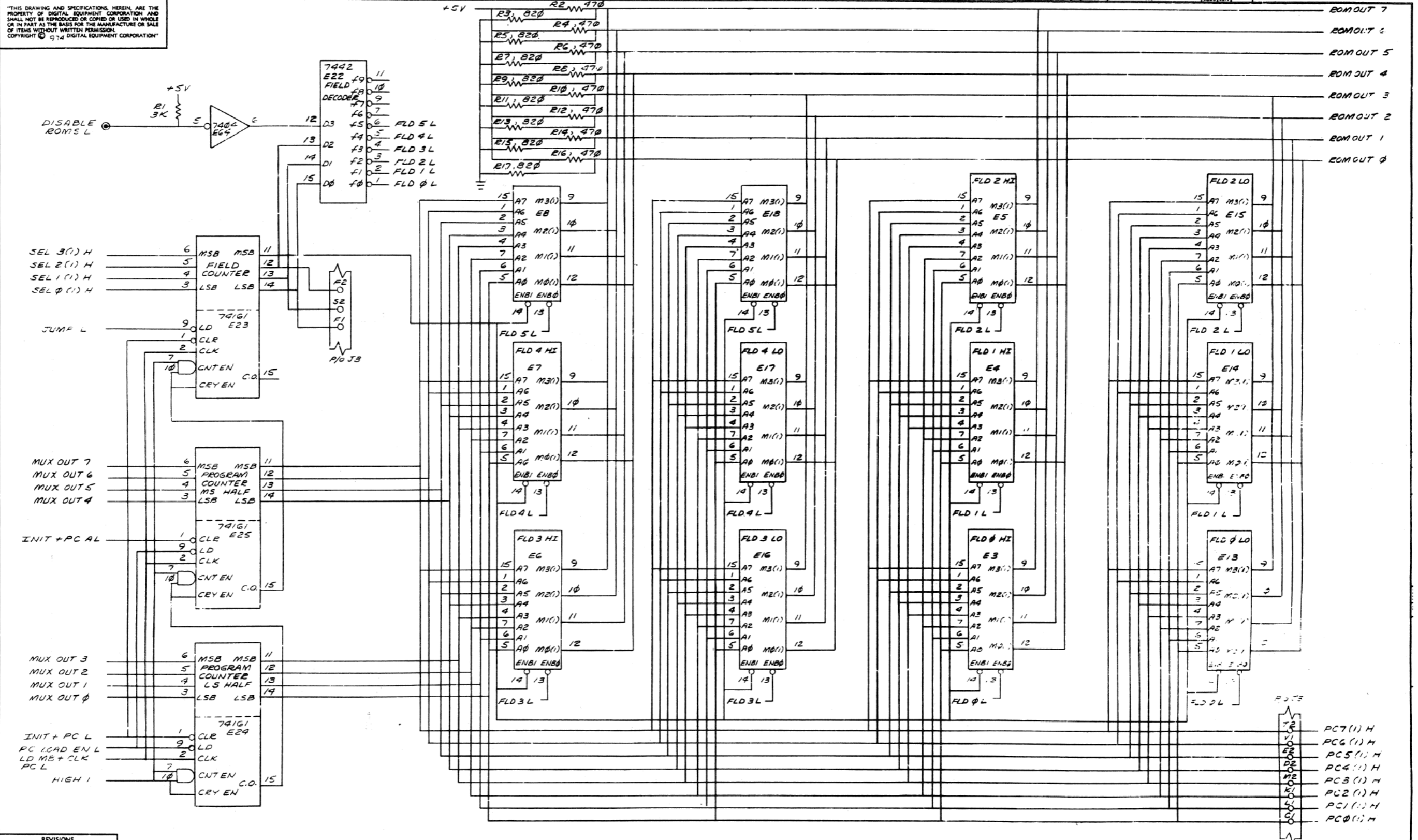
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REVISIONS		
CHK	CHANGE NO	REV.

TITLE	FLOPPY DISK CONTROLLER (D5)	SIZE CODE	D	NUMBER	M7726-0-1	REV.	J
SCALE		SHEET	5	OF	9	DIST.	

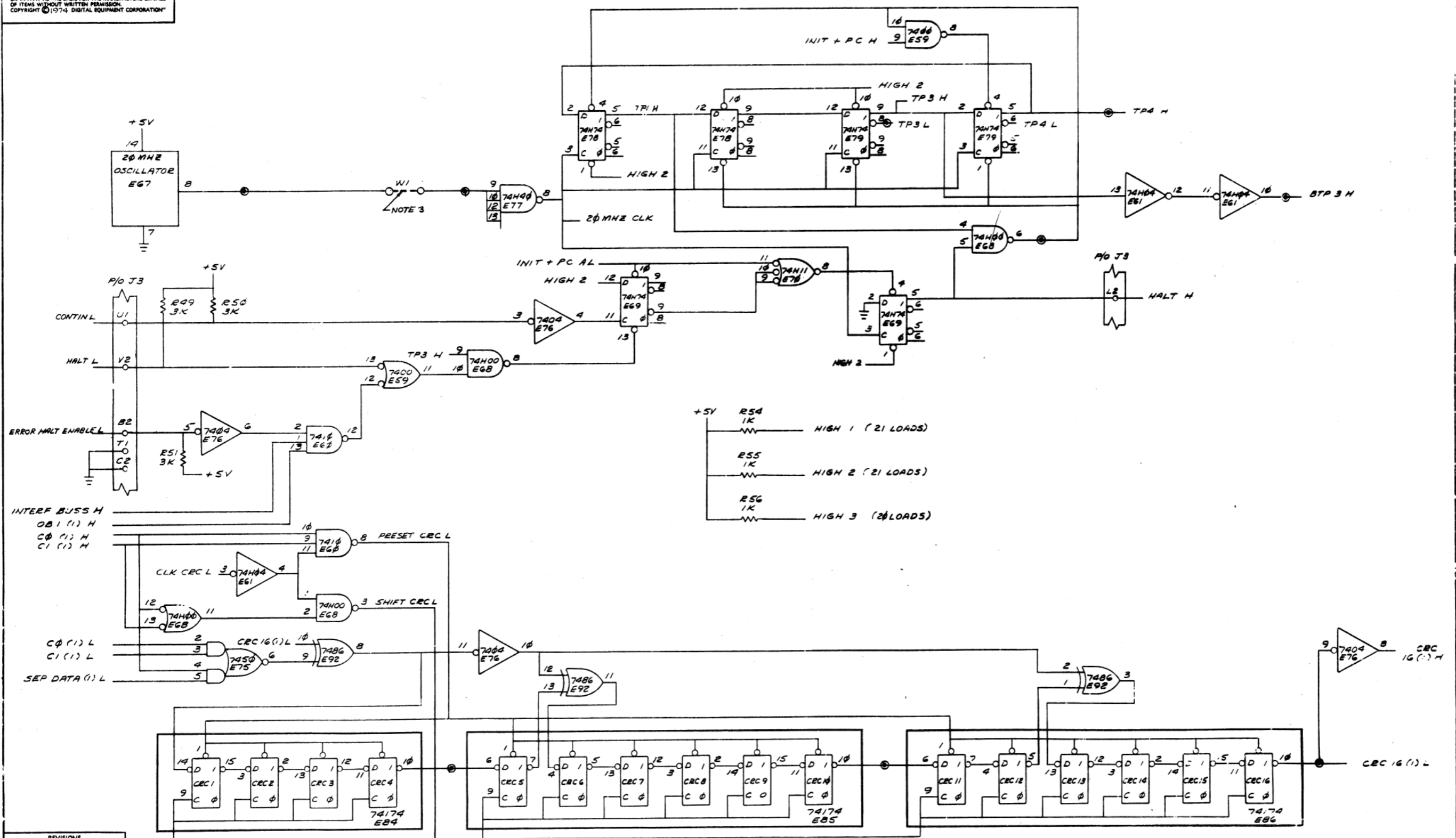
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REVISIONS		
CHK	CHANGE NO.	REV.

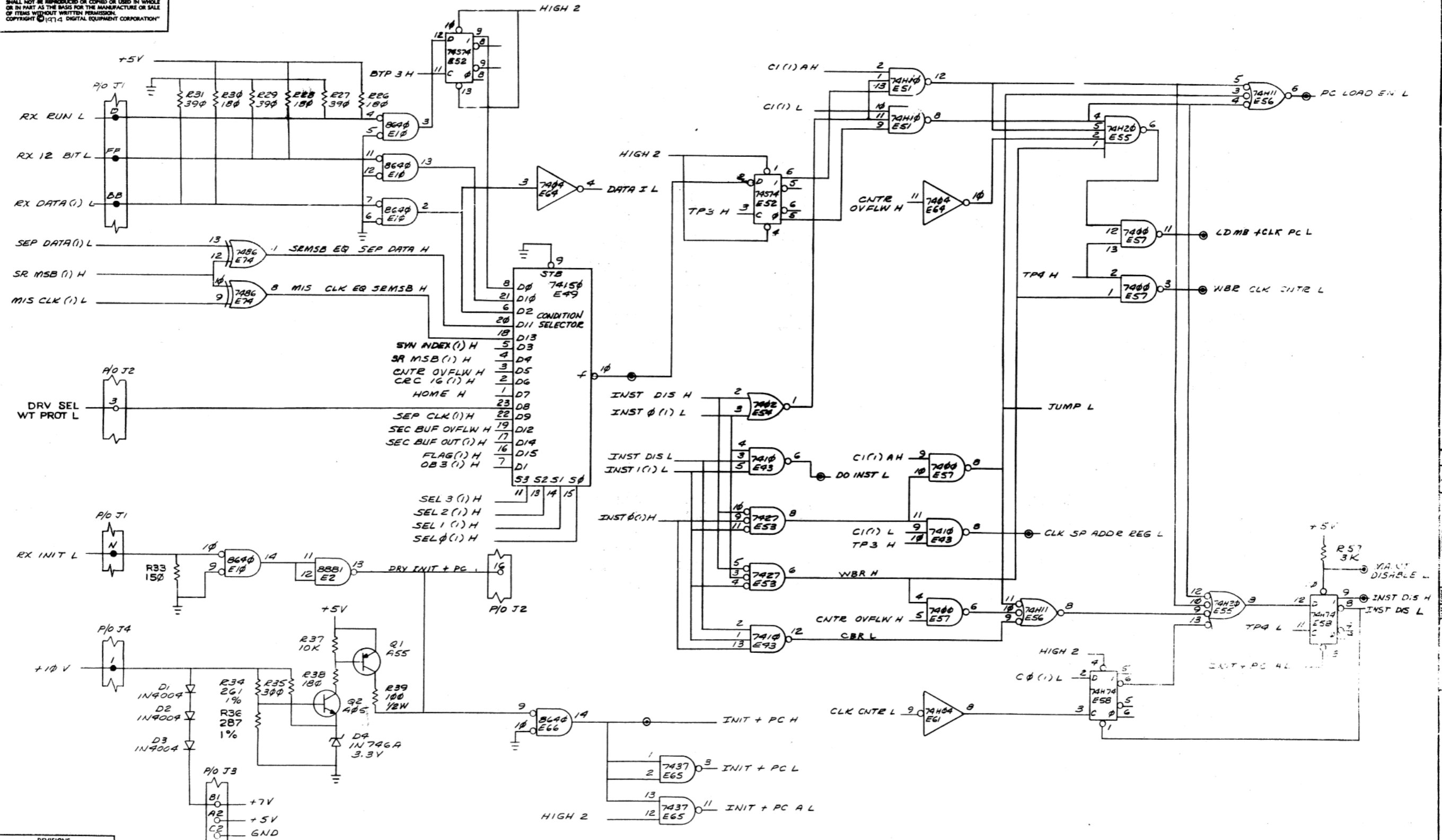
TITLE FLOPPY DISK CONTROLLER (06) SIZE CODE NUMBER DIST. DCS M7726-2-1 REV. 1

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REVISIONS			TITLE		SIZE CODE	NUMBER	REV.
CHK	CHANGE NO.	REV.	FLOPPY DISK CONTROLLER (07)		DCS	M7726-0-1	J
			SCALE	SHEET 7 OF 9	DIST.		

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	FLOPPY DISK CONTROLLER (DB)	SIZE CODE	DOSM7726-0-1	NUMBER		REV.	J
SCALE		SHEET	8 OF 9	DIST			

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THIS LIST GIVES THE SOURCE AND DESTINATIONS OF SIGNAL NAMES WITHIN THE M7726 PRINT SET. SIGNAL NAMES THAT DO NOT APPEAR ON THIS LIST ARE PRESENT FOR INFORMATION ONLY. THEY DO NOT INDICATE CONNECTIONS TO OTHER POINTS IN THE PRINT SET.

INTERFACE REFERS TO SIGNALS ON THE INTERFACE BUSS
 DRIVE REFERS TO SIGNALS ON THE DRIVE BUSS
 POWER SUPPLY REFERS TO VOLTAGES FROM THE POWER SUPPLY
 KM11 REFERS TO SIGNALS ON J3 THE MAINTENANCE CONNECTOR

SIGNAL NAME	ORIGIN	DESTINATION
BTP J H	D7-C1	D4-A5, D5-A6, D8-D6
CLK BAR L	D5-C7	D4-A3
CLK CNTR L	D5-B7	D3-B7, D8-A4
CLK CRC L	D5-C7	D7-B7
CMTR OVFLW H	D3-C5	D8-D4, D8-C5, D8-B4
CLK SRC BUF L	D5-C7	D4-B2
CLK SP ADDR REG L	D8-B3	D3-A4
CLK SR L	D5-B7	D3-B4
CONTIN L	KM11	D7-C7
CNC10 (1) H	D7-B1	D8-C6
CNC10 (1) L	D7-A1	D7-B7
C1 (1) AM	D3-A6	D4-B3, D5-B4, D8-D4, D8-C4
C1 (1) H	D3-A6	D3-C6, D3-B2, D7-B8
C1 (1) L	D3-A6	D5-D6, D7-B8, D8-D4, D8-B4
C0 (1) H	D3-A6	D3-C7, D3-A2, D4-B1, D5-B4, D7-B8
C0 (1) L	D3-A6	D3-B2, D4-B3, D7-B8, D8-B3
DATA I L	D8-D5	D4-A2
DISABLE ROMS L	TEST PAD	D8-DW
DO INST L	D8-H4	D5-HH
DRV BUSS H	D5-D4	D4-A4
DRV ERASE H	D5-B1	DRIVE
DRV OUT H	D5-C1	DRIVE
DRV LOCAL -EAD H	D5-A1	DRIVE
DRV STEP	D5-C1	DRIVE
DRV INIT - PC	D8-H6	DRIVE
DRV ABOVE TK 43 H	D5-B1	DRIVE
DRV RAW DATA L	DRIVE	D4-A8
DRV SEL DK 1 H	D5-B1	DRIVE
DRV SEL INDX H	DRIVE	D5-A1
DRV SEL TRK 0 H	DRIVE	D5-B1
DRV WT DATA	DRIVE	D5-B1
DRV WT GATE H	D5-C1	DRIVE
DRV EEL WT PROT L	DRIVE	D8-C8
END WIND L	D4-D3	D4-D8
ERROR HLT ENABLE L	KM11	D7-C7

OB1 (1) H	D5-D4	D7-B8
OB3 (1) H	D5-C4	D8-B6
PC 0 (1) H	D6-A1	KM11
PC 1 (1) H	D6-A1	KM11
PC 2 (1) H	D6-A1	KM11
PC 3 (1) H	D6-A1	KM11
PC 4 (1) H	D6-A1	KM11
PC 5 (1) H	D6-A1	KM11
PC 6 (1) H	D6-A1	KM11
PC 7 (1) H	D6-A1	KM11
PC LOAD EN L	D8-D1	D6-A8
ROM OUT 0	D6-D1	D3-C8
ROM OUT 1	D6-D1	D3-C8
ROM OUT 2	D6-D1	D3-C8
ROM OUT 3	D6-D1	D3-C8
ROM OUT 4	D6-D1	D3-C8
ROM OUT 5	D6-D1	D3-D8
ROM OUT 6	D6-D1	D3-D8
ROM OUT 7	D6-D1	D3-D8
RX DATA (1) L	D5-C1, INTERFACE	INTERFACE, D8-D8
RX DONE L	D5-D1	INTERFACE
RX ERROR L	D5-D1	INTERFACE
RX INIT L	INTERFACE	INTERFACE
RX OUT L	D5-D1	INTERFACE
RX RUN L	INTERFACE	D8-D8
RX SHIFT L	D5-C1	INTERFACE
RX TRANSFER REQUEST	D5-D1	INTERFACE
RX 12 HIT L	INTERFACE	D8-D8
SRC BUF OVFLW H	D4-A1	D8-C6
SRC HUF OUT (1) H	D4-C1	D5-C4, D8-B6
SRC HUF H	D5-B4	D5-C4
SFL 0 (1) H	D3-A6	D5-C8, D6-C8, D8-B6, KM11
SEL 1 (1) H	D3-A6	D5-C8, D6-C8, D8-B6, KM11
SEL 2 (1) H	D3-B6	D5-C8, D6-C8, D8-B6, KM11
SEL 3 (1) H	D3-B6	D5-C8, D6-C8, D8-B6, KM11
SEP CLK (1) H	D4-B4	D4-B4
SEP DATA (1) H	D4-B5	D8-C6
SEP DATA (1) L	D4-B5	D3-A2
SR H	D4-B5	D4-A2, D7-A8, D4-C8
SR LOAD H	D5-B4	D5-C4
SR HSB (1) H	D3-B1	D3-C4
SR HSB (1) L	D3-D3	D5-C4, D8-C8, D8-C6
SYM INDEX (1) H	D5-A5	D8-C6

FLAG (1) H	D5-B3	D8-B6
FLD 0 L	D6-D6	D6-A3, D6-A2
FLD 1 L	D6-D6	D6-B3, D6-B2
FLD 2 L	D6-D6	D6-C3, D6-C2
FLD 3 L	D6-D6	D6-A6, D6-A4
FLD 4 L	D6-D6	D6-B6, D6-B4
FLD 5 L	D6-D6	D6-C6, D6-C4
HALT H	D7-C3	KM11
HALT L	KM11	D7-C7
HIGH 1	D7-C4	D3-D6, D3-D4, D3-C6, D3-C4, D4-A3
HIGH 2	D7-B4	D4-B1, D5-D5, D6-A8
HIGH 3	D7-B4	D4-A5, D5-B7, D5-A7, D5-B4, D7-D5
HONE H	D5-H2	D7-D4, D7-C4, D7-C5, D8-D5, D8-B3
INIT + PC A L	D8-A1	D8-A5
INIT + PC H	D8-A4	D4-D8, D4-C8, D4-D7, D4-D5, D8-C6
INIT + PC L	D8-A4	D4-B5, D4-B8, D7-C5, D8-B2
INST 0 (1) H	D3-B6	D4-D5, D4-C5, D7-D4
INST 0 (1) L	D3-B6	D4-B3, D5-R5, D6-A8
INST 1 (1) H	D3-B6	KM11, D8-H5
INST 1 (1) L	D3-B6	D8-C5
INST DIS H	D8-B1	KM11
INST DIS L	D8-R1	D8-H5
INTERF BUSS H	D5-D4	D7-HR
JUMP L	D8-C3	D6-C4
LD MR + CLK PC L	D8-C1	D8-AH, D3-AH
LD SATCH PAD L	D8-H6	D7-HR
MAINT DIS L	TEST PAD	D8-H1
MIS CLK (1) L	D4-C4	D8-CU
MUX OUT 0	D3-C7	D6-AR
MUX OUT 1	D3-C7	D6-AR
MUX OUT 2	D3-C7	D6-AR
MUX OUT 3	D3-C7	D6-HR
MUX OUT 4	D3-C7	D6-HR
MUX OUT 5	D3-D7	D6-HR
MUX OUT 6	D3-D7	D6-HR
MUX OUT 7	D3-D7	D6-HR

TP3 H	D7-D3	D7-C6, D8-B4, D8-C5
TP3 L	D7-D3	D5-H8
TP4 H	D7-D2	D8-C3
TP4 L	D7-D3	D8-H2
WAR CLK CNTR L	D8-C2	D3-B7
20 MHZ CLK	D7-C5	D4-C8, D4-D7
GND	POWER SUPPLY	D1-A4
+5V	POWER SUPPLY	D1-A4, D8-C7
+7V	POWER SUPPLY	KM11
+10V	POWER SUPPLY	D8-H8

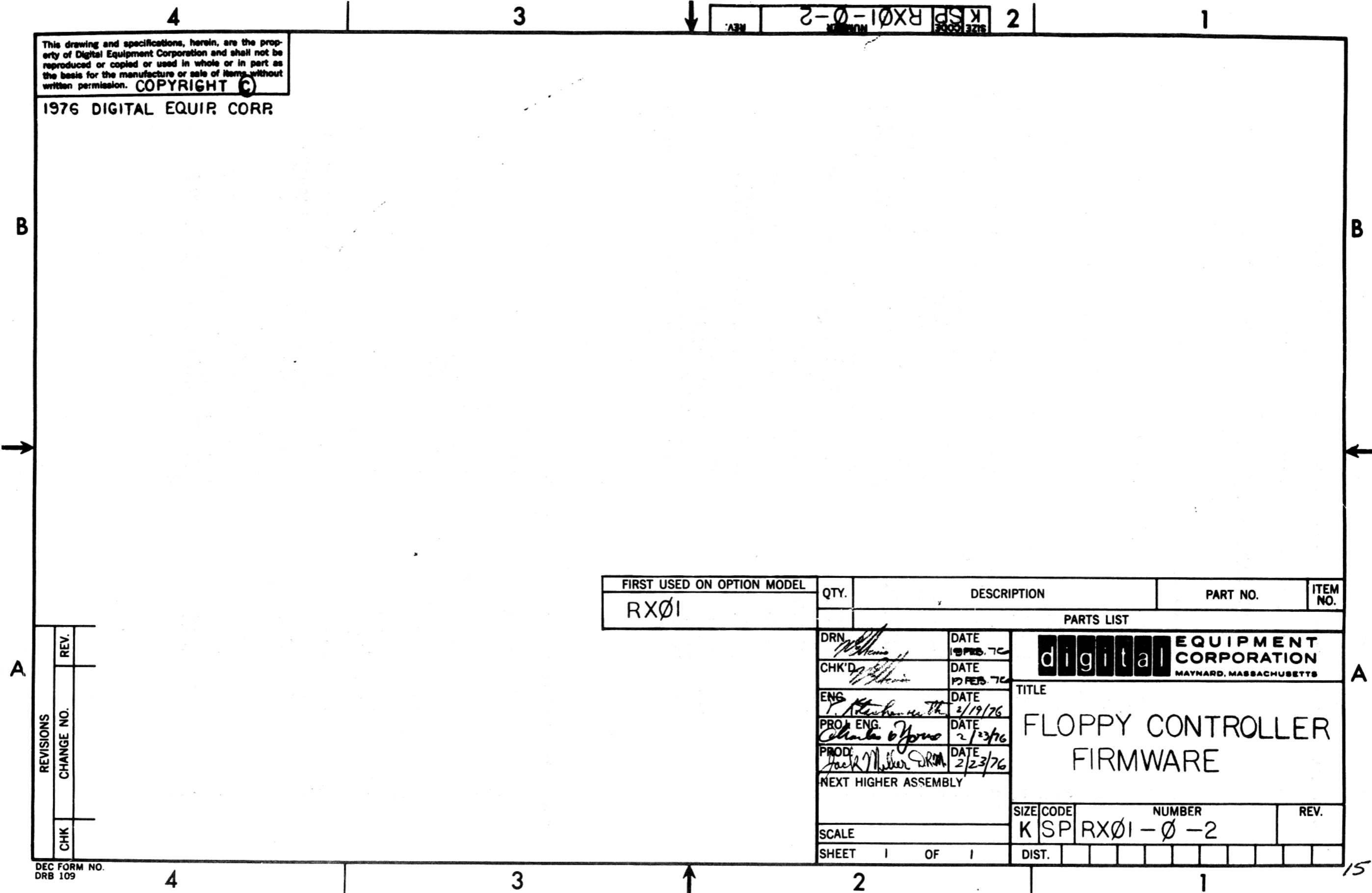
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
FLOPPY DISK CONTROLER	DCS	M7726-0-1	J
SCALE	SHEET 9	OF 9	DIST.

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SIZE CODE K SP
 NUMBER RXØ1-Ø-2
 REV. 2



FIRST USED ON OPTION MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RXØ1				
PARTS LIST				
DRN <i>W. H. Hines</i>	DATE 19 FEB 76	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS TITLE FLOPPY CONTROLLER FIRMWARE		
CHK'D <i>W. H. Hines</i>	DATE 17 FEB 76			
ENG <i>P. A. Steinhilber</i>	DATE 2/19/76			
PROJ. ENG. <i>Charles G. Jones</i>	DATE 2/23/76			
PROJ. <i>Jack Miller</i>	DATE 2/23/76			
NEXT HIGHER ASSEMBLY				
SCALE		SIZE CODE K SP	NUMBER RXØ1-Ø-2	REV.
SHEET 1 OF 1		DIST.		

REVISIONS	REV.
	CHANGE NO.
CHK	

DEC FORM NO. DRB 109

4 3 2 1

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/RX01 FLOPPY CONTROLLER FIRMWARE

/THIS SYMBOL TABLE REPLACES THE NORMAL PAL SYMBOL TABLE AND DEFINES /THE INSTRUCTIONS POSSIBLE BY THE RX01 CONTROLLER

/DO INSTRUCTIONS

```

0002 SET=2
0000 CLR=0
0002 ONE=2
0000 ZERO=0
0000
0004 I000=0
0004 I001=4
0010 I002=10
0014 I003=14
0020 I004=20
0024 I005=24
0030 I006=30
0000
0002 INTERF=CLR I000
0002 DISK=SET I000
0004
0010 ERR=I001
0010 XREQ=I002
0014 I00T=I003
0020 DONE=I004
0024 SHIFT=I005
0030 SECDAT=I006
0004
0010 WGate=I001
0012 STPHD=I002
0014 HDOUT=I003
0020 EGATE=I004
0024 L3MCUP=I005
0030
0034 UNIT=34
0040
0040 UNHD=40
0042 L0HD=42
0044
0044 BAP=44
0001 LONG=1
0000 SHORT=0
0002 INCR=2

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/INTERFACE-DISK BUSS OUTPUT BUFFER

/I000 SELECTS EITHER INTERFACE OR DISK BUSS. CLR= INTERFACE /SET=DISK

/INTERFACE BUFFER DEFINITIONS /SET TO INDICATE THAT AN RX01 ERROR HAS OCCURED /SET TO REQUEST AN RX01 WORD TRANSFER /DIRECTION FOR DATA LINE. SET=TO INTERFACE /SET TO INDICATE RX01 READINESS TO ACCEPT A COMMAND /SHIFT FOR DATA LINE /SELECTS SOURCE FOR DATA OUT OF CONTROLLER ON DATA LINE /SET=SECTOR BUFFER CLR=SHIFT REGISTER MOST SIG BIT

/DISK BUFFER DEFINITIONS /WRITE CURRENT ENABLE WHEN SET /HEAD STEP. TWO PULSES REQUIRED FOR EACH TRACK /DIRECTION OF HEAD MOTION /ERASE CURRENT FNABLE /SPECIFIES WRITE CURRENT LEVEL

/SELECTS ONE OF TWO DRIVES. UNIT (ZERO)(ONE)

/DEACTIVATES HEAD LOAD SOLENOID OF SELECTED DRIVE /ACTIVATES HEAD LOAD SOLENOID OF SELECTED DRIVE

/SECTOR BUFFER ADDRESS REGISTER CONTROL /FORMAT: CLR BAR (SHORT)(LONG) /SHORT PRESETS FOR COUNT OF 1024 /LONG PRESETS FOR COUNT OF 4096 /FORMAT: INCR BAR INCREMENT THE BUFFER ADDRESS REG.

/RX01 FLOPPY CONTROLLER FIRMWARE

```

0050 ARTBUF=50
0003 START=3
0000 FIN=0
0054 CRC=54
0057 PRECRC=57
0055 DATCRC=55
0060
0060 FLAG=60
0002 ON=2
0001 OFF=1
0003 TOG=3
0064 LSP=64
0070
0070 LCT=70
0071 ESP=71
0073 ICT=73
0074
0074 ROTATE=74
0075
0075 LSH=75
0077 DATSR=77

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/SECTOR BUFFER WRITE CLOCK /FORMAT: (STPAT)(FIN) WRIBUF /A 750NS MINIMUM PULSE IS REQUIRED

/CRC REGISTER CONTROL /FORMAT: CRC (ONE)(ZERO) SPECIFIES DATA TO /BE JAMMED INTO CRC GENERATOR/CHECKER /PRESETS CRC REG TO ALL ONES /SHIFTS SEPERATED DATA INTO CRC CIRCUIT

/GENERAL PURPOSE FLAG CONTROL /FORMAT: FLAG (ON)(OFF)(TOG) /SET FLAG /CLR FLAG /TOGGLE FLAG

/LOAD OPEN SCRATCHPAD REG WITH CONTENTS OF SHIFT REG /LOAD COUNTER WITH CONTENTS OF NEXT ROM LOCATION /LOAD COUNTER WITH CONTENTS OF OPEN SCRATCHPAD /INCREMENT COUNTER

/SHIFT REGISTER CONTROL /FORMAT: ROTATE(ONE)(ZERO) /SHIFTS SHIFT REG TOWARDS MOST SIGNIFICANT BIT /WHILE INSERTING A ONE OR ZERO INTO THE LEAST /SIGNIFICANT BIT /LOAD SHIFT REGISTER WITH CONTENTS OF COUNTER /SHIFT REG TOWARDS MSB WHILE INSERTING SEPERATED /DATA INTO LSR


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1RX01 FLOPPY CONTROLLER FIRMWARE PAL10 V142A 9-FEB-74 9:17 PAGE 3
/BRANCH INSTRUCTIONS AND CONDITIONS
/FORMAT: BR COND (T)(F)(ONE)(ZERO)
/IF CONDITION IS MET, A BRANCH IS MADE WITHIN
/THE CURRENT FIFD USING THE CONTENTS OF THE
/NEXT ROM LOCATION AS THE BRANCH ADDRESS
/IF THE CONDITION IS NOT MET, THE NEXT ROM LOCATION
/IS IGNORED AND THE FOLLOWING INSTRUCTION IS EXECUTED
/FORMAT: MBR COND (T)(ONE)
/THE COUNTER IS INCREMENTED WITH EVERY EXECUTION OF
/THIS INSTRUCTION. THE MBR IS REPEATEDLY
/EXECUTED UNTILL EITHER THE COUNTER OVERFLOWS OR
/THE CONDITION IS MET. IF THE CONDITION IS MET
/THE BRANCH IS MADE. IF THE COUNTER OVERFLOWS
/IS EXECUTED
/REQUIRES THE CONDITION TO BE FALSE
/REQUIRES THE CONDITION TO BE TRUE
/IF APPENDED TO THE JUMP, BR OR MBR INSTRUCTION,
/CAUSES THE BRANCH ADDRESS TO BE TAKEN FROM THE
/OPEN SCRATCHPAD RATHER THAN FROM THE NEXT ROM LOCATION
/WHEN ASSERTED INDICATES THAT THE INTERFACE HAS
/SERVICED A TRANSFER REQUEST, OR THAT A COMMAND
/IS PENDING
/INTERF/DISK OUTPUT BUFFER BIT 3
/BIDIRECTIONAL DATA LINE BETWEEN INTERFACE AND CONTROLLER
/DRIVE INDEX LATCH
/SHIFT REGISTER MOST SIGNIFICANT BIT
/OVERFLOW (ALL ONES) OF THE COUNTER
/BIT 16 OF CRC GENERATOR/CHECKER
/TRACK ZERO OF SELECTED DRIVE ANDED WITH HEAD
/DIRECTION BEING OUT
/WRITE ENABLED STATUS OF THE SELECTED DRIVE
/SEPERATED CLOCK FROM DISK DATA
/ASSERTED IF INTERFACE TRANSFERS ARE TO BE AS
/12 BIT WORDS RATHER THAN 8 BIT BYTES
/SEPERATED DATA EQUAL TO SHIFT REG BIT 7
/OVERFLOW CONDITION (ALL ONES) OF THE SECTOR BUFFER
/ADDRESS REGISTER
/MISSING CLOCK EQUAL TO SHIFT REG BIT 7
/OUTPUT OF SECTOR BUFFER
/STATE OF GENERAL PURPOSE FLAG
/SCRATCHPAD REGISTER SELECTION
/OPERAND
R0=4
R1=4
R2=10
R3=14
R4=20
R5=24
R6=30
R7=34
R8=40
R9=44
R10=52
R11=54
R12=60
R13=64
R14=74
R15=74
CURTK=0
CURTK=1
ERRREG=2
START=3
TART=4
TANSEC=5
TEMP=6
TEMP=7
TEMP=8
TEMP=9
TEMP=10
TEMP=11
TEMP=12
RTN=13
RTN=14
RTN=15
/DEFINITIONS OF SCRATCHPADS BY #
/DEFINITION OF SCRATCHPADS BY PNEUMONICS
/CURRENT TRACK ADDRESS OF DRIVE 0
/CURRENT TRACK ADDRESS OF DRIVE 1
/DEFINITIVE ERROR CODE IF ANY
/STATUS WORD OF RX01
/TARGET TRACK OF CURRENT DISK ACCESS
/TEMPORARY STORAGE
/TEMPORARY STORAGE
/TEMPORARY STORAGE
/BIT 7 IS UNIT SELECT BIT. 0 MEANS UNIT 1
/BIT 7 IS HEAD LOADED BIT. 1 MEANS HEAD LOADED
/TEMPORARY STORAGE
/TEMPORARY STORAGE
/RETURN ADDRESS FOR 3RD LEVEL NESTED SUBROUTINES
/RETURN ADDRESS FOR 2ND LEVEL NESTED SUBROUTINES
/RETURN ADDRESS FOR 1ST LEVEL SUBROUTINES

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175 /JUMP INSTRUCTION AND JUMP FIELD DEFINITIONS
 176 /JUMP#222
 177 /FORMAT: JUMP FX (IND)
 178 /CAUSES A BRANCH TO ONE OF SIX ROM FIELDS (0-5)
 179 /SPECIFIED BY X. THE BRANCH ADDRESS IS TAKEN FROM
 180 /THE ROM LOCATION FOLLOWING THE JUMP INSTRUCTION.
 181 /IF IND IS APPENDED, THE BRANCH ADDRESS
 182 /IS TAKEN FROM THE OPEN SCRATCH PAD

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TABLE OF DEFINITIVE ERROR CODES

0214	KXGV=214	/DRIVE 0 FAILED TO SEE HOME ON INITIALIZE
0224	KXGV1=214	/DRIVE 1 FAILED TO SEE HOME ON INITIALIZE. DOES NOT CAUSE ERROR
0234	KARONG=30	/FOUND HOME WHEN STEPPING IN 10 TRACKS FOR INIT
0240	KENTRAB=40	/TRIED TO ACCESS A TRACK GREATER THAN 76
0254	KHOMEERR=50	/HOME WAS FOUND BEFORE DESIRED TRACK WAS REACHED
0260	KSELFERR=60	/SELF DIAGNOSTIC ERR
0274	KXPRDR=76	/DESIRED SECTOR COULD NOT BE FOUND AFTER LOOKING /AT 52 HEADERS
0102	KAPROT=102	/WRITE FUNCTION ATTEMPTED ON A WRITE PROTECTED DISK
0110	KTIMEPR=110	/MORE THAN 40 MICROSECONDS AND NO SEPCLOCK SEEN
0120	KXKPPAM=120	/A PREAMBLE COULD NOT BE FOUND
0130	KXKIDAM=130	/PREAMBLE FOUND BUT NO ID MARK FOUND WITHIN ALLOWABLE TIME
0140	KXKRCER=140	/CRC ERROR ON WHAT APPEARED TO BE A HEADER. ERROR IS NOT ASSERTED
0150	KXKSPER=150	/THE TRACK ADDRESS OF A GOOD HEADER DOES NOT COMPARE /WITH THE DESIRED TRACK
0160	KXSTRYS=160	/TOO MANY TRIES FOR AN IDAM
0170	KXODAM=170	/DATA AM NOT FOUND IN ALLOTTED TIME
0200	KDCRCER=200	/CRC ERROR ON READING THE SECTOR FROM THE DISK
0210	KPARER=210	/PARITY ERROR ON SOME WORD FROM THE INTERFACE

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/ (SUBROUTINE: FINDTRACK)
/ THIS SUBROUTINE IS USED TO LOCATE A SPECIFIED SECTOR. IT PICKS
/ UP THE TRACK AND SECTOR ADDRESS FROM THE INTERFACE. CHECKS THAT
/ THE TRACK ADDRESS IS LEGAL (NOT GREATER THAN 114 OCTAL.), MOVES THE
/ HEAD OF THE SELECTED DRIVE TO THE SPECIFIED TRACK, VERIFIES
/ TRACK POSITION, AND LOCATES THE CORRECT SECTOR. EXIT FROM
/ THIS SUBROUTINE OCCURS AT WRITE TURN ON TIME OF THE SELECTED
/ SECTOR. ENTRANCE IS MADE WITH THE RETURN ADDRESS IN THE COUNTER

FINCTR, LSR OPEN RTN /SAVE THE RETURN ADDRESS
LSP
LCT /CLEAR THE ERROR REGISTER
Y
LSR
OPEL ERREG
LSP
OPEN TEMPD /SOFT UNIT BIT TO SR
ESP
LSR
BR SR7 ONE /IF SR=1 DRIVE 0 IS CURRENTLY SELECTED
UZERO
BR FLAG0 ZERO /IF FLAG=0 DRIVE 1 IS DESIRED AND ALREADY SELECTED
USAME
UNIT ZERO /DRIVE 0 IS DESIRED AND DRIVE1 WAS SELECTED, SELECT 0
LCT
OCTAL
ZPO
DECIMAL
JUMP F0
UDIF /GO STORE SOFT UNIT BIT
BR FLAG1 ONE /IF FLAG=1 DRIVE 0 IS DESIRED AND ALREADY SELECTED
USAME
UNIT ONE /DRIVE 1 IS DESIRED BUT DRIVE1 IS SELECTED, SELECT DRIVE 1
LCT
" /SET UP SOFT UNIT SELECT BIT AS DRIVE 1
LSR
LSP /STORE SOFT UNIT SELECT BIT
ROTATE ZERO /CLK SOFT HD LOAD BIT BECAUSE UNITS CHANGED

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/HX01 FLOPPY CONTROLLER FIRMWARE PALIP V102A 9-FEB-74 9:17 PAGE 7-1

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OPEN TEMPE
LSP
USAME, LCT /CALL GETWORD SURROUTINE FOR THE SECTOR ADDRESS
PUTSEC
JUMP F4
GETPRD
PUTSEC, LCT /MAKE FIRST BIT OF COMPLIMENTED SECTOR ADDRESS A 1 REGARDLESS OF DATA
-7-1
ROTATE ONE
BR COFL T
+7
LCT
BR SR7 T
+5
POTATE ZERO
JUMP F0
+7
OPEN TARSEC /PUT THE TARGET SECTOR AWAY
LSP
LCT
PUTTRK /CALL GETWORD SURROUTINE FOR TRACK ADDRESS
JUMP F4
GETPRD
PUTTRK, OPEN TARTRK /STASH THE TRACK ADDRESS
LSP
OPEN TEMPF /START SETUP FOR COMPARING THE
LSP /TARGET TRACK AND TRACK 76
OPEN TEMPG /IF TARGET TRACK
LCT /GE 77
-77-1
LSR
LSP
LCT
ILTRK /CALL SUBR MACCOM TO SEE IF TARGET TRACK
ILTRK /IS GREATER THAN 114 OCTAL, 76 DECIMAL.
LSP
OPEN RTNA
LSP
JUMP F5
MACCOM
ILTRK, JUMP F0 /TARGET TRACK IS 77, ILLEGAL ADDRESS
ERTRK /GO, REPORT THE ERROR
JUMP F0 /TARGET TRACK IS GREATER THAN 77
ERTRK /GO, REPORT THE ERROR

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432	0212	0244	OPEN TEMPD	/TARGET TRACK IS OK, GET THE DRIVE
433	0213	0071	ESP	/SELECT FROM TEMPD
434	0214	0075	LSR	
435				
436	0215	0200	OPEN CURTK0	/PRESELECT UNIT 0
437				
438	0216	0002	DISK	/SELECT DISK #002
439				
440	0217	0122	BR SR7 ONE	/WHICH UNIT SELECTED? BIT7=0 MEANS UNIT ONE
441	0220	0222	.+2	/ZERO, SKIP UNIT 1 SETUP
442	0221	0204	OPEN CURTK1	
443				
444	0222	0071	ESP	/PASS SELECTED CURRENT TRACK TO MAGCOM SUBR
445	0223	0075	LSR	
446	0224	0200	OPEN TEMPG	
447	0225	0064	LSP	
448				
449	0226	0220	OPEN TARTRK	/PASS TARGET TRACK TO MAGCOM SUBROUTINE
450	0227	0071	ESP	
451	0230	0075	LSR	
452	0231	0254	OPEN TEMPF	
453	0232	0064	LSP	
454	0233	0070	LCT	/CALL SUBROUTINE MAGCOM TO SEE IF TARGET
455	0234	0246	TRKEQ	/IS SAME AS CURRENT TRACK, F=TARGET, G=CURRENT
456	0235	0075	LSR	
457	0236	0270	OPEN RTNA	
458	0237	0064	LSP	
459	0240	0226	JUMP F5	
460	0241	2400	MAGCOM	
461				
462				
463	0242	0070	ERTFK, LCT	
464	0243	0040	KERTRK	/TRIED TO ACCESS A TRACK GREATER THAN 76 DECIMAL
465	0244	0226	JUMP F5	
466	0245	2610	GOERDN	
467				
468				
469	0246	0202	TRKEQ, JUMP F0	/TARGET EQUALS THE CURRENT TRACK, NO
470	0247	0357	NOSTPS	/STEPS ARE REQUIRED
471	0250	0270	OPEN RTNA	/NOOP; TARGET > ACTUAL RETURN
472	0251	0270	OPEN RTNA	/NOOP
473				
474	0252	0270	BOOT, OPEN RTNA	/TARGET IS LESS THAN ACTUAL, STEPS NEEDED ALSO START OF
475	0253	0070	LCT	/OF BOOT SUBROUTINE, SET UP RETURN FROM DIF SUBR
476	0254	0275	STPOUT	
477	0255	0075	LSR	
478	0256	0064	LSP	
479				
480	0257	0244	OPEN TEMPD	/SOFT UNIT SELECT BIT TO SR7
481	0260	0071	ESP	
482	0261	0075	LSR	
483				
484	0262	0204	OPEN CURTK1	/PRESELECT UNIT 1
485				
486	0263	0120	BR SR7 ZERO	/SR7=0 MEANS UNIT ONE

487	0264	0266	.+2	
488	0265	0200	OPEN CURTK0	
489				
490	0266	0071	ESP	/PASS SELECTED CURRENT TRACK TO DIF SUBR VIA SR
491	0267	0075	LSR	
492				
493	0270	0220	OPEN TARTRK	/PASS TARGET TRACK TO DIF VIA CNTR
494	0271	0071	ESP	
495				
496	0272	0016	SET HDOUT	/ASSUME A STEP OUT
497				
498	0273	0220	JUMP F5	/GO TO THE SUBROUTINE DIF TO CALCULATE THE STEPS NEEDED
499	0274	2462	DIF	
500				
501				
502	0275	0202	STPOUT, JUMP F0	/TARGET TRACK IS LESS THAN
503	0276	0300	.+2	/THE ACTUAL, MOVE OUT IS NECESSARY
504				
505	0277	0014	CLR HDOUT	/TARGET IS GREATER THAN ACTUAL, STEPS IN NEEDED
506				
507	0300	0070	LCT	/COMPLEMENT OF STEPS REQUIRED IS IN THE
508	0301	0305	DUNSTP	/SHIFT REG, SET UP RETURN FROM STPHD SUBR
509				
510	0302	0040	UNHD	/UNLOAD HEAD BEFORE MOVING
511				
512	0303	0222	JUMP F4	/CALL SUBROUTINE STPHD
513	0304	2100	STPHD	
514				
515				
516	0305	0220	DUNSTP, JUMP F5	/HOME FOUND BEFORE LAST STEP TAKEN
517	0306	2456	HDERR	
518				
519	0307	0244	OPEN TEMPD	/SOFT UNIT BIT TO SR7
520	0310	0071	ESP	
521	0311	0075	LSR	
522	0312	0220	OPEN TARTRK	/GET READY TO PASS TARGET TRK TO PROPER
523	0313	0071	ESP	/CURRENT TRACK
524				
525	0314	0200	OPEN CURTK0	/OPEN PROPER CURRENT TRACK REGISTER
526	0315	0122	BR SR7 ONE	/BIT7=0 MEANS UNIT ONE
527	0316	0320	.+2	
528	0317	0204	OPEN CURTK1	
529				
530	0320	0075	LSR	/UPDATE THE CURRENT TRACK ADDRESS
531	0321	0064	LSP	
532				
533				
534	0322	0220	HDSETL, OPEN TARTRK	/HEAD IS SETTLED DETERMINE IF ABOVE TRACK 43 DECIMAL
535	0323	0071	ESP	/PASS TARGET TO MAGCOM VIA TEMPF
536	0324	0075	LSR	
537	0325	0254	OPEN TEMPF	
538	0326	0064	LSP	
539				
540	0327	0070	LCT	/PASS 44 TO MAGCOM VIA TEMPG
541	0336	0323	-44-1	

542	0331	0075	LSR	
543	0332	0260	OPEN TEMPG	
544	0333	0064	LSP	
545				
546	0334	0026	SET LOWCUR	/ASSUME TARGET GREATER THAN 43
547				
548	0335	0070	LCT	/CALL MAGCOM SUBROUTINE
549	0336	0344	ABV43	/RETURN ADDRESS
550	0337	0075	LSR	
551	0340	0270	OPEN RTNA	
552	0341	0064	LSP	
553	0342	0226	JUMP F5	
554	0343	2400	MAGCOM	
555				
556				
557	0344	0202	ABV43, JUMP F0	/NOOP F=6 RETURN, ABOVE TRK 43
558	0345	0346	.+1	/NOOP
559				
560	0346	0202	JUMP F0	/F<G; ABOVE TRACK 43
561	0347	0351	.+2	
562				
563	0350	0024	CLR LOWCUR	/F>G; BELOW TRACK 43, WRITE WITH HIGH CURRENT
564				
565	0351	0070	CFINSE, LCT	/CALL FINDSEC SUBROUTINE TO LOCATE THE DESIRED SECTOR
566	0352	0355	RFINTR	
567	0353	0206	JUMP F1	
568	0354	0714	FINDSE	
569				
570	0355	0274	RFINTR, OPEN RTN	/RETURN FROM FINDTR SUBROUTINE
571	0356	0207	JUMP F1 IND	
572				
573				
574	0357	0250	HOSTPS, OPEN TEMPE	/NO STEPS REQUIRED
575	0360	0071	ESP	/SOFT HEAD LOAD BIT TO SR7
576	0361	0075	LSR	
577				
578	0362	0122	BR SR7 ONE	/IS HEAD LOADED?
579	0363	0322	HDSETL	/YES, GO UPDATE CURRENT CONTROL
580				
581	0364	0070	LCT	/NO, GO LOAD HEAD AND WAIT FOR 20MS SETTLE TIME
582	0365	0322	HDSETL	/RETURN ADDR FROM DLY25 SUBROUTINE
583	0366	0222	JUMP F4	
584	0367	2145	DLY25	
585				
586				
587	0370	0212	PFUNCT, JUMP F2	/POINTER FROM GETWORD SUBROUTINE TO
588	0371	1236	FUNCT	/FUNCTION DEC'DF
589				
590	0372	0226	PD:RCL, JUMP F5	/POINTER TO DRV ⁿ CHECK DONE AFTER RECALABPATE
591	0373	2625	DRCAL	
592				
593	0374	0000	0	/SPARE LOCATIONS
594	0375	0000	0	/OPEN
595	0376	0000	0	/OPEN
596	0377	0000	0	/OPEN

597				/(ROUTINE: WRITE SECTOR)
598				/THIS ROUTINE TURNS ON WRITE GATE AT WRITE TURN ON TIME,
599				/WRITES A PREFRAME OF 6 BYTES OF ZEROS, A DATA OR DELETED DATA MARK,
600				/THEN TURNS ON ERASE GATE. ENTER WITH CNTN=100 IF
601				/DELETED DATA, CNTN=0 IF NORMAL DATA MARK. THE DATA MARK, DATA FIELD, CRC
602				/AND ONE BYTE POSTHOLE ARE WRITTEN. WRITE CURRENT IS TURNED OFF.
603				/511 MICRO SECONDS LATER ERASE CURRENT IS TURNED OFF. A HEADER MUST
604				/THE BE HEAD TO INSURE DISK IS STILL UP TO SPEED BEFORE THE WRITE
605				/SECTOR FUNCTION IS COMPLETE.
606				
607				
608				
609				
610	0400	0214	WRTSEC, OPEN STAT	/DEL DATA BIT TO STAT6
611	0401	0075	LSR	
612	0402	0064	LSP	
613				
614	0403	0070	LCT	/CALL SUBROUTINE TO FIND DESIRED TRACK AND SECTOR
615	0404	0007	S-GATE	
616	0405	0202	JUMP F0	
617	0406	0103	FINDTR	
618				
619	0407	0061	S-GATE, FLAG OFF	/ALWAYS START WRITING WITH WRITE FLOP CLEARED
620				
621	0410	0140	RP WRTEN F	/GO REPORT ERROR IF NO WRITE ENABLE
622	0411	0503	PRERR	
623				
624	0412	0214	OPEN STAT	/DEL DATA BIT TO SR7 AND ENABLE WRT CURRENT
625	0413	0071	ESP	
626	0414	0000	SET WGATE	
627	0415	0075	LSR	
628	0416	0074	ROTATE ZERO	
629				
630	0417	0234	OPEN TEMPG	/USE TEMPG FOR SECOND HALF DATA AN PATTERN
631				
632	0420	0057	PRECRC	/JAM THE CRC GENERATOR WITH FIRST 6 BITS OF DATA AN
633	0421	0056	CRC ONE	
634	0422	0056	CRC ONE	
635	0423	0056	CRC ONE	
636	0424	0056	CRC ONE	
637	0425	0056	CRC ONE	
638	0426	0054	CRC ZERO	
639				
640	0427	0120	BR SR7 ZERO	/DELETED DATA?
641	0430	0460	DANSUP	/NO, REGULAR DATA MARK
642				
643	0431	0070	LCT	/YES, SECOND HALF OF DELETED DATA MARK TO CNTR
644			OCTAL	
645	0432	0325	325	/FLUX PATTERN
646			DECIMAL	
647				
648	0433	0054	CRC ZERO	/JAM LAST 2 BITS OF DELETED DATA MARK TO CRC GEN.
649	0434	0054	CRC ZERO	
650	0435	0002	DISK	/NOOP
651	0436	0002	DISK	/NOOP

```

652
653 0437 0063 STASH, TOG FLAG /END OF THE FIRST 0 BIT
654
655 0440 0075 LSR /PUT SECOND HALF OF THE DESIRED MARK IN THE TEMPB
656 0441 0064 LSP
657
658 0442 0070 LCT /SET UP RETURN FROM WRITE ZEROS SUBROUTINE
659 0443 0466 HLFCLY
660 0444 0075 LSR
661
662 0445 0070 LCT /STALL 1.0 MICRO SECONDS
663 0446 0374 -3-1
664 0447 0073 ICT
665 0450 0124 BR COFL F
666 0451 0447 ,=2
667 0452 0002 DISK /NOOP
668
669 0453 0070 LCT /SPECIFY 22 ZFRMS TO BE WRITTEN BY WRT0S SUBROUTINE
670 0454 0351 -22-1
671
672 0455 0063 TOG FLAG /WRITE SECOND CLOCK TRANSITION
673
674 0456 0212 JUMP F2 /CALL WRITE ZEROS SUBROUTINE
675 0457 1322 WRT0S
676
677 0460 0070 DAMSUP, LCT /LOAD SECOND HALF OF NORMAL DATA MARK
678 OCTAL
679 0461 0337 337
680 DECIMAL
681
682 0462 0056 CRC ONE /JAM LAST 2 BITS OF DATA MARK TO CRC GENERATOR
683 0463 0056 CRC ONE
684
685 0464 0206 JUMP F1 /GO PUT AWAY THE SECOND HALF OF THE DATA MARK
686 0465 0437 STASH
687
688 0466 0002 HLFCLY, DISK /NOOP
689
690 0467 0070 LCT /SET UP RETURN FROM WRITE ZEROS SUBROUTINE
691 0470 0514 WRTDAM
692 0471 0075 LSR
693
694 0472 0070 LCT /NOOP WASTE .P MICRO SECONDS
695 0473 0351 -22-1 /NOOP
696 0474 0070 LCT /NOOP
697 0475 0351 -22-1 /NOOP
698
699 0476 0070 LCT /SPECIFY 22 BITS TO BE WRITTEN BY WRT0S SUBROUTINE
700 0477 0351 -22-1
701
702 0500 0063 TOG FLAG /WRITE THE 25TH CLOCK TRANSITION
703
704 0521 0212 JUMP F2 /CALL WRT0S SUBROUTINE
705 0502 1322 WRT0S
706

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```

707 0503 0270 PRTRRN, LCT /SET WRITE PROTECT BIT OF STAT BECAUSE A WRITE FUNCTION WAS ATTEMPTED ON
708 /ON A WRITE PROTECTED DISKETTE
709
710 0504 0010 OCTAL
711 10 DECIMAL
712 0505 0075 LSR
713 0506 0214 OPEN STAT
714 0507 0064 LSP
715
716 0510 0070 LCT /ERROR CODE FOR WRT PROTECT ERROR
717 0511 0100 KWRPOT
718 0512 0226 JUMP F5
719 0513 0610 GOERDM
720
721
722
723 /THIS ROUTINE WILL WRITE EITHER A DATA MARK OR A
724 /DELETED DATA MARK. THE FIRST HALF OF BOTH MARKS ARE
725 /IDENTICAL. THE SECOND HALF IS SPECIFIED BEFORE ENTRY BY
726 /PUTTING THE SECOND HALF BIT PATTERN IN TEMPB
727
728
729 0514 0070 WRTDAM, LCT /WASTE 2.0 MICRO SECONDS
730 0515 0375 -2-1
731 0516 0073 ICT
732 0517 0075 LSR
733 0520 0124 BR COFL F
734 0521 0516 ,=3
735
736 0522 0063 TOG FLAG /WRITE A CLOCK BIT AS END OF 48TH ZERO
737
738 0523 0070 LCT /FIRST HALF OF DATA MARK PATTERN TO SR
739 OCTAL
740 0524 0352 352
741 DECIMAL
742 0525 0075 LSR
743
744 0526 0070 LCT /SET TRANSITION LOOP COUNTER FOR 8 LOOPS
745 0527 0370 -7-1
746 0530 0002 DISK /NOOP
747
748 0531 0120 AGAIN, BR SR7 ZERO /WHATS THE BIT?
749 0532 0562 A /ZERO, NO TRANSITION
750
751 0533 0044 CLR BAR /ONE, RESET THE BUFFER ADDR REG TO 0
752
753 0534 0063 TOG FLAG /WRITE FLUX TRANSITION
754
755 0535 0126 ABACK, BR COFL T /CHECK TRANSITION LOOP COUNT
756 0536 0543 SECHLF /GO GET SECOND HALF
757
758 0537 0074 ROTATE /SHIFT NEXT TRANSITION TO SR7
759
760 0540 0073 ICT /BUMP TRANSITION LOOP COUNTER
761

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762 0541 0206 JUMP F1 /DO ANOTHER LOOP
763 0542 0531 AGAIN
764
765 0543 0234 SECHLF, OPEN TEMPB /SECOND HALF OF DATA MARK TO SR
766 0544 0071 ESP
767 0545 0075 LSR
768
769 0546 0070 LCT /SET TRANSITION LOOP COUNTER FOR 8 LOOPS
770 0547 0370 -7-1
771
772
773 0550 0120 AGAIN1, BR SR7 ZERO /SHALL WE WRITE A TRANSITION?
774 0551 0564 B /NO
775
776 0552 0263 TOG FLAG /YES
777 0553 0002 DISK /NOOP
778
779 0554 0126 BBACK, BR COFL T /DONE DATA MARK?
780 0555 0566 WRTDAT /YES, GO WRITE DATA
781
782 0556 0073 ICT /NO, BUMP THE LOOP COUNTER
783
784 0557 0074 ROTATE /BRING UP NEXT HALF BIT TO SR7
785
786 0560 0206 JUMP F1 /DO ANOTHER LOOP
787 0561 0550 AGAIN1
788
789 0562 0206 A, JUMP F1 /WASTE 2 CYCLES TO SKIP FLUX TRANSITION
790 0563 0535 ABACK
791
792 0564 0206 B, JUMP F1 /WASTE 2 CYCLES TO SKIP FLUX TRANSITION
793 0565 0554 BBACK
794
795
796
797
798 /THIS ROUTINE WRITES THE CONTENTS OF THE SECTOR BUFFER.
799
800
801 0566 0022 WRTDAT, SET EGATE /TURN ON ERASE CURRENT AT START OF DATA FIELD
802 0567 0073 ICT /NOOP, WASTE 2 CYCLES
803 0570 0073 ICT /NOOP
804
805 0571 0170 DATA, BR WRTDAT ZERO /WHAT'S THE DATA BIT?
806 0572 0615 C /ZERO, GO WRITE NOTHING
807
808 0573 0056 CRC ONE /ONE, UPDATE THE CRC WITH 1
809
810 0574 0063 TOG FLAG /WRITE A DATA TRANSITION
811 0575 0073 ICT /NOOP FOR BIT CELL TIMING
812
813 0576 0162 CBACK, BR BAROFL T /DONE ENTIRE SECTOR?
814 0577 0624 WRTCRC /YES, GO WRITE THE CRC
815
816 0600 0046 INCR BAR /NO, BRING UP NEXT DATA BIT FROM SEC BUFFER

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817
818 0601 0070 LCT /NOOP - WASTE 5 CYCLES WITH
819 0602 0376 -2 /NOOP - A SELF TEST OF THE COUNTER
820 0603 0073 ICT /NOOP
821 0604 0124 BR COFL F /NOOP
822 0605 0624 SELFER /NOOP
823
824 0606 0063 TOG FLAG /WRITE A CLOCK TRANSITION
825
826 0607 0070 LCT /NOOP - WASTE 4 CYCLES WITH
827 0610 0377 -1 /NOOP - A SELF TEST OF THE COUNTER
828 0611 0124 BR COFL F /NOOP
829 0612 0624 SELFER /NOOP
830
831 0613 0206 JUMP F1 /GO WRITE ANOTHER DATA BIT
832 0614 0571 DATA
833
834 0615 0054 C, CRC ZERO /UPDATE CRC WITH 0 AND SKIP DATA TRANSITION
835 0616 0206 JUMP F1
836 0617 0576 CBACK
837
838
839 0620 0070 SELFER, LCT /A SELF DIAGNOSTIC HAS FAILED
840 0621 0060 WSELFER
841 0622 0226 JUMP F5
842 0623 0610 GOERDN
843
844
845 /THIS ROUTINE WRITES THE 16 BIT CRC GENERATED FOR THE
846 /PRECEDING DATA FIELD.
847
848
849 0624 0070 WRTCRC, LCT /PRESET BIT COUNTER FOR 16 BITS
850 0625 0357 -16-1
851
852 0626 0075 LSR /NOOP WASTE 4 CYCLES AND SELF TEST THE SR
853 0627 0022 DISK /NOOP
854 0630 0120 BR SR7 ZERO /NOOP
855 0631 0620 SELFER /NOOP
856
857 0632 0063 TOG FLAG /WRITE A CLOCK TRANSITION
858
859 0633 0076 ROTATE ONE /NOOP WASTE 6 CYCLES WITH MORE SELFTST
860 0634 0076 ROTATE ONE /NOOP
861 0635 0076 ROTATE ONE /NOOP
862 0636 0076 ROTATE ONE /NOOP
863 0637 0120 BR SR7 ZERO /NOOP
864 0640 0620 SELFER /NOOP
865
866 0641 0130 BR CRC16 ZERO /WHAT IS THE CRC BIT
867 0642 0653 C /ZERO, DO NOT WRITE ANYTHING
868
869 0643 0056 CRC ONE /ONE, BRING UP THE NEXT BIT
870
871 0644 0063 TOG FLAG /WRITE A DATA TRANSITION

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872 0645 0076          ROTATE ONE /NOOP
873
874 0646 0273  DBACK, ICT /BUMP THE BIT COUNTER
875
876 0647 0126          BR COFL T /COME CRC YET?
877 0650 0656          WRTPST /YES, GO WRITE A POSTAMBLE
878
879 0651 0206          JUMP F1 /NO, GO WRITE ANOTHER CRC BIT
880 0652 0627          E
881
882 0653 0054  D,      CRC ZERO /BRING UP NEXT CRC BIT AND SKIP DATA TRANSITION
883 0654 0206          JUMP F1
884 0655 0646          DBACK
885
886
887 /THIS ROUTINE WRITES THE ONE BYTE POSTAMBLE, TURNS OFF
888 /WRITE CURRENT, DELAYS 511 MICRO SEC AND TURNS OFF ERASE
889 /CURRENT. IT UTILIZES THE WRITE ZEROES SUBROUTINE.
890
891
892
893 0656 0270  WRTPST, LCT /SETUP TO CALL WRT0S TO WRITE 8 BITS OF ZEROES
894 0657 0666          CWGATE
895 0660 0275          LSR
896 0661 0270          LCT
897 0662 0367          -8-1
898
899 0663 0263          TOG FLAG /WRITE LAST CLOCK TRANSITION OF THE CRC FIELD
900
901 0664 0212          JUMP F2 /CALL THE SUBROUTINE WRITE ZEROES
902 0665 1322          WRT0S
903
904
905 0666 0204  CWGATE, CLR WGATE /DISABLE WRITE CURRENT
906
907 0667 0270          LCT /CALL WRT0S FOR 127 BITS (511.2 MICRO SEC)
908 0670 0676          CEGATE /DELAY TO ERASE TURN OFF
909 0671 0275          LSR
910 0672 0270          LCT
911 0673 0200          -127-1
912 0674 0212          JUMP F2
913 0675 1322          WRT0S
914
915
916 0676 0220  CEGATE, CLR EGATE /DISABLE ERASE CURRENT
917
918 0677 0270          LCT /CALL WRT0S FOR 25 BIT (101 MICRO SEC) DELAY
919 0702 0706          READOK /BEFORE TRYING TO READ
920 0701 0275          LSR
921 0702 0270          LCT
922 0703 0346          -25-1
923 0704 0212          JUMP F2
924 0705 1322          WRT0S
925
926 0706 0270  READOK, LCT /CALL FIND HEADER ROUTINE TO INSURE

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927 0707 0712          GODONE /THAT THE DISK IS STILL MOVING
928 0710 0216          JUMP F3
929 0711 1400          FINDHD
930
931 0712 0212  GODONE, JUMP F2 /WRITE SECTOR FUNCTION IS COMPLETE
932 0713 1400          OKDONE
933
934
935 /SUBROUTINE: FINDSECTOR)
936 /SUBROUTINE TO FIND A SPECIFIC SECTOR. ENTER WITH RETURN ADDRESS
937 /IN CNTR, DESIRED TRACK ADDRESS IN TARTRK AND DESIRED SECTOR ADDRESS
938 /IN TARSEC. THIS SUBROUTINE ASSUMES THAT THE TARGET TRACK HAS ALREADY
939 /BEEN REACHED.
940
941
942 0714 0270  FINDSE, OPEN RTNA /SAVE RETURN ADDRESS
943 0715 0275          LSR
944 0716 0264          LSP
945
946 0717 0260          OPEN TEMPG /PRESET SECTOR TRY COUNT TO 52 TRIES
947 0720 0270          LCT
948 0721 0313          -52-1
949
950 0722 0275  AGAIN2, LSP /STORE SECTOR TRY COUNT
951 0723 0264          LSP
952
953 0724 0270          LCT /CALL SUBROUTINE TO FIND A HEADER
954 0725 0270          CHKSEC
955 0726 0216          JUMP F3
956 0727 1400          FINDHD
957
958 0730 0174  CHKSEC, BR FLAG0 ZERO /CORRECT SECTOR FLAG=1 IF NO
959 0731 0743          WAIT /YES, GO WAIT FOR PREAMBLE
960
961 0732 0260          OPEN TEMPG /NO, RECALL SECTOR TRY COUNT AND INCREMENT IT
962 0733 0271          ESP
963 0734 0273          ICT
964
965 0735 0124          BR COFL F /52 TRIES MADE FOR SECTOR YET?
966 0736 0722          AGAIN2 /NO, TRY ANOTHER SECTOR
967
968 0737 0270  *XHDR, LCT /YES, CANN'T FIND THE SECTOR
969 0740 0270          KNXHDR
970 0741 0226          JUMP F5
971 0742 0610          GOERDN
972
973 0743 0270  WAIT, LCT /STALL 323.2 MICRO SECONDS TO WAIT FOR DATA PREAMBLE
974 0744 0345          -26-1
975 0745 0273          ICT
976 0746 0124          BR COFL F
977 0747 0745          -2
978 0750 0273          ICT
979 0751 0124          BR COFL F
980 0752 0750          -2
981 0753 0273          ICT

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982 0754 0124 BR COFL F
983 0755 0753 .-2
984
985 0756 0270 OPEN RTNA /RETURN FROM TMS SUBROUTINE AT WRITE TURN ON TIME
986 0757 0203 JUMP F0 IND /OF THE DESIRED SECTOR
987
988
989
990 /ROUTINE: READ SECTOR]
991
992 0760 0074 R0SEC, ROTATE ZERO /ZERO THE STAT
993 0761 0074 ROTATE ZERO
994 0762 0214 OPEN STAT
995 0763 0064 LSP
996
997 0764 0070 LCT /CALL THE FIND TRACK SUBROUTINE TO LOCATE DESIRED SECTOR
998 0765 0770 GOREAD
999 0766 0202 JUMP F0
1000 0767 0103 FINDTR
1001
1002 0770 0222 GOREAD, JUMP F4 /GO READ THE DATA FIELD
1003 0771 2167 READ
1004
1005
1006 0772 0000 0 /OPEN FREE LOCATIONS
1007 0773 0000 0 /OPEN
1008 0774 0000 0 /OPEN
1009 0775 0000 0 /OPEN
1010 0776 0000 0 /OPEN
1011 0777 0000 0 /OPEN

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1012 /ROUTINE: DONE AND ERROR DONE]
1013
1014
1015 1000 0220 ERDONE, CLR DONE
1016 1001 0010 CLR XREG
1017
1018 1002 0000 INTERF /SELECT INTERFACE BUSS
1019
1020 1003 0006 SET ERR /ASSERT ERROR LINE
1021
1022 1004 0012 JUMP F2 /SKIP NEXT INSTRUCTION
1023 1005 1007 .+2
1024
1025 1006 0004 ORDONE, CLR ERR /NEGATE ERROR LINE
1026
1027 1007 0214 OPEN STAT /OPEN STAT TO MOVE TO INTERFACE
1028
1029 1008 0071 ESP /STAT OR ERREG TO SR
1030 1009 0075 LSR
1031
1032 1012 0024 CLR SHIFT /CLEAR INTERFACE OUTPUT BUFFER
1033 1013 0020 CLR DONE
1034 1014 0010 CLR XREG
1035
1036 1015 0000 INTERF /SELECT INTERFACE OUTPUT BUSS
1037
1038 1016 0030 CLR SECDAT /SELECT SR AS DATA LINE SOURCE
1039
1040 1017 0016 SET IOOUT /DEFINE DATA DIRECTION AS OUT (TO INTERFACE)
1041
1042 1020 0070 LCT /MOVE SR TO INTERFACE SERIALLY
1043 1021 0367 -8-1
1044 1022 0026 SET SHIFT
1045 1023 0024 CLR SHIFT
1046 1024 0073 ICT
1047 1025 0074 ROTATE ZERO
1048 1026 0124 BR COFL F
1049 1027 1022 .-5
1050
1051 1030 0014 CLR IOOUT /NEXT TRANSFER WILL BE FROM INTERFACE
1052
1053 1031 0022 STDONE, SET DONE /FUNCTION IS DONE
1054 1032 0070 LCT /CALL GET COMMAND SUBROUTINE TO GET NEXT FUNCTION
1055 1033 0370 PFUNCTION
1056 1034 0222 JUMP F4
1057 1035 2001 GETCMD
1058
1059 1036 0074 FUNCT, ROTATE /MOVE UNIT SELECT BIT TO SR7
1060 1037 0074 ROTATE
1061 1040 0074 ROTATE
1062 1041 0122 BR SR7 ONE /FLAG IS ALREADY SET. SAVE UNIT IN FLAG, ON=UNIT 0
1063 1042 1044 .+2
1064 1043 0061 FLAG OFF
1065
1066 1044 0074 ROTATE /GET FIRST FUNCTION BIT TO SR7

```

1067				
1068	1045	0120	BR SR7 ZERO	
1069	1046	1066	FUNCT4	/FUNCTION 4 OR GREATER
1070				
1071	1047	0074	ROTATE	/GET 2ND FUNCTION BIT
1072				
1073	1050	0120	BR SR7 ZERO	
1074	1051	1057	FUNCT2	/FUNCTION CODE IS 2 OR 3
1075				
1076				
1077	1052	0074	ROTATE	/GET LAST FUNCTION BIT
1078				
1079	1053	0120	BR SR7 ZERO	
1080	1054	1107	EMPTYBUF	/FUNCTION CODE 1
1081				
1082	1055	0212	JUMP F2	/FUNCTION CODE 4
1083	1056	1110	FILLBUF	
1084				
1085	1057	0074	FUNCT2, ROTATE	/GET LAST FUNCTION BIT
1086				
1087	1060	0120	BR SR7 ZERO	
1088	1061	1105	PROSEC	/FUNCTION CODE 3
1089				
1090	1062	0070	LCT	/CLR CNTR BITS TO INDICATE NORMAL DATA
1091	1063	0200	0	
1092	1064	0206	JUMP F1	/FUNCTION 2
1093	1065	0400	WRTSEC	
1094				
1095	1066	0074	FUNCT4, ROTATE	/GET 2ND FUNCTION BIT
1096				
1097	1067	0120	BR SR7 ZERO	
1098	1070	1276	FUNCT6	/FUNCTION CODE IS 6 OR GREATER
1099				
1100	1071	0074	ROTATE	/GET LAST FUNCTION BIT
1101				
1102	1072	0120	BR SR7 ZERO	
1103	1073	1224	RDSTAT	/FUNCTION 5
1104				
1105	1074	0212	JUMP F2	
1106	1075	1243	CLRID	/FUNCTION 4=UNUSED
1107				
1108	1076	0074	FUNCT6, ROTATE	/GET LAST FUNCTION BIT
1109				
1110	1077	0120	BR SR7 ZERO	
1111	1100	1275	RDEREG	/FUNCTION 7
1112				
1113	1101	0070	LCT	/SET CNTR6 TO INDICATE DELETED DATA
1114			OCTAL	
1115	1102	0100	100	
1116			DECIMAL	
1117	1103	0206	JUMP F1	
1118	1104	0400	WRTSEC	/FUNCTION 6
1119				
1120	1105	0206	PROSEC, JUMP F1	/POINTER TO READ SECTOR FUNCTION
1121	1106	0760	RDSEC	

1122				
1123				
1124				
1125				
1126				
1127				
1128				
1129				
1130				
1131				
1132	1127	0216	EMPTYBUF, SET IOOUT	/IOOUT IS CLEARED, SET IT TO INDICATE DATA IS MOVING TO THE INTERFACE
1133				
1134				
1135	1110	0074	FILLBUF, ROTATE ZERO	/CLEAR STAT
1136	1111	0074	ROTATE ZERO	
1137	1112	0214	OPEN STAT	
1138	1113	0064	LSP	
1139				
1140	1114	0210	OPEN ERREG	/CLEAR ERREG
1141	1115	0064	LSP	
1142				
1143	1116	0061	FLAG OFF	/NOOP
1144				
1145	1117	0044	CLR BAR SHORT	/ADDRESS THE 1ST BIT OF SECTOR BUFFER
1146				
1147	1120	0070	LCT	/SET UP BYTE COUNT TO 128 (8 BIT) OR 64 (12 BIT)
1148	1121	0177	-128-1	
1149	1122	0150	BR XIIIBIT F	
1150	1123	1126	.+3	
1151	1124	0070	LCT	
1152	1125	0277	-64-1	
1153	1126	0230	OPEN TEMPA	
1154				
1155	1127	0106	BR IOB30T T	/WHICH FUNCTION IS THIS?
1156	1130	1210	EMPTY1	/EMPTYBUF
1157				
1158	1131	0012	XFR0, SET XREQ	/REQUEST DATA TRANSFER
1159				
1160	1132	0073	ICT	/INCREMENT BYTE COUNT AND RESTORE
1161	1133	0075	LSR	
1162	1134	0064	LSP	
1163				
1164	1135	0070	LCT	/CALL WAITRUN SUBR TO WAIT FOR DATA TRANSFER
1165	1136	1141	NEWORD	
1166	1137	0222	JUMP F4	
1167	1140	0312	WAITPN	
1168				
1169	1141	0230	NEWORD, OPEN TEMPA	/REOPEN THE BYTE COUNT REGISTER BECAUSE WAITRUN CLOSED IT
1170	1142	0070	LCT	/SET UP BIT COUNT IN CNTR TO 8 BITS OR 12 BITS
1171	1143	0367	-8-1	
1172	1144	0150	BR XIIIBIT F	
1173	1145	1150	.+3	
1174	1146	0070	LCT	
1175	1147	0363	-12-1	
1176				

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1177 1150 0104 BR IOB30T F /WHICH FUNCTION IS THIS?
1178 1151 1175 FILL1 /FILLBUF
1179
1180
1181 1152 0026 BYTEOUT, SET SHIFT /EMPTYBUF, MOVE A BYTE FROM SECTOR BUFFER
1182 1153 0046 INCR BAR /TO INTERFACE SERIALY
1183 1154 0024 CLR SHIFT
1184 1155 0073 ICT
1185 1156 0124 BR COFL F
1186 1157 1152 BYTEOUT
1187
1188 1160 0071 ESP /CHECK BYTE COUNT
1189 1161 0124 BR COFL F
1190 1162 1131 XFRQ /NOT DONE, GO REQUEST A DATA TRANSFER
1191
1192 1163 0012 SET XREQ /DONE, REQUEST TRANSFER OF LAST BYTE
1193
1194 1164 0100 BR RUN F /WAIT FOR TRANSFER COMPLETION
1195 1165 1164 .-1
1196
1197 1166 0010 CLR XREQ
1198
1199 1167 0212 JUMP F2 /EMPTYBUF FUNCTION IS COMPLETE
1200 1170 1006 OKDONE
1201
1202 1171 0050 FIN WRTBUF /END SECTOR BUFR WRT PULSE (800 NS)
1203
1204 1172 0046 INCR BAR /ADDRESS NEXT CELL OF SECTOR BUFFER
1205
1206 1173 0026 SET SHIFT /SHIFT NEXT BIT FROM INTERFACE
1207 1174 0024 CLR SHIFT
1208
1209 1175 0053 FILL1, START WRTBUF /START SECTOR BUFR WRT PULSE
1210
1211 1176 0073 ICT /LAST BIT OF BYTE?
1212 1177 0124 BR COFL F
1213 1200 1171 .-7 /NO, DO ANOTHER BIT
1214
1215 1201 0050 FIN WRTBUF /LAST BIT, END SECTOR BUFR WRT PULSE
1216
1217 1202 0046 INCR BAR /ADDRESS NEXT CELL OF SECTOR BUFFER
1218
1219 1203 0071 ESP /CHECK BYTE COUNT
1220 1204 0124 BR COFL F
1221 1205 1131 XFRQ /NOT DONE, GO GET ANOTHER BYTE
1222
1223 1206 0212 JUMP F2 /DONE FILLBUF FUNCTION
1224 1207 1006 OKDONE
1225
1226 1210 0032 EMPTY1, SET SECCAT /SELECT SECTOR BUFR AS DATA LINE SOURCE
1227
1228 1211 0073 ICT /INCREMENT AND SAVE THE BYTE COUNT
1229 1212 0075 LSR
1230 1213 0064 LSP
1231

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```

1232 1214 0070 LCT /SET UP THE BIT COUNT TO 8 BITS OR 12 BITS
1233 1215 0307 -8-1
1234 1216 0150 BR KIIBIT F
1235 1217 1152 BYTEOUT
1236 1220 0070 LCT
1237 1221 0303 -12-1
1238
1239 1222 0212 JUMP F2 /GO MOVE A BYTE TO INTERFACE
1240 1223 1152 BYTEOUT
1241
1242
1243
1244 /([ROUTINE: READ STATUS])
1245
1246
1247 1224 0244 RDSTAT, OPEN TEMPD /SELECT THE SOFT UNIT SCRATCH PAD
1248
1249 1225 0036 UNIT ONE /PRESELECT UNIT ONE
1250 1226 0070 LCT
1251 1227 0000 2
1252
1253 1230 0174 BR FLAG0 ZERO /WHICH UNIT? FLAG=0=UNIT 1
1254 1231 1235 .+4 /UNIT 1, SKIP UNIT 0 SETUP
1255
1256 1232 0034 UNIT ZERO /SELECT UNIT ZERO
1257 1233 0070 LCT
1258 OCTAL
1259 1234 0200 200
1260 DECIMAL
1261
1262 1235 0075 LSR /STORE SOFT UNIT BIT
1263 1236 0064 LSP
1264
1265 1237 0070 LCT /CALL CHECKRDY SUBROUTINE, RETURN TO CLRID
1266 1240 1765 PTRDY
1267 1241 0226 JUMP F5
1268 1242 2640 CHKRDY
1269
1270
1271
1272 1243 0214 CLRID, OPEN STAT /CLEAR INIT DONE BIT OF STAT
1273 1244 0071 ESP /STATUS TO SHIFT REG
1274 1245 0075 LSR
1275
1276 1246 0061 FLAG OFF
1277 1247 0070 LCT /END AROUND SHIFT OF FIRST 5 BITS
1278 1250 0372 -5-1
1279 1251 0122 ROT, BR SR7 T
1280 1252 1256 .+4
1281 1253 0074 ROTATE ZERO
1282 1254 0212 JUMP F2
1283 1255 1257 .+2
1284 1256 0076 ROTATE ONE
1285 1257 0073 ICT
1286 1260 0124 BR COFL F

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1287 1261 1251      .-8
1288
1289 1262 0176      BR FLAG0 T      /IF FLAG IS SET THEN ROTATE IS DONE
1290 1263 1272      GODUN
1291
1292 1264 0062      FLAG ON      /IF NOT, CLEAR INIT DONE AND FINISH ROTATE
1293 1265 0074      ROTATE ZERO
1294 1266 0070      LCT
1295 1267 0375      -2-1
1296 1270 0212      JUMP F2
1297 1271 1251      ROT
1298
1299
1300 1272 0064      GODUN, LSP      /RESTORE STAT AND GO DONE
1301 1273 0212      JUMP F2
1302 1274 1006      OKDONE
1303
1304      /([ROUTINE: READ ERROR REGISTER])
1305
1306
1307
1308 1275 0210      RDEREG, OPEN ERREG
1309 1276 0212      JUMP F2
1310 1277 1010      OKDONE+2
1311
1312
1313      /([SUBROUTINE: DELAY], THIS SUBROUTINE PROVIDES DELAYS IN MULTIPLES
1314 /OF .1MS. ENTER WITH RETURN ADDRESS IN THE SHIFT REG.
1315 /AND MULTIPLIER IN THE COUNTER
1316
1317
1318 1300 0264      DELAY, OPEN RTNB      /SAVE THE RETURN ADDRESS
1319 1301 0064      LSP
1320
1321 1302 0075      LSR      /MULTIPLIER TO SHIFT REGISTER
1322
1323 1303 0070      LCT      /DELAY 490 CYCLES (98 MICRO SECONDS)
1324 1304 0205      -122-1
1325 1305 0073      ICT
1326 1306 0264      OPEN RTNB
1327 1307 0124      BR COFL F
1328 1310 1305      .-3
1329
1330 1311 0071      ESP      /MOVE MULTIPLIER TO CNTR VIA RTNB
1331 1312 0064      LSP
1332 1313 0075      LSR
1333 1314 0071      ESP
1334 1315 0064      LSP
1335
1336 1316 0073      ICT      /INCREMENT THE MULTIPLIER
1337
1338 1317 0124      BR COFL F      /ANY MORE .1MS LOOPS?
1339 1320 1301      DELAY+1      /YES, GO TO IT
1340
1341 1321 0223      JUMP F4 IND      /NO, RETURN FROM SUBROUTINE

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1342
1343      /([SUBROUTINE: WRITE ZEROS])
1344 /THIS SUBROUTINE WRITES A SPECIFIED NUMBER OF ZEROS IF
1345 /WRITE GATE IS ON. IF WRITE GATE IS OFF IT ACTS AS A
1346 /DELAY OF .5 BITS. ENTRANCE IS MADE WITH RETURN ADDRESS
1347 /IN THE SR, NUMBER OF BITS IN THE CNTR, AND A CLOCK
1348 /TRANSITION OCCURRING IMMEDIATELY PRIOR TO THE JUMP INTO
1349 /THIS SUBROUTINE.
1350
1351
1352 1322 0274      WRTZS, OPEN RTNB      /SAVE RETURN ADDRESS
1353 1323 0064      LSP
1354
1355 1324 0075      LSR      /PUT BIT COUNTER IN SR
1356
1357 1325 0230      OPEN TEMPB      /TEMPB IS THE PATH THROUGH THE SR
1358
1359 1326 0070      LOOP, LCT      /STALL 2.6 MICRO SECONDS
1360 1327 0374      -3-1
1361 1330 0073      ICT
1362 1331 0124      BR COFL F
1363 1332 1330      .-2
1364 1333 0064      LSP      /NOOP
1365 1334 0071      ESP      /NOOP
1366
1367 1335 0063      TCG FLAG      /WRITE A CLOCK TRANSITION IF WRT GATE IS SET
1368
1369 1336 0064      LSP      /PUT BIT COUNT IN THE COUNTER
1370 1337 0071      ESP
1371
1372 1340 0073      ICT      /INCREMENT BIT COUNT
1373
1374 1341 0075      LSR      /PUT UPDATED BIT COUNT BACK IN SR
1375
1376 1342 0124      BR COFL F      /DONE ALL BITS?
1377 1343 1326      LOOP      /NO
1378
1379 1344 0274      OPEN RTNB      /YES, RETURN FROM SUBROUTINE
1380 1345 0207      JUMP IND F1
1381
1382
1383 1346 0222      PGOTIT, JUMP F4      /POINTER TO GETWORD FROM WAITRUN
1384 1347 0210      GOTIT
1385
1386
1387      /([ROUTINE: INITIALIZE CONT.])
1388
1389 1350 0061      TEST2, FLAG OFF      /CLEAR FLAG TO INDICATE R10 IS BEING TESTED
1390
1391 1351 0070      TEST1, LCT      /LOOP TO TEST THAT SR IS 252 AND THAT
1392 1352 0372      -5-1      /IT CAN BE SHIFTED.
1393 1353 0122      TSTAGN, BR SR7 ZERO
1394 1354 1374      INTER1      /TEST FAILURE
1395 1355 0076      ROTATE ONE
1396 1356 0122      BR SR7 ONE

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1397 1357 1374 INTER1 /TEST FAILURE
1398 1360 0074 ROTATE ZERO
1399 1361 0073 ICT
1400 1362 0124 BR COFL F
1401 1363 1353 TSTAGN
1402
1403 1364 0250 OPEN R10 /CONTENTS OF R10 TO SR, SHOULD BE 125
1404 1365 0071 ESP
1405 1366 0075 LSR
1406
1407 1367 0074 ROTATE ZERO /SHIFT SR ONCE TO CHANGE 125 TO 252
1408
1409 1370 0176 BR FLAGO ONE /HAS R10 BEEN TESTED ALREADY?
1410 1371 1350 TEST2 /NO
1411
1412 1372 0202 TESTDN, JUMP F0 /YES, RETURN TO REMAINING INITIALIZE ROUTINE
1413 1373 0004 TSTRTN
1414
1415 1374 0006 INTER1, SET FMR /SELF TEST ERROR, SET ERROR AND GO SET DONE
1416 1375 0212 JUMP F2
1417 1376 1031 STDONE
1418
1419 1377 0000 0 /OPEN

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1420 /[SUBROUTINE: FINDHEADER AND FIND DATA ADDRESS MARK]
1421 /SUBROUTINE TO LOCATE A LEGAL HEADER (CORRECT CRC AND TRACK #)
1422 /ENTER WITH THE RETURN ADDRESS IN CTR0. ALSO ROUTINE TO FIND A DATA MARK
1423 /ON DELETED DATA MARK.
1424
1425 /THIS ROUTINE LOCATES A SIX BYTE PREAMBLE OF ZEROS.
1426
1427
1428 1402 0204 FINDHD, OPEN RTNB /STORE RETURN ADDRESS
1429 1401 0075 LSR
1430 1402 0204 LSP
1431
1432 1405 0230 OPEN TEMPA /256 TO BAD START INNER COUNT
1433 1404 0070 LCT
1434 1405 0377 -1
1435 1406 0075 LSR
1436 1407 0204 LSP
1437
1438 1410 0234 OPEN TEMPB /3 TO CNTR FOR BAD START OUTER COUNT, 768 BAD STARTS ALLOWED
1439 1411 0070 LCT
1440 1412 0374 -3-1
1441
1442 1413 0075 TRYAGN, LSR /RESTORE BAD START COUNT
1443 1414 0204 LSP
1444
1445 1415 0205 CLR BAR LONG /RESET FOR A COUNT OF 4096 AS PREAMBLE FAILURE COUNT
1446
1447 1416 0240 OPEN TEMPC /24 TO CNTR AS ZERO BIT COUNT
1448 1417 0070 LCT
1449 1420 0347 -24-1
1450 1421 0075 MOREPS, LSR /RESTORE ZERO BIT COUNT
1451 1422 0064 LSP
1452
1453 1423 0070 LCT /PUT 0 IN SR7 FOR DATA COMPARISONS, ALSO CONSTANT FOR 40 MICRO SEC WAIT BRANCH
1454 1424 0067 -200-1
1455 1425 0075 LSR
1456
1457 1426 0346 -BR SEPCLK T /WAIT 40 MICRO SECONDS FOR SEP CLK
1458 1427 1432 .+3
1459
1460 1430 0216 JUMP F3 /ERROR, NO SEP CLK
1461 1431 1067 TIMERR
1462
1463 1432 0154 BR DECSR7 F /WHAT IS SEP DATA?
1464 1433 1746 NOZERO /ONE, GO CHECK PREAMBLE FAILURES
1465
1466 1434 0071 ESP /ZERO FOUND, CHECK ZERO COUNT
1467 1435 0073 ICT
1468 1436 0124 BR COFL F
1469 1437 1421 MOREPS /NEED MORE ZEROS FOR PREAMBLE
1470 1440 0061 FLAG OFF /FOUND PREAMBLE, CLR FLAG TO INDICATE SEARCH FOR IDAM
1471
1472 1441 0045 GETDAM, CLR BAR LONG /START SEARCH FOR IDAM OR DATA AM, BAR IS NOSTART COUNTER
1473
1474 1442 0070 LCT /WAIT 40 MICRO SEC FOR SEP CLK

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1475 1443 0067 -200-1
1476 1444 0346 WBR SEPCLK T
1477 1445 1450 .+3
1478 1446 0216 JUMP F3 /TIMING ERROR
1479 1447 1667 TIMERR
1480
1481 1450 0156 BR DEQSR7 T /WHAT IS SEP DATA?
1482 1451 1755 NOTYET /ZERO, GO DETERMINE IF TO MANY STARTS
1483
1484 1452 2164 BR MCEQSR F /ONE, MISSING CLOCK?
1485 1453 1673 BADSRT /YES, SHOULDN'T HAVE BEEN
1486
1487 1454 0057 PRECRC /JAM 1ST TWO BITS OF CRC
1488 1455 0056 CRC ONE
1489 1456 0056 CRC ONE
1490
1491 1457 0070 LCT /WAIT 40 MICRO SECONDS FOR SECOND CELL
1492 1460 0067 -200-1
1493 1461 0346 WBR SEPCLK T
1494 1462 1465 .+3
1495 1463 0216 JUMP F3
1496 1464 1667 TIMERR
1497
1498 1465 0156 BR DEQSR7 T /DATA SHOULD BE 1, MISSING CLK SHOULD BE T
1499 1466 1673 BADSRT
1500 1467 0166 BR MCEQSR T
1501 1470 1673 BADSRT
1502
1503 1471 0056 CRC ONE /JAM 3 MORE CRC BITS
1504 1472 0056 CRC ONE
1505 1473 0056 CRC ONE
1506
1507 1474 0070 LCT /WAIT FOR THIRD BIT CELL
1508 1475 0067 -200-1
1509 1476 0346 WBR SEPCLK T
1510 1477 1502 .+3
1511 1500 0216 JUMP F3
1512 1501 1667 TIMERR
1513
1514 1502 0154 BR DEQSR7 F /DATA SHOULD BE 0, MISSING CLK SHOULD BE F
1515 1503 1673 BADSRT
1516 1504 0164 BR MCEQSR F
1517 1505 1673 BADSRT
1518
1519 1506 0070 LCT /CLEAR SR
1520 1507 0000 0
1521 1510 0075 LSR
1522
1523 1511 0070 LCT /WAIT FOR 4TH BIT CELL
1524 1512 0067 -200-1
1525 1513 0346 WBR SEPCLK T
1526 1514 1517 .+3
1527 1515 0216 JUMP F3
1528 1516 1667 TIMERR
1529

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1530 1517 0154 BR DEQSR7 F /DATA SHOULD BE 0, MISSING CLK SHOULD BE F
1531 1520 1673 BADSRT
1532 1521 0042 LDMD /NOOP FOR LONG SEP CLOCK
1533 1522 0042 LDMD /NOOP FOR LONG SEP CLOCK
1534 1523 0164 BR MCEQSR F
1535 1524 1673 BADSRT
1536
1537 1525 0070 LCT /WAIT FOR FIFTH BIT CELL
1538 1526 0067 -200-1
1539 1527 0346 WBR SEPCLK T
1540 1532 1533 .+3
1541 1531 0216 JUMP F3
1542 1532 1667 TIMERR
1543
1544 1533 0156 BR DEQSR7 T /DATA SHOULD BE 1
1545 1534 1673 BADSRT
1546
1547 1535 0176 BR FLAGO T /IF FLAG SET FINISH LOOKING FOR DATA AM
1548 1536 1675 DAM
1549
1550 1537 0164 BR MCEQSR F /FINISH IDAM, MISSING CLK SHOULD BE F
1551 1540 1673 BADSRT
1552
1553 1541 0056 CRC ONE /JAM 6TH CRC BIT OF IDAM
1554
1555 1542 0070 LCT /WAIT FOR SIXTH BIT CELL
1556 1543 0067 -200-1
1557 1544 0346 WBR SEPCLK T
1558 1545 1550 .+3
1559 1546 0216 JUMP F3
1560 1547 1667 TIMERR
1561
1562 1552 0156 BR DEQSR7 T /DATA SHOULD BE 1, MISSING CLK SHOULD BE F
1563 1551 1673 BADSRT
1564 1552 2164 BR MCEQSR F
1565 1553 1673 BADSRT
1566
1567 1554 0042 LDMD /NOOP FOR LONG SEP CLOCK
1568
1569 1555 0056 CRC ONE /JAM 7TH CRC BIT OF IDAM
1570
1571 1556 0070 LCT /WAIT FOR SEVENTH BIT CELL
1572 1557 0067 -200-1
1573 1560 0346 WBR SEPCLK T
1574 1561 1564 .+3
1575 1562 0216 JUMP F3
1576 1563 1667 TIMERR
1577
1578 1564 0156 BR DEQSR7 T /DATA SHOULD BE 1, MISSING CLK SHOULD BE T
1579 1565 1673 BADSRT
1580 1566 0166 BR MCEQSR T
1581 1567 1673 BADSRT
1582
1583 1570 0054 CRC ZERO /IDAM FOUND, JAM LAST CRC BIT
1584

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```

1585
1586
1587
1588
1589 /THIS ROUTINE COMPARES THE HEADER TRACK ADDRESS TO THE
1590 /DESIRED TRACK ADDRESS ON THE FLY. IT IS ENTERED AFTER
1591 /FINDING THE IDAM, ERREG BIT IS SET IF AN ERROR IS DETECTED.
1592
1593
1594 1571 0220 HDRCOM, OPEN TARTRK /TARGET TRACK ADDRESS TO SR
1595 1572 0071 ESP
1596 1573 0075 LSR
1597
1598 1574 0070 LCT /SET BIT COUNTER TO 8
1599 1575 0367 -8-1
1600
1601 1576 0144 AGAIN3, BR SEPCLK F /WAIT FOR BIT CELL
1602 1577 1576 .-1
1603
1604 1600 0156 BR DEGSRT T /SEP DATA EQUAL TO SR??
1605 1601 1605 .+4 /NO, TRACK COMPARE ERROR
1606
1607 1602 0074 ROTATE ZERO /YES, GET NEXT TRACK ADDRESS BIT
1608 1603 0216 JUMP F3
1609 1604 1610 .+4
1610
1611 1605 0210 OPEN ERREG /SET ERREG BIT TO INDICATE TRACK ERROR
1612 1606 0076 ROTATE ONE
1613 1607 0064 LSP
1614
1615 1612 0055 DATCRC /UPDATE THE CRC
1616
1617 1611 0073 ICT /INCREMENT AND TEST THE BIT COUNTER
1618 1612 0124 BR COFL F
1619 1613 1576 AGAIN3 /GO DO NEXT BIT
1620
1621 1614 0070 LCT /TRACK COMPARED, SET UP BIT COUNTER FOR 8 BYTE
1622 1615 0367 -8-1
1623
1624 1616 0144 AGAIN4, BR SEPCLK F /WAIT FOR BIT
1625 1617 1616 .-1
1626
1627 1620 0061 FLAG OFF /CLEAR FLAG FOR NEXT ROUTINE
1628 1621 0061 FLAG OFF /NOOP FOR LONG SEP CLK
1629 1622 0061 FLAG OFF /NOOP FOR LONG SEP CLK
1630 1623 0061 FLAG OFF /NOOP FOR LONG SEP CLK
1631
1632 1624 0055 DATCRC /UPDATE CRC
1633
1634 1625 0073 ICT /INCREMENT AND TEST BIT COUNT
1635 1626 0124 BR COFL F
1636 1627 1616 AGAIN4 /GO DO ANOTHER BIT
1637 /CONTINUE
1638
1639

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1640 /THIS ROUTINE COMPARES THE HEADER SECTOR ADDRESS WITH THE
1641 /TARGET SECTOR ADDRESS ON THE FLY. IT IS ENTERED FROM
1642 /THE TRACK COMPARE ROUTINE. A MISMATCH WILL SET THE FLAG.
1643
1644
1645 1630 0224 OPEN TARSEC /TARGET SECTOR ADDRESS TO SR
1646 1631 0071 ESP
1647 1632 0075 LSR
1648
1649 1633 0070 LCT /SET UP BIT COUNTER FOR 8 BITS
1650 1634 0367 -8-1
1651
1652 1635 0144 AGAIN5, BR SEPCLK F /WAIT FOR A BIT
1653 1636 1635 .-1
1654
1655 1637 0156 BR DEGSRT T /HOW DO THEY COMPARE?
1656 1640 1643 .+3 /BAD, GO SET THE FLAG
1657
1658 1641 0216 JUMP F3 /GOOD, SKIP THE ERROR FLAG.
1659 1642 1644 .+2
1660
1661 1643 0262 FLAG ON /SET FLAG TO INDICATE MISMATCH
1662
1663 1644 0074 ROTATE ZERO /BRING UP NEXT BIT
1664
1665 1645 0055 DATCRC /UPDATE THE CRC
1666 1646 0073 ICT /BUMP THE BIT COUNTER
1667 1647 0124 BR COFL F /ALL BITS COMPARED?
1668 1650 1635 AGAIN5 /NO, LOOP BACK
1669
1670 1651 0070 LCT /YES, SETUP TO WAIT FOR END OF
1671 1652 0347 -24-1 /CRC
1672
1673 1653 0144 AGAIN6, BR SEPCLK F /WAIT FOR BIT
1674 1654 1653 .-1
1675
1676 1655 0074 ROTATE ZERO /NOOP FOR LONG SEP CLK
1677 1656 0074 ROTATE ZERO /NOOP FOR LONG SEP CLK
1678 1657 0074 ROTATE ZERO /NOOP FOR LONG SEP CLK
1679 1660 0074 ROTATE ZERO /NOOP FOR LONG SEP CLK
1680
1681 1661 0255 DATCRC /UPDATE CRC
1682
1683 1662 0073 ICT /BUMP THE BIT COUNTER
1684 1663 0124 BR COFL F /ALL DONE?
1685 1664 1653 AGAIN6 /NO, LOOP BACK
1686
1687 1665 0226 JUMP F5 /YES, GO CHECK IF CRC IS ALL ZEROES
1688 1666 2515 CMHCRC
1689
1690
1691 1667 0070 TIMERR, LCT /40 MICROSEC PASSED AND NO SEP CLOCK WAS SEEN
1692 1670 0110 RTIMERR
1693 1671 0226 JUMP F5
1694 1672 2612 GOERDN

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1695
1696
1697      1673 0226  BADSRT, JUMP F5      /POINTER TO BADSTART ON IDAM OR DATA AM
1698      1674 2555  BDSRT
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708      1675 0166  DAM,   BR MCEQSR T      /MISSING CLK SHOULD BE T
1709      1676 1673  BADSRT
1710
1711      1677 0054          CRC ZERO      /JAM 6TH CRC BIT OF DATA AM
1712
1713      1700 0070          LCT          /WAIT FOR SIXTH BIT CELL
1714      1701 0067          -200-1
1715      1702 0346          MBR SEPCLK T
1716      1703 1706          .+3
1717      1704 0216          JUMP F3
1718      1705 1667          TIMERR
1719
1720      1706 0164  BR MCEQSR F      /MISSING CLK SHOULD BE F
1721      1707 1673  BADSRT
1722      1710 0042          LDHD          /NOOP FOR LONG SEP CLK
1723
1724      1711 0156  BR DEQSR7 T      /IF DATA=0 THEN LOOK FOR DELETED DATA AM
1725      1712 1727  DELDAT
1726
1727      1713 0056          CRC ONE      /JAM 7TH BIT OF DATA AM
1728
1729      1714 0070          LCT          /WAIT FOR SEVENTH BIT OF DATA AM
1730      1715 0067          -200-1
1731      1716 0346          MBR SEPCLK T
1732      1717 1722          .+3
1733      1720 0216          JUMP F3
1734      1721 1667          TIMERR
1735
1736      1722 0056          CRC ONE      /JAM LAST BIT OF DATA AM
1737
1738      1723 0154  BR DEQSR7 F      /DATA SHOULD BE 1
1739      1724 1742  ENDDAM      /FLAG IS SET TO INDICATE NORMAL DATA MARK
1740
1741      1725 0216          JUMP F3
1742      1726 1673  BADSRT      /LAST DATA BIT WAS BAD
1743
1744
1745      1727 0054  DELDAT, CRC ZERO      /JAM 7TH CRC BIT OF DEL DATA AM
1746
1747      1730 0070          LCT          /WAIT FOR 7TH CELL OF DEL DATA AM
1748      1731 0067          -200-1
1749      1732 0346          MBR SEPCLK T
    
```

```

1750      1733 1736          .+3
1751      1734 0216          JUMP F3
1752      1735 1667          TIMERR
1753
1754      1736 0061          FLAG OFF      /CLR FLAG TO INDICATE DELETED DATA MARK
1755
1756      1737 0054          CRC ZERO      /JAM LAST CRC BIT OF DEL DATA AM
1757
1758      1740 0154  BR DEQSR7 F      /DATA SHOULD BE 0
1759      1741 1673  BADSRT
1760
1761      1742 0164  ENDDAM, BR MCEQSR F      /MISSING CLK SHOULD BE F FOR BOTH DATA AMS
1762      1743 1673  BADSRT
1763
1764      1744 0222          JUMP F4
1765      1745 2246          DATA      /GO PICK UP DATA FIELD
1766
1767
1768      1746 0046  NOZERO, INCR BAR      /INCREMENT AND TEST PREAMBLE FAILURE COUNT
1769      1747 0160  BR BAROFL F
1770      1750 1416          TRYAGN+3      /OK, TRY AGAIN FOR A PREAMBLE
1771
1772      1751 0070  KXPRAM, LCT      /TOO MANY BITS WITH NO ZEROS
1773      1752 0120          KXPRAM
1774      1753 0226          JUMP F5
1775      1754 2610          GOERDN
1776
1777
1778      1755 0246  NOTYET, INCR BAR      /INCR AND TEST IDAM OR DATA AM START FAILURE COUNT
1779      1756 0042          LDHD          /NOOP FOR LONG SEP CLK
1780      1757 0160          BR BAROFL F
1781      1760 1442          GETDAM+1      /OK, TRY AGAIN
1782
1783      1761 0070  NXIDAM, LCT      /TOO MANY ZEROS WHILE LOOKING FOR START OF
1784      1762 0130          KXIDAM      /IDAM OR DATA AM
1785      1763 0226          JUMP F5
1786      1764 2610          GOERDN
1787
1788
1789      1765 0212  PTRDY, JUMP F2      /POINTERS FROM CHECKRDY SUBROUTINE TO ROSTAT ROUTINE
1790      1766 1243          CLRID
1791      1767 0212  PYSRDY, JUMP F2
1792      1770 1243          CLRID
1793
1794      1771 0212  PNRDY, JUMP F2      /POINTERS FROM CHECK RDY TO INITIALIZE ROUTINE
1795      1772 1006          OKDONE
1796      1773 0226          JUMP F5
1797      1774 2631          INTRDY
1798
1799      1775 0000          0      /OPEN
1800      1776 0000          0      /OPEN
1801      1777 0000          0      /OPEN
1802
    
```

```

1803 /SUBROUTINES: GETWORD AND GETCOMMAND
1804 /SUBROUTINE TO GET AN EIGHT BIT WORD FROM THE INTERFACE,
1805 /IF TALKING TO A PDP8 INTERFACE IN 12 BIT MODE, THERE
1806 /WILL BE FOUR MEANINGLESS BITS PRECEDING THE DESIRED EIGHT
1807 /BIT WORD, ENTER THIS SUBROUTINE WITH THE RETURN ADDRESS
1808 /IN THE COUNTER, EXIT WITH THE ONES COMPLIMENT OF THE
1809 /DESIRED WORD IN THE SHIFT REGISTER, PARITY IS COMPUTED AND
1810 /CHECKED ON ALL WORDS,
1811
1812
1813 2000 0012 GETWRD, SET XREQ /REQUEST A WORD FROM INTERFACE
1814
1815 2001 0075 GETCMD, LSR /STASH THE RETURN ADDRESS
1816 2002 0270 OPEN RTNA
1817 2003 0064 LSP
1818
1819 2004 2070 LCT /CALL SUBR WAITRN TO WAIT FOR A WORD
1820 2005 1346 PGOTIT
1821 2006 0222 JUMP F4
1822 2007 2312 WAITRN
1823
1824 2010 0061 GOTIT, OFF FLAG /CLEAR FLAG FOR PARITY CHECK
1825
1826 2011 0004 CLR ERR /IN CASE RUN WAS A RESPONSE TO DONE
1827 2012 0020 CLR DONE
1828
1829 2013 0070 LCT /SET UP BIT COUNT IN CNTR, 8 BIT OR 12 BIT
1830 2014 0367 -8-1
1831 2015 0150 BR XIIBIT F
1832 2016 2021 +3
1833 2017 0070 LCT
1834 2020 0363 -12-1
1835
1836 2021 0112 WATDAT, BR DATAIN ONE /WHAT IS THE DATA BIT?
1837 2022 2030 GOTONE /ITS A ONE, GO SAVE IT
1838
1839 2023 0126 BR COFL T /ITS A ZERO, WAS IT THE PARITY BIT (9TH BIT)?
1840 2024 2041 CHKPAR /YES, GO CHECK PARITY
1841
1842 2025 0076 ROTATE ONE /NO SAVE THE DATA BIT COMPLIMENTED IN SR
1843
1844 2026 0222 JUMP F4 /GO SHIFT UP ANOTHER BIT.
1845 2027 2034 NUTHER
1846
1847
1848
1849
1850 2030 2063 GOTONE, TUG FLAG /COMPLIMENT THE PARITY GENERATOR
1851
1852 2031 0126 BR COFL T /WAS IT THE PARITY BIT?
1853 2032 2041 CHKPAR /YES, GO CHECK PARITY
1854
1855 2033 0074 ROTATE ZERO /NO, SAVE THE COMPLIMENTED DATA BIT IN SR
1856
1857 2034 2026 NUTHER, SET SHIFT /SHIFT PULSE AND INCREMENT BIT COUNT

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```

1858 2035 0273 ICT
1859 2036 2024 CLR SHIFT
1860
1861 2037 0222 JUMP F4 /GO TEST THIS BIT.
1862 2040 2021 WATDAT
1863
1864
1865 2041 2176 CHKPAR, BR FLAGD ONE /WHERE THERE AN ODD NO. OF ONES?
1866 2042 2076 GOTWRD /YES, PARITY WAS GOOD
1867
1868 2043 0214 OPEN STAT /NO, STAT TO SR
1869 2044 0071 ESP
1870 2045 2075 LSR
1871
1872 2046 0070 LCT /END AROUND SHIFT OF UPPER 5 BITS OF STAT IN SR
1873 2047 2072 -5-1
1874 2050 0122 BR SR7 T
1875 2051 2055 +4
1876 2052 0074 ROTATE ZERO
1877 2053 0222 JUMP F4
1878 2054 2056 +2
1879 2055 0076 ROTATE ONE
1880 2056 0073 ICT
1881 2057 0124 BR COFL F
1882 2060 2050 -8
1883
1884 2061 0074 ROTATE ZERO /CLEAR INIT DONE
1885 2062 0076 ROTATE ONE /SET PARITY ERROR
1886
1887 2063 0122 BR SR7 T /END AROUND SHIFT OF CRC ERROR BIT OF STAT IN SR
1888 2064 2070 +4
1889 2065 0074 ROTATE ZERO
1890 2066 0222 JUMP F4
1891 2067 2071 +2
1892 2070 2076 ROTATE ONE
1893
1894 2071 2064 LSP /RESTORE STAT TO SCRATCH PAD
1895
1896 2072 0070 LCT /ERRCODE FOR PARITY ERROR
1897 2073 0210 KPARER
1898 2074 0226 JUMP F5
1899 2075 2610 GOERDN
1900
1901 2076 0270 GOTWRD, OPEN RTNA /WORD WAS GOOD, EXIT FROM GETWRD, GETCMD
1902 2077 0203 JUMP F2 IND

```

```

1903
1904      /([SUBROUTINE: STEPHEAD])
1905      /THIS SUBROUTINE WILL STEP THE SPECIFIED NUMBER OF TRACKS IN THE
1906      /SPECIFIED DIRECTION. DIRECTION IS DETERMINED BY THE HD DIR FLOP
1907
1908      /THE NUMBER OF STEPS IS IN THE SR. RETURN ADDRESS IS IN THE CNTR.
1909      /EXIT IS TO THE RETURN ADDRESS IF HOMP IS DETECTED. EXIT IS TO RETURN
1910      /PLUS 2 IF THE LAST STEP HAS BEEN TAKEN. AFTER THE LAST STEP IS TAKEN,
1911      /THE HEAD IS LOADED AND A 25MS DELAY IS EXECUTED FOR HEAD SETTLE TIME
1912
1913
1914
1915
1916      2100 0270      STEPHD, OPEN RTNA      /STORE RETURN ADDR AND MOVE STEP COUNT TO CNTR
1917      2101 0064      LSP
1918      2102 0075      LSR
1919      2103 0071      ESP
1920      2104 0064      LSP
1921
1922      2105 0136      CKHOME, BR HOME T      /IS THE HEAD HOME?
1923      2106 2150      OUT      /YES, GO EXIT
1924
1925      2107 0073      ICT
1926      2110 0075      LSR      /NO, INCREMENT STEP COUNT AND STORE IN TEMPA
1927      2111 0230      OPEN TEMPA
1928      2112 0064      LSP
1929
1930      2113 0270      LCT      /PASS 30 TO DELAY SUBR FOR 3MS DELAY
1931      2114 2124      SECPLS
1932      2115 0075      LSR
1933      2116 0070      LCT
1934      2117 0341      -30-1
1935
1936      2120 0012      SET STPHD      /ISSUE STEP PULSE
1937      2121 0010      CLR STPHD
1938
1939      2122 0212      JUMP F2      /CALL DELAY SUBR
1940      2123 1300      DELAY
1941
1942      2124 0012      SECPLS, SET STPHD      /ISSUE SECOND STEP PULSE
1943      2125 0010      CLR STPHD
1944
1945      2126 0070      LCT      /CALL DELAY FOR 3MS DELAY
1946      2127 2135      DONSTP
1947      2130 0075      LSR
1948      2131 0070      LCT
1949      2132 0341      -30-1
1950      2133 0212      JUMP F2
1951      2134 1300      DELAY
1952
1953      2135 0230      DONSTP, OPEN TEMPA      /CHECK STEP COUNT
1954      2136 0071      ESP
1955      2137 0124      BR COFL F
1956      2140 2125      CKHOME      /NOT DONE, GO CHECK IF HOME
1957

```

```

1958      2141 0270      OPEN RTNA      /DONE STEPPING, INCREMENT RETURN ADDRESS BY 2
1959      2142 0071      ESP
1960      2143 0073      ICT
1961      2144 0073      ICT
1962
1963      2145 0270      DLY25, OPEN RTNA      /STORE RETURN ADDRESS ALSO START OF 25MS DELAY SUBROUTINE
1964      2146 0075      LSR
1965      2147 0064      LSP
1966
1967      2150 0042      OUT, LDMD      /LOAD HEAD
1968      2151 0250      OPEN TEMPE      /SET SOFT HD LOAD BIT
1969      2152 0070      LCT
1970      OCTAL
1971      2153 0200      200
1972      DECIMAL
1973      2154 0075      LSR
1974      2155 0064      LSP
1975
1976      2156 0270      LCT      /CALL DELAY SUBR FOR 25MS DELAY
1977      2157 2165      DONDLY
1978      2160 0075      LSR
1979      2161 0270      LCT
1980      2162 0000      -255-1
1981      2163 0212      JUMP F2
1982      2164 1300      DELAY
1983
1984      2165 0270      DONDLY, OPEN RTNA      /RETURN FROM STEP HEAD OR DELAY 25MS SUBROUTINE
1985      2166 0203      JUMP F0 IND
1986
1987
1988
1989
1990
1991
1992
1993      /([ROUTINE: READ SECTOR CONT.])
1994
1995      2167 0070      READ, LCT      /3 TO DATA MARK TRY COUNTER
1996      2170 0374      -3-1
1997      2171 0234      OPEN TEMPB
1998      2172 0075      LSR
1999      2173 0064      LSP
2000
2001      2174 0070      LCT      /STALL FOR 96 MICRO SEC (3 BYTES) TO AVOID WRT TURN ON SPLASH
2002      2175 0207      -120-1
2003      2176 0073      ICT
2004      2177 0062      FLAG ON      /SET THE FLAG TO SPECIFY DATA AM IN FIND AM ROUTINE
2005      2200 0124      BR COFL F
2006      2201 2176      -3
2007
2008      2202 0073      ICT      /CLR COUNTER AND SR
2009      2203 0075      LSR
2010
2011      2204 0216      JUMP F3      /GO TRY FIND THE ADDRESS MARK
2012      2205 1441      GETDAM

```

```

2013
2014
2015 /THIS ROUTINE FOLLOWS THE DISCOVERY OF A DATA MARK OR
2016 /A DELETED DATA MARK, IT MOVES THE NEXT 1024 BITS
2017 /INTO THE SECTOR BUFFER, THEN PICKS UP AND CHECKS THE CRC.
2018
2019 2206 0044 DATA, CLR BAR /CLEAR THE BUFFR ADDRESS REGISTER
2020
2021 2207 0144 BR SEPCLK F /WAIT FOR CLOCK
2022 2210 2207 .-1
2023
2024 2211 0053 START WRTBUF /START THE WRITE PULSE FOR THIS BIT
2025
2026 2212 0055 DATCRC /UPDATE THE CRC WITH SEP DATA
2027
2028 2213 0162 BR BAROFL T /IS BUFFER FULL YET?
2029 2214 2221 GETCRC /YES, GO GET THE CRC
2030
2031 2215 0050 FIN WRTBUF /NO, END THE WRITE PULSE
2032
2033 2216 0046 INCR BAR /ADDRESS NEXT SECTOR BUFFER CELL
2034
2035 2217 0222 JUMP F4 /LOOP BACK FOR NEXT BIT
2036 2220 2207 DATA+1
2037
2038 2221 0050 GETCRC, FIN WRTBUF /END THE WRITE PULSE FOR THE LAST BIT
2039
2040 2222 0070 LCT /SET BIT COUNT TO 16 FOR 2 BYTE CRC
2041 2223 0357 -16-1
2042
2043 2224 0144 BR SEPCLK F /WAIT FOR NEXT BIT
2044 2225 2224 .-1
2045
2046 2226 0042 LDMD /4 NOOPS FOR LONG SEP CLOCK
2047 2227 0042 LDMD
2048 2230 0042 LDMD
2049 2231 0042 LDMD
2050
2051 2232 0055 DATCRC /PUT CRC BIT IN THE CRC GENERATOR
2052 2233 0073 ICT /INCREMENT AND TEST BIT COUNT
2053 2234 0124 BR COFL F
2054 2235 2224 .-9 /NOT DONE, GET ANOTHER
2055
2056 2236 0214 OPEN STAT /STATUS TO SHFT REG
2057 2237 0071 ESP
2058 2240 0375 LSR
2059
2060 2241 0122 BR SP7 T /END AROUND SHIFT OF DRV RDY BIT OF STAT IN SR
2061 2242 2246 .+4
2062 2243 0074 ROTATE ZERO
2063 2244 0222 JUMP F4
2064 2245 2247 .+2
2065 2246 0076 ROTATE ONE
2066
2067 2247 0176 BR FLAG0 T /SET DEL DATA BIT OF STAT IF FLAG=0

```

```

2068 2250 2254 .+4
2069 2251 0276 ROTATE ONE
2070 2252 0222 JUMP F4
2071 2253 2255 .+2
2072 2254 0074 ROTATE ZERO
2073
2074 2255 0070 LCT /END AROUND SHIFT OF NEXT 5 BITS OF STAT IN SR
2075 2256 0372 -5-1
2076 2257 0122 BR SP7 T
2077 2260 2264 .+4
2078 2261 0074 ROTATE ZERO
2079 2262 0222 JUMP F4
2080 2263 2265 .+2
2081 2264 0074 ROTATE ONE
2082 2265 0073 ICT
2083 2266 0124 BR COFL F
2084 2267 2257 .-8
2085
2086 2270 0070 LCT /SET BIT COUNTER TO 16 FOR CRC TEST
2087 2271 0357 -16-1
2088
2089 2272 0132 BR CRC16 ONE /IS THIS CRC BIT OK
2090 2273 2304 DCR CER /NO, GO REPORT DATA CRC ERROR
2091
2092 2274 0054 CRC ZERO /YES, BRING UP NEXT CRC BIT
2093
2094 2275 0073 ICT /INCREMENT AND TEST BIT COUNTER
2095 2276 0124 BR COFL F
2096 2277 2272 .-5 /GO CHECK ANOTHER
2097
2098 2300 0074 ROTATE ZERO /CRC WAS GOOD, CLR CRC ERR BIT OF STAT IN SR
2099
2100 2301 0064 LSP /PUT THE STATUS WORD BACK IN SCRATCHPAD
2101
2102 2302 0212 JUMP F2 /EXIT TO DONE
2103 2303 1006 OKDONE
2104
2105 2304 0076 DCR CER, ROTATE ONE /INSERT 1 INTO CRC ERROR BIT
2106
2107 2305 0064 LSP /PUT THE STAT WORD BACK
2108
2109 2306 0070 LCT /ERROR CODE FOR CRC ERROR
2110 2307 0200 KDCR CER
2111 2310 0226 JUMP F5
2112 2311 2610 GOERDN

```

```

2113      /([SUBROUTINE: WAIT FOR RUN])
2114      /THIS SUBROUTINE WILL WAIT FOR RUN. IF 46MS ELAPSES, THE HEAD IS UNLOADED
2115      /AND THE ROUTINE CONTINUES WAITING FOR RUN. RETURN ADDRESS IS PASSED
2116      /VIA THE COUNTER
2117
2118
2119      2312 0264 WAITRN, OPEN RTNB /STASH THE RETURN ADDRESS
2120      2313 0075 LSR
2121      2314 0264 LSR
2122
2123      2315 0102 BR RUN T /GOT RUN?
2124      2316 2347 GOTRUN
2125
2126      2317 0240 OPEN TEMPC /PRESET LOOP COUNTER TO 0
2127      2320 0070 LCT
2128      2321 0000 0
2129
2130      2322 0075 BACK, LSR /RESTORE LOOP COUNT
2131      2323 0064 LSP
2132
2133      2324 0302 WBR RUN T /TIME WHILE WAITING FOR RUN
2134      2325 2347 GOTRUN
2135      2326 0302 WBR RUN T
2136      2327 2347 GOTRUN
2137      2330 0302 WBR RUN T
2138      2331 2347 GOTRUN
2139      2332 0302 WBR RUN T
2140      2333 2347 GOTRUN
2141
2142      2334 0071 ESP /INCREMENT AND TEST LOOP COUNT
2143      2335 0073 ICT
2144      2336 0124 BR COPL F
2145      2337 2322 BACK /46MS NOT ELAPSED YET
2146
2147      2340 0250 OPEN TEMPE /TIME IS EXPIRED (45.8 MS), CLEAR THE SOFT HOLD BIT AND UNLOAD THE HEAD
2148      2341 0073 ICT
2149      2342 0075 LSR
2150      2343 0064 LSP
2151      2344 0040 UNHD
2152
2153      2345 0100 BR RUN F /WAIT FOR RUN. FOREVER IF NECESSARY
2154      2346 2345 *-1
2155
2156      2347 0010 GOTRUN, CLR XREQ /IF RUN WAS RESPONSE TO XFREQ
2157
2158      2350 0204 OPEN RTNB /RETURN FROM WAITRN SUBROUTINE
2159      2351 0213 JUMP IND F2
2160
2161

```

```

2162      /([ROUTINE: INITIALIZE CONT.])
2163      /CONTINUATION OF THE INITIALIZE SELF TEST
2164
2165      2352 0070 TEST, LCT /LOAD R5 WITH TEST PATTERN 252
2166      OCTAL
2167      2353 0252 252
2168      DECIMAL
2169      2354 0075 LSR
2170      2355 0224 OPEN R5
2171      2356 0064 LSP
2172
2173      2357 0070 LCT /LOAD R10 WITH TEST PATTERN 125
2174      OCTAL
2175      2360 0125 125
2176      DECIMAL
2177      2361 0075 LSR
2178      2362 0250 OPEN R10
2179      2363 0064 LSP
2180
2181      2364 0062 FLAG ON /SET FLAG AND TEST IT
2182      2365 0176 BR FLAGO T
2183      2366 2371 *-3
2184      2367 0212 JUMP F2
2185      2370 1374 INTER1 /FLAG FAILURE
2186
2187      2371 0224 OPEN R5 /CONTENTS OF R5 TO SR, SHOULD BE 252
2188      2372 0071 ESP
2189      2373 0075 LSR
2190
2191      2374 0212 JUMP F2 /GO CONTINUE INIT TEST IN FLD 2
2192      2375 1351 TEST1
2193
2194
2195      2376 0000 0 /OPEN
2196      2377 0000 0 /OPEN

```

```

2197 /([SUBROUTINE: MAGNITUDE COMPARISON])
2198 /THIS SUBROUTINE COMPARES THE EIGHT BIT NUMBERS IN REGISTERS F AND G
2199 /EXIT IS TO THE RETURN ADDRESS IF F=G, IF F<G, RETURN IS TO RTNA+2,
2200 /IF F>G, RETURN IS TO RTNA+4, CONTENTS OF F AND G ARE UNDEFINED AT
2201 /THE END OF THE SUBROUTINE
2202
2203
2204
2205
2206 2400 0230 MAGCOM, OPEN TEMPA /FOR BIT COUNT
2207
2208 2401 0070 LCT /BIT COUNT IS 8
2209 2402 0367 -8-1
2210
2211 2403 0075 LSP /RESTORE BIT COUNT
2212 2404 0064 LSP
2213
2214 2405 0254 OPEN TEMPF /F TO SR
2215 2406 0071 ESP
2216 2407 0075 LSR
2217
2218 2410 0120 BR SR7 ZERO /TEST F
2219 2411 2443 TSTG0 /ITS 0
2220
2221 2412 0076 ROTATE ONE /ITS 1, BRING UP NEXT BIT
2222
2223 2413 0064 LSP /RESTORE F
2224
2225 2414 0260 OPEN TEMPG /G TO SR
2226 2415 0071 ESP
2227 2416 0075 LSR
2228
2229 2417 0120 BR SR7 ZERO /TEST G
2230 2420 2432 GLESSF /ITS 0, G IS LESS THAN F
2231
2232 2421 0074 NEXTG, ROTATE ZERO /ITS 1, BRING UP NEXT G BIT
2233
2234 2422 0064 LSP /RESTORE G
2235
2236 2423 0230 OPEN TEMPA /INCREMENT AND TEST BIT COUNT
2237 2424 0071 ESP
2238 2425 0073 ICT
2239 2426 0124 BR COFL F
2240 2427 2403 MAGCOM+3 /GO COMPARE ANOTHER BIT
2241
2242 2430 2272 OPEN RTNA /ALL BITS COMPARED, NO DIFFERENCE
2243 2431 0203 JUMP F0 IND
2244
2245 2432 0270 GLESSF, OPEN RTNA /G IS LESS THAN F RETURN TO RTNA +4
2246 2433 0071 ESP
2247 2434 0073 ICT
2248 2435 0073 ICT
2249 2436 0273 ICT
2250 2437 0073 ICT
2251 2440 0075 LSR
    
```

```

2252 2441 0064 LSP
2253 2442 0203 JUMP F0 IND
2254
2255 2443 0074 TSTG0, ROTATE ZERO /F HAS 0, BRING UP NEXT BIT
2256
2257 2444 0064 LSP /RESTORE F
2258
2259 2445 0260 OPEN TEMPG /G TO SR
2260 2446 0071 ESP
2261 2447 0075 LSR
2262
2263 2450 0120 BR SR7 ZERO /TEST G
2264 2451 2421 NEXTG /MATCHES F, GO BRING UP NEXT G BIT
2265
2266 2452 0270 OPEN RTNA /G IS LESS THAN F, RETURN TO RTNA +2
2267 2453 0271 ESP
2268 2454 0226 JUMP F5
2269 2455 2436 GLESSF+4
2270
2271
2272
2273 /([SUBROUTINE: FIND TRACK CONT.])
2274
2275 2456 0270 HOMERR, LCT /HOME FOUND BEFORE LAST STEP TAKEN
2276 2457 0050 KHOMERR
2277 2460 0226 JUMP F5
2278 2461 2610 GOERDN
2279
2280
2281 /([SUBROUTINE: DIFFERENCE])
2282 /THIS SUBROUTINE COMPUTES THE DIFFERENCE BETWEEN TWO EIGHT BIT
2283 /NUMBERS, ENTER WITH THE RETURN ADDRESS IN RTN, A IN THE
2284 /COUNTER AND B IN THE SHIFT REGISTER, EXIT IS MADE WITH THE
2285 /COMPLIMENT OF THE DIFFERENCE IN THE SHIFT REGISTER,
2286 /EXIT IS TO RTN IF A>=B, EXIT IS TO RTN+2 IF A<B
2287
2288
2289
2290
2291 2462 0230 DIF, OPEN TEMPA /OPEN TEMPORARY PATH THRU THE SP
2292
2293 2463 0120 BR COFL T /HAS A REACHED ALL ONES YET?
2294 2464 2501 DIFB /YES, GO GET M FOR THE DIFFERENCE
2295
2296 2465 0064 LSP /NO, GET B
2297 2466 0075 LSR /A INTO SHIFT REG
2298 2467 0071 ESP /B INTO COUNTER
2299
2300 2470 0120 BR COFL T /HAS B REACHED ALL ONES YET?
2301 2471 2503 DIFA /YES, GO GET A FOR THE DIFFERENCE
2302
2303 2472 0073 ICT /INCREMENT B
2304 2473 0064 LSP /, BRING BACK A
2305 2474 0075 LSR /B INTO SHIFT REG
2306 2475 0071 ESP /A INTO COUNTER
    
```

```

2307 2476 0073      ICT      /INCREMENT A
2308 2477 0226      JUMP FS  /GO BACK TO TEST A AGAIN
2309 2502 2463      DIF+1
2310
2311
2312 2501 0270      DIFB,   OPEN RTNA  /B IS THE COMPLIMENT OF THE DIFFERENCE
2313 2502 0203      JUMP F0 IND /EXIT A>=B
2314
2315
2316 2503 0270      DIFA,   OPEN RTNA  /A IS THE COMPLIMENT OF THE DIFFERENCE
2317 2504 0071      ESP      /INCREMENT THE RETURN ADDRESS BY 2
2318 2505 0073      ICT
2319 2506 0073      ICT
2320
2321 2507 0064      LSP      /RESTORE RETURN ADDRESS TO SCRATCHPAD AND A TO SR
2322 2510 0275      LSR
2323 2511 0071      ESP
2324 2512 0064      LSP
2325 2513 0075      LSR
2326
2327 2514 0203      JUMP F0 IND /EXIT A<B
2328
2329
2330 /[ROUTINE: FIND HEADER CONT.]
2331 /THIS ROUTINE CHECKS THE CRC, AND THE RESULTS OF THE TRACK
2332
2333 /AND SECTOR COMPARISONS.
2334
2335
2336
2337
2338 2515 0070      CKCRC,  LCT      /PRESET BIT COUNT TO 16 FOR CRC
2339 2516 0357      -16-1
2340
2341 2517 0132      BR CRC16 ONE  /IS CRC ZERO
2342 2520 2540      MRCER      /NO, LOG ERROR AND TRY AGAIN
2343
2344 2521 0073      ICT      /YES, CRC GOOD SO FAR, BUMP BIT CNTR
2345
2346 2522 0054      CRC ZERO   /BRING UP NEXT CRC BIT
2347
2348 2523 0124      BR COFL F   /ALL BITS TESTED?
2349 2524 2517      .-5      /NO, BRANCH BACK
2350
2351 2525 0210      OPEN ERREG  /YES, CRC WAS GOOD, CHECK TRK COMP
2352 2526 0271      ESP
2353 2527 0075      LSR
2354
2355 2530 0270      LCT      /ROTATE BIT 0 TO BIT 7
2356 2531 0370      -7-1
2357 2532 0074      ROTATE ZERO
2358 2533 0073      ICT
2359 2534 0124      BR COFL F   /DONE ROTATING?
2360 2535 2532      .-3      /NO
2361

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```

2362 2536 0122      BR SR7 ONE  /YES, WAS THERE A BAD COMPARE
2363 2537 2542      TKSKER     /YES, GO REPORT A TRACK SEEK ERROR
2364
2365 2542 0264      OPEN RTNA  /CORRECT TRACK, EXIT FROM FIND HDR SUBR
2366 2541 0207      JUMP F1 IND
2367
2368
2369
2370
2371 2542 0070      TKSKER,  LCT      /HEADER CRC WAS GOOD BUT TRACK
2372 2543 0150      KTKSKER   /ADDRESS DID NOT COMPARE, MUST
2373 2544 0226      JUMP FS   /EXIT TO ERROR DONE
2374 2545 2610      GOERDN
2375
2376
2377 2546 0070      MRCER,   LCT      /HEADER CRC WAS NOT CORRECT
2378 2547 0140      KMRCER
2379 2550 0075      LSR
2380 2551 0210      OPEN ERREG /LOG THE ERROR
2381 2552 0064      LSP
2382
2383 2553 0226      JUMP FS   /GO TRY ANOTHER HEADER
2384 2554 2557      RADHDR
2385
2386
2387
2388
2389 2555 0170      BDSRT,   BR FLAGO T  /BAD START ON DATA AM OR IDAM?
2390 2556 2577      RADDAM
2391
2392 2557 0230      BADHDR,  OPEN TEMPA  /IDAM, INCREMENT AND TEST BAD START INNER COUNT
2393 2560 0071      ESP
2394 2561 0073      ICT
2395 2562 0275      LSR
2396 2563 0064      LSP
2397 2564 0124      BR COFL F  /NO OVERFLOW, GO TRY ANOTHER HEADER
2398 2565 2615      PTRYAG    /INCREMENT AND TEST BAD START OUTER COUNT
2399 2566 0234      OPEN TEMPB
2400 2567 0071      ESP
2401 2570 0073      ICT
2402 2571 0124      BR COFL F  /NO OVERFLOW, GO TRY AGAIN
2403 2572 2615      PTRYAG    /TOO MANY TRIES FOR A HEADER
2404 2573 0070      XSTRYS,  LCT
2405 2574 0160      KXSTRYS
2406 2575 0226      JUMP FS
2407 2576 2610      GOERDN
2408
2409
2410 2577 0234      RADDAM,  OPEN TEMPB  /BAD START ON DATA AM, INCREMENT AND TEST BAD START COUNT
2411 2600 0071      ESP
2412 2601 0073      ICT
2413 2602 0075      LSR
2414 2603 0064      LSP
2415 2604 0124      BR COFL F
2416 2605 2617      PGETDA    /NO OVERFLOW GO TRY FOR DATA AM AGAIN

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```

2417 2606 0070 NODAH, LCT /TRIED 3 TIMES FOR DATA AM, GO FLAG THE ERROR
2418 2607 0170 KNODAH
2419 2610 0210 GOERDN, OPEN ERREG
2420 2611 0075 LSR
2421 2612 0064 LSP
2422 2613 0212 JUMP F2
2423 2614 1000 ERDONE
2424
2425 2615 0216 PTRYAG, JUMP F3 /POINTER TO FIND AN IDAM
2426 2616 1413 TRYAGN
2427
2428
2429 2617 0216 PGETDA, JUMP F3 /POINTER TO FIND DATA AM
2430 2620 1441 GETDAH
2431
2432
2433
2434 /([ROUTINE: INITIALIZE CONT.])
2435 2621 0070 WRONG, LCT /HOME WAS FOUND WHILE STEPPING OUT
2436 2622 0030 KARONG
2437 2623 0226 JUMP F5
2438 2624 2610 GOERDN
2439
2440 2625 0070 DNRCAL, LCT /CALL CHECK READY SUBROUTINE
2441 2626 1771 PNORDY
2442 2627 0226 JUMP F5
2443 2630 2640 CHKRDY
2444
2445 2631 0070 INTRDY, LCT /DRV 0 IS READY CALL BOOT SUBROUTINE TO
2446 2632 0770 GCREAD /MOVE TO TRACK 1, THEN GO TO READ ROUTINE TO
2447 2633 0274 OPEN RTN /PICK UP SECTOR 1
2448 2634 0075 LSR
2449 2635 0064 LSP
2450 2636 0202 JUMP F0
2451 2637 0252 BOOT
2452
2453
2454
2455

```

```

2456 /([SUBROUTINE: CHECKREADY])
2457
2458 /SUBROUTINE TO CHECK THE SELECTED DRIVE TO SEE IF THE
2459 /DISK IS INSERTED AND UP TO SPEED. THIS IS DONE BY CHECKING TO SEE IF
2460 /THE INTERVAL BETWEEN 2 INDEX PULSES IS BETWEEN 150 MS AND 180 MS. RETURN
2461 /ADDRESS IS PLACED IN THE COUNTER BEFORE ENTRY, NOT READY RETURN IS
2462 /TO THE RETURN ADDRESS. READY RETURN IS TO THE RETURN ADDRESS PLUS 2
2463
2464
2465
2466
2467 2642 0274 CHKRDY, OPEN RTN /SAVE RETURN ADDRESS
2468 2641 0075 LSR
2469 2642 0064 LSP
2470
2471 2643 0070 LCT /2 TO CNTR FOR INDEX PASS COUNT
2472 2644 0375 -2-1
2473
2474 2645 0230 OPEN TEMPA /FOR INDEX PASS COUNT
2475
2476 2646 0075 NEWPAS, LSR /RESTORE INDEX PASS COUNT
2477 2647 0064 LSP
2478
2479 2650 0061 FLAG OFF /CLOSE INDEX WINDOW
2480
2481 2651 0042 LDMD /TO CLEAR INDEX FLOP
2482
2483 2652 0070 LCT /FOR 15 TIMES THROUGH 10MS LOOP
2484 2653 0360 -15-1
2485
2486 2654 0234 STDLY, OPEN TEMPB /RESTORE OUTER COUNT
2487 2655 0075 LSR
2488 2656 0064 LSP
2489
2490 2657 0070 LCT /FOR 40 TIMES THROUGH .25MS LOOP
2491 2660 0327 -40-1
2492
2493 2661 0240 OPEN TEMPC
2494 2662 0075 SPBACK, LSR /RESTORE INNER COUNT
2495 2663 0064 LSP
2496
2497 2664 0070 LCT /WAIT .25 MS FOR INDEX
2498 2665 0005 -250-1
2499 2666 0116 BR INDX T
2500 2667 2714 SA=IND /FOUND INDEX
2501 2670 0073 ICT
2502 2671 0124 BR COFL F
2503 2672 2666 ,=4
2504
2505 2673 0240 OPEN TEMPC /INCREMENT AND TEST INNER COUNT
2506 2674 0071 ESP
2507 2675 0073 ICT
2508 2676 0124 BR COFL F
2509 2677 2662 SPBACK
2510

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2511 2700 0234 OPEN TEMPB /INCREMENT AND TEST OUTER COUNT
2512 2701 0071 ESP
2513 2702 0073 ICT
2514 2703 0124 BR COFL F
2515 2704 2655 STDLY+1
2516
2517 2705 0176 BR FLAGO ONE /WAS INDEX WINDOW OPEN?
2518 2706 2767 UNRDY /YES, NO INDEX WITHIN 100MS
2519
2520 2707 0062 FLAG ON /NO, OPEN WINDOW
2521
2522 2710 0070 LCT /FOR 3 TIMES THROUGH 10 MS LOOP
2523 2711 0374 -3-1 /THE WINDOW IS 30 MS WIDE
2524
2525 2712 0226 JUMP F5 /GO LOOK FOR INDEX
2526 2713 2654 STDLY
2527
2528
2529 2714 0230 SAWIND, OPEN TEMPB /INCREMENT AND TEST INDEX PASS COUNT
2530 2715 0071 ESP
2531 2716 0073 ICT
2532 2717 0124 BR COFL F
2533 2720 2646 NEWPAS /THIS WAS 1ST INDEX, GO LOOK FOR SECOND
2534
2535 2721 0174 BR FLAGO ZERO /THIS WAS 2ND INDEX, WAS THE WINDOW OPEN?
2536 2722 2767 UNRDY /NO, INDEX OCCURRED TOO SOON
2537
2538 2723 0274 OPEN RTN /YES, INDEX OCCURRED BETWEEN 150 AND 180 MS, INCREMENT
2539 2724 0071 ESP /RETURN ADDRESS BY 2
2540 2725 0073 ICT
2541 2726 0073 ICT
2542 2727 0075 LSR
2543 2730 0064 LSP
2544
2545 2731 0214 OPEN STAT /SET DRV RDY BIT OF STAT IN SR
2546 2732 0071 ESP
2547 2733 0075 LSR
2548
2549 2734 0076 ROTATE ONE
2550
2551 2735 0061 FLAG OFF /FLAG OFF TO INDICATE FIRST PASS
2552
2553 2736 0070 ROT3, LCT /END AROUND SHIFT OF THE NEXT 3 BITS OF STAT IN SR
2554 2737 0374 -3-1
2555 2740 0122 BR SR7 T
2556 2741 2745 +4
2557 2742 0074 ROTATE ZERO
2558 2743 0226 JUMP F5
2559 2744 2746 +2
2560 2745 0076 ROTATE ONE
2561 2746 0073 ICT
2562 2747 0124 BR COFL F
2563 2750 2740 -8
2564
2565 2751 0176 BR FLAGO T /WAS IT FIRST 3 OR LAST 3

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2566 2752 2764 EXCHRY /LAST, GO EXIT
2567
2568 2753 0140 BR WRTE F /UPDATE WRITE PROTECT BIT OF STAT IN SR
2569 2754 2760 +4
2570 2755 0074 ROTATE ZERO
2571 2756 0226 JUMP F5
2572 2757 2761 +2
2573 2760 0076 ROTATE ONE
2574
2575 2761 0062 FLAG ON /GO SHIFT AROUND LAST 3 BITS
2576 2762 0226 JUMP F5
2577 2763 2736 ROT3
2578
2579 2764 0064 EXCHRY, LSP /RESTORE THE STAT
2580
2581 2765 0274 OPEN RTN /RETURN FROM CHKRDY SUBROUTINE
2582 2766 0217 JUMP F3 IND
2583
2584 2767 0214 UNRDY, OPEN STAT /CLEAN DRV READY BIT OF STAT IN SR
2585 2770 0071 ESP
2586 2771 0075 LSR
2587 2772 0074 ROTATE ZERO
2588
2589 2773 0226 JUMP F5 /GO UPDATE REST OF STAT IN SR
2590 2774 2735 ROT3-1
2591
2592 2775 0000 2 /OPEN
2593 2776 0000 0 /OPEN
2594 2777 0000 0 /OPEN
2595
2596
2597

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14

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0900 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

0200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

0400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

0600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
0700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

1000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

1200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

1400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

1600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
1700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

2000 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2100 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

2200 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2300 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

2400 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2500 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

2600 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111
2700 11111111 11111111 11111111 11111111 11111111 11111111 11111111 11111111

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3000
3100

3200
3300

3400
3500

3600
3700

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4000
4100

4200
4300

4400
4500

4600
4700

5000
5100

5200
5300

5400
5500

5600
5700

6000
6100

6200
6300

6400
6500

6600
6700

7000
7100

7200
7300

7400
7500

7600
7700

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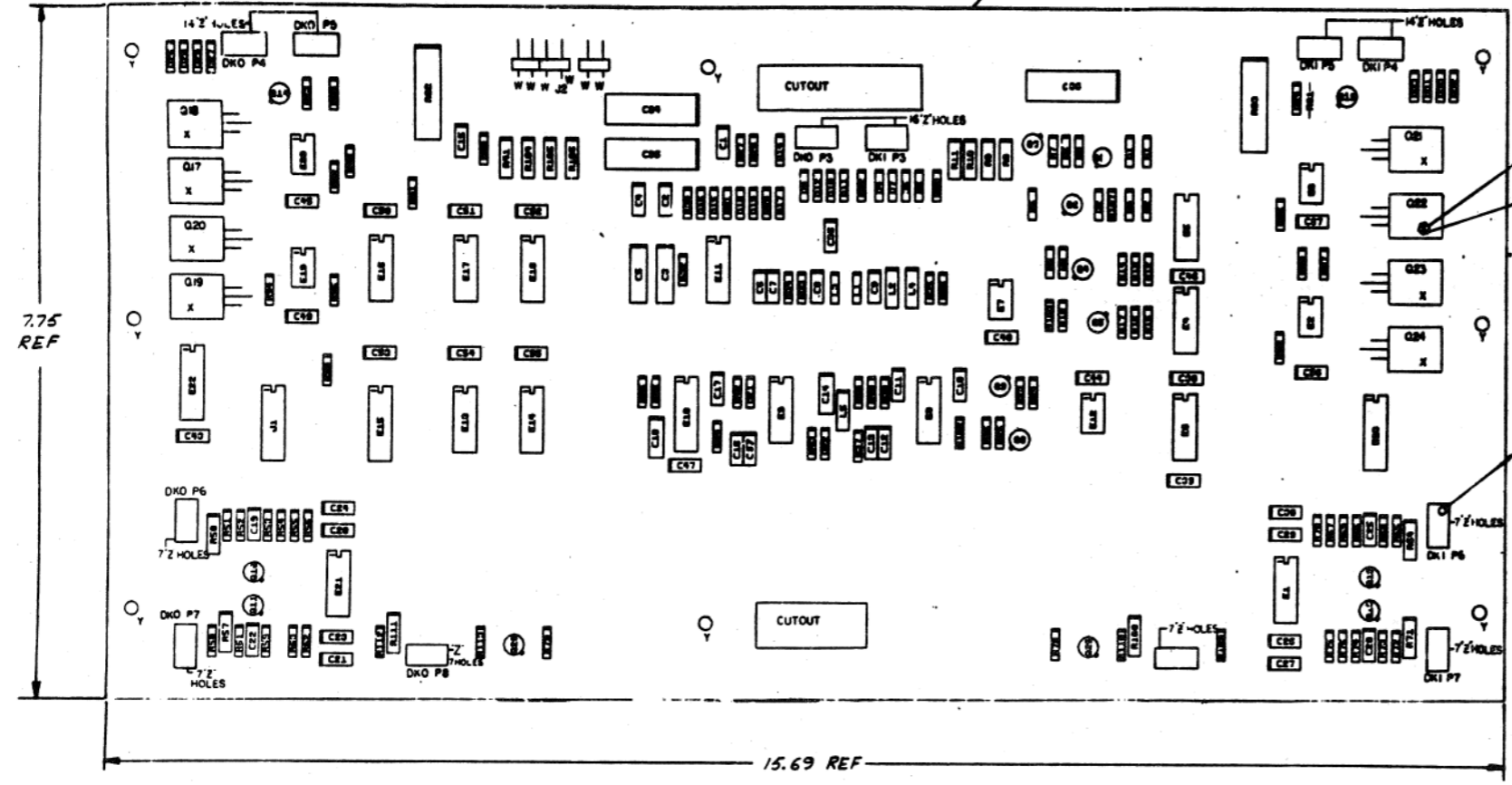
A	0562	ERTRK	0242	PFUNCT	0370	WHCHDR	0075
ABACK	0535	EXCHRY	2764	PGETDA	2617	WRONG	2621
ABV43	0344	FILL1	1175	PGOTIT	1346	WRT08	1322
AGAIN	0531	FILLBU	1110	PNORDY	1771	WRTCRC	0624
AGAIN1	0550	FINDHD	1400	PNTRDY	1765	WRTDAM	0514
AGAIN2	0722	FINDSE	0714	PRDSEC	1105	WRTDAT	0566
AGAIN3	1576	FINDTR	0103	PRTRER	0503	WRTPST	0656
AGAIN4	1616	FUNCT	1036	PTRYAG	2615	WRTSEC	0400
AGAIN5	1635	FUNCT2	1057	PUTSEC	0145	XFRQ	1131
AGAIN6	1653	FUNCT4	1066	PUTTRK	0166	XSTRY8	2573
B	0564	FUNCT6	1076	PYSRDY	1767		
BACK	2322	GETCMD	2001	RCALOK	0060		
BADDAM	2577	GETCRC	2221	RDEREG	1275		
BADHDR	2557	GETDAM	1441	RDSEC	0760		
BADSRT	1673	GETWRD	2000	RSTAT	1224		
BBACK	0554	GLESSF	2432	READ	2167		
BDSRT	2555	GODONE	0712	READOK	0706		
BOOT	0252	GODUN	1272	RECALP	0035		
BYTEOU	1152	GOERDN	2610	RECAL1	0034		
C	0615	GOREAD	0770	RFINTR	0355		
CBACK	0576	GOTIT	2010	ROT	1251		
CEGATE	0676	GOTONE	2030	ROT3	2736		
CFINSE	0351	GOTRUN	2347	SAWIND	2714		
CHKPAR	2041	GOTWRD	2076	SECHLF	0543		
CHKRDY	2640	HCR CER	2546	SECPLS	2124		
CHKSEC	0730	HDRCOM	1571	SELFER	0620		
CKHCRC	2515	HCSETL	0322	SPBACK	2662		
CKHOME	2105	HLFDLY	0466	STASH	0437		
CLRID	1243	HOMERR	2456	STDLY	2654		
CGATE	0666	ILTRK	0206	STDONE	1031		
D	0653	IN10	0045	STEPHD	2100		
DAM	1675	INTER1	1374	STPOUT	0275		
DAMSUP	0460	INTRDY	2631	SWGATF	0407		
DATA	2206	LOOP	1326	TEST	2352		
DATAA	0571	MAGCOM	2400	TEST1	1351		
DBACK	0646	MOREDS	1421	TEST2	1350		
DCRCER	2304	NEWORD	1141	TESTDN	1372		
DELAY	1300	NEWPAS	2646	TIMERP	1667		
DELCA1	1777	NEXTG	2421	TKSKER	2542		
DIF	2462	NOOAM	2606	TRKEG	0246		
DIFA	2503	NOSTPS	0357	TRYAGN	1413		
DIFR	2501	NOYET	1755	TSTAGN	1353		
DLY25	2145	NOZERO	1746	TSTG0	2443		
DMCAL	2625	NOTHER	2034	TSTRTN	0004		
DMOULY	2145	NOXDRV	0064	UDIF	0134		
DMSTP	2135	NOXDRV1	0270	UNRDY	2767		
DMSTP	0305	NOXDR	0737	UONE	0120		
E	0627	NOXIDAM	1761	USAME	0141		
EMPTV1	1210	NOXPRAM	1751	UZERO	0127		
EMPTVH	1107	NOXONE	1006	WAIT	0743		
ENDDAM	1742	OUT	2150	WAITRV	2312		
ENDONE	1120	PDRCL	0372	WATDAT	2021		

ERRORS DETECTED: 0
 LINKS GENERATED: 0
 RUN-TIME: 18 SECONDS
 3K CORE USED

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NOTES:

1. UNLESS OTHERWISE SPECIFIED:
A ALL RESISTORS ARE 1/4W, 25%.
2. WASHER TO BE USED BETWEEN ITEMS 57 AND 58 WILL BE SUPPLIED WITH THE 049CB TRANSISTOR ONLY BY G.E. THE WASHER IS ONLY REQUIRED WHEN USING THE G.E. TYPE TRANSISTOR.
- * 3. FOR TEST SEE NOTE ON PAGE 3 OF D-CB-M7727
4. DEC PART # 13-01668 MAY BE USED FOR INSERTION IF 13-01320 IS NOT AVAILABLE.
5. RES. REV. MAY ALSO BE CHANGED AT SYSTEM TEST.



IC TYPE	QTY	LOC
7473	11	4
7545	4	8
74157	0	16
7545c	4	3
74129	8	6
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTS ARE STATED ABOVE

IC PIN LOCATIONS

REV	DATE	BY	CHK	APP
1	3-21-77	H. DUBAB		
2	17 APR 77	D. ZWICKER		
3	17 APR 77	D. C. M7727-00003		
4	17 APR 77	W. SMITH		
5	17 APR 77	M7727-00002		
6	17 APR 77	C. YOUSE		
7	17 APR 77	M7727-00001		
8	17 APR 77	M. CHANGE NO.		

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
	M7727	ETCH BOARD REV. B		
PARTS LIST				
digital				
TITLE READ/WRITE CONTROL				
SIZE CODE NUMBER DCS M7727-0-1				
REV. E				
SCALE SHEET 1 OF 6				

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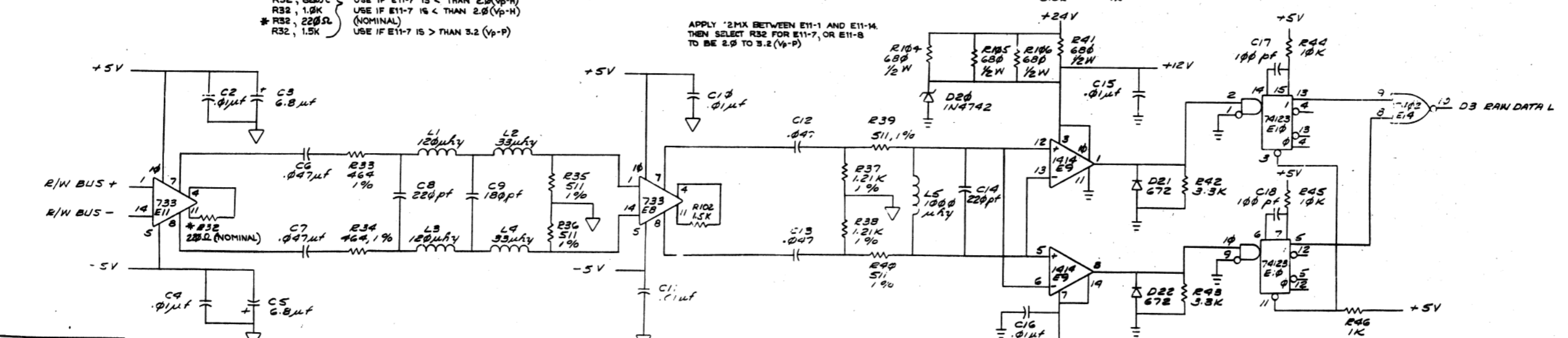
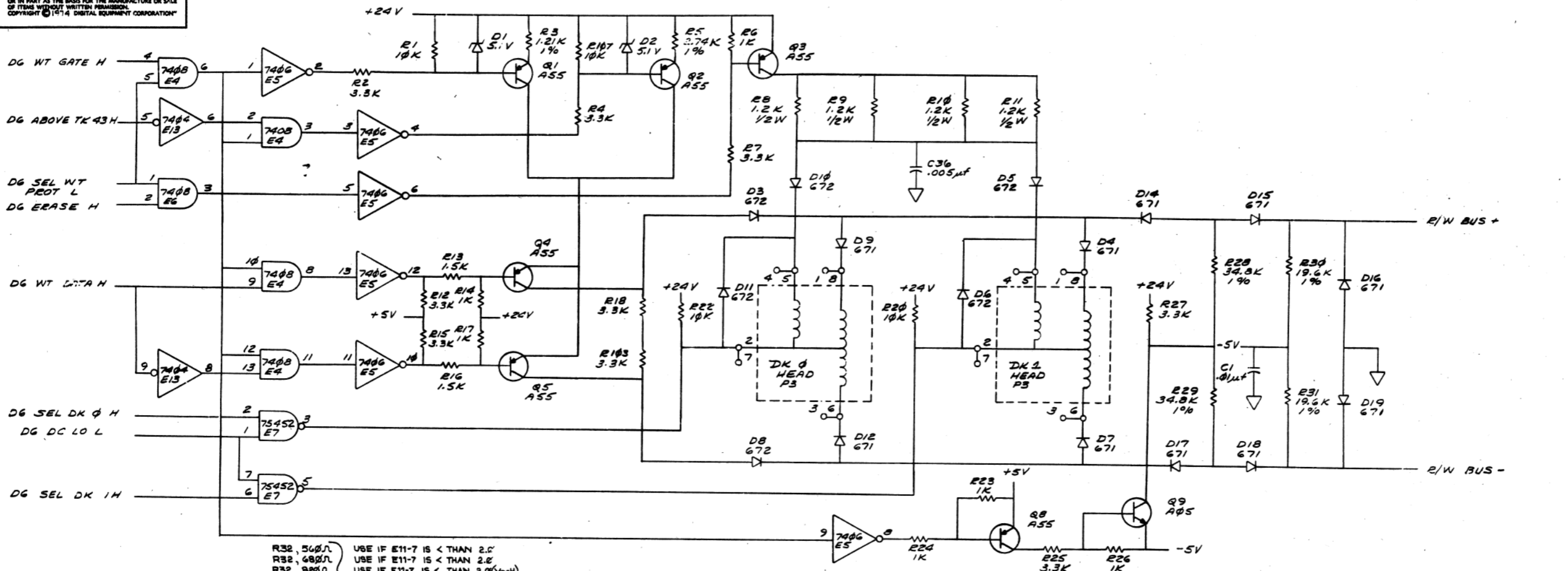
PARTS LIST				
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
		X-Y COORDINATE HOLE LOCATION	K-CO-M7727-0-4	1
		ASSY/ DRILL HOLE LAYOUT	D-AH-M7727-0-5	2
		MODULE ECO HISTORY	B-MH-M7727-0-6	3
1		ETCHED CIRCUIT BOARD	D-1A-501370-00	4
2	C17, C18	CAP 100 pf	1000016-00	5
	C9	CAP 180 pf	1000020-00	6
2	C8, C14	CAP 220 pf	1000021-00	7
32	C1, C2, C4, C10, C11, C15 C16, C20, C21, C23, C24 C26, C27, C29, C30, C37, C38, C39, C40, C43 C44, C45, C46, C47 C49 - C57	CAP .01 μf	1001610-00	8
2	C3, C5	CAP 6.8 μf 35V	1005306-00	9
2	C34, C35	CAP 190 μf	1009433-00	10
1	C33	CAP 50 μf	1000080-00	11
4	C7, C6, C12, C13	CAP .047 μf	1010978-32	12
5	C19, C25, C22, C28, C36	CAP .005 μf	1001765-00	13
10	D4, D7, D9, D12, D14 D15, D16, D17, D18, D19	DIODE D671	1103309-00	14
8	D3, D5, D6 D8 D10 D11, D21, D22	DIODE D672	1105275-00	15
10	D23, D24, D26, D27 D28, D29, D30, D31 D32, D33	DIODE 1N4004	1105796-00	16
1	D20	DIODE 1N4742 12V	1109502-00	17
2	D1, D2	DIODE 5.1V	1110713-00	18
9	R90, R92 - R99	RES 150 1/4W 5%	1300250-00	19
4	R41, R104, R105, R106	RES 680 1/2W 5%	1300347-00	20
12	R6, R14, R17, R23, R24, R26, R46 R78, R79, R80, R81 R91,	RES 1K 1/4W 5%	1300365-00	21
4	R8 - R11	RES 1.2K 1/2W 5%	1300385-00	22
6	R30, R57, R64, R71, R86, R111	RES 68 1/2W 5%	1309405-00	23
7	R13, R16, R53, R62 R68, R75, R102	RES 1.5K 1/4W 5%	1300391-00	24
4	R35, R36, R39, R40	RES 511 1/8W 1%	1302411-00	25
1	R5	RES 2.74K 1/8W 1%	1304868-00	26
11	R2, R4, R7, R12, R15 R18, R20, R25, R27 R42, R43	RES 3.3K 1/4W 5%	1300439-00	27
6	R1, R20, R22, R44 R45, R107	RES 10K 1/4W 5%	1300479-00	28
11	R3, R37, R38, R52 R58, R63, R66, R72 R76, R109 R112	RES 1.21K 1/8W 1%	1302871-00	29
1	R32	RES 220 Ω ±5%, 1/4W	1300271-00	30
2	R33, R34	RES 464 1/8W 1%	1303047-00	31
2	R28, R29	RES 34.8K 1/8W 1%	1303156-00	32
4	R51, R61, R65, R73	RES 10K 1/8W 1%	1303312-00	33
2	R82, R83	RES 100 5W 5%	1309094-00	34
2	R30, R31	RES 19.6K 1/8W 1%	1309419-00	35
6	R55, R59, R67, R74 R110, R113	RES 4.64K 1/4W 1%	1304856-00	36

REVISIONS		
CHK	CHANGE NO	REV

PARTS LIST				
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM
1	L5	CHOKE 1000 MHY	1602723-00	37
2	L2, L4	CHOKE 33 MHY	1601759-00	38
2	L1, L3	CHOKE 120 MHY	1610663-00	39
1	E17	I.C. 7450	1905580-00	40
2	E16, E18	I.C. 7473	1905587-00	41
1	E14	I.C. 7402	1909004-00	42
1	E13	I.C. 7404	1909686-00	43
2	E4, E6	I.C. 7408	1910155-00	44
3	E1, E9, E21	I.C. 1414	1910337-00	45
3	E2, E3, E12, E19, E20	I.C. 75451	1910406-00	46
1	E10	I.C. 74123	1910436-00	47
2	E8, E11	I.C. 72733	1910644-00	48
1	E15	I.C. 74157	1910655-00	49
1	E5	I.C. 7406	1910741-00	50
1	J1	I.C. SOCKET 16 PIN	1211813-02	51
9	Q9 THRU Q15, Q25 Q26	TRANS MXA05	1510705-00	52
6	Q1 - Q5, Q8	TRANS MXA05	1510706-00	53
8	Q17 - Q24	TRANS D44CB	1510421-00	54
86	"Z" HOLES	WIRE WRAP PIN	1210385-01	55
3	J2	CONN 2 POS	1212204-00	56
8	"X" HOLES	SCREW, PAN HD 4/40 X 5/16	9006010-01	57
8	"X" HOLES	NUT, KRP 4/40 X 1/4 X 3/32	9006557-00	58
1	E7	I.C. 75452	1910645-00	59
4	R54, R56, R69, R70	RES 14.7K 1/4W 1%	1302941-00	60

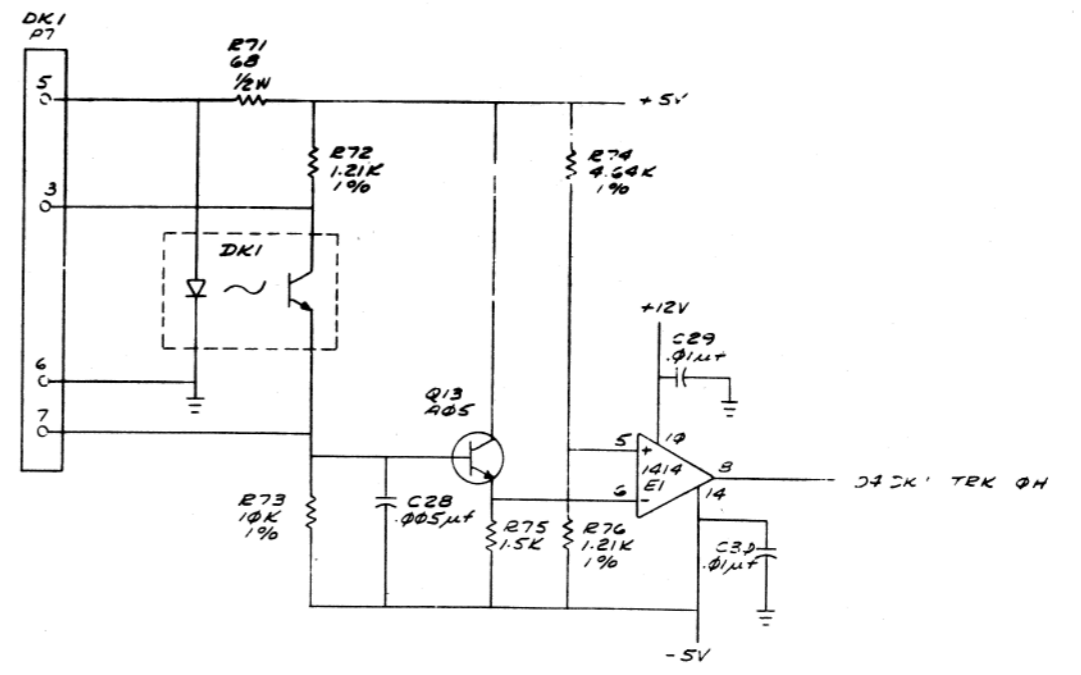
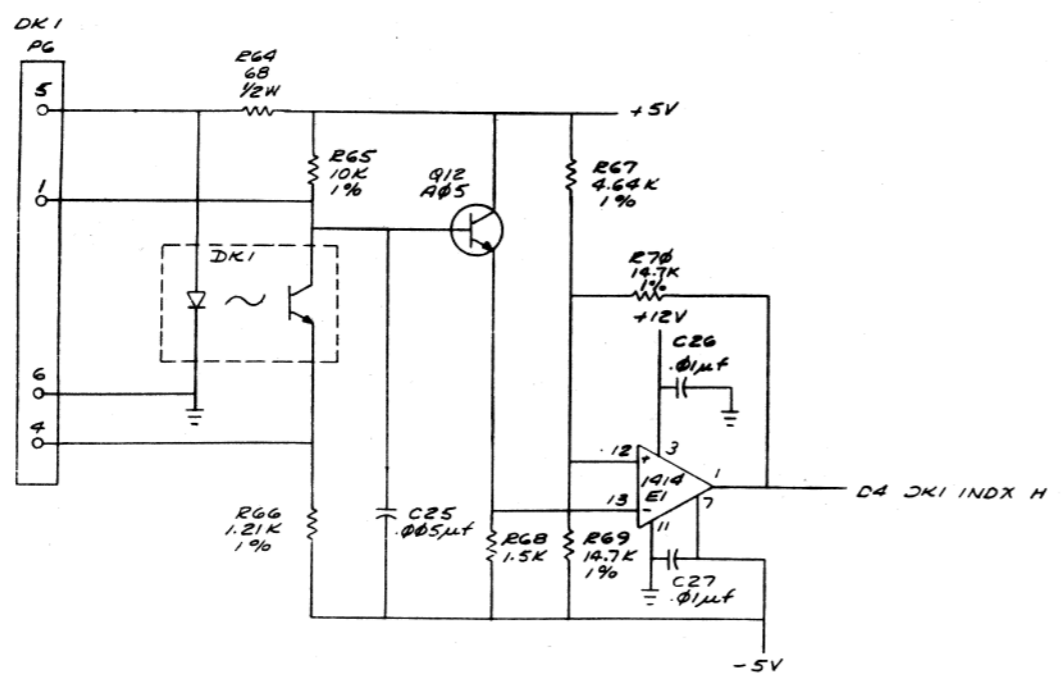
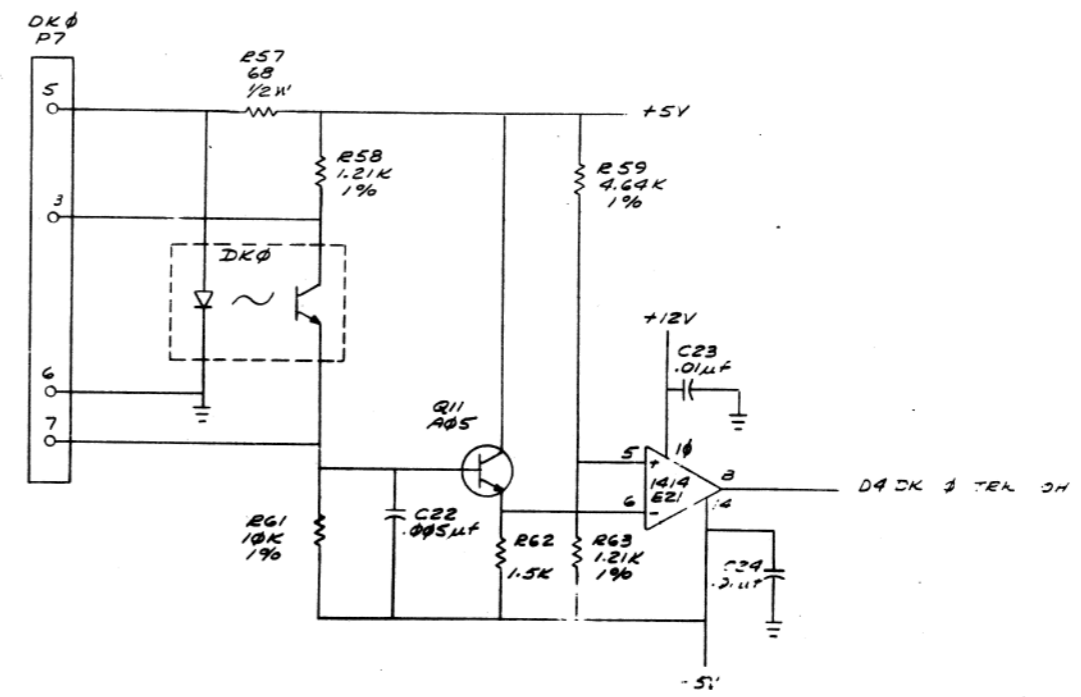
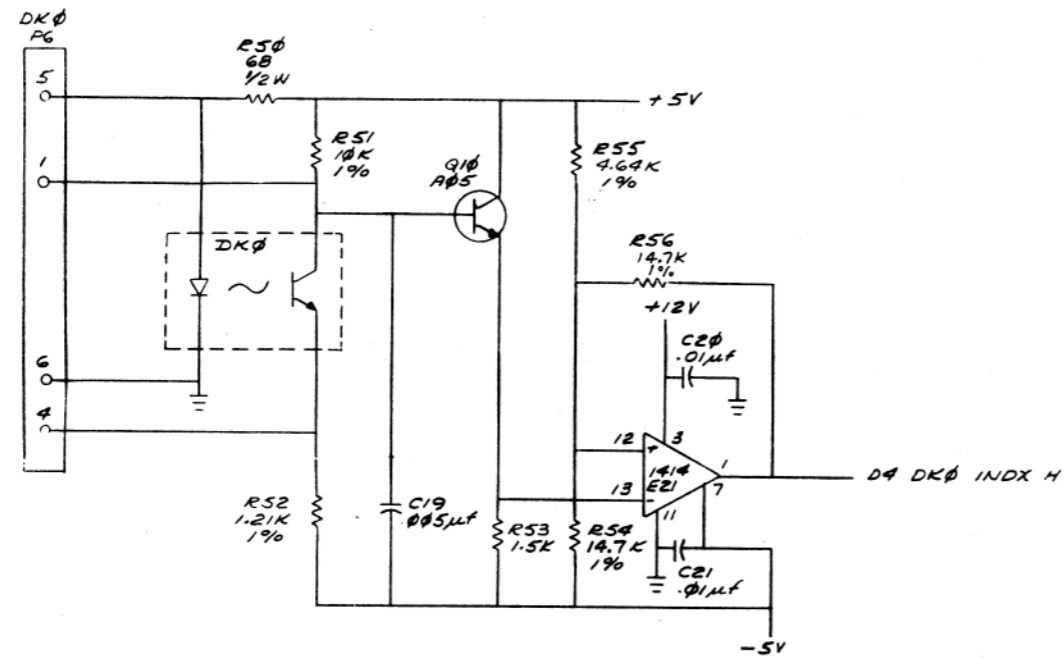
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D E S M 7727-0-1 E



REVISIONS	
CHK	REV.

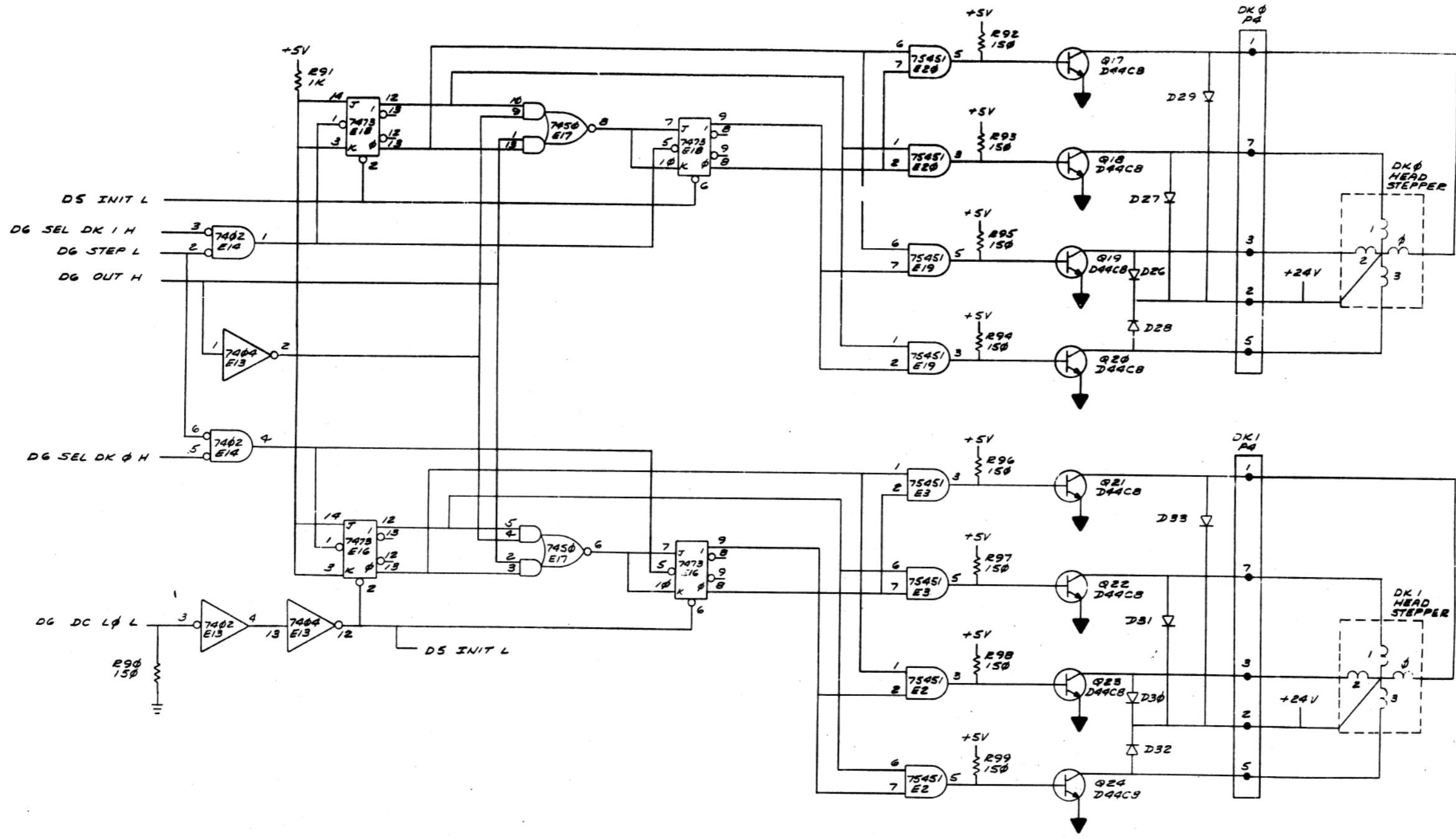
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CHK	CHANGE NO.	REV.

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3 1-777-0-1 DCS M7727-0-1 2 1



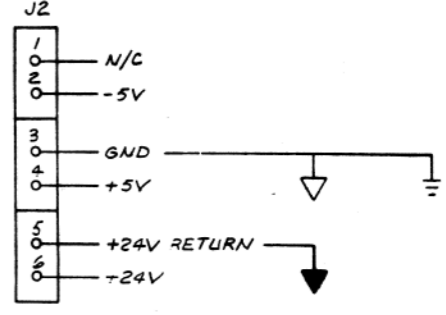
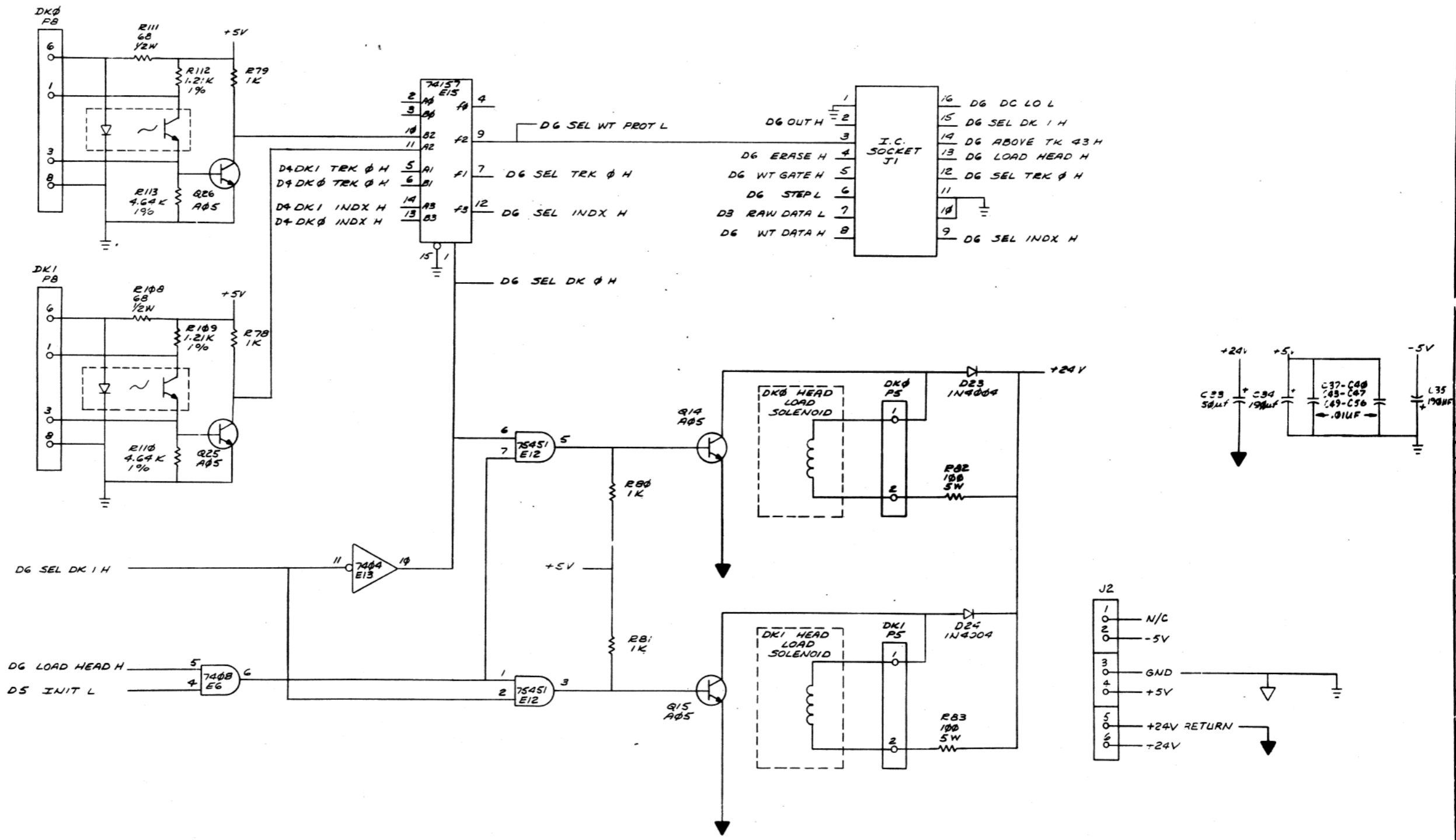
REVISIONS		
HK	CHANGE NO.	REV.

TITLE	READ / WRITE CONTROL (D5)	SIZE CODE	DCS	NUMBER	M7727-0-1	REV.	E
SCALE		SHEET	5	OF	6	DIST.	

48

8 7 6 5 4 3 2 1

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REVISIONS		
HK	CHANGE NO	REV.

TITLE	READ / WRITE CONTROL (D6)	SIZE CODE	D CS	NUMBER	M7727-2-1	REV.	E
SCALE		SHEET	6	OF		DIST.	

1

H771 POWER SUPPLY
UNIT ASSY
E-UA-H771- ϕ - ϕ

2

RX ϕ 1 POWER BOARD
ASSY
D-AD-7010718-0-0

TITLE	SHEET 2 OF 3	SIZE CODE	NUMBER	REV
H771 POWER SUPPLY		B DD	H771- ϕ	E

CUSTOMER PRINT SET		MECHANICAL					CUSTOMER PRINT SET		ELECTRICAL						
	MFG. SET	FIG. NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE		MFG. SET	FIG. NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
		1	E-UA-H771- β - β	E	2	H771 POWER SUPPLY ASSY		X		1	B-DD-H771- β	E	3	H771 POWER SUPPLY	
			E-MD-7412667-0-0	D	1	CHASSIS, POWER SUPPLY		X			D-CS-H771-A-1	B	1	H771-A CIRCUIT SCHEMATIC	
			D-AD-7010680-0-0	C	1	TRANSFORMER ASSY, 6 ϕ HZ		X			D-CS-H771-C-1	C	1	H771-C CIRCUIT SCHEMATIC	
			D-AD-7010704-0-0	E	1	TRANSFORMER ASSY, 5 ϕ HZ		X			D-CS-H771-D-1	C	1	H771-D CIRCUIT SCHEMATIC	
			C-AD-7010697-0-0	B	1	POWER CORD ASSY					A-SP-H771- β -1			ENGINEERING SPECIFICATION	
			C-IA-7010972-0-0	C	1	JUMPER									
			C-MD-7413344-0-0		1	BRACKET, FUSE MOUNTING									
			A-DC-7413403-0-0		1	DECAL, H771-A									
			A-DC-7414250-0-0	A	1	DECAL, H771-C									
			A-DC-7414251-0-0	A	1	DECAL, H771-D									
		2	D-AD-7010718-0-0		1	RX ϕ 1 POWER BOARD ASSY				2	D-AD-7010718-0-0	*	1	RX ϕ 1 POWER BOARD ASSY	
			D-IA-7010854-0-0	C	1	READ/WRITE BOARD HARNESS		X			D-CS-5411398-0-1	*	1	RX ϕ 1 POWER BOARD ASSY	
			D-IA-7010853-0-0	B	1	DISK CONTROL BOARD HARNESS		X							

CUSTOMER PRINT SET CODES
 X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
 C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
 S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE

H771 POWER SUPPLY

SIZE CODE

B DD

NUMBER

H771- β

REV

E

SHEET 3 OF 3

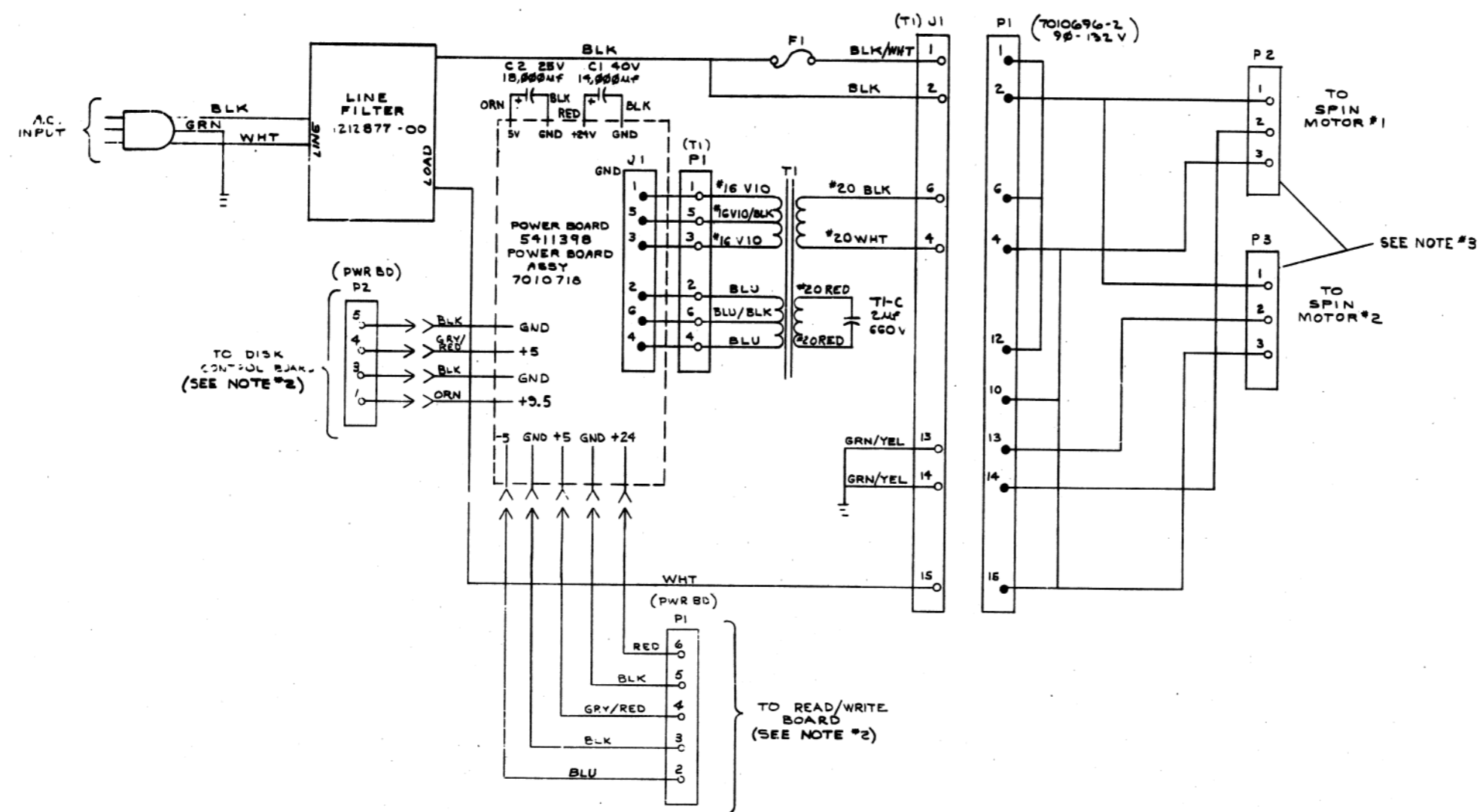
DRB 108

DEC 16-(325)-1062-2B-R972

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DIGITAL H771-A-1 2

- NOTES:
1. ALL WIRE TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.
 2. SLOT BETWEEN P1-4 + P1-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 + P2-5 ALSO CONTAINS A DUMMY PIN.
 3. NO DOUBLE CRIMPS ARE ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).



REV.	DATE	BY	CHK
1	1/22/75	WFM	WFM
2	2/10/75	WFM	WFM
3	3-18-75	WFM	WFM
4	3-18-75	WFM	WFM

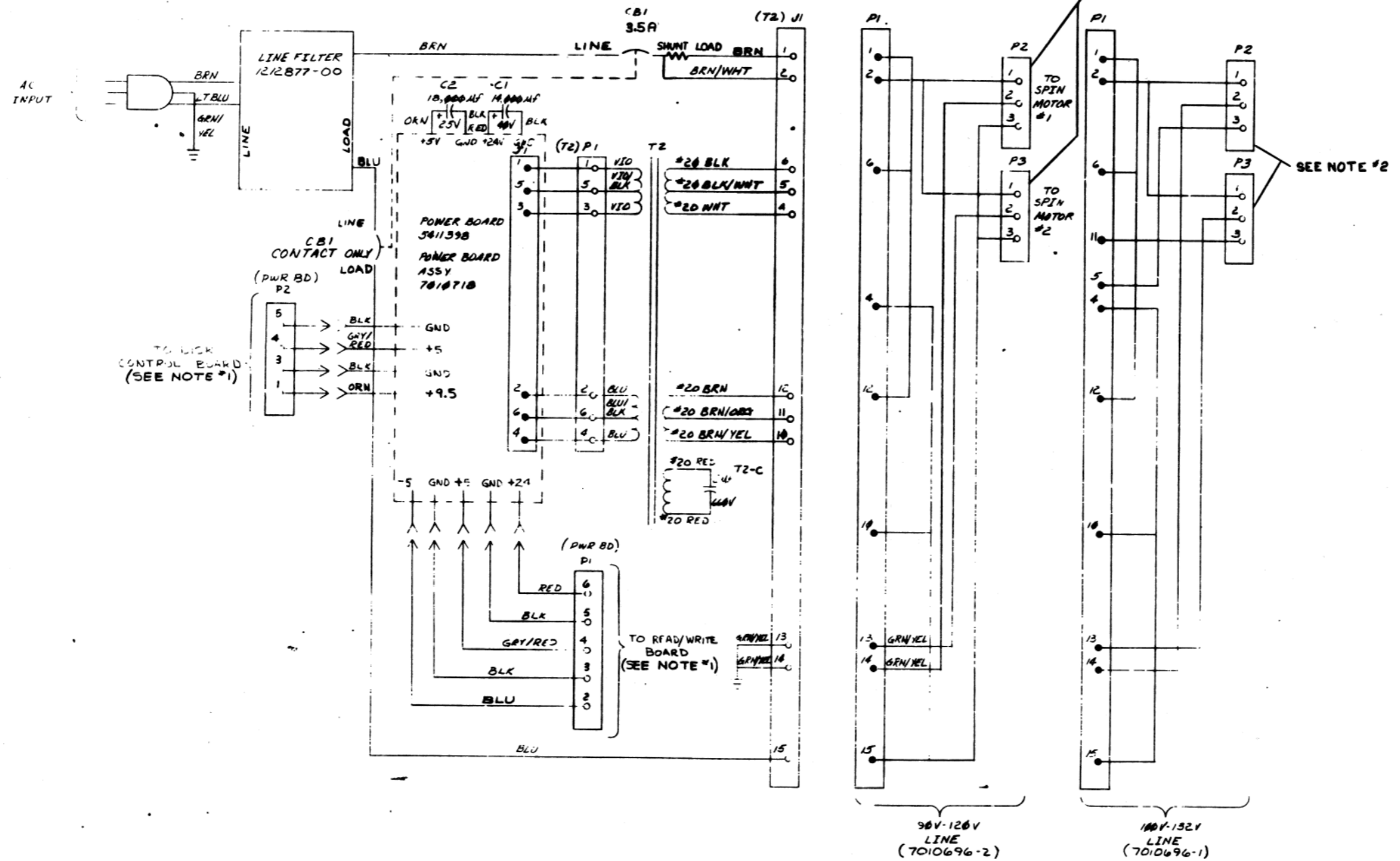
DRN. P.L. Moore	1/22/75	FIRST USED ON	R/O1
CHK'D WFM	2/10/75	TITLE	H771A POWER CONNECTIONS
ENG. B. J. Moore	3-18-75	SCALE	NONE
PROJ. ENG. WFM	3-18-75	SIZE	D CS
PROD. WFM	3/18/75	NUMBER	H771-A-1
NEXT HIGHER ASSY.		REV.	B
B-DD--771-0		SHEET	1 OF 1

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2 015 H771-B-1

NOTES:

- 1 SLOT BETWEEN PI-4 AND PI-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
- 2 NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTOR(S) TO MOTOR(S).
- 3 ALL WIRES TO BE #18 AWG UNLESS OTHERWISE SPECIFIED.

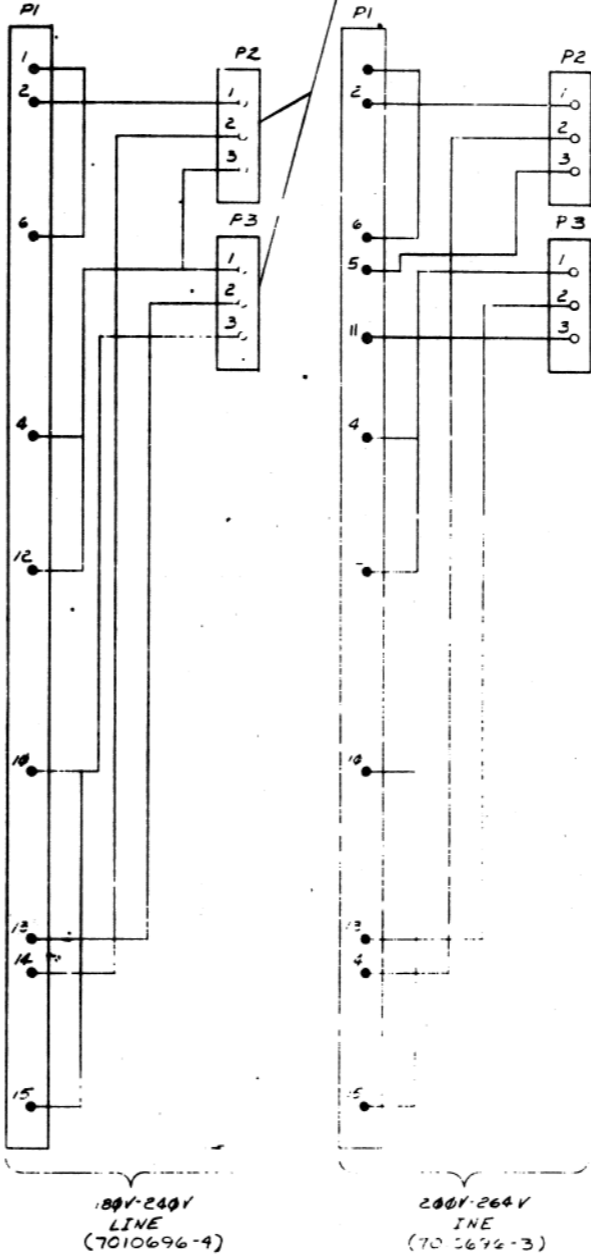
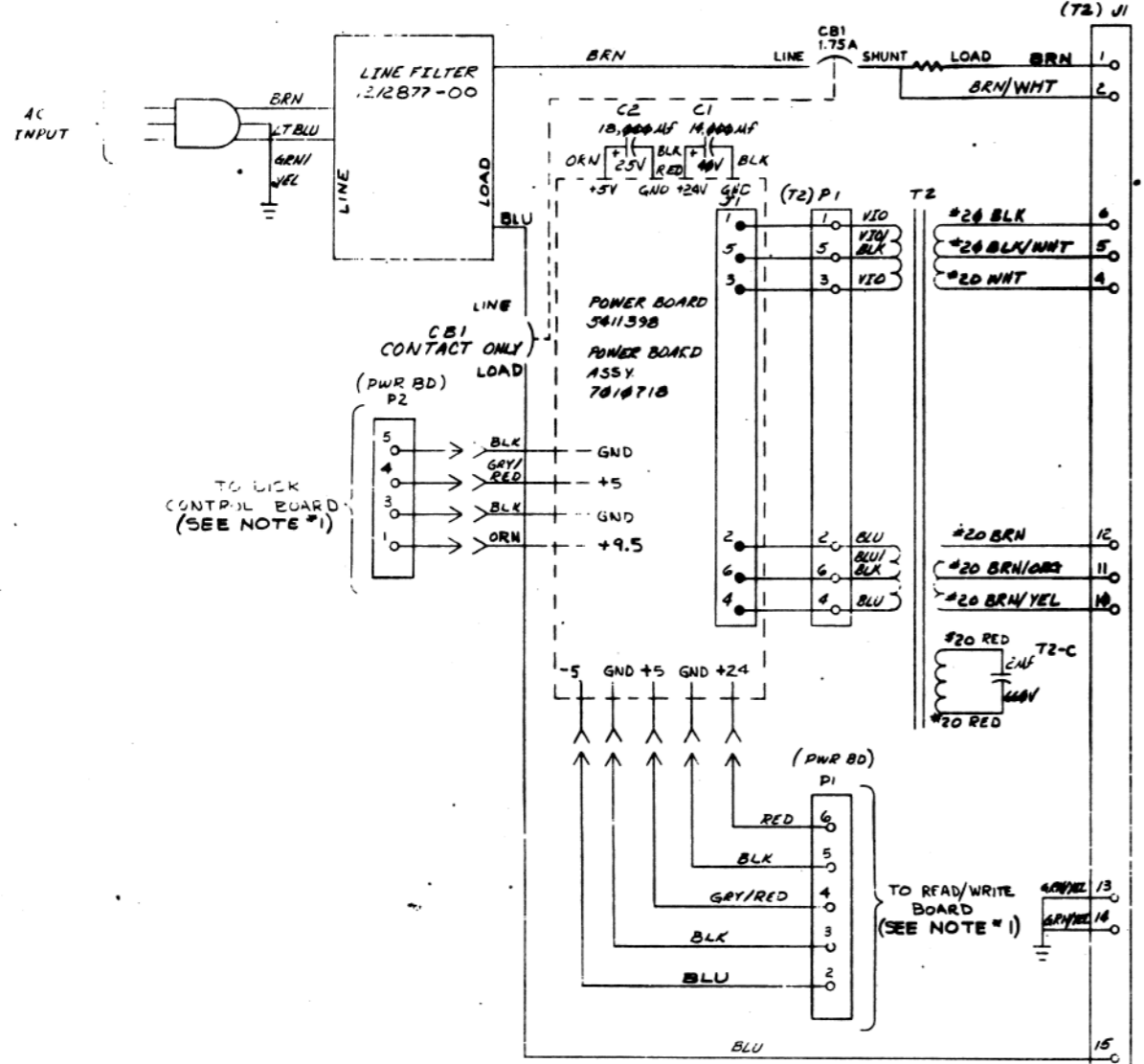


REV.	DATE	BY	CHK	DESCRIPTION
1	11-11-75	B. HAZEN	B. HAZEN	ISSUED FOR MANUFACTURE
2	12-11-75	B. HAZEN	B. HAZEN	REVISION
3	01-14-76	B. HAZEN	B. HAZEN	REVISION
4	02-11-76	B. HAZEN	B. HAZEN	REVISION
5	03-11-76	B. HAZEN	B. HAZEN	REVISION
6	04-11-76	B. HAZEN	B. HAZEN	REVISION
7	05-11-76	B. HAZEN	B. HAZEN	REVISION
8	06-11-76	B. HAZEN	B. HAZEN	REVISION

DRN: 01	FIRST USED ON: RX0
CHK: 6 REN. 0 8 5 1	TITLE: H771-C POWER CONNECTIONS
ENG: 0 0 0 0 0 0 0 0	PROJ. ENG: 0 0 0 0 0 0 0 0
PROD: 0 0 0 0 0 0 0 0	NEXT HIGHER ASSY: 0 0 0 0 0 0 0 0
B-DD-H771-0	SIZE CODE: D CS
SCALE: 1 OF 1	DIST: 0 0 0 0 0 0 0 0

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- NOTES:
1. SLOT BETWEEN PI-4 AND PI-5 CONTAINS A DUMMY PIN. SLOT BETWEEN P2-4 AND P2-5 ALSO CONTAINS A DUMMY PIN.
 2. NO DOUBLE CRIMPS ALLOWED IN MOLEX CONNECTORS TO MOTOR(S).
 3. ALL WIRES TO BE #18AWG UNLESS OTHERWISE SPECIFIED.



SEE NOTE #2

SEE NOTE #2

180V-240V LINE (7010696-4)

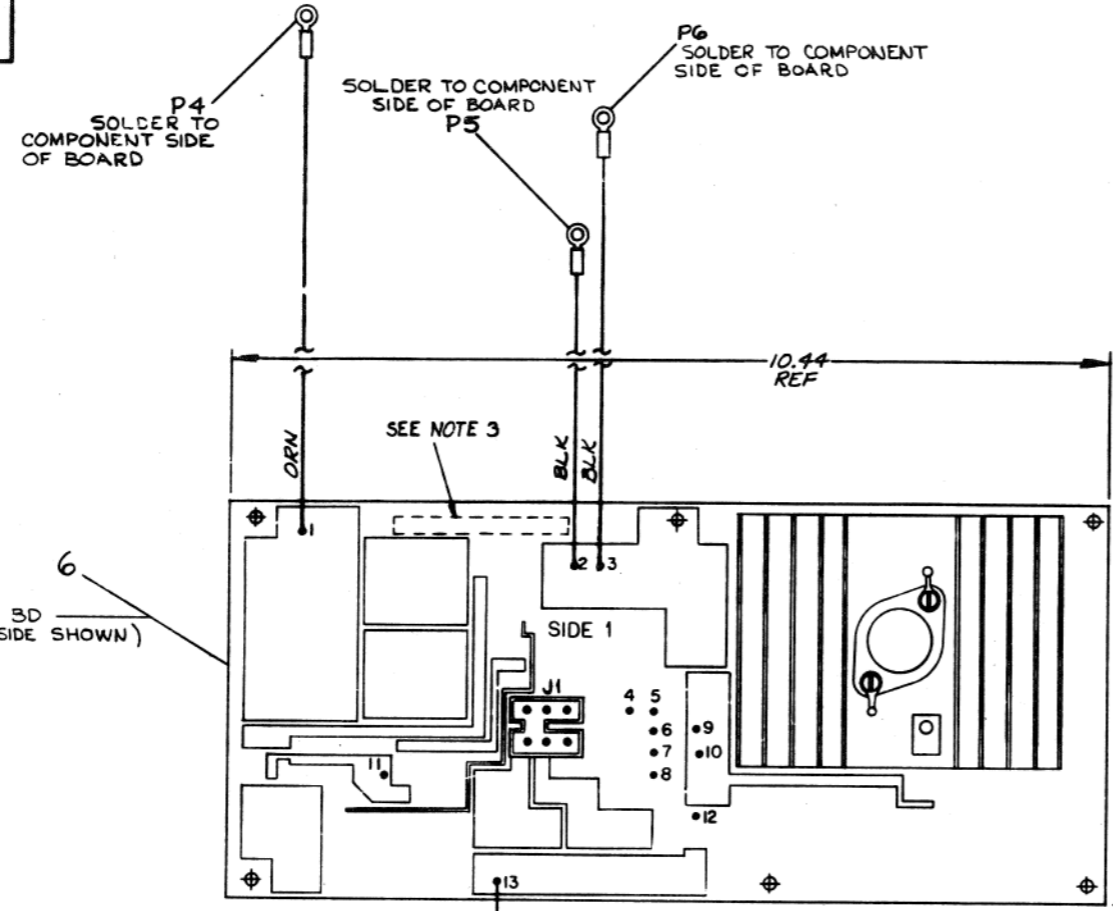
200V-264V LINE (7010696-3)

REV.	DATE	BY	CHKD.	DESCRIPTION
1	11-11-75	B. HAZEN		ORIGINATED
2	11-11-75	B. HAZEN		REVISED
3	11-11-75	B. HAZEN		REVISED
4	11-11-75	B. HAZEN		REVISED
5	11-11-75	B. HAZEN		REVISED
6	11-11-75	B. HAZEN		REVISED
7	11-11-75	B. HAZEN		REVISED
8	11-11-75	B. HAZEN		REVISED

DRN	2	FIRST USED ON	RX0
CHKD.	25	TITLE	H771-D POWER CONNECTIONS
ENG.	25	PROJ. ENG.	
PROD.		NEXT HIGHER ASSY	
B-DD-H771-0	SIZE	CODE	NUMBER
SCALE	D	CS	H771-D-1
SHEET	1	OF	1
DIST.			

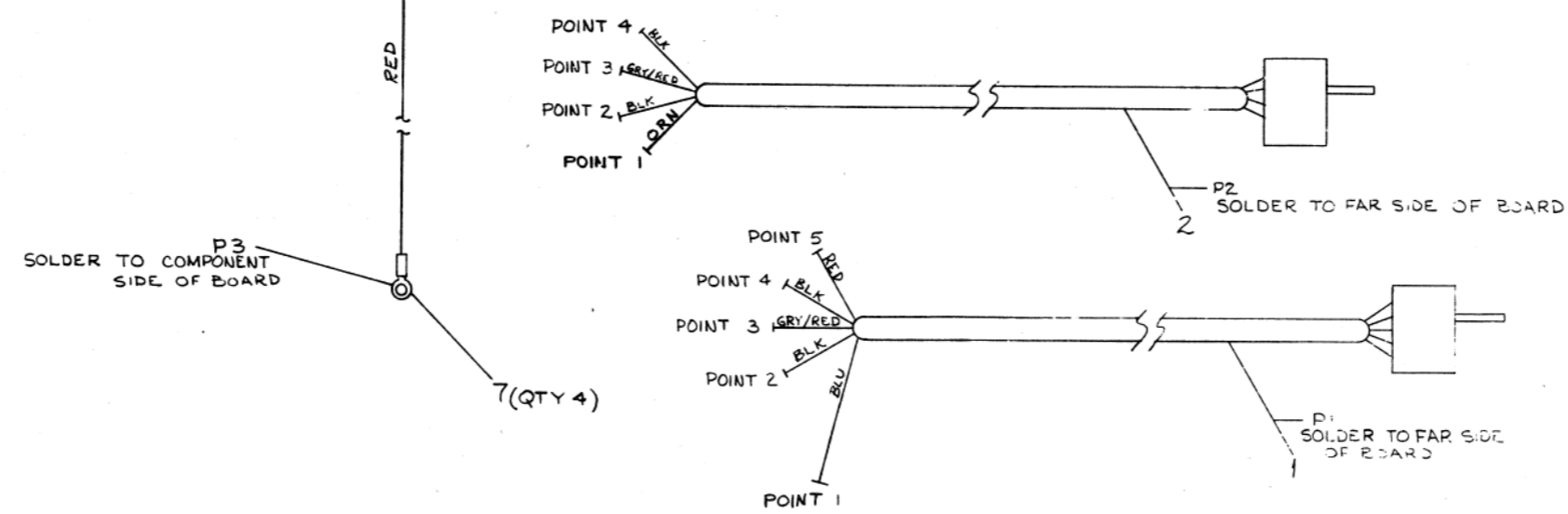
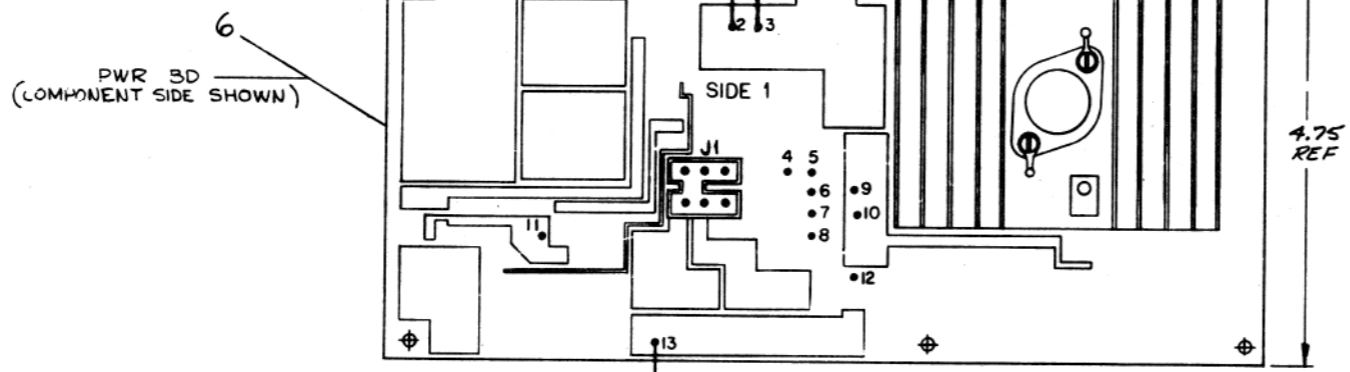
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8 0-U-912010Z LV 0 2 1



ITEM NO.	DESCRIPTION		FROM		TO		LENGTH
	AWG	COLOR	CONN	TERM	CONN	TERM	
1	18	BLU	P1	POINT 1	PWR #11	SOLDER	
		BLK	P1	POINT 2	PWR #6		
		GRY/RED	P1	POINT 3	PWR #9		
		BLK	P1	POINT 4	PWR #5		
		RED	P1	POINT 5	PWR #12		
2		ORN	P2	POINT 1	PWR #4		
		BLK	P2	POINT 2	PWR #7		
		GRY/RED	P2	POINT 3	PWR #10		
	18	BLK	P2	POINT 4	PWR #8		
3	14	RED	P3	ITEM 7	PWR #13		13 IN ±.25
4	14	BLK	P5	ITEM 7	PWR #2		7 IN ±.25
5	14	ORN	P4	ITEM 7	PWR #1		11 IN ±.25
4	14	BLK	P6	ITEM 7	PWR #3	SOLDER	9 IN ±.25

- NOTES:
1. STRIP LENGTH FOR ITEMS 3, 4 & 5 ARE TO BE .16 LONG.
 2. THE BLACK WIRES ON P1 & P2 CAN BE INTERCHANGED BETWEEN POINTS 5, 6, 7, & 8 ON THE POWER BOARD.
 3. INK STAMP ASS'Y NO. 7010718 IN FIGURES, 13 HIGH WHERE SHOWN.



DESCRIPTION	DWG. PART NO.	ITEM NO.
4 CONN, SOLDERLESS	9007928-00	7
1 POWER SUPPLY BOARD, RX01	005-541398-0-1	6
1/8 WIRE, #14 AWG, IPVC, ORANGE	9107370-33	5
1/8 WIRE, #14 AWG, IPVC, BLACK	9107370-00	4
1/8 WIRE, #14 AWG, IPVC, RED	9107370-22	3
1 HARNESS, DISK CONTROL BOARD	D-1A-7010853-0-0	2
1 HARNESS, READ/WRITE BOARD	D-1A-7010854-0-0	1

QUANTITY & VARIATION

THIRD ANGLE PROJECTION

REMOVE BURRS AND BREAK SHARP CORNERS

DO NOT SCALE DWG

MATERIAL SEE PARTS LIST

FINISH

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

ANGLES 10° 30'	CLASS OF ACCURACY (CHECK ONE)	NOMINAL DIMENSION RANGE INCHES				
		OVER 0 TO 0.2	OVER 0.2 TO 0.5	OVER 0.5 TO 1.2	OVER 1.2 TO 3.0	OVER 3.0 TO 40.0
	MEDIUM	±.004	±.008	±.012	±.016	±.024
	PREFERRED	±.012	±.016	±.025	±.031	±.051

DRN. T. G. Miller 1/28/75

CHK'D M. C. Miller 3/5/75

ENG. B. J. Miller 3/18/75

PROD. J. Miller 3/18/75

FIRST USED ON H771

TITLE RX01 POWER BOARD ASS'Y

E-UA-H771-0-0

SCALE 1/1

SHEET 1 OF 1

DIST.

REV.	CHANGE NO.	DATE	BY	CHK'D
A	00001	12/1/74	C. YOUSE	
B	00001	12/1/74	B. HAZEN	

DEC FORM NO. DRD 100-C

D AD 7010718-C-0

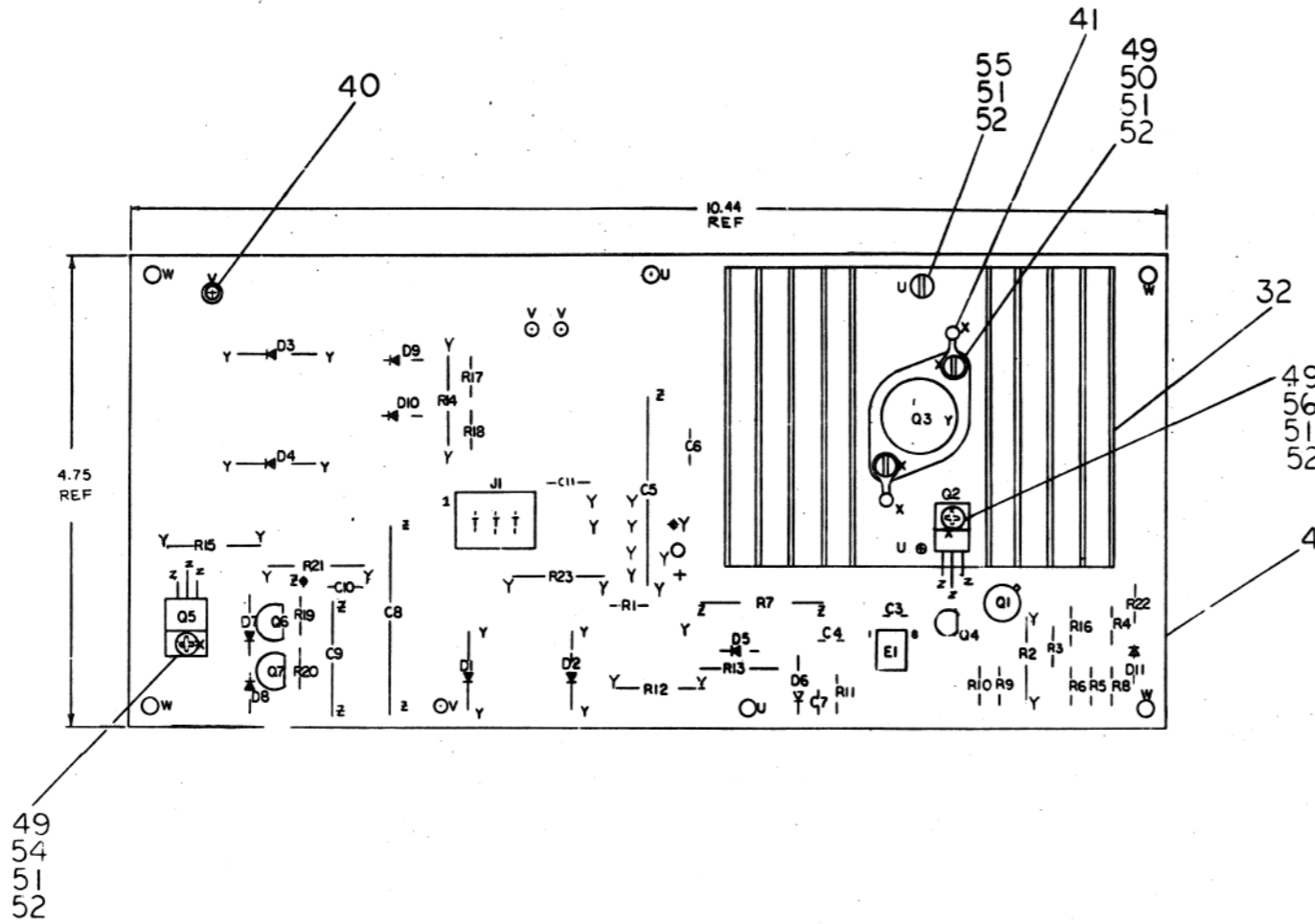
A

57

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NOTES:

- UNLESS OTHERWISE SPECIFIED
 A. ALL RESISTORS ARE 1/4W, 5%.
- DOTTED AREAS COMPONENT NOT ON BOARD.
- AT TIME OF MODULE ASSY, ITEM 49 SHOULD BE APPLIED BENEATH Q2, Q3 & Q5.
- AT TIME OF ASSEMBLY, Q2, Q3 AND Q5 MOUNTING HARDWARE MUST BE TORQUED TO 4.70 INCH POUNDS.
- Q4, Q6 AND Q7 OUTLINES CORRESPOND TO GENERAL ELECTRIC TYPE TRANSISTORS.
- FLAT RECTANGULAR WASHER SUPPLIED BY VENDOR TO BE MOUNTED UNDER Q2 AND Q5. SCREWHEAD.



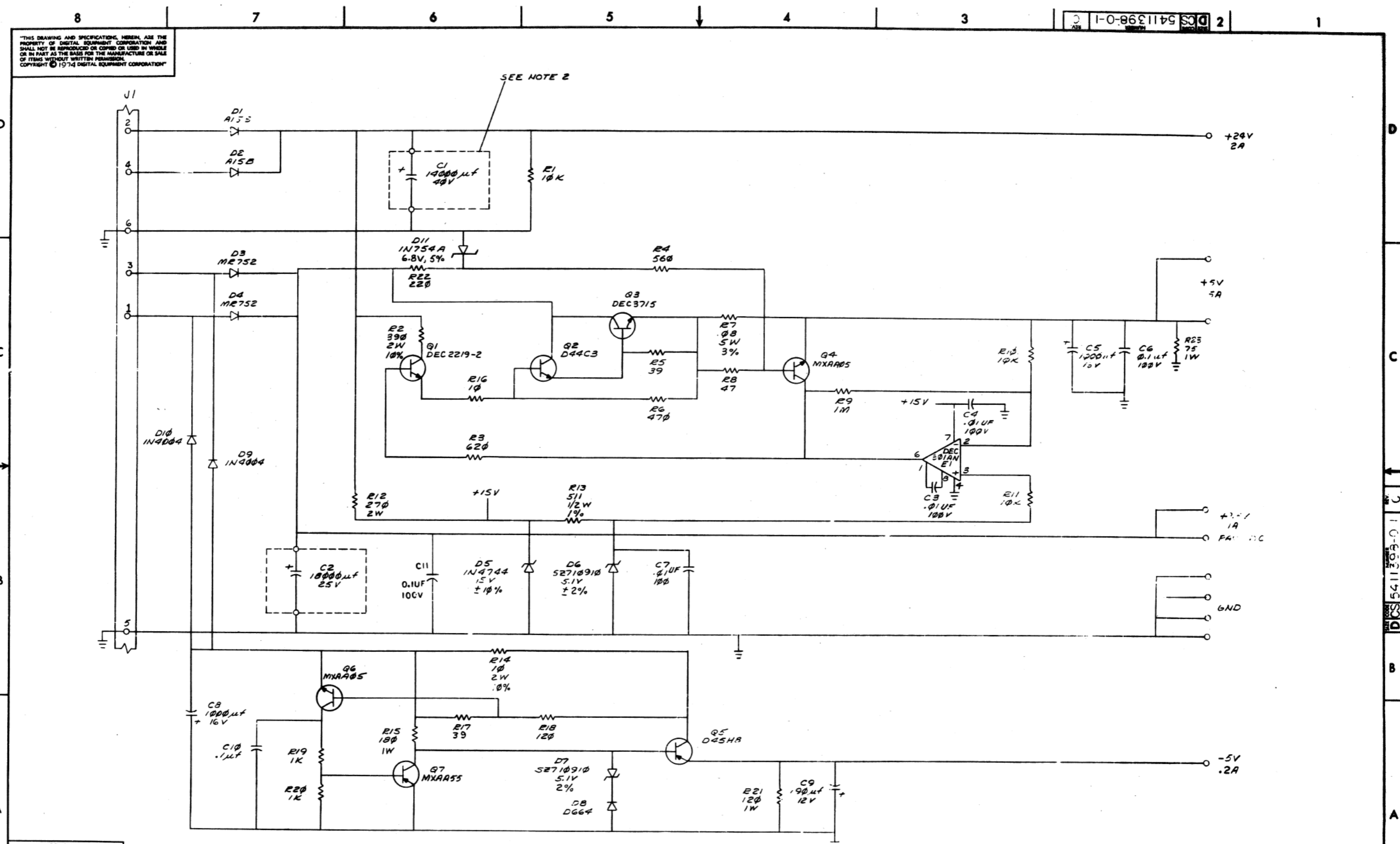
REF	QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
			X-Y COORDINATE HOLE LOCATION	DCS 5411398-0-1	1
			ASSY/DRILLING HOLE LAYOUT	D-AN-5411398-0-3	2
			MODULE ECO HISTORY	B-MH-5411398-0-6	3
			ETCHED CIRCUIT BOARD	3011397-00	4
3		C3, C4, C7	CAP .01 μF 100V 20% DISC	1001610-01	5
2		C5, C8	CAP 1000 μF 16V ELEC	1011849-02	6
3		C6, C10, C11	CAP .1 μF 100V 20% DISC	1000030-00	7
1		C9	CAP 190 μF 12V 10% ELEC	1009433-00	8
2		D1, D2	DIODE A138 (IN5624)	1110420-00	9
2		D3, D4	DIODE M752	1110613-00	10
1		D5	DIODE 1N4744 15V 10%	1105648-00	11
					12
2		D7, D6	DIODE 5Z710910 5.1V 3%	1110713-00	13
1		D8	DIODE D664	1100114-00	14
2		D9, D10	DIODE 1N4004	1105796-00	15
1		D11	DIODE 1N754A 6.8V 5%	1109991-00	16
2		R5, R17	RES 39 1/4W 5% CC	1302377-00	17
1		R6	RES 47C 1/4W 5% CC	1300312-00	18
1		R7	RES .08 5W 3% CC	1311603-00	19
1		R8	RES 47 1/4W 5% CC	1300202-00	20
1		R9	RES 1M 1/4W 5% CC	1309595-00	21
1		R12	RES 270 2W 5% CC	1305380-00	22
1		R13	RES 511 1/4W 1% CC	1300324-00	23
1		R14	RES 10 2W 10% CC	1300172-00	24
1		R15	RES 180 1W 5% CC	1300262-00	25
1		R16	RES 10 1/4W 5% CC	130317-00	26
					27
1		R18	RES 120 1/4W 5% CC	1300247-00	28
2		R19, R20	RES 1K 1/4W 5% CC	1300365-00	29
1		R22	RES 220 1/4W 5% CC	1300271-00	30
1		R21	RES 120 1W 5% CC	1301938-00	31
1			HEAT SINK	1212201-00	32
1		Q1	TRANS DEC 2219-2	1101883-00	33
1		Q2	TRANS 2A4C3	510171-01	34
1		Q3	TRANS DEC 3715	503069-00	35
2		Q4, Q6	TRANS MXA A05	510705-00	36
1		Q5	TRANS D45H8	1510708-01	37
1		Q7	TRANS MXA A05	1510705-01	38
1		E1	I.C. DEC 301AN	1910282-00	39
4			EYELET	9007836-00	40
2			TERMINAL LUG, SOLDER	9009576-00	41
1		J1	CONNECTOR 6 PIN	1211342-0 6	42
					43
1		R4	RES 560 1/4W 5% CC	1301330-01	44
1		R23	RES 75 1W 5% CC	1305281-00	45
3		R1, R10, R11	RES 10K 1/4W 5% CC	1300479-00	46
1		R2	RES 390 2W 5% CC	1301864-00	47
1		R3	RES 620 1/4W 5% CC	1303178-00	48
AIR			THERMAL COMPOUND	9008238-00	49
2			SCREW 4-40 X 1/2	9006013-04	50
5			KEPNUT 4-40	9006557-00	51
5			WASHER FLAT 4-40	9006655-00	52
					53
1			SCREW 4-40 X 5/16 (PHILLIPS HD)	9006011-1	54
1			SCREW 4-40 X 7/16	9006012-04	55
1			SCREW 4-40 X 1/2 (PHILLIPS HD)	9006013-1	56

FIRST USED ON OPTION MODEL		PARTS LIST	
PX01	ETCH BOARD REV. D		
DATE 11/27/74	DATE 1/18/75	DATE 1/24/75	DATE 1/24/75
DESIGNED BY [Signature]	DESIGNED BY [Signature]	DESIGNED BY [Signature]	DESIGNED BY [Signature]
CHKD BY [Signature]	CHKD BY [Signature]	CHKD BY [Signature]	CHKD BY [Signature]
REV. 1	REV. 1	REV. 1	REV. 1
DEC NO.	EIA NO.	DEC NO.	EIA NO.
SEMICONDUCTOR CONVERSION CHART			
SCALE		TITLE	
SHEET 1 OF 2		RX01 POWER SUPPLY	
DIST.		SIZE CODE NUMBER REV.	
D		DCS 5411398-0-1 C	

IC TYPE	4	7
301A		
GND		
+5V		
IC PIN LOCATIONS		

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DCS 5411398-0-1 2



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	RX01 POWER SUPPLY	SIZE CODE	NUMBER	REV.
SCALE	SHEET 2 OF 2	DIST.	DCS 5411398-0-1	C

817 FORM NO. 010 128

