Digital Equipment Corporation
Maynard, Massachusetts

digital

Maintenance Manual
Volume 1

RK8 DISK SYSTEM

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RK8 DISK SYSTEM
MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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Preface

The RK8 Disk operational and functional charactersitics are fully described in Volumes I and II of the associated Maintenance Manual. In Volume I all written data pertinent to the Disk is presented, and Volume II contains the RK8 Disk Engineering Drawing set showing the logic circuitry described in Chapter 5 of Volume I.

The drawings referenced in Chapter 5 of Volume I and the drawing identification in Volume II are prefixed by the Roman numeral II.

Chapter 1
General Information

The RK8 Disk System is a movable read/write head, random-access, removable bulk storage, digital memory device designed for use with DEC PDP-8 family-of-computer systems (see Figure 1-1). The RK8 accepts up to four RK01 Disk Drives that can be added to the system in 831,488 word increments providing a total of 3,325,952 words of storage. One RK08/RK01 provides up to 831,488 words of storage (12 bits). The single-cycle data break facility allows transfers at a rate of 16.7 μs per word. The average access time is 240 ms with the disk read/write head (one per surface) at extreme disk track positions, or 134 ms when the disk head is at random disk track positions. Worst-case access timing is 443 ms. (The accessing times include settling time.)

Figure 1-1 RK8 Disk System

The RK8 System has the following three features:

a. The RK08 Disk Control possesses many maintenance features useful in diagnostic program checking of registers, flags, and logic functions.

b. The system uses the single-cycle data break facility and is designed to minimize programming effort.

c. Delay networks, associated with data transfers, are derived from a crystal-controlled clock and give format stability over a wide range of environmental conditions.

Three basic functions of the disk are: normal read or normal write for accessing data, a read-all or write-all for formatting and accessing the header word, and a parity check that reads data without transferring it to the computer.

NOTE

All drawings referenced in Chapter 5 are contained in Volume II of this Maintenance Manual.

1.1 PERFORMANCE SPECIFICATIONS

Table 1-1 provides electrical, environmental, physical, and mechanical specifications for the RK8 Disk Drive System.

Table 1-1

Specifications

Characteristic	Specification
Electrical Power	115/230 ±10 Vac, 50/60 ±1/2 Hz at 1.5A 150W (510 Btu) for the RK08 Control and 6.1A, 700W (2380 Btu) or 8.7A (surge current), 1000W (3450 Btu) for each RK01 Disk Drive.
Disk Logic Voltage	+24 ±2 Vdc, -5A minimum, 6.0A maximum average with a 15A peak. +12 Vdc ±5% at 200 mA -26 Vdc ±5% at 200 mA +5 Vdc ±5% at 1.0A.
Disk Capacity	
Storage Capacity	Each RK01 Disk Cartridge stores 831,488 (includes 3 spare tracks) 12-bit words.
Expansion	Four RK01 Disk Drives can be controlled by one RK08 Control for a total of 3,325,952 words.
Data Tracks	200 (plus 3 spare tracks)
Words per Track	4096 (2048 words on 0 and 1 surfaces)
Sectors	16 (eight sectors per side)
Words per Sector	256
Minimum Block Size	256
Maximum Block Size	4096
Read/Write Heads	
Type	Tunnel erase
Number	2 (one per disk surface)
Recording Parameters	
Recording Method	Double Frequency - Time plus data
Density	704 bits/inch (outer track 000) 1026 bits/inch (inner track 203)
Speec	1500 ±30 rpm
Transfer Path	Single-cycle Data Break
Transfer Rate	16.7 μs per word

Table 1-1 (Cont)
Specifications

Characteristic	Specification
Recording Parameters (Cont)	
Minimum Access Time	2.0 ms step, plus 37 ms settle time (Adjacent Tracks)
Average Access	134 ms (includes settle time)
Maximum Access	441 ms (includes settle time)
Latency Maximum	40 ms (1 revolution)
Latency Average	20 ms (1/2 revolution)
Program Interrupts	Transfer Done Flag (Enabled Separately) Error Flag (Enabled Separately)
Write Lock	A programmable header word allows sector write lock. A pushbutton allows total disk write lock.
Environmental Conditions	
Operating Temperature	+65°F (+15°C) to +90°F (+32°C) 20°F per hour cycle rate.
Storage Temperature	+20°F (-7°C) to +165°F (74°C) for a period of six months when packaged for storage and shipment.
Operating Humidity	20% to 80%, excluding all conditions that would cause moisture to condense in or on the equipment.
Storage and Shipping	
Humidity	Range: minimum 5%, maximum 95% up to 100°F. No condensation, resulting in moisture in or on the equipment, is tolerable.
Mechanical	
Cabinets	One cabinet can accommodate one RK08 Control and one RK01 Disk Drive (an RK8 System), a second cabinet houses two RK01 units, and a third cabinet houses a fourth RK01 unit.
Physical	
Mechanical Package	One standard DEC cabinet accommodates the RK8 System, a second cabinet houses two RK01 units and a third cabinet houses a fourth RK01 unit.
Weight	500 lb uncrated (RK8) 590 lb crated Additional RK01 130 lb

Chapter 2
Description

2.1 PHYSICAL

The disk, its associated logic circuitry, the two power supplies, and the control and registry indicator panel are mounted in a free-standing, 19-in. wide H950 Cabinet (see Figures 1-1 and 2-1).

The STATUS, COMMAND, DATA, DISK ADDR (Disk Address), MAJOR STATES, BRK RQ (Break Request), BREAK, WRITE, and WCOV (word count overflow) indicator lamps are located on the upper front section of the cabinet. When lit, these lamps reflect the status of the registers.

Three RK08/RK01 logic mounting panels are located (behind two dress panels) directly below the indicator panel (see Figure 2-2). Removal of these panels exposes the logic mounting panel module connector pins.

A control panel consisting of the DISK LOCKOUT 0, 1, 2, and 3, the SECT PROT (Sector Protect), and the ATTN-OFF-ON (Attention-Off-On) push-button switches is located below the three dress panels; the Disk START/STOP switch and SAFE lamp are located on the disk control panel below the access door. The function of each switch is outlined in Table 4-7.

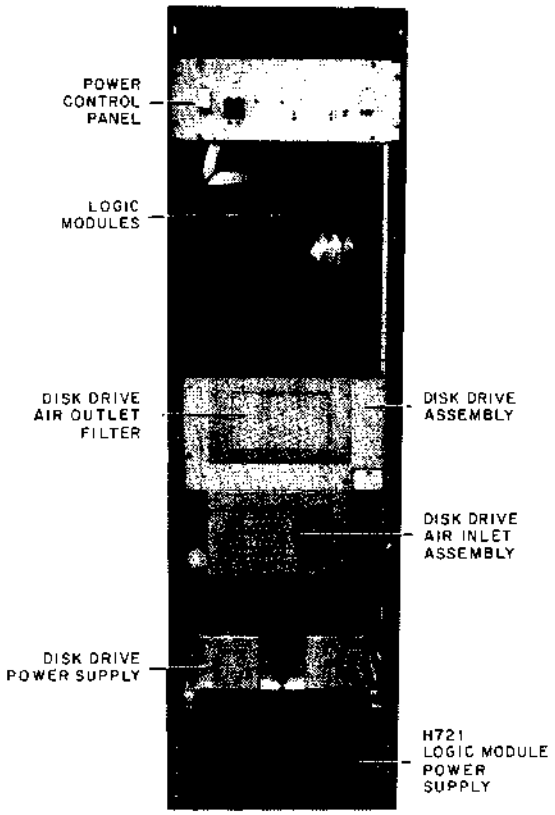


Figure 2-1 Rear View of Cabinet Interior

The front door of the disk drive unit is a removable panel allowing access to the disk logic mounting panel module pins. The power supply voltage terminations are accessible by removing the dress panel (second from the bottom of the cabinet). All

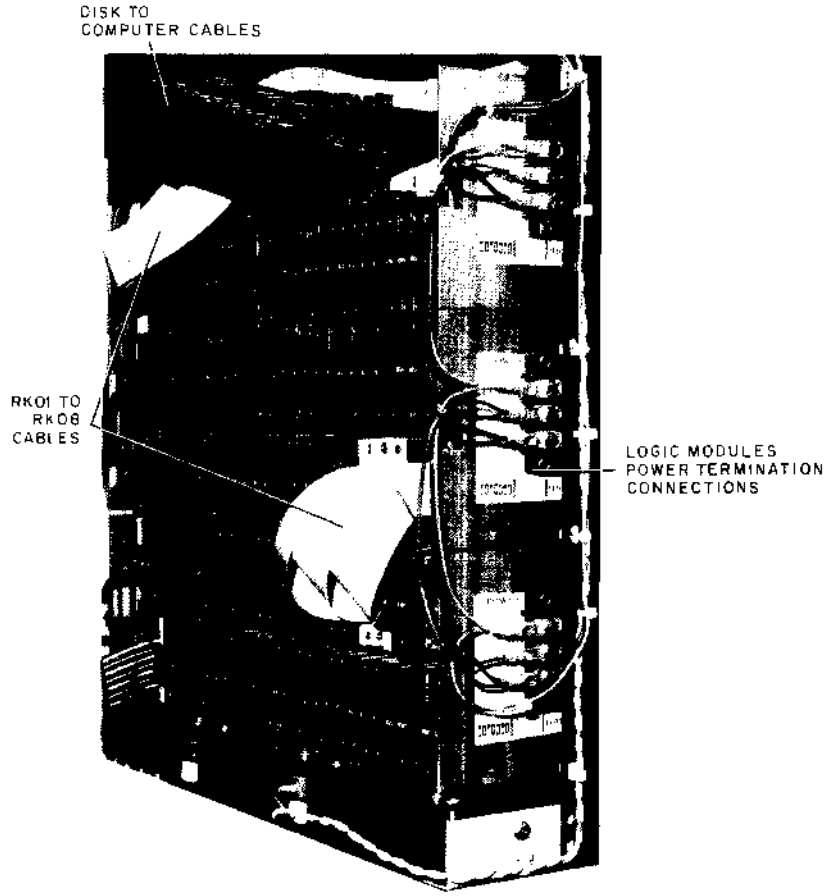


Figure 2-2 Logic Mounting Panels with Logic Modules

voltages are separately fused. The +5 and -15 Vac and ground connections for the three module mounting panels are on the left interior of the cabinet and each connection is identified.

2.2 DISK CABINET

The H950 Disk Cabinet is equipped with roll-around casters and permanent leveling feet. Although either can be used for installation purposes, it is recommended that the disk cabinet be mounted on the leveling feet.

NOTE

The disk air intake opening, located in the rear of the cabinet, must not be obstructed during installation; this is the air intake facility for the disk cartridge.

2.3 RECORDING DISK CARTRIDGE

The recording medium for the RK08 Disk is a removable disk cartridge which houses an aluminum, oxide-coated platter that rotates counterclockwise, when viewed from the top, when inserted into the disk drive assembly.

The unformatted storage capacity of a single disk is 1,929,000 6-bit characters. There are two recording surfaces per disk, the top designated side 0 and the other side 1. There are 203 data tracks per surface which are numbered, starting from the outer edge of the disk, from data track 000 to the center of the disk and track 202 (see Figure 4-1). The disk drive mechanism permits the interchanging of disk cartridges, the procedures for this operation are outlined in Chapter 3.

The disk cartridge is a semipermanently encased unit with an access door for entry of the read/write heads; the disk cartridge also contains an air valve on the bottom of the disk pack which allows filtered air to enter the cartridge. The pressurized air performs a two-fold function: 1) it keeps the disk aluminum platter operating at the required ambient conditions, and 2) it keeps foreign particles from entering the disk cartridge read/write head access door. When the disk cartridge is inserted into the disk, the read/write head access door is automatically opened by an interior spring arm that allows the aluminum platter to be positioned between the read/write heads (see Figure 2-3).

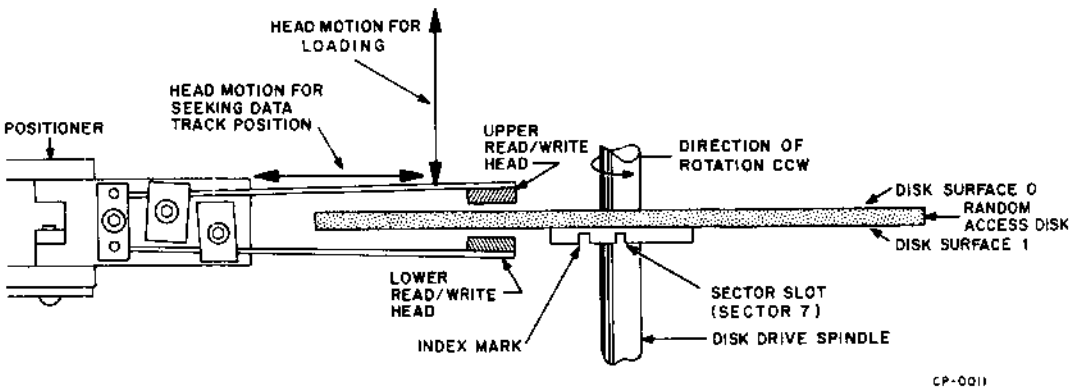


Figure 2-3 Disk Assembly Diagram

The disk cartridge is accurately positioned on the disk's internal mechanical drive spindle and is held in position until the disk cartridge activates an internal switch that issues a status level permitting the drive motor to turn on and bring the disk up to speed.

2.4 DISK READ/WRITE HEADS

Dara is recorded on and retrieved from the disk by upper and lower read/write heads (see Figure 2-4) which "fly" between 125 and 160 microinches from the disk recording surfaces on a self-generated film of air. The heads shown in Figure 2-5 consist of: a split erase element located behind the read/write gap, and the erase coil connected in series with the center tap of the read/write coil.

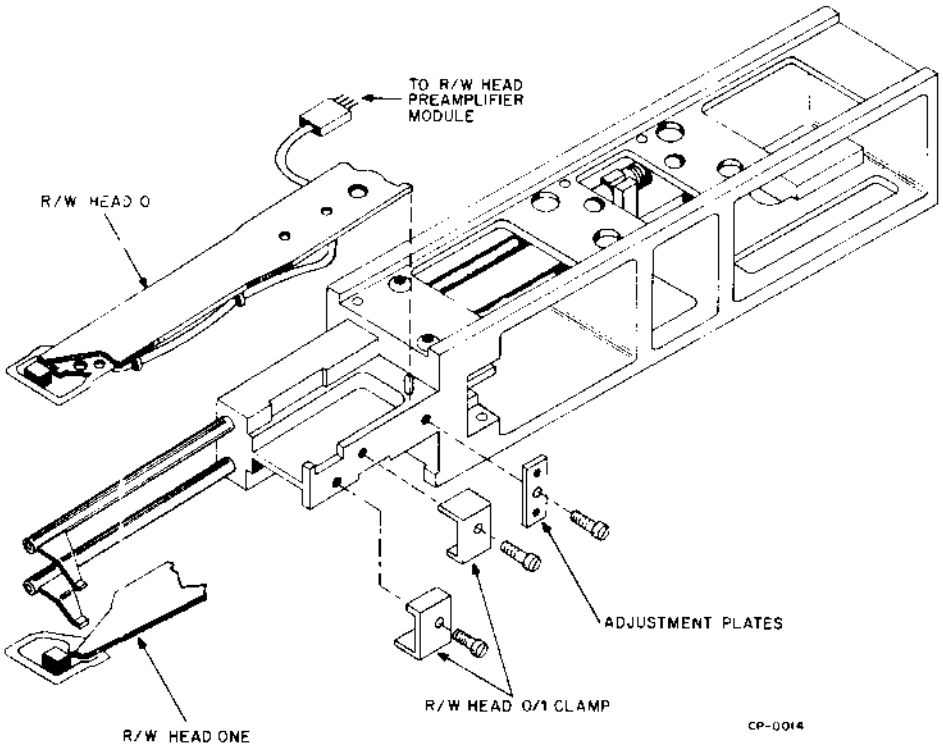


Figure 2-4 Read/Write Carriage Assembly Diagram

The disk surface velocity generates the film of air which supports the heads. The heads are not lowered onto the disk surface until the disk is close to or at its normal operating speed of 1500 rpm.

A CS circuit monitors all dc voltages, disk speed, and other disk parameters; if unsafe conditions exist, the heads are automatically retracted.

The read/write heads are mounted on two movable assemblies, one gliding over disk 0 surface and the other over disk 1 surface (see Figures 2-3 and 2-4).

NOTE

Heads must not be loaded manually when the disk cartridge has been removed from the disk receiver, when the disk has stopped rotating, or when the disk logic air blower is not operational. Heads can be loaded under static conditions only if a folded piece of Holterith card is inserted between the upper and lower heads giving protection to the gliding surfaces.

When reading/writing information from or onto the disk, the information is trimmed in width by the split erase head (see Figure 2-5). The difference in the recorded and the erased trimmed track compensates for mechanical tolerances in the head positioning mechanism and provides protection for data recorded on adjacent data tracks. For example, if the data on track 009 was not trimmed, the read head would read the data on track 009 in addition to partial data on track 010. The erase function occurs approximately 40 μs after the recording of data.

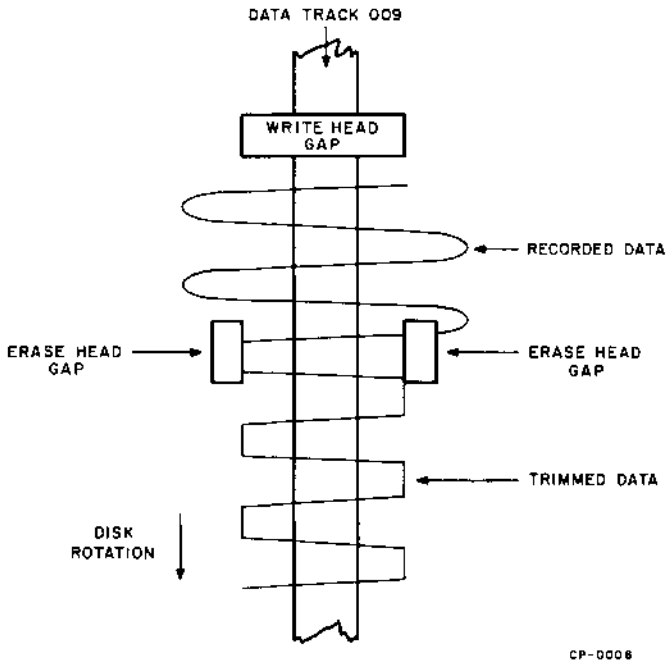


Figure 2-5 Data Trimming Diagram

2.5 DISK DRIVE ASSEMBLY

The main disk drive assembly (see Figure 2-6) is a 19-in. wide, 19-3/8-in. high, and 30-in. deep unit consisting of the following separate components:

a. The read/write head responsyn positioner assembly that accommodates the read/write magnetic head assemblies and their associated electronic control circuitry,

b. The disk cartridge drive and associated spindle mechanism,

c. The operator control panel with functional control indicators and the START/STOP switch,

d. The logic and control circuitry for operation of the disk,

e. A 10-ft I/O cable, and

f. An air blower and associated filter.

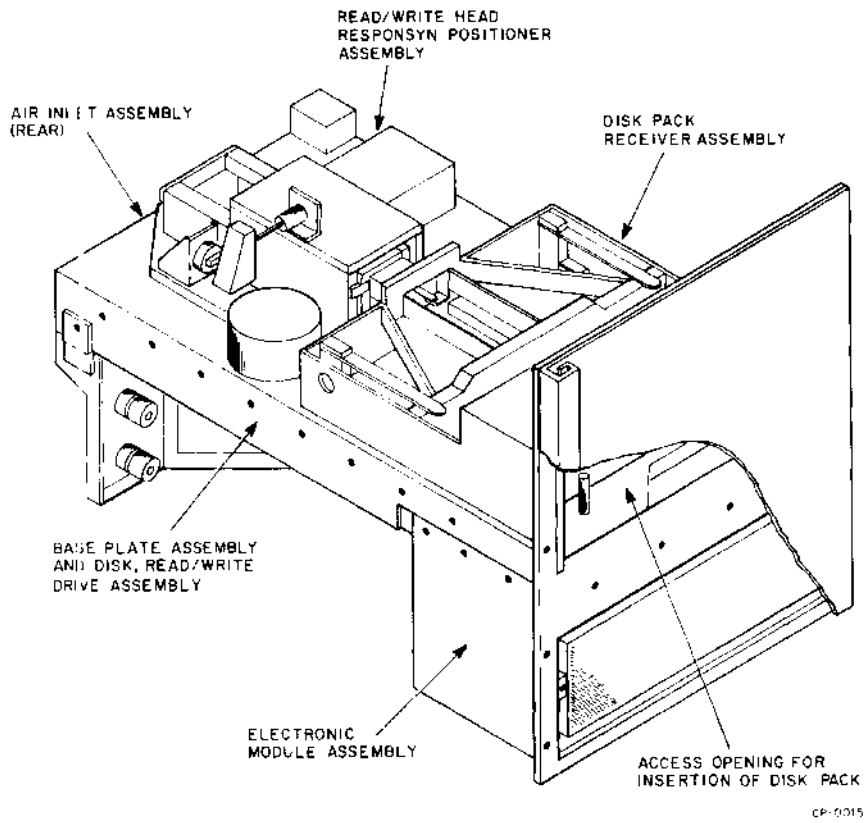


Figure 2-6 Main Disk Drive Assembly Diagram

The air blower assembly of the disk is mounted in the lower rear portion of the disk assembly, the logic and control circuitry in the lower front portion of the disk assembly, the read/write head responsyn positioner assembly on the interior base-plate assembly, and the functional control panel in the upper front portion of the disk.

2.6 RK08 DISK CONTROL LOGIC

The disk control circuitry is divided into a series of functions, each of which is controlled by the major state shift register. The functions, which are divided into MAJOR states A through K by the shift register, are described as follows:

a. Locate the data track,
b. Sync off the sector pulse,
c. Wait for the header words,
d. Read the header words (2) of the sector addressed,
e. Wait for the data words, and
f. Transfer the data to or from the computer memory.

2.7 DOUBLE-FREQUENCY RECORDING

Double-frequency recording, which is used in the RK08/RK01 Disk for recording and writing of data, provides an overall frequency of 1,440,000 bits/sec which includes the clock and data bits.

The reading and writing of data is performed by the read/write head which senses pattern changes in the head gap flux (see Figure 2-7).

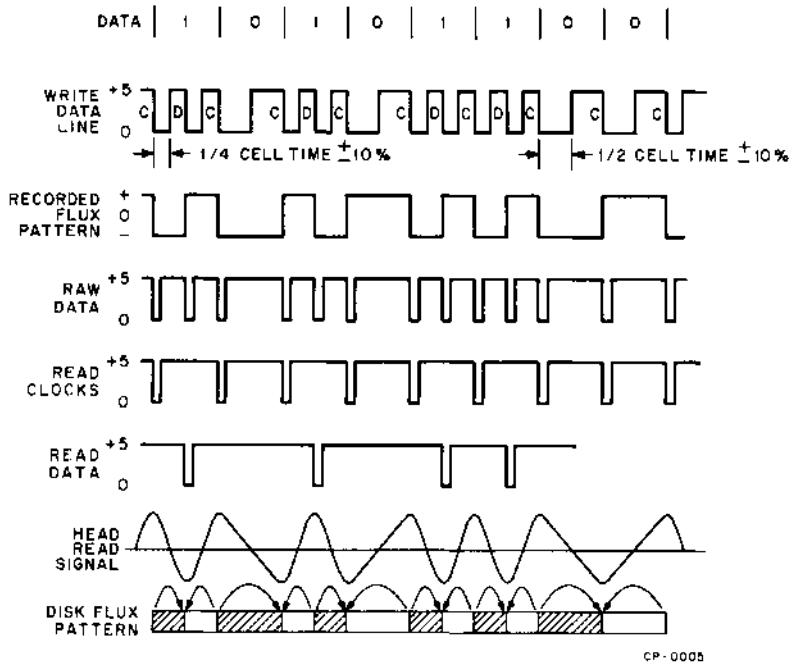


Figure 2-7 Double-Frequency Recording Data In/Out Relationship Diagram

2.7.1 Clock Frequency

The clock frequency signal is encoded in data pulses to produce a single composite signal at the read/write head. This signal presents a 0- or 1-bit condition for each bit-cell time generated by the clock.

Single disk storage uses the double-frequency method of magnetic recording; a clock frequency is used in establishing the basic bit-cell timing cycle. The insertion of a data pulse between clock pulses in a bit-cell time period produces a composite read/write signal that uses only clock pulses for a 0-bit indication and data pulses plus clock pulses for a 1-bit indication.

A 0 bit-cell time (clock pulses only) produces a single change in direction of the flux pattern, and a 1 bit-cell time (a data pulse located between two clock pulses) produces a double change in the disk flux pattern direction. In either case, the clock signal generates a change in the direction of magnetic polarity from plus-to-minus or minus-to-plus, causing a bit to be stored.

Because the clock and data information are synchronized on a composite signal, double-frequency recording is sometimes referred to as "self-clocking".

2.7.2 Double-Frequency Recording

With double-frequency recording, a clock bit is always inserted at the beginning of each bit-cell time to establish the basic recording frequency. A data bit is inserted between clock bits at twice the frequency; consequently, the bit generates two disk flux reversals within a single bit-cell time. If the data bit is not present, a single disk flux reversal occurs in a bit-cell time.

The magnetic recording head, which contains a split-ring core with a coil winding, causes a magnetic field in a given flux direction to prevail at the ring gap while the coil is energized. When current flows through the coil, the flux induced in the ring establishes a fringe flux at the gap, and as the magnetic recording surfaces passes by the gap, the fringe flux magnetizes the disk surface.

2.7.3 Write Operation

When writing data on the disk, a bit is recorded when the flux direction in the ring is reversed by switching between coils in the read/write head. The fringe flux is reversed in the gap and, therefore, the portion of the flux flowing through the recording medium is reversed.

If the flux reversal is instantaneous in relation to the motion of the recording surface and the gap is observed at the moment of reversal, the portion of the surface that has passed the gap is magnetized in one horizontal direction, while the portion directly under the gap is magnetized in the opposite direction. Between these two conditions the flux must reverse 180° which represents a bit.

2.7.4 Read Operation

During the read operation, the gap passes over an area that is magnetized in one horizontal direction, and a constant flux flows through the ring and coil. There is no output voltage for this condition, however, when the recorded bit and the 180° horizontal flux reversal passes the gap, the flux flowing through the ring and coil reverses 180°. The coil senses the flux change and produces a voltage output pulse.

2.8 OPERATOR CONTROL AND INDICATOR LIGHTS

The operational control and indicator lamps are readily accessible to the operator from the front of the disk. The function and purpose of each is described in Tables 2-1, 2-2 and 2-3.

Table 2-1
Control Switch

Control	Function
START/STOP	When placed in the START or up position, the disk starting cycle is initiated only if the disk cartridge is in place and the disk cartridge receiver handle is in the raised position. When placed in the STOP or down position, the disk STOP sequence is initiated.

Table 2-2
Indicator Lights

Light	Function
SAFE	When illuminated, the disk cartridge access door interlock is off, and it is safe for the operator to lower the disk cartridge receiver handle for removal or insertion of the disk cartridge. The indicator lamp illuminates approximately 35 seconds after a STOP sequence has been initiated.
READY	When illuminated, it is ready to begin communicating with the central processor of the computer. The lamp illuminates approximately 90 seconds after the START sequence has been initiated.

Table 2-3
Control Panel Switches/Lights

Switch	Function
DISK LOCKOUT 1-4	When depressed, the lamp illuminates indicating that the disk associated with the pushbutton is locked out and data cannot be written onto the disk platter. The panel controls up to four disks.
ATTN	When illuminated (red), the lamp indicates that the disk power supply has a malfunction. Pushing the STOP switch resets the power supply. NOTE This lamp is also illuminated after turning system power off with the computer on-off switch. Pushing this lamp switch resets the power supply. This interlocking action protects the data on the disk from spurious write signals while computer and disk controls are powered down.

Table 2-3 (Cont)
Control Panel Switches

Switch	Function
ON	When ON, power is applied to the disk.
OFF	When OFF, power is removed from the disk.
SECT PROT	Prevents writing on protected sectors, as specified by bit 0 of the second header word.

2.9 DISK DRIVE POWER SUPPLY

The disk drive power supply operates from a 115 Vac, 60 Hz primary power source which is controlled by a 15A power contactor relay K1. The 115 Vac input line and the ac neutral line are filtered by two 10A line filters (see Figure 2-8). The dc output voltages are terminated on connectors TB1, -2, -3, and -4, with the dc voltage common lines connected to chassis ground TB4 (see Figure 6-13). The dc outputs are capable of driving up to two disk drives, and both ac and dc lines are fuse-protected.

All terminal boards are mounted on the exterior of the power supply and are protected with an insulated cover to prevent accidental contact with live voltages or damage to the power supply.

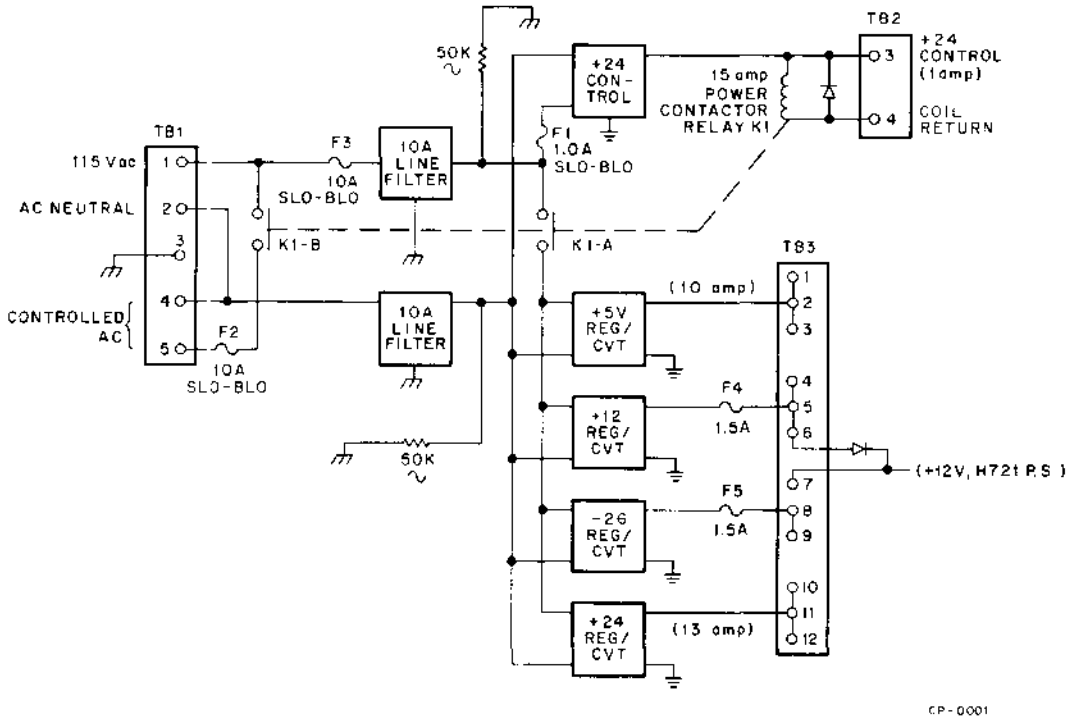


Figure 2-8 Disk Drive Power Supply Block Diagram

2.10 DISK DRIVE POWER INTERLOCK AND SEQUENCING

The interlock and sequencing of events which take place in the disk drive power supply are presented in the following sections.

2.10.1 ON Sequence

The ON sequence starts when the disk drive power supply interlock and sequencing logic accepts a momentary relay (K1) contact closure to ground of 20 mA maximum. With the relay contacts closed, the following sequence of events takes place: 1) a general reset is generated, 2) the dc ON LIGHT is illuminated, 3) all dc voltages are turned on in sequence except for the +24 Vdc control voltage, and 4) the power OFF LIGHT is deactivated.

2.10.2 General Reset

During this condition, the ground level from +5V is activated for a minimum of one millisecond after stabilization of all dc voltages during the START sequence.

2.10.3 Low Voltage

If the dc voltage, with the exception of the +24 Vdc control voltage, falls below the specified dc levels, the low voltage detector initiates an unconditional OFF sequence and illuminates the ATTEN LIGHT output voltage.

2.10.4 Interlock

The power supply sequencing logic has two individual interlock inputs which inhibit operation of the OFF SWITCH-initiated sequence with a ground input from +5 Vdc.

2.10.5 +24 Vdc Control Voltage

This voltage is activated directly from the primary ac power source and is not switched with the power supply sequencing logic or the ON or OFF relay contacts.

2.10.6 Indicator Lamp Outputs

The indicator lamp output control voltage is +24V when OFF.

Chapter 3
Installation and Operation

3.1 INSTALLATION

The RK8 Disk System is installed at the customer's site by DEC Field Service personnel; therefore, no attempt should be made by customer personnel to install the equipment.

3.2 INSPECTION

After removing the equipment packing material, inspect the equipment and report any damage to the local DEC sales office. Inspection procedures are as follows:

Step	Procedure
1	Inspect external surfaces of the cabinets and related equipments for surface, bezel, switch, and light damage, etc.
2	Remove the shipping bolts from the rear door, and internally inspect the cabinet for console, processor, and interconnecting cable damage; inspect for loose mounting rails, loose or broken modules, blower or fan damage, any loose nuts, bolts, screws, etc.
3	Inspect the wiring side of the logic panels for bent pins, cut wires, loose external components and foreign material. Remedy any defects found.
4	Inspect the power supply for proper seating of fuses and power connecting plugs.

3.3 CABINET INSTALLATION

The RK8 Disk cabinet is equipped with roll-around casters and adjustable leveling feet. It is not necessary to bolt the cabinet to the mounting floor unless conditions indicate otherwise (e.g., shipboard installation). Cabinet installation procedures are as follows:

Step	Procedure
1	With the cabinet in the desired position, lower the leveling feet so that the cabinet is supported on the leveling feet, not the roll-around casters.

Step	Procedure
2	Use a spirit level to level all cabinets and be certain that all leveling feet are firmly against the floor.
3	If necessary, tighten the bolts that secure the cabinet groups together, then recheck cabinet level. Again, make certain that all leveling feet are seated firmly on the floor.

3.4 PROTECTIVE COVERINGS

When the RK8 Disk System has been correctly positioned at the installation site, the protective packing of the read/write head and the associated head carriage assembly tie-down binding must be removed. Access to these components is gained through the rear door of the cabinet and through removing the top cover panel from the disk assembly.

3.5 PRIMARY AC POWER CABLES

The primary ac power cable is a three-wire cable which connects the installation site power source to the power supplies. The cable is connected at the factory to the disk power transformer for either 50 Hz or 60 Hz operation. The disk has a self-contained Type 721 Power Supply and an ac power cable (each wire in the cable is color coded, refer to Table 3-1 and Figure 3-1).

Table 3-1
Power Cable Line Identification

Pigtail Information		Terminal Strip Nomenclature	Plug
Line	Wire Color		
Green	Frame Ground	Frame Ground	W
White	Neutral/Line 2	Neutral or Line 2	X
Black	Line 1	Line 1	Y

WARNING

a. The green wire is the cabinet frame ground and does not carry load current; however, it must be connected for safety reasons. This wire must be securely connected from the disk cabinet to the grounding point on the primary power source.

b. The white or light gray wire is the neutral, common, ac return, or cold lead and must never be used for purposes of grounding the disk cabinet.

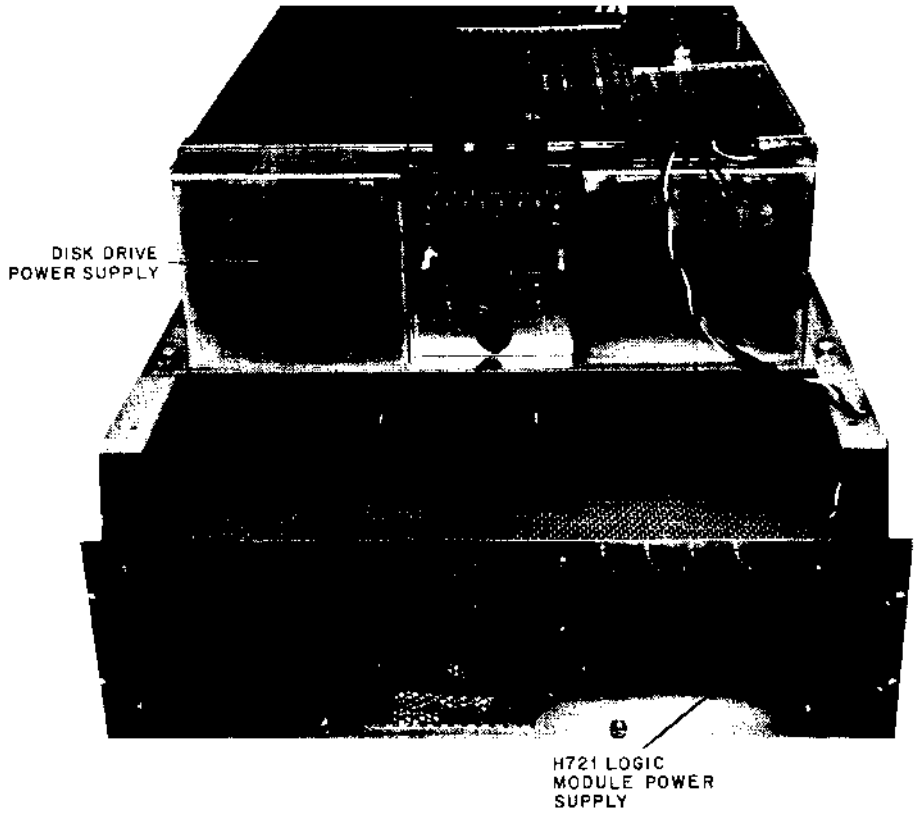


Figure 3-1 Disk and Type H721 Power Supplies

3.6 AC POWER CHECK-OUT PROCEDURES

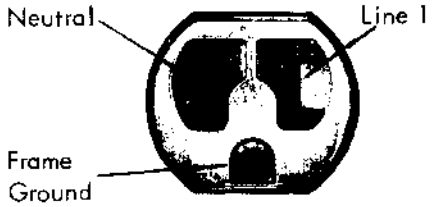
Before connecting the power cords to the disk, perform the following check-out procedures (see Figure 3-2).

CAUTION

Under no circumstances should the customer apply power to the RK8 Disk System unless a DEC Field Service Engineer is in attendance during installation.

Step	Procedure
1	Measure the power source ac voltage and ensure that the proper voltage is present.
2	Measure the voltage potential between the ac return and the frame ground lines to ensure that no potential exists between earth ground (cold water pipe) and the disk ground.
3	Refer to Figure 3-3 and check the power supply transformer T1 primary windings terminated on the Jones-type terminal strip to be certain they are connected for proper voltage and line frequency.

Service Outlet
120V 60 Hz
Single Phase
15 amp/U Gnd



When neutral is not available for 115 V 60 Hz 15 A service, a receptacle of this design shall be used except that both parallel slots shall be short so that polarized parallel blade plugs (caps) will not fit.

115V 60 Hz
Single Phase
30 amp/Twist Lock

230V 50Hz
Single Phase
20 amp/Twist Lock

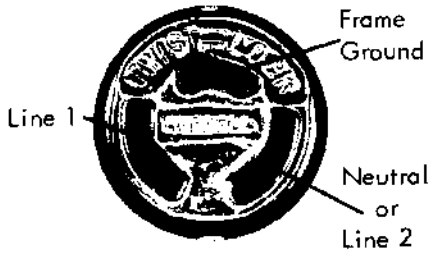


Figure 3-2 Hubbell Wall Receptacle Connector Diagram

Step	Procedure
4	Set the installation site primary power circuit breaker to the OFF position, then plug the disk primary power line cord into the wall outlet. The red lamp on the power supply control panel (see Figure 2-1) should illuminate indicating primary ac power is applied to the transformer.
5	Set the source power circuit breaker to ON.

3.7 OPERATION

The procedures presented in this section outline the sequential steps which initiate operation of the disk.

The dc power must always be ON before inserting a disk cartridge into the disk. If the disk cartridge is inserted without first turning the dc power on, the read/write head carriage assembly may be in a position other than the home or data track 000 position and the cartridge would strike the read/write heads. The disk is interlock protected; consequently, when dc power is on and ac drive motor power is turned off, the read/write head carriage returns to the home position.

NOTE

Do not write on CE disk cartridge data tracks 090 through 110 because this area contains prerecorded test tracks, 095, 100, and 105 which would be destroyed. Any other data tracks can be used for test purposes.

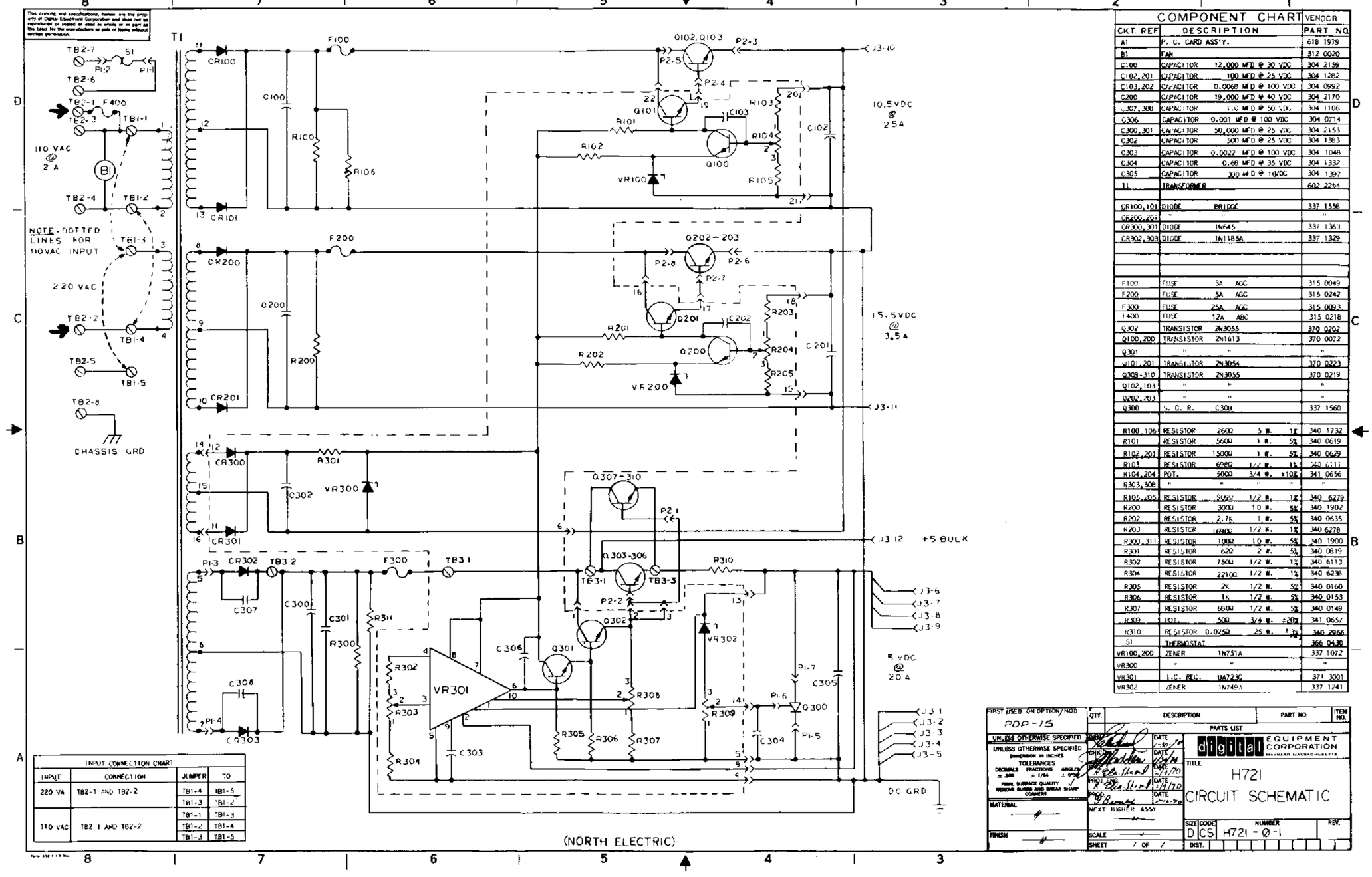
3.7.1 Sequencing

The correct sequencing procedure is as follows:

Step	Procedure
1	Depress the disk power supply dc ON/OFF switch to ON and observe that the associated dc ON lamp illuminates. The read/write heads now seek data track minus 003 at a relatively slow rate of speed (heads fully retracted).
2	When the SAFE lamp, on the front control panel of the disk, comes on and the handle lock unlatches, the disk is ready to be loaded with a disk cartridge.
3	Depress the disk power supply dc ON/OFF switch to OFF and observe that the disk sequences down.

NOTE

If there is the slightest indication of resistance to the insertion of the disk cartridge into the disk receiver, the cartridge should be removed and the interior of the disk receiver examined to determine the cause of resistance.



INPUT CONNECTION CHART			
INPUT	CONNECTION	JUMPER	TO
220 VA	TB2-1 AND TB2-2	TB1-4	TB1-5
		TB1-3	TB1-2
110 VAC	TB2 1 AND TB2-2	TB1-1	TB1-3
		TB1-2	TB1-4
		TB1-3	TB1-5

COMPONENT CHART					VENDOR
CKT. REF	DESCRIPTION				PART NO.
A1	P. C. CARD ASS'Y.				618 1979
B1	FAN				312 0020
C100	CAPACITOR	12,000 MFD @ 30 VDC			304 2159
C102, 201	CAPACITOR	100 MFD @ 25 VDC			304 1282
C103, 202	CAPACITOR	0.0068 MFD @ 100 VDC			304 0992
C200	CAPACITOR	19,000 MFD @ 40 VDC			304 2170
C307, 308	CAPACITOR	1.0 MFD @ 50 VDC			304 1106
C306	CAPACITOR	0.001 MFD @ 100 VDC			304 0714
C300, 301	CAPACITOR	50,000 MFD @ 25 VDC			304 2153
C302	CAPACITOR	500 MFD @ 25 VDC			304 1383
C303	CAPACITOR	0.0022 MFD @ 100 VDC			304 1048
C304	CAPACITOR	0.68 MFD @ 35 VDC			304 1332
C305	CAPACITOR	300 MFD @ 10VDC			304 1397
T1	TRANSFORMER				602 2204
CR100, 101	DIODE	BRIDGE			337 1558
CR200, 201	"	"			"
CR300, 301	DIODE	1N645			337 1363
CR302, 303	DIODE	1N1185A			337 1329
F100	FUSE	3A AGC			315 0049
F200	FUSE	5A AGC			315 0242
F300	FUSE	25A AGC			315 0093
F400	FUSE	12A AGC			315 0218
Q302	TRANSISTOR	2N3055			370 0202
Q100, 200	TRANSISTOR	2N1613			370 0072
Q301	"	"			"
Q101, 201	TRANSISTOR	2N3054			370 0223
Q303-310	TRANSISTOR	2N3055			370 0219
Q102, 103	"	"			"
Q202, 203	"	"			"
Q300	S. C. R.	C30U			337 1560
R100, 106	RESISTOR	260Ω	5 W.	1%	340 1732
R101	RESISTOR	560Ω	1 W.	5%	340 0619
R102, 201	RESISTOR	1500Ω	1 W.	5%	340 0629
R103	RESISTOR	698Ω	1/2 W.	1%	340 6111
R104, 204	POT.	500Ω	3/4 W.	±10%	341 0656
R303, 308	"	"	"	"	"
R105, 205	RESISTOR	309Ω	1/2 W.	1%	340 6279
R200	RESISTOR	300Ω	10 W.	5%	340 1902
R202	RESISTOR	2.7K	1 W.	5%	340 0635
R203	RESISTOR	1690Ω	1/2 W.	1%	340 6278
R300, 311	RESISTOR	100Ω	10 W.	5%	340 1900
R301	RESISTOR	620	2 W.	5%	340 0819
R302	RESISTOR	750Ω	1/2 W.	1%	340 6113
R304	RESISTOR	2210Ω	1/2 W.	1%	340 6238
R305	RESISTOR	2K	1/2 W.	5%	340 0160
R306	RESISTOR	1K	1/2 W.	5%	340 0153
R307	RESISTOR	6800	1/2 W.	5%	340 0149
R309	POT.	500	3/4 W.	±20%	341 0657
R310	RESISTOR	0.025Ω	25 W.	1%	340 2966
S1	THERMOSTAT				366 0430
VR100, 200	ZENER	1N751A			337 1072
VR300	"	"			"
VR301	I.C. REG.	UA723C			371 3001
VR302	ZENER	1N749A			337 1241

FIRST USED ON OPTION/MOD: POP-15	QTY.	DESCRIPTION	PART NO.	ITEM NO.
		PARTS LIST		
UNLESS OTHERWISE SPECIFIED	DRWN	DATE 1-30-70	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINISH SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	CHK	DATE 1-30-70	TITLE H721 CIRCUIT SCHEMATIC	
	ENGR	DATE 2-4-70		
	PROJ ENG	DATE 2-4-70		
	MFG	DATE 2-6-70		
MATERIAL	NEXT HIGHER ASSY		SIZE D CODE CS NUMBER H721 - 0 - 1 REV.	
FINISH	SCALE		DIST.	
	SHEET 1 OF 1			

Figure 3-3 Type H721 Power Supply Block Schematic Diagram (D-BS-H721-0-1)

3.7.2 Disk Cartridge Insertion

The proper procedure for inserting the disk cartridge is as follows:

Step	Procedure
1	Make certain the dc power is ON.
2	Pull the disk cartridge access door panel, then lower the disk cartridge receiver handle to the down or unloaded position. The cartridge receiver is now raised into position for insertion of the disk cartridge. The handle interlock will keep the cartridge receiver handle locked in its closed position whenever the SAFE lamp is turned OFF.
3	Slowly slide the disk cartridge into the receiver assembly and make certain there is no internal resistance to its insertion.
4	Raise the disk cartridge receiver handle to the up or loaded position to seat the disk armature plate securely on the spindle assembly. Do not force the handle. When the disk cartridge is properly loaded, a disk carriage microswitch places the disk in the ON position.
5	Close the disk cartridge access door. NOTE An interlock switch is activated when the disk cartridge is properly inserted. However, if the switch is not activated, the drive is not put in the ready condition. If the switch should transfer to its unoperative position during an otherwise normal operation, the disk will immediately sequence down to a stopped condition and the SAFE light will be illuminated.
6	Set the START/STOP switch to the START or up position to put the disk drive system into operation. A disk handle interlock will be activated to ensure that the handle cannot be raised during normal operation. The drive motor is then energized to bring the disk up to its proper operating speed.
7	A 90 second delay occurs after the disk has reached its operational speed of 1500 rpm allowing it to reach a stabilized condition. During this delay, the read/write heads are loaded on data track 000.
8	After the disk has stabilized, the READY lamp will illuminate, indicating that it is ready for actual operation.

3.7.3 Disk Cartridge Removal

The following procedure should be followed for disk cartridge removal:

Step	Procedure
1	Make certain the dc power is ON.
2	Set the START/STOP switch to the STOP or down position. In this position, the read/write heads are unloaded and the read/write head responsyn positioner assembly moves the heads to seek data track -003. The disk now begins its deceleration cycle which, when completed, will be in a SAFE condition.

Step	Procedure
3	After disk drive rotation has stopped, the disk cartridge receiver interlock is released and the SAFE lamp illuminates.
4	Open the disk cartridge access door and pull the cartridge receiver handle down.
5	Remove the disk cartridge from the cartridge receiver assembly.

3.7.4 Disk Cartridge Handling

The 0 and 1 surfaces of the aluminum, oxide-coated disk platter are sensitive to foreign particles introduced into the interior of the disk cartridge. For this reason, the disk cartridge read/write head access door and the air intake valve must not be opened after the disk cartridge is removed from the disk system. The only exception is when the disk must be cleaned and this must be done in a "white room" atmosphere.

The disk cartridge must not be subjected to top loading or protruding objects when removed from the machine because deformity of the cartridge-centering diaphragm can result. Damage to this diaphragm renders the cartridge useless and damage to the read/write heads is possible.

The aluminum disk contains valuable data pertinent to a user's program and therefore must be protected. To maintain extended life of the disk cartridge, the following steps should be followed:

Step	Procedure
1	Keep the external surface of the disk cartridge free of dust and dirt contaminants by wiping it with a lint-free cloth.
2	Replace a disk cartridge with broken or damaged access doors.
3	A preventive maintenance routine should be established to ensure that foreign particles have not entered the disk cartridge. If the disk cartridge becomes damaged or its interior becomes dirty, it should be replaced.
4	The disk cartridge cover must not be depressed while the disk is in operation because it will cause the cartridge cover to strike the surface of the disk rendering it useless.
5	Beverages should not be placed in close proximity to the disk. If a beverage is spilled onto the disk, it should be examined by DEC Field Service personnel to determine the extent of damage and whether the disk can be operated.
6	Do not smoke near the disk since ashes can damage the disk surface.
7	When the disk cartridge is removed from the disk cartridge receiver assembly, the disk cartridge access door and air valve should be checked to be certain they are securely closed. If open, a slight pressure on their external surfaces will close them.

Step	Procedure
8	When the disk cartridge is introduced into the installation room environment where the temperature change may be extreme, approximately two hours should be allowed for conditioning of the aluminum disk platter. A conditioning period of approximately 15 minutes is normally all that is necessary. If disk conditioning is not allowed, track registration and data recording retrieval errors can occur.

3.7.5 Storage and Shipping of Disk Cartridges

Disk cartridges that receive the most use should be stored in the room where the Disk is installed or in a similar environment. The suggested environmental conditions are 65°F to 90°F (32°C) and 20% to 80% relative humidity. A disk cartridge must be conditioned to the environmental conditions of the room it is to be operated in. Disk cartridges are best stored in their original shipping containers on flat surfaces, free of other objects.

NOTE

Only when the disk cartridges are in their original shipping containers can they be stacked or stored on edge.

When shipping disk cartridges, the original shipping containers must be used.

Disk cartridge specifications are described in Table 3-2.

Table 3-2
Disk Cartridge Specifications

Description	Specification	
Disk Cartridge (with cover)	Diameter: Height:	15.0 in. 1.5 in.
Shipping Container	Length: Height:	19.9 in. 6.5 in.
Temperature Range	Shipping: Operating: Relative Humidity:	40°F (-10°C) to 150°F (65°C) 65°F (18°C) to 90°F (32°C) 20% to 80%

Chapter 4
Programming

The software written for the RK8 Disk has increased its capabilities and expandability; it has also provided device-independent access to as many as fifteen I/O devices. It is possible to write a device handler in one, or in some cases, two core pages and interface it to the system software.

The user's program can call various monitor services, including file manipulation and program chaining with access to standard DEC programs.

To build the RK8 Disk System and to load programs, the user requires a minimum of 8K of core memory, at least one RK8 Disk and either a high-speed paper tape reader or DECtape.

4.1 DISK OPERATION

Before the disk becomes fully operational, a 90 second time delay occurs allowing the disk to reach a speed of 1500 rpm. During this time delay the magnetic read/write heads are loaded and flying above the surface of the disk and are in the data track 000 or home position.

Access to any of the 200 data tracks (203 with three spare data tracks) is achieved in an average positioning time of 134 ms. The read/write head responsyn positioner assembly operates in a sequential stepping mode with a minimum positioning time of 2 ms.

Frequency of data transmission is 720K data bits per second. Double-frequency recording is used with an overall frequency of 1,440,000 bits per second, including clock and data bits.

When the disk is operating, internal circuits are continuously monitoring the disk cartridge platter speed so that if the disk falls below speed, the RK01 automatically cycles down providing appropriate indications through the Disk Control. A hysteresis main drive motor maintains disk speed at a uniform rate.

4.2 PROGRAMMING

A normal programming sequence is as follows:

a. The word count and current address data is placed in the word count and current address registers.

b. The command register is then loaded. Normally only the unit number, extended memory address, or seek mode is changed. The change in the interrupt status or the rewriting of the protect and status word, normally does not take place.

c. The disk track, surface, and sector data is loaded from the AC, and the read, write, or parity check instruction is executed.

d. Program interrupts occur when either the data track is found, the data transfer is complete, or an error flag is raised.

NOTE

Any errors that occur halt data transfers.

4.3 FORMAT DESCRIPTION

Each new disk cartridge is considered to be void of useful data; therefore, track and sector information must be written on the disk before it can be used by normal programs. A disk surface is divided into 203 data tracks; each track being further divided into 16 parts called sectors. Sectors 0 to 7 are on cartridge side 0 and sectors 10 to 17 are on cartridge side 1. Each individual sector contains enough area to store track and sector information plus 256 data words, and each sector can be addressed by the RK01 control.

If a normal data transfer is made starting from sector 0, 4096 data words can be transferred: 2048 words on side 0 and 2048 on side 1. Transfer of data blocks that total more than the number of sectors from the starting sector to sector 17 is an error indicated by the raising of the track capacity error flag.

Within a sector, the area is subdivided into a two-word header region, a 256-word data region, an LP word, and a postamble (see Figure 4-1). The two word header contains track and sector information. The 256-word data region contains the data words. In addition, a 12-bit longitudinal parity word and a 12-bit postamble guard word provides a convenient area to turn off the write amplifiers.

4.3.1 Sector Detail

Each sector, shown in Figure 4-2, is written with an area of data zeroes in a preamble region, a data one for a sync bit, two 12-bit plus parity header words, another area of data zeroes (preamble before data), another data one for a sync bit, 256 12-bit data words, one 12-bit longitudinal parity word, and a 12-bit postamble word.

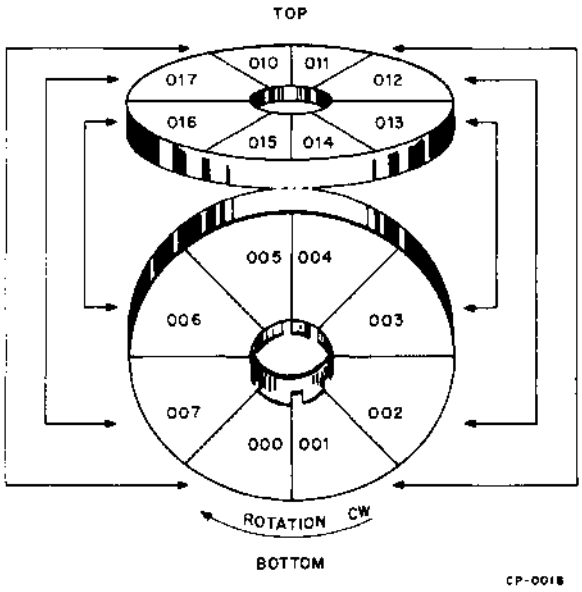


Figure 4-1 Disk Surfaces 0 and 1 Diagram

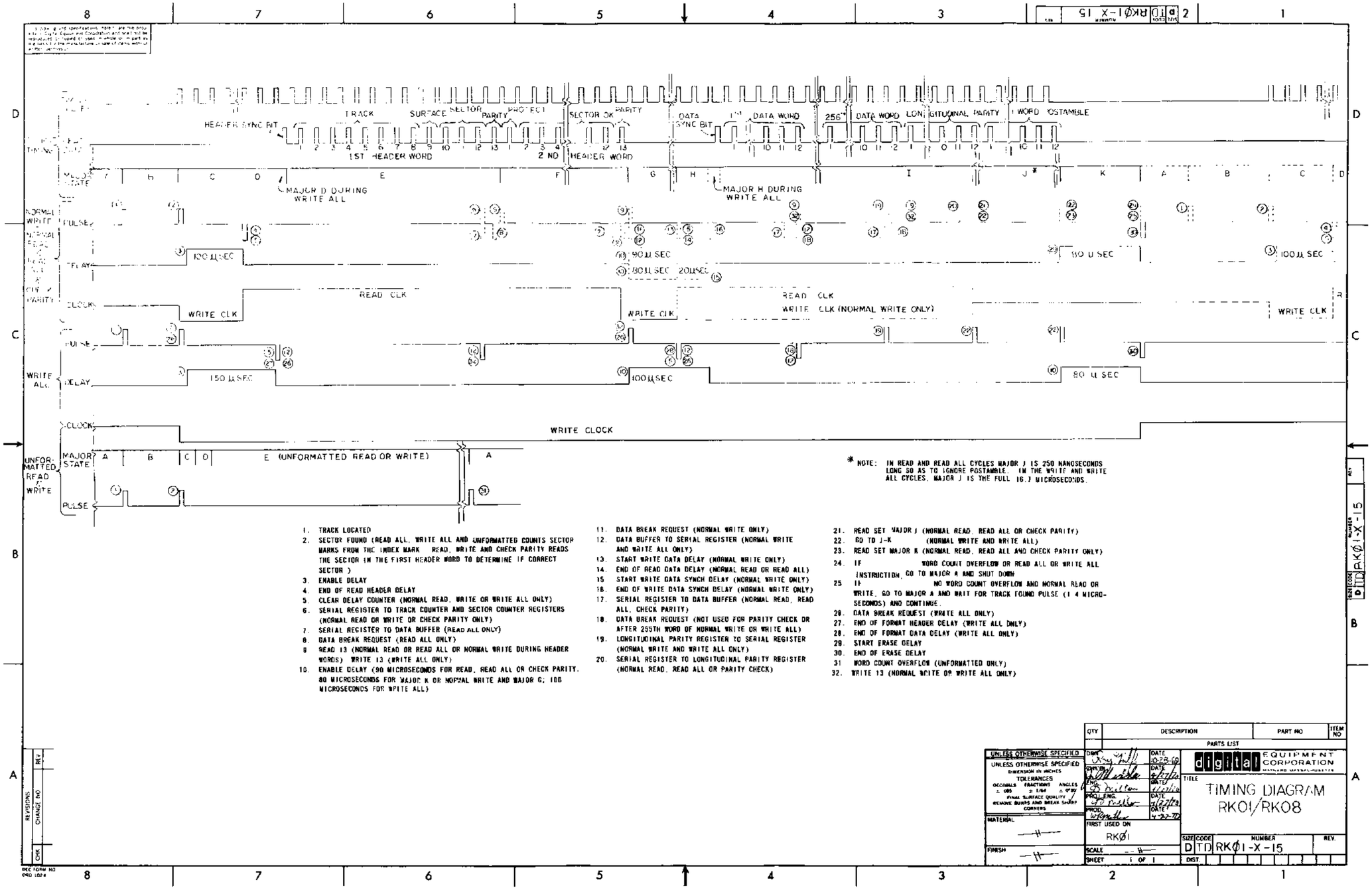
During a read cycle, the preamble region allows circuits to synchronize on the time pulses without being disturbed by data 1s. The first data 1 read after the first preamble region signifies that the region immediately following contains header information. Similarly, the preamble region following the header words and prior to the first data bit, is used for synchronization on timing pulses and the first data 1 bit after this region of data 0s signifies that data follows immediately.

Since the disk sector is divided into two areas, header and data, a read or a write function can be carried out after reading and checking the two header words. The preamble region between the header words and data is used to switch circuits from read to write when performing a normal write; therefore, during a normal write the two header words are read and checked by the control, the preamble region which follows is used to switch to write, and the 256 words of data plus longitudinal parity and postamble words are written.

NOTE

The two header words are not read into the computer during a normal read or write.

Normal read or write instructions are executed when bit 5 of the command register is 0; however, when this bit is a 1 and the sector protect switch is off, both the header words and the data region are available to the program as a 258 word data block. Having both the header words and data region enables a program to "format" the disk by writing the header words and reading them to ensure they were written correctly.



* NOTE: IN READ AND READ ALL CYCLES MAJOR J IS 250 NANOSECONDS LONG SO AS TO IGNORE POSTAMBLE. IN THE WRITE AND WRITE ALL CYCLES, MAJOR J IS THE FULL 16.7 MICROSECONDS.

1. TRACK LOCATED
2. SECTOR FOUND (READ ALL, WRITE ALL AND UNFORMATTED COUNTS SECTOR MARKS FROM THE INDEX MARK. READ, WRITE AND CHECK PARITY READS THE SECTOR IN THE FIRST HEADER WORD TO DETERMINE IF CORRECT SECTOR.)
3. ENABLE DELAY
4. END OF READ HEADER DELAY
5. CLEAR DELAY COUNTER (NORMAL READ, WRITE OR WRITE ALL ONLY)
6. SERIAL REGISTER TO TRACK COUNTER AND SECTOR COUNTER REGISTERS (NORMAL READ OR WRITE OR CHECK PARITY ONLY)
7. SERIAL REGISTER TO DATA BUFFER (READ ALL ONLY)
8. DATA BREAK REQUEST (READ ALL ONLY)
9. READ 13 (NORMAL READ OR READ ALL OR NORMAL WRITE DURING HEADER WORDS) WRITE 13 (WRITE ALL ONLY)
10. ENABLE DELAY (90 MICROSECONDS FOR READ, READ ALL OR CHECK PARITY. 80 MICROSECONDS FOR MAJOR H OR NORMAL WRITE AND MAJOR G; 100 MICROSECONDS FOR WRITE ALL)
11. DATA BREAK REQUEST (NORMAL WRITE ONLY)
12. DATA BUFFER TO SERIAL REGISTER (NORMAL WRITE AND WRITE ALL ONLY)
13. START WRITE DATA DELAY (NORMAL WRITE ONLY)
14. END OF READ DATA DELAY (NORMAL READ OR READ ALL)
15. START WRITE DATA SYNCH DELAY (NORMAL WRITE ONLY)
16. END OF WRITE DATA SYNCH DELAY (NORMAL WRITE ONLY)
17. SERIAL REGISTER TO DATA BUFFER (NORMAL READ, READ ALL, CHECK PARITY)
18. DATA BREAK REQUEST (NOT USED FOR PARITY CHECK OR AFTER 255TH WORD OF NORMAL WRITE OR WRITE ALL)
19. LONGITUDINAL PARITY REGISTER TO SERIAL REGISTER (NORMAL WRITE AND WRITE ALL ONLY)
20. SERIAL REGISTER TO LONGITUDINAL PARITY REGISTER (NORMAL READ, READ ALL OR PARITY CHECK)
21. READ SET MAJOR J (NORMAL READ, READ ALL OR CHECK PARITY)
22. GO TO J-K (NORMAL WRITE AND WRITE ALL)
23. READ SET MAJOR K (NORMAL READ, READ ALL AND CHECK PARITY ONLY)
24. IF WORD COUNT OVERFLOW OR READ ALL OR WRITE ALL INSTRUCTION, GO TO MAJOR A AND SHUT DOWN
25. IF NO WORD COUNT OVERFLOW AND NORMAL READ OR WRITE, GO TO MAJOR A AND WAIT FOR TRACK FOUND PULSE (1.4 MICROSECONDS) AND CONTINUE.
26. DATA BREAK REQUEST (WRITE ALL ONLY)
27. END OF FORMAT HEADER DELAY (WRITE ALL ONLY)
28. END OF FORMAT DATA DELAY (WRITE ALL ONLY)
29. START ERASE DELAY
30. END OF ERASE DELAY
31. WORD COUNT OVERFLOW (UNFORMATTED ONLY)
32. WRITE 13 (NORMAL WRITE OR WRITE ALL ONLY)

QTY	DESCRIPTION	PART NO	ITEM NO

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

DRWN — DATE 10-28-69
CHK'D — DATE 4-27-70
ENG. — DATE 4/27/70
PROJ. ENG. — DATE 4/27/70
PROD. — DATE 4-27-70
MATERIAL —
FIRST USED ON RKØ1
FINISH —
SCALE —
SHEET 1 OF 1

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
TIMING DIAGRAM
RKØ1/RKØ8

SIZE D | CODE TD | NUMBER RKØ1-X-15 | REV.
DIST.

REVISIONS: REV. | CHANGE NO | CHK

DEC FORM NO CKD 1024

Figure 4-2 Sector Timing Diagram (D-TD-RK01-X-15)

4.3.2 Formatting a New Disk

A new disk cartridge is void of all useful data and must be formatted. The formatting procedure is described in detail in the following section. The programmer is not required to know the format in great detail; it is sufficient for him to know that a 258 word block per sector is written when formatting the disk.

The formatting mode is chosen by setting bit 5 of the command register to a 1 and setting both the Disk Drive and sector Write Lockout switches to OFF.

In formatting mode, a maximum of 258 words are transferred, so the word count register is loaded with the 2's complement of 258.

The first data word to be written is in the same format as the track, surface, and sector address in a normal read, write, or parity check instruction. The second data word to be written is the sector protect and sector no good word which can be written as zeroes.

The next 256 words to be written are normal data words, whose values are not important in formatting.

The programming sequence is identical to that presented in the beginning of Section 4.3, except that 258 data words per sector are written. The two extra words are the header words which format the disk.

4.3.3 Effects of Errors on Data

The RK8 Disk is a highly reliable system, however, it is important for the user to know what happens to data when errors occur.

4.3.3.1 Control Busy Error - This flag aids the programmer in debugging a program. The control busy error flag indicates that the program issued an IOT instruction while the RK8 System was busy; this affects the correct operation of the system and aborts data transfer. To determine the effect the IOT has on data requires a complete analysis of the particular IOT and the state of the Disk Control when the IOT was issued.

4.3.3.2 Time Out Error Flag - This flag indicates that the control is "hung up"; it can be assumed that the data transfer was no good and a programmed data compare should be initiated.

4.3.3.3 Parity or Timing Bit Error - These two error signals produce parity error which can occur in either the header or data region.

If an error occurs in the header region during a read or write cycle, the error indicates that data transfer has not started; if an error occurs in the data region during a read cycle (the error can not occur in the data region during a write cycle), the data is incorrect. In either case, five attempts should be made to first, complete the data transfer before rewritting the header, or second, rewrite the data if the error occurs in the data region.

During a read operation, the program can determine whether the error is in the header or data region by checking the current address register which remains set to its initial value if a header error is still occurring.

4.3.3.4 Data Rate Error - This error flag indicates that the disk control was not granted access to the computer memory, and data was lost.

4.3.3.5 Track Address Error - This error flag occurs when the data track number read from the first header word does not agree with the data track selected by the program. At this point, data transfer is not started, but the error flag indicates to the user that the Disk Control and the Disk Drive do not agree on the track which is being read or written. This error can be corrected by issuing IOT instruction DCLA-6751 which clears the selected disk back to data track 000 and reinitializes the control.

4.3.3.6 Sector No Good Error - This error flag indicates that one of the data bits, 1 through 5, of the second header word was set to a binary 1 because of either a read error, or because a program had written these bits as a 1 indicating that the sector in question had a physical flaw and a permanent read/write error in which case, data transfer does not start.

4.3.3.7 Track Capacity Exceeded Error - This error flag indicates that the control filled up sector 17, and the word count register did not overflow. In this case, data transfer is successful and the number of data words not transferred is retained in the word count register.

The user can choose another disk address and continue the data transfer without having to reinitialize the word count and current address registers.

4.3.3.8 Select Error - This error flag indicates that either a nonexistent disk was selected or a disk was selected that is out of operation. A disk permanently out of operation requires user intervention to correct the situation. It can be temporarily out of operation because the disk has just been turned on, or because it has proceeded to an address less than data track 000 or greater than data track 202.

Both of these errors are only seconds long and readily come to the attention of the user. Note that the control does not respond to a read, write, or seek track instruction if an error or error flag has not first been cleared.

NOTE

If an error or an error flag has not been cleared and an attempt is made to read, write, or seek a data track, the control will not clear the error flag and will not execute the IOT command. In this case, the BUSY flag remains zero, the TRANSFER DONE flag is set, and the error flags remain set.

The select error flag, in particular, causes programming difficulty because it can not be cleared by a clear status level until the selected drive is available. In cases where the disk is cycled up or it is selecting a data track that is out of bounds, the select error flag can be cleared by the clear status signal when a disk drive is available.

4.3.4 First Header Word

The first header word used during normal read or write is the track, surface, and sector address, which is identical to the format of the address held in the computer accumulator when executing a read or write instruction. After being read, the first header word is compared to the track address registers of the control to ensure that the correct track is being accessed.

The sector portion of this header word is compared with the sector address requested by the program. If they are not equal, the control resets itself until the next sector. If they are equal, the transfer of 256 data words is completed. If another 256 data words are to be transferred and the word count is not equal to 0, a 1 is added to the sector address requested by program and this new sector is found in the same manner as before.

Note that sectors are identified by data written by a program, therefore, sector numbers do not have to be sequential but can be interleaved for maximum throughput.

4.3.5 Second Header Word

The second header word, when read during a normal read or write mode, is checked as follows:

If bit 0 is equal to a 1, the SECT PROT switch is ON and a normal write mode is requested, data transfer is terminated, and the WRITE LOCK ERROR flag is raised. If these conditions are not true, continue data transfer.

If any of bits 1 through 5 is a 1 during a normal read or write, data transfer is terminated and the SECTOR NO GOOD flag is set. These bits are set to a 1 to indicate that the sector has a permanent flaw and data cannot be reliably read from or written onto the disk surface.

Bits 6 through 11 are unused.

NOTE

The previously described functions (checking for correct track address, finding sector numbers, checking parity, write lock and sector no good bits) are all performed automatically and require no intervention by the program when carried out.

4.3.6 Accessing of Disk Sectors

Accessing disk sectors during a read/write cycle is accomplished through the formatting program, which should be sequential if large blocks of data are to be transferred (refer to Table 4-1). The data transfer rate is 4096 words in 40 ms.

Table 4-1
Sector Format Program

Surface 0 Track 000 to 199	Surface 1 Track 000 to 199
0	10
1	11
2	12
3	13
4	14
5	15
6	16
7	17

The following sector format should be used for calculations performed on data between data transfers. This sector format does not require the disk to make one revolution before the next sector appears (refer to Table 4-2). This format allows a time duration of 10 ms to occur between sectors with 4096 words being transferred in 240 ms.

4.3.7 Control Description

The RK01 Disk Control contains an up/down track address counter which maintains a count of the track number, and a track address register which is loaded from the accumulator. The track address counter holds the current location of the read/write heads and is the active track register. When the track address register is loaded by the correct IOT, the Control steps the track address counter and the Disk Drive read/write head positioner until the track address counter is equal to the track address register.

Table 4-2
Sector Format Program

Surface 0 Track 000 to 199	Surface 1 Track 000 to 199
0	10
3	13
6	16
1	11
4	14
7	17
2	12
5	15

After the RK01 Control finds the correct track, the header of the first sector that appears under the read/write head is read, and the track address portion of the header word is compared with the track address register. If they are not equal, the TRACK ADDR ERROR flag is raised and the operation terminated.

Sector selection is performed by loading a register from the accumulator with a sector number plus disk surface (0 or 1). The sector address portion of the header word is compared with the sector address register, if they are equal, the read or write operation continues. If they are not equal, consecutive sectors are read until the correct sector is located. If, after 56 revolutions, the correct sector is not located, the TIME OUT ERROR flag is set.

4.3.8 Multidisk Operations

When a drive is first selected during a normal read or write mode, and bit 5 of the command register is a 0, the control will read the track number which the read/write heads are positioned over. The information utilized is the first header word of any sector which contains the track number that the read/write heads are positioned over. This track number updates the track address counter and then executes any instructions issued from the computer. This operation is necessary only in multidisk operations and is performed so that the program is not forced to calculate a drive's current track location and to update the track address counter when switching from drive to drive.

4.4 IOT PROGRAMMING INSTRUCTIONS

The IOT instructions for controlling disk functions are shown in Table 4-3, also see Figures 4-3 through 4-6.

Table 4-3
IOT Instructions

Mnemonic	Octal	AC Bit	Function
DLDA	6731		Loads disk address (maintenance only)
DLDC	6732		Loads the command register from the AC, then clears the AC (see Figure 4-3).
DLDR	6733		Loads the track, surface, and sector address from the AC, then clears the AC. Starts to read data from the disk, if command register bit 4 = 0.
DLDW	6735		Loads the track, surface, and sector address from the AC, then clears the AC. Starts to write on the disk, if command register bit 4 = 0.
DCHP	6737		Loads the track, surface, and sector address from AC, then clears the AC. Reads data and checks parity, if command register bit 4 = 0.
DRDA	6734		Clears the AC and reads the track, surface, and sector counters into the AC. If the disk address is changing during reading, the result in the accumulator may be false.
DRDC	6736		Clears the AC and reads the command register into the AC.
DRDS	6741		Clears the AC and reads the status register into the AC (see Figure 4-4).
DCLS	6742		Clears the status register.
DMNT	6743		Loads the maintenance register from the AC and carries out the operation specified. Bits remain set until DMNT is issued with AC bits = 0 (see Figure 4-5).
		0	Transfers contents of track and surface/sector address register to counter registers.
		1	Transfers data register data to serial register.
		2	Transfers serial register data to data register.
		3	Clears AC and reads data register into AC.
		4	Shifts a 1 into the serial register.
		5	Shifts a 0 into the serial register.
		6	Unformatted disk
		7	Sector pulse
		8	Index pulse
		9-11	Not used
DSKD	6745		Skip on TRANSFER DONE flag = 1.
DSKE	6747		Skip on ERROR flag = 1.

Table 4-3 (Cont)
IOT Instructions

Mnemonic	Octal	AC Bit	Function
DCLA	6751		Clears selected disk to data track 00, then clears all control registers and flags except disk selection. TRANSFER DONE flag set when disk read/write heads are positioned on data track 000.
DRWC	6752		Clears AC, then reads the contents of the word count register into the AC.
DLWC	6753		Loads word count register from AC, then clears the AC.
DLCA	6755		Loads current address register from AC, then clears the AC.
DRCA	6757		Clears the AC, then reads the contents of the current address register into the AC.

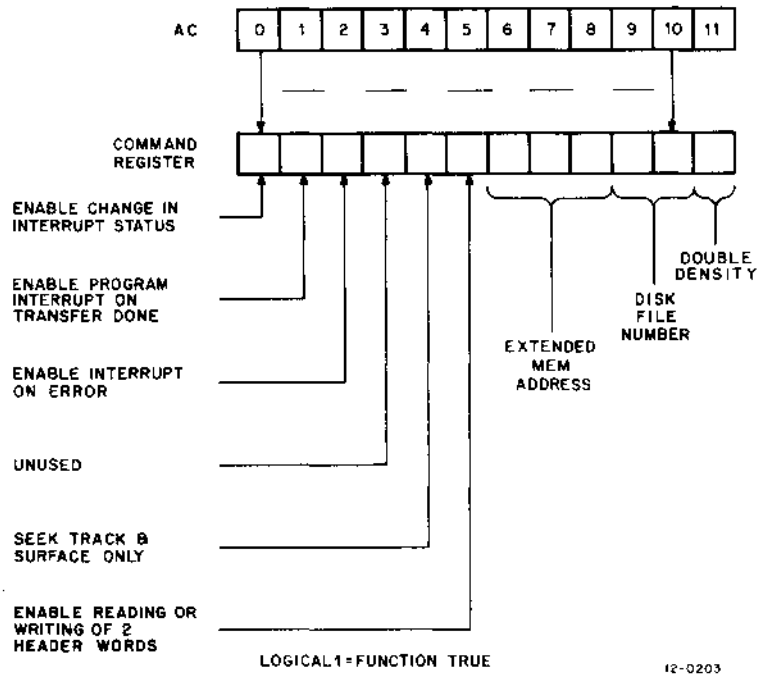


Figure 4-3 DLDC Command Register Diagram

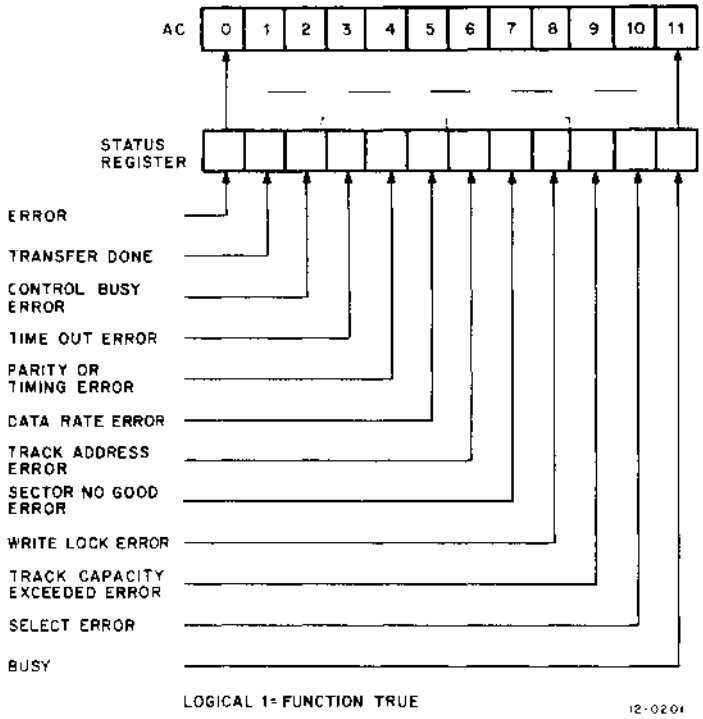


Figure 4-4 DRDS Instruction Register Diagram

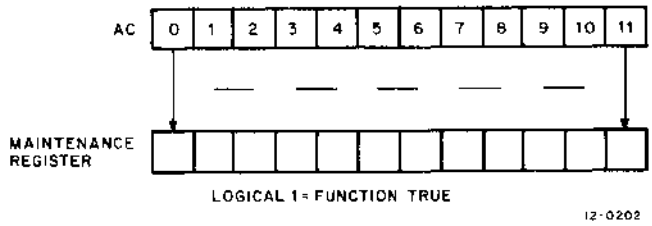


Figure 4-5 DMNT Instruction Register Diagram

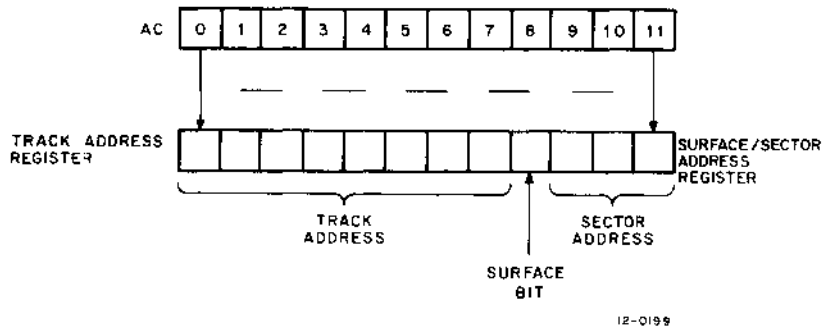


Figure 4-6 Disk Address Register Diagram

4.5 DETAILED PROGRAMMING INSTRUCTIONS

The command register is loaded from the AC, and the AC is cleared. AC bit usage is outlined in Table 4-4. The Disk IOT instructions in Table 4-4 are identical to those in Table 4-3 except that the function of each IOT is presented in greater detail.

Table 4-4
Detailed Programming Instructions

Mnemonic	Octal	AC Bits	Function
DLDC	6732	0	This bit allows changes to the interrupt status, if it is a 1. If it is 0, the interrupt status cannot be changed except by a DCLA instruction.
		1	If this bit is a 1 and bit 0 is a 1, the enable gate is set to allow a program interrupt when the TRANSFER DONE flag = 1. If this bit is a 0 and bit 0 is a 1, the enable gate is reset.
		2	If this bit is a 1 and bit 0 is a 1, the enable gate is set to allow a program interrupt when the ERROR flag = 1. If this bit is a 0 and bit 0 is a 1, the enable gate is reset.
		4	If this bit is a 1, seek the data track specified in the track address register but do not start data transfer. If this bit is a 0, seek the track, surface, and sector, and start the data transfer.
		5	If this bit is a 1, the header word is accessible to the programmer. Read Mode: The two header words plus data are read with the maximum number of words (258). The word count register determines the minimum number of words. Write Mode: The two header words plus data are written, and the protect switch must be in the OFF position. When the two header words are changed, data in that sector must be rewritten. The maximum and minimum number of words written is the same for the read mode. Since the protection bit is rewritten, formatting is the method used to "sector protect" an area of the disk; therefore, the program used to protect areas on the disk must be capable of formatting the disk and making certain that the sectors of the disk do not have irregularities that will cause read errors.
		6	Extended Memory Address 0
		7	Extended Memory Address 1

Table 4-4 (Cont)
Detailed Programming Instructions

Mnemonic	Octal	AC Bits	Function
		8	Extended Memory Address 2
		9 & 10	00 = Disk 0 01 = Disk 1 10 = Disk 2 11 = Disk 3
		11	Reserved for future double-density disks; 0 is for the lower data tracks and 1 is for the upper data tracks.
DLDR or DLDW or DCHP			Loads the track, surface, and sector address from the accumulator. The control executes the command register instructions. If track seek only has been selected, the TRANSFER DONE flag will be set when the correct track is reached.
DLDR	6733		Read Mode: After the correct track, surface, and sector number is found (see DLDW-6735), the control will read the second header word with bit 0 of this word being ignored. If any of bits 1 to 5 are set, the SECTOR NO GOOD flag is set and the read operation is terminated.
DLDW	6735		Write Mode: The first header word contains the track, surface, and sector address which is read by the control and compared with the selected address. If the track addresses differ, the TRACK ADDR ERROR flag is set and the write operation is terminated. If the two addresses are the same, the sector addresses are checked and if they are the same, the second header word is checked. If sector addresses are not the same, the next sector header is read until the correct sector is found. If bit 0 of the second header word is a 1 and the sector protect switch is on, the sector is protected, the WRITE LOCK ERROR flag is set, and the data transfer terminated immediately. If the bit is a 0, the rest of the header word is checked. If any one of bits 1 through 5 of the second header word is a 1, the sector has a permanent error and the SECTOR NO GOOD flag is set. The writing operation is terminated immediately. Bits 6 through 11 are unused.
DCHP	6737		The specified disk sectors are read for correct parity. The PARITY ERROR flag will be set if there is an error, the operation is terminated immediately, and the TRANSFER DONE flag is set.

Table 4-4 (Cont)
Detailed Programming Instructions

Mnemonic	Octal	AC Bits	Function
DRDA	6734		Clears the accumulator and reads the track, surface, and sector counters into the AC. This is a dynamic register that changes if a new data track or disk surface has been selected. The sector counter changes every 5 ms. The program must read these counters twice and then verify that the information is correct.
DRDC	6736		Clears the accumulator and reads the command register into the AC.
DRDS	6741		Clears the accumulator and reads the status register into the AC.
		0	ERROR flag - This flag is set when any error flags are set and control operation ceases when the ERROR flag is set, the TRANSFER DONE flag is set to 1, and the BUSY flag is set to 0.
		1	TRANSFER DONE flag - This flag is set whenever a control operation is terminated.
		2	CONT BUSY ERROR flag - Disk IOT, which would affect operation issued when control is busy.
		3	TIME OUT ERROR flag - The control did not complete an operation after 2 seconds.
		4	PARITY ERROR or TIMING BIT ERROR flag - A data, parity, or timing bit has been picked up or dropped during read mode. The word count and current address information can be used to identify the error.
		5	DATA RATE ERROR flag - The processor was busy and did not respond to a data break request within the required 13 μs.
		6	TRACK ADDR ERROR flag - The track address read from the disk did not agree with the address count register.
		7	SECTOR NO GOOD flag - The program attempted to read or write data on a sector whose header words indicated a bad sector.
		8	WRITE LOCK ERROR flag - The program attempted to write on a sector that was write protected.
		9	TRACK CAP EXC ERROR flag - The program attempted to read or write beyond sector 17_8.
		10	SELECT ERROR flag - Nonexistent drive error, position error, or drive not ready error.

Table 4-4 (Cont)
Detailed Programming Instructions

Mnemonic	Octal	AC Bits	Function
DMNT	6743	11	BUSY = 1 - This flag is in the 1 state when the control is busy, and when it goes to the 0 state, the TRANSFER DONE flag is set. AC bits 0-5, 7-8 are self-explanatory. Bit 6 (unformatted): Writes a block of memory as specified by word count and current address registers without formats. Writing starts immediately after the sector mark is sensed and continues until word count overflows. Two extra words are written at the beginning of the block of information. These words are the contents of the data register prior to initiating of the write mode. A read operation reads all data after a sector mark is sensed and continues until the word count overflows. This ability to read or write any format gives some degree of interchangeability between disk drives using different formats. With bit 6 = 1, the format written is generated by the program. Any format can be read and decoded, if the user knows the format that was read. When entering the unformatted mode of operation, the maintenance register should first be loaded with AC bit 6 before loading the command register. This is to let the command register know that any operations will not be a normal read or write and hardware reading of the first header word is not required when a different RK01-X Disk Drive is selected.
DLDA, DCLS, DCLA, DSKD, DSKT, DSKB, DRWE, DLWC, DLCA, DRCA are self-explanatory.			

Chapter 5
Theory of Operation

The theory of operation is presented in two parts, Section 5.1 describes the RK01-X Disk Drive Interface, and Section 5.2 describes the RK08 Disk Control. Each of these sections is further broken down into a description of each circuit making up the RK01-X and RK08.

The format for each Section is a) an overall description of the purpose or function of the logic, and b) a detailed description of the function of each block of logic.

The detailed description is not a gate-by-gate description but rather a description of how the block of logic fits into the total control.

5.1 RK01-X DISK DRIVE INTERFACE

The RK01-X Disk Drive Interface is a complete pluggable unit for the RK01 Disk Drive consisting of a single rack of M-Series logic modules that mount directly under the RK08 Disk Control and are connected to it by three 6-in. cables.

The RK01-X Disk Drive logic consists of format delays, drive selection, and track seek logic, all of which are described in the following sections.

The RK01-X Format, Block, Flow, and Timing Diagrams are shown in Figures II-1 through II-4.

5.1.1 Format Delays

The Format Delay logic pulses, shown in Figure II-5, provide the timing sequence for the RK08 Disk Control. Using an M405 crystal-controlled oscillator as the time-base, the DEL counter enables a selected NAND DELAY gate after counting to a specific count pattern, and then this gate is strobed by WRITE CLOCK H. The double-frequency flip-flop shown at coordinates B6 1/2 provides the Disk Drive with write information when recording data onto the disk.

The main timing pulse and time standard for the RK08 Disk Control is WRITE CLOCK H, which occurs at a 1.39 μs rate, 1/4th the 2.88 MHz oscillator rate. In addition to incrementing the DELay counter 01-64, it strobes each of the FORMAT DELAY gates.

A FORMAT HEADER and DATA DELAY output occur after the DEL counter has counted to the value which enables the DELAY NAND gate. These gates are strobed by WRITE CLOCK with the gate DELAY outputs being used in the RK08 Disk Control to continue the sequence of an operation.

When ENBL DELAY H enables the sync flip-flop at coordinates 7 1/2 A 1/2, WRITE CLOCK sets it, which in turn, enables DEL 01, allowing the DEL counter to count the WRITE CLOCK pulses which follow. After the DEL counter has counted to a pattern that enables the selected DELAY NAND gate, the next WRITE CLOCK pulse strobes the gate providing a DELAY output.

The total time delay includes the time to count to a specified value, the time to set the sync flip-flop, and the time for one more WRITE CLOCK pulse to strobe the DELAY NAND gate. For example, FORMAT DATA DELAY L takes 1.39 μs after the sync flip-flop is set to count the succeeding WRITE CLOCK H pulse; 97.3 μs to count-up until DEL 64, DEL 04, and DEL 02 are all on a 1; and 1.39 μs more for the next WRITE CLOCK H pulse to strobe the DELAY NAND gate. The total delay time is 100.08 μs, which is the time the RK08 Disk Control remains in MAJOR state G during a WRITE ALL instruction.

The DEL counter is cleared during MAJOR state C by CLEAR ALL, or after a Format DELAY pulse. The CLEAR DELAY CNTR L is pulsed through a gate enabled by a sync flip-flop, which disables the clearing of the DEL counter until after the delay pulse is issued. Signals between the interface and RK01-X Disk Control are shown in Figure 2-6.

5.1.2 Data to Disk

The M202 double-frequency flip-flop, shown in Figure II-5 at coordinates B6 1/2, provides the selected disk with DATA TO DISK, which is normally held off by R/W (0) L. The read mode is the normal control state with the R/W flip-flop on a 0. This flip-flop is set to a 1 during a write operation.

When the R/W flip-flop is first set to the 1 state, the DATA OUT flip-flop is in the 0 state. The DATA TO DISK flip-flop complements on every other pulse of the 2.88 MHz oscillator with this being the base frequency. For example, to write one data bit, DATA OUT (1) L causes the DATA TO DISK flip-flop to complement on every oscillator pulse, which is the double frequency. When this serial information is read by the discriminator circuit in the disk drive, the base-frequency pulses generate Disk Read Clock pulses and the double frequency appears as Disk Read Data pulses between the Disk Read Clock pulses (see Figure 5-1).

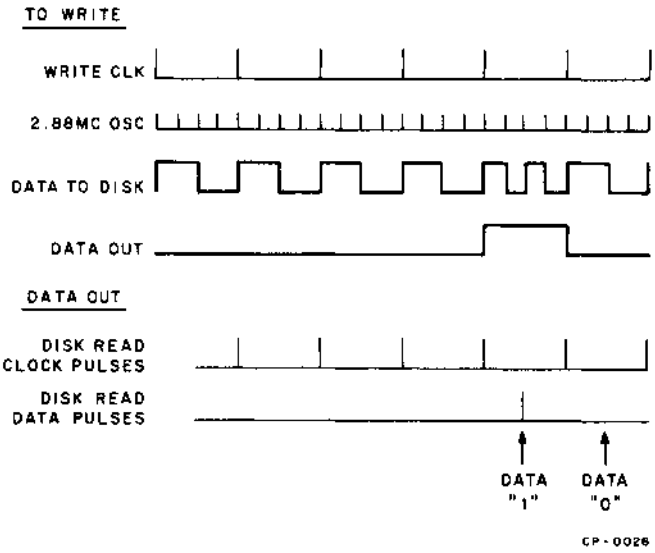


Figure 5-1 Data to Disk Timing Diagram

5.1.3 Track Seek Mode

The RK08 Disk Drive has a single pair of movable heads to access 202 data tracks; only one track is accessible at a time on either side 0 or 1 of the magnetic disk. The Track Seek logic moves the read/write heads and selects a data track because the Disk Drive itself has no logic to accomplish this. To effect this operation, it utilizes a track address register, a track counter register, a comparator, and stepping logic, which works in conjunction with the signals received from the Disk Drive.

5.1.3.1 Seek Track - The Track Seek logic, shown in Figures II-7 and 5-2, controls the seeking of a data track, loading of the track counter register when selecting a new disk drive, time-out logic, and the write protection.

Seeking a data track is initiated by IOT START; this signal is enabled by ORing either SET READ L (IOT-6733), SET WRITE L (IOT-6735), or SET CHECK PARITY L (IOT-6737) (see Figure II-14). These instructions also load the track address register from AC0-7 and the surface selection address from AC8-11, then clear the AC.

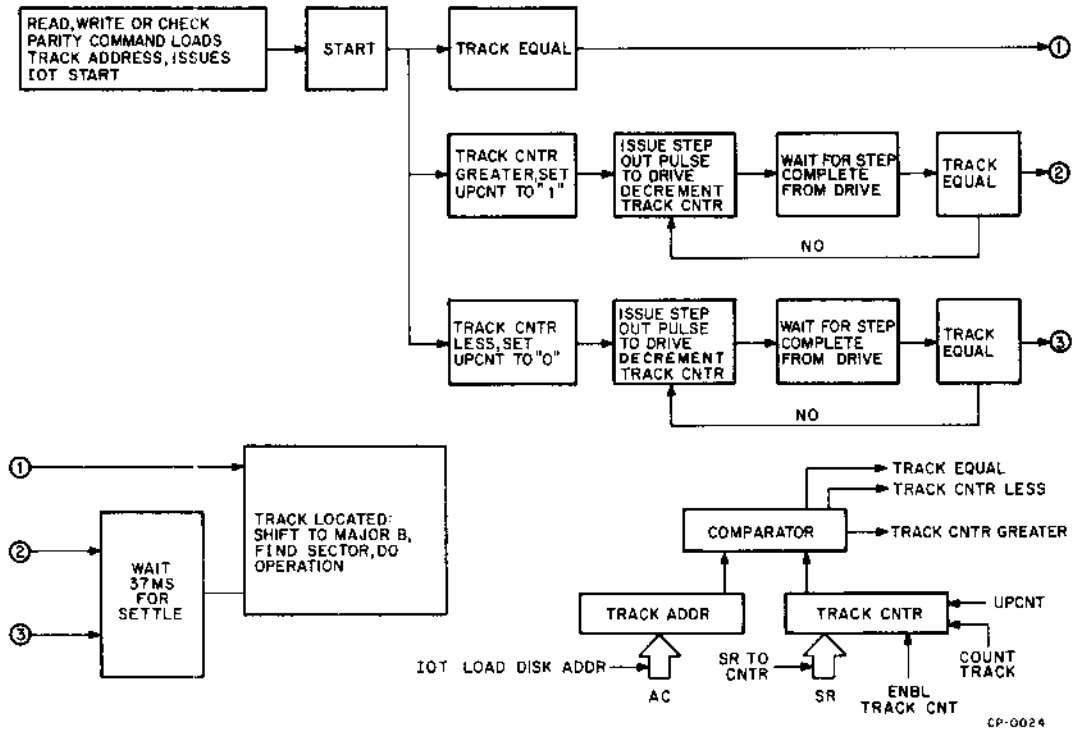


Figure 5-2 TRACK SEEK Mode

If a different data track is chosen where the track address register does not equal the track counter, the logic comparing these two registers indicates whether the disk drive should step the read/write heads in towards data track 000 or out towards data track 202. If a different data track is not chosen the heads remain on the same data track, and TRACK EQUAL remains true.

NOTE

If TRACK EQUAL is true, the signals that raise START bypass both the step logic and the 37 ms delay to generate TRACK LOCATED.

If the disk drive is to step the read/write heads either in or out, START initiates the step and strobes the UP CNT flip-flop, which makes certain that the track address counter counts in the correct direction. The track address counter counts up for STEP OUT and down for STEP IN. The track counter is incremented on the trailing edge of the stepping pulse.

After the disk drive has stepped once, it responds with STEP COMPLETE, which generates another stepping sequence if the disk drive has not reached the correct data track. If the disk drive has reached the correct data track, as determined by the status of the track address and track counter comparator network, STEP COMPLETE triggers the 37 ms time delay allowing time for head carriage mechanical movement to stop.

At the end of the 37 ms delay, reading or writing takes place, or if the instruction TRACK SEEK is executed, the TRANSFER DONE FLAG, shown on Figure II-27, is set.

5.1.3.2 FIND TRACK ZERO - Because it is necessary to reset a drive to data track 000 and to make certain that the logic is inactive while the calibration process is taking place, a disk drive is reset to data track 000 by the logic in the drive itself after either the upper or lower data track limit switch has been activated.

Therefore, to recalibrate a disk drive to data track 000, it is only necessary to drive the read/write head assembly back against the lower track limit switch.

When the program issues IOT CLEAR, FIND TRACK ZERO flip-flop is direct set forcing the read/write head assembly to step in towards data track 000. As in a normal stepping sequence, STEP COMPLETE retriggers the step logic. This stepping continues until the HOME POSITION limit switch is in the 1 state (HOME (1) H).

When the HOME POSITION switch is set, the read/write head assembly is close to the LOWER LIMIT switch. Because it is not advisable to purposely drive the head assembly at the full stepping rate into the LOWER LIMIT switch, the 37 ms time delay is tied into the stepping logic to effectively decrease the stepping rate and prevent STEP COMPLETE from directly driving the STEP IN/STEP OUT logic.

Instead, STEP COMPLETE first triggers the 37 ms delay, which then triggers the STEP IN/STEP OUT logic on its trailing edge.

When the LOWER LIMIT switch has been activated, POSITION becomes true and resets the FIND TRACK ZERO flip-flop preventing further stepping signals to the drive. Drive logic then takes over positioning the read/write heads over data track 000. When this has been accomplished, POSITION goes false, triggering a pulse amplifier which generates SET TRACK FOUND.

5.1.3.3 New Select - This logic is only used in a multiple Disk Drive system. When a new disk is selected, the track counter register will contain the data track information from the previously selected drive. Consequently, it is necessary to update the track counter so that it will contain the new track address. Updating is accomplished by setting the NEW SELECT flip-flop and going through a New Select cycle to transfer the data track portion of the first header word into the track counter. The New Select cycle is the same as a normal read cycle except it terminates at the end of MAJOR state E and the TRACK ADDR ERROR flag can not be set. Selecting a different drive sets the NEW SELECT flip-flop.

On completion of updating, at the end of MAJOR state E, RESET NEW SELECT resets the NEW SELECT flip-flop. If IOT READ, WRITE or CHECK PARITY was issued during the New Select cycle, the BUSY flip-flop would be set and at the end of MAJOR state E, RESTART would be generated.

RESTART then performs the same function as IOT START. TRACK SEEK mode is initiated by the RESTART signal if the Track Address and Track Counter are not equal. If IOT READ, WRITE or CHECK PARITY was not issued during the New Select cycle, the control would be idle after MAJOR state E. The New Select cycle is therefore transparent to the programmer.

At coordinates A5 and A6 of Figure II-7, the logic is located which disables track counter counting while it is either being loaded or while the up count/down count line, referred to as UP CNT, is being changed. Also included as part of this logic is the 4 μs delay shown in Figure II-7, coordinates D3.

The logic that write protects an entire disk drive, which generates sector protection, and the time-out delay logic is shown in Figure II-7. If the disk drive is busy for too long a period of time because the correct track and Sector have not been found, this logic generates an error signal; therefore, the program can take action to restart an operation.

5.1.4 Track Address, Counter, and Comparator

The track address register, shown in Figure II-8, is loaded from the AC when a read, write, or check parity command is given to the RK08 Disk Control. The track address register contains the octal number of the data track on which data is to be read or written.

The TRACK CNTR normally contains the octal number of the data track to which the read/write heads are selected and either upcounts or downcounts as the heads are stepped either out or in to select a new data track.

The comparator logic, shown in Figure II-9, compares the contents of the TRACK CNTR against that of the track address register. In making the comparison, the track seek logic determines whether the track counter is greater, less than, or equal to the track address register.

5.1.4.1 Track Seek Mode - When the program issues a read, write, or check parity command, the track address register is loaded with AC bits 00-07 and the surface/sector address in the Disk Control is loaded with AC bits 08-11. The above commands clear the AC with CLEAR AC L and issue IOT START, which generates START, in turn, initiating a track seek function if the track address and track counter are not equal. If they are equal or when they become equal, TRACK LOCATED L shifts the RK08 Disk Control to MAJOR state B. The read, write, or check parity operation is performed after the correct sector has been found.

If the comparator logic raises TRACK CNTR LESS when START is issued, the UPCNT flip-flop, as shown in Figure II-8, is set to a 1, and STEP OUT L pulses move the read/write heads outward towards the center of the disk; COUNT TRACK H increments the TRACK CNTR once with each STEP OUT pulse. If the comparator logic raises TRACK CNTR GREATER, the UPCNT flip-flop is set to a 0, and STEP IN L pulses move the read/write heads inward toward the edge of the disk; COUNT TRACK H decrements the TRACK CNTR.

After the read/write head stepping motor has stepped in or out (STEP IN/STEP OUT), the logic waits for STEP COMPLETE L from the RK01-X Disk Drive before it continues. The stepping action continues until the track address and track counter registers are equal, and the comparator logic raises TRACK EQUAL. After the raising of TRACK EQUAL, the last STEP COMPLETE from the RK01-X Disk Drive initiates a 37 ms delay allowing the read/write heads to settle on the data track before TRACK LOCATED L is raised, instructing the Disk Control to continue with the operation.

5.1.4.2 Formatted Disk - During MAJOR state E of a NORMAL READ or NORMAL WRITE mode, the TRACK CNTR performs a second function. The track address portion of the first header word, shift register bits 00-07, are read into the TRACK CNTR when SR TO COUNTER H is enabled. If the comparator output raises TRACK EQUAL, the operation continues. If the information read was wrong or the wrong data track was addressed, TRACK EQUAL L will be high causing a track address error condition in the RK08 Disk Control. The status ERROR flip-flop, shown in Figure II-27, is set and the operation terminated.

5.1.4.3 Enable Track Count - The ENBL TRACK CNT H level, when low, prevents the TRACK CNT from counting when it is loaded from either the shift or the track address register.

5.1.4.4 Reset Track/Sector Counter - The RESET/TRK CNTR level, shown in Figure II-8, is generated by IOT CLEAR L when the selected drive has been repositioned over data track 000.

The RESET TRK/SEC CNTRS L is generated in the RK08 Disk Control by the maintenance instruction MAIN RESET CNTR during MAJOR state E just before shift register data is transferred to the TRACK CNTR for comparison with the track address register.

5.1.5 Disk Selection

Any one of four possible Disk Drives (see Figures II-10 and II-11) can be selected by loading bits 09 and 10 of the command register from the AC with IOT load command instruction 6732. Bits 09 and 10 are loaded to the EXT DISK 0 and EXT DISK 1 flip-flops whose outputs are decoded through four AND gates that, in turn, provide levels DISK 00 L, DISK 01 L, DISK 02 L, or DISK 03 L (see Figure II-8).

The EXT DISK 0 and 1 flip-flops are direct cleared by INITIALIZE L so that programs can be bootstrapped easily from Disk Drive 0. The level SET NON DRIVE ERROR L is issued to the Disk Control if a Disk Drive is selected that is either nonexistent or is not ready.

Writing on a Disk can be prevented by using the SECTOR PROTECT SWitch or the appropriate PROTECT 0 H through 3 H switch for the appropriate Disk Drive (see Figure II-7). During an attempted operation when the R/W flip-flop is set to a 1, PROTECT L causes the WRITE LOCK ERROR status flip-flop to be set in the Disk Control terminating the operation.

The SECTOR PROTECT SWitch prevents the Disk Control from performing a normal write. A NORMAL WRITE can be done, except on those sectors which have been write locked, by having bit 0 of the second header word formatted as a 1.

Control and Output signals for disk selection are presented in Tables 5-1 and 5-2.

Table 5-1
Control Signals to a Selected Disk Drive

Signal	Function
HEAD SELECT L	When low, data is read/written from surface 0, and when high, data is read from surface 1.
WRITE SELECT L	When low, data is written onto the disk, and when high, data is read from the disk.
ERASE L	Trims the track edges during a write operation. The tunnel erase portion of the read/write head follows the head gap.
WRITE DATA L	This is a double-frequency input to the RK01-X Disk Drive, which is written onto the disk.
MOVE FORWARD PULSE L	Steps the read/write heads out towards data track 202.
MOVE REVERSE PULSE L	Steps the read/write heads in towards data track 000.

5.1.6 Cable Terminators

The cable terminators, shown in Figures II-12 and II-13, consist of resistive loads that are clamped to prevent excursion beyond +3V and ground; these loads are driven by a cable driver.

Table 5-2
Output Signals from a Selected Disk Drive

Signal	Function
DSK INDEX PULSE L	This is a synchronizing pulse that occurs for each revolution of the disk.
DSK SECTOR PULSE L	Indicates the beginning of a sector and is raised eight times for each revolution of the disk.
DSK READ CLOCK L	These are timing pulses from the disk that are raised during a read operation and used by the RK08 Disk Drive to strobe data information.
DSK READ DATA L	These are data pulses from the disk that are raised during a read operation. Each enabled pulse generates a binary 1 and no pulse a binary 0.
DSK STEP COMPLETE L	When the read/write heads are positioned over a new data track after being stepped, this level goes low. Following this, another MOVE FORWARD or REVERSE PULSE L signal can be issued.
DSK POSITION ERROR L	When the read/write heads are driven against the stops beyond the highest data track (203 including spares) that can be addressed or off the disk past data track 000, this level is raised.
DSK HOME POSITION L	The read/write heads have been repositioned over data track 000 by the Disk Drive logic after DISK POSITION ERROR has occurred.
DSK NOT READY L	The RK08 Disk Drive is not capable of transferring data.

5.2 RK08 DISK CONTROL

Presented in the following sections is a functional description of the RK08 logic.

5.2.1 IOT Decoding

The decoding of IOT instructions (see Figures II-14 and II-15) is performed in the M103 Device Selector Modules, and in the M161 Binary-to-Octal/Decimal Decoder.

Further decoding of the IOTs is obtained by having the CODE 1H and L through CODE 7H and L outputs ANDed with the IOT instructions. This operation provides seven unique IOTs instead of the normal three with further identification possible because of the 1 μs separation between IOP pulses. The P CODE 1H through 6H pulses are used as current drivers enabling AC input gating and further decoding of IOTs, where necessary.

The IOT decoding is performed by the M102 Device Selector Modules when the Disk is connected to negative bus devices such as the PDP-8/I or the PDP-8. The Logic Mounting Panel hard-wired pin connections are shared by both the M103 and M102 Modules. In all other cases, negative bus replacements for bus receiver/transmitter modules are pin compatible.

Two nonstandard signals used in the IOT decoding network are described below:

AC STROBE L:	This signal terminates in the AC input gating 00-11 network (see Figures II-32 and II-33) as the OR function of IOTs that strobe data into the AC.
DEVICE SELECT ENABLE L:	This signal terminates in the AC MB Inverter network (see Figure II-34) where it is gated with the BAC and BMB bits to prevent the signal outputs from the M101s from changing except when enabled thereby, reducing I/O bus loading.

5.2.2 SKIP and BREAK

When the computer power is initially turned on, or its associated KEY START switch is activated, the B INITIALIZE H level generates the INITIALIZE L level; this level raises all CLEAR ALL levels, which direct set all Disk major registers and flags to their 0 state (see Figure II-16).

The B RUN (0) H level generates the signal RUN (0) L indicating that the central processor is not executing an instruction, which, in turn, direct sets the sequencer register (see Figure II-18) to the Major "A" state, and the R/W flip-flop to the 0 state (see Figure II-19). This inhibits disk operation while the central processor is halted and prevents writing of transients.

The AC CLEAR BUS L level is true when IOTs are issued to the computer accumulator clearing it after external registers are loaded or clearing it prior to being loaded from external registers. These IOTs generate the signals LOAD DISK ADDR, LOAD COMMAND, MAIN DB TO AC, AC STROBE, LOAD WC, and LOAD CA level.

ANDing the TRANSFER DONE FLAG (L) H with CODE 5 H or ANDing ERROR (1) H with CODE 7 when IOT6741 is true generates the signal SKIP BUS L; this signal causes an increment of the program counter (PC+1), which is the SKIP instruction.

If the Disk has issued a data break request, the computer responds with B BREAK (1) L level indicating that it has responded to the break request. During this break cycle, BREAK (0) L is high, and BREAK (1) L is low.

BREAK (1) L level also enables loading of BMB data into the Disk control via the M101 bus interface modules. TS1 (3) H is generated by gating BTS01 (3) H with BREAK (0) L high during a break cycle. The end of data transfers is indicated when the WC OVERFLOW flip-flop is set.

When the Disk has transferred the data address to the memory address (MA) registers in the computer during a break cycle, it changes the B ADD ACCEPTED (0) H level to a low indicating that the computer has acknowledged receipt of the Disk data address. This operation raises the ADD ACCEPTED (1) H level resetting the BREAK REQ flip-flop and removing BRK RQST L level.

The TRANSFER DONE FLAG (1) H is raised when the BUSY flip-flop goes to the 0 state, indicating that the Disk control has completed a transfer cycle (see Figure II-26).

When the INT RQST BUS L level is enabled, a program interrupt occurs. This level is raised when the Disk has completed a data transfer, the TRANSFER DONE FLAG (0) H level has gone low, and the ENBL INT DONE flip-flop is set to its 1 state. The INT RQST BUS L level is also true when the ERROR flag and the ENBL INT ERROR flip-flops are set.

AC01 (1) H and AC02 (1) H are loaded to the ENBL INT DONE and ENBL INT ERROR flip-flops, respectively. This data is clocked into the registers by ANDing together the LOAD COMMAND H and AC00 (1) H levels. Raising CLEAR ALL (1) L for either INITIALIZE L or IOT CLEAR L, (IOT-6751) direct clears these flip-flops to their 0 states.

The BRK RQST L, DATA IN H, 3 CYCLE L, and MB INCREMENT L levels are inputs to the computer. The only two inputs that are enabled by the Disk Control are BRK RQST L and DATA IN L. The 3 CYCLE L and MB INCREMENT L are inhibited by having their low-level inputs connected to +3V. Setting the BREAK REQ flip-flop to its 1 state through the SET DATA BREAK REQ H pulse, causes the BREAK REQ (0) H level to go low, enabling the BRK RQST L level. This flip-flop is cleared by ADD ACCEPTED (1) H level or CLEAR ALL (1) H.

Depending on the status of DATA IN H, data is transferred either into or out of the computer.

When the LOAD DISK ADDR H or CLEAR ALL (1) H levels (see Figure II-19) are generated, they reset the WRITE FLOP to its 0 state. The WRITE FLOP (1) L level then goes false (high) and DATA IN is true, indicating that the Disk is performing a Disk-to-processor read operation. For write operation, the WRITE FLOP is set to a 1.

During TS3 when WRITE FLOP (1) H is true, the LOAD DB L pulse is generated, which loads the Data Buffer from the levels generated by the computer memory buffer ANDed with BREAK (1) L.

After the 12 data bits have been read during a read operation, the SET DATA BREAK REQ H pulse sets the BREAK REQ flip-flop to the 1 state. If the BREAK REQ flip-flop is already in the 1 state, the Data Rate ERROR L pulse is generated to set an error flag.

5.2.3 Maintenance Register

The maintenance register (see Figure II-17) provides the signals DISK ADD TO COUNTER, MAIN DB TO SR, MAIN SR TO DB, MAIN DB TO AC, MAIN (1) TO SR, MAIN (0) TO SR, MAIN SECTOR PULSE, and MAIN INDEX PULSE to test for their proper operation. When these control functions are used in conjunction with IOT instructions for loading and reading of the registers in the RK08, it is possible to verify 90 percent of the associated control logic circuitry without having an RK08 Disk connected on-line.

The UNFORMATTED signal is decoded by AC bit 06 of the maintenance register, which signifies to the command register that any operation will not be a normal read or write, and hardware reading of the first header word is not required when a different Disk drive is selected.

The two IOT pulses of the IOT instruction 6743 are used to load and execute the function of the maintenance registers. The IOP1 pulse loads the maintenance registers, and IOP2 executes the specific register function. The function of each output from the maintenance register is described in the logic section where the signal is terminated.

5.2.4 Major Sequencer Register

The state of the major sequencer register (see Figure II-18) controls each step that the RK08 disk control progresses through as it executes a read or write function. Each progressive step is represented by a specific state of the major sequencer, which defines the disk format. Refer to Figure II-3, Sections 5.2.1 and 5.2.3 for more detailed information on data flow and basic format.

The major sequencer or major state register is a shift register that shifts a binary 1 from left to right, starting with major state A and terminating at major state K. When the command RESET MAJOR is issued, it resets the register to major state A, which is the idle state of the Disk Control. When the first SHIFT MAJOR STATES pulse is raised, major state A is set to its 0 state, and major state B is set to its 1 state.

Major state registers A through K are sequentially shifted, one at a time, for each SHIFT MAJOR STATES pulse. This pulse is strobed by any one of the 16 READ/WRITE SET MAJOR inputs to the two eight-input NOR gates. Two different inputs enable the gates: the FORMAT, READ, or WRITE DATA DELAY timing pulses from the RK01 Disk Drive; and the signal from the previous major state. The data

delay timing pulse is the last pulse from the previous major state. For example, it is the end of a time delay or the 13th write clock pulse, WRITE 13, when writing a header word.

The SET MAJOR D or E L level is used in the UNFORMATTED mode to skip from MAJOR states C to D to E for each clock pulse; nothing is done in MAJOR STATE D during an unformatted read or write operation.

When the READ SET MAJOR E and I pulses are raised, data read during MAJOR STATE D or MAJOR STATE H will be true only when the HEADER and DATA SYNC BIT pulses are detected. These sync pulses are written before the header and before the 256 block of data words. Each pulse is detected as being the first read data signal.

Major state registers B through K are direct set to their 0 state by either CLEAR ALL 2 L, RUN (0) L, or ERROR (1) L, at the same time Major state register A is direct set to its 1 state.

5.2.5 R/W Command, Find Sector, and End Transfer

The read/write command, find sector, and end transfer logic (see Figure II-19) are made up of the command register, the R/W flip-flop, which controls the read/write signal to the disk, the ERASE flip-flop, the logic which determines whether a data transfer should continue or stop, and the CHECK SECTOR logic, which determines whether the correct sector has been found.

The decoded signals READ ALL, WRITE ALL, NORMAL READ, NORMAL WRITE, and UNFORMATTED are the instructions which the disk control must execute. The input to the decoder network is the output from the WRITE FLOP, which when set to a 1 is a write cycle, and when set to 0 it is a read cycle.

The ACCESS HEADER flip-flop is set by LOAD COMMAND, which originates in the IOT decoding network (see Figures II-15 and II-16), and the UNFORMATTED signal which originates in the maintenance register (see Figure II-20). CHECK PARITY is set in the IOT decoding network, as shown in Figures II-14 and II-15, by IOT6737 and is used to inhibit data break requests during a READ instruction (see Figure II-16).

The SEEK TRACK flip-flop is set from the command register and signifies to the RK01 control that a specific data track is to be found but no data is to be transferred. The signal is terminated in the RK01-X Disk Drive.

The R/W flip-flop determines whether the disk drive and control is either reading or writing at any instant of time. When the DLDW instruction is issued, the program can call for a write cycle. Although the WRITE flip-flop is immediately set, the R/W flip-flop is not set until MAJOR state C is entered for a WRITE ALL or UNFORMATTED WRITE cycle, or MAJOR state H for a NORMAL WRITE cycle.

The ERASE flip-flop, which controls the erase time to the disk drive, is set at the same time as the R/W flip-flop but is not cleared until the end of MAJOR state K, whereas the R/W flip-flop is cleared by MAJOR state K. Both flip-flops are direct cleared by ZERO SEQUENCER, which also clears all major control flip-flops in the RK08 Disk Control.

The decoded UNFORMATTED WRITE and NORMAL R/W signals are terminated in the read and write circuitry shown in Figures II-21 and II-22.

After the correct data track is found during MAJOR state A, TRACK LOCATED is generated putting the RK08 Disk Control in MAJOR state B. The SET MAJOR B and RESET MAJOR level make the decision whether to go to MAJOR state B and continue the operation, or to reset the major sequencer register to MAJOR state A. If the operation is to be terminated, the RK08 Disk Control remains in MAJOR state A. If it is seeking a sector, it will shift to MAJOR state B and wait for a sector pulse. The flip-flop at coordinates A3, Figure II-16, is direct set by FIND NEXT SECTOR, which is generated during MAJOR state E of a NORMAL READ or NORMAL WRITE cycle. When set, it first indicates that the first header word was read, then it checks to see if the correct sector was found, and if it was not found, it then checks the next succeeding sector. FIND NEXT SECTOR also resets MAJOR SEQUENCER to MAJOR state A.

At the end of MAJOR state E after the 13th BIT clears the Major Sequencer to Major state A, READ 13 generates set Major B. In MAJOR state B, the RK08 Disk Control waits for the next sector pulse then reads another header word to check for the correct sector. It must be noted that this logic is used only during a NORMAL READ or NORMAL WRITE cycle.

The sync flip-flop at coordinates B4, Figure II-16, is set to its 1 state by ERASE DELAY after a transfer of 256 words of data when WC OVERFLOW and ACCESS HEADER signals are both false. At the same time, INCR SECTOR ADDR is raised incrementing the sector address register. At the end of ERASE DELAY, the MAJOR SEQUENCER is always reset to MAJOR A. With the sync flip-flop set to its 1 state, the next WRITE CLOCK pulse generates MAJOR SET B. If the cycle is NORMAL READ/WRITE and word count has not overflowed (WC OVERFLOW (1) L), another cycle is started, INCR SECTOR ADDR is raised, and the sector address register is incremented by 1. In this manner, 16 sectors can be transferred without program intervention once the transfer has been started.

Data transfer is terminated if ACCESS HEADER is a 1 during a READ ALL or WRITE ALL mode, if WC OVERFLOW is a 1 when ERASE DELAY occurs, if there is an error, or if WC OVERFLOW is a 1 when UNFORMATTED is a 1.

The CHECK SECTOR logic performs two main functions, first it checks for the correct sector during a READ ALL, WRITE ALL or UNFORMATTED mode; second, it initiates a major sequencer transfer from MAJOR state B to MAJOR state C during the NORMAL R/W mode.

If an instruction is a READ ALL or WRITE ALL and either ACCESS HEADER or UNFORMATTED are raised, the WAIT INDEX flip-flop is set by IOT START H. With this flip-flop set, the RK08 Control will seek and find the correct data track but will wait in MAJOR state B until the index pulse from the disk drive appears. The disk drive index pulse generates CLEAR SECTOR L, which clears the WAIT INDEX flip-flop and, at the same time, strobes the direct set side of the CHECK SECTOR flip-flop. In MAJOR B, when accessing the header words or when in the unformatted mode, sector pulses are counted. The CHECK SECTOR flip-flop is set because once a sector pulse is detected, time must be allowed for the sector counter to settle before it checks to see if it is equal to the sector address.

The CHECK SECTOR output terminates in the format delay logic shown in Figure II-5.

At the end of a short time delay, SECTOR SYNC DELAY returns to reset CHECK SECTOR flip-flop to its 0 state and strobe SECTOR EQUAL.

When the sector address and sector counter are both equal, the control enters MAJOR C. If the address and counter are not equal, the control stays in MAJOR B until the next sector pulse appears, at which time COUNT SECTOR is again raised, setting the CHECK SECTOR flip-flop.

SET MAJOR C is enabled by the SECTOR SYNCH PULSE if a NORMAL R/W instruction is issued or the NEW SELECT flip-flop level is set to a 1. The SECTOR SYNCH PULSE occurs for each sector pulse from the Disk drive.

5.2.6 Read

The logic shown in Figure II-20 provides the timing, synchronization, and control levels for reading data from the disk into the shift register and data buffer. Also included in Figure II-20 is the error checking logic and the logic to strobe the block counter, which determines the end of a block of 256 data words.

The logic at coordinates A6 synchronizes the disk control with READ CLOCK and READ DATA. Prior to synchronization, the control and disk information is asynchronous. The logic at coordinates B4 controls the shifting of data (SHIFT SR) into the shift register and generates WORD PARITY. Logic at coordinates A-D1 checks for errors and the end of a block of 256 data words; while logic at coordinates D4 generates SR TO DB and READ FROM LP after the 12th data bit has been accumulated in the shift register.

Because the disk drive's idle mode of operation is read, the read signals must be inhibited so that extraneous data will not be read into the shift register. Therefore, DISK READ DATA is gated generating DATA only during MAJOR states E, F, and I. DATA then sets the SHIFT INPUT flip-flop only

when the correct information is present on the disk. DISK READ CLOCK also appears only during MAJOR states D, E, F, H, and I. The synchronization flip-flop at coordinates A6 ensures that the READ CLOCK is a full pulse.

The MISS PULSE flip-flop is set by READ CLOCK during MAJOR states E, F, and I. If the control is in MAJOR states E or I, it has detected a sync bit (1 data bit) during MAJOR states D or H; therefore, the clock pulse is the clock pulse following the sync bit. A data bit will be followed by another clock pulse which is the clock pulse used to strobe data into the shift register, shifting it one place.

This clock pulse and the clock pulses following strobe the gates generating SHIFT SR and reset the SHIFT INPUT flip-flop, if the data bit from the disk was a 1. WORD PARITY is formed simultaneously with this operation.

The remainder of the read logic is inactive until 12 data bits have been accumulated in the SHIFT REGISTER. READ CLOCK, DATA, and SHIFT SR are the only signals present in the disk control until that time.

The SHIFT SR pulses are counted by the 12-bit counter (see Figure II-29); when 12 pulses have been counted, BIT COUNT 12 (1) becomes true triggering the M602 pulse amplifier to produce the following six signals:

E RESET CNTR	When this signal is raised during normal read or write cycle, it is necessary to clear the track counter before loading it with the contents of SR bits 0-7, to be certain that the RK01-X and the drive have found the correct data track.
SR TO COUNTER	One hundred and fifty nanoseconds after the raising of E RESET CNTR, the shift register data is loaded into the track address counter.
READ FORM LP	The longitudinal checksum is formed only during MAJOR state 1 and is checked at the end of this major state.
SR TO DB	Data in the shift register is transferred to the data buffer except when the instruction is a normal read/write and the major sequencer is in MAJOR state E and F, because the two header words are not transferred to the computer. The SR TO DB signal also terminates in the write logic (see Figure II-21) to form COUNT BLOCK and SET DATA BREAK REQ.

UNFORM CLR INT CNT	This signal direct clears the 12-bit block counter (see Figure II-31), after the 12th data bit is shifted into the shift register, because word parity is not written or read during the unformatted mode. Once the 12-bit block counter is direct cleared, another 12-bit word can be accumulated in the shift register.
13TH BIT	This signal is generated when BIT COUNT 12 (1) is true but only during MAJOR state I; during this major state, only 12 data bits are read and written. This signal is also generated after the 13th clock pulse during MAJOR states E and F and shifts to the Major Sequences from E to F and F to G.

Assuming that BIT COUNT 12 (1) and UNFORMATTED (0) are true and the disk control is not in MAJOR state I, the next READ CLOCK pulse strobes the AND gate, shown at coordinates C8, generating 13TH BIT and approximately 250 ns later CLEAR BIT COUNT. The disk control, therefore, resets the bit counter (see Figure II-29) during MAJOR states E and F after 13 READ CLOCK pulses and during MAJOR state I after 12 READ CLOCK pulses.

The logic that generates SET TRACK ERROR and FIND NEXT SECTOR is shown at coordinate A1. The function of this logic is to be certain that the disk control and drive have moved the read/write heads to the correct data track, and that the sector being read is the correct one. The track and sector comparator outputs are strobed by 13TH BIT if the MAJOR state is E, it is a NORMAL R/W cycle, and NEW SELECT is 0. Data track accuracy is checked by comparing the track address register, which is loaded by the program, with the track counter register, which is loaded from bits 00-07 the first header word during MAJOR state E. To be certain that the correct sector has been found bits 09-11 of the first header word are checked.

FIND NEXT SECTOR direct clears the major sequencer register then indirectly sets it to MAJOR state B where the control waits until the next sector pulse arrives from the disk drive. Refer to Section 5.2.5.

5.2.6.1 Parity Checking - At coordinates B1/2-5 of Figure II-20 is an AND gate with inputs BIT COUNT 12 (0), MISS PULSE, and READ CLOCK. Its output is ORed with WRITE SHIFT SR, generating SHIFT SR and WORD PARITY.

NOTE

If BIT COUNT 12 (0) becomes true, namely BIT COUNT 12 (1), there will be no SHIFT SR pulses. Twelve bits of data will still only be accumulated during MAJOR states E and F although 13 bits of information are allowed to come off the disk. The 13th bit of information is parity which goes into the SHIFT INPUT flip-flop and is compared with the WORD PARITY flip-flop.

The 150 ns time delay, triggered by 13TH BIT and shown at coordinates C2, strobes the comparator logic at coordinates B1; if WORD PARITY and SHIFT INPUT are the same and the control is in MAJOR state E or F, SET WORD PAR ERR is generated. This description demonstrates that the 13TH BIT triggers a delay and checks for word parity on header words. This delay allows time for the signals to settle before strobing them.

The sector-protect bit SR00 and the sector no-good bits SR01 to 5 are checked by strobing them during MAJOR state F to generate PROTECT BIT ON and SET SECTOR NO GOOD. In addition, the 250 ns delayed pulse, also triggered by 13TH BIT, generates CLEAR BIT COUNT, which direct clears the SHIFT INPUT and WORD PARITY flip-flops.

In addition to the above signals generated by 13TH BIT, it also generates the important signal READ 13; this signal is used as a time reference throughout the rest of the control.

5.2.6.2 Block End, Read Set Major J and K - When the block counter (see Figure II-29) has counted to 256, BLOCK COUNT 256 (1) becomes true and the SR TO DB pulses, which the block counter has been counting, are gated off. Following this sequence the BLOCK END flip-flop is set to its 1 state by the NEXT 13TH BIT pulse, and 150 ns later RESET MAJOR J is generated, and 250 ns later READ 13 is generated.

The READ 13 pulse strobes the state of LONG PARITY, generating SET PARITY ERROR if the longitudinal parity register is not all 1s. It is also ANDed with BLOCK END (1), generating READ SET MAJOR K.

While the control is in MAJOR state J or K, READ CLOCK and READ DATA are gated off; therefore, this portion of the control is inactive until another read cycle is initiated.

5.2.7 Write

The write logic (see Figure II-21) controls all functions related to writing operations. Other logic on this print is common to both read and write modes.

The logic at coordinates C5 through C7 generates INH BREAK, MAJOR states E, F, I, and J, and ENBL DB TO SR; ENABLE SHIFT SR is also generated and controls the inputs and shift functions of the shift register.

The logic at coordinates A3 and A4 generates COUNT BLOCK and SET DATABREAK REQ; the logic at coordinates B1/2-1 generates DATA OUT. The remainder of the logic controls the general write operations.

The INH BREAK signal is used in a negated sense at the input to the eight-input AND gate at coordinates A6 1/2 to prevent an extra data break request from occurring at the end of MAJOR state E during WRITE ALL.

Miscellaneous signals, MAJOR I and J and MAJOR E, F, I, and J, are used throughout the control. Signals ENBL LP TO SR, ENBL SHIFT SR, and ENBL DB TO SR control the functions of the data shift register; however, only one can be true at a time. Therefore, if shift register data is not shifted or the longitudinal parity register (LP) data is not loaded into the shift register at the end of MAJOR state I when WORD 256 (1) is true, ENBL DB TO SR is true.

The COUNT BLOCK and SET DATA BREAK REQ levels are generated during a read cycle whenever SR TO DB is generated or during the write cycle under the conditions shown in Figure II-21. When SR TO DB is generated, a word is in the data buffer, ready for transfer to core memory.

Data must be fetched from memory before it is written on the disk; when SET MAJOR C is generated during WRITE ALL and SET MAJOR G during any write mode, they are used to fetch data prior to the actual transfer of data to the disk.

On overflow of the WC OVERFLOW register, WC OVERFLOW (0) H becomes true inhibiting all further data break requests. Block counting continues until WORD 256 (1) H becomes true, at which time LP TO SR is generated transferring longitudinal parity data to the shift register where the data is written onto the disk. Therefore, longitudinal parity is written as the 257th word under all conditions except in the UNFORMATTED mode. The disk control never goes beyond MAJOR state E in the UNFORMATTED mode, and therefore, the block counter has no effect during this mode of operation. The logic used for general writing of data is described in the following paragraphs.

The M310 delay module at coordinates B5 generates two timing pulses, which when ANDed with WRITE CLOCK, strobe all WRITE functions. The logic feeding this delay module input generates the conditions for raising these pulses.

Thirteen data bits are written during MAJOR states E or F and 12 during MAJOR state I, except during the UNFORMATTED mode when only 12 data bits are written during MAJOR state E.

When 12 bits are to be written, the transition of BIT COUNT 12 (1) going true triggers the pulse amplifier shown at coordinates C5, which in turn, generates the pulse UNFORMATTED WORD. UNFORMATTED WORD always triggers the delay during MAJOR state I and also triggers the AND gate shown at coordinates B8 during UNFORMATTED WRITE. The WRITE 13 pulse clears the bit counter.

If 13 data bits are to be written, UNFORMATTED WORD is blocked by AND gates, and the next WRITE 13 pulse appearing strobes the gate at coordinates B1/2-7, triggering the M310 time delay.

The word 256 and word 257 flip-flops, at coordinates A1/2-3 and 4, indicate the conditions for the end of data breaks and writing of longitudinal parity; the guard word is written after longitudinal parity. The WRITE FORM LP pulse, at coordinates A2, forms longitudinal parity at every WRITE 13 level during MAJOR state I.

The DATA OUT flip-flop receives data under the following four conditions:

a. writing a sync bit,

b. receiving normal data from bit 11 of the shift register when WORD 257 is written and BIT COUNT 12 are both 0,

c. the word parity is written during MAJOR state E and F when BIT COUNT 12 is a 1, and

d. longitudinal parity data from bit 11 of the shift register is used in an inverted sense when WORD 257 is a 1; longitudinal parity is written onto the disk in complement form.

5.2.8 Data Buffers

The data buffer logic (see Figure II-22) acts as a buffer between the computer memory buffer and the RK08 data shift registers.

During a read operation, data is shifted from the disk into the shift register, then transferred from the shift register into the data buffer; when the RK08 and the associated computer are synchronized, the data is transferred into the computer memory buffer. During the write operation, data flow is reversed.

The WRITE FLOP determines whether a write or read operation takes place. The flip-flop is set and cleared by IOT instructions. During a write operation when the write flip-flop is set to WRITE FLOP (1) L, gating enables the MB outputs to be transferred to the data buffer (DB). LOAD DB L is generated by one of the computer timing pulses and strobes the MB outputs into the data buffer (see Figure II-16).

During a read operation when the write flip-flop raises WRITE FLOP (0) H, gating enables the shift register inputs to be transferred to the data buffer. The pulse SR TO DB strobes the SR data into the DB. The pulse SR TO DB originates from the read logic (see Figure II-20).

The MAIN SR TO DB L pulse also transfers shift register data into the data buffer. This pulse is generated by issuing of IOT-6743 with AC02 on a 1. The data buffer is cleared by CLEAR ALL 1.

5.2.9 Data Shift Register

The data shift register (see Figure II-23) converts serial data from the disk into 12-bit words; during a read operation, the data is parallel transferred to the data buffer and longitudinal parity register. During a write operation, the data shift register accepts parallel data from the data buffer or longitudinal parity register and converts it to serial form for transmission to the disk.

Three possible states will enable the gates associated with the shift register: the shift state, the load data buffer into the shift register state, and load longitudinal parity into the shift register state. Each state is represented by the levels ENABLE SHIFT SR H, ENBL DB TO SR L, and ENBL LP TO SR L, which are generated in the write logic (see Figure II-21). The logic is designed to allow only one signal to be true at a time.

The enabling level, MAIN 01 (1) L, is ORed with ENBL DB TO SR L for the LOAD MAIN IOT-6743, which initiates the transfer from the data buffer to the serial register. Maintenance signals are shown in Figure II-17.

Serial information comes into the shift register from either bit 04 of the maintenance register, MAIN 04 (1) L, or from the disk (SHIFT INPUT (1) L). When ENABLE SHIFT SR H is true, the MAIN SHIFT SR L or SHIFT SR L pulses shift these inputs into the shift register. The SHIFT SR and MAIN SHIFT SR L pulses originate in the maintenance and read logic shown in Figures II-17 and II-20, respectively.

When ENBL DB TO SR L is true, DB TO SR L strobes the data buffer in parallel into the shift register. When ENBL LP TO SR L is true, LP TO SR L strobes the longitudinal parity register in parallel into the shift register. Both DB TO SR and LP TO SR levels originate in the write logic (see Figure II-21). The shift register is direct cleared by CLEAR ALL 1 H.

5.2.10 Longitudinal Parity

The logic, shown in Figures II-24 and II-25, keeps a running checksum of data written on the disk. The complement of this checksum is written onto the disk as the 257th data word. The gating on the input to the DATA OUT flip-flop shown in Figure II-21, performs the complement.

During a read function, a running checksum is again kept; the 257th word read is the checksum in complement form. When added to the data checksum, the final sum should be all 1s. If it is not, the PARITY ERROR flag is set.

The longitudinal parity register is a full adder; the shift register and longitudinal parity bits are gated into the adder whose output is then strobed into the longitudinal parity register.

The levels CLEAR ALL 1 and SET MAJOR I clear the longitudinal parity register; 0s are then gated into the register beccuse MAJOR I (1) is not true, yet both the longitudinal parity and shift registers are gated off. When MAJOR I (1) L is true, READ FORM LP or WRITE FORM LP strobe the adder output onto the longitudinal parity register. The strobe signals occur at approximately the same time that information is interchanged between the shift register and the data buffer.

The adder follows the restrictions of a full adder, with the signal levels shown; there is no carry into bit 11 because it is disabled by +3 V. A ground on the input to the longitudinal parity register sets the corresponding longitudinal parity bit to the 1 state with a STROBE LP signal.

5.2.11 Status Registers

The status registers (see Figure II-26) indicate the status of the Disk. Raising any error level raises the ERROR flag indicating that an error exists (refer to Table 5-3). All status registers except BUSY can be directly cleared to their 0 state by raising CLR ST REG L.

The BUSY register is direct set by IOT CLEAR L or IOT START H for SET READ, SET WRITE, or SET CHECK PARITY and is direct cleared by the INITIALIZE, END TRANSFER L, PROTECT L, or SET TRACK FOUND H.

Table 5-3
Error Flags

Flag	Explanation
ERROR	This flag is set when any error flags are set.
CONTROL BUSY ERROR	A Disk IOT is issued that effects operation when the control is busy.
TIME OUT ERROR	The control did not complete an operation after 56 revolutions of the disk.
PARITY ERROR	A bit in data, parity, or timing has been picked up or dropped during a read operation. Data Transfer terminates when the error occurs.

Table 5-3 (Cont)
Error Flags

Flag	Explanation
DATA RATE ERROR	The processor was busy and did not respond to a data break request within the required 13 μs time period. Transfer is terminated immediately on error.
TRACK ADDRESS ERROR	Track address, as read from the Disk header word, did not agree with the control track. The transfer is terminated immediately.
SECTOR NO GOOD	The program attempted to read or write data on a sector whose header words indicated a bad sector. The transfer is terminated immediately.
WRITE LOCK ERROR	The program attempted to write data on a sector that was write protected. The write operation is terminated immediately.
TRACK CAPACITY EXCEEDED ERROR	The program attempted to read or write beyond sector 17_8.
TRANSFER DONE	When this flag is in the 0 state, the transfer done flag will be set.

5.2.12 Sector Addressing

Because the disk is divided into eight sectors, it is necessary to find the sector from which data can be read or written. The sector address register (see Figures II-27 and II-28) is loaded from AC bits 09 through 11 by LOAD DISK ADDR H when the command, read, write, or check parity is given.

The SELECT SURFACE flip-flop is loaded by AC bit 08, which designates the selected disk surface: 0 or 1. When a READ ALL or WRITE ALL function is performed with command register bit 5 on a 1, or if an UNFORMATTED READ OR WRITE is performed with maintenance register bit 6 on a 1, the sector counter is direct cleared by the first disk sector mark following the disk index mark. When this occurs, SECTOR ZERO has been selected, and the succeeding sector marks from this point on count the sectors. If the contents of the sector counter are equal to the sector address register, or when they do become equal, SECTOR EQUAL H is generated in the comparator logic allowing the control to shift to MAJOR state C and continue with the operation (see Figure II-19).

The index mark occurs once for each revolution of the disk and signifies the starting point on the disk to be found. When IOT START, (see Figure II-14) is issued by a command, WAIT INDEX is set to a 1

preventing random sector counting. The INDEX MARK L sets the SEEK SEL flip-flop to a 1; therefore, the first SECTOR SYNCH PULSE received clears SEEK SEL flip-flop, the sector counter, and WAIT INDEX with CLEAR SECTOR L.

The next SECTOR SYNCH PULSE raised generates COUNT SECTOR L, which increments the sector counter by 1. The counter will also be incremented by 1 for each succeeding SECTOR SYNCH PULSE level.

The sector address register and sector counter comparator logic compare sector address bit 09 with sector counter bit 09, sector address bit 10 with sector counter bit 10, and sector address bit 11 with sector counter bit 11; therefore, if the track address and track counter registers contain the same binary numbers, then SECTOR EQUAL H is true, and the correct sector has been found.

During a NORMAL READ, NORMAL WRITE, or CHECK PARITY mode of operation, the sector counter performs no counting function. However, E RESET CNTR L clears the counter at the end of MAJOR state E, and SR TO COUNTER H loads the counter with the contents of shift register bits 09 through 11; the content of these bits is the sector portion of the first header word.

The first header word of each sector contains bits 09 through 11, which are formatted to a sector from 0 to 7. When a NORMAL READ or NORMAL WRITE occurs on a formatted disk, the control waits in MAJOR state B for the disk drive sector marks to appear and then reads the first header word on each sector. When a sector that contains the desired sector numbers is found, SECTOR EQUAL then allows the control to continue the operation.

Reading or writing on a sector is performed by transferring 256 data words or less from memory. Transferring more than 256 data words results in transferring from succeeding sectors until the word count overflows. If word count overflow has not occurred at the end of 256 data words, the control returns to MAJOR state B and reads the header words of each sector until the next one is found. Sector numbering of a formatted disk can be in numerical order or it can be arranged in some other desired sequence.

At the end of a sector, ERASE DELAY L generates INCR SECTOR ADDR H, which increments the sector address registers by 1. The ERASE DELAY L level also generates RESET MAJOR L, which resets the major sequencer to MAJOR state A.

From the RK01-X Disk Drive Interface, TRACK LOCATED sets the major sequencer register to MAJOR state B where the control waits for a sector pulse to appear, then continues to check the first header word.

5.2.13 Bit and Block Counter

The bit counter (see Figure II-29) is used to count 12 SHIFT SR pulses until the associated AND gate, at coordinates D5, has generated BIT COUNT 12 (1). The bit counter is then reset at the appropriate time by CLEAR BIT COUNT L, which is generated in the read logic shown in Figure II-20. The appropriate times are after the 13th header word bit has been read or written or after the 12th data bit has been read or written.

In addition, CLEAR ALL 1 L and MAJOR C (1) L ensure that the bit counter is reset before it is used.

The block counter is used to count the 256 words transferred to and from the computer. The signal COUNT BLOCK 256 (1) indicates that further data breaks are not required and gates the timing signals so longitudinal parity can be checked or written. The COUNT BLOCK signal is obtained from SET DATA BREAK REQ and is used to increment the 256 word block counter.

The counter is reset by either IOT START, MAJOR K, or MAJOR E. An extra reset pulse, during MAJOR F, is necessary because of an extra SET DATA BREAK REQ signal that generates COUNT BLOCK during the READ ALL mode.

5.2.14 Word Count and Current Address Registers

The Word Count register (see Figure II-30) is used to count the number of data words transferred to and from a computer memory. Initially it is loaded with the 2's complement of the number of words to be transferred and then it is incremented by 1 each time a word is transferred. A carry into the WC OVERFLOW flip-flop indicates that the last word has been transferred and no more data breaks are required. Specifically, the Word Count register is cleared and loaded from the AC by IOT-6753, which generates CLEAR WC L and LOAD WC H. Set DATA BREAK REQ H increments the Word Count register.

The Current Address register (see Figure II-31) is used to address the PDP-8 memory when the RK08 Disk Control transfers data to or from the computer memory. It is, therefore, the memory address register of the RK08 Disk. The Current Address register is initially loaded with the memory address, minus one, of the location where transfers are to start. It is then incremented each time there is a data break request.

The Current Address Register is cleared and loaded from the AC by IOT-6755, which clears the Current Address register and then loads it. The level, SET DATA BREAK REQ H, increments the Current Address register.

The extended memory address bits, 00 through 02, (EMA) are loaded from the AC by IOT-6732 (LOAD COMMAND), which are an extension of the current address bits and which address extended memory.

5.2.15 AC Input Gating 00-11

The AC input gating network (see Figures II-32 and II-33) provides the gating interface between the computer AC input bus and the status register error flags, word count register data, track, surface and sector counter data, data buffer data, current address register data, command register data, enable interrupt flags, seek track, access header, extended memory address data, and external disk data.

Each of these levels is gated onto the AC bus by an associated P CODE level, raised by selecting the appropriate MB09-11 bits and the AC STROBE L, which is raised when either a READ COMMAND L, READ DISK ADDR L, READ STATUS L, MAIN DB TO AC L, READ WC L, or READ CA L is enabled.

5.2.16 AC and MB Inverters

The AC and MB inverter circuit (see Figure II-34) converts the PDP-8/I negative BAC and BMB data bus to the positive bus if the bus was previously negative.

The enabling level for the BAC00-11 data is DEVICE SELECT ENABLE H, and the enabling level for MBM00-11 data is DEVICE SELECT ENABLE L or BREAK. Because these strobe levels are common to the AC and MB gates, data from both sources is strobed into the RK08 Disk Control in parallel.

5.2.17 Cable Terminators

The cable terminators (see Figure II-35) consist of resistive loads that are clamped to prevent excursion beyond +3V and ground. These loads are driven by a cable driver.

5.2.18 Interconnecting Cables

The cables that interconnect the RK08 to the RK01-X, I/O and Data Breaks, and the logic functions to the indicator panel are shown in Figures II-36, II-37, and II-38.

5.2.19 716 Power Supply

The Type 716 Power Supply (see Figure II-38) is a full-wave dc bridge rectifier network designed to provide 9 Vdc and 6.5 Vdc for the RK08 and RK01-X logic. The input to the supply is 115 Vac 50/60 Hz.

5.2.20 854 Power Control Panel

The ac voltages required by the RK08 and RK01-X logic power supply are controlled by the Type 854 Power Control Panel (see Figure II-40). Pin locations for the associated components making up the panel are shown in Figure II-41.

5.2.21 Disk Drive Power Supply

The Disk Drive Power Supply (see Figure 5-3) provides the ac and dc voltages required by the disk drive logic, in addition to positioning and sequencing control voltages. The supply, which will furnish power for up to two disk drives, consists of the following subassemblies: 1) the basic power supply, 2) the PSDT circuit board, and 3) the front panel. Each of the three subassemblies is described as follows:

Basic Supply	This supply provides the +5 Vdc, +12 Vdc, -26 Vdc, +24 Vdc, +24 Vdc control and the +12 Vdc sense voltages that are terminated at TB3. The basic supply also provides a switched 115 Vac that is terminated at TB1. This supply is energized through the contactor that is activated by grounding TB2-4. The +24 Vdc control voltage is not switched by the contactor and thus provides operational voltage to the PSDT circuit board whenever an ac input voltage is terminated at TB1. The +12V sense voltage is used to monitor the input power to this power supply.
PSDT Circuit Board	This board provides the sequencing and monitoring functions to the power supply as well as the drive voltage to the panel lights and contactor.
Front Control Panel	This panel contains a Power ON switch combined with an ON light, and an OFF switch combined with an OFF light and associated ATTENTION lights.

5.2.21.1 Operation - When the power supply is provided with 115 Vac input at TB1, the PSDT Circuit Board provides a ground at TB2-6 and TB3-13 to light the OFF light and give a GENERAL RESET (file) to the MD2101-2 Disk Drive. When the power ON switch is depressed, a momentary ground is applied to terminal 12 of the PSDT circuit board via TB2-9 to sequence the power supply ON. TB2-4 is grounded to energize the power supply; TB2-5 is grounded to light the ON LIGHT; and TB2-6 goes to +24 VDC to turn OFF the OFF LIGHT.

The general FILE RESET, TB3-13, is held low for 600 ms ±30% after the power supply is energized and then rises to 5.9 ±0.6V to allow the MD2101-2 disk drive to come to a SAFE condition. When the OFF SWITCH is depressed, a momentary open is provided to terminal 13 of the PSDT Circuit Board via TB2-8 to cycle the supply OFF. The OFF LIGHT is turned ON, and a general reset is sent to the MD2101-2 disk drive ground at TB3-13.

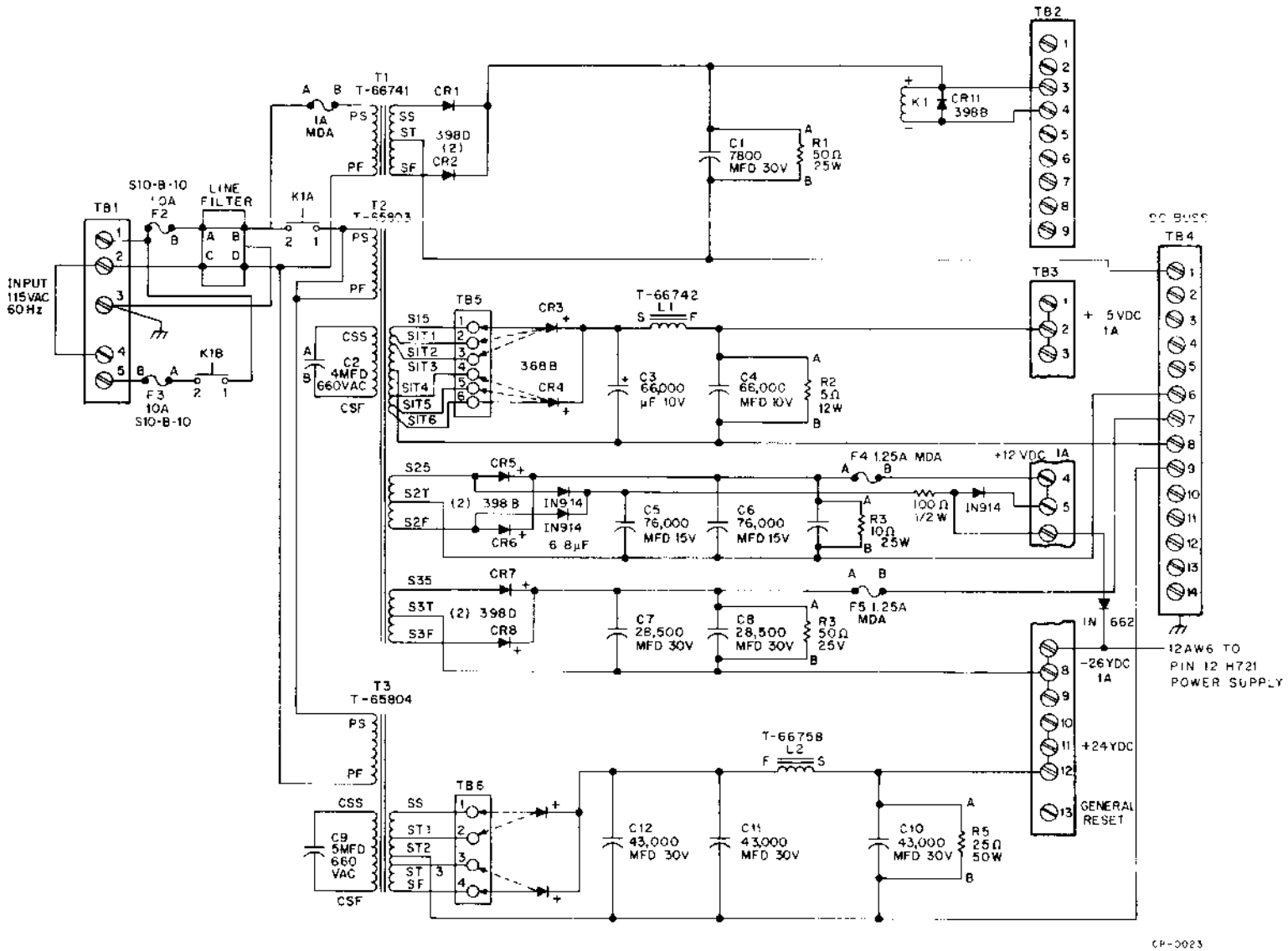


Figure 5-3 Power Supply Schematic

If the power supply is in an ON condition and a ground is applied at terminal 15 or 14 of the PSDT Circuit Board via TB2-1 and TB2-2, respectively, the power cannot be sequenced to an OFF condition by depressing the OFF SWITCH. This function provides an interlock; the supply cannot be turned OFF when the MD 2101 disk drive is in a READY condition.

A monitoring function is provided by the PSDT Circuit Board; all four dc supplies are monitored as well as the +12 Vdc sense voltage. The+12 Vdc power supply are diode ORed in the basic power supply and are fed to the PSDT board at terminal 4. If any dc power supply should fail or if either the fuse in the +12 Vdc output or the fuse in the -26 Vdc output should blow, the PSDT Circuit Board will send a general file reset to the MD2101 and sequence the power supply to an ATTEN condition.

In the ATTEN state, the power supply is de-energized and the OFF and ATTEN LIGHT are illuminated. To restart the power supply from an ATTEN state, the OFF SWITCH must first be depressed to sequence the power supply to an OFF condition, then the ON SWITCH is used to turn the power supply ON.

An additional monitor feature of the PSDT circuit board protects the MD2101 disk drive against input ac failure. The +12 Vdc sense circuit will on failure, sequence the power supply to an ATTEN circuit condition. This sequencing occurs within 15 ms after loss of input ac power. The MD2101 disk drive will unload the heads before the dc voltages fail. Thus, data stored on the disk is not lost on an input ac power failure.

5.2.22 New Select

In multiple drive systems, a program can select one drive and then another, however, there is only one track counter register that must be shared by up to four disk drives. It is, therefore, necessary to put the correct track information into the track counter when a new drive is selected.

This track information is placed in the track counter when normally checking to determine that the correct data track has been reached. If a new disk drive is selected and a normal read/write has previously been the mode of operation, a special cycle called NEW SELECT takes place, the instruction is stored and then executed when the NEW SELECT cycle is complete. To fully understand the NEW SELECT function, the following description of a READ cycle must be completely understood.

When the RK08 Disk Control is instructed to perform a NORMAL READ/WRITE function, and a new disk is selected, the NEW SELECT flip-flop (see Figure II-8) is set to its 1 state. On the next SECTOR SYNC PULSE from the disk drive, the major sequencer register is set to MAJOR B. The SECTOR SYNC PULSE that controls synchronization (see Figure II-28) is then enabled by MAJOR B. A normal read cycle occurs until the end of MAJOR E; at this time the normal transfer of SR bits 00-06 to the track counter takes place.

After the 13TH BIT (see Figure II-22) is generated, further checking for the correct data track or sector is prohibited, following which the checking of word parity occurs.

Finally, READ 13 and the 100 ns delayed 13TH BIT pulse raises ZERO MAJOR resetting MAJOR SEQUENCER and generating RESET NEW SELECT, which resets the NEW SELECT flip-flop to its 0 state.

If a new disk drive was selected, the NEW SELECT flip-flop is reset, and if a command was given to the RK08 Disk Control to read or write, the control is restarted in MAJOR STATE A just as if the new select cycle had not occurred. However, the track counter now contains the correct track address over which the read/write heads in the new drive are placed.

Chapter 6
Maintenance

6.1 GENERAL

To obtain maximum life and operating efficiency from the Disk, it is imperative that a regular preventive maintenance schedule be established. Unnecessary adjustments should not be made to the Disk; such adjustments can alter Disk performance resulting in time consuming maintenance.

Periodically inspect the Disk for any evidence of component overheating that discolors resistors and wiring insulation, thereby causing breakage and erroneous operation.

Waveforms used in this section for alignment purposes have been photographed in the correct alignment state. When performing tests or alignment procedures on the Disk, the input signal conditions must be checked because waveform outputs are dependent on these signals.

Keep the equipment as clean and dry as possible. An air blower or brush with long soft bristles makes an excellent dust remover. However, do not use such devices for cleaning the disk cartridge. A high-pressure air hose is not recommended; it can cause dust particles that scratch internal surfaces and components.

Before installing replacement parts, check the circuit to determine the cause of failure. For maintenance procedures not presented in this manual, the CMD 2101 Instruction Manual should be referenced.

CAUTION

Under no circumstances must adjustments be made to the disk assembly. Replacement or adjustments must be made by authorized DEC personnel only.

6.2 MAINTENANCE KIT

To perform maintenance on the Disk, special tools, test equipment, and software packages are required. These items, outlined in Table 6-1, can be purchased from the DEC Field Service Office in Maynard, Mass.

Table 6-1
Maintenance Equipment

Quantity	Item
1	Instruction Test
1	CE PWB Board
1	Set of open-ended wrenches
1	CE alignment disk cartridge (red stripe)
1	Set of feeler gauges
1	Set of Allen-head screwdrivers
1	R/W head preamplifier plug
1	Format program
1	Data reliability diagnostic
1	Set of read/write heads
1	Air filter
1	Spare new cartridge

6.3 PREVENTIVE MAINTENANCE

The following sections contain data that will enable the user to maintain the Disk in peak operating condition and will enable the user to detect problems before they affect the operational characteristics of the Disk.

NOTE

Under no circumstances must adjustments be made to satisfactorily operating mechanical or electrical components.

6.3.1 Functional Check for Head Alignment

This check establishes the need for adjusting read/write heads to the CE cartridge by verifying that the head-to-track alignment is maintained within the required tolerances. The procedures for checking read/write head alignment are provided in Paragraph 6.5 of this chapter.

6.3.2 Visual Inspection

At periodic intervals, the Disk electrical and mechanical components should be inspected for excessive build-up of dust and dirt, wear of mechanical components, loose wiring connections and hardware components, burnt contacts, in addition to any other irregularities that may be evident.

6.3.3 Head Damage

This check establishes the need for replacing read/write heads by visually inspecting them for wear and damage. The heads should not be removed for this check, but should be examined using a visual

aid such as a mirror. The types of conditions that cause damage to heads are described in Paragraph 6.3.10. Generally, disk damage by a faulty head can be detected by the following symptoms:

a. A persistent reddish-brown oxide collection on the suspected head after cleaning,
b. Helical scratches and 0.010-in. spaced radial scratches on the disk surface, and
c. Audible "tinging" noises. This is indicative of a bad cartridge.

NOTE

Do not replace read/write heads under any conditions unless Disk failure occurs. Head scratches do not always denote a faulty read/write head.

Whenever a head is replaced, remove the disk pack from the drive and inspect the disk surfaces to ensure that no "comet trails" with embedded particles are present to damage the new head.

6.3.4 Audible "Tinging" or Scratching

An audible tinging or scratching is an indication of head-to-disk interference. This noise is an initial symptom and may not continue if the particle is dislodged or flattened.

If this tinging occurs, examine the read/write heads and disk surfaces for scratches and "comet trails". The approximate radial position can be determined by noting the track positions of the carriage where the tinging occurred. Whenever this condition exists, the read/write heads must be thoroughly cleansed using scheduled maintenance procedures, and the disk cartridge replaced.

6.3.5 Scratches or Grooves Across the Head

If a read/write head has a series of 0.010-in. spaced grooves or scratches across the face of the slider, it has been flown on a disk containing an embedded particle that may or may not, still be embedded in the disk surface. The presence of these grooves does not indicate that the head is ruined since they become scratched during normal service. A damaged head will either not read/write data properly, or it will fly with an audible tinging.

6.3.6 Oxide Deposits on Heads

The distinctive color of the disk surface (reddish-brown oxide) makes it easy to detect on the head surface. Its presence may indicate that the disk surface is being scraped as a result of head-to-disk interference. Whenever this condition is apparent, the heads must be thoroughly cleansed, using the preventive maintenance procedures outlined in Paragraph 6.3.8.

6.3.7 Disk Surface Scratches

Some types of scratches on disk surfaces are practically harmless while others can affect recording performance or seriously damage the read/write heads. A particular type of harmful scratch is a "comet trail" where the head of the comet is an embedded particle protruding out of the disk surface. Scratches that are regularly spaced 0.010 in. apart indicate that a head with a protrusion on its slider face, or an embedded particle in the exposed epoxy, has been used on the disk.

6.3.8 Cleaning Read/Write Heads

Read/write heads must be cleaned at regular intervals of two to three months to prevent damage to the disk surface and the heads themselves. Read/write heads and disk surface imperfections include fingerprints, stains, residue from isopropyl alcohol, and lint and dust from a contaminated atmosphere. The presence of fingerprints, oily film, or stains on a head or disk surface leaves oil and salt deposits that can build up to a height greater than the "flying" height of the read/write head, causing head-to-disk interference. Continuous accumulation of foreign material on the head or disk surface results in generating read/write errors if scheduled maintenance is not followed.

The following procedure should be followed when cleaning the read/write heads.

Step	Procedure
1	Wrap a lint-free wiper on a paddle dampened with 91% isopropyl alcohol.
	NOTE When cleaning the heads, DO NOT touch the face of their flying surfaces with fingers; acids emitted from the skin can etch and ruin the head.
2	Using a second paddle to support the back of the read/write head, thoroughly wipe the face of each head with a lint-free wiper on a paddle.
3	After cleaning, be certain not to leave any alcohol residue on the face of the read/write head. DO NOT blow on the heads; moisture will rust and contaminate them.
4	Use the read/write head reflection of the upper head from the lower head to inspect the head surface to be certain that all dirt has been removed from the head surface, otherwise head damage may result. Follow the cleaning by wiping the head with a dry wiper.

6.3.9 Particle Damage to Disk Surface

Damage to a disk surface can be caused by small particles of foreign matter deposited onto the disk surface. The critical size of contaminants is determined by the "flying" height of the head, which is in the range of 125 to 150 microinches. If foreign particles of this size, or larger, are carried into

the gap between the head and disk surface, they may become embedded in the face of the read/write head or in the disk magnetic surface causing possible irreparable damage to either assembly.

Hard particles such as aluminum oxide embedded in the head can cut grooves in the disk surface as it flies over the surface. Particles embedded in the disk magnetic coating often leave a "comet trail" scratch on the disk surface as they are forced into the coating. Embedded particles can also cause dropouts or a loss of data and can, in turn, generate recording "noise."

6.3.10 Particle Damage to Read/Write Head

Read/write head damage can be caused by foreign particles on the disk surface while the head is flying over the surface. Damage will be evident by grooves cut into the head surface.

NOTE

Do not replace read/write heads unless errors occur. In such cases, check read/write heads 0 and 1 with a scope for proper amplitude.

Disk tracks are 0.010 in. apart, and when a head is moved to different tracks in the area of the embedded particle, a succession of 0.010-in. scratches are gouged into the face of the heads. A particle ultimately embedded into the disk surface can burr or distort the air gap between the head and disk surfaces, which if severe enough, will affect head performance; the head must then be replaced. A badly scored head flying over the disk will produce an audible tinging sound.

6.3.11 Nonparticle Damage

Damage to head and disk surfaces occurs as the result of head-to-disk interference from imperfections on their surfaces or from any imperfection in the slider curvature that interferes with proper head flying characteristics.

6.3.12 Electronic Circuitry

The function of the disk drive mechanism is dependent on the logic circuit, which should be periodically checked by using diagnostic programs.

Diagnostic programs combined with pulse checking is suggested for locating circuit problems. Logic modules and connections should be checked for proper seating in their connectors.

6.3.13 Cleanliness

Dust and dirt must not be allowed to accumulate within the Disk; their presence can impair the performance of head loading and disk cartridge movement.

Although the disk cartridge is pressurized to prevent contaminants from entering it, large dust or dirt particles can drop through the cartridge door, which, if trapped between the read/write heads and the disk surface, can result in severe damage to the heads and/or disk surface. If necessary, thoroughly vacuum or dust the drive assembly to eliminate the accumulation of dust and dirt.

NOTE

Under no circumstances must compressed air be used to clean the drive assembly.

Oil or grease MUST NOT be allowed to accumulate anywhere on the drive assembly; they will attract dust and dirt. The Disk should not be operated with the top cover removed unless maintenance is to be performed.

6.4 RK01-X MODULES

The RK01-X Disk logic consists of printed circuit, plug-in, M-series modules (see Table 6-2) that are mounted in the H911 Mounting Panel and H803 Connector Blocks E and F.

Table 6-2
RK01-X Logic Modules

Quantity	Type	Name
5	M111	Inverter
1	M112	NOR Gate
6	M113	Ten 2-Input NAND Gates
5	M115	Eight 3-Input NAND Gates
4	M119	Three 8-Input NAND Gates
3	M121	AND/NOR Gate
3	M202	J-K Flip-Flop
2	M204	General-Purpose Buffer and Counter
3	M206	General-Purpose Flip-Flop
2	M211	Binary Up/Down Counter
2	M302	Dual Delay Multivibrator
1	M405	Crystal Clock (2.88 mc)
2	M501	Schmitt Trigger
3	M602	Pulse Amplifier
1	M606	Pulse Amplifier
2	M617	4-Input Power NAND Gate
2	M623	Bus Driver

Table 6-2 (Cont)
RK01-X Logic Modules

Quantity	Type	Name
1	M627	NAND Power Amplifier
3	M901	Flexprint® Cable Connector
3	M939	Clamp Load
4	M904	Coaxial Cable Connector to Disk Drive
1	W021	Cable Connector to Switch Panel

® Flexprint is a registered trademark of Sanders Associates.

6.5 RK08 LOGIC MODULES

The RK08 Disk consists of the logic modules outlined in Table 6-3.

Table 6-3
RK08 Logic Modules

Module Type	Quantity	Modules
G775	2	Connector Board to Indicators
G717	1	Terminator
M101	3	Diode Gate
†M100	3	Diode Gate
M103	3	Device Selector
†M102	3	Device Selector
M111	7	Diode Inverter
M112	5	NOR Gate
M113	15	Diode Gate
M115	7	Eight 3-Input NAND Gates
M117	2	Six 4-NAND Gates
M119	4	Eight -1 Input NAND Gates
M121	11	X OR Gates
M161	1	Binary-to-Octal/Decimal Decoder
M202	9	J-K Flip-Flop
M203	1	Set-Reset Flip-Flop
M205	1	Six Flip-Flops
M206	14	Six Flip-Flops
M207	2	Flip-Flop
M212	2	Binary Shift Register
M214	2	Adder
M310	3	Delay Line
M602	2	Pulse Generator

†The M102 Module replaces the M103, the M100 Module replaces the M101, and the M633 Module replaces the M623 when the Disk is interfaced to a negative bus computer.

Table 6-3 (Cont)
RK08 Logic Modules

Module Type	Quantity	Modules
M606	2	Pulse Generator
M617	1	Six 4-Input NAND Gates
M623	5	Diode Gate
†M633	5	Diode Gate
M627	7	Six 4-NAND Gates
M901	3	Flexprint Cable
M904	5	Coaxial Cable Connector to Computer
M938	2	Terminator for PDP-8 or LINC-8 Signals
W021	1	Signal Cable Connector (PDP-8 or LINC8 only)

†The M102 Module replaces the M103, the M100 Module replaces the M101, and the M633 Module replaces the M623 when the Disk is interfaced to a negative bus computer.

6.6 CONTROL COMMANDS

Two types of control commands are provided: the user's commands to the disk, and the disk status commands to the user. Table 6-4 outlines both types of commands.

Table 6-4
Disk Input/Output Command Signals

Signal	Function
Input signals from RK08 to disk	
WRITE SELECT (L)	This signal, when enabled, controls the write function of the disk. Write current is supplied to the side of the write coil that is conditioned ON in the read/write head selected. When the WRITE SELECT signal is high, the write current does not flow through either of the write coils.
WRITE DATA (L)	This signal controls the switching of the write current from one write coil to the other, assuming that the WRITE SELECT line is low. Each time this line changes from a false to true condition, a flux change occurs at the write head gap producing a bit on the disk surface.

Table 6-4 (Cont)
Disk Input/Output Command Signals

Signal	Function
HEAD SELECT (L)	This signal controls the selection of the two read/write heads: head 0 when high and head 1 when low.
MOVE FORWARD PULSE (L)	When this line is low, it causes the read/write head responsyn positioner assembly to move forward one data track at a time (toward data track 202) for each negative pulse that appears on the line.
MOVE REVERSE PULSE (L)	When this line is low, it causes the read/write head responsyn positioner assembly to reverse its direction of travel and move one data track at a time toward track 000 for each negative pulse that appears on the line.
ERASE CONTROL (L)	When writing, the erase coil is energized on this low condition causing current to flow in the erase coil. When the line is high, erase current is turned OFF.
Output Signals from disk to RK08	
READ DATA (L)	When this line is low, it presents the serially read data from the double-frequency recorded information. The read data pulse appears between the read clock pulse if a 1 bit is present.
RD CLOCK (L)	When this line is low, it presents the signal that defines the bit-cell time, nominally 1.389 μs.
SECTOR PULSE (L)	This level will be low each time one of the eight sector pulses passes the internal disk photocell circuits. One complete revolution of the disk is represented by eight pulses on this line.
INDEX PULSE (L)	When this line is low, it indicates that the index pulse has occurred. It is used as a disk sector reference. One index pulse occurs for one complete revolution of the disk.
HOME POSITION (L)	When this line is low, it indicates that the read/write head responsyn positioner assembly is at the home position or data track 000 or -001. When the read/write head positioner is at a data track position other than 000, this line is high.

Table 6-4 (Cont)
Disk Input/Output Command Signals

Signal	Function
POSITION ERROR (L)	When this signal is low, it indicates that the read/write head positioner assembly has exceeded its positioning range. When this line is low, the read/write head positioner assembly is outside data track -001 or 206. All data tracks within this range will condition the line high. When this line is enabled low, the read/write head positioning assembly is automatically returned to data track 000.
NOT READY	When this level is high, it indicates that the disk is not ready to receive user commands. Conversely, if this line is low, it indicates that the disk is ready to receive and respond to the user commands.
INTERLOCK (L)	Interlock users do supply power to prevent inadvertent manual turn-off of the disk power supply while the read/write heads are loaded. This line is ground when loaded and floating when unloaded.

6.7 CE PWB SWITCH OPERATION

The CE alignment cartridge and PWB switch and logic panel (see Figure 6-1) are used to align and move the read/write heads. The function of each switch is described in Table 6-5.

Table 6-5
CE PWB Switches

Switch	Function
HD 0 and HD 1	This is a two-position switch that allows selection of upper head 0 or lower head 1.
1-8-32	This is a three-position switch that allows a single-step move, an eight-step move, and a 32-step move.
FWD/REV	This is a two-position switch that allows the read/write head to move either forward toward data track 200 or reverse toward data track 000.
INT	This is a two-position, momentary contact toggle switch that allows the read/write head positioner to move as determined by the setting of the 1-8-32 and FWD/REV switches.

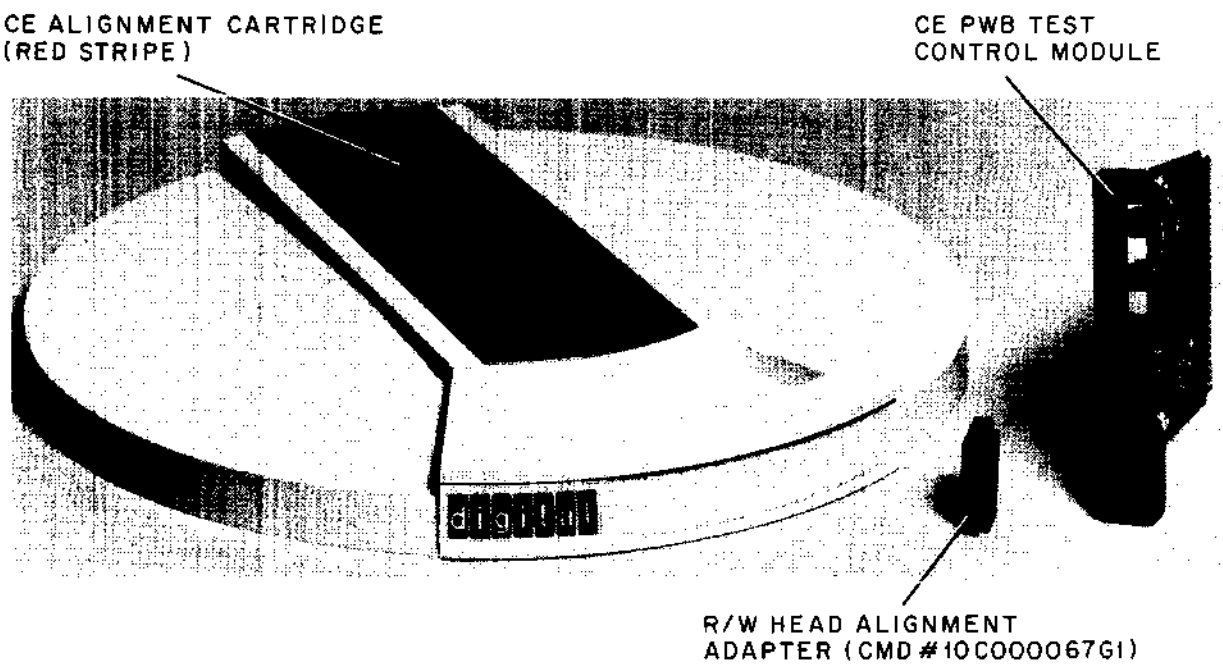


Figure 6-1 Alignment Cartridge, Control Module and Alignment Adapter

6.8 I/O INTERFACE CABLES AND TERMINATIONS

The IOP, data address, and data bus terminations are outlined in Table 6-6; the data break I/O cables are outlined in Table 6-7; and the I/O bus interface cable is outlined in Table 6-8.

Table 6-6
Termination Modules

Module Location	Module Type	Function
D01	G717	Terminates IOP 1, 2, 4; and TS 1, 3 signals.
D04	M938	Used when disk is installed on PDP-8 or LINC-8 bus. Module terminates the data address bus.
D05	M938	Used when disk is installed on PDP-8 or LINC-8 bus. Module terminates the data bus.

Table 6-7
Data Break I/O Cables to Computer

Module Location	Function
A01	BAC 00-11/BIOP 1, 2, 4/BTS 1, 3/BINITIALIZE inputs.
A02	BMB 00-11 inputs.
A03	AC input bus 00-11, SKIP, INTERRUPT RQST, AC CLEAR, RUN inputs.
A04	Data Address 00-11, BREAK REQUEST, DATA IN, BBREAK, BADDRESS ACCEPTED, MB INCREMENT inputs.
A05	Data bits 00-11; 3 cycle; BWC overflow; EXT DATA ADDRESS 0, 1, 2 inputs.
C05	EXT DATA, ADD 0, 1, and 2L (for PDP-8 and LINC 8 only)

Table 6-8
I/O Bus Interface

Module Location	Positive/Negative Bus Modules			
	No.	Positive Bus	No.	Negative Bus
A07, A08, C02	3	M101	3	M100
A09, A10, A11	3	M103	3	M102
B01, B02, B11, C01, C09	5	M623	5	M633

6.9 PREVENTIVE MAINTENANCE SCHEDULE

To ensure satisfactory operation and to maintain reliability, the following monthly Disk maintenance schedule, shown in Table 6-9, should be followed. The frequency at which these checks should be made is dependent on the usage given the Disk by the user and the cleanliness of his environment. These procedures are based on the Disk operating 200 hours per month.

Table 6-9
Maintenance Schedule

Month	Component	Procedure
2	R/W Heads	Clean and visually inspect the heads to determine if head oxide build-up is excessive. Also inspect the heads for physical wear or damage. Replace heads if wear is excessive.
4	Air Filter	The efficiency of the filter can be checked by holding the hand against the inside of the filter and checking for freedom of air flow. Clean the filter if air flow is restricted. If cleaning does not correct the problem, replace filter. The filter is located on the rear of the air inlet assembly, which is located on the rear of the disk.
6	Carriage Rail	Clean the carriage rail with lint-free tissue dampened in 91% Isopropyl Alcohol.
6	Carriage Bearing	Clean the outer bearing race by holding a dry, lint-free tissue against the bearing while moving the carriage back and forth.
6	Spindle Assembly	Magnetic particles can be removed by using adhesive tape. Clean each magnetic chuck piece with lint-free tissue dampened with 91% Isopropyl Alcohol.
6	R/W Heads	Check head alignment using the CE disk cartridge (red stripe) data tracks 100 and 105. Refer to Paragraph 6.10 in this chapter for alignment procedures.
6	Sector Pulse Timing	Check disk sector pulse timing using the CE cartridge (red stripe) data track 095. Refer to Paragraph 6.13 in this chapter for sector alignment procedures.
6	Base Plate, Casting and Covers	Inspect for cleanliness and presence of loose particles. Clean when necessary.
6	Fram Filter	If air flow is restricted clean the filter or replace it with a new one.
6	37 ms Time Delay (Refer to print D-BS-RK01-X-02)	Check the time delay to be certain that it is 37 ms.
6	20 μs Time Delay	Check the time delay by using the Data Reliability Test in the acceptance mode for a time duration of 10 hours per disk drive. Recoverable errors are allowed. Increases time depending on number of errors.

6.10 READ/WRITE HEAD ALIGNMENT

The procedures in the following alignment section serve as a check to determine the need for aligning the read/write heads to the CE test cartridge data track 100 and 105 by verifying that the head-to-track alignment is maintained within the required tolerance.

Correct alignment of both the upper and lower read/write heads is obtained when the waveform shown in Figure 6-4E is obtained.

The test equipment required for head alignment is described in Table 6-10.

Table 6-10
Test Equipment

Quantity	Equipment
1	CE PWB switch and logic module, see Figure 6-1
1	CE disk alignment cartridge, with red stripe
1	Read/write head preamplifier adapter CMD #10C000069G1
1	Set of feeler gauges
1	1/4-in. and 5/16-in. open ended wrenches
1	0.050-in. and 7/64-in. Allen screwdrivers

The CE PWB switch and logic panel enables data track 100 and 105 to be accessed by manipulation of the associated switches.

6.10.1 Alignment Procedures

Step	Procedure
1	Remove the RK01 Control cable from the Disk Electronic Module Assembly and install the CE cartridge in the disk per the Disk Cartridge Installation procedures in Chapter 3.
2	Install the CE PWB switch and logic module in slot 25 of the Electronic Module Assembly as shown in Figure 6-2 and install the read/write head alignment adapter CMD #10C000067G1 between the head cable plug and the head socket. The preamplifier is located on top of the responsyn positioner assembly (see Figure 6-3). Installation of the adapter causes the read/write and erase signal lines to be reversed. The signal being observed is the erase signal.

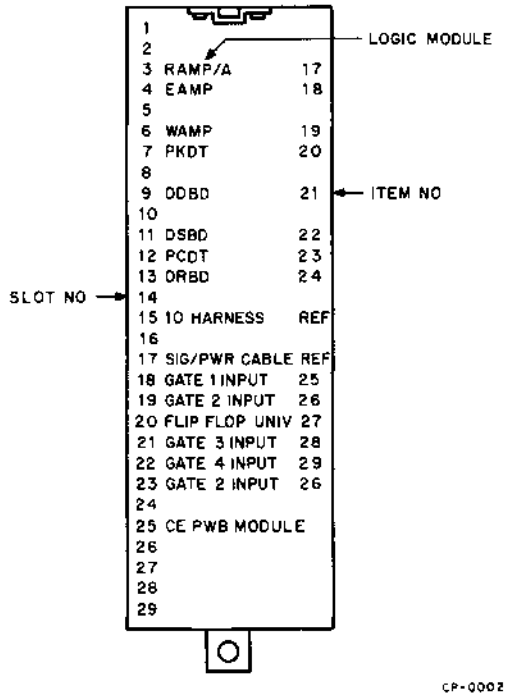


Figure 6-2 Electronic Module Assembly Diagram

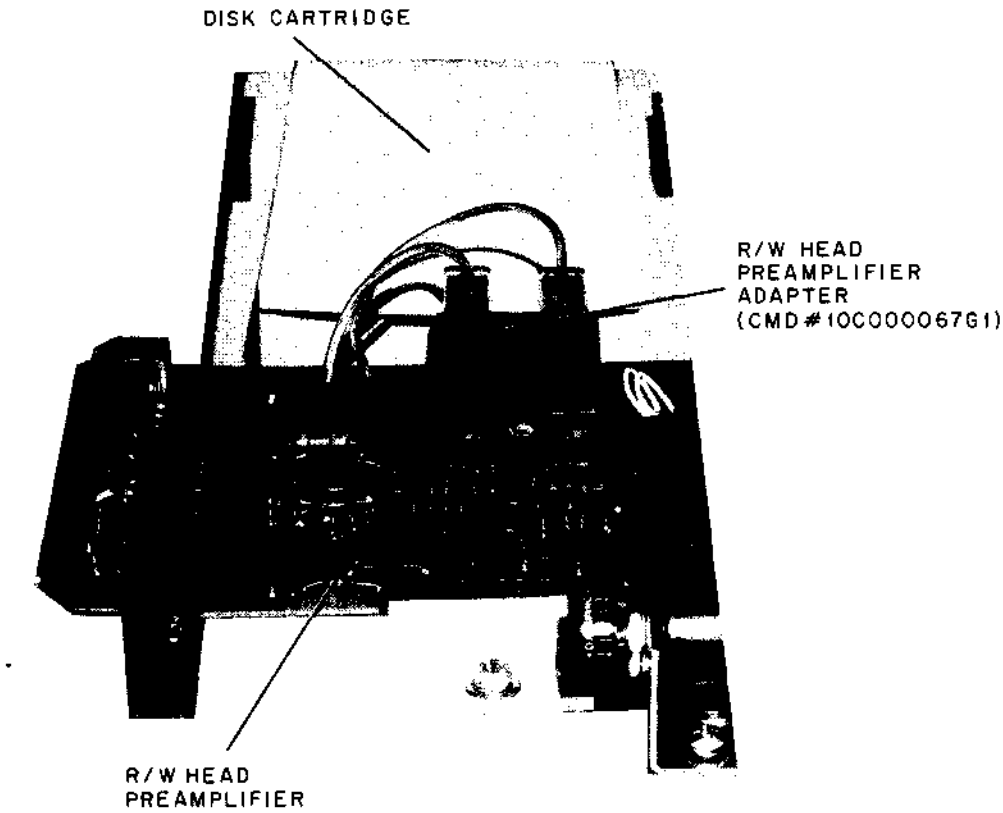


Figure 6-3 Read/Write Head Alignment Adapter

Step	Procedure
3	Apply power to the Disk by setting the START/STOP switch to START. The read/write heads are now loaded.

NOTE

The Disk must be allowed to operate continuously for a period of approximately 15 minutes to allow all Disk components to temperature stabilize.

4 Select head one by setting the CE PWB HD 0/HD 1 switch to HD 1.

5 Set the CE PWB 1-8-32 switch to 32 and activate the associated INT switch three times, then set the 1-8-32 switch to 1 and activate the INT switch four times. The read/write heads should now be on data track 100.

6 Synchronize the oscilloscope from the negative reference pulse by connecting the channel one probe to TP 7 on the PCDT module in slot 12 (see Figure 6-2). Connect channel two, direct or 10:1 probe of the oscilloscope, to TP 1 on the RAMP/A module in slot 3 (see Figure 6-2). Set the oscilloscope controls to produce a sensitivity of 100 mV/cm and a time base of 5 ms/cm.

The waveform viewed on channel 2 of the oscilloscope is the erase track output for head one. The disk platter makes one revolution in 40 ms as shown by the negative pulse on channel 1.

7 If the read/write heads are on data track 100, the waveform shown in Figure 6-4E should be viewed on the oscilloscope. If the display shows them to be out of alignment, the head that is the farthest from data track 100, is the head that must be aligned first.

NOTE

To determine whether head 0 or 1 is farthest from data track 100, alternately set the HD0 and HD1 to their respective positions while physically moving the head carriage assembly in the forward and reverse directions while viewing the waveform. Exert inward/outward pressure on the back of the carriage assembly.

8 If the read/write heads are adjusted beyond the center line of data track 100, the waveform shown in Figure 6-4F will appear on the oscilloscope. It is then necessary to shut down the Disk, remove the CE cartridge, slightly loosen the head locking clamp, loosen the adjustment screw until it is out of the way, and push the read/write head assembly back towards data track 000. Then slightly retighten the locking clamp to prevent the heads from becoming loose. The assembly must make three-point contact with head mounting assembly (see Figure 6-5). Using the CE PWB switches restep the read/write heads back to data track 100 and check for alignment.

9 If the read/write heads are still positioned too far forward for alignment (after making 3-point contact), loosen the four #10 motor mount screws on the four corners of the motor mount (see Figure 6-6).

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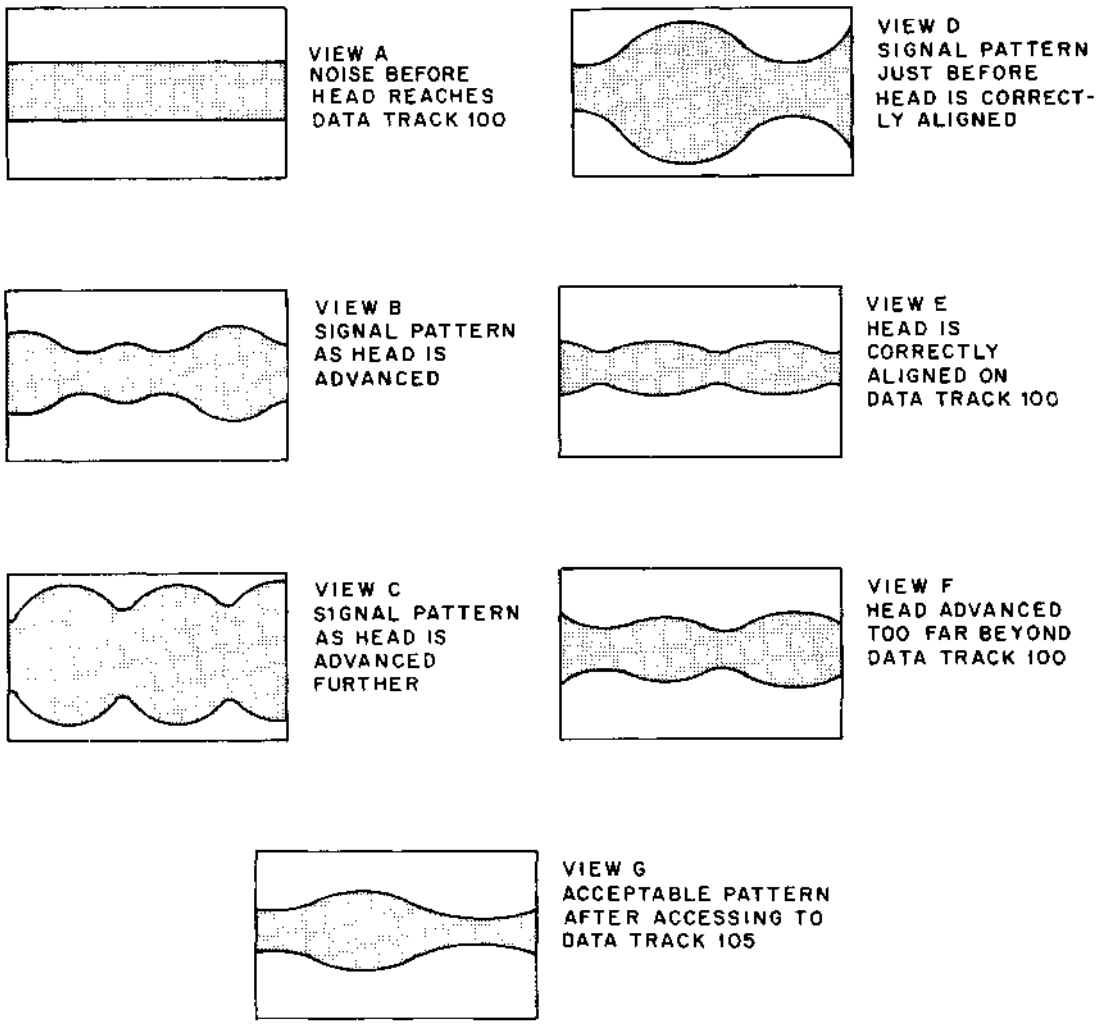

Figure 6-4 Signal Patterns for Data Track 100 Alignment

CP-0027

Step	Procedure
10	Access the motor mount adjusting screws from the rear of the Disk baseplate shown in Figure 6-6, then back the baseplate off to move the read/write head carriage assembly back. Retighten the four #10 screws after adjustment. After the motor mount screws have been tightened, check head alignment to be certain it has been maintained.
11	Set the HD0/HD1 switch to the position corresponding to the head that is farthest from track 100. Be sure the head hold-down clamp is firm enough to hold the head in place, but is loose enough that it will move during adjustment. Move the head towards track 100 and stop adjustment before the head reaches the position shown in Figure 6-4E. Slowly tighten the head hold-down clamp.

CAUTION

Do not overtighten the head clamp screw; the clamp will bend to a point where it will not hold the head assembly in the proper alignment position if it is overtightened.

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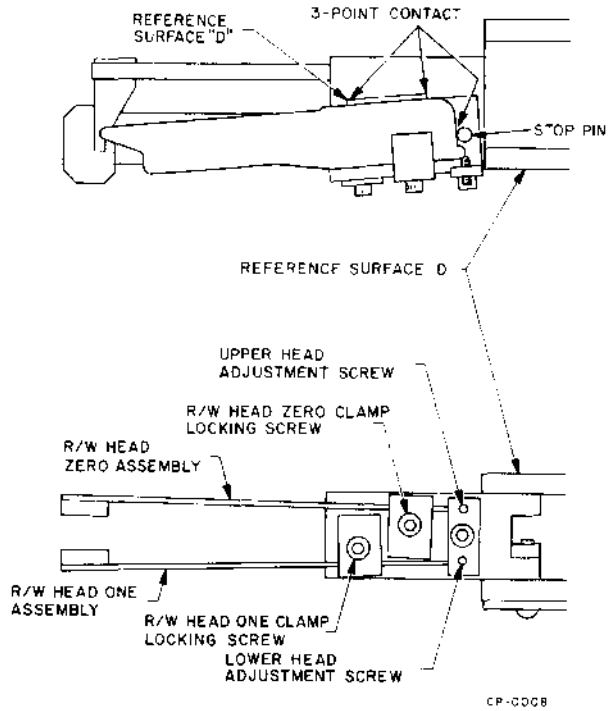

Figure 6-5 Head Adjustment Diagram

Step	Procedure
12	After completing Step 11, do not back-off the head adjustment screw.
13	Repeat Step 11 with the HD0/HD1 switch set to the opposite head.
14	With the head preamplifier adapter connected as in Step 3, set the CE PWB 1-8-32 switch to 1, increment the INT switch five times placing the read/write heads on data track 105, and check both the 0 and 1 side read/write head positions on data track 105 for acceptable limits (see Figure 6-4G).

NOTE

The read/write head adapter, CMD #10C000069G1 must remain connected in Step 4 until the 0 and upper/lower limit switches have been checked due to the switches having to be checked for accuracy with data track 100. A check to determine the accuracy of the OUT LIMIT switch alignment is to step the read/write heads back until they are out of bounds then step the heads forward to data track 100 and observe whether correct alignment is maintained. If alignment is not maintained, Steps 1 through 14 should be repeated. Because the locknuts are sealed, the alignment of the OUT LIMIT switch should normally not vary.

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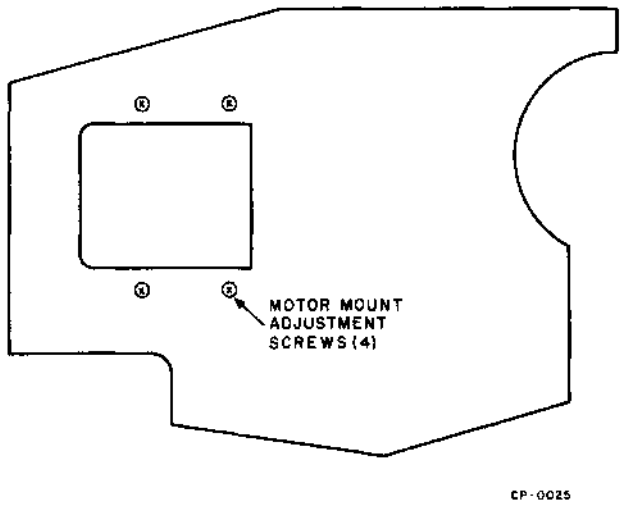

Figure 6-6 R/W Head Stepping Motor Baseplate Adjustment Diagram

Step.	Procedure
15	Following alignment of the read/write heads, return the read/write heads to track 000 and perform the 0 or Home Position Alignment procedures for adjusting home position switch S1 (if necessary). These procedures are described in the Home Position Switch S1 Alignment section of this manual.

6.11 HOME POSITION SWITCH S1 ALIGNMENT

Before performing the following procedures, make certain that read/write head alignment is correct. When performing the following steps, refer to Figure 6-7.

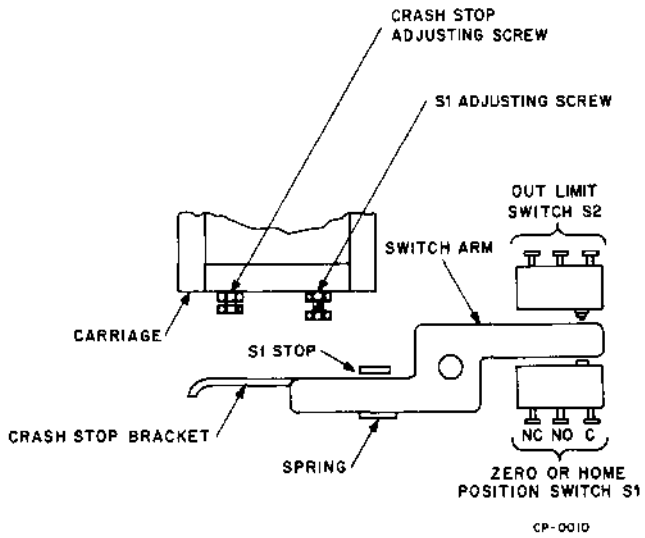

Figure 6-7 Home Position and Inner/Outer Limit Switch Diagram

Step	Procedure
1	Install the CE PWB switch and logic module in the Disk Electronic Module Assembly, slot 25, and load the head alignment CE cartridge, with the red stripe, into the disk in accordance with the Disk Cartridge installation procedures in Chapter 3.
2	Set the CE PWB positioner direction switch to forward and activate the 32 positioner mode switch three times, placing the read/write head on data track 96 followed by single stepping the single step switch four times placing the heads on data track 100. Check this data track to be certain that the correct data is observed before proceeding.
3	Set the CE PWB positioner direction switch to REC and step the 32 positioner mode switch three times placing the read/write heads on data track 004. Check to be certain that the crash-stop adjusting screw does not hit the crash-stop bracket as the heads are stepped the last four tracks to data track 000. If this is the case, compensate by turning the crash-stop adjusting screw inward. Also check to see if the S1 adjusting screw will cause the switch arm to trip the out-limit switch, S2. If this is the case, physically move the out-limit switch, S2, away from the switch arm or turn the S1 adjusting screw inward or both if necessary.
4	Connect a volt-ohmmeter across S1-C and S1-NC. The C connection is at ground and NC is at 0 to 5V. With the read/write heads still on data track 004, check for an audible click or a change in the voltage reading to be certain that the switch arm moves freely and that S1 contact is made and broken as the switch arm is physically moved. NOTE Be careful not to trip switch S2. If the S1 stop is bent so that S1 contacts can not be switched, carefully bend the S1 stop back and/or adjust S1 if necessary.
5	Single step the stepping switch four times to place the read/write heads on data track 000. With the S1 adjusting screw coarsely adjusted, contact is made, and the meter should read 0 Vdc.
6	Set the CE PWB positioner direction switch in the forward position and single step the positioner mode switch once placing the read/write head on data track 001.
7	Insert a 7 mil feeler gauge between the switch arm and the S1 adjusting screw and observe that S1 does not make contact. The meter should record a reading of 5V. Insert an 8 mil feeler gauge in place of the 7 mil gauge and observe that contact is made. The meter should record a reading of 0 Vdc.
8	If switch contact is made in Step 7 with the 7 mil gauge, loosen the inner lock nut on the S1 adjusting screw and readjust it until no contact is made (5V). Retighten the lock nut, and with the appropriate feeler gauge, be certain that S1 does not make contact. If there is contact, repeat Steps 7 and 8 until correct adjustment is attained.

Step	Procedure
9	Reset the CE PWB positioner direction switch to reverse and single step the positioner mode switch once placing the read/write head on data track 000. The distance between the S1 stop and the switch arm must be between 4-6 mils, if not, carefully bend the S1 stop until it is obtained.
10	Set the CE PWB positioner direction switch to forward and activate the 32-positioner mode switch three times placing the read/write head on data track 96 followed by single stepping the single four times which will place the head on data track 100. The signal appearing on data track 100 is shown in Figure 6-4E.
11	Single step the positioner mode switch five times so that the read/write head is on data track 105. The signal appearing on data track 105 is shown in Figure 6-4G. Set the CE PWB 1-8-32 switch to 32 and activate the INT switch three times then place the switch in position 8 and activate the INIT switch once. The read/write heads should be on data track 001. Using a feeler gauge recheck the Home Position S1 switch alignment. Refer to Step 7 of this section.
12	If the results of Steps 10 and 11 are not obtained, repeat the Home Position Switch Alignment procedures until the correct results are obtained.

6.12 OUTER/INNER LIMIT SWITCHES

Before performing the following procedures, make certain that home position switch settings have been correctly adjusted and that the computer central processor cable (CPU) is not connected to the Disk (see Figure 6-7).

6.12.1 Outer Track Stop Switch

Step	Procedure
1	Install the CE PWB switch and logic module in the Disk Electronic Module Assembly slot 25 as shown in Figure 6-2, then load the CE alignment cartridge, with the red stripe, into the disk in accordance with the Disk Cartridge Installation procedures in Chapter 3.
2	Apply dc power to the disk and wait for the READY light to illuminate indicating that the disk is ready for operation.
3	After power has been applied, the read/write head responsyn positioner assembly will return to data track 000.
4	Using a feeler gauge, adjust the out limit switch S2 until there is approximately 5 to 10 mils between the switch arm and the switch plunger on S2.
5	Insert a 20 to 30 mil feeler gauge between the S1 adjusting screw and the switch arm and note the size of the feeler gauge that causes the out limit switch S2 to just make contact. The insertion of the correct feeler gauge will cause the read/write head reponsyn positioner carriage assembly to move forward. Removal of the feeler gauge will allow the carriage to return to the home or data track 000 position.

Step	Procedure
6	If the feeler gauge causing the carriage assembly to move forward is not between 20 to 30 mils, physically adjust the out limit switch S2 so the distance between the switch arm and the plunger of S2 falls within these limits.

NOTE

The 20-30 mil adjustment between the out limit switch S2 and the switch arm is not critical but the adjustment between the home position switch and the S1 adjusting screw is critical.

7	After the correct feeler gauge is found in Step 6, add 5 mils to that size.
8	With the read/write heads positioned on data track 000, insert the feeler gauge calculated in Step 7 between the crash-stop adjusting screw and the crash-stop bracket. If necessary, readjust the crash-stop adjusting screw until the feeler gauge moves freely between the screw and the crash-stop bracket.
9	Retighten the crash-stop adjusting screw lock nut and recheck the clearance between the crash-stop bracket and the crash-stop adjusting screw to ensure free movement of the feeler gauge. If the initial adjustment has been altered appreciably, repeat Steps 8 and 9.
10	Set the CE PWB FWD/REV switch to REV, the 1-8-32 switch to 8, then activate the INIT switch placing the read/write head approximately on data track minus 008. The carriage will automatically reposition itself to data track 000. Reset the CE PWB switches to position the read/write heads on data track 100 and 105 checking each location to be certain correct alignment has been maintained.

6.12.2 Inner Track Stop Switch

Step	Procedure
1	Set the CE PWB FWD/REV switch to FWD, and the 1-8-32 switch to 32, then activate the INIT switch six times placing the read/write head on data track 192. Set the 1-8-32 switch to 8, then activate the INIT switch once placing the read/write head on data track 200.
2	Place the 1-8-32 switch in the single step position and activate the INIT switch four times observing that the in-limit switch S4 does not make contact on data track 204 but should by at least data track 207.
3	If necessary, the switch leaf-spring can be bent to obtain the correct adjustment. If the in-limit switch S4 is not correctly set in Step 2, loosen the S4 hold-down screws and physically reposition the switch until it does not make contact with the head on data track 204.

CAUTION

If the in-limit switch is pushed up against the carriage where contact is made all the time, the read/write head carriage will slowly increment in reverse until it reaches the ZERO or home position switch S1 where it will stop.

Step	Procedure
4	If the out-limit switch S2 and the in-limit switch S4 are made at the same time, the read/write carriage will attempt to increment forward one track then increment in reverse one track until either S2 or S4 are no longer made.
5	After all switch adjustments have been made and the S4 hold down screws are retightened, recheck the setting of the in-limit switch S4 to be certain that the switch does not make contact when the read/write head is on data track 204 but does on or before data track 207.

6.13 SECTOR TRANSDUCER ALIGNMENT

6.13.1 General

The index timing signal for a single disk storage is adjusted to a reference signal when the read/write head is on data track 095. This adjustment allows the Disk to be aligned from a common starting point to maintain capability between two disk drives when reading or writing at the beginning of sector field.

Eight equally-spaced sector pulses that establish the beginning of each sector field are generated during each revolution of the disk. The pulses occur at 5 ms intervals and are 380 ±80 μs wide.

A single 380 ± 80 μs wide index reference pulse is generated once for each revolution of the disk and occurs at a 40 ms time interval. This index pulse serves as a reference point for index timing adjustment.

Before proceeding with the following adjustments, the Head Alignment Adapter, CMB #10C000069G1, must be disconnected between the read/write head preamplifier connector and the preamplifier. It is imperative that data track 100, the 0 or home position switch S1, inner/outer limit switches S2 and S4, and the crash-stop have all been correctly aligned and adjusted.

6.13.2 Procedures

The following procedures aid in checking sector transducer alignment.

Step	Procedure
1	Disconnect the computer central processor (CPU) cable from the Disk and loosen the transducer hold-down screws that lock the transducer in the alignment position.
2	Install the CE PWB alignment cartridge, with the red stripe across its top, into the disk, in accordance with the Disk Cartridge Installation procedures in Chapter 3.

Step	Procedure
3	Apply dc power to the disk and wait approximately 1.5 minutes for the READY light to illuminate, indicating that the disk is ready for operation and the read/write heads are loaded.

CAUTION

Accurate sector transducer alignment cannot be achieved without first allowing 15 minutes for temperature stabilization between the disk surfaces and the read/write heads.

4	Connect the oscilloscope channel one probe to TP11 on the PCDT module in the Electronic Module Assembly slot 12. The resulting photocell output voltage should be 15 ±6V peak-to-peak. If necessary, adjust the voltage amplitude with PCDT control R3, located on the PCDT module.
5	Set the CE PWB 1-8-32 switch to 32 and the FWD/REV switch to FWD, then activate the INT switch twice. Reset the 1-8-32 switch to 8 and activate the INT switch three times, then set the switch to 1 and activate the INT switch seven times. The read/write heads should now be on data track 095.
6	Connect channel two direct or 10:1 probe of the oscilloscope to TP1 on the RAMP/A module in slot 3, and sync the oscilloscope from the index pulse at TP7 on the PCDT module in slot 12. Read the data from track 095.
7	Observe the time delay from the reference pulse to the peak of the timing pulse on data track 095 as shown in Figure 6-8. The delay from the end of the reference pulse to the timing pulse should be 30 ±5 µs for each head.

NOTE

Some waveform jitter will be evident when making this adjustment; therefore, the average pulse position should be used as a reference setting.

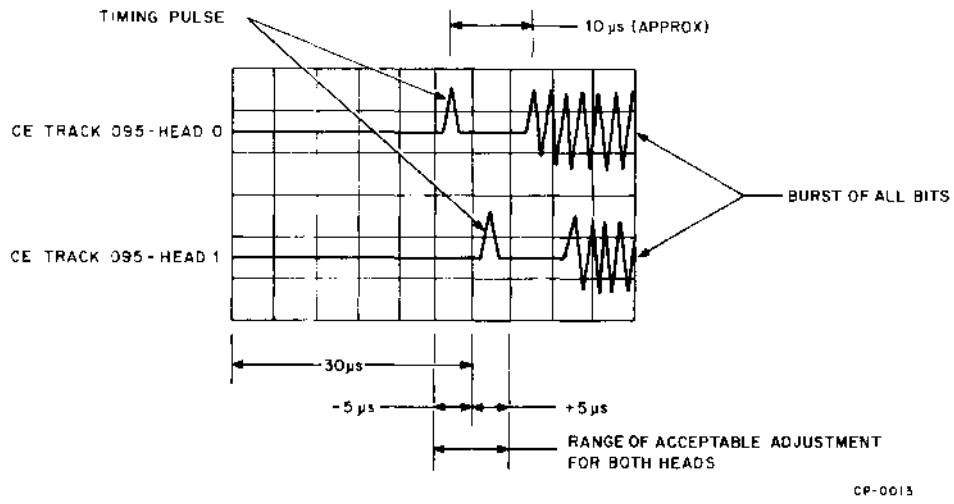

Figure 6-8 Sector Transducer Timing Diagram

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Step	Procedure
8	Determine the magnitude and direction, plus or minus, of the pulse timing correction to be made; a time delay of 30 ±5 μs should prevail for both read/write heads. Read/write head 0 (CE PWB switch setting HD 0) and head 1 (switch setting HD 1) must be checked.
9	The maximum allowable adjustment range between the two heads is shown in Figure 6-8. If the range of the two timing pulses exceeds 10 μs (from the 30 μs time base), the read/write heads must be readjusted using the Read/ Write Head Alignment procedures in Paragraph 6.9. If the adjustment range is exceeded, it is usually due to the read/write head three point spot check not being correct.
10	If adjustment is required as a result of Step 9, the entire disk must first be removed from the cabinet, the disk cover removed, and the two sector transducer locking screws slightly loosened, but not removed (see Figure 6-9).
11	The transducer adjusting screw is accessible from the front of the disk. Adjust this screw to increase or decrease the time delay. Turning the screw clockwise (CW) decreases the time delay and counterclockwise (CCW) increases the time delay. One 360 degree turn of the adjusting screw provides a time delay of 78 μs.
12	Turn the dc power off, remove the CE cartridge, and tighten the transducer locking screws (2) and the locking block to secure the adjustment.
13	Repeat Steps 4 through 8 to be certain that sector transducer timing has been maintained.

NOTE

If disk cartridges are transferred from one disk drive to another, it must be understood that the transducer as well as read/write head alignment must be within 20% of each other for the worst case condition. All alignment must be done with the same CE disk cartridge; disk cartridges have a tolerance range of 10%.

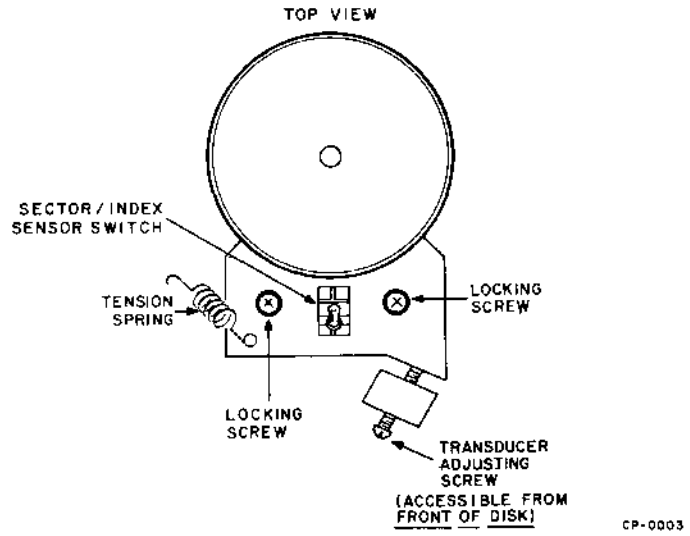

Figure 6-9 Sector Transducer Adjustment Diagram

6.14 LIGHT REPLACEMENT

The following procedures should be followed when replacing indicator and pushbutton lights (see Figures II-43 and II-44).

6.14.1 Replacing Register Indicator Lights

Step	Procedure
1	Remove the indicator light panel.
2	Remove the four Phillips screws securing the light panel to the two mounting brackets, and lower the panel so the printed circuit side of the light board faces upward. Do not put too much stress on the light panel cable.
	NOTE The light panel cable can be disconnected from the logic mounting panel allowing the light panel to be serviced on a bench.
3	Using a low watt soldering iron, approximately 35W, unsolder the leads of the defective bulb and then remove the bulb. A solder-sucker is recommended to remove the excess solder.
4	Before replacing the new bulb, clean out the bulb mounting holes; there should be no solder residue that will block insertion of the new bulb.
5	Install the bulb and cut the leads to the appropriate length, then bend them over; they must lie flat on the printed circuit board.
6	Solder the leads to the printed circuit board.
7	Reassemble the bulb mounting panel and associated dress panel.

6.14.2 Replacement of Pushbutton Lights

Step	Procedure
1	DISK LOCKOUT, SECT PROT, ATTN, OFF, and ON lights are replaced by pulling the plastic pushbutton out of its assembly then removing the bulb from its interior.
2	To replace the bulb, first insert the bulb in the plastic pushbutton, then push it onto the associated pushbutton assembly.

6.15 DISK DRIVE POWER SUPPLY

The physical location of the Disk Drive Power Supply terminal boards T81, -2, -3, and -4; the ac and dc line fuses F1, -2, -3, -4, and -5 are shown in Figure 6-10. The ac and dc voltages and the terminal boards where they terminate are presented in Table 6-11.

The dc input/output voltages for the interior mounted power supply circuit card are shown in Figure 6-11.

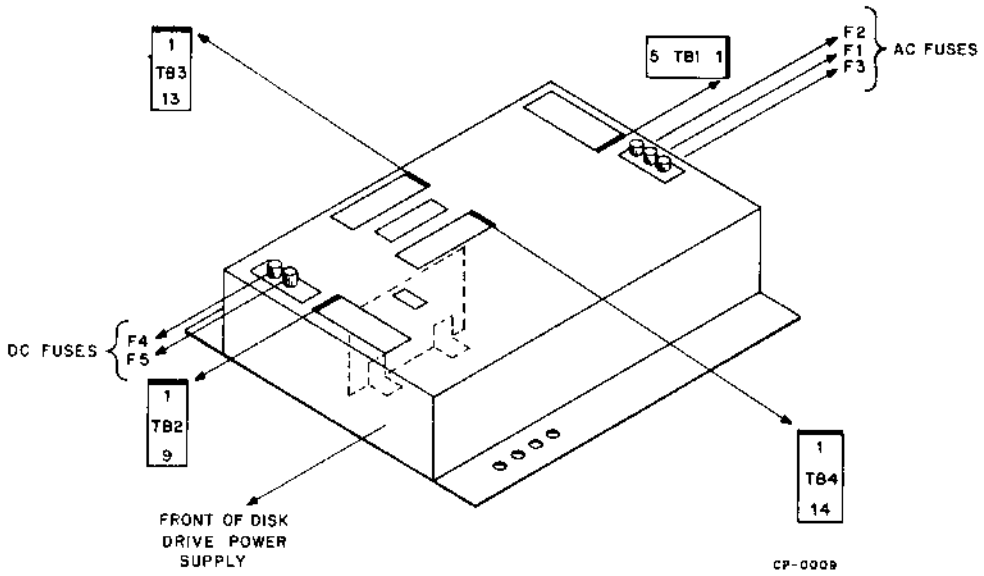

Figure 6-10 Disk Drive Power Supply Fuse and TB Location Diagram

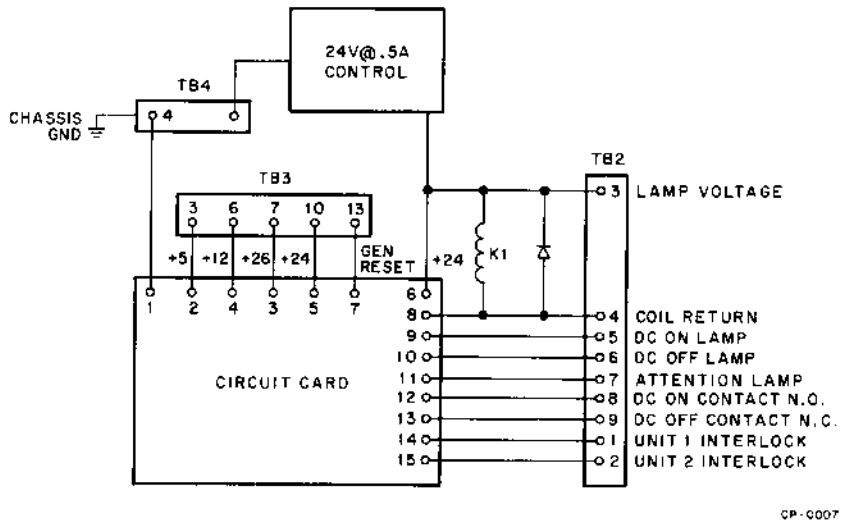

Figure 6-11 Disk Drive Power Supply Circuit Card Connection Diagram

6.16 ac/dc WIRING

The ac/dc power wiring harness within the Disk is shown in Figure II-44.

Table 6-11
AC-DC Voltages Terminal Board Connections

Voltage	Terminal Board and Pin No.
115 Vac, 60 Hz	TB1 - 1
115 Vac (neutral)	TB1 - 2
Earth Ground	TB1 - 3
115 Vac (neutral)	TB1 - 4
Controlled 115 Vac	TB1 - 5
Unit 1 Interlock	TB2 - 1
Unit 2 Interlock	TB2 - 2
+24V control voltage	TB2 - 3
DC ON lamp	TB2 - 5
DC OFF lamp	TB2 - 6
Attention lamp	TB2 - 7
DC ON contact - NO	TB2 - 8
DC OFF contact - NC	TB2 - 9
+5V	TB3 - 1,2,3
+12V	TB3 - 4,5,6
-26V	TB3 - 7,8,9
+24V	TB3 - 10,11,12
General Reset	TB3 - 13
Ground Bus	TB4 - 3 - 9, 12 - 14

6.17 SIGNAL INDEX

To easily determine the logic circuit the RK01-X and RK08 signals originate from, refer to Engineering Specifications RK08-0-30 and RK01-X-16.

— IOT DECODING — (D-BS-RK08-0-05)

Signal	Source	Drawing No.
INITIALIZE L	SKIP AND BREAK	D-BS-RK08-0-06
MAIN DB TO AC L	MAINTENANCE REGISTER	D-BS-RK08-0-07

— SKIP AND BREAK — (D-BS-RK08-0-06)

B BREAK (0) H	I/O AND DATA BREAK CABLES	D-BS-RK08-0-25
B ADD ACCEPTED (0) H	I/O AND DATA BREAK CABLES	D-BS-RK08-0-25
B INITIALIZE H	I/O AND DATA BREAK CABLES	D-BS-RK08-0-25
B RUN (0) H	I/O AND DATA BREAK CABLES	D-BS-RK08-0-25
BTS 03 (1) H	I/O AND DATA BREAK CABLES	D-BS-RK08-0-25
BTS 01 (1) H	I/O AND DATA BREAK CABLES	D-BS-RK08-0-25
CLEAR ALL (1) H	IOT DECODING	D-BS-RK08-0-05
SET DATA BREAK REQ H	WRITE	D-BS-RK08-0-11
CHECK PARITY (0) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
LOAD DISK ADDR L	IOT DECODING	D-BS-RK08-0-05
LOAD COMMAND L	IOT DECODING	D-BS-RK08-0-05
LOAD COMMAND H	IOT DECODING	D-BS-RK08-0-05
AC STROBE L	IOT DECODING	D-BS-RK08-0-05
LOAD WC L	IOT DECODING	D-BS-RK08-0-05
LOAD CA L	IOT DECODING	D-BS-RK08-0-05
CLEAR ALL 1 L	IOT DECODING	D-BS-RK08-0-05
WRITE FLOP (1) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
WRITE FLOP (0) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
ERROR (0) H	STATUS REGISTER	D-BS-RK08-0-15
ERROR (1) H	STATUS REGISTER	D-BS-RK08-0-15
CODE 7 H	IOT DECODING	D-BS-RK08-0-05
IOT 6741 L	IOT DECODING	D-BS-RK08-0-05
TRANSFER DONE FLAG (0) H	STATUS REGISTER	D-BS-RK08-0-15
TRANSFER DONE FLAG (1) H	STATUS REGISTER	D-BS-RK08-0-15
CODE 5 H	IOT DECODING	D-BS-RK08-0-05

— MAINTENANCE REGISTER —
(D-BS-RK08-0-07)

Signal	Source	Drawing No.
LOAD MAIN H	IOT DECODING	D-BS-RK08-0-05
MAIN GO H	IOT DECODING	D-BS-RK08-0-05
CLEAR ALL 1 H	IOT DECODING	D-BS-RK08-0-05
INDEX PULSE H	DISK SELECTION	D-BS-RK01-X-05
FORMAT H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09

— MAJOR SEQUENCER—
(D-BS-RK08-0-08)

WRITE CLOCK H	FORMAT DELAYS	D-BS-RK01-X-01
UNFORMATTED (1) H	MAINTENANCE REGISTER	D-BS-RK08-0-07
UNFORMATTED (0) H	MAINTENANCE REGISTER	D-BS-RK08-0-07
WRITE 13 H	WRITE	D-BS-RK08-0-11
READ 13 H	READ	D-BS-RK08-0-10
FORMAT HEADER DELAY L	FORMAT DELAYS	D-BS-RK01-X-01
READ HEADER DELAY L	FORMAT DELAYS	D-BS-RK01-X-01
RESET MAJOR L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
CLEAR ALL 2 L	IOT DECODING	D-BS-RK08-0-05
RUN (0) L	SKIP AND BREAK	D-BS-RK08-0-06
ERROR (1) L	STATUS REGISTER	D-BS-RK08-0-15
FORMAT DATA DELAY L	FORMAT DELAYS	D-BS-RK01-X-01
READ DATA DELAY L	FORMAT DELAYS	D-BS-RK01-X-01
WRITE DATA DELAY L	FORMAT DELAYS	D-BS-RK01-X-01
SET MAJOR B H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
SET MAJOR C H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
R/W (0) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
READ DATA H	READ	D-BS-RK-9-0-10
NEW SELECT (1) H	TRACK SEEK	D-BS-RK01-X-02, Sheet 1 of 2
BUFF SECTOR PULSE H	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 2 of 2
READ SET MAJOR J L	READ	D-BS-RK08-0-10
GO TO J-K H	WRITE	D-BS-RK08-0-11
READ SET MAJOR K H	READ	D-BS-RK08-0-10
GO TO MAJOR I H	WRITE	D-BS-RK08-0-11

— R/W COMMANDS, FIND SECTOR, END TRANSFER —
(D-BS-RK08-0-09)

Signal	Source	Drawing No.
UNFORMATTED (1) H	MAINTENANCE REGISTER	D-BS-RK08-0-07
LOAD COMMAND H	IOT DECODING	D-BS-RK08-0-05
CLEAR ALL 1 H	IOT DECODING	D-BS-RK08-0-05
CLEAR ALL 2 H	IOT DECODING	D-BS-RK08-0-05
LOAD DISK ADDR H	IOT DECODING	D-BS-RK08-0-05
WRITE DATA DELAY H	FORMAT DELAYS	D-BS-RK01-X-01
ZERO SEQUENCER H	MAJOR SEQUENCER	D-BS-RK08-0-08
ERASE DELAY H	FORMAT DELAYS	D-BS-RK01-X-01
UNFORMATTED (1) L	MAINTENANCE REGISTER	D-BS-RK08-0-07
I/O START H	IOT DECODING	D-BS-RK08-0-05
W/C OVERFLOW (1) L	W/C REGISTER	D-BS-RK08-0-18
ERASE DELAY L	FORMAT DELAYS	D-BS-RK01-X-01
FIND NEXT SECTOR L	READ	D-BS-RK08-0-10
ZERO MAJOR L	READ	D-BS-RK08-0-10
ERROR (1) L	STATUS REGISTER	D-BS-RK08-0-15
CLEAR ALL 1 L	IOT DECODING	D-BS-RK08-0-05
CLEAR ALL 2 L	IOT DECODING	D-BS-RK08-0-05
READ 13 H	READ	D-BS-RK08-0-10
TRACK LOCATED L	TRACK SEEK	D-BS-RK01-X-02
WRITE CLOCK H	FORMAT DELAYS	D-BS-RK01-X-01
NEW SELECT (1) L	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 1 of 2
SECTOR SYNCH DELAY L	FORMAT DELAYS	D-BS-RK01-X-01
CLEAR SECTOR L	SECTOR ADDRESSING	D-BS-RK08-0-16
SET WRITE L	IOT DECODING	D-BS-RK08-0-05
SET CHECK PARITY L	IOT DECODING	D-BS-RK08-0-05
SECTOR SYNCH PULSE H	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 2 of 2
SECTOR EQUAL H	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 2 of 2
COUNT SECTOR L	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 1 of 2

— READ —
(D-BS-RK08-0-10)

NORMAL R/W H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
BLOCK COUNT 256 (0) H	BIT AND BLOCK COUNTER	D-BS-RK08-0-17

Signal	Source	Drawing No.
UNFORMATTED (1) H	MAINTENANCE REGISTER	D-BS-RK08-0-07
UNFORMATTED (0) H	MAINTENANCE REGISTER	D-BS-RK08-0-07
R/W (0) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
BIT COUNT 12 (1) H	BIT AND BLOCK COUNTER	D-BS-RK08-0-17
CLEAR ALL 1 L	IOT DECODING	D-BS-RK08-0-05
DISK READ CLOCK L	DISK SELECTION	D-BS-RK01-X-05
DISK READ DATA H	DISK SELECTION	D-BS-RK01-X-05
WRITE 13 L	WRITE	D-BS-RK08-0-11
BIT COUNT 12 (0) H	BIT AND BLOCK COUNTER	D-BS-RK08-0-17
MAJOR E + F + I + J H	WRITE	D-BS-RK08-0-11
WRITE SHIFT SR L	WRITE	D-BS-RK08-0-11
DATA OUT (1) L	WRITE	D-BS-RK08-0-11
NEW SELECT (0) H	WRITE	D-BS-RK08-0-11
NORMAL R/W L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
SECTOR NOT EQUAL H	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 2 of 2
TRACK EQUAL L	COMPARE TRACK ADDRESS	D-BS-RK01-X-04
READ ALL L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
NORMAL WRITE H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
SECTOR PROTECT SW H	TRACK SEEK	D-BS-RK01-X-02 Sheet 2 of 2
ZERO SEQUENCER L	MAJOR SEQUENCER	D-BS-RK08-0-08
BLOCK COUNT 256 (1) H	BIT AND BLOCK COUNTER	D-BS-RK08-0-17
NEW SELECT (1) H	TRACK SEEK	D-BS-RK01-X-02 Sheet 1 of 2
CLR SHIFT IN WD PAR L	BIT AND BLOCK COUNTER	D-BS-RK08-0-07
LONG PARITY L	STATUS REGISTER	D-BS-RK08-0-15

— WRITE —
(D-BS-RK08-0-11)

Signal	Source	Drawing No.
WRITE ALL H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
BIT COUNT 12 (1) H	BIT AND BLOCK COUNTER	D-BS-RK08-0-17
BIT COUNT 12 (0) H	BIT AND BLOCK COUNTER	D-BS-RK08-0-17
R/W (1) L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
R/W (1) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09

Signal	Source	Drawing No.
NORMAL WRITE H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
WRITE CLOCK H	FORMAT DELAYS	D-BS-RK01-X-01
UNFORMATTED WRITE H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
UNFORMATTED (1) H	MAINTENANCE REGISTER	D-BS-RK08-0-07
WRITE DATA SYNCH DELAY	FORMAT DELAYS	D-BS-RK01-X-01
FORMAT DATA DELAY	FORMAT DELAYS	D-BS-RK01-X-01
FORMAT HEADER DELAY	FORMAT DELAYS	D-BS-RK01-X-01
BLOCK COUNT 256 (0) H	BIT AND BLOCK COUNTER	D-BS-RK08-0-17
UNFORMATTED (0) H	MAINTENANCE REGISTER	D-BS-RK08-0-07
WRITE FLOP (1) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
BLOCK COUNT 256 (1) H	BIT AND BLOCK COUNTER	D-BS-RK08-0-17
WC OVERFLOW (0) H	WC REGISTER	D-BS-RK08-0-18
SET MAJOR C H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
WRITE CLOCK L	FORMAT DELAYS	D-BS-RK01-X-01
SET MAJOR G H	MAJOR SEQUENCER	D-BS-RK08-0-08
WORD PARITY (0) H	READ	D-BS-RK08-0-10
SR TO DB L	READ	D-BS-RK08-0-10
MAJOR E + F H	READ	D-BS-RK08-0-10
	—DATA BUFFER— (D-BS-RK08-0-12)	
SR TO DB L	READ	D-BS-RK08-0-10
MAIN SR TO DB L	MAINTENANCE REGISTER	D-BS-RK08-0-07
LOAD DB L	SKIP AND BREAK	D-BS-RK08-0-06
WRITE FLOP (1) L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
CLEAR ALL 1 H	IOT DECODING	D-BS-RK08-0-05
BREAK (1) H	SKIP AND BREAK	D-BS-RK08-0-06

— DATA SHIFT REGISTER—
(D-BS-RK08-0-13)

Signal	Source	Drawing No.
SHIFT INPUT (1) L	READ	D-BS-RK08-0-10
ENBL DB TO SR L	WRITE	D-BS-RK08-0-11
ENBL LP TO SR L	WRITE	D-BS-RK08-0-11
LP TO SR L	WRITE	D-BS-RK08-0-11
CLEAR ALL 1 H	IOT DECODING	D-BS-RK08-0-05
ENABLE SHIFT SR H	WRITE	D-BS-RK08-0-11
SHIFT SR L	READ	D-BS-RK08-0-10
MAIN SHIFT SR L	MAINTENANCE REGISTER	D-BS-RK08-0-07
DB TO SR L	WRITE	D-BS-RK08-0-11

— LONGITUDINAL PARITY—
(D-BS-RK08-0-14, Sheet 1 of 2)

CLEAR ALL 1 L	IOT DECODING	D-BS-RK08-0-05
WRITE FORM LP L	WRITE	D-BS-RK08-0-11
SET MAJOR 1 L	MAJOR SEQUENCER	D-BS-RK08-0-08
READ FORM LP L	READ	D-BS-RK08-0-10

— LONGITUDINAL PARITY—
(D-BS-RK08-0-14, Sheet 1 of 2)

STROBE LP H	LONGITUDINAL PARITY	D-BS-RK08-0-14, Sheet 1 of 2
LP06 CRY L	LONGITUDINAL PARITY	D-BS-RK08-0-14, Sheet 1 of 2
LP ENBL H	LONGITUDINAL PARITY	D-BS-RK08-0-14, Sheet 1 of 2

— STATUS REGISTER—
(D-BS-RK08-0-15)

END TRANSFER L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
INITIALIZE L	SKIP AND BREAK	D-BS-RK08-0-06
PROTECT L	TRACK SEEK	D-BS-RK01-X-02, Sheet 2 of 2
SET TRACK FOUND H	TRACK SEEK	D-BS-RK01-X-02,
IOT START H	IOT DECODING	D-BS-RK08-0-05
IOT CLEAR L	IOT DECODING	D-BS-RK08-0-05
SET NON DRIVE ERROR L	DISK SELECTION	D-BS-RK01-X-05
SET TRACK CAP ERROR L	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 1 of 2

Signal	Source	Drawing No.
PROTECT BIT ON L	READ	D-BS-RK08-0-10
SET SECTOR NO GOOD L	READ	D-BS-RK08-0-10
SET PARITY ERROR L	READ	D-BS-RK08-0-10
SET DATA RATE ERROR L	SKIP AND BREAK	D-BS-RK08-0-06
SET TRACK ERROR L	READ	D-BS-RK08-0-10
LOAD COMMAND L	IOT DECODING	D-BS-RK08-0-05
LOAD DISK ADDR L	IOT DECODING	D-BS-RK08-0-05
MAIN GO L	IOT DECODING	D-BS-RK08-0-05
LOAD WC L	IOT DECODING	D-BS-RK08-0-05
LOAD CA L	IOT DECODING	D-BS-RK08-0-05
SET TIME OUT ERROR L	TRACK SEEK	D-BS-RK01-X-02 Sheet 2 of 2
CLEAR ALL 1 L	IOT DECODING	D-BS-RK08-0-05
CLEAR STATUS L	IOT DECODING	D-BS-RK08-0-05

— SECTOR ADDRESSING —
(D-BS-RK08-0-16, Sheet 1 of 2)

Signal	Source	Drawing No.
LOAD DISK ADDR H	IOT DECODING	D-BS-RK08-0-05
CLEAR ALL 1 H	IOT DECODING	D-BS-RK08-0-05
INCR. SECTOR ADDR H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
SR TO COUNTER H	READ	D-BS-RK08-0-10
DISK ADDR TO COUNTER H	MAINTENANCE REGISTER	D-BS-RK08-0-07
MAIN SECTOR PULSE L	MAINTENANCE REGISTER	D-BS-RK08-0-07
CLEAR ALL 1 L	IOT DECODING	D-BS-RK08-0-05
RESET SECTOR L	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 2 of 2
SECTOR SYNCH PULSE L	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 2 of 2
INDEX MARK L	MAINTENANCE REGISTER	D-BS-RK08-0-07
WAIT INDEX (0) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
SECTOR SYNCH PULSE H	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 2 of 2
FORMAT H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
E RESET CNTR L	READ	D-BS-RK08-0-10
MAIN RESET CNTR L	MAINTENANCE REGISTER	D-BS-RK08-0-07
CLEAR SECTOR L	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 1 of 2

Signal	Source	Drawing No.
SECTOR PULSE H	DISK SELECTION	D-BS-RK01-X-05
	— BIT AND BLOCK COUNTER — (D-BS-RK08-0-17)	
CLEAR ALL 1 L	IOT DECODING	D-BS-RK08-0-05
CLEAR BIT COUNT L	READ	D-BS-RK08-0-10
SHIFT SR H	READ	D-BS-RK08-0-10
IOT START L	IOT DECODING	D-BS-RK08-0-05
WRITE FLOP (0) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
COUNT BLOCK H	WRITE	D-BS-RK08-0-11
	— WC REGISTER — (D-BS-RK08-0-18)	
CLR WCOV L	IOT DECODING	D-BS-RK08-0-05
CLEAR WC L	IOT DECODING	D-BS-RK08-0-05
LOAD WC H	IOT DECODING	D-BS-RK08-0-05
SET DATA BREAK REQ H	WRITE	D-BS-RK08-0-11
	— CURRENT ADDRESS and EMA REG — (D-BS-RK08-0-19)	
CLEAR CA L	IOT DECODING	D-BS-RK08-0-05
LOAD COMMAND H	IOT DECODING	D-BS-RK08-0-05
CLEAR ALL 1 L	IOT DECODING	D-BS-RK08-0-05
SET DATA BREAK REQ H	WRITE	D-BS-RK08-0-11
LOAD CA H	IOT DECODING	D-BS-RK08-0-05
	— AC INPUT GATING 00-05 — (D-BS-RK08-0-20)	
ERROR (1) H	STATUS REGISTER	D-BS-RK08-0-15
TRANSFER DONE FLAG (1) H	STATUS REGISTER	D-BS-RK08-0-15
CONT BUSY ERROR (1) H	STATUS REGISTER	D-BS-RK08-0-15
TIME OUT ERROR (1) H	STATUS REGISTER	D-BS-RK08-0-15
PARITY ERROR (1) H	STATUS REGISTER	D-BS-RK08-0-15
DATA RATE ERROR (1) H	STATUS REGISTER	D-BS-RK08-0-15
ENABLE INT DONE (1) H	SKIP AND BREAK	D-BS-RK08-0-06
ENABLE INT ERROR (1) H	SKIP AND BREAK	D-BS-RK08-0-06
SEEK TRK (1) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09

Signal	Source	Drawing No.
ACCESS HEADER (1) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
AC STROBE L	IOT DECODING	D-BS-RK08-0-05
P CODE 1 H	IOT DECODING	D-BS-RK08-0-05
P CODE 2 H	IOT DECODING	D-BS-RK08-0-05
P CODE 3 H	IOT DECODING	D-BS-RK08-0-05
P CODE 4 H	IOT DECODING	D-BS-RK08-0-05
P CODE 6 H	IOT DECODING	D-BS-RK08-0-05
P CODE 7 H	IOT DECODING	D-BS-RK08-0-05
	— AC INPUT GATING 06-11 — (D-BS-RK08-0-21)	
TRACK ADDR ERROR (1) H	STATUS REGISTER	D-BS-RK08-0-15
SECTOR NO GOOD (1) H	STATUS REGISTER	D-BS-RK08-0-15
WRITE LOCK ERROR (1) H	STATUS REGISTER	D-BS-RK08-0-15
TRACK CAP EXC (1) H	STATUS REGISTER	D-BS-RK08-0-15
NON DRIVE (1) H	STATUS REGISTER	D-BS-RK08-0-15
BUSY (1) H	STATUS REGISTER	D-BS-RK08-0-15
AC STROBE L	IOT DECODING	D-BS-RK08-0-05
EXT DISK 0 (1) H	CURRENT ADDRESS & EMA REG.	D-BS-RK08-0-19
EMA 0 (1) H	CURRENT ADDRESS & EMA REG.	D-BS-RK08-0-19
EMA 1 (1) H	CURRENT ADDRESS & EMA REG.	D-BS-RK08-0-19
EMA 2 (1) H	CURRENT ADDRESS & EMA REG.	D-BS-RK08-0-19
EXT DISK 1 (1) H	CURRENT ADDRESS & EMA REG.	D-BS-RK08-0-19
EXT DISK 2 (1) H	CURRENT ADDRESS & EMA REG.	D-BS-RK08-0-19
P CODE 1 H	IOT DECODING	D-BS-RK08-0-05
P CODE 2 H	IOT DECODING	D-BS-RK08-0-05
P CODE 3 H	IOT DECODING	D-BS-RK08-0-05
P CODE 4 H	IOT DECODING	D-BS-RK08-0-05
P CODE 6 H	IOT DECODING	D-BS-RK08-0-05
P CODE 7 H	IOT DECODING	D-BS-RK08-0-05

— FORMAT DELAYS —
(D-BS-RK01-X-01)

Signal	Source	Drawing No.
DATA OUT (1) L	WRITE	D-BS-RK08-0-11
CHECK SECTOR (1) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
CHECK SECTOR (1) L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
WRITE ALL H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
NORMAL WRITE H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
R/W (0) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
R/W (0) L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
UNFORMATTED (0) H	MAINTENANCE REGISTER	D-BS-RK08-0-07
CLEAR ALL 2 L	IOT DECODING	D-BS-RK08-0-05

— TRACK SEEK —
(D-BS-RK01-X-02, Sheet 1 of 2)

IOT CLEAR L	IOT DECODING	D-BS-RK08-0-05
HOME (0) L	DISK SELECTION	D-BS-RK01-X-05
POSITION (1) L	DISK SELECTION	D-BS-RK01-X-05
IOT START H	IOT DECODING	D-BS-RK08-0-05
PROTECT L	TRACK SEEK	D-BS-RK01-X-02, Sheet 2 of 2
STEP COMPLETE H	DISK SELECTION	D-BS-RK01-X-05
TRACK CNTR GREATER L	COMPARE TRACK ADDR	D-BS-RK01-X-04
TRACK CNTR LESS H	COMPARE TRACK ADDR	D-BS-RK01-X-04
EXT DISK 0 (0) L	DISK AND TRACK ADDRESS	D-BS-RK01-X-03
EXT DISK 0 (1) L	DISK AND TRACK ADDRESS	D-BS-RK01-X-03
EXT DISK 1 (0) L	DISK AND TRACK ADDRESS	D-BS-RK01-X-03
DISK ERROR (1) L	STATUS REGISTER	D-BS-RK08-0-15
EXT DISK 1 (1)	DISK AND TRACK ADDRESS	D-BS-RK01-X-03

Signal	Source	Drawing No.
NORMAL R/W H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
LOAD DISK ADDR L	IOT DECODING	D-BS-RK08-0-05
POSITION (1) H	DISK SELECTION	D-BS-RK08-0-05
SEEK TRACK (0) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
SEEK TRACK (1) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
TRACK EQUAL H	COMPARE TRACK ADDR	D-BS-RK08-0-04
TRACK EQUAL L	COMPARE TRACK ADDR	D-BS-RK08-0-04
RESET NEW SELECT H	READ	D-BS-RK08-0-10
BUSY (1) H	STATUS REGISTER	D-BS-RK08-0-15
CLEAR ALL 02 L	IOT DECODING	D-BS-RK08-0-05
	— TRACK SEEK — (D-BS-RK01-X-02, Sheet 2 of 2)	
WRITE ALL L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
UNFORMATTED WRITE L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
WRITE FLOP (1) H	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
INDEX PULSE H	DISK SELECTION	D-BS-RK08-0-05
BUSY (0) L	STATUS REGISTER	D-BS-RK08-0-15
DISK 00 H	DISK SELECTION	D-BS-RK08-0-05
DISK 01 H	DISK SELECTION	D-BS-RK08-0-05
DISK 02 H	DISK SELECTION	D-BS-RK08-0-05
DISK 03 H	DISK SELECTION	D-BS-RK08-0-05
	— DISK AND TRACK ADDRESS — (D-BS-RK01-X-03)	
LOAD COMMAND L	IOT DECODING	D-BS-RK08-0-05
LOAD COMMAND H	IOT DECODING	D-BS-RK08-0-05
INITIALIZE L	SKIP AND BREAK	D-BS-RK08-0-06
CLEAR ALL 2 H	IOT DECODING	D-BS-RK08-0-05

Signal	Source	Drawing No.
SR TO COUNTER H	READ	D-BS-RK08-0-10
DISK ADDR TO COUNTER H	MAINTENANCE REGISTER	D-BS-RK08-0-07
RESET TRACK SEC CNTRS L	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 2 of 2
RESET TRACK CNTR L	TRACK SEEK	D-BS-RK01-X-02, Sheet 1 of 2
COUNT TRACK H	TRACK SEEK	D-BS-RK01-X-02, Sheet 1 of 2
ENABLE TRACK ENT H	TRACK SEEK	D-BS-RK01-X-02, Sheet 1 of 2
UP CNT (1) H	TRACK SEEK	D-BS-RK01-X-02, Sheet 1 of 2
LOAD DISK ADDR H	IOT DECODING	D-BS-RK08-0-05
	— DISK SELECTION — (D-BS-RK01-X-05)	
DISK 00 L	DISK AND TRACK ADDRESS	D-BS-RK01-X-03
DISK 01 L	DISK AND TRACK ADDRESS	D-BS-RK01-X-03
DISK 02 L	DISK AND TRACK ADDRESS	D-BS-RK01-X-03
DISK 03 L	DISK AND TRACK ADDRESS	D-BS-RK01-X-03
STEP IN L	TRACK SEEK	D-BS-RK01-X-02, Sheet 1 of 2
STEP OUT L	TRACK SEEK	D-BS-RK01-X-02, Sheet 1 of 2
ERASE (1) L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
SELECT SURFACE (0) L	SECTOR ADDRESSING	D-BS-RK08-0-16, Sheet 1 of 2
R/W (1) L	R/W COMMANDS, FIND SECTOR	D-BS-RK08-0-09
DATA TO DISK (0) L	FORMAT DELAYS	D-BS-RK01-X-01
BUSY (1) H	STATUS REGISTER	D-BS-RK08-0-15
DISK STEP COMPLETE 0 H	DISK CABLES	D-BS-RK01-X-06
DISK STEP COMPLETE 1 H	DISK CABLES	D-BS-RK01-X-06
DISK STEP COMPLETE 2 H	DISK CABLES	D-BS-RK01-X-06
DISK STEP COMPLETE 3 H	DISK CABLES	D-BS-RK01-X-06
DISK HOME POSITION 0 H	DISK CABLES	D-BS-RK01-X-06
DISK HOME POSITION 1 H	DISK CABLES	D-BS-RK01-X-06
DISK HOME POSITION 2 H	DISK CABLES	D-BS-RK01-X-06
DISK HOME POSITION 3 H	DISK CABLES	D-BS-RK01-X-06

Signal	Source	Drawing No.
DISK POSITION ERROR 0 H	DISK CABLES	D-BS-RK01-X-06
DISK POSITION ERROR 1 H	DISK CABLES	D-BS-RK01-X-06
DISK POSITION ERROR 2 H	DISK CABLES	D-BS-RK01-X-06
DISK POSITION ERROR 3 H	DISK CABLES	D-BS-RK01-X-06
DISK NOT READY 0 H	DISK CABLES	D-BS-RK01-X-06
DISK NOT READY 1 H	DISK CABLES	D-BS-RK01-X-06
DISK NOT READY 2 H	DISK CABLES	D-BS-RK01-X-06
DISK NOT READY 3 H	DISK CABLES	D-BS-RK01-X-06
DISK INDEX PULSE 0 H	DISK CABLES	D-BS-RK01-X-06
DISK INDEX PULSE 1 H	DISK CABLES	D-BS-RK01-X-06
DISK INDEX PULSE 2 H	DISK CABLES	D-BS-RK01-X-06
DISK INDEX PULSE 3 H	DISK CABLES	D-BS-RK01-X-06
DISK SECTOR PULSE 0 H	DISK CABLES	D-BS-RK01-X-06
DISK SECTOR PULSE 1 H	DISK CABLES	D-BS-RK01-X-06
DISK SECTOR PULSE 2 H	DISK CABLES	D-BS-RK01-X-06
DISK SECTOR PULSE 3 H	DISK CABLES	D-BS-RK01-X-06
DISK READ DATA 0 H	DISK CABLES	D-BS-RK01-X-06
DISK READ DATA 1 H	DISK CABLES	D-BS-RK01-X-06
DISK READ DATA 2 H	DISK CABLES	D-BS-RK01-X-06
DISK READ DATA 3 H	DISK CABLES	D-BS-RK01-X-06
DISK READ CLOCK 0 H	DISK CABLES	D-BS-RK01-X-06
DISK READ CLOCK 1 H	DISK CABLES	D-BS-RK01-X-06
DISK READ CLOCK 2 H	DISK CABLES	D-BS-RK01-X-06
DISK READ CLOCK 3 H	DISK CABLES	D-BS-RK01-X-06

Table 6-12
CMD Module Placement

Slot #	Color Code	CMD Ident. #	Function
A03	YY	RAMP/A	Read
A04	RO	EAMP	Erase
A06	RR	WAMP/A	Write
A07	YO	PKDT	
A09	OO	DDBD	
A11	RY	DSBD/A	
A12	WW	PCDT	
A13	WO	DRBD/A	
A15	WY	IOHN	Cable to Logic
A17	RW	SPCA	Cable to Disk
A18	BB	G11N	
A19	BO	G21N	
A20	BW	FFUN	
A21	BY	G31N	
A22	BR	G41N	
A23	BO	G21N	

Y - Yellow
R - Red
O - Orange
W - White
B - Blue

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Your comments and suggestions will help up in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgement is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

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What features are most useful? _____

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What faults do you find with the manual? _____

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Does it satisfy *your* needs? _____ Why? _____

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