DEC-11-HRFB-D

# RF11/RS11
# DECdisk system
# manual

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Edition March 1971
2nd Printing (Rev) August 1971

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# FOREWORD

This manual provides the user with the theory of operation and logic diagrams necessary to understand and maintain the RF11/RS11 DECdisk System. General and detailed descriptions of the RF11 Control and the RS11 Disk are included. It is assumed that the reader is familiar with basic PDP-11 operation.

Although control signals and data are transferred between the RF11 Control and the Unibus™, it is beyond the scope of this manual to cover the operation of the Unibus. A detailed description of the Unibus is presented in the *PDP-11 Unibus Interface Manual* (DEC-HIAA-D).

The manual is divided into 6 major sections: general description, installation, operation, programming, detailed description and maintenance. The appendix contains the RF11/RS11 signal designations and definitions.

A complete set of engineering drawings is provided with each RF11/RS11 DECdisk System. These drawings are contained in a separate volume entitled *RF11/RS11 DECdisk System, Engineering Drawings* and reflect the latest print revisions which correspond to the specific system shipped to the user.

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# CHAPTER 1
# RF11/RS11 GENERAL DESCRIPTION

## 1.1 INTRODUCTION

The RF11/RS11 DECdisk System is a PDP-11 Computer peripheral. The RF11/RS11 serves as an additional random access memory unit to the PDP-11 System. Each RF11/RS11 Disk System consists of an RF11 Controller and from one to eight optional RS11 Disk units. The RF11 Controller interfaces the RS11 Disk unit or units to the Unibus. The RF11 also converts the serial data off the RS11s to parallel data on the Unibus and vice versa. Therefore, the RF11/RS11 Disk System reads and writes serial memory information in parallel transfer to or from the PDP-11 Unibus.

## 1.2 FUNCTIONAL DESCRIPTION

The RF11 Control and the RS11 Disk combine as a fast, low-cost, random access, bulk storage package for the PDP-11 Computer. The system stores digital data on fixed-head rotating disks in a serial format. The data can be randomly accessed and, when necessary, protected from overwriting. One RS11 and the RF11 provide 262,144 ($2^{18}$) 17-bit words (16 data bits and one parity bit) of storage. Up to eight RS11 disks can be controlled by one RF11 for a total of 2,097,152 ($2^{21}$) words of storage. The RS11 units are interfaced with the RF11 by the parallel disk bus that carries both control and data information (see Figure 1-1).

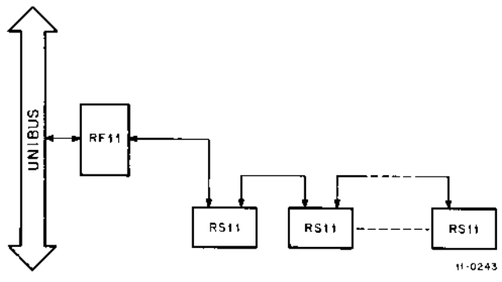



Figure 1-1 RF11/RS11 DECdisk Interface Block Diagram

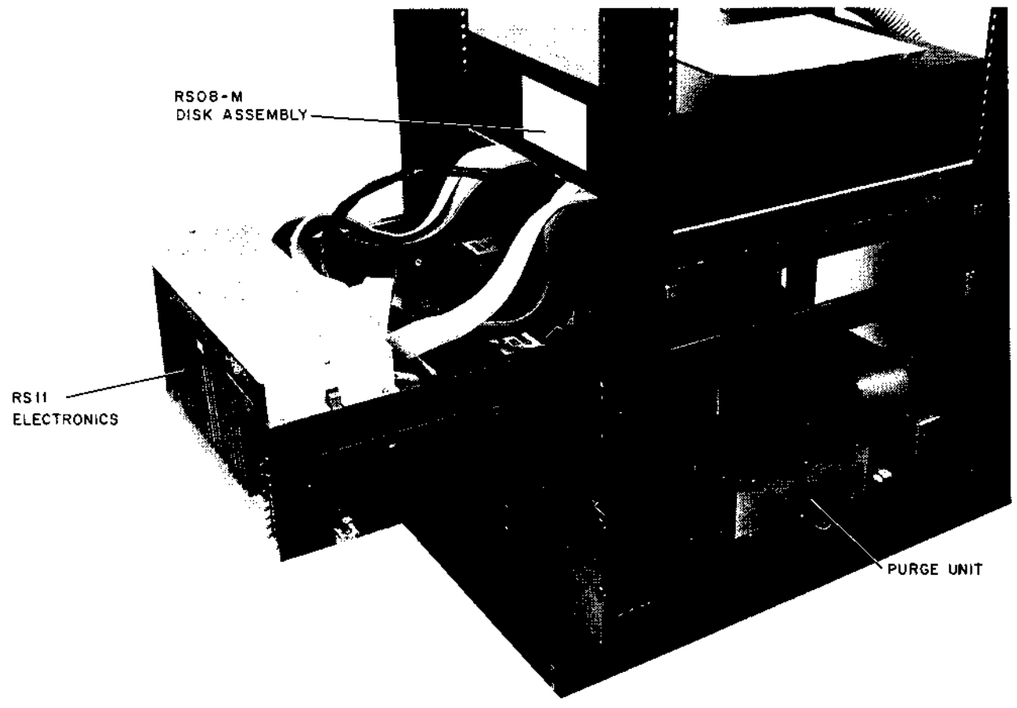



Figure 1-2 RS11 Disk Unit

### 1.2.1 RS11 Disk Unit

The RS11 Disk unit contains a nickel-cobalt-plated disk that is driven by a hysterisis synchronous motor (see Figure 1-2). Data is recorded on a single rotating disk surface by 128 fixed read/write heads. Each read/write head covers a separate track on the nickel-cobalt surface (see Figure 1-3); thus disk action is similar to the operation of many circular tapes running simultaneously in continuous loops. Each track on the disk can store 2048 16-bit words. As a track fills, the system automatically moves to the next track. The disk rotates at 1800 rpm (60-Hz power) and, therefore, can transfer a word every 16 μs. To achieve random access storage, each disk is logically segmented into 2048 slices or words; each slice is preassigned a number or address from 1 to $3777_8$. Therefore, the RF11 Control, in response to the computer, can select, at random, any track of a disk and any address along that track to read or write a word.

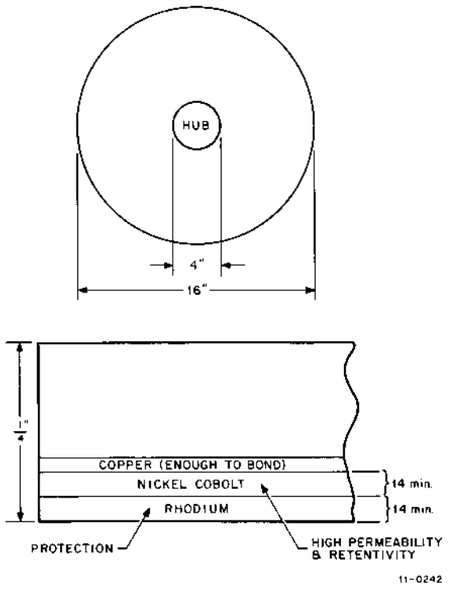



Figure 1-3 RS11 Disk Surface

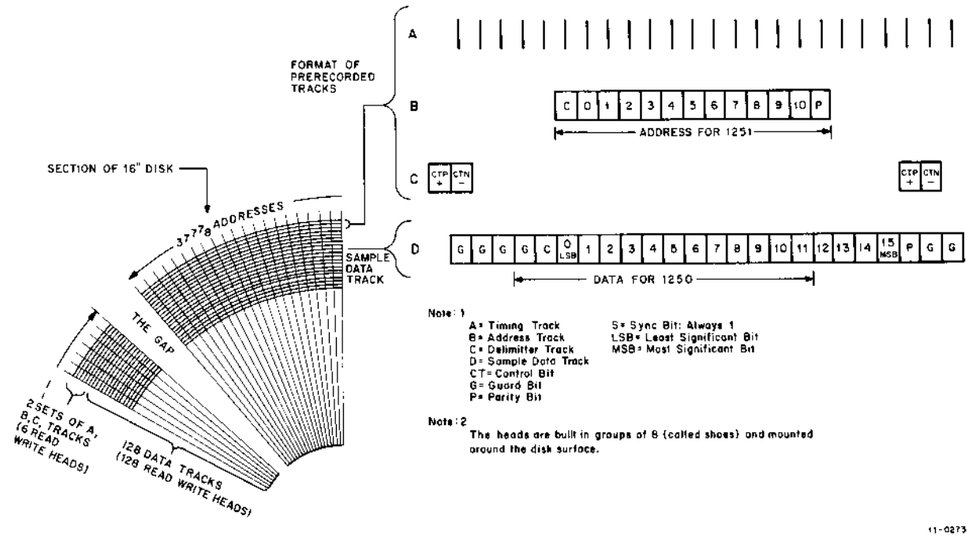



Figure 1-4 RS11 Disk Surface Recording Format

The RS11 Disk surface recording format (see Figure 1-4) consists of 2048 22-bit segments or addresses per track. A 16-bit word is stored in a 22-bit segment. A 2049th segment, called a gap, is provided to give the track selection matrix time to switch tracks. This segment has no address and stores no data or timing; it is used as a marker to notify the RF11 Control after a complete revolution. In addition to storing one 16-bit word, each data segment includes four guard bits, a parity bit, and a sync bit or control bit that operates the self-clocking logic of the RS11 Disk logic for reliable data recovery. The control bit adjusts the timing of the data strobing to ensure proper recovery of each word of data. Each 16-bit word is identified by an address that is prerecorded at the factory on a special track on the disk's surface. This address is recorded serially on the B track, exactly one word before the data word with which it is associated (see Figure 1-4). The word address can then be assembled and identified before the heads reach the word itself. Each address is 13-bits long: 11 bits supply addressing data, one bit is a control bit, and one bit is a parity bit. There are five additional prerecorded tracks on the disk surface. The A track is a prerecorded track that consists of timing pulses 720-ns apart; these pulses are used to develop a strobe to clock data into or out of the data tracks. The C track is used to delimit each word unit. The RF11 Control uses the C track to see when a word has been assembled or written. This enables the RF11 to communicate with the Unibus for data transfer at the proper time. Each of the three prerecorded tracks described – the A, B, and C tracks – are copied on three spare tracks that are used if one of the original tracks is accidentally erased. If the spare tracks are damaged, all the timing tracks can be rewritten in the field with a special timing track writer (see Paragraph 7.3.3.5). The remaining 128 data tracks on the RF11 Disk unit are used for data serially formatted in 22-bit word format.

### 1.2.2 RF11 Control Unit

The RF11 Control unit (see Figure 1-5) serves as the interface between the RS11 disks and the PDP-11 Unibus. Basically, the RF11 performs five functions: error detection, data conversion (serial-to-parallel for a disk Read and parallel-to-serial for a disk Write), Unibus data transfer supervision, disk position monitoring, and system maintenance. The RF11 directly connects to the Unibus and communicates with the processor for status and control information. For data information, the RF11 communicates directly with memory without processor supervision. This is called a non-processor request (NPR) data transfer.

The RF11 contains eight 16-bit hardware registers for communication with the processor and memory. These registers and their respective address assignments are listed in Table 1-1. These device registers initiate all software control of the RF11 and can be read or written into using software instructions that refer to their address. A detailed description of the registers and their bit assignments is presented in Chapter 4. Figure 1-6 shows the functional block diagram of the RF11/RS11 System.

**Table 1-1**
**RF11 Hardware Registers**

| Register | Address |
|---|---|
| Disk Control Status (DCS) | 777460 |
| Word Count (WC) | 777462 |
| Current Memory Address (CMA) | 777464 |
| Disk Address (DAR) | 777466 |
| Disk Address Ext. & Error (DAE) | 777470 |
| Disk Data Buffer (DBR) | 777472 |
| Maintenance (MA) | 777474 |
| Address of Disk Segment (ADS) | 777476 |

The MA register is provided as a maintenance tool.

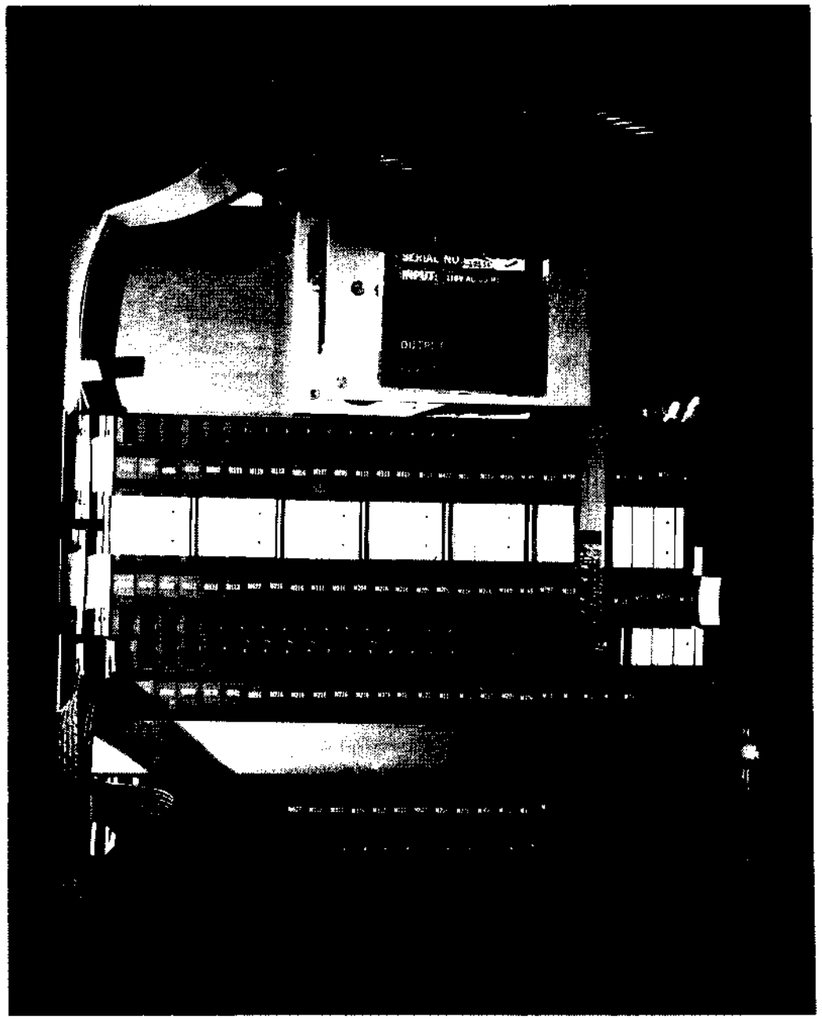


Figure 1-5 RF11 Control Unit

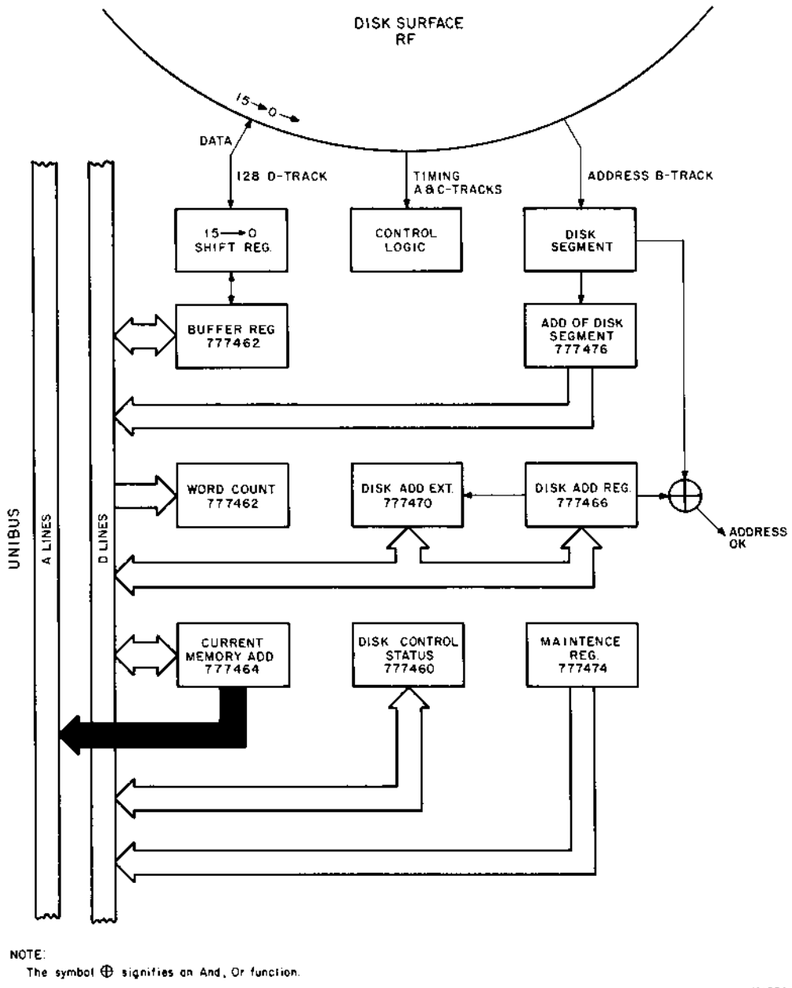



Figure 1-6 RF11/RS11 System, Block Diagram

Through the data transfer control function, the software operating system initializes the RF11 Control by selecting the RS11 Disk to be used, the track address within that disk (Data Track Matrix) to be used, and the first address within the track to be used. Also, it initializes the number of words to be transferred (WC) and the location in core that the transfer is to be made (CMA). One of three operations is then selected: Read the disk; Write on the disk; or Write Check what has already been written. The data conversion function assembles the word off the selected track for a Read operation, or writes the word bit by bit onto the track during a Write operation. When called for by the software system, a Write Check operation compares data in memory with corresponding data on the disk to check for a discrepancy in a Write operation. The data conversion function also notifies the control logic when it needs control of the Unibus (NPR) after it has assembled a word or needs another word to write, and the data is transferred to the Unibus. The system maintenance function simulates either the disk surface head signals or the RS11 output signals and is used exclusively for testing the RF11/RS11 System. Detailed coverage of the maintenance function is found in Chapter 7.

## 1.3 SPECIFICATIONS

The RF11/RS11 System specifications are grouped into six general areas: physical description, environmental limits, logic format, timing format, power requirements, and heat output.

### 1.3.1 Physical Description

RF11/RS11 System housing is provided by a cabinet designed to accommodate one RF11 and up to two RS11s and a power supply. Six additional RS11s can be mounted in two additional cabinets without additional power supplies. Other equipment should not be mounted in the RS11 Disk System cabinets.

Cabinet Dimensions: Height: 71-7/16 in.
Width: 21-11/16 in.
Depth: 30 in.

Shipping Information: Weight of RF11, one RS11, power supply, and cabinet.
590 lbs (crated)
500 lbs (uncrated)
Weight of RF11, two RS11's, power supply, and cabinet.
690 lbs (crated)
600 lbs (uncrated)
(The RF11/RS11 systems are shipped mounted in cabinets.)

### 1.3.2 Environmental Limits

The environmental limits required for proper operation of the RF11/RS11 System are listed below.

Temperature: (Operating) 65° to 90°F

Relative Humidity: (Operating) 20% to 55%

Condensation: (Operating or Storage) None

Vibration/Shock: (Operating) Good isolation is provided. To prevent data errors, extreme vibrations should be avoided while the RS11 is transferring information.

### 1.3.3 Logic Format

The logic format pertaining to data transfer and data storage in the RF11/RS11 System is listed below.

Disks: Eight RS11 Disks may be controlled by one RF11 for 2,097,152 16-bit words.

Tracks: Each RS11 has 128 data tracks and six timing tracks.

Words: Each data track includes 2048 data words.

Word Format: Data words are recorded in 22 bits.

Bits: Each word contains 16 data bits, four guard bits, one parity bit, and one sync bit. The guard bits are always 0 and the sync bit is always 1.

Recording Method: NRZI

Density: Maximum recording density is 1900 bpi.

Words per Disk: 262,144

Control Tracks: Each disk contains three timing tracks plus three spares (spares can be used to recover data on disk). The three tracks are the A track (timing), B track (addressing), and the C track (delimiter or control).

Data Transfer Path: Unibus (When the RF11 is bus master, direct memory access (DMA) is performed.)

Priority Interrupt: The RF11/RS11 has a priority level of BR5 and a interrupt vector address of 204. (However, the priority level is selectable.)



### 1.3.4 Timing Format

The various operation times and timing features of the RF11/RS11 System are listed below.

Data Transfer Rate: (DMA) 16 μs per word (60-Hz power) 19.2 μs per word (50-Hz power)

Access Time: For 60-Hz power:
Minimum Access Time: 258 μs
Average Access Time: 16.9 ms
Maximum Access Time: 33.6 ms
For 50-Hz power:
Minimum Access Time: 258 μs
Average Access Time: 20.3 ms
Maximum Access Time: 40.3 ms

NPR Transfers: Maximum Latency: 12 μs
Maximum Delay: 3 disk revolutions at 1800 rpm

Self-Clocking: The RF11 employs self-clocking keyed by the control bit in a data word on a data track for reliable data recovery.

### 1.3.5 Power Requirements

The power requirements pertaining to the logic and the RS11 motor in the RF11/RS11 system are listed below.

Power Requirements: 115/230 ±10% Vac, single phase, 50 ±2 or 60 ±2 Hz; for a one disk system, starting current of 14A, nominal current of 6.5A; for a eight disk system, starting current of 81A, nominal current of 21A. Power starting currents can be realized if disks are in sequence.

RS11 Motor Power Requirements: Specifications are the same as those for logic power, except additional line current is required. Motor start, 5.5A for 20 ±3 s. Motor run, 4.0A continuous at 115 Vac. (A stepdown autotransformer is provided for 230 Vac operation.)

Line Frequency Stability: Maximum line frequency drift is 0.1 Hz/s. A constant frequency motor-generator set or static ac/ac inverter should be provided for installations with unstable power sources.

Motor Bearing Life: Expected operating life of at least 20,000 hours, under standard computer environment.

Power Supplies: One H726A-2 Power Supply for RF11 logic. One 705B Power Supply for level converters and up to eight RS11 disk logic sets. One 716 power supply for indicator panel.
One 855 Line Filter for disk motors.

### 1.3.6 Power Dissipation

Power dissipation is dependent on the number of disks in the system; it varies from 0.75 kW (2550 btu/hr) for a one disk system to 2.42 kW (8230 btu/hr) for an eight disk system.

## 1.4 RELATED DOCUMENTS

This section provides a list of documents, related to the RF11/RS11 System, that pertain to its use as a peripheral of the PDP-11 Computer.

| Title | Number | Description |
|---|---|---|
| | | **General** |
| *PDP-11 Handbook* | Second Edition, 1970 | Discussion of overall system, addressing modes, and basic instruction set from a programming point of view. Some interface and installation data. |
| *Instruction List* | None | Pocket-size list of instructions. Lists group names, functions, codes, and bit assignments. Includes ASCII codes and the bootstrap loader. |
| *Logic Handbook* | DEC, 1970 | Presents functions and specifications of the M-series logic modules and accessories used in PDP-11 interfacing. Includes other types of logic produced by DEC but not used with the PDP-11. |
| | | **Hardware** |
| *Unibus Interface Manual* | DEC-11-HIAB-D | Used in conjunction with this manual; provides detailed theory, flow, and logic descriptions of Unibus and external device logic. Discusses methods of interface construction and provides examples of typical interfaces. |
| *PDP-11/20 System* | DEC-11-HR1A-D | Introduction, general description, specifications of entire PDP-11/20 system. Also contains operating procedures and controls and indicators for both PDP-11 and Teletype. |
| *KA11 Processor* | DEC-11-HR2A-D | Block diagram discussion, detailed theory of operation related to flow diagrams, instruction set, module descriptions and related logic diagrams, maintenance and adjustments. |
| *MM11-E Core Memory* | DEC-11-HR3A-D | General discussion, detailed theory of operation, bus transactions, adjustments, maintenance aids, and logic drawings. |
| *KL11 Teletype Control* | DEC-11-HR4A-D | Theory of operation, adjustment and calibration, programming data, maintenance aids, and logic drawings. |
| *H720 Power Supply & Mounting Box* | DEC-11-HR5A-D | Power supply block diagram discussion, theory of operation, circuit diagrams.<br>Mounting box description and specifications for all models and cabinets. Includes installation information. |
| *KY11-A Programmer's Console* | DEC-11-HR7A | General description, flow diagram discussion, module description and related logic diagram. Operation and controls & indicators covered in *PDP-11/20 System Manual*. |
| *PDP-11 Conventions* | DEC-11-HR6A-D | a. General Maintenance<br>b. Logic Symbology<br>c. Drawing Set Explanation<br>d. Processor Signals<br>e. Product Identification Codes<br>f. Glossary<br>g. Abbreviations |
| | | **Software** |
| *Paper Tape Software Programming Handbook* | DEC-11-GGPA-D | Detailed discussion of the PDP-11 software system used to load, dump, edit, assemble and debug PDP-11 programs. Also includes discussion of input/output programming and the floating-point and math package. |

# CHAPTER 2
# RF11/RS11 OPERATION

## 2.1 INTRODUCTION

Basic operation of the RF11/RS11 Disk System is accomplished through the PDP-11 software and the RF11 device registers. However, only the operation of the RF11/RS11 is pertinent to this manual.

## 2.2 CONTROLS AND INDICATORS

The RF11/RS11 controls and indicators consist of RS11 controls and RF11 indicators, respectively. The RS11 controls are the WRITE LOCK SWITCHES of the RS11 Disk unit. The RF11 indicators are located on the indicator panel of the master cabinet. The 855 Power Control contains the controls for the system's power supplies.

### 2.2.1 RS11 Controls

Each RS11 Disk unit contains a set of sixteen switches designated WRITE LOCK SWITCHES. These switches are capable of locking out any combination of sixteen 16,384 word blocks (8 tracks) (refer to Table 2-1). Each switch can inhibit the computer from overwriting on eight separate tracks (see Figure 2-1). A write locked-out disk will cause an error flag (WLO) to be set when an attempt is made to write on a locked-out section.

**Table 2-1**
**RS11 Controls**

| Track | | | |
|---|---|---|---|
| Switch | Decimal | Octal | |
| 00 | 0–7 | 0–7 | Matrix 0 |
| 04 | 8–15 | 10–17 | |
| 10 | 16–23 | 20–27 | |
| 14 | 24–31 | 30–37 | |
| 20 | 32–39 | 40–47 | |
| 24 | 40–47 | 50–57 | |
| 30 | 48–55 | 60–67 | |
| 34 | 56–63 | 70–77 | |
| 40 | 64–71 | 100–107 | Matrix I |
| 44 | 72–79 | 110–117 | |
| 50 | 80–87 | 120–127 | |
| 54 | 88–95 | 130–137 | |
| 60 | 96–103 | 140–147 | |
| 64 | 104–111 | 150–157 | |
| 70 | 112–119 | 160–167 | |
| 74 | 120–127 | 170–177 | |

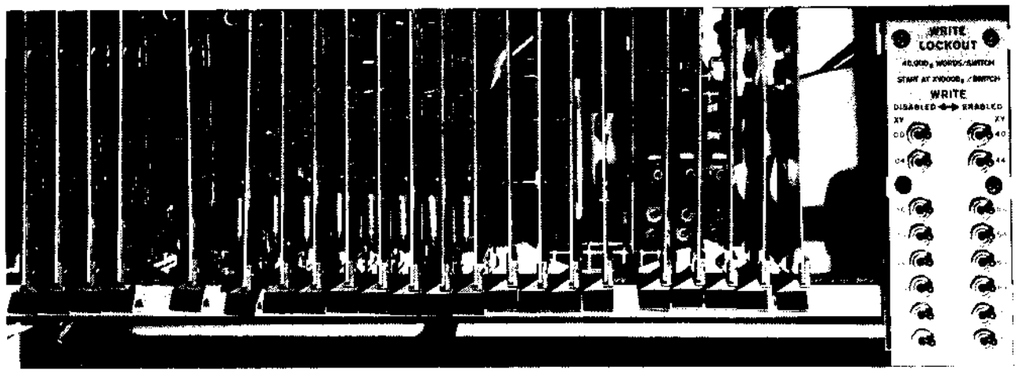



Figure 2-1 Write Lockout Switches

### 2.2.2 RF11 Indicators

The RF11 indicator panel shows the states of most of the register bits, along with some flip-flop states. These indicators are divided into address and error indicators (refer to Table 2-2) and are labeled on the panel (see Figure 2-2) as to the bit and the register, or to what the bit or flip-flop defines.

**Table 2-2**
**RF11 Indicators**

| Indicator | Function |
|---|---|
| **Address Indicators** | |
| Disk Segment | The dynamic shift register that assembles the serial address from the disk. If these indicators are dimly lit, the disk is communicating with the control. |
| Word Address | Displays bits 00 through 10 of the DAR register and indicates the segment on the disk a transfer is to be made to or from. |
| Track Address | Displays bits 11 through 15 of the DAR and bits 00 and 01 of the DAE registers. |

(continued on next page)

Table 2-2 (Cont)
RF11 Indicators

| Indicator | Function |
|---|---|
| | **Address Indicators (Cont)** |
| Disk ADDR | Displays bits 02 through 04 of the DAE register and indicates the disk unit selected. |
| XM | EXtended Memory bits. Indicates A16 and A17 on the Unibus when the control is Bus Master. |
| | **Error Indicators** |
| ERR | ERRor. Indicates that an error exists in the control. If FRZ is not lit, it is a "soft" error. |
| WCE | Write Check Error. Indicates that the control was performing a WRITE CHECK command and the word read from the disk did not compare with the word taken from core. Causes ERR to light. |
| DPE | Data Parity Error. Indicates that the data being read from the disk did not compare with the computed parity. Causes ERR to light. |
| DT | Data Timing Error. Indicates that the data word has missing or extra bits. Causes ERR to light. |
| NED | NonExisting Disk. Causes ERR to light. |
| DOFL | Disk OverFLow. Indicates that the control sequenced into disk $10_8$. |
| SEQ | SEQuence Error. Indicates the control sequenced into a non-existing disk in the system. |
| PSEL | Program SELect Error. Indicates the program selected a non-existing disk. |
| WLO | Write LockOut. Indicates the control tried to write into a write-protected area of the disk. A WLO switch on the RS11 chassis is enabled. Causes ERR to light. |
| MXF | Missed XFer. Indicates the control was unable to perform a transfer for three revolutions of the disk. Caused by the processor halting or ignoring an NPR request, failure of the control to find the disk address, or failure of the control to find data. Causes ERR to light. |
| DRL | Data Request Late. Indicates the control is ready to transfer data and the previous data has not been taken. Does not stop the current function or cause an error. |
| FRZ | FReeZe. Indicates a "hard" error occurred in the control. Causes ERR to light. |
| APE | Address Parity Error. Indicates that the address being read from the disk did not compare with the computed parity. Causes FRZ to light. |

Table 2-2 (Cont)
RF11 Indicators

| Indicator | Function |
|---|---|
| | **Error Indicators (Cont)** |
| MN | Missing Negative or extra positive pulses from the A Timing Track. Causes FRZ to light. |
| MP | Missing Positive or extra negative pulse from the A Timing Track. Causes FRZ to light. |
| BT | B Timing Track error. Indicates that there was an extra or missing pulse from the B Track. Causes FRZ to light. |
| CT | C Timing Track error. Indicates that there was an extra or missing pulse from the C Track. Causes FRZ to light. |
| NEM | NonExisting Memory. Indicates the control put an address on the Unibus for which no Slave Sync returned for 20 $\mu$s. Causes FRZ to light. |
| | **Additional Indicators** |
| FCTN | FunCTioN register. Indicates the functions being performed by the control; for maintenance functions, the disk signals must be simulated by the program. F0 lit indicates a Write. F0 and F1 lit indicates a Write Check. F1 lit indicates a Read. |
| PARITY | |
| ADDR | Indicates the parity of the disk addresses read from the disk surface. |
| DATA | Indicates the parity of the data word being read from the disk surface. |
| FLAG | |
| DISK | Indicates that an error condition exists in the control or that the control is ready to execute a function. If INT ENA is set, the control raises an Interrupt on the BR-5 level. |
| DATA | Indicates that the control is making an NPR request. |
| INT ENA | INTerrupt ENAble. Indicates that the control is conditioned to raise an Interrupt when Disk Flag is asserted. |
| CMA INH | Current Memory Address INHibit. Indicates that the program has selected a one-word transfer location in core. This prevents the CMA register from incrementing by two after each transfer. |
| OFLO | OverFLOw. Indicates that the control has completed a block of transfers and that the Word Count register has gone to 0. |
| WRITE | Indicates that the control is turning on the writers in the RS11. |
| DISK RUN | Indicates that the control is performing a transfer with the disk. |
| RDY | ReaDY. Indicates the control is ready to perform a function. RDY is the complement of the CONT BUSY signal in the control. |

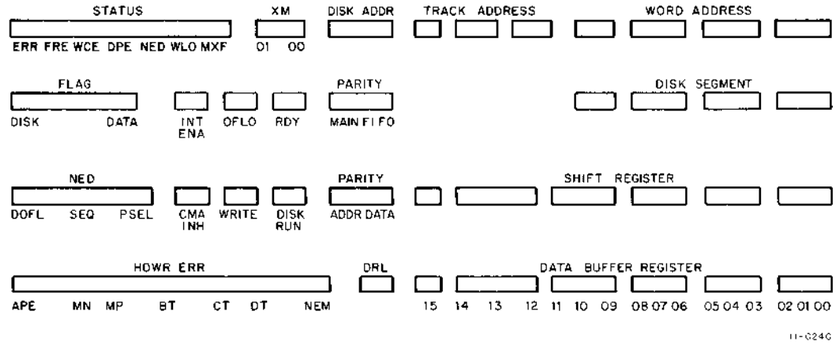



Figure 2-2 RF11 Indicators

### 2.2.3 855 Power Control

The 855 Power Control accepts a 30A power cord at either 115 or 230 Vac, filters the voltage, and delivers the voltage to either a switched or an unswitched output. A circuit breaker at the input controls all power. The switched output can be controlled locally or remotely by setting the LOCAL REMOTE, OFF switch. Both sides of the ac line are switched. Figure 2-3 shows the unit and drawing C-CS-855-0-1 shows its circuit schematic. Descriptions of the power supplies are contained in Chapter 5.

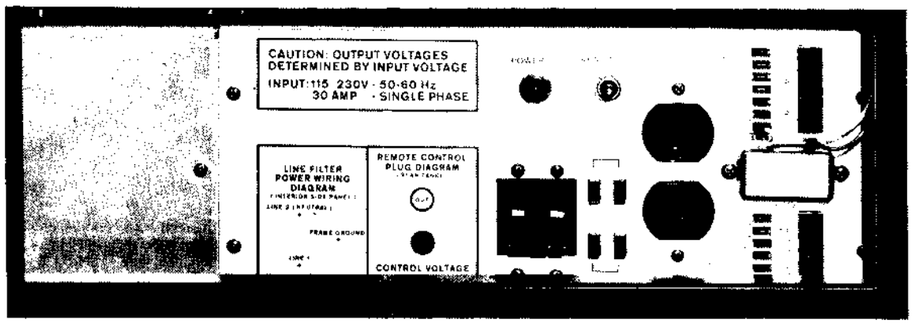



Figure 2-3 855 Power Control

# CHAPTER 3
# PROGRAMMING

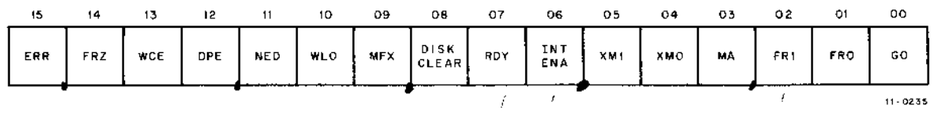
## 3.1 INTRODUCTION

This chapter presents the software interface of the RF11; this includes the device registers and the data format. Finally, programming examples are included to illustrate basic RF11 operation and the functions of the software interface.

## 3.2 DEVICE REGISTERS

All RF11 software control is done with the eight device registers. These registers are assigned memory addresses and can be read or written into (with the exceptions noted) using instructions that refer to the respective register address. The eight device registers and their bit assignments are listed in the following paragraphs. Unassigned and write only bits are always read as 0's. Loading unassigned or read only bits has no affect on the bit. The INIT signal refers to the initialization signal issued by the processor.

### 3.2.1 Disk Control Status Register (DCS – 777460)




| Bit | | Description and Operation |
|---|---|---|
| 15 | ERROR (ERR)<br>Read Only. Interrupts if INT ENA=1 | Logical OR of status bits 09–14 of DCS register. Set if any of the above bits are 1. Cleared if all of the above bits are 0. Causes the control to terminate present function. Will interrupt the program if INT ENA (bit 6 of DCS) is set. Status bits 09–13 indicate recoverable errors ("soft errors"). The program can continue from this condition by setting the GO bit. |
| 14 | FREEZE (FRZ)<br>Read Only. Sets ERROR (Bit 15) | Logical OR of status bits 10 and 12–15 of DAE register. Set if any of the above bits are 1. Cleared when all of the above bits are 0. Causes the control to terminate present function and disables the disk timing within the control. Freezes the control for further evaluation and sets ERROR (DCS bit 15). |
| 13 | WRITE CHECK ERROR (WCE)<br>Read Only. Sets ERROR (Bit 15) | Set when a comparison error exists between the word read from memory and the word read from the disk during WRITE CHECK. Cleared by INIT, DISK CLEAR or GO. The disk address of the word in error is the contents of the DAR (bits 00–10) minus one. The word in error is found in memory location CMA-4 or CMA-2 if the error occurred in the last word transferred. |
| 12 | DATA PARITY ERROR (DPE)<br>Read Only. Sets ERROR (Bit 15) | Set when the data parity does not agree with the computed parity of the data word just read. The control transfers the word containing the parity error and sets the error flag. Cleared by INIT, DISK CLEAR, or GO. The disk address of the word in error is the contents of the DAR (bits 00–10) minus one. The word in error is found in memory location CMA-2. |
| 11 | NONEXISTENT DISK (NED)<br>Read Only. Sets ERROR (Bit 15) | Set when any disk called for or sequenced into does not exist. Cleared by INIT and DISK CLEAR, or if a new disk address is loaded the operation can be continued by setting GO. The address of the nonexisting disk is found in the DAE (bits 02–04). If bit 05 of the DAE is set, disk $10_8$ was sequenced into. |
| 10 | WRITE LOCKOUT (WLO)<br>Read Only. Sets ERROR (Bit 15) | Set when attempting to write into a Write Protected address. Cleared by INIT, DISK CLEAR, or GO. The memory location of the word not written is CMA-2. DAR (bits 00–10) contains the disk address of the word not written. Reading or Write Check in a write protected area is permitted. Protection is provided by each disk, in increments of 16,384 words, via 16 toggle switches on each disk assembly. |
| 09 | MISSED TRANSFER (MXF)<br>Read Only. Sets ERROR (Bit 15) | Set when disk was busy and missed transferring data twice in succession from the same address. (More than one disk revolution occurred without a transfer.) Cleared by INIT, DISK CLEAR, or GO. Indicates failure in control or an overloaded NPR facility. |
| 08 | DISK CLEAR<br>Write Only | This bit initializes (power clear) the disk control when set. |

(continued on next page)

| Bit | | Description and Operation |
|---|---|---|
| 07 | CONTROL READY (RDY)<br>Read Only | Indicates that the control is ready to perform a function. Cleared when the control is executing transfers between the disk and the Unibus. Set by INIT, DISK CLEAR, or when disk function is terminated. |
| 06 | INTERRUPT ENABLE<br>Read/Write | When set, this bit allows the control ready signal (RDY) or error (DCS bit 07 or 15) to interrupt the program. Set by program, cleared by INIT, DISK CLEAR, or the program. |
| 05 | EXTENDED MEMORY 1 (XM 1)<br>Read/Write | MSB of Current Memory Address (extension of the CMA register). Can be loaded by the program. Cleared by INIT or DISK CLEAR. |
| 04 | EXTENDED MEMORY 0 (XM 0)<br>Read/Write | Second MSB of Current Memory Address (extension of the CMA Registers). Can be loaded by the program. Cleared by INIT or DISK CLEAR. |

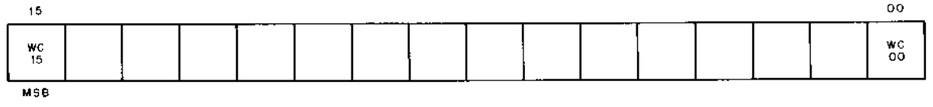
Note: The extended memory bits (DCS bits 4–5) are intended for systems equipped with the KT11-A Option and a memory larger than 32K words, and will cause the Nonexistent Memory bit (DAE bit 10) to get set if sequenced into by the CMA or selected by program, when the system has 32K words or less memory.

| | | |
|---|---|---|
| 03 | MAINTENANCE (MA)<br>Read/Write | When set, this bit indicates that a maintenance function is in process. Loaded by the program. Cleared by INIT, DISK CLEAR, or the program. |
| 01–02 | FUNCTION REGISTER (FR1, FR0)<br>Read/Write | The function register (FR) selects the operation to be performed by the disk control when a GO command is given. (DCS bits 00–1). The function code is described in Table 3-1.<br><br>The FR is loaded by the program and is cleared by INIT or DISK CLEAR. The FR retains the function until altered by the program or cleared, thus enabling the user to continue from a "soft error" condition with a GO command. |
| 00 | GO BIT (GO)<br>Write Only | When set, the GO bit will cause the disk control to carry out the function contained in the FR. The GO bit and the FR can be loaded simultaneously. |

Table 3-1
Function Code

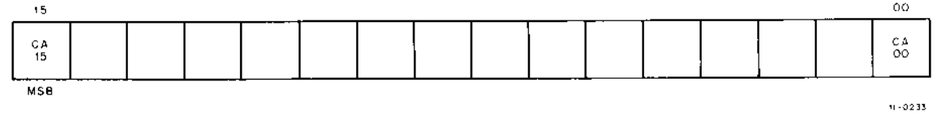
| FR01 | FR00 | Mode | Operation |
|---|---|---|---|
| 0 | 0 | NORMAL | NOP |
| 1 | 0 | NORMAL | READ |
| 0 | 1 | NORMAL | WRITE |
| 1 | 1 | NORMAL | WRITE CHECK |

### 3.2.2 Word Count Register (WC = 777462)



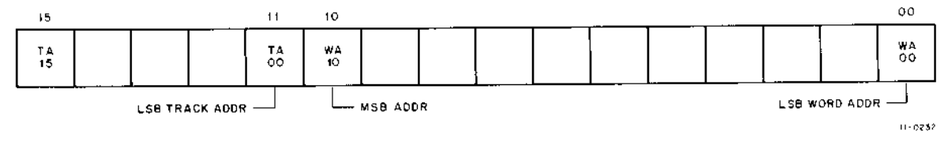

| Bit | | Description and Operation |
|---|---|---|
| 00–15 | WORD COUNT (WC)<br>Read/Write | Counts the number of data transfers to and from the disk. The WC register can be loaded and read from the bus, and shall be loaded with the 2's complement of the number of data transfers desired. The register will be incremented by the disk control before each data transfer. Cleared by INIT or DISK CLEAR. |

### 3.2.3 Current Memory Address Register (CMA = 777464)




| Bit | | Description and Operation |
|---|---|---|
| 00–15 | | Holds the core address of the data to be transferred next. Addressing will only be permitted on word boundaries. Thus CA00 must always be loaded with a 0.<br><br>The register will be set to the starting address. The disk control will increment the register by 2 after each data transfer. The register will carry into the extended memory bits (DCS bits 03–04). Register range: $000000_8$ – $177776_8$. Cleared by INIT or DISK CLEAR. |

### 3.2.4 Disk Address Register (DAR = 777466)



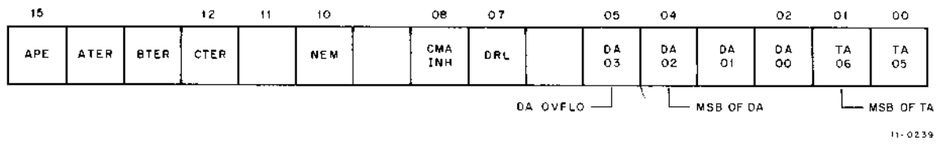

| Bit | | Description and Operation |
|---|---|---|
| 00–10 | WORD ADDRESS (WA)<br>Read/Write | Selects one of 2048 words on a disk track. The word address will carry into the track address, thus allowing spiral read or write. |

(continued on next page)

| Bit | | Description and Operation |
|---|---|---|
| 11–15 | TRACK ADDRESS (TA)<br>Read/Write | Selects one of 128 tracks per disk with bits 00–01 of DAE register. Bit 15 carries into bit 00 of the DAE (Disk Address Ext & Error Register). |

**GENERAL:** The DAR is incremented by the disk control when the disk data is transferred into the Data Buffer Register (DBR) during a Read operation, or when the disk data is transferred from the DBR during Write. The register can be loaded and read from the bus and is cleared by INIT or DISK CLEAR.

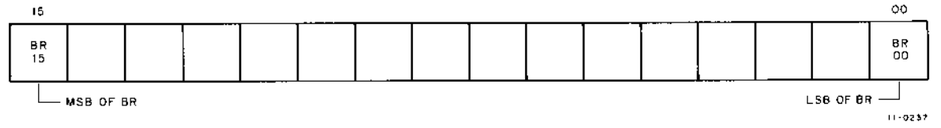
### 3.2.5 Disk Address Ext & Error Register (DAE = 777470)




| Bit | | Description and Operation |
|---|---|---|
| 15 | ADDRESS PARITY ERROR (APE)<br>Read Only. Sets FREEZE (FRZ) – (DCS Bit 14) | This bit is set when the disk control detects an address parity error. Allowed any time the disk is busy. This error will cause a FREEZE (FRZ) condition. Cleared by INIT or DISK CLEAR. |
| 14 | A TIMING TRACK ERROR (ATER)<br>Read Only. Sets FREEZE (FRZ) – (DCS Bit 14) | Detects missing or extra bits from the A Timing Track (clock). Causes a FREEZE (FRZ) condition when set. (See description of FRZ.) Set by the control upon detection of an error, cleared by INIT or DISK CLEAR. |
| 13 | B TIMING TRACK ERROR (BTER)<br>Read Only. Sets FREEZE (FRZ) - (DCS Bit 14) | Detects missing or extra bits from the B Timing Track (ADDR). Causes a FREEZE (FRZ) condition when set. (See description of FRZ.) Set by the control upon detection of an error, cleared by INIT or DISK CLEAR. |
| 12 | C TIMING TRACK ERROR (CTER)<br>Read Only. Sets FREEZE (FRZ) – (DCS Bit 14) | Detects missing or extra bits from the C Timing Track (SECTOR). Causes a FREEZE (FRZ) condition when set. (See description of FRZ.) Set by the control upon detection of an error, cleared by INIT or DISK CLEAR. |
| 11 | | Unused. |
| 10 | NONEXISTENT MEMORY (NEM)<br>Read Only. Sets FREEZE – (DCS Bit 14) | Set when the control fails to receive SSYN after asserting MSYN to the memory (time out after 20 $\mu$s. Cleared by INIT and DISK INIT. CMA contains address of NEM. |
| 09 | | Unused. |
| 08 | CURRENT MEMORY ADDRESS INHIBIT (CMA INH)<br>Read/Write | When set, this bit prevents the Current Memory Address Counter from incrementing. Set by program, cleared by INIT, DISK CLEAR, or the program. |
| 07 | DATA REQUEST LATE<br>Read/Write | This status bit is set when the processor has failed to allow an NPR transfer to be executed when the disk control was ready to transfer data. This status bit is intended as an overload warning and does not set ERROR (DCS bit 15). Cleared by INIT, DISK CLEAR, or the program. |
| 06 | | Unused. |
| 05 | DISK ADDRESS -$10_8$ (DA14)<br>Read/Write | This bit is set if we sequence into disk $10_8$, which does not exist. This will set NED (DCS bit 11) which sets ERROR to signal the program. Cleared by INIT, DISK CLEAR, or when a new disk ADDR is loaded. |
| 04–02 | DISK ADDRESS (DA)<br>Read/Write | Selects one of eight disks that can be controlled from one disk control. The track address (DAE bit 01) carries into the disk address enabling automatic data transfers across disks. |
| 01–00 | TRACK ADDRESS (TA)<br>Read/Write | These are the two most significant bits of the track address. The least significant bits are found in the DAR register (bits 11–15). Together they select one of 128 tracks per disk. |

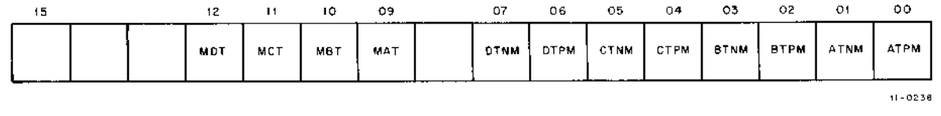
**GENERAL:** The disk address and the track address bits are cleared by INIT or DISK CLEAR.

### 3.2.6 Disk Data Buffer Register (DBR = 777474)




| Bit | | Description and Operation |
|---|---|---|
| 00–15 | BUFFER REGISTER (BR)<br>Read/Write | This register is provided mainly as a maintenance tool and can be loaded and read from the bus. Cleared by INIT and DISK CLEAR. |

### 3.2.7 Maintenance Register (MAR = 777474)




| Bit | | Description and Operation |
|---|---|---|
| 00–01 | A TIMING MAINTENANCE (ATM) Write Only | Simulated A Timing Track disk interface. |

(continued on next page)

| Bit | | Description and Operation |
|---|---|---|
| 02–03 | B TIMING MAINTENANCE (BTM) Write Only | Simulated B Timing Track disk interface. |
| 04–05 | C TIMING MAINTENANCE (CTM) Write Only | Simulated C Timing Track disk interface. |
| 06–07 | DATA TRACK MAINTENANCE (DTM) Write Only | Simulated Data Track disk interface. |

**GENERAL:** The above are simulated disk interface signals within the control. No disk is necessary. The diagnostic program determines the sequence of pulses and the bit rate.

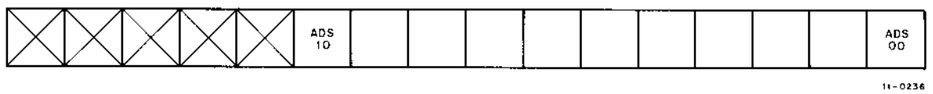
| | | |
|---|---|---|
| 08 | | Unused. |
| 09 | MAINTENANCE A TIMING (MAT) | Simulates the disk head signal to the A Timing read amplifier. |
| 10 | MAINTENANCE B TIMING (MBT) Write Only | Simulates the disk head signal to the B Timing Track read amplifier. |
| 11 | MAINTENANCE C TIMING (MCT) Write Only | Simulates the disk head signal to the C Timing Track read amplifier. |
| 12 | MAINTENANCE DATA (MDT) Write Only | Simulates the disk head signal to the data track read amplifier. |

**GENERAL:** The above signals cause the control to generate analog signals that simulate the disk head signals as received directly from the head. The diagnostic program determines the sequence and the bit rate of the signals. Each transfer is treated as if it was one cell space on the disk.

**NOTE**

**When a maintenance function is performed and the MA (DCS bit 02) is set, the effect of the disk control time outs is inhibited because of the lower bit rates encountered during maintenance.**

### 3.2.8 Address of Disk Segment Register (ADS = 777476)




| Bit | | Description and Operation |
|---|---|---|
| 11–15 | | Unused |
| 00–10 | ADDRESS OF DISK SEGMENT REG (ADS) Read Only | This register allows the user to read the real-time segment address of the disk. The contents of the ADS will indicate the address or the address + 1 of the data passing under the heads. The ADS register will contain the last address of the track while the disk is passing through the gap and buffer region. |

## 3.3 ADDRESSES

Each of the eight 16-bit registers is assigned a memory address. Each register and its respective address is listed on the following page.



| | | |
|---|---|---|
| Disk Control Status Register | address | 777460 |
| Word Count Register | address | 777462 |
| Current Memory Address Register (CMA) | address | 777464 |
| Disk Address Register (DAR) | address | 777466 |
| Disk Address Ext. & Error Register (DAE) | address | 777470 |
| Disk Data Buffer Register (DBR) | address | 777472 |
| Maintenance Register (MA) | address | 777474 |
| Address of Disk Segment Register (ADS) | address | 777476 |

The DBR and the MA registers are provided as maintenance tools.

The interrupt vector address for the RF11 is 0000204 and operates at a priority level of BR5. The priority level is selectable by replacing the priority chip in the G736 module located in slot A04 of the RF11 Control.

## 3.4 DATA FORMAT

The data format in the RF11 is the basic 16-bit word format of the PDP-11 System. In the RS11, the data is still in the 16-bit format; however, 4 guard bits are added along with a control bit and a parity bit. Therefore, the RS11 word length is 22 bits inclusive.

## 3.5 PROGRAMMING EXAMPLES

Program control of the RF11/RS11 Disk is accomplished by loading the disk control registers. The disk performs the specified function and when the function is done or when an error occurs, it will cause an interrupt to the routine whose starting address is in location 204, if the interrupt enable bit (DCS06) is set; otherwise the program may test the word count register and the error bit (DCS15) to determine completion.

A common technique is to use a subroutine to load the registers. The values to be placed in the registers can be assembled following the subroutine call using the .WORD assembler directive. The disk control begins operation when the GO bit in the DCS register is loaded, so a WAIT instruction follows the subroutine call. Note that the WAIT instruction is in the main program, not the register-loading subroutine; this enables the interrupt routine to provide a separate error return for each disk operation.

In the following example, the DISKIO subroutine and the DSKHNDLR interrupt routine are used by the subroutine calls shown to write a 256-word block on disk 0 and then do a write check of the same block.

The subroutine calls and additional codes which are included in the main program are written as follows:

```
          MAINPROG:          .
                             .
                             .
004567                JSR    R5,DISKIO      ;SUBROUTINE CALL
   .                  .WORD  DISK ADDRESS   ;DISK ADDRESS TO WRITE TO
   .                  .WORD  DATA ADDRESS   ;MEMORY ADDRESS TO WRITE FROM
   .                  .WORD  -256           ;WORD COUNT
   .                  .WORD  103            ;WRITE FUNCTION AND INTR ENB
000001                WAIT                 ;PROCESSOR WAITS FOR DISK HERE
004567                JSR    PC,ERROR       ;ERROR RETURN
004567                JSR    R5,DISKIO      ;NON ERROR RETURN IS A NEW CALL
   .                  .WORD  DISK ADDRESS   ;THE ASSEMBLED CODE IS THE
   .                  .WORD  DATA ADDRESS   ;SAME AS THE FIRST CALL
   .                  .WORD  -256           ;EXCEPT FOR THE FUNCTION,
   .                  .WORD  107            ;WHICH IS A WRITE-CHECK
```

(continued on next page)

```
000001                  WAIT                        ;PROCESSOR WAITS HERE
004567                  JSR         PC,ERROR2       ;ERROR RETURN, DIFFERENT ROUTINE
    .                               .
    .                               .
    .                               .
    .                   DISK DCS    177460
    .                   DISK WC     177462
    .                   DISK CMA    177464
    .                   DISK DAR    177466
```

The subroutine is assembled from the following code:

```
052767    DISKIO:   BIS     #400, DISK DCS    ;DISK CLEAR
012567              MOV     (R5)+, DISKDAR    ;LOAD DAR REGISTER
012567              MOV     (R5)+, DISKCMA    ;LOAD CMA REGISTER
012567              MOV     (R5)+, DISKWC     ;LOAD WC REGISTER
012567              MOV     (R5)+, DISKDCS    ;LOAD DCS REGISTER
000205              RTS     R5                ;RETURN TO CALL, LOADING
                                              ;DCS STARTS DISK FUNCTION
```

The interrupt handling routine is assembled from the following code:

```
005767    DSKHNDLR: TST     DISKDCS           ;TEST DCS15 (ERROR)
100067              BPL     NORMAL            ;BYPASS ERROR RETURN IF CLEAR
000002              RTI                       ;ERROR RETURN
062716    NORMAL:   ADD     #4, (SP)          ;MOVE OLD PC PAST ERROR CALL
                    RTI                       ;NORMAL RETURN
```

The interrupt vector for this routine is assembled from the following code:

```
                    .204
                    .WORD   DSKHNDLR          ;ADDRESS OF INTERRUPT ROUTINE
                    .WORD   340               ;INTERRUPT ROUTINE PRIORITY
```

The only change necessary to read the same block from the disk is to replace the statement .WORD 103 in the first subroutine call with the statement .WORD 105 (which sets the function to READ).

# CHAPTER 4
# DETAILED DESCRIPTION

## 4.1 INTRODUCTION

The detailed description of the RF11/RS11 System consists of discussions of all system logic, logic functions, and system operations. This discussion is divided into six functional areas: RS11 Disk Logic, Track Signal Error Detection Logic, RF11 Control Section Logic, System Data Transfer Logic, and Maintenance Logic.

The RS11 Disk Logic discusses the magnetic theory of the disk as to the reading and writing operations of a disk. The track signal generation circuitry and the logic and signals that interface to the RF11, are also described.

The Track Signal Error Detection Logic discusses the RF11 and RS11 logic that tests the respective RS11 track signals for errors. These errors are usually a random pulse or a lost pulse on a track. The significance of these errors is described in relation to system operation.

The RF11 Control Section Logic consists of RF11 initialization, bus receiver and driver logic, output gating, selection logic (register and disk), NPR logic, interrupt logic, function register logic, timing generation logic, self-clocking logic, bit counter, unlock sequence logic, disk addressing logic, current memory address, and word count registers.

The Data Transfer Logic consists of buffer and shift register logic, Write, Read, and Write Check logic, and Data Transfer Error Condition logic.

Maintenance Logic includes the logic used for establishing the maintenance mode operation in the RF11. Also described is how maintenance logic puts RF11 logic in a position where the programmer can generate signal simulations of the RS11.

## 4.2 RS11 DISK LOGIC

The RS11 Disk unit (see Figures 4-1 and 4-2) consists of two assemblies: the RS08-M Disk Assembly, and the RS11 Disk Electronics. These two units are functionally integrated. The discussion will concentrate on four functional areas: Read/Write Heads, Digital Recording Techniques, Read/Write Head Electronics, and RS11 Signal Format.

### 4.2.1 Read/Write Heads

Three basic considerations are involved in designing and constructing a magnetic recording for reproduction. These are:

1. A device that can translate an electrical signal into a magnetic field.
2. A magnetizable medium that conforms to and retains the field.
3. A device that can detect the magnetic field and convert it to a signal that can be identified with the original.

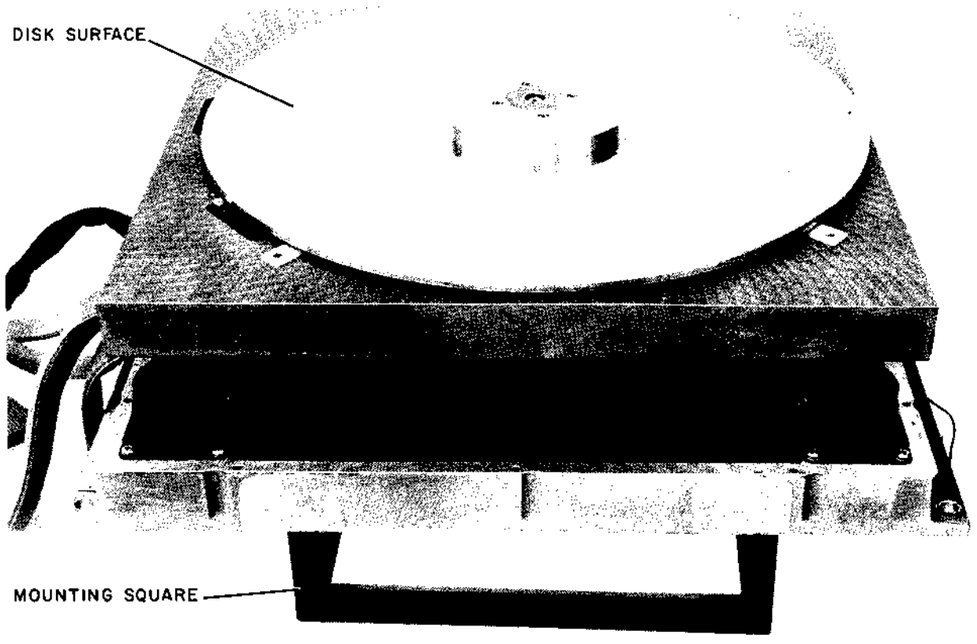



Figure 4-1 Disk Assembly with Cover Removed

These three elements take the physical form of the record head, the disk surface, and the reproduce head. With electronic amplification and a disk drive added to these elements, a basic magnetic disk is formed. In some applications, the record head and reproduce head are combined into one head, the read/write head.

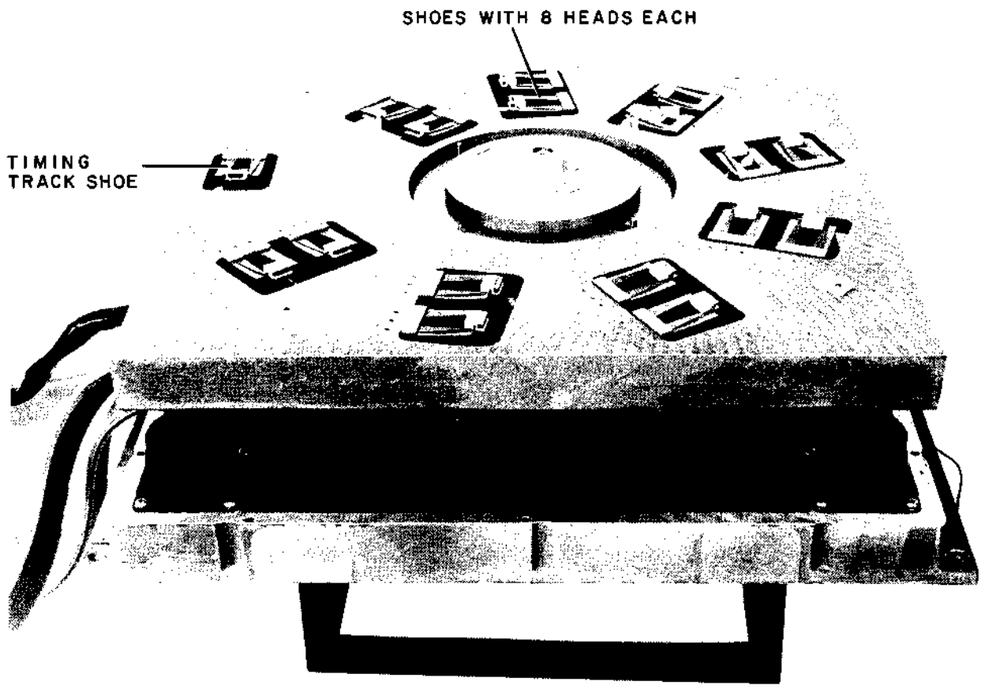



Figure 4-2 Disk Assembly with Cover and Surface Removed

The read/write head can be compared to a transformer with a single winding. When current flows in the winding, the current produces a magnetic flux similar to that in the core of a transformer. The core is made of a closed ring with a nonmagnetic gap. The gap is bridged by the magnetic surface of the disk, and the flux detours around the gap into the disk surface to complete its path. When the disk is moved across the gap, the magnetic material of the disk is subjected to a flux (polarity) that is proportional to the signal current on the head winding. As the disk material leaves the head gap during disk rotation, each particle retains the state of the magnetization that was last imposed on it by the protruding flux. Thus, the actual recording takes place at the trailing edge of the gap. Figure 4-3 illustrates this process.

To reproduce this signal, the magnetic pattern on the disk surface is moved across the head; the magnetic gap detours the magnetic flux through the core itself. The flux lines are proportional to the magnetic gradient of the magnetized surface, and the induced voltage of the head winding follows the law of electromagnetic induction: $e = \frac{Nd\Phi}{dt}$ . Thus, the output is the differential of the input. The waveforms recorded on the disk surface are determined by the method of recording used. There are two basic recording schemes used in digital systems, return to zero (RZ) and nonreturn to zero (NRZ). In general, both methods operate by saturating the magnetic coding in one of two directions.

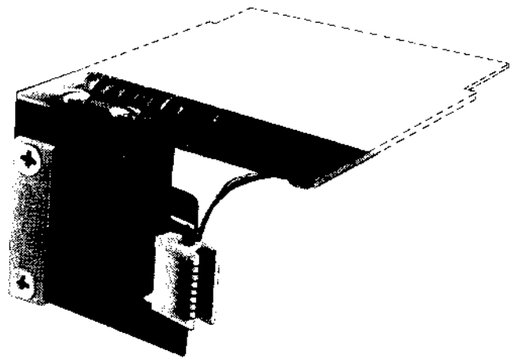


Figure 4-3 (a) RS11 Head Assembly

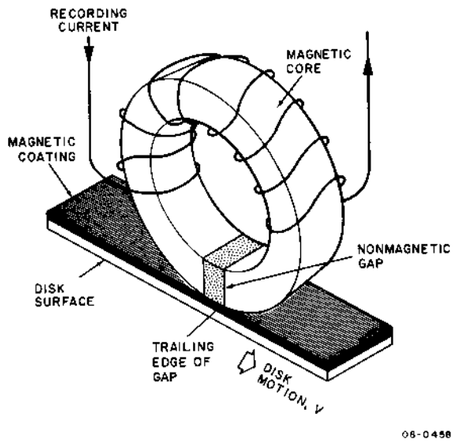



Figure 4-3 (b) Simplified Diagram of the Magnetic Recording Process

### 4.2.2 Digital Recording Techniques

The two basic methods of recording digital data on a magnetic disk are RZ to NRZ. The names refer to the nature of the head current, which in the first case stabilizes at zero when a bit is not being written; in the second case, the head current stabilizes at either a positive or a negative head current between bits. There are several different ways of recording binary digits with these two methods. One technique in RZ recording recognizes one state of saturation as a binary 1, and the other state as a 0; the 0 state represents nothing. The RS11, which uses NRZ, has no fixed state of magnetization assigned to either digit; rather, the state of magnetization is reversed every time a binary 1 is recorded, but left where it is if a binary 0 is recorded. The NRZ method is more efficient than the RZ method in that more data is recorded with fewer flux reversals. However, the RZ technique provides for a self-clocking format. Figure 4-4 illustrates differences in the head current waveform of the two methods.

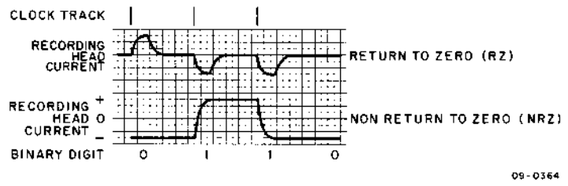



Figure 4-4 NRZ and RZ Recording Formats

The fact that the RS11 NRZ does not present a self-clocking format (some form of reference clock must be present to determine where the zeros fall) suggests that a clock must also be recorded along with the data. A clock track called the A track is recorded on one channel of the disk and is used as a timing reference to read and to write digits. Two more tracks, B and C, are also recorded to identify individual data words on the disk so that they can be retrieved.

### 4.2.3 The Read/Write Head Electronics

In the RS11, data is stored serially on 128 tracks around the disk surface (refer to Chapter 1). Only one of these tracks is engaged in reading or writing at any one time, although 128 heads are continually riding over each disk. At the same time, the A, B, and C tracks are continually being read and used to clock data either onto or out of the particular data track being used. This data track is selected by the RF11 through a matrix selection system. Once selected, a particular head either reads or writes according to the operation selected in the RF11. Since all of the heads in the matrix are identical, only one has been selected to illustrate the Read/Write operation. Figure 4-5 shows the Read/Write Head electronics. (The characteristics of the RS11 modules are described in Chapter 5.)

The data bit to be recorded is clocked by the A time clock into the G290 Writer flip-flop, which drives the electronics of the head. The coil L represents the head winding, which is the center leg of a simple bridge consisting of resistors R1 and R2; diodes D1 and D2; and the switching transistors T1 and T2. When the control reads or writes from this head, it does so by selecting the appropriate G286 Center Tap Selector and the corresponding G285 Series Switch. This combination applies +20V to node A, switches on transistors T1 and T2, and forward biases diodes D1 and D2. Current (approximately 5 mA) flows into the G085 Read Amplifier to -15V. If the G290 Writer has not been selected, this condition leaves the bridge balanced and no current flows through the coil. This is the case during a Read operation; the changing magnetic field from the disk surface induces a voltage into the coil that is seen across the input of the G085 Reader, subsequently amplified, and sliced to appear at OUT (see Figure 4-6). The polarity of the voltage across the coil, which is a function of the direction of flux change induced into the head, determines the relative polarity of the + and - OUT signal.

During a Write operation, the same voltages are applied by the G285 and G286 modules, but the bridge is unbalanced by a -15V level applied to the emitter of either T1 or T2 by the G290. This forces approximately 45 mA through the head coil in one of two directions, depending on which transistor sees the -15V. The transistor selected is a function of the G290 Writer flip-flop.

When a 1 is to be written, the G290 writer flip-flop is complemented by the clock; the -15V is switched from one transistor to the other; the current changes direction; and the resultant change in magnetic flux produces the field that is recorded on the disk surface. Note that current is always flowing in the coil; the current never returns to zero (NRZ). Because the three timing tracks are always selected, the G286 is replaced with the +20V centertap from the G085, and the diodes feed directly into the read amplifier's input.

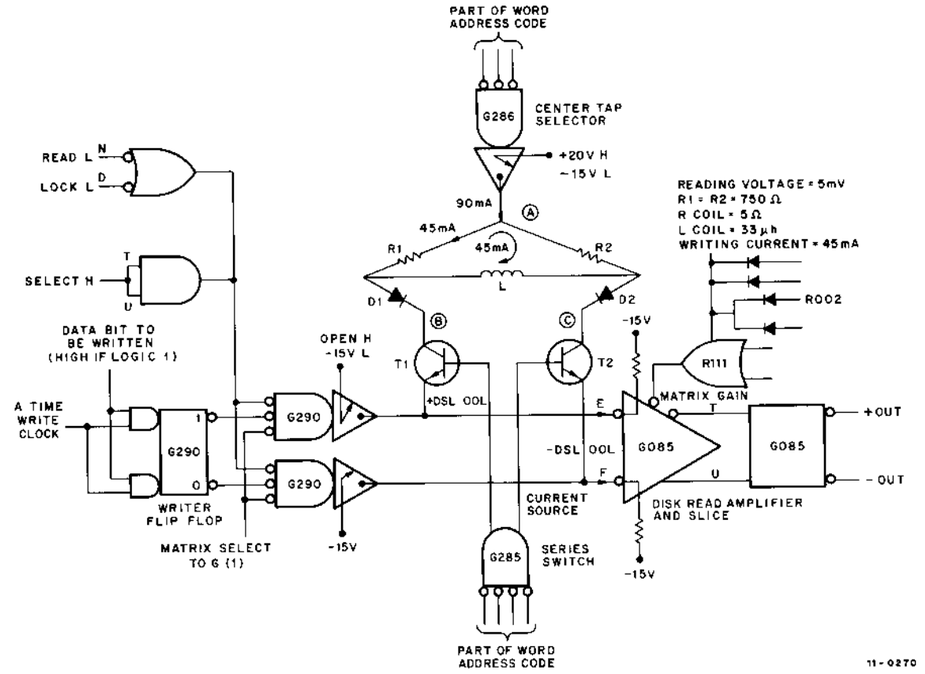



Figure 4-5 RS11 Read/Write Electronics

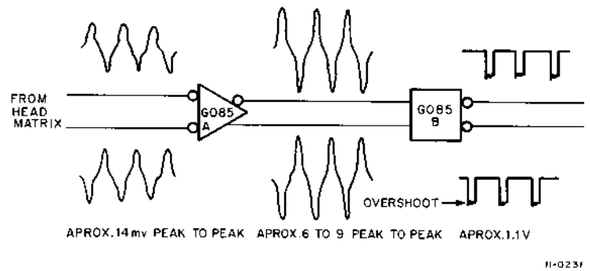



Figure 4-6 G085 Slicing Rectifier

Figure 4-7 shows some of the waveforms that occur in the read/write head circuitry. The read voltage, a bell shaped pulse, peaks approximately 400 ns after the CLOCK pulse. This voltage is amplified and sliced to appear either at +OUT or -OUT, depending on the voltage polarity. Note that the NRZ format used by this system always produces alternate pulses at +OUT and -OUT. A positive pulse cannot be followed by another positive pulse, nor a negative pulse by another negative pulse. This characteristic is utilized to detect errors in the A, B, C, and data tracks.

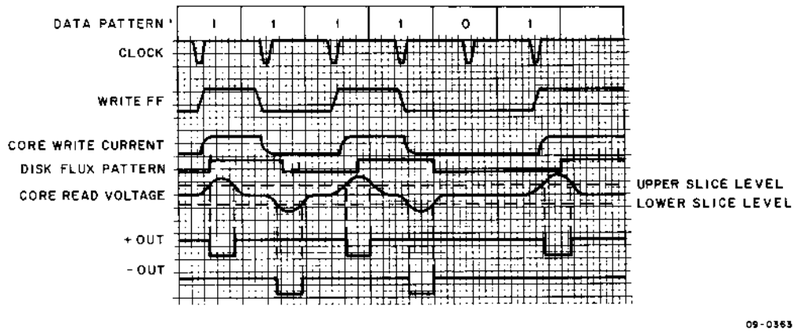



Figure 4-7 Read/Write Electronics Waveforms

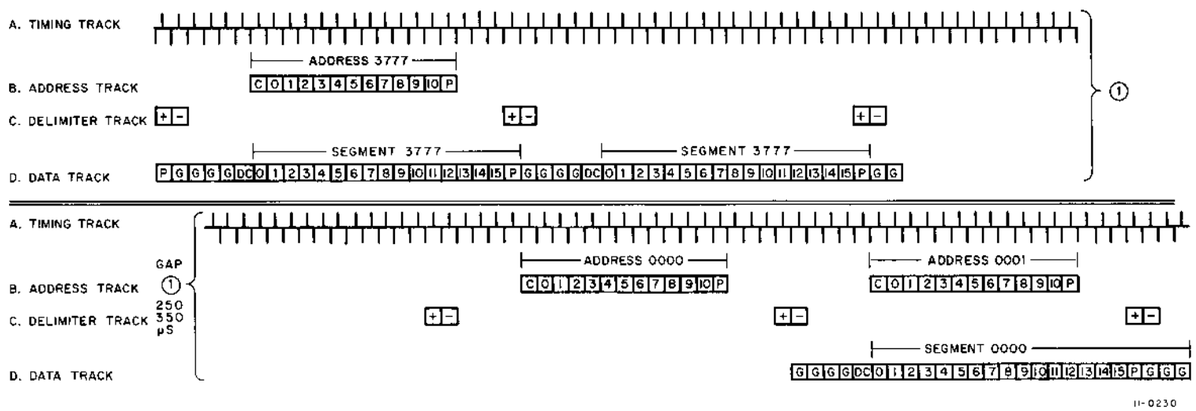



Figure 4-8 RS11 Disk Format

### 4.2.4 The RS11 Signal Format

The selection of specific areas on the disk to write into or read out of is accomplished on the disk by dividing the circumference of the disk into 2048 segments ($3777_8$) in such a way that each segment of any track records a complete word. One track (the B track) is then assigned to record the address of each segment; this track is made available to the RF11, which assembles and identifies these segments. Another track (the C track) is needed to delineate the segment, since the length of the address is less than that of the words. Each of the three prerecorded tracks (the A, B, and C tracks) are duplicated on three more tracks, to be used if the first set is destroyed in the field. If this occurs, the Field Engineer reverses the position of one end of the timing track head cable to activate the spare tracks.

Thus, the disk surface is actually divided into 134 tracks by 134 read/write heads, each riding slightly above the disk and covering a narrow circular ribbon of the disk surface. The heads are mounted in groups of eight on a unit called a shoe. The data shoes are set on cards, which are then inserted into slots under the disk surface. The slots are spread around the circumference of the disk (see Figure 4-2). The shoe that contains the six prerecorded A, B, and C tracks is mounted alone on a card (see Figure 4-2).

The relative positions of all the timing and data tracks are shown in Figure 4-8. The gap shown is a breather space for the RS11 at the point where it switches to the next head and track. The timing pulses stop at the gap, but after the data and addressing tracks, because there is a buffer zone on either side of the gap where no data or addresses are recorded (see Figure 4-9).

It is important to note that:

1. The address refers not to the segment in which it is but to the following segment. This allows the controller time to assemble and identify the address before the actual data area appears under the data heads.
2. The first bit of each address, the control bit, is always a binary 1. The first two bits of each data word, guard bits, are always a binary 0.
3. Each address and data bit calculate a parity bit, which they deposit at the end of the word. Parity ensures that an even number of ones is in each word.
4. The address always starts at bit 1 of the data word in its segment. The C track pulses are recorded at bits P and the next G data word.

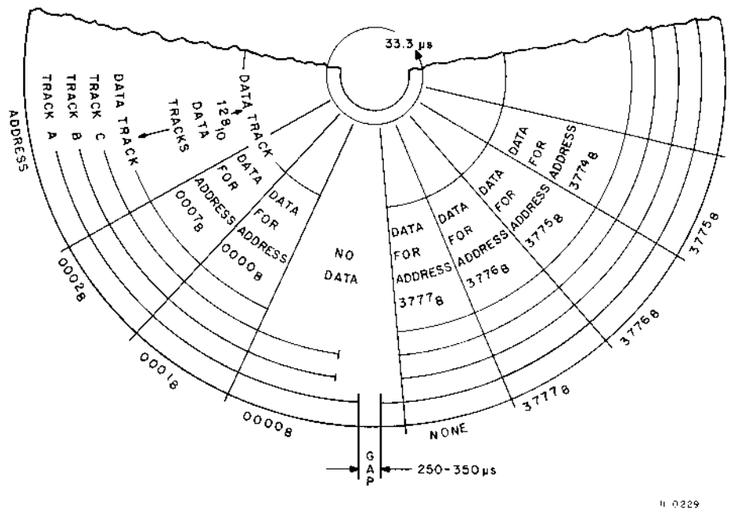



Figure 4-9 RS11 Track Layout

The preceding observations are particularly important when the disk is to be preformatted; that is, when the A, B, and C tracks are to be prerecorded onto the disk surface at the factory (this function is performed by the Timing Track Writer, which is explained in Paragraph 7.3.3.5).

## 4.3 TRACK SIGNAL ERROR DETECTION LOGIC

The Error Detection logic is part of the RF11 logic. It detects errors in the signals from the RS11 on the A, B, C, and data tracks. These error detection logic circuits are explained in the following paragraphs.

### 4.3.1 Error Detection Logic for the A Timing Track

The A track contains the main clock pulse for each disk in the RF11/RS11 System. A pulse train with a period of 1.44 μs is recorded. On playback, both negative and positive transitions are detected by the read electronics. The receiver (G085) slices each transition at a predetermined level; the two pulses are combined to form a pulse train with a period of 720 ns.

Engineering drawing D-BS-RF11-0-10 shows the logic used by the RF11 to detect either a dropout or extraneous pulse on the A timing track.

The positive- and negative-sliced outputs from the A timing track of the RS11 head electronics appear in the error logic as ATTP H and ATTN H, respectively. Each of these signals drives a M602 Pulse Amplifier, which converts the 600-ns ATTN and ATTP pulses to 110-ns pulses. This, in turn, drives M302 Delays set for 1.2 μs. These delays feedback to the respective M602s that enabled them; for the period they are set, these delays inhibit any noise from passing into the system. During this time, there should be no other pulses except noise spikes in the logic. The two delays are then logically ORed together to produce the signal ATOK (A timing track OK). ATOK releases registers in the RF11, and a start up sequence begins. Whenever the gap is reached, or an A track pulse is dropped, ATOK is removed and the RF11 is essentially turned off. (The A track timing diagram is shown in Figure 4-10.)

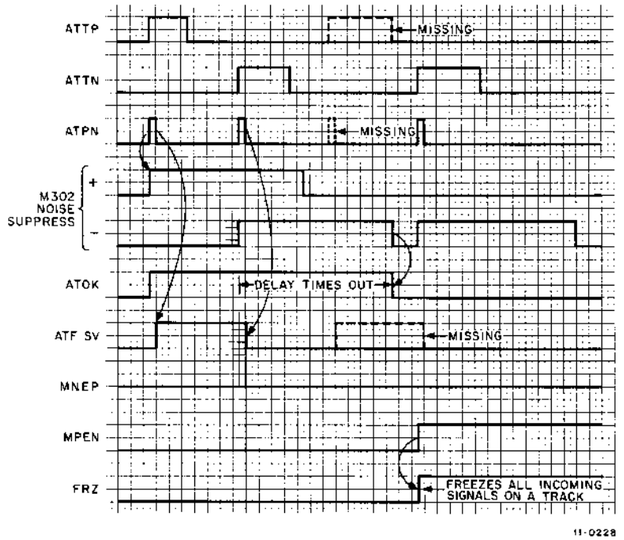



Figure 4-10 A Track Error Detection, Timing Diagram

The outputs of the two M602s are also logically ORed; the resultant pulse train is called ATPN H. This pulse train is the main timing signal for the RF11 which, together with the original M602 outputs, is fed into three flip-flops. If the circuit sees a negative pulse, immediately after a negative pulse, this logic sets the MPEN flip-flop. The error could have been caused by a dropped positive pulse or an extraneous, added negative pulse. If the circuit sees a positive pulse, immediately following a positive pulse, the MNEP flip-flop is set. The setting of either of these flip-flops causes the generation (due to an OR function between them) of the signal ATER H in the DAE logic (see engineering drawing D-BS-RF11-0-13). ATER H causes FRZ (freeze bit) to set in the DCS, which, in turn, sets ERR (error bit). When FRZ is set, it inhibits any additional sliced inputs from entering the RF11. Figure 4-10 shows the error case for two negative pulses.

### 4.3.2 Error Detection Logic for the B and C Tracks

The address of each disk segment is stored on the B track. Since this is not a predictable clock pulse, it is not possible to inhibit the time between signals. However, the preceding explanation of the A track applies with respect to positive and negative outputs; that is, a positive pulse cannot be followed immediately by another positive pulse, and a negative pulse cannot be followed by another negative pulse. Furthermore, the B track is strobed into its register by a narrow A track pulse at the optimum time, and is, therefore, extremely reliable.

The delimiters or word boundries for each disk segment are stored on the C track. The theory of error detection for the C track is the same as the B track. The following paragraph discusses error detection logic for the B and C tracks, respectively. The B and C track error detection logic is shown on engineering drawing D-BS-RF11-0-13, sheet 2. Figure 4-11 shows the B and C track time for two positive pulses in sequence.

The JK flip-flop BTF (B track fail) is inputted by the B track pulses BTP (B track positive) and BTN (B track negative) and toggled by the optimum time A track signal ATPN. Under correct conditions, the BTF flip-flop changes state with each ATPN toggle, as BTP and BTN should always alternate. However, if an extraneous pulse or a pulse

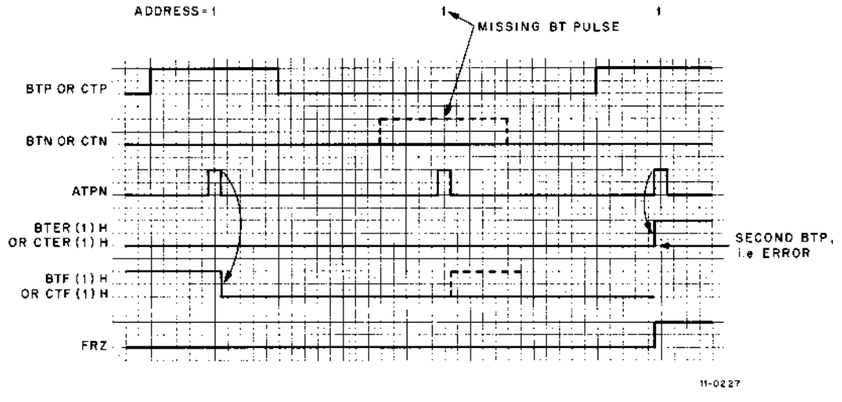



Figure 4-11 B and C Track Error Detection, Timing Diagram

dropout occurs on the B track, either two BTP or two BTN will input sequentially. When this happens, the BTF flip-flop does not change state and the second BTP or BTN pulse in sequence qualifies the M121 gate which asserts the condition to the BTER (B track error) flip-flop. BTER is clocked by ATPN if the disk is performing a function (DISK RUN is set); in turn, when BTER is set it sets FRZ in the DCS, which inhibits further ATPN signals and stops all action. If DISK RUN is not set, BTER does not set; therefore, no errors are detected.

C track error detection logic is identical to that of B track. In this case, CTP and CTN are the alternating C track pulses to be checked, and either two positive pulses in sequence or two negative pulses in sequence will set the C track error flip-flop CTER, which is clocked the same as BTER. Likewise, setting CTER causes FRZ to set in the DCS and stops all action. The B track parity error logic is discussed in Paragraph 4.4.12.

### 4.3.3 Error Detection Logic for the Data Tracks

The delay inhibit circuits for A track error detection cannot be used to check the data track. However, if two identical pulses are detected sequentially, a data track error is detected. The PDT and NDT flip-flops follow the data track input pulses and store them, a procedure that is necessary to compensate for skew between the data heads and the timing track heads. This skew does not occur among the A, B, and C tracks because the heads are all mounted on the same shoe; that is, they are mechanically interconnected. The following paragraph describes the data track error detection logic, which is shown in Figure 4-12, as well as engineering drawing D-BS-RF11-0-13, sheet 2.

STROBE is the ATPN pulse delayed; SBM is a pulse generated by the C track. STROBE defines the data track bit cell and SBM delimits the word boundary of the data track word. These two signals are ORed to clear PDT and NDT when high and clock DTE ENA when low. The PDT flip-flop is clocked by the data track positive pulses (DTP) and enabled during the time the bit counter (see engineering drawing D-BS-RF11-0-19) has not overflowed (BC05 (1) is low). The NDT flip-flop is clocked by the negative data track pulses and enabled by FOUND (1), which is asserted when PDT is set (indicating the control has found the sync bit). When combined, the DTE ENA flip-flop and M113 gating are essentially a JK flip-flop toggled by the OR of STROBE and SBM and inputted by PDT and NDT. SBM clears DTE ENA when a word is ready to come through. DTE ENA sets and resets for each alternating positive and negative data track pulse. Two positive or negative pulses in sequence will inhibit a DTE ENA change of state and qualify the M121 gate. This output, along with the shift register having been read or loaded (RD LD), asserts an input to the DTE flip-flop. DTE is clocked at the same time the shift register is clocked

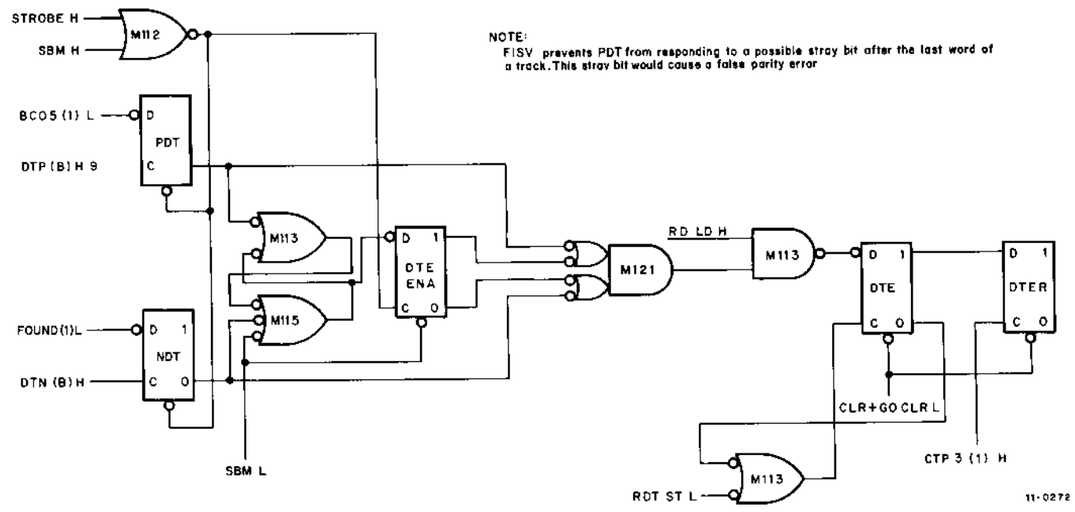



Figure 4-12 Data Track Error Detection Logic

during the Read operation. The DTE flip-flop sets DTER at CTP 3 time. DTER (data track error) sets FRZ in the DCS and all action stops. The data track timing for the error condition of two sequential negative pulses is shown in Figure 4-13.

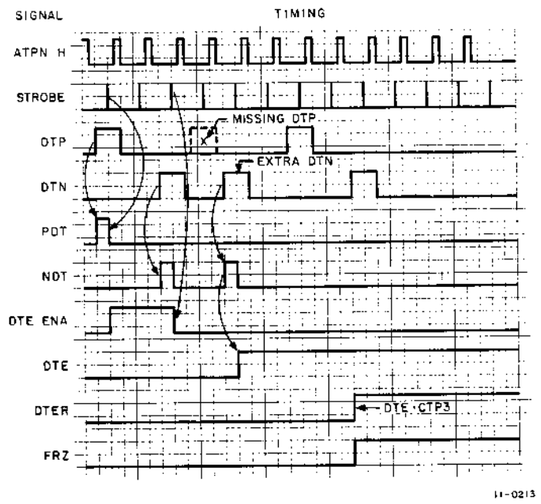



Figure 4-13 Data Track Timing Diagram

## 4.4 THE CONTROL SECTION LOGIC

The following paragraphs describe the various RF11 control functions that establish the primary functions performed by the RF11/RS11 System.

### 4.4.1 Initialization

RF11 initialization is accomplished by clearing all the registers before a data transfer. This operation is keyed by the BUS INIT signal off the Unibus which is inverted to the INIT signal. INIT is used to generate CLEAR, which initializes the RF11 Control logic independently (see engineering drawing D-BS-RF11-0-12). CLEAR is generated by gating either INIT or DCS IN HI, and D08 IN (DISK CLEAR). The signal GO CLR permits the RF11 to continue operation after a software error without re-initializing the RF11 Control registers. GO CLR is generated when the GO bit in the DCS is set.

### 4.4.2 Unibus Receivers and Drivers

The Unibus receivers and drivers are the gating circuits that send and receive bus information. The receivers gate all data lines, address lines, and control signals into the RF11. Also, the receivers invert signals so they are logically compatible with RF11 logic circuitry. The bus drivers invert and apply the RF11 execute device slave sync, and address gating signals to the bus.

### 4.4.3 Output Gating

The output gating gates all the register bits to the bus data lines. This output gating network is a NAND matrix to the bus driver network and puts DCS, DAE, DAR, and DBR information on the data lines. The WC and CMA registers are gated through the drivers to the Unibus. Their gating circuitry is included on the WC and CMA module.

### 4.4.4 Selection Logic

The RF11/RS11 System selection logic determines the registers addressed by the processor. This selection is accomplished by the M105 and the M797 module logic shown on engineering drawing D-BS-RF11-0-07. The M105 performs address selection; the M797 performs register selection. Also included is the disk selection logic shown on engineering drawing D-BS-RF11-0-17.

The M105 Address Selector module decodes address information from the Unibus. In the RF11, the M105 is arranged, due to the GND 08 connection, to recognize all address lines except A01, A02, and A04. Address line A00, which is the least significant digit of the address, is recognized by M105 to determine a byte or word operation. The exclusion of address lines A01, A02, and A03 in the M105 allows the logic to generate the signal DEV SEL D (device select) for eight addresses. This arrangement is due to the fact that the M105 can select only four registers, while the RF11 contains eight registers. Address lines A01, A02, and A03 represent the least significant octal bit of the register address whose value is recognized in the register selection logic discussed in the following paragraph. The jumpers on the M105 determine the eight possible addresses that will enable the DEV SEL D. The jumpers are set in the RF11 to recognize addresses 777460 through 777476. Although these addresses have been selected by DEC as the standard assignments for the RF11 registers, the customer can change the jumpers to any addresses desired. Finally, the M105 gates the BUS C01 and BUS C02 signals to generate IN and OUT signals, which determine whether a register is reading or writing.

The M797 Register Selection module determines which registers have been selected by the processor and whether these registers are reading or writing. The input signal DEV SEL D Lo from the M105 module is present when a valid address up to the least significant octal digit, has been recognized by the M105 with MSYNC. The input OUT gate with DEV SEL D to initiate the decoders for the generation of register IN and OUT signals for writing or reading these registers, respectively. The A01, A02, and A03 address line signals come off the bus receivers and determine which of the eight registers are selected. The least significant octal digit of the address is always even and the decoder then generates the register IN or OUT signals for the respective register addressed. Finally, STRT XTIM is generated by M797 when a valid address has been received through the decoder and will initiate the I/O strobe timing.

The disk selection logic is located on the G740 module. Up to eight disks can be selected on the G740 individually. This selection is achieved by inputting the disk address portion of the DAE register called for by the RF11 Control. The jumpers on the G740 are connected so as to account for or enable any of the disks in the particular RF11 controlled system. According to the number of disks used, the G740 then generates the appropriate SEL DSK (select disk) signals A to a possible J from 00 to a possible 07, respectively. These SEL DSK outputs (A through J0 are hard wired to disks 0 through 7, respectively, and the G740 allows any logical unit to be designated to them.

### 4.4.5 NPR (Non-Processor Request) Logic

The NPR operation occurs when the RF11/RS11 System wants to communicate and perform a data transfer with memory. In order to perform this operation, the RF11 must obtain control of the Unibus and become bus master. The following discussion illustrates the RF11 becoming bus master and initiating NPR data transfer. Refer to engineering drawing D-BS-RF11-0-03 (sheets 1 and 2) for the NPR logic. The timing diagram for the NPR operation is shown in Figure 4-14.

When the RF11 desires to perform a data transfer either to or from a RS11 disk, the DATA RQ flip-flop is set. The DATA RQ flip-flop is set when data is strobed out of the shift register to the buffer register during a Read or Write Check (SR0 (1)), when the first data word is to be written as indicated by WB FULL (0), F0SV (1), and GO;

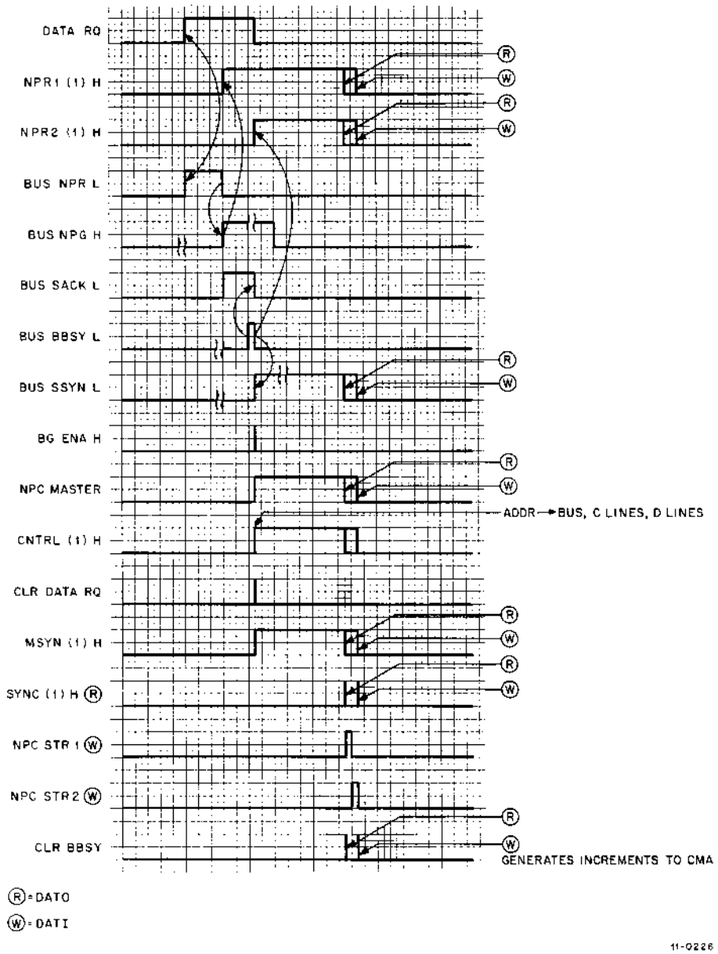



Figure 4-14 NPR Logic, Timing Diagram

or when the control is ready for the next word to be written, as indicated by data being strobed from the buffer register to the shift register without a word count (WC) overflow. Therefore, completing an RF11 data transfer operation will set DATA RQ and initiate an NPR.

Setting the DATA RQ flip-flop generates the BUS NPR signal, which requests NPR control of the bus from the processor. If the RF11/RS11 priority is such that the unit can be next bus master, the processor replies with NPG (non-processor grant) IN. NPG IN sets the NPR1 flip-flop which, in turn, generates BUS SACK to the processor. At this point, the RF11 is set up to be the next bus master and must now wait for the present bus operation to terminate. When BUS BBSY and BUS SSYN are removed from the bus as the previous operation terminates, the RF11 generates BG ENA (see D-BS-RF11-0-04) which, in the absence of BUS NPG, sets the NPR2 flip-flop. The RF11 drops BUS SACK and now asserts BUS BBSY on the bus and generates NPC MASTER. NPC MASTER sets the CONT flip-flop which gates the data (if Read Only) and address lines to the bus and enables the bus control lines. CONT generates CLR DATA RQ which clears the DATA RQ flip-flop and asserts BUS MSYN. When SSYN IN returns, the data has been transferred. This causes the SYNC flip-flop to set which, in turn, drops BUS MSYN and clears CONT. Clearing CONT generates CLR BBSY which drops BBSY from the bus, clears NPR1 and NPR2, and generates CMA CLK which increments CMA.

The foregoing description applies to Read, Write, and Write Check operations. However, the following describes what also occurs for a Write or Write Check operation. For either of these operations, SSYN IN generates NPC STR 1 for 200 ns. Upon completion of NPR STR 1, this signal is inputted to generate NPC STR 2 for 250 ns. These strobing signals are used in a Write or Write Check operation to strobe data into the DBR.

In an RF11 operation, if the SSYN IN signal does not occur 20 μs after MSYNC is asserted, then NEM (non-existent memory) sets in the DAE, indicating that a non-existent memory location was addressed in core. In turn, FRZ is set in the DCS. Setting NEM also sets the SYNC flip-flop in the NPR logic for termination of bus communication.

### 4.4.6 Interrupt Logic

The RF11 Control initiates an interrupt to the processor in either of two cases: the ERROR bit is set in the DCS, or the RDY (ready) bit in the DCS is set, indicating the end of a block transfer (WC goes to zero). However, INT ENA (1) (interrupt enable) must be set in the DCS for the interrupt to be initiated. Engineering drawing D-BS-RF11-0-04 shows the interrupt logic of the M782 Module. The interrupt condition is initiated by DISK FLAG, which reflects either of the conditions described above for an interrupt. This signal, along with INT ENA, will generate BR OUT (bus request) when the BR1 and BR2 flip-flops are cleared. The bus reply of BG IN (bus grant) sets BR1 which generates BUS SACK on the bus. When the bus drops SSYN and BUS BBSY, BG ENA (bus grant enable) is generated and BR2 is set. This condition generates BUS BBSY to the bus; INTR MASTER gates the interrupt vector address to the bus data lines, and BUS INTR initiates the processor's interrupt service routine. When BUS SSYNC returns, INTR CLR is asserted which relinquishes control of the bus and clears the BR flip-flops.

### 4.4.7 Function Register Logic

The function register consists of bits 01 and 02 of the DCS, and defines the type of operation performed by the RF11. The function register logic consists of the DCS function register flip-flops, F0 and F1, and two save flip-flops. These two save flip-flops, F0SV and F1SV, are loaded by the processor through the software. (Refer to engineering drawing D-BS-RF11-0-12, sheet 1, for the function register logic.) When the system is ready to perform the operation specified by software (see Paragraph 3.2 for function register coding), the GO bit is set in the DCS, which loads the software-initiated function from the save flip-flops into the respective function register flip-flops. The RF11 now acts on the function register order. If an error occurs during an operation, the function register flip-flops are cleared by ERR and the operation stops until the error situation is handled. However, even though the function register has been cleared, the function is saved in the save flip-flops, F0SV and F1SV. When the operator has handled the error and wants to resume operation, the GO bit is set in the DCS. Setting the GO bit clocks the contents of the save flip-flops into their respective function register flip-flops and RF11 operation is resumed. When the correct number of data transfers between the RF11 and the Unibus are completed (according to the WC register), F0 and F1 are cleared by WC CARRY OUT. WC CARRY OUT is generated by the WC overflow after the last transfer specified is completed.

### 4.4.8 Timing Generation Logic

The logic shown in Figure 4-15 generates the RF11 timing pulses from the A and C track signals received by their heads on the timing shoe. The A track pulses are fed through the G085 Amplifier where they are split into positive

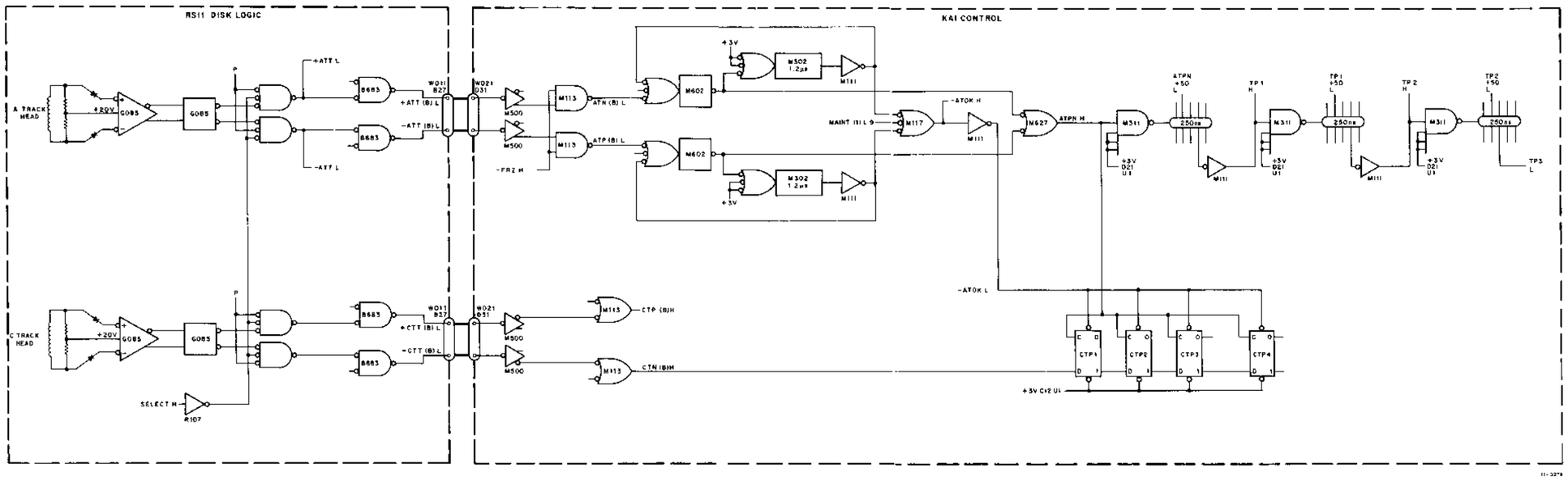



Figure 4-15 Timing Generator

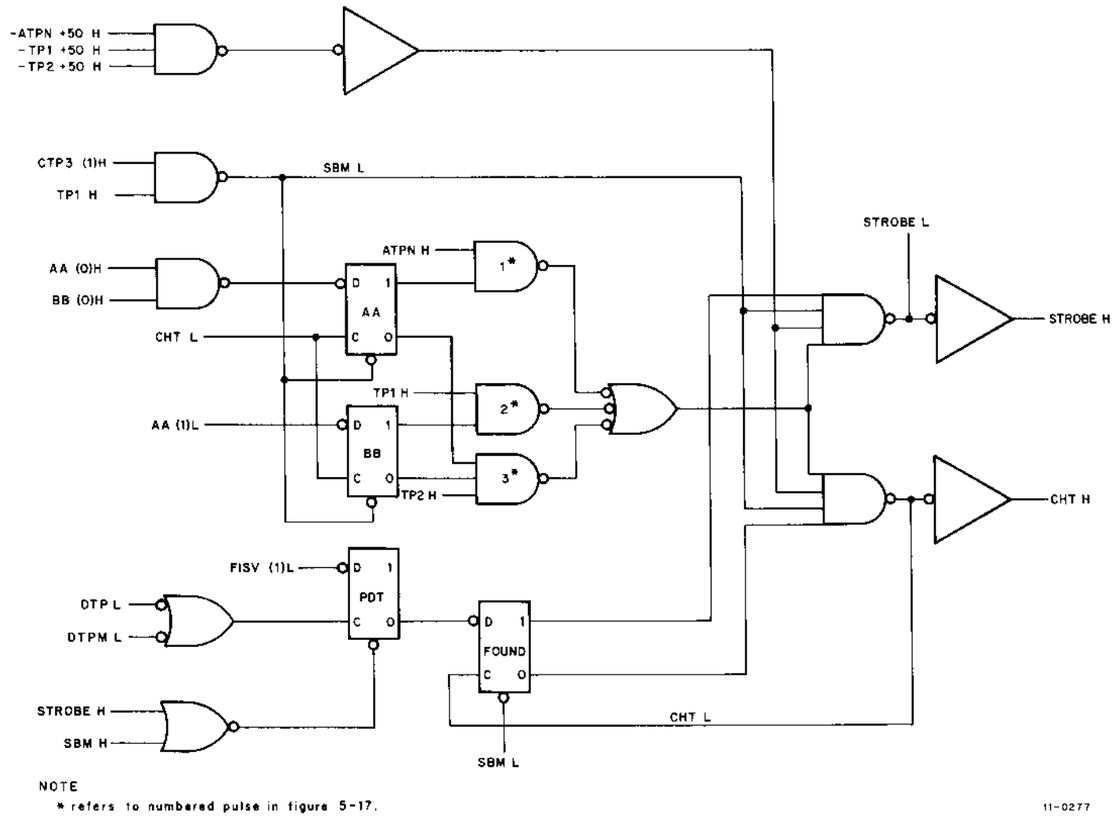



Figure 4-16 Self-Clocking Logic

and negative pulses that are 720-ns apart. The G085 passes the pulses on to the RF11 (as described in Paragraph 4.3.1) which generates the pulse train ATPN. ATPN feeds two fixed 225-ns delays and one fixed 200-ns delay, which generate timing pulses TP1, TP2, and TP3, respectively. These timing pulses are used throughout the RF11 (refer to engineering drawing D-BS-RF11-0-19).

The C track signals enter the RF11 by circuitry similar to that of the A track signals. Upon entering the RF11, the negative CTN signal is inputted to a 4-bit shift register, CTP1 through CTP4. This register detects the CTN pulse by strobing it with ATPN into CTP1. Each successive ATPN pulse shifts CTN through this shift register to CTP4. Each of the CTP flip-flops are used to supply signals according to their states that will initiate sequences of operations between data words. (Refer to engineering drawing D-BS-RF11-0-11, sheet 1, for CTP shift register logic.) The CTP2 and CTP3 flip-flops are used to generate the word boundary signals, WBM and SBM, in the RF11. (Refer to engineering drawing D-BS-RF11-0-19 for WBM and SBM signal generation logic.) SBM is generated by gating CTP3 with TP1; WBM is generated by gating CTP2 with TP2. These signals are used in the RF11 logic to define or delimit the word boundaries of data words.

### 4.4.9 Self-Clocking Logic

While a disk is rotating at normal speed, each head is moving microinches above the surface. However, when the disk is stopped and restarted, the heads touch the surface and friction forces each shoe to shift from its original position. This shifting can cause problems because all bits written on tracks covered by any shoe are written with reference to the timing track. Therefore, if a data shoe shifts with respect to the timing shoe, or vice versa, all data on the tracks covered by that shoe will shift also, and may possibly not be in the correct position to read. Furthermore, if a word is written onto this shifted track, it may not fall into the proper segment and, therefore, could interfere with the data bits of adjacent words. To compensate for these problems, two features are provided in the RF11: self-clocking to locate data bits that have possibly shifted, and tracking of guard bits between data words to prevent interference by adjacent word operations.

Figure 4-16 shows the self-clocking logic in the RF11 and Figure 4-17 shows the timing. The modulo three counter AA and BB successively gates each of the three timing pulses, ATPN, TP1, and TP2, to generate its own clocking pulse, CHT. The three counter remembers each CHT pulse that clocks as it counts its three states. Meanwhile, the PDT flip-flop examines the data track. Each word is always preceded by a control pulse or sync bit that is always a 1 and a positive pulse (DTP). As soon as the PDT flip-flop detects the control pulse and sets, CHT clocks the FOUND flip-flop with PDT set. As FOUND sets, it immediately stops the three counter and channels subsequent timing pulses to generate STROBE after each data bit, instead of CHT. The pulse that is now allowed to pass becomes the strobe timing for the subsequent word. STROBE, in turn, generates the SR CLK signal that loads the data into the shift register. Loading data into the shift register produces optimum timing of the data track, because the control pulse is fixed with respect to the data bits. Therefore, it is valid for all data bits in the word. When the next word appears, the self-clocking again adjusts itself to the optimum from the control pulse for correct operation in the word.

Each word is buffered on both ends with two guard bits. Therefore, there are four guard bits between adjacent words. If a data head moves, it can theoretically move by two bit positions either way and not interfere with an adjacent word. (In practice, the movement is restricted to 1-1/2 bits). Therefore, a word could be written into a complete segment after the head has shifted without interfering with existing data on adjacent segments of the same track.

### 4.4.10 Bit Counter

When a word is being either Read or Write Checked, once the control bit has passed the RS11 heads, the RF11 must count the number of data bits that pass through the shift register. This is done to ensure that the entire

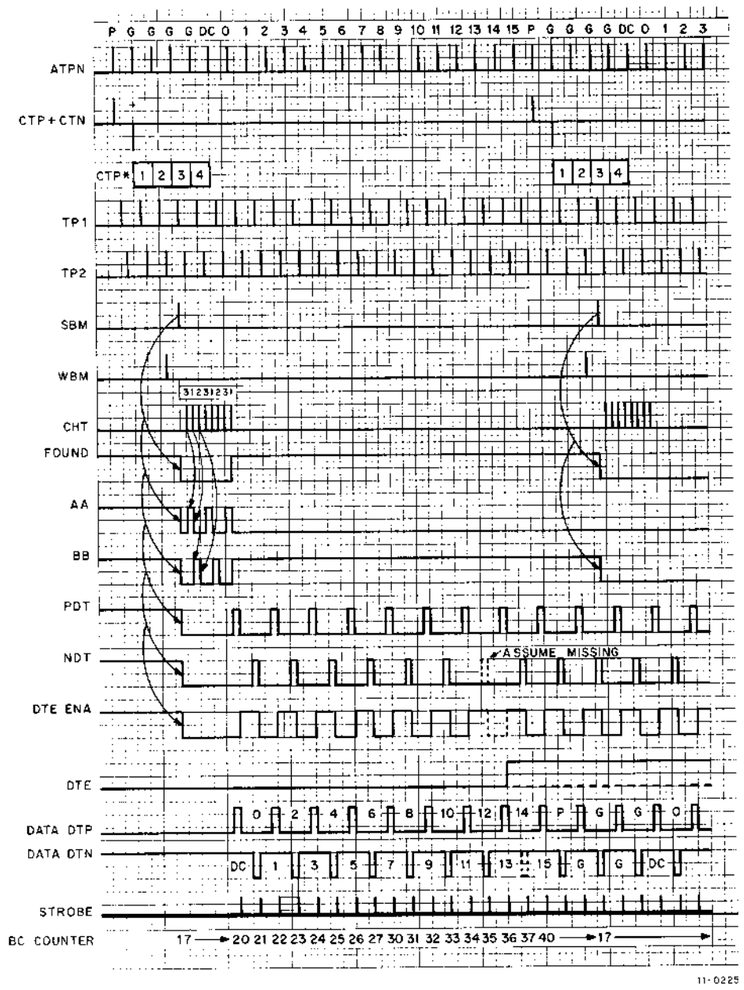



Figure 4-17 Self-Clocking Logic, Timing Diagram

word will be read or write checked and is accomplished by the bit counter (refer to engineering drawing D-BS-RF11-0-19). The bit counter is initialized by the signal CHT L to a count of $17_8$ or $15_{10}$ and overflows on a count of $40_8$ or $32_{10}$, giving a total of $21_8$ or $17_{10}$ bits. Therefore, at the last data bit of each word, BC05 sets and holds. The value of the bit counter is used in the read and write check logic explained in Paragraph 4.5.

### 4.4.11 Unlock Sequence Logic

Figure 4-18 illustrates the use of ATOK and the C track. The first time the CTP4 flip-flop is set after ATOK is asserted, and when a valid operation is specified in the function register, the DISK RUN flip-flop is set. The DISK RUN flip-flop is used to notify the RF11 Control that it is busy performing transfers to the disk. When DISK RUN

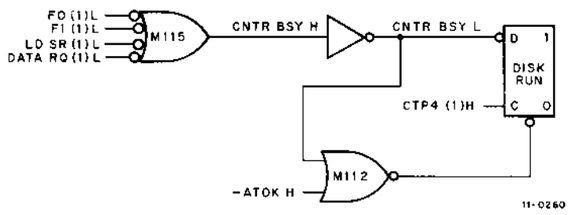



Figure 4-18 Unlock Sequence Logic

is set, RF11 logic is assured that the C track signal is valid and that the A track timing is correct (at least three valid ATPN pulses). These conditions initiate B track address decoding (see Paragraph 4.4.12) which locates the disk address called for by the program. DISK RUN resets when ATOK drops, which occurs during the gap or when an A track pulse is lost (A timing track error); or when the function register is cleared and CTP4 appears. When errors occur, DISK RUN is reset and disk operation stops.

### 4.4.12 Disk Addressing Logic

The disk addressing logic determines when the disk address, called for by the program, is reached on the disk by comparing the disk address register (word address section) and the non-addressable disk segment register. This comparison is achieved by equal comparison gating. When the disk segment register has assembled the address, it is transferred to the ADS register for program availability.

The disk segment register assembles the word address off the B track of the disk that is to be involved in a data transfer. (Refer to engineering drawing D-BS-RF11-0-15 for disk segment register logic.) The word address is clocked into the segment register by ATPN. Also, the ATPN signal toggles the APAR JK flip-flop, which checks the B track address parity. APAR is toggled each bit time. However, the first bit that comes off the B track is CTL, which causes the first toggle with ATPN and sets APAR for the first time. The next B track bit is the first address bit. When this address bit is 1, it causes APAR to change state with a toggle. If the B track bit coming through is 0, no change in state occurs when APAR is toggled by ATPN. The last bit of the address to toggle through APAR is the B track parity (P) bit. This parity bit is either 1 or 0, depending if the number of 1 bits in the address was odd or even, respectively. If the track address read is valid, then the APAR flip-flop will always complete the toggling through of an address in the same state which is zero. If, when the address has been toggled through, APAR is at 1, a parity error has occurred and APE is set in the DAE which causes a FRZ error condition. If APAR is set, CPT3, which generates DAW EN, will clock APE on the DAE to set. APAR is cleared when CTP4 is generated for the next incoming address. (The CTL flip-flop logic is used to enable clocking of the address bits through the segment register). When the initial CTL bit reaches the DS00 flip-flop on the next ATPN pulse, the CTL flip-flop is set and the address bits are completely in the segment register. Also, any further clocking of the segment register is disabled by setting CTL. In preparation for the next word to be transferred, CTP4 will clear CTL as well as the disk segment register and clocking of the register resumes. At this time, the disk word address is available for comparison with the DAR word address section. (Refer to engineering drawing D-BS-RF11-0-30 for the disk addressing logic timing.)

The disk address register consists of a track address and a word address (see engineering drawing D-BS-RF11-0-14, sheets 1 and 2). The track address portion is extended into the DAE (engineering drawing D-BS-RF11-0-13, sheet 1) which contains the track address portion's two most significant bits. For the track address portion, track address incrementing occurs when the last word of a track is reached. Incrementing is done during the gap when DISK RUN clears. The DAE also contains the disk address bits which are loaded and incremented in the same way as the track address bits, except that incrementing occurs when each disk fills. Incrementing the track address is initiated by setting the INC TA flip-flop, when WA10 (the most significant bit of the word address) changes from 1 to 0 (indicating that a transfer has occurred to the last word of a track). When the disk reaches the gap (after the last word has been read or written), INC TA is cleared when DR DLY (DISK RUN Delayed) appears, and the track address portion of the DAR is incremented. For the track address bits in the DAE, TA05 is incremented by INC DAE when TA04 overflows. Similarly, the INC DA in the DAE is set when the track address portion in the DAE overflows at the beginning of the gap and the disk address portion of the DAE is incremented. When DISK RUN sets, INC DA is cleared. The word address portion of the DAR is incremented every time a word is written or read, as indicated by flip-flops SR1 and SR0, respectively, to generate INC WA. These flip-flops or flags are covered in the read and write descriptions in Paragraph 5.5. The upper half of the DAR is incremented by the INC DAR flip-flop when WA07 overflows from 1 to 0. The purpose of this flip-flop is to prevent WA08 from settling when the low-order byte of the DAR register is loaded.

Equal comparison gating is illustrated in Figure 4-19, is a simple block diagram of the gating function between the disk segment register and the word address portion of the disk address register. (Refer to engineering drawing D-BS-RF11-0-16 for the detailed logic of comparison gating.) The two registers are compared in parallel by a series of exclusive OR gates. If they compare favorably, without a parity error on the B address track to invalidate the comparison, and if the RF11 is performing a function (DISK RUN is set), then ADR OK H (address OK) informs the RF11 logic that the next word coming under the read/write heads is the point to which the transfer is to be made.

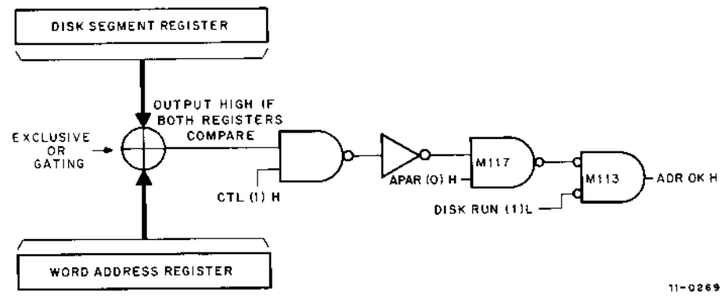



Figure 4-19 Equal Comparison Gating

The ADS (address of the disk segment register) is the addressable register that contains the address located in the segment register each time an address is assembled. Once an address is assembled in the segment register, it is transferred to the ADS where it is available to the programmer. (Refer to engineering drawing D-BS-RF11-0-24 for the ADS logic.) This is accomplished when the CTL flip-flop of the disk segment logic is set at the termination of an address assembly, and the program is not reading the ADS (ADS to BUS asserted). UPD ADS is clocked at this time by ATPN pulses which, in turn, clock the disk segment register contents into the ADS. ADS to BUS is generated by the register selection signal ADS OUT that appears whenever the ADS is addressed.

### 4.4.13 Current Memory Address Register Logic

The current memory address register (CMA) is loaded with an address that specifies the memory location to or from which data is transferred. The register is incremented by two after each bus transfer; thus, the register continually points to sequential memory locations. (Refer to engineering drawing D-BS-RF11-0-08 for the CMA logic.) The CMA is loaded with the initial address in memory from the bus data lines. This address is strobed into the register

by CMA IN, generated in the register selection logic, and I/O STR 2 generated by STRT XTIM in the register selection logic. CMA CLK increments CMA by two; CMA CLK is generated by CLR BBSY in the NPR logic. Every time the RF11 performs an NPR data transfer it issues CLR BBSY. Each address that appears in the CMA is available to the bus data lines and address lines for program use by directly addressing the CMA.

Two bits in the DCS (EX0 and EX1) provide two added (most significant) bits to the CMA. These added bits provide an increase in memory locations that can be addressed in the CMA. EX0 is clocked by CMA CARRY OUT which is generated when the CMA overflows. This overflow enables the extended CMA bits to increment due to bus transfers. These two bits (EX0 and EX1) are also loaded by the bus data lines (see engineering drawing D-BS-RF11-0-12, sheet 1). The CMA INH flip-flop in the DAE (see engineering drawing D-BS-RF11-0-13, sheet 2) is used to inhibit incrementing CMA. CMA INH is loaded by the program off the bus data lines and is clocked by DAE IN HI and I/O STR 2. Setting CMA INH will disable the generation of CMA CLK and, thus, prevent incrementing of the CMA.

#### 4.4.14 Word Count Register Logic

The word count register (WC) performs a bus transfer count operation. Initially, the register is loaded with the 2's complement of the number of words to be transferred to or from memory in the particular RF11 operation to be performed. Whenever SRO or SRI is generated, indicating a data transfer, the WC is incremented. If the new WC value is 0 (indicated by a register overflow), further transfers are inhibited and the data block transfer of the RF11 is complete. (Refer to engineering drawing D-BS-RF11-0-09.) The WC is loaded through the data lines of the bus. The new WC value is strobed into the register by WC IN from the register selection logic and by I/O STR 2 generated by STRT TIM in the register selection logic. A word transfer to or from the disk generates the signal INC WA, which increments the WC as well as the word address portion of the DAR. IN WA is generated by SRO or SRI, which means that a word is ready to be read or written, respectively. This means that a disk transfer is occurring and the WC is incremented for the next word transfer. When the 2's complement value of the WC overflows the register (register word count goes to 0), the signal WC CARRY OUT is generated. This signal clears the function register of the DCS and sets the OVFLO flip-flop (see engineering drawing D-BS-RF11-0-11, sheet 2) which stops further data transfers.

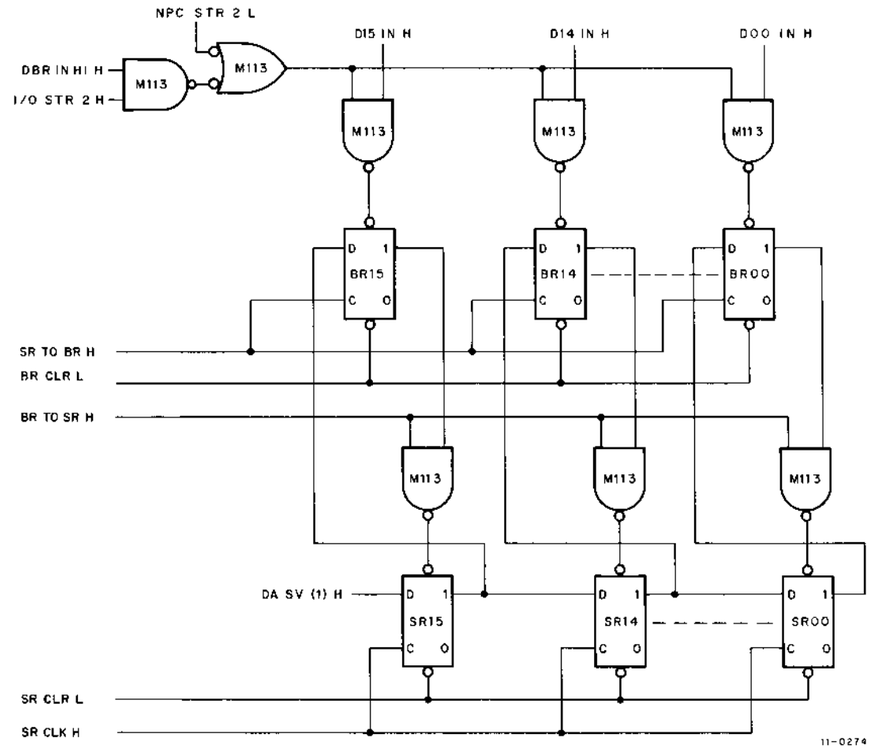



Figure 4-20 Buffer Register and Shift Register Interconnections

## 4.5 SYSTEM DATA TRANSFER LOGIC

This section describes the logic that handles the data being read or written by the disk and interfaces it to the bus. This logic consists of the buffer and shift register logic. Each type of RF11 operation (Write, Read, and Write Check) is described with reference to the hardware. Finally, the different types of data transfer error conditions and their respective logic are discussed.

#### 4.5.1 The Buffer and Shift Register Logic

The buffer and shift registers are continually passing data back and forth during the course of a data transfer. The buffer register accepts the data word from the bus during a bus transfer and passes the word to the shift register for writing on the disk surface for a write operation. Alternately, during a Read operation, the shift register assembles the word off the disk and passes it to the buffer register to be transferred onto the bus. Figure 4-20 shows the data paths between the two registers. The buffer register is filled from the bus (D15 IN – D00 IN) by NPC STR 2 from the NPR logic for a Write operation. The buffer register transfers data to the shift register under the command of BR to SR generated from SR CLR and ATPN (SR CLR is generated by SR1 and TP2). The shift register, in turn, transfers an assembled word to the buffer register with the SR to BR signal generated by SRO. The logic that controls these register to register signals is discussed in the following paragraphs in conjunction with the Read, Write, and Write Check operations. (Refer to engineering drawings D-BS-RF11-0-18, sheets 1 and 2, and D-BS-RF11-0-20 for the buffer and shift register logic, respectively.) The buffer register is also loaded by the program, with combinational logic of DBR IN and I/O STR 2, to check continuity between the processor and the RF11 Control.

#### 4.5.2 Write Operation Logic

Engineering drawings D-BS-RF11-0-11, sheet 2, and D-BS-RF11-0-31 show the logic and timing, respectively, that affect the RF11 during a Write operation. Assume that the Write operation has been loaded into the function register, DATA RQ is set, and that all other registers have been initiated. The GO command generated by I/O STR 2, DCS IN LO, and D00 IN sets the GO bit of the DCS, and clocks the write operation from the F0SV and F1SV flip-flops to the F0 and F1 bits of the function register. GO and F0SV (Write command) initiate the NPR for control of the bus. The combinational logic requests the first word to be written, which is loaded into the DBR by NPC STR 2 (see Figure 4-21). All successive words are requested by SRI until WC overflow occurs. NPC STR 2 also sets the WB FULL flip-flop which indicates to the RF11 that the buffer register has information that must be written. This prevents another word from being requested until the contents of the DBR are transferred into the SR. Meanwhile, the RF11 checks for equal comparison between the segment register and the disk address register. As soon as ADDR OK is generated, the level LS EN H enables the SRI flip-flop at CTP2 time, indicating that the disk location to be written into is almost under the write head. SRI is then clocked at TP2 time and set. SRI increments the word address portion of the disk address register, loads the word from the buffer register into the shift register with the signal BR to SR, sets LD SR(1) H, and clears WB FULL.

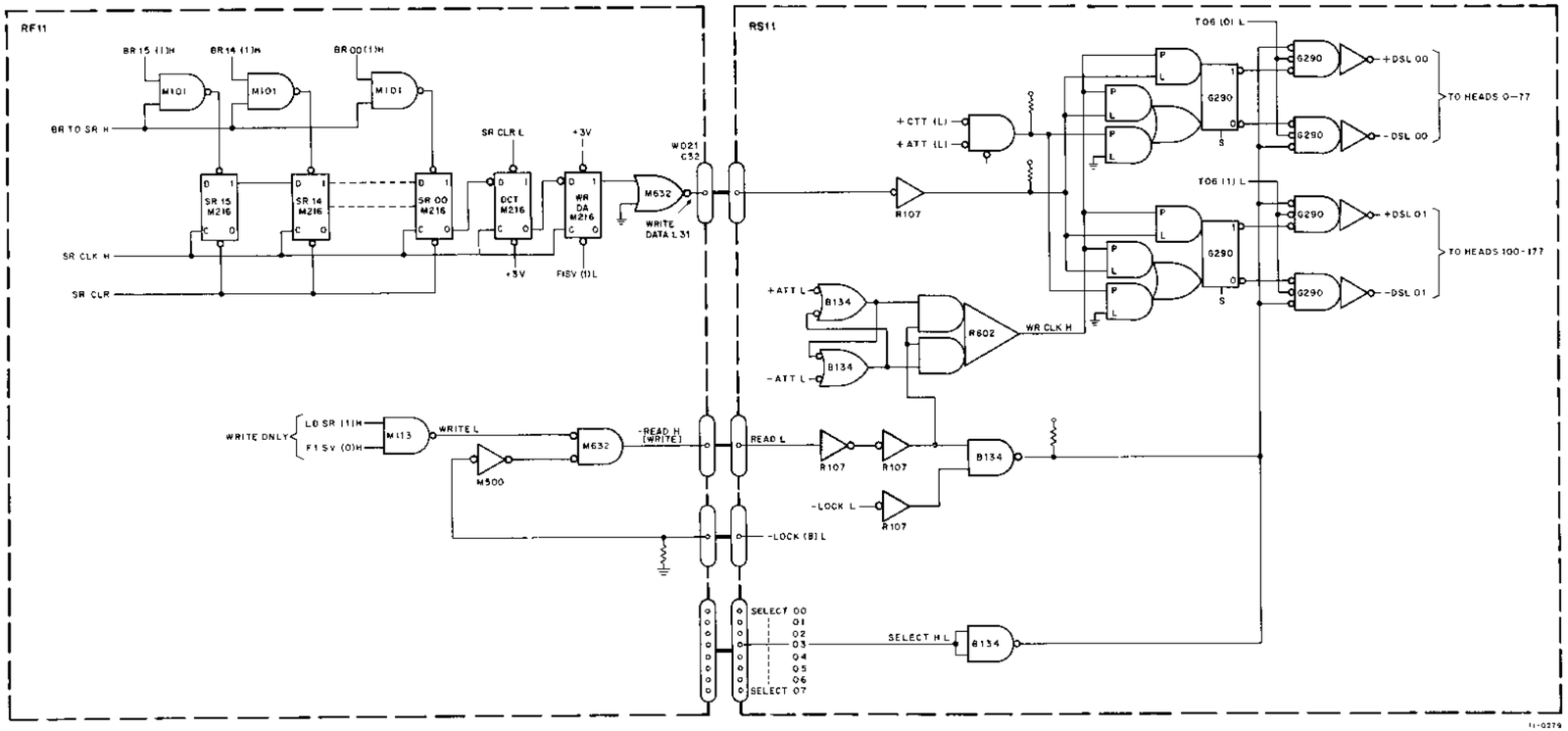



Figure 4-21 WRITE Circuitry to RS11

At this point the shift register begins shifting the word through flip-flops DCT and WR DA. The DCT flip-flop asserts the control bit at the beginning of the data word that is to be written on the disk. DCT is set when the shift register is cleared by SR CLR (00–07) before the shift register receives the word (SRI at TP2). The holding flip-flop WR DA (write data) clocks the shifting data through the RS11 cable to the RF11 disk circuitry. In the RS11 disk circuitry (see Figure 4-21) the data bits are clocked into the G290 Writer and through the heads to be written as flux changes on the disk surface. Note that the disk must be selected, a Write operation must be in process (LD SR (1)), and no lockout switch can be enabled (LOCK H), or the data bits are disabled at the input gates of the writer.

The AND of CTT (L) and ATT (L) clears the G290 Register before and after the data word is written. If the G290 flip-flop ends the word on a 0, the word has even parity (even number of 1's in the word), this gate has no effect. If the word has odd parity, the G290 ends on a 1 and is cleared by this gate. The flux change then records another 1, and also generates the even parity (sets the P bit to 1) that a complete word on a disk must have. In this way, each word is guaranteed to have the even and correct parity for which it is checked during a Read operation.

### 4.5.3 Read Operation Logic

Engineering drawings D-BS-RF11-0-11, sheet 1, and D-BS-RF11-0-32 show the logic and timing, respectively, that affects the RF11 during a Read operation. The logic up to the qualification of DA SV (see Figure 4-22) was explained in the description of the error detection circuitry (Paragraph 4.3). Each time PDT or NDT is set and subsequently reset by STROBE, indicating that a 1 bit has arrived, DA SV goes to 1. The SR CLK H pulses then shift the data down the shift register until the word is completely assembled. SR CLK H 1 and 2 are generated by the delay gating network shown on engineering drawing D-BS-RF11-0-19. These pulses are keyed by STROBE for a Read operation. For a Write operation, ATPN keys the SR CLK pulses.

At BC05 time (engineering drawing D-BS-RF11-0-19), the SRO flip-flop is enabled (provided RD SR is set and the last word taken) and sets with WBM at CTP2 time. SRO generates SR to BR and the contents of the shift register are loaded into the buffer register. At the same time, SRO sets the DATA RQ flip-flop in the NPR logic and the NPR logic is initiated. SRO also generates INC WA which increments the WC and the DAR. Finally, SRO sets RB FULL, which stays set until the bus takes the word out of the buffer register. When the memory has taken the word it issues SSYN which, combined with DATA to BUS H, clears RB FULL. At this time, the bus has taken the data and the next data transfer can begin.

In this description, the RD SR flip-flop is assumed to be set. It sets on the first CTP3 (0) H after the Read function is selected, as indicated in the function register, provided that the level RD DIS L is not present (i.e., ADDR OK has been generated by the comparison logic). (RD SR remembers that the last address was OK). RD DIS L is explained in Paragraph 4.5.7 with the start up circuits.

### 4.5.4 Write Check Logic

Write Check combines the logic and timing of the Read and Write operations. (Refer to engineering drawing D-BS-RF11-0-33 for the necessary Write Check timing.) The Write Check operation compares the data in memory to the corresponding data on the disk. Each word in memory is transferred into the buffer register as though performing a Write operation, and likewise loaded into the shift register. However, the RF11 logic now starts a Read operation (see Figure 4-22). The word off the RS11 disk is shifted through DA SV, while the word off the bus is shifted through DCT. DCT and DA SV always have related bits as the words are shifted through the shift register; that is, the words are compared bit by bit between DA SV and DCT as they are shifted into and out of the shift register. Figure 4-23 shows the comparison logic (refer to engineering drawing D-BS-RF11-0-12, sheet 2). If the comparison is not favorable, the error flip-flop WCE is set. The effects of this flip-flop are discussed in Paragraph 4.5.6.1.

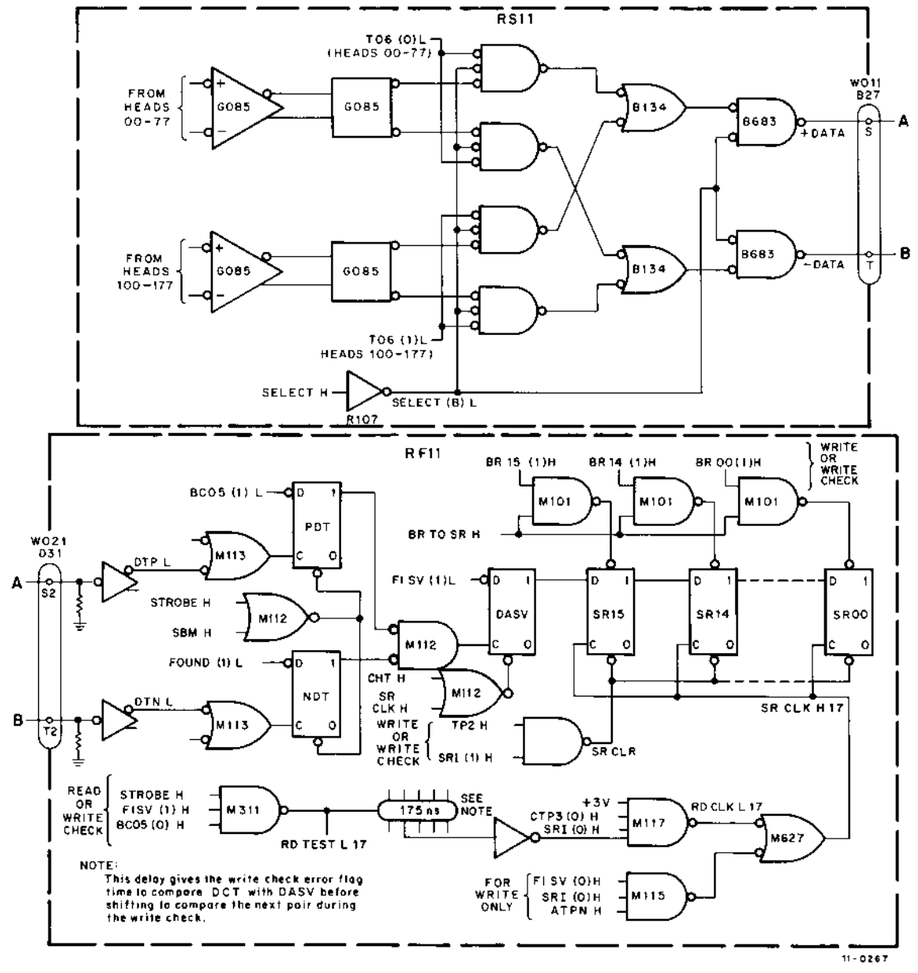



Figure 4-22 Read and Write Check SR and RS11 Logic

### 4.5.5 Data Transfer Error Condition Logic

The following paragraphs describe the data transfer error condition logic of the DCS. These are errors associated with data transfers and are considered correctable through the software or disk controls. The two DCS bits (FRZ and ERR) are described that tie in all RF11/RS11 System errors, both timing control errors (DAE) and data transfer errors (DCS).

**4.5.5.1 Write Check Error** – The Write Check Error (WCE) determines if there is an error during a Write Check operation (see Figure 4-23). The WCE flip-flop is set for this error if DCT and DA SV logic levels differ during the compare time. A Write Check error is latched until the control is cleared by CLR +GO CLR L. Therefore, the words compared in Write Check are different and there is a discrepancy error between the memory word and the corresponding disk word.

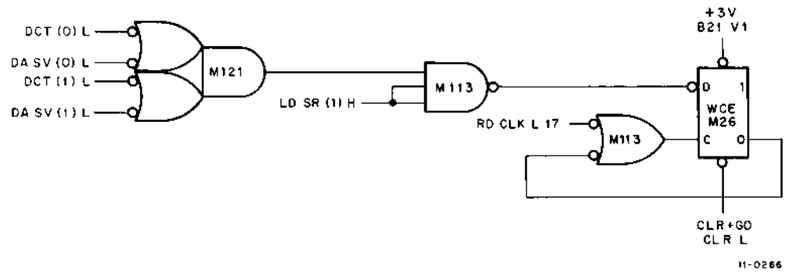



Figure 4-23 Write Check Error

**4.5.5.2 Error and FReeZe** – A FReeZe (FRZ) condition occurs if an A, B, or C track error is detected, if non-existent memory is in CMA, or if the address track indicates a parity error (see Figure 4-24). The ERRor (ERR) flag in the DCS that causes an interrupt is the OR of the flags shown in Figure 4-25. All ERR conditions are DCS bits except those that cause a FRZ.

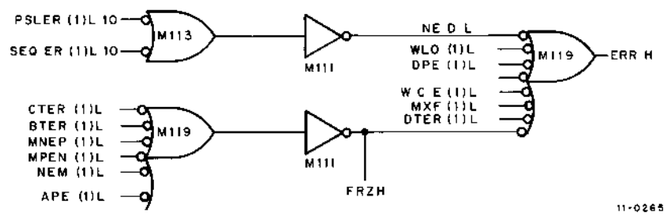



Figure 4-24 Error and Freeze

**4.5.5.3 Address Parity Error** – The APAR (Address PARity) flip-flop in the DAE continually examines the address bits (see Figure 4-25). Parity must be even; if on the last address bit APAR is set, a parity error has occurred. As a result, the APE (Address Parity Error) flip-flop is set at CTP3 time. The APE flip-flop remains set until cleared by CLEAR.

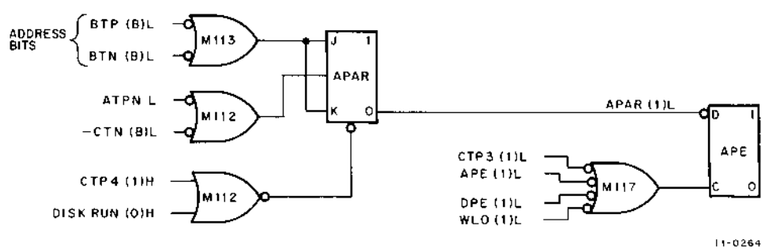



Figure 4-25 Address Parity Error

**4.5.5.4 Missed Transfer Error** – The MXF (Missed TransFer error) flag in the DCS is set if there is no ADDR → BUS L (see Figure 4-26) signal for 130 ms after CNTRL BSY is asserted, provided FRZ and MA are not asserted. In other words, if no data transfer is performed for three revolutions. Note that the M306 is an integrating one-shot that resets 130 ms after its input is unasserted.

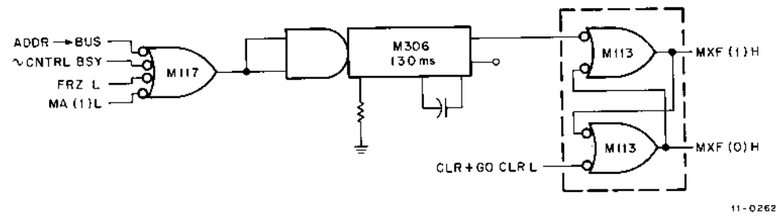



Figure 4-26 Missed Transfer Error

**4.5.5.5 Data Parity Error** – The DPAR (Data PARity) flag should be reset when the data word has been completely assembled (even parity) (see Figure 4-27). If the word is not completely assembled, DPAR remains set, indicating a Data Parity Error (DPE). As a result, the DPE flip-flop in the DCS is set at CTP3 time, if a Read operation has been specified and either RD SR is asserted (indicating valid data has been transferred) or LD LY is set (indicating a Write Check operation has been performed).

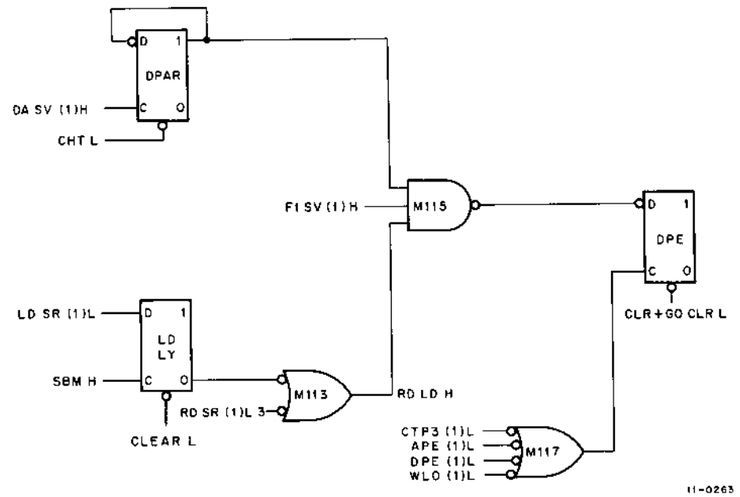



Figure 4-27 Data Parity Error

**4.5.5.6 Write Lockout Error** – In the RS11, the CT07 xH output of the G286 is +20 dc when selected (see Figure 4-28). The +20V signal is applied to the B683 driver when switch 34 is set to DISABLE WRITING. If the disk has been selected, a negative level is applied to the RF11, converted, and gated to the WLO (Write LockOut) flip-flop. The gating signals are generated before a valid Write operation.

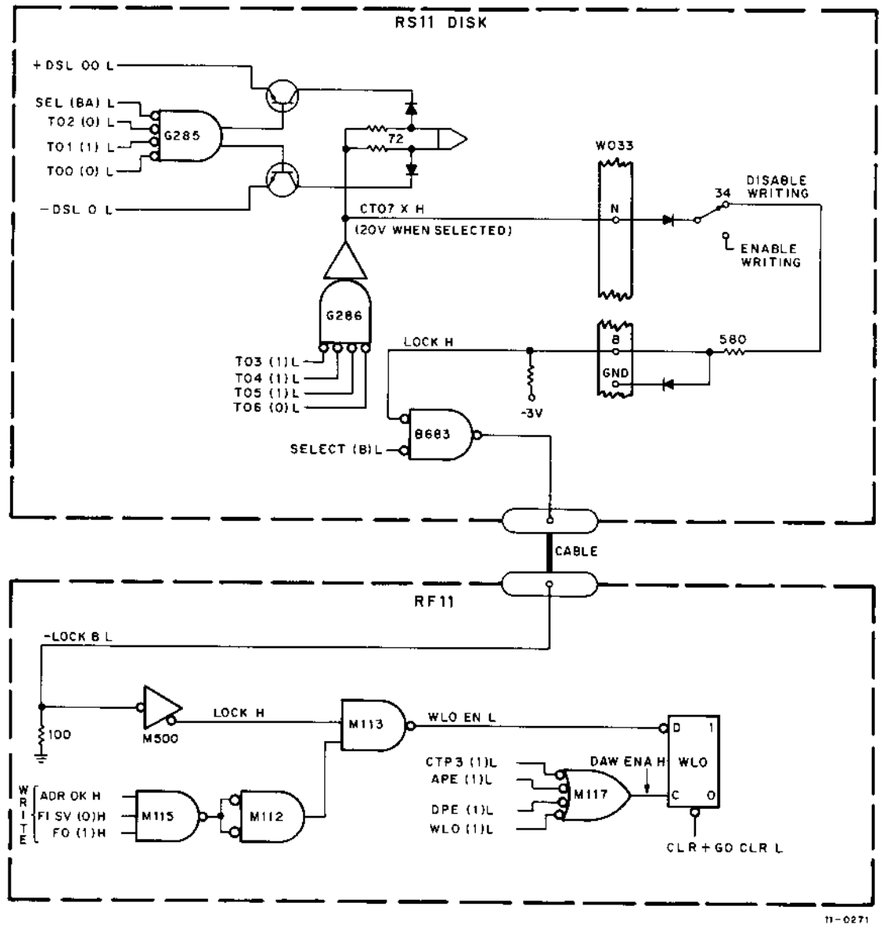



Figure 4-28 Write Lockout Error

At CTP3 time, WLO is set (if no data or address parity errors have been detected). Simultaneously, the Write operation is interrupted by LOCK H, as shown in engineering drawing D-BS-RF11-0-11, sheet 2, and the SRI flip-flop cannot be set.

**4.5.5.7 Nonexistent Disk Error (PSLER)** – The Program Select Error (PSLER) flip-flop sets if there is a SEL ERR (nonexistent disk selected) after a program-controlled disk selection (IOB TO DAE) (see Figure 4-29). The difference between PSLER and SEQ ER is that PSLER is the result of a program error rather than an error caused by stepping over bounds during a transfer. The 1.5-$\mu$s delay allows the selection logic (SEL ERR) to settle. The PSLER flag causes an NE D (NonExistent Disk) error signal.

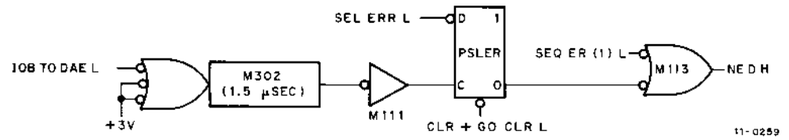



Figure 4-29 Nonexistent Disk by Program Selector Error

**4.5.5.8 Nonexistent Disk (SEQ ER)** – The NE D error signal can also be produced by the SEQ ER (Sequence Error) flag (see Figure 4-30). The SEQ ER flag is set under the following conditions:

*a.* If SEL ERR is enabled, indicating that a nonexistent disk has been selected.

*b.* If DA03 sets, indicating that the system capacity has been exceeded and the 9th disk was selected.

The flag is set by INC DA, which is delayed to wait for the settling time of the Disk Select logic. It is then gated with CNTR BSY and RB FULL (0) to the SEQ ER flip-flop. RB FULL (0) is set when the control has a word to transfer to core. As long as the control is waiting for that transfer, SEQ ER cannot occur. The SEQ ER flag causes an NE D error signal.

**NOTE**

**The SEQ ER flag is set only during a job transfer and not by an error in program control transfer.**

**4.5.5.9 Data Request Late Error** – The DRL (Data Request Late) flag indicates that NPR has failed and the data transfer was missed. The DRL bit of DAE sets under the following conditions (see Figure 4-31):

*a.* During Read, if RS TE sets because an SRO did not occur (the last word has not been transferred). This indicates that the data was not read by the data channel before SR was ready with next word. Therefore, NPR failed to establish bus control and the operation must be tried again.

*b.* During Write or Write Check, LS TE does not get reset by SRI (the word to be written did not arrive). This indicates that the data channel did not load the BR in time to transfer the SR to be written on the disk. Therefore, NPR has failed to establish a data channel in time and operation must be tried again.

### 4.5.6 The A TEST and Read Disable Signal

Several flags in the controller sense when the system is in a position to perform. The most critical of these flags is the DISK RUN flag (see Figure 4-32). This flag sets if there is a valid operation specified in the function register, the A track timing pulses are arriving on time, and a CTP4 (1) H level has asserted itself. Only if DISK RUN is set will ADR OK be allowed to happen (thereby allowing a Read, Write or Write Check operation). Note that DISK RUN resets as soon as ATOK goes away. This happens only if one of the A track pulses is dropped because of an error or because of the gap, as described in Paragraph 4.3. One of two error flip-flops also sets to indicate where the error occurred. The M306 delay, which is held high by DISK RUN, times out and resets, disabling A TEST L and stopping all timing track signals. The time it takes for the delay to reset gives the A track error detection logic a chance to set the appropriate error flag.

The M306 is triggered when DISK RUN is set. It does not reset until 5 $\mu$s after DISK RUN is reset, allowing A TEST L an extra 5 $\mu$s to function and the MNEP and MPEN flip-flops to set on the error condition.

Note that if ATOK was used (in place of A Test), no A timing error could ever exist.

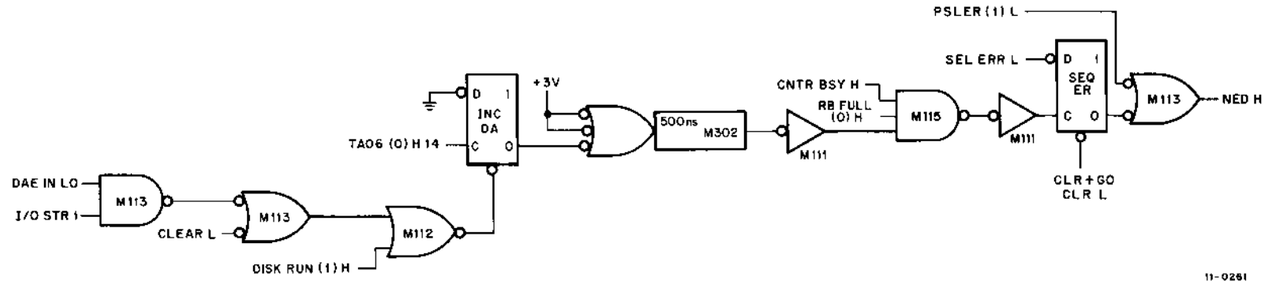



Figure 4-30 Nonexistent Disk by Sequence Error

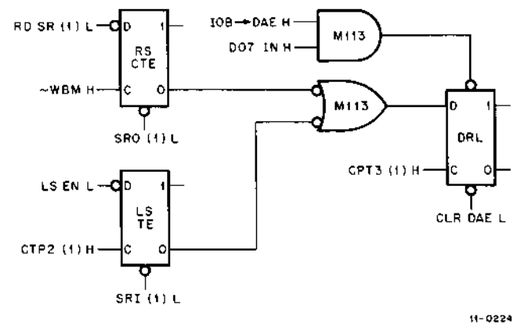



Figure 4-31 Data Request Late Error

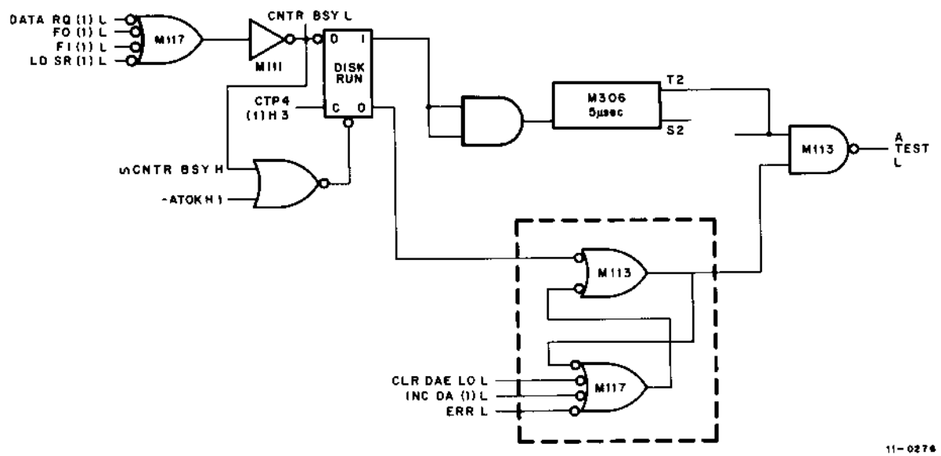



Figure 4-32 Disk Run Logic

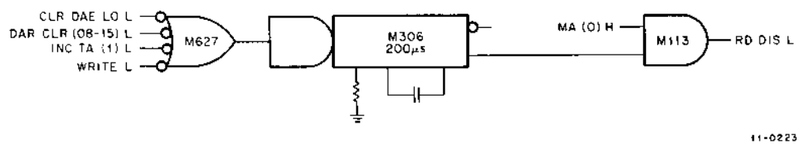



Figure 4-33 Read Disable Logic

The Read Disable signal is developed in Figure 4-33.

**NOTE**

**A Read operation is inhibited from starting for 200 μs when the RF11 is not in Maintenance mode after any of the following conditions:**

*a.* **The Track Address Register is incremented (INC TA (1) H).**

*b.* **The DAE Register is cleared by CLR DAE LOL.**

*c.* **A Write operation is performed.**

*d.* **The Disk Address Register is cleared (8–15).**

**The 200 μs is necessary to give the Disk Data Amplifiers time to settle and for Read head switching to be completed. In all cases, they are either reselected or going from Write to Read mode.**

### 4.5.7 The Gap

Before and after the gap, there is an area where the A track timing pulses are present, but no address or C track data is present. In these dormant areas, the controller does nothing because no valid address is decoded. In the gap proper, however, the A timing track stops. This causes DISK RUN to clear and the TA Register to increment. The Disk Address Register increments when the TA Register overflows and sets INC DA. When the A track returns, either because the present disk reached the end of the gap or a new disk is selected, DISK RUN sets, provided the disk control is still doing a valid functional CNTRL BSY is set. DISK RUN resets INC DA in preparation for the next TA Register overflow.

## 4.6 THE MAINTENANCE LOGIC

Engineering drawing D-BS-RF11-0-21 shows the logic that has been designed into the controller specifically for maintenance purposes. There are two distinct sections shown; the first section, which is made up of the four flip-flops MAT, MBT, MCT, and MDT, is used to simulate the signals coming from the heads of the disk surface. Three of the flip-flops are complemented (from D12IN to D10IN 1) under program command (I/O STR 1 and MA IN HI) and the MAT is toggled by the I/O STR 2. Their outputs are cabled to the input cable of the disk head (G789 head simulator cable). The second maintenance logic section is used to simulate the complete RS11 unit. Under program command, the output pulses from the RS11 can be generated from the processor using the AND gates of this logic. The MA flip-flop in the DCS is set when performing a maintenance function. MAT disables the error-detecting signal circuitry and ATOK (which would ordinarily prevent the RF11 from functioning because the A track signals cannot be generated quickly enough).

**NOTE**

**For this operation a special G681 terminator card must be used in place of the G711.**

# CHAPTER 5
# MODULE DESCRIPTIONS

## 5.1 INTRODUCTION

This section provides descriptions of special modules used in the RF11/RS11 System. Table 5-1 lists all the modules contained in the RF11/RS11 System and references as to where these modules are described.

**Table 5-1**
**Module Utilization**

| Module Number | Quantity Used | Title | Reference |
|---|---|---|---|
| | | **RS11 Modules** | |
| B134 | 2 | Diode Gate | |
| B152 | 1 | Binary To Octal Decoder | |
| B683 | 3 | Bus Driver | |
| G085 | 5 | Disk Read Amplifier | 3 |
| G285 | 8 | Series Switch | 3 |
| G286 | 4 | Centertap Selector | 3 |
| G290 | 2 | Writer Flip-flop | 3 |
| R002 | 1 | Diode Network | 1 |
| R107 | 1 | Inverter | 1 |
| R111 | 1 | Expandable NAND/NOR Gate | 1 |
| R602 | 1 | Pulse Amplifier | 1 |
| | | **RF11 Modules** | |
| G711 | 1 | Terminator Board | 3 |
| G723 | 3 | Negative Bus Terminator | 3 |
| G736 | 1 | Priority Selection | 3 |
| G740 | 1 | Disk Selection | 3 |
| G775 | 4 | Indicator Panel Connector Card | 3 |
| M105 | 1 | Address Selector | 2 |
| M106 | 1 | Dot NOR Gate | 3 |
| M111 | 2 | Inverter | 1 |
| M112 | 3 | NOR Gate | 1 |
| M113 | 16 | 10 2-Input NAND Gates | 1 |
| M115 | 4 | 8 3-Input NAND Gates | 1 |
| M117 | 3 | 6 4-Input NAND Gates | 1 |
| M119 | 2 | 3 8-Input NAND Gates | 1 |
| M121 | 3 | AND/NOR Gates | 1 |

**Table 5-1 (Cont)**
**Module Utilization**

| Module Number | Quantity Used | Title | Reference |
|---|---|---|---|
| | | **RF11 Modules (Cont)** | |
| M149 | 4 | 9 x 2 NAND Wired or Matrix | 3 |
| M161 | 1 | Binary to Octal/Decimal Decoder | 1 |
| M204 | 1 | Counter-Buffer | 1 |
| M205 | 6 | 5 "D" Flip-Flops | 3 |
| M207 | 1 | Flip-Flop | 1 |
| M216 | 18 | Six Flip-Flops | 3 |
| M302 | 3 | One-Shot Delay | 1 |
| M306 | 3 | Integrating One-Shot | 1,3 |
| M311 | 2 | Tap Delay | 3 |
| M500 | 2 | Neg Input Converter | 1,3 |
| M602 | 1 | Pulse Generator | 1 |
| M627 | 5 | Power Amplifier | 1 |
| M632 | 3 | Positive Input-Conv. Driver | 1,3 |
| M782 | 1 | Interrupt Control | 2 |
| M783 | 1 | Unibus Drivers | 2 |
| M784 | 2 | Unibus Receivers | 2 |
| M795 | 1 | WC and CMA | 2,3 |
| M796 | 1 | Unibus Master Control | 2,3 |
| M797 | 1 | Register Select | 3 |
| M798 | 1 | Unibus Driver | 2,3 |
| M920 | 4 | Unibus Cable Interface | 2 |
| W021 | 4 | RF11/RS11 Interface Cable Connector Card | 3 |
| | | **Maintenance and RS09-TA Modules** | |
| G681 | 1 | B Track Matrix | 3 |
| G787 | 1 | Signal Simulator Connector | 3 |
| G790 | 1 | Signal Simulator Generator | 3 |
| G821 | 1 | Regulator Control | 3 |

References: 1. The *Digital Logic Handbook* (1970 Edition)
2. *PDP-11 Unibus Interface Manual* (DEC-11-H1AA-D)
3. Special modules covered in this chapter.

## 5.2 DEC LOGIC

DEC builds three series of compatible below-ground logic (the B-, R- and S-series), two series of compatible above-ground logic (K- and M-series), an extensive line of modules to interface different types of logic (W-series), a line of special-purpose modules (G-series), and a line of support hardware for its module line (H-series).

With few exceptions, the DEC below-ground logic operates with logic levels of ground to -0.3V (upper level) and -3.2V to -3.9V (lower level), using diode gates that draw input current at ground. Figure 5-1 shows the voltage spectrum of negative logic systems.

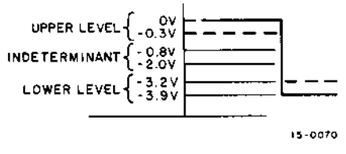



Figure 5-1 Voltage Spectrum of Negative Logic Systems

The compatible above-ground logic generally operates with levels of ground to +0.4V (lower level) and +2.4 to +3.6V (upper level), using TTL or TTL-compatible circuits with inputs that supply current at ground and outputs that sink current at ground. Figure 5-2 shows the TTL logic voltage spectrum.

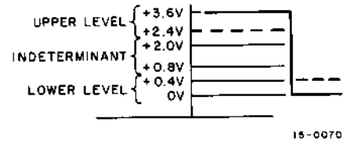



Figure 5-2 Voltage Spectrum of TTL Logic

The use of DEC's *Digital Logic Handbook*, 1970 edition, is recommended for readers of this manual who are not familiar with the basic principles of digital logic and the type of circuits used in DEC logic modules.

## 5.3 MEASUREMENT DEFINITIONS

Timing is measured with the input driven by a gate or pulse amplifier of the series under test and with the output loaded with gates of the same series (unless otherwise specified). Percentages are assigned with 0 percent indicating the initial steady-state level and 100 percent indicating the final steady-state level, regardless of the direction of change.

Input/output delay is the time difference between input change and output change, measured from 50 percent input change to 50 percent output change. Rise and fall delays for the same module are usually specified separately.

Rise time and fall time are measured from 10 percent to 90 percent of waveform change, either rising or falling.

## 5.4 LOADING

Input loading and output driving for TTL logic are specified in "units", with one unit equivalent to 1.6 mA. The inputs to low-speed gates usually draw 1 unit of load. High speed gates draw 1.25 low-speed units, or 2 mA.



## 5.5 MODULE MODIFICATIONS

The following is a list of modifications that are to be performed on some of the RF11/RS11 System modules prior to their installation in the system.

*a.* M105 – (must be Rev C or later) Remove address select jumpers 3, 4, 5, 8, 9, 10, 11, and 12.

*b.* M782 – Remove the vector address jumper 7.

*c.* M796 – Install a 56 MMF (Part no. 10-00012) timing capacitor on the split lugs.

*d.* G736 – Install a BR-5 priority level chip. The number on the chip must be toward the module handle.

*e.* G740 – Install one insulated jumper per number of disks in the system. The letters A–J correspond to the physical disks; the numbers 0–7 correspond to the disk address selected by the program.

## 5.6 MODULE CHARACTERISTICS

The following paragraphs describe the characteristics for all the RF11/RS11 System's special modules. This presentation includes module schematic diagrams and module component location diagrams. Modules G085 through G821 are described as RS11 modules, and modules G711 through M920 and cable W021 are described as RF11 modules. The 705B, 716, and H726-A are the RF11/RS11 System power supplies.

### 5.6.1 G085 Disk Read Amplifier

The G085 Disk Read Amplifier is a double-height module consisting of an ac-coupled amplifier with a bandwidth (-3 dB) from 20 kHz to approximately 1 MHz, followed by a slicer (see Figures 5-3, 5-4, and drawing C-CS-6085-0-1). The maximum voltage gain (under potentiometer control) is approximately 60 dB (1000). Common mode rejection ratio is approximately 40 dB. The amplifier is insensitive to any power supply ripple voltage less than 5 percent. Pin AM reduces the gain by approximately 30 percent when its input is low. The nonrectified slice output is gateable, and the slice point can be varied by logic inputs. A potentiometer is provided to adjust the slice. Pins at AT and AV are provided as amplifier test points. Proper grounding is critical in this module. G085 ground pins should not be bussed. Pins AS and AC should be connected to analog ground, and BF and BC should be connected to logical ground. All amplifier connections must be isolated from fast rise-time signals.

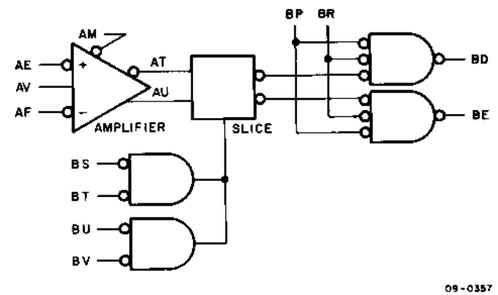
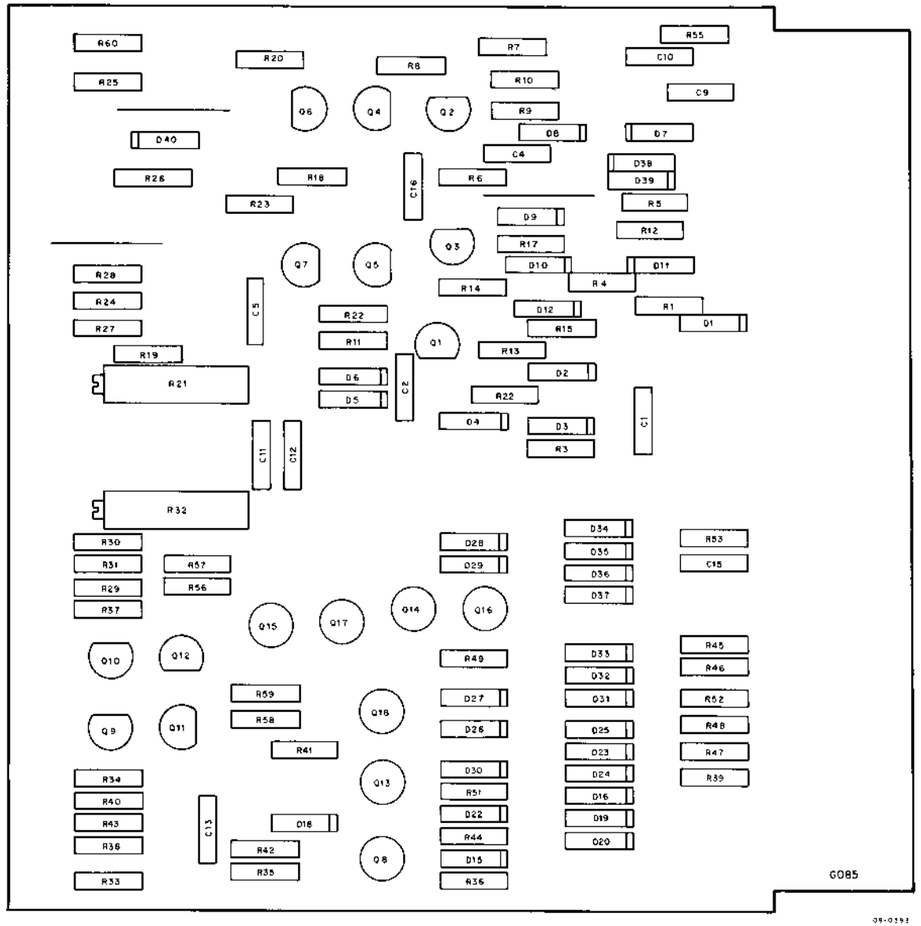



Figure 5-3 G085 Disk Read Amplifier and Slice, Block Schematic




**NOTE**
**R21 is used for gain adjustment, and R32 is used for slice adjustment.**

Figure 5-4 Disk Read Amplifier and Slice, Parts Location Diagram

Inputs: Voltage levels are 0 and -3V, except at the input to pins AE and AF.

| Pin | Function | Load or Input Voltage |
|---|---|---|
| AE,AF | Read Head Input | approx. 15 mV peak-to-peak |
| AM | Read Gain Control | 2 mA |
| BU,BV | Read Slice Control | 2 mA |
| BS,BT | Read Slice Control | 2 mA |
| BP,BR | Enable Output | 2 mA |

Outputs: Voltage levels are 0 and -3V except at AV, which provides +20V for the timing track center taps.

| Pin | Function | Drive |
|---|---|---|
| BE,BD | Signal Output | 10 mA |

Input/Output Delay: 120 ns

Power Dissipation: 2W at +20V
1.5W at -15V

Application: The G085 module is used to detect and amplify timing tracks and data signals for the disk system RS11.

### 5.6.2 G285 Series Switch

The G285 Series Switch is a single-height module consisting of two 4-input AND gates, each driving the base of two driver transistors (see Figures 5-5 and 5-6 and drawing B-CS-G285-0-1). When a gate is enabled, it in turn switches its corresponding transistors that form part of the select and read/write matrix of the disk or memory.

Inputs: Voltage levels to the gates are 0 and -3V. In levels to the signal inputs L and M are 0 and -15V.

| Pin | Function | Load |
|---|---|---|
| D,E,F,H,S T,V,M | Gate Enabling Inputs | 1 mA shared among inputs at ground |
| L,M | Signal Inputs | |

Outputs: Voltage levels are 0 and -15V (i.e., the input signal gated through the transistor). Each switch pole can drive up to 150 mA. Reverse voltage transients up to 100V do not destroy the switch circuits. Output pins J, K, R, and P must be returned through the load to +10V. The common pins (L and M) to both sets of switches must be returned to -15V. The switches will pass 1-MHz current. The voltage drop for 100 mA is approximately 1V.

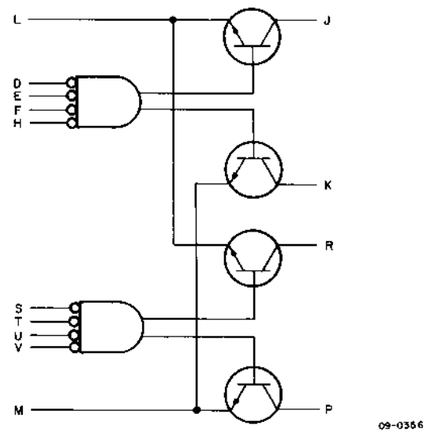



Figure 5-5 G285 Series Switch, Block Schematic

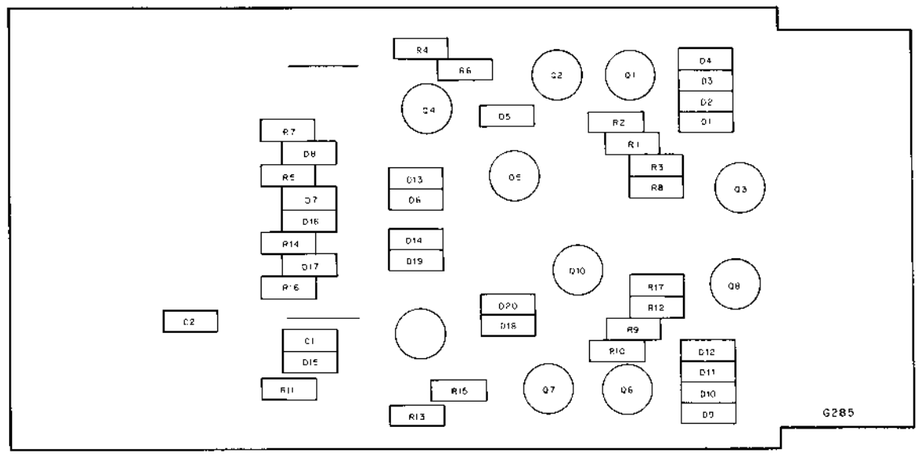



Figure 5-6 G285 Series Switch, Parts Location Diagram

Input/Output Delay: 1 μs

Power Dissipation: 1.5W

Application: This series switch is used together with the G290, the G286, and the G085 to form the read/write head matrix described in Paragraph 4.2

### 5.6.3 G286 Centertap Selector

The G286 Centertap Selector is a single-height module consisting of four AND gates, each of which drives a power output stage that applies a +20V level to its output pin when enabled by the gate (see Figures 5-7, 5-8 and drawing B-CS-G286-0-1).

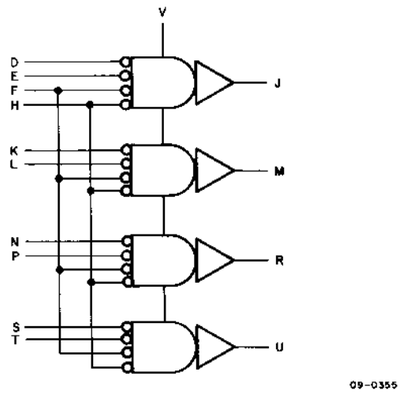



Figure 5-7 Centertap Selector, Block Schematic

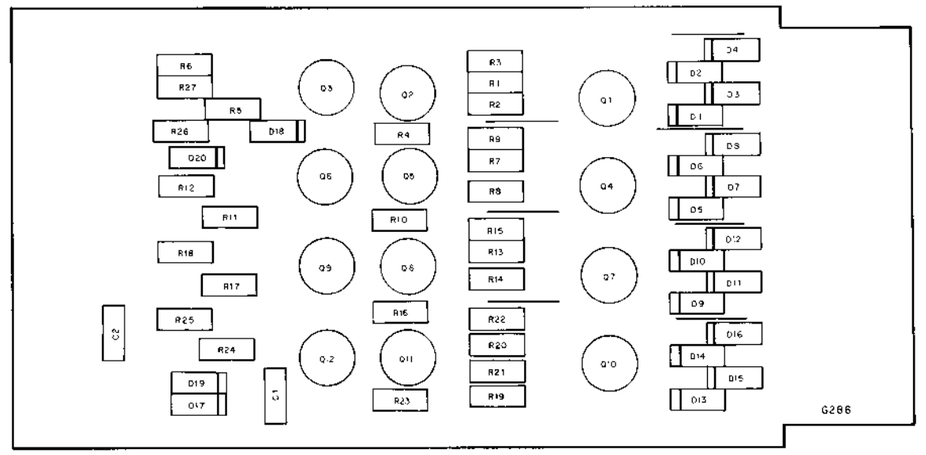



Figure 5-8 G286 Centertap Selector, Parts Location Diagram

Inputs: Voltage levels are 0 and -3V.

| Pin | Function | Load |
|---|---|---|
| D,E,K,L,N,P, | Gate inputs | 1 mA shared among |
| S,T,F,H | Gate inputs | inputs at ground in each circuit |

Outputs: Each output is +20V when the AND gate is enabled and 0V when the gate is not enabled. Each output drives 150 mA at +20V.

Input/Output Delay: 500 ns

Power Dissipation: 1.4W

Application: This module supplies the +20V read/write level to the coil of each head it drives in the matrix. Refer to Paragraph 4.2 for a more detailed description.

### 5.6.4 G290 Writer Flip-Flop

The G290 Writer Flip-Flop is a single-height board containing one JR flip-flop driving two AND gates and two power drivers. There are several gates to the input of the flip-flop (see Figures 5-9, 5-10 and drawing C-CS-G290-0-1).

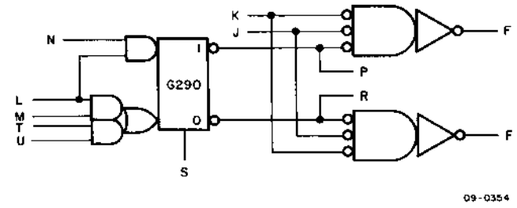



Figure 5-9 G290 Writer Flip-Flop, Block Schematic

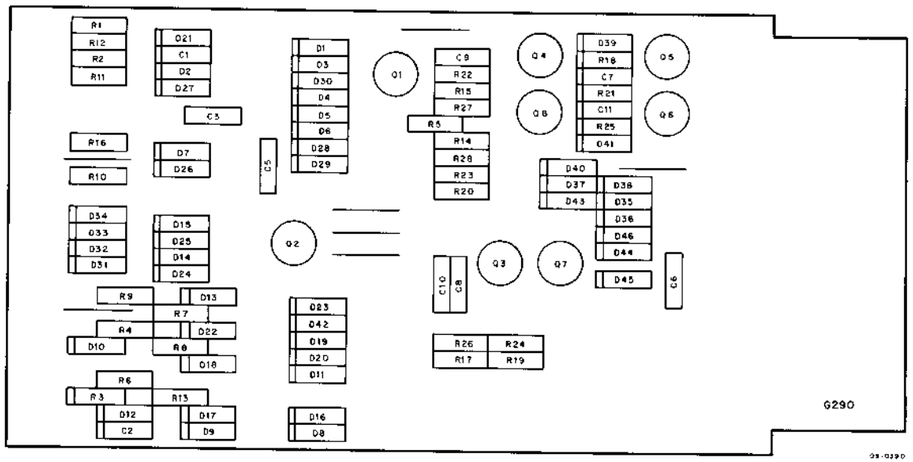



Figure 5-10 G290 Writer Flip-Flop, Parts Location Diagram

Inputs: Voltage levels are 0 and -3V.

| Pin | Function | Load |
|---|---|---|
| N,M,T,U, L | Inputs to flip-flop<br>Input to flip-flop | Each gate is a 1 mA load shared among its grounded inputs |
| S | Direct Clear | |
| K,J | Enable input to output driver gate | |

Outputs: The E and F outputs are -15V or an open collector. The P and R outputs are 0 and -3V.

| Pin | Function | Drive |
|---|---|---|
| E,F | Output to G285 Series Switch | 150 mA |
| P,R | Test output of flip-flop | 10 mA |

Input/Output Delay: 90 ns

Power Dissipation: 1W

Application: This module supplies the -15V write voltage to the G285 Series Switch. Details are given in Paragraph 4.2.

### 5.6.5 G681 B Track Matrix

The G681B Track Matrix is a single-height board containing the resistors and diodes for eight RF11/RS11 read/write heads (see drawing B-CS-G681-0-1). A complete description of the G681s used in the read/write circuitry is given in Chapter 4.

### 5.6.6 G789 Signal Simulator Connector

The G789 Signal Simulator Connector is a connector board for Flexprint used on the RF11 side of the head-simulator cable (see drawing B-CS-G789-0-1).

### 5.6.7 G790 Signal Simulator Generator

The G790 card is on the RS11 side of the head-simulator cable. The card consists of 4 transformer networks that accept the outputs of the maintenance flip-flops and convert their transitions to signals that resemble the signals from the read heads of the disk assembly (see drawing B-CS-G790-0-1).

### 5.6.8 G821 Regulator Control

The G821 Regulator Control is a double-height board serving as a voltage regulator that supplies +5 Vdc to the TTL logic of the timing track writer. It is capable of supplying a maximum current of 6A, provided it is supplied with an air circulation of at least 200 cfm. Without cooling, the G821 is rated at 2A.

Inputs: Ordinarily, the inputs are rated at 8 Vdc, 11 Vdc, and -15 Vdc. However, the timing track writer uses +10 Vdc and -15 Vdc supplied by the disk power supply.

Outputs: The timing track writer uses the regulated +5 Vdc output. This output can be varied between 4.5 and 5.5 Vdc by a potentiometer on the module. At 5 Vdc the regulation is 2 percent with a ripple of 25 mV peak-to-peak. The circuit schematic is given in drawing B-CS-G821-0-1.

### 5.6.9 G711 Terminator Board

The G711 Terminator Board is a single-height board containing 15 terminating resistors that present 100Ω to ground at each input pin (see drawing B-CS-G711-0-1).

Inputs: 100Ω to ground

Outputs: None

Power Dissipation: Approximately 90 mW per terminator

Application: This board must plug into the outside cable slot of the last RS11 on each RF11/RS11 disk cable bus.

### 5.6.10 G723 Negative Bus Terminator

The G723 is a single-height module containing nine terminating inputs for a negative bus (see drawing B-CS-G723-0-1).

### 5.6.11 G736 Priority Select Module

The G736 is a single-height module used to interface PDP-11 devices to the interrupt structure of the Unibus (see drawing C-CS-G736-0-1). The module contains a 14-pin IC socket that is designed to take specially etched chips for selection of an interrupt level from BR4 to BR7. The etched chips are used to discontinue the BR GRANT LINE to which the device is assigned.

### 5.6.12 G740 Disk Selection Module

The G740 is a single-height module used to jumper up to eight select lines to eight input signals (see drawing C-CS-G740-0-1). Split lugs are provided on the module for ease of inserting or removing jumpers. Each unjumpered output is clamped at +3V. Therefore, when a low of 0V is asserted at an input pin, the corresponding output to which it is jumpered is driven low.

The input pins are labeled from 0 through 7, while the output pins are labeled A through J, respectively.

### 5.6.13 G775 Indicator Panel

The G775 Indicator Panel is a connector card that provides isolation for logic levels and allows these levels to directly drive indicator bulbs without using light drivers (see drawing B-CS-G775-0-1). This connector card is designed to be used with the indicator panel, which supplies the necessary bias voltage.

| | |
|---|---|
| Inputs: | All inputs are 0 and -3V with 3 units of load each. |
| Outputs: | The output connects a Flexprint cable to the indicator board. |
| Power Dissipation: | 150 mW |

### 5.6.14 M106 Dot NOR Gates

The M106 is a single-height module containing six sets of 2-open collector NAND gates (see drawing C-CS-M106-0-1). Each set includes two gates with individual inputs and outputs and one common input. The module is generally used to gate signals onto an open collector bus.

### 5.6.15 M149 9 x 2 NAND Wired or Matrix

The M149 is a single-height module containing two sets of 9-open collector NAND gates wired together in an OR function to form nine output pins. The M149 also includes a pulse amplifier (see drawing B-CS-M149-0-1).

| | |
|---|---|
| Inputs: | Voltages are standard TTL levels. Input loading is 1 unit per input. |
| Outputs: | Voltages are standard TTL levels. Each output except V1 is an open collector that can sink 16 mA. The output at V1 can drive 10 unit loads. |
| Input/Output Delay: | 10 ns at output |
| Power Dissipation: | 350 mW |
| Application: | This module is generally used to gate signals onto an open collector bus. |

### 5.6.16 M205 5 D Flip-Flops

The M205 Module contains five separate D-type flip-flops. Each flip-flop has independent DATA, CLOCK, SET, and CLEAR inputs (see drawing B-CS-M205-0-1). Information must be present on the DATA input 20 ns (maximum) before the CLOCK pulse, and the information should remain at the input at least 5 ns (maximum) after the CLOCK pulse has passed the threshold voltage. Data transferred into the flip-flop by the previous CLOCK pulse will be present on the 1 output of the flip-flop. Typical time duration of the CLOCK pulse preset and reset pulses is 30 ns each. Maximum delay through the flip-flop is 50 ns. Refer to the M206 description for additional details.

The following are the input, output, and power characteristics of the M205 module.

| | |
|---|---|
| Input: | D inputs present 1 unit load each.<br>C inputs present 2 unit loads each.<br>SET inputs present 2 unit loads each.<br>CLEAR inputs present 3 unit loads each. |
| Outputs: | Each output (0 and 1) is capable of driving 10 unit loads. Two +3V supplies (U1 and V1), capable of 25 unit loads, are available. |
| Power Dissipation: | +5V at 55 mA (average), 100 mA (maximum). |

### 5.6.17 M216 Six D Flip-Flops

M216 is a single-height module containing six D flip-flops (see drawing B-CS-M216-0-1). All flip-flops operate independently except for their clear line, which is shared among three flip-flops.

Data must be present at the D input 20 ns before the clock pulse and should remain 5 ns after the leading edge of the clock pulse has passed the threshold voltage. The flip-flop settles in 50 ns. The CLOCK, DIRECT SET, and CLEAR inputs must be present for at least 30 ns.

Inputs: Voltages are standard TTL levels.

| Pin | Function | Load |
|---|---|---|
| B1,D2,H1,L2,N1,S2 | C Inputs | 2 units |
| C1,E2,J1,M2,P1,T2 | D Inputs | 1 unit |
| D1,F2,K1,N2,R1,U2 | DIRECT SET | 2 units |
| A1,K2 | DIRECT CLEAR | 9 units |

| | |
|---|---|
| Outputs: | Voltages are standard TTL levels. Each output is capable of driving 10 unit loads. |
| Input/Output Delay: | 50 ns |
| Power Dissipation: | 435 mW |

### 5.6.18 M306 Integrating One-Shot

The M306 is a single-height module containing one integrating monostable multivibrator (see drawing C-CS-M306-0-1). The integration timing is changed by changing the capacitance across Q2 and adjusting the R12 potentiometer. The minimum equivalent parallel resistance of capacitor leakage should always exceed 250KΩ. The resistive value of the potentiometer should not exceed 25000Ω. An input pulse of 30 ns will trigger the M306.

| | |
|---|---|
| Inputs: | Each input represents 1.25 load units. |
| Outputs: | Pin S will supply 12.5 load units and pin L will supply 11 load units. |
| Input/Output Delay: | 40 ns (maximum) |
| Power Dissipation: | +5V at 120 mA (maximum) |

### 5.6.19 M311 Tapped Delay Line

M311 is a single-height board containing two tapped delay lines (see Figure 5-11 and drawing B-CS-M311-0-1). Each delay line has ten taps, providing fixed delays from 25 ns to 250 ns. An input NAND gate to the delay line provides an additional delay of 10 ns. Input impedance of the delay line is 100Ω at ±5%.

| | |
|---|---|
| Inputs: | Voltages are standard TTL levels. Input loading is 1.25 units. |
| Outputs: | Voltages are standard TTL levels. Each output can drive 1.25 units. Maximum total drive is 6 units. Wire lengths should be kept to a minimum (less than 6 in.). |

Input/Output Delay:

| Pin | Delay |
|---|---|
| K2,J2 | 35 ns |
| L2,K1 | 60 ns |
| M2,L1 | 85 ns |
| N2,M1 | 100 ns |
| P2,N1 | 135 ns |

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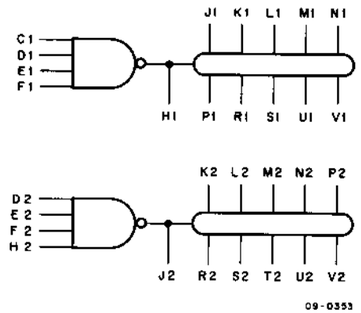



Figure 5-11 M311 Tapped Delay, Block Schematic

| | Pin | Delay |
|---|---|---|
| Input/Output Delay: (cont) | R2,P1 | 160 ns |
| | S2,R1 | 185 ns |
| | T2,S1 | 210 ns |
| | U2,U1 | 235 ns |
| | V2,V1 | 260 ns |

Power Dissipation: 850 mW

### 5.6.20 Negative Input Converter

M500 is an M-series single-height module containing eight I/O bus receivers that can accept negative logic levels and convert them to positive levels (see Figures 5-12, 5-13, and drawing C-CS-M500-0-1). Each M500 receiver has a negative input clamped to 0V and -3V. The threshold switching level is -1.5V with an input current of 100 $\mu$A.

Inputs:
- Minimum input impedance at 0V: 30 k$\Omega$
- Maximum current load to bus: 100 $\mu$A
- Inputs are standard negative logic levels of 0 and -3V.

Outputs:
- Fan Out Output No. 1: 12 units
- Output No. 2: 11 units
- Input/Output No. 1 delay: 50 ns
- Input/Output No. 2 delay: 40 ns
- Outputs are standard TTL logic levels.

Power Dissipation:
- 750 mW max from -15V
- 800 mW max from +5V

Application: The M500 module was designed to receive PDP-9 I/O bus signals for devices using positive logic. It provides a high input impedance.

### 5.6.21 M632 Positive Input-Converter Driver

The M632 is an M-series single-height module containing eight driver circuits (see Figures 5-14, 5-15 and drawing C-CS-M632-0-1). It accepts positive logic signals and converts them to negative logic levels.

Each driver consists of a TTL input gate and a negative open-collector output driver clamped to ground and -3V.

Inputs: Standard TTL levels – input current load at 0V is 1.25 units.

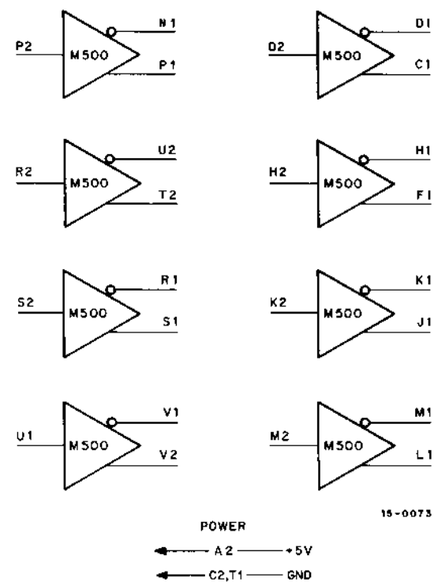



Figure 5-12 M500 Negative Receiver, Block Schematic

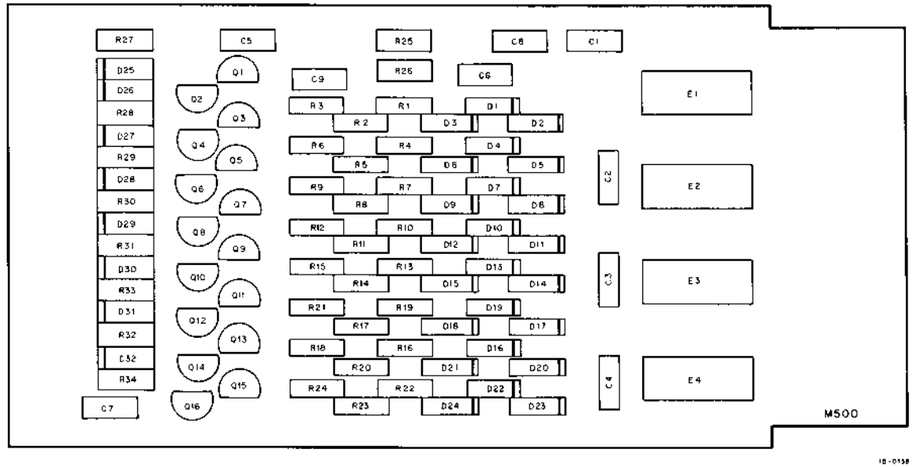



Figure 5-13 M500 Negative Receiver, Parts Location Diagram

Outputs: Outputs are standard negative logic levels.
- Risetime: 15 ns
- Falltime: 15 ns with 1.5 k$\Omega$ to -15V at output

Input/Output Delay: 50 ns (maximum)

(continued on next page)

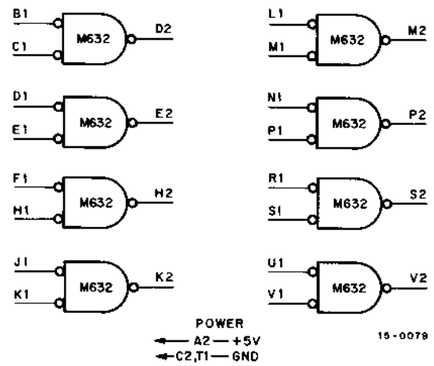



Figure 5-14 Negative Driver, Block Schematic

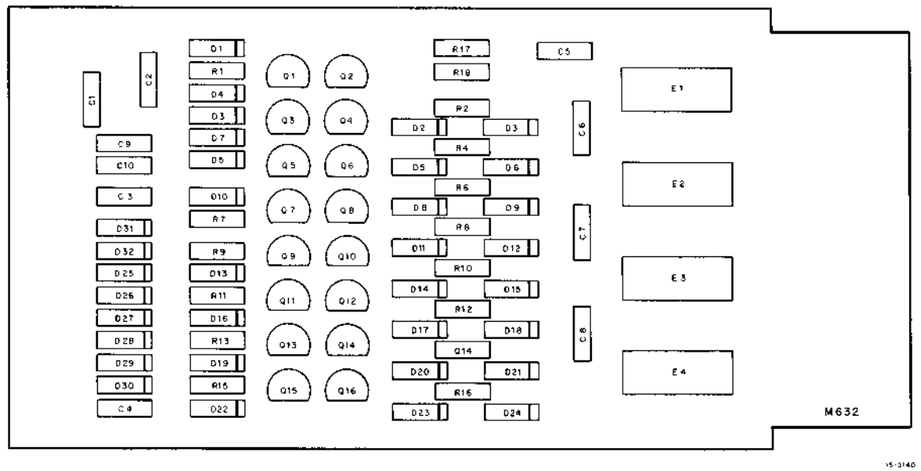



Figure 5-15 M632 Negative Driver, Parts Location Diagram

| | |
|---|---|
| Power Dissipation: | 600 mW from -15V (maximum)<br>900 mW from +5V (maximum) |
| Application: | The M632 is used to convert positive logic signals to negative logic levels that drive the PDP-11 negative I/O bus. The M632 is pin compatible with the M622. |

### 5.6.22 M795 Word Count & Current Memory Address Module (WC&CMA)

The M795 is used to interface Direct Memory Access (DMA) devices to the PDP-11 Unibus. The module provides two 16-bit counters used to count the number of data transfers that occur and to specify the bus address of the data to be transferred.

**5.6.22.1 Theory of Operation** – Block transfer devices that operate as bus master in data transfers usually need two registers to hold the parameters of the transfer. The first parameter is transfer count. A register is initially loaded with the 2's complement of the number of items to be transferred to or from memory. The register is incremented after each transfer. If the new value of the register is 0 (indicated by an overflow), further transfers are inhibited and the block transfer is complete. Information can be transferred in words (16 bits each) on the Unibus, and thus the name Word Count (WC) is usually assigned to this register.

The second parameter used in block transfers is the transfer address. A register is initially loaded with an address that specifies the memory location to or from which data will be transferred. The contents of this register are incremented after each transfer so that it continually "points" to sequential memory locations. Since memories as well as devices have addresses on the Unibus, this register is termed Current Memory Address (CMA).

**5.6.22.2 Functional Description** – The M795 is shown as a simplified block diagram in Figure 5-16. (See drawing D-CS-M195-0-1 for circuit schematics.) Both the CMA and WC are composed of 16 flip-flops; each register can be loaded by placing data on the 16 data line inputs common to both registers and asserting the appropriate loading signal. There are four independent loading signals: high byte of WC, low byte of WC, high byte of CMA, and low byte of CMA. The outputs of the 16 bits of the WC register are tied to a set of Unibus drivers (DEC 8881s). The contents of the WC register can be gated to the data bus when the appropriate gate signal is activated. The CMA register also has a set of Unibus drivers that allow its contents to be gated to the data bus. Note that the driver outputs of both WC and CMA are wire ORed together. In addition, the CMA register has a set of drivers with independent outputs that allow it to drive the address bus.

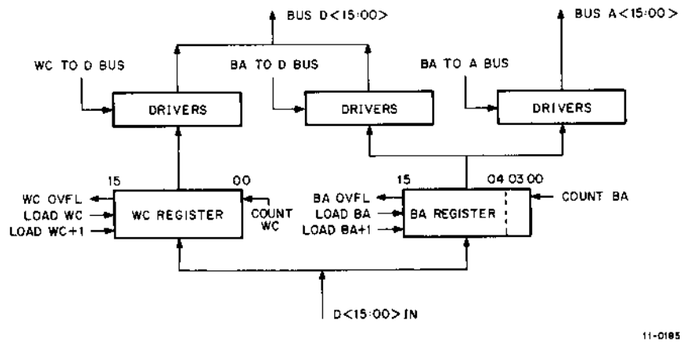



Figure 5-16 M795 Word Count and Bus Address, Block Diagram

The CMA register can be incremented by 1 or 2 as a function of a control input (grounded = +2; +3V = +1). In the RF11, the module allows the addressing of sequential words. The register is incremented on the trailing edge of a positive pulse applied to its count input. The carry between bits 3 and 4 is broken and brought out to the pins. In the RF11, these pins are jumpered together externally to allow for a full 16-bit count. An overflow pulse is provided as an output whenever the register is incremented from all 1's to all 0's. The WC increments on the trailing edge of a positive pulse applied to its count input. An overflow pulse is also available. Both registers are reset to all 0's whenever the clear signal is asserted. Tables 5-2 and 5-3 list the inputs and outputs of the M795, respectively.

Table 5-2
M795 Input Signals

| Signal Name | Assertion Level | No. of Signals | Loading | Operation |
|---|---|---|---|---|
| D(15:00)IN | +3V=1 | 16 | 1.5 | Data inputs to register. |
| LOAD WC<br>LOAD WC+1<br>LOAD CMA<br>LOAD CMA+1 | 0V | 4 | 1 | Loads data on input into selected byte of register. Low pulse of 250 ns minimum duration. |
| WC OUT<br>CMA OUT<br>ADDR → BUS | 0V | 3 | | Gates selected register to bus. |
| CLEAR | +3 | 1 | | Clear all bits. High level of 1 μs minimum duration. |
| INC WA<br>CMA CLK | +3V | 2 | 4 | Trailing edge of positive pulse increments register (100 ns minimum). |

Table 5-3
M795 Output Signals

| Signal Name | Assertion Level | No. of Signals | Drive Capability | Operation |
|---|---|---|---|---|
| CMA CARRY OUT | 0V | 2 | 10 | Register overflow; low-level pulse. |
| BUS D(15:00) | 0V=1 | 16 | Unibus | Drives data lines. |
| BUS A(15:00) | 0V=1 | 16 | Unibus | Drives address lines. |

### 5.6.23 M796 Unibus Master Control Module

The M796 is used to control data transfer operations on the PDP-11 Unibus. It provides the necessary sequence of signals to one of the four possible Unibus data transactions (see drawing D-CS-M796-0-1).

**5.6.23.1 Theory of Operation** – Each device in a Unibus system has the capability to gain control of the bus and, as bus master, transfer data to and from other slave devices on the bus. This type of operation is done independently of processor control and is usually termed Direct Memory Access (DMA). The logic necessary to gain mastership of the bus is provided by the M782 Interrupt Control module. This module can assert a request for bus use (usually done on the NPR level), receive the Bus Grant from the processor, assert Selection Acknowledge (SACK), and wait until the current bus master releases bus control, at which time it asserts BUS BUSY claiming bus control.

Once bus mastership is assumed by the device, it can conduct a data transfer. A DATI cycle is performed if the device needs data (byte or word) from memory; a DATO cycle is performed if the device is storing a word of data in memory (DATOB operation for bytes); and a two-cycle DATIP – DATO (B) operation is performed when data held in memory is to be modified (e.g., increment memory or add-to-memory).

To execute one of these cycles, the devices must set BUS C (1:0) for the type of data transfer, specify the address of the slave device with which it will be transferring, assert MSYN, and then wait for the slave's SSYN response. Data must either be gated to D(15:00) on a DATO cycle, or received and strobed at the proper time on a DATI cycle.

**5.6.23.2 Functional Description** – A block diagram of the M796 is shown in Figure 5-17. The outputs BUS C1 and BUS C0 can directly drive the Unibus and are asserted as a function of the control inputs. The following table lists the control input set ups for the four possible bus cycles. (Refer to Figures 5-18 and 5-19 for timing diagrams of DATI and DATO, respectively.

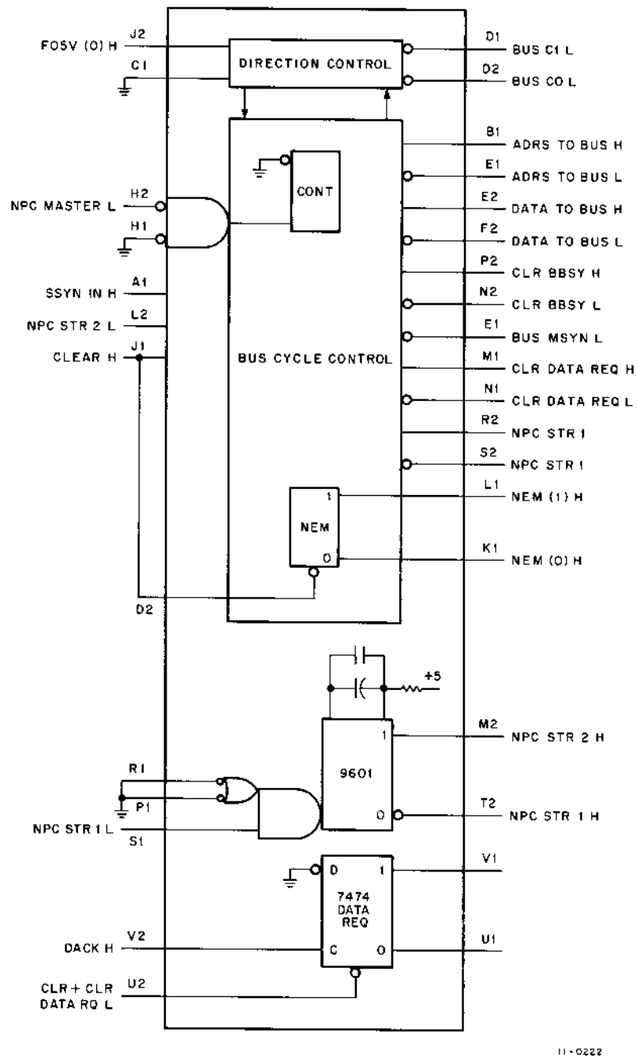



Figure 5-17 M796 Block Diagram

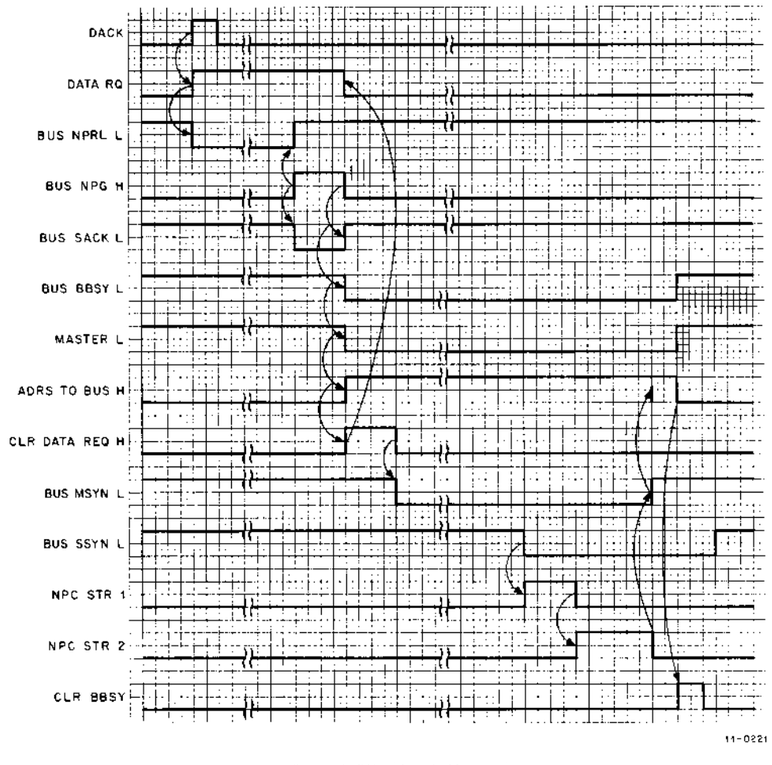



Figure 5-18 DATI Operation

| C1 Control | C0 Control | Data Operation |
|---|---|---|
| 0 | 0 | DATI |
| 0 | 1 | DATIP |
| 1 | 0 | DATO |
| 1 | 1 | DATOB |

(0=low level, 0V; 1=high level, +3V.)

In the RF11, the Data Operation is controlled by the function register (F0SV). The data transfer sequence is triggered by the assertion of NPC MASTER and can be either a DATI or DATO. At the transisition of NPC MASTER and CONT SETS, BUS C1 and BUS C0 are asserted as a function of their control inputs. Also, ADRS TO BUS is asserted. This signal is used to gate the CMA REG address onto BUS A⟨17:00⟩. If an output cycle is specified (F0SV (0) H = 1) DATA TO BUS is asserted and used to gate the DBR REG data to be transferred to the slave onto BUS D⟨15:00⟩.

200 ns after CONT SET, BUS MSYN is asserted. The master now waits for the slave's response.

In a data output cycle, SSYN assertion causes BUS MSYN to be negated immediately, with BUS C1, BUS C0, ADRS TO BUS, and DATA TO BUS negated after a 100-ns delay. When these signals drop, a pulse appears at CLR BBSY. This pulse is used to release control of the bus (removes BUS BBSY). In a data input cycle, the

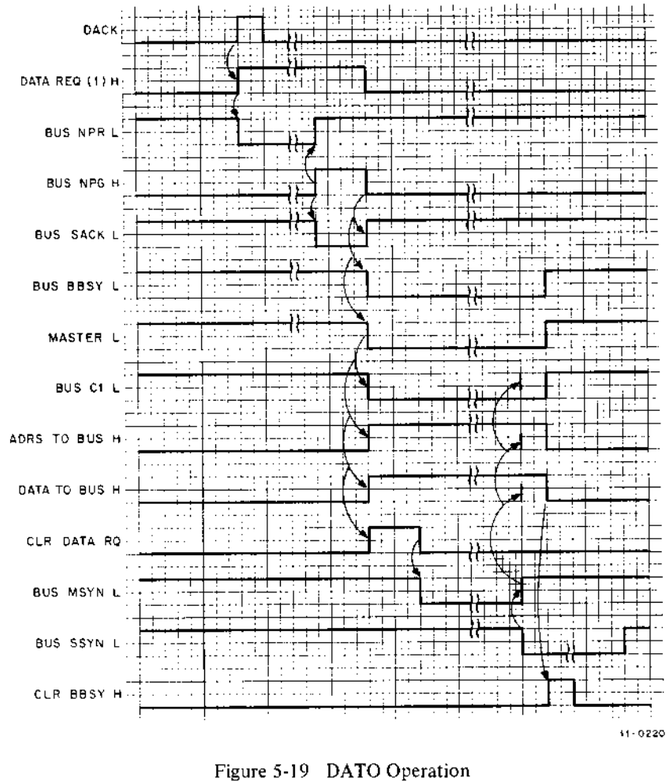



Figure 5-19 DATO Operation

assertion of SSYN produces a 200-ns pulse that appears on NPC STR 1. This delay allows the data being received to deskew and settle and is used to clear the DBR REG. The trailing edge of NPC STR 1 is used to trigger the one-shot provided on the module and create NPC STR 2 which strobes the data into the DBR REG. Once data has been received, the trailing edge of NPC STR 2 causes BUS MSYN to be negated, along with ADRS TO BUS, BUS C1, and BUS C0 100-ns later.

A NEM flip-flop is provided which sets if a SSYN response does not occur within 20 μs of asserting BUS MSYN. If this flop gets set, the bus cycle is aborted. NEM is cleared by asserting CLEAR H.

The M796 module also provides a flip-flop whose clock, reset, one side, and zero side are made available. A positive transition on the clock will set the flip-flop. The RF11 uses this flip-flop (DATA REQ) to flag the M782 that the control desires to become bus master.

### 5.6.24 M797 Register Selection Module

The M797 is a single-height module used to decode one of eight possible register addresses in conjunction with the M105 module (refer to Table 5-1 for M105 reference). In addition, control signals are used to select a read, write low byte, or write high byte (see drawing D-CS-M797-0-1).

**5.6.24.1 Theory of Operation** – The M797 contains three BCD/DEC decoders. Outputs 0 through 7 are used to select a register, and 8 and 9 are used to create a gating strobe. The module is enabled by the input at V1 (DEV SELD) at which time the control signals at A1 and D1 select the correct decoder(s) for the operation specified. Once a decoder or decoders have been selected its 8 and 9 outputs are driven high, which asserts STRT XTIM output at H1. One of the 0 through 7 outputs of the decoders is selected by the inputs at B2, B1, and C1. These inputs are inverted before reaching the decoders so that if they are all high the 0 output of the decoder will be selected. The input at V2 can be used to prevent the selection of the two decoders used to write into a register when it is asserted H (i.e., BUSY H). The exception to this is when the three address inputs are high (i.e., selection of a control register). In the RF11 this feature is not used and V2 is grounded.

### 5.6.25 M798 Unibus Drivers

The M798 is made up of 16 noninverting Unibus drivers. A typical circuit is shown in Figure 5-20. The module is used in device interfaces to minimize the loading effect of attaching several drivers to the same Unibus signal line, as is the case when a device is made up of multiple registers. (Loading of signal lines on the Unibus is restricted to one unit load per device, where a unit load is the equivalent of one receiver input and two driver outputs, 210 $\mu$A total.)

In addition, the M798 allows the Unibus to be driven by standard open collector TTL gates. The inputs to each circuit on the M798 are pulled to +5 through a 1K resistor. As shown in Figure 5-21, an internal wire-ORed bus is created that is driven from standard open-collector gates (available on M141 and M149), as well as Unibus drivers (available on M783 and M785) (see drawing D-CS-M798-0-1).

M798 Signals: Input loading (each of 16 inputs) = 4.1 TTL loads. Output drive (each of 16 outputs) = 50 mA sink @ 0.8V (maximum). Open collector leakage of 25 $\mu$A.

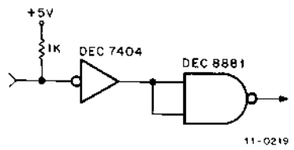



Figure 5-20 Noninverting Unibus Driver

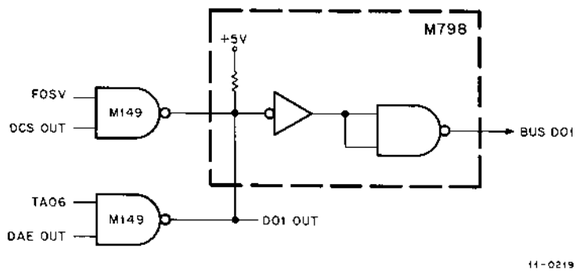



Figure 5-21 Internal Wire-ORed Bus

### 5.6.26 W021 RF11/RS11 Interface Cable

The W021 is a 16-lead ribbon cable that interfaces the RF11 with the RS11 (see drawing RS-B-W021). All communication between the units is done through this cable. The inputs and outputs are off the RS11 circuitry and the RF11.

## 5.7 RF11/RS11 POWER SUPPLIES

The following paragraphs describe the RF11/RS11 power supply units.

### 5.7.1 705B Power Supply

The 705B Power Supply provides the logic power needed for the RF11/RS11 System (see Figure 5-22 and drawing C-CS-705-B-1). It is designed for 50/60 Hz single-phase input.

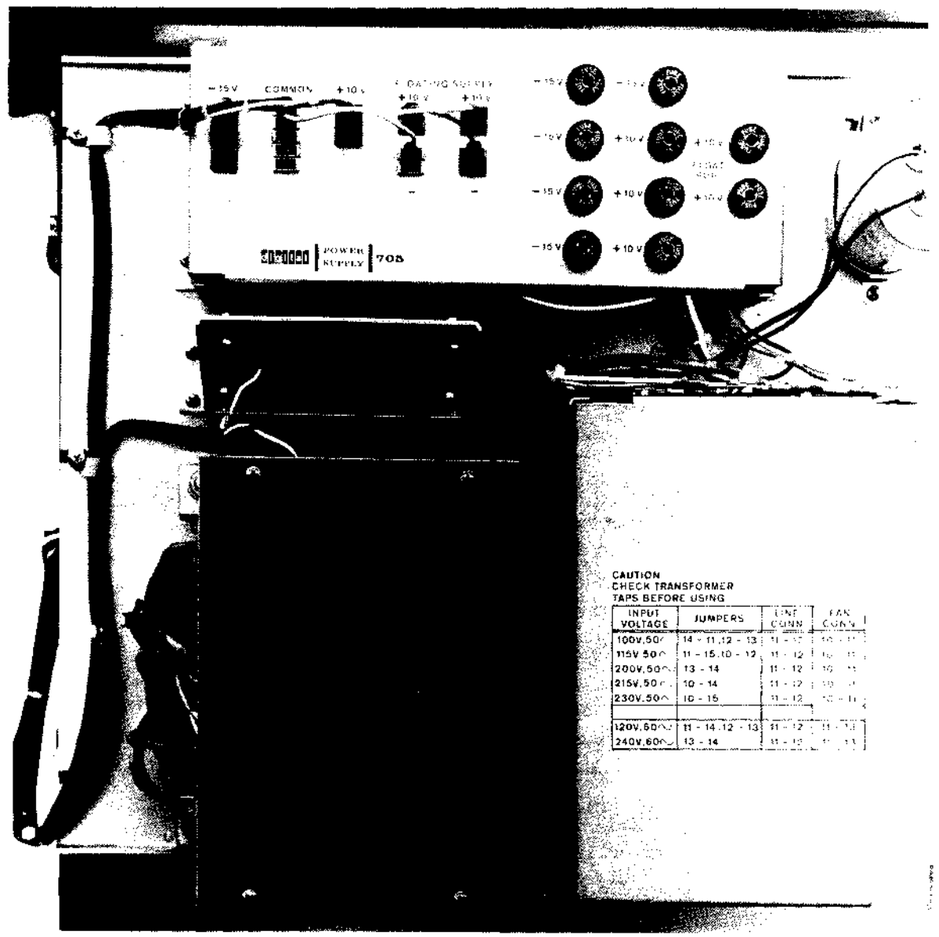



Figure 5-22 705B Power Supply

The 705B can be driven from the following voltage and frequency combinations by selection of the appropriate taps.

| | |
|---|---|
| 100 Vac ± 15% | 50 Hz ± 2% |
| 115 Vac ± 15% | 50 Hz ± 2% |
| 200 Vac ± 15% | 50 Hz ± 2% |
| 215 Vac ± 15% | 50 Hz ± 2% |
| 230 Vac ± 15% | 50 Hz ± 2% |
| 120 Vac ± 15% | 60 Hz ± 2% |
| 240 Vac ± 15% | 60 Hz ± 2% |

The 705B supply includes a primary autotransformer to supply 5A at 120 Vac, regardless of any line voltage fluctuations.

Logic Power: The dc-output voltages, as stated below, must be maintained under the following conditions:

Line variations of ± 15% of nominal line voltage.
Load variations of 1/2-load to full load.
Line frequency variations of ± 2% nominal line frequency.

| | | | |
|---|---|---|---|
| Output Voltages: | +10 Vdc | I (max) | 3.5A |
| | | Regulation | +9.4 Vdc to +11.0 Vdc |
| | | Ripple (max) | 300 mV |
| | -15 Vdc | I (max) | 24A |
| | | Regulation | -14.5 Vdc to -16 Vdc |
| | | Ripple (max) | 700 mV |
| Two Floating 10 Vdc: | Each | I (max) | 4A |
| | | Regulation | 9.4 Vdc to 11.0 Vdc |
| | | Ripple (max) | 300 mV |

Under loss of power for 25 ms, the various output dc-voltage drops are as follows:

| | |
|---|---|
| +10 Vdc | 1V |
| ±19 Vdc | 1V |
| -15 Vdc | 2.5V |

Input Surge Current Under Full Load:
7.5A at 120 Vac, 60-Hz input

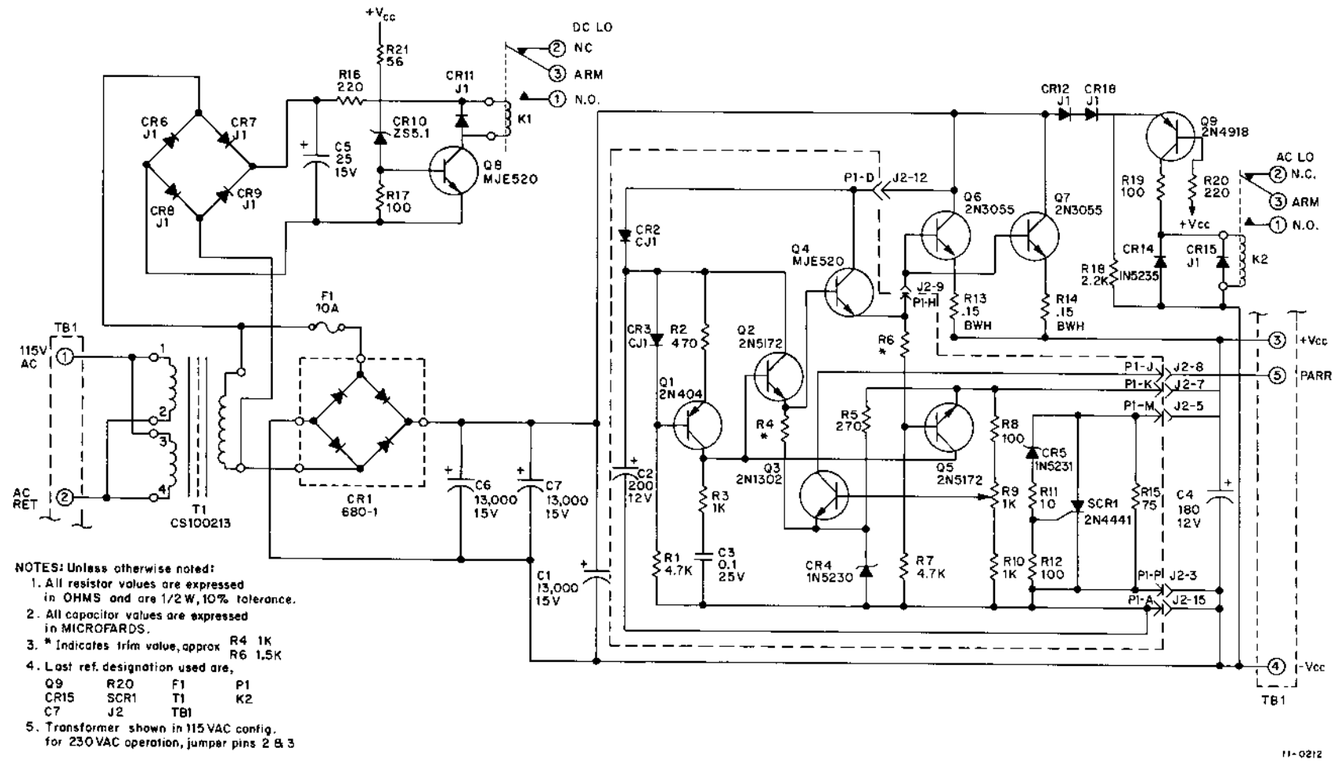
Recurrent Peak Current Input:
5.0A at 120 Vac, 60-Hz input

### 5.7.2 716 Indicator Supply

The 716 Indicator Supply is designed to be used with the indicator panel (see drawing B-CS-716-B-1). Its output is between 7 and 9 Vdc at 4.5A (black and orange terminals). An ac-signal source is also supplied at the white and blue terminals. Neither terminal should be grounded. This signal can be used as a clock or trigger for a synchronizing system.

### 5.7.3 H726A-2 Power Supply

The H726A-2 Power Supply (Figure 5-23) provides the logic power necessary for the RF11 Control. Its output is 5 Vdc at 7A continuous. Load regulation is ± 0.5% maximum and ripple and noise is 5 mV rms maximum at any LOAD and LINE Voltage in specification. The output has overvoltage protection with a crowbar type circuitry which takes effect whenever the output voltage reaches 6.5V ± 0.5V for more than 3.5 μs. In addition, there are two power-fail outputs (AC LO and DC LO) that can be used by the PDP-11 Processor. Input voltage is rated at 105–125 Vac or 210–250 Vac, 47 to 500 Hz.




NOTES: Unless otherwise noted:

1. All resistor values are expressed in OHMS and are 1/2 W, 10% tolerance.
2. All capacitor values are expressed in MICROFARDS.
3. * Indicates trim value, approx R4 1K, R6 1.5K
4. Last ref. designation used are,

| | | | |
|---|---|---|---|
| Q9 | R20 | F1 | P1 |
| CR15 | SCR1 | T1 | K2 |
| C7 | J2 | TB1 | |

5. Transformer shown in 115 VAC config. for 230 VAC operation, jumper pins 2 & 3

Figure 5-23 H726-E Power Supply, Circuit Schematic

# CHAPTER 6
# RF11/RS11 INSTALLATION

## 6.1 INTRODUCTION

RF11/RS11 System installation consists of procedures and requirements necessary to achieve operational status. Operational status is achieved through system configuration and installation planning, procedures, and testing.

## 6.2 SYSTEM CONFIGURATION

The RF11/RS11 System configuration depends on the number of RS11 Disk units to be used in a particular system. Figure 6-1 illustrates the equipment housing for up to a maximum of eight disks. The only options available on the system are additional RS11 disks. Each RF11 Control handles a maximum of eight RS11 disks. The initial one or two RS11 Disks are housed in the master cabinet with the RF11 Controller. Additional disks are then housed in up to two more cabinets depending on the number of RS11 Disks used. (Table 6-1 lists the disk options and their definitions.) In addition, the master cabinet houses the system's power supplies, line filter, the disk motor controls, and purge blowers for the master cabinet's equipment. The other two possible cabinets contain the disk motor controls and purge blowers for their respective RS11 Disk units. Cabinets and hardware required to make extra disks operational are supplied as part of the RS11 being added. The disk cabinets are dedicated cabinets; that is, no peripheral may be installed in unused space in any RF11/RS11 cabinet. Failure to observe this rule may result in lower disk reliability.

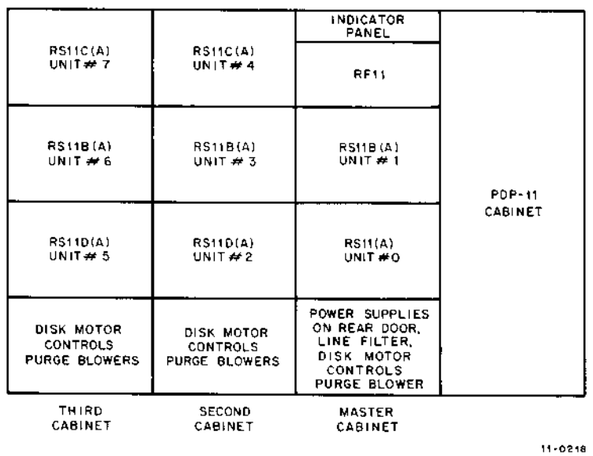



Figure 6-1 System Configuration

Table 6-1
Disk Options

| Option | Definition |
|---|---|
| RF11 | DECdisk control for RS11 Disks. Used on the PDP-11. |
| RS11 | 262K 16-bit 60-Hz DECdisk with a 19-in. cabinet. Used with the RF11 Control it is the first disk in the first cabinet. |
| RS11A | A 50-Hz RS11. |
| RS11B | The second 60-Hz DECdisk in the cabinet which mounts directly above the RS11 or RS11D. |
| RS11BA | A 50-Hz RS11B. |
| RS11C | The third 60-Hz DECdisk in the second or third cabinet which mounts directly above the RS09B. |
| RS11CA | A 50-Hz RS11C. |
| RS11D | 262K 16-bit 60-Hz DECdisk with a 19-in. cabinet. It is the first disk in the second or third cabinet. |
| RS11DA | A 50-Hz RS11D. |

Example: A 5-disk 60-Hz DECdisk system on a PDP-11 would include:

1 – RF11
1 – RS11
1 – RS11D
2 – RS11B
1 – RS11C

## 6.3 INSTALLATION PLANNING

Installation planning consists of requirements or constraints of the RF11/RS11 System. These consist of space, environmental, power, and cable requirements. Compliance with these requirements ensures proper and efficient installation of the RF11/RS11 System.

### 6.3.1 Power Requirements

Installation power requirements pertain to the power supplies used in the disk system and their installation. Discrete or specific power requirements are listed in Paragraph 1.3. Installation power requirements are on a system level.

The RF11/RS11 Disk System uses three power supplies: the H726A-2, 705B, and 716. A single H726A-2 Power Supply provides +5V power to the RF11 Controller exclusively. In addition, the H726A-2 supply provides power-fail signals which are used in the PDP-11 Processor. The H726A-2s mount behind the indicator panel in the uppermost mounting position in the master cabinet only. One 705B is required to supply -15V to both the RF11 Controller and the disk interface (RS11). In addition, the 705B provides +20V to the read/write amplifiers and +10V bias in the RS11. This power supply system has sufficient power to supply the maximum system of eight RS11 Disk units and is housed on the back door of the system's master cabinet. The 716 Power Supply (not H716) is required to provide power to the indicator panel. This power supply is also located on the back door of the system's master cabinet. See Chapter 5 for a detailed discussion of the power supplies.

The RF11/RS11 System can be operated from either 115 or 230 Vac single-phase, 50- or 60-Hz power. Line voltages must be maintained to within ±10 Vac, and the line frequency should not drift more than 0.1 Hz/s. A constant frequency should be provided for installations with unstable power supplies. Table 6-2 shows the power required for various configurations. The primary power line must terminate in Hubbell wall receptacles (shown in Figure 6-2), or their equivalent, to be compatible with the RF11/RS11 power line Hubbell connector.

**Table 6-2**
**Power Configurations**

| Configuration (Number of Disks) | Number of Cabinets | Current (115 Vac) | | Dissipation | |
|---|---|---|---|---|---|
| | | Start (Amperes) | Run (Amperes) | Heat (Btu/hr) | Power (kW) |
| 1 | 1 | 14.0 | 6.5 | 2550 | 0.75 |
| 2 | 1 | 23.0 | 8.0 | 3140 | 0.92 |
| 3 | 2 | 33.5 | 11.0 | 4310 | 1.27 |
| 4 | 2 | 42.5 | 12.5 | 4900 | 1.44 |
| 5 | 2 | 52.0 | 14.5 | 5690 | 1.75 |
| 6 | 3 | 62.5 | 17.5 | 6860 | 1.01 |
| 7 | 3 | 71.5 | 19.0 | 7450 | 2.18 |
| 8 | 3 | 81.0 | 21.0 | 8230 | 2.42 |

### 6.3.2 Space Requirements

Space requirements depend on the number of cabinets used and the cabinet size. The cabinets are 30 in. by 21-11/16 in. by 71-7/16 in. All cabinets in the RF11/RS11 Disk System are shipped singly or bolted together in pairs (unless otherwise specified). A diagram of the RF11 cabinet is shown in Figure 6-3. With regard to weight distribution, the floor loading weight equals the weight of the cabinet/square inch, since each caster covers approximately 1/4-inch square of floor space. The weights of the system per the number of disks used are listed in Table 6-3.

Two H911 mounting panels are used for the RF11 Controller logic modules. (See Table 6-4 for list of modules, type, and quantity for both the RF11 and RS11.) These panels have a special end plate to provide for +5V, -15V, GND, AC LO, and DC LO connections to the module connector blocks. The indicator panel (a 7006331-13 peripheral indicator panel) is mounted directly above the H911 mounting panels (see Paragraph 6.2.2.3). This indicator panel mounts in the top-most position of a DEC Type H961 equipment cabinet. The two logic panels mount directly below it. Each module row is labeled A, B, C, and D from top to bottom and so referred to in the logic print set (module utilization prints). The RS11 Disk units mount in the location specified by the RS11-0 Unit Assembly. A total of three Type H961 cabinets can be used to contain up to eight RS11 Disk units. Refer to drawing D-AR-RF11-0-28 for the cabinet arrangement.

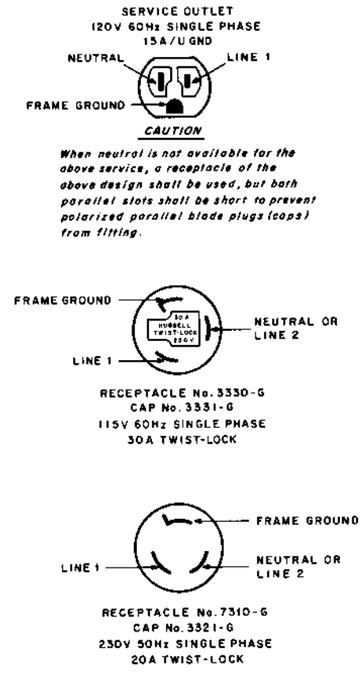



Figure 6-2 Hubbell Wall Receptacle Connector Diagram

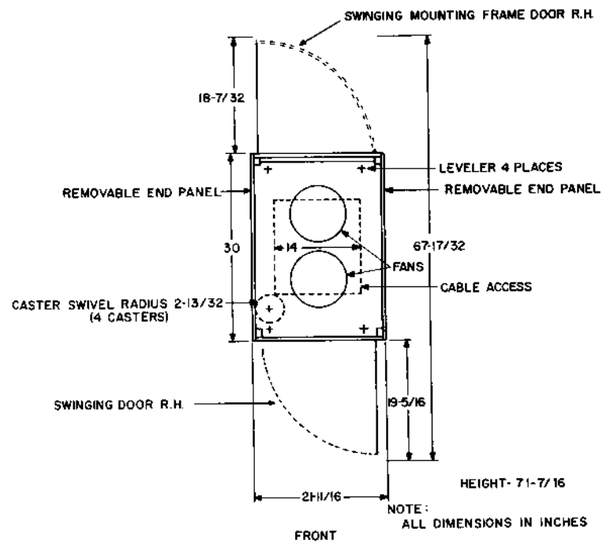



Figure 6-3 The RF11 Cabinet

Table 6-3
Weight Configurations

| Configuration (Number of Disks) | Number of Cabinets | Total Weight (lbs) Crated | Uncrated |
|---|---|---|---|
| 1 | 1 | 590 | 500 |
| 2 | 1 | 690 | 600 |
| 3 | 2 | 1090 | 1000 |
| 4 | 2 | 1190 | 1100 |
| 5 | 2 | 1290 | 1200 |
| 6 | 3 | 1690 | 1600 |
| 7 | 3 | 1790 | 1700 |
| 8 | 3 | 1890 | 1800 |

Table 6-4
Modules Required

| RF11 | | RF11 (cont) | | RS11 | |
|---|---|---|---|---|---|
| Type | Quantity | Type | Quantity | Type | Quantity |
| G711 | 2 | M207 | 1 | B134 | 2 |
| G723 | 3 | M216 | 18 | B152 | 1 |
| G736 | 1 | M302 | 3 | B683 | 3 |
| G740 | 1 | M306 | 3 | G085 | 5 |
| M105 | 1 | M311 | 2 | G285 | 8 |
| M106 | 1 | M500 | 2 | G286 | 4 |
| M111 | 2 | M602 | 1 | G290 | 2 |
| M112 | 3 | M627 | 5 | R002 | 1 |
| M113 | 16 | M632 | 3 | R107 | 1 |
| M115 | 4 | M782 | 1 | R111 | 1 |
| M117 | 4 | M783 | 1 | R602 | 1 |
| M119 | 2 | M784 | 2 | | |
| M121 | 3 | M795 | 1 | | |
| M149 | 4 | M796 | 1 | | |
| M161 | 1 | M797 | 1 | | |
| M204 | 1 | M798 | 1 | | |
| M205 | 6 | | | | |

### 6.3.3 Environmental Requirements

Paragraph 1.3 lists the temperature and humidity requirements for the RF11/RS11 System. In addition, the air should be free of dust and corrosive pollutants, the air pressure should be kept higher than that of adjacent areas to prevent dust infiltration. If air-conditioning is required, the size of the required unit can be calculated from the heat dissipation figures listed in Table 6-2.

### 6.3.4 Cable Requirements

Cable requirements for the RF11/RS11 System pertain to the Unibus cable, the disk bus cable, the indicator panel cable, and the power wiring. The Unibus cable is 10 ft long and is normally supplied with each RF11. (The I/O bus cable, the disk bus cable, and the indicator panel cable are shown in Figure 6-4.) The limiting condition for this cable is the maximum Unibus cable allowed by the processor. The limit for the PDP-11 is 50 ft. This cable is designated BC11A and plugs into slots A01 and B01 of the logic assembly (see engineering drawing D-IC-RF11-0-35). Slots A02 and B02 are reserved for an M930 terminator card if the RF11 is the last device on the Unibus or for the Unibus Out cable to the next device. The In and Out slots are not completely parallel wired, thus making it impossible to interchange their purposes.

A total of 60 ft of cable is required to connect eight disks to a disk control. Systems with greater than five disks must use BC09A cables as the disk bus to reduce the IR drop in the track select lines. The BC09A directly replaces the coaxial cables supplied. Timing considerations and IR drop limit the maximum disk bus using BC09A cables to 75 ft. Four W021–W011 coaxial cables are supplied; these cables connect each RS11 disk to the RF11 Controller or to each other (see engineering drawing D-IC-RF11-0-23). These cables are normally supplied with the RS11 Disk assembly.

The indicator panel cable transfers register bit states and certain flip-flop states to the indicator panel for visual examination. Engineering drawing D-IC-RF11-0-26 shows the indicator cable's terminations with the respective bit or flip-flop names.

The power wiring cabling applies power from the respective power supplies discussed in Paragraph 6.3.1 to the RF11, each RS11, and the indicator panel. Engineering drawing D-IC-RF11-0-27 shows the power application for the entire RF11/RS11 System with the respective termination names and wire colors. Also, power application for up to eight disks (three cabinets) are shown with the respective termination names and wire colors.

## 6.4 INSTALLATION PROCEDURE

Installation of the RF11/RS11 Disk System consists of unpacking the equipment, installing the equipment, and a power turn-on procedure. The system may arrive at the installation site either as a complete system (with RF11/RS11 Disk units, power supplies, indicator panel, and purge blowers mounted in their respective cabinets) or as an add-on system (with RS11 Disk units to be mounted in cabinets already available at the installation site).

### 6.4.1 Cabinet Unpacking

If the equipment arrives in cabinets, use the following procedure to unpack and position the equipment.

| Step | Procedure |
|---|---|
| 1 | Remove the outer shipping container, which may be either heavy corrugated cardboard or plywood. Remove all straps first, and then any fasteners and cleats securing the container to the skid. Remove any wood framing and supports. |
| 2 | Remove the Polyethylene covers from all cabinets. |
| 3 | Remove the tape or plastic shipping pins from the rear access doors. |
| 4 | Unbolt the cabinets from their shipping skids. The bolts can be reached through the rear doors. |
| 5 | Raise the leveling feet so that they are above the level of the roll-around casters. |
| 6 | Form a ramp with wooden blocks and planks from each cabinet skid to the floor, and roll each cabinet down this ramp. |
| 7 | Roll the system to its proper location. |

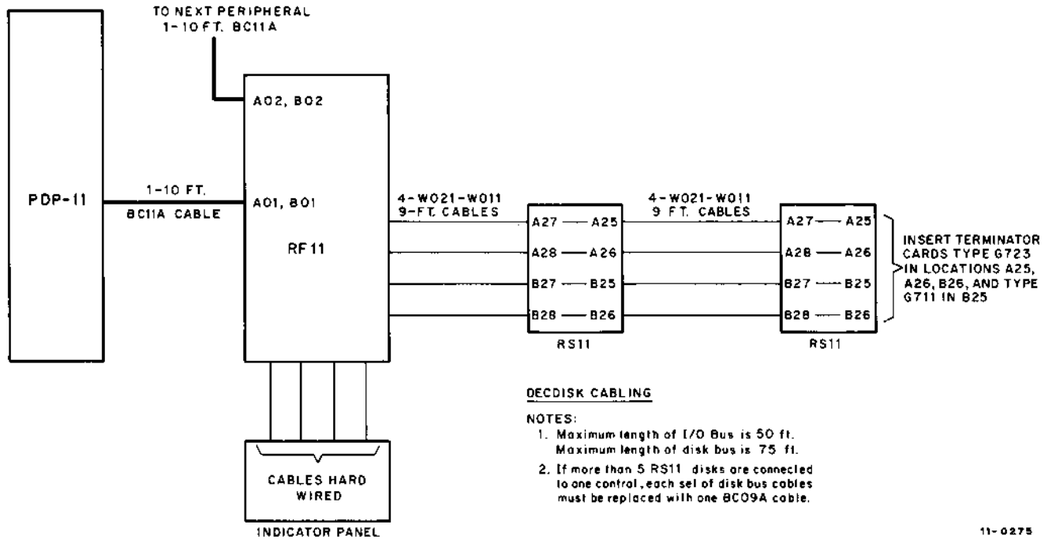



Figure 6-4 RF11/RS11 Disk System

### 6.4.2 Cabinet Installation

The DECdisk cabinets are equipped with roll-around casters and adjustable leveling feet. They do not have to be bolted to the floor. In multiple cabinet installations, cabinets are shipped either individually or in pairs. DECdisk cabinets should be connected together at the site. To install the cabinets, use the following procedure.

| Step | Procedure |
|---|---|
| 1 | Cabinets are joined by filler strips (see Figure 6-5). After the cabinets are positioned, put the cabinets together and bolt both filler strips and cabinets together. Do not tighten the bolts securely. |
| 2 | Lower the leveling feet until they support the cabinet. Using a spirit level, check that all cabinets are level and that the feet are firmly against the floor. |
| 3 | Tighten the bolts that hold the cabinets together and again check the leveling. |
| 4 | Remove the shipping bolts and tape from the slide runners of each disk drive. |
| 5 | Run a ground strap from the DECdisk cabinets to the PDP-11 cabinet. |

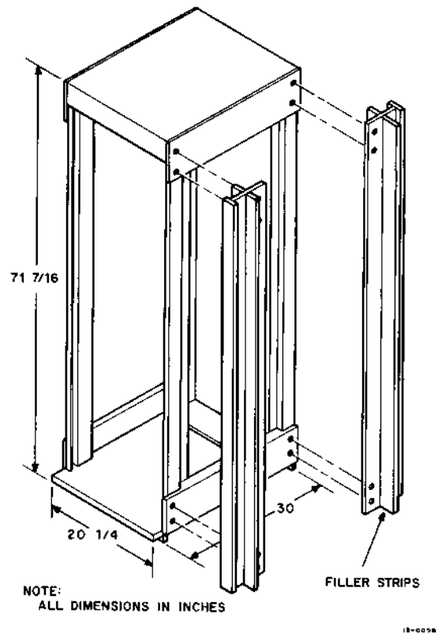



Figure 6-5 Cabinet Bolting Diagram

### 6.4.3 RF11 Controller Installation

The RF11 Controller comes mounted in a cabinet (No. 1) with at least one disk. Three installation steps must be followed.

| Step | Procedure |
|---|---|
| 1 | Remove any tape from the modules and check that existing wiring is not damaged, that hold down bars are in place, and that no modules have fallen out. |
| 2 | Install the Unibus cables in accordance with Figure 6-4. |
| 3 | Connect the ac remote turn-on cable between the computer and the 855 power control unit at the back of the cabinet (see Figure 6-6). Check that the line voltage is correct and that the transformer has been properly wired. (Refer to engineering drawing D-IC-RF11-0-27.) Note that on 220V systems only the 705B and the optional transformer must be wired for 220V. All other accessories are already wired for 115V. Make sure that the circuit breaker on the power control is OFF; then plug the primary power cable into the line voltage receptacle. |

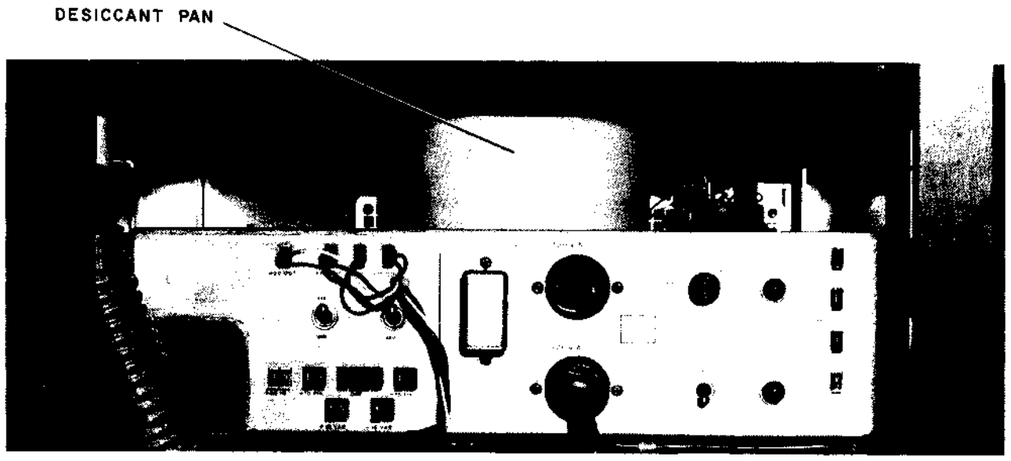



Figure 6-6 The Disk Assembly with Desiccant Pan

### 6.4.4 RS11 Unpacking

When the RS11 is shipped as an addition to an already installed system, it must be unpacked at the site and installed in its prelocated cabinet. The procedure for RS11 unpacking is as follows:

| Step | Procedure |
|---|---|
| 1 | Turn off the system and the 855 circuit breaker. |
| 2 | Remove the disks from their shipping containers and identify each according to its tag number. |
| 3 | Install each disk in its proper position in the cabinet according to Figure 6-1. Cables should be placed toward the front of the cabinet. |
| 4 | Install the disk cable bus according to Figure 6-4. |

### 6.4.5 RS11 Installation

At this point, it is assumed that the disks have been installed in their cabinets either at the site or the factory. For each new disk, perform the following procedures (see Figures 6-6 and 6-7):

| Step | Procedure |
|---|---|
| 1 | Remove the silver cloth tape from the pan containing desiccant (Drierite) and remove the pan from the motor. |
| 2 | Unwrap the blue, green, yellow, red, and black motor leads from the motor. |
| 3 | Connect these wires to the proper color-coded connections on the back of the RS11 motor control chassis. |
| 4 | Remove the motor lock and hold down the bracket. |
| 5 | Turn the motor switches on the back of the RS11 motor control chassis to the OFF position. |
| 6 | Ensure that the circuit breaker on the 855 Power Control is OFF and that the LOCAL, OFF, REMOTE switch is in the OFF position. |
| 7 | Connect the ac- and dc-power wiring in accordance with engineering drawing D-IC-RF11-0-27. |

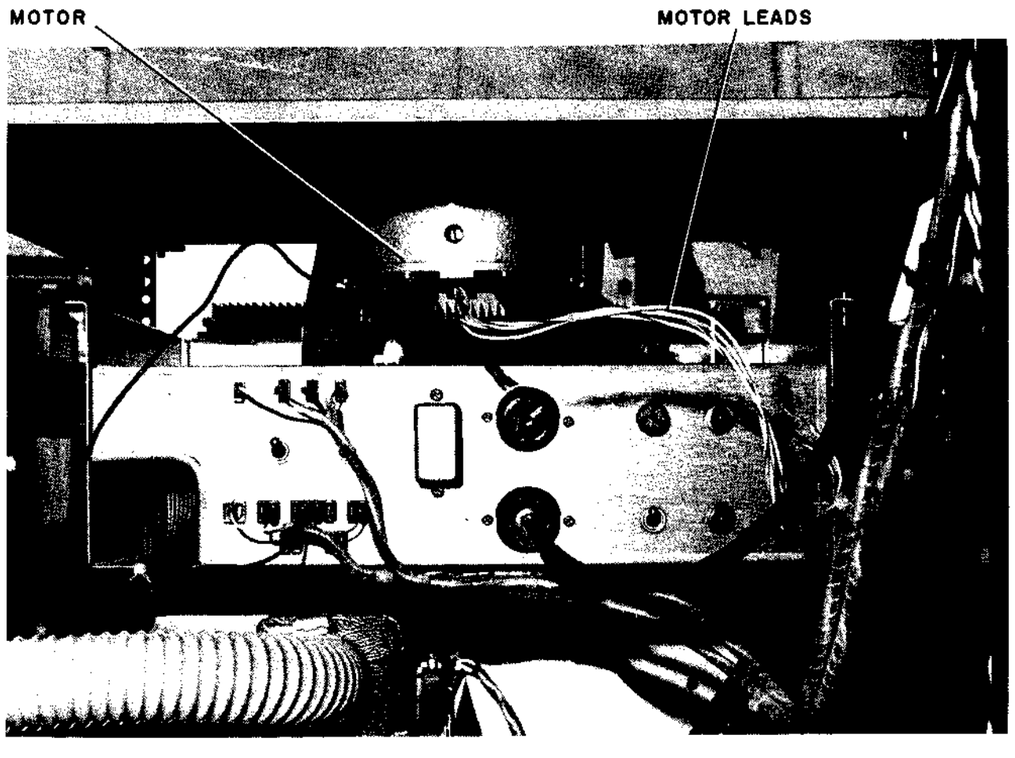



Figure 6-7 Disk Assembly with Pan Removed and Motor Leads Connected

| Step | Procedure |
|---|---|
| 8 | Switch the 855 Power Control circuit breaker to ON. (At this point, the hose on the purge unit has not been connected.) Thus, the purge unit itself is purged, and should continue to be purged for at least 30 min. The disk motor must be off at this time. |
| 9 | After the 30-min purge period, remove the cap from the disk unit and connect the purge unit's hose in the cap's place. |

### 6.4.6 Power-Up Sequence

Before starting the power-up sequence, all wiring should be double checked, the primary ac-power source should be tested for the correct voltage, and the positions of all relevant controls verified. The sequence to be followed to power-up the DECdisk system follows:

| Step | Procedure |
|---|---|
| 1 | Turn off the 855 Circuit Breaker and all power switches on the Disk Control chassis. Turn the REMOTE switch to OFF. Plug in the 855 Power Cord and turn on the circuit breaker. |
| 2 | Turn the DISK POWER switch of the first disk to ON. The START and OPERATE lights should illuminate. The START light should extinguish in approximately 20 s; until it does, the disk is inoperable. |
| 3 | Check that the disk is running and the blower is operating. If any unusual noises are heard, turn off the disk immediately and notify the local DEC office that depot repair is necessary. |
| 4 | Repeat this sequence for each disk. Do not turn on all disks simultaneously, or the surge current may trigger the circuit breaker. Do not attempt to use one disk while turning on another; noise transients can cause interference between disks during turn on. |
| 5 | Turn the REMOTE switch to REMOTE (if system is equipped with Power Fail). |

## 6.5 INSTALLATION TESTING

Installation testing ensures that the RF11/RS11 Disk System has been installed properly and that all equipment is operational. This is accomplished by running the system diagnostics and the system software. Three forms supplied with the system are used for customer acceptance procedures; these forms are:

*a.* The Customer Acceptance Form, in which is recorded any exceptions to normal operation found in the system during the acceptance procedure. Such items should include missing parts, manuals, or engineering drawings.

*b.* The Software Checklist, which catalogues all software that is normally supplied with the system. Each item should be checked off by the customer and the DEC Field Representative.

*c.* The Accessory Checklist, which catalogues all hardware items normally supplied with the system. Each item should be checked off by the customer and the DEC Field Representative.

### 6.5.1 Diagnostics

Three diagnostics are run to determine system operational status. They are:

*a.* Disk Data (MAINDEC 11-D51A), which is a series of address and data reliability routines that verify to the user that the disk controller and disk are operating properly.

*b.* Static Test (MAINDEC 11-D52A), which tests the RS11 logic and the RF11 computer interface. The program accesses and tests all RF11 interface registers, tests for random noise in the RF11, and executes the basic control functions. Both the Disk Data and the Static Test diagnostic instructions and descriptions are covered in the *Disk Data Document* (MAINDEC 11-D50A), supplied with the diagnostics.

*c.* Multi-Disk Test (MAINDEC 11-D5AA), which is a high-speed confidence test that assures the user that he can transfer data correctly without destroying the data on the disk. Multi-Disk uses all available core memory in the system as buffer areas. Included with this diagnostic is its related instruction and description documentation.

The diagnostic tests are covered in relation to their hardware. This discussion, however, is on a maintenance level. Therefore, detailed descriptions, instructions, and a printout can be found in the documentation supplied with the diagnostic tapes. The instructions for diagnostic acceptance of installation are listed below. These instructions should be referenced in the diagnostic documentation.

*a.* Static Test – The entire Static Test must be run for 1/2 hour. No errors are allowed.

*b.* Disk Data Test (Address Tests) – The Address Test section of Disk Data, together with one data pattern, must be run for 1/2 hour. Using the conversation mode:

(1) Reply No to "Data Test Only."

(2) Select Data Pattern No. 7.

(3) Select the standard block length.

(4) Select Write, Read, and Write Check.

No errors are allowed.

*c.* Disk Data (Data Tests) – Using the conversation mode of the Disk Data Test, select the Data Test Only. Use the standard block length and all data patterns (Data Pattern No. 22). The test must be run using Write, Write Check, and Read Modes. The program must be run for 2 passes per disk. Run System's Exerciser program (T-17) D0QC for all devices for 15 min. and GTR for 15 min.

The acceptable error rate is one (1) nonrecoverable error and three (3) recoverable read errors per seven passes (END typeouts) of the disk. Data comparison errors are not allowed. If errors occur, run an additional seven passes to ensure reliability with no duplicate errors allowed.

Definition: A nonrecoverable error may fall into one of the cases listed below:

(1) Any write or write check error is an unrecoverable error.

(2) Two read errors on the same data, consecutive or nonconsecutive, are deemed a nonrecoverable error. See Disk Data Test writeup for error format.

A recoverable error is a read error that occurs only once during the three read attempts.

*d.* Multi-Disk Test – Using the Multi-Disk Test, operate all units available for 1/ hr per RS11. No errors are allowed.

*e.* Power Fail Test – This test is to be run only on controls with power supplies equipped with power fail circuitry.

Using Disk Data Test, run PFT1 and PFT2 tests. Refer to the program writeup for operating procedures and definition of failure. Power fail should be accomplished by turning off the main circuit breaker (see Figure 6-3) in the power control unit.

*f.* Head Amplitude Tests – Check A, B, and C tracks for 6.0V amplitude and 1.1V slice. Check average track for both upper and lower matrices, settings listed on the disk, and 1.1V slice. Report all discrepancies in Field Service Installation Report.

### 6.5.2 System Software

The system is operated using the checkout procedure in the Advanced Software System Checkout Package for bulk storage systems. If the computer system has DECtape, this package includes a complete set of advanced software manuals, a DECtape monitor for RF11 bulk storage, and peripheral routines for bulk storage on DECtape. If the computer system does not have DECtape, the package consists of a complete paper tape advanced software system and a complete set of advanced software manuals.

The successful demonstration of both the diagnostics and the system software constitutes the acceptance procedure. Any discrepancies found must be listed in the Customer Acceptance Form.

# CHAPTER 7
# RF11/RS11 MAINTENANCE

334-1515

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## 7.1 INTRODUCTION

RF11/RS11 Disk System maintenance can be divided into two categories: organizational maintenance and field-level maintenance. These two maintenance areas are distinguished because of the differences in complexity and test equipment required. However, both categories are necessary to maintain the RF11/RS11 Disk System at operational status.

## 7.2 ORGANIZATIONAL MAINTENANCE

Organizational or first-level maintenance refers to maintenance that can be performed on the system at the site without using special test equipment. Organizational maintenance is subdivided into four areas: preventive maintenance, adjustment procedures, changing timing tracks, and diagnostics.

### 7.2.1 Preventive Maintenance

Preventive maintenance includes visual inspection of the DECdisk system according to the list in Table 7-1 and performance of the maintenance tasks listed below.

*a.* The prefilter of the purge unit must be removed and cleaned once each month. The prefilter part number is 7407181 (see Figure 7-1).

*b.* The absolute filter of the purge unit must be replaced every six months. The absolute-filter part number is 12-09388 (see Figure 7-1).

**Table 7-1**
**Visual Inspection Checklist**

| Item | Check |
|---|---|
| Mechanical Connections | *a.* Check that all screws are tight and that all mechanical assemblies are secure.<br>*b.* Check that all crimped lugs are secure and that all lugs are properly inserted in their mating connectors. |
| Wiring and Cables | *a.* Check all wiring and cables for breaks, cuts, frayed leads, or missing lugs. Check wire wraps for broken or missing pins.<br>*b.* Check that no wires or cables are strained in their normal positions or have severe kinks. Check that cables do not interfere with doors, and that they do not chafe when doors are opened and closed. |

**Table 7-1 (Cont)**
**Visual Inspection Checklist**

| Item | Check |
|---|---|
| Air Filters | Check all air filters for cleanliness and normal air movement through cabinets. Check the purge unit and purge hose for cracks. |
| Modules and Components | Check that all modules are properly seated. Look for areas of discoloration on all exposed surfaces. Check all exposed capacitors for signs of discoloration, leakage, or corrosion. Check power supply capacitors for bulges. |
| Indicators and Switches | Check all indicators and switches for tightness. Check for cracks, discoloration, or other visual defects. |

### 7.2.2 RS11 Maintenance Adjustments

The RS11 maintenance adjustments are those of the RS11 Read Amplifiers. To perform these adjustments or calibrations, the following equipment and documentation are required: a Tektronix 547 oscilloscope or equivalent, complete with two 10X probes; and the Disk Data Test program, complete with tape, listing, and writeup. The RS11 Read Amplifier adjustment procedure is listed below.

#### 7.2.2.1 Read Amplifier Adjustment Procedure –

| Step | Procedure |
|---|---|
| 1 | Turn system power on and load the Disk Data Test program. Refer to the program writeup for instructions on loading and starting locations for each test section. |
| 2 | Using conversation mode write a 52525 pattern on the entire disk. Pattern #10 |
| 3 | Start the STAMP section of the program and select the correct disk address from the processor switch register. Table 7-2 indicates the corresponding bit positions. |
| 4 | Adjust the three timing-track read amplifiers for 6V mean gain and 1.1V slice. Refer to Paragraph 7.2.2.2 for the correct method of making these adjustments. The location of the timing track read amplifiers in the RS11 logic rack is as follows:<br>*a.* ATT – G085 module in A02 – B02<br>*b.* BTT – G085 module in A03 – B03<br>*c.* CTT – G085 module in A04 – B04 |

(continued on next page)

| Step | Procedure |
|---|---|
| 5 | Adjust the two data read amplifiers for the average peak-to-peak gain indicated by the tag on the front of the disk enclosure. The average track for each matrix must be selected by the processor switch register for each adjustment. Set the slice at 1.1V. Refer to Paragraph 7.2.2.2 for the correct method of making these adjustments. The location of the data read amplifiers in the RS11 logic rack is as follows:<br>*a.* Lower Matrix – G085 module in A05 – B05<br>*b.* Upper Matrix – G085 modules in A07 – B07 |

**Table 7-2**
**Processor Register Bit Positions**

| Register | Bit Positions | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| CP Switch | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| Disk Address | DA2 | DA1 | DA0 | | | | | | | |
| Track Address | – | – | – | TA06 | TA05 | TA04 | TA03 | TA02 | TA01 | TA00 |

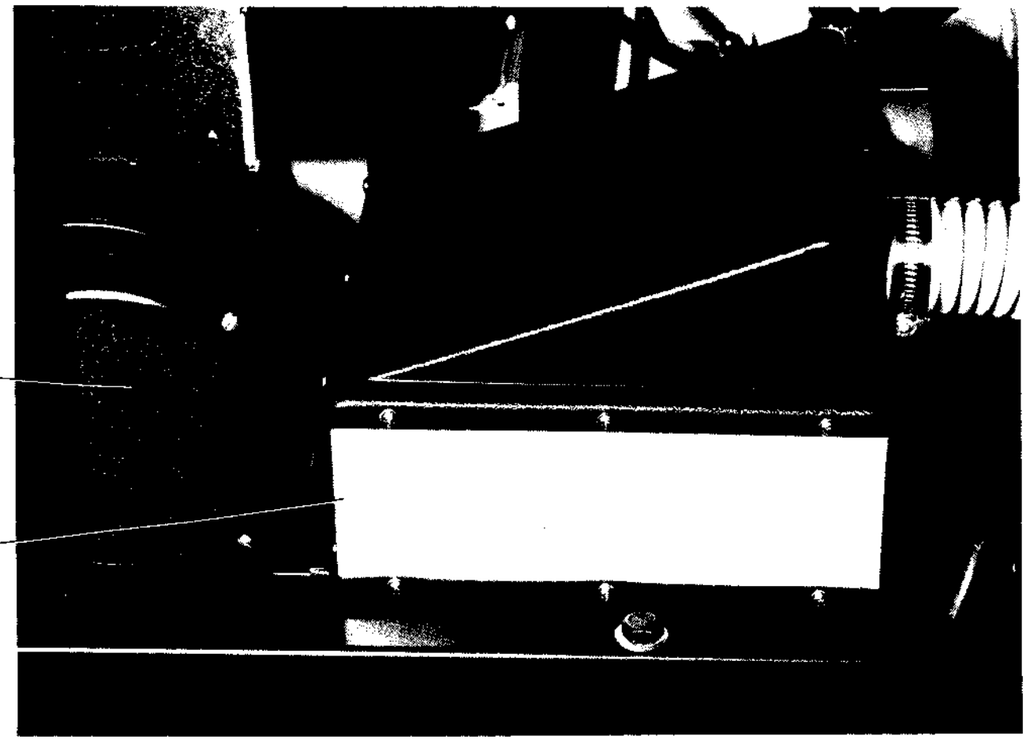



Figure 7-1 Purge Unit and Filters

7.2.2.2 G085 Adjustment –

**CAUTION**

**All probes and oscilloscopes must be calibrated and compensated before making any adjustments. A ground strap should be connected from the oscilloscope to the RS11 chassis. The oscilloscope should be plugged into the 855 Power Control in the the rear of the first disk cabinet.**

To initiate G085 adjustment, place Channel A oscilloscope probe on the signal output of G085 pin A–T and the the ground strap on pin A–C. For Channel B, place the oscilloscope probe on the slice output of the G085 pin B–E and the ground strap on pin B–C. The following steps list the procedures for gain adjustment and slice adjustment.

**Gain Adjustment**

| Step | Procedure |
|---|---|
| 1 | Set oscilloscope time base to 5 ms/cm and trigger on line. Set input switch to dc and mode to CH-1. |
| 2 | Point A is lowest point (smallest peak-to-peak value). Point B is highest point (largest peak-to-peak value). |
| 3 | Place point A on a reference line and the number of centimeters between point A and point B times V/cm is the average peak-to-peak voltage (see Figure 7-2) for this signal. Adjust the potentiometer located on the A section of the G085 Module for the desired value. |

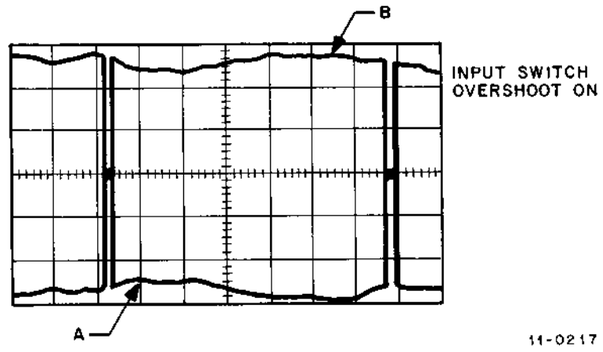



Figure 7-2 Average Gain Measurement

**Slice Adjustment**

| Step | Procedure |
|---|---|
| 1 | Set oscilloscope trigger to Internal, input switch to dc, and mode to CH-2. Measure the overshoot on slice output (see Figure 7-3) and record this value. Overshoot is the amount of signal above the positive level. |

(continued on next page)

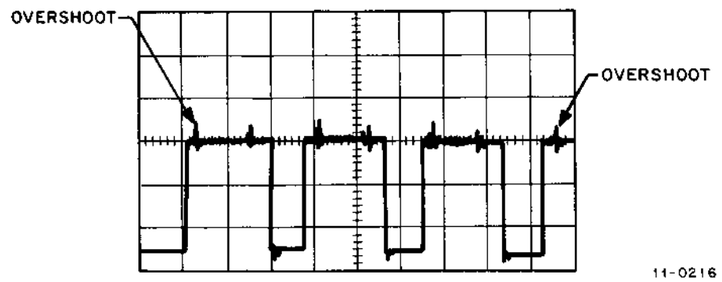
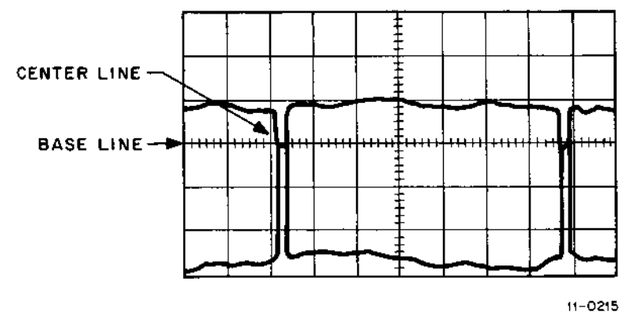



Figure 7-3 Slice Overshoot

| Step | Procedure |
|---|---|
| 2 | Set oscilloscope trigger to line, time base to 5 ms/cm, and mode to ADD. Add the two signals together on a 1V/cm scale and set center line on the base line (see Figure 7-4). |




Figue 7-4 Average Slice Measurement

| Step | Procedure |
|---|---|
| 3 | Decrease the time base and read the amplitude of points A and B (see Figure 7-5). Subtract the overshoot found in Step 1 from point B and calculate the slice voltage. |

$$\text{Slice Setting} = \frac{A + B - \text{Overshoot}}{2}$$

Set the slice to 1.1V by adjusting the potentiometer on the B section of the G085 Module.

### 7.2.3 Changing The Timing Tracks

An extra set of timing tracks is always recorded on the disk. This set is to be used if the first set is accidentally erased in the field. To bring the second set into operation, reverse the timing track head cable connector at the RS11 electronics, slot A01. (The gain settings on the A, B, and C tracks should be recalibrated.) This procedure disconnects the damaged tracks and connects the spares. If the spares are also damaged, the timing tracks must both be rewritten, using the timing Track Writer explained in Paragraph 7.3.2.5.

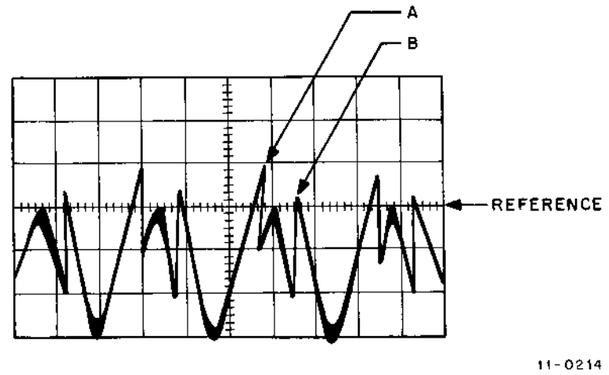



Figure 7-5 Slice Measurement

A view of the RS11 electronics with posted data is shown in Figure 7-6.

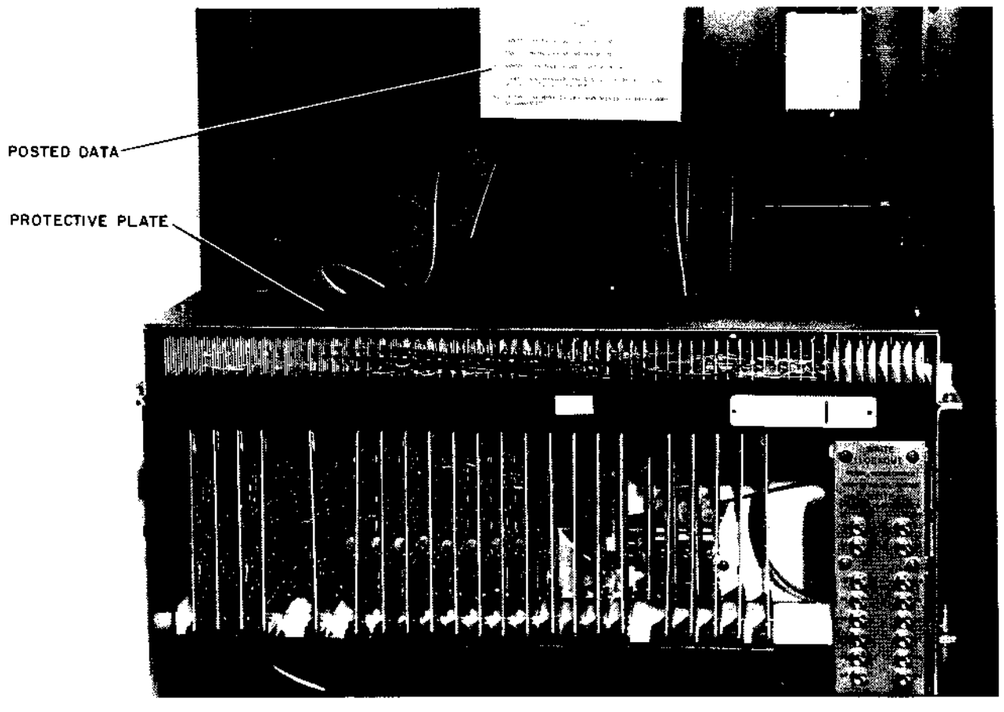



Figure 7-6 RS11 Electronics Showing Posted Data

### 7.2.4 Diagnostics

The three diagnostics, listed with their instructions in Paragraph 6.5.1, are also run as part of organizational field maintenance, to verify that the system is operating properly, or to locate faults. These programs are provided with the system, along with complete descriptions of how they are used.

## 7.3 FIELD-LEVEL MAINTENANCE

Field- or second-level maintenance includes complex work performed on the system using special repair kits and diagnostics. Only qualified DEC field engineers, with the necessary special-service equipment, should attempt to perform the following procedures. Field-level maintenance consists of on-line check, disk assembly repairs, and RS11 calibration. These maintenance procedures are performed for problems that occur in the RF11 or RS11 that cannot be solved using the procedures listed in Paragraph 7.2.

### 7.3.1 On-Line Check

The On-Line Check for the RF11/RS11 System is an operational test to determine if the system is installed properly and ready to function. The following equipment and documentation are required to perform the On-Line Check: PDP-11; Tektronix 547 oscilloscope or equivalent, complete with three 10X probes; Disk Static Test program, complete with tape, listing, and writeup; Disk Data Test program, complete with tape, listing, and write-up; and Multi-Disk program, complete with tape, listing, and write-up. The following steps are taken to perform the On-Line Check:

| Step | Procedure |
|---|---|
| 1 | Check that the Unibus connects from the processor to locations A01 – B01 of the RF11 Controller, and that the M930 terminator card is in locations A02 – B02. |
| 2 | Check that the three G723 terminator cards are in slots A25, A26, and B26 of the last RS11 Disk logic. Check that the G711 terminator card is in location B25 of the RS11. |
| 3 | Check that the disk bus cables connect as follows:<br>RS11 RF11<br>*a.* W011 – A27 to W021 – C31<br>*b.* W011 – A29 to W021 – C32<br>*c.* W011 – B27 to W021 – D31<br>*d.* W011 – B28 to W021 – D32 |
| 4 | Turn disk control power on (if not controlled by the processor). |
| 5 | Turn processor power on and load the Static Test diagnostic. Refer to the diagnostic program writeup for details. |
| 6 | The following is the adjustment of delays in the disk control. I/O STR-1 and I/O STR-2 are the only adjustable delays in the control. They may be adjusted as follows:<br>*a.* Load Address at 200, start, and then halt.<br>*b.* Load Address at 370<br>*c.* Set bit 11 to 1 in the Switch Register. |



| Step | Procedure |
|---|---|
| 6 (cont) | *d.* Depress START.<br>*e.* Connect oscilloscope probe to A19F1. Trigger on A channel with positive trigger slope.<br>*f.* Adjust bottom potentiometer on M302 module in location C10 for a 250-ns pulse.<br>*g.* Connect oscilloscope probe to A25J2. Trigger on A channel with positive trigger slope.<br>*h.* Adjust upper potentiometer on the M302 module on location C10 for a 300-ns pulse. |
| 7 | All other delays in the Disk Control are preset. The diagnostic program does not check delays; therefore, it is necessary to manually verify that they are operational and within reasonable limits. Failure to verify these delays may result in a marginal system. Table 7-3 lists the section of the Static Test program to be used, the pins to check, and the limits expected.<br>**NOTE**<br>**Before selecting the program sections specified, it is necessary to start the program at location 200 and halt. Set bit 11 in the Switch Register to loop on test.** |

(continued on next page)

**Table 7-3**
**On-Line Static Program Requirements**

| Delay | Program Section | Sync + Channel A | Check Channel B | Limits |
|---|---|---|---|---|
| ATP Noise Suppressor | STAI 17 | D24F2 | – – – | 1.2 μs ±20% |
| ATN Noise Suppressor | STAI 17 | D24T2 | – – – | 1.2 μs ±20% |
| DR DLY | STAI 22 | C19E1 | D13T2 | 5 μs ±20% |
| RD DIS | STAI 25 | B24R2 | C11T2 | 200 μs ±20% |
| PSLER | STAI 20 | A23F1 | A26T2 | 1.5 μs ±20% |
| SEQER | STAI 77 | B22U1 | A26F2 | 500 μs ±20% |
| NEM | NXMTSM | B07N1 | B07K1 | ⩾ 20 μs |
| NPC STR-1 | STA 114 | B07R2 | – – – | ⩾ 150 ns |
| NPC STR-2 | STA 114 | B07M2 | – – – | 300 ns ±20% |
| MXF | STA 103 | B28B1 | A27V2 | 130 ms ±20% |

**NOTE**
**For verification of MXF Delay it is necessary to ground pin A27–A1 by placing a jumper from it to A27–C2. To delete error typeout, set bit 14 in the Switch Register to 1.**

| Step | Procedure |
|---|---|
| 8 | Start the Disk Static Test program and follow all steps outlined in its diagnostic writeup. The control should allow the program to sequence through all tests without an error. Five passes should be run. |
| 9 | On completing the Disk Static Test, load and start the Disk Data program. Operating instructions are included in the program writeup. Refer to the acceptance procedure section of the writeup for the acceptable error rate. |
| 10 | Load and run five passes of the Multi-Disk program signified by End typeouts. The control should allow no errors with this program. When the above programs have run satisfactorily, On-Line Check is complete. |

### 7.3.2 Disk Assembly Repairs

The RS11 Disk assemblies are very sensitive devices. The parts of disk assembly that usually require replacement are the shoes and the surface itself. A shoe can be damaged electrically (by a burned out diode or resistor in the disk logic, or mechanically (if the shoe crashes into the surface or breaks a lead from the head to its card). In either case, the assembly must be removed from its cabinet and disassembled. The disk surface may be damaged electrically (by stray fields or accidental currents through the head from a multimeter, for example) or mechanically (by a crashing head). In the first case, the two sets of timing tracks may have to be rewritten with the portable timing track writer designed for this purpose. The assembly does not have to be disassembled for this procedure. The procedure is outlined in Paragraph 7.3.3.5. If the disk surface is damaged mechanically, the surface must be replaced. The assembly must be removed from its cabinet and disassembled. When a new disk is mounted (or even if the old disk is removed and remounted), the timing tracks must be rewritten with the timing track writer. Each time a shoe or a surface is replaced or the disk surface is cleaned, the system must be recalibrated following the procedure given in Paragraph 7.3.3.

**7.3.2.1 Removing the Disk Assembly** – To gain access to the shoes or the disk surface, the disk assembly must be removed from its cabinet and dismantled on its mounting square. The kit shown in Figure 7-7 is provided for this purpose.

Turn off all power to the system and proceed as follows:

| Step | Procedure |
|---|---|
| 1 | Remove power from motor. |
| 2 | Pull the disk electronics out on its rack as shown in Figure 7-8. |
| 3 | Unplug the head cables from the RS11 electronics. |
| 4 | Unplug the purge hose and the motor power leads shown in Figure 7-9. |
| 5 | Remove the four bolts that hold the assembly to its rails. |
| 6 | Pull the disk out of its cabinet and mount it on the mounting square found in the kit. |
| 7 | Remove the twelve mounting screws that hold the cover on. Note that these screws are found along the sides of the assembly. On some disk-assembly versions there are four more screws in each corner that hold the shock mounts in place. Do not remove these screws. |
| 8 | Remove the cover (see Figure 7-10). The cards which hold the shoes are now accessable as shown in Figure 7-11. Be careful not to contaminate the heads or the disk surface itself. |

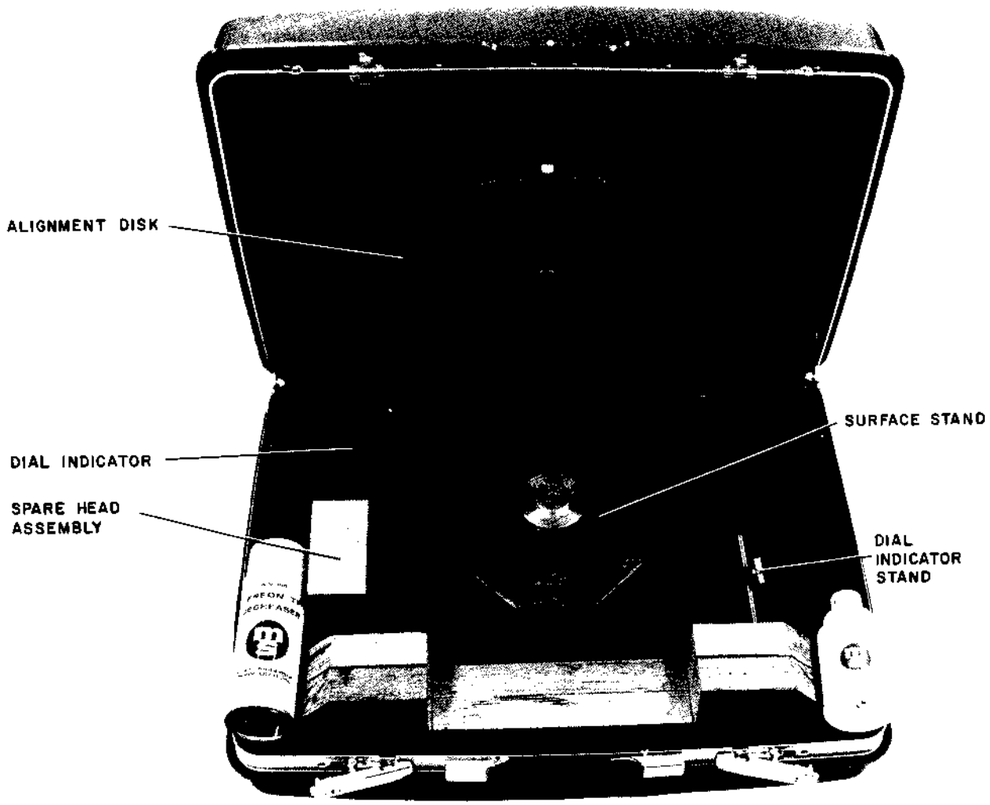



Figure 7-7 Disk Assembly Dismantling Kit

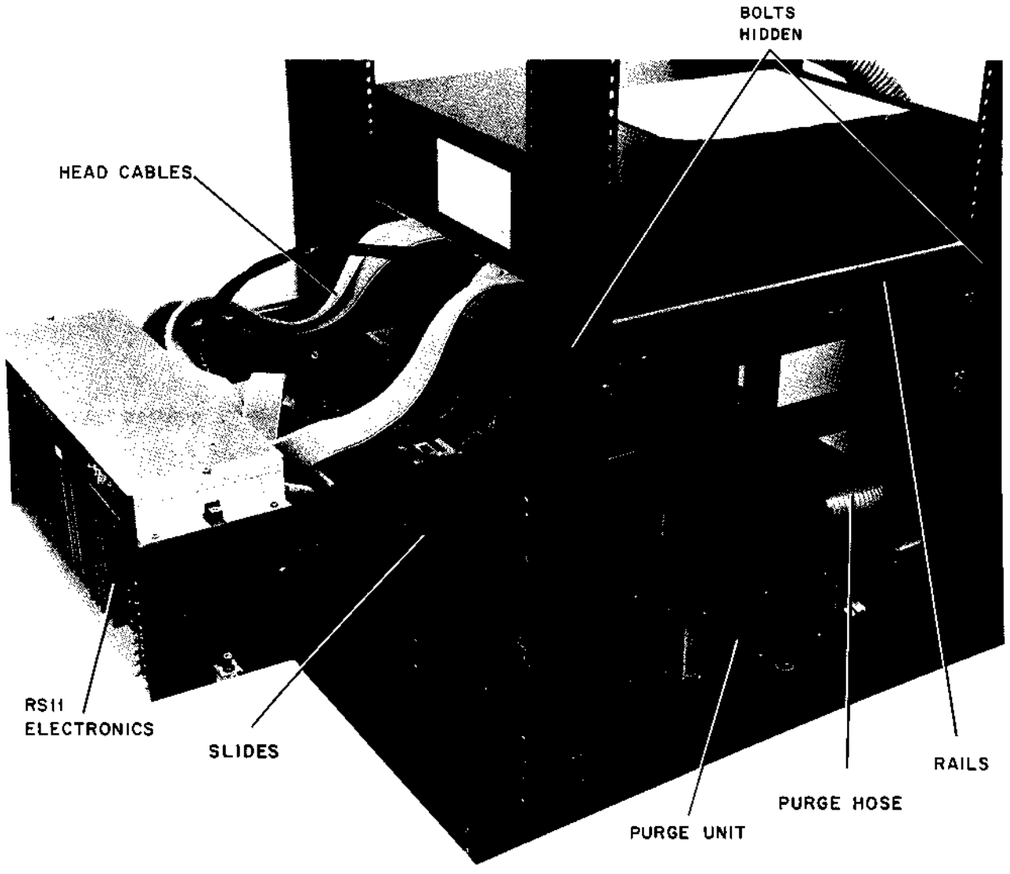



Figure 7-8 Removing the Disk Assembly from the Cabinet

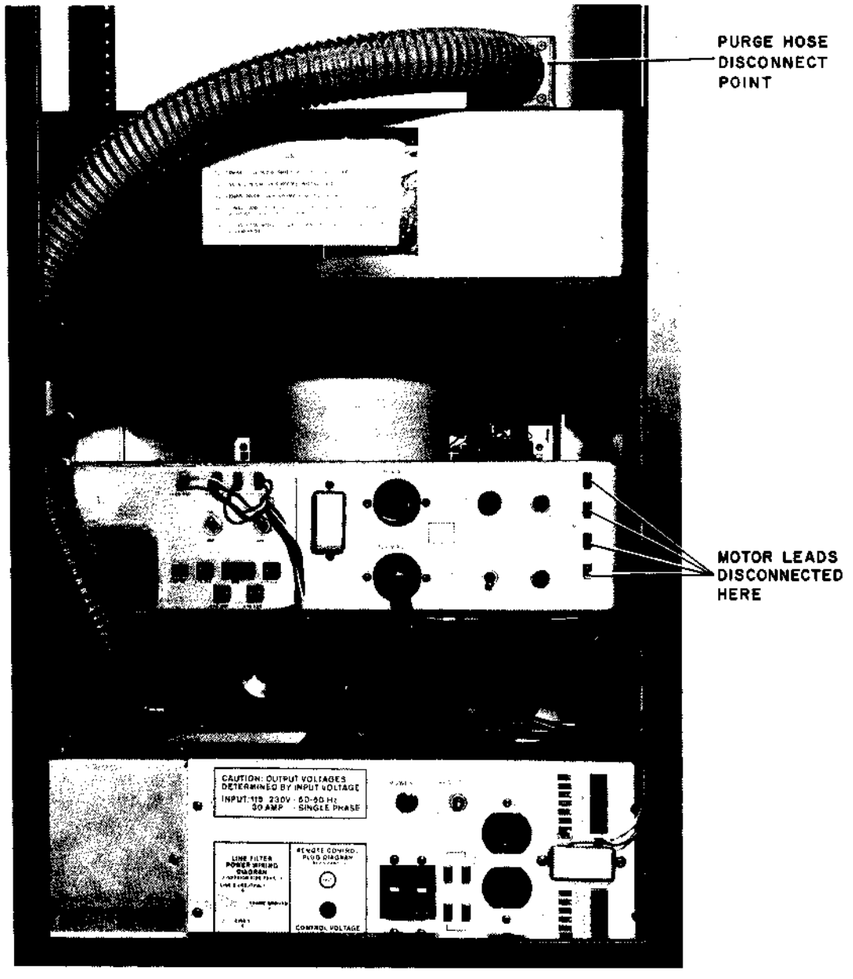



Figure 7-9 Disconnecting Motor Leads and Purge Hose

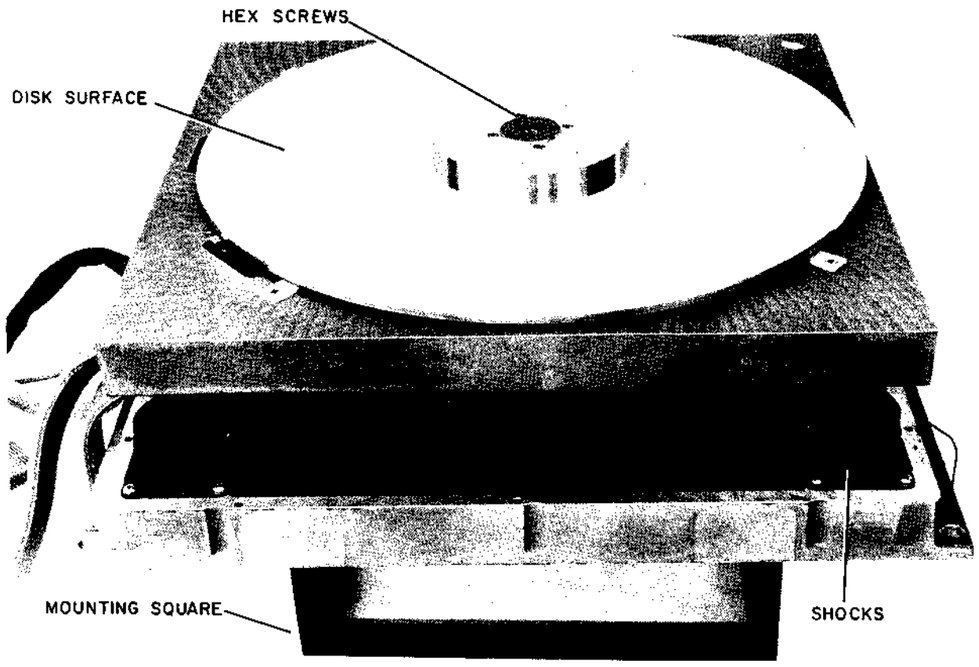



Figure 7-10 Disk Assembly with Cover Removed

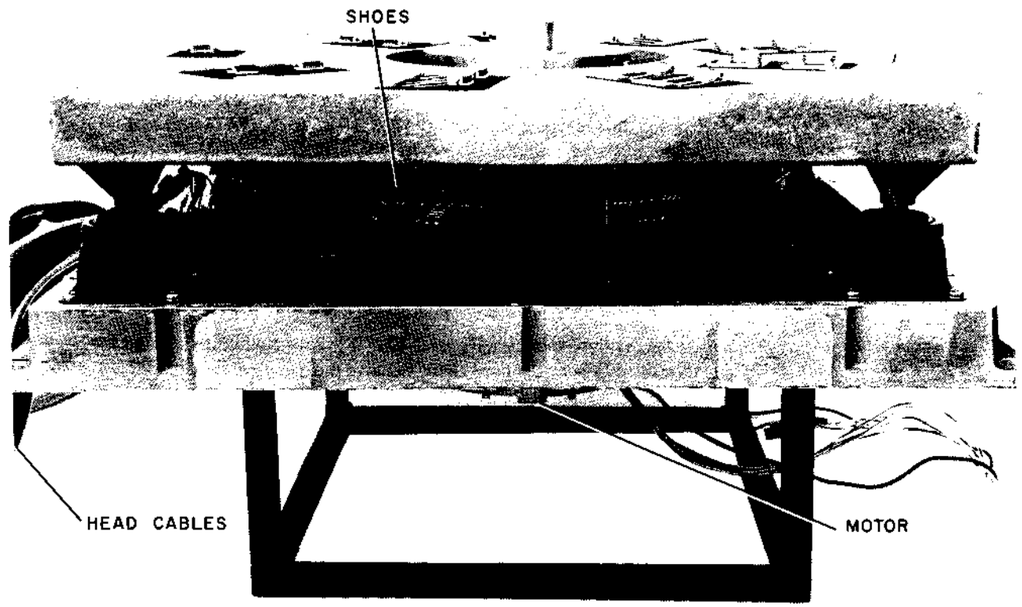



Figure 7-11 Disk Assembly with Cover and Surface Removed

**7.3.2.2 Removing the Disk Surface** – To remove the disk surface, proceed as follows:

| Step | Procedure |
|---|---|
| 1 | Dismantle the assembly, following the instructions of Paragraph 7.3.3.1. |
| | **CAUTION**<br>**Do not turn the disk clockwise while it is in contact with the heads.** |
| 2 | Remove the four hex screws on the disk hub (see Figure 7-10). |
| 3 | Remove the disk surface by lifting it straight up while giving it a slight counterclockwise twist in order to clear the heads. |
| 4 | Note which surface was used. Place the disk on its stand. Be careful that it is not contaminated with dirt. |

**7.3.2.3 Replacing the Shoes** – To replace the shoes, perform the following steps:

| Step | Procedure |
|---|---|
| 1 | Dismantle the assembly according to the instructions in Paragraph 7.3.3.1; then remove the surface using the procedures outlined in Paragraph 7.3.3.2. |
| 2 | Locate the damaged shoe (see Figure 7-12). If it is an inside shoe, the outside shoe must then be removed first. Remove the damaged shoe. |
| 3 | Examine the new shoe. If it must be cleaned, flush it with Methanol spray and blow it dry. If any contaminants remain, saturate a cotton swab with Methanol and carefully wipe the head. Insert the new shoe. |
| 4 | To align the heads, cut out a single layer of Kimwipe approximately 4 in. by 4 in., and lay the Kimwipe over the motor hub to ensure a tight fit for the alignment disk. |
| 5 | Gently fit the alignment disk over the tissue and hub until it is well sealed. Ensure that the heads are seated firmly against the disk. |
| 6 | The outermost track on every pad must be in line with its scribe line on the disk, as shown in Figure 7-13. |
| 7 | Start with the outermost track on pad 0 (see Figure 7-14) and set it so that its inner edge is just touching the inside edge of the outside scribe line. Rotate the motor so that the radial line is over the next pad. Check that its outside track is lined up with the next track on the disk. |
| 8 | If any track is off center, loosen the three mounting screws on the bottom of the block and position it properly. |

**7.3.2.4 Replacing and Cleaning the Disk Surface** – To replace the disk surface, proceed as follows:

| Step | Procedure |
|---|---|
| 1 | Clean the disk surface that is to be replaced with a mild soap and Kimwipes. Do not forget which side is to be used. |
| 2 | Place the platter down on the hub and rotate it slightly counterclockwise. |
| 3 | Check the disk surface with the dial gauge. The disk surface must be flat to within 1 mil through 360°. |

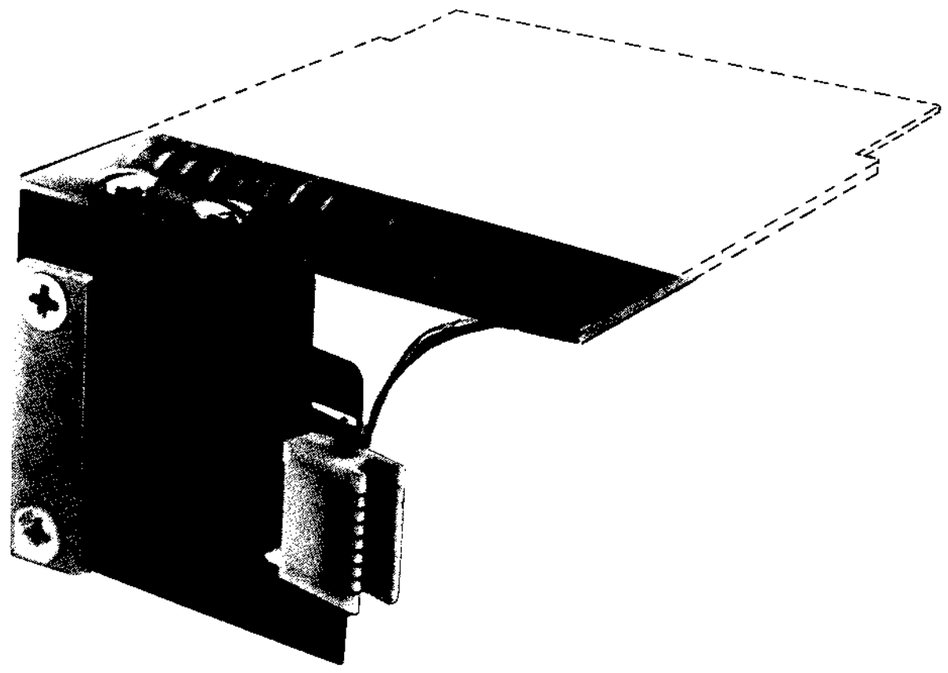


Figure 7-12 Shoe Assembly Removed

| Step | Procedure |
|---|---|
| 4 | Tighten the four hex nuts just enough to lock the washers. |
| 5 | Recheck Step 3. Adjust the hex nut pressure to compensate for any TIR (Total Indicated Runout) that does not meet specifications. |
| 6 | Replace the cover. |

For RS11 cleaning perform the following procedures for DM1 Surfaces: There are two kinds of disk surfaces used. One is the original Techmet surface which is silver and highly polished. The second is a new surface, DM1, generally a dark blue and/or yellowish color. Variations in color and spots need not be of concern.

With the phasing in of a new disk, an entirely new cleaning procedure was developed to resist corrosion and lubricate the surface. Each disk kit (suitcase) will be supplied with enough DEC cleaning fluid and lint free towels to clean one DM1 surface.

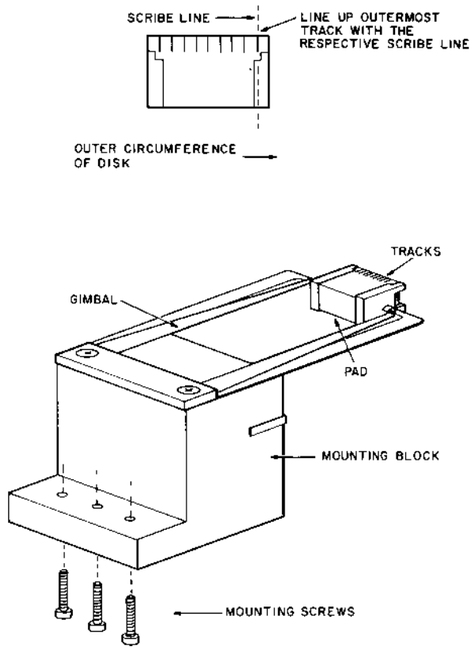


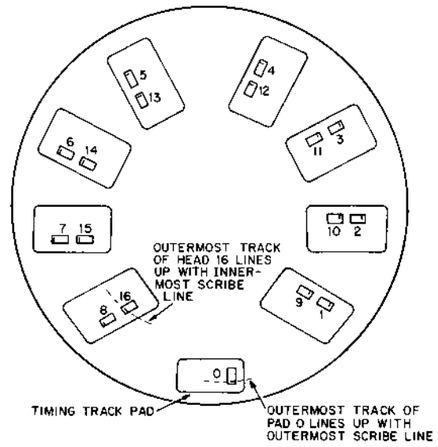

Figure 7-13 Aligning the Heads

**NOTE**

**This cleaning fluid is to be used only on the DM1 surfaces, continue using current procedure on Techmet surface (soap and water).**

The DM1 cleaning procedure is as follows:

| Step | Procedure |
|---|---|
| 1 | Use special DEC cleaning fluid only on DM1 disks. |
| 2 | Mount the disk on a spin stand. Apply DEC cleaner to a clean lab towel and wipe the surface of the disk. Use the clean side of the towel to wipe the disk surface dry. |
| 3 | Apply DEC cleaner to disk surface. Let a thin layer of the solution stand on the disk surface. |
| 4 | After the solvent completely evaporates, take another clean lab towel and start buffing the surface, using clean side of the towel after every few strokes. |
| 5 | Continue buffing using new towels whenever necessary until there is no dark spot or stain on the disk surface. |
| 6 | Wipe the edges of the disk. The disk is now ready to be mounted on the hub. |




NOTE:
The numbering system used to designate pads is only for representation. It is not necessarily the way the pads are actually numbered.

09-0412

Figure 7-14 Aligning the Heads

| Step | Procedure |
|---|---|
| 7 | After mounting the disk, turn it slowly by hand. |
| 8 | If it feels hard to turn, remove the disk and rebuff with dry towels. If the disk is properly buffed, the heads will not stick to the disk. |
| 9 | Reassemble the disk as before. |

**NOTE**

**If the disk surface has not been buffed satisfactorily, the excess DEC cleaner can collect on the Ferrite pads. When reassembling the disk units, the heads must be cleaned and examined in the usual manner.**

DM1 cleaning kits are available in the field. Each suitcase should contain two DM1 cleaning kits along with its present complement of paraphernalia. Each time a DM1 disk is cleaned, discard the used DM1 kit completely and order a new one.

7.3.2.5 **Timing Track Writer** – The timing track writer is the device used in the depot to record the A, B, and C timing and address tracks on the surface of the RS11 disk. The writer is built of M-series modules and mounted in a single H911 panel. It needs no computer and cables directly to the read/write heads of the RS11. This allows the RS11 units to be preformatted before they are checked out (if the heads, disk, and disk drive are functional).

Figure 7-15 is a block diagram of the timing track writer. In RF11 mode, the timing track writer consists of a clock, an 11-bit serial counter, a 5-bit modulo 22 counter, the logic to measure the length of the gap, and the drivers and receiver for the read/write heads. When the clock is enabled by a momentary switch, and the WRITE OFF switch is turned on, equipment operation begins. The disk must be rotating and the writer cabled to it. The counter keeps track of the number of bit cells, the decoding of the correct time when the C track pulses should be written, and the times at which the shift counter should start and stop its shifting. (Refer to engineering drawings D-BS-RS09-TA-1 through -6 for the timing track writer logic.)

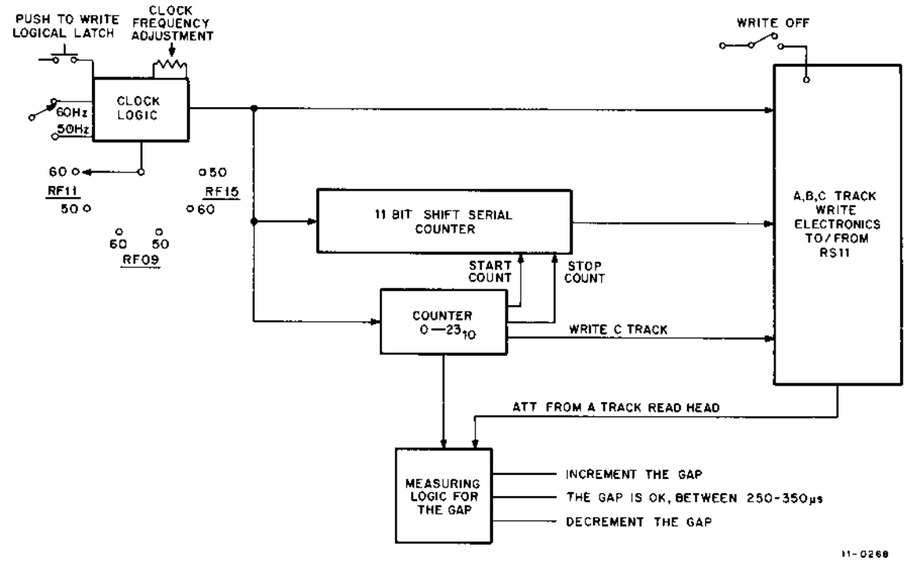



Figure 7-15 Timing Track Writer, Block Diagram

The 11-bit serial counter starts at all zeros and then shifts its contents from the least significant bit onto the B or address track and, at the same time, back into its most significant bit. The counter then automatically increments itself by one for the next address.

Meanwhile, the clock is recording the A or timing track. When the gap comes up at the end of the revolution, the gap-measuring logic examines the time between the last clock bit and the first appearance of an A timing track pulse. If the time is less than 250 μs, a light (INC) flashes on to inform the operator to increase the clock frequency. If the time is greater than 350 μs, light DEC flashes on to inform the operator to decrease the clock frequency. When the clock frequency is set so that the gap lies between 250 and 350 μs, the OK light flashes on, and the operator knows that the disk has been preformatted properly. Both sets of timing are recorded at the same time.

Assume that the WRITE OFF switch is enabled. The PUSH TO WRITE switch (shown in drawing D-BS-RS09-TA-3) triggers a 100-ms delay that times out and issues a CLR (H) to initiate the system. During this delay, the disk is cleared of any timing signals. The CLR H signal clears the WA serial counter and the BC counter (drawing D-BS-RS09-TA-4). It also sets the Write Enable flag (WR EN) which, in turn, enables the M401 Clock. The clock drives a 2-bit ring counter made up of CLK and A CLK flip-flops. These flip-flops provide the main timing pulses for the counters and timing tracks. The two flip-flops are 90° out of phase.

The BC counter begins to count; the level C00 EN is asserted on a count of $21_{10}$, and the next pulse sets C00. C00 also enables the word address portion of the DAR to start writing into the B track by setting WR ADR and gating WA00 to the input of the G290. Meanwhile, the A CLK has been writing timing pulses 720-ns apart onto the A track. The WA serial counter shifts its address; at the same time it serially increments itself by shifting its least significant bit into the CRY flag, detecting the first 0 to appear, and forcing a 1 into the most significant bit at that point. All 1's before this 0 are shifted back as 0's, and all bits after this point are shifted back the way they emerge. The feedback function is the exclusive OR of CRY and WA00. CRY is initialized to a 1, and reset on the first 0 it sees from the WA Register.

When the counter reaches 11, the C11 flag (drawing D-BS-RS09-TA-2) is set and the address writing stops. The flag WR ADR is reset, as is the G290 if an odd parity existed in the address. (This parity is written.)

When the counter reaches $15_{10}$, the C track writing is enabled and the CTP and CTN pulses are recorded. The flag LADR (Last Address) is set when C11 is cleared while CRY is still on a 1. This signifies that the last segment is approaching, i.e., that CRY stayed on through a complete string of 1s for address 3777. When WA01 comes up, at the count of 2 after overflow, the WR CLR flag shown on drawing D-BS-RS09-TA-3 is set by C11 to prepare the logic for the approaching gap. The WR EN flag is cleared on C00, and all writing stops. The R303 delay of print RS09-TA-3 disables the output of the read amplifier until it recovers after writing; when the read amplifier sets, it passes the A track through its reader. At the same time, two M302 delays are also set, and they time out to 250 μs and 350 μs. If the A track passes any timing track pulse before 250 μs are up, the INC flag is set to tell the operator to increase the clock frequency (increase the gap time). If the next A track timing pulse comes between 250 μs and 350 μs, the OK flag is set. The DEC flag sets if the A pulse arrives after 350 μs and the operator should decrease the clock frequency (decrease the gap time). If either INC or DEC occur, the system is cleared out and starts again. Otherwise, the system stops formatting, having completed its job.

When a new surface is installed or a disk surface is cleaned, the timing tracks must be rewritten. This is done with the timing track writer (Figure 7-16) as follows:

| Step | Procedure |
|---|---|
| 1 | Remove the dc voltage from the RS11 logic. This may be accomplished by turning the power off at the power control unit. The ac power to the disk unit and purge unit must remain on. |
| 2 | Remove the timing track cable from the RS11 unit. The cable is located in slot A1 of each RS11. |
| 3 | Remove the cover from the RS09 timing track writer and remove the dc wiring cable from the box. The dc wiring cable contains four wires with HEYCO Tab connectors on the ends. The wires are:<br>*a.* Yellow +20V<br>*b.* Red +10V<br>*c.* Blue -15V<br>*d.* Black GND |

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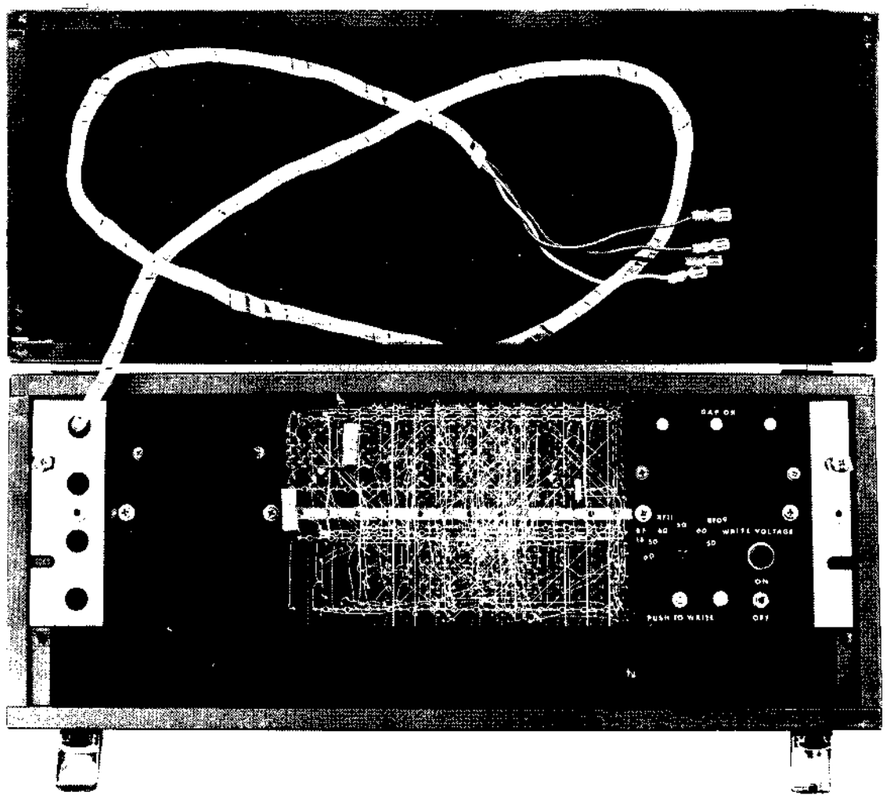



Figure 7-16 Timing Track Writer

| Step | Procedure |
|---|---|
| 3 (cont) | Mount the timing track writer box in the cabinet via the holding pins on the rear of the tester box. These pins should slide into the pre-punched holes in the cabinet frame directly above the RS11 logic. Insert the dc power cable for the timing track writer between the disk unit and the disk logic. The cable will plug into the dc power bus on the rear of the RS11 disk chassis. Insert the individual wires into the proper voltages as indicated on the rear of the RS11 chassis. All wires and tabs are color coded for easy identification. |
| 4 | Insert the timing track cable from the disk into the slot provided in the front of the tester. |

**NOTE**

**This cable is a dual connector and may be plugged in on either side.**

| Step | Procedure |
|---|---|
| 5 | Turn power on. Dc power should now be applied to the RS11 logic as well as the tester. |
| 6 | Select the switch setting for the proper disk motor speed, i.e., RF11 50 or 60 Hz. |

**NOTE**

**Complete Steps 7 through 9 as quickly as possible after turning the Write Voltage switch ON. Failure to do so will damage the head center tap resistors that are inside the disk enclosure.**

| | |
|---|---|
| 7 | Set the WRITE VOLTAGE ENABLE switch on the front panel to the on position. The red indicator light should come on. |
| 8 | Press the WRITE button under the selector switch to begin the actual writing. The timing track writer will automatically recycle if the gap is not correct and will indicate this via a flashing INC (increase) or DEC (decrease) light. Slowly turning the knob in the direction indicated by these lights will result in a properly written timing track and will be indicated via the OK light. Push the WRITE button once more without adjusting the knob. The OK light should come on without flashing either the INC or DEC lights. Minor adjustment may be necessary to meet this requirement. |
| 9 | Set the WRITE VOLTAGE switch to OFF. |
| 10 | Turn dc power off and remove the dc power lines from the tester to the RS11. Timing tracks should now be properly recorded. |
| 11 | Plug the timing track cable from the disk enclosure back into slot A01 of the RS11 logic panel. |

### 7.3.3 RS11 Calibration

If a new surface or new shoes have been installed, calibration must be carried out and recorded on the sheets illustrated in Figure 7-20. The tests include one test to measure surface modulation and several to measure the mean voltage of each matrix and establish an optimum gain for the readers.

**7.3.3.1 Measuring Surface Modulation** – This test is performed on the A track only. Surface modulation is the result of variations in the properties of the surface around the disk. It is measured using the following procedure:

| Step | Procedure |
|---|---|
| 1 | Connect a calibrated oscilloscope probe to pin A02T of the RS11 (A timing track read amplifier). |
| 2 | Connect the oscilloscope ground strap to A02C. |
| 3 | Place the oscilloscope setting on dc. |
| 4 | Trigger the oscilloscope on LINE. |
| 5 | Set the time base to 5 ms/cm. |
| 6 | Measure Vmax pp and Vmin pp, as shown in Figure 7-17. Surface modulation = $\frac{\text{Vmax pp - Vmin pp}}{\text{Vmax pp + Vmin pp}}$ x 100 (surface modulation should be less than 20 percent.) |

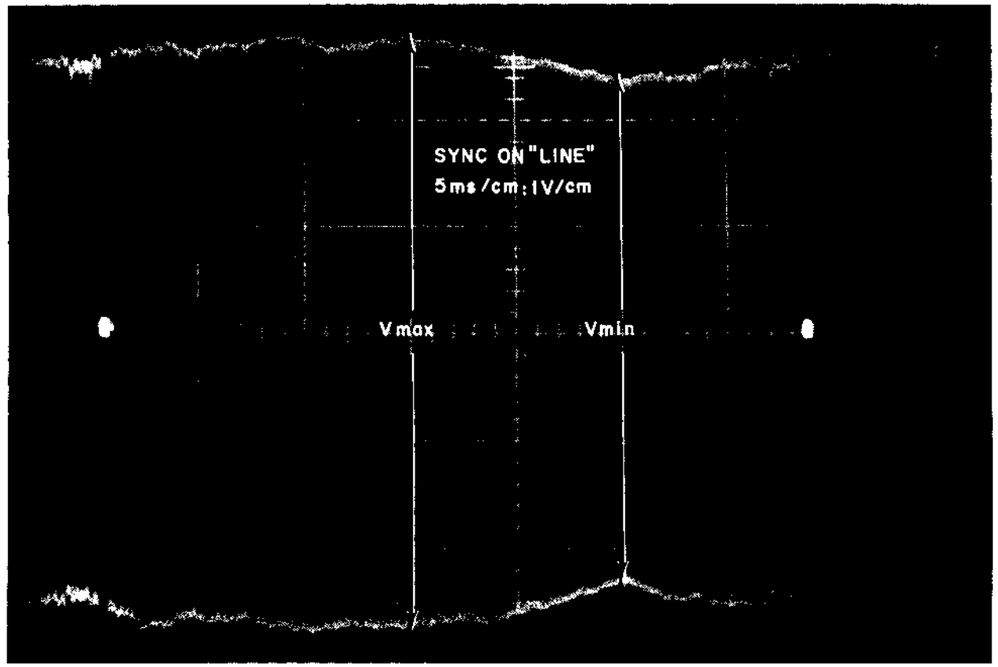



Figure 7-17 Measuring Surface Modulation on the A Track

**7.3.3.2 Analyzing the Gain of the Data Tracks** – When a new disk is installed or the heads are replaced, the A, B, and C track gain and slice must be adjusted (see Paragraph 7.2.2); then the data tracks must be recalibrated. This process involves measuring the mean voltage from each head, the mean value for each shoe, and the percentage deviation for each matrix. The percent deviation is the measure of the difference in the readings. The smaller this value is, the more consistent the readings are in the matrix. To reduce this deviation, the shoe with the lowest reading is given a 20-percent boost in gain and the deviation is recalculated. If the result is a reduction, the reading is given another boost in gain and the deviation is recalculated. This process is continued until adding more gain to the next shoe does not decrease the percentage of deviation. The entire process of gain increase and deviation increase is done on paper recording each reading. When this process is complete, it is repeated with an AGC jumper installed in the RS11 to affect each gain increase. If the percentage of deviation is reduced another jumper is installed and so on until no percentage deviation decrease is affected.

The readings taken during this calibration are recorded on the Head Data sheet. When all the readings have been taken, the average shoe for each matrix is located; its readings are posted on the disk as a calibration standard to set the G085 readers in the future. The procedure to carry this out follows.

**NOTE**

**The arithmetic mean reading for each head (0–177) must be taken and recorded on the Head Data sheet.**



| Step | Procedure |
|---|---|
| 1 | Make sure all AGC jumpers have been removed. |
| 2 | Set the first track gain reading in each matrix to 8.0V by using the procedure given in Paragraph 7.2.2, with track 000 being the lower matrix and track 100 the upper matrix. |
| 3 | Without further adjustment to the read amplifiers (G085), take all the track readings and record them on the RS11 Data Sheet as shown in Figure 7-20, sheet 1.<br><br>**NOTE**<br>**Track $XYZ_8$ is where X = matrix (0 or 1)**<br>**Y = track on each shoe (0–7)**<br>**Z = shoe** |
| 4 | From the previous readings, find the percentage of deviation for each shoe, using the formula:<br><br>$\frac{Vmax - Vmin}{Vmax + Vmin} \times 100 = \%$ deviation<br><br>where: Vmax is the largest mean peak-to-peak voltage taken on that shoe<br>Vmin is the smallest mean peak-to-peak voltage taken on that shoe.<br><br>This value should be less than 20 for any shoe. If it is more than 20, the shoe should be replaced. |
| 5 | Find the mean peak-to-peak voltage for each shoe with the formula:<br><br>$\frac{Vmax + Vmin}{2}$ = A mean; then insert the value on the RS11 data sheet. |
| 6 | From the mean for each shoe, calculate the percentage of deviation for each matrix with the formula:<br><br>$\frac{Amax - Amin}{Amax + Amin} \times 100 = \%$ deviation<br><br>where: Amax = the maximum mean of all shoes<br>Amin = the minimum mean of all shoes<br><br>Attempt to reduce the percentage of deviation by adding 20 percent of the lowest reading to itself. Repeat this for the next lowest reading and check to see if it reduces the result. Continue this procedure until seven shoes have been added to, or the percentage of deviation starts to increase. If the percentage of deviation decreases further when an eighth jumper is added, the computation has been done incorrectly. An average of four jumpers are used. This process is illustrated in the following example:<br><br>**Example**<br><br>**A Mean** **A Mean** **A Mean**<br>0 6.35 (Min) + 20% = 7.62 7.62<br>1 7.21 7.21 (Min) + 20% = 8.65 (Max)<br>2 7.46 7.46 7.47<br>3 8.00 8.00 (Max) 8.00<br>4 7.65 7.65 7.65<br>5 7.40 7.40 7.40 (Min) |

(continued on next page)

| Step | Procedure | | | |
|---|---|---|---|---|
| 6 (cont) | A Mean | | A Mean | A Mean |
| | 6 | 7.65 | 7.65 | 7.65 |
| | 7 | 7.46 | 7.46 | 7.46 |
| | % = | Dev | | |
| | | 11.5 % *(a)* | 5.2 % *(b)* | 7.8 % *(c)* |

Look for minimum % deviation.

*a.* $\frac{8.00 - 6.35}{8.00 + 6.35} \times 100 = \frac{1.65}{14.35} \times 100 = 11.5\%$

*b.* $\%\ \text{Dev} = \frac{0.79}{15.21} = 5.2\%$

*c.* $\%\ \text{Dev} = \frac{1.25}{16.05} \times 100 = 7.8\%$

By increasing shoe 0 by 20 percent, the deviation was reduced to a minimum. In order to effect this increase in gain on this shoe, a jumper must be installed. Table 7-4 indicates the proper jumper for each shoe. In this case, assuming matrix 0 was under test, pin B17M would be jumpered to pin B20D.

7 Example b in step 6 is now the true set of means for the shoes in that matrix. Using these means, calculate the average track from the formula:

$$\frac{\text{Amax} + \text{Amin}}{2} = \text{Average track}$$

Find a track that is within 10 percent of the mean peak-to-peak voltage, but that is not in a shoe that has a gain jumper, and identify it as the average of that matrix. Repeat the procedure for the other matrix. From the example:

$$\frac{8.00 + 7.21}{2} = 7.655$$

Since the track's means are not part of this example, the actual average track cannot be shown. (It is most likely to be in shoe no. 4, however.)

If a track without a gain jumper within 10 percent of the average track cannot be found, multiply the average track value times 5/6 and look for a track in a shoe with a gain jumper that comes within 10 percent of this number. Once a track has been selected, multiply that track value by 6/5 to take oscilloscope readings, then record the readings on the RS11 sheet.

**Table 7-4**
**Jumpers to Increase Gain**

| Shoe No. | Pin | | Matrix 0 Gain | Matrix 1 Gain |
|---|---|---|---|---|
| XX0 | B17M | | B20D | B20K |
| XX1 | B17N | | B20E | B20L |
| XX2 | B17P | | B18D | B18L |
| XX3 | B17R | To Matrix 0 gain | B18E | B18M |
| XX4 | B17S | OR Matrix 1 gain | B18H | B18P |

**Table 7-4 (Cont)**
**Jumpers to Increase Gain**

| Shoe No. | Pin | Matrix 0 Gain | Matrix 1 Gain |
|---|---|---|---|
| XX5 | B17T | B18J | B18R |
| XX6 | B17U | | |
| XX7 | B17V | | |

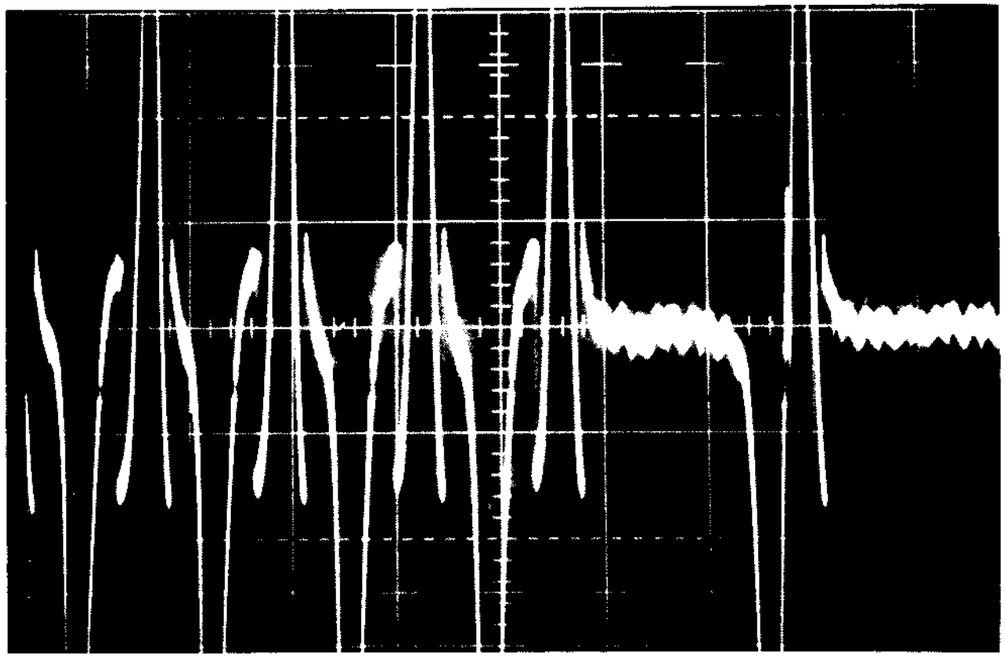
| Step | Procedure |
|---|---|
| 7 (cont) | If seven shoes require gain, run the matrix wire B18V to B18K (Matrix 0) or to B18S (Matrix 1); and add a jumper B18T or B18U. No matrix should ever need more than seven jumpers. |
| 8 | *a.* Using the RS08-M test data sheet that accompanies the RS08-M, list the arithmetic mean (A mean) on the next column after each shoe. |
| | *b.* Star those shoes requiring gain jumpers. |
| | *c.* Circle the track in each matrix used as the reference for the G085 gain adjustment. |
| | *d.* Record each reference track and its respective peak-to-peak voltage setting (computed on the RS11 test data sheet) on both the RS11 test data sheet and the cover of the disk. |

**7.3.3.3 Calibrating the Gain of the Data Readers** -- In the previous paragraph, the optimum configuration for minimum percentage of deviation was established among the shoes. In this paragraph, the optimum gain for each reader is determined; this is done by determining the operating range of the slice-to-gain ratio. The highest operating gain with the smallest operating slice is found; and, conversely, the lowest possible gain with the highest possible slice. When these two ratios are found, the gain is set to the point that lies midway between the two at a normalized slice of 1.1V. Record all readings on the test data sheet of Figure 7-20, sheet 2.

The Disk Data program is used to run optional test patterns. Proceed as follows:

| Step | Procedure |
|---|---|
| 1 | Continuously read and write the optional pattern no. 21 for random data on the entire disk. This is a random data pattern. |
| 2 | Go to Read mode. Set the slice of the first matrix to 1.1V from the average track. Raise the gain of that reader until one failing point occurs while reading entire lower surface. If no failure occurs, leave the gain on maximum and start to lower the slice below 1.1V. When a failure occurs, scope these points and determine the reason for the failure (i.e., look for a drop out). Figure 7-18 illustrates the waveforms. |
| 3 | Repeat Step 2 for the other matrix. |
| 4 | Go to Read mode. Set the slice of the first matrix reader to 1.1V from the average track. Lower the gain of the reader until a failure occurs while reading the entire upper matrix. If there is no failure at the lowest gain, start to raise the slice level above 1.1V until a failure does occur. Scope these points and determine the reason for the failure. Record these readings. Figure 7-19 illustrates the waveforms. |

(continued on next page)



SYNC ON RD SR
2μsec/cm 1V/cm

Figure 7-18 Maximum Gain, Minimum Slice

| Step | Procedure |
|---|---|
| 5 | Repeat Step 4 for the other matrix |
| 6 | Calculate the optimum gain for each reader from these readings. This is done by taking the lowest maximum gain and the highest minimum gain from the two tests, normalizing to 1.1V. and finding the center point between the two gains. |

**Example**

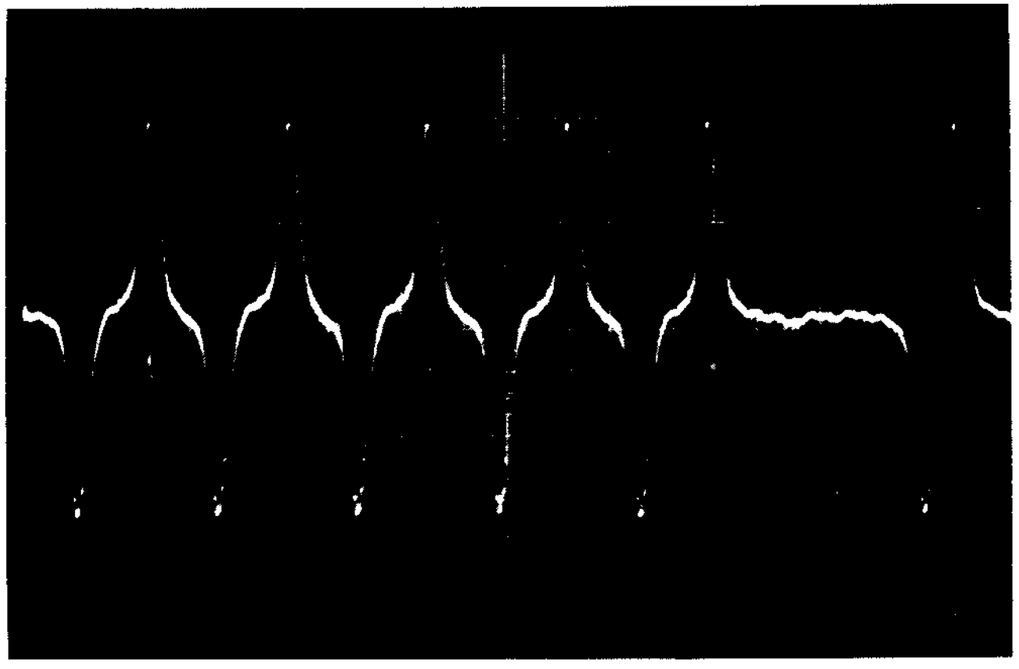
High gain = 14 failed at slice 0.8V

Low gain = 4.8 slice at 4.6V

$$\text{Normalized gain} = \frac{14 \times 1.1}{8} = 19 \text{ for high}$$

$$= \frac{4.8 \times 1.1}{4.6} = 1.15$$

$$\text{Gain setting should be } \frac{19 - 1.15}{2} = 8.9$$



SYNC ON RD SR
10μsec/cm 2V/cm

Figure 7-19 Minimum Gain, Maximum Slice

| Step | Procedure |
|---|---|
| 6 (cont) | The average track should be selected, and its mean peak-to-peak output voltage set at 8.9V. This step should be repeated for the other matrix. |
| 7 | Calculate the Figure of Merit (see Figure 7-20, sheet 2) for the disk. This figure must be better than 40 percent. If the Figure of Merit is less than 40 percent, the disk must be replaced. |

## RS08M DATA SHEET

O = Average Track
* = Gain Added

Date: _____ By: _____ Disk Mfg. & #: 432 Head Tester #: none Motor Freq.: 50 Htz

Scope Type & #: 453 Preamp Type & #: 038518 Type Probes: P6047 X10

| | AGC | Pos. | Grams Per Side | Signal Reading 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | A Mean | After Gain | % Deviation Shoe | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| X | | | | | | | | | | | | | | | |
| 1 | | TT | | | | | | | | | | | | | |
| 2 | * | 0X0 | | 6.2 | 6.4 | 5.9 | 6.0 | 6.6 | 6.8 | 6.7 | 6.6 | 6.35 | 7.62 | | |
| 3 | | 0X1 | | 7.0 | 7.1 | 7.2 | 7.4 | 7.1 | 7.4 | 7.0 | 7.3 | 7.21 | 7.21 | | |
| 4 | | 0X2 | | 6.2 | 6.0 | 7.8 | 7.2 | 7.0 | 7.5 | 7.92 | 6.5 | 7.46 | 7.46 | | |
| 5 | | 0X3 | | 8.0 | 8.5 | 7.5 | 7.0 | 7.2 | (7.6) | 8.8 | 9.0 | 8.0 | 8.0 | | |
| 6 | | 0X4 | | 7.28 | 7.9 | 7.5 | 7.7 | 7.6 | 7.4 | 8.0 | 7.3 | 7.65 | 7.64 | | |
| 7 | | 0X5 | | 6.8 | 6.9 | 7.0 | 6.9 | 6.9 | 7.8 | 7.0 | 7.0 | 7.4 | 7.4 | | |
| 8 | | 0X6 | | 7.0 | 7.2 | 8.3 | 7.1 | 7.3 | 7.1 | 7.2 | 7.0 | 7.65 | 7.65 | | |
| 9 | | 0X7 | | 7.4 | 7.9 | 7.0 | 7.5 | 7.1 | 7.92 | 7.8 | 7.3 | 7.46 | 7.46 | | |
| 10 | | 1X0 | | 6.0 | 5.8 | 5.9 | 5.6 | 6.2 | 5.6 | 5.7 | 5.7 | 5.8 | 5.8 | | |
| 11 | | 1X1 | | 6.0 | 5.8 | 5.5 | 5.5 | 5.7 | (5.8) | 5.8 | 5.8 | 5.75 | 5.75 | | |
| 12 | | 1X2 | | 5.8 | 5.4 | 5.6 | 5.6 | 5.8 | 4.9 | 5.1 | 5.9 | 5.4 | 5.4 | | |
| 13 | * | 1X3 | | 5.2 | 5.0 | 5.0 | 5.6 | 5.3 | 5.2 | 4.6 | 4.6 | 5.1 | 6.12 | | |
| 14 | * | 1X4 | | 5.2 | 4.8 | 5.1 | 4.8 | 4.8 | 4.6 | 4.6 | 5.2 | 4.9 | 5.88 | | |
| 15 | * | 1X5 | | 5.3 | 5.0 | 4.5 | 4.7 | 5.1 | 4.2 | 4.5 | 4.8 | 4.75 | 5.7 | | |
| 16 | * | 1X6 | | 5.0 | 4.6 | 5.0 | 4.8 | 5.2 | 5.2 | 4.2 | 5.0 | 4.85 | 5.82 | | |
| 17 | * | 1X7 | | 5.0 | 4.9 | 4.8 | 4.9 | 4.6 | 4.8 | 4.6 | 4.2 | 4.6 | 5.52 | | |
| | | | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | |

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**Note: Each shoe must not have more than 20 percent deviation.**

Figure 7-20 RS11 Test Data Sheet (Sheet 1)

## RS11 TEST DATA SHEET

RS08M # _____ Date _____
RS11 # _____ Name _____
RF11 # _____
Surface Modulation on A Track _____ %

**MAX GAIN/SLICE RATIO**

| High Gain Setting / Low Slice Setting = | Matrix 0 | Matrix 1 |
|---|---|---|
| | _____ = A/B | _____ = C/D |

Matrix 0 Reason for Failure _____

Matrix 1 Reason for Failure _____

**MIN GAIN/SLICE RATIO**

| Low Gain Setting / High Slice Setting = | Matrix 0 | Matrix 1 |
|---|---|---|
| | _____ = E/F | _____ = H/J |

Matrix 0 Reason for Failure _____

Matrix 1 Reason for Failure _____

Using the reading obtained above -- Compute:

Matrix 0 = A/B = X0 = _____ E/F = Y0 = _____

Matrix 1 = C/D = X1 = _____ H/J = Y1 = _____

(X0 + Y0)/2 = Z0 = _____ (X1 + Y1)/2 = Z1 = _____

Setting slice to 1.1V compute:

Z0 x 1.1 = _____ = Voltage setting of Ave track in each matrix respectively

Z1 x 1.1 = _____ =

Now set slice to 1.1V and set the voltage gain settings of the Ave track to the values obtained above.

Compute figure of merit. FM must be greater than 40.

(X0 - Y0)/(X0 + Y0) x 100 = FM -/+ x 100 = _____ (X1 - Y1)/(X1 + Y1) x 100 = FM -/+ x 100 = _____

Figure 7-20 RS11 Test Data Sheet (Sheet 2)

# APPENDIX A
# RF11/RS11 SIGNAL SUMMARY

| Signal | Summary |
|---|---|
| AA | First bit of the adaptive counter |
| ADDR OK | ADDRess OK logic signal. A true signal exists whenever the DS Register equals the WA Register, APAR is a zero, and the CTL bit has successfully shifted through all positions of the DS Register. |
| ADDR TO BUS | Gates CMA bits to Unibus A lines. |
| ADS | Address of Disk Segment. Bits of a register that save the DS shift register for real-time program control read-back. |
| ADS OUT | Gates ADS Register to Unibus D lines. |
| ADS TO BUS | Signal that places the ADS Register on the Unibus D lines. |
| APAR | Address PARity flip-flop. Computes parity of address read from Disk. Includes the Control (CTL) bit. |
| APE | Address Parity Error. |
| ATEST | This signal allows A track pulses to enter the A track error detection circuitry. |
| ATF SV | A Timing track SaVe flip-flop. Remembers which polarity ATT came last. |
| ATN (B) | A Timing Pulse Negative. |
| ATNM | A Timing Pulse Negative generated by Maintenance logic. |
| ATOK | A Timing OK. A timing pulses are occurring at their normal rate. |
| ATP (B) | A Timing Pulses Positive. |
| ATPM | A Timing Pulse generated by the Maintenance logic. |
| ATPN | Logical OR of the A Timing Pulses. |
| ATPN + 50 | ATPN pulses delayed by 50 ns. |
| ATTN | A Timing Track Negative. Level converted or buffered RS11 signal -ATT. |
| ATTP | A Timing Track Positive. Level converted or buffered RS11 signal +ATT. |
| ATT | A Timing Track. RS11 interface clocking signal. Unrectified signal pairs of this signal are designated +ATT and -ATT. |
| BB | Second bit of the adaptive counter. |
| BC | Bit Counter. A six-bit counter which counts data bits in each word. |
| BR | Buffer Register. |

| Signal | Summary |
|---|---|
| BR CLR | CLeaR the Buffer Register. |
| BR TO SR | Transfer the Buffer Register TO Shift Register. |
| BTER | B Timing track ERror. Missing or extra signal from the BTT. |
| BTF | B Timing track Flip-flop. Remembers which polarity BTT came last. |
| BTN | B Timing track Negative. Level converted or buffered RS11 signal -BTT. |
| BTN M | B Timing pulse Negative generated by Maintenance logic. |
| BTP | B Timing track Positive. Level converted or buffered RS11 signal +BTT. |
| BTP M | B Timing pulse Positive generated by Maintenance logic. |
| BTT | B Timing Track. RS11 interface signal containing the eleven bit address of the disk segment. Unrectified signal pairs of the address track are +BTT and -BTT. |
| CHT | Clock pulse for adaptive clock counter. |
| CLEAR | CLEAR – the OR of all power clear signals. |
| CLR BBSY | CLeaR Bus Busy. Relinquishes control of the Unibus. |
| CLR DATA RQ | CLeaR Data ReQuest. Removes the flag when the request has been honored. |
| CMA CARRY OUT | Current Memory Address overflow. |
| CMA CLK | Increments CMA register. Developed from CLR BBSY. |
| CMA INH | INHibits the CMA from incrementing. |
| CMA OUT | Gates CMA Register to Unibus D lines. |
| CMA IN | Gates HIgh and LOw bytes into CMA register. |
| CNTR BSY | CoNTRol BuSY. Requested disk transfer not complete. |
| CTER | C Timing track ERror. Missing or extra signal on the CTT lines. |
| CTF | C Timing track Flip-flop. Remembers which polarity of CTT was last present. |
| CTL | ConTroL. First bit read from the BTT. Used to control checking of the DS with the WA and shifting of the DS register. |
| CTN | C Timing track Negative. Level converted or buffered RS11 signal -CTT. |
| CTP | C Timing track Positive. Level converted or buffered RS11 signal +CTT. |
| CTP1 | C Timing Phase 1. First bit of a one bit 4-position ring counter used for word boundary control functions. |

| Signal | Summary |
|---|---|
| CTP 2 | C Timing Phase 2. Second bit of counter described in CTP 1. |
| CTP 3 | C Timing Phase 3. Third bit of counter described in CTP 1. |
| CTP 4 | C Timing Phase 4. Fourth bit of counter described in CTP 1. |
| CTT | C Timing Track. RS11 interface word boundary indicator. Unrectified signal pairs of this signal are designated +CTT and -CTT. |
| DA | Disk Address. Bits of a three-bit register indicating which disk of eight is selected. |
| DACK | Data ACKnowledged. Control is ready for next transfer. |
| DAE OUT | Gates DAE Register to Unibus D lines. |
| DAR IN | Gates HIgh and LOw bytes into DAR register. |
| DAR OUT | Gates DAR register to Unibus D lines. |
| DASV | DAta SaVe. Accepts each data bit to be shifted into the SR. |
| DATA ERR | The OR of a data parity error and a data hardware error flag. Read by the program as a data parity error. |
| DATA FLAG | Flag raised by the control when an NPR transfer is required. |
| DATA RQ | Asserts an NPR request for Unibus control. |
| DATA TO BUS | Gates DBR register to Unibus D lines during an NPR transfer in the Read mode. |
| DAW ENA | DPE, APE, and WLO ENAble latches the error condition. |
| DBR IN | Gates HIgh and LOw bytes into DBR register. |
| DBR OUT | Gates DBR register to Unibus D lines during a program transfer. |
| DCS IN | Gates HIgh and LOw bytes into DCS register. |
| DC LO | Power fail signal. |
| DCS OUT | Gates DCS register to Unibus D lines. |
| DCT | Data ConTrol; synchronizing bit for adaptive clocking. |
| DEV SELD | DEVice SELecteD. RF11 address decoded and Bus MSYN. |
| DEV SSYN | DEVice Slave SYNc. Response to processor when DEV DEL. |
| DISK FLAG | Flag raised by either an ERR or a Ready that will raise an interrupt in INT ENA is set. |
| DISK RUN | Disk transfer requested (BUSY) and a word boundary has been found (CTP 3). |
| DPAR | Data PARity flip-flop. The flip-flop that calculates the data parity. |
| DPE | Data Parity Error. A flag set if there is a parity error in a data word. |
| DR DLY | Disk Run DeLaYed. |
| DRL | Data Request Late. Processor failed to allow an NPR before the next word was ready. |
| DS CLR | Disk Segment register CLeaR. |
| DS | Disk Segment. Bits of the Disk Segment address 11-bit shift register. |
| DTE | Data Timing Error. Missing or extra signal on the DTT lines detected here. |

| Signal | Summary |
|---|---|
| DTER | Data Timing ERror. Missing or extra signal on the DTT lines stored here. |
| DTN | Data Track Negative. Level converted or buffered RS11 signals -DTT. |
| DTP | Data Track Positive. Level converted or buffered RS11 Signal +DTT. |
| DTT | DaTa Track. RS11 interface read data signal. Unrectified signal pairs of this signal are +DTT and -DTT. |
| ERR | ERROR – the OR of the error flags. |
| EX | EXtended memory bits. |
| FOUND | Indicates data control pulse (DCT) was sensed by the adaptive clocking logic. |
| FRZ | FReeZe. Signal disables clock input to control as a result of a HDWR ERR, NEM, or an APE. |
| F0 | Function Register bit 0. |
| F0 SV | Function register bit 0 SaVe. |
| F1 | Function register bit 1. |
| F1 SV | Function register bit 1 SaVe. |
| GO | Signals the control to execute the function loaded. |
| GO CLR | Initializes soft errors. |
| INC DA | INCrement Disk Address. Occurs after the last word of each disk has been successfully transferred. |
| INC TA | INCrement Track Address. Occurs after the last word of each track has been successfully transferred. |
| INC WA | INCrement Word Address register. Occurs for each successful transfer to the disk. |
| INT ENA | INTerrupt ENAble. Control flip-flop that determines if the Disk flag will cause an interrupt. |
| I/O STR | STRobe pulse used during program transfers. |
| IN | Control signal for a processor DATI during program control. |
| INC DAE | INCrement DAE. Prevents a ripple carry when the DAR is loaded. |
| INC DAR HI | INCrement DAR HIgh byte. Prevents a ripple carry when the DAR low byte is loaded. |
| INIT | INITialize. Processor power clear. |
| INTR CLR | Clears the Interrupt flag. |
| INTR MASTER | Gates the Interrupt flag and Vector to the Unibus. |
| LDSR | LoaD Shift Register. Control has found the location of the word to be Written or Write Checked, has transferred the BR to SR, and is shifting the data onto the WRITE DATA line. |
| LDLY | Load DeLaY. A flag set during the Write Check operation to check for data parity errors. |
| LOCK | RS11 interface signal signifying that the Disk and Track selected is Write Protected. |
| LS EN | Load Shift register ENable. Control signal that allows loading of Shift Register (SR) during Write or Write Check. |

| Signal | Summary |
|---|---|
| LSTE | Load Shift register Timing Error. A flag that is set and reset when the Buffer Register is filled during a Write or Write Check operation. If it resets too slowly, a DRL flag is posted. |
| MA | MAintenance flip-flop. Holds off RF11 delay time-outs during maintenance instructions. |
| MAT | Maintenance A Timing signal. Program control maintenance logic that simulates the RS11 head signal to the ATT read amplifier. |
| MBT | Maintenance B Timing signal. Program control maintenance logic that simulates the RS11 head signal to the BTT read amplifier. |
| MCT | Maintenance C Timing signal. Program control maintenance logic that simulates the RS11 head signal to the CTT read amplifier. |
| MDT | Maintenance DaTa signals. Program control maintenance logic that simulates the RS11 head signal to the DTT read amplifier. |
| MNEP | Missing Negative or Extra Positive pulse from ATTs. Causes FRZ status. |
| MPEN | Missing Positive or Extra Negative pulse from the ATTs. Causes FRZ status. |
| MXF | Missed X (Trans)Fer. Disk was BUSY and missed transferring data twice in succession from the same address. More than three disk revolutions occurred without a transfer. |
| NDT | Negative DaTa flip-flop that stores the negative data bit. |
| NED | NonExistent Disk. Error status indicating an attempt to use a nonexistent disk. May be caused either by sequencing into or by direct program command. |
| NEM | NonExisting Memory. Bus SSYN did not return from the address the control asserted on the bus. |
| NPC MASTER | NonProcessor Control of the Unibus. |
| NPC STR | STRobe pulse used during a Write or Write Check NPR. |
| OFLO | OverFLOw flag set when the Word Count overflows during a DECdisk transfer. |
| OUT | Control signal for a processor DATO or DATOB during program control. |
| PDT | Positive DaTa – flip-flop that stores the positive data bit. |
| PSLER | Program SeLect ERror. A nonexistent disk was selected by the program. One of the inputs to the NED status. |
| RB FULL | Read Buffer FULL. Control has loaded the BR from the SR and the processor has not as yet taken the data. |
| RD CLK | ReaD CLocK. Pulse used to shift the SR during Read or Write Check. |
| RD DIS | ReaD DISable. Signal disables the read portion of the control logic to allow time for the RS11 read amplifiers to recover. Nullified in MA mode. |
| RD LD | ReaD LoaD. During Read or Write Check this signal is one of the elements that enables data parity error detection. |
| RD SR | ReaD (into the) Shift Register. Control has found word to be read from RS11 and is shifting the data into the SR. |
| RD TEST | ReaD TEST. A pulse that clocks the DTE error flag. |

| Signal | Summary |
|---|---|
| READ | Signal from controller to RS11 enabling the read amplifiers. |
| RSTE | Read Shift register Timing Error. If set will cause the DRL flag to be posted. |
| SMB | Sync Boundary (word) Marker synchronizes adaptive clocking logic. |
| SEL ERR | SELect ERRor. Signal to indicate that an NED was selected. |
| SEL DSK | SELect DiSK. Unary decoded signals from the DA register for selecting one disk of eight. |
| SELECT | SELECT line from each disk. |
| SEQ ER | SEQuence ERror. A nonexistent disk was selected during a job transfer. |
| SR CLK | Shift Register CLocK pulse. |
| SR CLR | Shift Register CLeaR pulse. |
| SR to BR | Shift Register to Buffer Register transfer pulse. |
| SR | Shift Register. Serial/parallel disk data converter. |
| SRI | Shift Register In. Command to transfer data from BR to SR during Write or Write Check. |
| SRID | Shift Register In Delayed. Signal delayed to test overflow before raising a data flag. |
| SRO | Shift Register Out. True whenever the SR has assembled the data word to be read and the BR is ready to receive it. |
| STRT XTIM | STaRT X (trans)fer TIMing begins I/O strobing for program transfers. |
| STROBE | Main clock pulse determined from the adaptive clock logic. |
| TA | Track Address register. |
| TP1 | Timing Pulse 1. |
| TP2 | Timing Pulse 2. |
| TP3 | Timing Pulse 3. |
| T00 T06 | Track address lines to RS11. |
| UPD ADS | UPDate ADS. Clocks the DS register into the ADS for program availability. |
| WA | Word Address register. An 11-bit register containing the address desired on the disk. The WA is compared with the DS to give ADDR OK. |
| WB FULL | Write Buffer FULL. Processor has loaded the BR with data requested during Write or Write Check and the control has not transferred the data from the BR to SR. |
| WBM | Word Boundary Marker. Defines end of word transfer. |
| WC CARRY OUT | Word Count overflow. |
| WC IN | Gates HIgh and LOw bytes into WC register. |
| WC OUT | Gates WC register to Unibus D lines. |
| WLO EN | ENable Write LockOut. If any tracks are locked out, this signal effects the lockout. |
| WLO | Write LockOut. Error Status bit that occurs whenever an attempt is made to Write in an address that is Write Protected. |

| Signal | Summary |
|---|---|
| WCE | Write Check Error. Indicates a comparison error exists between the word from core memory and the word read from the disk during Write Check. |
| WR DA | WRite DAta flip-flop that receives the Shift Register output to be written on the disk. |
| WRITE | WRITE function decoded from Function Register. |
| WRITE DATA | RS11 interface signal line over which the RF11 sends the serial data to be written. |

RF11/RS11 DECDISK
DEC-11-HRFB-D

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