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PDP-X Technical Memorandum # 31

Title: PDP-X/II Programmers Console

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Index Keys: Console
Processor

Distribution Keys: A,B,C,D,E

Obsolete: None

Revision: None

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The console of a digital computer is used to perform two functions:

1. Allow the programmer to examine or modify the state of the machine and his program and hence act as a debugging tool.

2. Provide information about the state of the processor that is necessary for the maintenance and trouble-shooting of the system..

While the console features required for these two functions overlap, only the first one will be treated here. Details of the console features required for maintenance and trouble-shooting will be determined as the hardware details of the implementation become firmer.

The console features required for program debugging depend upon the system configuration. In large configurations, most program debugging is done through software systems such as DDT, traces and core dumps. The user may never actually use the computer console. In small configurations, the user may not wish to pay the resident core penalty required by these software systems. (With retrievable storage devices techniques have been developed to allow DDT to be transparent to the user, i.e., the PDP-8/I disk software.) In this case, the user may rely upon the console to aid in the debugging of his program. The usual techniques are to step through a program, examine or modify memory and to observe the state of the processor and IO devices.

In addition to program debugging, the console is used by the computer operator to start or stop programs, reset the IO system or to initiate program loading.

To facilitate these operations, PDP-X/II will have a console with several indicators, switches and keys as described below:

I. Indicators

1. RUN (1 bit)

The RUN indicator is lit when the processor is executing instructions. It is not lit (cleared) when the processor has been stopped

by manual intervention (STOP, RESET, SINGLE INSTRUCTION) or because the processor has executed a HLT (halt) instruction.

2. SR (Status Register, 16 bits)

The SR contains the status word of the currently active process (contained in the RG bits, SR10-12). The contents of the SR may be manually altered by use of the DEPOSIT Key (See below).

3. IR (Instruction Register, 16 bits)

The IR contains the operation code, R bits, X bits and D_1 bits of the instruction being executed. When the processor is stopped, the IR contains the instruction last executed. If an IO output was the last operation performed before the processor was stopped, D_1 field (IR8-15) contains the last data byte outputted. In all other cases, D_1 will contain the D_1 field of the instruction last executed.

4. MI (Memory Interface, 16 bits)

The MI has no meaning when the processor is running. When the processor is stopped, th e MI will contain the address of the next instruction to be executed. After an EXAMINE or DEPOSIT operation, the MI will contain the address of the word examined or the address of the word into which data has been deposited (see EXAMINE, DEPOSIT below).

5. CI (Console Indicators, 16 bits)

The CI lights represent the state of the CI register which may be loaded under program control by the execution of the WCI (Write Console Indicators) instruction. If the program executes a HLT instruction, the effective word is loaded into the CI and the processor is stopped. After an examine or deposit operation, the CI will contain the

contents of the word examined or the new contents of the word into which data has been deposited (see EXAMINE, DEPOSIT below).

6. PI EXR (Program Interrupt External Request, 8 bits)

The PI EXR lights indicate priority interrupt (1-7) or special multiplexor channel (8) requests from external devices. When an external request is higher than the highest PI ACT level and the highest PI INH level, then an interrupt will be granted and the PI ACT indicator corresponding to the highest PI EXR bit will be set.

7. PI INR (Program Interrupt INternal Request, 7 bits)

The PI INR lights indicate internal interrupt requests generated by the program by the execution of the PSR instruction (See PDP-X Technical Memorandum #29, sections 2.6.7, 2.7). When an internal request is higher than the highest PI EXR level and the highest PI ACT level and the highest PI INH level, then an interrupt will be granted, the highest PI INR bit will be cleared and the corresponding PI ACT indicator will be set

8. PI INH (Program Interrupt INhibit, 8 bits)

The PI INH lights indicate which program interrupt levels are inhibited. Only interrupt requests (PI EXR or PI INR) that are at a level higher than the highest PI INH will be granted. (See PDP-X Technical Memorandum #29, sections 2.6.7, 2.7).

9. PI ACT (Program Interrupt ACTive, 7 bits)

The PI ACT lights indicate those priority levels on which processes have been initiated. The RG bits of the SR indicate the process that is currently active (this corresponds to the highest PI ACT indicator).

II. Switches

1. CSW (Console SWitches, 16 bits)

There are 16 switches which comprise the CSW These switches may be read by the operating program by the execution of the RCS (Read Console Switches) instruction. These switches are also used to manually enter data and addresses by means of the START, EXAMINE, DEPOSIT, DEPOSIT NEXT keys. The right-hand six bits (CSW10-15) are also used to select the device for automatic program loading (READIN).

2. POWER

The POWER switch controls the application of primary power to the computer and to external devices whose power controls are interfaced to it.

3. CONSOLE LOCK

The CONSOLE LOCK switch has two positions: locked and unlocked. When the console is unlocked, all keys and switches are operable. When the console is locked, no switches are operable. The program may still execute WCI, RCS or HLT instructions.

III. Keys

1. SI (Single Instruction)

The SI key has two positions: off (up) and on (down). When the SI switch is on, the program will stop at the completion of every instruction with the MI containing the address of the next instruction to be executed. Repetitive depressing of the CONTINUE switch while SI is on, steps the program through its sequence one instruction at a time.

2. STOP

The STOP key has two positions: off (up) and operate (down, spring-loaded return). When this switch is depressed, the processor is stopped at the completion of the current instruction. The MI will contain the address of the next instruction to be executed.

3. RESET

The RESET key has two positions: off (up) and operate (down, spring-loaded return). When this switch is depressed, the processor is stopped at the completion of the current instruction, the IO system is reset, PI EXR, PI INR, PI INH and PI ACT are cleared, RG is set to zero and the SR (level 0) is cleared. On a system with the (optional) protection feature, PI ACT bit 1 is set, RG is set to one.

4. CONTINUE

The CONTINUE key has two positions: off (up) and operate (down, spring-loaded return). Depressing CONTINUE resumes program execution from the point at which it was stopped. If the processor is running, depressing CONTINUE will have no effect.

5. START

The START key has two positions: off (up) and operate (down, spring-loaded return). Depressing START causes the contents of the CSW to be placed into the program counter (at level RG) and the processor to be started at level RG. If the processor is running, depressing START will have no effect.

6. READIN

The READIN key has two positions: off (up) and operate (down, spring-loaded return). Depressing READIN causes the IO system to be reset, PI EXR, PI INR, PI INH and PI ACT to be cleared, RG to be set to zero and the device whose Device Address Code appears in CSW10-15 to be selected in Readin Mode. If the processor is running, depressing READIN will have no effect.

7. EXAMINE

The EXAMINE key has two positions: off (up) and operate (down, spring-loaded return). Depressing EXAMINE causes the contents of the word specified by the CSW to be placed in the CI. If the processor is not running, the address of the word examined (contents of CSW) will be placed in the MI. The address used during EXAMINE, DEPOSIT, EXAMINE NEXT and DEPOSIT NEXT is the address as seen by the currently active process, i.e., it is mapped with RG. The operator must, thus, be careful when examining accumulators when the processor is running since at the instant when EXAMINE is depressed, the processor may be executing an IO service routine and the CI will be loaded with the accumulator at the level associated with that service routine.

8. DEPOSIT

The DEPOSIT key has two positions: off (up) and operate (down, spring-loaded return). Depressing DEPOSIT places the contents of the CSW in the CI and in the memory location specified by the contents of the MI.

If the processor is running, depressing DEPOSIT will have no effect. The address of the word into which data is to be deposited may be placed in the MI by the use of the EXAMINE key.

9. EXAMINE NEXT

The EXAMINE NEXT key has two positions: off (up) and operate (down, spring-loaded return). Depressing EXAMINE NEXT causes the contents of the MI to be incremented and the contents of the word specified by the new value of the MI to be placed in the CI. If the processor is running, depressing EXAMINE NEXT will have no effect.

10. DEPOSIT NEXT

The DEPOSIT NEXT key has two positions: off (up) and operate (down, spring-loaded return). Depressing DEPOSIT NEXT causes the contents of the MI to be incremented and the contents of the CSW to be placed in the CI and in the memory location specified by the new value of the MI. If the processor is running, depressing DEPOSIT NEXT will have no effect.