PDP-X Technical Memorandum # 19

Title: PDP-X Diagnostic Goals

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Index Keys: Diagnostics
                    Goals

Distribution
        Key: A,B,C

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The following is a general description of diagnostic software goals for the PDP-X:

I. Basic Premises

    A.   Diagnostic software will be primarily concerned with the problems of field maintenance and system acceptance. In-house production and checkout will use special equipment and test systems.

    B.   The "hard-core" logic of the PDP-X processor represents a substantial percentage of the entire system making "module callouts" and detailed diagnosis impossible.

    C.   Most of the logic in PDP-X will be inaccessible to the diagnostic processor.

II. Preliminary Conclusions

    A.   Because of A, B, C above, the diagnostics will be more like exercisers (i.e., as for PDP-9). These will allow detection of errors in data paths, noise, repetition rate problems, etc., as well as validation of memories and IO devices.

    B.   Since basic timing, data paths, and instruction sequencing require the operation of a large percentage of the machine, a means will be provided to validate their operation:

        1.   A means will be provided for off-line cycling of main memory. This will allow "basic operation" verification as well as off-line maintenance.

        2.   Basic control memory loops will be provided to test central processor registers and to cycle the fast memory.

        3.   The maintenance console of the system will allow for:

            a.   Single instruction execution

            b.   Single memory cycle execution

            c.   Control memory single step

III. Diagnostics

Because of B on the previous page, the diagnostic programs may assume that the basic control processor is functioning and then may concentrate on the types of problems described in A on the previous page.

Tests for IO devices will be organized along the lines of current IO diagnostics checking both the operation of the control and validating the operation of the physical data medium.

Central processor diagnostics will be written to do as many "hard computations" per unit time as is possible. They will progress from cursory instruction validation to detailed data validation.

Diagnostics will be no larger than 4K in size and will be modular so that major re-work will not be required for Model I Systems.