PDP-X Technical Memorandum # 12

Title: Detailed Model Specifications

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Index Keys: Design Decisions
Models
Specifications

Distribution Keys: A, B, C

Obsolete: None

Revision: None

Date: July 21, 1967

A wide range of system performance is available with PDP-X as described elsewhere.[1] This document describes the proposed models and outline expandability and compatability among these models. The two basic software packages require, respectively, the Ia and IIa models.

I.

The smallest PDP-X model has no hardware general registers. It has two priority levels, main program and interrupt level as in current small computer products. Since both the program counter and accumulators now reside in memory, it will run approximately twice as slow as Model II. The Model I instruction set will consist of only the basic instructions.[2] All EOP class instructions will trap. Memory is expandable from 4K to 32K. The basic register subassembly will be identical to the one used in the larger models permitting production economies. The control may be either control memory or an 8I type control, depending upon detailed cost considrations. All peripheral equipment will run on Model I within the constraints of the single interrupt level.

Since all PDP-X models operate asynchronously with their memory systems, a truly low-cost system is achievable by using an 8 micro-second memory. This would give a 32 micor-second add time, comparable to 8S. The 33 ASR Teletype is standard on Model I systems.

The Model I processor may not be upgraded to a Model II processor. All of the other components of the system, however, may be used with a Model II processor.

II

The medium sized PDP-X model has two sets of hardware general registers. It has two priority levels, main program and interrupt level. The Model II instruction set consists of the basic instructions and extended instructions. The Basic configuration consists of High-Speed Paper Tape and the 33 KSR Teletype with an 8K memory.

Since program counter and accumulators are now in fast memory, the add time is 2 memory cycles. The Model II processor is expandable as follows:

1. The Priority Interrupt System may be added. This option adds 6 sets of general registers, the priority interrupt structure and special instructions to modify the state of the interrupt system.

2. The Protection Option may be added. This option consists of the user mode/ executive mode, the memory paging system and certain special instructions to alter the state of the paging hardware. The Priority Interrupt system is required before this option may be added.

3. Power Fail, Memory Parity, Machine Check hardware may be added. Parity may be added without any alterations to the existing memory system.

4. The memory system may be increased to 32K or to 128K if the Protection Option is installed.

References:

1. "PDP-X Technical Memorandum #6", July 6, 1967.

2. "PDP-X Processor Description", June 26, 1967.

Models

Model	Register Sets	Instruction Set	Standard Memory	Standard IO	Interrupt Structure	Protection System	Add Time	Multiply Time (Signed)	Index Time
I_a	2, core	Basic	4k - 8μ	33 ASR	2 levels	None	32μ	subroutine	8μ
I_b	2, core	Basic	4k -.75μ	33 ASR	2 levels	None	3μ	subroutine	.75μ
II_a	2, hard-ware	Extended Set	8k -.75μ	33 ASR High-Speed Paper Tape	2 levels	None	1.5μ	< 14μ	0
II_b	8, hard-ware	Extended Set	8k -.75μ	33 ASR High-Speed Paper Tape	8 Fully Nested Levels	None	1.5μ	< 14μ	0
II_c	8, hard-ware	Extended Set	16K-.75μ	33 ASR High-Speed Paper Tape	8 Fully Nested Levels	User/Exec Modes Paging	1.5μ	< 14μ	0