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PDP-X Technical Memorandum # 4

Title: PDP-X Design Decisions

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Having had discussions with DEC personnel, several customers, and others, we have arrived at the following processor design decisions:

a. The basic word length has been chosen to be 16 rather than 18 bits in order to maintain compatibility with the majority of the newer computers, especially IBM. The byte and character are 8 bits long; a double word consists of 4 bytes; a floating point word, with hexadecimal radix, consists of either 4 or 8 data bytes.

b. The word, 16 bits of data, has been chosen to be the basic addressable unit although instructions are available which reference bits, bytes, doublewords, etc. as data. Doubleword instructions need not fall on doubleword boundaries although double data words must.

c. The basic structure contains multiple accumulators/index registers. The general register structure simplifies the order code and proves greater programming power over more conventional single accumulator organizations. The floating point registers, more of a programming convention than hardware feature, are distinct from the general registers.

d. No base registers are used in addressing, instructions are capable of addressing relatively, indexed, and to page 0 in the short format. A long format permits direct specification of any word anywhere in the entire memory system as well as indexed or immediate data. The most common instructions are available in short form, all are available in long form.

e. The basic unit of IO data is the byte. This unit is natural for paper tape peripherals, the most common types, as well as the teletype. The bus organization permits the transmission of a full word whenever necessary.

f. A priority interrupt system which permits direct device recognition is provided as standard. Separate register sets for the interrupt levels are provided to maximize IO bandwidth.

g. A standardized, unified IO structure common to all processors permits both program controlled and channel controlled transfers over the same bus with a minimum of device hardware.