System Overview

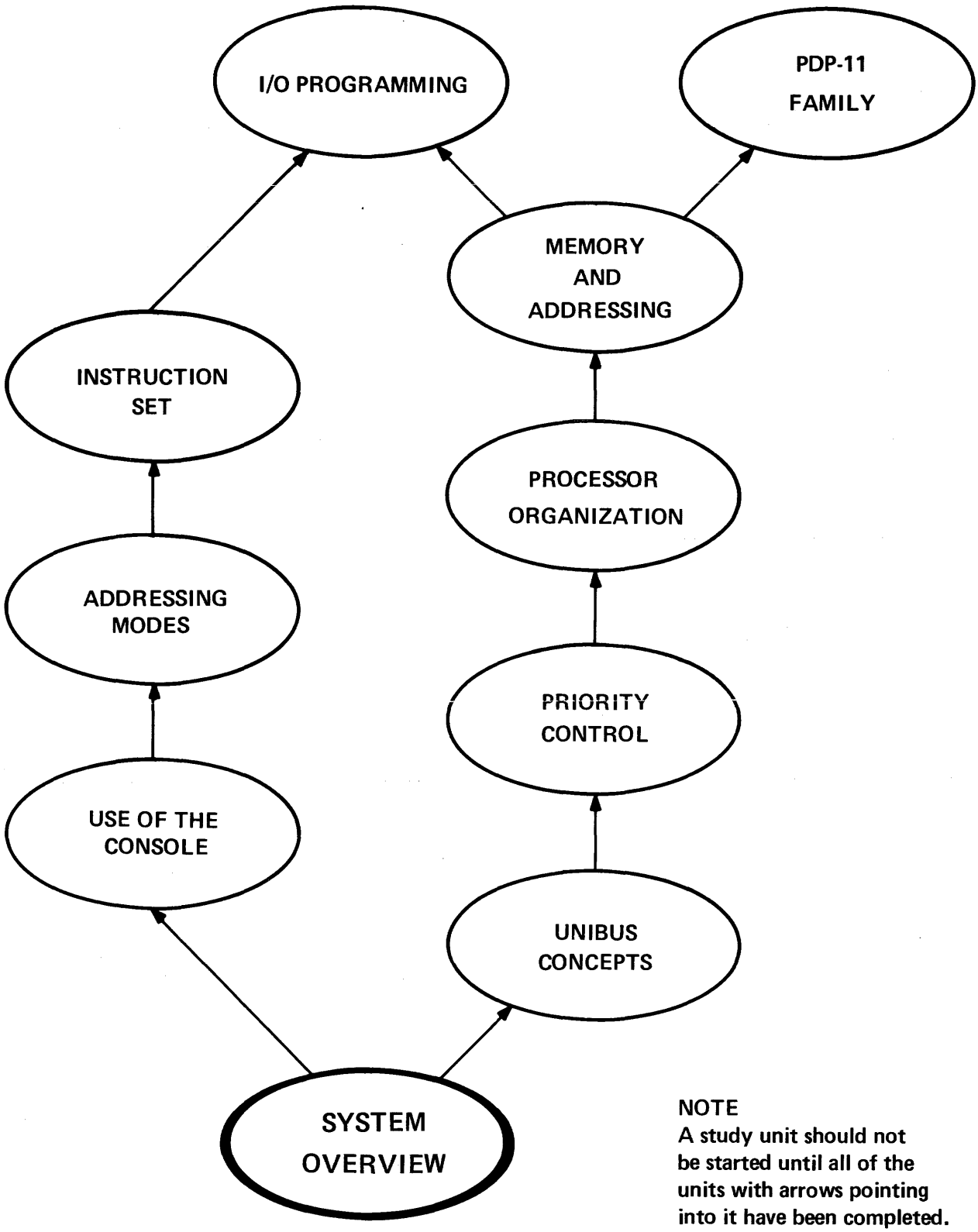
student workbook introduction to the pdp11

digital equipment corporation · maynard. massachusetts

1st Printing, March 1974
2nd Printing (Rev), November 1974
3rd Printing (Rev), April 1977

Printed in U.S.A.

course map



NOTE
A study unit should not be started until all of the units with arrows pointing into it have been completed.

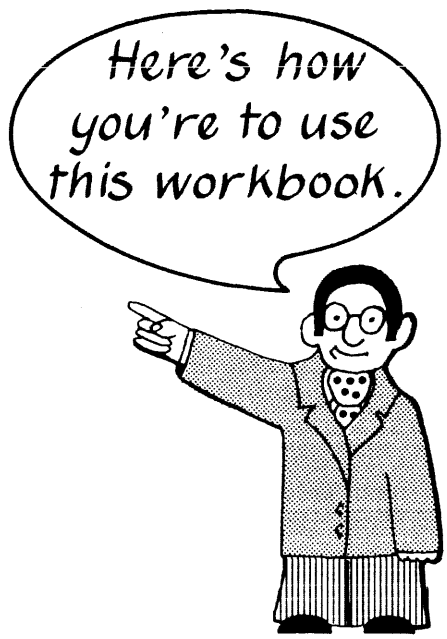
read on

READ
LEARNING
OBJECTIVES
(page 1)

NOW RUN FILM
CARTRIDGE A

REVIEW
MATERIAL
(pages 3 – 11)

NOW GO ON TO THE
NEXT STUDY UNIT.



read on

objectives

After completing this study unit, you should be able to . . . .

★ Explain how the PDP-11 differs from more traditional computers in terms of:

- The number of buses that interconnect the processor, memory, and I/O devices.
- The manner in which the instruction set is used.

★ Explain why PDP-11 instructions can be used with the processor, or with memory, or with I/O devices.

★ Define the term "upward compatible" as it relates to PDP-11 processors.

★ Explain the function of an I/O interface.

★ Describe PDP-11 memory with regard to the following basic points:

- The three types of memories that are available.
- The significance of the terms "low byte" and "high byte".
- Memory organization as it relates to bytes and 16-bit words.

★ Explain, in a general sense, how PDP-11 addresses are allocated between memory and I/O devices.

additional resources

- **PDP-11/04/05/10/34/35/40 Processor Handbook** — Read Chapter 1.

The following material is covered in this study unit:

Topic	*Key Points*	*Visual Ref.*
overview	★ This study unit is an overview of the PDP-11 computer system and deals with basic concepts *common* to *all* PDP-11 systems. It covers: • PDP-11 versus traditional systems. • PDP-11 system elements. • Typical PDP-11 systems.	1–5
basic concepts	★ Any computer system can be divided into three main *functional* elements. • *Memory* – for storing information that is readily available to the processor. • *Processor* – for calculating and for routing information between the other two elements. • *Input/Output Device* – to permit communication between man and machine.	6
PDP-11 VS TRADITIONAL SYSTEMS	★ The two primary differences between the PDP-11 computer and traditional computer systems are: the paths (or buses) that interconnect system elements; and the instruction set.	

read on

Topic	*Key Points*	*Visual Ref.*
traditional bus	★ A traditional system has either two or three separate and independent buses. • *Memory bus* – for connecting the memory to the processor. • *I/O bus* – for connecting the processor to one or more input/output devices. • *DMA bus* – direct memory access bus for connecting memory to I/O devices. ★ Because these buses are physically and functionally separate, an element designed for one bus cannot work with another bus. For example, an I/O device could not be connected to a memory bus.	7–9
PDP-11 bus	★ In a typical PDP-11 system, memory, the central processor, and the I/O devices communicate over a single bus. ★ This single bus is called a *Unibus*. ★ Elements can be continually added to the Unibus, in either direction. ★ This Unibus is a *common path* so that any computer element can communicate with any other element on the bus. • Processor can communicate with memory. • Processor can communicate with an I/O device, or vice versa. • I/O devices can deal directly with memory while the processor is doing another job. This is called direct memory access (DMA). ★ The Unibus actually consists of 56 lines, or wires, to handle address, control, and data functions.	10–15

read on ➧

Topic	*Key Points*	*Visual Ref.*
traditional instruction set	★ A traditional computer system requires up to three separate instruction sets. • Memory reference instructions – to deal with memory. • Input/output instructions – to deal with I/O devices. • Arithmetic instructions – to permit the processor to perform calculations. ★ These three sets of instructions cannot be intermixed; for example, an I/O instruction cannot be used with the processor or with memory. ★ The programmer must constantly deal with three completely different sets of instructions, making certain he does not mix them up.	16–19
PDP-11 instruction set	★ Because all devices operate from a common Unibus, there is only *one* instruction set. One bus . . . one instruction set. ★ The programmer keeps track of only one instruction set, regardless of what devices he is dealing with. For example, we can do many things with a MOVe instruction. • MOV transfers data from memory to the processor. • MOV transfers data from the processor to an I/O device to tell the device what job to perform. • MOV transfers data from the I/O device to memory for storage. • MOV transfers I/O status information to the processor for monitoring.	20–26

read on

Topic	*Key Points*	*Visual Ref.*
PDP-11 SYSTEM COMPOSITION	★ All PDP-11 systems are constructed from a large number of "building blocks".	27, 28
	★ These blocks can be assembled in many different combinations to produce a variety of PDP-11 computer systems.	
	★ Because of the "building block" concept, the PDP-11 is not just one computer system, it is an entire family of systems.	
	★ The three major building block categories are:	
	• Processors	
	• Memories	
	• Input/Output Devices	
processors	★ A number of 16-bit processors can be used to build PDP-11 systems.	29, 30
	★ Although these processors incorporate the same basic PDP-11 architecture, they have different *performance factors* such as:	
	• *Size* of the instruction set.	
	• *Speed* of instruction execution.	
	• *Number* of memory locations that can be addressed by the processor.	
	★ All PDP-11 processors are *upward compatible.* In other words, with but a few exceptions, programs developed for a small processor can be run equally well on one of the medium or large processors.	
	★ Each of the available processors is supported by several memories and a wide selection of input/output devices.	

read on ➧

Topic	*Key Points*	*Visual Ref.*
input/output devices	★ There is a wide selection of input/output (I/O) devices that can be used in PDP-11 systems. For example: • *Common I/O devices* – such as teleprinters, paper-tape readers and punches, card readers, line printers, and graphic displays. • *Mass storage devices* – such as disks and magnetic tape units.	31
I/O interface	★ An I/O device *cannot* be connected directly to the Unibus. Each device must have an *interface* unit. • The interface connects to the Unibus and handles communication between the I/O device and other system elements. • In other words, the interface converts information on the bus into the data and control signals required by the device. • Each device interface is different; an interface designed for one type of device cannot be used with another device. This is due to the fact that each device requires a unique set of control signals. • Typically, the Unibus is connected to the *interface*. The *device* is connected to the interface by means of an I/O cable.	32–35

read on

Topic	*Key Points*	*Visual Ref.*
memory	★ There are three basic types of memory that can be used with PDP-11 systems: • *core memory* • *read-only memory* • *semiconductor memory* ★ Memory consists of a number of storage locations each holding 8 bits, or one "byte" of information. ★ Each byte location is given a consecutive address starting with zero.	36, 37
bytes vs words	★ Pairs of bytes are combined to form the 16-bit PDP-11 *word.* • The byte forming the right side of the word has an *even* address and is called the *low* byte. • The byte forming the left side of the word has an *odd* address and is called the *high* byte. • Because of this addressing structure, the user can select just a low byte, or just a high byte, or a full word. This increases the power of the instruction set because many instructions can operate on either bytes or words.	38, 39

read on ➧

Topic	*Key Points*	*Visual Ref.*
16-bit address	★ The basic PDP-11 system uses a 16-bit address structure. ★ A 16-bit address permits either: • 32K of *word* addresses. • 64K of *byte* addresses. ★ *Not all* of these addresses are used for memory: • 28K of word addresses are used for addressing memory locations. • 4K of word addresses are reserved for registers located in the processor and I/O devices.	40
18-bit address	★ Some PDP-11 systems use an expanded 18-bit address. The expanded address is used when the system is equipped with memory management hardware. ★ An 18-bit address permits either: • 128K of word addresses. • 256K of byte addresses. ★ Not all of these addresses are used for memory: • 124K of word addresses are used for addressing memory locations. • 4K of word addresses are *still* reversed for registers located in the processor and I/O devices. **NOTE** **The PDP-11/70 is designed to handle a *22-bit* address. With this expanded address, an 11/70 can access up to 2 million words (4 million bytes) of main storage.**	41

read on ➧

	LSI-11 & 11/03	11/04	11/05 & 11/10	11/34	11/35 & 11/40	11/45 11/50 11/55	11/70
Processing Modes (Names)	Kernel	Kernel	Kernel	Kernel User	Kernel User	Kernel Supervisor User	Kernel Supervisor User
Number of GPRs	8	8	8	9	9*	16	16
Number of Hardware Interrupt Levels	1	4	4	4	4	4	4
Number of Software Interrupt Levels	none	none	none	none	none	7	7
Maximum Address Space (Words)	32K	32K	32K	128K	128K	128K	2M
Maximum Memory Size (Words)	28K	28K	28K	124K	124K	124K	1.9M
Bus Structure (Names of Buses)	LSI-11 Bus	Unibus	Unibus	Unibus	Unibus	Unibus & Fast Bus	Unibus DMA Bus Memory Bus
Types of Memory	Core MOS PROM	Core MOS	Core	Core MOS	Core	Core MOS Bipolar	Core & Cache
Number of Hardware Stacks	1	1	1	2	2*	3	3
Memory Management (Not available, Optional, or Standard)	N/A	N/A	N/A	Std	Opt	Std	Std

*With Memory Management option.

read on

review material

Topic	*Key Points*	*Visual Ref.*
typical PDP-11 systems	★ PDP-11/03 microcomputer	43
	• Small, low-cost member of the PDP-11 computer family.	
	• Executes all of the basic PDP-11 instructions.	
	★ PDP-11/04 minicomputer	44
	• Designed primarily for dedicated applications such as patient monitoring or process control.	
	★ PDP-11/34 minicomputer	45
	• Designed to handle multiple-task applications such as a time-sharing system where several users are interacting with the computer.	
	★ PDP-11/70 computer system	46
	• Largest, most powerful computer in the PDP-11 family.	
	• Features include extremely fast throughput, cache memory, and the ability to access up to 2 megawords of main memory.	
	• Can accommodate many different tasks on a concurrent basis (i.e., batch processing, real-time processing, and interactive time-sharing).	
summary table	★ The table on page 10 lists and describes the family of PDP-11 computers. The characteristics listed in this table (i.e., processing modes, number of GPRs, interrupt levels, etc.) are defined and discussed in later study units.	

read on ➧