EK-0TS11-TM-003

TS11 Subsystem

Technical Manual

Prepared by Educational Services
of
Digital Equipment Corporation

1st Edition, October 1980
2nd Edition, January 1983
3rd Edition, January 1984

The information in this document is subject to change without notice. Digital Equipment Corporation assumes no responsibility for any errors that may appear in this document.

This equipment generates, uses, and may emit radio frequency. The equipment has been type tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such radio frequency interference. Operation of this equipment in a residential area may cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Faston™ and Mate-N-Lok™ are trademarks of AMP, Inc.

The following are trademarks of Digital Equipment Corporation, Maynard, Massachusetts.

digital	DECwriter	RSTS
DEC	DIBOL	RSX
DECsystem-10	MASSBUS	UNIBUS
DECSYSTEM-20	PDP	VAX
DECUS	P/OS	VMS
DECmate	Professional	VT
DECnet	Rainbow	Work Processor

CONTENTS

CHAPTER 6 THEORY OF OPERATION

CHAPTER 7 SERVICING

FIGURES

TABLES

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The TS11 Subsystem is a low price, medium performance, 9-track tape storage system featuring microprocessor controlled electronics for high data reliability and maintainability.

The TS11 fully integrated tape storage system is packaged with its associated interface and power supply in a standard 19-inch rack mountable frame. It can be configured in several cabinets to complement various Digital computer systems. Reading and writing are performed at 45 inches per second and data is recorded at 1600 bits per inch (bit/in) phase encoded (PE). ANSI standard format recording allows data to be transferred easily between computer systems.

The TS11 subsystem consists of a tape transport with an integrated formatter and a single hex size interface/controller module. This module, M7982, is designed for Unibus PDP-11 and VAX-11 processors. It plugs into any hex sized slot in a Unibus small peripheral controller (SPC), and it communicates with one tape transport.

TS11 Subsystem Features

Performance

114 cm/sec (45 inches/sec) read/write speed
72,000 bytes per second transfer rate
380 cm/sec (150 inches/sec) rewind speed
Bidirectional reading capability

Capacity

1600 bit/in phase encoded ANSI compatible recording
15.24 cm to 26.67 cm (6 inches to 10.5 inches) tape reel capacity

Reliability/Data Integrity

Automatic error correction
Read after write check
In-line diagnostics that run continuously during drive standby mode
Off-line self diagnostics
Simple, rugged design

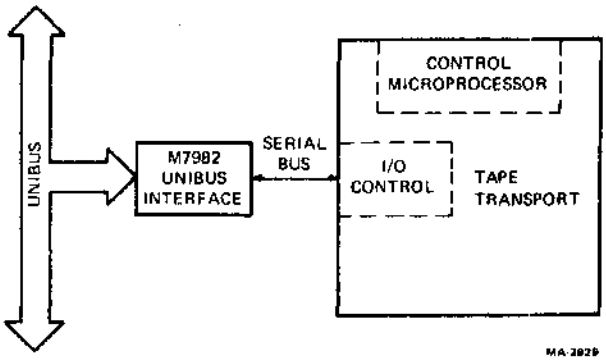


Figure 1-1 TS11 Subsystem Configuration

1.2 SUBSYSTEM OVERVIEW

Figure 1-1 shows the TS11 subsystem block diagram. The subsystem contains one transport, one TS11 interface module (M7982), and a serial bus interface cable.

The M7982 interface plugs into the Unibus and receives parallel data in the packet protocol format. (Packet protocol is discussed in Chapter 5 of this manual.) A serial bus interface cable then connects the interface to the transport. Parity for the transport command and data information is maintained and checked in the serial data stream. This ensures that an accurate transfer has been made on the serial bus interface cable.

During data transfers, the transport resident formatter controls data fetching, formatting, and transmission. It also oversees the handling of error corrections. Single track read errors are corrected by the hardware automatically. The read after write feature verifies accurate recording of data on the tape.

Each vertical frame of the 9-track tape represents one character of eight bits plus a parity bit. Groups of characters are combined to form records that, under program control, can vary in length. Each record block is separated by a formatted interrecord gap (IRG) that has a minimum length of 0.5 inches.

The TS11 features bidirectional tape reading. Writing occurs only while the tape is moving forward. Tape motion is controlled by a servo-controlled capstan. Tape buffering between capstan and reels is accomplished by low inertia tension arms.

The tape drive can be controlled locally from the front control panel. All operational tape motion is controlled by two pushbutton switches.

Whenever the TS11 is in standby mode for more than 500 ms, an extensive set of drive resident diagnostics is executed to assure the continued operating integrity of the TS11. These diagnostics exercise the electronics to the fullest extent possible short of moving the tape or altering data and status register contents.

The TS11 microprocessor controls such things as capstan speed; it monitors read and write strobe times, sets read and write voltage threshold levels, and determines the length of interrecord gaps. This advanced control system provides further confidence in the operating integrity of the TS11.

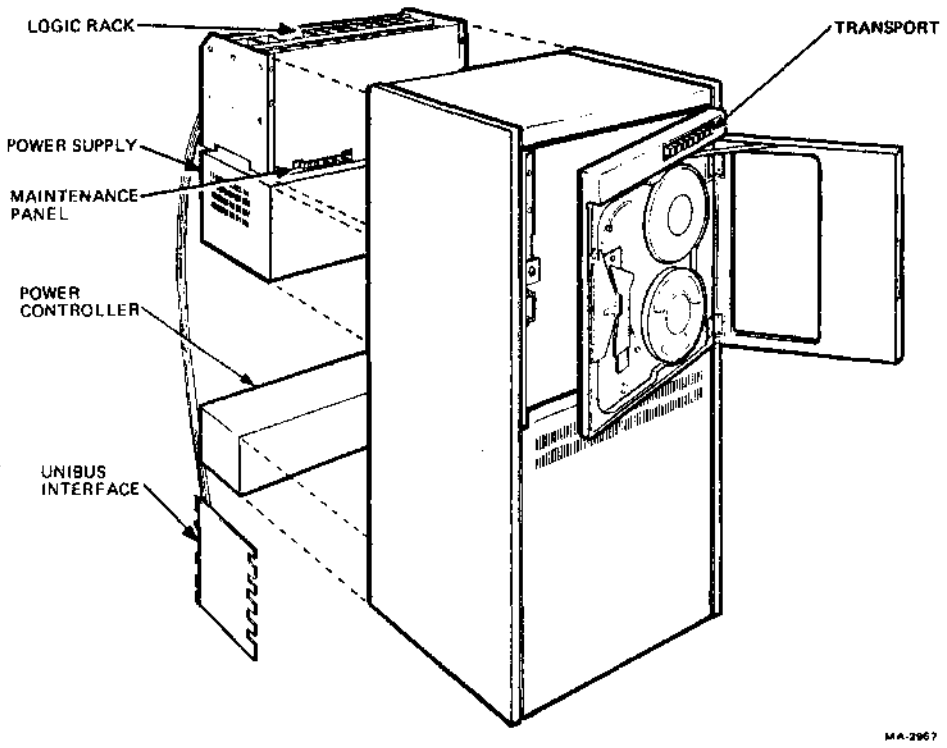


Figure 1-2 TS11 Subsystem Major Assemblies

1.3 PHYSICAL DESCRIPTION

Figure 1-2 shows the TS11 major assemblies.

1.3.1 Unibus Interface

The Unibus interface is a standard PDP-11 hex height, multilayer two sided module (M7982 module designation). It can be placed in any small peripheral controller (SPC) slot that is wired for all Unibus signals and accepts hex height modules. Also, it can plug into DD-11 series SPC backplanes in BA11 series expander boxes. This module links the transport with the Unibus via a serial bus interface cable.

NOTE

The nonprocessor grant (NPG) jumper must be removed when the M7982 is installed.

1.3.2 Transport

The tape transport subsystem (Figures 1-2 and 1-3) includes the following major assemblies.

Main deckplate
Reel servo
Capstan servo
Head assembly and read preamplifiers
Tape transport control and operator control logic
Power supply

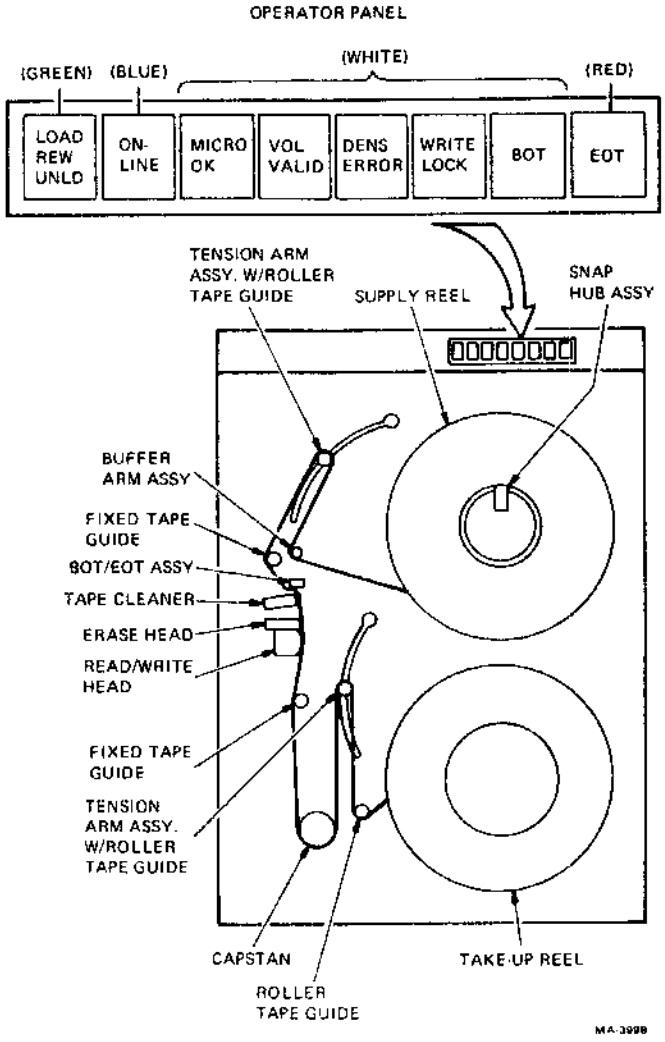


Figure 1-3 Transport Assemblies (Front View)

Main Deckplate – The main deck is die cast aluminum. It provides a single coplanar set of mounting surfaces. These machined surfaces become a single reference plane on which all tape path determining parts are mounted (Figures 1-2 and 1-3).

The casting, and hence the drive, is mounted to a cabinet rack by two hinge blocks. It swings out (hinged on the right side) to allow servicing. Also, for servicing, several reference pads are provided to check hub and reel alignment. The door, mounted to the same hinge area, can also be opened if the drive is swung outward.

Reel Servo – The reel servo consists of the supply reel servo motor and snap lock hub, take-up reel servo motor and take-up reel, G158 reel motor control module, and tension arm assemblies (Figures 1-3 and 1-4). All of these components mount directly to the main deck assembly.

The tension arms control tape tension and allow rapid tape start and stops without damage to the tape or servo motors. Tension arms also sense tape motion in order to drive the reel servo motors. The G158 module receives these signals and controls the speed and direction of both servo motors.

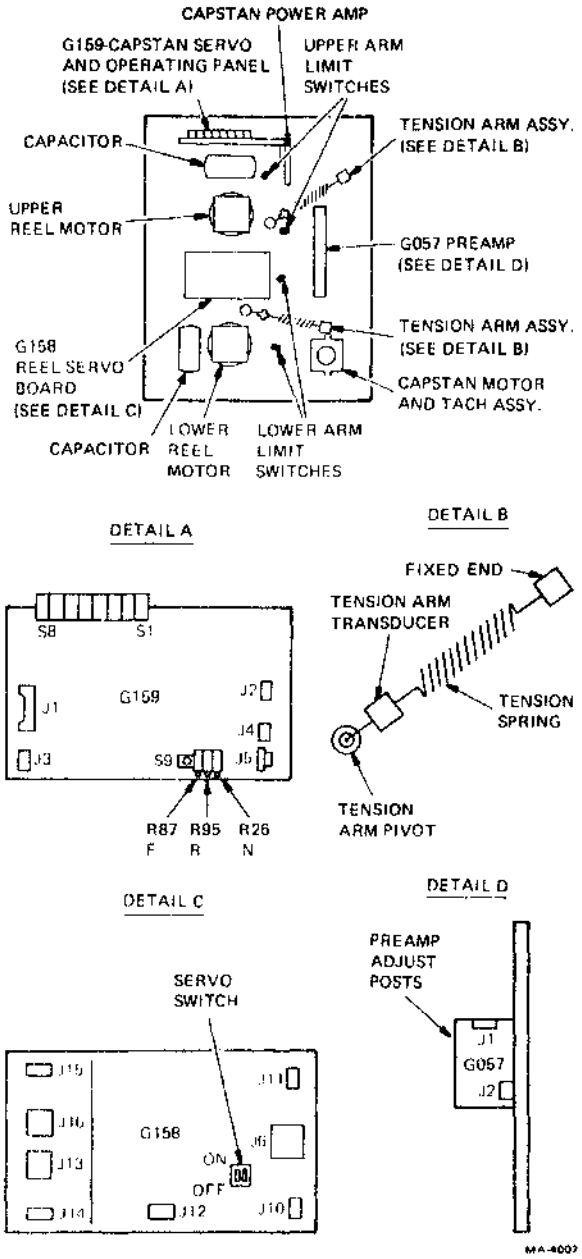


Figure 1-4 Transport Assemblies (Rear View)

Capstan Servo – The capstan servo system consists of the capstan motor/tachometer assembly and the G159 capstan servo module (Figures 1-3 and 1-4). The capstan motor assembly moves the tape across the read/write head. The G159 module sets the direction and drives the motor while the optical tachometer senses the tape speed. The optical tachometer then loops the information back to the G159 module, which in turn drives the capstan motor to the correct speed.

Head Assembly – The head assembly consists of a precision head mounting plate, read/write head, head tape guides, tape cleaner, erase head, and a BOT/EOT sensor (Figure 1-3). The head mounting plate provides a precision mounting surface for the head, cleaner, and guides.

The G057 module (read preamplifiers) is contained in a shielded enclosure and mounted to the rear of the deck casting.

Operator Controls – The transport (Figure 1-3) incorporates three lighted operator pushbuttons (colored) and five indicators (white). Chapter 4 details the operation of these controls.

These controls perform a dual function: operating and diagnostic control. Microdiagnostic errors are displayed in either mode. A switch on the printed circuit board backplane selects the mode.

Power Supply – All transport voltages are supplied by the TS11 power supply. The supply operates at 50 Hz or 60 Hz ± 1 Hz with no changes required. For 120 V or 240 V operation, only the ac input box and line cord need to be changed. A TS11K-AA kit converts a 240 V unit to 120 V and a TS11K-AB kit converts a 120 V unit to 240 V. The power system is modularized for easy maintenance and uses standard parts for increased reliability.

1.4 SYSTEM FUNCTIONAL DESCRIPTION

The functions listed in Table 1-1 make up the TS11 command set. These commands use device registers to operate the transport and to transfer data. This section describes register manipulation and provides an overview of packet protocol (the format used to transfer commands and data). Detailed descriptions of the commands are provided in Chapter 5 of this manual.

Table 1-1 TS11 Assigned Command Modes

Command Name	Mode Name
Get Status	Get status
Read	Read next (forward) Read previous (reverse) Reread previous (space reverse, read forward) Reread next (space forward, read reverse)
Write Characteristics	Load message buffer address and set device characteristics
Write	Write data Write data retry (space reverse, erase, write data)
Position	Space records forward Space records reverse Skip tape marks forward Skip tape marks reverse Rewind
Format	Write tape mark Erase Write tape mark retry (space reverse, erase, write tape mark)
Control	Message buffer release Rewind and unload Clean tape
Initialize	Drive initialize

Figure 1-5 is a simplified block diagram of the TS11. The transport is under the complete control of the microprocessor and related microcode. Two TS11 registers (TSBA and TSSR) are presented to the Unibus and communication between the CPU and the transport is via packet protocol (controlled by the microcode).

The TS11 (M7982) has eight registers which occupy only two Unibus word locations: a Unibus data buffer (TSDB), a Unibus address register (TSBA), and a status register (TSSR). The five additional registers elsewhere in PDP-11 memory provide status information.

The TSDB is an 18-bit register that is parallel loaded from the Unibus or serially loaded from the transport. A 16-bit portion of this register is used as a word buffer register to the M7982 when the M7982 is the bus slave (for beginning an operation). The same word buffer register is also used by the transport [for data during nonprocessor request (NPR) transfers] when the M7982 is the bus master. The TSDB can be loaded when the M7982 is the bus slave by three different transfers from a bus master. Two transfers are for

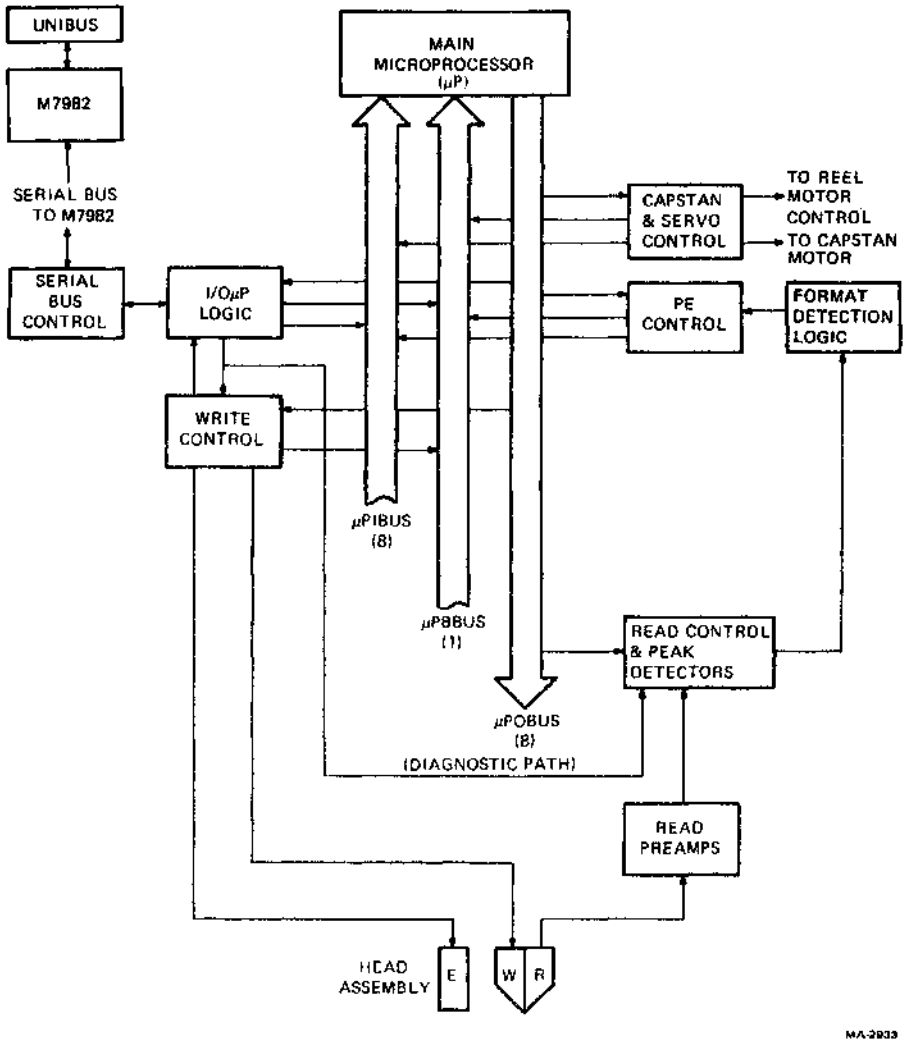


Figure 1-5 TS11 Simplified Block Diagram

maintenance purposes (byte transfer; DATOB at high/low byte). The third transfer is for normal (word) operation (DATO). This register is write only and is not cleared at power on, subsystem initialize, or bus initialize. It cannot be loaded without the complete transport unit connected (to supply a serial bus synchronous clock). The M7982 responds with SSYN (system synchronized) every time the TSDB is accessed.

Commands are not written to the drive's Unibus registers. Instead, command pointers, which point to a command packet somewhere in memory space, are written to the TSDB register. The command pointer is used in the TS11 to retrieve words in memory called the command packet. The words in the command packet instruct the transport as to the function to be performed. These words contain any function parameters such as bus address, byte count, record count, and modifier flags.

The TSBA is an 18-bit register that is parallel loaded from the TSDB every time the TSDB is loaded as Unibus slave. TSDB bits 15-2 load into TSBA bits 15-2; TSDB bits 1 and 0 load into TSBA bits 17 and 16; and zeros are loaded into TSBA bits 1 and 0. TSBA bits 17 and 16 are displayed in TSSR bits 9 and 8 respectively. The register can be instructed by the transport to increment or decrement by two for nonprocessor request (NPR) word transfers, or by one for NPR byte transfers. The TSBA register has two major purposes.

1. The TSBA can be used as a command pointer to the remote transport device registers (command and message buffers). These are located somewhere in the Unibus address space. The contents, loaded into the TSDB when the M7982 is the bus slave, is considered the command pointer. In this mode, the M7982 receives data (initiated by the transport) at this command pointer address and sends the command packet (data) to the drive unit for storage and/or execution.

2. The TSBA can be used as a data pointer, pointing to data buffer areas located somewhere in the Unibus address space. In this mode, the transport serially loads the TSDB with the data buffer address and transfers the contents of TSDB (0 to 17) into TSBA. The contents are then used to point to data buffer areas [while the M7982 transfers data by the NPRs (initiated by the transport)] and to message packets where the TSBA is left with the highest message buffer address + 2.

The TSSR is a 16-bit register that can be updated only from the transport or M7982 internal logic. It cannot be modified from the Unibus except for SPE, UPE, RMR, NXM, and SSR bits that are cleared when the TSDB is written by the host CPU. Here system status can be observed.

Before the TS11 can begin a function, a command packet must be assembled in the system memory. Every packet must have four words, even though not every command requires all four words. The packet may be thought of as three remote device registers (Figure 1-6).

1. Command Register (CMDR)

2. Data Pointer (DPR), which is made up of two word locations:

   Low order address word (A15:00) CMDR+2
   High order address word (A17:16) CMDR+4
   in bits 1 and 0

3. Positive Byte Count Register (BPCR)

   Data operations (DPR required) CMDR+6
   Nondata operations (no DPR required) CMDR+2

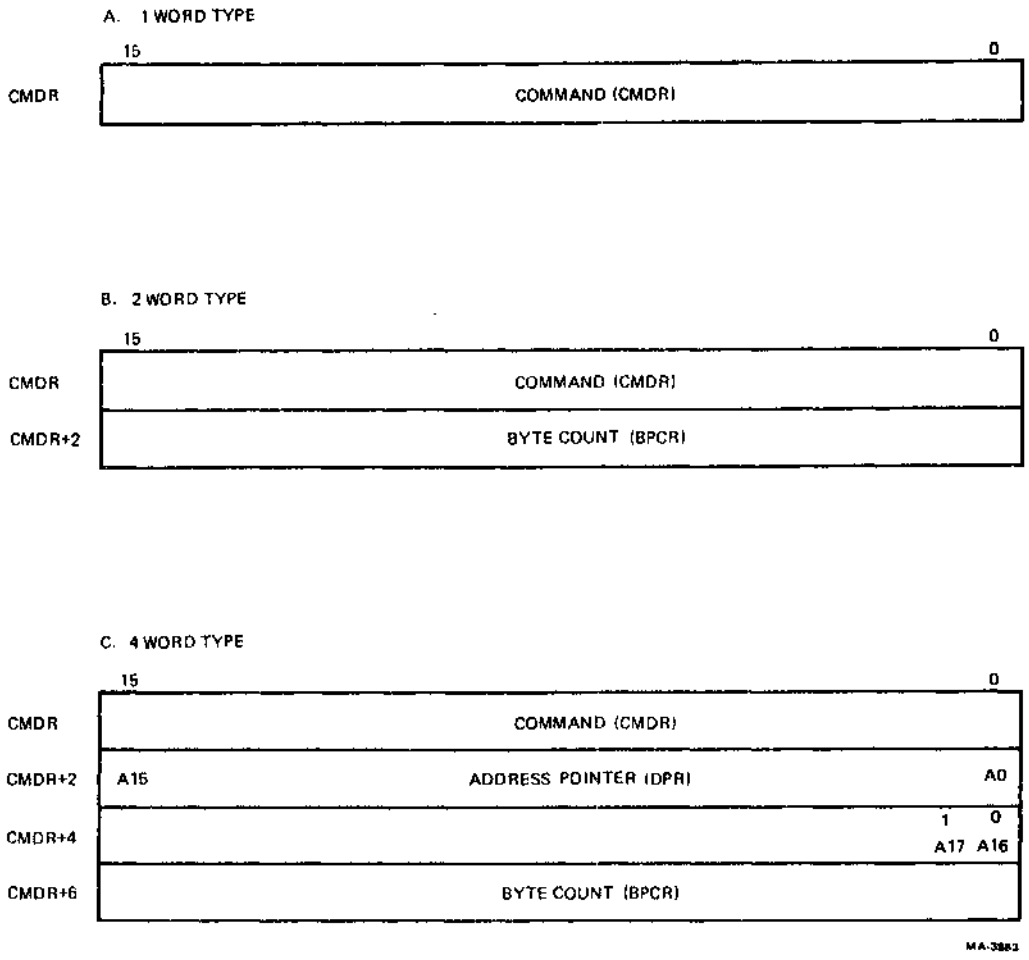


Figure 1-6 Command Packets

Message packets are issued by the transport and deposited in the host CPU memory space. These message packets contain complete device status information. Subsystem operation requires a message buffer address on a set characteristics command. This command must be the first command issued to the subsystem. Otherwise, all tape motion commands will be rejected.

The command pointer must be an address on a modulo-4 boundary (that is, beginning at 0, 4, 10, 14, etc.), because only the high order 16-bits can be specified by the command pointer.

The DPR is eventually loaded into TSBA to be used as the Unibus address for NPR data transfers. The BPCR is used to indicate the number of bytes (8-bits of data per byte) to be moved to or from the transport during a data transfer. It is also used to specify the number of records in a space record command or the number of files in a skip file command. The CMDR specifies the function the transport will execute.

Figure 1-5 is a simplified block diagram of the TS11. If a read forward operation is commanded, the following occurs. The capstan interface logic directs the capstan servo logic to supply motor current to the capstan servo. This moves the tape forward. When the tape is up to speed, the transport read logic is enabled and receives data from the read heads. The read data output of the read heads (RD0-RD7, RDP) is checked for vertical parity errors. If any such errors are detected, the transport error logic is notified to take appropriate corrective action.

Read data from the formatter is then sent to the main microprocessor via the microprocessor in bus (μPIBUS). Under microprocessor control, read data is then sent to the I/O control and sequencing logic via out bus (μPOBUS). From here, the I/O microprocessor transfers read data to the serial bus control logic via the I/O out bus (I/O OBUS), where the data is gated serially to the M7982 interface. A serial to parallel conversion occurs and the data word is parallel transferred to memory via the Unibus on the M7982.

If a write operation is commanded and the request is granted, the following occurs. The capstan servo logic supplies motor current to the capstan, moving the tape forward. The first data character is placed on the Unibus and enters the M7982 when requested by the microprocessor. Subsequent transfers occur and fill up the silo in the I/O microprocessor, before writing on tape occurs. When the tape is up to speed, transferring data characters begins. As data characters are written on tape, new characters are transferred to the silo. This occurs until all data is transferred from memory to silo, and finally, silo to tape. The preamble is loaded into the silo before write data. The postamble is loaded in after. All data transfers (serial transfers) are under the control of the I/O microprocessor. The data is sent via the serial bus cable to the serial bus control logic. The I/O bus then transfers data to the write control logic and on to the write heads. The main microprocessor checks the data for write errors by doing a read after write.

Refer to Chapter 6 for detailed TS11 operating information.

1.5 UNIT SPECIFICATIONS

Table 1-2 lists the operational, environmental, mechanical, and electrical specifications for the TS11.

Table 1-2 TS11 Subsystem Specifications

Category	Specifications
Main Specifications	
Storage medium	12.7 mm (0.5 in) wide magnetic tape (industry compatible)
Data transfer rate	72,000 characters per second, maximum
Transports per controller	1
Data Organization	
Number of tracks	9
Recording density	64 rows/mm (1600 bpi)
Interrecord gap	12.7 mm (0.5 in) minimum
Recording method	PE mode at 64 rows/mm (1600 bpi); conforms with ANSI DOC. X3.39-1973

Table 1-2 TS11 Subsystem Specifications (Cont)

Category	Specifications
Tape Motion	
Speed, forward and reverse	114 cm/sec (45 in/sec)
Rewind speed	380 cm/sec (150 in/sec) 3 minute average for 10.5 inch reel
Tape transport	Direct drive ac reel motors, servo controlled; capstan has biphase tachometer outputs; tension arm tape buffering with constant tension
Start distance	4.57 mm ± 0.5 mm (0.180 in ± 0.050 in)
Stop distance	4.11 mm ± 1.1 mm (0.162 in ± 0.050 in)
Start time	8 ms ± 1 ms
Stop time	8 ms + 1 ms, −2 ms
Tape Characteristics	
Width	12.7 mm (0.5 in)
Length	732 m (2400 ft) maximum
Type	Mylar base, iron-oxide coated (ANSI standard)
Thickness	0.038 mm (1.5 mils)
Tension	255 g (9.0 oz)
Reel diameter	26.7 cm (10.5 in)
Reel hub	9.37 cm (3.69 in) diameter (industry standard)
Mechanical	
Tape transport mounting	Mounts on slides in standard 48.3 cm (19 in) cabinet

Table 1-2 TS11 Subsystem Specifications (Cont)

Category	Specifications
Transport dimensions in rackmount option	
Depth	76 cm (30 in)
Width	48 cm (19 in)
Height	66 cm (26 in)
Weight	68 kg (150 lbs)
Electrical	
Frequency	50 Hz ± 1 Hz or 60 Hz ± 1 Hz
Voltage	90 Vac to 128 Vac or 184 Vac to 256 Vac single phase
Power	400 W (standby); 1200 W maximum (start/stop)
Input current (Transport)	10 A maximum at 90 Vac to 128 Vac; 5 A maximum at 184 Vac to 256 Vac
Input current (M7982 Interface)	3.5 A maximum at 5 Vdc
Environment	
Operating temperature	15° to 32° C (60° to 90° F)
Relative humidity	20% to 80%, with maximum wet bulb 25° C (77° F) and minimum dew point 2° C (36° F)
Maximum altitude	2438 m (8000 ft)
Other	
BOT, EOT detection	Photoelectric sensing of reflective strip (industry standard)
Skew control	Deskewing electronics in the tape transport correct static skew
Write protection	Write protect ring sensing on the tape transport
Magnetic heads	Nine track, dual gap read after write (full-width erase)

1.6 APPLICABLE DOCUMENTS

The documents listed in Table 1-3 are applicable to the TS11 system and are available through the local Digital Sales and Service Office or the Accessories and Supplies Group. See Paragraph 3.3.4 for details.

Table 1-3 Applicable Documents

Title	Number	Description
TS11 Subsystem User Guide	EK-0TS11-UG	Contains functional overview, installation, operating, and programming information.
TS11 Subsystem Technical Manual	EK-0TS11-TM	Combines the user guide with theory of operation and maintenance information.
TS11 Subsystem Pocket Service Guide	EK-0TS11-PS	Provides a quick reference to maintenance procedures for the trained service person.
TS11 Subsystem Illustrated Parts Breakdown	EK-0TS11-IP	Provides a listing and illustration of replaceable parts.
872 Power Controller	EK-00872-IP	
861 Power Controller	EK-00861-IP	
TS11 A	EK-TS11A-IP	
TS11 B	EK-TS11B-IP	
TS11 C	EK-TS11C-IP	
TS11 D	EK-TS11D-IP	
PDP-11 Processor and Systems Manual*		A series of maintenance and theory manuals that provide a detailed description of the basic PDP-11 system.
PDP-11 Processor Handbook†		A general handbook that discusses system architecture, addressing modes, the instruction set, programming techniques, and software.

* Applicable manuals accompany the system at the time of installation. The document number depends on the specific PDP-11 family processor.

† Use the processor handbook unique to the actual CPU.

1.7 AVAILABLE OPTIONS

Table 1-4 lists the options available for the TS11 subsystem.

Table 1-4 Available Options

Option	Description
TS11-AA	Rackmount with M7982 120 Vac, 50/60 Hz
TS11-AB	Rackmount with M7982 240 Vac, 50/60 Hz
TS11-BA	TS11-AA in H9602 corporate cabinet
TS11-BB	TS11-AB in H9602 corporate cabinet
TS11-CA	TS11-AA in H9646 cabinet
TS11-CB	TS11-AB in H9646 cabinet
TS11-DA	TS11-AA in H960 tall cabinet
TS11-DB	TS11-AB in H960 tall cabinet
TS11K-AA	TS11 240 Vac to 120 Vac conversion kit
TS11K-AB	TS11 120 Vac to 240 Vac conversion kit

CHAPTER 2
INSTALLATION

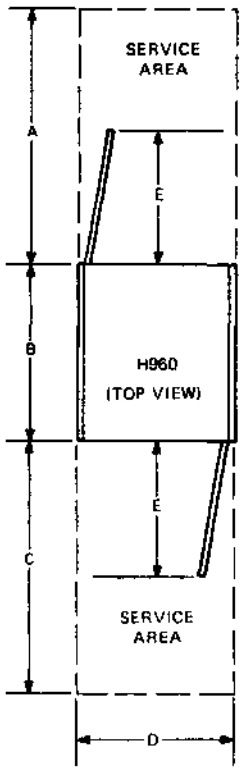
2.1 SITE PLANNING AND CONSIDERATIONS

Before installing the TS11 subsystem, careful site planning is necessary to satisfy physical and electrical requirements. These aspects of site preparation are discussed in the following paragraphs.

2.1.1 Space Requirements

The transport is available as a rackmount option or as an H960, H9602, H9646 cabinet. Figures 2-1, 2-2, and 2-3 respectively show the space and service clearance required for each cabinet.

The TS11 interface requires a single slot in an SPC backplane or DD-11 series SPC backplane in a BA11 series expander box. The transport must be located close enough to the M7982 mounting slot to accommodate an interconnecting cable of 7.4 m (25 feet).



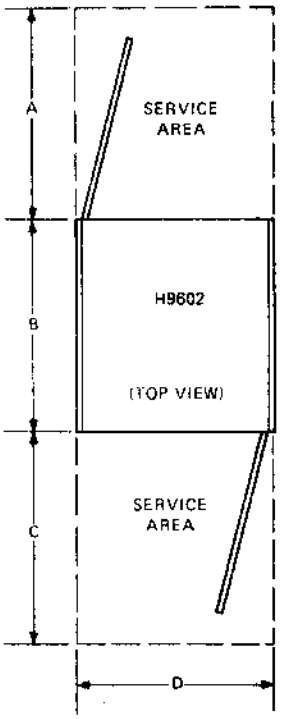
DIMENSIONS	A	B	C	D	E
INCHES	36	29	36	22	19.5
CENTIMETERS	91.5	73.7	91.5	55.9	49.5

NOTES:

1. REAR DOORS MAY BE LH OR RH. ALLOW SPACE FOR EITHER CASE.
2. CABINET IS 182.28 cm. (71 7/16 in.) HIGH (FLOOR LINE TO CABINET TOP).
3. IF THIS IS A STAND-ALONE OR THE END CABINET (ie., NO ADDITIONAL CABINET BOLTED TO THIS SIDE) THE END PANEL MUST BE REMOVED BEFORE THE TRANSPORT ASSEMBLY CAN BE SWUNG OPEN.

MA-3553

Figure 2-1 Space and Service Clearance, H960 Cabinet and Rackmount (Top View)



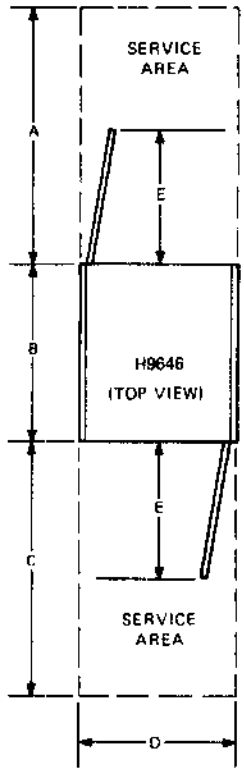
DIMENSIONS	A	B	C	D
INCHES	30	30	30	27.5
CENTIMETERS	76.2	76.2	76.2	09.9

NOTES:

1. REAR DOORS MAY BE LH OR RH, ALLOW SPACE FOR EITHER CASE.
2. TRANSPORT ASSEMBLY SWINGS OPEN RH ONLY. LOWER FRONT CABINET DOOR SNAPS ON AND OFF, IT DOES NOT SWING.
3. 127 cm (50 in.) OR 152 cm (60 in.) HIGH DEPENDING ON MODEL (FLOOR LINE TO CABINET TOP).

MA-3884

Figure 2-2 Space and Service Clearance, H9602 Cabinet (Top View)



DIMENSIONS	A	B	C	D	E
INCHES	36	30	36	22	19.5
CENTIMETERS	91.5	76.2	91.5	55.9	49.5

NOTES:

1. CABINET IS 152.3 cm (60 in.) HIGH (FLOOR LINE TO CABINET TOP).

MA-3983A

Figure 2-3 Space and Service Clearance, H9646 Cabinet (Top View)

2.1.2 Power Requirements

Both the 60 Hz ± 1 Hz and 50 Hz ± 1 Hz transports operate from 90 Vac to 128 Vac or 184 Vac to 256 Vac power sources. Operating input power is approximately 400 W nominal (standby), with an operating peak of approximately 1200 W. Maximum operating current in the low voltage range is 10.0 Arms maximum; in the high voltage range it is 5.0 Arms.

Table 2-1 provides a list of receptacles that accept the various voltages. The appropriate circuit breakers are also necessary.

The TS11 (M7982) typically draws 2.0 A, with a maximum of 3.5 A, calculated at +5 Vdc. No other voltage is required. A hex height SPC module is allowed to draw a maximum of 6 A at +5 Vdc (1 A maximum per module section) from an SPC slot. Do not exceed the power available to an SPC slot, DD-11 backplane, or expander box. Also, maximum usable SPC power is not always available in expander boxes. Be sure sufficient power is available.

Digital Equipment Corporation must be notified of available input power well in advance of shipment, so that the correct TS11 subsystem can be shipped.

2.1.3 Floor Loading

Table 2-2 lists floor loading data.

Table 2-1 TS11 Power Plugs and Receptacles

Rackmount	Plug	Receptacle
120 V NEMA	5-15P	5-15R
120 V Digital	90-08938	12-05351
240 V NEMA	6-15P	6-15R
240 V Digital	90-08853	12-11204
Digital Standard Cabinets (H960, H9602, H9646)	**Plug**	**Receptacle**
120 V NEMA	L5-30P	L5-30R
120 V Digital	12-11193	12-11194
240 V NEMA	L6-20P	L6-20R
240 V Digital	12-11192	12-11191

Table 2-2 Floor Loading

TS11 Option	Weight
TS11-AA/AB Rackmount (TS11 in mounting frame)	68 kg (150 lbs)
TS11-BA/BB Rackmount in H9602	231 kg (506 lbs)
TS11-CA/CB Rackmount in H9646	188 kg (415 lbs)
TS11-DA/DB Rackmount in H960	230 kg (504 lbs)

2.1.4 Installation Constraints

The route that the equipment will travel from the receiving area to the installation site should be studied in advance to ensure problem free delivery. Among the factors to consider are the height and location of loading doors, the size, capacity, and availability of elevators, the number and size of aisles and doors in route, and any restrictions, such as bends or obstructions, in the hallways. Any constraints should be reported to Digital Equipment Corporation as soon as possible, so that requirements of the individual installation site can be considered when the unit is packed for shipment.

Locate the TS11 in an area free of excessive dust and dirt or corrosive fumes and vapors. Place equipment so that cabinet fan inlets and air outlets are not obstructed in any way.

If the system you are installing is housed in an H9602 cabinet, the following precautions should be understood before installation.

1. Observe the caution symbols on the cabinet containers.

2. These cabinets arrive without shipping skids. A fork lift is not necessary, but one can be used if it lifts from the side of the cabinet.

3. When moving the cabinets, push them only on the side indicated by the caution symbols. The casters are locked to facilitate movement in the direction indicated.

4. Handle the cabinets carefully to avoid excessive shock.

CAUTION

Exercise special care when moving cabinets up or down ramps; they may become unstable when tilted more than 10 degrees.

2.1.5 Fire and Safety Precautions

The TS11 does not present unusual or additional fire or safety hazards to an existing computer system. However, check wiring carefully, to ensure that its capacity is adequate for the added load and for any contemplated expansion.

2.1.6 Temperature

The environmental operating temperature of the TS11 may range from 15° to 32° C (59° to 90° F); the maximum gradient is 17° C per hour.

2.1.7 Relative Humidity

Humidity control is very important in a data storage system environment. Static electricity, which varies with humidity, can cause errors in any CPU with memory. The TS11 operates efficiently in a relative humidity range of 20 to 80 percent with a maximum wet bulb temperature of 25° C (77° F) and a minimum dew point of 2° C (36° F).

2.1.8 Heat Dissipation

Heat dissipation of the transport is 900 Btu/hr nominal and 3800 Btu/hr maximum. The approximate cooling requirements for the system can be determined by performing the following calculations. Add the above figure to the maximum heat dissipation for the other system components. Then adjust the results to compensate for such factors as the number of personnel, heat radiation from adjoining areas, sun exposure through windows, system efficiency, etc. A safety margin at least 25 percent above the estimated cooling requirements is suggested.

2.1.9 Acoustics
While most computer sites require some degree of acoustic treatment, the TS11 should not contribute unduly to the overall acoustic problem. However, the acoustic materials at the site should not produce or harbor dust.

2.1.10 Altitude
Computer systems may encounter heat dissipation problems at high altitudes. At altitudes over 610 m (2000 ft), the maximum allowable operating temperature is reduced by a factor of 1.8° C for each 1000 m (1° F for each 1000 ft). The maximum altitude specified for the transport is 2438 m (8000 ft). Therefore, its maximum allowable operating temperature at 2438 m (8000 ft) would be reduced to 27.60° C (81.7° F).

2.1.11 Radiated Emissions
Radiation sources, such as FM or radar transmitters, in close proximity to the computer system may affect the operation of the processor and some peripheral equipment. The effects of these emissions can be minimized by the following actions.

1. Ground window screens and other large metal surfaces.
2. Shield interconnecting cables with a grounded shield.
3. Provide additional grounding to the system cabinets and chassis.

In environments subject to extreme radiation, the system may require a grounded cage.

2.1.12 Required Tools
In addition to the standard DEC Tool Kit (PN 29-18303), a spirit level is also required for unpacking and installation.

2.2 UNPACKING
The TS11 may be shipped in four variations: as a rackmount version, or three cabinet styles (H960, H9602, or H9646). Unpacking and installation procedures vary with the choice of cabinets.

No matter which variation is chosen for the transport, the device is shipped with all interconnecting cables installed. The M7982 Unibus interface module is delivered in a separate package.

When packaged for shipment, the transport in its cabinet weighs up to 230 kg (500 lbs). Although the package is excessively heavy and bulky for single-person handling, it does not require the use of a forklift or similar equipment to move or lift it.

CAUTION

When moving or lifting the transport, always grasp the frame structure. Do not hold any part of the top or side covers.

2.2.1 Rackmount Option

Unpack the rackmount option as follows.

1. Remove the outer shipping container.

> NOTE
> **The container may be heavy corrugated cardboard or plywood. In either case, remove any fasteners and cleats securing the container to the skid. If applicable, remove wood framing and supports from the perimeter.**

2. Remove the polyethylene cover from the transport. The transport is now ready to be mounted in its cabinet.

> CAUTION
> **The TS11 AA/AB option weighs 68 kg (150 lbs). A minimum of two people are needed to move the transport to its mounting place.**

2.2.2 H960 Cabinet Unpacking

Unpack the H960 cabinet as follows.

1. Remove the outer shipping container.

> NOTE
> **The container may be heavy corrugated cardboard or plywood. In either case, remove any fasteners and cleats securing the container to the skid. If applicable, remove the wood framing and supports from the cabinet perimeter.**

2. Remove the polyethylene cover from the cabinet.

3. Unbolt the cabinet(s) from the shipping skid. Remove the bolts located on the lower supporting side rails; they are exposed by opening the access door(s).

4. Raise the leveling feet above the level of the roll around casters. Refer to Figure 2-4.

5. Use wood blocks and planks to form a ramp from the skid to the floor. Carefully roll the cabinet onto the floor.

6. Roll the system to the proper location for installation.

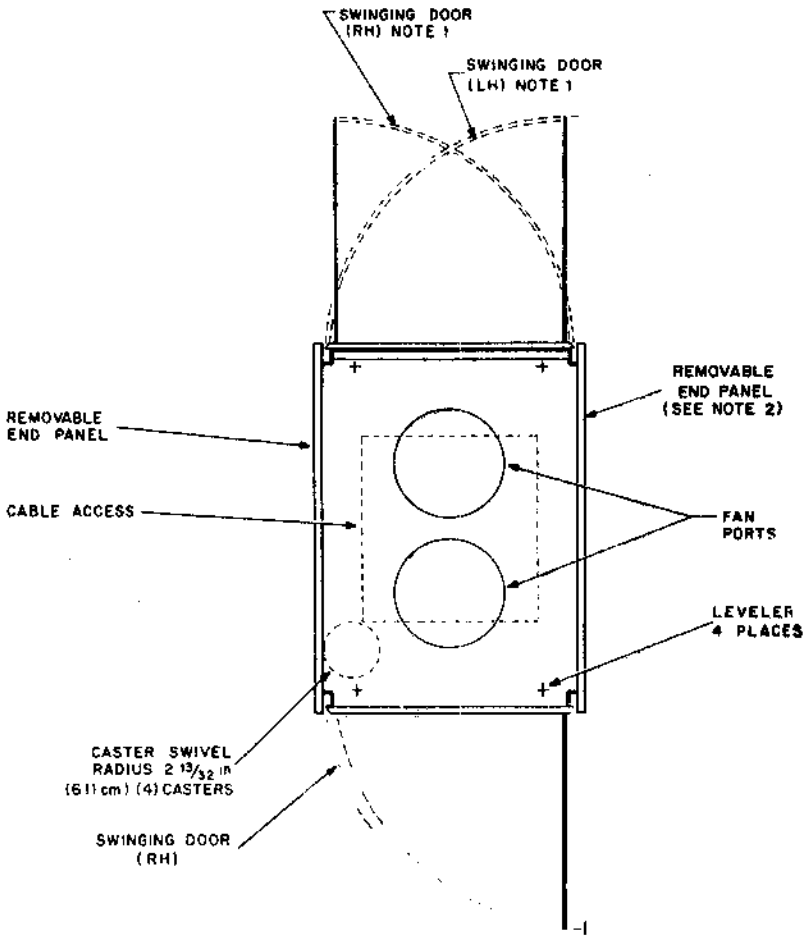


Figure 2-4 H960 Cabinet Installation

2.2.3 H9602 Cabinet Unpacking

Unpack the H9602 cabinet as follows.

1. Unbolt the bottom protector from the crate at the front, back, and sides. Remove the protector.
2. Unbolt and remove the front panel of the crate.
3. Slide the sides, back, and top panels off, as one piece.

NOTE

Following step 3 will ensure that the cabinet face is not damaged. Do not ship the crating material back to the factory; it can be discarded or retained for reshipping, if reshipping is necessary.

4. Ensure that the leveling feet are above the level of the shock isolating casters (Figure 2-5).
5. Roll the cabinet(s) to the proper location for installation.

2.2.4 H9646 Cabinet Unpacking

Unpack the H9646 cabinet as follows.

1. Cut the binding straps and remove the bottom foam protector and top cardboard protector.

NOTE

This unit is shipped on shock isolating casters. No skid is used.

2. Roll the unit to the proper location for installation.

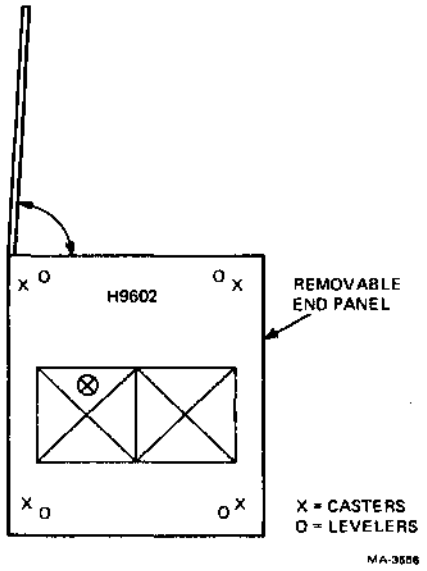


Figure 2-5 H9602 Cabinet Installation

2.3 INSPECTION

After removing the equipment from its container, inspect it and report any damage to the responsible shipper and the local Digital sales office. Inspect the equipment in the following manner.

1. Inspect all switches, indicator/switches, and panels for any obvious damage.

2. Open or remove equipment covers, where necessary, and inspect for loose or broken modules, blower or fan damage, and loose nuts, bolts, screws, and cable connections.

3. Inspect the wiring side of the logic enclosure panel (motherboard assembly) for bent pins, broken wires, and any foreign material.

4. Check the transport for any foreign material that may be lodged in the take-up reel or in other moving parts.

5. Check the transport power supply to make sure the fuses and power connectors are seated properly.

2.4 TRANSPORT INSTALLATION AND CABLING

This section provides procedures for installing and cabling the TS11.

CAUTION

For all installations, the transport must be adjacent to or bolted to the cabinets in which the M7982 is installed. A ground cable must connect the TS11 frame to the cabinet. This provides shielding for the data cable and reduces local amounts of EMI/RFI from entering the system.

2.4.1 Rackmount Installation

The TS11 AA/AB option can be installed in any standard 19-inch RETMA cabinet. Complete documentation and installation instructions are shipped with the option.

CAUTION

The TS11 AA/AB option weighs 68 kg (150 lbs). A minimum of two people are needed to move the transport to its mounting place.

NOTE

Some side skins and top covers for this style of cabinet may interfere with service clearances.

2.4.2 H960 Cabinet Installation

Install a TS11 shipped in an H960 cabinet as follows.

1. Lower the leveling feet so that the cabinet is resting on them, not on the roll around casters.
2. Use a spirit level to level the cabinet. Make sure that all leveling feet are resting firmly on the floor.
3. Remove the shipping screws that secure the equipment to the cabinet.
4. When this cabinet is bolted to another H960 cabinet, install filler strips (Filler Strip Set, PN H952-GA) between the cabinets as shown in Figure 2-6. Make sure that the notched strip is mounted at the cabinet fronts. Tighten the bolts that secure the cabinets together and then re-check to ensure that the cabinets are level.
5. Remove the plastic shipping pin from the top of the cabinet rear access door.
6. Install a cabinet ground strap from the transport frame directly to the M7982 mounting box.
7. Replace the end panels and doors as needed.
8. Install the safety stabilizer legs to the front of the cabinet.
9. If necessary, clean all the outer surfaces.

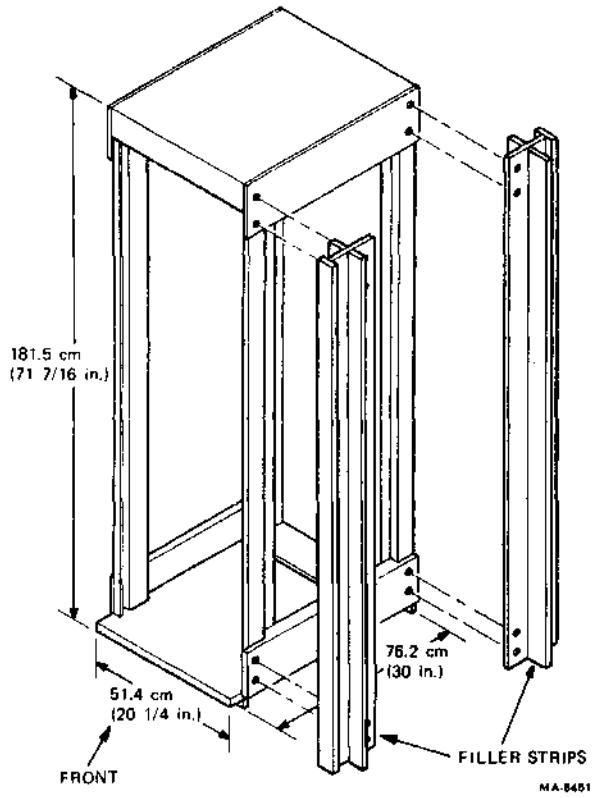


Figure 2-6 H960 Cabinet Filler Strips

2.4.3 H9602 Cabinet Installation

This section lists installation procedures for a TS11 shipped in an H9602 cabinet.

2.4.3.1 Cabinet Disassembly – All H9602 cabinets must be dissasembled before installation.

NOTE

Separate ground straps (10 gauge stranded wire) connect the front panel, end panel, and the back door to the cabinet frame. To completely remove each panel, separate the panel from the frame (instructions below), disconnect the ground strap, and completely remove the panel.

After you remove the shipping crate, disassemble the cabinet as follows.

1. An array of vertical slots constitute venting in the cabinet front cover. A quick release latch is located approximately 2.5 cm (1 inch) behind each end of this array. Insert a thin bladed tool, such as a small steel rule, into one of the end slots. Push on the latch while simultaneously exerting a forward pull to release one corner of the front cover. In the same manner, while continuing to exert a forward pull, release the remaining latch at the other end of the array. This will totally free the front panel.

2. Leveler pads are wrapped in blister wrap and taped to the inside of the front cover. Remove the leveler pads.

3. Raise the interlock rods and remove the stabilizers from the stabilizer sleeve assemblies (Figure 2-7).

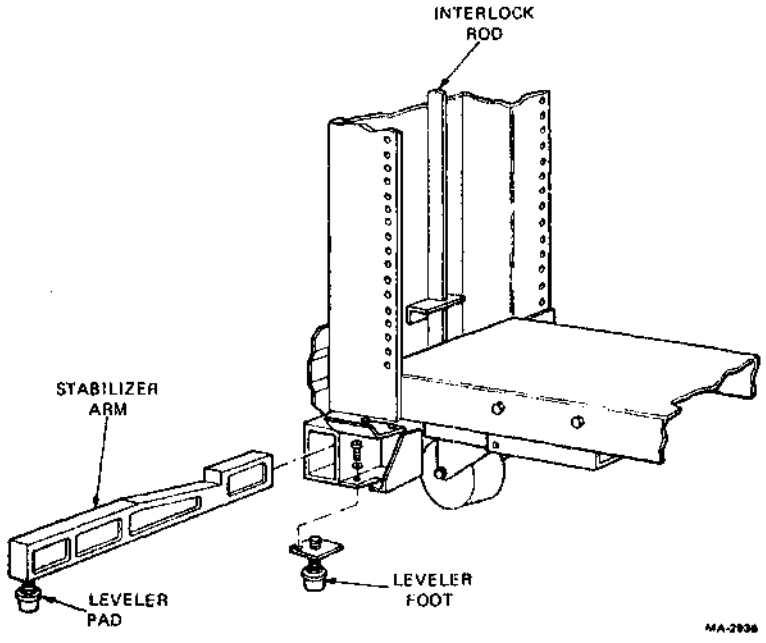


Figure 2-7 H9602 Stabilizer Leg and Leveler Feet Locations

4. Screw the leveler pads into the stabilizers.

5. Raise the interlock rods and reinsert the stabilizers into the stabilizer sleeve assemblies (Figure 2-7).

6. Unlock the rear door using the opening tool provided for that purpose. Insert the tool in the lock and turn one quarter turn counterclockwise. Remove the door by swinging it open 90 degrees and lifting it off at the hinges.

7. Locate the fastener attached to the underside of the top cover. If any hard mounted equipment is blocking access to the underside of the top cover, the fastener was not installed. Therefore, you must proceed to step 8. If slide-mounted equipment is blocking access to the top cover, pull the stabilizer legs out until they are fully extended to the locking position. Then slide the equipment out and proceed to step 8.

8. Release the top cover by turning the fastener one quarter turn counterclockwise. When it is released, the fastener hangs by a wire from the cover support. Push the top cover forward approximately 1.27 cm (0.5 inch). Then proceed to the front of the cabinet and lift off the cover.

9. Remove one end panel by grasping it by both sides and lifting. Remove the other end panel the same way.

10. Use a phillips screwdriver to remove the trip strips from the top, front, and rear cabinet edges.

2.4.3.2 Caster Locks – Caster locks (PN 7417593) are supplied with each cabinet frame (Figure 2-8). They facilitate cabinet movement by preventing two of the four cabinet casters from swiveling. They also help provide cabinet stability by restricting the direction of cabinet movement. The caster locks are mounted with hardware; they may be removed if moving the cabinet during installation becomes absolutely necessary. In any case, the locks are to be removed when the cabinet has been installed at its final destination. The locks are to be stored with the cabinet; they can be used in the future if the cabinet has to be moved.

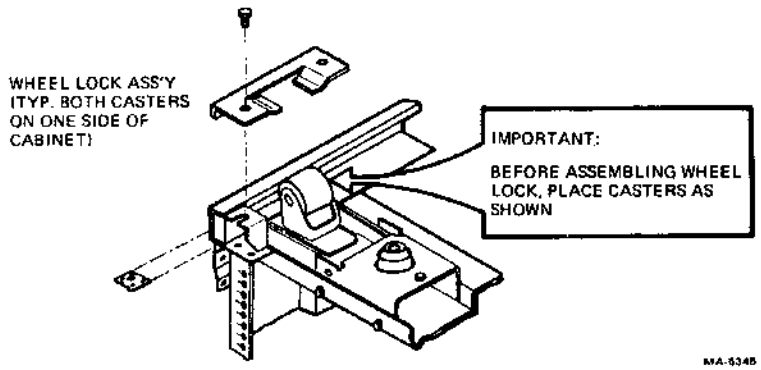


Figure 2-8 Caster Lock Assembly

2.4.3.3 Cabinet Leveling – Cabinet leveling is the next procedure to perform. Individual cabinets must be leveled before bolting any cabinets together. This action is necessary because of the weight differentials and self-contained shock mounts. Push the cabinets together until they adjoin. Level them as follows. (Also use this procedure for leveling a single standalone cabinet.)

1. Install the leveler feet in four places on each cabinet frame (Figure 2-7).

2. Using a 9/16 inch wrench, lower the leveler feet until all four feet on each cabinet contact the floor.

3. Adjust the highest cabinet until most of its weight is shifted from the casters to the leveler feet.

4. Using a spirit level, adjust the leveler feet until the cabinet is level.

5. Adjust the adjoining cabinet(s) to the level of the highest cabinet.

2.4.3.4 Bolting Cabinets Together – Each H9602 cabinet has four bolting plates; there are two on each side, located at the upper and lower edges. Bolt cabinets together as follows.

1. Align the bolting (middle) hole at each end of each bolting plate with the bolting hole on the plate of the adjoining cabinet.

2. After aligning the bolting holes of both cabinets, insert 1/4-20 bolts into the holes and secure them with kep nuts. (The bolts and nuts are provided.) Bolting the cabinets in this manner provides horizontal alignment.

3. After the cabinets have been bolted together, extend the stabilizer legs and lower the adjustable leveler pad on each leg until each pad touches, yet easily slides along the floor.

2.4.3.5 Cabinet Reassembly – Reassemble each cabinet as follows.

1. Insert screws to hold the top trim strips in place.

2. Add the front and rear vertical trim strips.

3. Remount all the panels and doors in the following sequence.

   End panels
   Top cover
   Rear door
   Front panel

2.4.4 H9646 Cabinet Installation

This section provides H9646 cabinet installation procedures.

2.4.4.1 Rear Door Removal – Remove the rear door as follows.

1. Unlock the rear door using a 5/32 inch hex key.
2. Disconnect the ground wire.
3. Unlatch the door (top latch pulled down) and lift off.

2.4.4.2 End Panel Removal – Remove the end panel as follows.

1. Remove the hinge/end panel locking brackets by loosening screws. Lift brackets off.
2. Lift panels up and away from the cabinet.
3. Remove the ground strap and save for later use.

2.4.4.3 Leveling Feet Installation – Install the leveling feet as follows.

1. Assemble the leveling feet and slide them into the slot at the base of the cabinet. The slots are located on the sides (Figure 2-9).

2.4.4.4 Cabinet Leveling – Level the cabinet as follows.

1. Use a spirit level and adjust the leveler feet as required.

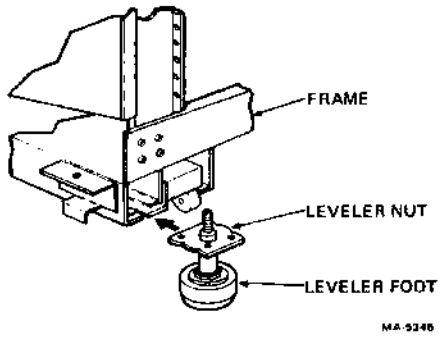


Figure 2-9 H9646 Leveler Foot Locations

2.4.4.5 Cabinet Stabilizers – Install the cabinet stabilizers as follows.

1. Assemble leveler foot into the stabilizer arm.
2. Install the arm into the channel located at the bottom rear of the cabinet.
3. Remove the retaining cable from the rear of the cabinet base and attach it to the rear of stabilizer arm. (This limits the forward travel of the arm.)

2.4.4.6 Bolting Cabinets Together – Bolt the cabinets together as follows.

1. Remove the end panels where the cabinets will be joined.
2. Install the H9544-J add-on kit as follows. Screw the key buttons into the cabinet sides of both cabinets. Drop the add-on panel onto the key buttons of the stationary cabinet.
3. Roll the add-on cabinet into position (Figure 2-10) so the add-on cabinet can be pushed onto the key buttons of the stationary cabinet.
4. Pull the add-on cabinet forward to it into the key button slots (Figure 2-10).
5. Install the front and rear interconnecting bars as shown in Figure 2-11.

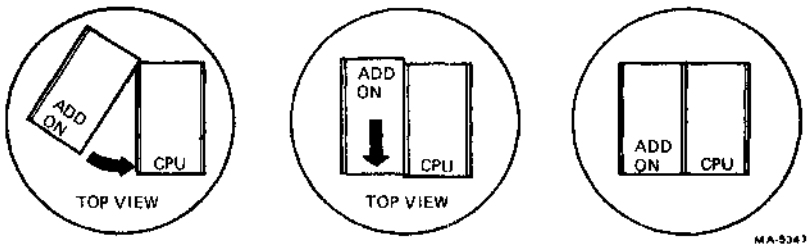


Figure 2-10 H9646 Add-On Positioning

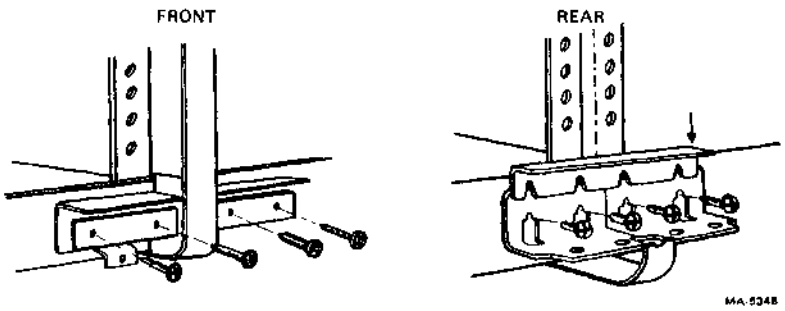


Figure 2-11 H9646 Interconnecting Bars

2.5 TS11 INTERFACE INSTALLATION

NOTE
The M8929 module must be Etch Rev. D (Circuit Schematic Rev. F) minimum to be FCC compliant.

The M7982 Unibus interface module can be placed in any small peripheral controller (SPC) slot that is wired for all Unibus signals. It accepts hex height modules and has adequate power including DD-11 series SPC backplanes in BA11 series expander boxes.

NOTE
The nonprocessor grant (NPG) jumper (CA1 to CB1) must be removed before the M7982 can perform data transfers. If the M7982 is removed from the SPC slot, insert a module that passes NPG or replace the jumper.

Install the TS11 (M7982) as follows.

1. Remove the TS11 (M7982) from its shipping container.
2. Make sure that the correct priority plug (BR5/BG5; PN 54-08778) is installed in E57 (Figure 2-12).
3. Select the correct Unibus address and interrupt vector. Use Table 2-3 as a guide.
4. Use Figure 2-12 and Table 2-4 to correctly configure the address switch (E90) and interrupt vector switch (E34).

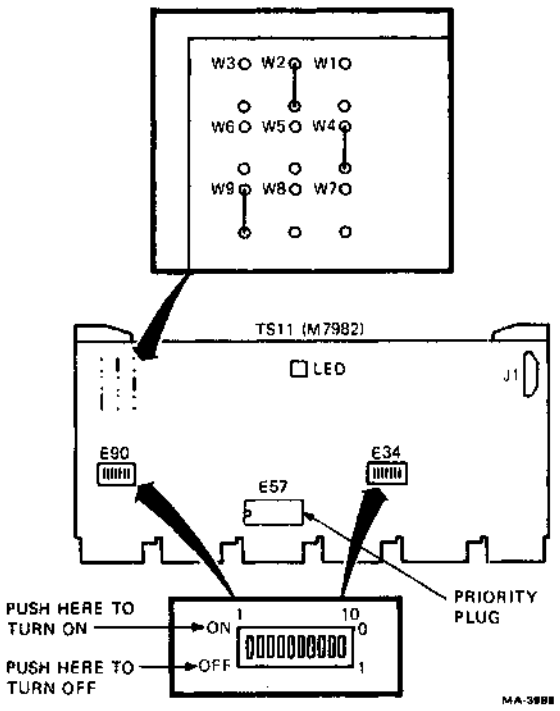


Figure 2-12 M7982 Interface Module

Table 2-3 Unibus Address and Interrupt Vectors

Number of M7982 Modules	Interrupt Vector	Unibus Address	Register
1	224	772 520 772 522	TSBA/TSDB TSSR
2	Floating (rank 37)	772 524 772 526	TSBA/TSDB TSSR
3	Floating (rank 37)	772 530 772 532	TSBA/TSDB TSSR
4	Floating (rank 37)	772 534 772 536	TSBA/TSDB TSSR

Table 2-4 Address and Vector Examples

Address

7			7			2			5			2			0		
17 22	16 22	15 22	14 22	13 22	12 22	11 22	10 22	9 22	8 22	7 22	6 22	5 22	4 22	3 22	2 22	1 22	0 22
x	x	x	x	x	1	0	1	0	1	0	1	0	1	0	0	x	x
					E34					E90							
x	x	x	x	x	1	1	10	9	8	7	6	5	4	3	2	x	x
x	x	x	x	x	off	on	off	on	off	on	off	on	off	on	on	x	x

Vector

0			0			0			2			2			4		
x	x	x	x	x	x	11 22	10 22	9 22	8 22	7 22	6 22	5 22	4 22	3 22	2 22	1 22	0 22
x	x	x	x	x	x	x	x	x	0	1	0	0	1	0	1	x	x
												E34					
x	x	x	x	x	x	x	x	x	8	7	6	5	4	3	2	x	x
x	x	x	x	x	x	x	x	x	on	off	on	on	off	on	off	x	x

on = 0; off = 1; x = Don't care

5. Make sure jumpers W1 through W9 are set correctly as shown in Figure 2-12. W2, W4, and W9 should be set in; all others should be set out.

6. Remove the G727 bus grant card from the SPC slot.

7. Insert the 7-foot CPU adapter cable (PN 17-00450-01) into J1 of the interface module with the red reference edge toward the handle. Figure 2-12 shows the location of J1.

8. Insert the interface module into the backplane. Use care to prevent the cable from chaffing against other modules and chassis parts.

9. Mount the 7-foot adapter to the CPU bulkhead (Figure 2-13).

10. Install a ground strap directly from the M7982 mounting box to the transport frame.

2.5.1 Cabling

The external interface cable (BC18B-15) connects from the I/O connector bracket on rear of TS11 power supply to the CPU bulkhead. The 7-foot CPU adapter cable connects from the M7982 to the CPU bulkhead (Figure 2-13).

NOTE

The 7-foot cpu adapter cable attaches to the M7982 with the red reference edge toward the handle. The 18-inch adapter cable attaches to the motherboard with the red reference edge to the left.

Route cables to allow slack for servicing the equipment. Keep the cables away from sharp frame edges.

CAUTION

Before connecting the transport to the local power source, make sure the line voltage and frequency are compatible with transport power requirements.

NOTE

All TS11 configurations must have ground straps installed between the transport frame and the host CPU.

Plug the power cable, supplied with the TS11 option, into a local power outlet.

Although all the internal cables are connected before shipping, Figure 2-13 provides an overview of transport cabling.

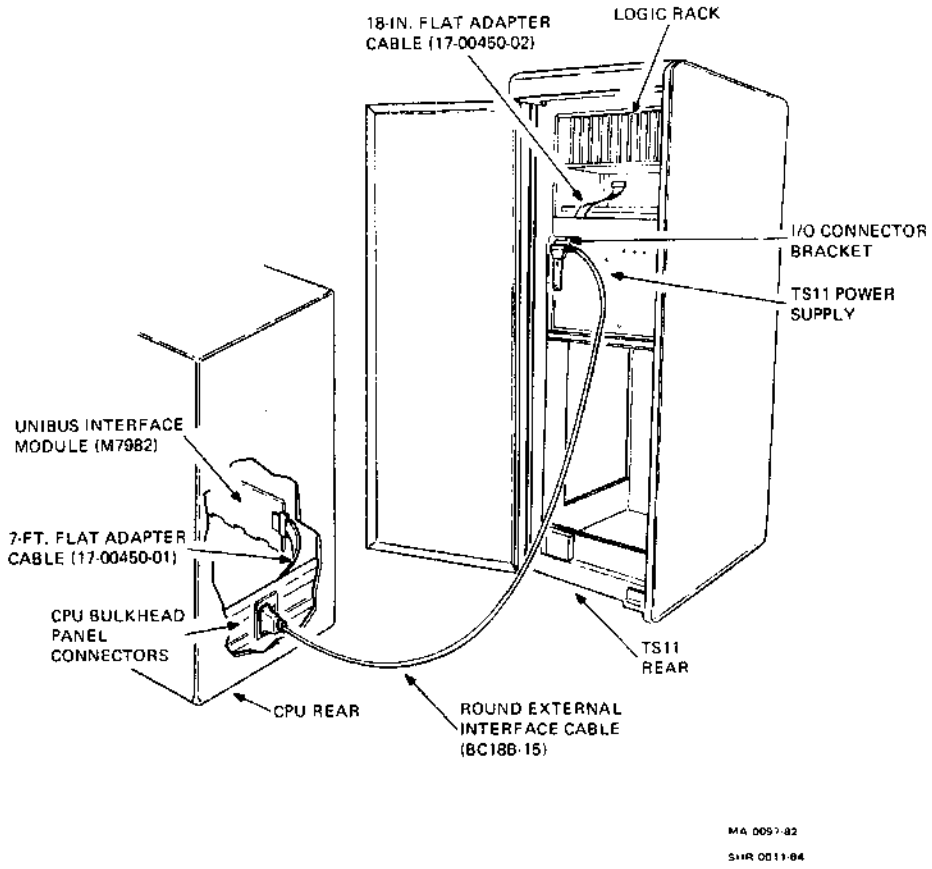


Figure 2-13 TS11 Signal Cabling

2.6 CONFIGURATION GUIDELINES

Up to four M7982 interface modules may be configured into a host system. The first M7982 has been assigned interrupt vector 224, while the second, third, and fourth are assigned vectors from the floating vector area. Therefore, it is necessary to know the next available floating vector to assign subsequent addresses.

Because the standard data cable length is 8 m (25 feet), placement of cabinets should be within 5 m (15 feet) of the host system.

The standard power cable length is 2 m (6 feet) for the rackmount and 3 m (9 feet) for the cabinet options.

2.7 ACCEPTANCE TESTING

This section lists and describes all the tests and test procedures necessary to test and accept the TS11. When the tests are run correctly, the TS11 is operating correctly. Refer to Chapter 7 and the *TS11 Subsystem Pocket Service Guide* for detailed procedure.

2.7.1 TS11 Off-Line Checkout

Off-line checkout is accomplished by successful completion of the off-line maintenance mode microdiagnostics. (These are run in auto sequence mode.) These tests require the use of a special test tape. Refer to Chapter 7 or the *TS11 Subsystem Pocket Service Guide* for complete operating details and instructions.

2.7.2 Customer Confidence Check (Optional)

Run this check twice (with a special test tape loaded) to ensure that the transport is adjusted properly and that the transport is operational. Refer to Chapter 4 for operating instructions.

2.7.3 Corrective Maintenance Diagnostics (On-Line)

Run the appropriate diagnostic (PDP-11 series or VAX) for one complete pass, including adjustments, as required by printouts and the program listing. Refer Paragraph 7.4.3 or the *TS11 Subsystem Pocket Service Guide* for details.

CHAPTER 3
USER INFORMATION

3.1 CUSTOMER RESPONSIBILITIES

The customer is directly responsible for the following tasks.

1. Obtaining operating supplies, including magnetic tape and cleaning supplies.
2. Maintaining the required logs and report files consistently and accurately.
3. Making the necessary documentation available in a location convenient to the system.
4. Keeping the exterior of the system and the surrounding area clean.
5. Ensuring that ac plugs are securely plugged in each time the equipment is used.
6. Performing the specific operations for equipment care described in Paragraphs 3.2 and 3.3 at the suggested periods, or more often if usage and environment warrant.

3.2 CARE OF MAGNETIC TAPE

1. Do not expose magnetic tape to excessive heat or dust. Most tape read errors are caused by dust or dirt on the read head; keeping tape clean is imperative.
2. Always store tape reels inside containers when the tape is not in use; keep empty containers tightly closed to guard against dust and dirt.
3. Never touch the portion of tape between the beginning of tape (BOT) and end of tape (EOT) markers; oil from fingers attracts dust and dirt.
4. Never use a contaminated reel of tape; this spreads dirt to the clean tape reels and could adversely affect tape transport reliability.
5. Always handle tape reels by the hub hole; squeezing the reel flanges leads to tape edge damage when winding or unwinding tapes.
6. Do not smoke near the tape transport or storage area; tobacco smoke and ash are especially damaging to tapes.
7. Do not place magnetic tape near line printers or other devices that produce paper dust.
8. Do not place magnetic tape on top of the tape transport or in any other location where it may be affected by hot air.
9. Do not store magnetic tape near electric motors.

3.3 CUSTOMER PREVENTIVE MAINTENANCE

Digital Equipment Corporation tape transports are highly reliable precision instruments that provide years of trouble-free performance when properly maintained. A planned program of routine inspection and maintenance is essential for optimum performance and reliability. The following information will assist the customer in caring for equipment.

3.3.1 Preventive Maintenance

To ensure trouble free operation, a preventive maintainance schedule should be kept. Preventive maintenance consists of cleaning only a few items, but the cleanliness of these items is essential to proper tape transport operation. The frequency of maintenance operations will vary with the environment and the degree to which the transport is used. Therefore, a rigid schedule for all machines is difficult to define. Cleaning after every eight hours of operation is recommended for units in constant operation in ordinary environments. This schedule should be modified if experience shows other periods are more suitable. Paragraph 3.3.3 contains the cleaning instructions.

Before performing any cleaning operation, remove the supply reel and store it properly. When cleaning, be gentle but thorough.

CAUTION

Do not use acetone, lacquer thinner, rubbing alcohol, or trichlorethylene to clean the tape path.

3.3.2 Magnetic Tape Transport Cleaning Kit

A magnetic tape transport cleaning kit (TUC01) has been carefully assembled to provide cleaning materials that will not harm tape equipment or leave any residue to interfere with data reliability. The hints contained in the following few paragraphs will ensure that the very best results will be obtained from the kit.

The cleaning fluid in this kit is one of the best cleaners available. Unscrew the top and punch a small hole in the metal seal covering the pour spout.

WARNING

When using DECmagtape cleaning fluid, avoid excessive skin contact and contact with the eyes. Do not swallow it. Use the cleaning fluid only in a well-ventilated area.

When cleaning tape equipment, never dip a dirty cleaning swab or wipe into the can. To transfer fluid onto the swab, pour a little into the screw cap and dip the swab into the cap. Discard the remaining fluid when the cleaning operation is complete.

Always keep the can of fluid tightly closed when not in use; the fluid evaporates rapidly when exposed to air.

Use the cleaning materials from the kit to clean tape heads, tape guides, tape cleaner, capstan, reel hubs, and any part of the drive where dirty residue could ultimately contact the tape. To clean other parts of the drive, such as the exterior surfaces of doors, use any reasonably clean, lint-free material with or without cleaning fluid.

CAUTION

To clean the capstan, use only the cleaning fluid provided in the TUC01 cleaning kit. Other cleaning fluids may damage the capstan. Never use alcohol.

Should you encounter any unusually stubborn dirt deposit that resists the cleaner, try a mild soap and water solution to dislodge it. After using soap, be sure to wash down the affected area thoroughly with cleaning fluid to remove soapy residue.

3.3.3 Cleaning the TS11 Subsystem Transport

Use this procedure to clean the TS11.

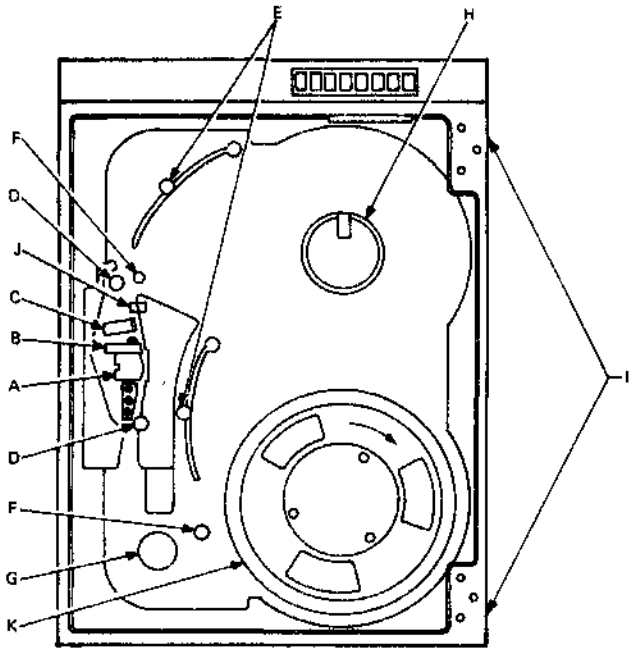
1. Dismount the tape from the unit.

2. Clean the following components of the transport, using a foam-tipped swab soaked in cleaning fluid (Figure 3-1).

   Read/write head (A)
   Erase head (B)
   Tape cleaner (C)
   Two fixed headtape guides (D)
   Tension arm assemblies with roller tape guide (E)
   Roller tape guide (F)
   Capstan (G)

NOTE

When cleaning the roller guides, the cleaning fluid should contact only the tape-bearing surfaces. This will prevent degreasing the roller guide bearings.



A. READ/WRITE HEAD
B. ERASE HEAD
C. TAPE CLEANER
D. FIXED HEADTAPE GUIDES (2)
E. TENSION ARM ASSY. W/ROLLER TAPE GUIDES (2)
F. ROLLER TAPE GUIDES
G. CAPSTAN
H. SNAP HUB ASSY.
I. HINGE BLOCKS (2)
J. BOT/EOT ASSY.
K. TAKE-UP REEL

MA-2942

Figure 3-1 Transport Components to Clean

3. Use cleaning fluid provided in the TUC01 Cleaning Kit with a foam-tipped swab to clean the capstan.

4. Use a lint-free wipe with a polishing action to remove any remaining deposits from the heads.

5. Finally, use a dry wipe to clean the reel-contacting metal surfaces of the upper hub. Dirt on these surfaces may cause tape reel slippage.

3.3.4 Ordering

You can order supplies, accessories, or documentation by phone or mail, as follows.

Continental USA

Call 800-258-1710 or mail order to:
Digital Equipment Corporation
P.O. Box CS2008
Nashua, NH 03061

New Hampshire

Call 603-884-6660 or mail order to:
Digital Equipment Corporation
P.O. Box CS2008
Nashua, NH 03061

Alaska or Hawaii

Call 408-734-4915 or mail order to:
Digital Equipment Corporation
632 Caribbean Drive
Sunnyvale, CA 94086

Canada

Call 800-267-6146 or mail order to:
Digital Equipment Corporation
P.O. Box 13000
Kanata, Ontario Canada K2K 2A6
Att: A&SG Business Manager
Telex: 610-562-8732

CHAPTER 4
OPERATION

4.1 CONTROLS AND INDICATORS

The operator controls are located at the upper-right corner of the transport (Figure 4-1). They consist of three lighted pushbuttons (colored) and five indicators (white).

The controls perform a dual function: operational control and diagnostic control. The transport must be off-line for the operator to use these functions. Both features are defined in this chapter.

The operational functions of the controls and indicators are listed in Table 4-1 and 4-2, respectively.

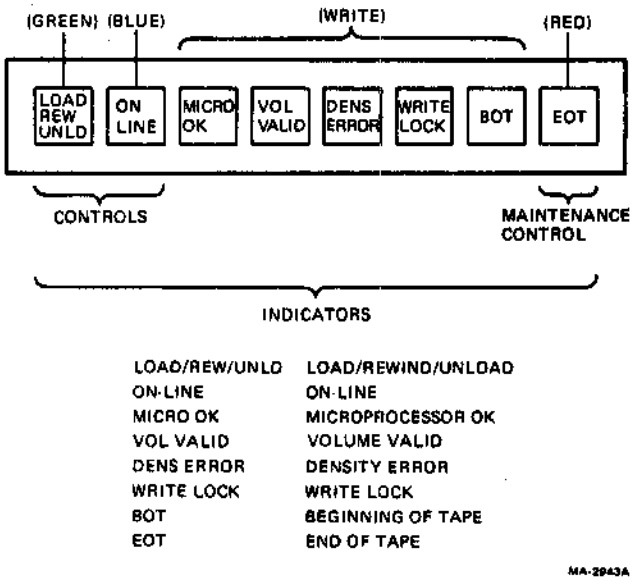


Figure 4-1 TS11 Transport Controls and Indicators

Table 4-1 Control Switch Functions

Switch	Function
LOAD REW UNLD (Green)	This control switch is the main operational switch; it has the following three functions. (Figure 4-2 diagrams these functions.) **Loading Tape** If a supply tape is correctly mounted and threaded (with tension arms not against limit switches) pressing LOAD/REW/UNLD initiates the following sequence. The tape moves forward until either 7.65 m (25 ft) of tape (calculated by tachometer ticks) has been loaded or the beginning of tape (BOT) marker is sensed. If tape moves forward 7.65 m (25 ft) without sensing BOT, tape motion stops and rewinds past the BOT marker, then forward to BOT. Tape motion stops with the tape resting at BOT. **Rewinding Tape (to BOT, prior to an unload)** Pressing LOAD/REW/UNLD when the tape is loaded causes tape to rewind to the BOT marker and stop. **Unloading Tape** Once the tape is rewound and resting at BOT, pressing LOAD/REW/UNLD causes the tape to automatically unload from the transport tape path onto the supply reel. The tape then stops. NOTE **The LOAD/REW/UNLD switch can be operated more than once during a cycle. For example, pressing the switch while the drive is rewinding off-line will cause the drive to unload. Pressing the switch again will cause the drive to just rewind and not unload.** The LOAD/REW/UNLD indicator is on when the tape is correctly loaded.
ON LINE (Blue)	This is a locking switch which puts the transport on- and off-line. Pushing it in (locking it) puts the transport on-line. Pushing it again unlocks the switch and puts the transport off-line. This switch is inoperative when the LOAD/REW/UNLD switch indicator is off. The ON LINE indicator is on when the transport is on-line.
EOT (Red)	This switch controls several maintenance functions. The only use in user-mode function is the customer confidence check, described later in this chapter. Pushing this button, when in non-maintenance mode and/or when a microdiagnostic error is displayed causes the microprocessor to restart.

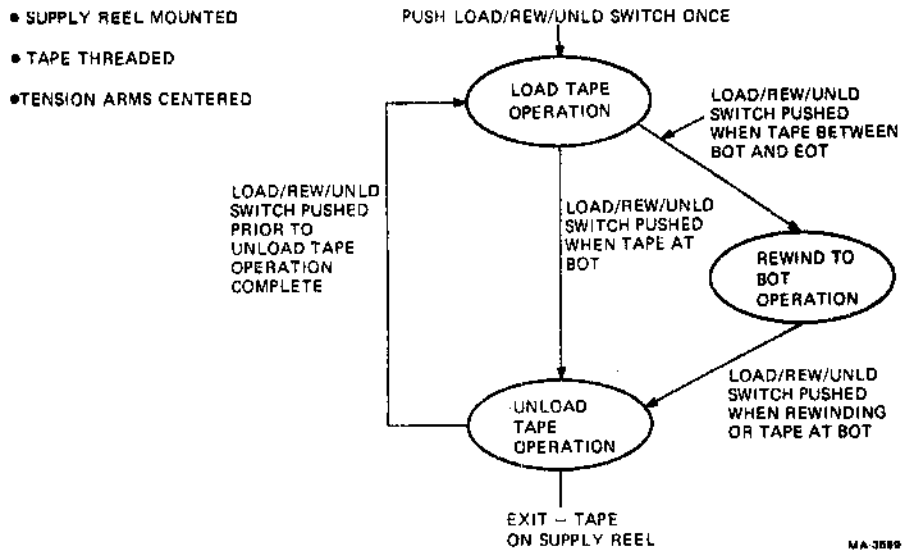


Figure 4-2 Load Switch State Diagram

Table 4-2 Operation Indicators

Indicator	Definition
MICRO OK (White)	Microprocessor OK: This indicator is on when the control microprocessor is operating with no errors.
VOL VALID (White)	Volume Check: This indicator is on when any change in status occurs (going off-line or on-line; reinitializing the microprocessor).
DENS ERROR (White)	Density Check: This indicator is on if a valid identification burst (IDB) is not seen at BOT. (The tape can still be read if it is the correct density.) If writing, DENS ERROR causes a tape position lost class error because the IDB was not written properly.
WRITE LOCK (White)	Write Lock: This indicator is on if no tape reel is mounted, or if a reel is mounted without a write-enable ring.
BOT (White)	Beginning of Tape: This indicator is on when the BOT marker is positioned over its sensor.
EOT (Red)	End of Tape: This indicator is on when the tape has been moved past the EOT marker. The subsystem software initialize command resets the EOT bit regardless of the tape position. **NOTE** **Manually moving tape past the EOT marker will not cause the indicator to come on.**

4.2.3 Unloading Tape

Depending on whether or not the tape is at the BOT marker, use one of the following unloading procedures.

4.2.3.1 Tape Loaded, Not at BOT – If the tape is not at BOT, unload as follows.

1. Make sure the transport is off-line.

2. Press the LOAD/REW/UNLD switch. The transport should execute a high speed rewind operation. When the BOT marker is sensed, tape motion stops. (Goes past, then forward, and stops at BOT.)

3. Press the LOAD/REW/UNLD switch again. (It may be pressed during rewind operation.) An unload sequence begins with the tape gently winding onto the upper supply reel. When the tape runs off the take-up reel, motion stops.

4. Manually wind the remaining tape onto the supply reel. If you wish to remove the supply reel, unlock the snap lock lever on the hub and gently pull the reel off.

4.2.3.2 Tape Loaded, at BOT – If the tape is at BOT, unload as follows.

1. Make sure the transport is off-line.

2. Press the LOAD/REW/UNLD switch. The unload sequence begins with the tape gently winding onto the upper supply reel. When the tape runs off the take-up reel, motion stops.

3. Manually wind the remaining tape onto the supply reel. If you wish to remove the supply reel, unlock the snap lock lever on the hub and gently pull the reel off.

4.2.4 Restart After Power Failure

In the event of a power failure, the transport automatically shuts down and tape motion stops without any physical damage to the tape. If the ON-LINE switch was on, the transport performs an auto-load sequence. If the ON-LINE switch was off, the transport stays unloaded and off-line.

4.2.5 Restart After Fail-Safe

If, for some reason, either tension arm limit is exceeded, causing a fail-safe condition, tape motion automatically stops without damaging the tape. When this fail-safe condition occurs, the transport does not respond to either on-line or off-line commands. To restart the transport follow the load tape procedure.

NOTE

Before restarting, this failure should be recorded in the system log with an indication of which fail-safe switch was exceeded. This information will aid Field Service in resolving the problem should the fail-safe condition be due to a tape transport problem.

4.3 OPERATOR TROUBLESHOOTING

Before any maintenance personnel are called to correct a problem, the operator can make a few minor checks and possibly avoid a service call. The following precautions may isolate an easily correctable error.

1. If the tape does not stop at BOT, make sure the tape has a BOT marker.

2. If a write operation is to be performed, make sure that the write enable ring is inserted in the tape reel.

3. If problems are related to the transport's read/write, clean the tape path according to the daily (eight hour) preventive maintenance procedures listed in Chapter 3.

4. Verify that the circuit breaker on the back of the TS11 power supply is on.

5. If the transport does not power up for cabinet mounted variations, make sure the power controller circuit breaker is on. Also make sure that the REMOTE ON/OFF/LOCAL ON power controller switch is in the REMOTE ON position.

6. Make sure the front door is closed.

4.4 CUSTOMER CONFIDENCE CHECK

The customer confidence check verifies the transport's operating characteristics. The test consists of several transport resident diagnostics that run sequentially and automatically once initiated.

4.4.1 Running the Customer Confidence Check

CAUTION

This test reads and writes on tape; therefore, it is necessary to remove any currently mounted tape to save the data on it.

An industry standard tape (also known as special test tape) that is known to be good must be used to prevent media-related defects from registering as hardware problems. This tape is provided as part of a Digital Maintenance Agreement. Nonservice contract customers may obtain the tape through the Digital Accessories and Supplies Group by ordering PN 29-11696. Refer to Paragraph 3.3.4 for ordering information.

Run the customer confidence check as follows.

1. Make sure the special test tape has a write enable ring inserted in the back of the supply reel.

2. Mount and load the tape. Make sure the LOAD indicator is on.

3. Make sure that the WRITE LOCK indicator is off; leave the drive off-line.

4. Push the leftmost (LOAD/REW/UNLD) and rightmost (EOT) operator panel pushbuttons at the same time.

   The operator panel will indicate that the test is ready to run by lighting the two leftmost indicators (LOAD/REW/UNLD, ON LINE).

5. Pressing the ON LINE switch once will start the test. Let the test run to completion, then press the switch again to stop the test and return the machine to normal operation. If the test is passed, the indicators display a rotating pattern of left-shifting 1s and 0s. If a test is failed, its specific test number will blink in the operator panel indicators. These panel indicators represent a binary register whose octal value is the failing test number. Clean the tape transport as described in Chapter 3 and try the test again. If the test is still failed, record the new failing test number and contact your local service representative.

CHAPTER 5
PROGRAMMING

5.1 TS11 REGISTERS

This chapter describes and defines the TS11 registers and packet processing. In addition, programming examples and packet formats are provided to illustrate basic TS11 programming concepts.

It is important to understand that command and data packets are used to transfer command and data information to the transport. The traditional method of writing a command or data word to a Unibus register is not used. A command packet consists of a command word and up to three additional words of command modifiers or qualifiers. This command packet is assembled in host CPU memory space on modulo-4 memory addresses. The beginning address of the command packet is the command pointer. Only the high 16-bits of the 18-bit address are used. This pointer is used by the controller to NPR transfer the command packet to the subsystem.

The eight TS11 (M7982) registers are as follows.

(1)	TSBA	- Unibus Address Register
(1)	TSDB	- Unibus Data Buffer
(1)	TSSR	- Status Register
(5)	XST	- Extended Status Registers

5.1.1 TSBA (Unibus Address Register - Base Address - Read Only)

The TSBA is an 18-bit register. It is parallel loaded from the TSDB every time the TSDB is loaded as a Unibus slave by the CPU. TSDB bits 15 through 2 load into TSBA bits 15 through 2; and TSDB bits 1 and 0 load into TSBA bits 17 and 16. Zeros are loaded into TSBA bits 1 and 0. TSBA bits 17 and 16 are displayed in TSSR bits 9 and 8 respectively. TSBA can be instructed by the transport to increment or decrement by two for nonprocessor request (NPR) word transfers, or by one for NPR byte transfers. The TSBA is the base address in the read only mode and it is not cleared on power up, subsystem INIT, or bus INIT. It can also be read at any time with or without the drive unit connected.

Figure 5-1 shows the TSBA register, and Table 5-1 lists and defines the bits. The TSBA register serves the following two major purposes.

1. The TSBA can be used as a command and message pointer to the remote transport device registers (command and message buffers). These are located somewhere in the Unibus address space. The content, loaded into TSDB when the M7982 is the bus slave, is considered the command or message pointer. In this mode, the M7982 receives data (initiated by the transport) at this command pointer address and sends it to the transport for storage and/or execution. The message buffer address tells the M7982 where to place the message sent to the CPU address space. When used as a message pointer, the highest message buffer address + 2 is left in the TSBA.

2. The TSBA can be used as a data pointer (NPR's bus address 0), pointing to data buffer areas located somewhere in the Unibus address space. [In this mode, the transport will serially load the TSDB with data (18 address bits); TSDB bits 17 through 0 load into TSBA bits 17 through 0, but bits 17 and 16 are displayed in TSSR bits 9 and 8, respectively.] The contents of TSBA are then used to point to data buffer areas while the M7982 transfers data by NPRs.

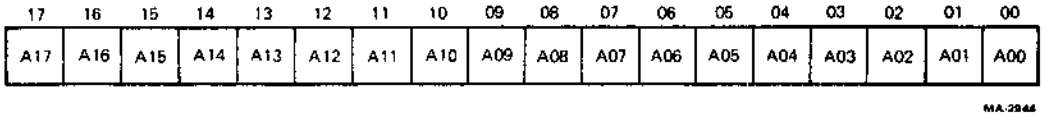


Figure 5-1 TSBA Register

Table 5-1 TSBA Bit Definitions

Bit	Name	Definition
17	A17	Bus address bit 17
16	A16	Bus address bit 16
15	A15	Bus address bit 15
14	A14	Bus address bit 14
13	A13	Bus address bit 13
12	A12	Bus address bit 12
11	A11	Bus address bit 11
10	A10	Bus address bit 10
09	A09	Bus address bit 09
08	A08	Bus address bit 08
07	A07	Bus address bit 07
06	A06	Bus address bit 06
05	A05	Bus address bit 05
04	A04	Bus address bit 04
03	A03	Bus address bit 03
02	A02	Bus address bit 02
01	A01	Bus address bit 01
00	A00	Bus address bit 00

5.1.2 TSDB (Unibus Data Buffer Register – Base Address – Write Only)

The TSDB is an 18-bit register that is parallel loaded from the Unibus or serially loaded from the transport. A 16-bit portion of this register is used as a word buffer register to the M7982 when the M7982 is the bus slave (for beginning an operation). The same word buffer register is also used by the transport (for data during NPR transfers) when the M7982 is bus master. The TSBD can be loaded when the M7982 is bus slave by three different transfers from a bus master. Two transfers are for maintenance purposes (DATOB to high byte and DATOB to low byte). The third transfer is for normal (word) operation (DATO). This register is write only and is not cleared at power up, subsystem initialize, or bus initialize. It cannot be loaded without the complete transport unit connected and a serial bus synchronous clock. The M7982 responds with SSYN any time the TSDB is written to.

Figure 5-2 shows the TSDB register, and Table 5-2 lists and defines the bits.

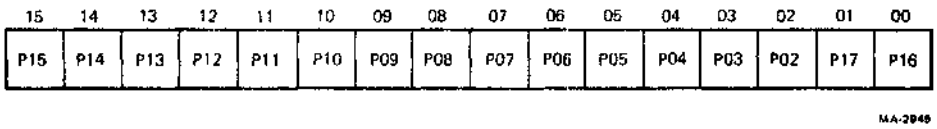


Figure 5-2 TSDB Register (Loaded with a Command Pointer)

Table 5-2 TSDB Bit Definitions

Bit	Name	Definition
15	P15	Command pointer bit 15
14	P14	Command pointer bit 14
13	P13	Command pointer bit 13
12	P12	Command pointer bit 12
11	P11	Command pointer bit 11
10	P10	Command pointer bit 10
09	P09	Command pointer bit 09
08	P08	Command pointer bit 08
07	P07	Command pointer bit 07
06	P06	Command pointer bit 06
05	P05	Command pointer bit 05
04	P04	Command pointer bit 04
03	P03	Command pointer bit 03
02	P02	Command pointer bit 02
01	P17	Command pointer bit 17
00	P16	Command pointer bit 16

5.1.2.1 Normal Operation – When TSDB is loaded by a DATO (write a word to TSDB) the following happens. Bit 0 and bit 1 are loaded with zeros. Bits 2 through 15 are loaded with bits 2 through 15, respectively, from the Unibus. Bits 16 and 17 are loaded from bits 0 and 1, respectively, from the Unibus. The bus address is 16XXXX, where XXXX can be any unused address from 0 through 17776. The M7982 indicates to the transport a TSDB word load when the M7982 is bus slave.

5.1.2.2 Data Wraparound Internal to the M7982 (Diagnostic Mode) – When TSDB is loaded by a DATOB to TSDB high byte, the following happens. Bits 0 through 7 are loaded with bits 8 through 15, respectively, from the Unibus. Bits 8 through 15 are loaded with bits 8 through 15, respectively, from the Unibus. Bits 16 and 17 are loaded with bits 8 and 9 respectively, from the Unibus. The TSDB is then loaded into TSBA. The bus address is 16XXXX (odd). This transfer is executed anytime a DATOB to the TSDB high byte is done. If SSR (see TSSR bit 07) is clear, an error (RMR TSSR bit 12) occurs, but the transfer is still executed and completed. The TSSR is not affected (except for SSR bit 07, which gets cleared). The TS11 tells the transport over the serial bus to stop the transport from updating TSSR. To use the transport again, the M7982 must initialize the transport (that is, write the TSSR).

5.1.2.3 Data Wraparound External with Transport – When TSDB is loaded by a DATOB to TSDB low byte, the following happens. Bits 0 through 15 are loaded with bits 0 through 15, respectively, from the Unibus. (Most PDP-11 CPUs assert all zeros for bits 8 through 15 except for a MOVB; this sign extends bit 07. See the respective processor handbook for a MOVB instruction.) Bits 16 and 17 cannot be determined. The bus address is 16XXXX (even). The M7982 sends TSDB bits 0 through 15 and a qualifier to the transport.

The transport returns the same data and another qualifier which instructs the M7982 to load the TSDB bits 0 through 17 into TSBA bits 0 through 17, respectively, and to load bits 0 through 15 into TSSR bits 0 through 15, respectively. (Some bits cannot be loaded; see the TSSR register description which follows.) The M7982 then returns a serial bus transfer complete to the transport. To use the transport again, the M7982 must initialize the transport (that is, write the TSSR).

5.1.3 TSSR (Status Register – Base Address + 2 – Read/Write)
The TSSR is a 16-bit register that can only be updated from the transport or internal M7982 logic; it cannot be modified from the Unibus except for SPE, UPE, RMR, NXM, and SSR bits that are cleared when the TSDB is written by the host CPU. It is a read/write register at base address 16XXXX+2. (The DATO/DATOB write transfers cause the M7982 to modify 16XXXX+2.) It can be read at any time with or without the transport unit connected. Figure 5-3 shows the TSSR register and Table 5-3 lists and defines the bits.

TSSR register bits 14 through 11 and 7 are cleared only on system power up, TS11 power up, subsystem initialize, or at the beginning of any write command to the TSSR register. Bits 15 and 7 are also under control of the transport. These may be set or cleared independently of any TS11 operation. Bits 10 and 6 through 0 are exclusively controlled by the transport and reflect the transport status as indicated.

NOTE

Any write function to the M7982 base address 16XXXX+2 is decoded as a subsystem initialize. This resets the TS11 and transport no matter what state they are in and causes an automatic load sequence returning the tape to BOT if the transport is on-line.

The TSSR register utilizes several bits to increase its status reporting capabilities. TSSR bits 4 and 5 report four fatal class error codes and TSSR bits 1, 2, and 3 report seven termination class status codes. Fatal error bits are valid only if the termination class equals 7.

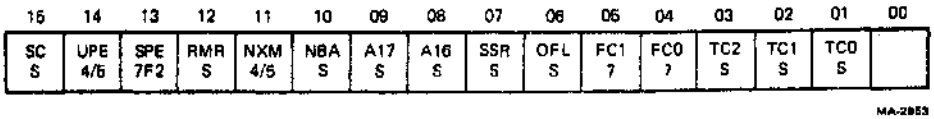


Figure 5-3 TSSR Register

Table 5-3 TSSR Bit Definitions

Bit	Name	Causes Termination Class (TC)	Definition
15	SC	S	Special Condition: When set, this bit indicates that the last command was not completed without incident. Specifically, either an error was detected or an exception condition occurred. An exception condition could be a tape mark on read commands, reverse motion at BOT, EOT while writing, etc.
14	UPE	4/5	Unibus Parity Error: This bit is set by the M7982 when it detects a parity error in the memory data being transferred from the CPU memory.
13	SPE	7F2	Serial Bus Parity Error: This bit is set by the M7982 when it detects a serial bus parity error on data received from the transport. 7F2 means termination class 7 and fatal class 2.
12	RMR	S	Register Modification Refused: This bit is set by the M7982 when a command pointer is loaded into TSDB and subsystem ready (SSR) is not set. This bit may set on a bug free system if ATTN interrupts are enabled.
11	NXM	4/5	Nonexistent Memory: This bit is set by the M7982 when trying to transfer to or from a memory location which does not exist. It may occur when fetching the command packet, fetching or storing data, or storing the message packet.
10	NBA	S	Need Buffer Address: When set, this indicates that the transport needs a message buffer address. This bit is cleared during the set characteristics command if the transport gets valid data; it is always set after subsystem initialization.

Table 5-3 TSSR Bit Definitions (Cont)

Bit	Name	Causes Termination Class (TC)	Definition
09	A17	S	Bus Address Bit 17: A17 and A16 (bits 08 and 09) display the values of bits 17 and 16 in the TSBA register.
08	A16	S	Bus Address Bit 16: See A17 above (bit 09).
07	SSR	S	Subsystem Ready: When set, this bit indicates that the TS11 Subsystem is not busy and is ready to accept a new command pointer.
06	OFL	S	Off-Line: When set, this bit indicates that the transport is off-line and unavailable for any tape motion commands.
05	FC1	7	Fatal Termination Class 01: FC1 and FC0 (bits 05 and 04) are used to indicate the type of fatal error that has occurred on the transport. These bits are valid only when SC is set and the termination class code bits are all set (111). Refer to special conditions and errors, Paragraph 5.3.3 of this manual.
04	FC0	7	Fatal Termination Class 00: See FC1 (bit 05) above.
03	TC2	S	Termination Class Bit 02: This bit, along with the TC1 and TC0 bits, acts as an offset value when an error or exception condition occurs on a command. Each of the eight possible values of this field represents a particular class of errors or exceptions. The conditions in each class have similar significance and, as applicable, recovery procedures. The code provided in this field is expected to be utilized as an offset into a dispatch table for handling the condition. These bits are valid only when special condition (SC) is set. Refer to special conditions and errors, Paragraph 5.3.3 of this manual.
02	TC1	S	Termination Class Bit 01: See TC2 (bit 03) above.
01	TC0	S	Termination Class Bit 00: See TC2 (bit 03) above.
00	–	–	Not used.

On fatal errors (fatal class bits equal seven), if the need buffer address is not set (NBA=0), then the message may be valid. If the need buffer address is set (NBA=1,) then there was no message.

The RMR bit will not affect the error class codes because RMR may occur on a bug free system. However, RMR will set the special condition (SC). (You may have tried to perform the next command while the drive was outputting the ATTN MSG.) If RMR is seen in the TSSR, the CPU must have written the TSDB while the command was executing.

NOTE

The TSSR may not reflect the current state of the hardware if ATTNs are not enabled and the message buffer is not released. (That is, the drive may be off-line while the TSSR shows on-line.) To keep the TSSR up to date would violate message packet protocol.

Fatal Class Codes

TSSR Bits 5 4	**Description**
0 0	Internal microdiagnostic failure in diagnostic mode or capstan runaway in operational mode (337 octal in operator panel). See the fatal error code byte (XSTAT3) for the diagnostic function. Cleared by drive initialize command or subsystem initialize. Subsequent tape operations will not be accepted (command reject) until, as a minimum, a drive initialize is issued.
0 1	I/O sequencer CROM parity error. Cleared by drive initialize or subsystem initialize.
1 0	Microprocessor CROM parity error, I/O silo parity error, serial bus parity error, or other fatal error. Cleared only by subsystem initialize.
1 1	Low ac or loss of ac power has been detected and a power down is in effect. Cleared only by subsystem initialize.

NOTE

TSSR is not cleared immediately after initialization. The microprocessor runs to complete an automatic load sequence. When tape is at BOT, TSSR updates.

Termination Class Codes

TSSR Bits 3 2 1	Description
0 0 0	Normal termination
0 0 1	Attention condition
0 1 0	Tape status alert
0 1 1	Function reject
1 0 0	Recoverable error (Tape position is one record down from start of function.)
1 0 1	Recoverable error (Tape not moved.)
1 1 0	Unrecoverable error (Tape position lost.)
1 1 1	Fatal controller error (See Fatal Class bits.)

5.1.4 XST (Extended Status Registers)

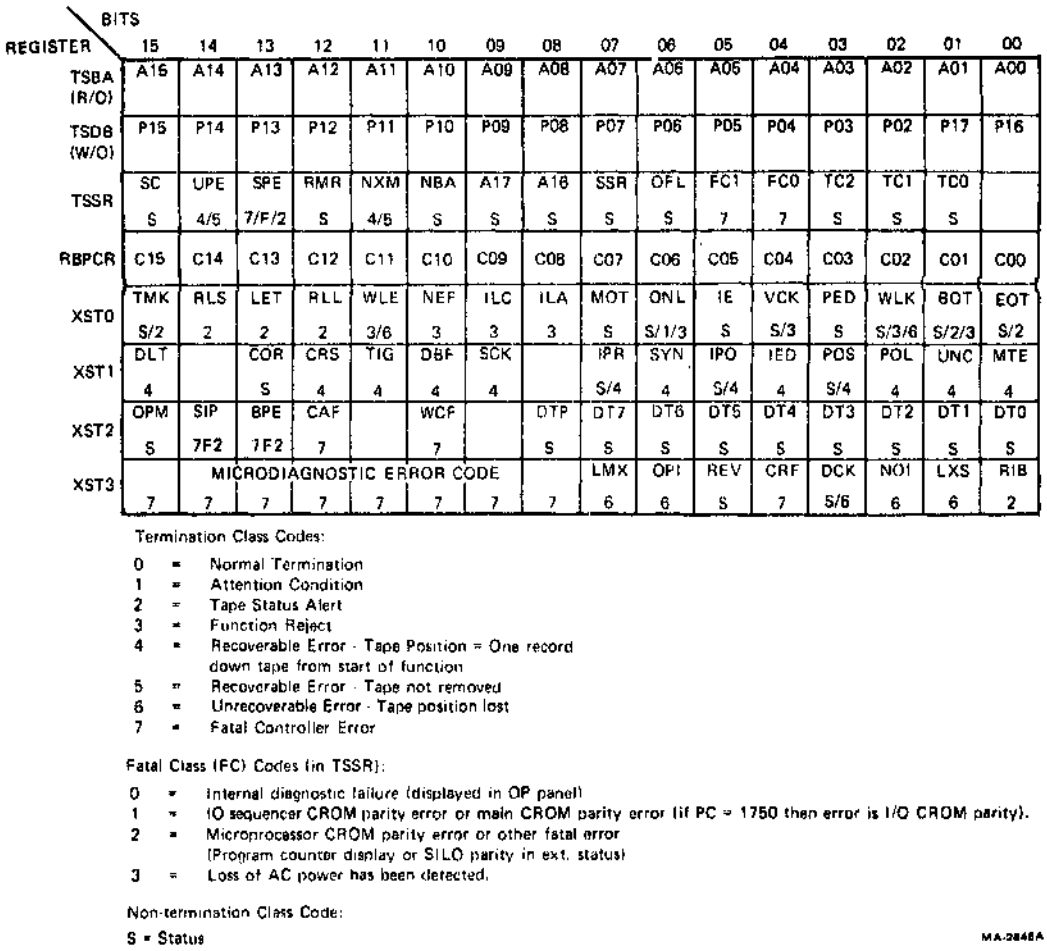
Five additional registers are employed to provide additional status information: residual frame count register (RBPCR) and extended status register 0, 1, 2, and 3. Figure 5-4 shows these registers. Tables 5-4 through 5-8 list and define the bits.

The extended status registers are not read directly from the registers accessible at the Unibus interface. At the end of a command or by issuing a Get Status Command the message packet information is updated.

The end message packet which results from the get status contains the extended status words. This means that a message buffer has to be defined to the subsystem before the extended status registers are available to the software.

5.1.5 TS11 Register Summary

Figure 5-4 is a summary of the TS11 registers.



REGISTER \ BITS	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TSBA (R/O)	A16	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
TSDB (W/O)	P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P17	P16
TSSR	SC S	UPE 4/5	SPE 7/F/2	RMR S	NXM 4/5	NBA S	A17 S	A16 S	SSR S	OFL S	FC1 7	FC0 7	TC2 S	TC1 S	TC0 S	
RBPCR	C15	C14	C13	C12	C11	C10	C09	C08	C07	C06	C05	C04	C03	C02	C01	C00
XST0	TMK S/2	RLS 2	LET 2	RLL 2	WLE 3/6	NEF 3	ILC 3	ILA 3	MOT S	ONL S/1/3	IE S	VCK S/3	PED S	WLK S/3/6	BOT S/2/3	EOT S/2
XST1	DLT 4		COR S	CRS 4	TIG 4	DBF 4	SCK 4		IPR S/4	SYN 4	IPO S/4	IED 4	POS S/4	POL 4	UNC 4	MTE 4
XST2	OPM S	SIP 7F2	BPE 7F2	CAF 7		WCF 7		DTP S	DT7 S	DT6 S	DT5 S	DT4 S	DT3 S	DT2 S	DT1 S	DT0 S
XST3	MICRODIAGNOSTIC ERROR CODE 7	7	7	7	7	7	7	7	LMX 6	OPI 6	REV S	CRF 7	DCK S/6	NOI 6	LXS 6	RIB 2

Termination Class Codes:

0 = Normal Termination
1 = Attention Condition
2 = Tape Status Alert
3 = Function Reject
4 = Recoverable Error - Tape Position = One record down tape from start of function
5 = Recoverable Error - Tape not removed
6 = Unrecoverable Error - Tape position lost
7 = Fatal Controller Error

Fatal Class (FC) Codes (in TSSR):

0 = Internal diagnostic failure (displayed in OP panel)
1 = IO sequencer CROM parity error or main CROM parity error (if PC = 1750 then error is I/O CROM parity).
2 = Microprocessor CROM parity error or other fatal error (Program counter display or SILO parity in ext. status)
3 = Loss of AC power has been detected.

Non-termination Class Code:

S = Status

MA-2845A

Figure 5-4 TS11 Register Summary

Table 5-4 RBPCR Bit Descriptions

Bit	Name	Description
15 to 0	C15 to C0	This word contains the octal count of residual bytes, records, tape marks for the read, space records, and skip tape mark commands. The contents are meaningless for all other commands.

Table 5-5 XSTAT0 Bit Definitions

Bit	Name	Causes Termination Class (TC)	Definition
15	TMK	S/2	Tape Mark Detected: This bit is set when a tape mark is detected during a read, space, or skip command and as a result of the write tape mark or write tape mark retry commands.
14	RLS	2	Record Length Short: This bit indicates one of the following three cases. The record length was shorter than the byte count on read operations. A space record operation encountered a tape mark or BOT before the position count was exhausted. Or, the third possibility, a skip tape marks command was terminated by encountering BOT or a double tape mark (if skip tape marks command is enabled, see LET) before exhausting the position counter.
13	LET	2	Logical End of Tape: This is set only on the skip tape marks command under two conditions: when either two contiguous tape marks are detected or when moving off BOT and the first record encountered is a tape mark. The setting of this bit will not occur unless this mode of termination is enabled through use of the set characteristics command.
12	RLL	2	Record Length Long: When set, this bit indicates that the record read was longer than the byte count specified.
11	WLE	3, 6	Write Lock Error: When set, a TC3 indicates that a write operation was issued but the mounted tape did not contain a write enable ring. When set, TC6 indicates the WRITE LOCK switch was activated during write operation.
10	NEF	3	Nonexecutable Function: When set, this bit indicates that the command could not be executed due to one of the following conditions. The command specified reverse tape direction but the tape was already positioned at BOT. A motion command was issued without the clear volume check (CVC) bit being set while the volume check bit was set. A motion command was issued when the transport was off-line. A write command was issued when the tape did not contain a write enable ring [write lock status (WLS)].

Table 5-5 XSTAT0 Bit Definitions (Cont)

Bit	Name	Causes Termination Class (TC)	Definition
09	ILC	3	Illegal Command: This bit is set when a command is issued and either its command field or its command mode field contains codes not supported by the transport.
08	ILA	3	Illegal Address
07	MOT	S	Capstan is moving.
06	ONL	S/1/3	On-Line: When set, this bit indicates that the transport is on-line and operable. It causes a TC1 on ATTN interrupt or a TC3 for a non-executable function if rejected because the transport was off-line.
05	IE	S	Interrupt Enable: This bit reflects the state of the interrupt enable bit supplied on the last command.
04	VCK	S/3	Volume Check: This bit is set when the transport changes state (on-line to off-line and vice versa). It is always set after initialization.
03	PED	S	Phase Encoded Drive: When set, this bit indicates that the transport is capable of reading and writing only 1600 bit/in phase encoded data. It should always be set.
02	WLK	S/3/6	Write Locked: When set, this bit indicates that the mounted tape reel does not have a write enable ring installed. Therefore the tape is write protected.
01	BOT	S/2/3	Beginning Of Tape: When set, this bit indicates that the tape is positioned at the load point as denoted by the BOT reflective strip on the tape. This causes TC2 if reversed in BOT, and TC3 if at BOT when a reverse command occurs.
00	EOT	S/2	End Of Tape: This bit is set whenever the tape is positioned at or beyond the end of tape reflective strip. It is not reset until the tape passes over the reflective strip in the reverse direction under program control. Subsystem initialization always resets this bit (status on read, TC2 on a write). Manually moving EOT mark over the EOT sensor will not set or reset the EOT bit.

Table 5-6 XSTAT1 Bit Definitions

Bit	Name	Causes Termination Class (TC)	Definition
15	DLT	4	Data Late: This bit is set when the I/O silo is full on a read or empty on a write. The conditions occur whenever the Unibus latency exceeds the transport's data transfer rate for a significant number of transfers.
14	–	–	Not used.
13	COR	S	Correctable Data: This bit is set when a correctable data error has been encountered (on a read command only). It will not cause a termination class error but there is a dead track. Dead track bits will indicate the error. This is used primarily as a diagnostic feature.
12	CRS	4	Crease Detected: This bit is set when eight of nine data tracks go dead for less than 0.1 inches before a valid postamble is detected.
11	TIG	4	Trash In The Gap: This bit is set when nonerased data is detected in a gap during a read, write, write tape mark, or erase command.
10	DBF	4	Deskew Buffer Fail: This bit is set when one of the deskew buffers fails to set output ready within 20 microseconds after being enabled. The dead track bits indicate on which tracks this failure occurred. This error is probably a result of a broken formatter.
09	SCK	4	Speed Check: This bit is set when average tape speed varies more than five percent during a write operation.
08	–	–	Not used.
07	IPR	S,4	Invalid Preamble: This bit is set if the preamble is shorter than 36 characters or longer than 44 characters. It is also set if the preamble is incorrectly encoded beyond the fifteenth character in read or the tenth character in read after write. It is status on read, TC4 on a write.
06	SYN	4	Synchronization Failure: This bit is set if the formatter is unable to achieve synchronization in the preamble.
05	IPO	S/4	Invalid Postamble: This bit is set during read or write if any of the first 39 characters of the postamble are not read correctly. It is status on read, TC4 on a write.

Table 5-6 XSTAT1 Bit Definitions (Cont)

Bit	Name	Causes Termination Class (TC)	Definition
04	IED	4	Invalid End of Data: This bit is set when eight out of nine tracks go dead before the postamble is detected.
03	POS	S/4	Postamble Short: This bit is set during a read or write when fewer than 38 all-zero characters are read following the all-one characters. It is status on read, TC4 on a write.
02	POL	4	Postamble Long: This bit is set during read or write operations when the postamble exceeds 42 characters.
01	UNC	4	Uncorrectable Data: This bit is set when a parity error occurs without a corresponding dead track indication. This bit is a normal write error for any dead track.
00	MTE	4	Multitrack Error: This bit is set if more than one dead track occurs in the preamble or in the data field.

Table 5-7 XSTAT2 Bit Definitions

Bit	Name	Causes Termination Class (TC)	Definition
15	OPM	S	Operation In Progress (Tape moved.)
14	SIP	7F2	Silo Parity Error: This bit causes fatal class two (FC2) because the error might have occurred during the transmission of the message packet.
13	BPE	7F2	Serial Bus Parity Error At Drive: This bit is set at the transport when a parity error is detected on data transmitted from the M7982 to the transport. It causes FC2 because the error might have occurred during the transmission of the command packet.
12	CAF	7	Capstan Acceleration Fail: This bit is set if, after acceleration of tape for 45 ticks (0.5 inches), the tape speed was checked and found out of tolerance by more than ten percent (averaged over 8 ticks).
11	-	-	Not used.

Table 5-7 XSTAT2 Bit Definitions (Cont)

Bit	Name	Causes Termination Class (TC)	Definition
10	WCF	7	Write Card Fail: This bit is set if the write card did not empty the I/O silo. This error can be the result of the write board clock not being turned on.
09	–	–	Not used.
08	DTP	S	Dead Track Parity: This bit indicates which tracks went dead, if any, during the last data transfer operation. If deskew buffer fail (DBF) is set, these bits indicate which channel failed.
07	DT7	S	Dead track 7 (See DTP)
06	DT6	S	Dead track 6 (See DTP)
05	DT5	S	Dead track 5 (See DTP)
04	DT4	S	Dead track 4 (See DTP)
03	DT3	S	Dead track 3 (See DTP)
02	DT2	S	Dead track 2 (See DTP)
01	DT1	S	Dead track 1 (See DTP)
00	DT0	S	Dead track 0 (See DTP)

NOTE

On the write characteristic command, bits 07 through 00 contain the microcode revision level; on the get status command, these bits contain the residual capstan tick count (the number of ticks from the ideal stopping point; useful for diagnostics).

Table 5-8 XSTAT3 Bit Definitions

Bit	Name	Causes Termination Class	Definition
15 to 08	-	7	Microdiagnostic Error Code: There is one operational error, 337 or left justified to 157400 in a 16-bit register (capstan runaway), which is displayed here. This means that the capstan was commanded to stop but exceeded the allowable stopping window. Drive must be initialized to be used for tape motion again.
07	LMX	6	Limit Exceeded: This bit is set when the tape tension arms have exceeded their allowable travel during an operation and have caused the activation of the limit switches. No tension exists on the mounted tape.
06	OPI	6	Operation Incomplete: This bit is set when a read, space, or skip operation has moved 25 feet of tape without detecting any data on the tape. It is also set by a write command when the read head fails to see data transitions after four feet of tape.
05	REV	S	Reverse: This bit is set when the direction of current tape operation is reverse. For multifunction retry commands, if at least one of the commands is reverse, the bit is set.
04	CRF	7	Capstan Response Fail: This bit is set if the capstan logic is commanded to move, but no tachometer pulses are received within five milliseconds.
03	DCK	S/6	Density Check: The current operation will be done. However, note that read, space, and skip operations will complete without error (if no other errors occur) to allow tapes with a bad IDB to be read. On a write command, when a bad IDB is sensed, tape position lost will occur.

NOTE

If you append to a tape with a bad IDB, you will not receive any DCK error until a write.

Table 5-8 XSTAT3 Bit Definitions (Cont)

Bit	Name	Causes Termination Class	Definition
02	NOI	6	Noise Record: This bit is set during a space operation when a burst of flux changes, which do not qualify as a record (but too many to ignore), are detected.
01	LXS	S	Limit Exceeded Statically: This bit is set by tension arms that have actuated their limit switches; it remains set when tension arms are returned to normal position. It can be reset only by loading tape.
00	RIB	2	Reverse Into BOT: This bit is set when a read, space, skip, or reverse command already in progress encounters the BOT marker when moving tape in the reverse direction. Tape motion will be halted at BOT.

5.2 PACKET PROCESSING

The packet protocol scheme allows the drive to send a large amount of status and error information to the CPU while taking up only two words of Unibus address space. The packet protocol also prevents the drive from updating the error and status information asynchronously, that is, while the CPU is reading the error and status information.

NOTE

This section is not intended to detail all aspects of packet protocol or packet processing. It is intended to illustrate how these concepts are implemented in the TS11.

To allow the drive to take up only two words of address space, we allow the CPU to define a set of locations in memory. These locations (command buffers) are used to tell the drive what operation to perform. The CPU also defines a set of locations (message buffers) in memory where the drive will put the error and status information. The CPU must give both the command buffer address and message buffer address to the drive. The CPU gives the command buffer address to the drive on every command. (The CPU writes the address of the command packet into the TSDB of the drive.) The CPU gives the message buffer address to the drive every time the CPU does a set characteristics command.

To prevent the drive from updating the message buffer while the CPU is reading the message buffer, we have defined the concept of ownership. Both the command and message buffers can be owned. Each buffer may be owned by the drive or the CPU, but not by both simultaneously. Ownership of a buffer can only be transferred by the current owner.

There are four different combinations that transfer the ownership of the two buffers.

Command buffer CPU to drive by the CPU
Command buffer drive to CPU by the drive
Message buffer CPU to drive by the CPU
Message buffer drive to the CPU by the drive

The CPU transfers ownership of the command buffer to the drive by writing the address of the command packet into the TSDB. This write clears the TSSR subsystem ready (SSR) bit.

The drive transfers ownership of the command buffer to the CPU by setting the acknowledge (ACK) bit in the message buffer. When the drive outputs the message buffer, the drive sets SSR in the TSSR to indicate that the message is in the message buffer. If the message buffer does not contain the ACK bit, the CPU will know that the drive did not see the last command buffer and the CPU still owns the command buffer. The command may be reissued by the CPU.

The CPU transfers ownership of the message buffer to the drive by setting the ACK bit in the command buffer. If the command buffer does not contain the ACK bit, the drive will know that the CPU did not see the last message buffer and the drive still owns the message buffer. The drive outputs the TSSR again (with the SSR bit up) and interrupts (if IE is set) without sending out a message.

The drive transfers ownership of the message buffer to the CPU in one of two ways. The first way is used after the end of a command: the drive sets the SSR bit in the TSSR to indicate that the command is done (and interrupts if IE is set). The second way is used during an attention (ATTN). SSR will already be up because an ATTN only happens when the drive is inactive. The drive clears SSR, outputs the message, then sets SSR again and interrupts (if IE set).

Note that if the CPU writes the TSDB while the SSR is clear during an ATTN, the register modification refused (RMR) error bit will be set and that command will be ignored. The ATTN message will not have the ACK bit set since the drive does not own the command buffer. Note that RMR may set in this way on a bug-free system because the CPU happened to try to perform a command at the same time the drive wanted to perform an ATTN. All other settings of the RMR indicate a software bug. (The CPU tried to do a command before the previous command was finished.)

If the CPU command was lost because the transport was outputting an ATTN message, VOL CHK and INT ENB are not updated. If the CPU command was rejected (illegal command, etc.), VOL CHK and INT ENB are updated to the start of the rejected command.

When the drive is initialized, the drive updates the TSSR. At this time, both the command and message buffers are defined as belonging to the CPU. When the CPU wants to do a command (the first one must be a set characteristics to set up the message buffer address), the CPU writes the address of the command buffer into the TSDB of the drive. This command must have the ACK bit set to give ownership of the message buffer to the drive. At this point, the drive owns both the command and message buffers.

The drive executes the set characteristics command and sends out a message to the message buffer address with the ACK bit set; this indicates that the drive has recognized the command and is finished with the command buffer. The drive then sets SSR and interrupts (if IE is set). At this point, the CPU owns both the message and command buffers again.

As you can see, the ownership of both buffers transfers simultaneously from CPU to drive and then from drive to CPU.

Now consider the case where ATTNs are enabled by the proper characteristics mode word and the drive wants to do an ATTN. An ATTN only occurs when the drive is not active. If the CPU owns both the command and message buffers, the drive must queue up the ATTN and not do anything until the CPU releases the message buffer on the next command. So when the CPU executes the next command (with the ACK bit set), the drive outputs the ATTN message with the ACK bit 0; this indicates that the command was lost (except for the transfer of the message buffer ownership to the drive). The drive refuses to accept ownership of the command buffer. The CPU will then still own the command buffer (because the drive did not accept the command) and will also own the message buffer now filled with an ATTN message. If the CPU still wants to do the ignored command, the CPU must reissue the command (with the ACK bit set).

Now consider the case where the CPU wants to be notified of a change in status right away while the drive is inactive for a long period of time. To accomplish this, the drive must own the message buffer for that long period of time. Everything up to now has indicated that the drive gives up the message buffer at the end of every command. The message buffer release command is a special command from the CPU. It tells the drive not to give ownership of the message buffer back to the CPU at the end of the command. The drive does not output a message at the end of the command, but just outputs the TSSR (with the SSR bit set) and interrupts (if the proper characteristics mode word is set up). The drive then maintains ownership of the message buffer until an ATTN condition is seen. The drive then immediately clears SSR, outputs the message (with the ACK bit not set since the drive is not responding to a command), and then sets SSR and interrupts (if IE is set). At this time, the system is back to the state of the CPU owning both buffers. Another ATTN is not done until the CPU does a command with the ACK bit set to release ownership of the message buffer containing the ATTN message.

Suppose the CPU has done a message buffer release command and wants to do another command but has not received an ATTN from the drive (so that the drive still owns the message buffer from the message buffer release command). The CPU can do a command without the ACK bit set in the command buffer. At the time of the command, the CPU does not own the message buffer so the CPU cannot release the message buffer. If the CPU does set the ACK bit, nothing will happen (except the CPU might miss an ATTN if the drive was sending out an ATTN at the same time that the CPU was doing a command).

Message packet protocol may be violated if the transport gets an error (NXM, memory parity, serial bus parity error, or I/O silo parity error) during the reading in of the message packet. When one of these errors occurs, the transport always sends out a failure message (because the packet is not reliable).

The system software should be written so it will not crash if the TS11 M7982 interrupts while the CPU is servicing a TS11 M7982 interrupt. However, this case may happen but only if the TS11 should receive a fatal hardware error.

5.2.1 Command Packet/Header Word

Figure 5-5 shows the command packet header word, and Table 5-9 lists and defines the bits. Table 5-10 gives the command code and mode field definitions.

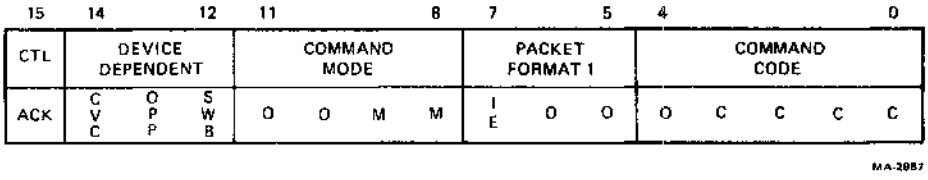


Figure 5-5 Command Packet Header Word

Table 5-9 Command Packet Header Word Bit Definitions

Bit	Name	Function
15	Acknowledge	This bit is set when a command is issued and the CPU owns the message buffer. It informs the M7982 that the message buffer is now available for any pending or subsequent message packets. This passes ownership of the message buffer to the transport.
14 to 12	Device Dependent Bits/Field	The following shows how these three bits are implemented. **Bit / Name / Definition** 14 / CVC / Clear volume check 13 / OPP / Opposite (reverse the execution sequence of the reread commands) 12 / SWB / Swap bytes
11 to 8	Command Mode Field	This bit acts as an extension to the command code and mode field and allows specification of extended device commands (seek, rewind, erase, write tape mark, etc.). Command code and mode field are detailed in Table 5-10.
7 to 5	Packet Format #1 Field	The following two values are defined in this field. **Bit Values / Definition** 000 / One word header; interrupt disable 100 / One word header; interrupt enable
4 to 0	Command Code	Refer to Table 5-10.

Table 5-10 Command Code and Mode Field Definitions

Command Code Field	Command Name	Command Mode Field	Mode Name
00001	Read	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (space reverse, read two)
		0011	Reread next (space forward, read reverse)
00100	Write Characteristics	0000	Load message buffer address and set device characteristic
00101	Write	0000	Write data (text)
		0010	Write data retry (space reverse, erase, write data)
00110	Write Subsystem Memory	0000	Normal (diagnostic use only)
01000	Position	0000	Space records forward
		0001	Space records reverse
		0010	Skip tape marks forward
		0011	Skip tape marks reverse
		0100	Rewind
01001	Format	0000	Write tape mark
		0001	Erase
		0010	Write tape mark entry (space reverse, erase, write tape mark)
01010	Control	0000	Message buffer release
		0001	Rewind and unload
		0010	Clean
01011	Initialize	0000	Drive initialize
01111	Get Status Immediate	0000	Get status (END message only)

Bits 3 and 4 of the command code field determine the format and length of command packets. The command packet formats and lengths are as follows.

Code Bits	Definition
00XXX	Four words (header, two word address, count)
01XXX	Two words (header, parameter word) or one word (header)

The swap byte bit in the command packet header word (bit 12) instructs the M7982 to alter the sequence of storing and retrieving bytes from the CPU's memory. When swap bytes equal 1, an industry-compatible sequence (beginning with an even byte) is used. When swap bytes equal 0, the swapping begins with an odd byte. (This is so only for data transferring; it is ignored otherwise.)

Figures 5-6 and 5-7 indicate the memory positions for the bytes as they are read from or written on the tape. In these examples, the bytes of data in the record block on tape are numbered starting at 0. Byte 0 is always the data byte at the beginning of the block (that is, the part of the block that is closest to BOT).

NOTE

When reading in reverse, the first data byte read is the last data byte of the sequence written. The read reverse command stores this first byte in the last buffer position; the next byte in the next-to-last buffer position, etc. This results in having data put in memory in the right order when reading the buffer sequentially.

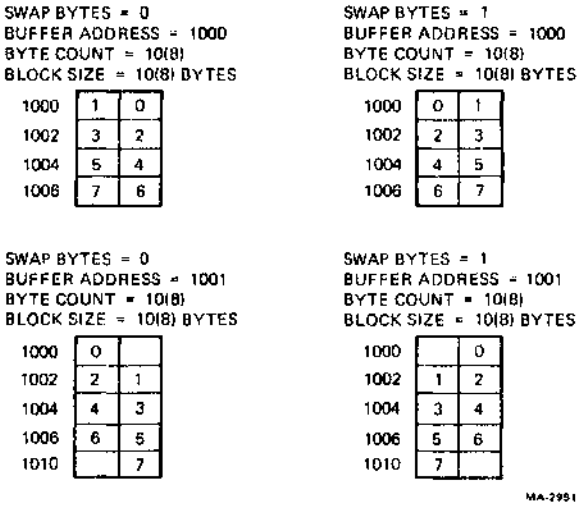


Figure 5-6 Byte Swap Sequence, Forward Tape Direction (Read or Write)

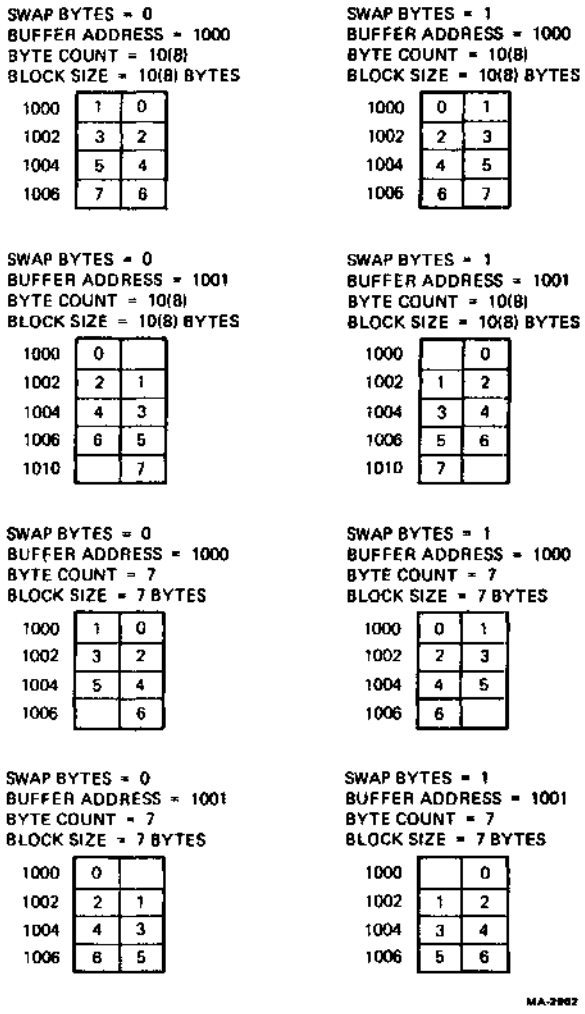


Figure 5-7 Byte Swap Sequence, Reverse Tape Direction (Read)

5.2.2 Command Packet Examples

This section provides examples of the command packets and operational programming notes used in the TS11. Refer to the figure and paragraph number corresponding to the command packet example you are interested in.

NOTE

All four words of the command packet are always read in, even if the command takes only one word (rewind) or two words (space). Thus, the command packet must contain four words, and it must have good parity because the transport will reject the command packet on the basis of errors in the unused words.

Command Packet Example	Figure Number	Para. Number
Get status	5-8	5.2.2.1
Read	5-9	5.2.2.2
Write characteristics	5-10	5.2.2.3
Write	5-11	5.2.2.4
Position	5-12	5.2.2.5
Format	5-13	5.2.2.6
Control	5-14	5.2.2.7
Initialize	5-15	5.2.2.8

5.2.2.1 Get Status Command – Figure 5-8 shows the get status command packet. This command causes an update of the five extended status registers in the message buffer area. However, after the end of any command, the TS11 hardware automatically updates the extended status registers. Therefore, this command need only be used when the TS11 has been left idle for some time or when a status register update is desired without performing a read, write, or position tape command.

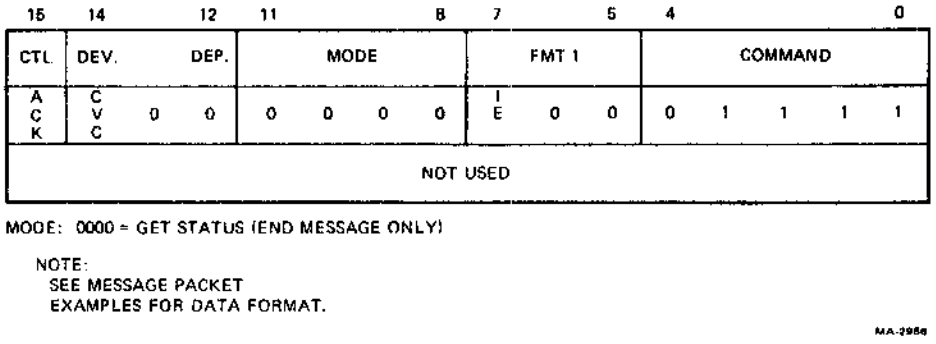


Figure 5-8 Get Status Command Packet Example

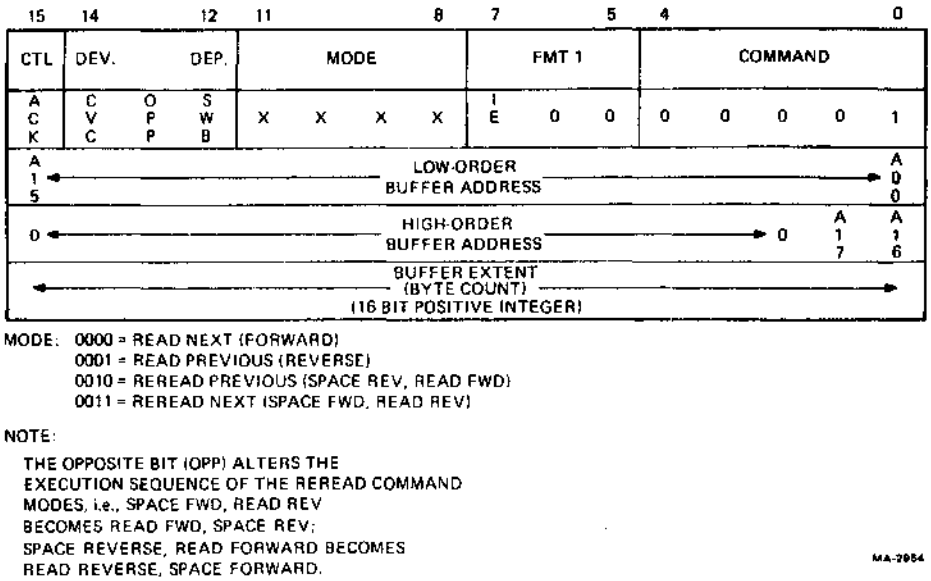


Figure 5-9 Read Command Packet Example

5.2.2.2 Read Command – Figure 5-9 shows the read command packet. There are four modes of operation: read forward, read reverse, reread previous, and reread next. In all cases a read operation is assumed to be for a record of known length. Therefore, the correct record byte count must be known. If the byte count is correct, normal termination occurs. If the record is shorter than the byte count, record length short (RLS) will set and a tape status alert (TSA) termination occurs. If the record is larger than the byte count, record length long (RLL) and tape status alert (TSA) will be set. Also, any read operation that encounters a tape mark does not transfer any data. In this case tape mark (TMK) and record length short (RLS) are set and a tape status alert (TSA) termination occurs.

Read reverse operations which run into BOT cause Reverse Into BOT (RIB) to set and cause a tape status alert (TSA) termination. Tape motion will stop at BOT. Read reverse while at BOT will cause a function reject (NEF) status, with no tape motion.

NOTE

When reading reverse, the first data byte read is the last data byte of the sequence written. The read reverse command stores this first byte in the last buffer position; the next byte in the next to last buffer position, etc. This results in having data put in memory in the right order when reading the buffer sequentially.

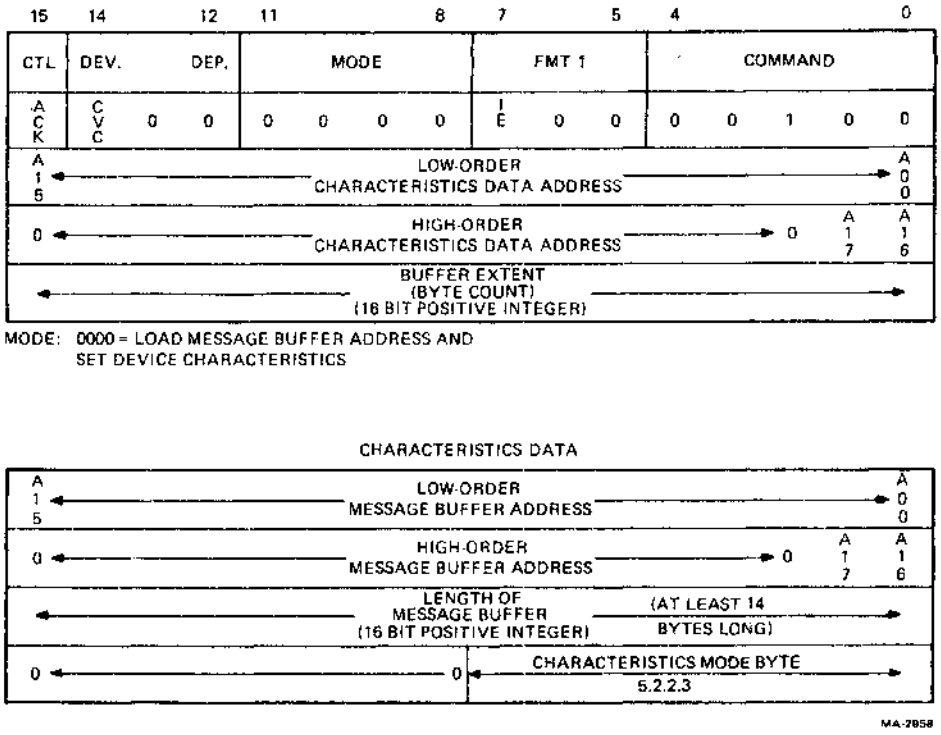


Figure 5-10 Write Characteristics Command Packet Example

5.2.2.3 Write Characteristics Command – Figure 5-10 shows the write characteristics command packet. This packet tells the TS11 the location and size of the message buffer in CPU memory space. The message buffer must be at least seven contiguous words long and begin on a word boundary.

The write characteristics command also transfers a characteristics mode word to the transport. This word causes specific actions for certain operational modes. Table 5-11 defines the bits for this word.

If a good message buffer address has not been loaded with a write characteristics command, the need buffer address (NBA) bit in the TSSR register is set.

The following notes concern bit usage in the characteristics word.

Interrupts Enabled – If interrupts are enabled (IE), interrupts may occur at any time. This is due to the possibility of diagnostic interrupts, ACLO, or CROM parity errors occurring immediately after normal terminations (even if ATTN interrupts are not enabled). The software must therefore defend against unexpected interrupts. The drive may not be usable, but the software still should not crash.

Attention Interrupts Enabled – With attention interrupts enabled, a nonfatal diagnostic failure is not reported until control of the message buffer returns to the transport. A fatal failure may interrupt at any time as long as interrupt enable is set. Also note that the drive could break in such a way that interrupts may be issued even with IE reset.

Attention Interrupts Disabled – With attention interrupts disabled, a diagnostic failure will not be noticeable until the next command is issued. At this time the command is rejected.

Table 5-11 Write Characteristics Data Bit Definitions

Bit	Name	Definition
15 to 08	–	Not used.
07	ESS	Enable Skip Tape Marks Stop: When this bit is set, it instructs the transport to stop during a skip tape mark command when a double tape mark (two contiguous tape marks) has been detected. In the default setting of 0, the skip tape marks command will terminate only on tape mark count exhausted or if it runs into BOT.
06	ENB	This bit is only meaningful if the ESS bit is set. If the drive is at BOT, when a skip tape marks command is issued and the first record seen is a tape mark, then the transport will set LET and stop after the first tape mark. If the bit is clear, the drive would not set LET but just count the tape mark and continue.
05	EAI	Enable Attention Interrupts: When this bit is a 0, attention conditions, such as off-line, on-line, and microdiagnostic failure, will not result in interrupts to the CPU. If set to a 1, interrupts will be generated.
		NOTE **Transport must own the message buffer, via message buffer release, to set attention interrupts.**
04	ERI	Enable Message Buffer Release Interrupts: If this bit is 0, interrupts will not be generated when a message buffer release command is received by the transport. Upon recognition of the command, only subsystem ready (SSR) will be reasserted. If ERI is a 1, an interrupt will be generated.
03	–	Not used.
02	–	Not used.
01	–	Not used.
00	–	Not used.

5.2.2.4 Write Command – Figure 5-11 shows the write command packet. There are two modes: write data and write data retry (space, reverse, erase, write data). Each operation is straightforward and designed to transfer data onto tape in the forward direction only.

If a write command is executed at or beyond the EOT marker a tape status alert (TSA), termination occurs. EOT remains set until passed in the reverse direction or a subsystem initialize.

If a write command is executed anywhere and the identification burst (IDB) was previously written bad or was not found when it left BOT, then density check (DENS ERROR) is set and tape position lost termination occurs.

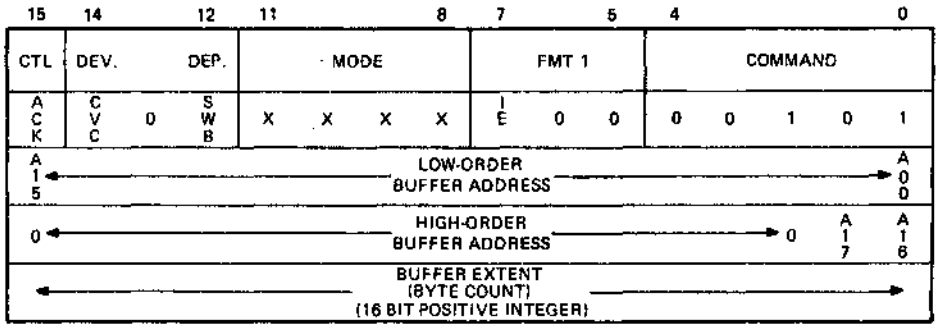


Figure 5-11 Write Command Packet Example

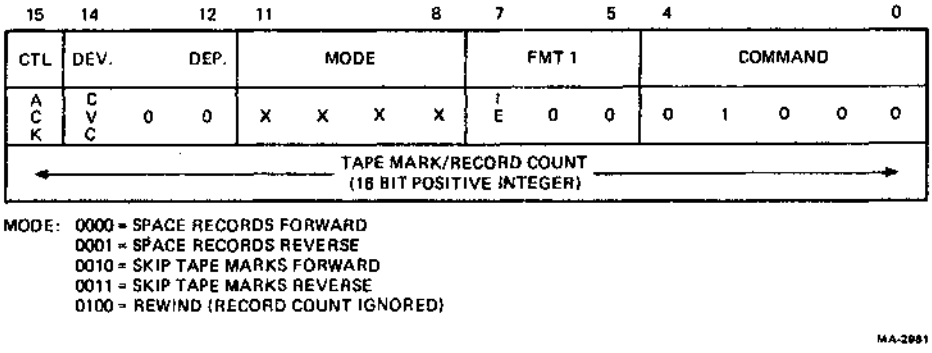


Figure 5-12 Position Command Packet Example

5.2.2.5 Position Command – Figure 5-12 shows the position command packet. This command causes tape to space records forward or reverse, skip tape marks forward or reverse, and to rewind to BOT. An exact tape mark/record count must be the second word of the packet for skip tape mark and space record commands.

A space records operation automatically terminates when a tape mark is traversed. Also, record length short (RLS) is set if the record count was not decremented to zero.

A skip tape marks command terminates when it encounters a double tape mark and the enable skip stop mode is specified (ESS bit set) in the characteristics word. Termination also occurs if a tape mark is the first record off BOT and ESS and ENB bits are set in the characteristics word. Record length short (RLS) is set if the record count is not decremented to zero.

A space records reverse or skip tape marks reverse, which runs into BOT, sets reverse into BOT (RIB) and causes a tape status alert termination.

When a rewind command is issued, the interrupt does not occur until the tape reaches BOT in the forward direction and starts to decelerate. Due to tape speed during rewind, the drive overshoots BOT in the reverse direction and then moves the tape forward until BOT is located before terminating the operation. Normal termination is indicated if the operation is completed without incident. If the tape is already at BOT, the rewind will still be done to make sure the tape is correctly positioned.

NOTE

If the tape is positioned between BOT and the first record and you do a space reverse or skip reverse, RIB will set and the residual frame count equals the specified count in the original command.

5.2.2.6 Format Command – Figure 5-13 shows the format command packet. This command can write a tape mark, rewrite a tape mark, and erase tape. In all cases, executing a format command at or beyond EOT causes a tape status alert (TSA) termination. The EOT bit remains set until passed in the reverse direction. A subsystem initialize can also reset the EOT bit. Also, any format command executed with density check (DENS ERROR) set causes a tape position lost termination.

Density check is set when an invalid identification burst (IDB) is read off BOT. This occurs in a read after write mode within the first three inches of tape and is transparent to the user's operation.

The erase command erases 3 inches of tape. This length is controlled automatically by the transport hardware. Successive erase commands can be used to erase more than three inches (in 3-inch increments).

5.2.2.7 Control Command – Figure 5-14 shows the control command packet. The three modes of operation are message buffer release, unload, and clean. The message buffer release command, when executed with the ACK bit set, allows the transport to own the message buffer so it can update the status in the message buffer area on an ATTN. This is beneficial when the operating system is processing data in other areas not concerned with operating the TS11 and the host wants to know the current drive status.

The unload command rewinds tape completely onto the supply reel. When the command is executed, termination occurs immediately; an interrupt occurs if IE is set.

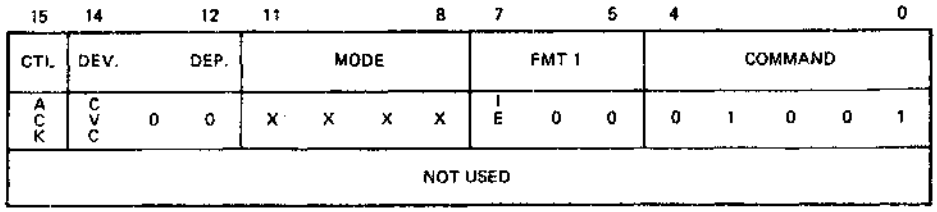
The clean tape command moves 10 inches of tape over the tape cleaners and returns it to the original position. Successive clean tape commands are not recommended since the tape may creep outside the interrecord gap (IRG) margins. Also, the clean tape command does not recognize BOT. (That is, you can clean tape and reverse past BOT and back again without setting status bits.)

5.2.2.8 Initialize Command – Figure 5-15 shows the initialize command packet. This command is not very useful, but is included for compatibility with packet protocol. A drive initialize can be done by a write to the TSSR, as this action does not need a command packet.

The drive initialize command is a no-op. It results in a message update, just like a get status, if there are no microdiagnostic or runaway errors. However, if errors are displayed, the command does the same thing as a write to the TSSR. Paragraph 5.1.3 contains TSSR details.

5.2.3 Message Packet Header Word

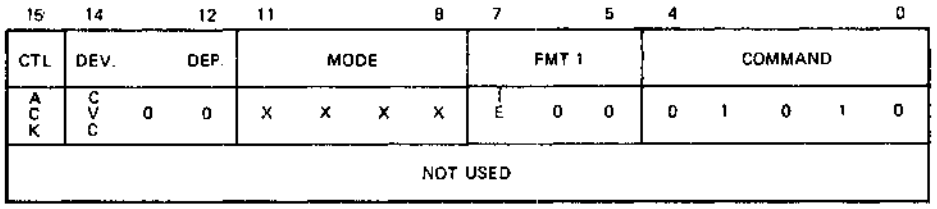
The first message packet header word is shown in Figure 5-16 and defined in Table 5-12.



MODE: 0000 = WRITE TAPE MARK
0001 = ERASE
0010 = WRITE TAPE MARK RETRY (SPACE REV, ERASE, WRITE TAPE MARK)

MA-2962

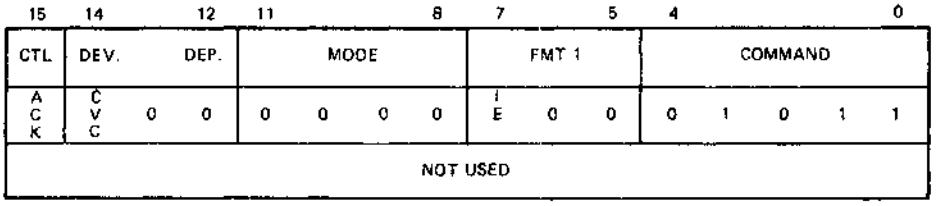
Figure 5-13 Format Command Packet Example



MODE: 0000 = MESSAGE BUFFER RELEASE
0001 = UNLOAD
0010 = CLEAN TAPE

MA-2960

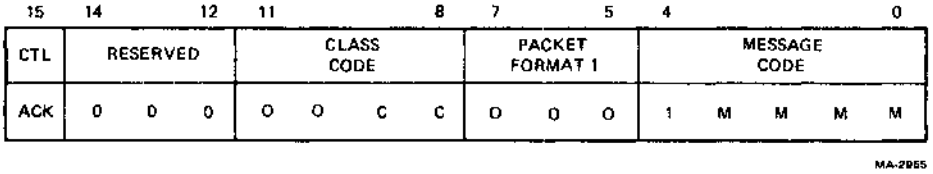
Figure 5-14 Control Command Packet Example



MODE: 0000 = DRIVE INITIALIZE

MA-2963

Figure 5-15 Initialize Command Packet Example



MA-2965

Figure 5-16 Message Packet First Header Word

Table 5-12 Message Packet First Header Word Bit Definitions

Bit	Name	Function
15	Acknowledge	This bit is used by the M7982 to inform the CPU that the command buffer is now available for any pending or subsequent command packets. On an ATTN message, this bit will not be set since the drive does not own the command buffer.
14 to 12	Reserved	These bits are reserved for future expansion.
11 to 8	Class Code Field	These bits define the class of failures found in the rest of the message buffer.

MSG Type	Class Value	Definition
ATTN	0000	On- or off-line
ATTN	0001	Microdiagnostic failure
FAIL	0000	Serial bus parity error (packet bad)
FAIL	0001	Other (ILC, ILA, NBA)
FAIL	0010	Write lock error or nonexecutable function
FAIL	0011	Microdiagnostic error

7 to 5	Packet Format #1 Field	The single value supported by the TS11 is as follows.

Value	Definition
000	One word header

4 to 0	Message Code		
	Term Class	**Value**	**Definition**
	0,2	10000	End
	3	10001	Fail
	4,5,6,7	10010	Error
	1,7	10011	Attention

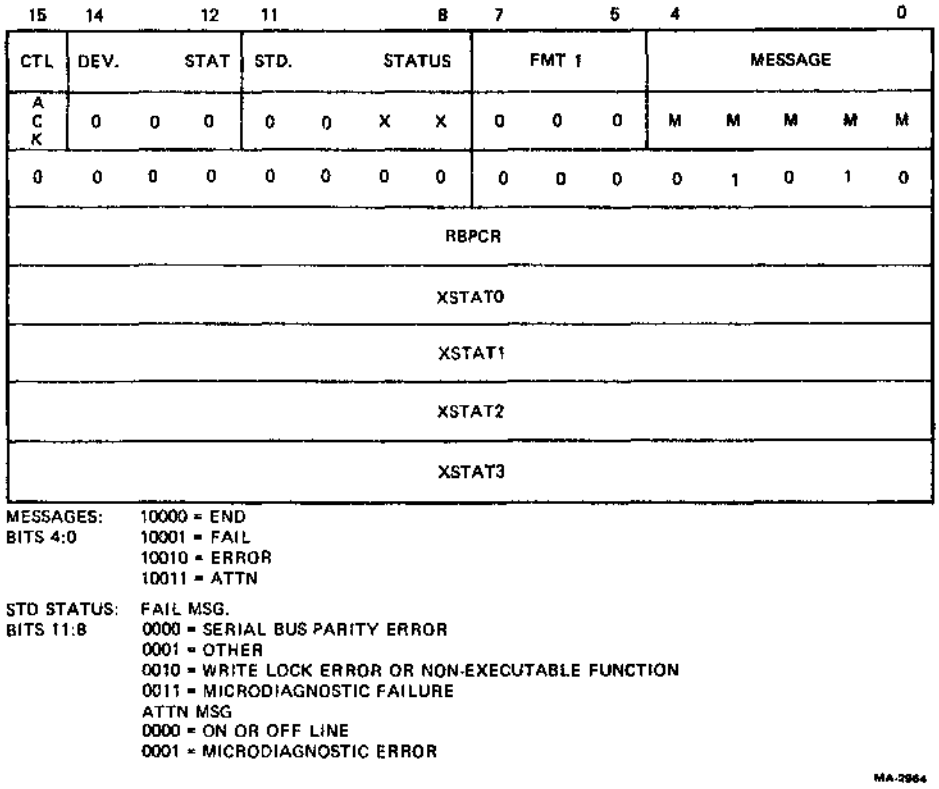


Figure 5-17 Message Packet Example

5.2.4 Message Packet Example

All message packets are identical. Each message packet contains the message packet header word just described, plus a data length field word and the five extended status registers. Figure 5-17 shows the message packet format.

5.3 OPERATIONAL INFORMATION

The following information considers the operation and programming requirements of the TS11.

5.3.1 Unibus Registers

Each TS11 has two Unibus word locations used as device registers. The base address, when written to, is the data buffer register (TSDB). When read, it is the bus address register (TSBA). The second device register (base address + 2) is the status register (TSSR). Writing to the TSSR causes a subsystem initialize command, and reading the TSSR reads device status.

The TSDB register is the only register written to during normal operations. DATO or word access must be used to properly write command pointers to the TSDB. DATOB or byte access to the TSDB causes maintenance functions.

Commands are not written to the drive's Unibus registers. Instead, command pointers, which point to a command packet somewhere in CPU memory space, are written to the TSDB register. The command pointer is used by the transport to retrieve the words in the command packet. The words of the command packet tell the transport the function to perform. They also contain any function parameters such as bus address, byte count, record count, and modifier flags.

5.3.2 Command and Message Packets

Command packets must reside on modulo-4 address boundaries within CPU memory space. This means the starting address of the packet must be divisible by 4 (that is, octal 00, 04, 10, 14, etc.).

All four words of a command packet must exist and have good memory parity, even if all four words are not used by a command. (For instance, rewind uses only one word.)

Message packets are issued by the subsystem and are deposited into the CPU's memory space. Controlled operation of the TS11 requires that it be supplied a message buffer address on a write characteristics command. The five extended status registers are stored in this message buffer area. The END message packet, which results at the end of any command, contains these extended status words.

5.3.3 Special Conditions and Errors

Table 5-13 includes the meanings of the binary values within the termination class code field in the TSSR register. Table 5-14 shows the fatal class code field for the TSSR.

Table 5-13 Termination Class Codes

TC2-0 Value	Msg Type	Offset	Meaning
0	END	00	Normal Termination: This bit indicates the operation was completed without incident.
1	ATTN	02	Attention Condition: This code indicates that the transport has undergone a status change: going off-line, coming on-line, or a microdiagnostic failure.
2	END	04	Tape Status Alert: This bit indicates a status condition has been encountered that may have significance to the program. Bits of interest include TMK, EOT, RLS, and RLL.
3	FAIL	06	Function Reject: This bit indicates the specified function was not initiated. Bits of interest include OFL, VCK, BOT, WLE, ILC and ILA.
4	ERR	10	Recoverable Error: This bit indicates tape position is one record beyond what its position was when the function was initiated. Suggested recovery procedure is to log the error and issue the appropriate retry command.
5	ERR	12	Recoverable Error: This bit indicates tape position has not changed. Suggested recovery procedure is to log the error and reissue the original command.

Table 5-13 Termination Class Codes (Cont)

TC2-0 Value	Msg Type	Offset	Meaning
6	ERR	14	Unrecoverable Error: This bit indicates tape position has been lost. No valid recovery procedures exist unless the tape has labels or sequence numbers.
7	ATTN/ERR	16	Fatal Subsystem Error: This bit indicates the subsystem is incapable of properly performing commands or at least that the subsystem's integrity is seriously questionable. Refer to the fatal class code field in the TSSR register for additional information on the type of fatal error.*

* The fatal class code field in the TSSR register is defined in Table 5-14. The meanings are valid when the termination class code bits are all set (value of 7, offset of 16).

Table 5-14 TSSR Fatal Class Codes

FC1-0 Value	Meaning
0	This bit indicates there is an internal microdiagnostic failure in the diagnostic mode or a capstan runaway in the operational mode (337 octal in operator panel). See the fatal error code byte (XSTAT3) for the diagnostic function. This is cleared by the drive initialize command or subsystem initialize. Subsequent tape operations will not be accepted (command reject) until, as a minimum, a drive initialize is issued.
1	There is a I/O CROM parity error. This is cleared by drive initialize or subsystem initialize.
2	There is a microprocessor CROM, I/O silo, serial bus parity error, or another fatal error. This is cleared only by subsystem initialize.
3	Loss of ac power has been detected and a power down is in effect. This is cleared only by subsystem initialize.

5.3.4 Status Error Handling Notes

TSSR error bits, other than the fatal class, termination class, and SC bits, are cleared by loading a command pointer into the TSDB register. SC is reset if it is due to a TSSR error (UPE, SPE, RMR, or NXM). Extended status error bits are cleared after the END message is sent.

All commands (even get status command) clear the XSTAT error bits; except XSTAT3 bits 15 through 8 (microdiagnostic error code) and bit LXS are not cleared.

If a density check condition is detected during a read, space, or skip function, the DCK bit is set, but the operation is not stopped. If DCK is the only status bit set during the operation, normal termination is reported. This allows tapes with good data but bad density check areas to be read. If a wrong density tape has been mounted, other errors are reported and the operation stops. Note that if only the density check area is bad, the density check indicator on the drive's operator panel indicators, even though the data records might be the correct density. The DENS ERROR indicator stays on until BOT is encountered again or until a subsystem initialize is performed. Note that if you begin reading a tape, get a density check condition with no other errors, then append to the tape; the write will get a termination class code of 6. This indicates that the tape position is lost because density check will remain set. The whole tape should be copied over so that drives depending on the IDB can read the tape.

A command is not responded to while another command is in progress (result is RMR), except in the following cases.

1. A DATO (word access) to the TSSR (subsystem initialize) brings any operation in progress to an immediate halt. All subsystem parameters which had been in the subsystem's memory (VOL VALID reset, EOT, etc.) are erased. Also, if the ON-LINE switch is on, the drive performs an auto-load sequence and positions the tape at BOT.

2. The transport responds to any nontape motion command while performing a rewind unload (while the drive is off-line) because SSR is still up.

The transport also responds to any nontape motion commands (get status, drive initialize, set characteristics, and message buffer release) when off-line, except when in maintenance mode. (The subsystem ready command, SSR, is not asserted in this case and results in RMR.)

The following failures can occur without resulting in an interrupt, even though the specified command had interrupt enable set.

SPE	The possibility exists that the drive cannot transfer valid data or command information via the serial bus to the TS11. In this case the SC, TC2, TC1, and TC0 bits are not valid either.
NXM UPE BPE	These might occur before the interrupt enable bit is fetched as part of the command packet.

These cases may result in a hung controller (SSR does not come up again until a subsystem initialize). The same is true when the fatal class codes are 2 or 3.

5.4 OPERATIONAL DIFFERENCES

The following describes three differences in the operation of the TS11 compared to earlier DECmagtape products.

- The skip tape marks (files) function is implemented in the hardware on this subsystem. Earlier DECmagtapes had this function emulated by the software driver through use of the space records command.

- If a space records command is issued while positioned at or beyond EOT, the operation is not terminated after one record has been traversed. The termination criteria remains the same as for any other location on tape; that is, record count exhausted or tape mark encountered. The skip tape marks command operates in the same manner. EOT is not allowed to alter its operation.

- A skip files command could take 15 to 20 minutes to complete to the end of a 2,400 foot reel of tape. There is no abort procedure other than a subsystem initialize. This causes an automatic load sequence.

NOTE

As a debugging aid, set the message buffer to all 1s. This eliminates any confusion that might be caused by earlier messages.

a. Load a scratch tape to BOT. Place the unit into maintenance mode. *Carefully* remove the clamp washers on the top of the fixed guides. A ceramic washer under the clamp washer comes off at the same time. Handle these washers with care; they are extremely hard and brittle. Also, note that the washer is beveled on one side. This beveled side must be mounted facing the tape when you reassemble the guides. When you remove the screw holding the washer, the guide remains mounted to the headplate.

b. Use test 50 and move the tape forward and reverse. Observe the relative position of the tape with respect to the capstan. Ideally, the tape should remain in the center of the capstan when tape is moving in either direction. If the tape moves on the capstan when you change directions, use an Allen wrench to turn gimbal screw 1 (Figure 7-14) about one turn (in either direction, remembering which direction you turned the screw). Perform this adjustment while the tape is moving. If the tape motion is reduced, you are turning the screw in the right direction. If motion increases, turn the screw in the opposite direction.

   Repeat the above procedure until there is no visible tape motion on the capstan. Then stop test 50.

c. Now use test 11 to run the tape in a steady state condition forward. If the tape is not tracking in the center of the capstan, turn gimbal screw 2 (Figure 7-14) as follows. If the tape is tracking too close to the deckplate, turn screw 2 counterclockwise. If the tape is tracking away from the deckplate, turn the screw in a clockwise direction.

d. Use test 11 to run the tape in a steady state condition, and press the two spring-loaded washers on the lower part of the fixed guides. Monitor the reference edge of the tape (the edge closest to the operator). It should track right at the edge of the top of both guides. If this does not happen, adjust screw 2.

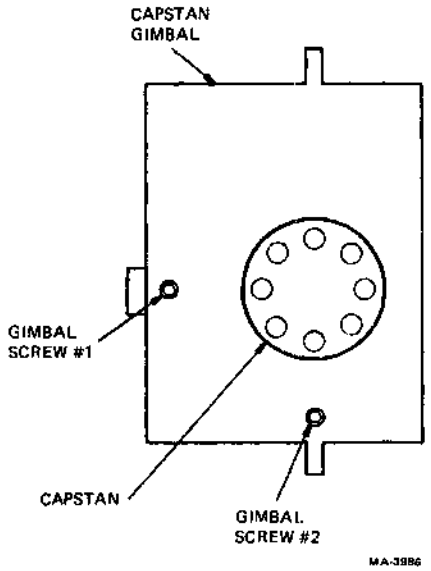


Figure 7-14 Capstan Gimbal Adjustment

CHAPTER 6
THEORY OF OPERATION

6.1 INTRODUCTION

This chapter provides a functional description of TS11 operation. Each function in the TS11 block diagram (Figure 6-1) is described. The Unibus interface board (M7982) is included in the I/O functional description. The read function, PE formatter, and write function descriptions are subsections of the tape data handling function. In addition, Paragraph 6.2 identifies what functions are contained on the various boards and defines the various buses. Paragraph 6.7 describes the function of the μP BBUS and I/O branch bus. Throughout this chapter, the designation TS11 refers to the entire subsystem (that is, M7982 and everything contained in the TS11 cabinet).

NOTE

In this chapter the abbreviation μP is used for the control microprocessor.

This chapter does not describe the principles or standards of magnetic recording techniques; nor does it include descriptions of how the various linear and digital IC circuits operate. Gate-by-gate descriptions are included only where necessary. Detailed descriptions of how the microcode operates are not within the scope of this chapter; however, various CROM (both μP and I/O) bit tables are included. The tape transport is controlled through the two CROMs which select/enable OBUS destinations, IBUS sources, discrete logic conditions, BBUS and branch sources, and sequencing.

Major data flow for a write operation is from the Unibus, through the Unibus interface board to the serial bus; over the serial bus to the shift register in the serial bus control board; over the Shift Register (SR) lines to the silo in the silo and frame count board; from the silo to the write control board and the write heads.

On a read operation, data flows from the read heads through the read preamplifier and read amplifier boards; through the PE formatter to the μP IBUS; over the μP IBUS to the μP OBUS via the ALU and timing board; over the μP OBUS to the silo; from the silo in the silo and frame count board over the SR lines to the shift register in the serial bus control board; from the shift register over the serial bus to the Unibus via the Unibus control board. The remainder of this chapter describes the operations necessary to implement the data flow.

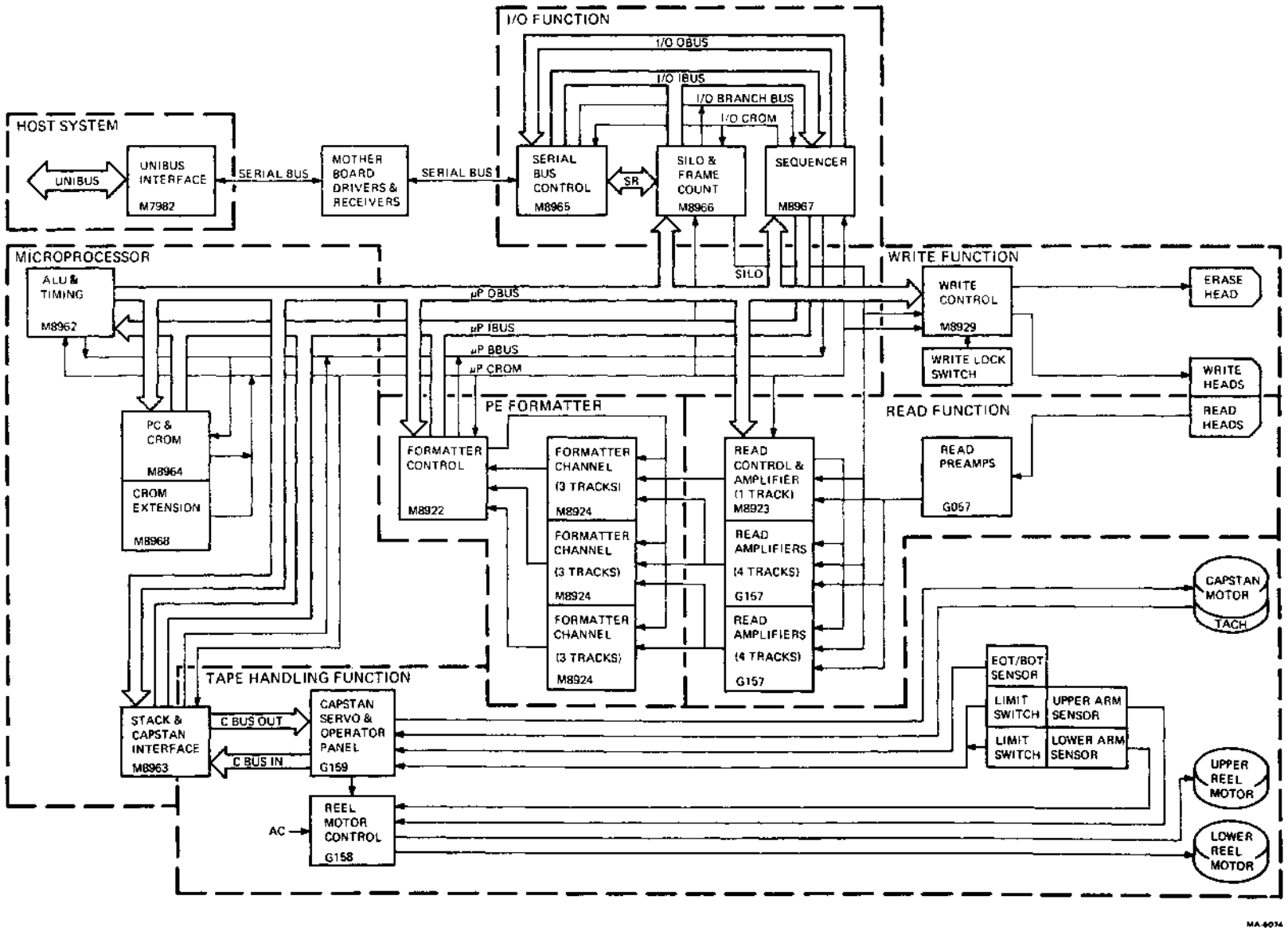


Figure 6-1 TS11 Block Diagram

6.2 SYSTEM DESCRIPTION

This section describes the physical location of the TS11 functional components on each module, the TS11 buses, and major interconnecting lines.

6.2.1 Modules

This section describes the TS11 modules.

6.2.1.1 M7982, Unibus to Serial Bus Controller – This module contains the Unibus transceivers and handshake circuits, device address and vector switches, the address register TSBA, the data buffer TSDB, the status register TSSR, address decode logic, op code generator and latch, and serial bus control and parity circuits. The Unibus and serial bus are connected to this module, which is mounted in a small peripheral controller slot in the host system.

6.2.1.2 G057, TS04 Read Preamplifiers – This module contains the read preamplifiers and adjustments for all nine tracks, and is mounted on the tape transport assembly (Figure 6-2).

6.2.1.3 G157, TS04 Read Amplifiers – Each of the two G157 modules contains four read amplifiers and threshold checking circuits for the data tracks. (The read amplifier for the parity track is part of the M8923 module.) Both modules are mounted on the motherboard (Table 6-1).

6.2.1.4 G158, Reel Servo – This module contains the upper and lower tension arm position sensor amplifiers, the servo amplifiers for the supply and take-up reel motors, and the parking brake control logic for each reel motor. It is mounted on the tape transport assembly (Figure 6-2).

6.2.1.5 G159, Capstan Servo – This module contains the capstan control circuitry, the capstan tachometer amplifier, capstan status multiplexers, EOT and BOT sensing amplifiers, and operator panel pushbuttons and indicators. It connects to CBUSI and CBUSO and is mounted on the tape transport assembly (Figure 6-2). All of the following modules are mounted on the motherboard as shown in Table 6-1.

6.2.1.6 M8922, Branch Logic and VCO Control – This module contains the voltage-controlled oscillator (VCO) and its control logic, the major state register, vertical parity error detection logic, and a ROM data pattern look-up table. This table decodes such things as ID bursts, tape marks, and preambles, as part of the branch control logic. The VCO connects to the main CROM, μP BBUS, μP IBUS, and μP OBUS via an over-the-top connector to M8962 (Table 6-2).

6.2.1.7 M8923, Read Control – This module contains the read amplifier for the parity track, read threshold level generation circuitry for all tracks, read command logic for all tracks, and skew measuring circuitry. It connects to the μP OBUS.

6.2.1.8 M8924, PE Formatter – Each of the three M8924 modules contains window control logic, data discrimination logic, dead track logic, and deskew buffer logic for three tracks.

6.2.1.9 M8929, Write Control – This module contains the write control logic, write data buffers, write strobe generators, write head drivers, and erase head driver. It connects to the μP OBUS.

6.2.1.10 M8962, Microprocessor Board 1 – This module contains the dual 2901 main microprocessor, its associated control and attention (pseudointerrupt) logic, and the system clock crystal oscillator and distribution circuits. It connects to the M8922 module via an over-the-top connector (Table 6-2). It also connects to the μP BBUS, μP IBUS, and μP OBUS.

6.2.1.11 M8963, Microprocessor Board 2 – This module contains a 64-location × 9-bit RAM with control logic that permits random or stack addressing, and the control logic for the capstan bus (CBUS). It connects to CBUSI, CBUSO, μP BBUS, μP IBUS, and μP OBUS.

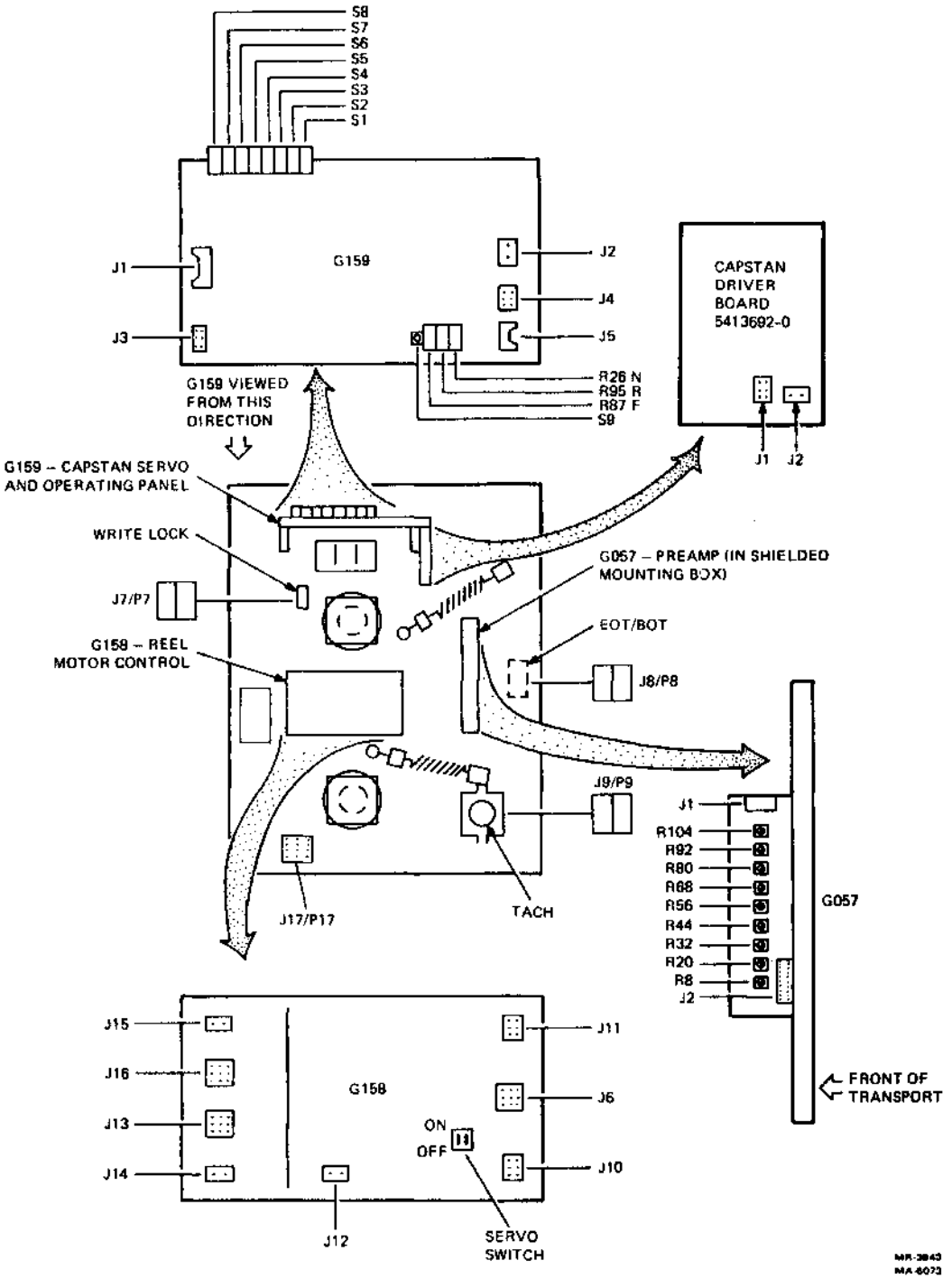


Figure 6-2 Tape Transport Assembly

Table 6-1 Module Layout

Module	Motherboard Connector	Slot	
G157	A1/B1	J6	1
G157	A2/B2	J7	2
M8923	A3/B3	J8	3
M8924	A4/B4	J9	4
M8924	A5/B5	J10	5
M8924	A6/B6	J11	6
M8922	A7/B7	J12	7*
M8962	A8/B8	J13	8*
M8964	A9/B9	J14	9
M8968	A10/B10	J15	10
M8963	A11/B11	J16	11
M8967	A12/B12	J17	12
M8929	A13/B13	J18	13
M8966	A14/B14	J19	14
M8965	A15/B15	J20	15

* Refer to Table 6-2 for over-the-top connector wiring.

Table 6-2 M8922–M8962 Over-the-Top Connector Pins

Signal Name		Pin	Signal Name		Pin
μP CROM 00 B	H	EU1	μP OBUS 3	H	ES2
μP CROM 01	H	EN2	μP OBUS 4	H	EE2*
μP CROM 08	H	ED1*	μP OBUS 5	H	EF2*
μP CROM 09	H	EP2*	μP OBUS 6	H	EV1
μP CROM 10	H	EU2*	μP OBUS 7	H	EL2
μP CROM 17 B	H	EV2	μP IBUS 0	H	EA1
μP CROM 18 B	H	ES1	μP IBUS 1	H	EK1
μP CROM 19 B	H	EK2	μP IBUS 2	H	EM1
μP CROM 20 B	H	EJ2	μP IBUS 3	H	EL1
μP CROM 21	H	ER1	μP IBUS 4	H	EC1
μP CROM 22	H	ED2	μP IBUS 5	H	EB1
μP CROM 23	H	EE1	μP IBUS 6	H	EF1
μP CROM 24	H	EN1	μP IBUS 7	H	EJ1
μP OBUS 0	H	ER2	BBUS H		EH1
μP OBUS 1	H	ET2	FMT CLK L		EH2
μP OBUS 2	H	EM2	WRT CLK L		EP1

* No connection to pin on M8922 board.

6.2.1.12 M8964, ROM Board – This module contains 2048 locations of 28-bit control ROM (CROM), the program counter (PC) and its control logic, and logic to address an additional 4096 locations of CROM contained on the M8968 board. M8964 connects to the μP BBUS, μP IBUS, and μP OBUS. CROM outputs from this board and M8968 are connected as shown in Table 6-3. Tables 6-4 and 6-5 show CROM field configurations for addressing registers/multiplexers.

Table 6-3 CROM Bit Pin Out

Microprocessor CROM Bit	Module M8964 M8968	M8962	M8922 *	M8923	M8929	M8963	M8966	M8967
	Pin							
00	BP2	BP2†	EU1	–	–	BP2	–	–
01	AC1	AC1†	EN2	AN1	AA1	AC1	AC1	AC1
02	AB1	–	–	–	–	–	–	–
03	BM2	–	–	–	–	–	–	–
04	AJ1	AJ1	–	–	–	–	–	–
05	–	AF2	–	–	–	–	–	–
06	AE2	AE2	–	–	–	–	–	–
07	AJ2	AJ2	–	–	–	–	–	–
08	BV2	BV2	ED1†	–	–	–	–	–
09	AS1	AS1	EP2†	–	–	–	–	–
10	AT2	AT2	EU2†	–	–	–	–	–
11	BV1	BV1	–	–	–	–	–	–
12	BE2	BE2	–	–	–	–	–	–
13	BH2	BH2	–	–	–	–	–	–
14	BL2	BL2	–	–	–	–	–	–
15	BB2	BJ1	–	–	–	AV1	–	–
16	BF2	–	–	–	–	–	–	–
17	AK2	AK2	EV2	–	–	AK2	–	AK2
18	AP1	AP1	ES1	–	–	AP1	–	AP1
19	AR1	AR1	EK2	–	–	AR1	–	AR1
20	AS2	AS2	EJ2	–	–	AS2	–	AS2
21	BB1	BB1	ER1	BA1	AB1	BB1	BB1	BB1
22	BK2	BK2	ED2	AR1	BV1	BK2	BK2	BK2
23	BJ2	BJ2	EE1	AS1	BV2	BJ2	BJ2	BJ2
24	BK1	BK1	EN1	AU1	AJ1	BK1	BK1	BK1
25	BF1	BF1	–	–	–	–	–	–
26	BE1	BE1	–	–	–	–	–	–
27	AP2	–	–	–	–	–	–	–

* Via M8962 board and over-the-top connector (Table 6-2)
† Not used on this board.

Table 6-4 CROM Field Configuration

I*	O†	Register or Signal Addressed	Print Set Page Register	Address Logic	Remark
22	30	U STACK ADDRESS REG	M8963-1	M8963-2	MUX M8963-2
–	32	PUSH/STACK WRITE	–	M8963-2	–
23	–	POP/STACK READ	–	M8963-1	–
–	33	FORCE STACK PAR ERR	–	M8963-2	–
–	31	RESET AC-LO IN ATTN REG	–	M8963-2	Control bit
03	–	U ATTEN REG	M8963-2	M8963-2	STK DATA MUX
01	02	PC BUFF LO ORDER BITS	M8964-3	M8964-2	MUX M8964-2
–	22	PC BUFF HI ORDER BITS	M8964-3	M8964-3	Write only
–	36	ATTEN ENAB + CAP MUX SEL	M8963-3	M8963-2	–
02	–	CAPSTAN DATA INPUT	M8963-2	M8963-2	MUX and STK ADD
–	37	CAPSTAN BD DATA OUTPUT	M8963-3	M8963-2	–
–	11	I/O SEQUENCER CONTROL	M8967-2	M8967-1	–
–	10	I/O SEQUENCER DATA OUT	M8967-2	M8967-1	–
–	15	I/O SILO DATA⁻ BUFFER OUT	M8966-1	M8966-2	–
–	14	I/O SILO CTL BUFFER OUT	M8966-1	M8966-2	–

* Micro input address from CROM (0,20) (19,18,17) octal

† Micro output address from CROM (1,24) (23,22,21) octal

Table 6-4 CROM Field Configuration (Cont)

I*	O†	Register or Signal Addressed	Print Set Page Register	Address Logic	Remark
17		I/O SEQUENCER DATA IN	M8967-2	M8967-1	–
–	16	I/O SILO CLOCK	–	M8966-2	Clocks silo.
–	13	I/O RESTART AT LOC 0	–	M8967-1	Restart I/O μP.
–	12	RESET I/O RDY BIT	–	M8967-1	–
–	17	WRITE I/O FRAME COUNT	M8966-2	M8966-2	Low byte
05	–	FORMATTER OUTPUT READY	M8922-2	M8922-3	From 3 M8924 boards
25	–	ONES OR DEAD TRACK	M8922-2	M8922-3	
06	–	TRACK ACTIVE UNDESKEWED	M8922-2	M8922-3	
26	–	FORMATTER DATA (DESKEWED)	M8922-2	M8922-3	
07	–	DEAD TRACK (DESKEWED)	M8922-2	M8922-3	
27	–	ZEROS OR DEAD TRACK	M8922-2	M8922-3	
–	04	MAJOR STATE CONTROL	M8922-3	M8922-3	–
–	05	CLOCK DESKEW BUFFER	–	M8922-3	Clocks silo.
–	20	READ CONTROL REGISTER	M8923-1	M8923-1	–
–	01	WRITE CONTROL REGISTER	M8929-1	M8929-2	–
–	23	CLEAR FIELD BIT	M8968-2	M8968-2	External address
–	24	SET FIELD BIT	M8968-2	M8968-2	External address

Table 6-5 I/O CROM Field Configuration

I*	O†	Register or Signal Addressed	Print Set Page Register	Address Logic	Remark
01	–	DATA INPUT REG (MUX)	M8967-3	M8967-2	From main μP
02	–	HIGH ORDER FRAME COUNT	M8966-2	M8967-2	–
03	–	SILO DATA REG	M8966-2	M8967-2	From I/O silo
04	–	SHIFT REG (MUX)	M8965-3	M8967-2	Low byte
05	–	OPCODE AND ERROR REG	M8965-3	M8967-2	From M7892
–	00	8 BITS OF I/O PC	M8967-2	M8967-2	Low byte
–	01	2 BITS OF I/O PC	M8967-2	M8967-2	High bits
–	02	DATA OUTPUT REG	M8967-2	M8967-2	To main μP
–	10	OPCODE REG	M8965-1	M8965-3	To M7982
–	15	SHIFT REG (HIGH BYTE)	M8965-1	M8965-3	–
–	16	SHIFT REG COUNTER	M8965-3	M8965-3	–
–	17	HI UNIBUS ADDRESS 2 BITS	M8965-1	M8965-3	A16, A17

* Micro input address from CROM (0,20) (19,18,17) octal
† Micro output address from CROM (1,24) (23,22,21) octal

NOTE
The next three modules are commonly called the I/O microprocessor.

6.2.1.13 M8965, I/O Section 1 – This module contains the op code shift, high shift, and low shift registers, and their associated control logic. It connects to the Shift Register (SR) lines, I/O BBUS (I/O branch bus), I/O IBUS, I/O OBUS, and the serial bus.

6.2.1.14 M8966, I/O Section 2 – This board contains the 8-bit × 64-location control silo and identical data silo, their associated buffers and control logic, and the frame counter. It connects to the SR lines, I/O BBUS, I/O IBUS, I/O OBUS, and μP OBUS.

6.2.1.15 M8967, I/O Section 3 – This module contains 1024 locations of dedicated 16-bit CROM, its own PC, test and branch logic, system clock regeneration circuits, a control register, and logic to set the main microprocessor attention flag. It connects to the I/O BBUS, I/O IBUS, I/O OBUS, μP BBUS, μP IBUS, and μP OBUS.

6.2.1.16 M8968, ROM Extension Board – This board contains 4096 locations of 28-bit main microprocessor CROM. Its CROM outputs are the same as those of the M8964 board.

6.2.2 Buses and Major Interconnecting Lines

This section describes the TS11 buses and their interconnecting lines.

6.2.2.1 Unibus – The Unibus connects the TS11 to the host system via M7982. It is a standard 56-line Unibus.

6.2.2.2 Serial Bus – The serial bus contains six active lines. Table 6-6 lists the lines, connecting points, signal names, and direction. The lines are run in a 20-conductor cable between 20-pin connectors (J1 and J4 in Table 6-6), with the unused lines grounded.

6.2.2.3 Shift Register Lines – The SR lines consist of eight lines. They get I/O OBUS data from M8965 and SR DATA IN from M7982, and carry it to the I/O IBUS input multiplexer on M8965.

Table 6-6 Serial Bus Configuration

M8965 Signal Name		J20 Pin	Motherboard Signal Name	J4 Pin	M7982 Signal Name		J1 Pin
SR CLK		BN2 →	BUS CLK OUT	18 →	SER BUS CLK		3
SER BUS DAT	OUT	BV1 →	BUS DATA OUT	6 →	SER BUS DAT	FM DRV	15
SER BUS SHFT	OUT	BV2 →	BUS SHFT OUT	12 →	SER BUS SHFT	FM DRV	9
SER BUS CLR		BS1 ←	BUS CLR	15 ←	SER BUS INIT		6
SER BUS DAT	IN	BU1 ←	BUS DATA IN	3 ←	SER BUS DAT	TO DRV	18
SER BUS SHFT	IN	BR1 ←	BUS SHFT IN	9 ←	SER BUS SHFT	TO DRV	12

6.2.2.4 Input/Output BBUS – The I/O branch bus is a single-bit bus with two lines (high and low). Multiplexers on any of the three I/O boards can assert the I/O BBUS and thereby enable part of the logic to load the I/O microprocessor PC on M8967.

6.2.2.5 Input/Output IBUS – The I/O input bus is an eight-line multiplexed bus connected to each of the I/O boards. The following are inputs to the I/O IBUS.

SR lines
Op code and error bits on M8965
Data silo
μP OBUS
I/O CROM

The I/O IBUS is an input to the I/O OBUS and the μP IBUS on M8967.

6.2.2.6 Input/Output OBUS – The I/O output bus is an eight-line bus that is connected from M8967 to M8965. It gets its input from the I/O IBUS on M8967 and is the data (next location) input to the I/O PC on that board. On M8965, the I/O OBUS is the data input to the op code shift register and high shift register.

6.2.2.7 Main Microprocessor BBUS – The bit bus is a single-line multiplexed bus that carries a selected error or status signal from multiplexers on M8922, M8962, M8963, or M8967 to M8964. On M8964, it enables part of the logic to load the main PC.

6.2.2.8 Main Microprocessor IBUS – The input bus is an eight-line multiplexed bus that carries data to the main microprocessor on M8962. It is also an input to the μP OBUS on the M8962. The μP IBUS gets its input from multiplexers on M8922, M8963, M8964, or M8967.

6.2.2.9 Main Microprocessor OBUS – The output bus is an eight-line bus that gets its input on M8962 from either the main microprocessor or the μP IBUS. It is an input to the major state register on M8922, the input register on M8923, the write control register on M8929, the COM OBUS on M8963, the main PC on M8964, the control silo, data silo, and I/O IBUS multiplexers on M8966, and the data input and control register on M8967.

6.2.2.10 Main Microprocessor CROM Lines – Sometimes referred to as the μP CROM bus, the main CROM lines carry CROM bit data from M8964 and M8968 (Table 6-3).

6.2.2.11 COM OBUS – The COM OBUS is an extension of the μP OBUS and is confined to M8963. It provides data and address input to the stack and is the input to 10 of the 12 CBUSO lines.

6.2.2.12 Capstan Output Bus – CBUSO consists of 12 lines that carry capstan command and operator panel status information from M8963 to J1 on G159. Table 6-7 lists command and status interpretation.

6.2.2.13 Capstan Input Bus – CBUSI is an eight-line multiplexed bus that carries status information from G159 to M8963. Table 6-8 lists multiplexed status.

Table 6-7 CBUSO Command and Status Interpretation*

CBUS ADDR 0 to 2	Function	
	Commands – Capstan and Maintenance (CBUS REG SEL = 0)	
7	Maintenance Mode	
6	Simulate Tachometer Phase 1	
5	Simulate Tachometer Phase 2	
4	Rewind	
3	Forward	
2	Reverse	
1	Clock Enable	
0	μP Reel Enable	
	Status – Operator Panel Indicators (CBUS REG SEL = 1)	
7	LOAD REW UNLD	Load
6	ON-LINE	On-line
5	MICRO OK	Main μP okay
4	VOL VALID	Volume check
3	DENS ERROR	Density check
2	WRITE LOCK	Write lock
1	EOT	End of tape
0	BOT	Beginning of tape

* CBUS WRT REG = 1, CBUS REG DATA = 1

Table 6-8 CBUSI Status Interpretation

CBUS MUX 1	CBUS MUX 0	CBUSI 0 to 7	Function	
0	0		**Switch/Sensor Status**	
		0	EOT	End of tape
		1	BOT	Beginning of tape
		2	WLK SWIT	WRITE LOCK switch
		3	ENTER ZERO	EOT switch. Enter 0s in maintenance mode.
		4	DO IT SWIT	LOAD switch. Enter 1s in maintenance mode.

Table 6-8 CBUSI Status Interpretation (Cont)

CBUS MUX 1	CBUS MUX 0	CBUSI 0 to 7	Function	
0	0		**Switch/Sensor Status**	
		5	LIMIT	Tension arm limit switch
		6	ONL SWIT	ON-LINE switch. In maintenance mode: a. Start/stop test. b. Load tape if not already loaded.
		7	RL MTRON	Reel Motor On
0	1		**Capstan/Switch/Sensor Status**	
		0	EOT	End of tape
		1	BOT	Beginning of tape
		2	MOVING	Capstan Motion
		3	FWD DIR	Capstan Direction
		4	TACH2	Tachometer Phase 2
		5	LIMIT	Tension arm limit switch
		6	TACH1	Tachometer Phase 1 (or CS3 1 KHz)
		7	RL MTRON	Reel Motor On
1	0		**Operator Panel Indicator Status (Readback CBUSO)**	
		0	EOT LT	EOT indicator
		1	BOT LT	BOT indicator
		2	WRITE LOCK LT	WRITE LOCK indicator
		3	IDB LT	DENS ERR indicator
		4	VV LT	VOL VALID indicator
		5	MICRO OK LT	MICRO ok indicator
		6	ON LINE LT	ON-LINE indicator
		7	LOAD LT	LOAD indicator
1	1		Capstan Speed Register	
		0 to 7	CS0 to CS7	

6.3 CONTROL MICROPROCESSOR

The control microprocessor (μP) is the central control element of the tape subsystem. All other functional areas of the tape subsystem depend on the control microprocessor for their control inputs.

This chapter uses "μP" or "main μP" interchangeably when referring to the control microprocessor.

The μP consists of an ALU and timing board (M8962), a program counter and control ROM board (M8964), a control ROM extension board (M8968), and part of M8963 (stack logic).

6.3.1 Microprocessor Basic Description

The "heart" of the μP is made up of the control read only memory (CROM), the CROM addressing logic (PC, branch logic, and associated data paths) and the ALU (two AMD 2901s). The timing and clock control logic generates the timing signals used for moving data throughout the tape subsystem.

Refer to Figure 6-3 for a basic block diagram of the major elements and data paths of the μP.

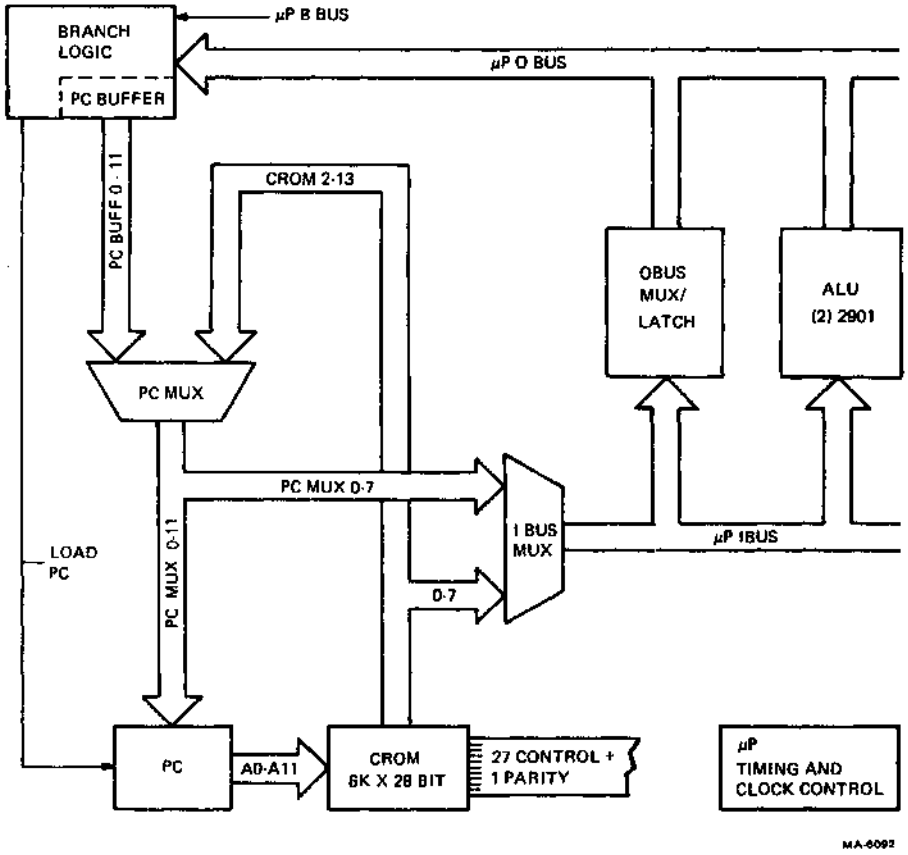


Figure 6-3 Microprocessor Block Diagram

The CROM contains 6144 28-bit words. Various parts of these control words are routed to the different sections of the tape subsystem. (Table 6-3 for destinations of the various CROM bits.) Each control word is an instruction which may do the following.

1. Route data from one place to another.

2. Change the sequence of CROM addressing either unconditionally or as the result of testing a condition (jumps).

3. Perform one of eight arithmetic or logic operations on data.

4. Set or reset control circuits.

(Instructions are discussed in more detail in Paragraph 6.3.2.3.)

The instructions in CROM are organized into program routines or subroutines. The instructions in the routines are normally accessed in sequential order until a jump instruction alters the program counter (PC). This enables looping within routines and changing from one routine to another.

Data transfers, both within the μP and between the μP and the rest of the subsystem, are over the μP IBUS and the μP OBUS. The OBUS carries data from the CROM (via the IBUS MUX and the OBUS MUX/LATCH) or the ALU to the branch logic (PC buffer register) or the rest of the subsystem. The IBUS carries data from CROM or a register outside the μP to the OBUS MUX/LATCH or the ALU. All data transfers over these buses are controlled by CROM and the timing logic.

The μP BBUS (microprocessor bit bus) allows specific bits in the tape subsystem to be tested (via conditional jump instructions). The CROM control lines will cause a specific signal to be sent to the branch logic over the BBUS where its condition is tested. If the signal matches the condition specified by the conditional jump, the PC will be loaded with a new value from either CROM (bits 13 through 2) or the PC buffer register.

The ALU (two 2901s) contains 16 8-bit words of RAM and circuitry to perform 8 arithmetic and logic operations on data from the IBUS, or the internal RAM. The results of the operations may be sent to the OBUS, a temporary register (Q), and/or to the internal RAM. All of these operations are controlled by the CROM control lines.

6.3.2 Microprocessor Functional Description

This section describes the 2901 and CROM operations.

6.3.2.1 2901 – The 2901 is a 4-bit microprocessor slice. 2901s may be linked together to allow data word lengths to be any multiple of 4-bits. Two 2901s are used in the TS11 to utilize 8-bit data words.

The remainder of this section refers to the two 2901 chips as a single unit, possessing 8-bit data paths and registers.

Figure 6-4 is a block diagram of the 2901 as used in the TS11. Refer to this figure for the remainder of this section.

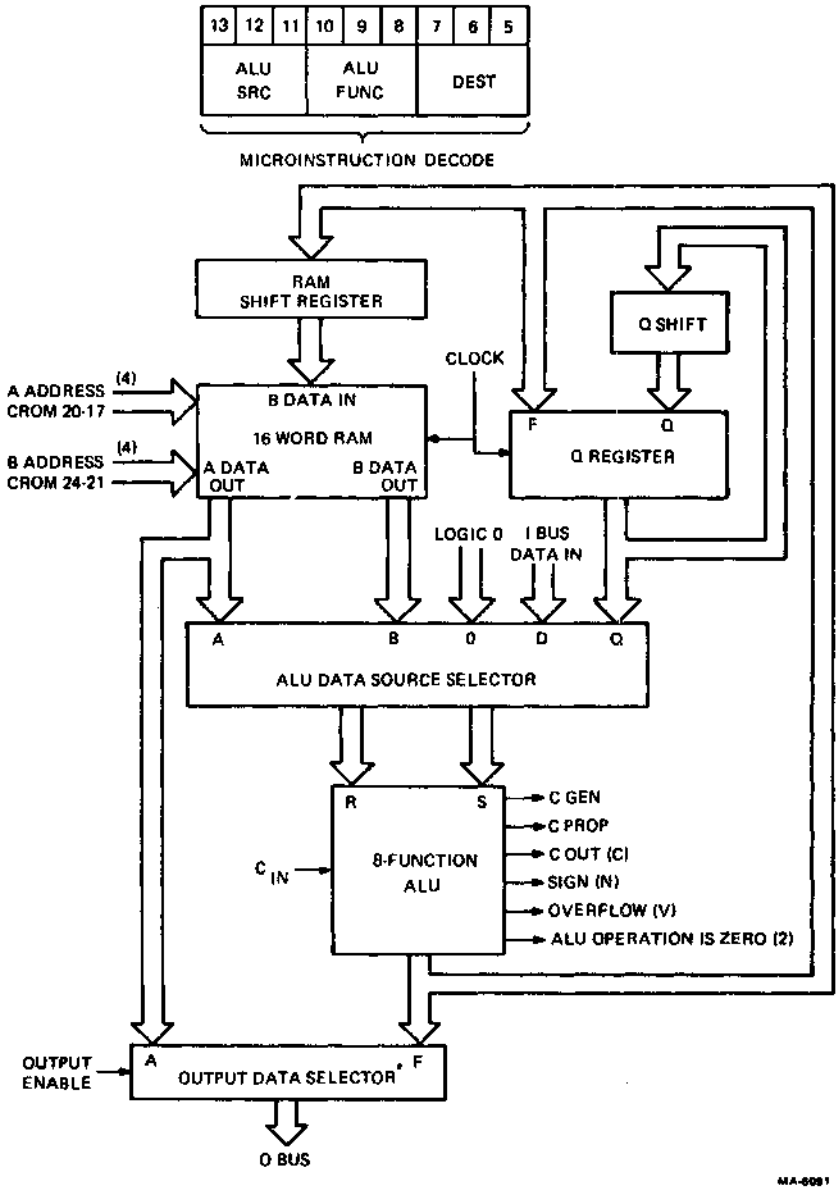


Figure 6-4 2901 Microprocessor Slice

The 2901 has a 16-word RAM with two output ports and a single input port. Two 4-bit fields from the CROM are used to address the RAM. The A address (CROM 20 through 17) is used to select data from the RAM to be output at port A. The B address (CROM 24 through 21) selects a location for output on port B and for storing data in the RAM.

The ALU data source selector selects two of five possible inputs to the eight function ALU. The selector is under the control of the SRC field of the CROM (CROM 13 through 11). Depending on the value in the SRC field, two of the following data sources will be input to the ALU.

1. RAM port A
2. RAM port B
3. Logic 0
4. IBUS data in
5. Q register

See Table 6-9 for the inputs selected by the various values of SRC.

The eight function ALU is under the control of the FUNC (function) field (CROM 10 through 8). It receives its inputs from the source selector and the CARRY IN bit (Cin = CROM 4). The ALU performs one of eight arithmetic or logic operations (Table 6-9) under the control of the FUNC field. The output from the ALU is sent to the output data selector, Q register, and RAM shifter. There are also status signals generated by the ALU. These are carry out (C), sign (N), overflow (V), and zero (Z). Only Z and C are used by the TS11. (An N signal is derived from μP OBUS bit 7 by logic external to the 2901s.)

The RAM shifter and data input, the Q shifter and Q register input, and the output data selector are all under control of the DEST field (CROM 7 through 5). The OBUS output is also controlled by the Output Enable signal. (See Table 6-9 for the destinations of data within the 2901.)

The RAM shifter allows the results of the operation to be shifted left or right before being stored in the location designated by the B address field. The shifter will either shift data one place (left or right) or pass the data unchanged to the RAM input.

The Q register is used as a temporary storage register. Its inputs are the output of the ALU or the Q shifter. The shifter allows data from the Q register to be shifted one place (for each instruction) right or left and then placed back into the Q register.

The output data selector puts data from either the ALU or RAM port A on the output. The Output Enable signal will either allow the data to pass onto the OBUS or hold the output in the high impedance state. (OBUS outputs are tristate.)

The clock input controls the RAM, RAM output ports, and the Q register. When the clock input is high, the RAM output ports are open and pass the data from the RAM locations addressed by the A and B address fields. When the clock input is low, the ports latch and hold the last data present while the clock was high. If the DEST field from CROM calls for data to be written into the RAM, the data will be written while the CLOCK is low. Data will be written into the Q register (if the DEST field allows it) on the low to high transition of the CLOCK. (More information is given on timing in Paragraph 6.3.2.4.)

6.3.2.2 CROM Organization – The μP CROM, CROM addressing (including branch logic), and CROM parity checking logic, are contained on two circuit boards, M8964 and M8968.

M8964 holds the PC, branch logic, CROM parity checking logic, and the first 2K of CROM (addresses 0000 through 3777). M8968 holds the extended addressing logic and the upper 4K of CROM.

Table 6-9 Microprocessor Function Summary

	27	26	25	24 23 22 21	20 19 18 17	16	15	14	13 12 11	10 9 8	7 6 5	4	3	2	1	0
INT-INT ARITH AND MOVE	P	0	0	RAM B ADDR	RAM A ADDR	0	0	0	SRC 0,1,2,3,OR 4(8)	FUNC	DEST	*	0	0	0	0
EXT-INT ARITH AND MOVE	P	0	0	RAM B ADDR	SRC REG	PB	0	0	SRC 6 7 (8)	FUNC	DEST	*	0	0	0	SEX
INT-EXT ARITH AND MOVE	P	0	1	DEST REG	RAM A ADDR	0	0	0	SRC 0 2 OR 4 (8)	FUNC	DEST 0 OR 1 (8)	*	0	0	DEX	0
JUMP	P	1	0	MASK	SRC REG	PB	0	1	NEW PC						JCT	SEX
LDB	P	1	0	RAM B ADDR	0 0 0 0	0	1	0	SRC 6 OR 7 (8)	FUNC	VALUE					
LDQ	P	1	0		0 0 0 0	0	1	1	SRC 6 OR 7 (8)	FUNC	VALUE					
LDX	P	1	1	DEST REG	0 0 0 1	0	0	1		VALUE					DEX	SEX
EXT-EXT MOVE	P	1	1	DEST REG	SRC REG	1	0	1							DEX	SEX

*=C_{IN}

NOTES:

1. C ROM BIT 16 IS SET WHEN THE PC BUFFER IS USED AS A SOURCE REGISTER OR AS THE SOURCE OF THE ADDRESS DURING JUMPS.
2. C ROM BITS 1 AND 0 ARE USED AS DESTINATION AND SOURCE ADDRESS EXTENSION BITS WHEN ABBREVIATED DEX AND SEX.
3. C ROM BIT 1 CONTROLS WHETHER A CONDITIONAL JUMP WILL OCCUR ON CONDITION = TRUE (BIT 1 SET) OR CONDITION = FALSE (BIT 1 = 0)
4. BLANK FIELDS ARE "DON'T CARE".

SRC (8)	R	S
0	RAM A	Q REG
1	RAM A	RAM B
2	0	Q REG
3	0	RAM B
4	0	RAM A
5	I BUS	RAM A
6	I BUS	Q REG
7	I BUS	0

FUNC (8)	
0	R+S
1	S-R
2	R-S
3	R OR S
4	R AND S
5	R AND S
6	R EX OR S
7	REX NOR S

* NOT USED IN TS11 MICROCODE

DEST (8)	RAM B GETS	Q REG GETS	O BUS GETS *
0	NONE	FUNC	FUNC
1	NONE	NONE	FUNC
2	FUNC	NONE	RAM A
3	FUNC	NONE	FUNC
4	$\frac{FUNC}{2}$	$\frac{Q\ REG}{2}$	FUNC
5	$\frac{FUNC}{2}$	NONE	FUNC
6	2X FUNC	2X Q REG	FUNC
7	2x FUNC	NONE	FUNC

* WHEN C ROM BITS 25 AND 26 ARE SET, THE OBUS OUTPUT FROM THE 2901 IS INHIBITED.

MA-6079

6.3.2.2.1 CROM Bit Fields – The CROM control words are divided into fields which control various parts of the μP and the subsystem data paths. Tables 6-9 and 6-10 show how these fields are broken down within the control word and the permissible values for different instructions.

Table 6-10 CROM Bit Definition

Bit	Description	
27	Parity bit	
26	Op code field:	3 = EXT-EXT MOVE or LDX
	2 = JMP,LDB,LDQ	1 = INT-EXT ARITH or MOVE
25	0 = INT-INT ARITH, EXT-INT ARITH or MOVE	
24	RAM B address select, mask select on jumps,	
23	Destination register select (with CROM 01) for ops	
22	sending data to registers outside the 2901s	
21		
20	RAM A address select or source register select	
19	(with CROM 00) for ops requiring data from	
18	registers outside 2901s	
17		
16	PC MUX CONTROL 1 = PC BUFF 0 = CROM 02 to 13	
15	Set only on LDB, LDQ	
14	Set on all JMPS, LDX, LDQ, EXT-EXT MOVES	
13	SRC controller for 2901s;	13 to 02 = New PC on JMPS
12		
11		
10	Function code for 2901s;	09 to 02 = Value on LDX
09		
08		
07	Destination code for 2901s;	07 to 00 = Value on LDB,LDQ
06		
05		
04	C(N) bit on ARITH ops	
03	Part of new PC or value on JMPS or LD ops	
02		
01	Destination EX/JCT, 1 = JMP if true, 0 = JMP if false	
00	SRC EX	LSB of value on LDB,LDQ

EXT = External
EX = Extension

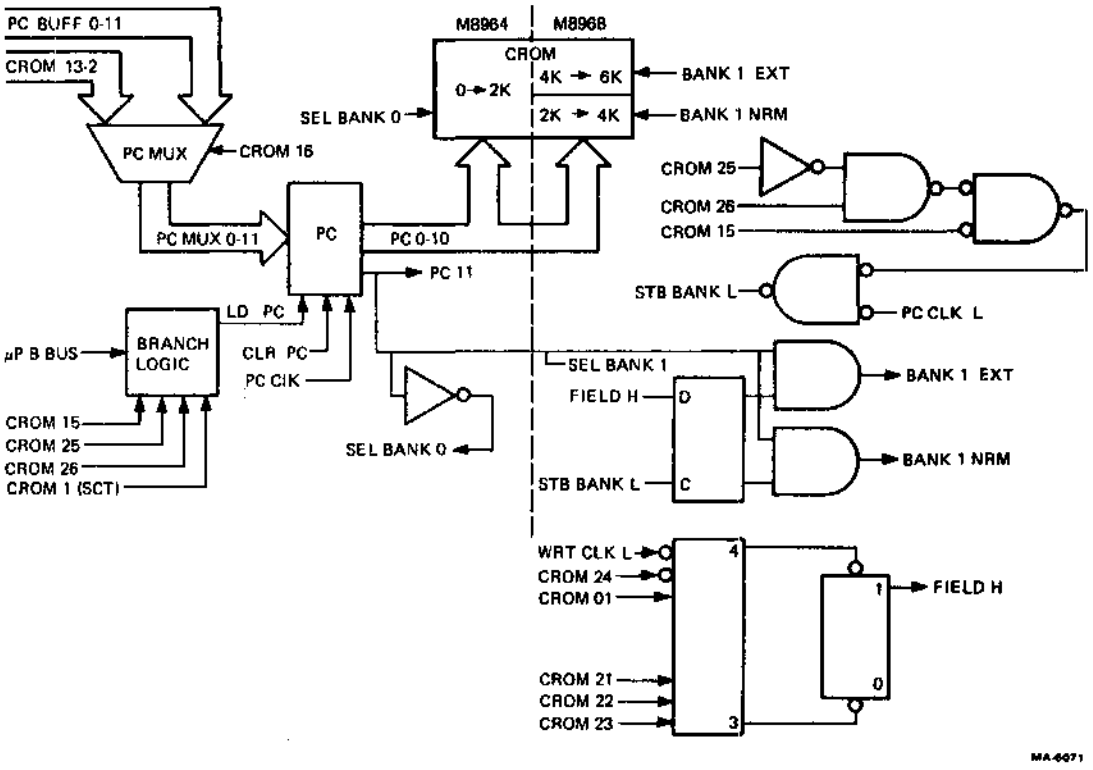


Figure 6-5 CROM Addressing

6.3.2.2.2 CROM Addressing (Figure 6-5) – The PC increments with each low-to-high transition of PC CLK. This causes the CROM locations to be accessed sequentially in ascending order. Jump instructions can cause the PC to be loaded with a new value from either the PC Buffer register or from CROM 13 through 2 of the jump instruction. This causes the PC to start incrementing from the new value. Thus, control of the μP can pass from one area of CROM to another.

The PC contains 12 bits, which allow direct addressing of 4K of CROM. Since the TS11 uses 6K of CROM, a bank selection scheme was adopted.

Bank 0 = 0 through 2K
Bank 1 NRM = 2K through 4K
Bank 1 EXT = 4K through 6K

PC bits 0 through 10 are applied to every ROM. PC bit 11 is used, along with a field bit, in the bank selection scheme. The field bit is not part of the PC. It must be set or reset under program control. Also, the field bit will not take effect until a jump instruction is decoded.

The field bit is set by a register write to address 24 and reset by a write to address 23. The 1 output of the field flip-flop is applied to a second D type flip-flop (EXT MEM). The EXT MEM flip-flop will not change states until the trailing edge of the STB BANK L signal. STB BANK L is generated by a jump instruction (CROM 26 = 1 and CROM 15 and 25 both = 0) anded with PC CLK L. The output from the EXT MEM flip-flop is applied to two AND gates along with PC bit 11. These two AND gates select one or the other of the two high banks of CROM.

When PC bit 11 is 0 (addresses 0000 through 3777), SEL BANK 0 will select the first 2K of CROM. This is true no matter what the state of the field bit and EXT MEM flip-flop. When PC bit 11 is 1, the EXT MEM flip-flop determines which of the upper banks will respond to addresses 4000 through 7777. If EXT MEM is set, addresses 4000 through 7777 address the 4K through 6K bank. If EXT MEM is reset, addresses 4000 through 7777 address the 2K through 4K bank.

PC bits 0 through 10, SEL BANK 0, and EXT MEM are sent to the maintenance panel and can be observed via LEDs.

6.3.2.2.3 Branch Logic – The branch logic tests the μP BBUS on jump instructions and, if the conditions of the jump instruction are satisfied, generates the signal LD PC (load program counter). The PC is loaded with the output of the PC multiplexer.

The PC multiplexer is controlled by CROM bit 16. When bit 16 is a one, the output of the PC multiplexer is the contents of the PC Buffer register. When bit 16 is 0, the output of the PC multiplexer is the data from CROM bits 13 through 2 of the current instruction.

CROM bit 1 (JCT bit = Jump Condition True) controls the condition on which the jump occurs. If CROM 1 is set, the jump will occur if the BBUS is high. If CROM 1 is not set (0), the jump will occur if the BBUS is low.

Paragraph 6.7 gives a complete description of the BBUS logic.

6.3.2.2.4 CROM Parity Checking – All of the CROM bits are sent to a parity checking network on M8964. This network checks the 28 CROM bits for overall odd parity. If the parity is not odd, μP CROM PAR ERR is sent to the clock logic on M8962 where it stops the timing signals. Microprocessor CROM PAR ERR is also sent to the maintenance panel and displayed via a LED.

6.3.2.3 Basic Instructions – The microprocessor has seven basic instruction types.

1. INT-INT ARITH or MOVE
2. EXT-INT ARITH or MOVE
3. INT-EXT ARITH or MOVE
4. JUMPs
5. LDB/LDQ
6. LDX
7. EXT-EXT MOVE

Figure 6-6 and Tables 6-9, 6-10, and 6-11 should be used for reference while reading the descriptions of the instruction types.

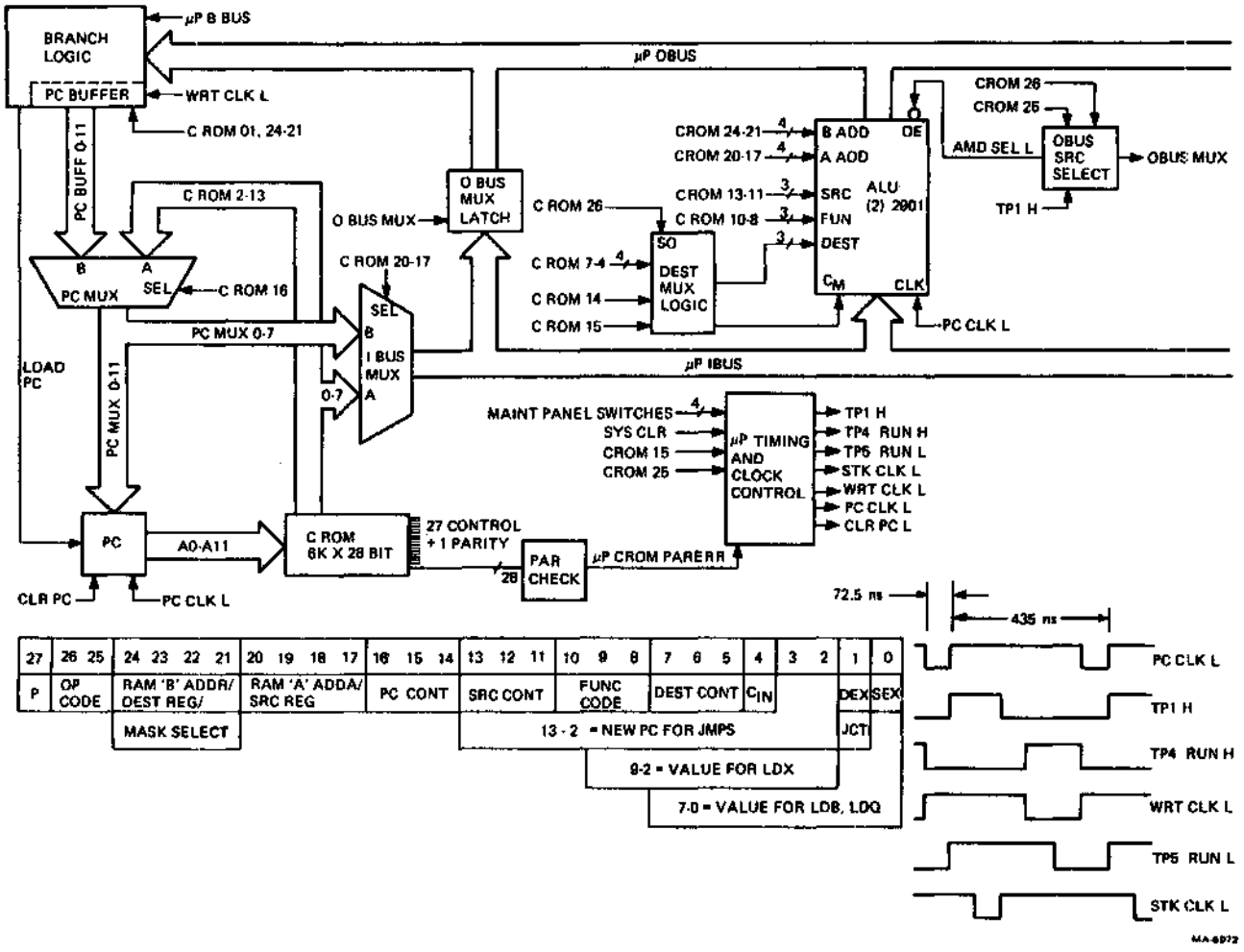


Figure 6-6 Basic Instruction Flow

Table 6-11 Destination Registers and Addresses

I*	O†	Register or Signal Addressed	Print Set Page Register	Address Logic	Remark
22	30	U STACK ADDRESS REG	M8963-1	M8963-2	MUX M8963-2
–	32	PUSH/STACK WRITE	–	M8963-2	–
23	–	POP/STACK READ	–	M8963-1	–
–	33	FORCE STACK PAR ERR	–	M8963-2	–
–	31	RESET AC-LO IN ATTN REG	–	M8963-2	Control bit
03	–	U ATTEN REG	M8963-2	M8963-2	DATA MUX
01	02	PC BUFF LO ORDER BITS	M8964-3	M8964-2	MUX M8964-2
–	22	PC BUFF HI ORDER BITS	M8964-3	M8964-3	Write only
–	36	ATTEN ENAB + CAP MUX SEL	M8963-3	M8963-2	–
02	–	CAPSTAN DATA INPUT	M8963-2	M8963-2	MUX and ADD
–	37	CAPSTAN BD DATA OUTPUT	M8963-3	M8963-2	–
–	11	I/O SEQUENCER CONTROL	M8967-2	M8967-1	–
–	10	I/O SEQUENCER DATA OUT	M8967-2	M8967-1	–
–	15	I/O SILO DATA BUFFER OUT	M8966-1	M8966-2	–
14		I/O SILO CTL BUFFER OUT	M8966-1	M8966-2	–
17	–	I/O SEQUENCER DATA IN	M8967-2	M8967-1	–

* Micro input address from CROM (0,20) (19,18,17) octal
† Micro output address from CROM (1,24) (23,22,21) octal

Table 6-11 Destination Registers and Addresses (Cont)

I*	O†	Register or Signal Addressed	Print Set Page Register	Address Logic	Remark
–	16	I/O SILO CLOCK	–	M8966-2	Clocks silo.
–	13	I/O RESTART AT LOC 0	M8967-1	–	Restart I/O μP.
–	12	RESET I/O RDY BIT	–	M8967-1	–
–	17	WRITE I/O FRAME COUNT	M8966-2	M8966-2	Low byte
05	–	FORMATTER OUTPUT READY	M8922-2	M8922-3	From 3 M8924 boards
25	–	ONES OR DEAD TRACK	M8922-2	M8922-3	
06	–	TRACK ACTIVE UNDESKEWED	M8922-2	M8922-3	
26	–	FORMATTER DATA (DESKEWED)	M8922-2	M8922-3	
07	–	DEAD TRACK (DESKEWED)	M8922-2	M8922-3	
27	–	ZEROS OR DEAD TRACK	M8922-2	M8922-3	
–	04	MAJOR STATE CONTROL	M8922-3	M8922-3	–
–	05	CLOCK DESKEW BUFFER	–	M8922-3	Clocks silo.
–	20	READ CONTROL REGISTER	M8923-1	M8923-1	–
–	01	WRITE CONTROL REGISTER	M8929-1	M8929-2	–
–	23	CLEAR FIELD BIT	M8968-2	M8968-2	External address
–	24	SET FIELD BIT	M8968-2	M8968-2	External address

* Micro input address from CROM (0,20) (19,18,17) octal

† Micro output address from CROM (1,24) (23,22,21) octal

6.3.2.3.1 INT–INT ARITH or MOVE – Internal-to-internal arithmetic or move instructions manipulate data internal to the 2901.

All function (FUNC) and destination (DEST) configurations are legal. The source (SRC) must be 0 through 4 since only data internal to the 2901s is used. The OBUS output is not used because CROM bit 25 must be a 1 and CROM bit 15 must be a 0 to allow write clocks.

6.3.2.3.2 EXT–INT ARITH or MOVE – External-to-internal arithmetic or move instructions move or perform operations on data external to the 2901s and store the results internally (results remain within the 2901s).

The external data is placed on the μP IBUS by the SRC REG field (CROM 0 and 20 through 17) and is selected by a SRC field (CROM 13 through 11) value of 6 or 7. All FUNC and DEST values are legal, but the OBUS outputs from the 2901 are not used. Refer to Table 6-11 for the registers/multiplexers selected by different values of the SRC REG field.

6.3.2.3.3 INT–EXT ARITH or MOVE – The internal-to-external arithmetic or move instructions perform operations on data internal to the 2901s and write the results in an external register.

The operation is performed within the 2901s and the result is placed on the OBUS. The DEST REG field (CROM bits 1 and 24 through 21) selects the register to be written and write clock (WRT CLK L) strobes the data into the register. All FUNC values are legal. The SRC field may be 0, 2, or 4 and the DEST field may be 0 or 1. Refer to Table 6-11 for the DEST REGs and their addresses.

6.3.2.3.4 JUMP – The jump instructions test the state of the μP BBUS and can replace the current contents of the PC with a new value or leave the PC unchanged, depending on the results of the test. The new value can come from either the jump instruction itself (CROM bits 13 through 2) or the PC buffer register. (The PC buffer must be loaded with the desired value prior to the jump instruction.)

CROM bits 24 through 17 and 0 of the jump instruction cause the signal to be tested to be placed onto the BBUS. CROM bit 1 determines if the jump will occur with the BBUS a high or a low. If the condition is satisfied, the PC is loaded with a new value. If the condition is not satisfied, the PC remains unaltered. Refer to Paragraphs 6.7 and 6.3.2.2.2 for a complete description of the μP BBUS and the branch logic.

CROM bit 26, when set, causes the output of the DEST MUX LOGIC to be controlled by CROM bits 14 and 15. In the jump instructions the Cin bit is forced low and the DEST input to the 2901 is forced to a 1. This causes an effective NO OP within the 2901 and, since bit 25 is not set, the OBUS output goes nowhere.

6.3.2.3.5 LDB/LDQ – The LDB and LDQ instructions place the value contained in CROM bits 7 through 0 in either the RAM location (LDB) or the Q register (LDQ).

The op code of these instructions is the same as the jump instruction. Note that these are the only two instructions in which CROM bit 15 is set. CROM bit 15 is used along with 25 and 26 in decoding the jump instruction. When bit 15 is set, a LDB/LDQ is decoded instead.

In both of these instructions the SRC REG field must be 0. This selects CROM 7 through 0 as the source of data on the IBUS.

In LDB the DEST input to the 2901 is forced to a 2. In LDQ the DEST input of the 2901 is forced to a 0. The OBUS outputs of the 2901 in both instructions are ignored because CROM bit 25 is reset, inhibiting write clocks.

6.3.2.3.6 LDX – The LDX instruction places a value from CROM 9 through 2 into a register on the OBUS. The 2901 is not used during the instruction.

CROM bits 25 and 26 are both set for the LDX instruction. This causes the signal AMD SEL L to go high, disabling the OBUS outputs of the 2901s. Bits 25 and 26 both set also cause the OBUS MUX/LATCH to pass data from the IBUS onto the OBUS.

The DEST inputs to the 2901 are forced to a value of 1. Since the OBUS outputs are disabled, the 2901 will do a NO OP (that is, take nothing and put it nowhere).

The SRC REG field must be a 1 and CROM bit 16 must be 0. This selects CROM 13 through 2 as the source for the PC MUX, and PC MUX outputs 0 through 7 as the source for the IBUS. Since bit 25 is set and bit 15 is 0, the data from the IBUS is passed through the OBUS MUX/LATCH onto the OBUS and written into the register specified by the DEST REG field with a write clock.

6.3.2.3.7 EXT–EXT MOVE – The external-to-external move instruction takes data from a register multiplexer on the IBUS and writes it into a register on the OBUS.

The 2901s are disabled as in the LDX instruction (Paragraph 6.3.2.3.6).

The SRC REG field selects the register which contains the desired data. The data is placed onto the IBUS, passed through the OBUS MUX/LATCH onto the OBUS, and written into the register selected by the DEST REG field.

6.3.2.4 Clock Generation and Control (Figure 6-7) – The clock generation and control logic are responsible for generating and controlling the timing signals used throughout the subsystem. Figure 6-7 is a simplified logic diagram of the circuits used to control and generate these timing signals.

The crystal oscillator (top left of Figure 6-7) operates at 13.8 MHz. Its output leaves M8962, is routed through the backplane, and reenters M8962 as MAIN CLK H. (MAIN CLK H also goes to the I/O section.)

MAIN CLK H is connected as the clock input to a shift register which is used as a divide by six circuits. Each output of the shift register is at 1/6 the frequency of MAIN CLK H (that is, 2.3 MHz). (Refer to Figure 6-8 for the timing relationships of these signals. Note that TP 1 and TP 2 correspond to TP 7 and TP 8, respectively.)

The signals from the shift register are sent to a set of six AND/NAND gates (top right of Figure 6-7) where they are combined with STOP II L, CROM control signals, and each other. The outputs of these gates control the timing of the μP and its buses.

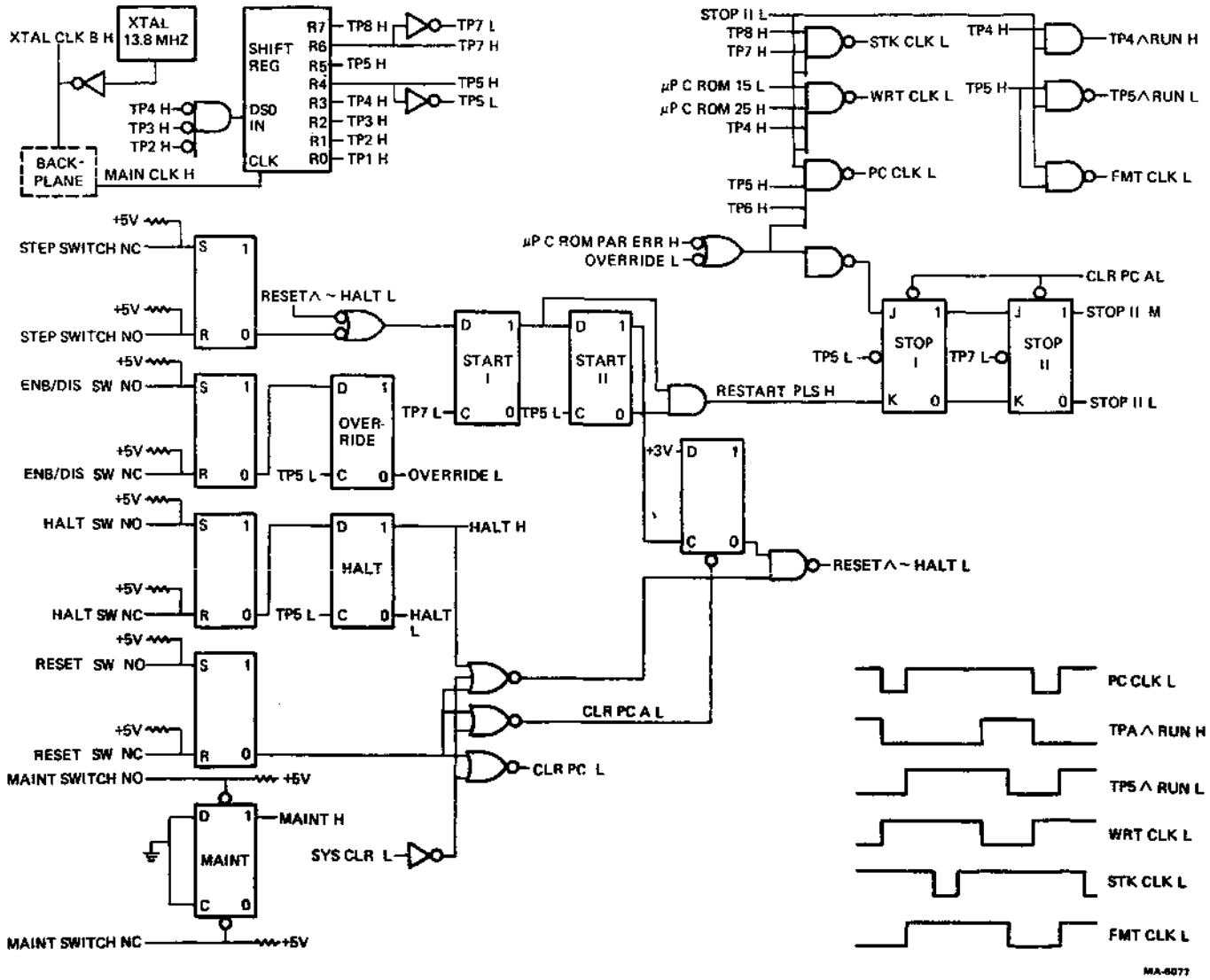


Figure 6-7 Clock Generator and Control Logic

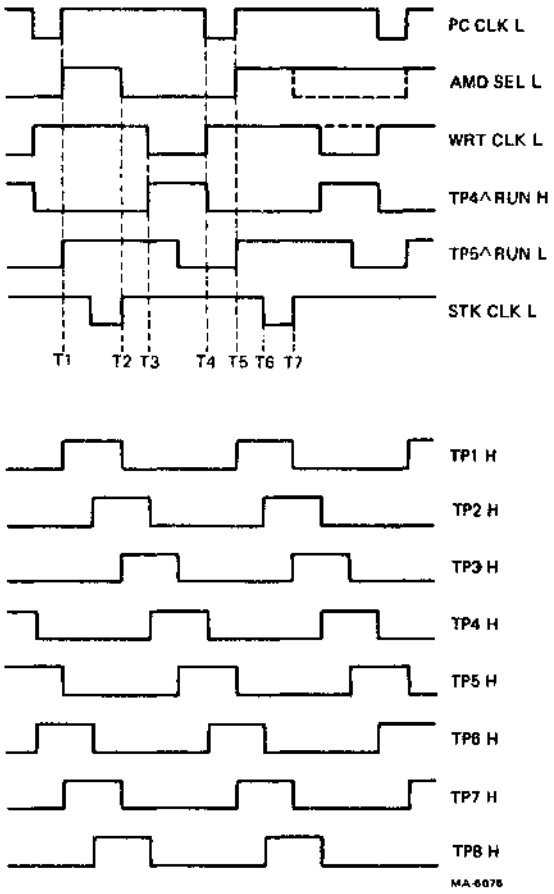


Figure 6-8 Timing Signals

6.3.2.4.1 Instruction Timing – The signals which control μP instruction timing are shown at the top of Figure 6-8.

The instruction cycle starts with the low-to-high transition of PC CLK L at T1. At this point the PC is incremented (or possibly loaded with a new value if a jump instruction was just done). AMD SEL L also goes high at this time, disabling the outputs of the 2901s. This allows time (about 145 ns) for the PC to increment and the CROM outputs to become stable before placing data on the OBUS.

NOTE
If CROM bits 25 and 26 both are 1s then AMD SEL L will stay high for the complete instruction cycle. The source of data for the OBUS would be the IBUS via the OBUS MUX/LATCH.

At T2, the OBUS outputs of the 2901s are enabled and data is placed on the OBUS. If the instruction calls for data to be written into a register on the OBUS, the data will be written at T3. If the instruction did not call for data to be written (that is, CROM bit 25=0 or CROM bit 15=1), the write clock (WRT CLK L) will not occur.

At T4, data is written into the 2901s RAM (if the DEST field called for data into the RAM).

At T5, the 2901s will write data into the Q register (if called for), and the PC will increment to start a new instruction. If the current instruction is a jump and the condition is satisfied, the PC will be loaded at T5 instead of incremented.

T6 and T7 deal with stack operations and are discussed in Paragraph 6.3.2.5.

6.3.2.4.2 Halt and Single Step – During normal operations (μP is running without error), STOP II L is a high. Any condition which sets the stop II flip-flop causes the major timing signals to be disabled and stops the μP.

The halt switch on the maintenance panel will cause the stop II flip-flop to set and stop the μP. Activating the halt switch sets the S/R flip-flop on the input to the halt flip-flop. On the trailing edge of TP5 L the halt flip-flop sets. HALT L goes low causing the output of the NAND gate feeding the J input of the stop I flip-flop to go high. The leading edge of the next TP5 L sets STOP I. TP7 L causes STOP II to set, disabling the timing signals.

Microprocessor CROM PAR ERR H has the same effect as the halt switch but disables PC CLK L immediately. Microprocessor CROM PAR ERR H can be overridden in the clock control logic by the ENB/DIS switch on the maintenance panel. Activating the ENB/DIS switch sets the override flip-flop on the next low-to-high transition of TP5 L. The signal OVERRIDE L is applied to the NOR gate with μP CROM PAR ERR H and causes its output to go high.

The step switch on the maintenance panel allows single-step operation of the μP and is a means of restarting the μP after it has been halted.

Assume that the μP has been halted via the HALT switch. Both STOP I and STOP II are set. The J input to STOP I is high. Activating the STEP switch on the maintenance panel causes a low on the lower input to the OR gate feeding the start I flip-flop. The output of the OR gate goes high and START I sets on the trailing edge of TP7 L. START II is not yet set so both inputs to the AND gate feeding the K input of STOP I are high.

At this point STOP I and STOP II are both set, START I is set and START II is reset, and both J and K inputs of STOP I are high. STOP I will toggle on the leading edge of TP5 L. START II sets on the trailing edge of TP5 L causing the high on the K input of STOP I to go low. STOP II resets on the leading edge of TP7 L.

The timing signals are now enabled and the μP starts the instruction cycle. On the next TP5 L STOP I is set and on TP7 L STOP II is set, disabling the timing signals once again. Thus each time the STEP switch is activated, one cycle of each of the timing signals occur and the μP does one instruction. The start II flip-flop makes sure that only one RESTART PLS H signal occurs each time the step switch is activated.

If the HALT switch is deactivated and the STEP switch is activated, the same events take place except that the stop I flip-flop does not set at TP5 L because the J input is now low. This allows the STEP switch to restart the μP after the HALT switch has been deactivated.

6.3.2.4.3 System Clear and Reset – The RESET switch on the maintenance panel and the SYS CLR L signal both have the same effect on the μP. They both cause the PC to clear and the μP to start running the microcode starting at location 0000. (SYS CLR L is generated by either UNIBUS INIT or by a write over the Unibus to the TSSR register address).

SYS CLR L and the output of the flip-flop reset by the RESET switch are applied to three NOR gates (bottom center of Figure 6-7). The output of all three NOR gates go low. CLR PC L clears the PC. CLR PC A L directly sets the stop I and stop II flip-flops and directly resets the D type flip-flop feeding the RESET AND NOT HALT NAND gate. This enables the top input to the NAND gate. The bottom input of the NAND gate is held low while the RESET or SYS CLR L signals are active. When these signals go low (and the HALT switch is not set), the bottom input goes high and causes RESET AND NOT HALT L to go low.

RESET AND NOT HALT L is applied to the NOR gate feeding the start I flip-flop. START I sets on the trailing edge of the next TP7 L, generating RESTART PLS H. On the leading edge of TP5 L STOP I resets and on the trailing edge of TP5 L START II sets. The 1 output of start II sets the D type flip-flop feeding the RESET and not HALT gate causing RESET AND NOT HALT L to go high. The 0 output of the start II flip-flop causes RESTART PLS H to go low. On the leading edge of TP7 L the stop II flip-flop resets, enabling the μP timing signals.

6.3.2.5 Stack Operation – The stack on M8963 is an auxilliary storage area for the μP. It contains 64 8-bit words (plus one parity bit) and may be accessed as either a LIFO (last in first out) stack or as an area of auxiliary RAM.

The following description of stack operation refers to Figure 6-9.

The write data path to the stack is the μP OBUS to the COM OBUS to the 64 × 9-bit RAM or the stack counter. The read data path is from the 64 × 9-bit RAM to the μP IBUS multiplexer. (The stack address can also be read by reading register address 22. This logic is not shown on Figure 6-9.)

When the stack is used as a randomly addressed memory, two operations are required to write or read data. First, the stack counter must be loaded (μP writes DEST REG 30) with the address of the data to be read or the address minus one of the location to be written. Then a push (μP write to DEST REG 32) or a pop (μP read SRC REG address 23) instruction must be done to write or read the data.

To load the stack counter, the μP places the data on the OBUS and TP4 and RUN H strobes it into the COM OBUS LATCH. The DEST REG field from CROM causes the decoder to assert LD STACK ADDRS L at WRT CLK L time which loads the stack counter. LD STACK ADDRS L also resets the push and pop flip-flops and the FORCE STK PAR ERR flip-flop.

The stack counter points to the top of the stack unless it has just been loaded with a new value. Thus, the top of the stack has its address selected and the data is on the STK DATA lines all the time.

In the pop operation, a 23 in the CROM SRC REG field causes SRC 03 L to go low. Microprocessor CROM 00 L selects STK DATA as the source for the IBUS. The data is sent to the μP just as in any other register read operation. TP4 and RUN L, SRC 03 L, and μP CROM 00 L, and μP CROM 15 H set the pop flip-flop. This causes the stack counter to decrement so that it now points to the next lower location on the stack. At the trailing edge of TP5 and RUN L, the pop flip-flop is reset and the operation is complete.

The push operation is initiated by a write to a DEST REG field of 32. The decoder generates PUSH L when the DEST REG field is equal to 32 and a WRT CLK L is received. This sets the push flip-flop on the leading edge of WRT CLK L and increments the stack counter on the trailing edge. The data to be written is strobed into the LATCH by TP4 and RUN H where it is held until the next TP4 and RUN H.

The stack counter is now pointing to the next higher location (new top of the stack). When STK CLK L goes low, the signal WRT STACK L enables the contents of the latch to be written into the 64 × 9-bit RAM.

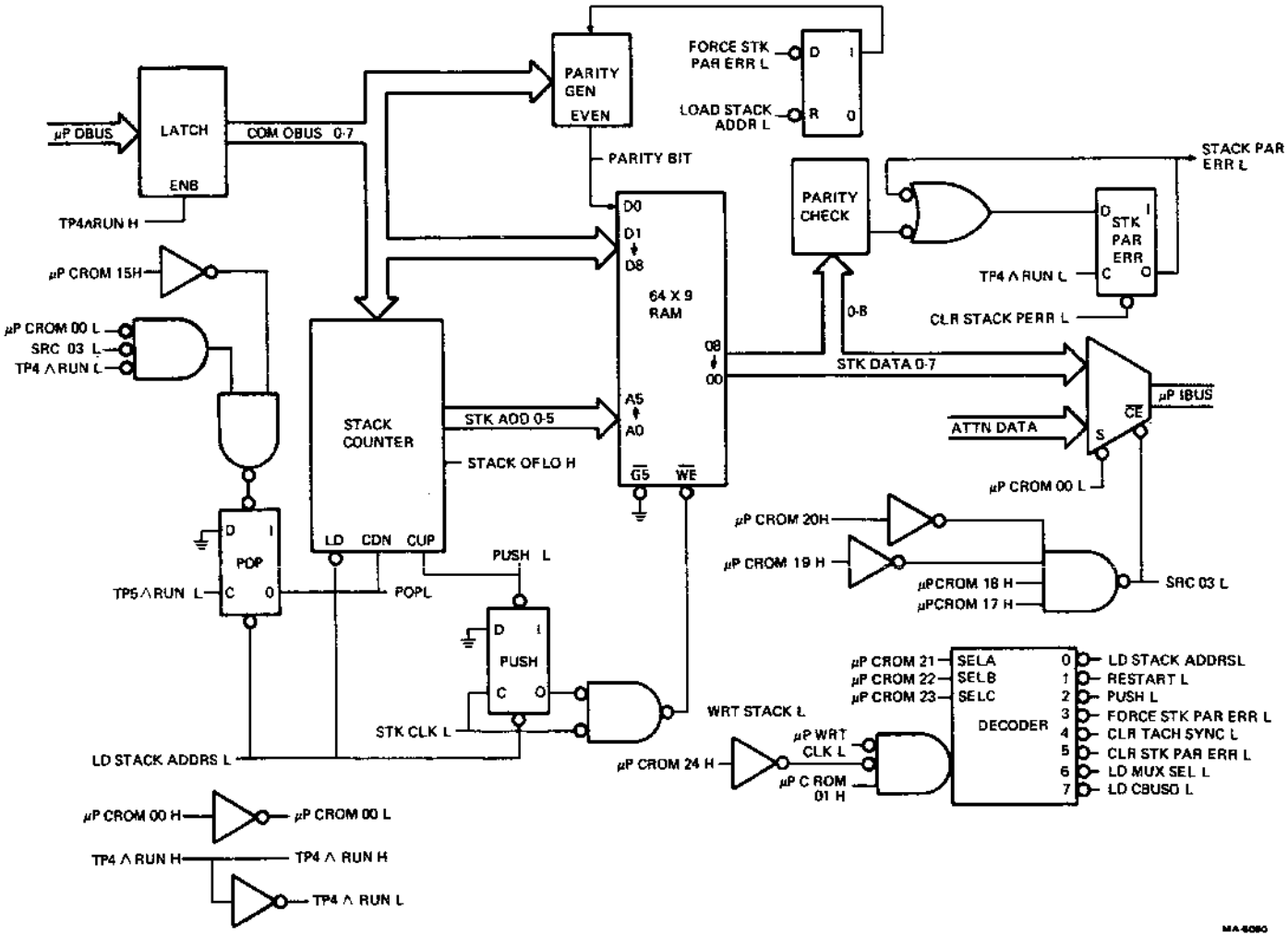


Figure 6-9 Stack Operation

STK CLK L occurs during the instruction cycle following the instruction containing a push. The STK CLK L signal is generated at T6 of Figure 6-8. This is the time in which the 2901s outputs are disabled. At T7, the STK CLK L signal goes high and resets the push flip-flop, terminating the push operation.

NOTE

The push operation will not be completed during single step mode. The enabling STOP II L signal will be low when TP7 and TP8 are both high, preventing STK CLK L from going low. A second single-step instruction cycle is needed to complete the push.

There are provisions for forcing stack parity errors. A register write to DEST REG 33 causes the decoder to generate FORCE STK PAR ERR L. This signal sets a flip-flop which is input to the parity generator and causes bad parity to be written until the flip-flop is reset.

A LD STACK ADDRS L signal is needed to reset the flip-flop and stop writing bad parity to the stack.

Parity is checked on all data read from the stack. If bad parity is detected, a flip-flop is set and STACK PAR ERR L is sent to the attention logic.

The parity error flip-flop is reset by doing a register write to a DEST REG address of 35.

6.4 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Packet processing is described in Chapter 5 of this manual and is not discussed in detail in this section. The descriptions in this section assume that packet protocol is being used.

The input and output functions of the TS11 tape subsystem are performed by four circuit modules.

1. M7982 Unibus to serial bus controller
2. M8965 I/O Section 1
3. M8966 I/O Section 2
4. M8967 I/O Section 3

The M7982 module plugs into a small peripheral controller (SPC) slot of the processor's Unibus. All Unibus signals connect to the M7982. The three I/O boards are plugged into the TS11 subsystem motherboard.

The M7982 connects to the motherboard via a six-line serial bus (Paragraph 6.2.2).

6.4.1 Serial Bus

The serial bus connects M7982 with the remainder of the TS11 subsystem. Data transfers across the serial bus may contain the following.

1. A 4-bit op code and parity bit
2. 16 data bits and 4 op code bits and a parity bit
3. 18 data bits and 4 op code bits and a parity bit (This occurs only when the subsystem transfers an 18-bit address to the M7982.)

Data is sent MSB first in the following order: data (if any), then op code, then parity. The parity bit will cause the total number of 1 bits transferred to be odd.

Five of the serial bus lines are used in moving data while one is used to initialize the subsystem.

NOTE
The following signal names are used on the M7982.

1. CLK – This signal is derived from the main microprocessor clock and is used for synchronizing all operations on the serial bus.

2. DAT FM DRV – This line carries serial data from the drive to M7982.

3. SHFT FM DRV – A control line used to let the M7982 know that data is coming from the drive. This line remains asserted while the drive is transferring data to the M7982.

4. DAT TO DRV – The line carrying serial data from the M7982 to the drive.

5. SHFT TO DRV – A control line used to let the drive know that data is coming from the M7982. The line remains asserted throughout the data transfer.

6. INIT – This line is used to initialize the subsystem. Generated by UNIBUS INIT or a write to the TSSR.

6.4.2 M7982 – Unibus to Serial Bus Controller

The M7982 module links the TS11 tape subsystem to the system Unibus. There may be up to four TS11 subsystems connected to the Unibus. Each subsystem requires its own M7982 and connecting serial bus cable. (Refer to Table 6-12.)

The programming and register description information for the TS11 subsystem is in Chapter 5 of this manual and is not repeated here.

As seen from the Unibus, the TSDB register is a write-only register while TSBA and TSSR are read-only registers. A DATO (write) operation to the TSSR address is decoded as a subsystem initialize. This restarts the main microprocessor in the drive and leaves the I/O section halted.

Table 6-12 Multidrive Address

TS11	Interrupt Vector	Unibus Address	Register
First	224	772520 772522	TSBA/TSDB TSSR
Second	XXX	772524 772526	TSBA/TSDB TSSR
Third	XXX	772530 772532	TSBA/TSDB TSSR
Fourth	XXX	772534 772536	TSBA/TSDB TSSR

XXX = floating vector address with the rank of 37.

6.4.2.1 M7982 Data Path (Figure 6-10) – The major data path of M7982 centers around the TSDB (C). All serial and parallel data entering M7982 passes through the TSDB.

The serial input data path is from the serial bus to the op code latch (C) to the TSDB. The serial output data path runs from the op code latch to the TSDB and then through the serial bus parity circuits (L) to the serial bus.

The parallel input data path runs from the Unibus transceivers (M) to the TSDB and the TSDB MUX (D). On word loads (DATO by the processor) bits 8 through 15 go directly to the TSDB and bits 0 through 7 pass through the TSDB MUX to the TSDB. Data bits 0 and 1 are duplicated in bits 16 and 17 respectively of the TSDB. Data bits 2 through 17 of the TSDB are then gated to the TSBA (H) with bits 0 and 1 of the TSBA forced to 0.

The internal parallel data path is from the TSDB to the TSBA and TSSR. DB0 through 17 go to the TSBA and DB0 through 6 and 10 go to the TSSR.

The parallel output data path centers around the DATA MUX. The DATA MUX can select any one of four sources to gate onto the Unibus via the Unibus transceivers. The selection of the source is under control of the Unibus transfer request logic (F).

1. TSDB bits 00 through 15

2. TSBA bits 00 through 15

3. TSSR – TSSR has 8 bits which may be loaded from the TSDB; 00 through 06 and 10, A16, and A17 from the TSBA, with the remainder made up of status and error bits.

4. The vector address switches (N)

When the processor does DATOB operations the M7982 decodes them as maintenance functions. A DATOB to the TSDB high byte causes the TSDB Mux to load Unibus data bits 8 through 15 into TSDB bits 0 through 7. Bits 8 through 15 also go directly into TSDB bits 8 through 15. The TSDB then has the same data in both the high and low byte. The TSDB is then loaded into the TSBA and a maintenance op code is serially shifted to the drive over the serial bus. The contents of the TSBA can then be examined by reading the base address. This function tests the TSBA.

A DATOB to the TSDB low byte places Unibus data bits 0 through 15 in TSDB 0 through 15 and then into the TSBA. The TSDB is then serially shifted to the drive with a maintenance op code. The drive will return the same 16 data bits over the serial bus with an op code to load the TSSR (D) and TSBA with the data. This function tests the serial bus and the TSSR.

After either maintenance function the drive will stop updating the TSSR. A DATO to the TSSR (subsystem initialize) must be done by the processor after either maintenance function to set the SSR bit (TSSR bit 07).

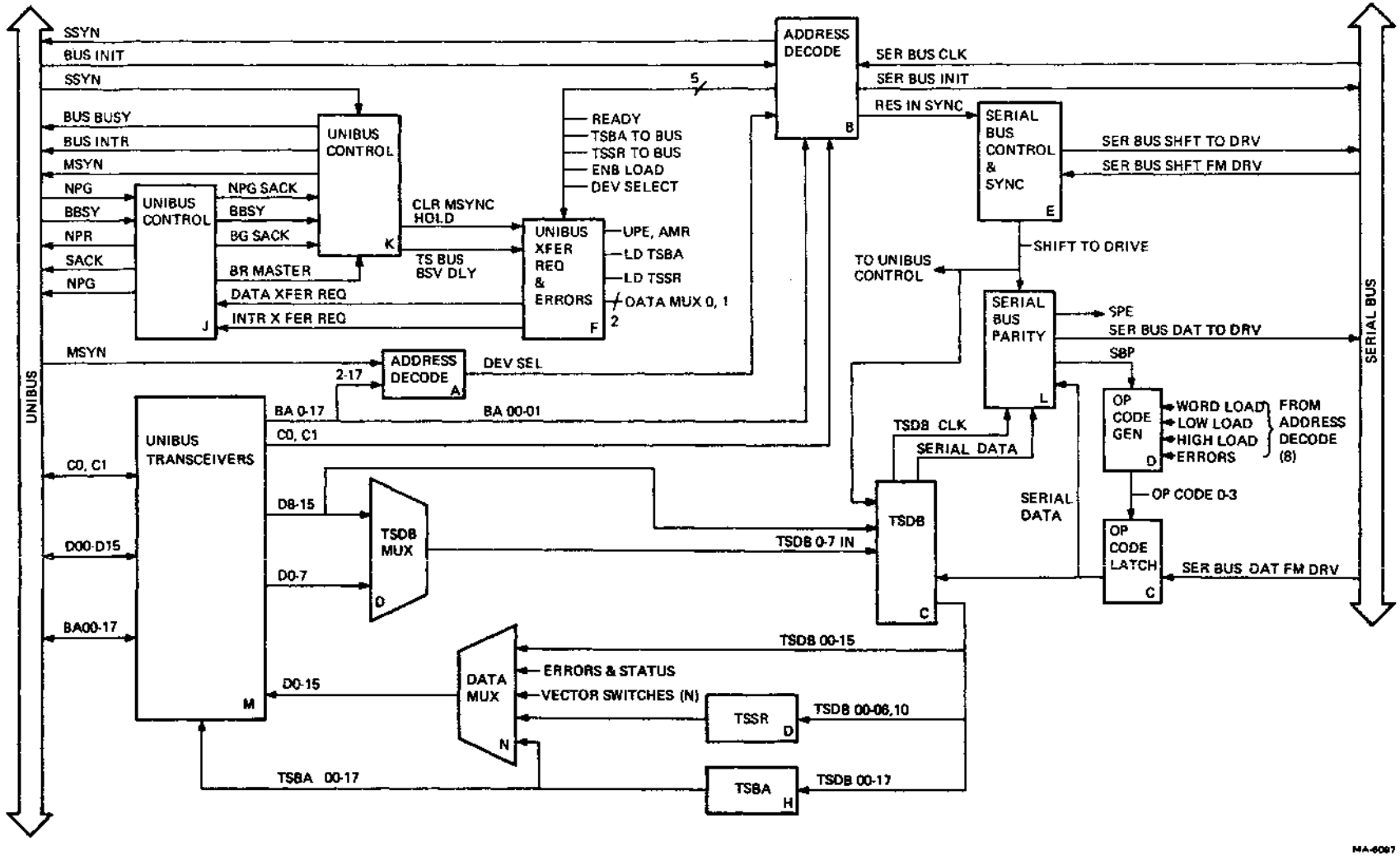


Figure 6-10 M7982 Data Path

6.4.2.2 M7982 Operation – The processor will assert the address and data along with MSYNC on the Unibus. The address will be decoded by the address decode circuits (A and B) which will generate the needed timing signals internal to the M7982. D0 through 15 will be gated from the Unibus transceivers (M) to the TSDB and the TSDB MUX (D). Bits 8 through 15 go directly to TSDB while bits 0 through 7 pass through the TSDB MUX and then to the TSDB (C).

Data bits 0 and 1 are duplicated in TSDB 16 and 17 respectively. The data in TSDB 2 through 17 is then gated into TSBA (H) bits 2 through 17. Bits 0 and 1 are forced to 0. The Address decode circuits then gate out SSYN to the Unibus ending the Unibus portion of the transfer.

When the address decode circuits detected a DATO to the TSDB the WORD LOAD signal was sent to the op code generator circuit (D). WORD LOAD causes the op code generator to load a 15 into the 4-bit op code latch (C).

Once the data is in the TSBA, the serial bus control and sync logic (E) asserts SHIFT TO DRV and the 4-bit op code is serially shifted to the drive with the serial bus parity logic (L) forming correct parity. When the op code and parity bits have been transferred to the drive the operation is complete.

Note that the TSBA is immediately loaded from the TSDB when the TSDB is written (DATO) by the processor. Bits 2 through 17 form a module 4 address which will be used by the TS11 to access the command packet.

If the processor attempts to write the TSDB when the READY bit (TSSR bit 7) is not set, a Register Modification Refused (RMR) error will be generated. This will cause an op code of 16 to be sent to the drive on the next response by the M7982 to a drive command.

The DATI operations (read TSSR or TSBA) may be done by the processor at any time.

The address is decoded by the address decode circuits which generate gating signals to the DATA MUX (N). The Data Mux selects the TSSR (D) or TSBA bits 0 through 15 and passes the data to the Unibus transceivers and on out to the Unibus on D0 through 15. The ADDRESS DECODE circuits then assert SSYNC and the operation is done.

No communication takes place between the M7982 and the drive as the result of a DATI by the processor.

When the drive receives notification that a command pointer has been received (op code 15) it will usually send an op code to the M7982. This op code will usually cause the M7982 to issue an NPR to the Unibus. When NPG is received, the M7982 will assert SACK, BUS BUSY, and MSYNC while gating out the command pointer in TSBA on the Unibus address lines.

When SSYN is received, the data is gated from the Unibus transceivers to the TSDB. Bits 0 through 7 pass through the TSDB MUX and bits 8 through 15 are sent directly to the TSDB. The M7982 drops the bus control signals, asserts SHFT TO DRV, and increments the TSBA by 2. The data is shifted to the drive serially followed by an op code and parity bit.

Notice that the TSBA is now pointing to the next address in the command packet.

This process will repeat until the the entire command packet has been received. All command packets must contain four words even if all are not used.

The drive will do the command, write the message buffer and interrupt the processor.

To write the message buffer or a data buffer in CPU memory space the TS11 does NPR DATO transfers. The drive sends an 18-bit address to the M7982 with an op code which causes it to be loaded into the TSBA. The drive then sends data to the M7982 over the serial bus with an op code which causes the M7982 to do an NPR transfer to memory.

At this point the M7982 has the buffer address in the TSBA and the data to store in the TSDB. When M7982 receives NPG, the data is gated from the TSDB through the DATA MUX to the Unibus. The TSBA is gated to the Unibus address lines and the Unibus control logic (K) asserts MSYNC.

When SSYNC is received the M7982 drops MSYNC and shifts a transfer complete op code (17) to the drive. Depending on the op code received from the drive which requested the NPR, the TSBA may be either incremented or decremented. In either case the TSBA now points to the next location to be written in the buffer.

When the drive receives the transfer complete op code, it repeats the operation from the point of loading the data and op code to the TSDB requesting an NPR. This continues until all the data has transferred to the buffer.

When a message buffer is filled, the drive sends an op code to M7982 to load the TSSR and interrupt the CPU when done.

M7982 can request an interrupt on any one of BR4 through 7 depending on what priority jumper plug is installed. (BR-5 is normally used on the TS11.)

When M7982 sends a BR out and gets BG back it gates the vector switches (N) through the DATA MUX to the Unibus.

If the command received by the drive is to write data to tape, M7982 does NPR DATI operations. The drive sends an 18-bit address to M7982 with an op code to load it into the TSBA. Then the drive sends an op code to do an NPR DATI (read from memory) and either increment or decrement the TSBA when done.

The NPR takes place; then when the data is in the TSDB, M7982 serially shifts it to the drive with a transfer complete op code. The transfer complete op code signals the drive to request another word from memory and the process repeats from the point of the drive sending the op code requesting an NPR.

When the command is complete, the drive writes the message buffer and interrupts the processor.

If any transmission from the drive to M7982 has bad parity, the op code is ignored and M7982 immediately returns an op code of 11 to the drive.

The drive resets the SSR bit (TSSR bit 7) immediately after receiving the command word and keeps it reset for the duration of the command. Any attempt by the processor to write the TSDB in this period results in an RMR error which is sent to the processor when the drive writes the message buffer.

6.4.2.3 M7982 Op Codes – M7982 generates six op codes.

1. 17 – completed NPR, BR transfer or serial bus transfer.
2. 16 – RMR, NXM, or UPE error on a bus transfer.
3. 15 – TSDB was loaded with a word.
4. 13 – TSDB high byte (bits 8 through 15) was loaded.
5. 11 – serial bus parity error was detected on the data from the drive.
6. 7 – TSDB low byte (bits 0 through 15) was loaded.

M7982 decodes 14 op codes from the drive.

1. 00 – DATI and increment TSBA by 2 when done.
2. 01 – DATI and increment TSBA by 2 and invert TSBA bit 00 before transfer.
3. 04 – Load the TSSR from TSDB and interrupt the processor.
4. 05 – Load TSBA from TSDB.
5. 06 – Load TSSR from TSDB.
6. 07 – Load TSBA and TSSR from TSDB.
7. 10 – DATO and increment TSBA by 2 when done.
8. 11 – DATO, invert TSBA bit 00, and increment TSBA by 2.
9. 12 – DATO and decrement TSBA by 2 when done.
10. 13 – DATO, invert TSBA bit 00, and decrement TSBA by 2.
11. 14 – DATOB and increment the TSBA by 1 when done.
12. 15 – DATOB, invert TSBA bit 00, and increment TSBA by 1.
13. 16 – DATOB and decrement TSBA by 1 when done.
14. 17 – DATOB, invert TSBA bit 00, and decrement TSBA by 1.

6.4.3 Drive I/O

The Drive I/O section is made up of three modules: M8965, M8966, and M8967.

These modules are not discussed in detail separately. They are discussed as a single functional unit which has its components distributed among the three modules.

The discussion centers on the data flow along the buses and between the registers in the I/O section of the drive. (For a brief summary of these registers and buses, refer to Paragraphs 6.2.1 and 6.2.2.)

The I/O section may be viewed as a dedicated processor which acts as a slave of the control microprocessor. Its function is to move data between the drive and the Unibus via M7982 and the serial bus. Because of this limited role, the I/O section has no ALU. It is used mainly to move data around and does not need to do arithmetic operations. It tests for certain conditions and branches depending on the results of the test.

The I/O section performs the following functions.

1. It acts as an interface for transmission of command and status information between the control microprocessor and M7982.

2. It initiates NPRs during a tape write operation and sends data and parity to the write module (M8929).

3. It accepts data from the microprocessor during tape read operations and initiates NPRs transfers of read data to memory.

4. It accepts write format data from the microprocessor and sends this data to the write module.

5. It provides buffering to compensate for Unibus latency. (64 by 8-bit silo memory)

6. It initiates bus request (BR) cycles on demand from the microprocessor. It initiates BR cycles under its own initiative, if the microprocessor has a CROM parity error or if a silo parity error is detected (silo parity is also a check on the data path to the microprocessor).

7. It assembles data bytes on a read operation for the following.

   Odd byte starting address
   Odd byte ending address
   Even byte starting address
   Even byte ending address
   Forward and Reverse operation
   Normal and Swap Byte format
   It assembles data bytes on write operations.

The discussion in the remainder of this section refers to Figure 6-11.

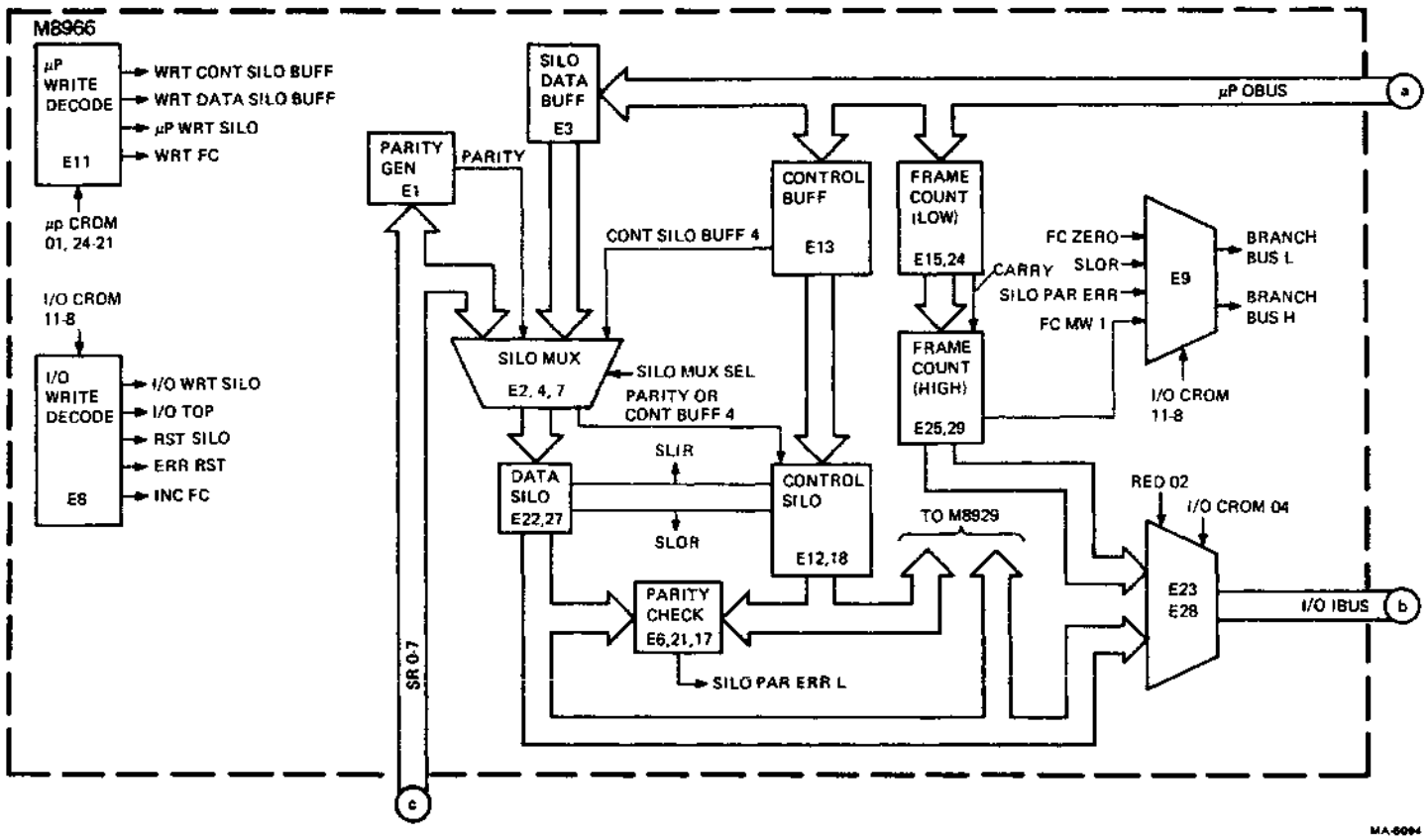


Figure 6-11 I/O Registers (Sheet 1 of 3)

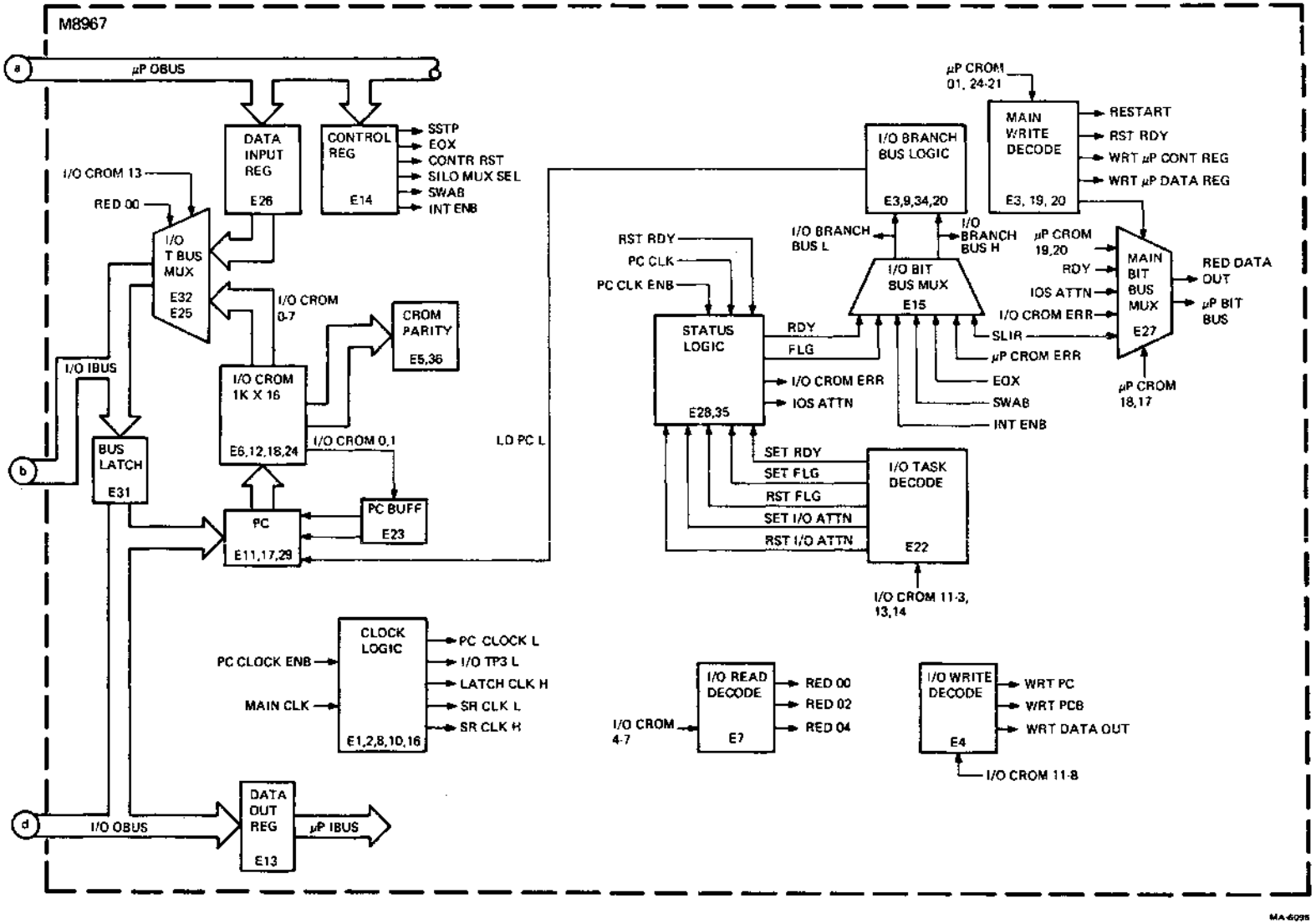


Figure 6-11 I/O Registers (Sheet 2 of 3)

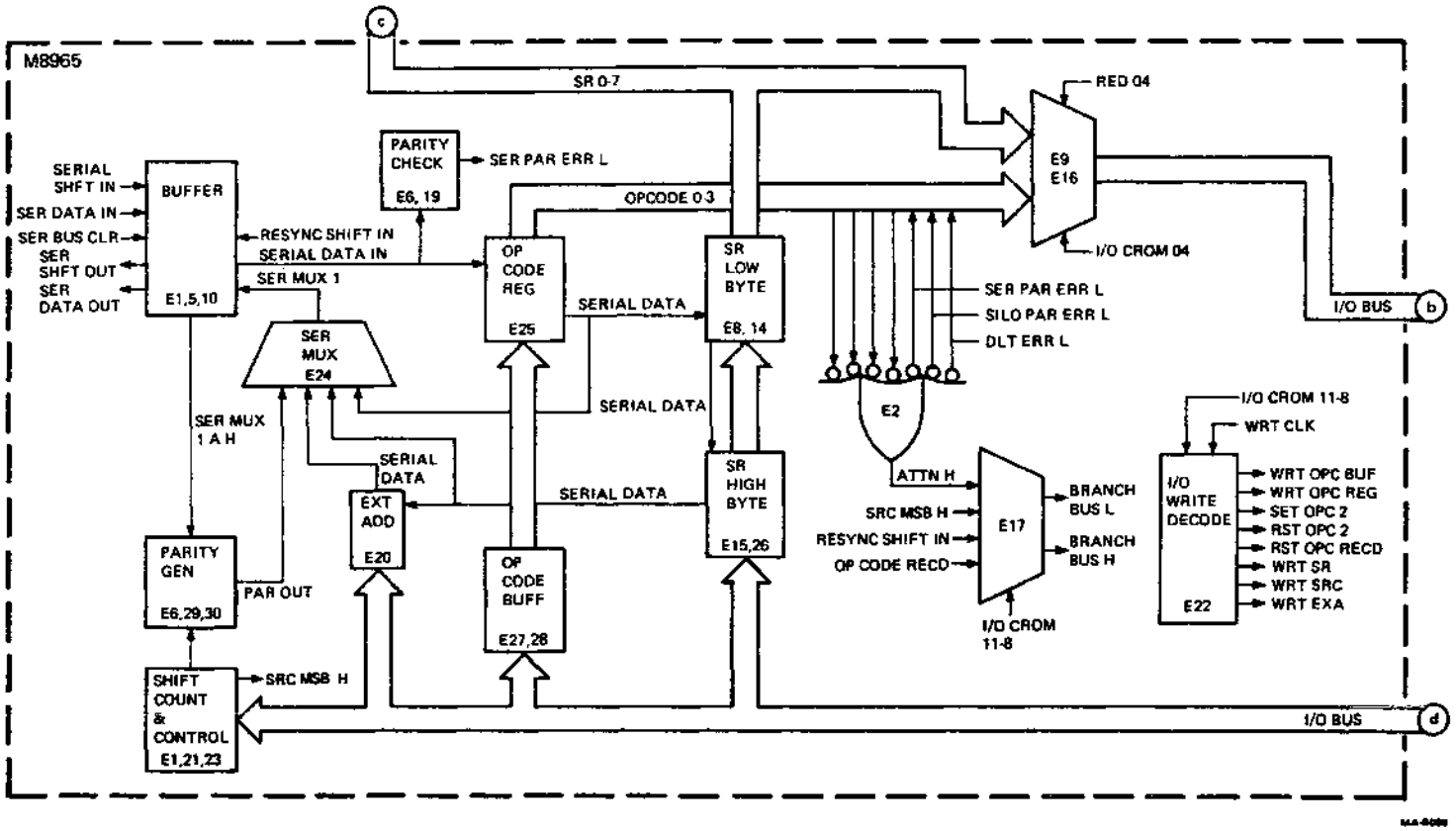


Figure 6-11 I/O Registers (Sheet 3 of 3)

6.4.3.1 I/O Registers – This section gives a brief description of the registers and busses in the I/O section of the drive. For a summary of register addressing, refer to Table 6-11.

6.4.3.1.1 Control Register – The control register is on the M8967 (also referred to as the I/O sequencer) module. The μP OBUS loads this 6-bit control register.

The μP writes the control register to control various aspects of the I/O section's operation.

Bit 0 – SSTP ; allows single step operation of the I/O section.

Bit 1 – EOX ; used by the μP to signal the end of current transfer. The 2901 will not transfer any more data to the silo.

Bit 2 – CONT RST L ; cleared by the μP to restart the I/O program counter at 0.

Bit 3 – SILO MUX SEL H ; when set, gives the μP input access to the data silo through the silo data buffer register. When the bit is 0, then the I/O section has input access to the data silo.

Bit 4 – SWAB ; these are swap bytes relative to host memory.

Bit 5 – INT ENAB ; when set, M7982 allows interrupts to the CPU.

Bits 1, 4, and 5 are used by the microcode and have no direct effect on the logic.

6.4.3.1.2 Data Input Register – This register is used by the μP to send data to the control portions of the I/O section. The register gets its input from the μP OBUS and its output feeds the I/O IBUS MUX.

6.4.3.1.3 Frame Count Register – This register keeps track of how many bytes have been transferred to or from M7982. The counter is incremented with each byte transfer.

The frame count register functions as a 16-bit counter which may be parallel loaded. It is organized as two 8-bit sections; high and low.

Loading takes place through the low byte of the counter. Data is taken from the μP OBUS and parallel-loaded into the low byte. At the same time, whatever was in the low byte is transferred to the high byte in parallel. It requires 2 writes to the low byte to load the entire 16 bits.

The frame count may be read via the high byte which feeds a multiplexer connected to the I/O IBUS. Another write to the low byte is required to transfer its contents to the high byte where it may be read.

6.4.3.1.4 Control Silo Buffer – The control silo buffer register allows the μP to write data into it once and have that data input to the control silo each time the silo input is clocked. It is only necessary to change the data in the buffer when the current operation requires a different data pattern. This allows the μP to write the register once for each type of operation even though many bytes are written to the data silo. The control silo output would then have the same configuration for each byte exiting the data silo.

6.4.3.1.5 Silo Data Buffer – This register allows the μP to write a constant pattern into the data silo with only one data transfer. The μP writes the desired pattern into the buffer and that pattern is transferred to the data silo with each WRT SILO command. This allows less data handling when writing preambles, postambles, etc.

During normal read operations the data buffer would be written each time a character was to be transferred to the data silo.

The silo data buffer is connected to the μP OBUS on its input and its output feeds the SILO DATA MUX.

6.4.3.1.6 Data Silo – The data silo is a 64 location by 8-bit first in first out (FIFO) memory used to compensate for Unibus latency. The data silo may be written by the μP via the silo data buffer or by the output of the shift register (SR).

During write operations the silo gets its data from the shift register via the SILO MUX. During read operations the silo gets its data from the μP via the silo data buffer.

The output of the silo is routed to the write module (M8929) and to the I/O IBUS via a multiplexer. During write operations the output is used by the write module. During read operations the output is routed by the I/O section to the shift register for transfer to the system CPU.

6.4.3.1.7 Control Silo – The control silo is a FIFO identical to the data silo (Paragraph 6.4.3.1.6) used for controlling the operation of the write module during write operations. The control silo is written by the μP via the control buffer.

The actual writing of the control and data silos occurs at the same time. The output of the silo multiplexer and the control buffer are applied to the inputs of the respective silos and clocked in at the same time. The same thing occurs at the output end of the silos. Each time the data silo is read so is the control silo.

6.4.3.1.8 Data Out Register – The data out register permits the I/O section to pass data to the μP. The data is usually requested by the μP when the μP calls a routine in the I/O to retrieve data.

The input to the register is the I/O OBUS and the output of the register is to the μP IBUS.

6.4.3.1.9 Shift Register – The shift register (SR) sends and receives data to and from the M7982 module via the serial bus. The register is 16 bits divided into 2 sections, high byte and low byte.

For serial data transmission and reception the data paths are as follows.

Data from the M7982 comes into the SR via the serial bus, a buffer and the op code register. It enters the low byte at the LSB end and is shifted serially through the low byte and then to the high byte.

Data to the M7982 leaves the SR via the MSB of the high byte and goes either to the EXT address register or to the serial multiplexer. From the serial multiplexer the data goes to the buffer and then to the M7982 via the serial bus.

The parallel load path for the SR is from the I/O OBUS to the high byte. Each time the high byte is loaded the data that was in the high byte is parallel shifted to the low byte. It requires two writes into the high byte to write the entire SR.

Data leaving the SR in parallel exits the low byte on SR0 through 7. These lines are connected to two multiplexers which feed the I/O IBUS or the data silo respectively. The high byte must be written to shift its contents to the low byte where it may be read.

6.4.3.1.10 Op Code Buffer – The op code buffer register has two functions. The lower four bits of the register hold the op code to be sent over the serial bus. The high order three bits (4 through 6) control the shift register data paths.

Bits 4 and 5 control the serial multiplexer select lines. These bits control the source of data to be shifted out on the serial bus. The data will come from the EXT ADD register if a 23-bit shift is to take place. It will come from the shift register if a 21-bit shift out is used. Or it will come from the shift register if a 5-bit output is desired.

Bit 6 is used to allow an op code to be shifted in from the serial bus without disturbing the shift register. This is used during read operations to load the shift register with data while waiting for the confirmation op code to be received from M7982.

The op code buffer is loaded from the I/O OBUS. The lower portion of its output (bits 0 through 3) are loaded into the op code register before shifting data out on the serial bus.

6.4.3.1.11 Op Code Register – The op code register holds the op code received from or to be transmitted to the M7982. The register is 4 bits and can be loaded in parallel or serially.

The op code register receives its serial input from the serial buffer. It enters the LSB end of the register and is shifted serially toward the MSB.

The serial output of the op code register is taken from the MSB end and is sent to the SR and the serial mux.

The op code register may be parallel loaded from the op code buffer. The contents of the op code register may be read via a multiplexer which feeds the I/O IBUS. The 4 op code register bits are routed onto the I/O IBUS along with SILO PAR ERR, SER PAR ERR, and DLT ERR whenever that input to the multiplexer is selected.

6.4.3.1.12 Extended Address Register – The extended address (EXT ADD) register is 2 bits in length. It is used in conjunction with the SR register to assemble an 18-bit address for transmission to the M7982.

The register is loaded from the I/O OBUS bits 0 and 1. It receives serial input from the SR and outputs serially to the SER MUX.

6.4.3.1.13 Shift Register Counter – This is an 8-bit register/counter. The lower five bits control the shift operation. The top three bits operate the diagnostic/wrap mode. This register is within the block titled shift count and control on the block diagram (Figure 6-11).

The register is loaded from the I/O OBUS with the 2's complement of the desired shift count. There may be 5, 21, or 23 shift clocks, depending on the length of the transmission to the M7982. (Refer to Paragraph 6.4.1.)

6.4.3.2 Data Paths (Figure 6-11) – In the following discussion, the I/O section is divided into four major data paths.

1. Microprocessor data path
2. Internal control and data path
3. Silo data path
4. Serial data path

6.4.3.2.1 Microprocessor Data Path – The μP data path in the I/O section consists of the μP OBUS, the μP IBUS, and the μP bit bus.

The μP OBUS connects to the control and data input registers on M8967 and to the frame count, control buffer, and silo data buffer on M8966. The addressing for these registers is decoded by the main write decode block on M8967 and by the μP write decode block on M8966.

The only register in the I/O section connected to the μP IBUS is the data out register on M8967. Its addressing comes from the main bit bus multiplexer on M8967.

The μP bit bus connects to the main bit bus multiplexer on M8967. The inputs that feed the μP bit bus are Silo Input Ready (SLIR), IO CROM ERR, RDY (the I/O ready flip-flop) and IOS ATTN.

6.4.3.2.2 Internal Control and Data Path – The internal control and data path consists of the I/O IBUS, the I/O OBUS, and the I/O branch bus.

The I/O IBUS is fed by three multiplexers, one on each module of the I/O section. The I/O IBUS feeds the I/O OBUS through a bus latch on M8967. This bus latch is clocked during every I/O timing cycle, placing the data from the IBUS onto the I/O OBUS.

The selection of the multiplexers feeding the I/O IBUS is controlled by the I/O read decode circuit on M8967 and I/O CROM bits 04 and 13.

The I/O OBUS feeds the PC and the data out register on M8967 and the SR, op code buffer, EXT ADD register, and the shift register counter (SRC) on M8965. The single source of data on the I/O OBUS is the bus latch. The I/O section timing is such that an I/O IBUS multiplexer can be selected, the data latched into the bus latch, and then gated into a register on the I/O OBUS in a single timing cycle.

The address decoding for the registers on the I/O OBUS is done in the I/O write decode circuits (one each on the M8967 and M8966 modules).

The I/O branch bus takes its inputs from three multiplexers (M8967-E15, M8966-E9, and M8965-E17). The outputs of these multiplexers feed the I/O branch bus logic on M8967, which causes the PC to be loaded from the I/O OBUS and the PC buffer register if the condition being tested is satisfied. This gives the I/O section its test and branch capability.

The I/O CROM and PC are not part of the data path but they do control its operation. The CROM and PC are on M8967, also called the I/O sequencer.

The CROM contains 1K of 16-bit control words which control the data path internal to the I/O section.

The PC sequentially addresses the CROM locations to cause data to be routed from one part of the I/O section to another. The sequential CROM locations form routines to perform various functions. Looping can be accomplished using the branch bus inputs to cause the PC to be loaded with a new value which itself came from CROM (bits 00 through 07). The PC can be cleared by the μP through the control register (CONTR RST).

6.4.3.2.3 Silo Data Path – The data silo takes its input from the silo multiplexer. The silo multiplexer selects either the silo data buffer register or SR lines 0 through 7 as the input to the data silo. The controlling input for the silo mux is SILO MUX SEL from the control register on M8967.

The input to the control silo is the control buffer register. Control silo bit 4 comes from the silo multiplexer. The silo multiplexer selects either the output of the parity generator or control buffer 4 as the input to bit 4 of the control silo.

If the silo multiplexer has the silo data buffer selected as the source for the data silo then bit 4 from the control buffer is routed to the bit 4 input of the control silo. If the silo mux has the SR lines selected for input to the data silo then the output of the parity generator is sent to the bit 4 input of the control silo.

The silo input is gated by either μP WRT SILO or IO WRT SILO from the write decode circuits on M8966. Both silos' inputs are written at the same time by either of these signals.

The output of both silos goes to a parity check circuit and to the write board (M8929). The output of the data silo also goes to a multiplexer which feeds the I/O IBUS.

The output of the silos is shifted out by signal WRT REQ SILO L (from M8929) or IO TOP. Either signal causes the next sequential data word to be output.

6.4.3.2.4 Serial Data Path – The serial data path is contained entirely on M8965. It consists of a buffer, op code register, SR, EXT ADD register, and serial multiplexer.

For serial input from the serial bus the buffer, op code register, and the SR may be thought of as a single serial shift register 21 bits long.

Serial input data enters the buffer, is delayed one-half I/O timing cycle and then is passed to the op code register. The data enters the LSB end of the op code register and is shifted serially to the MSB.

If the transmission is data and op code, the data is sent to the SR low byte. If the transmission is just an op code the shifting stops when the data reaches the MSB of the op code register. At this point the parity bit will be left in the buffer and is checked by the parity check circuit.

If the transmission was 21 bits (data plus op code plus parity) the data is passed from the op code register to the SR low byte. It is shifted through the low byte then passed to the high byte. When the entire shift operation is done the op code will be in the op code register, the data in the SR and the parity bit in the buffer.

For serial output to the serial bus the op code register, the SR and the EXT ADD (extended address) registers may be thought of as a 22-bit shift register. This shift register may be split into segments containing the op code register or the op code register plus the SR or the op code register plus the SR plus the EXT ADD register. This will allow transmissions of 5 bits (op code plus parity), 21 bits (data plus op code plus parity) or 23 bits (2 extended address bits plus 16 address bits from the SR plus op code plus parity). The parity bit is appended at the end of transmission and cannot be considered part of a shift register.

The serial multiplexer determines the source of the serial data to be shifted out. The selection lines to the serial multiplexer are controlled by the op code buffer and the SRC.

The op code buffer and SRC must be loaded before any shift out operation to set up the data path and the proper number of shifts. If data is to be sent out, the SR must also be loaded prior to starting the shift out. If an 18-bit address is to be sent then the EXT ADD register must also be loaded before starting the transmission. All of these registers are loaded via the I/O OBUS.

The SRC must be the last register loaded prior to starting the shift. Loading the SRC causes the shift out operation to begin.

6.4.3.3 Drive I/O Operation – The major job of the I/O section is to keep the silo full on data write operations and to empty it on read operations.

On data write operations the I/O along with the M7982 will get data from memory and put it in the silo. The write board (M8929) takes the data from the silo and sends it to the write head assembly.

On data read operations the μP puts read data from the formatter in the silo. The I/O takes the data from the silo and sends it to the M7982. The M7982 then puts the data into memory.

The I/O also has to get command information and pass it to the drive and send message packets from the drive to memory.

All of these operations are under the control of the main μP. The I/O is only a slave to the μP. It does virtually nothing on its own.

6.4.3.3.1 I/O as Slave of Microprocessor – The I/O section is normally in a loop waiting for the μP to tell it to do something. The μP starts by loading the data input register with the address of the desired I/O routine. The μP then resets the RDY bit on M8967.

The following is an example of what happens when the μP reads the frame count.

When the RDY bit resets the I/O gates the data input register into the PC. The PC then contains the initial address of the routine to read the frame count register.

The I/O gates the contents of the frame count (high byte) into the data output register, sets the RDY bit, and goes back to the wait loop.

The μP sees the RDY bit (via the μP bit bus) and reads the data output register. Since the frame count register is 16 bits, the μP only has the high byte at this point. The μP writes the frame count register to push the contents of the low byte to the high byte.

At this point the μP again writes the data input register with the same address as before and reset RDY.

The I/O loads the PC with the address and repeats the routine a second time.

6.4.3.3.2 Read Operation Transfers – Assume that the drive has received a command packet which told it to read tape. Also assume the data buffer in CPU memory space starts at location 20000 (8). And that the file to be read is 512 (10) characters.

The μP causes the I/O section to load: 0s into the EXT ADD register, 020000 into the SR; and op code 5 into the op code buffer (5 says load TSBA). The I/O then loads 351 (-23 decimal) into the SRC register.

Shifting operation begins when the SRC is loaded.

While the I/O was setting up the M7982, the μP was starting the read operation. The μP writes the silo data buffer register with the read data and strobes it into the data silo. It also loads the control buffer with the proper parity for each character. Parity is not generated by the hardware on transfers from the silo data buffer to the data silo. The μP must supply this information.

The I/O enters the wait loop after receiving the transfer complete op code from the M7982. The μP then enters the routine to transfer read data to the CPU.

The I/O waits for the first data to bubble through the silos (this may take several microseconds). The silo asserts SLOR when data is at the Silo output. The I/O will take the data and load it into the SR high byte. The I/O again waits for SLOR and then transfers the next byte to the SR. The first word is assembled.

The I/O loads a 10 into the op code buffer and strobes it into the op code register (10 says DATO and increment by 2). The op code buffer has bit 6 set to enable reception of the reply op code from the M7982 without disturbing the SR. Then the I/O loads the SRC with 353 (-21 decimal) to initiate the transfer.

The I/O waits for SLOR and transfers the next byte to the SR. When the next word is assembled and the reply from the first transfer is received, the I/O strobes the op code buffer into the op code register. It then loads 353 into the SRC and the operation repeats.

This operation will repeat all the data that is transferred to the memory.

6.4.3.3.3 Write Operation Transfers – Assume that a command packet is received and that the drive is to write data to tape. The starting address of the data in memory is 105000 (8) and 256 16-bit words will be written.

The μP sends the I/O the address of the routine to load into the TSBA. The I/O takes address from the μP via the data input register and places 0s in the EXT ADD, 105000 in the SR, and 5 into the op code buffer. The I/O then strobes the op code from the buffer into the op code register and loads 351 into the SRC.

The data is shifted out to the M7982 and when the reply op code is received, the I/O goes back to the idle loop.

The μP writes the frame count register with −512 (decimal) in two writes. It then loads any control bits required into the control silo buffer and the I/O control register, to set up the silo mux sel bit. The μP then loads the preamble data into the silos.

Then the μP writes the I/O control register to set up the silo multiplexer for data from the SR.

Next, the μP sends the I/O the starting address of the routine to move data from memory into the silo for a write operation. The I/O starts the routine and loads the op code buffer with an op code of 00. The I/O writes the op code register and loads the SRC with 353 (−5 decimal). The op code is shifted to the M7982 and the I/O waits for the data.

After data and the op code are received from the M7982 the following occurs: the I/O transfers the SR low byte to the silo and strobes it in if SLIR is asserted. If SLIR is not asserted the I/O waits until it comes up to transfer data to the silo. The I/O increments the frame count register, writes to the SR (to push the data from the high byte to the low byte) and again transfers the low byte to the silo. The I/O then increments the frame count and repeats the procedure from the point of loading the op code register.

The above process continues until the frame count register goes to 0. At a count of 0, the transfers from memory are complete but not the write operation. The I/O signals the μP that the frame count is 0 and to start writing postamble data to the silo. The μP then writes the I/O control register to change the SILO MUX SEL bit and commences writing postamble data to the silo.

When the postamble data is in the silo, the write board must still finish taking it from the silo and getting it to the tape.

6.5 TAPE HANDLING

This section describes the functions of moving tape forward and reverse, rewinding tape, and maintaining correct tape tension. Figure 6-12 is an overall block diagram of the tape handling function.

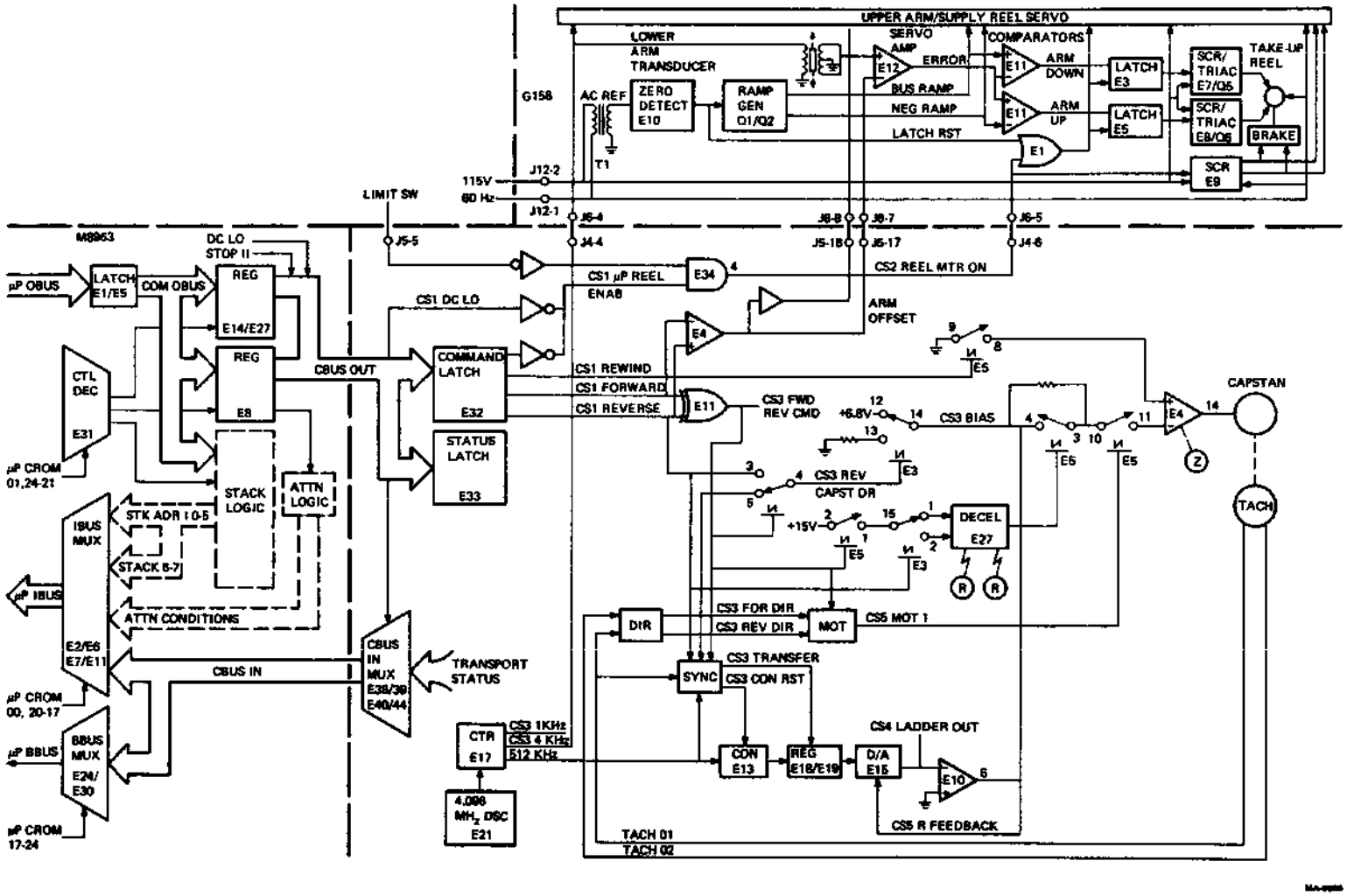


Figure 6-12 Tape Handling Function

6.5.1 Overview

The main microprocessor issues capstan commands to control tape motion. Feedback from an optical tachometer (on the capstan assembly), provides constant forward or reverse capstan speed of 45 in/s. During rewind the majority of the capstan control circuitry is bypassed and tape speed is 150 in/s. For maintenance purposes, the main microprocessor can issue commands to simulate motion; and a switch (S9) is provided on the G159 capstan servo board to move tape forward or reverse.

Supply and take-up reel motors maintain tape tension. These motors are controlled by a servo error signal that is proportional to the position of the respective tension arms. For example, when the capstan moves tape forward, the upper tape loop becomes smaller, forcing the upper tension arm down. Movement of the arm develops an error signal that feeds the supply reel motor. The direction of the error signal causes the motor to move forward, delivering more tape to the upper loop and allowing the tension arm to return to its normal position. At the same time forward tape motion increases the size of the lower tape loop and allows the lower tension arm to move up. This motion develops an error signal that causes the take-up reel motor to move forward. This takes the slack out of the lower tape loop, forcing the lower arm to return to its normal position.

6.5.2 Tape Handling Commands and Status (Figure 6-12)

Data on the μP OBUS is latched into latch E1/E5 on the M8963 board. The output of the latch is COM OBUS and may be capstan data, stack data, or attention data. The output of decoder CTL DEC E31 is selected by μP CROM 01,24-21 to route COM OBUS according to the type of data. Capstan data is loaded into register REG E14/E27 when μP CROM 01,24-21 = 37, and into REG E8 when μP CROM 01,24-21 = 36. (Table 6-11 lists μP CROM fields 01,24-21 and 00,20-17.)

Command latch E32 and status latch E33 are addressable latches. The outputs of the status latch drive the operator panel indicators. Addressing and outputs of the two latches are listed in Table 6-7.

The status signals from CBUS IN are placed on the μP IBUS through IBUS MUX E2/E6/E7/E11 on M8963 when μP CROM 00,20-17 = 02. Other inputs to this multiplexer are selected by μP CROM 00,20-17 = 22, 03 or 23 (Table 6-11). Microprocessor CROM field 24 through 17 values of 010 through 017 to BBUS MUX E24/E30 can select any of the CBUS IN lines (0 through 7) to assert μP BBUS.

To summarize, the main microprocesser sends commands (or status) to the capstan servo via μP OBUS, COM OBUS, and CBUS OUT. COM OBUS is routed to CBUS OUT by the code in μP CROM 01,24-21. The main microprocessor samples transport status by selecting the input to CBUS IN with CBUS MUX SEL 0 and 1, and then selecting CBUS IN as the input to the μP IBUS with μP CROM 00,20-17.

Signals CAPS MUX 0 and 1 from REG E8 become CBUS MUX 0 and CBUS MUX 1 and select the inputs to CBUS IN MUX E38/E39/E40/E44 on the G159 board. The multiplexer inputs selected are shown in Table 6-8.

NOTE

Enter 0s in maintenance mode.
Enter 1s in maintenace mode.
In maintenance mode:

1. **Start/stop test.**
2. **Load tape if not already loaded.**

Tachometer Phase 1 or CS3 1 KHz.

6.5.3 Capstan Motion

The capstan servo board, G159, controls capstan motion. The motion functions performed by this board are motion detection, direction detection, speed regulation, capstan drive, and deceleration control. (Refer to Figure 6-12 for an illustration of the entire board. Figures 6-13 through 6-21 show more detail.)

6.5.3.1 Motion and Direction Detection (Figure 6-13) – The first of two motion flip-flops sets, by DC LO, when the TS11 powers up. Setting either flip-flop causes CS5 MOT 1 to be low. The first forward or reverse command asserts the CS3 FWD REV CMD signal. This resets both motion flip-flops and asserts CS5 MOT 1 for normal operation (not maintenance mode).

When the capstan starts turning in the forward direction, CS5 TACH 0 (phase) 2 will lead TACH 0 1 by 90 degrees. The direction flip-flop will then set and assert CS3 FOR DIR. In the reverse direction, TACH 0 1 leads TACH 0 2 by 90 degrees, resetting the direction flip-flop and asserting CS3 REV DIR.

CS5 MOT 1 remains asserted unless DC LO is again asserted, CS1 MAINT MODE is asserted, or CS3 FWD REV CMD is low and the tachometer signal phase relationship reverses (which changes the state of the direction flip-flop).

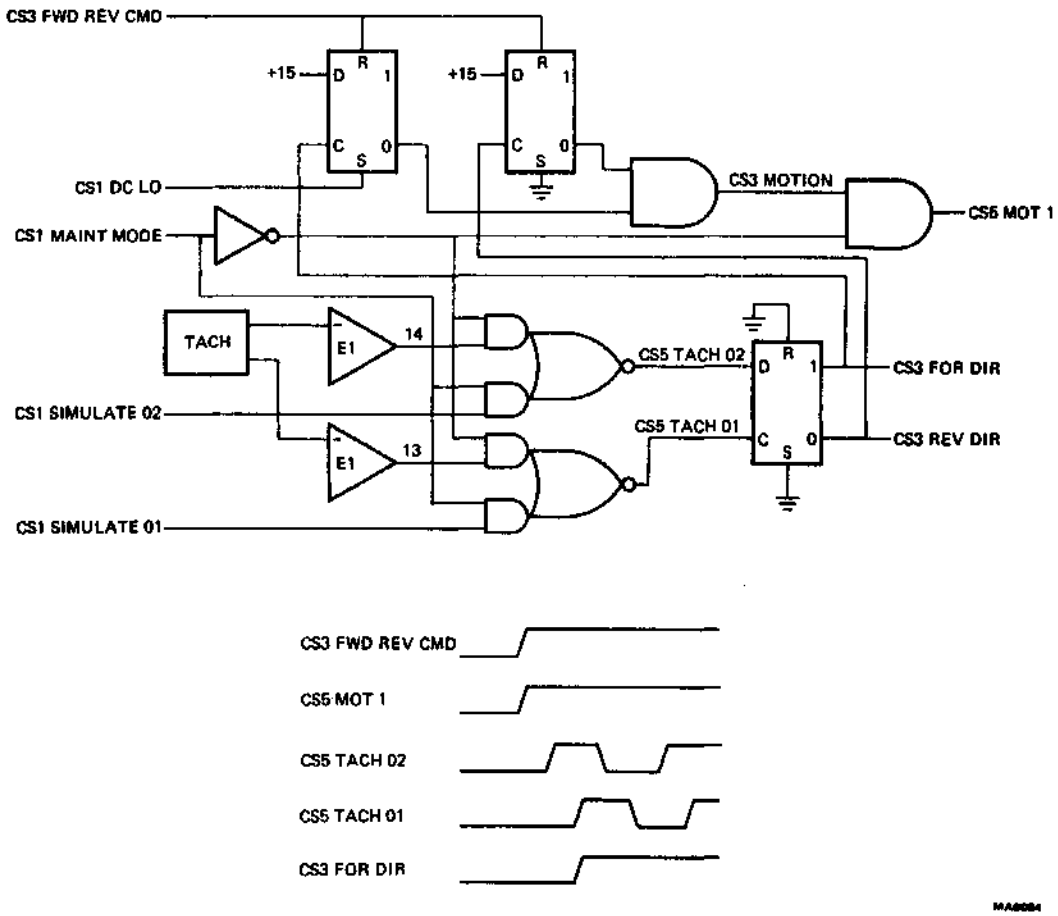


Figure 6-13 Motion and Direction Detection

6.5.3.2 Speed Regulation (Figure 6-12) – Capstan speed is controlled through a resistive ladder digital-to-analog converter, D/A E15. The D/A converter is driven by a resettable counter and register combination, CON E13 and REG E18/E19. Counter CON E13 counts 512 KHz clocks from free running counter CTR E17 and is synchronized to the tachometer by a four flip-flop sync chain, SYNC.

Turn to Figure 6-14 and its associated timing diagram, Figure 6-15. When the capstan is idle (not turning), CON E13 counts up until it reaches 256. Then CS4 CON NO OC sets and stops the 512 KHz clocks to CON E13. CON E13 resets when the capstan starts to turn.

As the capstan begins to turn (forward), CS3 TRANSFER sets within two 512 KHz clock cycles after the first CS5 TACH 0 1. The maximum count (256) from CON E13 transfers to REG E18/ E19, and CS4 ladder out sets to its maximum value. This maximum input from D/A E15 overcomes the inertia of the capstan and brings it quickly up to speed. One-half 512 KHz clock cycle after CS3 TRANSFER sets CON E13 resets. This causes CS3 CON NO OC to reset and CS3 CON CLK starts clocking CON E13.

At capstan speed of 45 in/s, CON E13 reaches a count of 128 before being reset in synchronization with CS5 TACH 0 1. If the capstan turns at less than 45 in/s, the time between successive TACH 0 1 signals increases and so does the count in CON E13. If the capstan turns above 45 in/s, the TACH 0 1 interval is shorter and the count in CON E13 is less than 128.

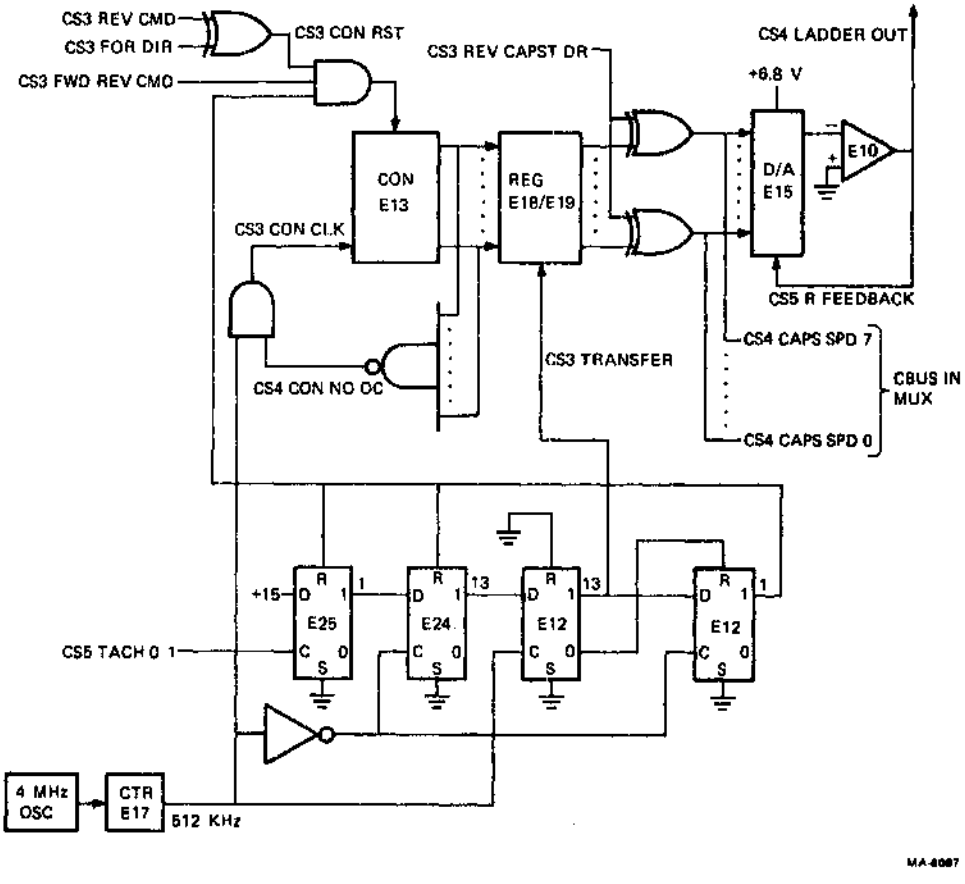


Figure 6-14 Capstan Speed

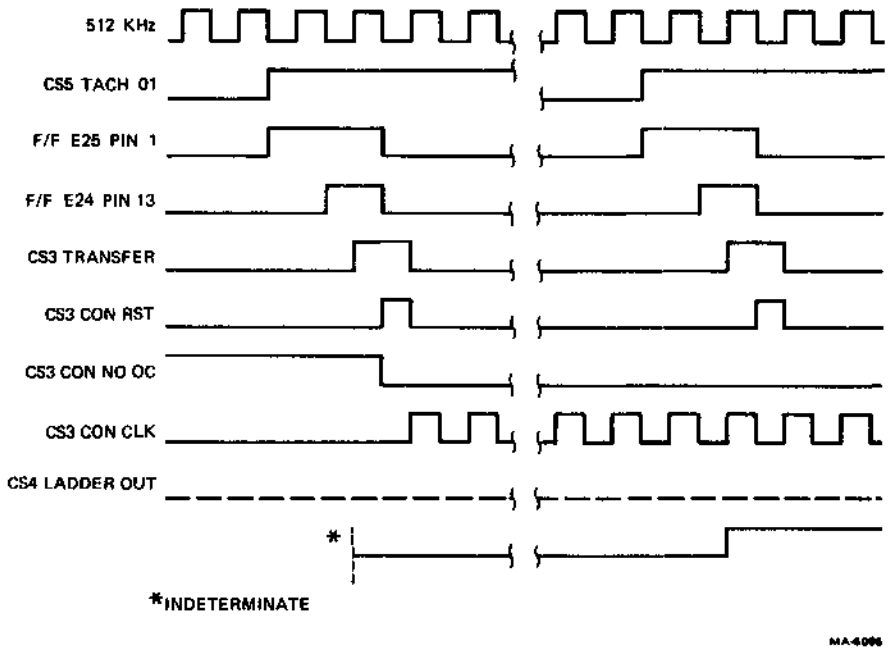


Figure 6-15 Capstan Timing Diagram

In the forward direction, a higher count (slow speed) increases the output of the D/A converter, and a lower count (high speed) lowers the output. In the reverse direction, CS3 REV CAPST DR to each exclusive-OR gate causes the count in REG E18/E19 to be 1's complemented. Thus a high count (slow speed) in the reverse direction lowers D/A output, and a low count (high speed) raises D/A output.

Rewind bypasses the speed regulation circuits.

6.5.3.3 Capstan Drive (Figure 6-12) – Switches labeled E3 and E5 are electronically controlled and are shown deactivated (the control input is low). Some of these same switches appear in simplified schematics (Figures 6-16 and 6-17) and have functional names in those figures. The simplified schematics are referenced in the following descriptions of idle, forward, reverse, and rewind operation. Figure 6-20 shows a comparison of how circuit parameters vary between these operations, without attempting to list actual parameter values.

6.5.3.3.1 Idle (Figure 6-16) – The reference input to amplifier E4 (pin 12) is tied to +3.4 V. The circuit attempts, through feedback, to maintain the inverting input (pin 13) at the same level as the reference input.

At idle, the DECEL SW, MOT SW, and REWIND SW are all open. The BIAS SW is closed, pin 12 to 14. Amplifier E4 pin 14 is driven in a positive direction to overcome the level from the +6.8 V to -15 V voltage divider on the inverting input. The circuit is designed so that at idle, the current through Q1 and Q2 is balanced and the capstan does not turn. R26 adjusts to the balance (null adjustment).

6.5.3.3.2 Forward (Figure 6-17) – When the capstan rotates forward the REWIND SW is open. The BIAS SW is closed, pin 12 to 14. The MOT SW was closed by CS5 MOT 1, and the DECEL SW is closed (operation of the DECEL SW is described below). The signal at the inverting input (pin 13) to E4 is now

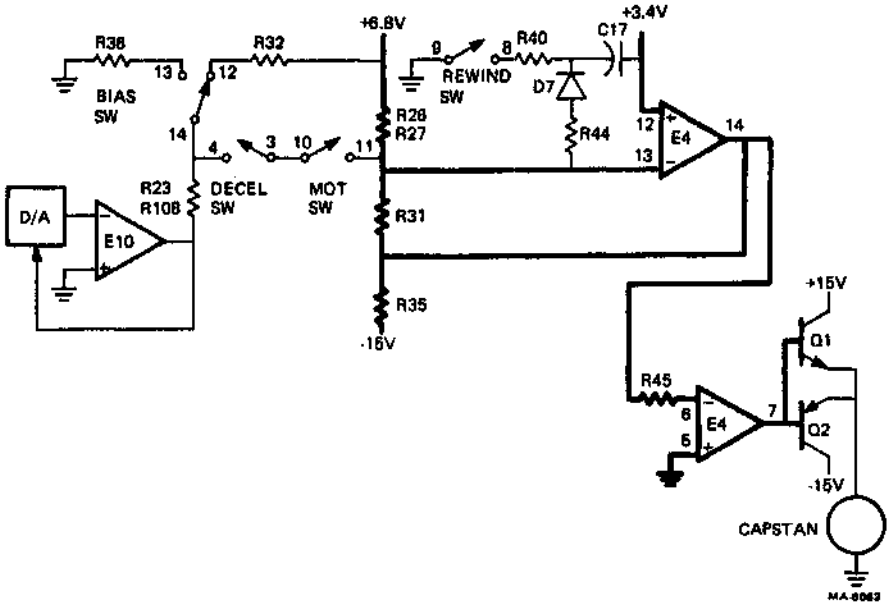


Figure 6-16 Idle – Capstan Drive

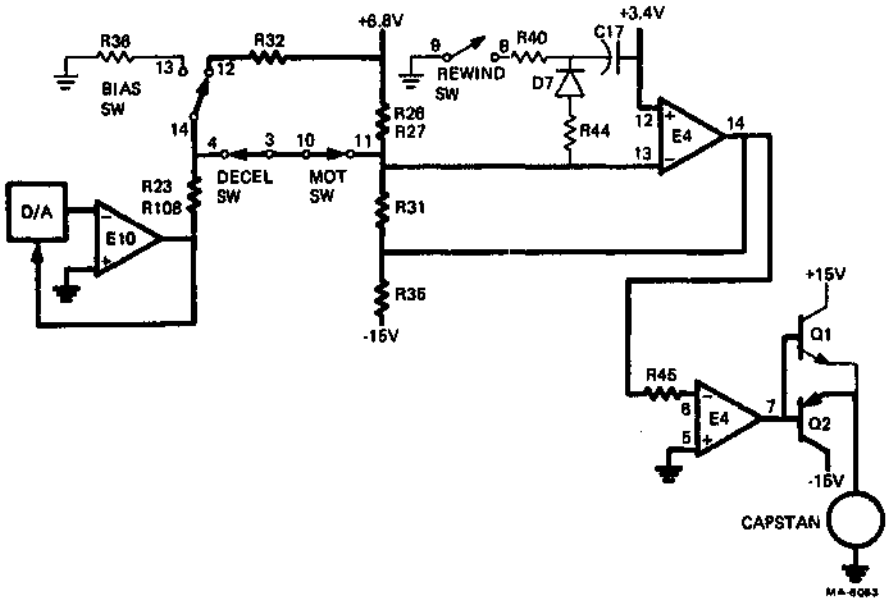


Figure 6-17 Forward – Capstan Drive

determined by CS4 ladder out from E10, the positive bias from +6.8 V through the BIAS SW, the +6.8 V to +15 V voltage divider and the feedback from E4 pin 14. In the forward direction, E4 (pin 14) operates in the more positive portion of its range. This causes E4 (pin 7) to increase the forward bias on Q2 and to decrease forward bias on Q1, unbalancing the circuit and supplying forward drive current to the capstan.

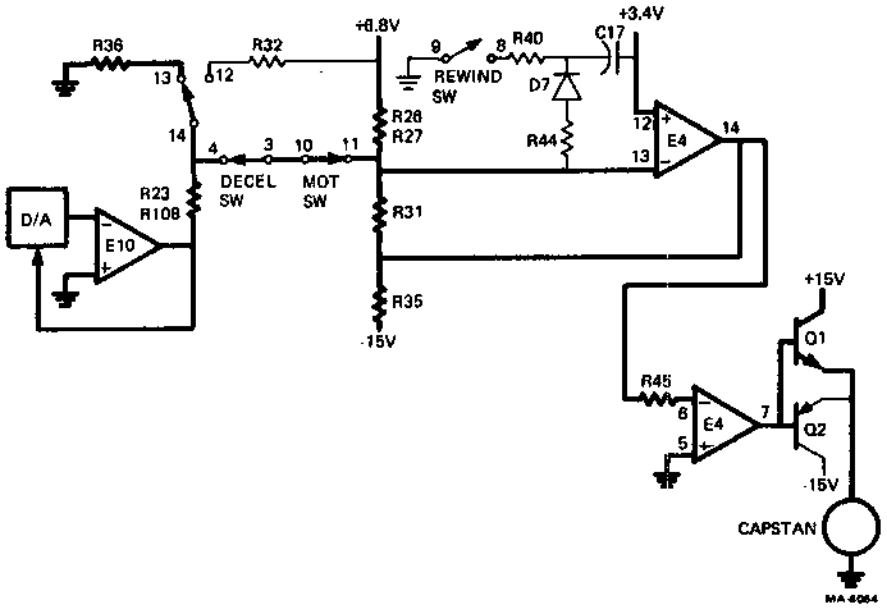


Figure 6-18 Reverse – Capstan Drive

6.5.3.3.3 Reverse (Figure 6-18) – When the capstan rotates reverse the switch operation is the same as in the forward direction except that CS3 REV CAPST DR activates the BIAS SW closing pin 13 to 14. Bias through the BIAS SW is now closer to ground, causing E4 (pin 14) to operate in the less positive portion of its range. E4 (pin 7) increases the forward bias on Q1 and decreases the forward bias on Q2, increasing reverse drive current through the capstan.

6.5.3.3.4 Rewind (Figure 6-19) – The REWIND SW is closed by CS1 REWIND. All the other switches are deactivated. The inverting input (pin 13) to E4 is now more positive (closer to ground) than its normal operating range for reverse rotation. E4 (pin 14) is operating near the minimum positive end of its range, and the forward bias is high on Q1, low on Q2. Rewind speed is determined by component parameters. Diode D7 limits the positive swing of the inverting input to E4, thereby limiting rewind speed.

6.5.3.4 Deceleration – The capstan stops by reversing the drive current through it. The deceleration circuit prevents excessive overshoot (rotation in the opposite direction) when the capstan is stopped. This description references most of the figures previously used in this section.

Refer to Figure 6-12. Assume the capstan is turning forward at 45 in/s and the forward command is dropped. CS3 FWD REV CMD goes low and switch E5 (pins 1 and 2) at the input to the DECEL circuit opens. Switch E3 (pins 3, 4 and 5) deactivates, closing pins 5 to 4 as shown. At this point the following occurs.

1. Refer to Figure 6-13. CS3 FOR DIR stays high until the capstan begins to turn in the reverse direction causing CS5 TACH 0 1 to lead CS5 TACH 0 2, resetting the direction flip-flop. CS3 FOR DIR asserts CS3 REV CAPST DR through switch E3 pins 4 and 5 (Figure 6-12).

2. Refer to Figure 6-14. When CS3 FWD REV CMD goes low, CS3 CON RST is disabled, and counter CON E13 counts up to 256. At 256 CS4 CON NO OC goes high and stops CS3 CON CLK.

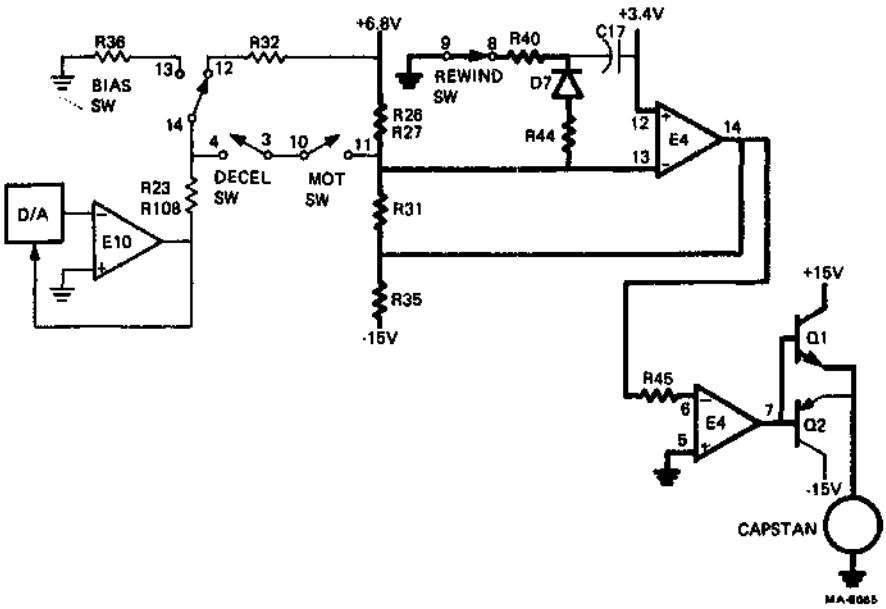


Figure 6-19 Rewind - Capstan Drive

CAPSTAN SPEED	CAPSTAN DIRECTION	COUNT	D/A OUT	E4 PIN 14	E4 PIN 7	Q1 DRIVE	Q2 DRIVE
START	FORWARD	256	MAX	MAX	MAX-	MIN	MAX
<46	FORWARD	>128	↑	↑	↑	↓	↑
46	FORWARD	128					
>46	FORWARD	<128					
IDLE	-	-	-		0	=Q2	=Q1
>46	REVERSE	<128	↑		↓	↓	↑
46	REVERSE	128					
<46	REVERSE	>128					
START	REVERSE	256	MIN	MIN	MAX+	MAX	MIN
150	REWIND	-	-	>MIN	<MAX+	<MAX	>MIN

MA-6061

Figure 6-20 Parameter Comparison

3. Refer to Figure 6-14. CS3 REV CAPST DR high at the input to the exclusive-OR gates complements the output of register REG E18/E19. Usually, this output is complemented when the capstan is turning in the reverse direction (Paragraph 6.5.3.2).

4. Refer to Figure 6-12. CS3 REV CAPST DR high activates switch E3 BIAS SW (pins 12, 13 and 14) closing pins 13 to 14. Usually, pins 13 and 14 are closed when the capstan is turning in the reverse direction.

NOTE

At this point the speed regulation circuits and BIAS SW are set up for reverse rotation, although the capstan is still turning in the forward direction.

5. Refer to Figure 6-14. The next CS5 TACH 0 1 signal triggers the SYNC flip-flops and generates CS3 TRANSFER (Figure 6-15). The maximum count from CON E13 transfers to REG E18/E19, complements, and drives CS4 LADDER OUT to its minimum value.

6. Refer to Figure 6-18. Although the capstan is turning in the forward direction, the drive circuits are configured for reverse, and the output from E10 (CS4 LADDER OUT) is at maximum reverse drive signal. As a result, Q1 gets maximum forward bias, Q2 gets minimum, drive current reverses, and the capstan begins to slow down.

NOTE

The electrical and mechanical characteristics of the capstan are such that, if left alone the capstan would slow down, coast through idle, and start to accelerate in the reverse direction.

7. Refer to Figure 6-21. When E5 pins 1 and 2 open, the charge on C21 maintains the output of E27 high. The DECEL SW stays closed until C21 discharges through R86 and R87. This RC time is calculated (and adjustable) to allow the reverse drive current to reduce forward speed by about 80 percent before opening the DECEL SW. Two RC circuits compensate for unequal forward and reverse circuit parameters.

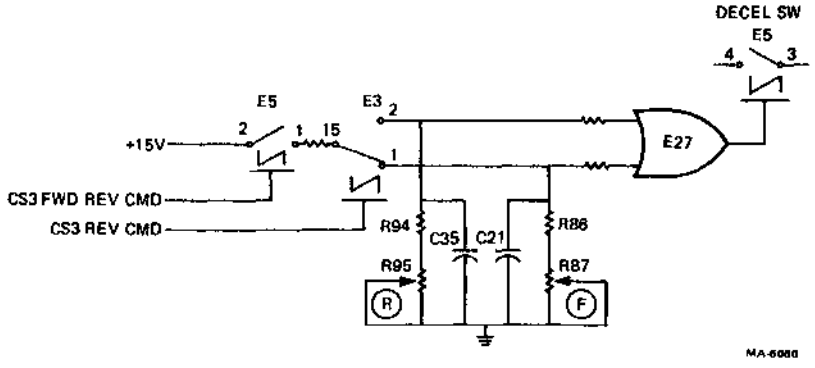


Figure 6-21 DECEL Switch

8. Refer to Figure 6-13. When the DECEL SW opens, removing bias and CS4 LADDER OUT from the drive circuits, the capstan coasts through idle, and the tachometer signal phase relationship reverses. However, the capstan does not move in the reverse direction. CS5 TACH 0 1 leads CS5 TACH 0 2, resetting the direction flip-flop and asserting CS3 REV DIR. The second motion flip-flop sets causing CS5 MOT 1 to go low. This opens the MOT SW in the drive circuits.

9. When the direction flip-flop resets, CS3 FOR DIR goes low, causing CS3 REV CAPST DR to drop, deactivating the BIAS SW and uncomplementing the output of REG E18/E19.

In summary, when a forward or reverse command is dropped, the capstan drive circuit sets up reverse drive current and electronically brakes the capstan. The deceleration circuit is adjusted to allow a calculated amount of overshoot.

6.5.4 Tape Tension

Supply and take-up reels maintain motors correct tape tension. The reel motors respond to error signals generated by the tension arm transducers which are mechanically coupled to the tension arms. The error signal produced is proportional to tension arm movement.

The reel servo board, G158, is shown in the upper right of Figure 6-12. The board contains the following items.

ramp generator
reel motor brake control
upper arm/supply reel servo assembly
lower arm/take-up reel servo assembly

The tension arm transducers and reel motors are not mounted on the board. Because the servo assemblies are the same, operation of only the lower is described.

Figure 6-22 provides more detail of the transducer error circuitry, Figure 6-23 shows signal relationships, and Figure 6-24 shows the tape load path. Table 6-13 gives a summary of the operation of the tape tension function.

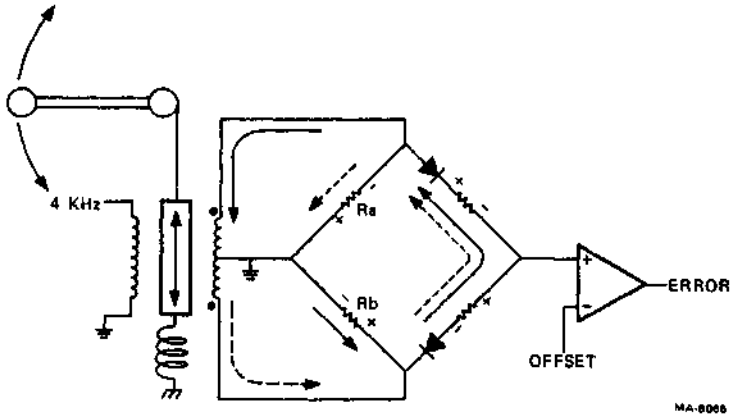


Figure 6-22 Tension Arm Transducer

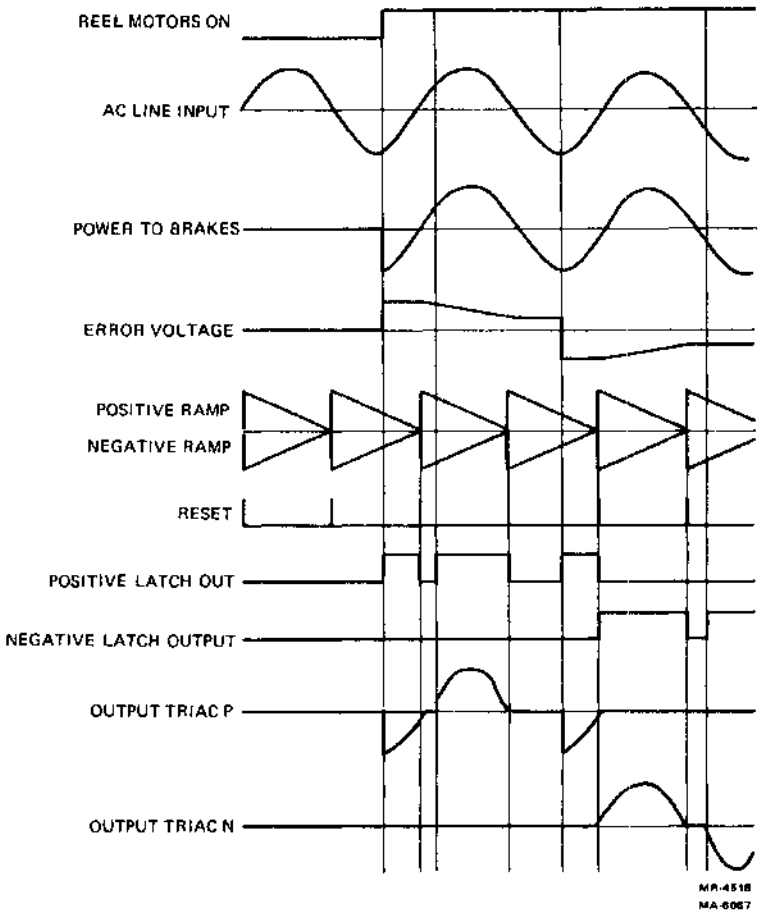


Figure 6-23 Signal Relationships

6.5.4.1 Tension Arm Error Signal (Figure 6-22) – The tension arm transducer is a transformer with a moveable core or slug. The slug is connected between the pivot end of the tension arm and tension spring. Tape motion moves the tension arm causing the slug to move. The degree of coupling between the primary transformer winding and one half of the secondary is increased, causing the current to increase in the secondary winding. Coupling to the other half decreases, decreasing secondary current in that half. The secondary winding is wound so that these currents are out of phase, and connected to the input of a bridge. Current flows through one half of the secondary winding or the other on alternate half cycles of the 4 KHz input. The signal at the noninverting input to the error signal amplifier becomes:

1. zero when the tension arm (and slug) is centered;
2. negative when the arm is off center and the current through Ra is greater; or
3. positive when the arm is off center in the opposite direction and the current through Rb is greater.

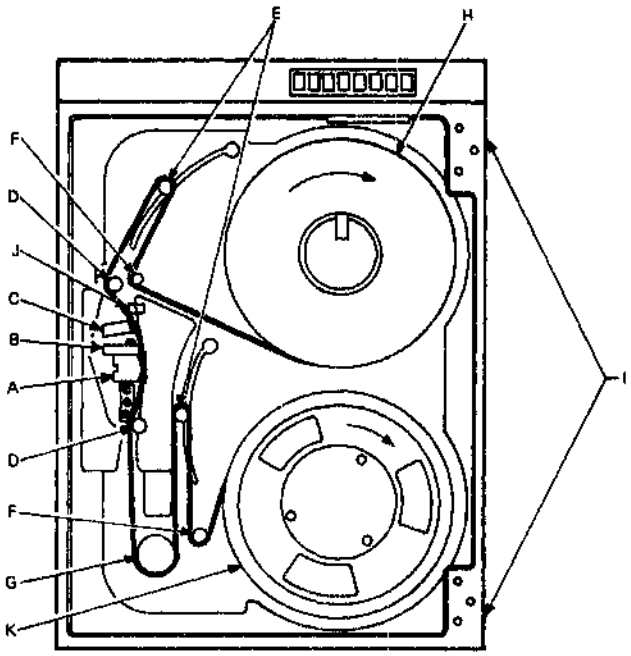


Figure 6-24 Tape Loading Path

The offset signal to the inverting input of the amplifier is negative for forward tape motion commands and positive for reverse tape motion commands (opposite for the upper arm servo). This signal aids or opposes the error signal, depending on arm position and tape direction. It offsets the effect of reel momentum when tape motion is reversed. For example, when tape moves in the reverse direction, and the lower arm is down (too much tension), the error signal increases reverse drive to the lower motor. The lower reel motor supplies more tape to the lower loop, decreasing tension. The offset signal polarity is positive to the lower reel servo when tape is moving reverse increasing slack in the lower loop. If the tape is moving forward reel momentum would tend to increase tape tension. The additional slack provided by the offset signal compensates for the momentum, and prevents the tension arm from hitting the limit switch.

Not shown is an RC network on the inverting input. This network causes a temporary increase in amplifier gain when there is a very large input signal from the bridge. The amplifier then supplies a large error signal to overcome reel motor inertia when tape reverses direction or starts from rest.

Table 6-13 Tape Tension Function Summary

Reel Servo	Tension Arm Position	Offset Signal	Error To Comparator	Comparator Output	Reel Motor Direction	Loop Size Result
	Forward Tape Motion					
UPPER	Down	POS*	NEG	ARM DOWN	Forward	Increase
	Up	POS	POS	ARM UP	Reverse	Decrease
LOWER	Down	NEG	NEG	ARM DOWN	Reverse	Decrease
	Up	NEG*	POS	ARM UP	Forward	Increase
	Reverse Tape Motion					
UPPER	Down	NEG	NEG	ARM DOWN	Forward	Increase
	Up	NEG*	POS	ARM UP	Reverse	Decrease
LOWER	Down	POS*	NEG	ARM DOWN	Reverse	Increase
	Up	POS	POS	ARM UP	Forward	Decrease

* Aids error signal.

6.5.4.2 Ramp Generator (Figure 6-12) – The error signal feeds the inverting input on the ARM DOWN comparator, and the noninverting input on the ARM UP comparator. The noninverting input of the ARM DOWN comparator feeds the POS RAMP, and the NEG RAMP feeds the inverting input of the ARM UP comparator.

The positive and negative ramps are sychronized to the zero crossing point of the ac input (Figure 6-23). When the error signal exceeds the ramp voltage, the output of the comparator is asserted. An error signal exceeding the positive ramp asserts ARM DOWN, and an error signal exceeding the negative ramp will assert ARM UP. Thus the relationship between the error signal and the ramps determine how long the ARM UP or ARM DOWN signal is asserted during each half cycle of the ac input.

Notice that the zero crossing detector generates LATCH RST every time the ac input crosses zero.

6.5.4.3 Reel Motor Control – Each latch provides the input to an optically isolated SCR. When the latch is set, the SCR conducts turning on its associated TRIAC. The TRIAC supplies power to the reel motor. Thus the direction of the transducer error signal determines direction of the reel motor by turning on the forward or reverse TRIAC; and the magnitude of the error signal determines reel motor torque by determining the duration of TRIAC conduction.

6.5.4.4 Reel Motor On (Figure 6-12) – The REEL MTR ON signal from the capstan servo board resets the latches on the reel servo board, and triggers the reel brake SCR applying power to the brakes in order to release them. The REEL MTR ON signal is disabled by DC LO or by any of the tension arm limit switches being closed.

6.6 TAPE DATA HANDLING

This three-part section talks about transferring data to and from tape.

1. The read function describes how data flows from the read heads to the PE formatter.

2. The PE formatter function describes how read data flows through the I/O section via the μP.

3. The write function describes how data flows from the I/O section to the write heads, via the μP, and how the read after write function works.

6.6.1 Read Function

Figure 6-25 is a simplified diagram of the read function and is referenced throughout this description.

6.6.1.1 Read Preamplifiers – Each of the nine read heads connects to a two-stage read preamplifier. (These preamps are shown in the upper left of Figure 6-25.) The preamps provide maximum flux reversals per inch (frpi) gain at a frequency bandwidth that is equivalent to 1600 to 3200. The nominal PE signal from the read heads is 6 mV p-p. The maximum signal output from the preamps is 16 V p-p and 10 V p-p during preamble/postamble. Each of the nine preamps has a gain adjustment potentiometer. Test points are provided on the G057 read preamplifier board and the motherboard for each output signal.

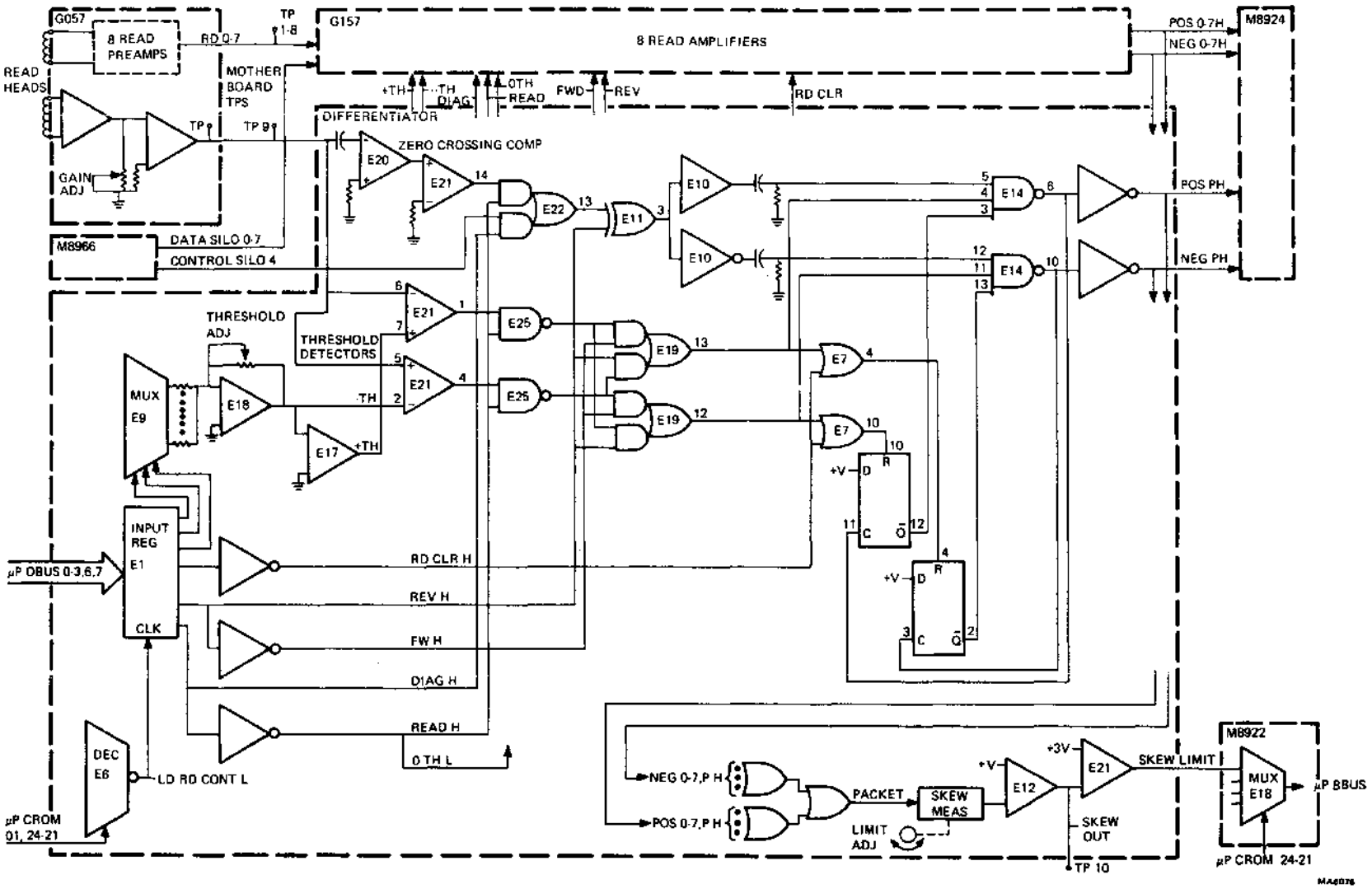


Figure 6-25 Read Function

6.6.1.2 Read Amplifiers – The outputs of the nine read preamps connect to nine read amplifiers, four on each of two G157 boards and one on the M8923 board. M8923 also contains read control circuits common to all nine amplifiers. Each amplifier circuit is the same, so only the parity track amplifier on M8923 is described. M8923 is shown in the central portion of Figure 6-25.

The signal RD P connects to a peak detector consisting of an active differentiator E20 and a zero crossing comparator E21 (output pin 14); and to +TH threshold detector E21 (ouput pin 1) and –TH threshold detector E21 (output pin 2).

The peak detector output signal at E21-14 changes when the direction of the input signal RD P reverses (Figure 6-26). This signal is ANDed with the READ signal at the input to E22, and fed to exclusive-OR E11. This gate complements the output of E22 when the tape is moving in the reverse direction. (Compare Figures 6-26 and 6-27.) On Figure 6-27, asterisks denote significant signal differences compared to the forward direction. The ouputs of E10 are differentiated to provide sharply defined read pulses to both NAND gates E14; noninverted at pin 5 and inverted at pin 12.

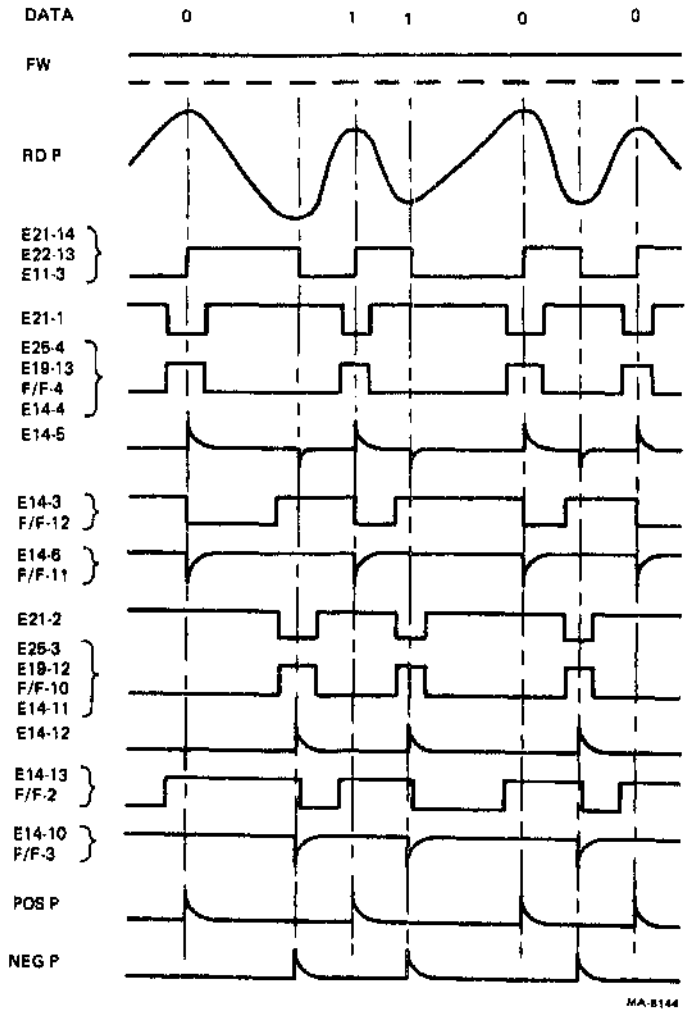


Figure 6-26 Forward Signal

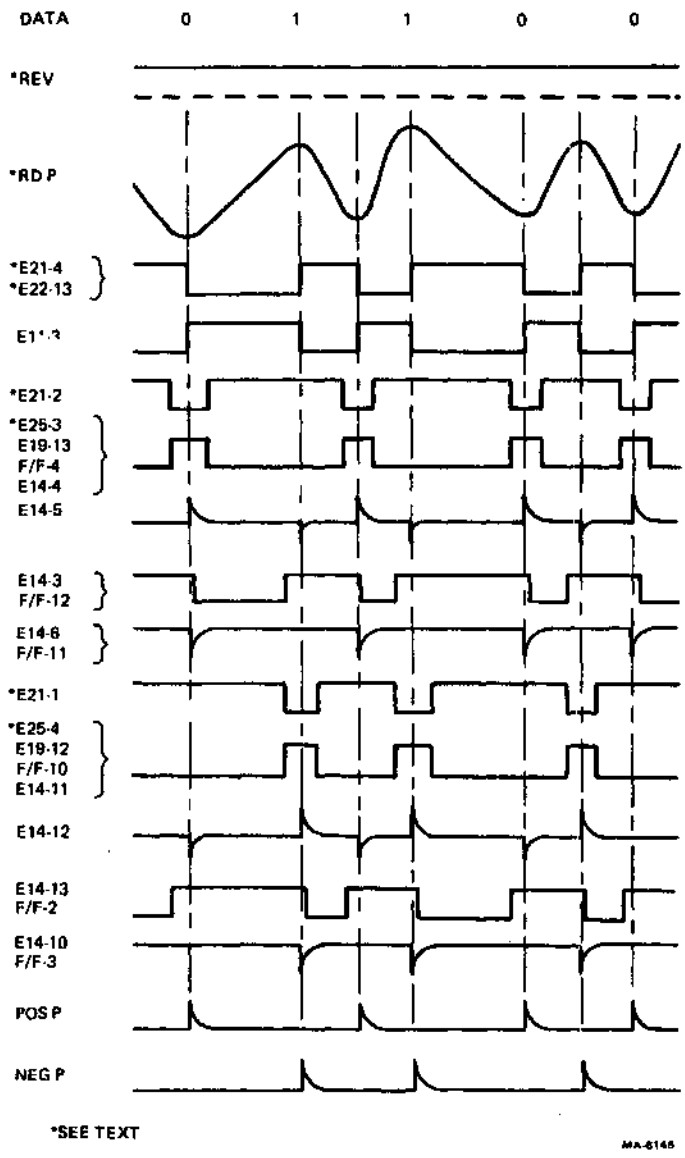


Figure 6-27 Reverse Signal

Look at the two threshold detectors E21 (output pins 1 and 2). RD P on the inverting input (pin 6) is compared to the positive threshold +TH on pin 7 of the top detector. If the positive going half of RD P is of sufficient amplitude to overcome +TH, a negative gating signal, that straddles the detected peak of RD P, is produced at the output E21-1. The gating signal is ANDed with the READ signal and inverted by E25 (output pin 4).

Similarly, the negative half of RD P is compared to −TH, and, if more negative than the threshold, a negative gating signal is produced at E21, pin 2. The gating signal is ANDed with the READ signal and inverted by E25 (ouput pin 3).

Note that because RD P is applied to the inverting input (pin 6) in the first case, both positive and negative transitions of RD P result in negative gating signals straddling the peaks of RD P, at E21 pins 1 and 2 (Figure 6-26).

The gating signals from E25-4 and E25-3 are ANDed with either the FW or REV signal through both halves of E19. The operation of E19 is such that in the forward direction (FW high), the gating signal from E25-4 is gated through to E14-4; and the gating signal from E25-3 is gated through to E14-11. When REV is high the action is reversed: the gating signal from E25-4 shows up at E14-11, while the signal from E25-3 is fed to E14-4. The signal through E11 is complemented when REV is high, and appears at E14-12 as a sharply defined positive going read pulse (Figures 6-26 and 6-27).

The outputs of E19 (pins 13 and 12) are also ORed with the RD CLR signal on the direct reset input of two flip-flops. When RD CLR is low, the operation of the flip-flops makes sure that POS P outputs are alternated with NEG P outputs. For example, if the left flip-flop is reset and the right flip-flop is set, E14-3 will be high and E14-13 low. A positive transition of RD P in the forward direction (FW high) will result in a high gating signal at E19-13. This makes E14-4 high, and resets the right flip-flop making E14-13 high. The positive transition of RD P also causes a positive pulse at E14-5, which is gated through E14, appearing as a negative pulse at pin 6. The trailing edge (positive transition) of this pulse sets the left flip-flop, making E14-3 low, and inhibiting this (POS P) leg. It is not enabled again until a negative transition of RD P occurs, and its associated gating signal resets the left flip-flop. Figures 6-26 through 6-29 show operation of the flip-flops. The flip-flops block the effect of spurious signals induced by tape noise, as shown in Figure 6-28. Note that the negative transition of RD P leading into the spurious signal, is not negative enough to overcome −TH, and does not produce a gating signal.

RD CLR may be asserted under microcode control to defeat the noise filtering function of the flip-flops.

Figure 6-29 shown the effects of a read signal too low to overcome the threshold. Note that a missing bit creates a dead track situation, and the remaining data in that track is ignored. (More information on detecting dead tracks is provided in Paragraph 6.6, PE Formatter).

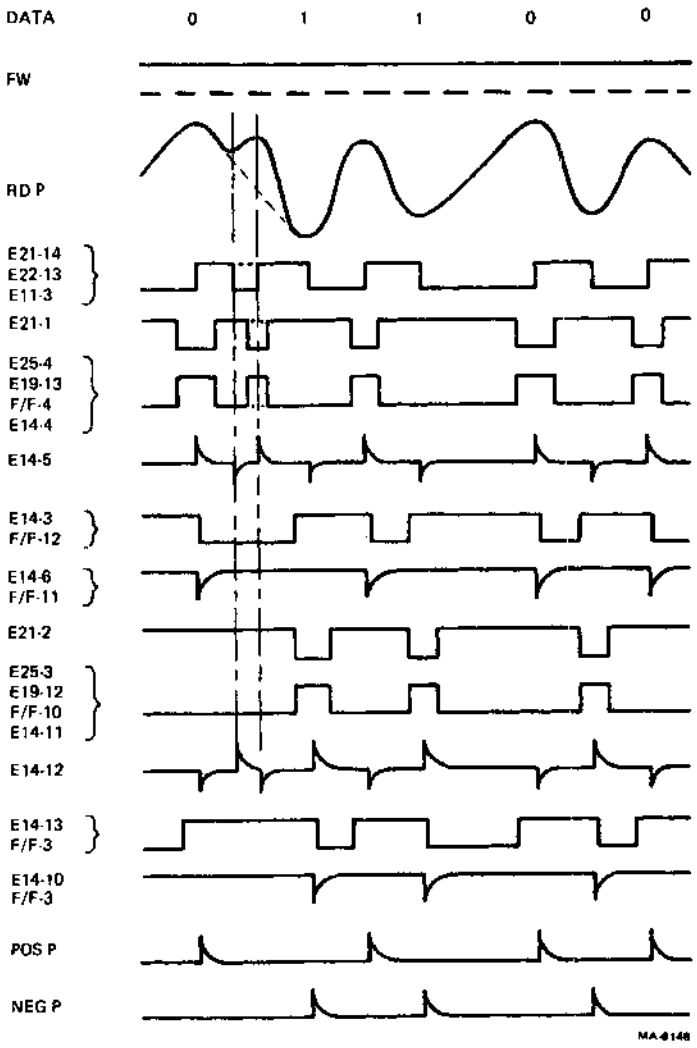


Figure 6-28 Spurious Signal

6.6.1.3 Read Control – The threshold generator is shown in the lower left of Figure 6-25. The threshold levels +TH and −TH are selected by the main μP via INPUT REG E1 and a D/A converter. The D/A converter consists of multiplexer MUX E9 and a resistor ladder on its output. The output of the D/A converter feeds amplifier E18 to produce −TH. Inverting −TH through amplifier E17 generates +TH. A potentiometer is provided to fine tune the thresholds.

INPUT REG E1 is loaded from the μP OBUS by the trailing edge (positive transition) of LD RD CONT L. LD RD CONT L is asserted by decoder DEC E6 when μP CROM 01,24-21 = 20.

Refer to Table 6-14 for threshold levels and their uses.

Note that when the DIAG signal is high, the data input to E22 comes from control silo 4 (Data Silo 0-7 for the other read amplifiers) on M8966.

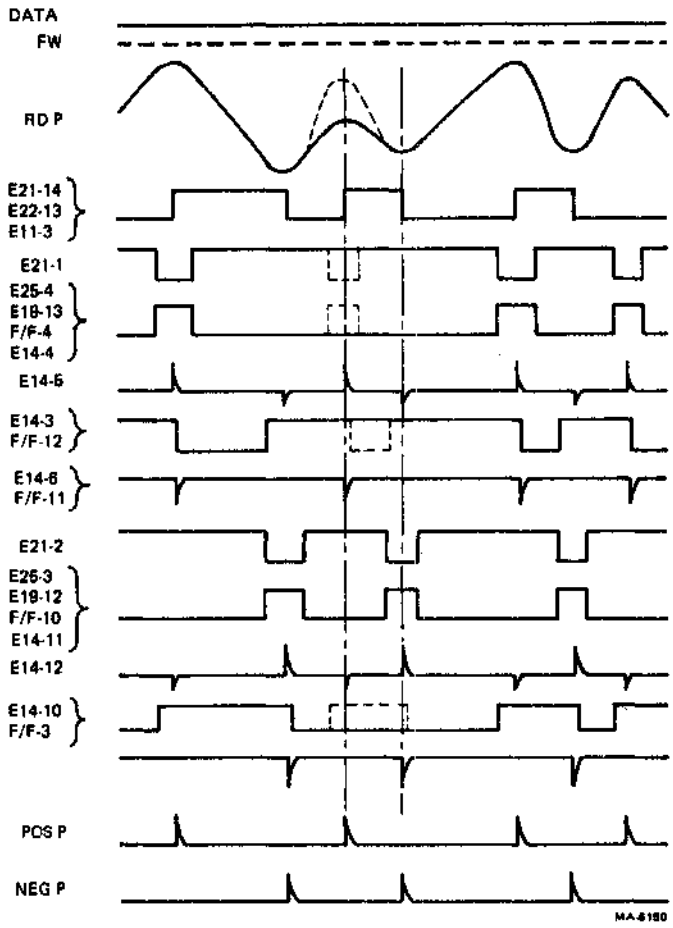


Figure 6-29 Low Signal

Table 6-14 Threshold Levels

Decoded Level	Percentage of Nominal Tape Signal	Normal Operation	Diagnostic Check
7	120	–	Maximum preamp gain
6	80	–	Minimum preamp gain
5	54	–	Residual erase
4	60	–	Forward/reserve amp balance
3	40	–	
2	20	PE Write*	–
1	12	PE Read	Read/write crosstalk
0	7	PE Error Recovery†	Erase function

* Read after write
† Data portion only

The PACKET signal is the inclusive-OR of all read pulses and reflects gap scatter, jitter, and skew. This signal is fed to the skew measuring circuits (lower right of Figure 6-25). The SKEW MEAS circuit measures the time between the arrival of the first pulse and the last pulse for one frame, and converts that time to an analog signal SKEW OUT. The amplitude of SKEW OUT is proportional to the time between the first and last pulse. SKEW OUT is also fed to comparator E21 where it is compared to a reference voltage. If the time between the first and last pulse is great enough, SKEW OUT will reach an amplitude that exceeds the reference level and signal SKEW LIMIT will be asserted. SKEW LIMIT is an input to multiplexer MUX E18 on M8922. SKEW LIMIT asserts μP BBUS when μP CROM 24-21 = 07.

6.6.1.4 Outputs – The outputs of the nine read amplifiers, POS 0-7, P and NEG 0-7, P are connected in groups of three to three M8924 boards. The M8924 boards and the M8922 board make up the PE formatter. This is where the read signals are deskewed and decoded into tape marks, preamble, postamble, and data.

6.6.2 PE Formatter

The PE formatter includes four circuit boards: three M8924 boards and one M8922 board. Each M8924 contains data tracking and detection logic for three tracks. The three M8924 boards thus have a capacity of nine tracks. The M8922 board contains control circuits which are common to all nine channels.

The remainder of this section uses block diagrams and timing diagrams to describe VCO operation, data tracking and detection, deskew buffer and ROM look-up table operation, and the overall read operation.

6.6.2.1 VCO Operation – The VCO is part of a phase locked loop (PLL) that synchronizes the data detection circuits to the incoming data. The frequency of the VCO will increase or decrease to follow changes in the frequency of data coming from the tape due to minor variations in tape speed or bit density. For the following description of VCO operation, refer to Figure 6-30.

The VCO takes its inputs from the FMT MAJOR STATE REG, and tracks 4 and 5 (parity and bit 5) data detection circuits. The VCO output is sent to all three M8924 boards.

The nominal frequency of the VCO is 64 times the data frequency. (64 × 1600 bits/in × 45 in/s = 4.6 MHz) This frequency will vary with tape speed and with minor changes in the recording density. Tape speed may not be a constant 45 in/s and bit density may not be exactly 1600 bits/in.

The VCO becomes a reference for the data detection circuits on the M8924 modules. Even though the incoming data rate changes, the reference (VCO output) changes along with it.

The operating mode of the VCO is controlled by the FMT MAJOR STATE REG. When VCO SYNC is not set, the VCO runs at the nominal frequency (4.6 MHz) determined by the frequency adjustment potentiometer. When VCO SYNC is set, the VCO output will follow the data frequency from the tape.

Two frames after VCO SYNC is set, the divide by 64 counter is enabled and the AMP will start following the input from the phase comparator. This two frame delay is caused by the delay shift register. While VCO SYNC is reset, a constant clear is applied to the delay shift register. When VCO SYNC is set, this clear is removed and WIND 5 H is allowed to shift 1s into the shift register. (Window generation is discussed Paragraph 6.6.2.2.) When the 1 output of the shift register goes high, the clear input to the divide by 64 counter goes low, as does the input to the phase comparator (PC) disable circuit.

The divide by 64 counter is one input to the phase comparator. The second input is the signal SY PLS H. SY PLS H comes from either VCO STRB 5 or VCO STRB P (track 5 or 4 respectively). Track 5 is normally used as the source for SY PLS H. If track 5 should go dead the SY PLS select circuit will shift to the parity track for the source of SY PLS.

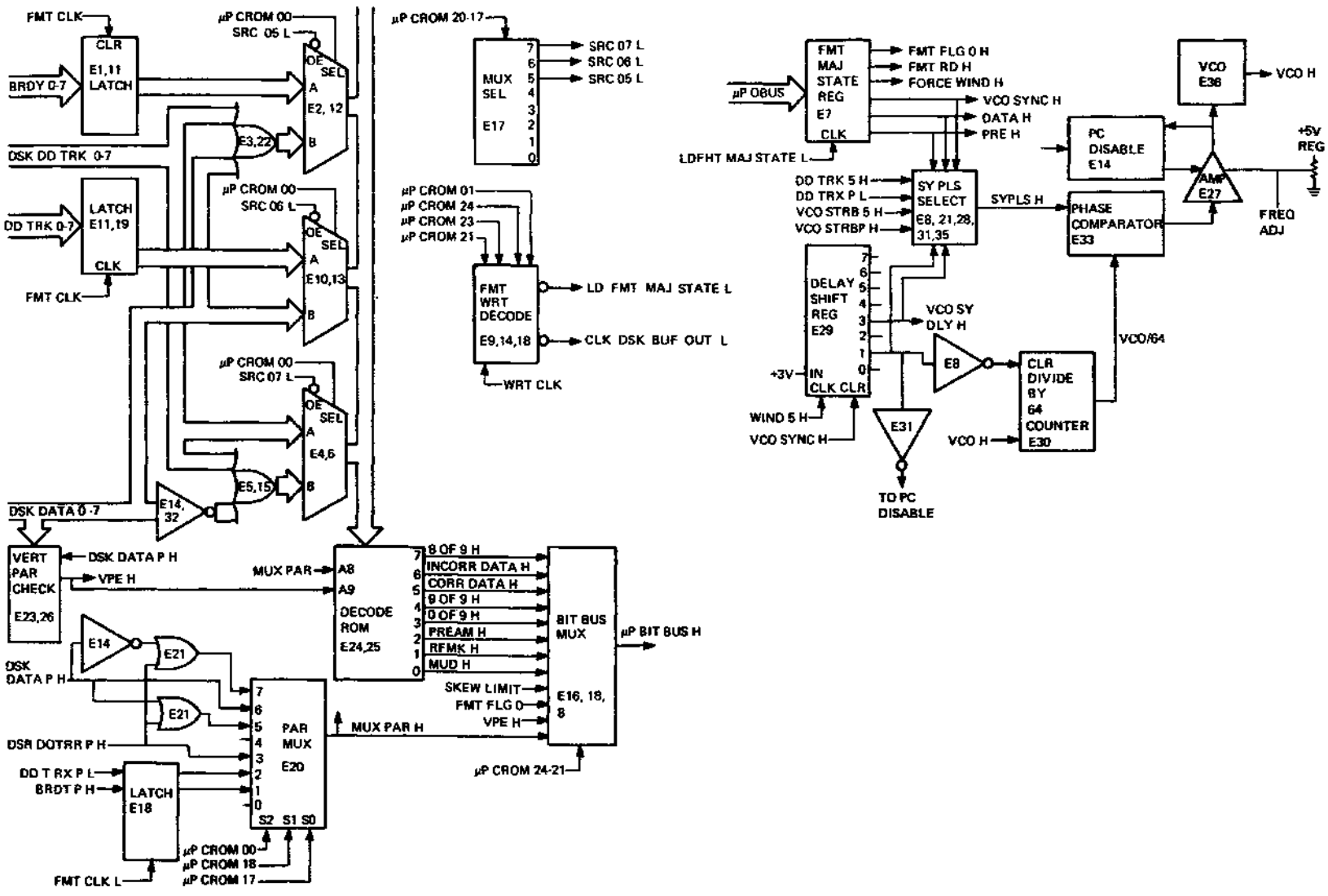


Figure 6-30 VCO Operation

The phase comparator generates a voltage proportional to the phase difference of the low-to-high transitions on its inputs. Any phase difference generates an output which is sent to the AMP as an error signal.

The AMP uses the error signal to modify the static voltage level set up by the frequency adjustment. This modified voltage level is sensed by the VCO and it either increases or decreases its output frequency. This change in VCO frequency is felt by the divide-by-64 counter, bringing its output more nearly into phase with the SY PLS. This causes the phase comparator's output error voltage to decrease.

This process continues until the VCO frequency is 64 times the incoming data rate.

Note that for every change in the data rate there is a corresponding change in the VCO frequency.

6.6.2.2 Data Detection – The data detection circuits are on the M8924 boards. Each track has a data detection circuit of its own. Thus there are three data detection circuits on each M8924. Each data detection circuit contains timing logic (window), a data flip-flop, dead track detection circuits, and a deskew buffer.

The M8924 has some logic that is common to all three channels on the board.

Reading PE data requires the bit cell boundaries to be defined. A transition in the cell center is a data bit. The direction of the transition determines if the bit is a 1 or a 0. Transitions may also be required on the cell boundaries to set up the direction of the transition in the cell center. Therefore, you must be able to distinguish between boundary transitions (phase bits) and data transitions (bit strobes).

Defining the bit cell boundaries is the job of the window circuit. The window circuit splits each bit cell into two parts, a phase half and a data half. Data is detected only during the data half of the bit cell.

Data transition should be received exactly in the center of the window. The time at which the data arrives varies due to speed variations and deviations in the tape path over the heads. To keep the data centered in the window, adjust the window timing. If no transition is detected within the window boundaries, the track is considered dead.

6.6.2.2.1 Window Generation – The following discussion is limited to channel A of an M8924 board, except where logic common to all three channels is discussed (Figure 6-31).

The internal timing logic uses the VCO H signal to produce four internal timing signals. Each of these signals is active on alternate VCO H cycles. Thus, each timing signal is one half the VCO frequency or 32 times the data frequency. (Refer to Figure 6-32 for the timing relationships of these signals.)

The shift register counter defines the timing of the window for detecting data. Assume that the counter is initially clear. The output of counter stage 8 (CT8 H) is low. This signal is inverted (CT8 L) and applied to the input of the counter. Each assertion of TIME 2 H will clock a 1 into the counter until CT8 H goes high. At this point (eight transitions of TIME 2 H) there are eight 1s in the counter. CT8 L goes low and after eight more transitions of TIME 2 H the counter is again all 0s. The entire cycle will repeat until the window must be adjusted.

The window flip-flop toggles each time the counter fills with ones. To adjust the timing of the window, the normal sequence of the counter must be altered. Figure 6-33 shows the normal relationships of the counter, the window signal, and the signals received from the read circuits (M8923 and the two G157 boards).

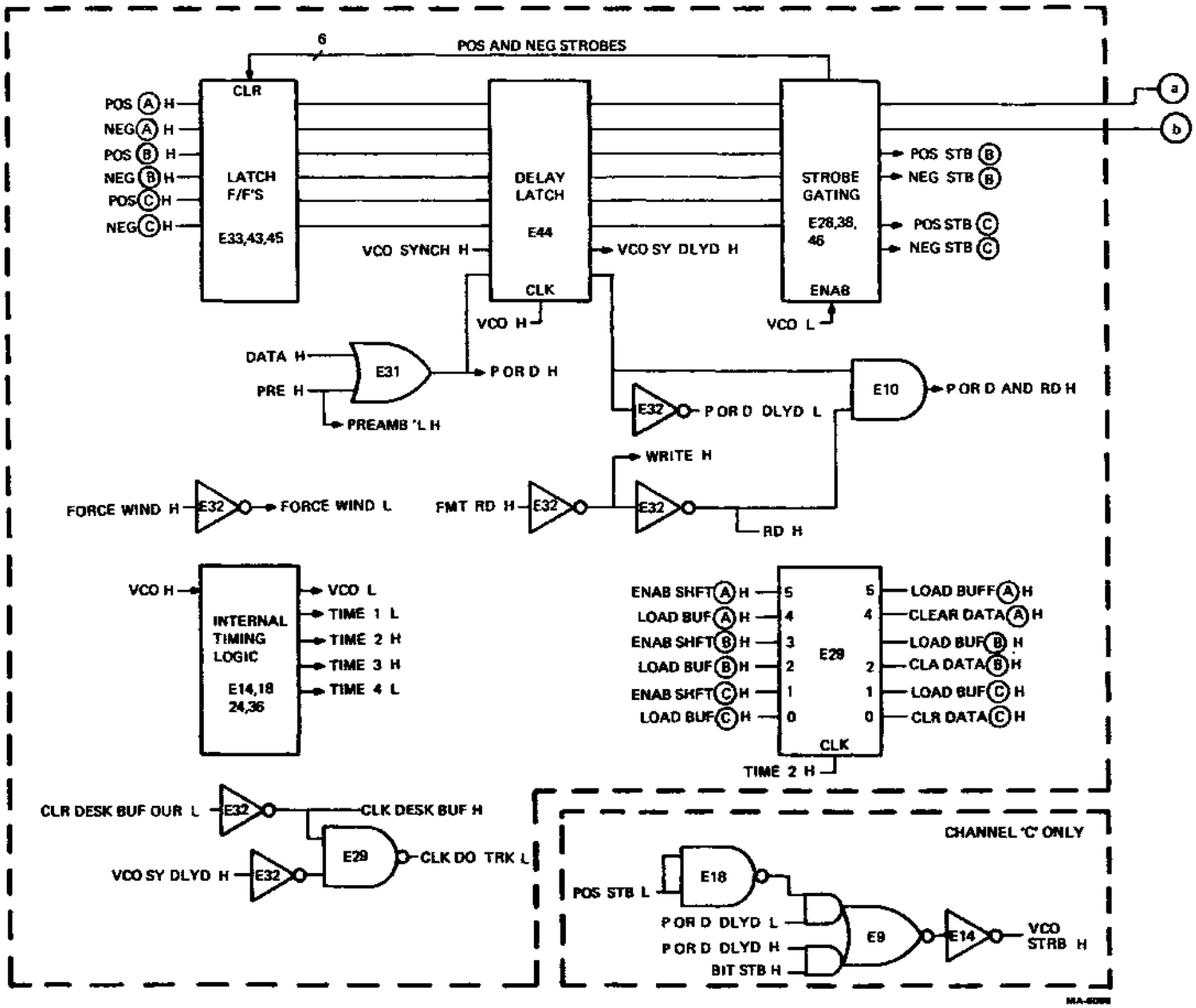


Figure 6-31 Window Generation (Sheet 1 of 2)

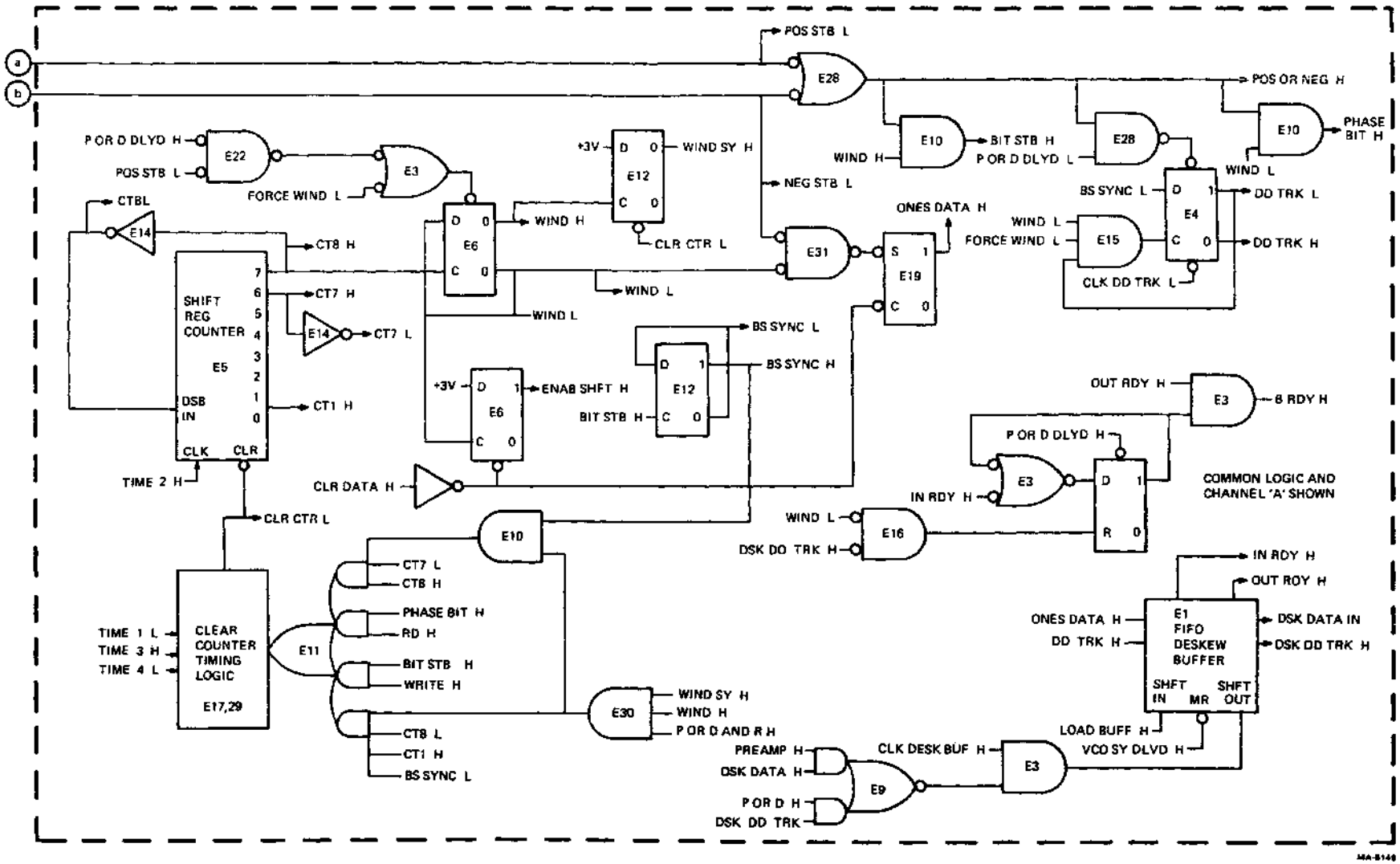


Figure 6-31 Window Generation (Sheet 2 of 2)

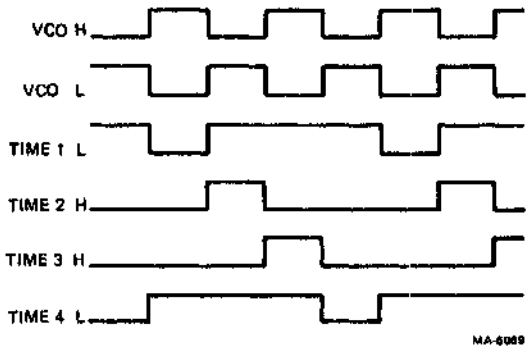


Figure 6-32 Timing Relationships

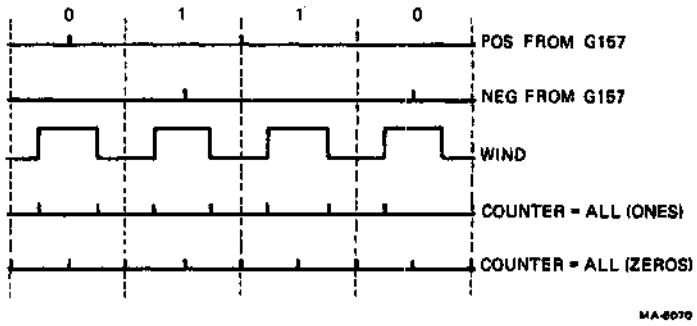


Figure 6-33 Counter-Normal Signal Relationships

Notice that the signals from the read circuits occur when the counter is all 0s. Thus, the all 0s condition of the counter defines both the center of the window and the cell boundaries. Two full cycles of the counter (i.e., 32 counts of TIME 2 H) are used to determine the center and boundaries of each bit cell.

If a POS or NEG signal from the read circuits occurs when the counter is not all 0s, the normal counting cycle is altered. This is done with the clear counter timing logic and the gating which feeds it.

The POS and NEG signals enter the M8924 from the read circuits and latch into the latch flip-flops. On the next VCO H clock, the POS or NEG gates into the delay latch. When VCO L goes high, the signals gate through the strobe gating and out to the channel logic as POS STB L or NEG STB L. These POS or NEG strobes also reset the corresponding latch flip-flop.

The strobes are ORed in the channel logic (E28) and then applied to two AND gates (E10) where they are ANDed with WIND H and WIND L. The outputs of these gates are BIT STB H and PHASE BIT H.

The PHASE BIT H signal is ANDed with the signal RD H and applied to the clear counter timing logic through E11. This signal causes the counter to clear whenever a phase bit is detected during a read. Since a phase bit always occurs on a cell boundary, clearing the counter whenever a phase bit is detected assures that the window occurs at the proper time (eight counts of TIME 2 H after the phase bit).

When the window flip-flop sets (WIND H goes high), its output sets the WIND SY (window sync) flip-flop and causes WIND SY H to go high. The WIND SY flip-flop is cleared whenever the clear counter timing logic clears the counter.

To adjust the window on data rather than phase bits, the top and bottom AND inputs to E11 are used. If the data occurs too early in the window, the top input is used. If the data is late in the window, the bottom input is used. Either of these inputs will cause the counter to reset one count from its normal all 0s time. Thus, data will adjust the window timing 1/32 of a bit cell at a time.

WIND SY H, WIND H, and P or D and R H (preamble or data and read) are enabling signals to AND gate E30. E30 is one signal applied to AND gate E10, which is fed to the top input of E11. The second input to AND gate E10 is BS SYNC H (bit strobe SYNC). The BS SYNC flip-flop is set by BIT STB H. The output from AND gate E10 is ANDed with CT7 L and CT8 H in the top input to E11. If the BS SYNC flip flop is set more than one count before the center of the window (counter = all 0s), then the counter will be cleared when a single 1 remains in the last stage of the counter (CT8 H = high and CT7 L = high). This shortens the normal counting cycle of the counter by one count. Figure 6-34 shows the window adjustment.

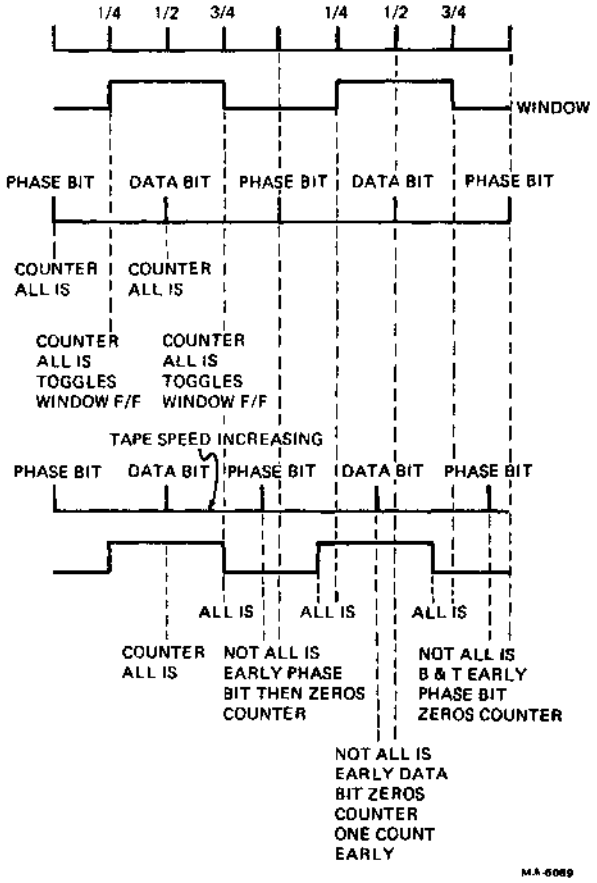


Figure 6-34 Window Adjustment

The bottom input to E11 uses AND gate E30, the reset side of the BS SYNC flip-flop (BS SYNC L), CT8 L, and CT1 H. If the counter counts one count past the center of the window and BS SYNC is not yet set (CT8 L = high, CT1 H = high, BS SYNC L = high), the counter will be cleared. This extends the normal counting cycle by one count.

During read after write operations, the window is adjusted with data. Phase bits are not used to adjust the window on a read after write.

BIT STB H is ANDed with WRITE H (WRITE H is the RD H signal inverted) on the input to E11. A BIT STB will always zero the counter during a read after write.

6.6.2.2.2 Data Sampling – One bits are detected by the ones data flip-flop (E19). NEG STB L and WIND L are ANDed in E31 to set the flip-flop. If the data is a zero (POS STB) then the flip-flop will not be set. The output of the flip-flop (ONES DATA H) is applied to the input of the FIFO deskew buffer.

Data is clocked into the deskew buffer by the LOAD BUFF signal. LOAD BUFF is generated by ENAB SHFT H. The ENAB SHFT flip-flop is set by the low-to-high transition of WIND L (that is, on the trailing edge of the data window). On the next transition of TIME 2 H, the ENAB SHFT H signal is clocked into a latch (E21). The output of the latch is LOAD BUFF H.

LOAD BUFF H is also looped around to the input of the latch and, on the next TIME 2 H, will be output as CLR DATA. The CLR DATA H signal is inverted and sent to the reset inputs of the ENAB SHFT flip-flop, the BS SYNC flip-flop, and the ones data flip-flop.

6.6.2.2.3 Dead Track Flip-Flop – The dead track flip-flop (sometimes called track active flip-flop) is used in two ways. During the data portion of a record, it detects the absence of a BIT STB during the window. If no BIT STB is detected the flip-flop resets, indicating the track is dead. This flip-flop may also be used as an NRZ detector (not to be confused with 800 bpi NRZ data) which detects transitions regardless of polarity. The output of the dead track flip-flop is sent to M8922 and to the deskew buffer.

The signal FORCE WIND L is asserted when the dead track flip-flop is used as an NRZ detector. FORCE WIND L disables the normal clock input to the dead track flip-flop and causes the window flip-flop to be constantly set. The constantly set condition of the window flip-flop disables most of the channel logic.

The only active inputs to the dead track flip-flop during this time are the direct set and direct reset. P or D DLY'D L will be high, enabling POS or NEG H to directly set the dead track flip-flop. Thus, the dead track flip-flop sets on a transition in either direction.

The dead track flip-flop is reset by the signal CLK DD TRK L. This signal comes from VCO SY DLY'D and CLK DESK BUF. (Both of these signals are under μP control.)

Since the window logic is disabled, the deskew buffer will not be clocked when the dead track flip-flop is used as an NRZ detector. All sampling of the dead track flip-flop must be done by the μP.

In normal operation (when used for detecting dead tracks), the dead track flip-flop sets via the D and C inputs. BS SYNC H connnects to the D input. The C input comes from AND gate E15. This gate has DD TRK L, WIND L, and FORCE WIND L as inputs.

BS SYNC H is asserted when a transition occurs during the window. FORCE WIND L is high. When WIND L goes high, BS SYNC H will be clocked into the flip-flop. If BS SYNC H is high when WIND L goes high, the track is active. If BS SYNC H is low when WIND L goes high, the track is dead and the flip-flop is reset. DD TRK L on the input to AND gate E15 will disable further inputs to the flip-flop once it is reset.

6.6.2.2.4 Deskew Buffer – The deskew buffer is a 64-location FIFO memory identical to the chips which make up the I/O silo (67401s). Each channel has its own deskew buffer. Only two of the four bits in the chip are used; one for data, the other for dead track information. Each M8924 has three deskew buffers.

The deskew buffer's output is controlled by AND gate E3. This gate takes its inputs from CLK DESK BUF H (controlled by μP) and OR gate E9. E9 disables further shifting of data to the buffer output on two conditions.

The first condition that disables shifting data out of the buffer is if preamble is set (controlled by μP) and a 1 appears on the DSK DATA output of the buffer. This permits deskewing the output of all nine channels on the all 1s character at the end of the preamble. Shifting data out is only permitted on those deskew buffers which have not yet seen the one bit of the preamble. The μP continues issuing CLK DESK BUF commands until it sees a 1 on the output of all nine channels. The μP then clears preamble mode and normal shifting resumes.

The other condition that disables shifting the output of the buffer is if preamble or data mode is set and the DSK DD TRK output of the buffer is a 1. Thus, if a dead track is indicated on the output of the buffer during the preamble or data portions of a record, the buffer's output is frozen.

The μP must have a way of determining if data is ready to be shifted out of the buffer. This is accomplished by the BRDY H (buffer ready) signal. This signal is controlled by OUT RDY H from the buffer and the output of flip-flop E4. These signals are ANDed in E3 to generate BRDY H.

Flip-flop E4 is set unless IN RDY H is a low when WIND L goes low. This condition indicates that the buffer is either full or is not functioning correctly. In either case, data is lost because the buffer will not accept more data.

While flip-flop E4 remains set, the BRDY H signal is asserted whenever OUT RDY H is high.

6.6.2.3 Formatter Multiplexers and ROM Look-Up Table (Figure 6-30) – The formatter multiplexers (on M8922) route data from the M8924 boards to the μP IBUS and the ROM look-up table (decode ROM) under μP control. The decode ROM enables the μP to make single instruction decisions about the data from the M8924 boards. This saves a great deal of time for the μP.

There are three multiplexers that route data to the μP IBUS. These multiplexers are addressed by μP CROM 00 and 20 through 17. (Refer to Table 6-4 for addresses and the data that is gated through). Two of the inputs to the multiplexers are latched on M8922 (DD TRK 0 through 7 and BRDY 0 through 7).

There is also a PAR MUX (parity multiplexer) on M8922, which routes data from the parity track to the decode ROM and the bit bus mux. This multiplexer responds to the same addresses as the μP IBUS multiplexers, gating through the same data for the parity track. The PAR MUX will also respond to these addresses minus 4 (that is, with μP CROM bit 19 reset). This allows the parity channel to be addressed separately as well as with the data channels.

The decode ROM is 1024 words $\times$ 8 bits. Addresses 0 through 7 are taken from the μP IBUS. Address line 8 is from the PAR MUX and address line 9 is from the VERT PAR CHECK circuit.

Any address from the ROM asserts one or more of the 8 output bits. Table 6-15 describes the output bits.

Table 6-15 ROM Look-Up Configurations

Output	Addresses that assert*
	AAAAAAAAAA 9 8 7 6 5 4 3 2 1 0
MUD	XDDDDDDDDD
RFMK	XXX0100X11 X110X001XX
PREAM	XAACBCCABB†
9 OF 9	X111111111
0 OF 9	X000000000
CORR DATA	1000000001 1000000010 1000000100 1000001000 1000010000 1000100000 1001000000 1010000000
INCOR DATA	1000000000
8 OF 9	X111111111 X111111110 X111111101 X111111011 X111110111 X111101111 X111011111 X110111111 X101111111 X011111111

D = 2 or more of 0, X = do not care

* A0–A7 = Mux 2^0–2^7, A8 = Mux Parity, A9 = Latched Parity Error

† Must have at least one of A, B, and C.
Must have all of A, B, or C.

The output of the ROM is sent to the bit bus mux along with four separate lines. These separate lines are Vertical Parity Error (VPE H), multiplexed parity (MUX PAR H), skew limit (from M8923), and flag bit from the format major state register (FMT FLG 0 H). The bit bus mux is addressed by μP CROM 24 through 21.

Typically, the μP will route data from the M8924 boards through one of the multiplexers (addressed by μP CROM 20 through 17) to the μP IBUS. At the same time, the bit bus mux will select (via μP CROM 24 through 21) one of the lines on its input and gate it through to the μP bit bus. The μP will jump if the bit it is testing is asserted.

This allows the μP to make many decisions based on the data from the M8924s in a relatively short time (i.e., each decision requires only one conditional jump instruction).

The μP may also examine the data by addressing the appropriate multiplexer during a register read rather than a conditional jump operation. The μP will usually make a series of decisions about the data and then take the data and do something with it (send the data to the I/O, etc.).

6.6.2.4 Read Operation – This section is an overview of the read operation. It is not intended to be an exact step-by-step breakdown of all the things which happen during the operation.

The read operation involves record recognition, VCO sync-up, deskewing the data on the preamble 1s character, checking the data for errors, correction of errors, data transfer to the I/O section, and recognition of postamble/end of record.

After receiving the read command packet from the system CPU, the μP will set up the I/O section and start tape motion. When tape is moving the μP starts searching for the beginning of the record to be read.

To recognize a record, the μP sets NRZ mode (set the force wind bit in the FMT MAJ STATE register). This causes the dead track flip-flops to act as NRZ detection circuits. The μP monitors the dead track lines via the decode ROM and the μP bit bus using conditional jumps. Each time the output from the dead track flip-flops looks like a preamble, the μP increments an internal count and then resets the flip-flops.

When a sufficient number of frames which look like a preamble have been detected, the μP resets force wind and sets VCO SYNC and FMT RD in the FMT MAJ STATE register. This causes the VCO to synchronize with the data from the tape. The μP allows about 20 frames for the VCO to synchronize. During VCO synchronization, the channel logic will also be adjusting the data windows. After the synchronizing period, the μP will clear out the deskew buffers (during sync up the deskew buffers may fill with bad data) and then set the PRE bit in the FMT MAJ STATE register.

At this point the VCO should be in sync with the data and the channel window logic should have the data windows properly positioned. The FMT MAJ STATE register will have the VCO SYNC, FMT RD, and PRE bits set. The μP will start sampling the output of the deskew buffers looking for the preamble all 1s character. Each time nine of nine BRDYs occur, the μP clocks the buffer outputs. When nine of nine DSK DATA lines are true, the μP sets the DATA bit and resets the PRE bit in the FMT MAJ STATE register.

The μP will start checking the deskewed data from the buffers for errors, using the decode ROM and conditional jumps. If the data has no errors, the μP transfers it to the I/O section where it is sent to the system memory. The μP also checks the data to see if it looks like a postamble. If the data is in error but is correctable (bad parity and one dead track) the μP corrects the data, sends it to the I/O section, and sets a flag (this flag shows up in XSTAT 1 in the message buffer). If the data has an incorrectable error (parity error and no dead tracks), the μP sets a fatal error.

When the μP detects the postamble, it checks to make sure that the postamble is neither too long nor too short. It then decelerates the capstan to the center of the interrecord gap and sends the message packet to the CPU.

6.6.3 Write Function (Figure 6-35)

This section describes the write function.

6.6.3.1 Control and Data Silo – The write function has two modes of operation. The first, for writing data, is phase encoded (PE); the second, for writing ID bursts (IDB) and tape marks, is referred to as NRZ. In either mode data for tracks 1 through 3 and 5 through 8 comes from data silo 0 through 7 and data for the parity track (track 4) comes from control silo 4 on the M8966 board (upper-left of Figure 6-35).

In PE mode, control silo 4 is the calculated parity bit, based on the 8 data bits. Control silo 3, (the LRCC ENAB bit) and control silo 5 (the NRZ bit) are both cleared by the main μP.

In NRZ mode, all the data and control silo bits are directly controlled by the main μP. For writing an IDB the data silo bits are cleared, control silo 4 is filled with alternate 1s and 0s, control silo 3 is cleared, and control silo 5 is set. To write tape marks, data silo 0,1,2,5,7 and control silo 4 are filled with 1s, control silo 5 is set, and control silo 3 and the rest of the data silo bits are cleared. The main μP also updates control silo bit 7 (silo parity). The control and data silo are described in more detail in the section on I/O function description.

Data is strobed out of the silos by signal WRT BD REQ SILO L from the M8929 (Paragraph 6.6.3.2).

6.6.3.2 Write Control – The Write Control register (E7) (lower-left of Figure 6-35 is loaded from μP OBUS 0 through 5 when μP CROM 01,24-21 = 01. For most normal write operations in either mode, WRT ENAB, 144 KHz EN, HEAD ENAB and ERASE ENAB are selected. MAINT WRT is not implemented in current microcode.

In addition to the signals controlling the write logic, a switched voltage supply, + VSW, provides power to the write and erase heads. (Refer to the lower-right of Figure 6-35). When a reel containing a write-enable ring is mounted, the WRL SOLENOID plunger is pressed, closing the WRL SWITCH, and the + VSW SUPPLY is turned on. + VSW is applied to the WRITE HEAD and ERASE HEAD amplifiers, and to the WRL SOLENOID control amplifier. When the REEL MTR ON signal from the capstan servo board G159 goes high, the WRL SOLENOID amplifier is switched on, energizing the solenoid, retracting the plunger further (and keeping the WRL SWITCH closed) to eliminate drag on the write-enable ring.

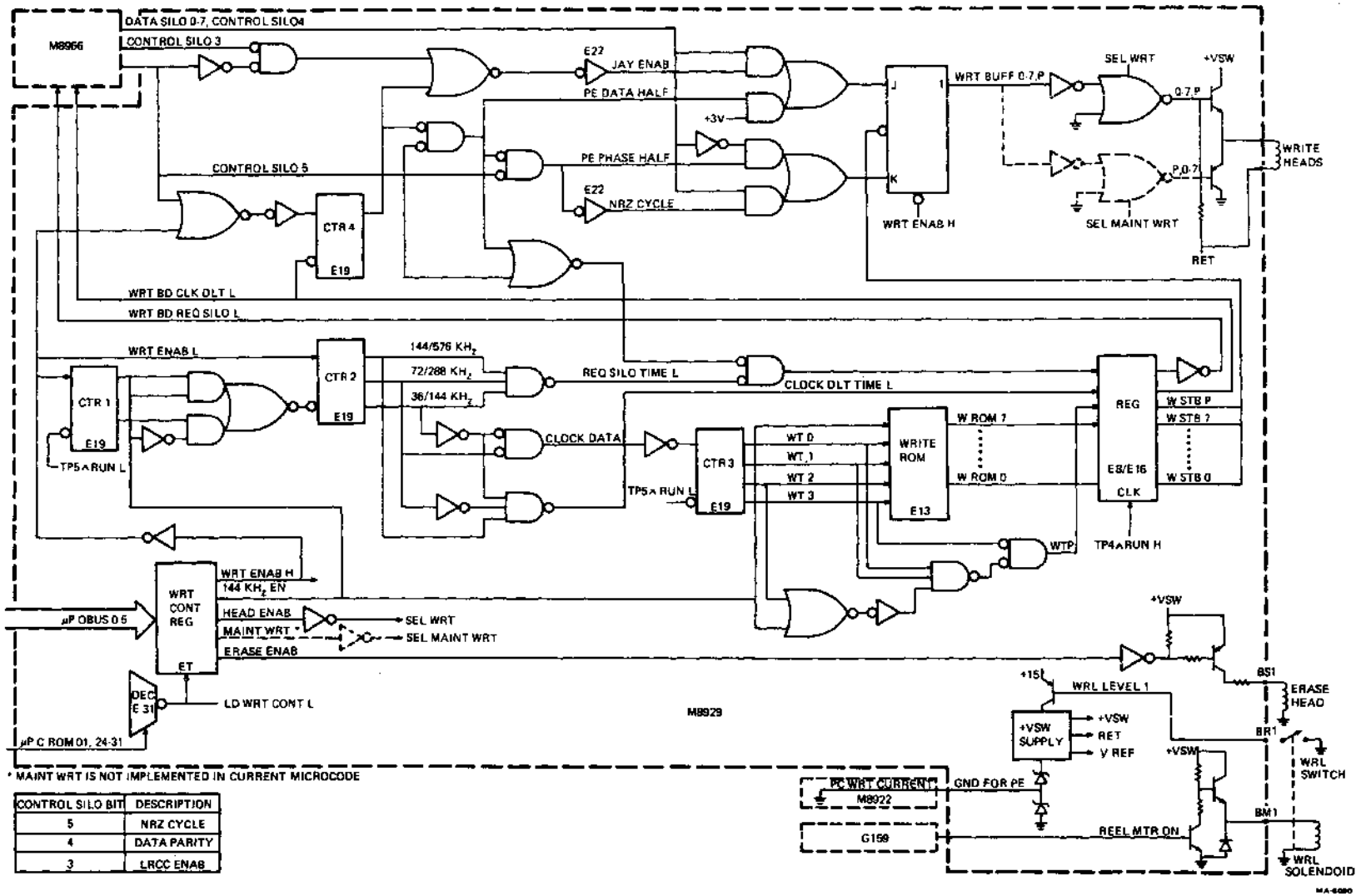
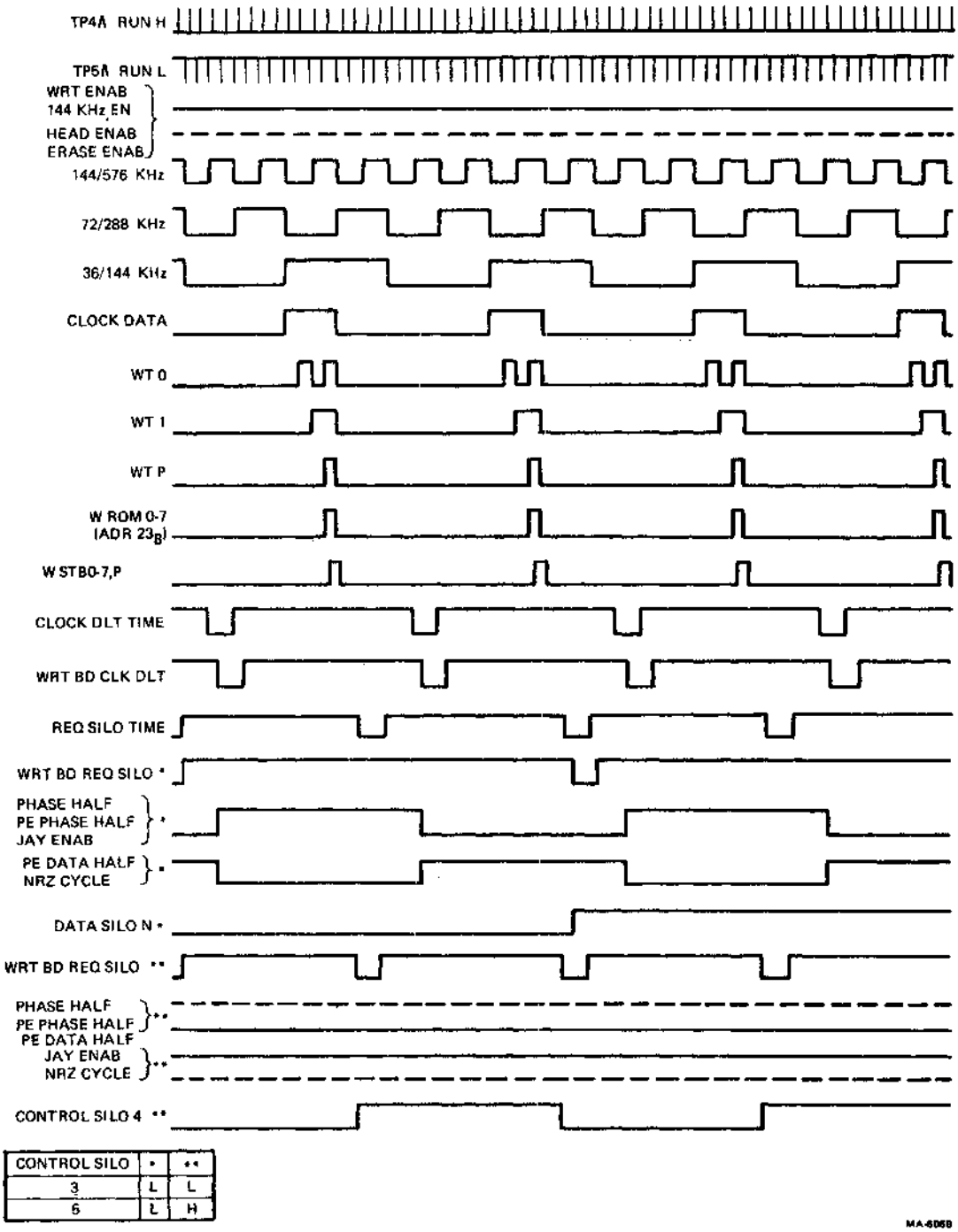


Figure 6-35 Write Function

6.6.3.3 Data Write Operation – Timing for write operations is shown in Figure 6-36. Operation of the WRT BUFF flip-flops is shown in Figures 6-37 through 6-40.



CONTROL SILO	*	**
3	L	L
6	L	H

Figure 6-36 Write Function Timing

Refer to Figures 6-35 and 6-36. Basic timing for the write function is supplied by TP4/RUN H and TP5/RUN L. These are 2.3 MHz clocks offset from each other by approximately 145 ns. Binary counter CTR 1 divides TP5/RUN into 1152 KHz and 288 KHz clocks. When 144 KHz EN is high, binary counter CTR 2 divides the 1152 KHz clock into 576 KHz, 288 KHz, and 144 KHz signals. These three signals from CTR 2 are then used to derive CLOCK DATA, REQ SILO TIME, and CLOCK DLT TIME.

When CLOCK DATA is high, binary counter CTR 3 is enabled and counts TP5/RUN ticks to produce write timing signals WT0 and WT1. (The counter is reset by CLOCK DATA L before producing WT2 and WT3.) WT0 and WT1 are the two LSBs of address for the WRITE ROM. The 144 KHz EN signal is the MSB of the ROM address. The WRITE ROM is blasted so that address 23 (octal) contains all 1s (addresses 20 through 22 are all 0s). Thus when the count in CTR 3 reaches 3, W ROM 7 through W ROM 0 are all high. At the same time WTP is high. The outputs of the WRITE ROM and WTP are clocked into register REG E8/E16 by TP4/RUN to form the strobes W STB P and W STB 7 through W STB 0 for the write buffer JK flip-flops.

Notice that CLOCK DATA, and therefore the write strobes, are asserted at the 144 KHz rate. This corresponds to 3200 frpi at 45 in/s (3200 × 45), the maximum rate of flux changes for PE recording.

Signal CLOCK DLT TIME is clocked through REG E8/E16 and becomes WRT BD CLK DLT. It is fed to M8966 and also clocks binary counter CTR 4. On M8966, WRT BD CLK DLT is compared with the silo output ready signal (ANDed with SOR L). If the the silo output ready signal is not high when WRT BD CLK DLT L is asserted, a data late error signal (DLT ERR) is asserted.

On M8929, when WRT ENAB is asserted and CONTROL SILO 5 is low (data write), CTR 4 divides WRT BD CLK DLT by two. Signals JAY ENABLE, PE DATA HALF, PE PHASE HALF, and NRZ CYCLE are alternately high and low (Figure 6-36).

To see the operation of the write buffer flip-flops, refer to Figure 6-37. Keep in mind that the JK flip-flops will toggle if strobed with both J and K inputs high, and will not change if strobed when both inputs are low. The dominant signal states are indicated in boldface.

Data is read out of the silos by signal WRT BD REQ SILO L. This signal, from REG E8/E16, is asserted by REQ SILO TIME during the time that PE DATA HALF is asserted.

6.6.3.4 IDB and Tape Mark Write – When an identification burst or tape mark is to be written, the main μP writes both the data and control silos. Control silo bit 5, the NRZ cycle bit, is set and alters the operation of the phase half and data half signals which control operation of the write buffer flip-flops. Control silo 5 high also causes the timing of the WRT BD REQ SILO signal to be altered.

Refer to Figure 6-35. When CONTROL SILO 5 is high, CTR 4 in the upper left is disabled. CONTROL SILO 3 is not set, so that JAY ENABLE is high. PE DATA HALF is low. PE PHASE HALF is low, making NRZ CYCLE HIGH. WRT BD REQ SILO from REG E8/E16 will now follow REQ SILO TIME. This means that data is read from the silos at twice the rate that it is read during a data write. The timing differences are shown at the bottom of Figure 6-36.

For an IDB burst, CONTROL SILO 4 is alternately 1 and 0. Because of the doubled data rate, the input to write buffer flip-flop WRT BUFF P is high when one write strobe arrives, and low when the next arrives. Consequently, WRT BUFF P changes state with every other write strobe (Figure 6-38). All the data silo bits are 0 and the other write buffer flip-flops do not change (Figure 6-40). Flux on track 4 is reversed at half the write strobe rate, or 1600 frpi.

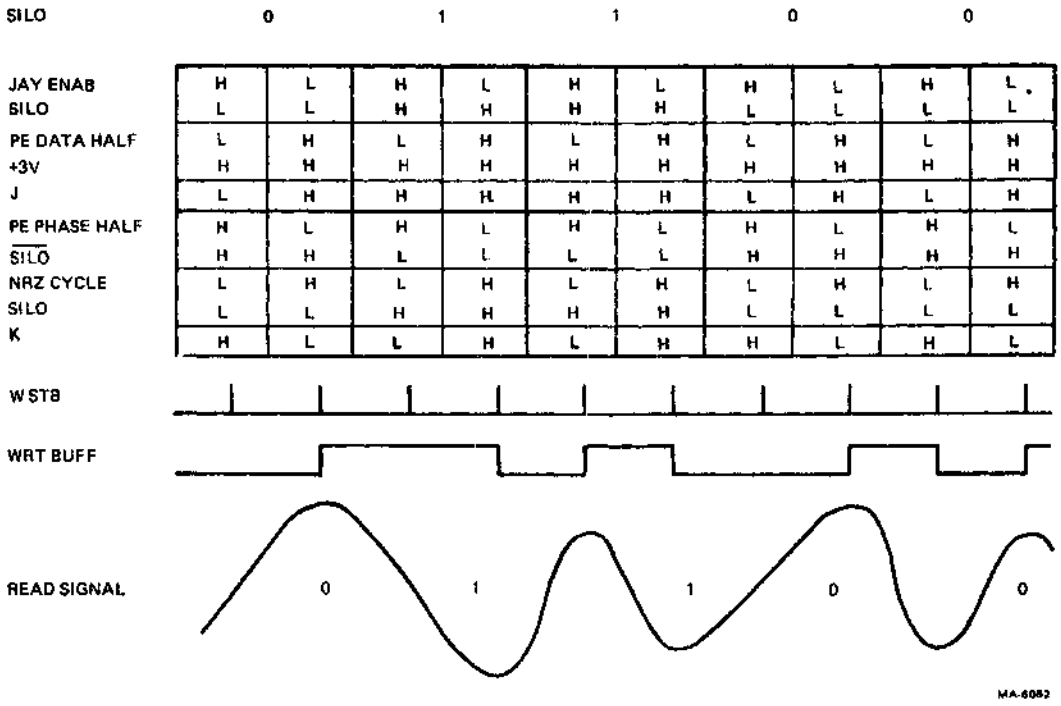


Figure 6-37 Write Data – Track n

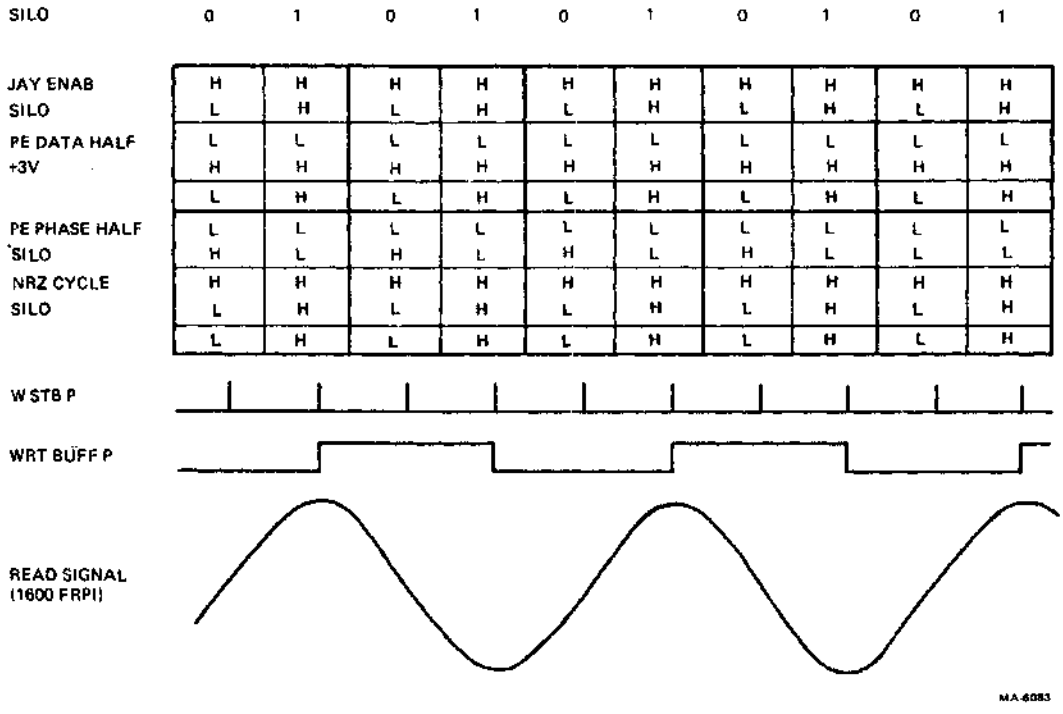


Figure 6-38 Write IDB – Track 4

When a tape mark is to be written, data silo 1, 2, 5, 7, and 8, and control silo 4 are set. Data silo 3, 6 and 9 are cleared. Therefore, the data inputs to WRT BUFF 1, 2, 5, 7, 8, and P flip-flops are high when each write strobe arrives, and the flip-flops change state with each strobe. WRT BUFF 3, 6 and 9 do not change. Flux reverses on tracks 1, 2, 4, 5, 7 and 8 at the same rate as the write strobe, or 3200 frpi (Figures 6-39 and 6-40).

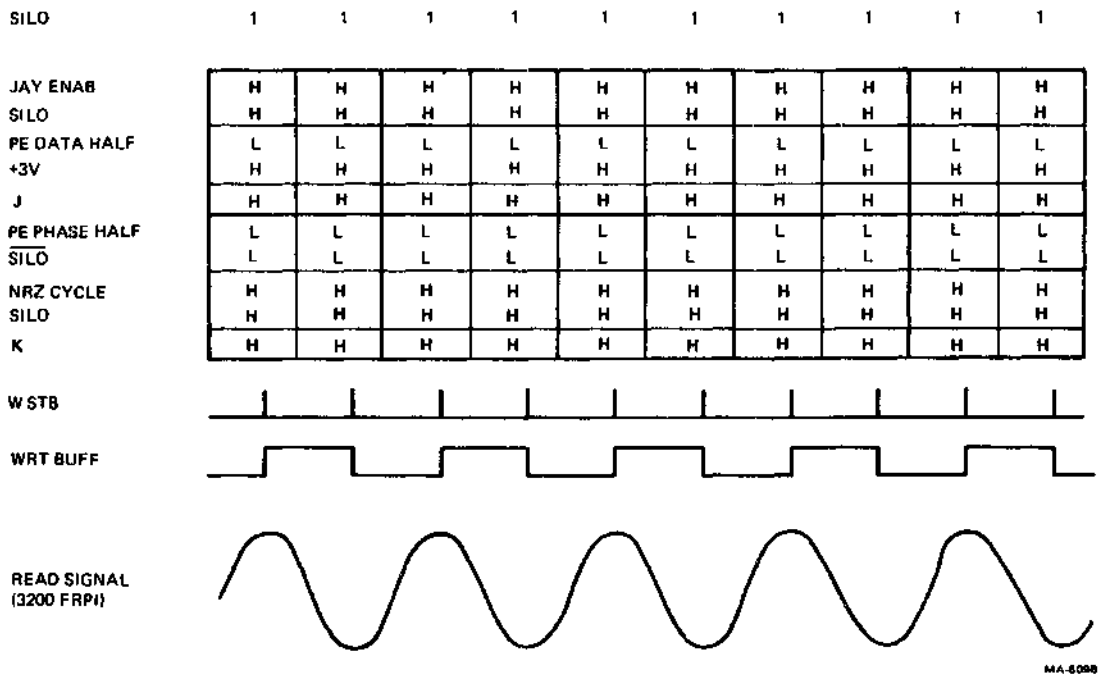


Figure 6-39 Write Tape Mark - Tracks 1, 2, 4, 5, 7, 8

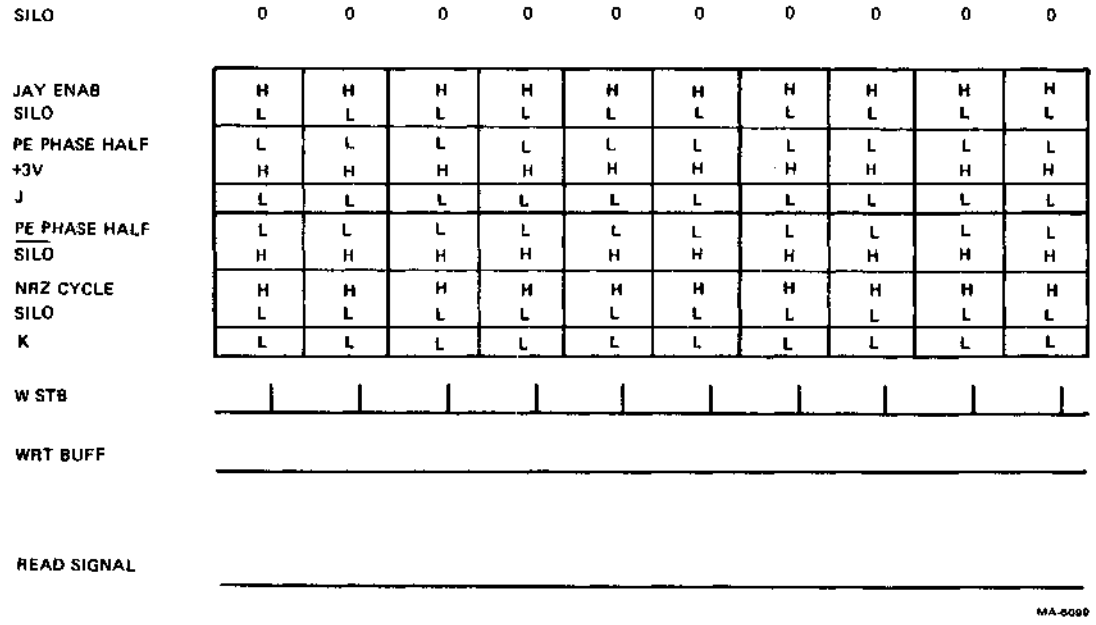


Figure 6-40 IDB and Tape Mark - Unwritten Tracks

6.6.3.5 Read After Write – Read after write is the same as a normal read (Paragraphs 6.6.1 and 6.6.2) with the following exceptions.

1. The read threshold is adjusted upward by the main μP to 20 percent of nominal tape signal.

2. The PE formatter windows are adjusted only on data bits, rather than on phase and data bits.

3. The main μP does not transfer read data to the I/O function, but does check for errors. For example:

   Dead tracks
   Parity
   Preamble/postamble format

Any error is flagged as a fatal write error.

6.7 STATUS REPORTING

In the preceding sections, various hardware components and functions have been shown to cause attention conditions, assert the I/O branch bus or μP BBUS, or otherwise provide status information to the main μP. The main μP uses this information to determine the operational condition of the machine and to maintain the TSSR and extended status registers. This section discusses the status reporting features of the hardware as a distinct function.

Many status conditions have no direct correlation with a specific hardware component or feature. For example, DCK (density check) is a condition determined by the main μP by checking for the presence of the IDB. On the other hand, there is no direct status check on some of the major hardware functions. The write function has no means of reporting status directly to the main μP. Instead, the main μP can test to see that the silo is emptied at the proper rate and the write and erase functions are checked during read after write.

Figure 6-41 is a simplified functional diagram of the status reporting function. Table 6-16 provides amplifying information.

In a general sense, status conditions are used to determine branch points within or at the end of some microcode routine. Main CROM bits 24 through 17 (and bit 00 in one case) are coded to select a particular input to a μP BBUS multiplexer. If the condition is asserted, the μP BBUS will be asserted, satisfying the condition to execute a jump instruction. For example if a jump were to be executed when IOS ATTN is high, bits 24 through 17 of the jump instruction would be encoded as 044 (octal). As in Table 6-16 and Figure 6-41, the output of DEC E19 that enables μP BBUS MUX E27 on the M8967 board would be selected (bits 24 through 22 = 0, bit 22 = 1), and input 2 to that multiplexer would be selected (bit 18 = 1, bit 17 = 0). Note that in the jump instruction the CROM fields are labeled MASK (bits 24 through 21) and SRC REG (bits 20 through 17). Refer to Paragraph 6.3.2.3.4 for a complete description of the jump instruction. The address of the next location may come from CROM 02 through 13 or from the μP OBUS via the PC buffer. The I/O section operates in a similar manner.

The ATTN logic on the M8963 board requires additional preparation on the part of the microcode. Many of the attention conditions must be enabled by a register write over the μP OBUS before the condition can assert ATTN. Furthermore, some conditions are multiplexed onto the μP IBUS. Similarly, the appropriate CBUS IN inputs must be selected by means of a register write before MUX E24 on M8963 is sampled. For example, if a jump were to be executed when the Enter 0 switch was closed, CBUS MUX 0 and CBUS MUX 1 would both be cleared by a register write via the μP OBUS, prior to the jump instruction. CROM bits 24 through 17 in the jump instruction would be 026 (octal) to select CBUS IN 3 as the input to μP BBUS MUX E24 on the M8963 board.

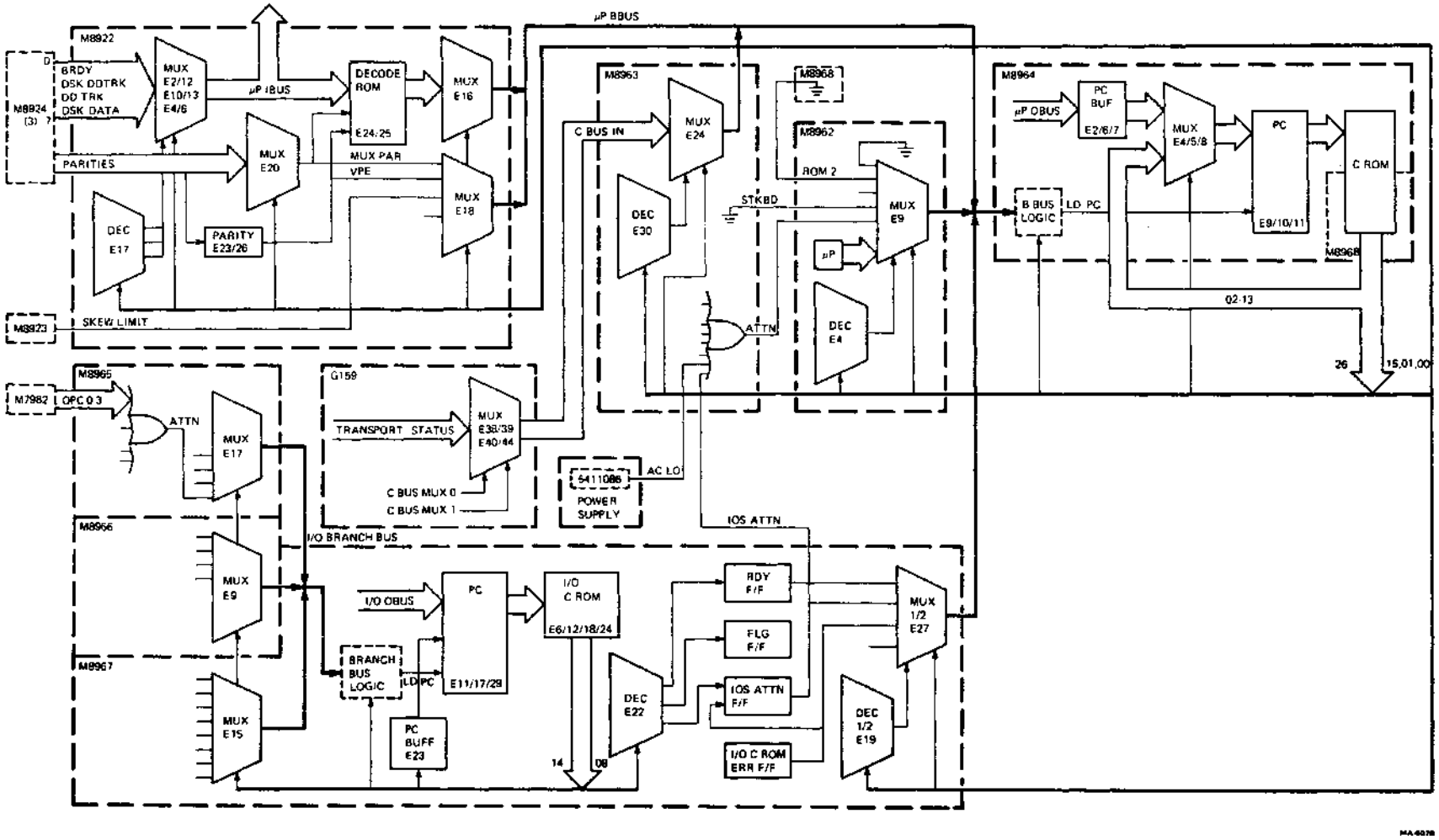


Figure 6-41 Status Reporting

Table 6-16 Status Reporting Summary

μP CROM	μP BBUS Condition				
22222 1110 43210 9870					
00000	Selects M8962 E4/E9.				
00000 000X	μP N				
00000 001X	μP Z				
00000 010X	μP C				
00000 100X	ATTN ∧ STK BD	Attention conditions STACK PERR STACK OFLO WRITE FLAG IOS ATTN ATTN LIMIT ATTN TACH AC LO LATE			
00000 101X	STK BD (GND)				
00000 110X	ROM 2 (GND)				
00000 111X	GND				
00001	Selects M8963 E30/E24.				
		CBUS MUX 0 ∧ CBUS MUX 1			
		00	01	10	11
00001 000X	CBUSIN0	EOT SEN	EOT SEN	EOT LT	CAP SPD0
00001 001X	CBUSIN1	BOT SEN	BOT SEN	BOT LT	CAP SPD1
00001 010X	CBUSIN2	WRL SW	MOTION	WRL LT	CAP SPD2
00001 011X	CBUSIN3	ENT 0 SW	FOR DIR	DCK LT	CAP SPD3
00001 100X	CBUSIN4	DO IT SW	TACH 2	VV LT	CAP SPD4
00001 101X	CBUSIN5	LIMIT SW	LIMIT SW	UOK LT	CAP SPD5
00001 110X	CBUSIN6	ONLINE SW	CLK TACH	ONL LT	CAP SPD6
00001 111X	CBUSIN7	REEL MTR ON	REEL MTR ON	LOAD LT	CAP SPD7

X = Do not care

Table 6-16 Status Reporting Summary (Cont)

μP CROM	μP BBUS Condition
22222 1110 43210 9870	
0001X	Selects M8967 E19/E27.
0001X X00X	I/O CROM ERR
0001X X01X	RDY
0001X X10X	IOS ATTN
0001X X11X	SLIR
0100X	Selects M8922 E18
0100X X000	MUX PAR = GND
0100X X001	MUX PAR = BRDY P
0100X X010	MUX PAR = DD TRK P
0100X X011	MUX PAR = DSK DD TRK P
0100X X100	MUX PAR = GND
0100X X101	MUX PAR = DSK DD TRK P V DSK DATA P
0100X X110	MUX PAR = DSK DATA P
0100X X101	MUX PAR = DSK DD TRK P V -DSK DATA P
0101X XXXX	VPE
0110X XXXX	FMT FLG
0111X XXXX	SKEW LIMIT
1000X	Selects M8922 E16.
1000X XXXX	MUD
1001X XXXX	RFMK
1010X XXXX	PREAM
1011X XXXX	9 OF 9
1100X XXXX	0 OF 9
1101X XXXX	CORR DATA
1110X XXXX	INCORR DATA
1111X XXXX	8 OF 9

Table 6-16 Status Reporting Summary (Cont)

I/O CROM	I/O BBUS Condition	
1100		
1098		
0XXX	Selects M8967 E15.	
0000	PLUS D (High)	
0001	RDY	
0010	FLG	
0011	INT ENAB	
0100	SWAB	
0101	EOX	
0110	μP CROM ERR	
0111	SLIR	
10XX	Selects M8966 E9.	
1000	FC ZER	
1001	FC MIN 1	
1010	SLOR	
1011	SILO PAR ERR	
11XX	Selects M8965 E17.	
1100	RESYNC SHFT IN	
1101	SRC MSB	
1110	OPC RECD	
1111	ATTN	Attention conditions
		DLT ERR
		SER PAR ERR
		SILO PAR ERR
		OPC 3, OPC 2, OPC 1, OPC 0 — Any op code except 17 (octal)

X = Do not care

Table 6-16 Status Reporting Summary (Cont)

I/O CROM	IOS ATTN / RDY / FLG Condition
111 100 431 098	
010 XXX	Selects M8967 E22.
010 001	SET RDY
010 010	SET FLG
010 011	RST FLG
010 100	SET IOS ATTN
010 101	RST IOS ATTN

X = Do not care

CHAPTER 7
SERVICING

7.1 SCOPE

This chapter provides complete TS11 preventive and corrective maintenance procedures. Figures 7-1 through 7-3 show the major assemblies referenced throughout this chapter.

You can access all deckplate components, the maintenance panel, and TS11 backplane by simply turning the service latch and swinging open the deckplate. You can access all modules in the card cage and the power supply by opening the rear door of the equipment cabinet.

7.2 MAINTENANCE PHILOSOPHY

The TS11 DECmagtape transport system is a highly reliable system that will provide years of trouble-free performance when correctly maintained.

There are no required Field Service preventive maintenance (PM) procedures.

Customer care should include daily cleaning of the head and tape path and running of the Customer Confidence Test at least once every six months.

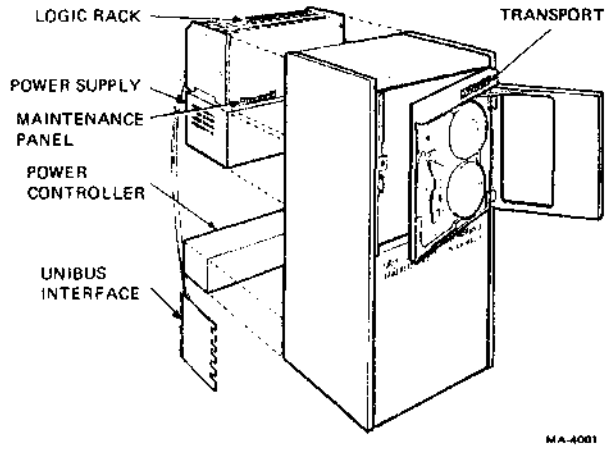


Figure 7-1 TS11 Subsystem Major Assemblies

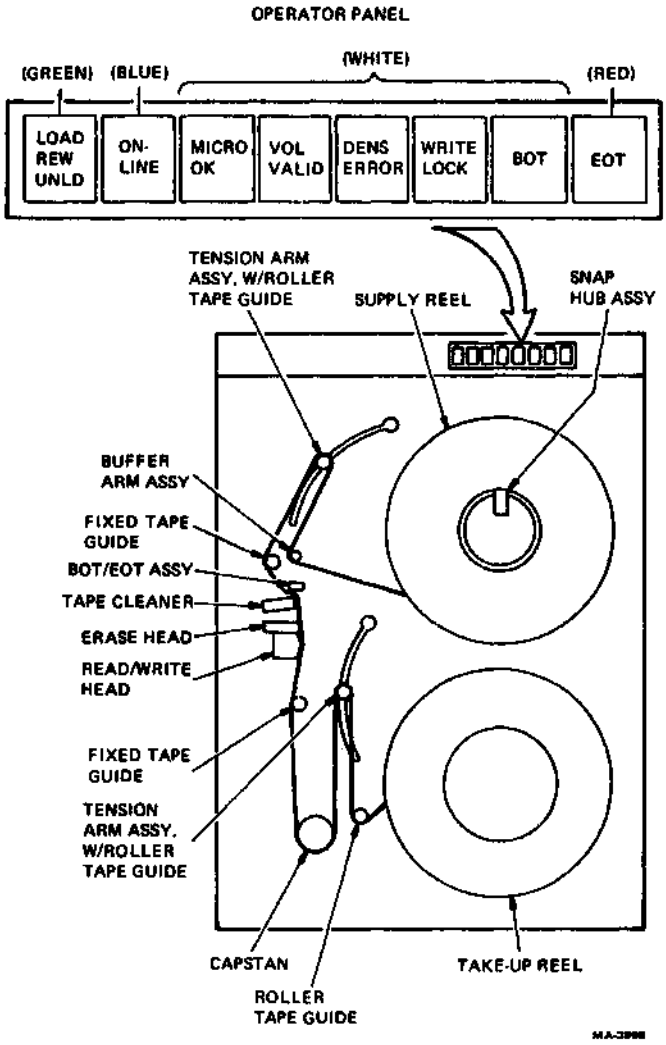


Figure 7-2 Transport Assemblies (Front View)

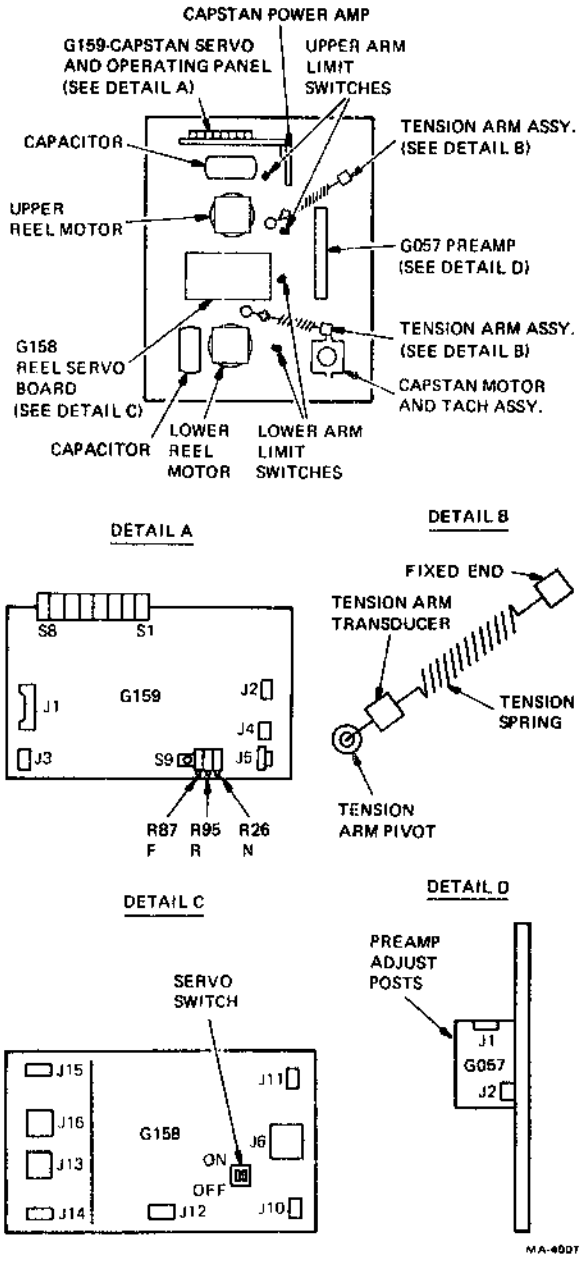


Figure 7-3 Transport Assemblies (Rear View)

A series of internal microdiagnostics run automatically, and provide failure information, whenever the TS11 is powered up, initialized, or not busy.

Corrective maintenance (CM) involves troubleshooting at the system level with on-line diagnostics, and at the subsystem level with TS11 microdiagnostics and visual methods to locate the failure. Figure 7-4 outlines the suggested troubleshooting procedure. You should isolate the failure to an electrical area (module) or a mechanical assembly. Then you can replace or adjust the faulty module or mechanical assembly as required.

7.3 SPECIAL TOOLS

In addition to the standard Digital tool kit (PN 29-18303), you need the tools listed in Table 7-1 to service the TS11.

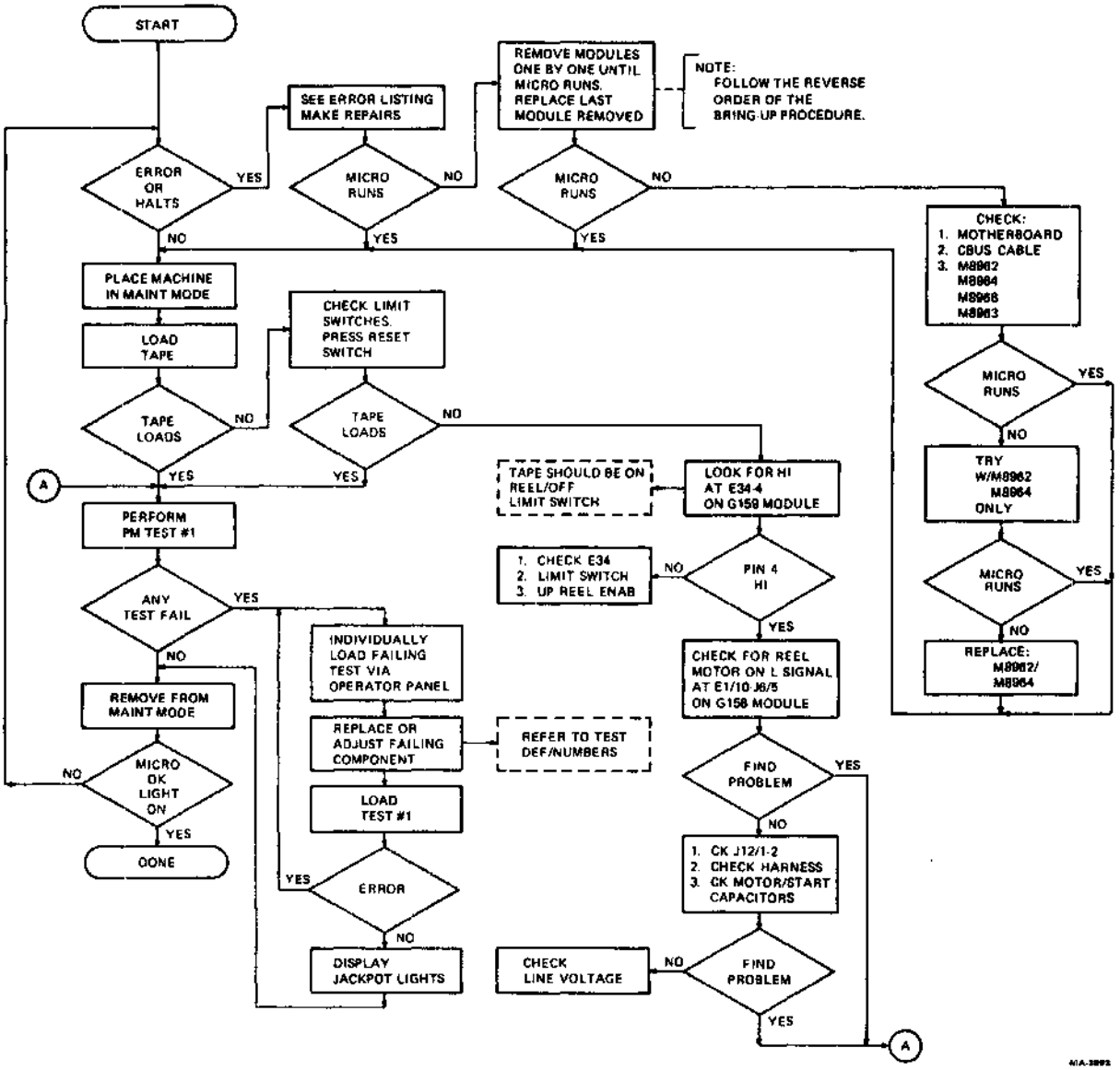


Figure 7-4 Troubleshooting Flowchart

Table 7-1 Test Equipment

Description	Part Number
Oscilloscope with probes (2-X10)	–
Master skew tape (1200 ft)	29-19224
Master skew tape (600 ft)	29-22020
Penlight	29-10780
BOT/EOT markers	90-09177
Hub spanner wrench	29-22999
Double-height extender	W984
1-3/8 in. socket (3/4 in. drive)	9 GT47549
(Local purchase)	Sears Roebuck part number
3/4 in. drive torque wrench	9 GT4443
(Local purchase)	Sears Roebuck part number
Hub height gauge	96-07951
Special test tape	29-11696
Tension gauge (0 g to 1000 g)	29-20664
Torque screwdriver	29-13212
Phillips bit 2 (for use with torque screwdriver)	29-11772
Digital multimeter	Fluke 8020A or equivalent
Lamp removal and replacement tool	29-24042

7.4 DIAGNOSTICS

The TS11 microdiagnostics and on-line software diagnostics together provide you with the tools necessary to quickly check out and repair a TS11 subsystem. On-line diagnostics include PDP-11 and VAX-based software. The TS11 microdiagnostics include initialization diagnostics, in-line diagnostics, and off-line diagnostics.

7.4.1 Initialization and In-Line Diagnostics

These diagnostics consist of five tests contained in the TS11 microcode and executed by the TS11 main microprocessor. These diagnostics run without operator intervention and without tape motion. Two tests detect fatal errors, and the other three detect nonfatal errors. The maintenance panel displays information identifying fatal errors. The operator panel displays information identifying nonfatal errors.

The five tests together are referred to as initialization diagnostics. The microprocessor runs the initialization diagnostics when activated by a subsystem power up, maintenance panel RESET, subsystem initialization, or Unibus inititialization. The five tests are listed here in the order of their execution. During execution, certain transport registers are reset to an initial value.

1. UTSTM
2. STAKM
3. IOTSM
4. CATSM
5. PETSM

UTSTM, CATSM, and parts of the remaining three tests make up the in-line diagnostics. The in-line diagnostics run in the same sequence as the initial diagnostics. However, portions of STAKM, PETSM, and IOTSM are not run because of operational requirements (for example, to preserve the contents of transport registers). The microprocessor runs the in-line diagnostics anytime the host has not accessed the TS11 for 500 ms in normal operation (that is, with the MAINT MODE/NORMAL switch, on the maintenance panel, in the down position).

7.4.1.1 UTSTM – This tests the M8962 microprocessor module, M8964 main ROM module, M8968 extended ROM module, and part of the M8963 microprocessor module. The test may run with only the M8962 and M8964 modules plugged in. If M8968 is not plugged in, UTSTM loops and tests only M8962 and M8964. If M8968 is plugged in, the microcode senses its presence and expands the sequence to test the module. Similarly, if M8963 is not present, the microprocessor loops and tests M8962, M8964 and M8968. UTSTM runs to completion only if all four modules are plugged in. Note that the UTSTM microcode includes two subtests, DISPM and MTCTM.

The UTSTM test exercises all TS11 instructions, and checks the microprocessor input bus (μP IBUS) and microprocessor output bus (μP OBUS). This test also checks the ability to execute instructions at various locations (for example, address tests that turn PC bits on and off).

All errors found by UTSTM are considered fatal. These errors halt the microprocessor. And on the maintenance panel, the CLK STP and CROM PERR indicators turn on and the PC11 to PC0 LEDs display the error PC. However, with UTSTM successfully completed, the microprocessor goes on to the STAKM test.

The UTSTM test cannot locate problems in the following areas of the M8962, M8964, and M8968 modules.

- Logic on M8962 associated with maintenance panel switches. You can test this logic manually.
- Logic on M8962 that generates special clock signals for M8922 and M8963. A malfunction in the M8962 logic is indicated by failure of microdiagnostic tests associated with M8922 and M8963.
- Some memory locations that are not exercised on the M8968 extended ROM module. Incorrect data received from an untested location is normally indicated by a CROM parity error and a halt at the bad location.
- Logic on M8964 that asserts a CROM parity error, or logic on M8962 that detects a CROM parity error. You can test this logic by unplugging the CBUS cable while running the STAKM test. As a result, the CBUS test fails because of a bad parity location.

7.4.1.2 STAKM – This tests M8963 and its communication with the G159 via the CBUS cable. The test runs with M8962, M8963, M8964, and M8968 plugged in. If the CBUS cable is not plugged in, the program halts at location 1776, indicating a CBUS communication failure. Note that unplugging the CBUS cable is a good test for detecting CROM parity errors, since the absence of the cable causes a parity error.

STAKM does an address and data test on the 64-byte push/pop RAM on M8963. Also, STAKM tests stack parity, overflow detection logic, attention branch logic, and attention register inputs associated with the stack. In addition, STAKM performs data wraparound on the CBUS and checks all the CBUS branch logic.

The STAKM test cannot locate the following problems on M8963.

• CBUS MUX 00 L hung high. CBUS MUX 01 L hung low. CBUS CLR REG L hung high. CBUS REG SEL L hung low. Tach sync flip-flop failed. Tach attention flip-flop failed.	These errors result in CATSM failure.
• CBUS CLR SWITCHES L or ATTEN LIMIT L hung high or low.	You can diagnose these errors by using a switch loop (Paragraph 7.5.2).
• CBUS STOP CAPS L hung high.	You can test this signal by stopping the microprocessor while the capstan is moving under micro control. The capstan should stop and the reel motors should turn off.
• ATTN H stuck low because Unibus signal AC LO.	You can check this problem by powering down the TS11, with the host CPU connected and the MICRO OK indicator on. The result should be TC = 16 and FC = 3 in the TSSR.
• IOS ATTN H failure.	This signal is tested by IOTSM.

With STAKM successfully completed, the microprocessor goes on to the IOTSM test if M8967 is plugged in. If M8967 is not present, the operator panel indicators display error number 100 (I/O micro test failure).

7.4.1.3 IOTSM – This tests M8965, M8966, and M8967, and the attention logic on the M8963 involving IOS ATTEN H. It also performs a data wraparound of the TS11 serial bus. If the bus is not connected, the test fails and the operator panel displays 110. All IOTSM errors are considered nonfatal and are identified as numbers 100 through 110 on the operator panel, when the test fails.

IOTSM mainly tests M8965, M8966, and M8967 as a set. However some testing on individual boards is possible. With only M8967 plugged in, the first two parts of IOTSM run. Error number 100 then appears to indicate correct operation of M8967. Then the M8966 can be added, with error number 103 indicating correct operation. M8965 can be added in a similar manner.

The IOTSM test does not locate the following problems.

- Any errors on M8966 associated with the write board silo test. These errors are detected by PETSM.
- Any errors on M8965 associated with SERIAL BUS INIT L. This signal is initiated by a CPU instruction. In practice, running the control logic test or pressing START on the CPU console asserts SERIAL BUS INIT L.
- Any bad I/O ROM locations that require an operational sequence for valid data content. The bad locations are indicated by a fatal error report to the TSSR when the sequences are initiated (Paragraph 5.1.3). Note that the TSSR records no errors if an I/O ROM parity error exists in the part of the microcode that delivers I/O messages to the TS11.

7.4.1.4 CATSM – This tests the G159 capstan module and that part of M8963 not tested by STAKM and IOTSM. The first thing CATSM checks is the 1 KHz clock generated by the G159 capstan module. During the remainder of the test, the microprocessor gives the capstan module forward and reverse commands in maintenance mode, while simulating optical tachometer pulses to check the logic portion of the digital servo system.

CATSM does not test the following areas.

• Multiplexers on analog side of speed register	Checked by off-line tests.
Deceleration one-shots	
Servo amplifier	
Rewind command	
Tachometer pulse amplifier	
Reel Motor On signal (from G159)	
Light bulbs	
D/A ladder	

- WRITE LOCK switch — Checked by switch loop (Paragraph 7.5.2).

  Limit switches

  EOT sensor

  LOAD/REW/UNLD switch

  EOT switch

  BOT sensor

  ON-LINE switch

  Attention Limit signal (from M8963)

7.4.1.5 PETSM – This tests parts of M8923, G157, M8929, M8924 and M8922. You can check most of what is not tested here with the off-line diagnostics. The remainder is tested by the control logic test.

PETSM checks the clock logic on M8929, including the silo interface signals to the M8966 that are not checked by IOTSM. The test also checks the 200 ms pulse generators on G157 and M8923 (for example, POS P H and NEG P H). In addition, PETSM checks the center frequency of the VCO on M8922, and the ability of the M8924 window logic to track POS/NEG peaks.

PETSM checks the data flow through G157, M8923, M8924, and M8922. This test also performs an XOR/checksum test on the M8922 formatter table look-up ROM. The Control Logic program checks each location for good data.

7.4.2 Off-Line Diagnostics

These diagnostics consist of 57_8 microdiagnostic test routines in the TS11. These tests check transport operations including tape motion, read data, and write data. You must load a special test tape on the transport to run the off-line tests. The off-line tests are classified as follows.

Maintenance mode diagnostics – Refers to all 57_8 routines that are selected and run by trained service personnel. You can execute these tests by using the operator panel while the TS11 is in maintenance mode (with the MAINT MODE/NORMAL switch, on the maintenance panel in the up position). Maintenance mode diagnostics can execute individually. However, selecting test 1 causes the TS11 to run tests 2 through 47_8 in autosequence mode.

Customer confidence test – Refers to a subset of off-line tests that the customer can run in autosequence to verify TS11 operation. You can execute these tests by using the operator panel in normal operation.

Table 7-2 lists all 57_8 maintenance mode tests. An asterisk (*) indicates that a test also runs as part of the customer confidence test.

Table 7-2 Maintenance Mode Diagnostics

Test	Test Name
0	Illegal (Causes reel motors to turn on.)
1	PM test (auto-sequence tests 2 through 47)
2	Capstan clock (1 KHz clock) (CATSM)
3	Capstan servo simulation forward (CATSM)
4	Capstan servo simulation reverse (CATSM)
5*	Reel motors off
6*	Reel motors on
7*	Tach phase forward
10*	Tack phase reverse
11*	Forward speed
12*	Reverse speed
13*	Capstan deceleration
14	Loop IOTST (Check I/O micro attention logic and data path.)
15	Loop IOT1 (IOCNO register frame counter test)
16	Loop IOT2 (silo with good parity/write flag)
17	Loop IOT3 (silo with bad parity/data late)
20	Loop IOT4 (IO looparound zeros)
21	Loop IOT5 (IO looparound ones)
22	Loop IOT6 (IO looparound MUX/shift length)
23	Loop IOT7 (Silo clocked by WRT board.)
24	Loop PETS1 (FMT flag/FMT mode)
25	Loop PETS2 (peak shift/FWD-REV MUX)
26	Loop PETS3 (format ROM checksum test)
27	Not used
30	Not used
31	Skew signal calibration
32*	Write head
33*	Erase head
37*	Feedthrough
40*	Tracking
41*	PE data (write)
42*	PE data (write, read forward)
43*	PE data (write, read reverse)
44*	PE signal sag RD FWD HI threshold
45*	PE signal sag RD REV HI threshold
46*	Rewind
47	Loop IOT7 (serial bus wraparound)

This is the end of the auto-sequenced tests. You must access the following tests directly by test number.

34	Minimum amplitude
35	Maximum amplitude
50	Forward/reverse skew
51	Forward read
52	Reverse read
53	Write zeros
54	Write alternating ones/zeros
55	Loop STAKM
56	Loop CBUS
57	Manual switch and light (switch loop)

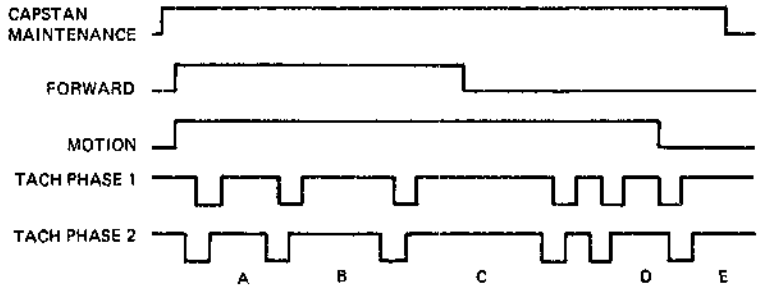
7.4.2.1 Customer Confidence Test – The customer can run this test without going inside the cabinet and setting the MAINT MODE switch. The test verifies the drive. A special test tape must be loaded (LOAD indicator on), write enabled, and the drive must be off-line. To run the test push both the LOAD and EOT operator panel pushbuttons together. The display will show 300, indicating the customer confidence test will run as soon as you press the ON-LINE switch on. If a test fails, the test number flashes in the indicators. If all tests pass, the indicators display a rotating pattern (Jackpot). To return the drive to normal operation at any time, press the ON-LINE switch again.

7.4.2.2 Maintenance Mode Diagnostics – These tests are used by trained service personnel to debug or adjust the TS11. Paragraph 7.5.1 explains how to operate the TS11 in maintenace mode. The following section list and describes the maintenance mode diagnostics.

Test 1. Auto Sequence
This test causes automatic sequencing of tests 2 through 47. If any test fails, further testing is suspended and the failing test number is left flashing on the operator panel. If no test fails, the operator panel displays the current test in progress. And when all tests are done, the panel displays the Jackpot pattern (three ones rotating left in a field of zeros).

Test 2. Capstan Board Test
This test checks the period of the capstan 1 ms clock on the G159. The test also checks the tach sync flip-flop and Attention (ATTN H) signal on the M8963. In normal operation, a positive edge on signal Tach Phase 1 sets the tach sync flip-flop, and also asserts the Attention signal if enabled. For diagnostic purposes, the capstan clock appears on the CBUS line normally used for Tach Phase 1.

Test 3. Capstan Simulated Motion Forward Test
This test turns on the Capstan Maintenance signal to prevent the capstan from moving, and then simulates an acceleration and deceleration in the forward direction. The test checks the speed register, the Motion signal, and the Forward signal. Figure 7-5 shows the scope trace you should see in the forward direction.



TIME	LOOK FOR
A	DIRECTION SIGNAL SHOULD BE VALID, MOTION SIGNAL SHOULD BE 1.
B	SPEED REGISTER SHOULD READ BETWEEN 174 AND 204. MOTION SIGNAL SHOULD BE 1.
C	SIMULATE VERY SLOW SPEED. SPEED REGISTER SHOULD READ 377 IN FORWARD, 0 IN REVERSE. MOTION SIGNAL SHOULD BE 1.
D	SIMULATE DECELERATION AND VERY FAST SPEED. SPEED REGISTER SHOULD READ 0 IN FORWARD, 377 IN REVERSE. MOTION SIGNAL SHOULD BE 1.
E	MOTION SIGNAL SHOULD BE 0 BECAUSE DIRECTION WAS REVERSED BY 1 TICK.

MA-8414

Figure 7-5 Capstan Simulated Motion Waveforms

Test 4. Capstan Simulated Motion Reverse Test
This test is the same as test 3, except that the simulated motion is in the reverse direction. Figure 7-5 also applies to test 4. However, the Reverse signal is active (as opposed to the Forward signal) and the tach phases are reversed.

Test 5. Reel Motors Off
This test turns the reel motors off and checks for the negation of the Reel Motor On signal generated by G159.

Errors

1 Reel Motor On signal is 1.

Test 6. Reel Motors On
This test turns the reel motors on and checks for the assertion of the Reel Motor On signal generated by G159.

Errors

1 Reel Motor On signal is 0.

Test 7. Tach Phase Test Forward
While moving the tape forward, this test checks the phase relationship between signals Tach Phase 1 and Tach Phase 2. These signals are generated by the capstan tachometer. The correct phase difference between the two tach signals is 90 degrees. If this test fails, try to adjust the tachometer (Paragraph 7.6.3.2). After repeated failure, replace the capstan motor assembly or G159.

Errors

4 Phase angles totally confused (for example, overlapping).

3 Phase difference exceeds limit.

Test 10. Tach Phase Test Reverse
This test is the same as test 7, except for reverse tape motion.

Test 11. Forward Speed Test
This test checks capstan speed in the forward direction. The tape accelerates for 20 capstan ticks and then stops. The speed is averaged over 8 capstan ticks. Ideal speed is 177, but a speed between 172 and 204 is acceptable.

Errors

1 Capstan too slow.

2 Capstan too fast.

Test 12. Reverse Speed Test
This test is the same as test 11, except for reverse tape motion. Ideal speed is 200, but a speed between 173 and 205 is acceptable.

Test 13. Capstan Deceleration Test
This test accelerates the tape in the forward and then reverse direction. For each direction, the test moves the tape 45 ticks and then turns off the capstan drive to stop the capstan. In each case, the test measures the number of ticks required for the tape to change direction after the capstan drive turns off. The tick limits are 13 to 19 while running in maintenance mode and exactly 16 when looping on this test. Note that it is impossible to adjust most drives well enough to completely turn off the operator panel indicators while looping on this test. A well-adjusted drive does not have any indicator completely on.

Errors

10 REV overshoot (Took too many ticks to stop in REV.)

4 REV undershoot (Took too few ticks to stop in REV or bounced back.)

2 FWD overshoot (Took too many ticks to stop in FWD.)

1 FWD undershoot (Took too few ticks to stop in FWD or bounced back.)

Test 14. I/O Micro Basic Test
In this test, the main microprocessor sets the I/O microprocessor on M8967 to single-step through the following sequence. Executing this sequence ensures that the I/O micro can set and reset the I/O Attention signal to the main micro, cause the enabling and disabling of the main micro Attention line, and accept from and pass data to the main micro. This sequence also tests the .IORDY bit. The main micro then requests the I/O micro to run the CROM parity test (IRSPAT) that contains bad parity. The I/O micro should halt with a parity error and set .IOATN.

Now the I/O is allowed to free run. The first routine requested is the CROM parity test. This test contains bad parity; the I/O should halt with a parity error and the .IOATN should be set.

Test 15. I/O Micro Flag and Frame Counter Test
This test again tests the I/O microprocessor's ability to send good data to the main microprocessor. This ability is required for on-line testing. The test also checks the three flag bits that the main micro can set and the I/O micro can sense: IC.EOX, IC.SWB, and IC.IE. In addition, the test checks the frame counter.

The first part of the test runs IR$DTT, which executes in the I/O CROM address space, returns 070, and sets .IORDY. The main micro then checks for 070 and clears .IORDY. The I/O micro then returns 307 and sets .IORDY again. The internal I/O flag (.FLG) is checked here too.

Then the main micro requests three tests (IR$CB0, IR$CB1, IR$CB2) to run, to test the IC.EOX, IC.SWB and IC.IE flag bits. In each test, the main micro sets one of the flag bits and clears the others. For example in IR$CB0, the main micro sets IC.EOX.

The second part of the test loads all 1s into the frame counter and causes the I/O micro to run IR$FCT. Running IR$FCT increments the frame counter and returns 0 if the FC0 and FC1 bits are all right. The main micro then loads 377 into the frame counter. The I/O micro transfers the 377 to the window register. And the main micro checks that the window register is 377. Finally, the test rotates a 0 in a field of 1s and causes the I/O micro to make sure that the FC1 bit is 0.

Test 16. I/O Silo Good Parity Data Test
This test writes a sequence of data bytes with good parity into the I/O silo. The sequence is 000, 377, 000, 001, 002, 004, 010, 020, 040, 100, 200. The main micro writes the first two bytes, since IC.SMX equals 1. IS.WRF (write flag bit) equals 0 for the first byte, and 1 for the second byte. The I/O micro writes the other nine bytes in the sequence, since IC.SMX equals 0. The main micro then causes the I/O micro to clock the data back from the I/O silo. On the first two bytes, the test checks the write flag attention bit in the ATTN register, and the Attention signal from the main micro. Finally, the I/O micro returns the contents of the OPERI register to the main micro. In effect, the main micro double-checks to see if an I/O silo parity error occurred on any of the bytes.

Test 17. I/O Silo Bad Parity Data Test
This test puts a 1 into the silo data register (IOSDO) and rotates a 1 in the silo control register (IOSCO), each time clocking the data into the silo. Then the main microprocessor puts 200 in IOSCO and rotates a 1 in the IOSDO register, clocking the silo as before. The above sequence is done 4 times to fill the silo, which can store 64 bytes. The silo is clocked one more time to make sure the data late error bit can be set. Then the main micro causes the I/O micro to run a routine that empties the silo byte-by-byte while checking for a silo parity error. Finally, the test writes a 1 into the IOSCO register and causes the I/O micro to write a byte into the silo. The I/O micro reads a byte and should detect bad silo parity.

Test 20. I/O Looparound Zeros Test
This test causes the I/O micro to write a 3 into the I/O extended address register (EXADRO), a 0 into the opcode register, and a 0 into the shift register. The test then does eight shifts, to move the data from the opcode and extended address registers to the shift register, where it can be read. The test allows for the parity bit during the shift. Two conditional jump bits, Shift Out (.SHOUT) and Opcode Received (.OPREC), are checked. The I/O micro then returns the contents of the shift register, which should be 006. A 367 is the mask of relevant bits because of serial bus parity uncertainty. If any conditional jump bits are bad, the I/O micro returns data that appears bad from the shift register, and therefore an error is declared.

Test 21. I/O Looparound Ones Test
This test is the same as test 20 except that the shift register receives a -1, the extended address register (EXADRO) receives a 0, and the opcode register receives a 17. The data returned to the main micro should be 361. A 367 is the mask of relevant bits because of the serial bus parity uncertainty.

Test 22. I/O Looparound Multiplex Test
This test checks the ability of the I/O micro to multiplex the shifting sequence from a 5-bit, to a 21-bit, to a 23-bit shift. The test also checks the I/O STWORD and STBYT instructions used for opcode modification.

The I/O micro first clears the extended address register (EXADRO) and shift register (SHFHO), and sets the opcode register to 1000_2 with the shift multiplexer in 5-bit shift mode (CC.5C). The I/O micro then shifts by 4 so the opcode register should contain $X100_2$. Then the I/O micro selects the 21-bit shift mode (CC.21C), shifts 24 times, and returns the resulting data from the low byte of the shift register to the main micro for data comparison. The data should be XX XX $X10_2$.

The second part of the test checks the 23-bit shift mode, STBYT, and STWORD. The I/O micro writes 0s into the EXADRO and shift registers, and writes 0100_2 into the opcode buffer with 23-bit shift mode (CC.23C). The I/O micro then does a STBYT instruction to make the buffer contain 0 110_2, and shifts 5 bits so the low byte of the shift register contains XX X01 $10X_2$. In addition, the I/O micro moves the 1 $10X_2$ to the opcode buffer.

The I/O micro then does a STWORD instruction to make the opcode buffer contain 1 $00X_2$ and shifts 4 bits so the low byte of the shift register equals XX XX1 $00X_2$. Finally, the I/O micro moves this result to the main micro for data checking.

Test 23. Write Board Clock Test
This test makes sure that the M8929 write control board can empty the silo at three selectable data rates. The test has three parts for low, medium, and high frequency. The main micro loads the I/O silo with 7, 14, or 28 data bytes, plus an extra byte with the write flag turned on. For each frequency, the main micro turns on the write control board and counts the time from the turn-on until the write flag appears. The time must be within a certain range or an error is declared.

Test 24. Formatter Flag and Sync-Up Test
The first part of the test sets and clears the formatter control flag (FC.FLO) and makes sure the conditional jump works.

The next part of the test loads twenty 0s into the I/O silo for the formatter to sync up with, and then loads 70 frames of alternating 1s and 0s in all tracks. While loading, the write control board and formatter are turned on. The formatter is in FC.VCC mode. The write control board then clocks the data off the I/O silo for the formatter to sync up with. However, before the first 1s character, the main micro loads FC.RRE and FC.VCO to keep data from being clocked off the formatter silo. The test then waits for any of the nine tracks to go dead, indicating that the formatter silo is full. The time to fill the formatter silo must be within an acceptable range or an error is declared.

For the rest of the test, all 64 bytes stored in the formatter silo are read. All these bytes are checked for data integrity.

Test 25. Formatter Peak Shift and FWD/REV MUX Test
This test checks the ability of the formatter (on the M8924 boards) to shift the data and phase window, in order to follow the peak shift and the FWD/REV MUX on the M8923 and G157 boards. The test has eight subtests. Four tests run with the tape moving in the forward direction, and the same four tests then run in the reverse direction. At the beginning of each subtest, the preamble mode bit (FC.PRE) is pulsed to provide a scope trigger/reference point.

Each test does a data shift in write mode and then read mode. The FC.RD bit in the formatter control register is set in read mode and cleared in write mode. This bit affects how the data or phase window shifts to follow the shifted phase reversal coming from the tape. In write mode, the data window should shift. In read mode, neither the data nor the phase window should shift significantly. The test passes if the track goes dead within +1.6 μs of the trailing edge of the first data window without any data. Note that for diagnostic purposes, the I/O micro simulates the tape data.

Test 26. Formatter Table Look-Up ROM Checksum Test
This test exercises the two table look-up ROM chips on the M8922 board and calculates a checksum of the data seen. This checksum is compared with what is known to be good.

The test runs a subroutine once per ROM location for a total of 1024 times. Each subroutine goes through a VCO sync-up phase, a preamble mode phase, and a data phase. But the only critical part of the test is the last couple of data bytes where the ROM outputs are actually polled.

Test 27. Not Used

Test 30. Not Used

Test 31. Skew Meter Calibration Test
Using microprocessor-generated data, this test checks the calibration of the skew meter circuit on M8923. The skew meter limit must be between 2.6 μs and 3.5 μs.

Errors

2 Skew limit too loose; to correct, turn R49 on M8923 counterclockwise.

1 Skew limit too tight; to correct, turn R49 on M8923 clockwise.

NOTE
For tests 32 through 40, the indicators display all errors in the following format.

200 Track active data error
100 Data timeout on tests that expected to see data, or noise present on tests that expected to see no data
20 Byte count error
17 Track in error (binary weight; 10 is parity track.)

Test 32. Data Head Test
This test writes data at 3200 FCI (flux changes per inch), and does a read after write at 40 percent threshold to verify the function of each of the read/write heads. The tracks are written one at a time in binary weight order. Eight 64-byte bursts are written per track, for a total of 72 bursts for all 9 tracks. All 64 bytes are verified as correct for a good burst, and 5 of 8 bursts must be good for a good track. The error display indicates the binary weight of the track that gives the first error. Note that this test also exercises M8929, M8923, G057, and part of M8924 and M8922.

Track-In-Error Decode Chart

		Operator Panel Indicators				
Track	**Bit Weight**	**VOL VALID**	**DENS ERROR**	**WRITE LOCK**	**BOT**	**EOT**
1	2 (RD2)	on	on	off	on	off
2	0 (RD0)	on	off	off	off	off
3	4 (RD4)	on	off	on	off	off
4	P (RDP)	on	on	off	off	off
5	5 (RD5)	on	off	on	off	on
6	6 (RD6)	on	off	on	on	off
7	7 (RD7)	on	off	on	on	on
8	1 (RD1)	on	off	off	off	on
9	3 (RD3)	on	off	off	on	on

If this test fails, inspect the analog outputs of the read preamps at the test points on the motherboard. Also check the following items, which can cause this test to fail.

Bad read or write head cable

Preamp not adjusted or bad

Threshold circuitry not adjusted or bad

Bad G057, G157, M8923, M8924, or M8922

Erase head not erasing tape properly (Run test 33 to verify erase head.)

Test 33. Erase Head Test
This test uses the Data Head Test (test 32) to write data on tape. The test then verifies that the drive can erase the tape so that the residual signal is less than 7 percent. The test writes the bursts in a forward direction, goes reverse with the erase head activated, and then goes forward again looking for transitions. If any transitions are seen, an error is declared.

The error display indicates the binary weight of the track that gives the first error. An error is usually caused by a dead or incorrectly adjusted erase head. However, the erase head driver on the M8929 could also be bad.

NOTE

The next several tests are related to threshold adjustments. This drive has eight microcode-selectable threshold levels (codes 0 through 7) generated by the M8923 board. One or more of the levels may be bad. To test the threshold selection, place a scope probe on the positive (A03A1) or negative (A0381) threshold voltage. With the drive running normally (not in maintenance mode), the drive continually selects one after another threshold; you should see a step pattern as code 0, then code 1 through code 7. The following thresholds are available.

Code	Volts	Threshold (Percent)
0	0.35	7
1	0.6	12
2	1.0	20
3	2.0	40
4	3.0	60
5	2.7	54
6	4.0	80
7	6.0	120

Test 37. Feedthrough Test
This test does a read simultaneous with the write, using test 32 patterns (except 800 FCI) with a 7 percent threshold. The test sets an error bit if any transitions are detected during the write. The test stops looking for transitions before the burst on tape gets to the read head.

The error display indicates the binary weight of the track that gives the first error. If the test fails, you may have to replace the head.

Track-In-Error Decode Chart

		Operator Panel Indicators				
Track	Bit Weight	VOL VALID	DENS ERROR	WRITE LOCK	BOT	EOT
1	2 (RD2)	on	on	off	on	off
2	0 (RD0)	on	off	off	off	off
3	4 (RD4)	on	off	on	off	off
4	P (RDP)	on	on	off	off	off
5	5 (RD5)	on	off	on	off	on
6	6 (RD6)	on	off	on	on	off
7	7 (RD7)	on	off	on	on	on
8	1 (RD1)	on	off	off	off	on
9	3 (RD3)	on	off	off	on	on

Test 40. Tracking Test
This test makes sure the tape tracks over the head the same way in reverse as in forward. The test writes data by using test 32 patterns while the tape moves in the forward direction. The tape then reverses direction, going over the data again with the write head turned on and the erase head turned off. The tape reverses direction again, moving forward while scanning the reverse-written area at 7 percent threshold. The test declares an error if any noise is picked up.

The error display indicates the binary weight of the track that gives the first error. If the test fails, you should check tape path alignment.

NOTE

For tests 41 through 45, the indicators display all errors in the following format.

200 Fatal error (for example, limit exceeded, no data)
100 Data error; VCO lost sync.
40 Tape mark seen.
20 Data error; VCO still synced.

No track information is available with these tests.

Test 41. PE Data Test (Write)
This test writes 72 records (256 bytes) of alternate 1s and 0s at normal threshold (12 percent gap, 20 percent data). The test sets an error bit if more than 4 of 72 records are bad.

Test 42. PE Data Test (Write, Read Forward)
This test does the write of test 41, the read reverse of test 43 without checking for errors, and then a read forward at 54 percent data threshold and 12 percent gap threshold. The test sets an error bit if more than 30 bad records are detected.

Test 43. PE Data Test (Write, Read Reverse)
This test does the write of test 41, and then a read reverse at 60 percent data threshold and 12 percent gap threshold. The test sets an error bit if more than 30 bad records are detected.

Test 44. PE Signal Sag Test (Read Forward)
This test writes 64 records, positions back and forth over the data 10 times, then does a final read forward to check for errors. An error is declared if the drive cannot read 32 records without error at 54 percent threshold on the read forward.

If this test fails, the drive may be erasing the tape slightly on repeated passes. The erase head may be too close to the tape or touching the tape. A worn write head may allow the erase head to get too close to the tape.

Test 45. PE Signal Sag Test (Read Reverse)
This test is the same as test 44, except that the final read is in reverse at 60 percent threshold.

Test 46. Rewind
This test rewinds the tape and stops at BOT. The indicators display an error if the limit switch is exceeded.

Errors

200 Limit switch exceeded or other fatal error.

Test 47. I/O Serial Bus Wraparound
This test ensures that the TS11 interface can minimally respond to opcodes and data from the I/O micro. The I/O micro sends the TS11 18 bits of data with a serial bus parity error. The I/O micro also sends the opcode (received from M7982) to the main micro for checking. This opcode should be 11_8, indicating a serial bus parity error detected by M7982. Then the I/O micro sends data with good serial bus parity to M7982 and expects to see a 17_8 opcode return. However, as mentioned above, the actual check is done by the main micro. The data sent in the second transfer should appear in the TSBA register for examination via the host panel. The data in the high byte should be 252. The edit level of the I/O microcode should appear in the low byte.

All other tests in the maintenance mode sequence run, even if the serial bus is not plugged in. This is because test 47 is the last test in the sequence.

NOTE
The following tests do not run during the auto-sequence. They must be individually selected.

Test 34. Minimum Amplitude Test
This test writes data, using test 32 patterns with a read after write threshold of 80 percent. A good burst must contain at least 56 of 64 flux changes; only 1 of 8 bursts must be verified as correct for a good track. Note that the threshold voltage should be 4 V (that is, 80 percent of 5 V) for this test.

The error display indicates the binary weight of the track that gives the first error. If the test fails, look at the POS and NEG bit strobes, generated by G157 and M8923. Most of the strobes should be present in most of the bursts. Note that you must run this test with the special test tape, because different tapes have widely varying responses.

Test 35. Maximum Amplitude Test
This test writes data, using test 32 patterns with a read after write threshold of 120 percent. A good burst must contain at least 8 of 64 flux changes; only 1 of 8 bursts must be verified as correct for a good track. Note that the voltage threshold should be 6 V (that is, 120 percent of 5 V) for this test.

The error display indicates the binary weight of the track that gives the first error. If the test fails, look at the POS and NEG bit strobes, generated by G157 and M8923. For most bursts, only a couple of strobes should be present. You must run this test with the special test tape, because different tapes have widely varying responses.

Test 50. Forward/Reverse Skew Test
This test checks skew in both forward and reverse directions. The test rocks back and forth over about 3 feet of tape, and displays an error only if the skew meter limit is exceeded during most of the pass. You must run this test with a skew tape.

Errors

2 Reverse skew error

1 Forward skew error

NOTE
For tests 51 through 54, the operator panel displays the following error codes.

200 Fatal error (for example, limit exceeded, no data)
100 Data error; VCO lost sync.
40 Tape mark seen.
20 Data error; VCO still synced.

Test 51. Forward Read
This test does a normal PE read cycle.

Test 52. Reverse Read
This test is the same as test 51, except for reverse tape motion.

Test 53. Write Zeros
This test writes 256-character, all-zero records.

Test 54. Write Alternating Ones
This test is the same as test 53, except the data is alternating ones and zeros.

Test 55. Stack Test
This test loops the stack verification test in the STAKM microcode, with good and bad parity. The logic tested is on M8963. If the test detects an error, the main micro indicates a fatal error by halting and displaying an error code between 1775 and 1777 on the maintenance panel. The operator panel display is meaningless.

Test 56. CBUS Test
This test loops the CBUS communication test in the STAKM microcode. If the test detects an error, the main micro indicates a fatal error by halting and displaying an error code between 1775 and 1777 on the maintenance panel. The operator panel display is meaningless.

Test 57. Manual Switch and Indicator Test (Switch Loop)
With the capstan stopped, this test displays the condition of the following capstan board bits continuously.

200 – Reel Motor On
100 – ON-LINE switch
*40 – Limit switches exceeded
20 – LOAD switch
10 – EOT switch
* 4 – WRITE LOCK switch
* 2 – BOT sensor
* 1 – EOT sensor

NOTE

An asterisk (*) indicates the signal is latched. To reset, press the ON-LINE switch in. With the ON-LINE switch in, these signals should still come through, but should not hold in the latched state when the signal goes away.

The only way to exit this loop is to press RESET on the maintenance panel.

Track-In-Error Decode Chart

		Operator Panel Indicators				
Track	**Bit Weight**	**VOL VALID**	**DENS ERROR**	**WRITE LOCK**	**BOT**	**EOT**
1	2 (RD2)	on	on	off	on	off
2	0 (RD0)	on	off	off	off	off
3	4 (RD4)	on	off	on	off	off
4	P (RDP)	on	on	off	off	off
5	5 (RD5)	on	off	on	off	on
6	6 (RD6)	on	off	on	on	off
7	7 (RD7)	on	off	on	on	on
8	1 (RD1)	on	off	off	off	on
9	3 (RD3)	on	off	off	on	on

7.4.3 On-Line Diagnostics

This section describes the PDP-11 and VAX-based diagnostics used for the TS11. Paragraphs 3.8 and 3.9 in the *TS11 Pocket Service Guide* provide operational details of the tests.

7.4.3.1 PDP-11 Based Diagnostics

There are three PDP-11 based diagnostics for the TS11.

Control Logic Diagnostic (CZTSI)
This diagnostic consists of 10 tests that can run individually or in an autosequence mode. CZTSI executes data wraparound through the TS11 and exercises the various TS11 commands and protocol logic.

Each failure produces a printout at the console, detailing specific error information and a probable failing FRU.

Data Reliability (CZTSH)
This diagnostic consists of five tests that can run individually or in an autosequence mode. CZTSH tests the ability of the TS11 to read and write large amounts of data in both a standalone mode and a compatability mode. CZTSH can also perform an operator-selected sequence that can be helpful in troubleshooting.

Each failure produces a printout at the console, detailing specific error information.

DECX TS11 Module (CXTSA)
This test runs under the appropriate DECX monitor and tests the TS11 in its true system environment. It does numerous reads, writes, and compares, and reports the error information at the console.

7.4.3.2 VAX-Based Diagnostics

There are two VAX-based diagnostics for the TS11.

Data Reliability Diagnostic (EVMAA)
This test thoroughly checks out the tape system. EVMAA allows the operator to test the tape system without powering the system down. The diagnostic contains four sections: Qualification Test, Data Reliability Test, Multidrive Test and Conversation Mode Test.

Subsystem Repair Diagnostic (EVMAD)
This is a standalone diagnostic that can test from 1 to 16 TS11 subsystems. The diagnostic provides fault detection/isolation to the module level whenever possible.

For further information on these diagnostics, refer to the appropriate diagnostic listing.

7.4.4 Failure Description

This section explains error information supplied by the various TS11 diagnostics.

7.4.4.1 Fatal Microprocessor Errors – These errors are caused by a microcode failure. The errors turn off the MICRO OK operator panel indicator and turn on the CLK STP and CROM PERR maintenance panel indicators. The PC indicators show the fatal error; the accepted range is from 1750 through 1777. Values outside this range indicate CROM parity errors. Table 7-3 lists the fatal error code, error description, and the module that probably failed.

NOTE

The present display in the operator panel indicators may not apply to the error.

To loop microdiagnostics on error halt, raise the Override (OVR) switch. Set the HALT/RUN switch to HALT for single step. Set the HALT/RUN switch to RUN to loop continuously. Press the STEP switch to recycle.

Table 7-3 Fatal Microprocessor Errors

Error (PC counter)	Test	Error Description	Probable Module
1750		Main micro detected CROM parity error in I/O during operational code. OP END entry called at wrong time; microcode bug halt. IOM received bad data from I/O at end of data operation when expecting record-length flags. Probably means I/O microproblem. Start I/O operation called at wrong time; probably microcode bug.	M8967
		NOTE **DISPM and MTCTM are part of UTSTM.**	
1751	DISPM	Spurious ATTN (Noise on .NATTN line?)	M8963
1752	DISPM MTCTM	Fatal stack parity error or overflow error occurred, may be hardware failure of stack board or microcode stack bug halt.	M8963
1753	DISPM	Stack not empty and nothing more to do; may be hardware stack pointer problem or microcode bug (too many pushes or pops).	
	MTCTM	Maintenance mode fatal microcode bug halt.	
1754	UTSTM	Stack pointer will not hold data.	M8962 M8963 M8964
1755	UTSTM	Failure of one of branch tests.	M8964 M8968 M8962

Table 7-3 Fatal Microprocessor Errors (Cont)

Error (PC counter)	Test	Error Description	Probable Module
1756	UTSTM	Failure of Z bit test – Z bit says result of last arithmetic operation was zero.	M8962 M8964
1757	UTSTM	Failure of N bit test – N bit says result of last arithmetic operation was negative or OBUS bit 7 was a one during last instruction.	M8962 M8964
1760	UTSTM	Failure of ones (not Z) test – Z bit was set, even though result of last operation was nonzero.	M8962 M8964
1761	UTSTM	Failure of C bit test – C bit says result of last arithmetic operation should have caused carry out of high-order stage of ALU.	M8962 M8964
1762	UTSTM	Failure of write/read external test – Unsuccessful attempt to write and read an external register (the PC buffer).	M8964 M8962
1763	UTSTM	Failure of register address/data test – Each internal register written with its own number, but gave discrepancy when read back.	M8962 M8964
1764	UTSTM	Failure of register test 2 – Each register written with complement of its own number, but gave discrepancy when read back.	M8962 M8964
1765	UTSTM	Failure of add arithmetic function.	M8962 M8964
1766	UTSTM	Failure of ASUB test.	M8962 M8964
1767	UTSTM	Failure of BSUB test.	M8962 M8964

Table 7-3 Fatal Microprocessor Errors (Cont)

Error (PC counter)	Test	Error Description	Probable Module
1770	UTSTM	Failure of shift test – Unsuccessful attempt to shift (rotate) data left or right.	M8962 M8964
1771	UTSTM	Failure of logical operands test (AND, OR, NAND, XOR, etc.).	M8962 M8964
1772	STAKM	Failure of stack parity test – Bad parity written into the stack, but stack parity error not detected.	M8963
1773	STAKM	Failure of stack underflow/overflow test – Attempted to push data on stack past location 77 (overflow) or pop data off stack past location zero (underflow), and did not get error (or attention condition).	M8963
1774	STAKM	Failure of stack address data test – Some location(s) of stack do not contain correct data after being written.	M8963
1775	STAKM	Failure of capstan bus datawrap test – Data written into light register and different data read back.	G159 M8963 CBUS cable
1776	STAKM	Failure of CBUS branch condition test.	M8963
1777	STAKM	Failure of limit attention flag – LIMIT ATTN was enabled, and status of limit switch does not agree with corresponding position in attention register.	M8963

NOTE

You can use off-line tests to scope loop after detection of a STAKM error. For STAKM errors 1772 through 1774, loop on off-line test 55. For STAKM errors 1775 through 1777, loop on test 56.

7.4.4.2 Nonfatal Microprocessor Errors – These errors turn off the CLK STP and CROM PERR maintenance panel indicators, and display an octal value from 100 to 337 in the operator panel indicators. Table 7-4 lists the error codes, error descriptions, the module that probably failed, and scope loop.

NOTE

Table 7-4 is valid when in-line or initialization microdiagnostics are running. If off-line test were running, refer to Paragraph 7.4.4.3.

Table 7-4 Nonfatal Microprocessor Errors

Scope Loop Test Number	Operator Panel Error (Octal)	Test	Error Description	Probable Cause
–	337	Operational Code	Capstan runaway error – Capstan did not stop within acceptable window after last command.	G159 Capstan motor assembly
–	300	Operational Code	Limit switch or initialization failure.	–
14	100	IOTSM	Basic I/O micro failure – Parity error, IOATN, handshaking, or data window test between I/O and main micro.	M8967
			NOTE **Error 100 can also be caused by the serial bus .SHIN (shift in) stuck asserted.**	
15	101	IOTSM	Error in I/O control register test.	M8966 M8967
15	102	IOTSM	Failure of frame counter test.	M8966 M8967
16	103	IOTSM	Failure of I/O silo nonparity error data test or write flag.	M8966 M8963 M8967
17	104	IOTSM	Failure of I/O silo parity error test or data late test.	M8966 M8967
20	105	IOTSM	Failure of shift loop with zeros.	M8965

Table 7-4 Nonfatal Microprocessor Errors (Cont)

Scope Loop Test Number	Operator Panel Error (Octal)	Test	Error Description	Probable Cause
21	106	IOTSM	Failure of shift loop with ones.	M8965
22	107	IOTSM	Failure of shift length multiplexer.	M8965
47	110	IOTSM	Failure to receive correct operating code from TS11 when responding to data sent over the serial bus.	M8965 Serial bus cable
			NOTE **If CPU power is off, error 110 will occur.**	
2	111	CATSM	Failure of 1 KHz clock test, also test tach sync flip-flop.	G159 CBUS cable M8963
3,4	112	CATSM	Indicator register changed when motion register cleared.	G159
3,4	113	CATSM	FWD or MVG bits wrong after one tick of simulated command, and tach pulses.	G159
3,4	114	CATSM	Failure of simulated capstan speed test – Speed counter was out of range when tape motion at speed was simulated.	G159
3,4	115	CATSM	Failure of simulated slow capstan test – Speed counter did not latch up with maximum count when slow tach ticks were simulated.	G159

Table 7-4 Nonfatal Microprocessor Errors (Cont)

Scope Loop Test Number	Operator Panel Error (Octal)	Test	Error Description	Probable Cause
3,4	116	CATSM	Failure of simulated capstan deceleration test – Counter not 0 for forward or 377 for reverse while decelerating, or MVG bit not 1.	G159
3,4	117	CATSM	Failure of moving flop to go to zero after stopping (direction reversal for one tach tick).	G159
23	120	PETSM	Failure of write board to turn on and empty silo, or data late bit does not work.	M8929 M8966
23	121	PETSM	Failure of write board to empty silo at correct speed.	M8922 M8929
24	124	PETSM	Formatter flag does not work on M8922.	M8922
24	125	PETSM	Formatter silo filling and data error.	M8922 VCO adj. M8923 M8924
25	126	PETSM	Peak shift test error.	M8924 M8922 M8923 G157
26	127	PETSM	Formatter table look-up ROM checksum test error.	M8922 M8923 M8924

7.4.4.3 Off-Line Test Errors – These errors occur only when running off-line tests. If running in autosequence mode the failing test is displayed first. This failing test can be entered to run in standalone mode. The resulting error code in the operator panel describes the failure and the module that probably failed. Paragraph 7.5.1 explains how to run off-line tests in maintenance mode, and 7.4.2.1 explains how to run the customer confidence test. Table 7-5 lists the failing test, operator panel indication, error description, and probable cause. The asterisks (*) indicate customer confidence tests.

Table 7-5 Customer Confidence or Maintenance Mode Test Errors

Scope Loop Test Number	Operator Panel Error (Octal)	Error Description	Probable Cause
All	300	Init failure loaded, door interlock not out, limit switch closed.	No test number
1	Various	Indicates failed test number.	See failed test description
2	111	1 ms capstan clock off speed TAC sync flip-flop or TAC ATTN signals not working.	M8963, G159, motherboard, CBUS cable
3,4	112	Operator panel affected by WRT CLR to MOT REG.	G159, CBUS cable
3,4	113	MVG or FWD/REV flip-flop not okay.	G159, CBUS cable
3,4	114	SPD REG out of tolerance (on speed).	G159, CBUS cable
3,4	115	SPD REG wrong (slow cable).	G159, CBUS cable
3,4	116	SPD wrong (deceleration).	G159, CBUS cable
3,4	117	MVG not set during deceleration.	G159, CBUS cable
5*	1	Reel motors off; Reel Motors On signal was 1.	G158, G159, reel motor, CBUS cable

Table 7-5 Customer Confidence or Maintenance Mode Test Errors (Cont)

Scope Loop Test Number	Operator Panel Error (Octal)	Error Description	Probable Cause
6*	1	Reel motors on; Reel Motors On signal was 0.	G158, G159, reel motor
7 to 10*	4	Phase angles confused.	G159, tach adjustment, capstan motor assembly
7 to 10*	3	Phase exceeded limit.	G159, tach adjustment, capstan motor assembly
11 to 12*	2	Capstan speed too fast.	G159
11 to 12*	1	Capstan speed too slow.	G159
13*	10	REV overshoot – Too many ticks to stop REV.	G159, decel adjustment
13*	4	REV undershoot – Too few ticks or bounced back.	G159, decel adjustment
13*	2	FWD overshoot – Too many ticks to stop FWD.	G159, decel adjustment
13*	1	FWD undershoot. Too few ticks or bounced back.	G159, decel adjustment
14	100	I/O Micro step, I/O ATTN	M8967, M8963
15	101	IOCNO register test failed.	M8967, M8966
15	102	Frame counter test failed.	M8966
16	103	Silo good parity-data flag.	M8966, M8963
17	104	Silo bad parity-data late.	M8966
20	105	I/O looparound zeros test failed.	M8965
21	106	I/O looparound ones test failed.	M8965

Table 7-5 Customer Confidence or Maintenance Mode Test Errors (Cont)

Scope Loop Test Number	Operator Panel Error (Octal)	Error Description	Probable Cause
22	107	I/O looparound shift length multiplexer test failed.	M8965
47	110	Serial bus/TS11 alive.	M8965, M7982, motherboard
23	120	I/O silo not being clocked by write board.	M8929, M8966
23	121	Write board silo clock out of range.	M8929
24	124	FMT FLG in FMT CNTL REG test	M8922, VCO adjustment
24	125	PE FMT mode, data, silo	M8922, M8923, M8924, G157, VCO adjustment
25	126	PE FMT early/late bit shift test failed.	M8922, M8923, M8924, G157, VCO adjustment
26	127	PE FMT table look-up ROM checksum test	M8922
31	2	Skew limit too loose – Turn R49, M8923 counterclockwise.	M8923, G157
31	1	Skew limit too tight – Turn R49, M8923 clockwise.	M8923, G157
		NOTE **Any of four error codes (17, 20, 100, 200) can occur while running tests 32 through 40. More than one may appear at the same time (120 for example).**	
32*	200	Track active data error.	G057, M8929, G157, cables, M8923, M8924, erase head, head

Table 7-5 Customer Confidence or Maintenance Mode Test Errors (Cont)

Scope Loop Test Number	Operator Panel Error (Octal)	Error Description	Probable Cause
33	100		Erase head
34 to 35	100	Data timeout if data expected (tests 32, 34). Noise when no data expected (tests 33, 35 through 40).	G057, M8922, preamp adjustment, threshold adjustment, VCO
37*	17	Track in error – 10 is parity track; decode to bit weight.	Head
40*	100		Head
		NOTE **Any of four error codes (20, 40, 100, 200) can occur when running tests 41 through 45 or 51 through 54.**	
41 to 45*	200	Fatal error. Limit exceeded or no data.	Media, head threshold adjustment
51 to 54	100	Data error – VCO lost sync.	M8922, M8924, M8929, threshold adjustment
	40	Tape mark seen.	M8922, M8924, M8929, threshold adjustment
	20	Data error – VCO still synced.	M8922, M8924, M8929, threshold adjustment
		NOTE **Any of four error codes (20, 40, 100, 200) can occur when running tests 41 through 45 or 51 through 54.**	
50	2	Reverse skew error.	Head skew adjustment tape path, head

Table 7-5 Customer Confidence or Maintenance Mode Test Errors (Cont)

Scope Loop Test Number	Operator Panel Error (Octal)	Error Description	Probable Cause
50	1	Forward skew error.	Head skew adjustment tape path, head
		NOTE **Errors on tests 55 or 56 are indicated by the PC LEDs. The meaning of an error in the PC LEDs is shown in the "Fatal Microprocessor Errors" table.**	
57	200	Reel motors on.	Limit switches
57	100	ON-LINE switch in. (Turns on ON-LINE indicator.)	ON-LINE switch
57	40	Limit switch exceeded, latch set. (All limit switches turn on MICRO OK indicator.)	Limit switches
57	20	LOAD switch in. (Turns on VOL VALID indicator.)	LOAD switch
57	10	ZEROS switch in. (Turns on DENS ERROR indicator.)	ZEROS switch
57	4	Write lock lever out, write locked. (Turns on WRITE LOCK indicator.)	Write lock assembly
57	2	BOT latch set. (BOT sensor turns on BOT indicator.)	BOT/EOT sensor
57	1	EOT latch set. (EOT sensor turns on EOT indicator.)	BOT/EOT sensor
		NOTE **Test 57 loops on itself. The loop is broken by pressing RESET on the maintenance panel.**	

7.4.4.4 On-Line Failures – All failures generated when running on-line diagnostics produce an error printout at the console. The printouts include at least the function under test, associated status, and error register information. Refer to Chapter 5 or the associated diagnostic listing for further information on troubleshooting these failures.

7.5 TROUBLESHOOTING

This section describes the troubleshooting procedures for the TS11.

7.5.1 Maintenance Mode Operation

You must load a write-enabled special test tape on the transport for maintenance mode operation. You can enter maintenance mode by setting the MAINT MODE/NORMAL switch on the maintenance panel to MAINT MODE. When the TS11 enters maintenance mode, all operator panel indicators are off. Also, the host CPU cannot access the TS11.

You can select a test to execute in maintenance mode by entering the test number (octal) via the operator panel. The following table shows the switches to use.

Operator Panel Normal Mode	Maintenance Mode	Description
LOAD REW UNLD	ONES	Enters a 1 into the LSB position, shifts the entire contents left, and displays the digit in the operator panel.
EOT	ZEROS	Enters a 0 into the LSB position, shifts the entire contents left, and displays the digit in the operator panel.
ON-LINE	START/STOP	When pressed, executes the selected test. If the operator panel indicators are all off, the reel motor turns on. When released, halts the test running.

NOTE

In maintenance mode, the tape cannot be loaded and automatically positioned to BOT. This function can be done only when the TS11 is in normal mode. If the tape is loaded and positioned at BOT before entering maintenance mode, pressing ON-LINE with all operator panel indicators off has no effect.

In maintenance mode, the operator panel displays error information in octal. Error information can be displayed in one of two ways.

1. When you run test 1 (Auto Sequence), the operator panel displays the current test as it executes. If a failure occurs, the indicators continue to flash the failing test number.

2. When you run any individual test other than test 1, the operator panel displays error information related to that specific test. To interpret this information, refer to Paragraph 7.4.4.3.

Successful completion in autosequence mode is shown by a rotating pattern in the operator panel indicators (only when connected to a TS11 with power applied). Exit to normal operation by setting the MAINT MODE/NORMAL switch to NORMAL, then replace the scratch tape.

7.5.2 Manual Switch Test (Test 57)

In maintenance mode, test 57 verifies the operation of various TS11 switches and the operator panel. Usually, you select this test through the operator panel. The following procedure lets you execute test 57 from the maintenance panel, if you suspect the operator panel is bad or the main microprocessor did not get to the microcode allowing selection of a test.

1. Set HALT and clear MAINT MODE.
2. Press RESET (PC = 0).
3. Press STEP three times (PC = 41, 42, 43).
4. Set MAINT MODE and clear HALT.
5. Press STEP.

The test is now running. Refer to Paragraph 7.4.4.3 for test 57 error and status information. The only way to exit this test is to press RESET on the maintenance panel.

7.5.3 Bring-Up Procedure

This special procedure lets you bring up the system when it is "dead in the water." This condition exists when nothing else works (tape cannot be loaded or microdiagnostics run) and the power is okay. One of the modules that makes up the microprocessor or control read only memory (CROM) is not working, or a module that hangs on the microprocessor buses is hanging the bus.

Hardware and microcode are structured so that all modules except the main micro and main ROM board can be removed from the system and then added one by one until a failure occurs. The diagnostic senses the modules as they are added and expands the test loop to include the new module's function. Perform the following initial set-up procedures.

1. Power off.
2. Remove all PC cards in the logic rack except M8962 (microprocessor) and M8964 (PC and ROM 1).
3. Remove the cable from J2 on the backplane. This disconnects G159 (capstan servo board).
4. Remove the cable from J4 on the backplane (disconnects TS11 Unibus interface card M7982).
5. Set the MAINT MODE/NORMAL switch to NORMAL, the enable error (OVR) switch to enable, and the HALT/RUN switch to RUN.

Starting with only M8962 and M8964 installed, perform the following test sequence procedure.

1. Power up.
2. Wait 20 seconds.
3. Press RESET on the maintenance panel.

4. Table 7-6 lists the correct contents of the maintenance panel and operator panel displays. If the displays differ from Table 7-6, the last module added is bad.

5. If all display indicators are correct, perform these steps.

   a. Power off.

   b. Insert the next card listed in the add column of Table 7-6.

   c. Go back to step 1 and continue testing.

Table 7-6 Bring-Up Procedure Errors

Module Added	Maintenance Panel CLK STOP	Maintenance Panel CROM PERR	Operator Panel Errors (Octal)	Comment
M8962, M8964 Rev C	off	off	-	Loop basic micro test
M8968 Rev F	off	off	-	Loop basic micro test
M8963	on	on	-	Control bus test
G159 cable (J2 on motherboard)	off	off	100	Basic IC test
M8967 Rev D	off	off	100	Frame control test
M8966	off	off	103/100	I/O silo test
M8965	off	off	110	Serial bus wrap test
M7982 (J4 on motherboard)	off	off	120*	Write board/silo test
M8929	off	off	124	PE FMT flag test
M8922 and interconnect jumper	off	off	125	PE silo test
M8923, M8924, G157	off	off	Micro okay	System up (VCK OK). VOL VALID indicator on.

* 110 if host CPU power off.

NOTE

The indications in this table are correct for the highest Rev level of the ROM modules listed. Other Rev levels may show a different indication. If the operator panel displays something other than the errors listed in Table 7-6 and the latest module added is not the cause, check the nonfatal microprocessor errors (Table 7-4) for the probable cause of the error.

7.5.4 Data Track Card Identifier

Table 7-7 shows which card is dead for each dead track recorded in extended register 2 (XSTAT2), using Data Reliability Program (CZTSH) Test 2 on PDP-11 systems or Data Reliability Program (EVMAA) Section 2 on VAX systems.

Table 7-7 Dead Track/Module Locations

Dead Track	Bit	Head Track	Probable Bad Location/Module	
1	0	2	2 / G157	6 / M8924
2	1	8	2 / G157	6 / M8924
4	2	1	1 / G157	6 / M8924
10	3	9	1 / G157	5 / M8924
20	4	3	1 / G157	5 / M8924
40	5	5	2 / G157	5 / M8924
100	6	6	2 / G157	4 / M8924
200	7	7	1 / G157	4 / M8924
400	P	4	3 / M8923	4 / M8924

7.6 CHECKS AND ADJUSTMENTS

This section describes the checks and adjustments for the TS11.

7.6.1 Power Supply Checks and Adjustment

Check the power supply outputs listed in Table 7-8 with a digital voltmeter (DVM). Adjust the +5 V and +15 V outputs if necessary. Figure 7-6 shows the power supply, and Figure 7-7 shows the layout of the Mate-N-Lok connectors. The power outputs are on connectors P1PS and P2PS. Table 7-9 lists the signals and wire colors at all four Mate-N-Lok connectors.

Table 7-8 Voltage Checks and Adjustments

Voltage	Range (Volts)	Test Point	Wire Color	Adjustment Point
+5 Vdc regulated	5.0 to 5.20	P1PS-7 P1PS-10	Red Red	H744 regulator
+15 Vdc regulated	14.5 to 15.5	P1PS-3	Yellow	5411086 regulator
−15 Vdc regulated	14 to 16	P1PS-11	Blue	Not adjustable
+18 Vdc unregulated	15 to 23	P2PS-1	Yellow	Not adjustable
−18 Vdc unregulated	15 to 23	P2PS-4	Blue	Not adjustable
AC LO 5 Vdc	7.0 (max)	P1PS-6	Orange	Not adjustable
DC LO 5 Vdc	7.0 (max)	P1PS-12	Green	Not adjustable

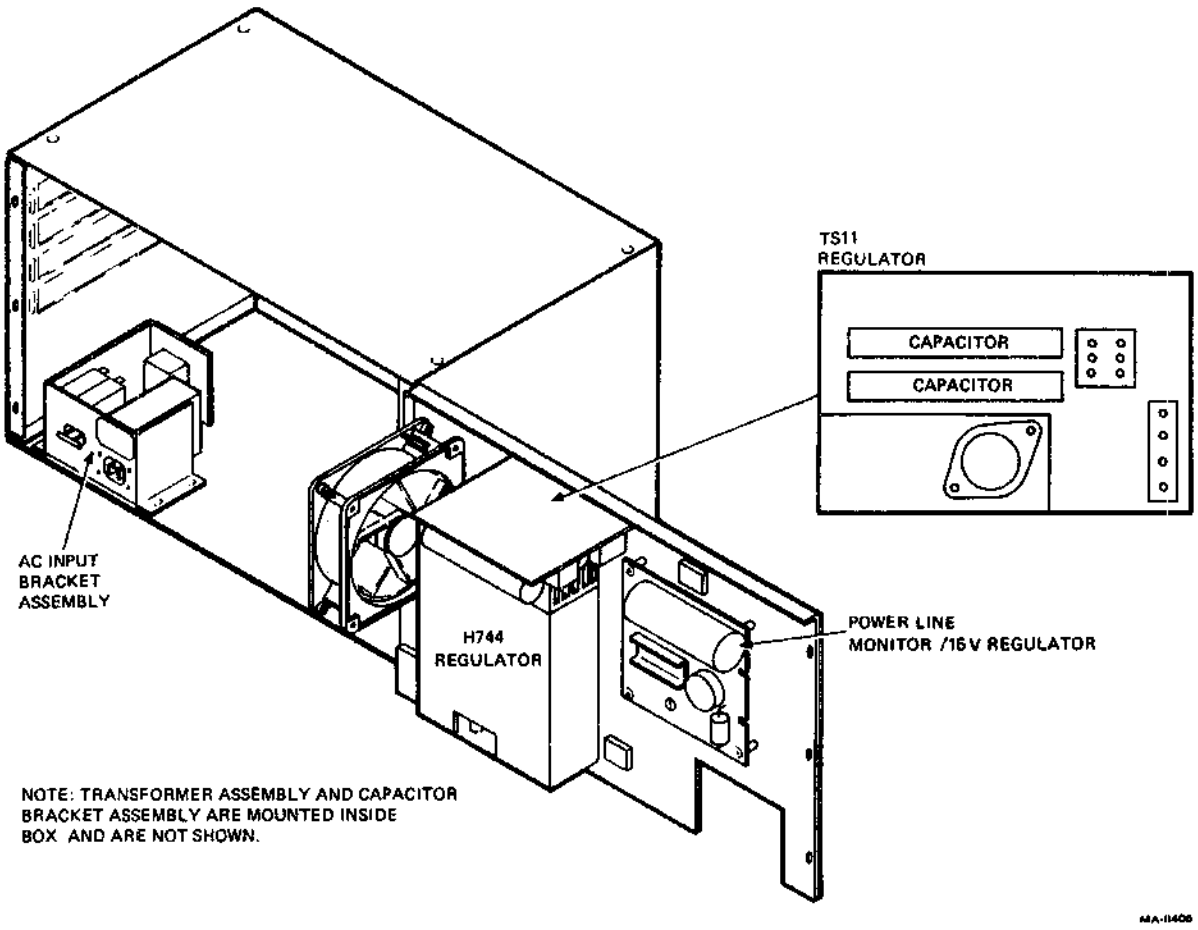


Figure 7-6 Power Supply

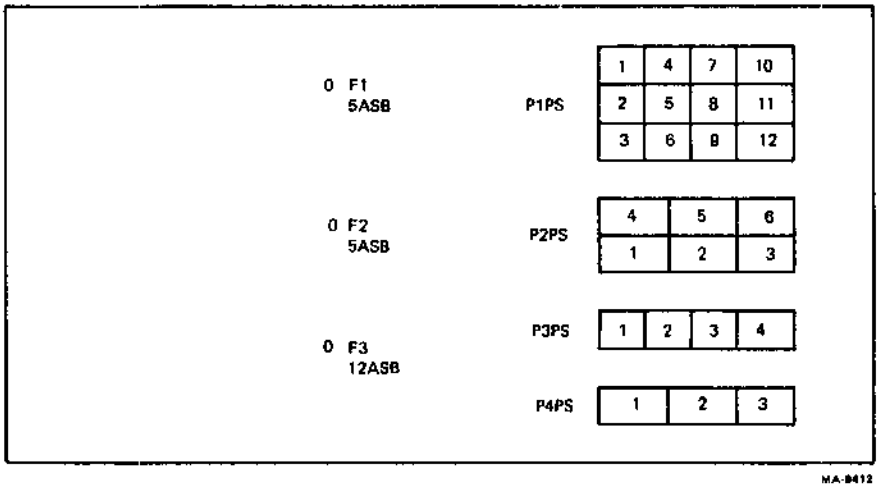


Figure 7-7 Power Supply Mate-N-Lok Connector Layout

Table 7-9 Wiring Charts for TS11 70-16288 Power Supply Mate-N-Lock Connectors

Connector Plug	Color	Connector Plug	Color
P1PS-1	—	P2PS-1	Yellow (+18 V unregulated
P1PS-2	Black (ground)	P2PS-2	Black (ground)
P1PS-3	Yellow (+15 V regulated	P2PS-3	Black (ground)
P1PS-4	—	P2PS-4	Blue (−18 V unregulated)
P1PS-5	Black (ground)	P2PS-5	—
P1PS-6	Orange (AC LO)	P2PS-6	—
P1PS-7	Red (+5 V regulated)	P3PS-1	Blue (AC LO)
P1PS-8	Black (ground)	P3PS-2	Brown (logic cage fan)
P1PS-9	Black (ground)	P3PS-3	Green/Yellow (ground)
P1PS-10	Red (+5 V regulated)	P3PS-4	-
P1PS-11	Blue (−15 V regulated)	P4PS-1	White (AC LO)
P1PS-12	Green (DC LO)	P4PS-2	Black (reel motor)
		P4PS-3	— (G158)

7.6.2 Mechanical Adjustments

This section describes mechanical adjustments for the TS11.

7.6.2.1 Snap Lock Hub Height Check and Adjustment – Check and adjust the snap lock hub height as follows. Refer to Figures 7-8 and 7-9.

Check

1. Insert the hub height gauge (PN 9607951) from the rear of the door casting through the slot to the left of the hub. The base of the gauge should rest against the rear of the casting, with the concave side facing the reel motor.

2. Hold the base of the gauge tight against the rear of the casting, and rotate the three surfaces on the end of the gauge. The rear of the "Go" surface should just clear the front surface of the hub flange. The "No Go" surface should not clear the flange surface.

Adjustment

1. Remove the snap lock hub assembly (Paragraph 7.7.2.1).

2. Add or remove shims as needed to satisfy the set position of the gauge.

3. Replace the inner hub (Paragraph 7.7.2.2).

4. Repeat step 2.

5. If correct, replace outer hub (Paragraph 7.7.2.2).

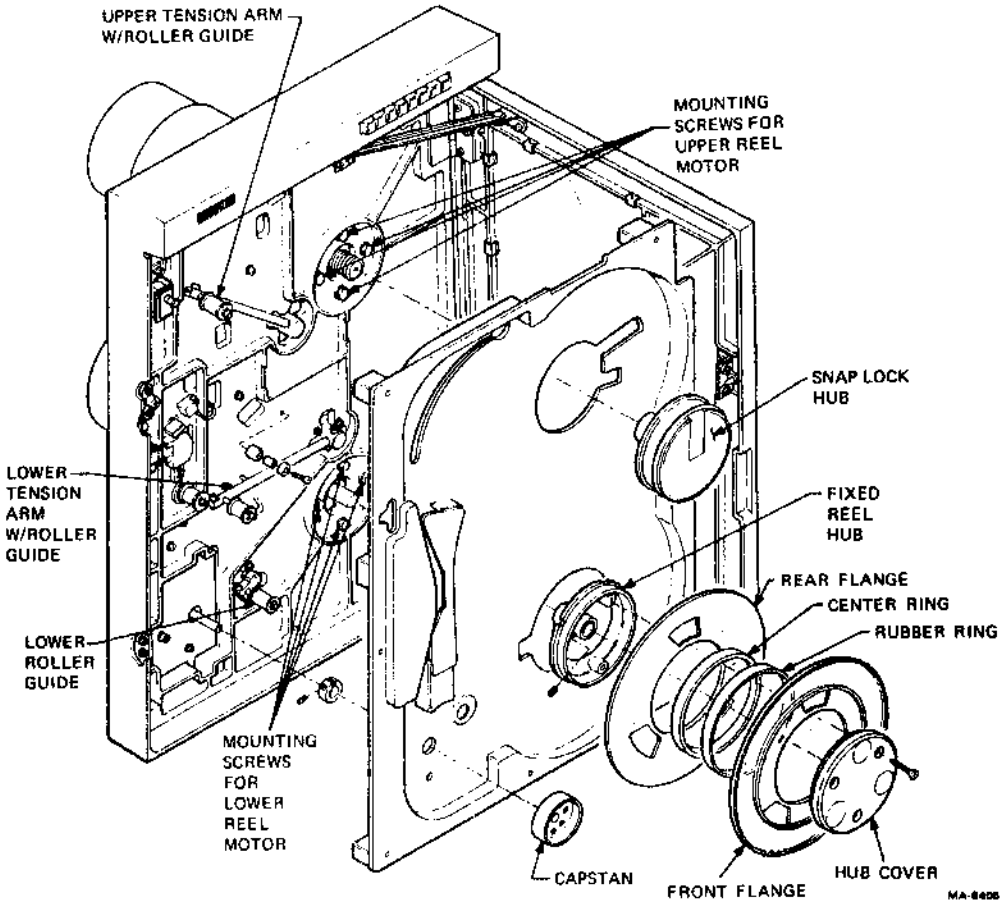


Figure 7-8 Deckplate Assembly

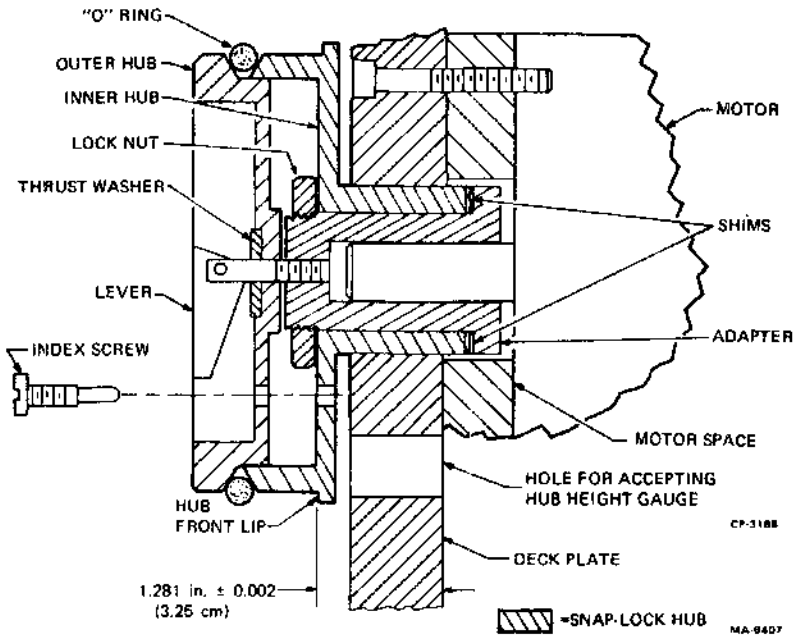


Figure 7-9 Snap Lock Hub Cross Section

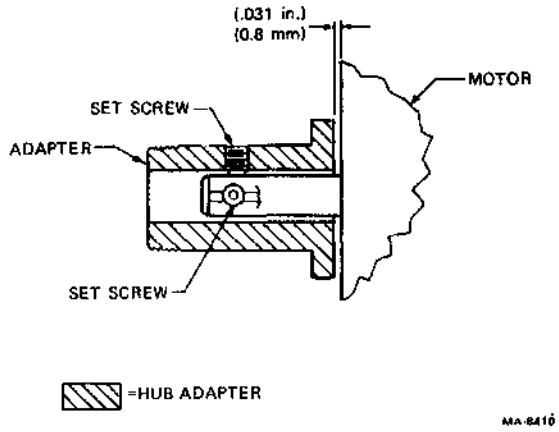


Figure 7-10 Hub Adapter

7.6.2.2 Fixed Reel Hub Height Adjustment – Check and adjust the fixed reel hub height as follows. Refer to Figures 7-8 and 7-10.

Check

1. Remove the three phillips screws holding the reel to the hub, and remove the reel assembly.

2. Insert the hub height gauge (PN 9607951) from the rear of the door casting through the slot to the left of the hub. The base of the gauge should rest against the rear of the casting, with the concave side facing the reel motor.

3. Hold the base of the gauge tight against the rear of the casting, and rotate the three surfaces on the end of the gauge. The rear of the "Go" surface should just clear the front surface of the hub flange. The "No Go" surface should not clear the flange surface.

Adjustment

1. If an adjustment is needed, loosen the two set screws holding the hub to the motor shaft.

2. Position the "Set" surface of the hub height gauge over the front surface of the hub flange. Hold the base of the gauge tight against the casting, and move the hub until contact is made between the "Set" surface and the hub flange.

3. Now tighten the two hub set screws and check the adjustment with the "Go" and "No Go" surfaces of the gauge as described in the check procedure.

4. Reinstall the reel assembly.

7.6.2.3 Tension Arm Transducer Coarse Adjustment – Perform the tension arm transducer coarse adjustment as follows.

NOTE

To perform the following adjustment, remove any tape mounted. Then lower each tension arm to its lowest position and insert a screwdriver into the holes at the rear of the deckplate to hold the tension arms in position. The hole for the upper arm is behind the upper tension spring. The hole for the lower arm is just above the lower tension spring.

1. Switch to maintenance mode. Run test 6.
2. Loosen the tension arm transducer holding screws.
3. Adjust the upper transducer for no movement of the supply reel. Tighten the screw.
4. Adjust the lower transducer for no movement of the takeup reel. Tighten the screw.
5. Stop test 6, remove the screwdrivers, and do the fine adjustment.

7.6.2.4 Tension Arm Transducer Fine Adjustment – Perform the tension arm transducer fine adjustment as follows.

1. Load a scratch tape.
2. Run test 50 in maintenance mode.
3. Observe the position of the tension arms while the tape is moving. There should be a clearance of 1/2 inch to 1 inch between the tension arms and the limit switches at both ends of their travel. If an arm is close at one limit and far away at the other limit, a fine adjustment is necessary.
4. With the tension arms moving, adjust the transducer for the tension arm needing adjustment until the clearance between the tension arm and the limit switches (at both ends of travel) are equal.

NOTE

Use caution when adjusting transducers while the tape is moving; a large adjustment may exceed the limits, dropping tape tension.

5. Tighten transducer screws.
6. Repeat step 3.

7.6.2.5 Reel Motor and Brake Check – The brakes and the reel motors are both controlled by G158. The brakes are used only as a "parking brake," and engage when the reel motors are powered down. Check the reel motor and brake as follows.

1. Apply power to the system, noting fan motor operation.

2. Load the tape.

3. Power down reel motors by either tripping a limit switch or the interlock switch manually, and observe the tension arms. If either tension arm reaches the upper limit switch, the brake is not holding; replace the associated reel motor.

7.6.2.6 Tape Tension Coarse Adjustment – Perform the tape tension coarse adjustment as follows. Refer to Figure 7-11.

1. Power down the system.

2. Use a 1 foot length of tape with loops at each end to attach a 2 pound force gauge to the upper arm as shown. Place the tape between the upper fixed guide and the upper roller guide, then pull the arm in the direction shown to the approximate center of its swing. Take care to zero the force gauge in the actual position used to make the measurement. Adjust the upper spring adjustment screw on the back of the deckplate until the gauge reads 475 g ± 15 g.

3. Use the same 1 foot length of tape to attach the 2 pound force gauge to the lower arm as shown. Place the tape between the capstan and the lower roller guide, then pull the arm in the direction shown to the approximate center of its swing. With the gauge properly zeroed, adjust the lower spring adjustment screw on the back of the deckplate until the gauge reads 525 g ± 15 g.

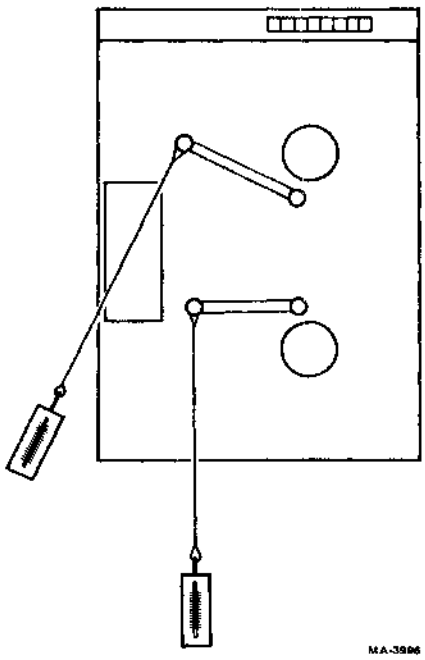


Figure 7-11 Tension Arm Adjustment

7.6.2.7 Tape Tension Fine Adjustment – Perform the tape tension fine adjustment as follows.

1. Mount a scratch tape and load to BOT.
2. Disconnect both push-on leads from the capstan motor.
3. Connect one lead of a 0 to 1 amp ammeter to a +5 V source. (You can use C1 on G159.) Connect the other lead to one of the capstan motor terminals.
4. Use a wire lead to connect the other capstan motor terminal to ground. The motor will start to turn when the connection is made.
5. To reverse the direction of the capstan motor, switch the ammeter and ground leads on the capstan terminals.
6. Measure the current in both directions and adjust the upper spring adjusting screw until the current reading is equal in both directions.
7. Disconnect the meter and reconnect the motor leads.
8. Press RESET on the maintenance panel.
9. Check the capstan deceleration adjustment (Paragraph 7.6.3.4).

7.6.2.8 Tape Path Alignment – You must align the tape path if you replace any part in the tape path, or if you see tape edge damage. The tape path includes the supply reel, rollers, tension arms, tape spring guides, capstan, and take-up reel (Figure 7-12). The alignment procedure's main purpose is to guarantee that the magnetic tape moves in the same plane as the reference surface (the rear machined surface of the deck-plate), in both forward and reverse. To ensure this, the capstan and all guides must be perpendicular to the tape reference surface, and all set at the same height.

You can see the effects of capstan misalignment in both the horizontal and vertical planes. If the capstan is misaligned in the horizontal direction, then the tape moves in and out, with respect to the tape reference surface, as the tape moves in the forward and reverse directions.

NOTE

Forward tape motion is when tape moves from the magnetic head toward the capstan. Reverse tape motion is when tape moves from the capstan toward the magnetic head.

If the capstan is misaligned in the vertical direction, the tape remains off center of the capstan, regardless of tape direction.

If a roller guide is misaligned, you can see puckering of the tape at that guide.

NOTE

Ensure that the hub height adjustment is correct before continuing.

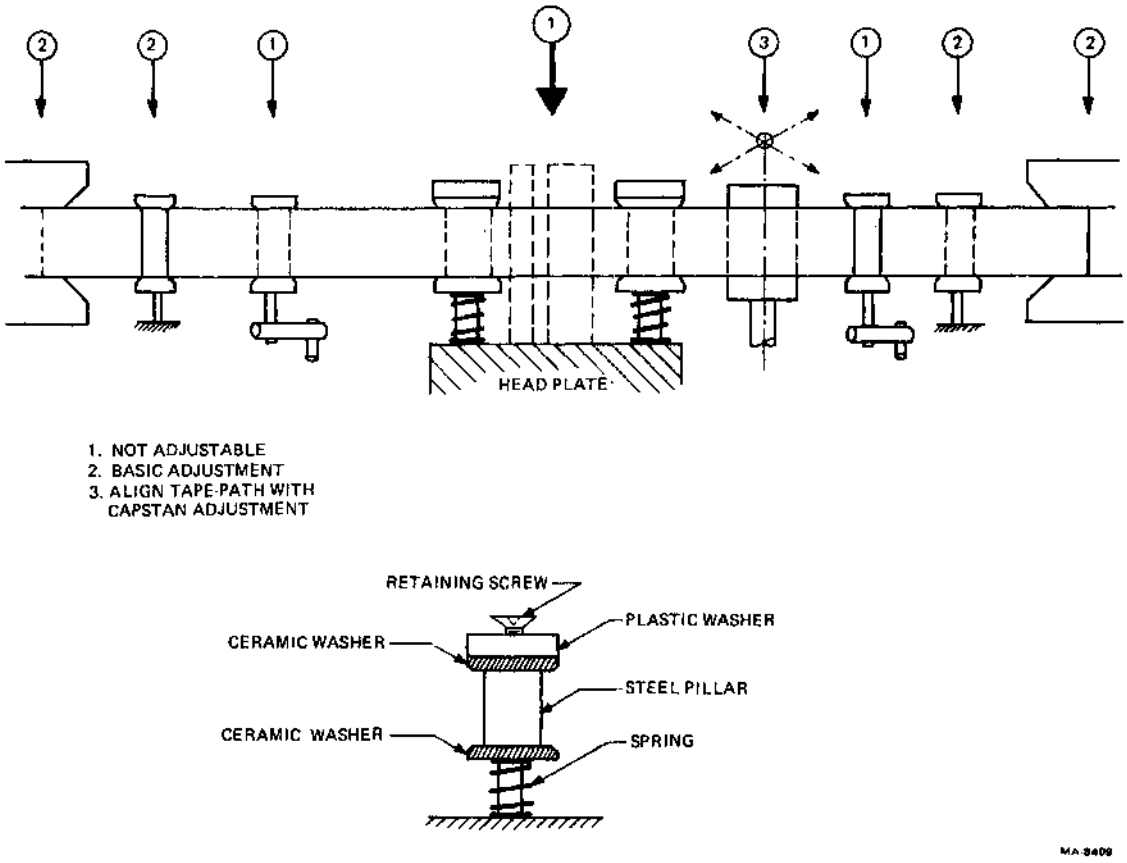


Figure 7-12 Tape Path Alignment

1. Proceed as follows to position the capstan on the motor shaft (Figure 7-13).

   a. Loosen the capstan locking clamp with an Allen wrench. Remove the capstan and clamp. Check the capstan inside surface for roughness or foreign material that may inhibit correct fitting to the shaft. Also check the capstan shaft for roughness or excessive dirt.

   b. Clean the capstan surface with a wipe or lint-free cloth moistened with water, or the special solution in the DECmagtape cleaning kit (TUC01). *Do not* use any cleaner other than water or DECmagtape cleaner to clean the capstan.

   c. Reposition the capstan and locking clamp onto the capstan motor shaft. The end of the motor shaft should be flush with the capstan's front surface. Tighten the locking clamp.

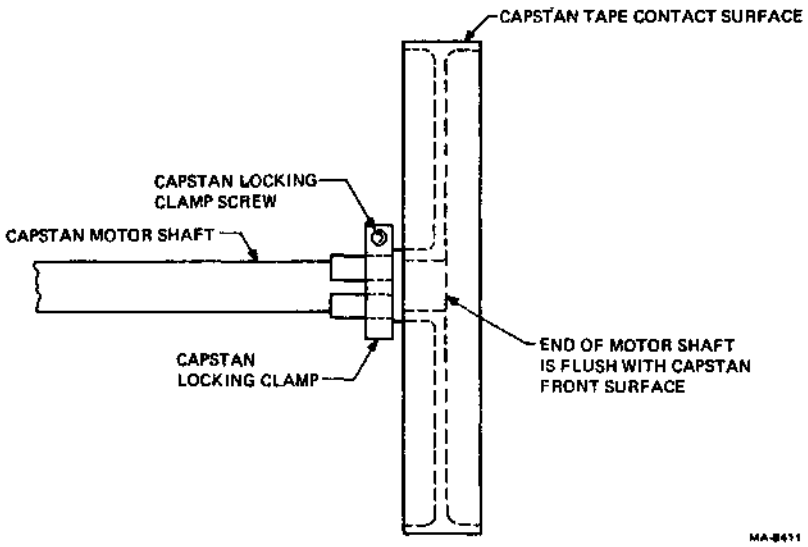


Figure 7-13 Capstan Positioning on Capstan Motor Shaft

2. Proceed as follows to inspect the tape path (Figure 7-12).

   a. Mount and thread a scratch tape, but do not load (reel motors are off, but tension arms are in approximate center of their swing).

   b. Make sure the tape is on the center of the capstan surface.

   c. Examine the tape from one roller to another. See if either tape edge has slack when compared to the other edge. Using a pen light to reflect from the tape improves this inspection. If an edge shows any slack, the roller at that point is not aligned correctly and should be replaced.

NOTE

The tension arm and rollers are preadjusted as a subassembly before mounting on the tape deck. If more than one arm assembly is replaced and the slackness persists, check that the headplate is seated correctly. Also check that no foreign material is jammed between the rear of the deckplate and the arm assembly.

   d. When the slackness is removed, proceed with the capstan alignment.

3. Proceed as follows to align the capstan.

NOTE

Adjusting screw 2 may cause the tape to start moving on the capstan while the tape is moving forward and reverse.

a. Load a scratch tape to BOT. Place the unit into maintenance mode. *Carefully* remove the clamp washers on the top of the fixed guides. A ceramic washer under the clamp washer comes off at the same time. Handle these washers with care; they are extremely hard and brittle. Also, note that the washer is beveled on one side. This beveled side must be mounted facing the tape when you reassemble the guides. When you remove the screw holding the washer, the guide remains mounted to the headplate.

b. Use test 50 and move the tape forward and reverse. Observe the relative position of the tape with respect to the capstan. Ideally, the tape should remain in the center of the capstan when tape is moving in either direction. If the tape moves on the capstan when you change directions, use an Allen wrench to turn gimbal screw 1 (Figure 7-14) about one turn (in either direction, remembering which direction you turned the screw). Perform this adjustment while the tape is moving. If the tape motion is reduced, you are turning the screw in the right direction. If motion increases, turn the screw in the opposite direction.

   Repeat the above procedure until there is no visible tape motion on the capstan. Then stop test 50.

c. Now use test 11 to run the tape in a steady state condition forward. If the tape is not tracking in the center of the capstan, turn gimbal screw 2 (Figure 7-14) as follows. If the tape is tracking too close to the deckplate, turn screw 2 counterclockwise. If the tape is tracking away from the deckplate, turn the screw in a clockwise direction.

d. Use test 11 to run the tape in a steady state condition, and press the two spring-loaded washers on the lower part of the fixed guides. Monitor the reference edge of the tape (the edge closest to the operator). It should track right at the edge of the top of both guides. If this does not happen, adjust screw 2.

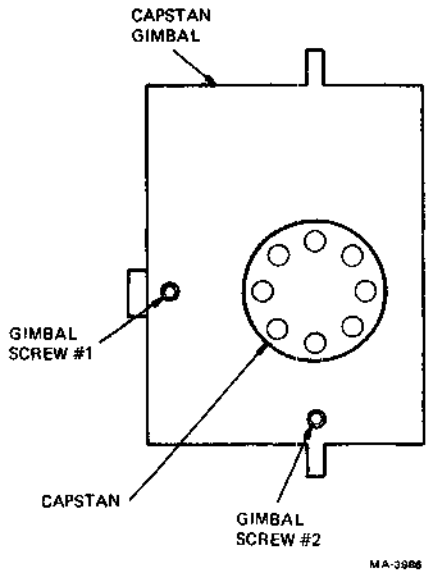


Figure 7-14 Capstan Gimbal Adjustment

e. Now use test 50 to run the tape forward and reverse. Again, press the spring-loaded washers and monitor the tape reference edge at the guide. If there is any movement of tape position, slightly readjust screw 1.

Repeat steps d and e for the best condition.

f. Reassemble the ceramic washer and clamp washer to the fixed guide, using 5 in.lbs. of torque.

CAUTION
Excessive torque will crack the ceramic washer.

7.6.2.9 BOT/EOT Adjustment – To adjust the BOT/EOT sensor (Figure 7-15), loosen the holding screw and position the sensor so the face of the sensor is parallel to a mounted tape.

With the BOT reflector strip positioned under the sensor, you should see a voltage of 3V or more at E1 pin 5 on G159. With the BOT reflector strip not under the sensor, the voltage should be 1V or less at E1 pin 5.

With the EOT reflector strip positioned under the sensor, you should see a voltage of 3V or more at E1 pin 7 on G159. With the EOT reflector strip not under the sensor, the voltage should be 1V or less at E1 pin 7.

If the adjustment of the sensor is correct and the signal levels are wrong, replace the sensor.

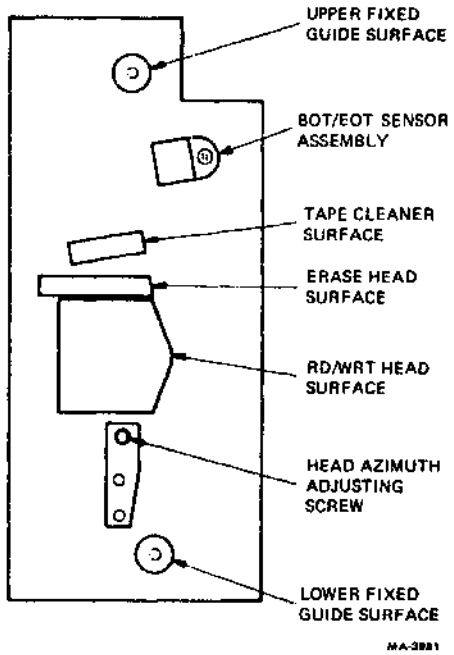


Figure 7-15 BOT/EOT Sensor and Head Skew Adjustment

7.6.2.10 Limit Switches Check – Use the microdiagnostics manual switch test (test 57) to check proper operation of the tension arm limit switches. (Refer to Paragraph 7.5.2 and Figure 7-3.)

7.6.2.11 Write Lock Assembly Adjustment – Adjust the write lock assembly as follows.

1. With no tape on the transport, the clearance between the outer edge of the snap lock hub and the actuator arm of the write lock assembly should be 0.100 inches to 0.350 inches, when measured with a feeler gauge.

2. To adjust the write lock assembly, loosen the two screws that fasten the assembly to the back of the deckplate and slide the assembly in the necessary direction.

3. Tighten the screws.

7.6.3 Electrical Checks and Adjustments
This section describes the electrical checks and adjustments for the TS11.

7.6.3.1 Capstan Null Adjustment – Adjust the capstan null as follows.

1. With the TS11 powered up, connect a DVM between the red lead of the capstan motor and ground.

2. Adjust R26 on G159 (marker N on the module) for 0 V ± 0.1 V.

7.6.3.2 Capstan Tachometer Alignment (Duty Cycle and Phasing)

NOTE
Tape should not be loaded when aligning the tachometer.

The optical tachometer provides the feedback signal to the capstan servo logic. The tachometer must be accurately aligned to ensure correct TS11 operation. (Refer to Figure 7-16.) Align the optical tachometer as follows.

CAUTION
The encoder disk is very sharp. Be careful to keep your fingers away from the disk while you are adjusting the assembly, or you could easily cut yourself.

1. Carefully remove the encoder dust cover. Make sure that the encoder disk is free of dirt and scratches, and is in the approximate center of the encoder base slot; take care that the disk is not rubbing against either inside slot edge. If the disk is rubbing (or not near the center), loosen the collar clamp and adjust the disk to near the slot center. Tighten the collar clamp screw.

2. Turn the G159 null potentiometer R26 (Figure 7-3) approximately four turns in the clockwise direction. Note that the capstan begins turning in a counterclockwise direction, as viewed from the front of the transport.

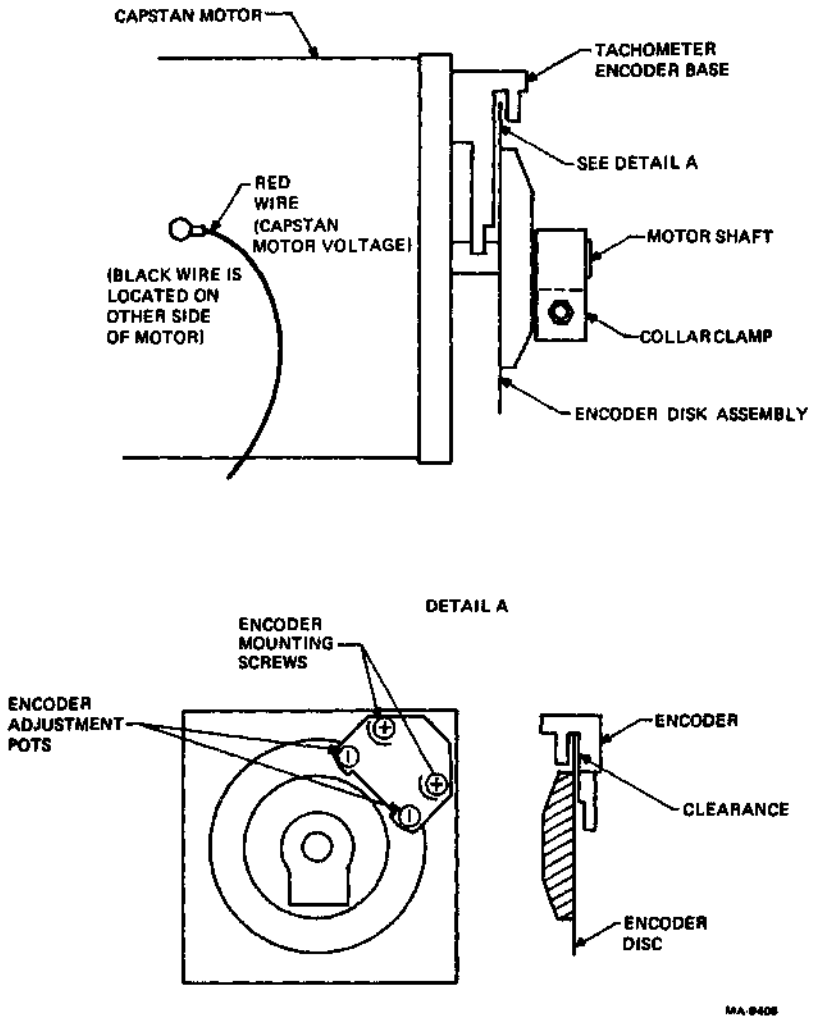


Figure 7-16 Capstan Tachometer Encoder Assembly

3. Set up a test oscilloscope as follows.

Channel 1	5 V/cm
Channel 2	5 V/cm
Vertical coupling	dc
Horizontal	100 μs/cm
Trigger	Channel 1, normal, positive slope, AC coupled
Mode	Chop

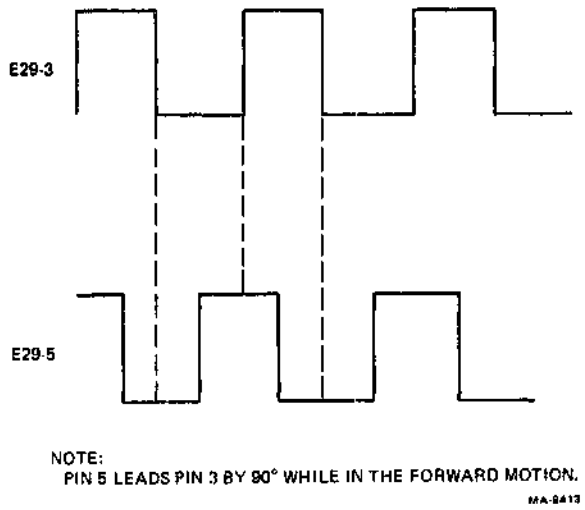


Figure 7-17 Capstan Tachometer Phase

4. Place a pin extender onto G159 chip E29. Place probe 1 onto E29 pin 3 and probe 2 onto E29 pin 5.

NOTE
At this time, the capstan motor is not running under servo control. Therefore, do not worry if speed error and jitter appear to be out of spec.

5. Place oscilloscope trace 1 at the top of the screen and trace 2 at the bottom. Adjust the two encoder assembly potentiometers (Figure 7-16) for 50 percent ±5 percent duty cycle square waves on both traces. Note that the potentiometers independently adjust each wave shape.

6. Slightly loosen the two encoder assembly mounting screws (Figure 7-16). Carefully move the assembly in or out (a very small amount) to obtain a 90 degree ±10 percent phase shift between the two traces, with pin 5 (probe 2) *leading* pin 3 (probe 1) as shown in Figure 7-17. Tighten the mounting screws.

7. Recheck the square waves and the phase shift. If either or both are out of tolerance, perform the adjustment(s) again.

8. If these adjustment tolerances cannot be met, replace the capstan motor assembly and perform the adjustments again.

9. Perform the capstan null adjustment (Paragraph 7.6.3.1).

10. Toggle S9 on G159 in alternating directions and observe the capstan motion. Check for 50 percent duty cycle square waves and the 90 degree phase shift in both forward and reverse directions. If they are not correct, perform the procedure(s) again. The trace for channel 2 will flip 180 degree from forward to reverse.

7.6.3.3 Capstan Speed Check – Check the capstan speed as follows.

1. Load a scratch tape and run test 50 in maintenance mode.

   Set up the oscilloscope as follows.

Channel 1	5 V/cm
Vertical coupling	dc
Horizontal	50 μs/cm
Trigger	Channel 1, normal, positive slope, AC coupled
Mode	Channel 1

2. Check at E29 pin 3 (Tach Phase 1) or E29 pin 5 (Tach Phase 2) on G159.

3. Check that the Tach Phase (1 or 2) signal is at a 250 μs period. The limits are 243 μs to 257 μs, in both forward and reverse (Figure 7-18).

4. Check the jitter on the leading edge of the signal (Figure 7-18). This is the same edge that the scope is triggered from. The jitter should be less than 12.5 μs +5 percent. If all capstan adjustments are good and jitter is more than 12.5 μs replace the capstan.

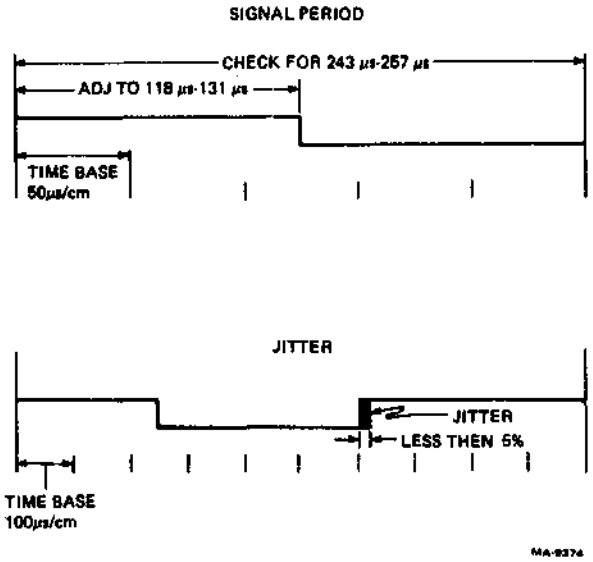


Figure 7-18 Capstan Speed Adjustment

7.6.3.4 Capstan Forward and Reverse Deceleration Adjustment – Adjust the capstan forward and reverse deceleration as follows.

1. Load a reel of tape.
2. Run test 13 in maintenance mode.
3. Observe the operator panel indicators EOT, BOT, DENS ERROR, and WRITE LOCK. EOT and BOT correspond to the forward direction; DENS ERROR and WRITE LOCK correspond to reverse. None of these indicators should be solid on or solid off. They should all flicker equally.
4. Adjust R87 on G159 for forward (F on the module).

   Adjust R95 on G159 for reverse (R on the module).

NOTE
This adjustment will drift if the test continues to run after the adjustment is made. Make this adjustment once and do not adjust for drift.

7.6.3.5 Read Preamplifiers – Adjust the read preamplifiers in maintenance mode, with the special test tape loaded.

Set up the oscilloscope as follows.

Channel 1	2 V/cm
Vertical coupling	dc
Horizontal	0.5 ms
Trigger	Auto Trig

1. Remove the preamplifier board shield.
2. Run test 54.
3. Connect the channel 1 scope probe to TP0 (Figure 7-19).
4. Adjust the bit weight zero gain potentiometer (Figure 7-19) for 10 V p-p + 0.25 V in the preamble section of the analog signal on the scope (Figure 7-20).
5. Move the scope probe to the remaining test points and adjust the corresponding gain potentiometers, including test point TPP (Figure 7-19).
6. Make sure the data section of the signals at TP0 through TP7 does not exceed 16.7 V p-p (Figure 7-20).
7. Reinstall the board shield.

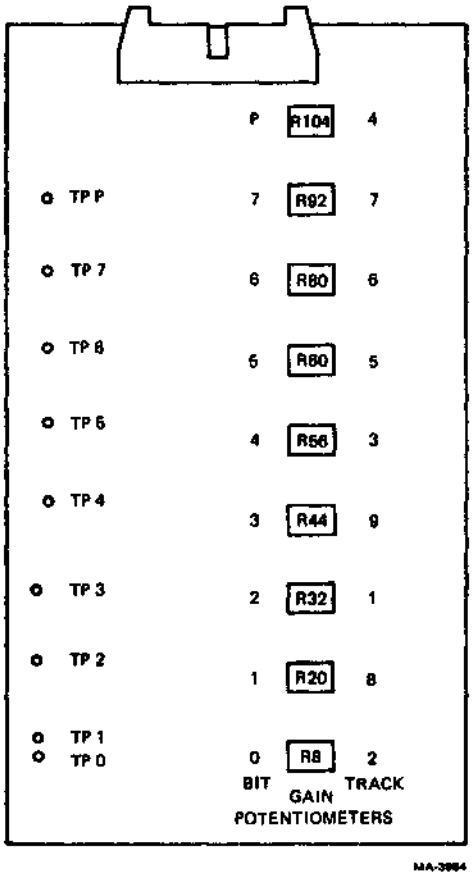


Figure 7-19 Read Preamplifier Locator

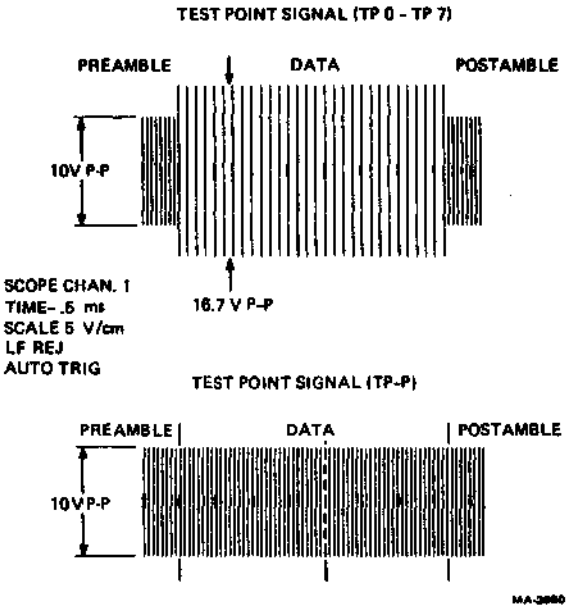


Figure 7-20 Read Preamplifier Adjustment

7.6.3.6 VCO Adjustment – Adjust the VCO in maintenance mode, with a special test tape loaded. Set up the oscilloscope as described for the threshold adjustment.

Channel 1	Monitor RDO on the maintenance panel.
Channel 2	Monitor VCO test point on M8922 (lower test point).

1. Run test 54. Adjust the potentiometer on M8922 for minimal level shift (dc between data and no data portions of the signal on channel 2 at 3 Vdc level). Refer to Figure 7-21.

7.6.3.7 Threshold Adjustment – Adjust the threshold in maintenance mode, with a special test tape loaded.

Set up the oscilloscope as follows.

Channel 1	5 V/cm
Channel 2	1 V/cm
Vertical coupling	dc
Horizontal	2 ms/cm
Trigger	Channel 1, normal, positive slope
Mode	Alternate
Channel 1	Monitor RDO on the maintenance panel.
Channel 2	Monitor pin A3A1 on the backplane.

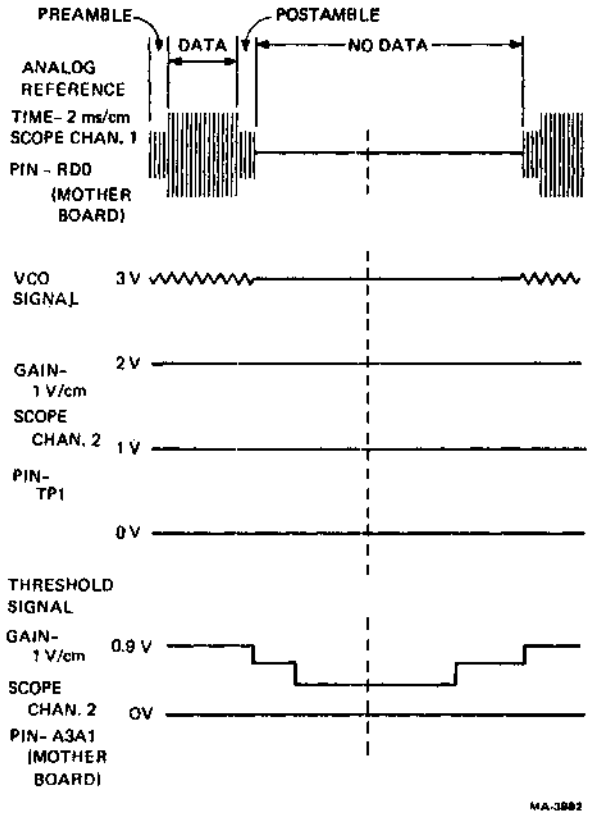


Figure 7-21 VCO and Threshold Waveforms

1. Run test 54 and verify that pin A3A1 is 0.9 V ± 0.1 V during the data section of the analog signal (Figure 7-21).

2. Adjust the top potentiometer (R46) of the M8923 if needed.

7.6.3.8 Skew Meter Adjustment – Adjust the skew meter as follows.

NOTE

This adjustment does not affect any operational characteristics of the TS11. The skew meter is a circuit used by the TS11 microdiagnostics to determine electrically if the head is skewed properly. Check the skew meter before the head is deskewed.

1. Run test 31 in maintenance mode.

2. The operator panel indicators should not be on for this adjustment. However, it is helpful to center the adjustment.

3. To center the adjustment, turn R49 (bottom potentiometer) on M8923 until either the BOT or EOT indicators turn on.

4. Turn R49 in the opposite direction, counting the number of turns until the other indicator turns on.

5. Turn R49 back half the amount of turns counted in step 4. All operator panel indicators should turn off.

NOTE

During this adjustment, there will be some delay between the time R49 is adjusted and the indicators change.

7.6.3.9 Head Skew Check and Adjustment – Check the head skew as follows.

NOTE

Check the skew meter (Paragraph 7.6.3.8) and tape path alignment (Paragraph 7.6.2.8) before doing this adjustment.

Check

1. Load a master skew tape.

2. Run test 50 in maintenance mode.

3. Observe the operator panel; all indicators should be off. The following indicators show errors.

   1/EOT – Forward skew error
   2/BOT – Reverse skew error

Adjustment

1. Load a master skew tape.

2. Run test 51 in maintenance mode to check the forward skew, or test 52 to check the reverse skew.

3. Connect the channel 1 scope probe to the skew out test point on the maintenance panel. Adjust the head azimuth screw (Figure 7-15) to meet these voltages.

Forward	At or near 0 V (2.5 V max)
Reverse	At or near 0 V (3.0 V max)

4. Run test 50 to ensure there are no errors.

Alternate Adjustment

Set up the oscilloscope as follows.

Channel 1	2 V/cm
Vertical coupling	dc
Horizontal	1 μs/cm
Trigger	Channel 1, normal, positive slope
Channel 1	Monitor B3V1 (packet signal).

1. Load a master skew tape.

2. In maintenance mode, run test 51 and test 52 to check forward and reverse skew respectively.

3. Make sure that the packet signal is 2.5 μs or less in the forward direction and 3.0 μs or less in the reverse direction. Adjust the head azimuth screw (Figure 7-15) to meet these specifications.

4. Run test 50 to ensure there are no errors.

7.7 REMOVAL AND REPLACEMENT PROCEDURES

This section outlines the removal and replacement procedures for the TS11 component assemblies. Refer to Table 7-10 for the adjustments that are necessary when you replace a component. Some components have a single removal and replacement procedure.

NOTE

The capstan, capstan motor/tachometer, tension arms, lower fixed guide, and head assembly directly affect the path of the tape as it moves through the tape transport. If you replace any of these items, you must align the tape path (Paragraph 7.6.2.8).

Table 7-10 Component Replacement and Adjustment Cross-Reference

Component Replaced	Adjustment to Check or Perform
Reel motor	Hub height Reel fitting (upper) Write ring (upper)
Capstan motor assembly	Capstan motor null adjustment Capstan deceleration Tape path alignment
Capstan wheel	Tape path alignment
Snap lock hub	Hub height Reel fitting Write ring
Fixed hub	Hub height
Headplate assembly	Tape path alignment Preamplifier Threshold Head skew
Tension arm transducer	Transducer null Tape tension
Tension arm	Transducer null Tape tension Tape path alignment
Buffer arm	Tape path alignment
Write lockout assembly	Write lockout assembly
Limit switch	Limit switch
BOT/EOT sensor	BOT/EOT sensor
Power supply	Voltage (+5 V)
G159	Capstan motor null Capstan deceleration
G057	Preamplifier
G158	Transducer null
M8922	VCO
M8923	Skew limit and threshold

7.7.1 Module Removal and Replacement

This section describes module removal and replacement procedures.

7.7.1.1 Double-Height Module – Remove any double-height module as follows.

1. Remove power from the TS11.
2. After gaining access to the rear of the TS11, remove the module retaining bar.
3. The modules are numbered 1 to 15 (Figure 7-22).
4. To remove a module, grasp the plastic handle and pull straight out.
5. When removing M8962 or M8922, remove the interconnect jumper block first.
6. To install a module, align the module with the correct slots in the logic rack and push firmly straight in.
7. Reinstall the retaining bar.

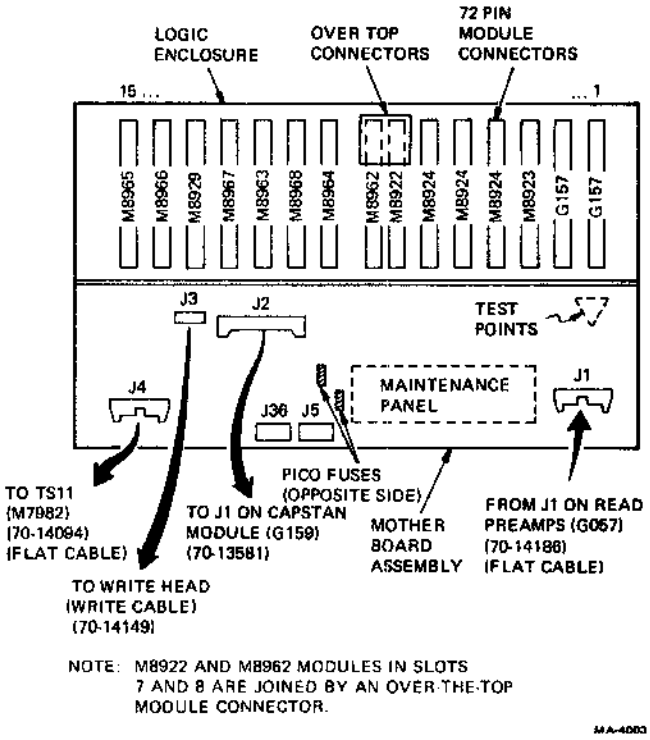


Figure 7-22 Logic Rack (Rear View)

7.7.1.2 G158 Reel Servo Board – Remove the G158 reel servo board as follows.

1. Remove power from the TS11.
2. Open the front door. Unlock and swing open the transport.
3. Disconnect plug connectors J6/P6, J10/P10, J11/P11, J12/P12, J13/P13, J14/P14, J15/P15, and J16/P16 from G158 (Figure 7-3).
4. Release the flat cable from the cable clip on the triac heat sink cover.
5. Remove the four screws holding G158 to the deckplate.
6. Remove G158.
7. Remove the triac heat sink cover containing the flat cable clip and warning label.
8. To install G158, reverse steps 3 through 7.
9. Reapply power to TS11.

7.7.1.3 G159 Capstan Servo Board – Remove the G159 capstan servo board as follows.

1. Remove power from the TS11.
2. Open the front door. Unlock and swing open the transport.
3. Disconnect plug connectors J1/P1, J2/P2, J3/P3, J4/P4, and J5/P5 from G159 (Figure 7-3).
4. Remove the four screws holding G159 to the mounting brackets.
5. Remove G159.
6. To install G159, reverse steps 3 and 4.
7. Reapply power to the TS11.

7.7.1.4 G057 Read Amplifier Board – Remove the read amplifier board as follows.

1. Remove power from the TS11.
2. Open the front door. Unlock and swing open the transport.
3. Remove the board shield covering G057.
4. Disconnect plug connectors J1/P1 and J2/P2 from G057 (Figure 7-3).
5. Remove the three screws holding G057; take care not to lose the insulating washers on the back of the board, or under the screw heads.
6. Remove G057.

7. To install G057, reverse steps 3 through 5. Make sure the insulating washers are between the back of the board and the metal standoffs, and under the correct screw heads.

8. Reapply power to the TS11.

NOTE
If you replace a ROM module, make sure to perform the bring-up procedure (Paragraph 7.5.3) and record the indications for use in troubleshooting.

7.7.2 Snap Lock Hub Assembly (Supply Reel)

This section describes how to remove, replace, and rebuild the snap lock hub assembly.

7.7.2.1 Removal – Remove the snap lock hub as follows.

1. Remove power from the TS11.

2. Remove the tape reel, if mounted.

3. Lift the locking tab and remove the index screw from the outer hub.

4. Grasp the outer hub and rotate it counterclockwise to unthread the hub from the hub adapter. Remove the outer hub.

5. Remove the latch lever and the thrust washer from the outer hub.

6. Remove the 1-3/8 inch nut from the hub adapter with a 1-3/8 inch socket, while holding the inner hub in place with a spanner wrench.

7. Remove the inner hub and woodruff key. The woodruff key is the small piece of metal in the groove of the hub adapter.

NOTE
If hub adapter does not have to be removed, skip steps 8 and 9.

8. Remove the motor and motor spacer from the casting (Paragraph 7.7.10).

9. With the motor removed, unscrew the two Allen screws that hold the hub adapter to the motor shaft. Remove the hub adapter.

7.7.2.2 Replacement – Install the snap lock hub as follows.

1. Remove power from the TS11.

2. With the reel motor removed from the transport casting, assemble the hub adapter to the motor shaft by sliding it on and lining up the two setscrews with the two flat surfaces on the shaft. Use a feeler gauge to set the spacing between the hub adapter and the motor mounting surface. Once the spacing (0.8 mm or 0.031 inches) is established, tighten the two setscrews (Figure 7-9).

3. Position the motor spacer on the motor mounting surface, making sure to align the mounting holes of the spacer with the mounting holes of the motor.

4. Install the motor and motor spacer on the deckplate, using four 1/4-20 × 1 inch hex screws and four 1/4 inch split washers.

5. Slide four 0.010 circular metal shims (part of the hub kit) onto the hub adapter.

6. Slide the inner hub onto the hub adapter as follows.

   a. Make sure the woodruff key in the hub adapter is in place.

   b. Line up the slot on the inner hub with the woodruff key in the hub adapter, and slide the inner hub into place.

7. Thread the 1-3/8 inch nut onto the adapter and finger tighten.

8. Adjust the hub height (Paragraph 7.6.2.1).

9. Using a 1-3/8 inch socket and a torque wrench (see special tools list), tighten the 1-3/8 inch nut onto the hub adapter, while holding the inner hub in place with a spanner wrench. Tighten to a torque of 20 ft. lb (24 N.m).

10. Lightly lubricate the O ring chamfer on both outer and inner hub pieces with silicone grease.

11. Place the O ring over the outer hub assembly.

12. Lubricate the thrust washer with silicone grease before sliding it over the latch lever shaft.

13. Install the shaft through the outer hub and thread it into the adapter, making sure that the O ring is in place.

14. Hold the inner hub while rotating the outer hub clockwise, until the outer hub bottoms. Continue to hold the inner hub and rotate the outer hub counterclockwise until the latch lever closes smoothly.

15. Wipe away any excess grease from the outer surfaces of the hub assembly and mount a number of tape reels, fine tuning this rotational adjustment to ensure a constant engagement of all the reels.

16. Install the index screw through the outer hub into the inner hub. Locate the nearest hole in the inner hub before screwing it in (Figure 7-9).

17. Verify that the WRITE LOCK switch adjustment is still within tolerance (Paragraph 7.6.2.11).

7.7.2.3 Rebuilding – If the snap lock hub requires rebuilding, use the following procedure.

1. Perform steps 1 through 4 of Paragraph 7.7.2.1.

2. Remove the old O ring from around the outer hub and replace it with the new O ring from the rebuild kit.

3. Remove the old thrust washer from the front of the outer hub and replace it with the new thrust washer from the rebuild kit.

4. Replace the hub assembly as detailed in Paragraph 7.7.2.2, steps 10 through 16.

7.7.3 Take-Up Reel

This section describes how to remove and replace the fixed take-up reel.

7.7.3.1 Removal – Remove the take-up reel as follows.

1. Remove power from the TS11.
2. Remove the three phillips screws from the front of the reel (Figure 7-8).
3. The reel now comes apart in four pieces: trimplate, front flange, inner hub, and rear flange.

NOTE
Step 4 is required only when replacing the lower motor or the hub casting itself. Otherwise, you are finished removing the fixed take-up reel with step 3.

4. Remove the hub casting by loosening the two Allen screws and sliding the casting off the reel motor shaft.

7.7.3.2 Replacement – Install the take-up reel as follows.

NOTE
If the hub casting has not been removed, start at step 3.

1. Slide the hub casting onto the lower motor shaft.
2. Adjust the hub height (Paragraph 7.6.2.2).
3. Install the rear flange (Figure 7-8) over the hub casting.
4. Place the center ring onto the hub casting.
5. Install the front flange.
6. Place the trimplate over the front flange and secure it with three phillips screws used in step 2 of removal. Do not tighten.
7. Rotate the front and rear flanges until the flange holes line up with each other.
8. Tighten the three phillips screws.

7.7.4 Capstan Wheel

Remove the capstan wheel (PN 74-18010) as follows.

1. Remove power from the TS11.
2. Remove the capstan by loosening the locking clamp screw (Figure 7-13) with an Allen wrench and by sliding the wheel and clamp off the capstan motor shaft.
3. Check the end of the shaft for burrs. If any burrs exist, remove them with an abrasive cloth (crocus or emery).

4. Install the new capstan wheel by placing the clamp over the split ring and sliding the wheel over the shaft. Make sure the outside surface of the capstan wheel is flush with the end of the capstan motor shaft.

5. Tighten the clamp on the shaft.

6. Check tape path alignment (Paragraph 7.6.2.8).

7. Run microdiagnostics to completion.

7.7.5 Capstan Motor and Tachometer

Remove the capstan motor and tachometer assembly (PN 70-16677-00) as follows.

NOTE

The capstan motor and tachometer is a single assembly; you cannot replace the tachometer alone.

1. Remove power from the TS11.

2. Open the front door. Unlock and swing open the transport.

3. Unplug the black and red wires from the capstan motor. Remember where the wires were connected.

4. Disconnect the tachometer signal cable at in-line plug P9/J9.

5. Remove the capstan wheel (Paragraph 7.7.4).

6. Remove the front bezel (Paragraph 7.7.11) and take-up reel assembly (Paragraph 7.7.3.1).

7. While supporting the motor from the rear, remove the four phillips screws from the front of the casting that hold the motor and tachometer assembly to the gimbal mounting surface.

8. Install the new motor and tachometer assembly by reversing steps 3 through 7. Make sure the motor cable and cable clamp are near the top of the motor when installed.

NOTE

When you replace the older style capstan motor with the Mate-N-Lock 4-pin connector, you must use a special adapter (PN 70-17511-00).

9. Align the tape path (Paragraph 7.6.2.8).

10. Run microdiagnostics to completion.

7.7.6 Lower Roller Guide

Remove the lower roller guide (PN 70-15475) as follows.

NOTE

You can only replace the lower roller guide; the upper guide is part of the head assembly.

1. Remove the front bezel (Paragraph 7.7.11.1) and take-up reel (Paragraph 7.7.3.1).
2. Remove the lower roller guide assembly by removing the two phillips screws that hold the assembly to the casting (Figure 7-8).
3. Install a new lower roller guide, using the two screws removed in step 2.
4. Install the front bezel (Paragraph 7.7.11.2) and take-up reel (Paragraph 7.7.3.2).
5. Check the tape path alignment (Paragraph 7.6.2.8.)
6. Run microdiagnostics to completion.

7.7.7. Headplate Assembly

Remove the headplate assembly as follows.

NOTE

The components of this assembly are not field replaceable. Do not attempt to replace or align the read/write head, erase head, tape cleaner, or any of the tape guides. If you suspect any problems with the above parts, replace the entire headplate assembly.

1. Remove power from the TS11.
2. Open the front door. Unlock and swing open the transport.
3. Unplug the read, write, and erase head cables, and BOT/EOT sensor cable.
4. Unplug the upper cable connected to the G057 read preamplifier module.
5. Remove the G057 module and housing assembly by removing the two phillips screws.
6. Support the headplate assembly and remove the two phillips screws at the front of the casting, holding it in place.
7. Remove the BOT/EOT sensor from the headplate and install on the new headplate.

NOTE

It is possible to install the headplate assembly upside down. Make sure you mount it in the correct position (read/write head points to the right).

8. Mount the new headplate assembly, using the two screws removed in step 6.

9. Mount the G057 module and housing assembly, using the screws removed in step 5.

10. Plug in the upper G057 cable.

11. Plug in the read, write, and erase head cables, and the BOT/EOT sensor cable.

12. Align the tape path (Paragraph 7.6.2.8).

13. Adjust the read preamplifiers (Paragraph 7.6.3.5).

14. Adjust the skew (Paragraph 7.6.3.9).

15. Adjust the threshold (Paragraph 7.6.3.7)

16. Run microdiagnostics to completion.

7.7.8 BOT/EOT Sensor Assembly

Remove the BOT/EOT sensor assembly (PN 12-11720) as follows.

1. Remove power from the TS11.

2. Open the front door. Unlock and swing open the transport.

3. Locate the sensor mounted on the headplate assembly (Figure 7-15).

4. Disconnect the sensor assembly from its cable harness by separating the in-line plug and connector.

5. Loosen and remove the mounting screw, being careful not to come in contact with any of the head surfaces.

6. Remove the sensor assembly.

7. Mount the new sensor assembly, using the screw removed in step 5.

8. Reconnect the sensor assembly cable to its wiring harness by joining the in-line plug pieces.

9. Align the new sensor (Paragraph 7.6.2.9).

7.7.9 Lower Reel Motor Assembly

The reel motor, brake, and fan are one assembly. You cannot replace the components individually. Remove the lower reel motor assembly (PN 70-13578) as follows.

1. Remove power from the TS11.

2. Remove the take-up reel flanges and take-up reel hub assembly (Paragraph 7.7.3.1).

3. Open the front door. Unlock and swing open the transport.

WARNING

There is 115 Vac applied to connector J12 on G158. Make sure you remove power from the TS11 before touching G158.

4. Unplug the motor control and power cable (J13) and the reel motor fan power cable (J14) on G158. Also disconnect the ground wire from the deckplate.

CAUTION

When removing these four screws, you must support the reel motor assembly from the rear. If support is not supplied, the motor and/or spacers will fall when the screws are removed.

5. Remove the four hex screws that hold the lower motor to the transport (Figure 7-8).

6. Remove the reel motor.

CAUTION

Due to motor spacing, the upper reel motor is mounted with 1 inch screws, while the lower motor is mounted with 3/4 inch screws. Do not use any other size screws, or damage to the motor will result.

7. Install the new lower reel motor assembly, using the screws removed in step 5.

8. Install the hub casting and the flanges (Paragraph 7.7.3.2).

9. Plug in the motor control and power cable (J13) and the reel motor fan power cable (J14) removed in step 4 to G158. Also connect the ground wire to the deckplate.

10. Check the hub height adjustment (Paragraph 7.6.2.2).

7.7.10 Upper Reel Motor Assembly

Remove the upper reel motor assembly (PN 70-13578) as follows.

1. Remove power from the TS11.

2. Remove the snap lock hub assembly (Paragraph 7.7.2.1).

3. Open the front door. Unlock and swing open the transport.

WARNING

There is 115 Vac applied to connector J12 on G158. Make sure you remove power from the transport before touching G158.

4. Unplug the motor control and power cable (J16) and the reel motor fan power cable (J15) on G158. Also disconnect the ground wire from the deckplate.

CAUTION

When removing these four screws, you must support the reel motor assembly from the rear. If support is not supplied, the motor and/or spacers will fall when the screws are removed.

5. Remove the four hex screws that hold the upper motor to the transport (Figure 7-8).

6. Remove the reel motor and motor spacer.

CAUTION

Due to motor spacing, the upper reel motor is mounted with 1 inch screws, while the lower motor is mounted with 3/4 inch screws. Do not use any other size screws, or damage to the motor will result.

7. Install the upper reel motor and motor spacer assembly, using the screws removed in step 5.

8. Install the snap lock hub assembly (Paragraph 7.7.2.2).

9. Plug in the motor control and power cable (J16) and the reel motor fan power cable (J15) removed in step 4 to G158. Also connect the ground wire to the deckplate.

10. Check the hub height adjustment (Paragraph 7.6.2.1).

7.7.11 TS11 Bezel

This section describes how to remove and replace the TS11 bezel.

7.7.11.1 Removal – Remove the TS11 bezel as follows.

1. Remove tape from the drive.

2. Remove the take-up reel (Paragraph 7.7.3.1).

3. Remove the capstan wheel (Paragraph 7.7.4).

4. Swing the deckplate open and remove the nine screws (eight on some drives) from the rear of the deckplate.

5. Remove the bezel by lifting away from the front of the deckplate.

NOTE

On the new style deckplate, bezel mounting screws are located on front.

7.7.11.2 Replacement – Install the TS11 bezel as follows.

1. Set the bezel on the front of the deckplate.

2. Secure the bezel to the deckplate by fastening the nine screws (eight on some drives) from the rear of the deckplate.

3. Install the capstan wheel (Paragraph 7.7.4).

4. Install the take-up reel (Paragraph 7.7.3.2).

5. Check the tape path alignment (Paragraph 7.6.2.8).

7.7.12 Tension Arm

This section describes how to remove and replace the tension arm.

7.7.12.1 Removal – Remove the tension arm as follows.

NOTE
You remove and replace tension arms as an assembly. Do not remove or replace individual parts.

1. Remove the take-up reel (Paragraph 7.7.3.1), the capstan wheel (Paragraph 7.7.4), and the front bezel (Paragraph 7.7.11.1).

2. Hold the upper end of the upper tension spring securely with your index finger (thumb against the edge of the transport). While holding the spring, loosen and remove the adjusting block screw in the upper spring tension block to remove the spring.

3. Move the tension arm to its near vertical position, against the upper stop.

4. Unhook the transducer cable from the locating pin in the pivot arm housing.

5. Unscrew the three phillips screws (from the front) that hold the tension arm assembly to the deckplate.

6. Rotate the assembly 90 degrees (to the casting), then remove the assembly from the rear through the clover-shaped opening in the casting.

7.7.12.2 Replacement – Install the tension arm (PN 70-14014) as follows.

1. Insert the tension arm in the casting from the rear, through the clover-shaped opening and position it over the three mounting holes. Mount the arm with the three screws used in step 5 of the removal procedure. Make sure the hole in the pivot arm housing opens toward the tension block assembly. This ensures that the cable does not rub against the pivot arm housing.

2. Return the tension arm to near vertical position.

3. Reconnect the transducer cable to the locating pin in the pivot arm housing.

4. Again, tensioning the spring by hand, pull the spring toward the tension adjusting block and begin turning the adjusting block screw into the spring adjusting block.

5. The upper tension arm should rest against its upper limit switch (in a near vertical position).

6. Perform the tension arm coarse adjustment (Paragraph 7.6.2.6).

7. Perform the tension arm fine adjustment (Paragraph 7.6.2.7).

8. Install the front bezel (Paragraph 7.7.11.2) and take-up reel (Paragraph 7.7.3.2).

9. Perform the transducer coarse adjustment (Paragraph 7.6.2.3).

10. Perform the transducer fine adjustment (Paragraph 7.6.2.4).

11. Check the tape path alignment (Paragraph 7.6.2.8).

12. Run microdiagnostics to completion.

7.7.13 Tension Arm Transducer

This section describes how to remove and replace the tension arm transducer.

7.7.13.1 Removal – Remove the tension arm transducer as follows.

1. Remove power from the TS11.

2. Unhook the transducer cable from the associated tension arm (Paragraph 7.7.12.1).

3. Disconnect the appropriate plug from G158.

   J10 – lower transducer
   J11 – upper transducer

4. Loosen the screw holding the transducer in the transducer block.

5. Slide the transducer from the transducer block.

7.7.13.2 Replacement – Install the tension arm transducer as follows.

1. Install the new transducer in the transducer block.

2. Insert (do not tighten) the screw holding the transducer.

3. Plug in the appropriate cable on the G158.

4. Connect the transducer cable to the associated tension arm (Paragraph 7.7.12.2).

5. Perform the tension arm coarse adjustment (Paragraph 7.6.2.6).

6. Perform the transducer coarse adjustment (Paragraph 7.6.2.3).

7. Perform the tension arm fine adjustment (Paragraph 7.6.2.7).

8. Perform the transducer fine adjustment (Paragraph 7.6.2.4).

9. Check the tape path alignment (Paragraph 7.6.2.8).

7.7.14 Write Lock Assembly

Remove the write lock assembly (PN 70-16318) as follows.

1. Remove power from the TS11.

2. Open the front door. Unlock and swing open the transport.

3. Separate the in-line cable Mate-N-Lok connector P7/J7 on the write lock assembly.

4. Remove the two phillips screws holding the write lock assembly to the rear of the deckplate casting.

5. Install a new write lock assembly, using the screws removed in step 4.

6. Reconnect the in-line cable connector P7/J7.

7. Adjust the write lock assembly (Paragraph 7.6.2.11).

7.7.15 Reel Motor Capacitors

Remove a reel motor capacitor (PN 10-17233) as follows.

1. Remove power from the TS11.

WARNING

Make sure that you remove power from the transport. There is 115 Vac applied to G158, which you will be working near.

2. Open the front door. Unlock and swing open the transport.

3. Disconnect the two black wires connected to the capacitor with Faston connectors.

4. Remove the four phillips screws holding the capacitor mounting plate to the rear of the deckplate.

5. Mount the new capacitor with the four screws removed in step 4.

6. Connect the two black wires to the new capacitor.

NOTE

If you have the old style 40 μF capacitors in the TS11, replace with 50 μF capacitors (330 V, PN 10-17233).

7.7.16 Limit Switches

Remove a limit switch (PN 70-15666) as follows.

1. Remove power from the TS11.

2. Open the front door. Unlock and swing open the transport.

3. Locate the switch you are replacing.

4. Disconnect the two wires connected to the switch by Faston connectors.

5. Remove the phillips screw holding the limit switch to the rear of the casting.

6. Install a new limit switch using the screw removed in step 5.

7. Connect the two wires to the appropriate terminals on the new switch.

8. Check the limit switch adjustment (Paragraph 7.6.2.10).

7.7.17 Operator Control Panel Bulbs

Replace defective control panel bulbs (PN 12-12716) as follows.

1. Remove power from the TS11.
2. Firmly grasp the switch cover of the bulb you are replacing with the thumb and forefinger.
3. Pull firmly, straight out. Pulling at an angle may damage the switch cover or the switch locating tab.
4. Remove the defective bulb from its socket by pulling the bulb straight out.
5. Insert a new bulb in the socket and push straight in until the bulb is seated.
6. Replace the switch cover by keying it with the locating tab and pushing the cover straight on.