DEC-11-HRPCA-C-D

RP11-C disk pack drive controller maintenance manual

digital equipment corporation · maynard, massachusetts

1st Edition, December 1972
2nd Printing (Rev) April 1973
3rd Printing (Rev) August 1973
4th Printing October 1973
5th Printing August 1974

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CHAPTER 1
INTRODUCTION AND DESCRIPTION

1.1 INTRODUCTION

This manual describes the RP11-C Disk Pack Drive Controller, manufactured by Digital Equipment Corporation. The RP11-C, shown in Figure 1-1, interfaces with any PDP-11 Programmed Data Processor, via the Unibus, to control up to eight RP03 Disk Pack Drives.

Figure 1-1 RP11-C Disk Pack Controller

1.1.1 Scope of Manual

The purpose of this manual is to provide DEC Field Service and customer maintenance personnel with sufficient installation, operation, and servicing information to install and maintain the RP11-C. Because the RP11-C Disk Pack Drive Controller is intended specifically for use with the RP03 Disk Pack Drives, a brief description and summary of RP03 operation is included in this manual to provide an overall understanding of disk pack system operation. However, complete installation and servicing information on the RP03 is provided in the separate manual listed in the table of related documentation.

1.1.2 Related Documentation

Table 1-1 lists related documentation that supplements the information contained in this maintenance manual.

1.2 DISK PACK SYSTEM

Figure 1-2 shows the major components of a PDP-11 disk pack storage system. The processor and memory components can be any of several types in the PDP-11 family, since all of these components are equipped with the standard Unibus interface. Functional descriptions of these components are provided in related technical manuals. The following paragraphs describe the operational characteristics of the RP02P Disk Pack, the RP03 Disk Pack Drive, and the RP11-C Disk Pack Drive Controller.

1.2.1 RP02P Disk Pack

The RP02P Disk Pack, shown in Figure 1-3, is the recording medium used with the RP11-C system, and is designed to mount on an RP03 Disk Pack Drive. The RP02P comprises 11 aluminum disks coated with magnetic oxide and mounted 1/2 in. apart on a common hub. Information is recorded on the 20 inner surfaces.

Table 1-1
Related Documentation

Title	Document Number
Model 715D Disk Storage Drive Operation, Service, and Diagrams; Information Storage Systems, Inc. (RP03 Disk Pack Drive)	UD002341-1
PDP-11 Peripherals and Interfacing Handbook	112.01071.1854
H740D Power Supply Maintenance Manual	DEC-11-H740A-A-D
861-A,B,C Power Controller	DEC-00-H861A-A-D

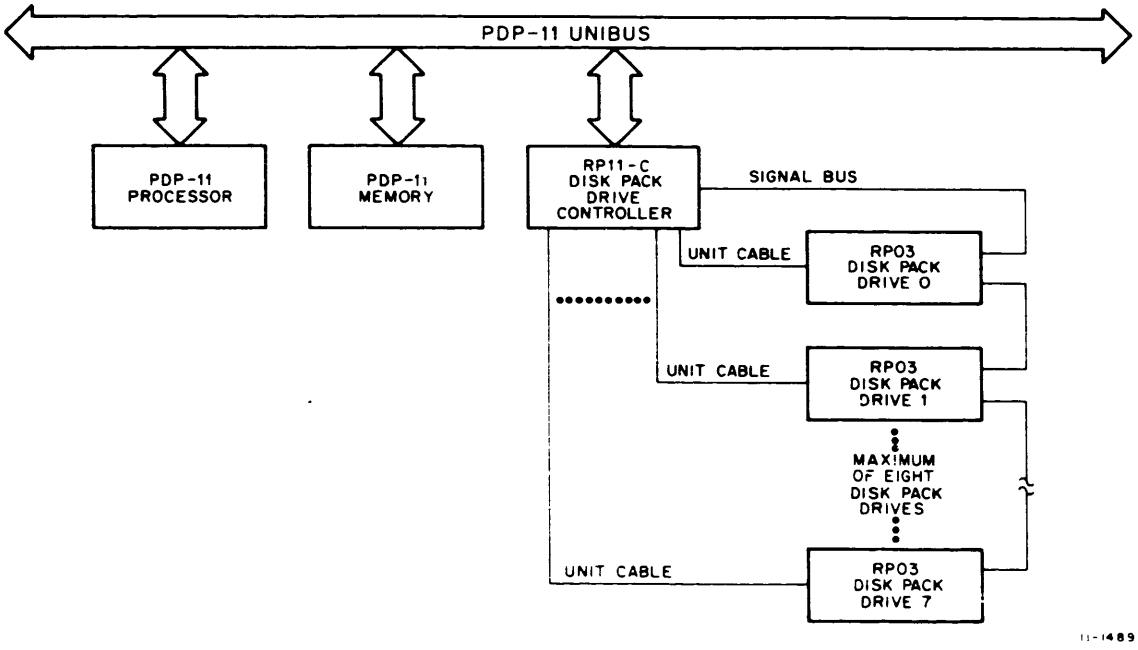


Figure 1-2 PDP-11 Disk Pack System, Block Diagram

The bottom disk is not used for recording and is notched to produce timing pulses for synchronization with the controller. This bottom disk contains 20 evenly spaced notches and a 21st notch called the index. The drive is equipped with an LED (light-emitting diode) and a phototransistor sensor that senses these notches. Circuitry within the disk pack drive divides these pulses by 2 and sends the resultant 10 sector pulses to the controller. An additional circuit separates the index pulse.

Each of the 406 cylinders on each of 20 tracks is formatted into 10 sectors. The sector formats are written onto the RP02P surface by means of an FP11-C Write Format function.

The basic format of the disk pack is such that at the beginning of each sector there is a preamble and a header identification area. The header identifies this specific area of the disk by cylinder, surface, and sector. The header is followed by a gap and a second preamble, a data area, a longitudinal parity (LP) word, and a postamble (Figure 1-4).

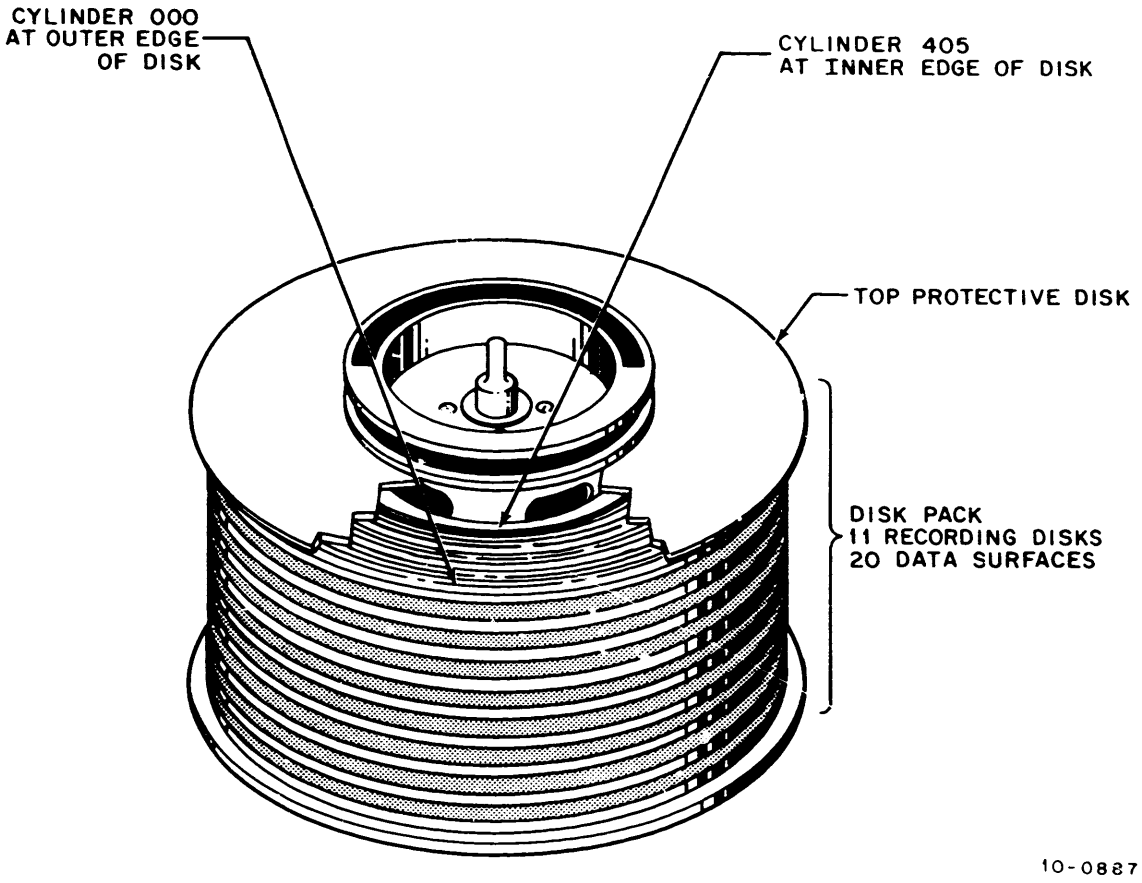


Figure 1-3 RP02P Disk Pack

1.2.2 RP03 Disk Pack Drive

The RP03 Disk Pack Drive is the mechanism controlled by the RP11-C controller. It comprises two major subassemblies: the spindle driving mechanism and the head positioning system.

The spindle driving mechanism is made up of an ac motor, mounted below the baseplate, that transmits a rotation of 2400 r/min to the disk pack by driving a conical spindle through a drive pulley and belt loop. The spindle secures the pack with a locking shaft within the spindle and washers below the spindle pulley. A mechanical lock is actuated by raising the cover. A pack-on switch disables the spindle drive motor power until a pack is installed.

The head positioning system consists of a linear positioning motor that moves a T-bar tower along a horizontal carriage, either toward or away from the center of drive motor rotation. When the T-bar is fully retracted, the disk pack may be removed once it has been stopped and latched by opening the access cover. The T-bar is used to mount 20 back-to-back head assemblies that are unloaded by camming action when the linear motor is fully retracted. An electronic detenting mechanism stops the head assembly over the selected cylinder position.

The drive provides a means of monitoring head position, drive speed, and rotational position. Head position is monitored by an assembly that consists of two glass plates between a photodiode assembly and its light source. One glass plate is stationary while the other is attached to the T-bar. Because of a unique set of lines etched into the glass, the output of the photodiode assembly is a sine/cosine function as the T-bar moves. This waveform is converted to a series of pulses representative of head cylinder crossings. This signal is fed to an up/down counter in the RP03 logic. In this way, the RP03 logic is able to keep up with instantaneous head position. Drive speed and rotational position

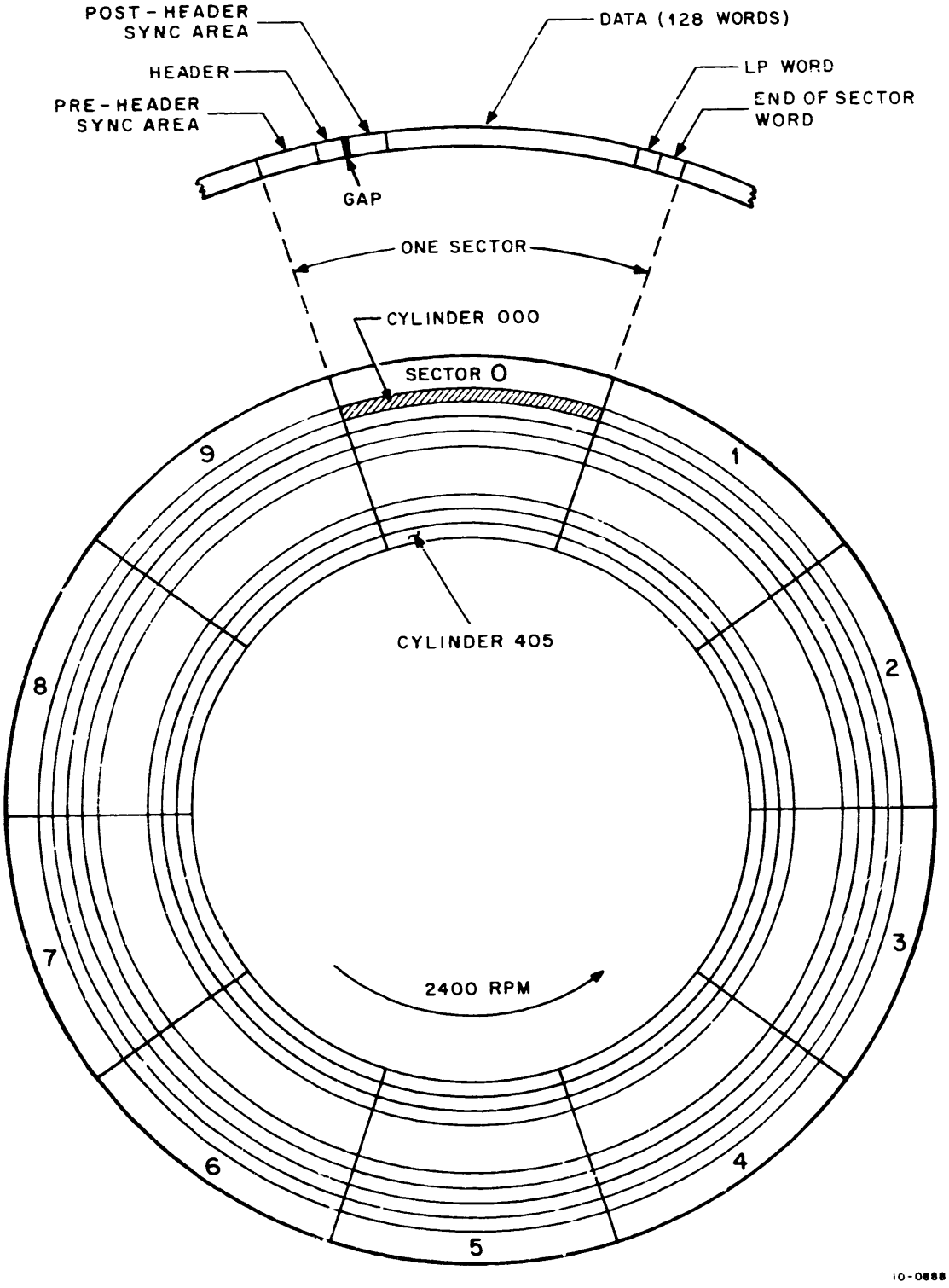


Figure 1-4 Format of Disk Surface

are monitored by a phototransistor and LED assembly that senses slots in the bottom disk of the pack (Figure 1-3). This signal is sent back to the controller to indicate disk position, and to a flip-flop rate sampler within the drive logic to generate an up-to-speed indication to the controller whenever the drive reaches 70 percent of rated speed.

Dynamic braking of the drive motor is accomplished by replacing ac power with dc power until the pack has stopped, whenever the STOP switch is pressed.

CAUTION

A mechanical detenting mechanism, designed to hold the spindle still for pack installation/removal, is actuated when the cover is raised. For this reason, the cover should never be raised while the pack is rotating.

The read/write head contains two read/write coils wound on a ferrite core. The read/write coils are wound one on top of the other with their leads connected in series by a center tap. Current applied to the write coils causes the existing data to be erased as bits are written. Write data pulses are sent from the RP11-C to the RP03 write circuits. The two read/write coils establish the polarity of current to magnetize the disk surface; one direction to write a 1 bit, and in the opposite direction to write a 0 bit. The polarity at the coils is controlled by the write driver switching network, which detects the state of the bit pattern and flips back and forth to energize the respective coil to record a bit. The head selection circuits select one head to read or write data before initiation of a Seek command. Control of head selection originates at the control unit. The RP03 drive logic interprets RP11-C commands to activate a line for the required head. The heads are gimbal-mounted in the horizontal plane and leaf-spring loaded in the vertical plane; when the disk is up to speed, the heads fly on a cushion of air over the surface of the disk.

The four basic operations performed by the drive under RP11-C controller command are:

a. Seek
b. Write
c. Read
d. Restore

The Seek operation is initiated by the receipt of a cylinder address from the controller. The drive logic compares this address with its present address and determines the direction in which the heads must move. Head motion is then accomplished and monitored by a difference count within the drive and is held in position by servo electronics when the count reaches zero. The time required to locate the next cylinder address is limited to 100 ms by a time delay actuated at the start of the Seek. Failure to electronically re-detent during this time results in a Seek Incomplete to the controller. When the new address is reached, and the head carriage velocity is zero, the drive indicates to the controller its readiness to accept another command.

When Write is commanded, the controller supplies data to the write-selected head as a double-frequency, non-return-to-zero pulse train, together with clock pulses for synchronization. The data and clock information are recorded as reversals in magnetic flux on the selected disk track.

When Read is commanded, the same head is read-selected to sense the previously recorded flux changes, producing current reversals in the head windings. This signal, which contains both data and clock pulses, is sent to the RP11-C for processing.

When Restore is commanded, the heads are moved by a forced forward Seek that sends the carriage to the forward stop. When the carriage reaches the stop, it executes a normal reverse Seek to home position (cylinder 000). When carriage speed reaches zero, the RP03 signals the RP11-C that it is ready for instructions.

NOTE

The sequence just described also occurs as a first Seek whenever the drive START switch is depressed and after the motor has reached 70 percent of rated speed.

Several safety circuits are included in the RP03 drive. These circuits protect data from destruction in the event of component failure. With the exception of a power failure, all failure conditions issue a File Unsafe Violation (FUV) indication to the RP11-C, deselect heads, and terminate read/write operations. The FUV indication can be reset by switching START/STOP to the STOP position or by depressing the File Unsafe reset switch inside the rear panel on those drives so equipped. Loss of primary power removes all dc voltages from the machine, automatically preventing write current. If any dc logic voltage is lost, heads are deselected to prevent writing. If an unsafe condition is present when a drive is turned on, an indication of File Unsafe is given immediately. If the heads are extended when primary ac power fails, if STOP is depressed, or if the disk compartment door is opened before depressing STOP, the heads will automatically retract.

1.2.3 RP11-C Disk Pack Drive Controller

The function of the RP11-C Disk Pack Drive Controller is to synchronize data transfers between the disk pack drive and the Unibus. It adapts serial transfers of the drive to parallel transfers on the Unibus, and vice versa. The RP11-C interfaces the PDP-11 processor to the RP03. Data transfers occur directly between the RP11-C and the PDP-11 memory on a Unibus master (RP11-C)/slave (PDP-11 memory) basis. The RP11-C is bus master in those transactions with memory. All status and control information is transferred via the Unibus as memory (RP11-C registers) to memory (PDP-11 registers or memory locations) transactions.

The RP11-C controller interfaces from one to eight RP03 Disk Pack Drives to the PDP-11 processor. Each RP03, when equipped with the RP02P Disk Pack, provides the PDP-11 system with an additional 20.48×10^6 16-bit words of storage capacity. Data is transferred at a rate of 7.4 μs/word through the non-processor request (NPR) facility provided by the Unibus. Data transfers are buffered by a 64-word Silo Memory. The following paragraphs describe the general sequence of Read and Write functions.

1.2.3.1 Read Function – To read data from the RP03 Disk Pack Drive and transfer it into PDP-11 memory, the PDP-11 processor initiates a Read function, under program control. The sequence of operations is summarized briefly in the following steps:

1. The processor moves the number of words to be read, from a memory location into the RP11-C Word Count Register (RPWC). The word count is in 2's complement.

2. The processor moves the cylinder address into the RP11-C Cylinder Address Register (RPCA) and the track and sector address into the RP11-C Disk Address Register (RPDA). The RPCA and RPDA then specify the starting location on the disk; i.e., where the first word is located.

3. The processor moves the address of the first memory location into the RP11-C Bus Address Register (RPBA). This indicates the memory address at which the first data word is to be stored.

4. The processor moves a command word into the RP11-C Control Status Register (RPCS). The command word selects which disk drive unit is to be read, provides mode control and extended memory address information, and specifies the Read function.

5. The RP11-C decodes the command code and controls the selected disk pack drive to start the Seek operation that positions the disk read/write heads.

6. The selected disk drive signals the RP11-C when it is ready (within 1/2-cylinder of the selected address) and the RP11-C turns on the disk drive read amplifiers.

7. The sector header, consisting of nine cylinder address bits, five head address bits, and four sector address bits, is read from the disk.

8. The RP11-C logic compares each sector header with the unique disk address stored in the RPCA and RPDA. When the correct hea is found, the RP11-C starts shifting serial data into the Shift Register (SR). In the PDP-11 mode of o ation, the data consists of two 16-bit data words, four serial checksum bits, and a parity bit.

9. When the 36-bit data word has been assembled in the Shift Register, it is parallel-shifted into the 36-bit Buffer Register (BR). It is also exclusive-ORed into the Longitudinal Parity Register (LPR).

10. The contents of the Buffer Register consist of two 16-bit words, which are transferred to the Silo Memory in two consecutive cycles.

11. The 64 X 16-bit Silo Memory provides 64 words of buffering between the disk and the Unibus. The silo operates on a first-in/first-out basis. It initiates an NPR Unibus transaction whenever a new data word "bubbles" to the output. The RP11-C can continue reading serial data from the disk into the silo for nearly 474 μs while the RP11-C Unibus control logic is waiting for Bus Grant.

12. As each data word is transferred, the RP11-C Word Count Register (RPWC) and the RP11-C Bus Address Register (RPBA) are incremented. Thus, once the RP11-C is initiated, it keeps track of the number of data words to be read and where they are to be stored in memory. When the RPWC overflows, data transfers stop.

13. The remainder of the present disk sector is read and parity is checked. The RP11-C then notifies the PDP-11 processor that the operation is completed.

1.2.3.2 Write Function – To write data from the PDP-11 memory onto the disk, the PDP-11 processor initiates a Write function, under program control. The initialization and termination operations are similar to those described for the Read function. The sequence of operations is summarized in the following steps:

1. The processor, operating under program control, loads the RP11-C bus registers with word count, disk address, and memory address information, as described in Steps 1, 2, and 3 of Paragraph 1.2.3.1.

2. The processor then moves a command word into the RP11-C Control Status Register (RPCS) to specify the Write function.

3. The interchange between the RP11-C and the selected RP03 is identical to that described in Steps 5, 6, and 7 of Paragraph 1.2.3.1.

4. The Silo Memory is enabled and NPRs are issued to start transferring 16-bit data words from the memory location specified by the RPBA contents. The Silo Memory can be loaded with up to 64 16-bit data words.

5. The RP11-C compares each sector header read from the disk with the disk address stored in the RPCA and RPDA. When the correct header is found, the 16-bit data words in the silo are transferred to the 36-bit Buffer Register in two consecutive Silo Memory cycles.

6. The contents of the Buffer Register are loaded into the Shift Register and serially transmitted to the disk. Each 36-bit Buffer Register word is also exclusive-ORed into the Longitudinal Parity Register.

7. After each Unibus transaction, the RPWC and RPBA registers are incremented. The RP11-C keeps track of where the data is to be read from memory and the total number of words to be read. When the RPWC overflows, data transfers cease. When the silo word counter overflows, the remainder of the current disk sector is filled with 0s.

1.2.3.3 Write Check Function – The RP11-C performs a Write Check function, a combination of Read and Write functions, which is used to verify that data on the disk compares bit-for-bit with data stored in memory. If any discrepancy exists, an error is reported. The data on the disk and in memory remains unchanged.

1.3 SPECIFICATIONS SUMMARY

The following RP11-C controller and RP03 disk drive specifications are subject to change without notice.

1.3.1 RP11-C Disk Pack Drive Controller Specifications

Mechanical

Cabinet	One H961-A Cabinet
Dimensions:	71-7/16 in. high, 21-11/16 in. wide, 30 in. deep (180 cm X 55 cm X 76 cm)
Weight:	325 lb (147 kg) (approx.)
Logic Panels	Four H911 Mounting Panels
Dimensions:	31-1/2 in. high, 19 in. wide, 16-3/4 in. deep (80 cm X 48 cm X 42.5 cm)
Weight:	28 lb (13 kg) (approx.)

Electrical

Input Power:	115/230 Vac ± 10%, 47–63 Hz
Power Supplies:	H740D Logic Power 716 Indicator Power H704 Analog Voltage
Module Type:	M Series
Logic Voltage:	1 = +3V, 0 = 0V (TTL)
Environmental	Limited only by RP03 requirements.
Heat Dissipation	5100 Btu/hour (approx.)

1.3.2 RP03 Disk Pack Drive Specifications

Mechanical

Height:	40 in.
Width:	30 in.
Depth:	24 in.
Weight:	415 lb
Capacity:	466.8×10^6 bits
Bits Available to a Single Access:	1,167,040
Number of Recording Surfaces:	20
Tracks per Surface:	400 plus 6 spares

Performance

Rotational Time:	25 ms
Track-to-Track Position Time:	7.5 ms
Average Position Time:	29 ms
Maximum Position Time:	55 ms
Data Reliability (see note):	
Read Error:	Less than 1 failure in 10^9 bits
Write Error:	Less than 1 failure in 10^{10} bits
Density Track 000:	1530
Density Track 405:	2228 bpi
Data Transfer Rate:	2.5×10^6 bits/sec

NOTE

A data error is specified when the data read from a particular disk sector fails to compare identically with the data written in the same sector. The following are definitions of read and write errors.

Read Error: An error is detected when reading a disk sector but the data can be recovered successfully by performing a sequence comprising ten rereads, one reaccess to the same track following a Home Seek, and ten additional rereads.

Write Error: An error is detected when reading a disk sector and the data cannot be recovered by performing the sequence described under Read Error above.

Electrical

Input Power:	208/230 Vac ± 10% 60 Hz ± 0.5 Hz
Input Current:	6A (maximum starting surge = 30A)
Power Consumption:	1260W (approx.)

Environmental

Temperature:	60°F to 90°F
Humidity:	8% to 80% (maximum wetbulb temperature is 83°F)
Heat Dissipation:	3500 Btu/hour

CHAPTER 2
INSTALLATION

2.1 SITE CONSIDERATIONS

The RP11-C Disk Pack Drive Controller is contained in a single H961-A Cabinet. This cabinet is normally adjacent to the PDP-11 system; however, it may be placed in any convenient location, provided the maximum Unibus length (50 ft) is not exceeded.

Each RP03 is a self-contained, stand-alone unit, 30 in. wide X 24 in. deep X 39 in. high. For convenience, all RP03 Disk Pack Drives should be located together; however, this is not a system restriction.

NOTE

The RP03 Disk Pack Drives should be located in a clean, temperature-stabilized environment. Any disk drive system can be seriously damaged by the introduction of particles between the disk surfaces and the flying heads.

2.2 CABLES AND CABLE LENGTH LIMITATIONS

Figure 2-1 shows the three major system components: PDP-11 processor, RP11-C controller, and up to eight RP03 disk drives. The standard configuration requires that the processor and controller be adjacent. Each cable is designated by a letter/number combination as shown in Figure 2-1 and described in the following paragraphs. Figure 2-2 shows the RP11-C cable slots.

2.2.1 Interface Cable "A"

Interface Cable "A" interfaces the controller and the PDP-11 Unibus. This cable is supplied with the RP11-C controller.

2.2.2 Interface Cable "B"

Interface Cable "B" provides a remote 115/230-Vac signal to the controller. The controller can be operated in either the remote or local mode, depending on the setting of a switch on the 860 Power Control mounted in the top of the RP11-C cabinet.

2.2.3 Interface Cables "C"

"C" cable interfaces are designated by suffixes (0 through 7) which specify that the cables may be physically different (although logically identical). Each cable is supplied with the unit indicated by the suffix. All "C" cables bus in and out of each unit and provide the interface between the controller and all signals common to all drives.

2.2.4 Interface Cables "E"

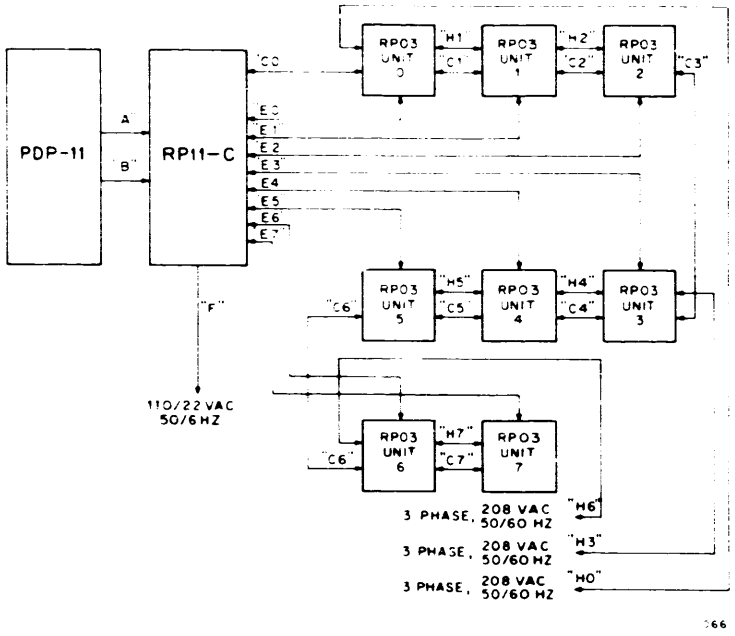
Each "E" interface cable is also assigned a 0 through 7 suffix. These suffixes have meanings identical to those described in Paragraph 2.2.3. The controller and all signals peculiar to a particular drive are interfaced by "E" cables.

2.2.5 Interface Cable "F"

Interface cable "F" supplies ac power to the RP11-C controller. This cable terminates at one end with a female, 30A Hubbell Twist-Lock connector and at the other end with an equivalent male connector. Cable "F" is provided with the RP11-C controller.

2.2.6 Interface Cables "H"

All "H" cables are assigned suffixes having the same meanings as those described in Paragraph 2.2.3. These cables supply the ac power required by the RP03 units. Each unit uses one leg of the 3-phase supply; therefore, the cabling should be configured exactly as shown in Figure 2-1.



DESIGNATION	CABLE	DEC PART NO	LENGTH (FEET)
A	Unibus Cable	BC11-A	50 (Max)
B	Power Control Cable	7008288	8
C0	Bus Cable (Controller)	7006463-15 7006463-25 7006463-40	15 25 40
C1 thru C7	Bus Cable (Jumper)	7006465-1 7006465-2	8 25
E0 thru E7	Unit Cable	7006601-1 7006601-2 7006601-3	15 25 40
F	Power Cable	861 (Power Control)	25
H0, H3, H6	Power Cable (Plug)	7006464	25
H1, H2, H4, H5, H7	Power Cable (Jumper)	7006600-1 7006600-2	8 25

Figure 2-1 RP11-C/RP03 System Cables

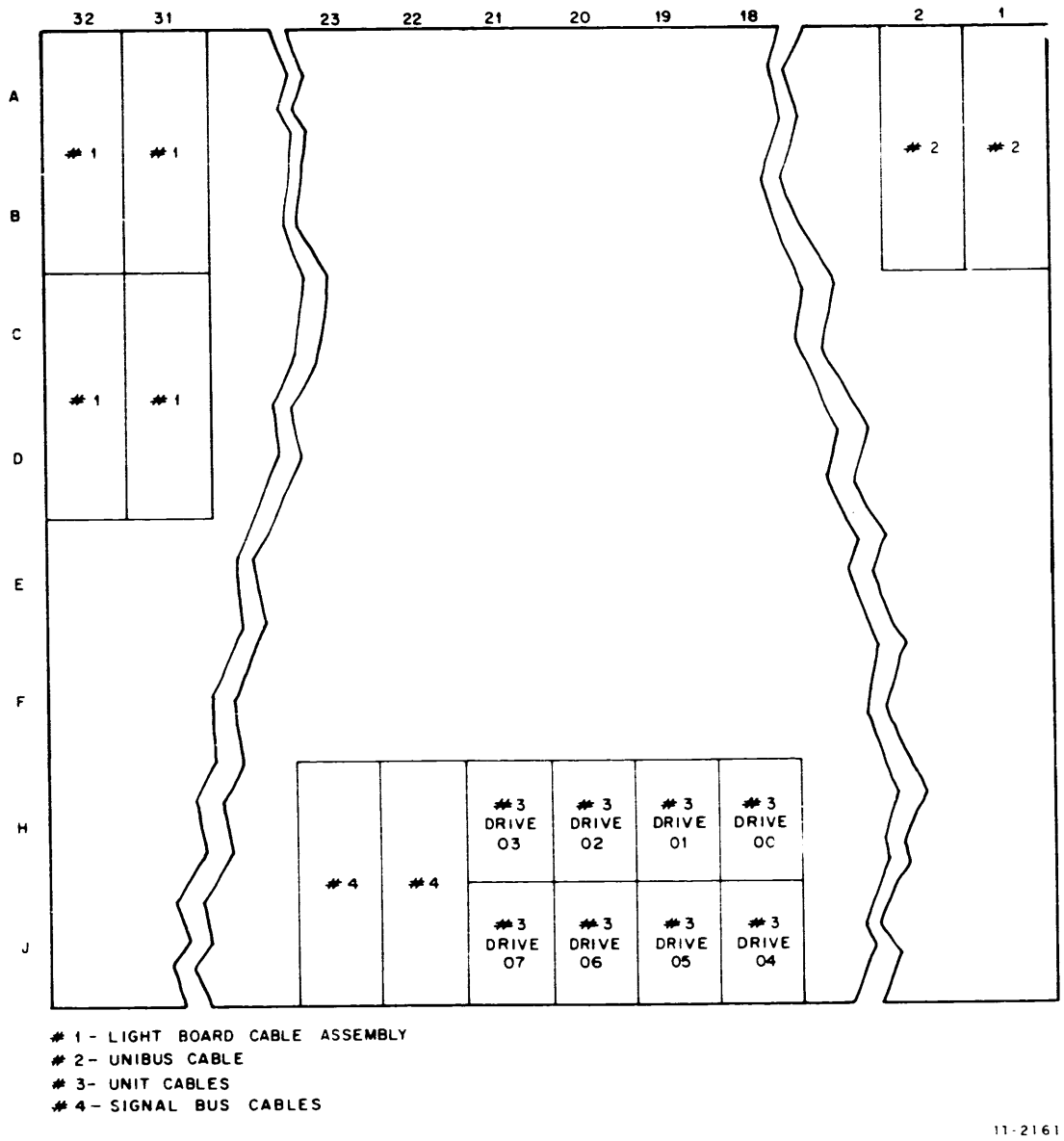


Figure 2-2 RP11-C Cable Slots

2.3 GROUNDING

No special signal grounding requirements exist. Safety considerations require that frame grounds on all RP03 Disk Pack Drives be common to the RP11-C and the PDP-11 system ground.

2.4 UNPACKING AND INSPECTION

The RP11-C is packed in accordance with the best commercial practice. No special handling procedures are required beyond normal care afforded any piece of scientific equipment of comparable size and weight. Particular care should be exercised in the use of cranes or hoists to prevent damage to the unit.

On receipt, inspect the equipment for any visible damage in transit, such as dents and abrasions. Inspect the logic modules for foreign matter which might have lodged in them during shipment. Any damage observed should be reported immediately to both the carrier and the manufacturer. Check the contents of the carton with the shipping document. Report any omissions immediately to the local DEC Sales Office.

2.5 POWER REQUIREMENTS

The RP11-C is supplied with its own self-contained power supplies. All voltage requirements of the unit are provided by DEC type H740D, H704C and 716 Power Supplies. Differences for accommodating either 50 or 60 Hz are made within the basic unit, designated RP11-CA for 60-Hz operation and RP11-CB for 50-Hz operation.

The RP03 contains its own internal power supply for the transport mechanism and logic circuitry. AC power for the unit is taken by daisy-chain jumper wiring. Units are wired in phase rotation to equalize ac loading.

2.6 INSTALLATION PROCEDURE

Install the RP11-C and RP03 per site plan. Overall physical dimensions are given in Figure 2-3.

2.6.1 Installing the RP11-C Cabinet

The RP11-C cabinet is provided with roll-around casters and adjustable leveling feet. It is not necessary to bolt the cabinet to the mounting floor unless conditions indicate otherwise (e.g., shipboard installation).

CAUTION
Do not attempt installation until DEC has been notified and a Field Service Representative is present.

Install the RP11-C cabinet using the following procedures:

1. Remove power from all systems.
2. Position the RP11-C cabinet according to the site plan.
3. If the RP11-C cabinet is to be mounted adjacent to one of the cabinets of the PDP-11 system, remove the sides of the cabinets affected.
4. Butt the cabinets together while holding the filler strips in place; bolt through both cabinets and the filler strips. Do not tighten the bolts securely at this time.
5. Lower the leveling feet, making sure that the cabinets are not resting on the roll-around casters but are supported on the leveling feet.
6. Level both cabinets with a spirit level and ensure that all leveling feet are seated firmly on the floor.
7. Tighten the bolts that secure the cabinet groups together and then recheck the cabinet leveling. Again ensure that all leveling feet are seated firmly on the floor.

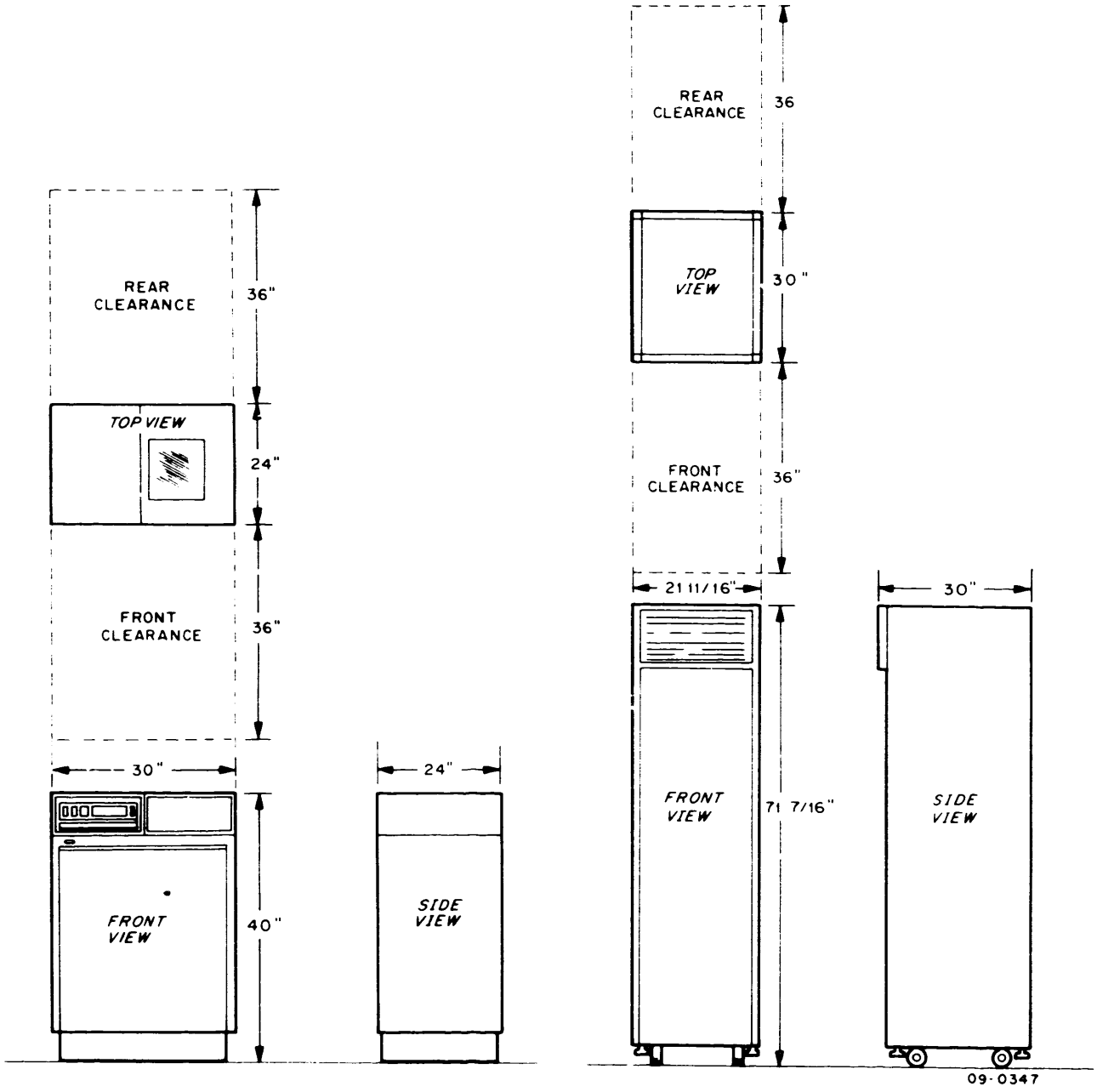


Figure 2-3 RP03 and RP11-C Physical Dimensions and Space Requirements

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 RP03 OPERATOR CONTROLS AND INDICATORS

The RP03 control panel is shown in Figure 3-1. Complete details on RP03 operation are described in the separate RP03 manual (Table 1-1, Related Documentation).

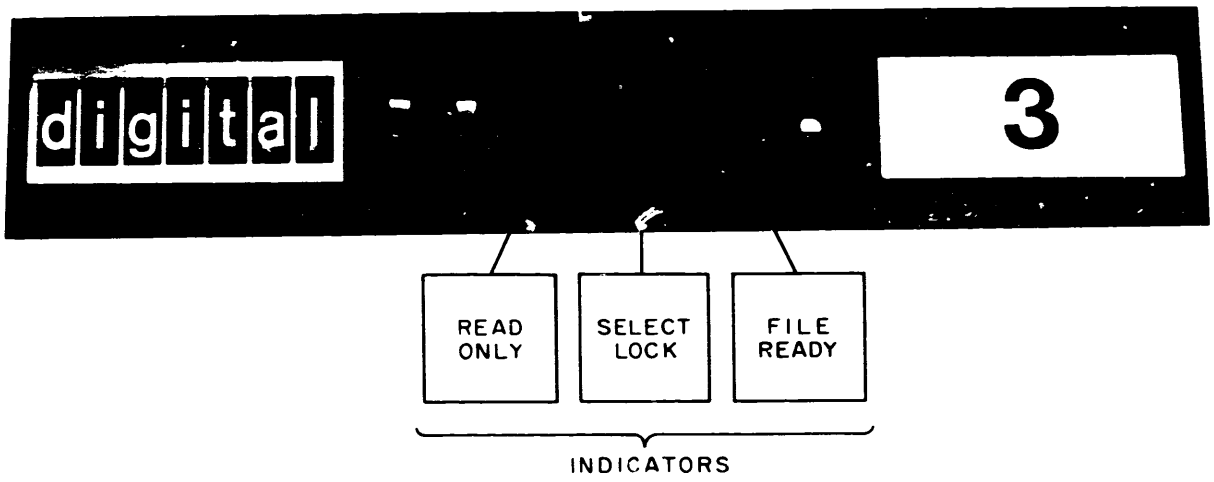


Figure 3-1 Control Panel Arrangement

3.1.1 Start/Stop Switch

This toggle switch energizes the disk drive motor and initiates the power-on sequence when placed to START. The power-on sequence causes the brush cycle to start, disk pack to come up to speed, and heads to access into the pack. The heads move to the forward stop to perform an automatic check of drive circuits. After contacting the forward stop, the heads move in reverse and stop at cylinder 000. The FILE READY indicator lights if an operational status is achieved. The SELECT LOCK indicator lights if a malfunction is present.

The STOP position shuts down the drive. This switch action causes ac power to be removed from the drive motor and initiates the power-off sequence. Read/write heads are retracted out of the disk pack and dynamic brake power is applied to stop disk rotation.

3.1.2 Enable/Disable Switch

This toggle switch permits the drive to be operated for maintenance purposes without physically disconnecting it from the control unit. In this way, communications with the control unit are inhibited and the drive's operating time is not recorded if a usage meter is installed. The DISABLE position blocks communication with the control unit by placing the drive off-line and inhibiting meter operation. The ENABLE position restores communication between the drive and control unit and enables meter operation.

3.1.3 File Ready Indicator

This indicator lights green when the power-on sequence is completed and the drive is ready to accept commands from the control unit. The light goes out if the drive is turned off, system power is dropped, or a Seek Incomplete occurs.

3.1.4 Select Lock Indicator

This indicator lights red to indicate the presence of an unsafe condition in the drive. This light remains on only when the heads do not unload in conditions such as Heads Unsafe, AC Write Unsafe, and DC Write Unsafe. Other unsafe conditions such as 30 Vdc Unsafe, Velocity Unsafe, and Pack Speed Unsafe allow the light to go out immediately after the heads unload from the pack. Correcting the unsafe condition and turning the drive off and back on also causes the indicator light to go out. A select lock condition may also be cleared by depressing the microswitch mounted on top of the electronic gate, if this option is installed.

3.1.5 Read/Write – Read Only Switch

This toggle switch enables/prohibits execution of Write commands.

3.1.6 Read Only Indicator

This indicator lights yellow whenever the write circuits are disabled by the READ ONLY switch.

3.2 OPERATIONAL PROCEDURES

3.2.1 Disk Pack Handling Procedures

The instructions provided by the disk pack manufacturer should be used by the operator as a reference source. IBM File No. S360-07, Form A26-3599-2 describes essential procedures for the 2316 Disk Pack. The handling, labeling, receiving and storage requirements are described in sufficient detail to satisfy the special needs of the operator. Disk packs are to be protected against improper handling and environmental abuse as specified by the disk pack manufacturer.

3.2.2 Installing the RP02P Disk Pack

The disk pack is always carried by the built-in handle on the top cover. It is conditioned to room temperature before installation. A self-locking device in the handle permits removal of the top cover only when the disk pack is mounted on the drive.

Perform the following steps to install the disk pack:

1. Verify that the drive is stopped and raise the operator cover to gain access to the disk pack spindle.

CAUTION

Never raise cover until STOP switch is operated; otherwise, dynamic braking of spindle is overridden.

2. Remove the bottom cover from the disk pack using the bottom cover knob.
3. Place the disk pack on the spindle.

4. Turn the top cover at the handle in a clockwise direction until it comes to a full stop. Continue to turn, even though the cover may disengage, to assure that the full stop point is reached and the pack-in-place switch is closed.

5. Remove the disk pack top cover.

6. Close and latch drive operator cover. Reassemble disk pack top and bottom covers and store in a designated area.

3.2.3 Removing the RP02P Disk Pack

Perform the following steps to remove the disk pack:

1. Make certain the drive switch is positioned to STOP.
2. Wait for the disk pack to come to a complete stop (approximately 20 seconds) before opening the operator cover.
3. Open the operator cover.
4. Position the disk pack cover over the top of the pack.
5. Turn the cover in a counterclockwise direction for two full turns so that the cover becomes securely fastened to the disk pack as an integral unit.
6. Remove the disk pack by its top cover handle.
7. Immediately attach the bottom cover to create a positive dust seal and store in a designated area.

3.2.4 RP03 Disk Pack Drive Start-Up

NOTE

If the operator is charged with the responsibility to record time of the usage meter before the drive is started, this task should be completed at this time.

Perform the following steps to start the drive:

1. Visually check to determine that the disk pack is installed in the drive and the pack top cover removed. The drive is now ready to be turned on.
2. Position the START/STOP switch to START.
3. Observe that the drive is on and check visually to determine that the FILE READY indicator lights green (about 20 seconds after Step 2).
4. Make certain that the ENABLE/DISABLE switch is positioned to ENABLE. The drive is now ready to receive control unit commands to seek and to transfer data.

3.2.5 RP03 Disk Pack Drive Shut-Down

Perform the following operation to stop the drive.

Position the START/STOP switch to STOP. In approximately 20 seconds, the heads are retracted from the disk pack, the pack rotation is braked to a stop, and power to the drive motor circuits is interrupted.

For operator safety reasons, power to the drive is interrupted and the heads become retracted whenever the operator cover is unlatched/raised with the switch positioned to START. However, pack rotation is not electrically braked and, therefore, requires about 60 seconds to coast to a stop. Observe the following precautions:

a. For safety – wait for the pack to stop rotating before raising the operator cover (for any reason).

b. To save time – shut down the drive only by positioning the drive switch to STOP. Never raise the cover to stop the drive.

c. To avoid program interruption, never shut down the drive while it is operating unless permission is obtained from the center operations manager. (Such an operator error causes the heads to retract off the pack and will negate subsequent instruction from the control unit.)

3.2.6 Responding to Malfunctions

Disk drive malfunctions are serviced only by authorized maintenance personnel. Conditions which define drive malfunctions are as follows:

a. No green light 20 seconds after placing switch to START.

b. Illumination of the red light at any time.

Authorized responses to malfunctions observed by the operator are as follows:

a. Position the START/STOP switch to STOP.

b. Report the observed malfunction to the supervising operator, the computing center manager, or equivalent personnel.

3.3 RP11-C OPERATOR CONTROLS

A small panel, located in the lower right hand corner of the RP11-C, houses three rocker switches and eleven toggle switches (Figure 3-2).

3.3.1 FORMAT ENABLE

The rocker switch labeled FORMAT ENABLE/NORMAL, in the FORMAT ENABLE position, causes the RP11-C to interpret a Write Header operation as a Format operation; i.e., a bare disk pack is prepared for normal data storage operation by writing header information in the header fields, and clock information (0s) over the rest of the disk surface. While in the NORMAL position, this switch causes the RP11-C to interpret a Write Header operation as one which takes header information from PDP-11 memory and writes this information in the addressed disk sector header area.

3.3.2 WRITE LOCKOUT

The rocker switch labeled WRITE LOCKOUT/WRITE ENABLE, in the WRITE LOCKOUT position, causes the selected address lockout to be in effect. In the WRITE ENABLE position, any Write operation is allowed on any drive so long as the drive itself is write enabled.

3.3.3 MAIN ENABLE

The rocker switch labeled MAIN ENABLE/NORMAL, in the MAIN ENABLE position, allows the RP11-C maintenance circuits to become active, providing for performance of controller maintenance without the RP03 Disk Pack Drive. While in the NORMAL position, this switch disables the maintenance circuits, providing for RP11-C operation with the RP03 Disk Pack Drive.

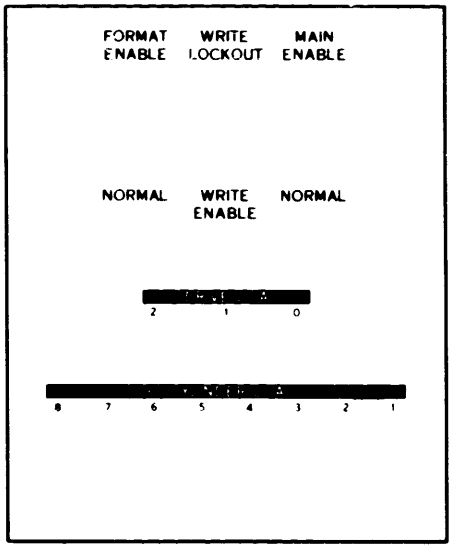


Figure 3-2 Maintenance Panel

3.3.4 Lockout Address Switches

Two types of write protection are available in the disk pack system. The first type is the READ/WRITE – READ ONLY switch on each individual RP03 Disk Pack Drive which enables or inhibits execution of Write commands for that unit. In the READ ONLY position, the entire unit is write protected. If the unit receives a Write command, the Write function is prohibited and an interrupt is generated.

The second type of write protection is offered by the lockout address (LOA) switches on the maintenance panel (Figure 3-2) of the RP11-C. When the WRITE LOCKOUT – WRITE ENABLE switch is set to WRITE LOCKOUT, the LOA switches are enabled. A binary 1 is selected as a lockout address bit when the LOA switch is in the up position. In WRITE LOCKOUT, all disk areas up to and including the one designated by the LOA switches are write protected.

DRIVE LOA switches 2-0 are used to write protect entire RP03 Disk Pack Drive units. For example, assume that the DRIVE LOA 2-0 switches are set for octal 3. Then, writing is prohibited on disk drives 0, 1, and 2.

CYLINDER LOA switches 8-1 are used to write protect cylinders on the next higher numbered disk drive unit than the one designated by the DRIVE LOA switches. The eight CYLINDER LOA switches select only the eight most significant bits of the 9-bit cylinder address. Thus, the lockout boundary must always be an even numbered cylinder. With an all 0 switch setting in the DRIVE LOA and CYLINDER LOA switches, cylinders 0 and 1 of drive 0 are write protected when the lockout switch is in the WRITE LOCKOUT position.

If, in addition to the DRIVE LOA switches being set for octal 3 (previous example), CYLINDER LOA 8-1 switches are set for binary 001 111 100 (octal 174), then cylinders $0\text{-}124_{10}$ on RP03 Disk Pack Drive unit 3 are write protected in addition to disk drive units 0, 1, and 2. Write functions will only be permitted on cylinders $125\text{-}400_{10}$ on disk drive unit 3, and on all cylinders of disk drive units 4 through 7.

If an attempt is made to write into a write-protected area of the disk pack system, the Write function is inhibited and the Write Protect Violation (WPV) flag is set in the RP11-C Error Register (RPER).

3.4 RP11-C INDICATOR PANEL

The RP11-C indicator panel displays the states of major logic signals and is shown in Figure 3-3. Table 3-1 lists the lamps and the significance of each lamp when lit.

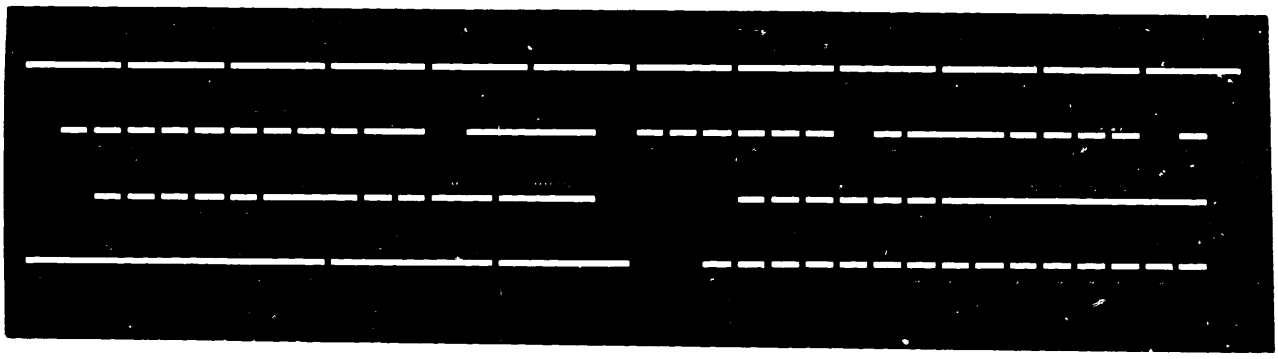


Figure 3-3 RP11-C Indicator Panel

Table 3-1
RP11-C Indicator Panel

Lamp(s)	Significance
BUFFER REGISTER 00 through 35	Buffer Register. 36-bit data register that buffers the data read from the RP03 Disk Pack Drive and the Unibus.
READ	Read. RP11-C is reading data from an RP03 Disk Pack Drive. **NOTE** **This bit does not indicate the function the RP11-C is currently performing. For example, the RP11-C is in the "read" state while searching for the correct header during a Write command.**
WRIT	Write. RP11-C is writing data to a RP03 Disk Pack Drive.
ERAS	Erase. "Trim" erase current is flowing in the selected RP02 head.
HA	Head Advance. RP11-C is requesting that the RP03 advance to the next higher numbered head.
RS	Restore. RP11-C is requesting that the RP03 execute a Home Seek.
SC	Set Cylinder. RP11-C is requesting that the RP03 load its Cylinder Address Register from the data on the Bus Out lines.
RH	Reset Head. RP11-C is requesting that the RP03 reset its Head Address Register.
SH	Set Head. RP11-C is requesting that the RP03 load its Head Address Register from the data on the Bus Out lines.
SS	Seek Start. RP11-C is requesting that the RP03 begin a Seek operation.
BOC 01, 00	Bus Out Control (two bits). Controls the sequence and timing of signals on the Bus Out and Tag lines.
SCK 03, 02, 01, 00	Serial Checksum. Four-bit counter that generates and checks the serial checksum in the PDP-11 data mode.
HW	Header Window. RP11-C is searching for a sector's header word.
HS	Header Sync. RP11-C is searching for the pre-header SYNC bit.
HF	Header Found. Header read from the present sector is the header addressed by CAR, TAR, and SAR.
DW	Data Window. RP11-C has reached the data field of a sector.

(Continued)

Table 3-1 (Cont)
RP11-C Indicator Panel

Lamp(s)	Significance
DS	Data Sync. RP11-C is searching for the post-header SYNC bit.
EOS	End Of Sector. End of a sector has occurred during any operation.
RPM	RP Master. RP11-C is the Unibus master.
REQ 02, 01, 00	Request. Indicates which part of the word is being transferred between the Silo Memory and the Buffer Register.
ORDY	Silo Output Ready. A word is available at the Silo Memory output.
IRDY	Silo Input Ready. Silo Memory is ready to accept a word.
WCOF	Word Count Overflow. Silo and Bus Word Count Registers have been incremented to the overflow condition (all 0s).
BAOF	Bus Address Overflow. RPBA has been incremented to the overflow condition (all 0s).
INTR	Interrupt Request. RP11-C is requesting a PDP-11 interrupt.
ERR	Error. OR of all RP11-C error conditions.
HE	Hard Error. OR of all RP11-C "hard" error conditions.
AE	Attention Enable. RP11-C will interrupt the PDP-11 when any attention line becomes true.
MODE	Mode. RP11-C is in the PDP-10/15 mode.
HDR	Header. RP11-C will perform the command specified by COM2–0 in the header mode.
DRIVE SEL 02, 01, 00	Drive Select. Three lamps that display the encoded value of the disk drive currently selected.
NR	Not Ready. RP11-C is not in the Ready state.
IDE	Interrupt On Done Enable. RP11-C will interrupt the PDP-11 when an operation is completed or when an error is detected.
MEX 01, 00	Memory Extension (2 bits). Extended memory address bits.

(Continued)

Table 3-1 (Cont)
RP11-C Indicator Panel

Lamp(s)	Significance
COMMAND 02, 01, 00	Command Field (3 bits). Specifies the operation the RP11-C to perform as follows: **Code** — **Function** 0 — Idle (Reset) 1 — Write (Implied Seek) 2 — Read (Implied Seek) 3 — Write Check (Implied Seek) 4 — Seek 5 — Write (No Implied Seek) 6 — Home Seek 7 — Read (No Implied Seek)
SRDY	Selected Unit Ready. From RP03. Indicates that the selected drive is ready to accept a new command.
HNF	Header Not Found. Disk pack has made more than two revolutions without finding the addressed sector.
SUSI	Selected Unit Seek Incomplete. Selected unit has failed to successfully complete a Seek operation.
SUSU	Selected Unit Seek Underway. Selected unit is presently performing a Seek operation.
SUFU	Selected Unit File Unsafe. Selected unit has recognized a condition that may cause disk operation to be unreliable.
UWP	Selected Unit Write Protected. Either the write protect switch on the RP03 is set, or the addressed sector is within the selected address lockout range.
UNIT ATTENTION 07, 06, 05, 04, 03, 02, 01, 00	Unit Attention (8 bits). Individual bits from each drive indicating that the drive has finished a Seek operation (either successfully or not).
CYLINDER ADDRESS REGISTER 08, 07, 06, 05, 04, 03, 02, 01, 00	Cylinder Address Register (9 bits). Register containing the desired cylinder address.
TRACK ADDRESS REG 04, 03, 02, 01, 00	Track Address Register (5 bits). Register containing the desired track address.
SECTOR ADDR REG 03, 02, 01, 00	Sector Address Register (4 bits). Register containing the desired sector address.

(Continued)

Table 3-1 (Cont)
RP11-C Indicator Panel

Lamp(s)	Significance
WPV	Write Protect Violation. Write operation has been attempted while WRITE PROTECT is true.
FUV	File Unsafe Violation. Disk operation has been attempted while FILE UNSAFE is true.
NXC	Non-Existent Cylinder. Disk operation was attempted while the Cylinder Address Register contained a value greater than 405_{10}.
NXT	Non-Existent Track. Disk operation was attempted while the Track Address Register contained a value greater than 19_{10}.
NXS	Non-Existent Sector. Disk operation was attempted while the Sector Address Register contained a value greater than 9_{10}.
PROG	Program Error. Data transfer was attempted while WCOF was true, or any operation was attempted with a drive not on-line, or while another instruction was still in progress.
FMTE	Format Error. Error was detected while reading the pre-header sync.
MDE	Mode Error. Header operation was attempted while the RP11-C was in the PDP-11 mode.
LPE	Longitudinal Parity Error. At the end of a sector, the computed longitudinal parity word does not equal the longitudinal parity word stored on the disk.
WPE	Word Parity Error. Parity of any 37-bit disk word is even.
CSME	Checksum Error. Computed serial checksum does not equal that stored on the disk for a 36-bit word while the RP11-C is in the PDP-11 mode.
TIME	Timing Error. PDP-11 Unibus did not respond in time to prevent loss of data.
WCE	Write Check Error. During the Write Check operation, data from PDP-11 memory did not compare with data from the disk.
NXME	Non-Existent Memory Error. Address specified by the Bus Address Register did not respond within 10 μs during an NPR data transfer.
EOP	End Of Pack. Data transfer operation exceeded the limits of the currently selected disk drive.

3.5 RP02P DISK PACK STRUCTURE

The total storage capacity of the RP02P Disk Pack is 494,505,000 bits, excluding the top and bottom disk surfaces. Because these two surfaces are not used for recording, and because inner-most cylinders 400 through 405 are only used for maintenance, the actual data storage capacity available to the user is reduced.

The usable RP02P storage capacity is divided into sectors as follows:

400 cylinders X 20 tracks/cylinder X 10 sectors/track = 80,000 sectors

Within each sector, some of the storage capacity is used for synchronization and parity. The format of a sector differs for each of the two modes of operation: PDP-11 and PDP-10/15. Therefore, the usable data storage capacity and disk pack sector format is described separately for each mode of operation.

3.5.1 PDP-11 Mode of Operation

Figure 3-4 shows the sector format used in the PDP-11 mode of operation. The sector consists of 165 37-bit words, organized as follows:

a. 30 Pre-header sync words

b. 1 Header word

c. 4 Post-header sync words

d. 128 Data words

e. 1 Longitudinal parity word

f. 1 End of sector word

3.5.1.1 Pre-Header Sync Words – These contain all 0s except for a 1 bit as the last bit of the last word. This area of the sector is used to synchronize the RP11-C VFO-controlled clock with the recorded sync bits.

3.5.1.2 Header Word – This 37-bit word contains the complete disk address required to identify each sector. It consists of seventeen 0s, the 9-bit cylinder address, the 5-bit track address, a space, followed by a 4-bit sector address, and the parity bit.

3.5.1.3 Post-Header Sync Words – These contain all 0s except for a 1 bit as the last bit of the word before the data.

3.5.1.4 Data Words – In the PDP-11 mode of operation, each of the 128 disk data words contains two 16-bit processor words, followed by a 4-bit serial checksum and an odd-parity bit. Thus, in the PDP-11 mode of operation, each sector capacity is 256 16-bit processor words and the total usable data storage of an RP02P Disk Pack is:

80,000 sectors X 256 words = 20,480,000 16-bit words

3.5.1.5 Longitudinal Parity Word – The longitudinal parity word at the end of the sector is the exclusive-OR of all the data words in the sector. It consists of 36 longitudinal parity bits plus an odd-parity bit.

3.5.1.6 End of Sector Word – This word provides buffering time between the last written data and the disabling of the write amplifiers in the RP03 Disk Pack Drive.

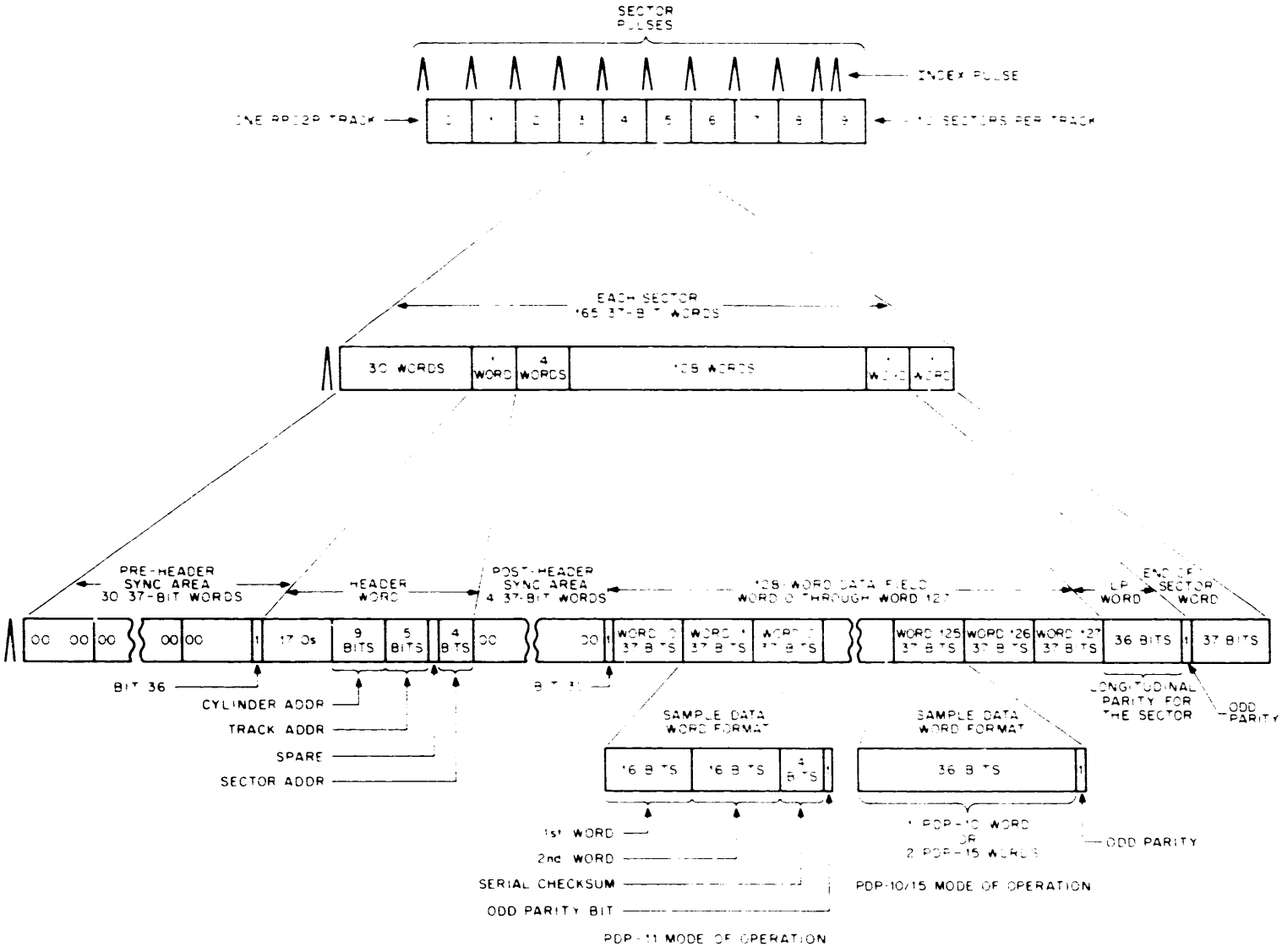


Figure 3-4 RP02 Format for RP11 Controller

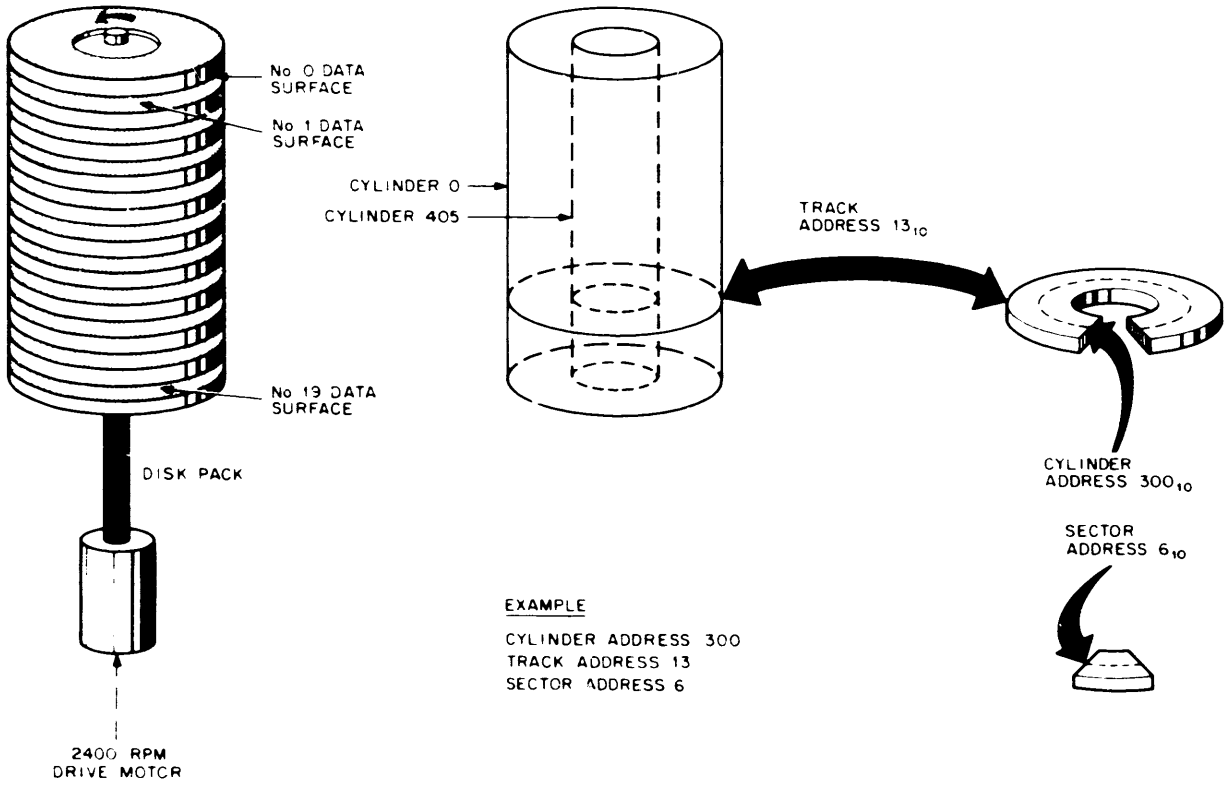
3.5.2 PDP-10/15 Mode of Operation

The only difference between the PDP-11 and PDP-10/15 sector formats is in the organization of each data word. In the PDP-10/15 mode of operation, each data word consists of 36 data bits and a parity bit, as shown in Figure 3-4. Thus, the total usable data storage capacity of the RP02P Disk Pack is as follows:

80,000 sectors X 256 18-bit words = 20,480,000 PDP-15 words
or
80,000 sectors X 128 36-bit words = 10,240,000 PDP-10 words

3.6 DISK PACK ADDRESSING

The disk pack consists of 11 evenly-spaced recording platters mounted on a single shaft (Figure 3-5). Because of this physical arrangement, the highest and lowest surfaces are not used for recording. The lowest surface has an attached metal disk with 20 evenly-spaced notches and an index slot in the periphery.



SUMMARY

MODE	CYLINDERS/ PACK	TRACKS/ CYLINDER	SECTORS/ TRACK	WORDS/ SECTOR	WORDS/ PACK
PDP-11	400	20	10	256	20,480,000
10/15 PDP-15	400	20	10	256	20,480,000
PDP-10	400	20	10	128	10,240,000

11 1500

Figure 3-5 RP02P Disk Pack Structure

A circuit designed to detect these notches rejects alternate notches, thereby dividing the disk pack into ten equal sectors. These sectors are addressed by the 4-bit Sector Address Register. Sector addresses are coded 00_8 through 11_8. Illegal codes 12_8 through 17_8, when detected by the controller, set an error flag causing appropriate interrupts.

A separate read/write head is provided for each of the 20 inner recording surfaces. These heads are mounted in parallel, in vertical alignment with one another, and attached to a common head tower. The heads are selected by the 5-bit Track Address Register. Head addresses are coded 00_8 through 23_8. Illegal codes 24_8 through 37_8, when detected by the controller, set an error flag resulting in appropriate interrupts.

The position of all heads, vertically aligned with respect to the vertical axis which passes through the center of all surfaces, is called a cylinder. Head positioning is controlled by a linear positioning motor and electronic detenting designed to stop the heads in 406 different cylinders. These cylinders are coded 000_8 through 625_8 from the outer-most cylinder to the inner-most cylinder, respectively. Cylinders are addressed by the 9-bit Cylinder Address Register. Illegal codes 626_8 through 777_8, when detected by the controller, set an error flag causing appropriate interrupts.

The intersection of a cylinder, head, and sector address defines a unique sector which is the smallest addressable unit in the system. Each sector contains a data field of 256 16-bit PDP-11 words and a header word which uniquely defines that sector.

3.7 FUNCTION CONTROL

The RP11-C provides the hardware for the execution of the eight different functions listed in Table 3-2.

Home Seek and Seek are designated initiate functions because their execution requires only 16 μs of controller time after the command is issued. For this period, the controller is busy. Initiate commands require that the target unit be selected for only this busy period; i.e., although a Seek may require 50 ms for completion, the unit affected need only be selected for the busy period. Idle (Reset) requires only 4 μs of RP11 time. Execute instructions, however, use all the time the controller requires for completing the function. The controller, therefore, is busy for the entire operation. Also, the target unit must be selected for the entire operation and cannot, therefore, be deselected for beginning initiate-type functions.

Table 3-2
Hardware Executed Functions

Function	Code	Type
Idle (Reset)	0	Initiate
Write	1	Execute
Read	2	Execute
Write Check	3	Execute
Seek	4	Initiate
Write (No Seek)	5	Execute
Home Seek	6	Initiate
Read (No Seek)	7	Execute

Functions are selected by loading a 3-bit field, COM(02:00), of the Controller Status Register (RPCS) with an octal number equal to the function code.

3.7.1 Idle (Control Reset, Function = 0)

The Idle function is the no operation state of the control. This function is entered when the RP11-C is initially cleared, or when the Function Register contents equal 0.

If GO is set while the content of the Function Register equals zero, CONTROL RESET is generated. This operation requires 4 μs of RP11-C time and no interrupt is generated upon completion.

3.7.2 Write (Function = 1)

The Write function includes a Seek to the starting disk address (cylinder and track). This function is executed by loading its octal code (1) into the Function Register and setting GO. WRITE transfers data from the PDP-11 memory to the RP03 beginning with the memory location specified by the Data Address Register. Each data word transferred increments the Current Address and Word Count Registers. The content of the RPWC at the beginning of the transfer determines the number of data words to be transferred. When the RPWC overflows, data transfer ceases and the remainder of the present sector is filled with 0s.

NOTE

Because the disk pack system uses 36-bit disk words, the word count must be equal to a multiple of the number of PDP-11 memory words per disk word. For example, in the PDP-11 mode, there are two PDP-11 words per disk word, and the word count must be a multiple of two. In PDP-10/15 mode, there are three PDP-11 words per disk word, and the word count must be a multiple of three. Also, the initial contents of the RPBA must be such that the number of transfers specified by the RPWC will not overflow the bounds of existing bus addresses.

3.7.3 Read (Function = 2)

The Read function includes a Seek to the starting disk address (cylinder and track). This function is executed by loading its octal code (2) into the Function Register and setting GO. READ transfers data from the RP03 to the PDP-11 beginning with the memory location specified by the Current Address Register. Each data word transferred increments the Current Address and Word Count Registers. The content of the RPWC at the beginning of the transfer determines the number of data words to be transferred. When the RPWC overflows, data transfer stops. The remainder of the present sector is read and parity checked before the DONE flag is set. The Current Address Register contains the address of the last data word transferred plus one. At this point, a CONTINUE may be effected by reloading the Word Count and Current Address Registers and setting GO.

3.7.4 Write Check (Function = 3)

The Write Check function includes a Seek to the starting disk address (cylinder and track). The WRITE CHECK command is a combination of the Write and Read functions. Data words are transferred from the PDP-11 memory to the RP11-C and simultaneously read from the RP03 and transferred to the RP11-C. In the RP11-C, the two words are compared. Discrepancies set the status bit to cause an appropriate interrupt. Data remains unchanged in both the memory and the disk.

3.7.5 Seek (Function = 4)

The Seek function can be executed by loading its octal code (4) into the Function Register and setting GO. The Seek operation positions the heads of the selected unit as specified by the contents of the Cylinder Address Register. The unit Attention line, if it has been previously cleared by the program, is raised when the Seek has been completed or when a 100-ms period times out and the Seek has been unsuccessful. If the Seek is unsuccessful, the Selected Unit Seek Incomplete status line is raised and the appropriate interrupts occur. However, at the successful completion of a Seek function, the Selected Unit Ready status line is set Attention, Selected Unit Seek Incomplete, and Selected Unit Ready status signals are explained in Paragraph 3.10.1.

The Seek function also allows the program to specify the RP03 head (track) for the first block of data to be transferred. In this manner the track is specified for the non-seeking Read and Write functions.

NOTE

Because Seek is an initiate-type function, the disk pack drive unit need only remain selected for 16 μs following its execution. A system with several drives can start Seek operations in chain fashion, providing a 16-μs hold exists. If, at the conclusion of the 16-μs period, Interrupt on Done Enable is set, the PDP-11 will be interrupted.

On a multi-drive system, it is possible to initiate simultaneous Seek operations on several drives. The first drive to complete the Seek operation and respond by raising the Attention signal will cause an interrupt only if the AIE (attention interrupt enable) bit has been set.

The programmer usually expects to be interrupted at the completion of any Seek operation, and sets the AIE bit accordingly. Because the attention lines from each of the drives are effectively ORed (by the attention bits in the RPDS), when any drive raises the Attention signal, an interrupt is generated. At the completion of the interrupt, the AIE bit will be cleared by the hardware, thus inhibiting further interrupts during the data transfer which normally follows. When the AIE bit is enabled again by the program, any remaining or new Attention bits will initiate another interrupt and again clear AIE. In this way, each Attention can be handled individually or they can be handled collectively.

3.7.6 Write (No Implied Seek, Function = 5)

This Write function is identical to the other (Write, Function = 1) except that no initial Seek is performed, and the previously selected head remains selected. This function is particularly useful if the programmer desires to perform an additional transfer at the same starting surface and cylinder.

NOTE

In order to ensure that this function is performed at the correct disk address, a Seek specifying both cylinder and track address must be performed before initiating Write.

When this operation is performed, it is important to remember that if the data transfer is sufficiently large as to exceed the disk surface boundaries or cause the heads to reposition to the next cylinder, the drive will respond with an Attention signal. If the AIE bit has been set, this will, in turn, cause an interrupt.

3.7.7 Home Seek (Function = 6)

The Home Seek function is executed by loading its function code into the Function Register and setting GO. The Home Seek function recovers the head position after a Selected Unit Seek Incomplete. When this function is completed, the heads are placed at cylinder 000_8 and Unit Attention is set with Selected Unit Ready.

3.7.8 Read (No Implied Seek, Function = 7)

This Read function is identical to the other (Read, Function = 2) except that no initial Seek is performed, and the previously selected head remains selected. The note in Paragraph 3.7.6 also applies to this function.

When this operation is performed, it is important to remember that if the data transfer is sufficiently large as to exceed the disk surface boundaries or cause the heads to reposition to the next cylinder, the drive will respond with an Attention signal. If the AIE bit has been set, this will result in an interrupt.

3.8 HEADER OPERATIONS

If the HEADER bit in the RP11-C Controller Status Word (RPCS) is true, the Write and Read functions are modified as described in the following paragraphs.

3.8.1 Write Header

The Write Header (Write command with header bit set) command allows the PDP-11 programmer to change the effective address of any sector on the disk pack. The Write Header command is similar to the Write command with the following exceptions:

a. Only the sector's header word is written from memory. The RPWC must be loaded with multiples of -3 to specify the three PDP-11 words of one or more headers.

b. Sector addressing is absolute; i.e., the header is written in the sector addressed relative to the index mark. It is not written relative to the sector's previous address.

3.8.2 Read Header

The Read Header (Read command with header bit set) command is similar to the Read command with the following exceptions:

a. Only the sector's header word is read into memory. The RPWC must be loaded with -3 to specify the three words of the header.

b. Sector addressing is absolute; i.e., the header is read from the sector addressed relative to the index mark. It is not read relative to the sector's header word.

3.9 WRITE FORMAT

The Write function with header bit set in RPCS and the FORMAT ENABLE switch set causes the RP11-C to Write Format a disk pack. This command writes all 0s in the sync and data fields and writes the current sector address (relative to the index mark in the header field of each sector). This operation begins from the currently addressed sector and continues to the end of the pack.

3.10 PROGRAMMING

The bus address assignments are listed in Table 3-3.

Table 3-3
Bus Address Assignments

Bus Address	Register
776710	Device Status Register (RPDS)
776712	Error Register (RPER)
776714	Control Status Register (RPCS)
776716	Word Count (RPWC)
776720	Bus Address (RPBA)
776722	Cylinder Address (RPCA)
776724	Disk Address (RPDA)
776726	Maintenance 1 (RPM1)
776730	Maintenance 2 (RPM2)
776732	Maintenance 3 (RPM3)
776734	Selected Unit Cylinder Address (SUCA)
776736	Silo Memory (SILO)

All interrupt requests raised by the RP11-C specify location 254, on Bus Level 5.

3.10.1 Device Status Register (RPDS)

The Device Status Register (RPDS) holds the current state of the selected drive and the Attention signals from each of the eight possible drives. The eight attention bits are read/clear, and, as such, can be selectively cleared by moving a 1 to the desired bit location(s). The other bits of RPDS are read only. Table 3-4 lists the RPDS bits with the significance of each bit when set.

The ATTN bits can be altered under program control. When a DATOB is performed on this register, the previous contents are lost and the new value is written. A DATI will read the RPDS but will not alter its contents.

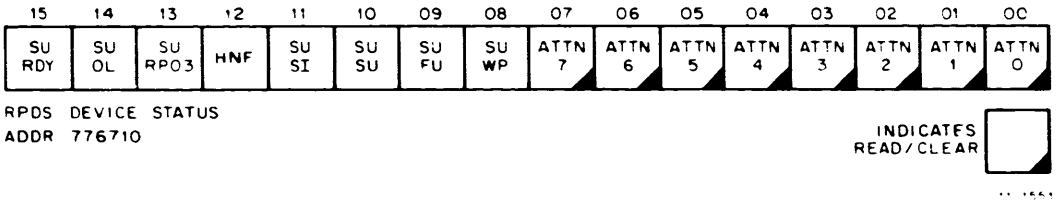
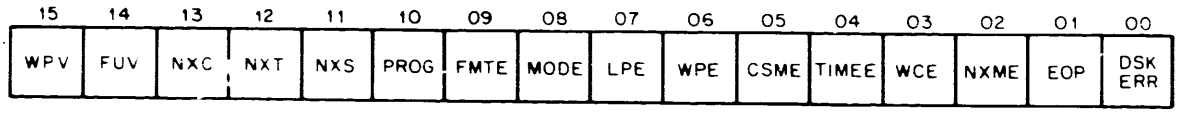


Table 3-4
Device Status Register (RPDS)

Bit	Function
00–07	DRIVE 00–07 ATTENTION. ATTENTION is set by a drive when a Seek is successfully completed or a 100-ms period elapses after Seek initiation indicating an incomplete Seek.
08	SELECTED UNIT WRITE PROTECTED. This bit is set when the WRITE PROTECT switch on the selected drive is set and when contents of RPCA and RPDA fall within the bounds of the selected address lockout if the WRITE LOCKOUT switch is set.
09	SELECTED UNIT FILE UNSAFE. The selected drive has detected a self-error condition and is prohibiting all operations.
10	SELECTED UNIT SEEK UNDERWAY. The selected drive has initiated a Seek operation, but the Attention signal has not yet been returned.
11	SELECTED UNIT SEEK INCOMPLETE. The selected drive has failed to successfully complete a Seek operation.
12	HEADER NOT FOUND. The selected drive has completed a full revolution without locating the addressed sector.
13	SELECTED UNIT RP03. The selected drive is an RP03.
14	SELECTED UNIT ON LINE. The selected drive ENABLE/DISABLE switch is set to ENABLE.
15	SELECTED UNIT READY. The selected drive is capable of performing another operation.

3.10.2 Error Register (RPER)

The Error Register (RPER) contains all error conditions generated within the RP11-C controller. In the normal mode, RPER is a read only register; in the maintenance mode, Write into RPER capability is provided. Table 3-5 lists the RPER bits with the significance of each bit when set.



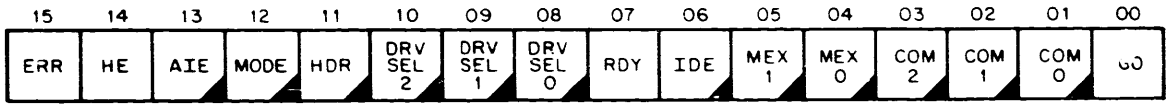
11-1552

Table 3-5
Error Register (RPER)

Bit	Function
00	DISK ERROR. OR condition of header has not been found and the selected unit Seek is incomplete.
01	END OF PACK. Data transfer (Read or Write) is attempted across the end of the last sector of the pack.
02	NON-EXISTENT MEMORY. More than 10 μs were required to complete a Unibus transaction.
03	WRITE CHECK ERROR. Data read from the disk pack does not compare with data read from memory during the Write Check operation.
04	TIMING ERROR. Data is lost because the Unibus did not respond in time to meet disk requirements.
05	CHECKSUM ERROR. Calculated checksum does not compare with that read from the disk.
06	WORD PARITY ERROR. Calculated word parity does not compare with that read from the disk.
07	LONGITUDINAL PARITY ERROR. Calculated longitudinal parity does not compare with that read from the disk.
08	MODE ERROR. Header operation was attempted while the RP11-C is in the PDP-11 mode.
09	FORMAT ERROR. Parity error was detected in a sector's header word.
10	PROGRAM ERROR. Data transfer operation was attempted with the content of the RPWC equal to zero, or an operation was attempted on an off-line drive, or while another instruction was still in progress.
11	NON-EXISTENT SECTOR. Disk operation was attempted when the content of the Sector Address Register was not within the 0 through 9_{10} range.
12	NON-EXISTENT TRACK. Disk operation was attempted when the content of the Track Address Register was not within the 0 through 19_{10} range.
13	NON-EXISTENT CYLINDER. Disk operation was attempted when the content of the Cylinder Address Register was not within the 0 through 405_{10} range.
14	FILE UNSAFE VIOLATION. Disk operation was attempted when SUFU was true.
15	WRITE PROTECT VIOLATION. Disk Write operation was attempted when SUWP was true.

3.10.3 Control Status Register (RPCS)

The bit configuration loaded into the Control Status Register (RPCS) initiates and controls a disk function. Table 3-6 lists each RPCS bit with the significance of each when set. All bits are read/write unless noted otherwise.



RPCS: CONTROL STATUS
ADDR: 776714

11-155

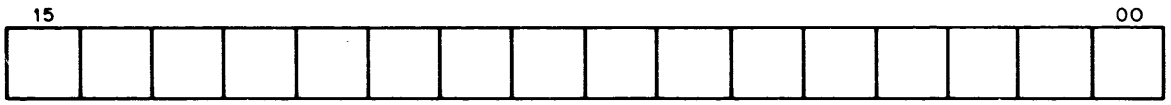
Table 3-6
Control Status Register

Bit	Function
00	GO. Set from the bus causes the RP11-C to initiate the operation encoded in bits 03 through 01 of the RPCS. This write-only bit is always read as a 0.
01–03	FUNCTION BITS. Specify the operation to be performed. These functions are described in detail in Paragraph 3.7.
04–05	MEMORY EXTENDED ADDRESS. Specifies the 32K field of PDP-11 memory used in data transfer.
06	INTERRUPT ON DONE (ERROR) ENABLE. Causes the RP11-C to raise an interrupt request when a disk operation is complete, or if an error occurs.
07	READY. The RP11-C is in a condition to accept and execute a new operation. READY is a read-only bit.
08–10	DRIVE SELECT. Specify the disk drive which is to be the subject of any controller action.
11	HEADER. The function of the Function Register is a Header operation.
12	MODE. The RP11-C is conditioned to read or write disk packs in DECsystem-10 or PDP-15 format.
13	ATTENTION INTERRUPT ENABLE. Causes the RP11-C to raise an interrupt request whenever any drive raises its Attention line. This bit is cleared at the completion of the interrupt.
14	HARD ERROR. OR of all errors except data errors. This is a read-only bit.
15	ERROR. OR of all errors. This is a read-only bit.

NOTE
The RP11-C device handler software must include routines that will test the ERR and HE flags to validate the current operation before proceeding.

3.10.4 Word Count Register (RPWC)

The Word Count Register (RPWC) is loaded from the bus and specifies the number of words to be transferred during Read, Write, or Write Check operations. Incrementation takes place after a memory transaction has occurred and the RPWC, therefore, must be loaded with the 2's complement of the number of words to be transferred. The RPWC is a read/write register.



RPWC: WORD COUNT
ADDR: 776716

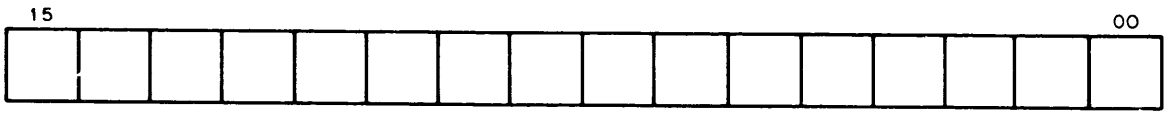
11-1555

NOTE

Because the disk pack system uses 36-bit disk words, the word count must be equal to a multiple of the number of PDP-11 memory words per disk work; i.e., in PDP-11 mode, there are two PDP-11 words per disk word and the word count must be a multiple of two. In PDP-10/15 mode, there are three PDP-11 words per disk word, and the word count must be a multiple of three.

3.10.5 Bus Address Register (RPBA)

The Bus Address Register (RPBA) is loaded from the bus and specifies the bus address of data transferred during Read, Write, or Write Check operations. Incrementation takes place after a memory transaction has occurred. The RPBA, therefore, is loaded with the address of the first data word to be transferred (not first data word address minus one). The RPBA is a read/write register.

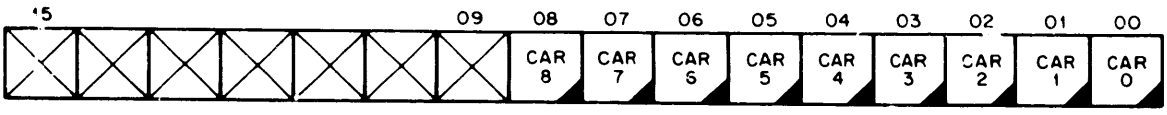


RPBA BUS ADDRESS
ADDR: 776720

11-1556

3.10.6 Cylinder Address Register (RPCA)

Bits 08–00 of the Cylinder Address Register (RPCA) are loaded from the bus and specify the disk cylinder for any disk operation. Bits 08–00 are read/write bits. Bits 15–09 are not used.



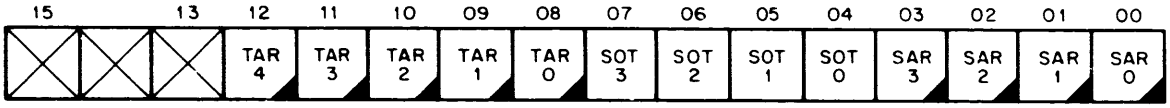
RPCA CYLINDER ADDRESS
ADDR 776722

11-1553

3.10.7 Disk Address Register (RPDA)

Bits 03–00 of the Disk Address Register (RPDA) are loaded from the bus and specify the disk sector address for any operation other than Seek or Home Seek. Bits 03–00 are read/write. Bits 07–04 are read-only bits which contain the current physical sector (number of sectors past index) of the selected drive.

Bits 12–08 are loaded from the bus to specify the track address for any disk operation. Bits 12–08 are read/write.

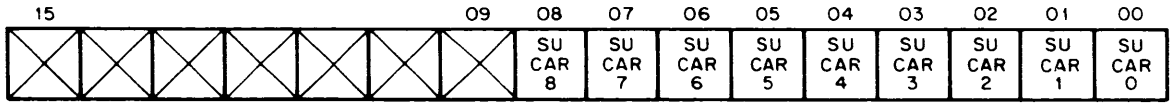


RPDA: DISK ADDRESS
ADDR: 776724

11-1

3.10.8 Selected Unit Cylinder Address (SUCA)

The Selected Unit Cylinder Address (SUCA) register stores the contents of the selected RP03 cylinder address register in bits 08–00.



SUCA: SELECTED UNIT CYLINDER ADDRESS
ADDR: 776734

11-1550

3.11 MAINTENANCE REGISTERS

3.11.1 Maintenance 1 Register (RPM1)

The Maintenance 1 Register (RPM1) is read-only and provides a means for the PDP-11 to examine the state of the RP11-C's interface to the RP03 Disk Pack Drive. This register may be read at any time, but because of the asynchronous operation of the interface, meaningful results cannot be expected unless the RP11-C is in the maintenance mode. Table 3-7 lists the Maintenance 1 Register bits with the significance of each.

Table 3-7
Maintenance 1 Register, Address 776726

Bit	Function
00–07	BUS OUT 00–07. BUS OUT 00–07 signals to the RP03 Disk Pack Drive.
08	SET CYLINDER. State of the control tag SET CYLINDER.
09	SET HEAD. State of the control tag SET HEAD.
10	CONTROL. State of the control tag CONTROL.
11	SILO IN READY. Silo is ready to receive data.
12	SILO OUT READY. Silo has data ready for output.

3.11.2 Maintenance 2 Register (RPM2)

The Maintenance 2 Register (RPM2) is write-only and, in conjunction with RPM3, allows the PDP-11 to simulate the RP03 Disk Pack Drive while in the maintenance mode. Loading this register in the normal mode has no effect. Table 3-8 lists the Maintenance 2 Register bits and their significance.

3.11.3 Maintenance 3 Register (RPM3)

The Maintenance 3 Register (RPM3) is write-only and, in conjunction with RPM2, allows the PDP-11 to simulate the RP03 Disk Pack Drive while in the maintenance mode. Loading this register in the normal mode has no effect. Table 3-9 lists the Maintenance 3 Register bits with their significance.

Table 3-8
Maintenance 2 Register, Address 776730

Bit	Function
00–07	MAINTENANCE ATTENTION 00–07. Simulate the Attention signals from the eight possible disk drives.
08–15	MAINTENANCE CYLINDER ADDRESS REGISTER. Set by the bus, simulate the lower eight bits of the Cylinder Address Register signals from the selected drive.

Table 3-9
Maintenance 3 Register, Address 776732

Bit	Function
00	MAINTENANCE CLOCK. When set by the bus causes one cycle of the RP11-C control clock to be generated.
01–07	Not Used
08	MAINTENANCE SECTOR. When set by the bus simulates a Sector Pulse from the selected drive.
09	MAINTENANCE END OF CYLINDER. When set by the bus simulates the selected drive signal End of Cylinder.
10	MAINTENANCE SEEK INCOMPLETE. When set by the bus simulates the selected drive signal Seek Incomplete.
11	MAINTENANCE FILE UNSAFE. When set by the bus simulates the selected drive signal File Unsafe.
12	MAINTENANCE INDEX. When set by the bus simulates an Index Pulse from the selected drive.
13	MAINTENANCE ON LINE. When set by the bus simulates the selected drive signal On Line.
14	MAINTENANCE READY. When set by the bus simulates the selected drive signal Ready.
15.	MAINTENANCE READ ONLY. When set by the bus simulates the selected drive signal Read Only.

3.11.4 Silo Memory

The Silo Memory is a 64-word, 16-bit, first-in/first-out (FIFO) MOS storage device. It can be loaded from the Unibus whenever the SILO IN READY bit in the Maintenance 1 Register is logic 1. If no readout is performed, the silo will accept 64 words before dropping SILO IN READY. The silo may be read whenever the SILO OUT READY bit in the Maintenance 1 Register is logic 1. As soon as all words previously stored have been read out, SILO OUT READY will go low and remain low until further data is stored. A transit time of 32 μs maximum is required for an input word to "bubble" to the output.

For maintenance purposes, the Silo Memory is assigned a Unibus device register address, 776736. This allows maintenance personnel to check out that portion of the RP11-C by moving a data word to and from the Silo Memory.

CHAPTER 4
THEORY OF OPERATION

4.1 GENERAL

This chapter describes how the RP11-C logic executes the eight command functions specified by the command code that is issued by the processor under program control. Figure 4-1 shows the operational flow for each RP11-C function. The RP11-C remains in the Idle state until a function is initiated by setting the GO bit in the RPCS. Then, depending upon the command code loaded into the RPCS, the RP11-C logic proceeds through the logic operations required to execute the command.

Each function is controlled by the information loaded into the RP11-C register and the RP11-C control switch settings. When the function has been satisfactorily executed, the RP11-C is done and returns to the Idle state. If the Interrupt on Done (IDE) bit in the RPCS is set, the RP11-C logic initiates a program interrupt to notify the program.

The RP11-C logic checks for numerous error conditions throughout the execution of each function. The error conditions are described in Chapter 3. At the point that an error is detected, the RP11-C logic terminates the current operation and proceeds to Done, as indicated in Figure 4-1.

NOTE

If an error is detected during an operation that normally terminates at Done, such as Read Data or Write Data, that operation will not be terminated, but will continue until Done.

The RP11-C device handler software must include routines that will test the RP11-C error flags to validate the operation before proceeding.

The flow chart terminals shown in Figure 4-1 represent complex operations that are sometimes common to more than one function. For example, the Seek and Search operations are common to the Read, Write, and Write Check functions. Detailed flow chart descriptions of the complex operations and special functions are included in this chapter.

The contents of this chapter are organized to provide optimum flow chart continuity, as the best means of understanding several related operations. Therefore, some major topics are not presented in any chronological order. For example, a disk pack must be formatted before any Search, Read Data, or Write Data operations can be executed. However, the Write Format operation is described in Paragraph 4.12.

4.1.1 RP11-C Functional Block Diagram

Figure 4-2 is a unit block diagram of the RP11-C that shows the data paths, major control signals, and functional sections. The block diagram is also intended for use as a guide to the block schematics provided in the RP11-C engineering drawing set. The reference number in the lower corner of each block indicates the drawing that shows all the logic within that functional block. For example, "D30" indicates that the 64 X 16 Silo Memory logic is shown on drawing D-BS-RP11-C-30.

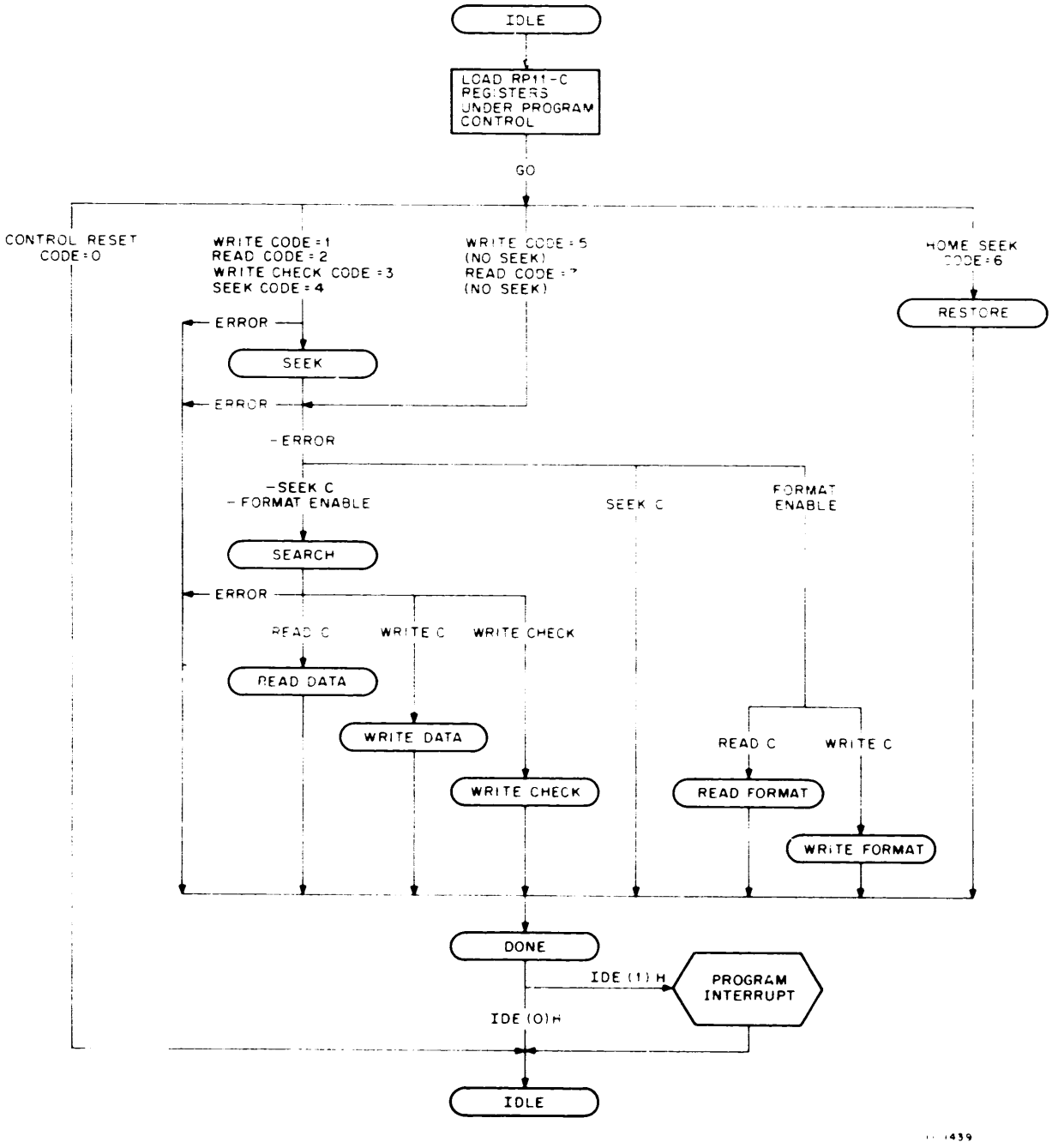


Figure 4-1 Overall Operational Flow Chart

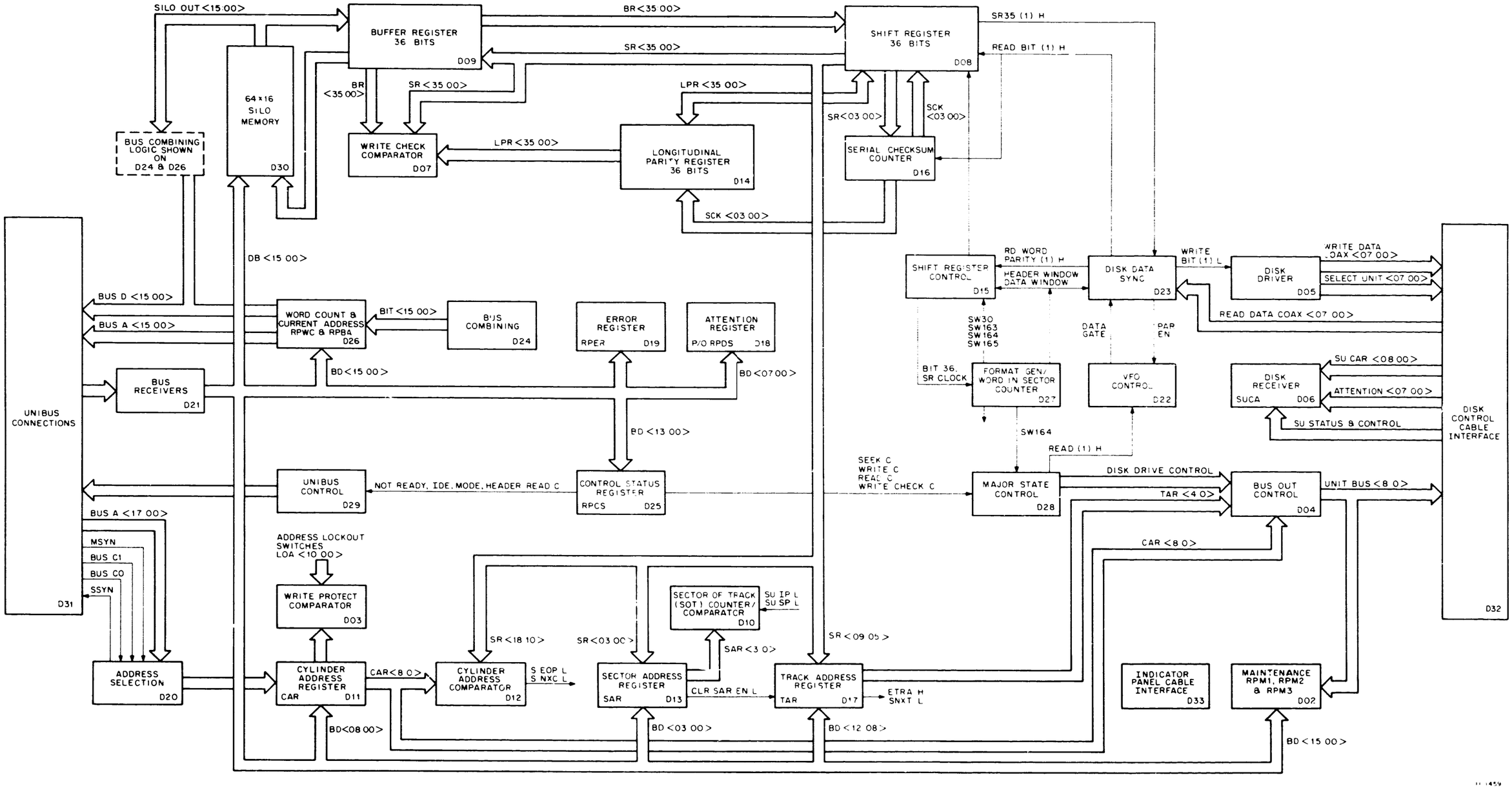


Figure 4-2 RP11-C Disk Pack Controller, Unit Block Diagram

4.1.2 Drawing Conventions

Appendix A describes the flow chart and logic symbology that is used in this manual and in the RP11-C engineering drawings.

4.2 DEVICE REGISTERS

Prior to executing any RP11-C function, the applicable RP11-C registers must be loaded under program control, as described in Chapter 3. The following paragraphs describe how each of the registers is implemented in the hardware. Figure 4-2 shows the relationship between the device registers and indicates where they are shown in the block schematics.

4.2.1 Bus Address Register (RPBA)

The RPBA is part of the M795 Word Count and Bus Address module shown on drawing D26. An M795 module circuit schematic is included in the engineering drawings. It is loaded from bus data lines BD (15:00) H when BUS TO RPBA L is asserted. This happens when the processor initiates a DATO bus transaction that specifies the RPBA address 776720.

Each time a Unibus word transfer is transacted, the RPBA is incremented to the next word address by ADDRESS TO BUS H. A RPBA overflow output, BAOF L, is asserted if the register is incremented from all 1s to all 0s. BAOF L is used by the RP11-C to increment the extended memory bits MEX 1–0.

ADDR TO BUS L gates the RPBA contents to the Unibus address lines during each transaction. When the contents of the RPBA are read under program control, RPBA TO BUS L gates the contents of the RPBA to the Unibus data lines.

4.2.2 Word Count Register (RPWC)

The RPWC is included as part of the M795 Word Count and Bus Address module shown on drawing D26. It is loaded from bus data lines BD (15:00) H when BUS TO RPWC L is asserted. It is loaded with the 2's complement of the number of words to be transferred. This happens when the processor initiates a DATO bus transaction that specifies the RPWC address 776716.

Each time a Unibus word transfer is transacted, the RPWC is incremented by 1 by ADDRESS TO BUS H. During the transfer of the last word, the content of the RPWC will be all 1s. When ADDRESS TO BUS H increments the RPWC again, the resultant all 0s will assert the WCOF L output, which is used to terminate the transfer. The RPWC limits the maximum words that can be transferred to 2^{16}.

The RPWC can also be read under program control. A DATI that specifies the RPWC address 776716 produces RPWC TO BUS L, which gates the RPWC contents to the Unibus data lines.

4.2.3 Cylinder Address Register (RPCA)

The position of all heads, vertically aligned with respect to the vertical axis that passes through the center of all disk pack surfaces, is called a cylinder, as described in Chapter 3. Head positioning is controlled by a linear motor that stops the read/write heads in one of 406 different cylinders. These cylinders are coded 00_8 through 625_8, from the outer-most cylinder (0) to the inner-most cylinder (405_{10}). Cylinders are addressed by a 9-bit register called the Cylinder Address Register (CAR).

Refer to drawing D11, which shows the CAR logic. The CAR is loaded from bus data lines BD (08:00) when a DATO to RPCA address 776722 is initiated by the processor. CAR incrementation is a function of the Search operation (Paragraph 4.4.4). Any CAR contents greater than 625_8 (405_{10}) are detected as a non-existent cylinder address (626_8 through 777_8). Error detection logic that raises the NXC error flag is shown on drawing D12.

4.2.4 Track and Sector Address Register (RPDA)

4.2.4.1 SAR – The bottom surface of every disk pack is notched to divide each disk surface into ten equal sectors. (There are actually 20 notches, but only half are used with the RP11-C). These sectors are addressed by loading a 4-bit register called the Sector Address Register (SAR), shown on drawing D13. The legal sector addresses are coded 00_8 through 11_8, which leaves illegal codes 12_8 through 17.

The SAR is loaded from bus data lines BD (03:00) when a DATO to RPDA address 776724 is initiated by the processor. SAR incrementation and clearing is a function of the Search operation (Paragraph 4.4.4). Drawing D13 shows the logic that decodes illegal sector addresses to assert E SEC A L (Error Sector Address). This signal sets the Non-Existent Sector (NXS) flag during the ERR SYNC 1 (1) H interval.

4.2.4.2 TAR – A separate read/write head is provided for each of the twenty disk pack recording surfaces. The heads are mounted in parallel and in vertical alignment with each other, and are attached to a common head tower. The heads are selected by a 5-bit register called the Track Address Register (TAR), shown on drawing D17.

The TAR is loaded from bus data lines BD (12:08) when a DATO to RPDA address 776724 is initiated by the processor. TAR incrementation and clearing is a function of the Search operation (Paragraph 4.4.4). Drawing D17 shows the error detection logic that decodes illegal track addresses 24_8 through 37_8 to assert ETRA H (Error Track Address). This signal sets the NXT flag during the ERR SYNC 1 (1) H interval.

4.2.5 Control Status Register (RPCS)

Drawing D25 shows the logic that implements the RPCS in hardware. The RPCS is loaded from bus data lines BD (15:00) when a DATO is initiated to RPCS address 776714 by the processor. The function of each bit in the RPCS is described in Chapter 3.

Note that the GO bit is not stored in a flip-flop. Instead, it asserts a level which initiates the specified operation and sets the NOT READY bit. Note also that the ERR (Error) and HE (Hard Error) bits are not stored in flip-flops, but are logic levels asserted by the error detection logic to terminate an operation.

4.3 SEEK

The Seek operation positions the selected RP03 read/write heads to the selected cylinder and track locations. This is accomplished by issuing a series of control commands to the selected unit. As indicated in the operational flow chart (Figure 4-1), the Seek operation is common to the Write, Read, Write Check, and Seek functions.

4.3.1 Initiation

Figure 4-3 is a detailed flow chart of the logic steps involved in the Seek operation. The flow chart is initially entered through the SEEK terminal. When the RP03 read/write heads need to be repositioned during the course of an extensive Write, Read, or Write Check operation, the flow is re-entered through the Search operation (Paragraph 4.4.4).

As indicated by the drawing references, most of the logic is shown on drawing D28, sheets 1 and 2. The C CLK (Control Clock) is used to step through the Seek operation. This is a 1-MHz clock that is available whenever the MAINTEN switch is off. During the initial Seek, the logic checks for NXC, NXT, NXS errors during the time ERR SYNC 1 is set. If any are detected, the Seek operation terminates at Done. If the IDE bit is set, the processor is notified by a program interrupt (Paragraph 4.8.1).

Refer to the ERR SYNC timing diagram shown in Figure 4-4. If none of these errors are detected, ERR SYNC 2 gets set. If the selected unit is ready and no other operation is in progress, DO H is asserted. For a Seek function this is sufficient to set SEEK SYNC. For Write, Read, or Write Check functions, DATA CONT H must also be asserted to set SEEK SYNC.

DO H and SEEK SYNC (1) H initiate a chain of control commands that are sent to the selected RP03. Each command is transmitted by a Bus Out Control (BOC) cycle.

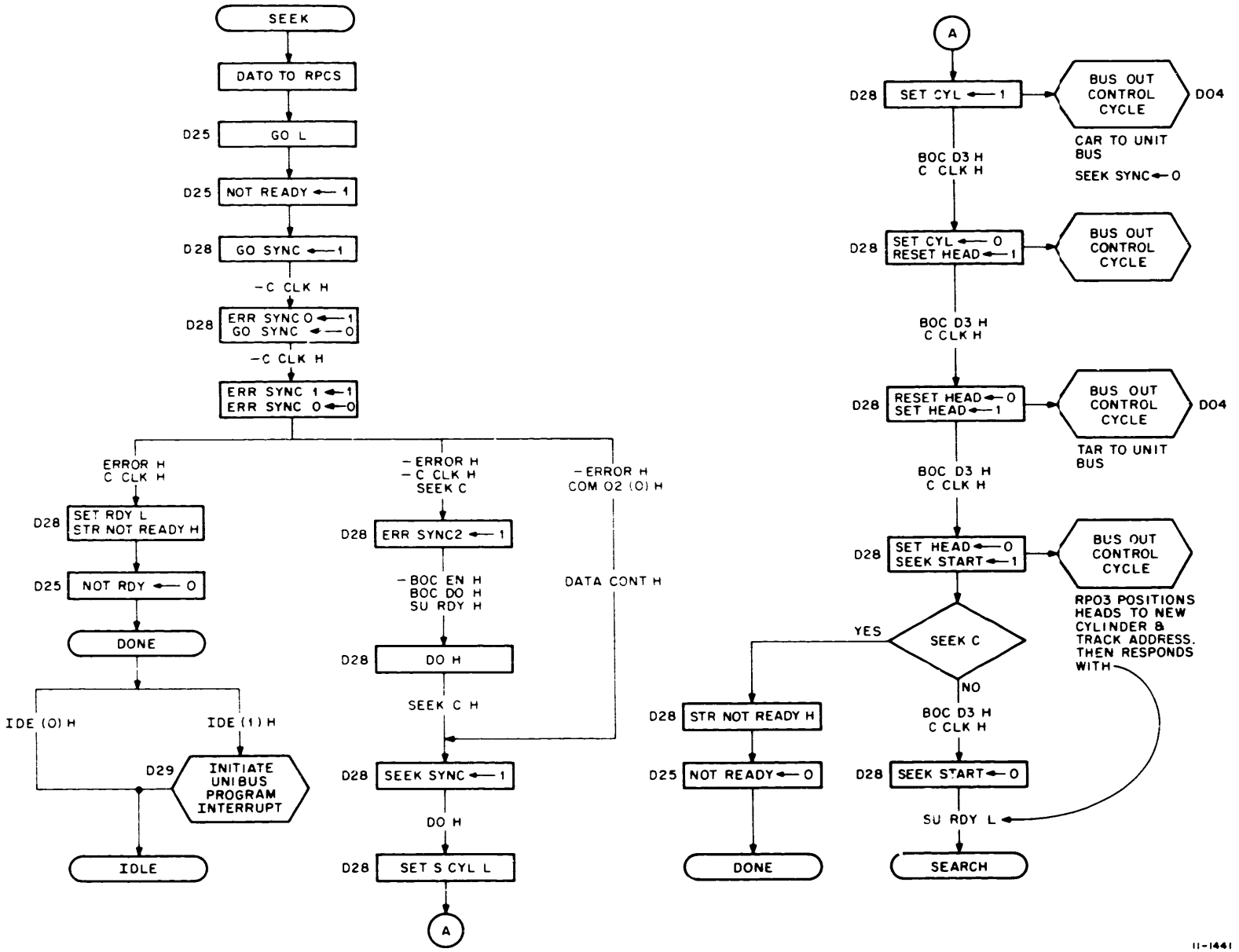


Figure 4-3 SEEK Operation, Detailed Flow Chart

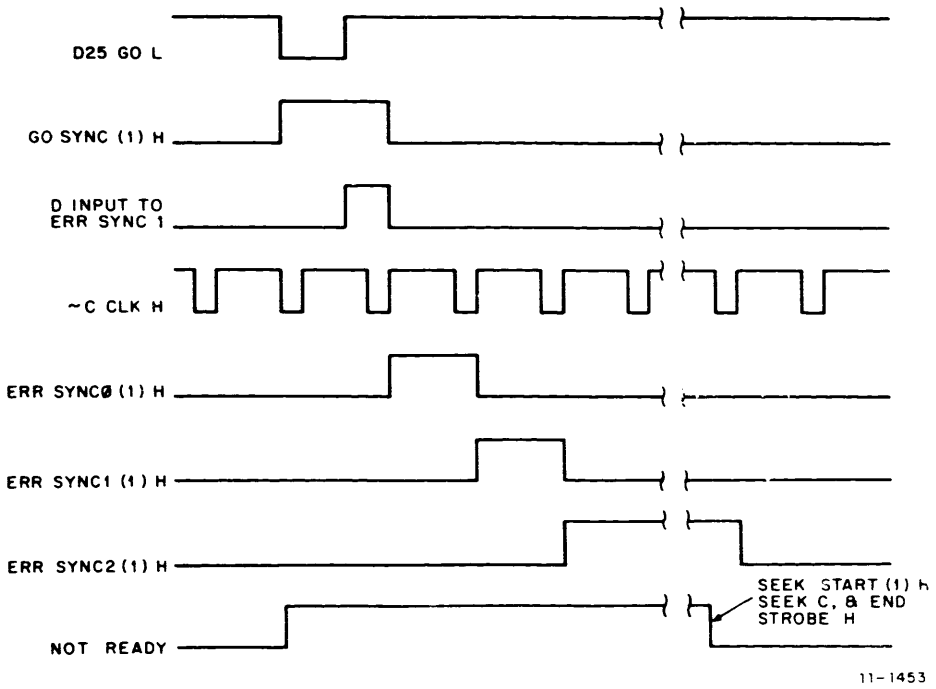


Figure 4-4 ERROR SYNC Timing Diagram

4.3.2 Bus Out Control Cycle

Refer to drawing D28, sheet 2 and the Bus Out Control (BOC) timing diagram shown in Figure 4-5. The BOC cycle is initiated by BOC EN H. The timing provides a 3-μs window, BOC D0, on the bus line to the selected RP03. Centered in this window is a 1-μs strobe pulse, BOC D2 H, that is sent on the tag line to the selected RP03. The bus and tag line levels are used to strobe the appropriate command into the RP03. If the command is not Read or Write, SELECT HEAD H allows the cycle to advance to BOC D3, which clears the command and ends the strobe.

NOTE

When the command is Read or Write, BOC D0 H and BOC D2 H remain asserted until the Read or Write operation is completed. Only then will BOC D3 H be asserted to end the BOC cycle.

4.3.3 Seek Sequence

The four BOC cycles that are initiated to execute the Seek sequence are shown on the flow chart (Figure 4-3):

a. SET CYL initiates the first BOC cycle. During this cycle, the contents of the CAR are gated onto the unit bus as shown on drawing D04.

b. BOC D3 H and C CLK H reset SET CYL and set RESET HEAD, which initiates the next BOC cycle. During this cycle, the RP03 Head Address Register (HAR) is reset. At the end of this cycle, BOC D3 H is again asserted.

c. BOC D3 H and C CLK H reset RESET HEAD and set SET HEAD, which initiates the third BOC cycle. During this cycle, the contents of the RP11-C TAR are gated on the unit bus to the selected RP03 Head Address Register. At the end of this BOC cycle, BOC D3 H is asserted.

d. BOC D3 H and C CLK H reset SET HEAD and set SEEK START which starts the RP03 head positioning sequence. This is the final BOC cycle of the Seek sequence.

Upon receiving the Seek Start command, the RP03 positions the read/write heads to the new cylinder and track address. When it is done, it sends an SU RDY signal to the RP11-C.

NOTE

If the RP11-C is executing a Seek function, it is Done at this time.

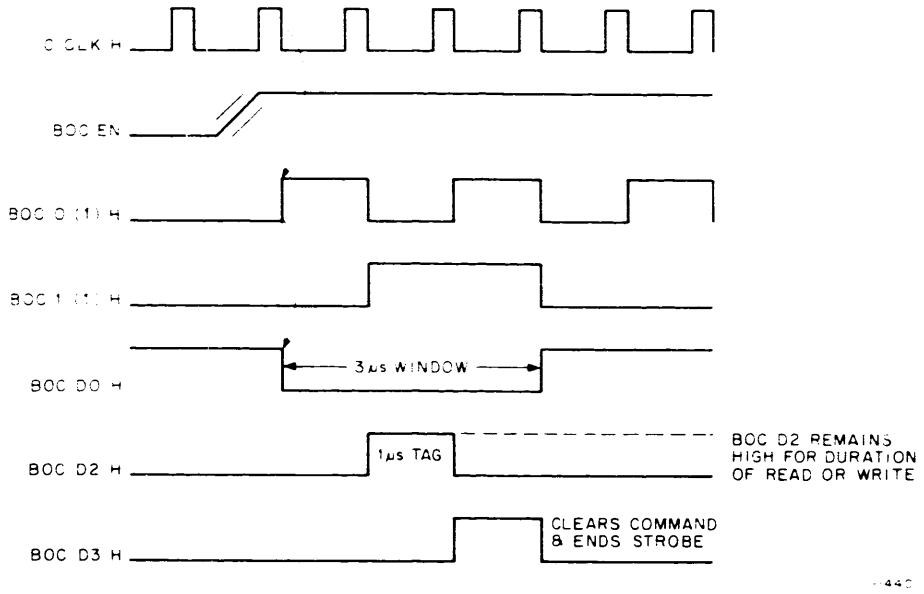


Figure 4-5 Bus Out Control (BOC) Cycle, Timing Diagram

4.4 SEARCH

The purpose of the Search operation is to find the sector on the disk pack that corresponds to the sector address in the RP11-C SAR. The general flow chart (Figure 4-1) shows that the Search operation is entered from the Seek for Write, Read, and Write Check functions.

NOTE

If the selected unit has been previously commanded to seek a specified cylinder and track, the Write code 5 or Read code 7 is used at this point to eliminate Seek and enter Search directly upon receipt of GO.

A new Seek operation is initiated by any transfer that involves segments on more than one disk surface. Figure 4-6 is a detailed flow chart of the complete Search operation.

4.4.1 Initialization

The Search operation is initiated by the receipt of an SU SECTOR L pulse from the selected RP03. As a result READ is set and a BOC cycle is initiated to send the Read command to the RP03.

NOTE

READ remains set until the end of header on a Write, or until the end of sector on a Read.

The received sector pulse signal also clears the Bit Counter (BCNT) and the Word in Sector Counter (WSC).

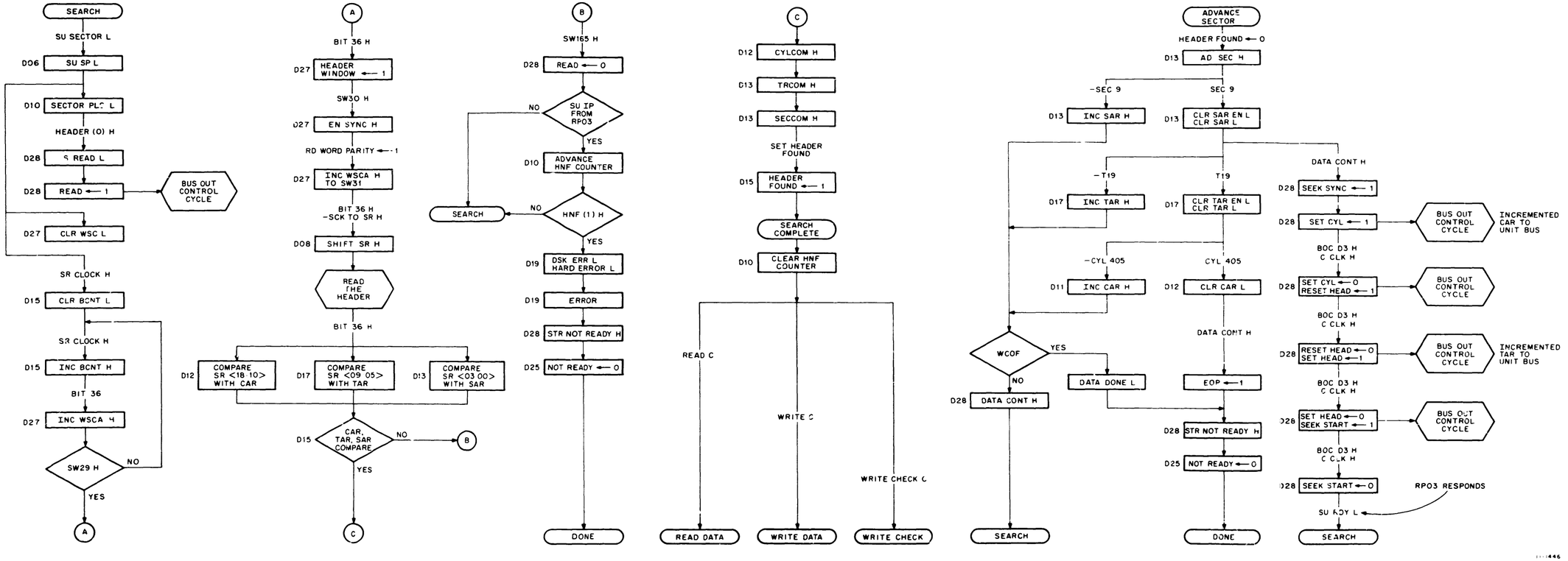


Figure 4-6 Search Operation, Detailed Flow Chart

4.4.1.1 Bit Counter (BCNT) – The Bit Counter, shown on drawing D15, is a modulo-37 counter used to define the boundaries of each 37-bit word. The Bit Counter is initially cleared by the selected unit sector pulse SU SP L, synchronized by SR CLOCK H. It is then incremented by each SR CLOCK H pulse.

Two important bit counts are decoded. BIT 31 H is decoded to indicate the last data bit before the serial checksum. BIT 36 H is decoded to indicate the last bit (the parity bit) before the next word. BIT 36 L is also used to clear the Bit Counter for the next word.

The Bit Counter is inhibited by EN SYNC L twice during each sector (drawing D27). The first time occurs at the beginning of the header window. SW30 H and HEADER WINDOW (1) H assert EN SYNC L to inhibit INC BCNT H. The Bit Counter stops during SW30 and waits for the 1 bit at the end of the pre-header sync. As soon as that 1 bit is detected (RD WORD PARITY (1) H), INC WSCA H is asserted to increment the WSC to SW31.

EN SYNC L is again asserted to stop the bit counter by SW35 H and DATA WINDOW (1) H. The Bit Counter stops during SW35 and waits for the 1 bit at the end of the post-header sync. As soon as that 1 bit is detected, INC WSCA H increments the WSC to SW36 and the Bit Counter continues to count to 37 as each disk data word is read or written.

4.4.1.2 Word In Sector Counter (WSC) – The Word in Sector Counter (WSC), shown on drawing D27, is used to generate the format of the disk sector during Write operations and is used to interpret the serial data read from the sector during the Search and Read operations. Figure 4-7 shows the format of a sector of the RP02P Disk Pack. Each disk sector consists of 165 words. These are designated by the WSC as 0 through 164.

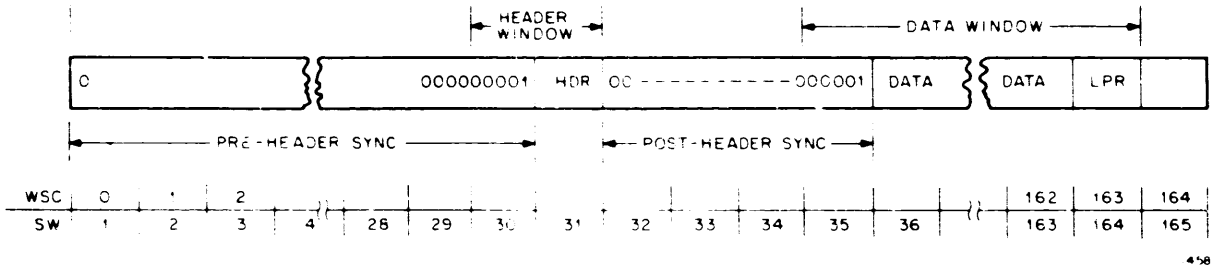


Figure 4-7 Sector Format Details

NOTE
The 165 states of the WSC are designated SW01 through SW165.

The WSC is cleared by the selected unit sector pulse, SU SP L, that is detected at the beginning of each disk sector. It is then incremented by assertion of INC WSCA H. Incrementation is usually accomplished by BIT 36 H and SR CLOCK H. However, the Bit Counter is inhibited during SW30 and SW35. Under these conditions EN SYNC H is asserted and the logic waits for the 1 bit in the pre-header and post-header sync patterns (RD WORD PARITY (1) H) to assert INC WSCA H.

NOTE
The WSC stages are designated such that WSC0 is the most significant bit and WSC7 is the least significant bit.

Several important sector word counts are decoded by the logic shown on drawing D27. The purposes of these decoded signals are summarized in Table 4-1.

Table 4-1
Decoded Sector Word Signal Functions

Sector Word	Used With	Purpose
SW29	INC WSCA H	Used to set the header window, which starts at SW30.
SW30	HEADER WINDOW (1) H	Inhibits Bit Counter and allows logic to wait for 1 bit in pre-header sync before incrementing the WSC.
SW31	INC WSCA H	Clears the HEADER WINDOW flip-flop. Enables SR TO BR during header mode operations. Sets the FORMAT ERROR flag if the 1 bit in pre-header or post-header sync pattern is not present.
SW35	BIT 31 H DATA WINDOW (1) H	Used to set the data window, which starts at SW36. Inhibits Bit Counter and allows logic to wait for 1 bit in post-header sync before incrementing the WSC.
SW163		Used with BIT 36 to provide LPR TO SR during WRITE C.
SW164	INC WSCA H	Clears the DATA WINDOW flip-flop after the LPR word. -SW164 enables D CLK and SR TO BR.
SW165		Indicates end of sector. Clears HEADER FOUND flip-flop.

4.4.2 Pre-Header Sync

At this point, it is important to review the sector format. Figure 3-4 shows the sector format from a programmer's viewpoint. Figure 4-7 shows some additional details that are important to understanding how the RP11-C logic operates.

The pre-header sync consists of 30 37-bit words, all 0s except for the very last bit. The Bit Counter starts incrementing at the SR CLOCK H frequency. (At this time, SR CLOCK H is provided by CLOCK L from the VFO, as described in Paragraph 4.11.) At each bit 36, the WSC is incremented. The Bit Counter and WSC continue incrementing to sector word 29 (SW29), bit 36 at which time HEADER WINDOW is set.

During SW30, the last word of pre-header sync, the logic waits for the 1-bit to be read, as indicated by RD WORD PARITY (1) H.

NOTE
SW30 H and HEADER WINDOW (1) H assert EN SYNC L, which enables the Bit Counter to be cleared.

Therefore, the Bit Counter and the WSC will not advance until the 1-bit at the end of pre-header sync is read from the disk. If the WSC should ever increment to SW31 with RD WORD PARITY (0) H, the FMTE flag (drawing D19) will be set to indicate a format error.

4.4.3 Header Read

When the last bit of the pre-header sync is a 1, INC WSCA H is asserted to advance to SW31, which contains the header for the sector. SHIFT SR H allows READ BIT (1) H to be shifted into the SR. At bit 36, the contents of the SR are compared with the CAR, TAR, and SAR. If the Seek operation was successful, the CAR and TAR should always compare. The Search operation is primarily for the purpose of locating the correct sector. However, all three registers are compared with the sector header word in the SR.

If they do not compare, the logic takes the B path through the Search operation (Figure 4-6). This returns to search the next sector. But first, it checks to see if all ten sectors have been searched. If they have, a selected unit index pulse (SU IP) from the RP03 will advance the Header Not Found (HNF) counter. If the correct header has not been found after two complete disk revolutions, HNF will set, indicating a hard error.

When the CAR, TAR, and SAR compare with appropriate fields of the SR, CYLCOM H, TRCOM H, and SECCOM H are ANDed to set HEADER FOUND. At this point, the Search operation is complete, and, depending upon the function being executed, the logic flow enters the Read Data, Write Data, or Write Check operations.

4.4.4 End of Search

At the end of a successful Search operation, the SAR (and possibly the TAR and CAR) will be incremented in anticipation that the specified function will continue into the next sector. The updating process in initiated by HEADER FOUND (1) H and is shown in the Advance Sector branch of the Search operation flow chart (Figure 4-6).

If the heads were not already over sector 9, the SAR is incremented and, pending no word count overflow, the logic waits for the next sector pulse to begin the Search operation again. However, after the last sector, the SAR must be cleared and the TAR incremented. Also, after the last track address in a cylinder has been searched, the TAR must be cleared and the CAR incremented.

When the CAR or TAR have been incremented, new Seek commands are sent to the selected RP03, via BOC cycles, to reposition or select the heads for the new cylinder and track addresses.

4.5 READ DATA

A detailed flow chart of the Read Data operation is shown in Figure 4-8. The Read Data logic flow is described at this point in text to provide the reader with a smooth transition from HEADER FOUND (which is part of the Search operation) to DATA WINDOW. However, it is important at this point for the reader to be completely familiar with the VFO and Read Data Separator logic, which is described in Paragraph 4.11. Also, you should be aware of how the serial checksum is generated and written for each disk word (Paragraph 4.9) and how the longitudinal parity word is generated and written for each sector (Paragraph 4.10).

4.5.1 Data Window

Once the header is found during the Search operation, the logic is directed to READ DATA by the Read function (code 2 or 7). The Bit Counter and WSC continue to increment, reading all 0s in post-header sync words SW32, SW33, and SW34. At bit 31 of SW35, the logic sets DATA WINDOW and waits for the 1-bit at the end of post-header sync. The Bit Counter is cleared by EN SYNC L, which is asserted by DATA WINDOW (1) H and SW35 H. Thus, only RD WORD PARITY (1) H will increment the WSC to SW36, the beginning of the data words.

4.5.2 Reading Data

Path A of Figure 4-8 shows how 164 words of data are read from the disk and serially shifted into the SR. At bit 36, the contents are gated to the BR. They are also exclusive-ORed into the LPR. The LPR operation is described in Paragraph 4.10. Each time a word is shifted into the BR, BR STR 1 H asserts SILO REQ H and the logic flow shown in path B is initiated. Figure 4-9 shows how the logic checks for odd parity in each disk word. BR STR 1 H is asserted only for the 128 data words in the sector (SW36 through SW163). It is inhibited by SW164; thus SW164 (the LPR word for the sector) is only exclusive-ORed to the LPR. DATA WINDOW is cleared at the end of SW164.

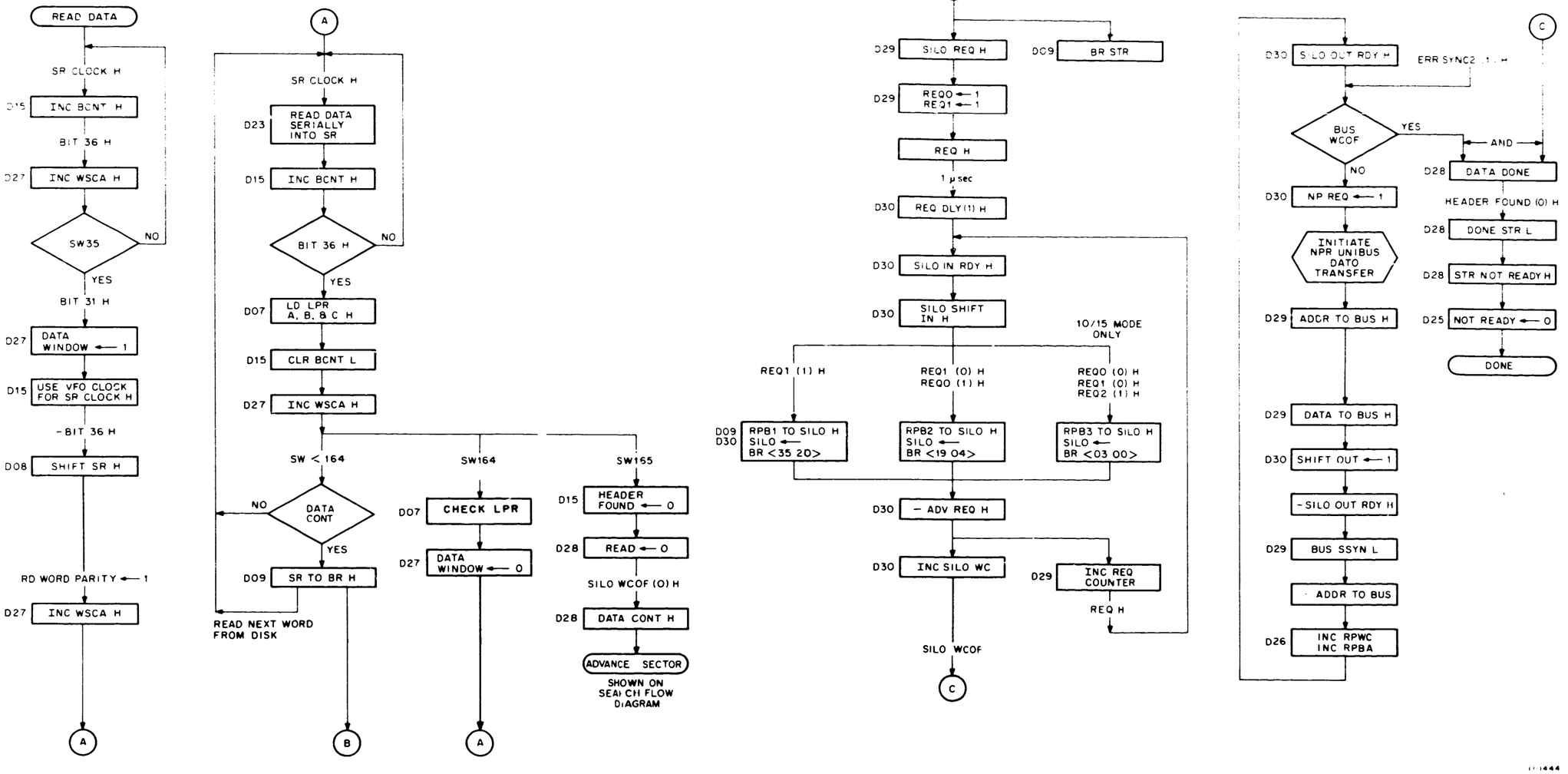


Figure 4-8 Read Data Operation, Detailed Flow Chart

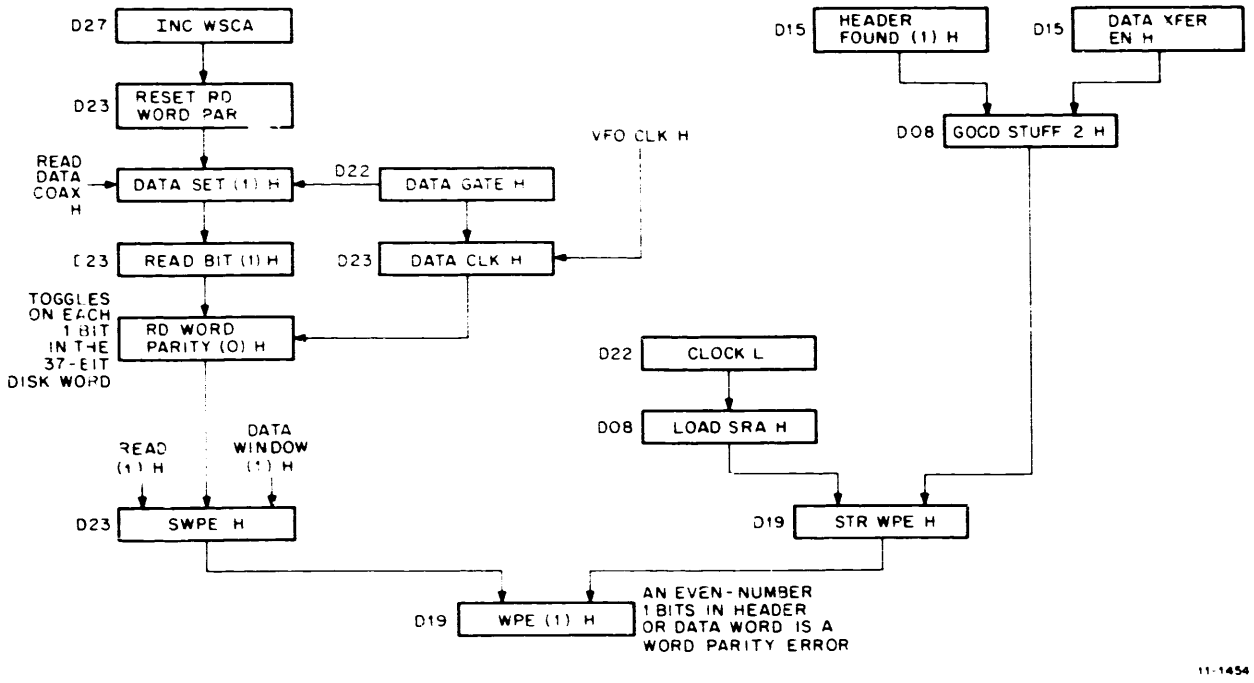


Figure 4-9 Word Parity Error (WPE) Detailed Flow Chart

The Bit Counter and WSC continue to increment to SW165, which clears HEADER FOUND and READ and returns to the Search operation, if there is no word count overflow.

NOTE

While each data word is being shifted into the SR, the silo word counter is being incremented as earlier words are being loaded into the silo from the BR. Once the specified number of words has been loaded into the silo, SILO WCOF inhibits SR TO BR H. Although the remaining words in the current sector will be shifted into the SR, they will not be transferred to the BR.

4.5.3 Loading the Silo Memory

As soon as the first word is transferred from the SR to BR, the logic begins to load the 64-word Silo Memory, as shown in Path B of the flow chart. A request counter keeps track of which BR bits are loaded into the 16-bit-wide silo. REQ1 is initially set to provide RPB1 TO SILO H, which loads BR (35:20) into the silo. After a short delay, the silo is again ready for an input and SILO IN RDY H asserts ADV REQ L, which increments the request counter. On the next pass, RPB2 TO SILO H is generated, which loads BR (19:04) into the silo.

If the RP11-C is in the 10/15 mode, the request counter will be advanced for a third load, during which BR (03:00) is loaded into the silo. This is only for 36-bit word transfers. In the 11 mode, only data bits BR (35:20) and BR (19:04) are loaded into the silo, and the serial checksum in BR (03:00) is not sent out on the Unibus.

4.5.4 Silo Output to Unibus (DATO)

The logic flow for this part of the Read Data operation is almost independent of the Read Data operations previously described. Note that there is no direct connector between these parts of the Read Data flow chart. As long as no errors are detected, and there is no bus word count overflow, the Silo Memory will initiate an NPR (non-processor request) for a Unibus DATO transfer whenever SILO OUT RDY H indicates the silo is ready to output.

Each time the RP11-C becomes bus master, the logic proceeds to output a word to memory. The Unibus control timing is shown in Figure 4-10. The Unibus control sequence for the Read Data DATO operation is as follows:

1. With READ C H asserted, the Silo Memory asserts SILO OUT RDY H when a word is ready to be output on the Unibus. This sets NP REQ.
2. NP REQ (1) H causes the M7821 Interrupt Control module to issue an NPR Unibus request.
3. When the processor priority arbitration logic recognizes the NPR, it responds with BUS NPG IN H, which the M7821 acknowledges with BUS SACK L.
4. Having thus fulfilled all requirements to become bus master, the M7821 asserts BUS BBSY L and RP MASTER L when any current bus master drops BUS BBSY L.
5. RP MASTER L is applied to the M796 Unibus Master Control module. ADDRESS TO BUS, BUS C1, and BUS C0 are asserted. With READ C H asserted, BUS C1 L is high and a DATO Unibus cycle is specified.
6. NP REQ (1) H and READ C H have enabled the D input to the SHIFT OUT flip-flop. Under DATO conditions, RP MASTER L asserts DATA TO BUS, which clocks the SHIFT OUT flip-flop.
7. BUS MSYN L is asserted about 200-ns later. The RP11-C then waits for the addressed memory to respond.
8. When the memory responds with BUS SSYN L, BUS MSYN L is negated. After about 100-ns delay, ADDRESS TO BUS, DATA TO BUS, BUS C1, and BUS C0 are dropped.
9. An END CYCLE H pulse is provided by the M796 module. The complement, END CYCLE L, is used to clear the NP REQ and SHIFT OUT flip-flops.
10. The next Unibus DATO transaction will not be initiated until SILO OUT RDY H is again asserted, indicating that the Silo Memory is ready to output another data word.

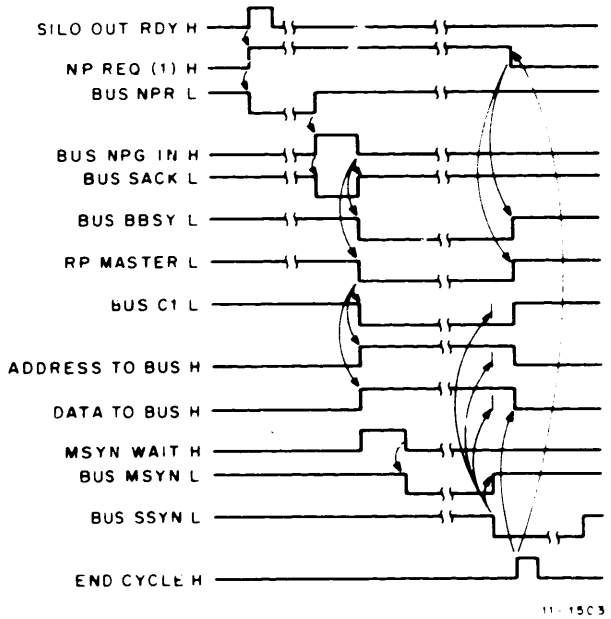


Figure 4-10 Unibus Control Timing, DATO (Read)

4.5.5 Read Data Done

During the Read Data operation, two word-count conditions must be satisfied before the Read Data operation is done. These are SILO WCOF and BUS WCOF. The silo word counter and the RPWC are both loaded with the 2's complement of the word count prior to initiating the Read function. The silo word counter is incremented as each word is loaded into the silo. When it overflows, no more words are transferred from the SR to the BR. The RPWC is incremented by each Unibus transfer to memory. When both word counters have overflowed, the Read Data operation is done. The Done Interrupt sequence is described in Paragraph 4.8.1.

4.6 WRITE DATA

A detailed flow chart of the Write Data operation is shown in Figure 4-11. As indicated in the operational flow chart (Figure 4-1), the Write Data flow is entered immediately upon completion of the Search operation (for Write functions, codes 1 and 5). The Write Data operation consists of four major parts, as shown on Figure 4-11. These are:

a. Loading the Silo Memory by Unibus DATI transfers (Paragraph 4.6.1).

b. Unloading the Silo Memory to the BR to form the disk word (Paragraph 4.6.2).

c. Switching from the VFO clock used to find the header to the crystal-controlled clock used to write the data (Paragraph 4.6.3).

d. Forming the 36-bit data word, plus parity, in the SR and serially shifting it out to the disk (Paragraph 4.6.4).

4.6.1 Unibus Input to Silo

The logic flow for this part of the Write Data operation is almost independent of the other parts of the Write Data flow chart. As soon as ERR SYNC2 is set during the Seek operation, the Silo Memory control logic will initiate an NPR for a Unibus DATI transfer. Each time the RP11-C becomes bus master, the logic proceeds to input a word from memory. The Unibus control timing is shown in Figure 4-12. The Unibus control sequence is as follows:

1. When the Silo Memory is ready for a word, SILO IN RDY sets the NP REQ flip-flop.

2. NP REQ (1) H causes the M7821 Interrupt Control module to issue an NPR Unibus request.

3. When the processor priority arbitration logic recognizes the request, it responds with BUS NPG IN H, which the M7821 acknowledges with BUS SACK L.

4. Having fulfilled all requirements to become bus master, the M7821 asserts BUS BBSY L and RP MASTER L when the Unibus is available.

5. RP MASTER L is applied to the M796 Unibus Master Control module. The Unibus address and control signals are gated to the bus.

6. After approximately 200 ns, BUS MSYN L is asserted and the RP11-C waits for a response from the memory that has been addressed.

7. When the memory responds with BUS SSYN L, the M796 produces a 200-ns DATA WAIT H pulse, which sets the SHIFT IN flip-flop on the trailing edge.

8. SHIFT IN (1) H asserts SILO SHIFT IN and the data word is shifted into the Silo Memory.

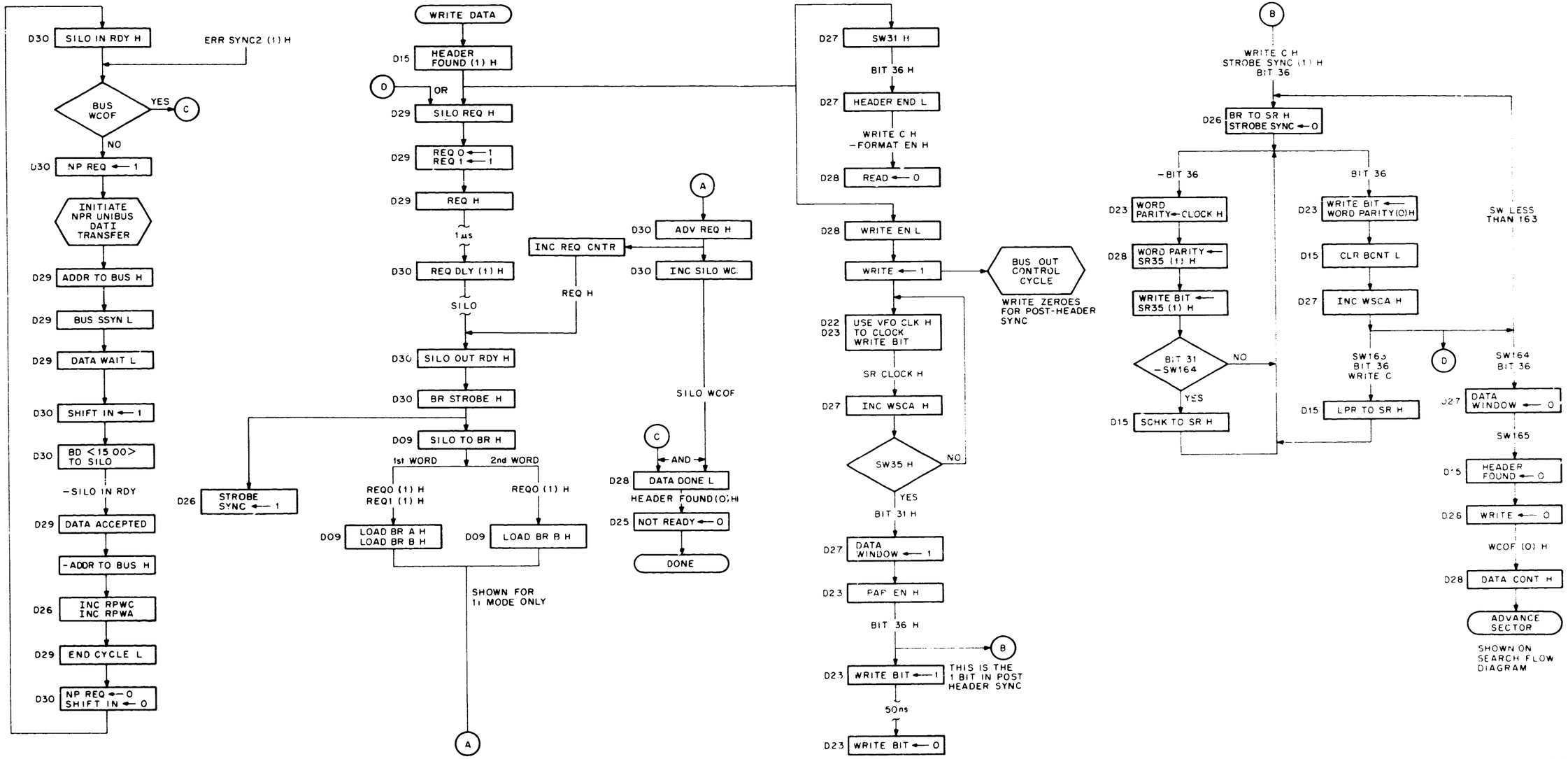


Figure 4-11 Write Data Operation, Detailed Flow Chart

9. Internal Silo Memory timing produces SILO IN RDY L. This signal is applied to the M796 as a DATA ACCEPTED signal. As a result, BUS MSYN L is dropped, and 100-ns later, ADRS TO BUS, BUS C1, and BUS C0 are dropped.

10. A 100-ns END CYCLE H pulse is produced by the M796. The complement, END CYCLE L, clears the NP REQ and SHIFT IN flip-flops.

11. The next Unibus DATI transaction will not be initiated until SILO IN RDY H is again asserted, and the Silo Memory is ready to accept another data word input.

NOTE

This same operation is performed for the Write Check function described in Paragraph 4.7.

Each time ADDR TO BUS H is asserted, the RPWC and RPBA are incremented. The Silo Memory control logic will continue to load the silo from memory as fast as NPRs are granted. The 64-word capacity of the Silo Memory provides sufficient buffering to prevent the RP11-C from experiencing overruns if NPR latency deteriorates as a result of heavy Unibus activity. This is accomplished as described in the following paragraphs.

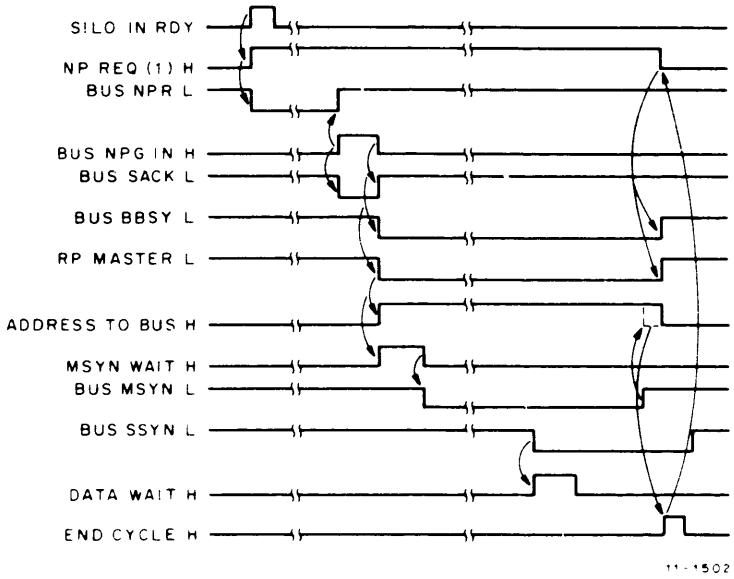


Figure 4-12 Unibus Control Timing, DATI (Write or Write Check)

4.6.2 Unloading the Silo to BR

Upon completion of a successful Search operation, HEADER FOUND (1) H asserts SILO REQ H. This presets the request counter and sends a delayed request to the silo. When the silo is ready to output, BR STROBE H strobes the word into both sections of the BR. SILO TO BR H is always asserted during Write or Write Check functions.

At the time the first word is strobed into both sections of the BR, ADV REQ L increments the request counter and the silo word count. By the time the silo is ready to output the second word, REQ1 is cleared and only the B section BR (19:04) is loaded.

4.6.2.1 PDP-11 Mode – In the PDP-11 mode, REQ2 never gets set and the C section of the BR [BR(03:00)]is never loaded from the silo. After the first two words are loaded into the BR, the request counter returns to the zero state. As a result, two 16-bit Unibus data words are sequentially loaded into BR (35:20) BR (19:04).

4.6.2.2 PDP-10/15 Mode – In this mode of operation, three 16-bit Unibus words are loaded into the BR on three successive transfers. REQ2 is set after the first word is strobed into the BR. REQ2 causes the appropriate bits of the third 16-bit word to be strobed into BR (03:00) to construct the full 36-bit data word in the BR.

4.6.3 Writing the Post-Header Sync

As soon as the header is found during a successful Search operation, READ is cleared and WRITE is set, as shown on the flow chart (Figure 4-11). This causes the crystal-controlled oscillator to be the source of VFO CLK H and SR CLOCK H. A BOC cycle is initiated to send the Write command to the selected RP03. WRITE remains set until the end of the sector.

The Bit Counter and WSC continue to increment from SW31 to SW35, and at bit 31 of SW35, DATA WINDOW is set. PAR EN H is asserted, so that at bit 36, WRITE BIT will be set to provide the 1-bit at the end of the post-header sync pattern.

4.6.4 Writing the 37-Bit Word

Path B of the Write Data flow chart shows how the 37-bit word to be written on the disk is formed in the SR. The contents of the BR are set in the SR at bit 36.

NOTE
This is only true for a Write command.

After bit 36, the SR is shifted at the crystal-controlled clock rate. SR35 (1) H is clocked into WRITE BIT. Thus, the SR contents are serially shifted to become the WRITE DATA COAX data stream to the selected RP03.

4.6.4.1 SCHK TO SR – At bit 31, the contents of the 4-bit serial checksum counter are strobed into SR (35:32) and these bits enter the serial data stream as part of the 37-bit word. The serial checksum logic is described in Paragraph 4.9.

4.6.4.2 WORD PARITY – WORD PARITY is cleared at the beginning of each word. From bit 0 to bit 35, it is toggled by each 1-bit shifted out of the SR. This includes the serial checksum bits. Thus, after an even-number of 1s has been shifted out of the SR, WORD PARITY will be clear at bit 36. If the SR contained an odd-number of 1s, WORD PARITY will be set at bit 36. The complement, WORD PARITY (0) H, is written onto the disk at bit 36 to provide odd-parity for the preceeding 36 data bits that were written.

4.6.4.3 Writing the LPR Word – Paragraph 4.10 describes how the longitudinal parity word is formed in the LPR. The B path of the logic flow chart continues to write serial data words through SW163. At bit 36 of SW163, LPR TO SR H is asserted during a Write operation. The LPR word for the complete sector is then written as the last word in the sector. Parity is generated for the LPR in the same way as described for the data (Paragraph 4.6.4.2).

4.6.5 Write Data Done

After the LPR is written, DATA WINDOW, HEADER FOUND, and WRITE are cleared as shown on the flow chart (Figure 4-11). If there is no word count overflow, DATA CONT H initiates the Search operation to prepare for the next sector to be written. Two word-count conditions must be satisfied before the Write Data operation is done: SILO WCOF and BUS WCOF. As soon as the RPWC overflows, (BUS WCOF), no further Unibus DATI transfers are initiated. The remaining words in the Silo Memory continue to be loaded into the BR until SILO WCOF occurs. The last data word is written onto the disk. Any remaining data words in the sector are written as 0s. DATA DONE L is asserted by WCOF H and the Write Data operation is Done.

4.7 WRITE CHECK

The Write Check function checks each word written on the disk against each corresponding word stored in memory. It is normally executed after a Write operation to be sure that all the data has been written correctly. A detailed flow chart of the Write Check operation is shown in Figure 4-13. Basically, it consists of the following three major parts:

1. Loading the Silo Memory from the Unibus and unloading the silo to the BR (Paragraph 4.7.1).

2. Reading the data from the disk into the SR (Paragraph 4.7.2).

3. Comparing the data in the BR and SR to determine if there are any errors (Paragraph 4.7.3).

The Write Check operation is entered directly from the successful Search operation. There is no change over to the crystal-controlled clock between HEADER WINDOW and DATA WINDOW. The VFO-controlled clock used during the Search operation is used to continue reading in sector words.

4.7.1 Reading From Memory

This part of the Write Check operation is almost identical to the Write Data operation, up to the point of loading the SR from the BR. Only WRITE C will assert BR TO SR H. Therefore, in the Write Check operation, BR TO SR H is inhibited.

The Silo Memory control logic starts initiating NPRs as soon as RR SYNC2 is set. The Write Check Data part of the operation is exactly as described in Paragraphs 4.6.1 and 4.6.2.

NOTE

SILO REQ H is only asserted by HEADER FOUND for the first word loaded into the BR. After that, SILO REQ H is a function of DATA XFER EN H, which is controlled by bit 36. Thus, DATA XFER EN H is the signal that synchronizes the BR contents with the SR contents, throughout the Write Check operation.

4.7.2 Reading From Disk

This part of the Write Check operation is very similar to the Read Data operation, up to the point of loading the BR from the SR. SR TO BR H can only be asserted by READ C; it is therefore inhibited during the Write Check operation.

After the header is found, the Bit Counter and WSC continue to increment up to SW35, bit 31, which sets DATA WINDOW. The post-header sync bit and the data are read as described in Paragraphs 4.5.1 and 4.5.2. DATA WINDOW allows bit 36 to assert DATA XFER EN L, which provides GOOD STUFF 2 H. This signal is used to assert SILO REQ H which synchronizes loading the BR and loading the SR.

4.7.3 Comparing BR With SR

This is done at bit 36 of each sector word, as indicated on the flow chart (Figure 4-13). As long as the contents of both registers compare bit for bit, the Write Check operation continues through the sector. If the Write Check word count specifies that more than one sector of data is to be checked, the Search operation is entered at the end of each sector. If the BR and SR do not compare, the Write Check Error (WCE) flag is set and the Write Check operation is terminated as shown in Figure 4-13.

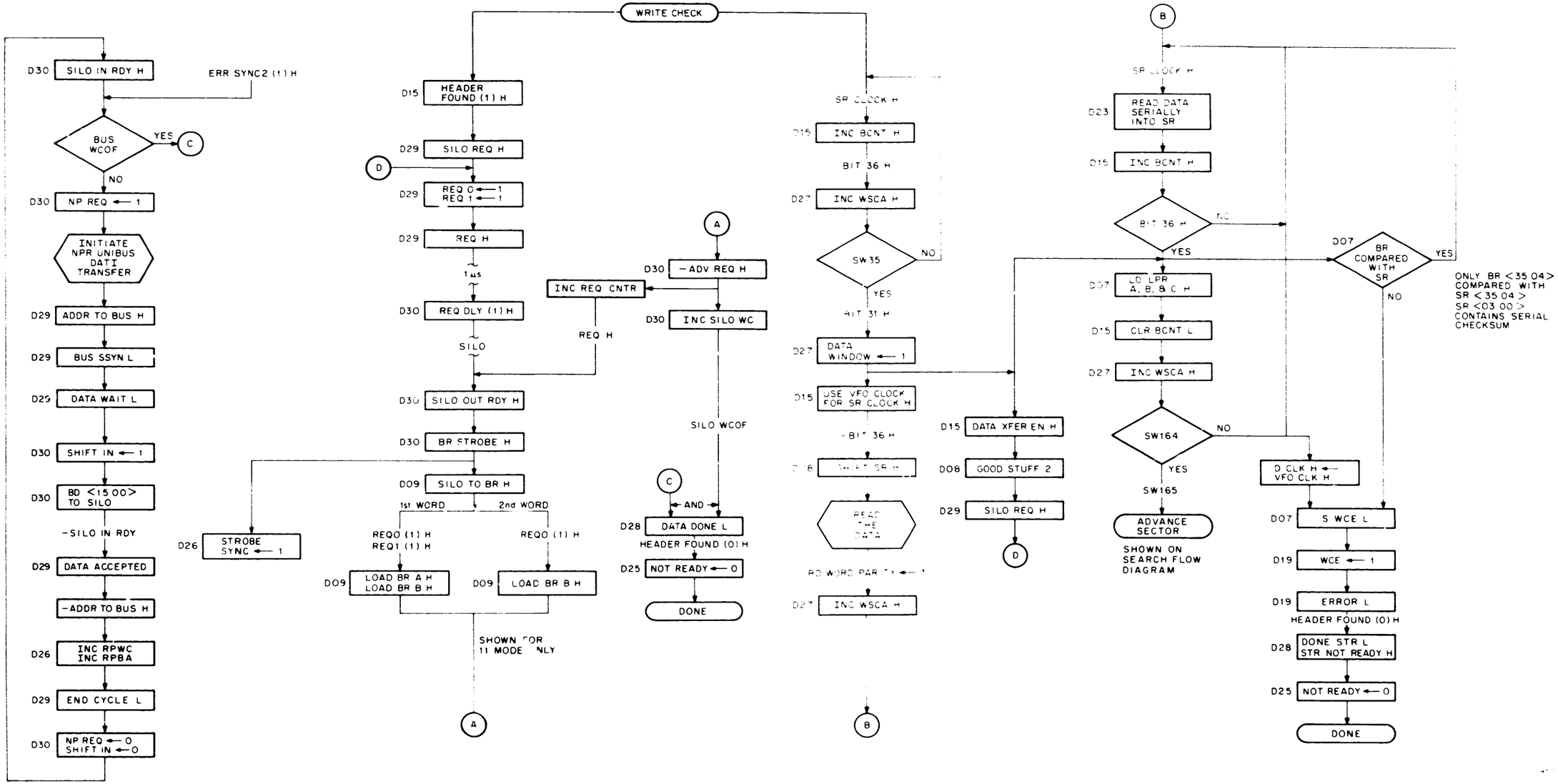


Figure 4-13 Write Check Operation, Detailed Flow Chart

4.8 INTERRUPT CONTROL

4.8.1 Done Interrupt

To enable the Done Interrupt logic, the Interrupt on Done Enable (IDE) bit in the RPCS must be set under program control. Whenever any operation is successfully completed, or if a condition that invalidates that operation is detected, the program wants to be interrupted. All the above conditions are ORed to produce STR NOT READY H. STR NOT READY H clears the NOT READY flip-flop (drawing D25). NOT READY (0) H and IDE (1) H are applied to the M7821 Interrupt Control module to assert BUS BR 5 L.

The processor priority arbitration logic responds with BUS BG 5 L to grant the interrupt request. The M7821 logic asserts the MASTER B L output, which is connected to the START INTR A, B L inputs. As a result, BUS INTR L is asserted and a jumper-selected vector address is asserted on bus data lines BUS D (07:00)

NOTE

Usually for single RP11-C applications, the M7821 is jumpered to specify vector location 254 [BUS D (07:00) = 10101100].

The processor receives the BUS INTR L signal, waits 75 ns for deskew to ensure that all bits of the interrupt vector address are available, and asserts BUS SSYN L when the data is read in. When BUS SSYN L is received by the M7821 Interrupt Control module, it asserts the INT DONE H output, which is fed back to the MASTER CLEAR B input to clear the interrupt control logic. When BUS INTR L is cleared, the processor clears BUS SSYN L and enters the interrupt service sequence to store the current contents of the PC and PS registers, and replace them with the contents of the locations specified by the interrupt vector address.

4.8.2 Attention Interrupt

The Attention Interrupt logic is enabled by setting the Attention Interrupt Enable (AIE) bit in the RPCS under program control. The logic is implemented by the second M7821 Interrupt Control module shown on drawing D29.

When a selected RP03 Disk Pack Drive successfully completes a Seek, it notifies the RP11-C by raising the ATTENTION signal. The input sets the appropriate flip-flop in the attention register, drawing D18. The ATTN (07:00) (1) L outputs are ORed to assert ATTN H. ATTN H and ATTN ENABLE (1) H initiate the bus interrupt sequence. The remainder of the Attention Interrupt sequence is identical to the Done Interrupt sequence, described in Paragraph 4.8.1. The ATTN bits can be cleared individually, and ATTN H may be reasserted by another ATTN flip-flop. ATTN ENABLE is cleared at the completion of each interrupt.

4.9 SERIAL CHECKSUM LOGIC

The purpose of the serial checksum logic, shown on drawing D16, is to count (modulo 16) the number of 1-bits in each 32-bit data word that is written onto the disk. That serial checksum is written onto the disk as part of the 37-bit serial data word. When each data word is read from the disk, the serial checksum logic again counts the number of 1-bits in the data word and compares the resultant serial checksum with the serial checksum written at the end of the disk word. If the written and read serial checksums do not compare, a serial checksum error is flagged.

4.9.1 Writing the Serial Checksum

Refer to drawing D16. The serial checksum counter is cleared by INC WSCA L at the beginning of each word. During the first 32 data bits, BCNT5 (0) H is asserted. During the Write, WRITE (1) H is high and each 1-bit in the data word, SR35 (1) L, increments the serial checksum counter by asserting INC SCK H.

When the last data bit has been shifted, BIT 31 H asserts SCHK TO SR H, as shown on drawing D15. This signal inhibits the SHIFT SR H and parallel shifts serial checksum counter bits SCK (03:00) into SR (35:32). At bit 32, SHIFT SR H is restored and the serial checksum count is shifted out as part of the 37-bit disk word that is written.

4.9.2 Reading the Serial Checksum

During the Read operation, the serial checksum counter is again cleared at the beginning of each word. Under these conditions READ (1) L and READ BIT (1) L are used to provide the INC SCK H pulses that increment the serial checksum counter. The BCNT5 (0) H signal allows only the 32 data bits to be tested. At bit 36, all the data and the four serial checksum bits have been shifted into the SR from the disk. SHIFT SR H is inhibited by bit 36, as shown on drawing D08. The contents of the serial checksum counter are then compared with the serial checksum bits in the SR. If they do not compare, S SCK ERR L is asserted to set the SCK ERR bit in the error register, shown on drawing D19.

4.10 LONGITUDINAL PARITY

The longitudinal parity word for each sector is formed in the LPR by exclusive-ORing data word bits with the LPR contents. The detailed flow chart shown in Figure 4-14 shows how the LPR is written, how it is read, and how the longitudinal parity of every sector is checked.

4.10.1 Writing the LPR

The LPR is loaded from the SR at bit 36, when the SR is not shifting. SR (35:04) contain data and SR (03:00) contain the serial checksum. At the end of SW163, the LPR contains the exclusive-OR of all the data words. At bit 36 of SW163, the LPR is gated to the SR to become SW164.

NOTE

The SR receives the complement of the LPR, because the total number of 1s, including the LPR, must be odd.

4.10.2 Checking the LPR

During the Read Data operation, as each data word is read from the SR to the BR, it is also exclusive-ORed into the LPR. After SW163, the LPR will contain the exclusive-OR of all the data words that have been read. At the end of SW164, the SR contains the complement of the LPR word formed when the sector was written (Paragraph 4.10.1). This complement, when exclusive-ORed with the current LPR contents, should produce all 1s in the LPR if the sector is read exactly as written.

If the LPR contents are not all 1s at the end of the sector, the Longitudinal Parity Error (LPE) flag is set. The logic enters path A of the flow chart to set the LPE flag and terminate the Read Data operation.

4.11 READ DATA SEPARATION (VFO)

The recording technique used in the RP11-C (Double Frequency NRZ) is dictated by the characteristics of the recording material used on the RP02P Disk Pack. The fact that it is a disk, and not a drum, renders the device speed-frequency sensitive, a sensitivity factor that becomes more critical as the recording head nears the center of the disk. (A drum is speed-frequency sensitive, but this sensitivity is a constant since the diameter remains constant.) Add to this sensitivity the fact that any magnetizable material is an imperfect medium, at best, due to its reluctance to change; the need for the technique used for data separation becomes apparent.

The disk pack system is susceptible to a phenomenon termed "pulse crowding." When a series of 1s are recorded on a track, they assume positions equally spaced from one another. If, however, a 1-bit is removed, the adjacent bits tend to fill the vacant cell. This effect is similar to lining up a series of bar magnets end-to-end. When a bar magnet located in the middle of the chain is removed, the adjacent magnets move in to fill the gap. Since the resultant locations can shift in either direction, a means must be provided to read through a precisely timed window so that the original timing may be recovered.

The RP11-C uses a double-frequency, non-return-to-zero (NRZ) recording technique. A 5-MHz clock signal is divided to produce two 2.5-MHz signals with a 180° phase relationship (see VFO Control drawing D22). When writing, the leading 2.5 MHz continuously records 1-bits on the disk surface, while the trailing signal samples the data to produce data bits. If the data to be written is continuous 0s, a 2.5-MHz signal is recorded on the disk surface. If the data to be written is continous 1s, then a 5.0-MHz signal is recorded. Therefore, for any given data cell, the recorded frequency is either 5 MHz for a 1 data bit, or 2.5 MHz for a 0 data bit.

To recover data recorded in this manner, the 0s rate frequency component must be removed; this is done by using a phase-locked, variable-frequency oscillator (VFO) that is similar to a sample-and-hold circuit. The VFO is capable of sampling the 0s rate pattern in the preamble of each record, phase-locking on this pattern, and then maintaining phase through the record, making only minor corrections with the use of the 0s rate component of each data cell. The VFO then removes the 0s rate component with which it is familiar, leaving only the recovered data.

The 0s rate component (2.5 MHz) removed from the Read signal is also used. This signal and its Write counterpart are the main sources of timing in the RP11-C. Because the RP03 has no clock track, this system provides self-clocking (Figure 4-15).

The RP11-C VFO Control is shown in Figure 4-16 and drawing D22. The circuit consists of a 5-MHz source, an M420 module, a frequency divider flip-flop, and associated delays and gates. The RP02P Disk Pack has no clock track of its own; therefore, a means must be provided to record the timing on the disk with the data to be stored at the moment that data is recorded. In this way, a firm relationship between clock and data can be established at the write time, so that at read time, that relationship can be reconstructed regardless of small differences in drive speed over a period of time.

To accomplish this recording, a format has been set up to provide a synchronization period at the beginning of each sector (Figure 4-17) consisting of no data (continuous 0s). As shown in Figure 4-17(a), this signal consists of a string of pulses recorded on the disk, at a frequency of 2.5 MHz, representing the 0s rate component. This signal determines the 1s rate component and establishes the basic timing for information to be written on the disk or read from the disk, independent of drive-speed differentials between write time and read time. These 2.5-MHz pulses are recorded at the beginning of each data cell throughout the format, thereby maintaining the basic timing across the entire sector.

During Write, the VFO is switched off and the synchronization area is generated in the RP11-C from a self-contained crystal-controlled 5-MHz source; the output of this source is divided to produce two 2.5-MHz pulse trains, each of which bears a 180° phase relationship with each other. The leading 2.5-MHz signal produces the sync bits at the beginning of each bit cell time. The trailing 2.5-MHz signal establishes the middle of that bit cell.

The recording system is termed "double-frequency non-return-to-zero (NRZ)"; i.e., the state of magnetization of the disk material does not change except when excited with a 1-bit, and then in the opposite polarity. The recording head is, in reality, a gap that constitutes discrete space, the actual shape of magnetization change will not be a square waveform, but rather some sinusoid that is an instantaneous function of field strength, field rate-of-change, gap width, surface reluctance, and drive speed (Figure 4-17(b)). The waveform is a constant frequency for an all 0s data pattern, but when 1s are introduced (c), the sync bits tend to be displaced by the data bits. It is this displacement that increases with pulse density and is described as pulse crowding.

Because both data and sync bits can shift when they are written and when they are read, the timing for Read must be based on a variable device that can be changed within the limits of expectable variance. The functions of the VFO are:

a. To sample the incoming clock bits received from the disk.

b. To establish an internal clock gate based upon the average leading edge of those clock bits.

c. Set up a reading window during which the condition of data is sampled, since the data variance will be relatively the same as clock variance.

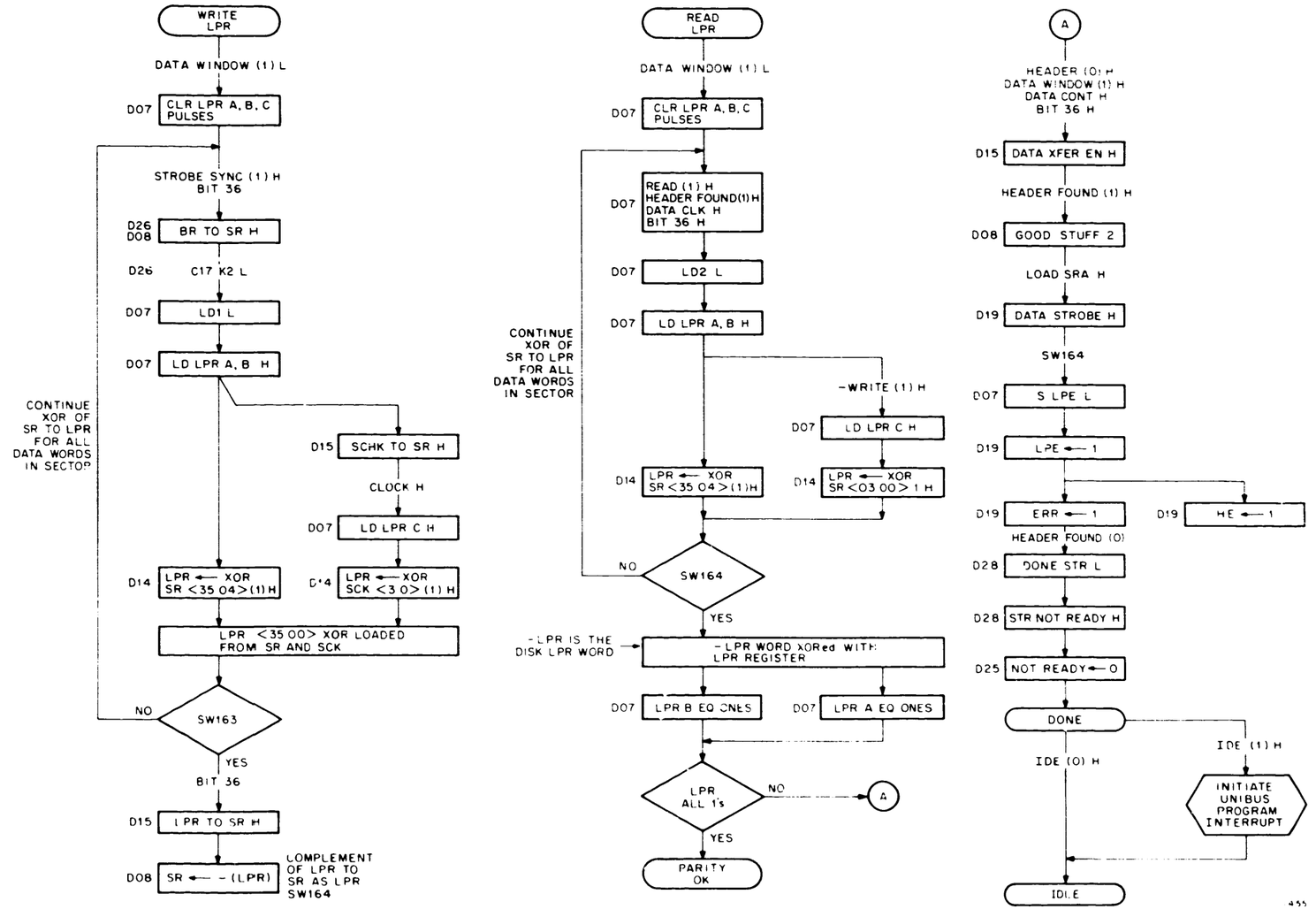


Figure 4-14 Longitudinal Parity, Detailed Flow Chart

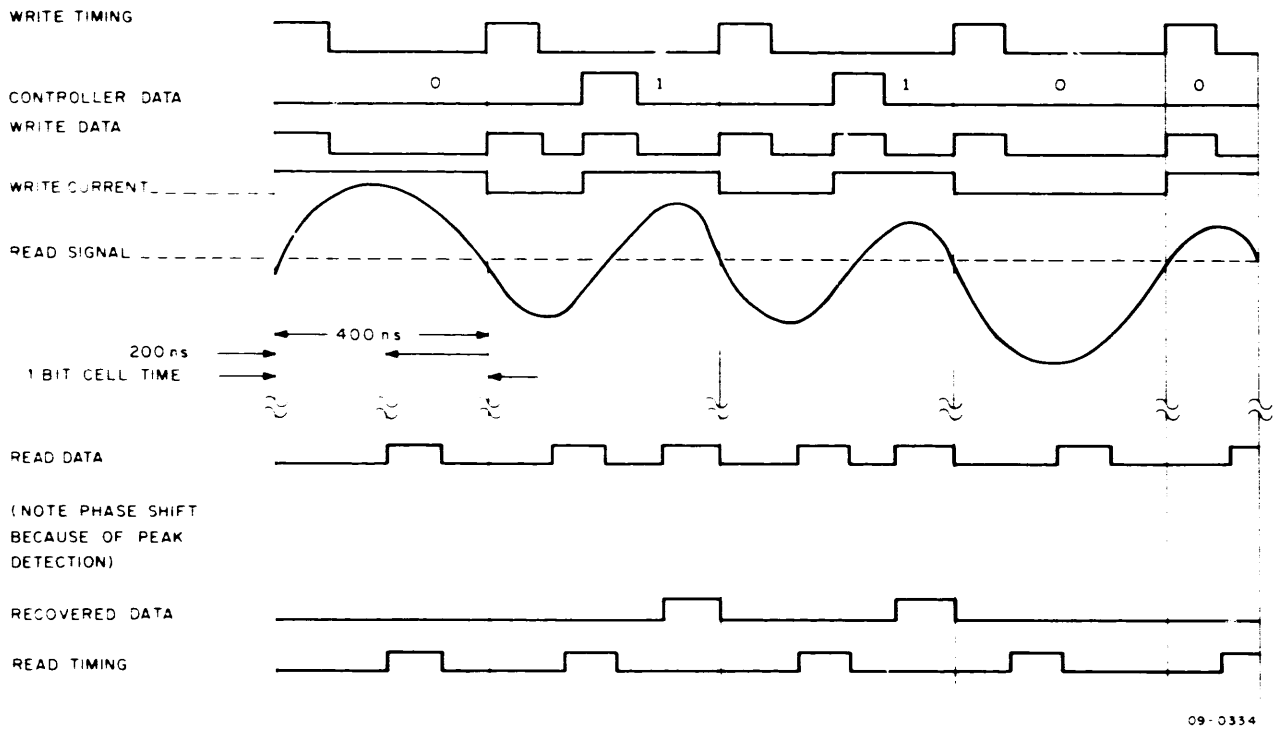


Figure 4-15 Disk Pack System Read/Write Timing Waveforms

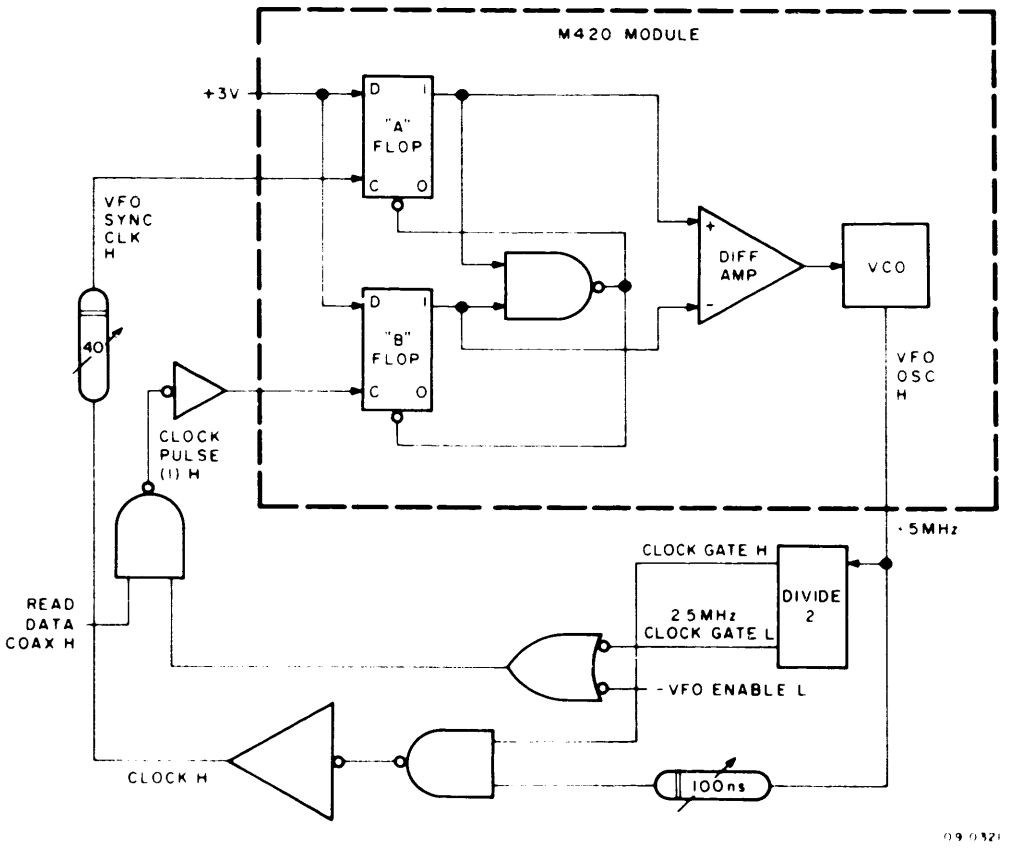


Figure 4-16 RP11-C VFO Control, Block Diagram

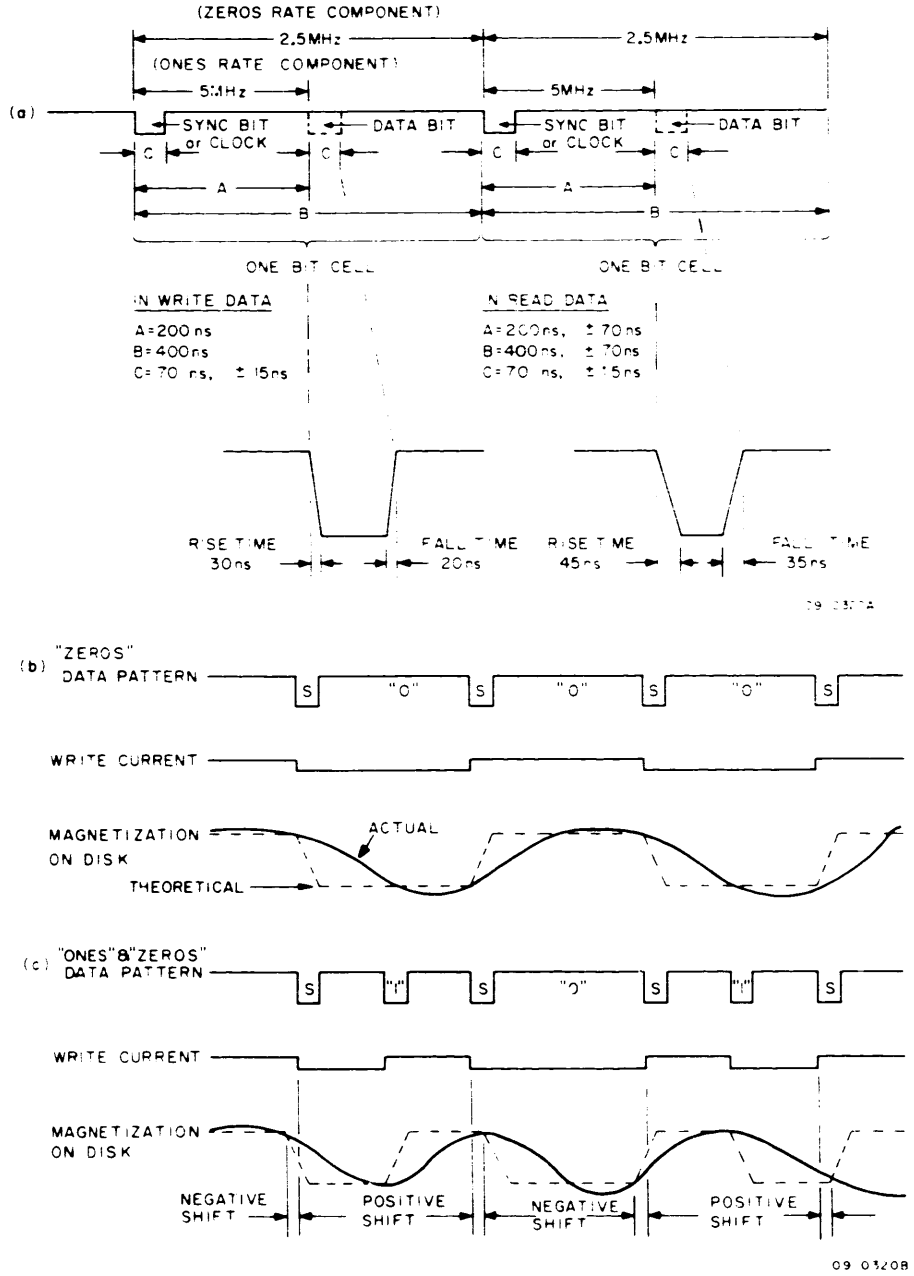


Figure 4-17 RP03 Recording Characteristics

The heart of the VFO Control is the M420 module, which is shown within the dashed lines in Figure 4-16. Basically, the module contains two D-type flip-flops with their data inputs tied high; a clearing AND gate tied to the 1-side of both flip-flops; a differential amplifier, whose plus input looks at the 1-side of one flip-flop and whose minus input looks at the 1-side of the other flip-flop; and a voltage-controlled oscillator, the output frequency of which is controlled by the voltage output of the differential amplifier. As configured, the circuit will reproduce a recurring input for a period of time after that input has been removed.

There are two inputs to the M420 (Figure 4-16 and drawing D22). The generated clock pulse (VFO SYNC CLK H) from the VFO, which runs at approximately 2.5 MHz, sets the "A" flip-flop; the separated clock pulse [CLK PULSE (1) H] from READ DATA COAX H sets the "B" flip-flop. Theoretically, when both flip-flops are set, both are cleared. Figure 4-18 is a timing diagram of this operation. Assume that the frequency of clocks from the disk [CLK PULSE (1) H] is slightly higher than VFO SYNC CLK H; the "B" flip-flop will be set longer than the "A" flip-flop and the width of its 1 state will lengthen as it sets earlier and earlier before being cleared each time the "A" flip-flop sets. In Figure 4-18(b), the opposite is true when the incoming clock pulse frequency [CLK PULSE (1) H] is lower than VFO SYNC CLK H. In this case, the "A" flip-flop is set longer and longer as it sets earlier in the cycle. In both cases, the "A" flip-flop reaches a point where it lines up with the "B" flip-flop; at this point the cycle starts again. The up time of the "A" or "B" flip-flops will lengthen at some sinusoidal rate equal to the difference in frequency between CLK PULSE (1) H and VFO SYNC CLOCK H. The output width of the flip-flop whose input is lowest in frequency will be very small (close to zero); the output width of the flip-flop whose input is highest in frequency will be finite. As such, the "A" and "B" flip-flops function together as a phase detector that feeds the differential amplifier with an error voltage on the higher frequency input, whether it be "A" or "B", that is proportional to the frequency of mismatch.

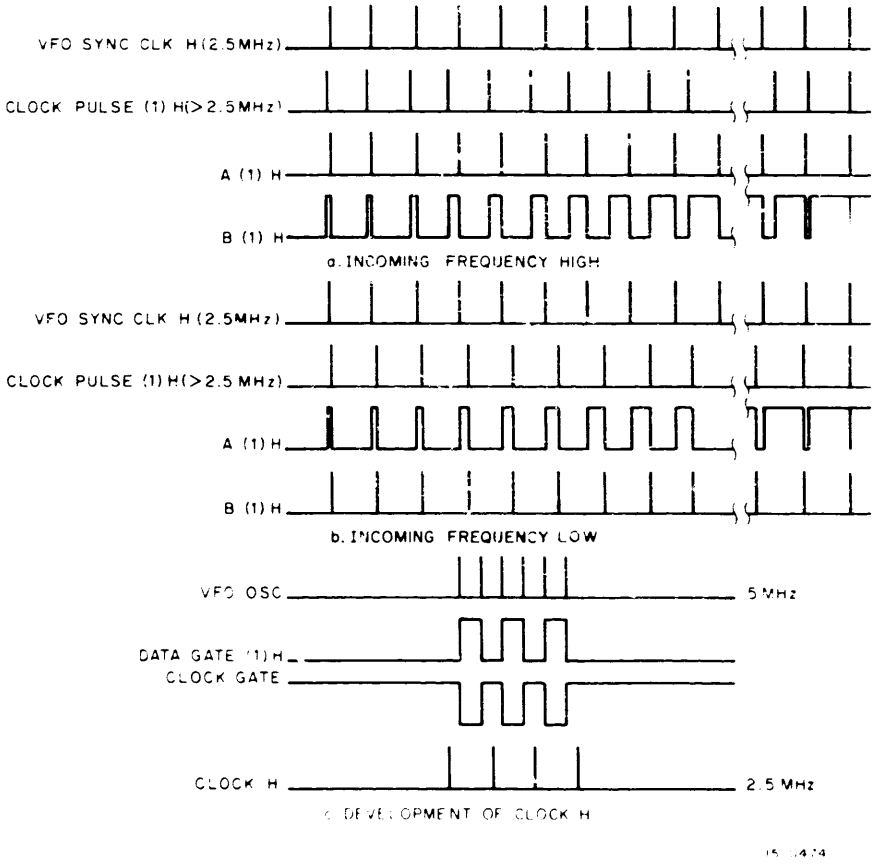


Figure 4-18 VFO Timing Waveforms

The M420 Differential Amplifier takes the difference of these two flip-flops, integrates that difference, and produces a plus or minus error voltage to the VFO that causes it to increase or decrease its frequency to match that which it received from the disk. At this point, an output from the M420 module is seen; it is called VFO OSC H. This output is approximately 5 MHz and is gated by READ (1) H to produce DATA GATE CLOCK H, which is then tied to the DATA GATE flip-flop. The flip-flop functions to divide the output by 2, yielding two 2.5-MHz signals that are 180° out of phase with each other. The 1 state of the flip-flop is designated DATA GATE; the 0 state serves as the

CLOCK GATE. The 5-MHz signal (DATA GATE CLOCK H) is also delayed approximately 100 ns to produce VFO CLK H which is ANDed with CLOCK GATE H, then inverted, to generate CLOCK H (Figure 4-18(c)). CLOCK H occurs at a 2.5-MHz rate and falls in the middle of CLOCK GATE. Because of logic delays and the variability of circuit delays, the 100-ns delay is adjustable so that the leading edge of CLOCK H can be placed exactly in the middle of its gate. CLOCK H is further delayed approximately 40 ns to produce VFO SYNC CLOCK H which, in turn, is fed directly into the input of the M420 closing the loop.

During Read, the 1109 sync bits of the preamble are fed to the VFO via READ DATA COAX H for approximately 350 to 400 μs. This is a sufficient sample to force the VFO to reproduce its input so that it can continue as a phase-locked loop through the remainder of the disk sector. During this synchronization period, –PAR EN L is low; this allows everything on the READ DATA COAX to enter the M420. Presumably this period in the format contains no data, but rather clock pulses which are then used to synchronize the VFO. Once the VFO is synchronized, –PAR EN L goes high and the circuit depends on DATA GATE (0) L inverted (equal to CLOCK GATE H) to gate the READ DATA COAX into the VFO. Because of the delays discussed, this occurs at the average of all clock pulses received from the disk; the VFO has essentially separated the clock pulses from the READ DATA COAX [CLOCK PULSE (1) H]. In Figure 4-16, CLOCK PULSE (1) H is shown as the output of an AND gate; this is a functional equivalent to actual hardware as shown in drawing D22. In reality, this is the CLOCK PULSE flip-flop whose data input is the OR of either DATA GATE (0) L or –PAR EN L, and is clocked by READ DATA COAX H. When CLOCK PULSE sets, it clears itself, producing a pulsed input to the M420. In operation, the VFO operates similarly to a closed-loop AFC circuit. Once it is synchronized, the VFO locks in and remains in sync.

The 40-ns delay forces the clock pulses from READ DATA COAX to line up in phase with LOAD SR A. Since READ DATA COAX must go through the CLOCK PULSE flip-flop before entering the M420, and since the CLOCK PULSE flip-flop can have a logical delay of between 0 and 50 ns, this variable delay adjusts for the difference and eliminates constant phase errors.

Relating the simplified diagram shown in Figure 4-3 to the logic schematic in drawing RP11-0-22, the output of the M420 module is labeled VFO OSC H. This signal is sent to an M121 AND/NOR Gate module where a logic decision is made as to whether or not the controller is in the Read state [READ (1) H or READ (0) H]. If it is not in the Read state, the VFO is turned off (allowed to go into saturation) and the crystal clock is used as timing for the Write state. If it is in Read state, the output of the VFO is gated through the M121 to a pulse amplifier (PA). An output called GATED VFO OSC L will be seen at the PA. This signal is fed to an M311 Tap Delay module to input a coarse adjustment on the centering delay.

From the M311, the signal emerges as DATA GATE CLK H and is used to complement the DATA GATE flip-flop. It is further delayed through the M311, then through a 40-ns variable delay (M312), to yield VFO CLOCK H; from there it enters an M627 NAND Power Amplifier module where it is gated with CLOCK GATE H to produce CLOCK L.

NOTE

This is shown in Figure 4-3 as the output of VFO OSC H through a 100-ns delay and gated with CLOCK GATE. The output CLOCK L, asserted at another delay, generates LOAD SR A, the main timing pulse.

The signal CLOCK L is inverted to produce LOAD SR A and CLOCK H. Delayed by one variable 40-ns delay, CLOCK L yields VFO SYNC CLK H. This pulse is then fed back into the VFO, closing the loop.

The other input to the VFO is CLOCK PULSE (1) H from the CLOCK PULSE flip-flop. The CLOCK PULSE flip-flop can be set by any pulse on the READ DATA COAX during synchronization; after synchronization, it can be set by a pulse from READ DATA COAX, whenever DATA GATE (0) L is true [same as CLOCK GATE (1)]. When DATA GATE (0) is true, its output will indicate CLOCK GATE H, thereby separating clock pulses from data pulses on the READ DATA COAX.

During synchronization, PAR EN H at the input of the CLOCK PULSE flip-flop forces the D-input high until the VFO has synchronized. Under this condition, every pulse from READ DATA COAX will set CLOCK PULSE. Unless errors exist in the synchronization field, these are all clock pulses required for synchronization. Once the VFO is synchronized, PAR EN H goes high. Now CLOCK PULSE sets only when DATA GATE is on a 0 L and the clock pulses from the disk are separated.

4.12 WRITE FORMAT

The Write Format operation is an RP11-C function that writes the sector word format onto the complete RP02P Disk Pack. It is an absolutely essential operation that must be initially performed on each RP02P Disk Pack before that disk pack can be used in the disk pack system.

A detailed flow chart of the Write Format operation is shown in Figure 4-19. The operation consists of five major parts:

1. An initial Seek operation to position the read/write heads of the selected RP03 on which the RP02P Disk Pack is mounted (Paragraph 4.12.1).

2. A sector locating sequence (Paragraph 4.12.2).

3. The pre-header sync and header format sequence (Paragraph 4.12.3).

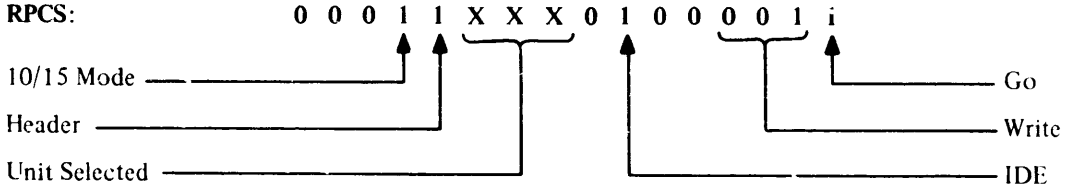
4. The post-header sync and data format sequence (Paragraph 4.12.4).

5. The end of sector sequence (Paragraph 4.12.5).

4.12.1 Initial Format Seek

Before initiating the Write Format operation, the RPCA and RPDA are loaded with the disk address to specify the start of formatting. For practical applications, RPCA and RPDA will be cleared, to format the complete disk pack. (For maintenance purposes, the duration of the Write Format operation can be abbreviated by loading RPCA and RPDA with a high address.) The FORMAT ENABLE switch is turned ON.

The Write Format operation is then initiated by a DATO to the RPCS that specifies the following:



The Format Seek sends the RP03 commands that position the read/write heads. The RP11-C checks for errors and then waits for the SU RDY L response from the RP03. It then begins the sector locating sequence.

4.12.2 Sector Locating Sequence

The first index pulse, SU IP L, sets INDEX SYNC. Following that, the next sector pulse, SU SP L, clears the Sector of Track (SOT) counter and clears INDEX SYNC so that future SU SP L pulses will increment the SOT.

The SOT is compared with the SAR. If RPDA was initially cleared, an immediate compare will result. If the SAR was loaded with a value other than 0, the SOT is incremented by succeeding sector pulses until it equals that value. When SOT equals SAR, SECTOR FOUND sets WRITE, and a ROC cycle is initiated to send the Write command to the RP03. WRITE remains set until the END OF SECTOR.

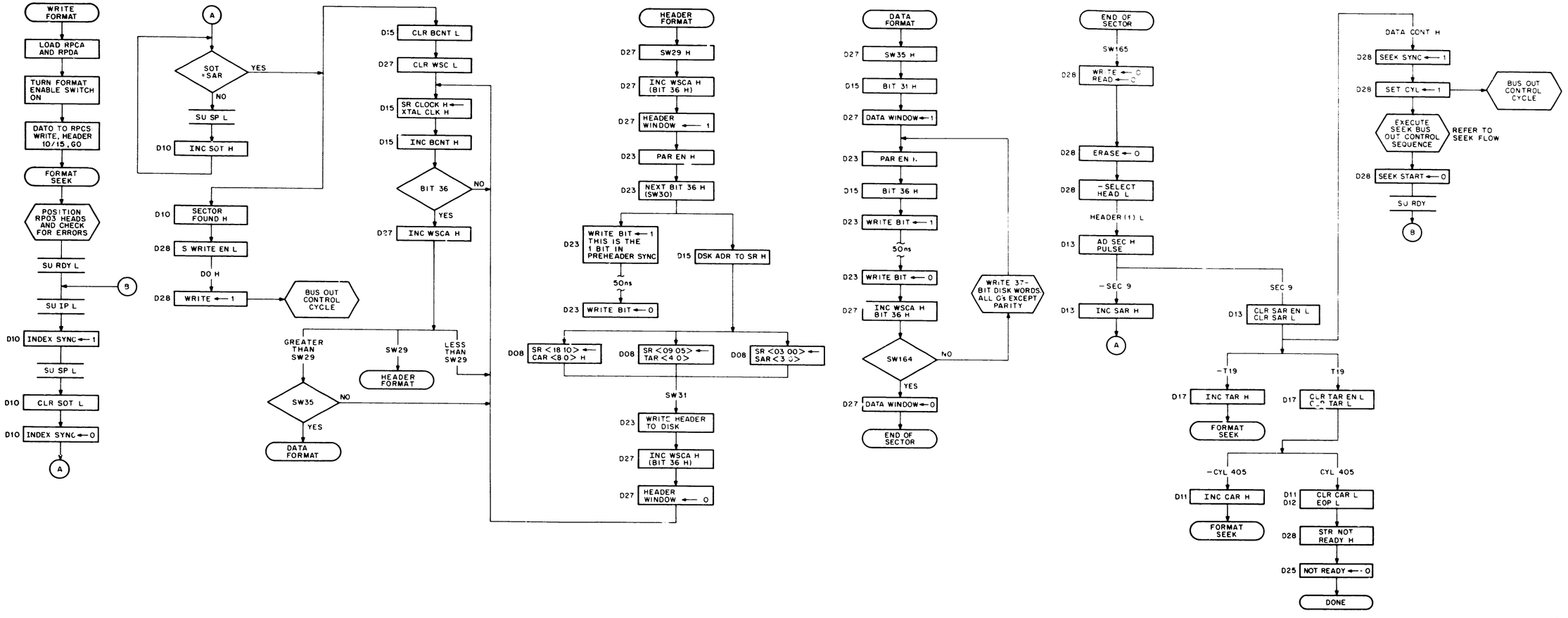


Figure 4-19 Write Format, Detailed Flow Chart

4.12.3 Pre-Header Sync and Header Format

When SOT equals SAR, the Bit Counter and WSC begin incrementing under control of the crystal clock. As the WSC increments up to SW29, all 0s will be written to the disk. At SW29, the HEADER FORMAT path of the flow chart is entered. The logic causes a 1 to be written as bit 36 of SW30. At this time, DSK ADR TO SR H is also asserted, and the contents of CAR, TAR, and SAR are strobed into the SR. During SW31, this header is written onto the disk. At the end of SW31, bit 36 clears HEADER WINDOW.

4.12.4 Post-Header Sync and Data Format

After HEADER WINDOW is cleared, the Bit Counter and WSC continue incrementing to SW35. The logic enters the DATA FORMAT path. At bit 31 of SW35, DATA WINDOW is set. As a result, PAR EN H causes WRITE BIT to set at bit 36. This writes the 1-bit at the end of post-header sync.

Each INC WSCA L clears WORD PARITY. As each all-0 data word is written during Write Format, WORD PARITY remains reset. At bit 36, WORD PARITY (0) H sets WRITE BIT. Thus, odd parity is generated and written on the disk as part of the Write Format operation. The WSC increments to SW164, clears DATA WINDOW, and enters the END OF SECTOR path of the flow chart.

4.12.5 End of Sector

At the end of each sector, SW165 produces the AD SEC H pulse, as shown in Figure 4-19. If the SAR is not at the highest legal address (sector 9), the SAR is incremented and the logic returns to the sector locating sequence (Paragraph 4.12.2). When the SAR is at sector 9, the SAR is cleared and the TAR is incremented. The new TAR must be sent to the RP03 by a BOC cycle so that the read/write heads can be re-positioned.

When the TAR is at track 19, the TAR is cleared and the CAR is incremented. The new CAR must also be sent to the RP03 by the BOC cycle, as part of re-positioning the read/write heads. Thus, when either the TAR or CAR is incremented, the flow returns to the FORMAT SEEK terminal and waits for the SU RDY L response and the SU IP L pulse. The Write Format operation continues as described in Paragraphs 4.12.2 through 4.12.5 until sector 9 of track 19 of cylinder 405 has been formatted. Then it is done, and, if the IDE bit was set in the RPCS, a program interrupt is initiated to notify the processor.

NOTE

Once the RPCS is loaded with the GO bit set, the Write Format operation is performed by the RP11-C and the selected RP03 without intervention by the processor.

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

RP11-C maintenance philosophy conforms to that of other DEC equipment; i.e., an optimum amount of preventive procedures performed on a routine schedule eliminates many costly equipment breakdowns, and forecasts impending failures long before they occur. When a specific item does fail, the design of the equipment is such that quick replacement of modular elements (Figures 5-1 through 5-3) restores the equipment to service in minimum time. A design objective of the RP11-C Disk Pack Controller is to provide a dependable and relatively maintenance-free assembly. This chapter contains both preventive and corrective maintenance procedures.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum unscheduled down time. These tasks include visual inspection, operational checks, cleaning, adjustment, and replacement of borderline, or partially defective parts.

Preventive maintenance scheduling is determined by the existing environmental and work-load conditions at the installation site. Under normal conditions, a schedule of preventive maintenance, consisting of inspection and cleaning every 600 hours of operation, or every four months, whichever occurs first, is recommended. Equipment operated in conditions of extreme temperature, humidity, dust and/or abnormally heavy work loads demand more frequent maintenance.

Preventive maintenance procedures for the RP03 Disk Pack Drive are not included in this manual. For those procedures, refer to the *ISS Disc Storage Drive Maintenance Manual* supplied with each RP03.

5.2.1 Test Equipment Required

Maintenance activities for the RP11-C require the standard test equipment and special materials listed in Table 5-1, plus standard hand tools, cleaners, test cables, and probes.

5.2.2 Mechanical Checks

Inspect the RP11-C controller periodically as follows:

1. Inspect the controller for completeness and general condition.

2. Clean the interior and exterior of the cabinet using a vacuum cleaner or clean cloth moistened in nonflammable solvent.

3. Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.

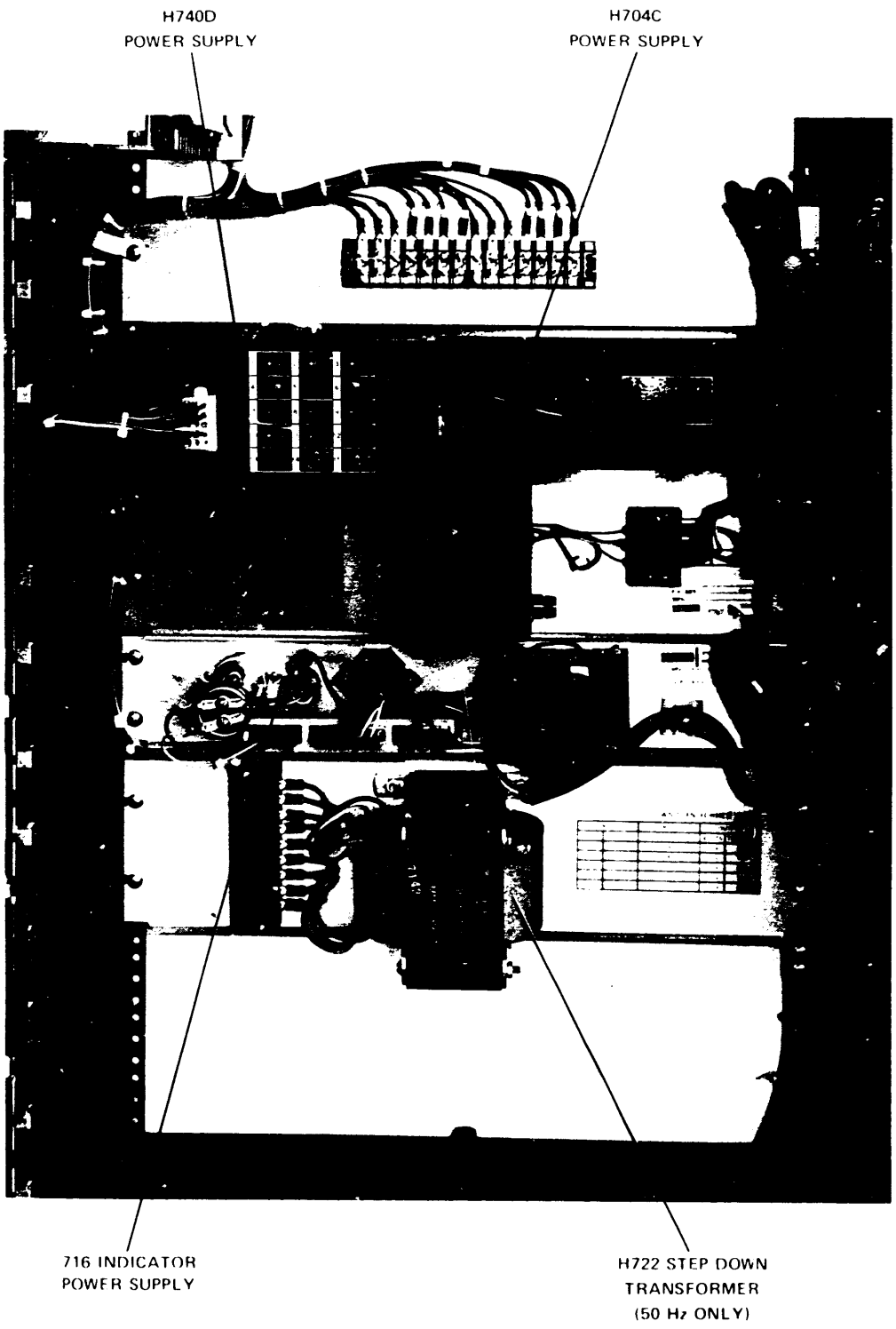


Figure 5-1 RP11-C Side View

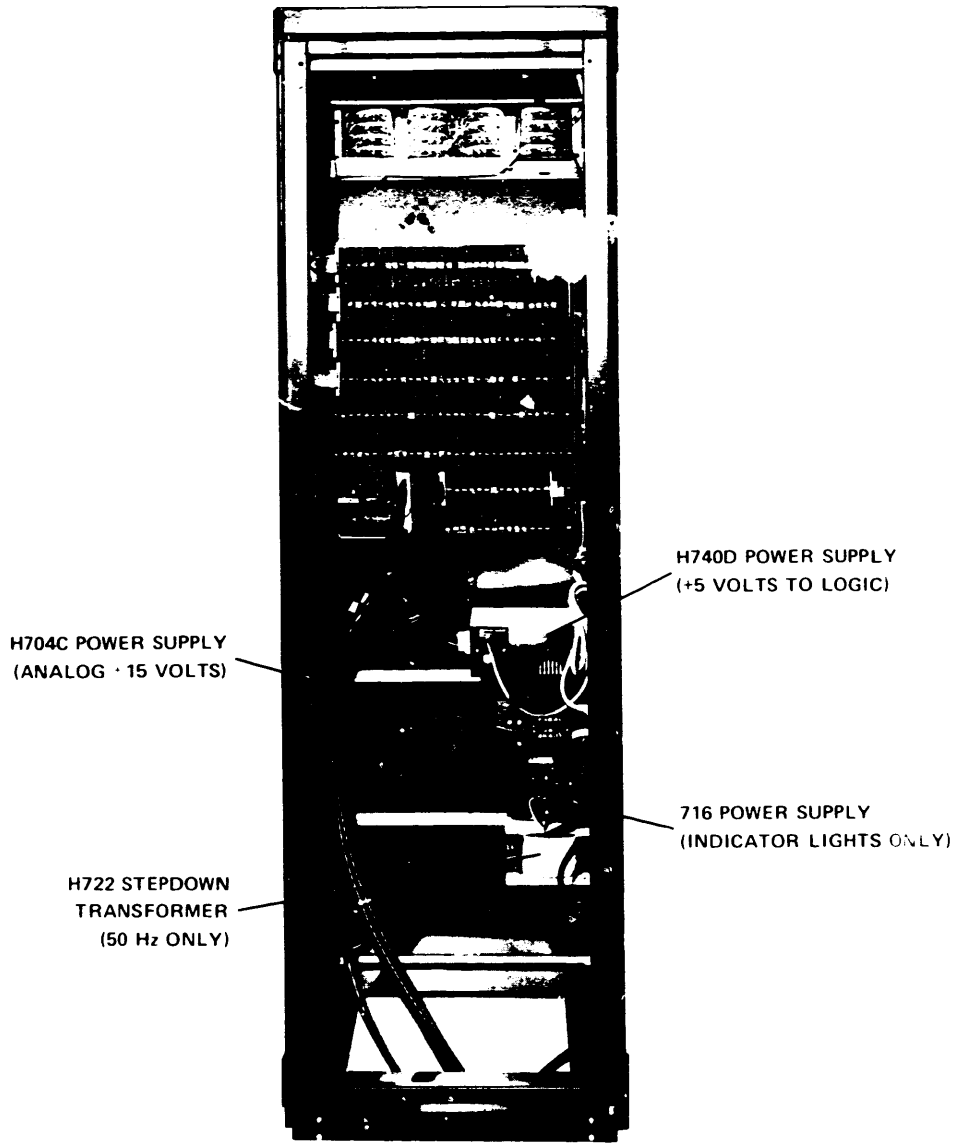


Figure 5-2 RP11-C Rear View

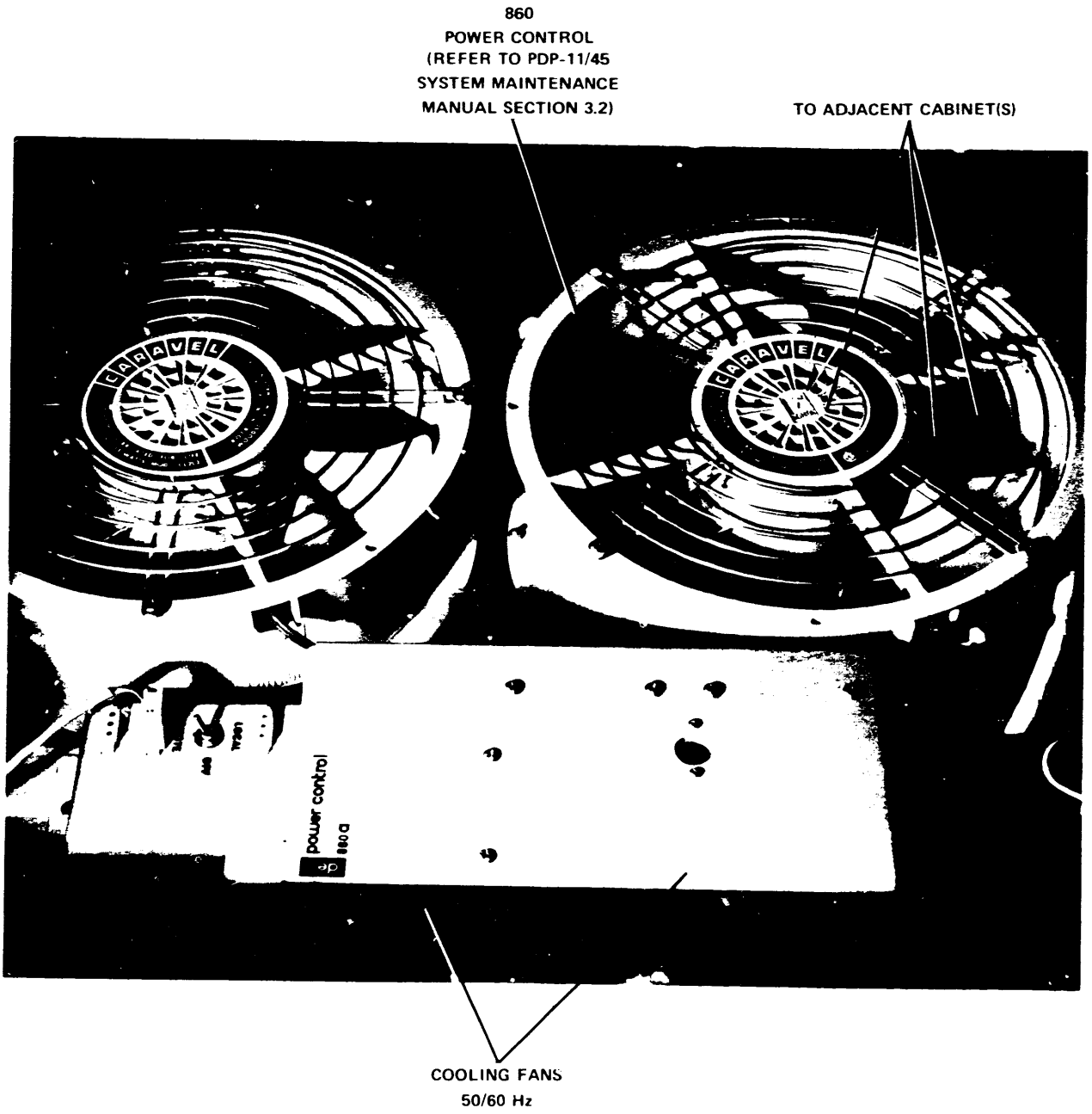


Figure 5-3 RP11-C Inside Top View (Early Models)

NOTE

Recent models of the RP11-C are shipped with the 861 Power Controller, which is located at the bottom of the cabinet and shown in Figure 5-4.

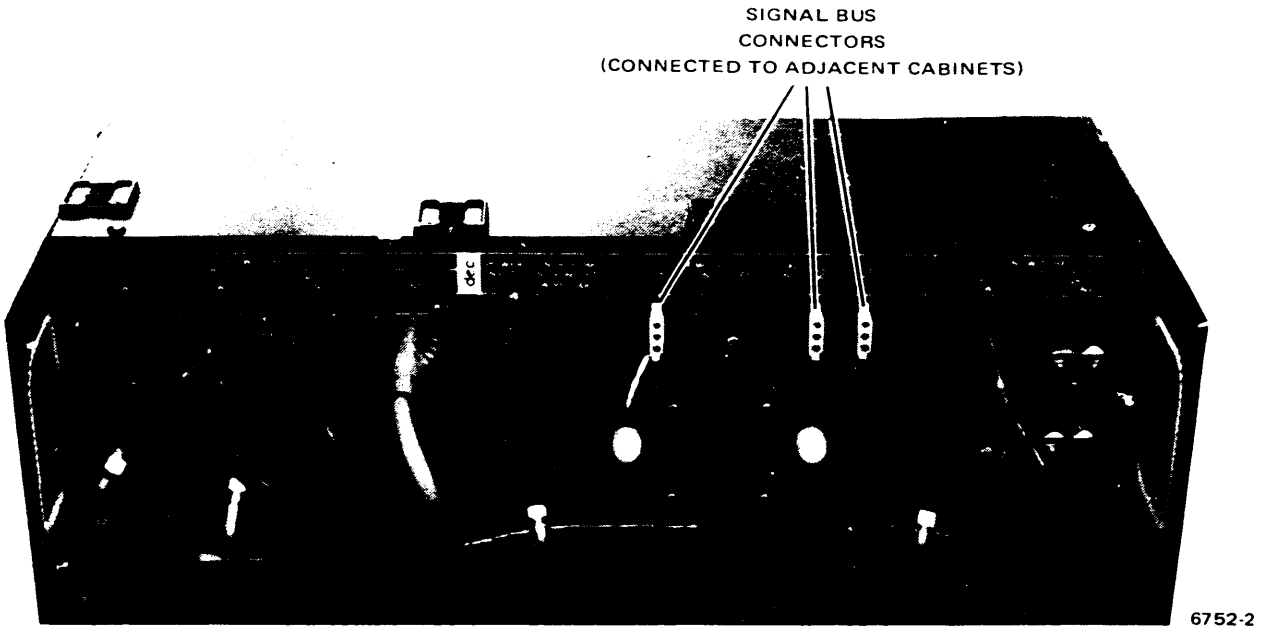


Figure 5-4 861 Power Controller

Table 5-1
Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 353
X10 Probe	Tektronix	
X1 Probe	Tektronix	
Hand Unwrapping Tool	Gardner-Denver	H812A505 244–475
Hand-Operated Wire-Wrap Tool with 504221 bit for 30 AWG Wire and 500350 Sleeve	Gardner-Denver	14H1C
Module Extender	DEC	Type W982
Diagnostic Self-Test Routines	DEC	MAINDEC-11-DZRPA MAINDEC-11-DZRPB MAINDEC-11-DZRPC MAINDEC-11-DZRPD

5.2.3 Electrical Checks and Adjustments

5.2.3.1 Power Supply Checks and Adjustments

Perform the power supply output checks described in Table 5-2 and Figure 5-5. Use a multimeter to check the output voltage measurements with the normal load connected. Use an oscilloscope to measure the ripple content on all dc outputs of the supply. Voltage measurements should be made at the logic racks. Refer to Table 5-3 for a listing of reference drawings and to Figure 5-6 for locations of adjustments. Proceed with the adjustments as follows:

1. Adjust R50, located on the regulator board of the H740-D Power Supply, for +5V ± 5 percent.

NOTE

R35 and R26, the +15V and -15V adjustments of H740-D Power Supply, are not used in the RP11-C.

2. Adjust analog +15V at H704-C Power Supply for +15V ± 5 percent.

3. Adjust analog -15V at H704-C for approximately -15V. This brings -15V in range of -12V regulator W7040 in H03. Continue to adjust -15V at H704-C while monitoring for optimum -12V ± 5 percent at A23K1, U1, or B23A1, U1 (-12V) to A23C2 (GND).

4. Adjust analog +5V at G820 in H02 slot for +5V ± 5 percent.

Table 5-2
Power Supply Output Checks

Measurement Point	Nominal Voltage	Acceptable Range	Maximum Ripple (mVrms)
A01A2(+) to A01C2(-)	+5V	4.75 – 5.25V	200
H01E2(+) to H01C2(-)	Analog +15V	14.25 – 15.75V	100
H03D2(-) to H03N2 (+)	Analog -15V	14.5 – 15.5V	100
J01A2(+) to J01C2(-)	Analog +5V	4.75 – 5.25V	300 (400 ns)

5.2.3.2 Data Separator Delay Checks – Check the critical delays in the data separator at least once in every six month period to verify that each is within its specified tolerance range (Paragraph 4.1.1). Replace or adjust those modules that do not meet specifications.

5.2.4 Cleaning

For trouble-free operation take the same environmental care as is indicated for magnetic tapes. In particular, the heads and the packs should be kept clean.

Materials and equipment needed for cleaning are as follows:

a. Lint-free wipers (cloth or paper), such as Kimwipes Type 900-S, Stock No. 3415 (about 8 in. X 5 in.).

b. Isopropyl alcohol, at least 90 percent, such as Merck or NF (99 percent by weight) or Lilly (91 percent by volume).

NOTE

Store alcohol in its original container or in a glass jar.

c. Q-tips and pipe cleaners.

d. Wooden tongue depressors, 6 in. X 3/4 in.

NOTE

Do not use plastic depressors (these are softened by alcohol).

e. A high-intensity light or other strong light source.

f. A piece of white cardboard or stiff paper (8-1/2 in. X 11 in.).

Inspect the heads for dirt accumulation at least twice monthly (weekly for around-the-clock operation). When necessary, clean the heads carefully with a Q-tip soaked in alcohol, and clean out the two holes in each head with a pipe cleaner, also soaked in alcohol. Keep all cabinet and pack filters clean and fresh. Dirty heads can be caused by poor head flight due to poor air flow through the pack or cabinet. Always replace a single head that collects dirt while others in the same drive remain clean.

Do not clean all of the packs at an installation just for the sake of cleaning them. If a pack is subject to random errors, or if vital information that is not duplicated elsewhere cannot be retrieved, and the problem is not alleviated by cleaning the heads, then clean the pack. In any event, depending on environmental conditions, test all packs every few months by cleaning a couple of surfaces at random in each; clean all surfaces in any pack in which dirt is discovered.

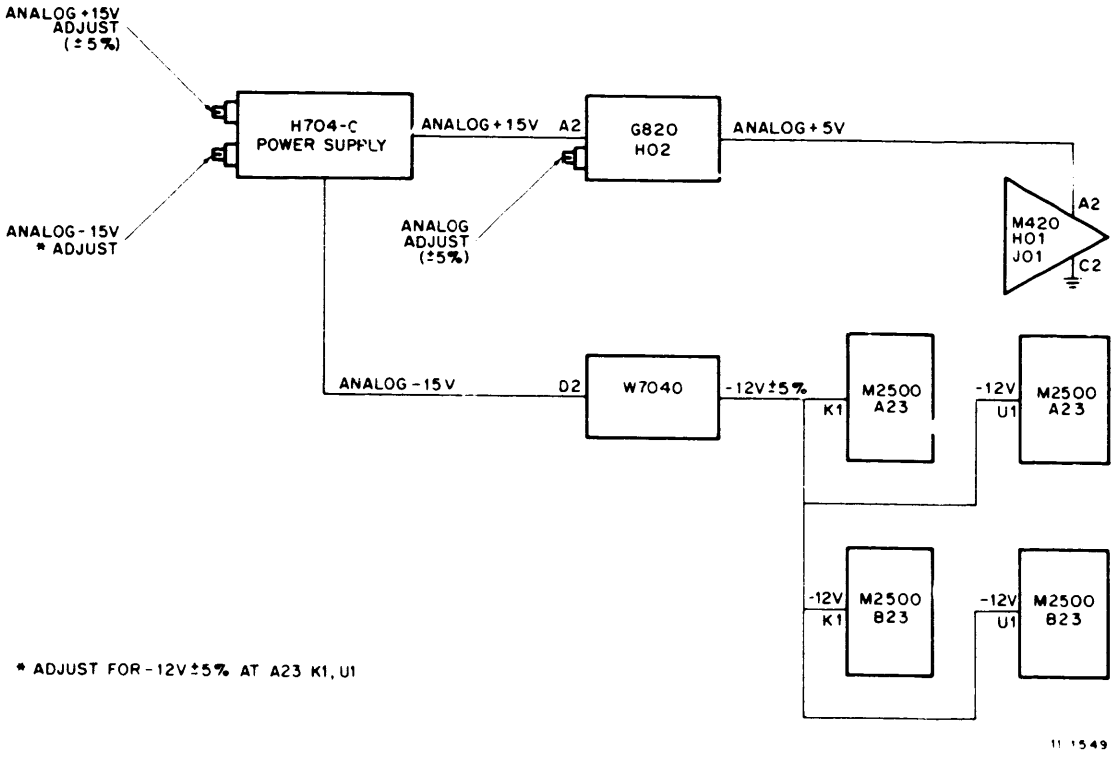


Figure 5-5 Analog DC Power Distribution

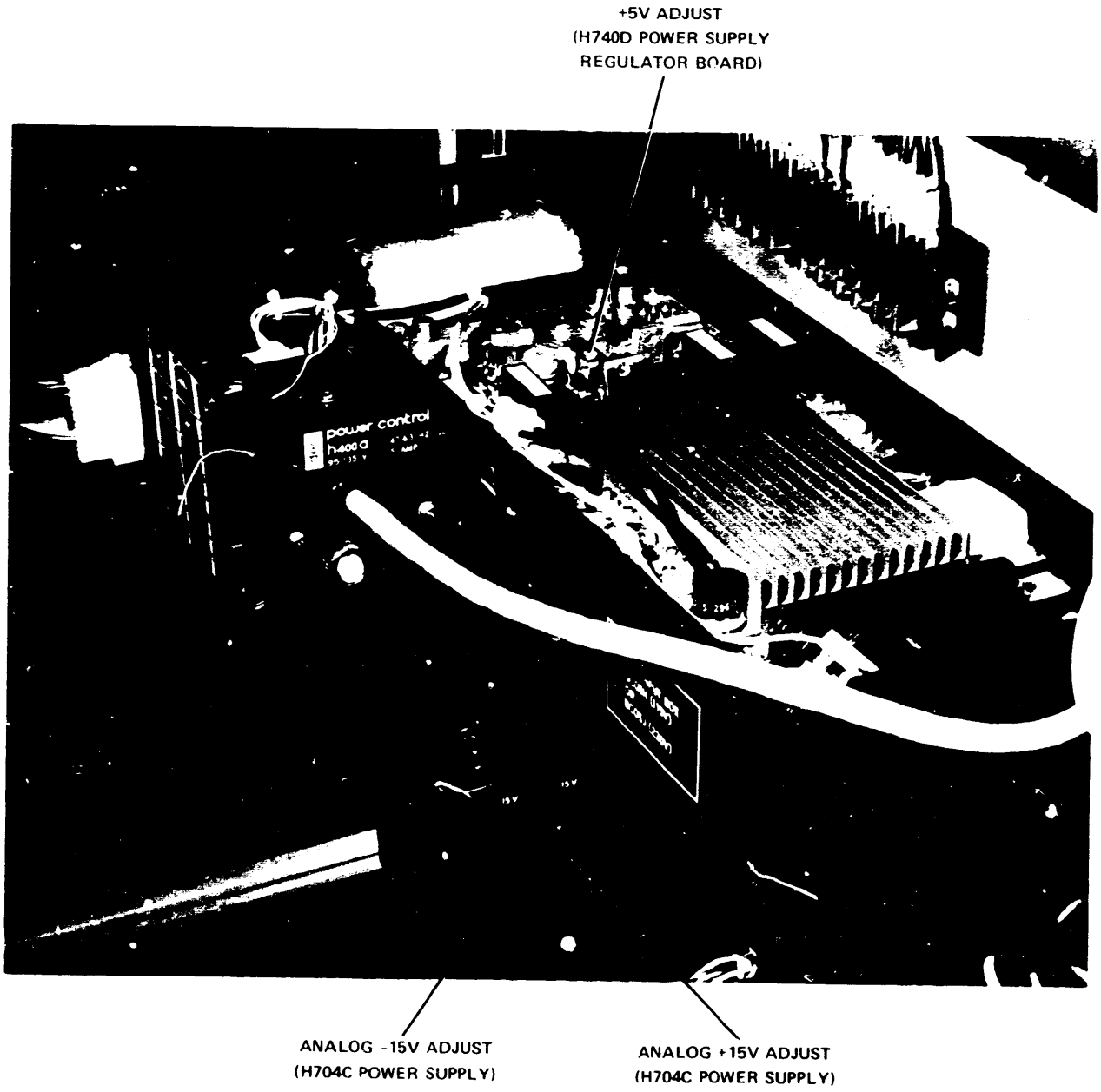


Figure 5-6 RP11-C Power Supply Adjustments

Table 5-3
RP11-C Power Supply Reference Drawings

Title	Drawing Number
H740-D Circuit	D-BD-H740-D-1
Transformer Ass'y	D-IA-7008726-0-0
Regulator Board	E-IA-5409728-0-0
	D-CS-5409728-0-1
Line Set	C-UA-BC05J-0-0
230 Vac 4 A	
Line Set	C-UA-BC05H-0-0
115 Vac	
(H704-C) Power	D-UA-H704-C-0
Supply Ass'y (115 Vac)	A-PS-12-03186
H704-C Test	A-SP-H704-C-1
Procedure	
H722 Stepdown	D-UA-H722-0-0
Transformer	
Indicator	D-UA-H716-0-0
Power Supply 716	
RP11-C Disk	D-UA-RP11-C-0
Controller	

To clean, mount a pack on a drive from which the upper case panels have been removed or on a free-standing spindle mechanism that allows the pack to be turned by hand with the cover removed. Place the light with the white cardboard as a background so that plenty of light shines into the pack. Use the following procedure for cleaning each surface:

1. Position the light so the surface is clearly visible.

2. Wrap a fresh wiper around a depressor with the wiper extending 3/8 in. beyond the wood at one end.

3. Soak one side of the wrapped depressor with the alcohol (be sure to wet the full width of the depressor).

4. Spin the pack by hand at 40–60 r/min (use the flat top surface of the plastic bezel on the top of the pack).

5. With the pack spinning, insert the prepared depressor with the protected end toward the center, and press the wet side against the surface. Maintain the pack spin while applying about 5–10 pounds pressure against the surface; wet the surface across the full width of the tracks. The pressure may be lightened as the surface dries, but be sure to keep the wiper on the surface with the pack spinning until the surface is completely dry and has a high gloss. Keep the pack spinning while removing the depressor, and check the wiper for dirt.

6. Inspect the surface carefully for scratches. If a scratch corresponds in position to a bad sector as determined by the program, then further cleaning is unlikely to make the sector usable.

WARNING

Do not attempt to use the drive motor when cleaning a pack. Always turn drive power off and spin the pack manually.

Do not clean a pack if either the pack or the alcohol is below 40°F (under these conditions water vapor may condense on the surface).

5.3 CORRECTIVE MAINTENANCE

The logic description provided in this manual permits the use of standard troubleshooting for isolating the faults quickly and efficiently. Usually the most economical procedure is to replace the inoperative module with a spare and return the defective module to DEC for repair or replacement.

5.3.1 General Corrective Procedures

Before beginning troubleshooting procedures, verify that the processor portion of the PDP-11 and Unibus interface are operating properly. Refer to the specific maintenance manual to determine the status. Also, examine the maintenance log to determine if the fault has occurred before and note what steps were taken to correct the condition. Verify that primary power is within allowed tolerance and that all power supplies are operating properly (Paragraph 5.2.3.1). Visually inspect the physical and electrical security of all cables, connectors, modules, and wiring. Check the indicator lamps for proper operation. In particular, check the security of ground connections between racks. Faulty grounds can produce a variety of faults.

5.3.2 Diagnostic Testing

Maintenance diagnostic programs (MAINDEC) are provided by DEC to assist in localizing faults within the RP11-C. Functionally, the programs fall into two categories: test and reliability (Table 5-4). Test programs isolate genuine go/no-go type hardware failures that are easily recognizable, while the reliability programs isolate failures that are more difficult to detect because they are marginal in nature and/or occur infrequently or sporadically. The family of test programs are written so that, when run successively, they test the equipment beginning with small portions of the hardware and gradually expanding until they involve the entire machine. To accomplish this end, the test programs are written around instructions and portions of instructions whose demands on equipment capabilities progress from simple transfers and skips to the most involved data manipulations and computations. As portions of the system are proven operable, they become available to succeeding tests for use in checking out unproven portions of the machine.

To perform a diagnostic routine on the RP11-C alone, run MAINDEC-11-DXRPA.DOC (RP11-C Diskless Diagnostic). If the RP11-C is operating correctly, this test should run without failure.

5.3.2.1 Vibration Tests – Many malfunctions may be located by performing a timing margin check on the PDP-11 while running a particular diagnostic. In addition, a vibration test may be performed on the RP11-C.

To perform a vibration test, use the following procedures:

1. Check switches for immunity from vibration and shock by wiggling them and tapping them with the fingers.

2. Check modules for immunity from vibration and shock in two planes. To check the plane perpendicular to the module mounting plane, tap each module handle with the fingers. To check the plane parallel to the module mounting plane, slide a Teflon rod horizontally across the modules. This should be done slowly, twice in each direction. This test will indicate bad components and poor solder joints.

CAUTION

If vibration tests are applied too vigorously, damage to modules could result.

After localizing the fault to within a functional logic element, run a diagnostic which uses all functions of that element. Trace signal flow through the suspected element with an oscilloscope by synchronizing the oscilloscope sweep with control signals or clock pulses. Check for proper levels, durations, rise and fall times, and timing of all input and output signals.

Table 5-4
Maintenance Diagnostics Abstracts

Diagnostic	Abstract
MAINDEC-11-DZRPA.DOC RP11-C Diskless Diagnostic	Exercises RP11-C in maintenance mode and normal mode. This program has two segments. The first segment verifies the RP11-C logic by utilizing three maintenance registers to simulate signals passing between RP11-C and RP03. Segment two operates in normal mode to verify the switches on the controller and disk drive.
MAINDEC-11-DZRPB.DOC RP11-C Reliability Diagnostic	This program tests addressing capability and data reliability of RP11-C and RP03. The program consists of seven tests, each selectable by the operator. A conversation mode allows operator to define test parameters.
MAINDEC-11-DZRPC.DOC Multidrive Diagnostic	This program tests from one to eight RP02/RP03 disk drives on an RP11-C controller. The program seeks to a random address and writes or reads random data. Concurrent with data transfers are Seek operations on other drives. This test checks for interaction on the bus lines.
MAINDEC-11-DZRPD.DOC Disk Pack Formatter	The RP11-C formatter consists of the following three segments: 1. Formats an RP03 disk and checks all addresses for validity. 2. Allows operator to change the address of a desired sector. 3. Formats and verifies disk with sequence of sector addresses specified by operator.

5.3.3 Read Data Separator Calibration

If parity, checksum, or longitudinal parity errors are occurring from random drives, surfaces, or bits, the read data separator is probably at fault. This failure can be caused by a bad module or by poor alignment. If a module is at fault, the module should be replaced with one known to be good; otherwise, perform the following procedure. The purpose of this calibration procedure is to adjust the variable elements of the data separator so that data being read from the disk pack drive is correctly separated into data bits and clock bits under all combinations of bit shift and speed variations from the drive, and worst case circuit conditions in the data separator.

Equipment required for this calibration procedure is as follows:

a. Dual-trace oscilloscope, Tektronix Type 453.

b. Oscilloscope probes fitted with short (i.e., 3-in. or less) grounding leads.

NOTE

The differential delay between probes should be less than 2 ns. This should be checked by connecting both probes to a convenient waveform (e.g., E20K1, 5 MC H), setting the oscilloscope time base to 5 ns/div and measuring the delay between the channels at the -1.5V level.

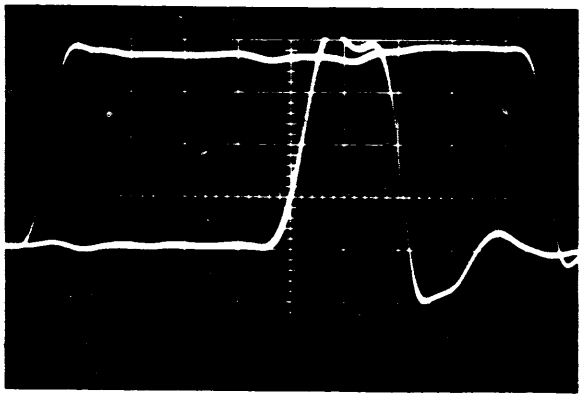
Adhere *strictly* to the following procedures and make all adjustments as precisely as possible.

1. Set the oscilloscope for an external trigger from Channel 1; vertical sensitivity to 1V/div and time base to 20 ns/div, positive trigger.

2. Connect Channel 1 to F18L1, CLOCK GATE H. Connect Channel 2 to F11S2, LOAD SR A, and adjust the variable delay line (F17) so that the positive transition of Channel 2 crosses the 1V level exactly half way between the positive and negative 1V intersections of Channel 1 (Figure 5-7).

3. Run MAINDEC-11-DZRPB and record the delay between F13M2, READ DATA COAX, and F13R2, CLOCK PULSE (1).

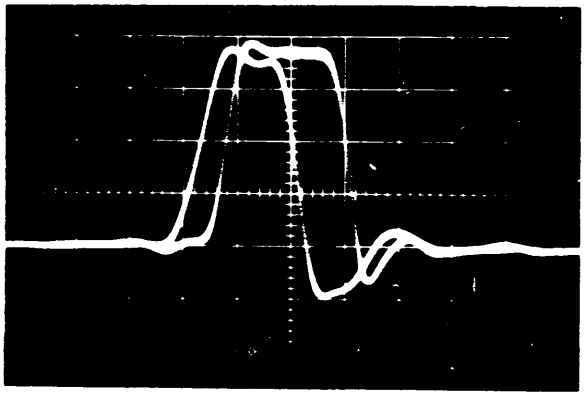
4. Connect Channel 1 to F11S2, LOAD SR A; connect Channel 2 to J01H2. The waveform should appear as in Figure 5-8. Adjust the variable delay line (F15) so that the delay between the positive-going 1V levels of each channel is exactly equal to the value recorded in Step 3.



Oscilloscope

Channel 1	Channel 2
F18L1	F11S2 Trigger from Channel 1
1V/div	1V/div
20 ns/div	20 ns/div Pos. Trigger

Figure 5-7 Read Data Separation Calibration (Step 2)



Oscilloscope

Channel 1	Channel 2
F11S2	J02H2 Trigger from Channel 1
1V/div	1V/div
20 ns/div	20 ns/div Pos. Trigger

Figure 5-8 Read Data Separation Calibration (Step 4)

5.3.4 General Troubleshooting Guides

The following paragraphs contain suggested methods of correcting recurring problems. Additional information is available in applicable DEC Field Service manuals and DEC Tech Tips published periodically.

5.3.4.1 Isolating Silo Memory Failures – To determine if the Silo Memory is the cause of failure, perform the following routine:

1. Press HALT key on CPU.
2. Press START key.
3. Enter Silo Memory address 776736 into processor SWITCH REGISTER.
4. Press LOAD ADDR.
5. Enter desired data pattern into SWITCH REGISTER.
6. Lift DEP switch. ORDY should illuminate and IRDY should remain illuminated.
7. Enter Silo Memory address 776736 into CPU SWITCH REGISTER.
8. Press LOAD ADDR.
9. Press EXAM. Observe data pattern in CPU DATA indicators. ORDY should extinguish. (11/45 Data Select switch in DISPLAY REGISTER position.)

To detect intermittent Silo Memory failures, perform the following procedures:

1. Load the following test program using the PDP-11 console.

	Code	Description
START	013737	;MOVE SWITCH
	177570	;REGISTER CONTENTS
	176736	;TO SILO MEMORY
	013737	;MOVE SILO MEMORY
	176736	;OUTPUT TO DISPLAY
	177570	REGISTER
	000771	BR→START

2. Load starting address.
3. Press START key.
4. Key any data pattern in SWITCH REGISTER and observe same in DISPLAY REGISTER.

5.3.4.2 Disk Pack Compatibility – To determine if two disk packs are compatible, run the RP11-C MAINDEC-11-DZRPB, and swap packs, reading first on the second drive. If any errors occur, the drives are considered to be incompatible.

NOTE

All drive diagnostic programs must be run successfully before attempting compatibility tests. The pack used must be formatted with the drive under test.

If the drives are found to be incompatible, each should be aligned as described in the *RP03 Maintenance Manual.*

CAUTION

C.E. (Customer Engineering) Packs are not indestructible. The associated specially recorded track can be destroyed, rendering the pack unusable. Therefore, extreme care should be exercised with the use of C.E. Packs. They should be used only when aligning heads or checking head alignment. They should never be used for any other troubleshooting or alignment procedures.

5.3.4.3 Proper Use of C.E. Packs – The following procedures protect and indefinitely extend the usable life of C.E. Packs. This is an abbreviated procedure; a more comprehensive procedure can be found in *ISS Model 715D Disk Storage Drive Manual* (UD002341-1), Section 6.7.3.

1. Do not connect the tester until all power has been removed from the drive.

CAUTION

Before cables are removed, all power must first be removed from all drives (via S1) as well as from the RP11-C. Failure to do so can result in damage to the steering diodes in the power sequencing network.

2. Connect DSDDU tester. (Refer to ISS Manual, Chapter 7.)

3. Set the drive to READ ONLY.

CAUTION

Always disable WRITE AMP by switching to READ ONLY before using C.E. Packs to ensure safety of specially recorded elliptical tracks.

4. Apply power to drive the S1, then apply power to tester.

5. Press UNIT DESELECT on tester.

NOTE

This step is necessary to prevent accidental writing over the test track, which would effectively destroy its usefulness.

Head and Pack Thermal Equilibrium:

1. Before heads are adjusted, thermal equilibrium procedures should be followed. The temperature stabilization cycle, which assures standard operating temperature during head alignment, consists of first running the drive with the C.E. Pack installed and all covers on for 1 hour and 15 minutes, then running the drive with the C.E. Pack installed and the two top covers off for an additional 20 minutes before attempting alignment.

2. Use only the special tools for maintenance (i.e., beryllium screwdriver, torque wrench, etc.).

NOTE

All RP03 vendor manuals are serialized and contain specific information pertaining to that drive (i.e., ECOs, updated prints, etc.). Each manual must be maintained as engineering documentation.

When a C.E. Pack is used on the RP03, the READY signal will not occur. Therefore, jump A17-32 to A17-2 and A06-01 to A06-19. This indicates to the drive logic that an index pack is being used, instead of a sectored pack.

5.3.4.4 Search Errors – Search Errors (Header Not Found) can be caused by a variety of conditions. A known formatter pack should be run. If search errors occur on only specific surfaces of a drive, the drive read logic should be checked. If search errors occur from all drives, the data separator operation should be checked. To do this, synchronize from the positive transition of F25E1 [HEADER WINDOW (1)] and view F13M1 [READ Bit (1)]. This bit should be on a 1 for approximately 200 ns, 15 μs after HEADER WINDOW. If READ BIT is not a 0 after 100 μs, or if it never transitions to a 1, the separator is at fault. However, if READ BIT performs correctly the Shift Register or header compare logic is at fault.

5.3.4.5 Controller Data Errors – Word parity errors occurring alone (not in conjunction with other errors) indicate failure in either the Word Parity (Write) Circuit or the RD Word Parity (Read) Circuit. To test the logic, run MAINDEC-11-DZRPB to verify that both circuits are operating properly (capable of assuming Read and Write states).

Longitudinal parity errors occurring alone (not in conjunction with other errors) indicate failure of the longitudinal parity circuit. To test this logic, run MAINDEC-11-DZRPB and verify that the Longitudinal Parity Register is loaded during both Read and Write operations and that the combining logic associated with this register is operating properly.

Checksum errors occurring alone (not in conjunction with other errors) indicate failure of the checksum circuits. To test this logic, run MAINDEC-11-DZRPB and verify that the Checksum Counter is operating properly during both Read and Write operations. Also verify that the checksum is written on the disk for each 36-bit disk word.

NOTE

Word parity, checksum, and longitudinal parity errors in combination specify improper operation of the RP03 drive or data separator logic. Refer to Paragraphs 4.6 and 5.3.3 for information concerning the data separator and to the *RP03 Maintenance Manual* for drive maintenance procedures.

5.3.4.6 Non-Controller Data and Write Check Errors – Data and Write Check errors generated by the PDP-11 computer and not occurring in conjunction with RP11-C errors indicate probable fault within the Buffer Register of the Unibus interface. To test this logic, run MAINDEC-11-DZRPB and verify that the Silo Memory or Buffer Register can be loaded from both the Shift Register and the Unibus and that the Unibus interface and addressing functions are not failing.

5.4 RP03 HEAD ALIGNMENT, USING RP11-C

The RP11-C includes maintenance logic that allows it to control a selected RP03 for the purpose of performing head alignment, without the need for special head alignment tester equipment.

To perform RP03 head alignment, load the following program from the programmer's console:

	Content	Explanation
START	000005	Reset
	012737	
	000222	Cylinder 222 = (146 decimal)
	776722	RPCA
	013737	
	177570	TAR from Switch Register 12–8
	776724	RPDA
	012737	
	000011	Select Drive 0–7 (0 shown), Seek, Go.
	776714	RPCS
	000000	
	000764	BR→START

Proceed as follows:

1. Connect jumper between J13M2 and J13C2.
2. Load starting address.
3. Set Switch Register to select desired head, using switches 12–8.
4. Press START.
5. Use the oscilloscope to observe RP03 waveforms as described in Paragraph 6.7 of the RP03 manual, *Model 715D Disk Storage Drive Operation, Service, and Diagrams*, UD002341-2.
6. To reselect new head, change Switch Register 12–8 to the desired head and press CONT.

NOTE
Remove jumper after completion of head alignment procedure.

APPENDIX A
SIGNAL GLOSSARY

Signal Mnemonic	Drawing Reference	Signal Function
AD SEC H	D13	Advance Sector increments SAR after each new sector header is found.
ADV REQ L	D30 Sheet 2	Advance Request Register signal asserted during Read operation by SILO IN RDY H and asserted during Write or Write Check operations by SIL OUT RDY H. Increments Request Register to next state.
ATTN (07:00) L	D02 Sheet 1	Attention signals generated by maintenance logic or by RP03 drive at inputs shown on drawing D06.
BCNT (05:00)	D15	Contents of bit counter flip-flops 5 through 0. Counts bits per word of each sector.
BIT 31 H	D15	Bit counter contents equal 31 (32nd bit).
BIT 36 H	D15	Bit counter contents equal 36 (37th bit).
BOC D0 H	D28 Sheet 2	Bus Out Cycle signal D0 is derived from BOC state counter to establish a 3 μs window on unit bus line (Figure 4-5).
BOC D2 H	D28 Sheet 2	Bus Out Cycle signal D2 is derived from BOC state counter to provide 1 μs tag on unit bus line (Figure 4-5).
BOC D3 H	D28 Sheet 2	Bus Out Cycle signal D3 is derived from BOC state counter to provide 1 μs pulse to clear Command flip-flop at end of BOC (Figure 4-5).
BOC EN H	D28	Bus Out Cycle Enable signal initiates transmission of a disk drive command to the selected unit.

Signal Mnemonic	Drawing Reference	Signal Function
C CLK L	D28	Control clock used to advance the control sequence logic.
CLK HNF H	D10	Clock HNF (Header Not Found) flip-flop, which will set if correct header has not been found after two complete disk revolutions during a Search operation.
CLR SAR EN L	D13	Clear SAR Enable is asserted at the end of sector 9 by the AD SEC (Advance Sector Counter) signal.
CLR SOT L	D10	Clear Sector of Track counter on the first sector pulse after the index pulse.
COMP*MSYN L	D20	Compare AND Master Sync signal enables any one of 12 RP11-C addresses, 176710 through 176736, to be decoded.
CYL COM H	D12	Cylinder Address Register (CAR) contents match contents of SR (18:10). Part of Search operation.
CYL 405 H	D11	Cylinder 405 is the address in CAR
D CLK H, L	D07 Sheet 2	Data Clock pulses, at VFO clock frequency, present during data gate except during sector word 164.
DATA CONT H	D28 Sheet 1	Data Continue signal is asserted during Read, Write, or Write Check operation until Silo Memory word count overflow occurs.
DATA DONE L	D28 Sheet 1	Data Done signal indicates word count overflow has occurred during Read, Write, or Write Check operation (i.e., all of the data transfer operation is done).
DATA GATE CLOCK H	D22	Data Gate Clock pulses generated by VFO during Read operation; otherwise generated by 5 MHz crystal clock. Gates data to the drive after every clock pulse.
DATA XFER EN H	D15	Data Transfer Enable asserted during data window to allow SR TO BR during Read operation, after the last bit of each word.
DONE STR L	D28 Sheet 1	Done Strobe clears the Not Ready flip-flop at the completion of a transfer.

Signal Mnemonic	Drawing Reference	Signal Function
DONE STR 1 L	D28 Sheet 1	Clears Not Ready flip-flop except when in Header mode.
DSK ADR TO SR H	D15	Disk Address to Shift Register signal is asserted at end of sector word 31 to load SR (18:00) with CAR (09:00), TAR (04:00), SAR (03:00) during Write Format operation.
ESECA L	D13	Error in Sector Address signal, asserted by any SAR contents greater than 11_8 (only sector addresses 0 through 9 are allowed).
EN CNT H	D04	Enable Control signal loads control information onto unit bus.
EN SYNC H	D27	Enable Sync is asserted to inhibit bit counter incrementing and allow logic to wait for 1 bit in preheader and postheader sync.
END STROBE H	D28 Sheet 2	End Strobe pulse clears Command flip-flop, also clears Not Ready after Seek or Restore operation is complete.
ERR SYNC 1	D28 Sheet 1	ERROR SYNC 1 flip-flop establishes time to check for cylinder, track, or sector address errors during Seek operation (Figure 4-4).
ERR SYNC 2	D28 Sheet 1	ERROR SYNC 2 flip-flop establishes time to detect any drive not ready errors during initiation of Seek operation. (Figure 4-4).
ETRA H	D17	Error in Track Address. TAR exceeds 23_8 (track 19).
GOOD STUFF 1 H	D08 Sheet 3	Good Stuff 1 signal indicates the SR contains a valid header word to be transferred (read or write format).
GOOD STUFF 2 H	D08 Sheet 3	Good Stuff 2 signal indicates the SR contains a valid data word to be transferred.
GOOD STUFF 3 L	D27	Good Stuff 3 signal inhibits SILO REQ H to prevent LPR from being loaded into Silo Memory during Read operation and inhibits further Unibus load into Silo Memory at end of sector during Write operation.
INC SOT H	D10	Increment Sector of Track Counter with each sector pulse from drive.

Signal Mnemonic	Drawing Reference	Signal Function
INC WSCA H	D27	Increment Word in Sector Counter. A signal asserted by SR clock at bit 36 of each word or when word parity (sync) bit is read in preheader or postheader sync during a Write operation.
INC WSC B H	D27	Increment Word in Sector Counter B signal clocks WSC (00:03) flip-flops after each 16-state cycle of WSC (04:07) counters.
LOAD BR A H	D09 Sheet 1	Load BR A is asserted during first request register state to load BR (35:20) from SR (35:20) or Silo.
LOAD BR B H	D09 Sheet 1	Load BR B is asserted during second request register state to load BR (19:04) from SR (19:04) or Silo.
LOAD BR C H	D09	Load BR C is asserted during the third request register state, which occurs only in 10/15 mode, to load BR (03:00) from SR (03:00) or Silo.
LPR A EQ ONES H	D07 Sheet 1	Longitudinal Parity Register Section A, bits LPR (15:00) (1) H are all set.
LPR B EQ ONES H	D07 Sheet 1	Longitudinal Parity Register, Section B, bits LPR (33:18) (1) H are all set.
READ BIT (1) H	D23	During a Read operation, this is the first stage at which data enters the RP11-C from the selected drive.
REQ H	D29	Request signal used to initiate next Silo Memory transfer to or from BR.
REQ DLY	D30 Sheet 1	REQ DLY flip-flop allows 1 μs delay between REQ and SILO SHIFT IN or SILO SHIFT OUT.
RESET WCOF H	D26	Reset Word Count Overflow when word count is loaded or during Write Format operation.
RPB1 TO SILO H	D09 Sheet 3	RP11 Buffer to Silo signal loads Silo with BR (35:20) during first request register state.
RPB2 TO SILO H	D09 Sheet 3	RP11 Buffer to Silo signal, loads Silo with BR (19:04) during second request register state.

Signal Mnemonic	Drawing Reference	Signal Function
RPB3 TO SILO H	D09 Sheet 3	RP11 Buffer to Silo signal loads Silo with BR (03:00) during third request register state, which occurs only in 10/15 mode.
S LPE L	D07	Set Longitudinal Parity Error flag if either section of LPR is not equal to 1s.
SNXC L	D12	Set Non-Existent Cylinder flag.
SNXS L	D13	Set Non-Existent Sector flag.
SNXT L	D17	Set Non-Existent Track Address flag.
S PE L	D28 Sheet 1	Set Program Error flag if an operation is attempted while another operation is in progress, selected unit is not on-line, or if some error other than address is detected.
S SCK ERR L	D16	Set Serial Checksum Error flag if SCK (03:00) and SR (03:00) do not compare during 11 mode Read operation.
SCHK TO SR H	D15	Serial Checksum to SR gates SCK (03:00) to SR (35:32) at BIT 31 to write serial checksum in 11 mode only.
SEC COM H	D13	Sector Compare is asserted when SR (03:00) match contents of SAR.
SECTOR FOUND LEV H	D10	Sector Found Level is asserted when the Sector of Track (SOT) counter matches the Sector Address Register (SAR) contents.
SEEK SYNC	D28 Sheet 1	SEEK SYNC flip-flop set by Seek command and initial Bus Out Control cycle of Seek operation.
SEOP L	D12	Set End of Pack flag at cylinder 405.
SEQ OUT L	D05	Sequence Out signal is sent out to the drives to provide control ground for power up sequencing.
SET CYLINDER L	D04	Set Cylinder signal gates CAR contents to unit bus.
SET HEAD L	D04	Set Head signal gates TAR contents to unit bus.
SFEE H	D23	Set Format Error flag if parity error is detected in a sector header word.

Signal Mnemonic	Drawing Reference	Signal Function
SFUV L	D03	Set File Unsafe Violation. Asserted when the selected unit has detected an unsafe condition and is prohibiting all operations.
SHIFT SR H	D08 Sheet 1	Shift SR enables SR bits to shift right with each CLOCK L pulse. Inhibited by BIT 36 or SCHK TO SR.
SILO REQ H	D29	Silo Request signal initiates unloading Silo Memory to BR (Write flow diagram, Figure 4-11) or loading Silo Memory from BR (Read flow diagram, Figure 4-8).
SR TO BR H	D09 Sheet 3	Shift Register to Buffer Register occurs only during a Read Data operation; to read the header at SW31, or to read the data while the data window is open. Does not include the LPR word (SW164).
SU CAR(07:00)L	D02 Sheet 1	Response from selected drive SU CAR lines.
SW 29 H	D27	Sector Word 29 (29th state of WSC). Sets HEADER WINDOW in preparation for reading sync bit.
SW 30 H	D27	Sector Word 30 (30th state of WSC). Signal inhibits bit counter incrementing to allow logic to wait for 1 bit in preheader sync.
SW 31 H	D27	Sector Word 31 signal clears HEADER WINDOW, enables SR TO BR during header mode.
SW 35 H	D27	Sector Word 35 sets DATA WINDOW.
SW 163 H	D27	Sector Word 163 signal is used with BIT 36 to provide LPR TO SR during Write operation.
SW 164 H	D27	Sector Word 164 signal clears DATA WINDOW after LPR; also inhibits D CLK and SR TO BR.
SW 165 L	D27	Sector Word 165 signal indicates end of sector and clears HEADER FOUND.
SWCE L	D07 Sheet 2	Set Write Check Error Flag. Asserted by D CLK H if SR and BR do not compare during Write Check operation.

Signal Mnemonic	Drawing Reference	Signal Function
SWPE H	D23	Set Word Parity Error flag if calculated word parity does not compare with parity bit read from disk.
SWPV L	D03	Set Write Protect Violation. Asserted when attempting to write into a write-protected address of a selected drive.
TRCOM H	D17	TAR (04:00) and SR (09:05) compare (SR holds track address).
WCC 0 → 7 L	D07 Sheet 4	Write Check Compare of associated SR and BR bits.
WCC 8 → 15 L		
WCC 16 → 23 L	D07 Sheet 3	
WCC 24 → 31 L		
WCOF H	D30	Word Count Overflow signal is AND of BUS WCOF (1) H and SILO WCOF (1) H.
WRITE BIT (1) H	D23	During a Write operation, this is the last data stage on the RP11-C before the data is shifted out to the selected drive.
XFER TO SR H	D08 Sheet 2	Transfer to SR signal loads LPR or disk address into SR.
XFER TO SR H	D08 Sheet 2	Transfer to SR signal loads LPR or disk address into SR.
XFER TO SR 1 H	D08 Sheet 1	Transfer to SR1 signal loads serial checksum into SR (35:32) or LRR (35:30) into SR (35:30).
XTAL L	D15	Crystal 2.5 MHz clock provides SR CLOCK H pulses to shift in preheader sync area of sector.

RP11-C DISK PACK DRIVE CONTROLLER
MAINTENANCE MANUAL
DEC-11-HRPCA-C-D

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