

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS <b>PARTS LIST</b>					QUANTITY/VARIATION									
MADE BY BILL BLODGETT		CHECKED D. HEALY		SECTION										
DATE 1/22/75		DATE 1/29/75		1										
ENG <i>Ronald A. No</i>		PROD DON WEAVER		ISSUED SECT.										
DATE <i>2/28/75</i>		DATE 3-26-75		1	MJ11-AA	MJ11-AB	MJ11-AC	MJ11-AD	MJ11-AE	MJ11-AM	MJ11-AY	MJ11-AZ	MJ11-AG	MJ11-AH
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION												
1	E-IA-7009769-0-0	CHASSIS 10.5"			1	1	1	1	-	-	1	1	1	1
2	D-PS-1211825-02	SLIDE, 3 POS TILT			1	1	1	1	1	1	1	1	1	1
3	E-AD-7010694-0-0	POWER SUPPLY MJ11 115V			1	-	1	-	-	-	1	-	1	-
4	E-AD-7010694-1-0	POWER SUPPLY MJ11 230V			-	1	-	1	-	-	-	1	-	1
5	D-PS-1211630-0-0	CARD GUIDE			30	30	30	30	-	-	30	30	30	30
6	E-AD-7010497-0-0	PACK PLANE (MEM)			1	1	1	1	-	-	1	1	1	1
7	E-AD-7010497-1-0	BACK PLANE (MEM EL-FAB)												
8	D-IA-7010580-0-0	HARNESS POWER			1	1	1	1	-	-	1	1	1	1
9	D-IA-7010581-0-0	HARNESS AC/DC LO			1	1	1	1	-	-	1	1	1	1
10	D-IA-7009768-0-0	COVER, CHASSIS			2	2	2	2	-	-	2	2	2	2
11	D-AD-7010824-0-0	EXP DATA CABLE ASSY (BAY Ø) 7ft.			1	1	-	-	-	-	-	-	1	1
12	D-AD-7010824-1-0	EXP ADD. CABLE ASSY (BAY Ø) 7ft.			1	1	-	-	-	-	-	-	1	1
13	D-AD-7010826-0-0	EXP CABLE ASSY. (INTER BAY) 10ft.			-	-	1	1	-	-	-	-	-	-
14	D-CS-H217-C-1	H217C 16K X 18 BIT STACK			2	2	2	2	2	1	2	2	8	8
15	D-CS-G235-Ø-1	G235 16K MEM. DRIVE BOARD			2	2	2	2	2	1	2	2	8	8
16	9006022-3	SCR, PHL TRUSSHD #6-32 X .38			11	11	11	11	-	-	11	11	11	11
17	9006633	WASHER INT. TOOTH LOCK #6			7	7	7	7	-	-	7	7	7	7
18	9007651	WASHER EXT. TOOTH LOCK #10			8	8	34	34	-	-	8	8	8	8
19	9009599-2	SCR, PHL FLAT HD #10-32 X .531(SPECIAL)			6	6	6	6	-	-	6	6	6	6
20	906071-3	SCR, PHL HD TRUSS #10-32 X .38			8	8	12	12	-	-	8	8	8	8
21	D-CS-G114-Ø-1	G114 16K SENSE/INHIBIT BOARD			2	2	2	2	2	1	2	2	8	8
* MAY BE USED AS A REPLACEMENT FOR ITEM #6														
TITLE UNIT ASSY MJ11-A				ASSY NO. E-AD-MJ11-A-Ø	SIZE CODE A PL	NUMBER MJ11-A-Ø			REV. D	ECO NO. MJ11-A-00004				
SHEET 1 OF 3				DIST.										

DEC FORM DEC 16-(325)-1031-N870  
DRA 110

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS <b>PARTS LIST</b>					QUANTITY/VARIATION									
MADE BY BILL BLODGETT		CHECKED D. HEALY		SECTION										
DATE 1/22/75		DATE 1/29/75		1										
ENG <i>Ronald A. No</i>		PROD DON WEAVER		ISSUED SECT.										
DATE <i>2/28/75</i>		DATE 3-26-75		1	MJ11-AA	MJ11-AB	MJ11-AC	MJ11-AD	MJ11-AE	MJ11-AM	MJ11-AY	MJ11-AZ	MJ11-AG	MJ11-AH
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION												
<del>22</del>	<del>B-MD-7413204-0-0</del>	<del>CARD GUIDE REWORK</del>			<del>6</del>	<del>6</del>	<del>6</del>	<del>6</del>	<del>-</del>	<del>-</del>	<del>6</del>	<del>6</del>	<del>6</del>	<del>6</del>
23	D-AD-7010532-0-0	FULL DOOR UNIT ASSY.			-	-	1	1	-	-	-	-	-	-
24	D-AD-7010791-0-0	FRONT DOOR ASSY.			-	-	1	1	-	-	-	-	-	-
25	D-IA-7010780-1-0	PANEL LOGO			-	-	1	1	-	-	-	-	-	-
26	C-PL-7006501-35-0	BASIC CABINET ASSY. 19"			-	-	1	1	-	-	-	-	-	-
27	E-UA-861-D-0	POWER CONTROL 115V			-	-	1	-	-	-	-	-	-	-
28	E-UA-861-E-0	POWER CONTROL 230V			-	-	-	1	-	-	-	-	-	-
29	9006073-3	SCR, PHL TRUSS HD #10-32 X .50			-	-	20	20	-	-	-	-	-	-
30	9007786	NUT, TINNER MAN #10-32			-	-	26	26	-	-	-	-	-	-
31	9007086	CLAMP, CABLE			1	1	1	1	-	-	1	1	1	1
32	907031	WRAP, TIE			-	-	6	6	-	-	-	-	-	-
33	D-CS-M8148-Ø-1	M8148 MEM. CONT & TIMING MODULE			1	1	1	1	-	-	1	1	1	1
34	D-CS-M8149-Ø-1	M8149 MEM. TRANCEIVER CARD			1	1	1	1	-	-	1	1	1	1
35	9006077-3	SCR, PHL HD TRUSS #10-32 X 1.00			-	-	2	2	-	-	-	-	-	-
36	B-MD-7413664-0-0	BRKT. LOCKING			-	-	2	2	-	-	-	-	-	-
37	9006634	WASH, INT. TOOTH #8			1	1	1	1	-	-	1	1	1	1
38	9006418-1	SCR PH HD PAN SELF TAP #8-32 x .38			1	1	1	1	-	-	1	1	1	1
<del>39</del>	<del>9006658</del>	<del>WASH, FLAT #6</del>			<del>12</del>	<del>12</del>	<del>12</del>	<del>12</del>	<del>-</del>	<del>-</del>	<del>12</del>	<del>12</del>	<del>12</del>	<del>12</del>
40	D-AD-7011027-0-0	CABLE, TROUGH ASSY			-	-	2	2	-	-	-	-	-	-
41	3612425-02	DECAL, CABINET DESIGNATION			-	-	1	1	-	-	-	-	-	-
42	3612423-00	MJ11 MEMORY STICKER			1	1	1	1	-	-	1	1	1	1
<del>43</del>	<del>9006565</del>	<del>NUT KEPS #10-32</del>			<del>2</del>	<del>2</del>	<del>-</del>	<del>-</del>	<del>-</del>	<del>-</del>	<del>2</del>	<del>2</del>	<del>2</del>	<del>2</del>
TITLE UNIT ASSY. MJ11-A				ASSY NO. E-AD-MJ11-A-Ø	SIZE CODE A PL	NUMBER MJ11-A-Ø			REV. D	ECO NO.				
SHEET 2 OF 3				DIST.										

DEC FORM DEC 16-(325)-1031-N870  
DRA 110

**DIGITAL EQUIPMENT CORPORATION**  
MAYNARD, MASSACHUSETTS  
**PARTS LIST**

MADE BY	BILL BLODGETT	CHECKED	D. HEALY	SECTION
DATE	1/22/75	DATE	1/29/75	1
ENG	<i>Ronald O. [Signature]</i>	PROD	Don Weaver	ISSUED SECT.
DATE	2/28/75	DATE	3-26-75	1

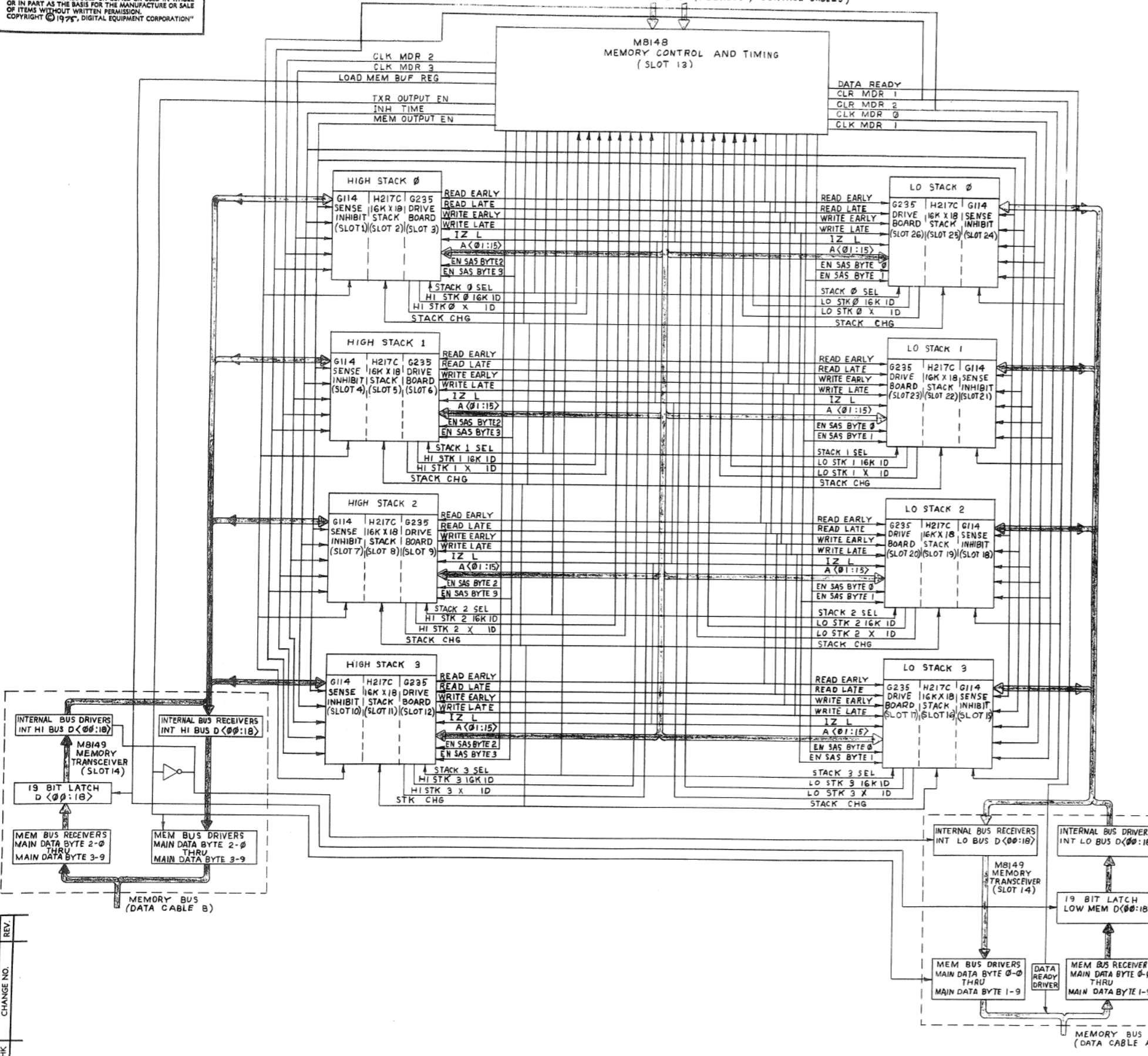
**QUANTITY / VARIATION**

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	MJ11-AA	MJ11-AB	MJ11-AC	MJ11-AD	MJ11-AE	MJ11-AM	MJ11-AY	MJ11-AZ	MJ11-AG	MJ11-AH
			44	C-IA-7010695-0-0	861-D to 861-D HARNESS	-	-	1	1	-	-	-
45	9006568	Nut, Keps 5/16-18	-	-	1	1	-	-	-	-	-	-
46	9008887	Jumper Assy	-	-	1	1	-	-	-	-	-	-
47	C-MD-7413975-0-0	SPACER, SHIM	-	-	1	1	-	-	-	-	-	-
48	C-MD-7414018-0-0	PROTECTOR, RIGHT, METAL EDGE	2	2	2	2	-	-	2	2	2	2
49	C-MD-7414016-0-0	PROTECTOR, LEFT, METAL EDGE	1	1	1	1	-	-	1	1	1	1
50	9006074-03	SCR, PHL TRUSS HD *10-32 X.62	1	1	1	1	-	-	1	1	1	1
51	3612493-0-0	DECAL WARNING	2	2	-	-	-	-	2	2	2	2
52	9009715	SCR, PHL TRUSS HD *10-32 X.25 LG BLACK OXIDE	1	1	1	1	-	-	1	1	1	1
53	A-SP-3700194-0-0	PACKAGING INSTRUCTION (INTERPLANT)	4	4	6	6	-	-	4	4	4	4
54	A-SP-3700195-0-0	PACKAGING INSTRUCTION (CUSTOMER)	1	1	-	-	-	-	1	1	1	1
55	9006565	NUT KEPS *10-32	1	1	-	-	-	-	1	1	1	1
			-	-	1	1	-	-	-	-	-	-

TITLE	UNIT ASSY. MJ11-A	ASSY NO.	E-AD-MJ11-A-Ø	SIZE	CODE	NUMBER	REV.	ECO NO.
				A	PL	MJ11-A-Ø	D	
		SHEET	3	OF	3	DIST.		

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D  
C  
B  
A



DATA BIT NAME EQUIVALENCY

MEMORY BUS NAME	INTERNAL BUS NAME (MJ11 BACK PANEL)
MAIN DATA BYTE 0-0 L	LOW BUS D00 L
MAIN DATA BYTE 0-1 L	LOW BUS D01 L
MAIN DATA BYTE 0-2 L	LOW BUS D02 L
MAIN DATA BYTE 0-3 L	LOW BUS D03 L
MAIN DATA BYTE 0-4 L	LOW BUS D04 L
MAIN DATA BYTE 0-5 L	LOW BUS D05 L
MAIN DATA BYTE 0-6 L	LOW BUS D06 L
MAIN DATA BYTE 0-7 L	LOW BUS D07 L
MAIN DATA BYTE 0-8 L	LOW BUS D08 L
MAIN DATA BYTE 0-9 L	LOW INT BUS D09 L
MAIN DATA BYTE 1-0 L	LOW INT BUS D10 L
MAIN DATA BYTE 1-1 L	LOW INT BUS D11 L
MAIN DATA BYTE 1-2 L	LOW INT BUS D12 L
MAIN DATA BYTE 1-3 L	LOW INT BUS D13 L
MAIN DATA BYTE 1-4 L	LOW INT BUS D14 L
MAIN DATA BYTE 1-5 L	LOW INT BUS D15 L
MAIN DATA BYTE 1-6 L	LOW INT BUS D16 L
MAIN DATA BYTE 1-7 L	LOW INT BUS D17 L
MAIN DATA BYTE 1-8 L	LOW INT BUS D18 L
MAIN DATA BYTE 1-9 L	LOW INT BUS D19 L
MAIN DATA BYTE 2-0 L	HI BUS D00 L
MAIN DATA BYTE 2-1 L	HI BUS D01 L
MAIN DATA BYTE 2-2 L	HI BUS D02 L
MAIN DATA BYTE 2-3 L	HI BUS D03 L
MAIN DATA BYTE 2-4 L	HI BUS D04 L
MAIN DATA BYTE 2-5 L	HI BUS D05 L
MAIN DATA BYTE 2-6 L	HI BUS D06 L
MAIN DATA BYTE 2-7 L	HI BUS D07 L
MAIN DATA BYTE 2-8 L	HI INT BUS D16 L
MAIN DATA BYTE 3-0 L	HI BUS D09 L
MAIN DATA BYTE 3-1 L	HI BUS D10 L
MAIN DATA BYTE 3-2 L	HI BUS D11 L
MAIN DATA BYTE 3-3 L	HI BUS D12 L
MAIN DATA BYTE 3-4 L	HI BUS D13 L
MAIN DATA BYTE 3-5 L	HI BUS D14 L
MAIN DATA BYTE 3-6 L	HI BUS D15 L
MAIN DATA BYTE 3-7 L	HI BUS D18 L
MAIN DATA BYTE 3-8 L	HI INT BUS D19 L
MAIN DATA BYTE 3-9 L	HI INT BUS D18 L

TO TIE THE INTERNAL BUS SIGNAL NAME TO SIGNAL NAME ON G114 CIRCUIT SCHEMATIC (TO LOCATE DATA BIT ELECTRONICS ON SENSE/INHIBIT):

1. DETERMINE WHETHER DATA BIT IS IN HIGH OR LOW WORD
2. DETERMINE WHICH "STACK" BIT IS IN.
3. TO LOCATE BIT LOGIC, DELETE "HI" OR "LO" PREFIX FROM INTERNAL BUS SIGNAL NAME. (EG. LOW BUS D09 BECOMES BUS D09). THE RESULTANT SIGNAL NAME AGREES WITH G114 CIRCUIT SCHEMATIC.

STEPS 1 AND 2 LOCATE THE CARD SLOT IN WHICH THE DESIRED SENSE/INHIBIT CARD RESIDES. STEP 3 TIES THE SENSE/INHIBIT SCHEMATIC TO THE DESIRED CARD.

CONTROL SIGNAL NAME EQUIVALENCY

M8148 SIGNAL NAME	GOES TO	SCHEMATIC WHERE RECEIVED	SIGNAL NAME WHERE RECEIVED
MCTF READ EARLY L	G 235 (ALL)	DRVC	MATB READ EARLY L
MCTF READ LATE L	G 235 (ALL)	DRVC	MATC READ LATE L
MCTF WRITE EARLY L	G 235 (ALL)	DRVC	MATD WRITE EARLY L
MCTF WRITE LATE L	G 235 (ALL)	DRVC	MATD WRITE LATE L
MCTF EN SAS B0 H	G 235 (SLOTS 17,20,23,26)	DRVA	MATH WRITE BYTE 0 L
MCTF EN SAS B1 H	G 235 (SLOTS 17,20,23,26)	DRVA	MATH WRITE BYTE 1 L
MCTF EN SAS B2 H	G 235 (SLOTS 3,6,9,12)	DRVA	MATH WRITE BYTE 0 L
MCTF EN SAS B3 H	G 235 (SLOTS 3,6,9,12)	DRVA	MATH WRITE BYTE 1 L
MCTC STACK SEL 0 H	G 235 (SLOTS 3 & 26)	DRVA	ADA H
MCTC STACK SEL 1 H	G 235 (SLOTS 6 & 23)	DRVA	ADA H
MCTC STACK SEL 2 H	G 235 (SLOTS 9 & 20)	DRVA	ADA H
MCTC STACK SEL 3 H	G 235 (SLOTS 12 & 17)	DRVA	ADA H
MCTH ADB-ADC-ADDH	G 235 (ALL)	DRVC	ADB H, ADC H & ADD H
MCTH ALATE L	G 235 (ALL)	DRVC	ALATE L
MCTF AEARLY L	G 235 (ALL)	DRVC	AEARLY L
MCTF CLR MDR 1 L	G 114 (ALL)	SINA	MATB CLR MDR 1 L
MCTF CLR MDR 2 L	G 114 (ALL)	SINA	MATB CLR MDR 2 L
MCTF MEM OUT EN H	G 114 (ALL)	SINA	MATC OUTPUT ENABLE H
MCTF INHIBIT TIME H	G 114 (ALL)	SINA	MATD INH TIME H
MCTF CLK MDR 0 L	G 114 (SLOTS 15,18,21 & 24)	SINA	MATB CLK MDR 0 L
MCTF CLK MDR 1 L	G 114 (SLOTS 15,18,21 & 24)	SINA	MATB CLK MDR 1 L
MCTF CLK MDR 2 L	G 114 (SLOTS 1,4,7,10)	SINA	MATB CLK MDR 2 L
MCTF CLK MDR 3 L	G 114 (SLOTS 1,4,7,10)	SINA	MATB CLK MDR 3 L
MCTF STCHG H	G 235 (ALL)	DRVA	MATD STACK CHARGE H

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
MJ11				

DIMENSIONAL TOLERANCE		DATE	
DRN.	2-13-75	DATE	2-13-75
CHK'D.	3/21/75	DATE	3/21/75
ENG.	7/6/75	DATE	7/6/75
PROJ. ENG.	7/21/75	DATE	7/21/75
PROD.	7/21/75	DATE	7/21/75

UNLESS OTHERWISE SPECIFIED

MILLIMETERS	INCHES	ANGLES
X,XX ±0.10	.XX ±0.005	±0° 30'
X.X ±0.5	.X ±0.02	
X ±2	.X ±1	

THIRD ANGLE PROJECTION REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓

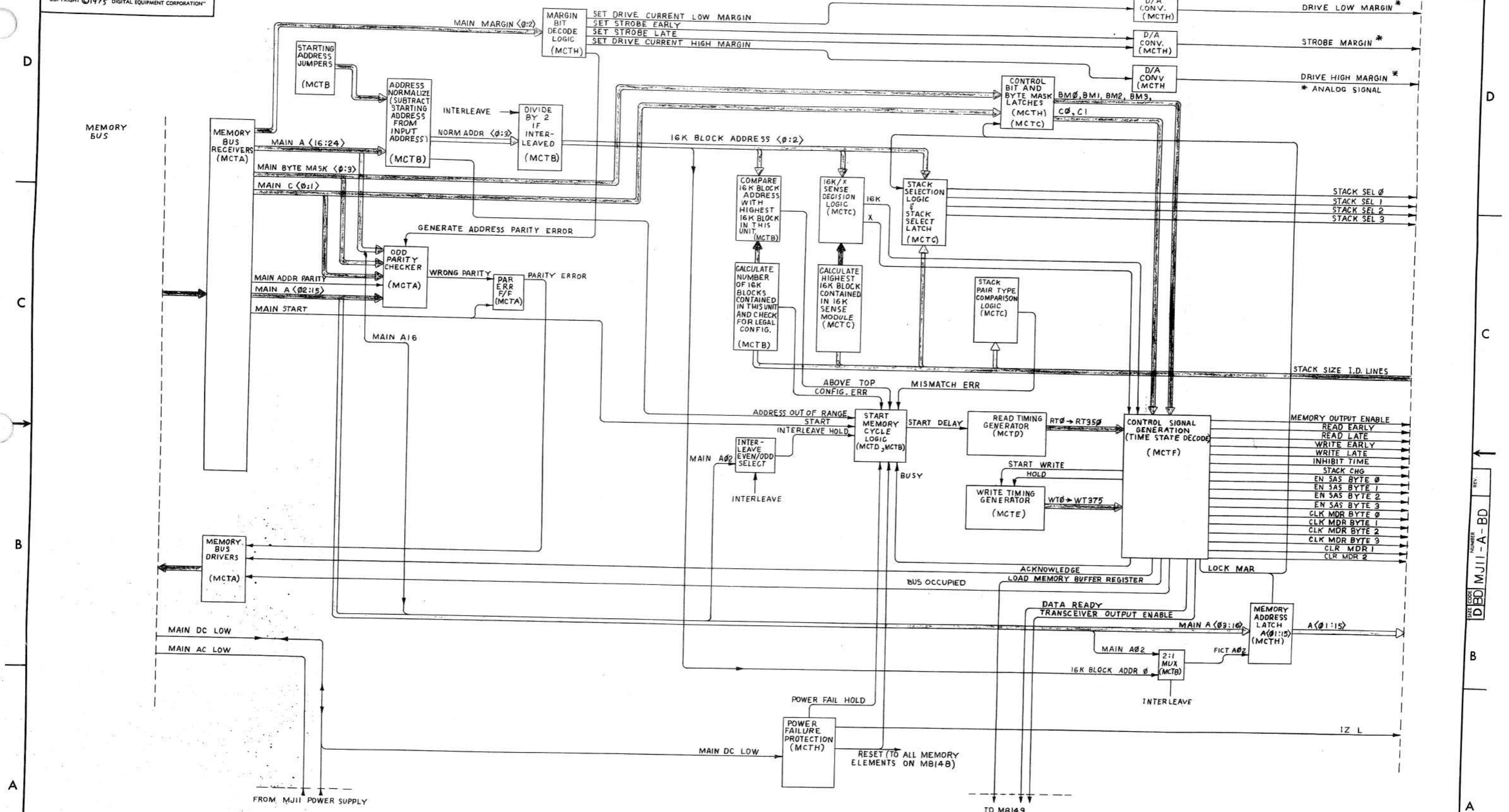
NEXT HIGHER ASSY.

MATERIAL	FINISH	SIZE CODE	NUMBER	REV.
B-DD-MJ11-A-0	SCALE	D BD	MJ11-A-BD	
	SCALE			
	SCALE			

REV. NUMBER  
DBD MJ11-A-BD

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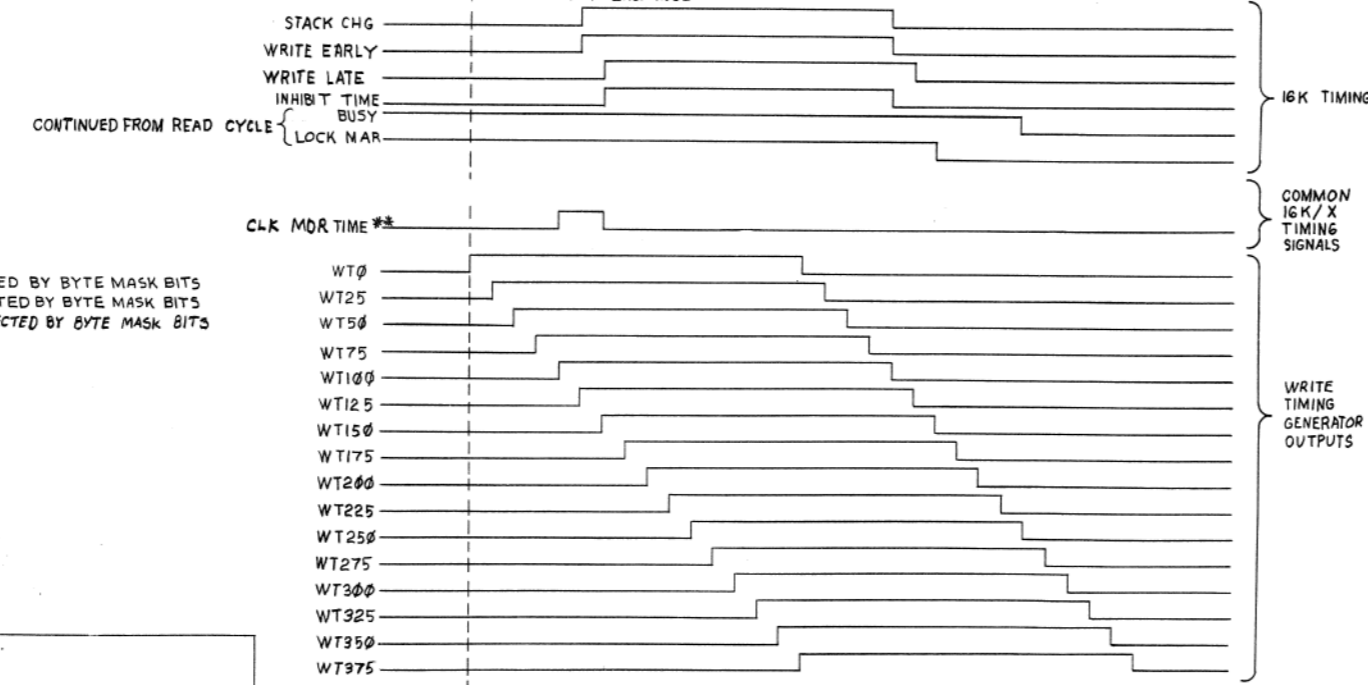
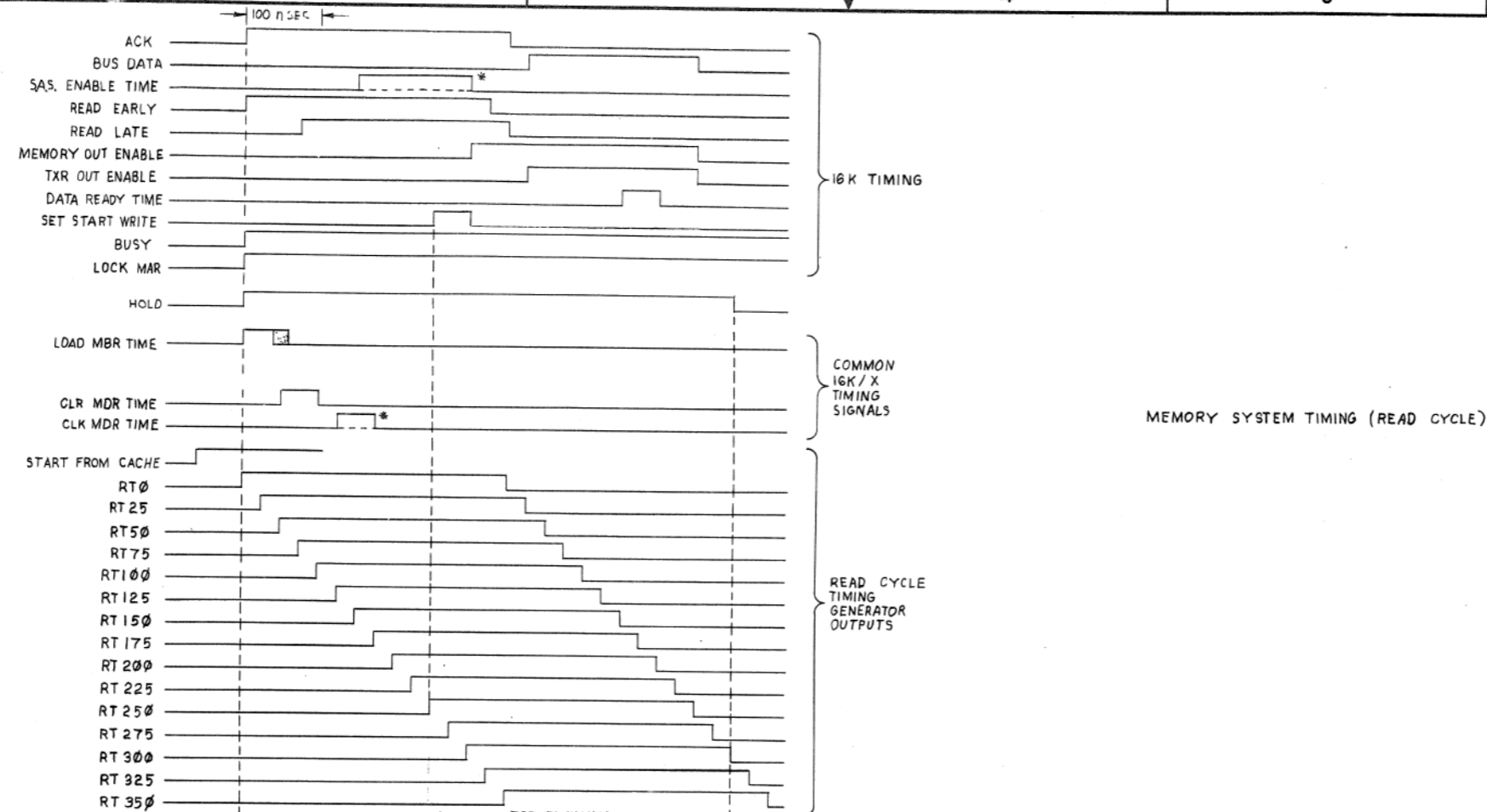
REV. 2  
 SIZE CODE D BD  
 NUMBER MJ11-A-BD



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE MJ11  
 BLOCK DIAGRAM (M8148)  
 SCALE 1:1  
 SHEET 2 OF 2  
 SIZE CODE D BD  
 NUMBER A - BD  
 REV. 2

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\* WRITE CYCLE ONLY - CLK MDR FOR BYTES SELECTED BY BYTE MASK BITS  
- DISABLE SAS FOR BYTES SELECTED BY BYTE MASK BITS  
\*\* EXCHANGE CYCLE ONLY - CLK MDR FOR BYTES SELECTED BY BYTE MASK BITS

REV.	CHG.	NO.

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
MJ11					
DIMENSIONAL TOLERANCE					
DIMENSIONS ARE MILLIMETERS UNLESS OTHERWISE SPECIFIED					
MILLIMETERS	INCHES	ANGLES			
X.XX ±0.10	.XXX ±0.005	±0° 30'			
X.X ±0.05	.XX ±0.02				
X ±2	.X ±0.1				
THIRD ANGLE PROJECTION		REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY		NEXT HIGHER ASSY.	
		MATERIAL		8-DD-MJ11-A-0	
		FINISH		SCALE	
				SHEET 1 OF 1	
PARTS LIST			TITLE		
DRN. 2/17/75			DATE 2/17/75		
CHK'D. 2/17/75			DATE 2/17/75		
ENG. 2/17/75			DATE 2/17/75		
PRJ. ENG. 2/17/75			DATE 2/17/75		
PROD. 2/17/75			DATE 2/17/75		
SHEET 1 OF 1			DATE 2/17/75		
DIGITAL			MJ11 MEMORY TIMING		
SIZE CODE DTD			NUMBER MJ11-A-TD		
REV.			REV.		

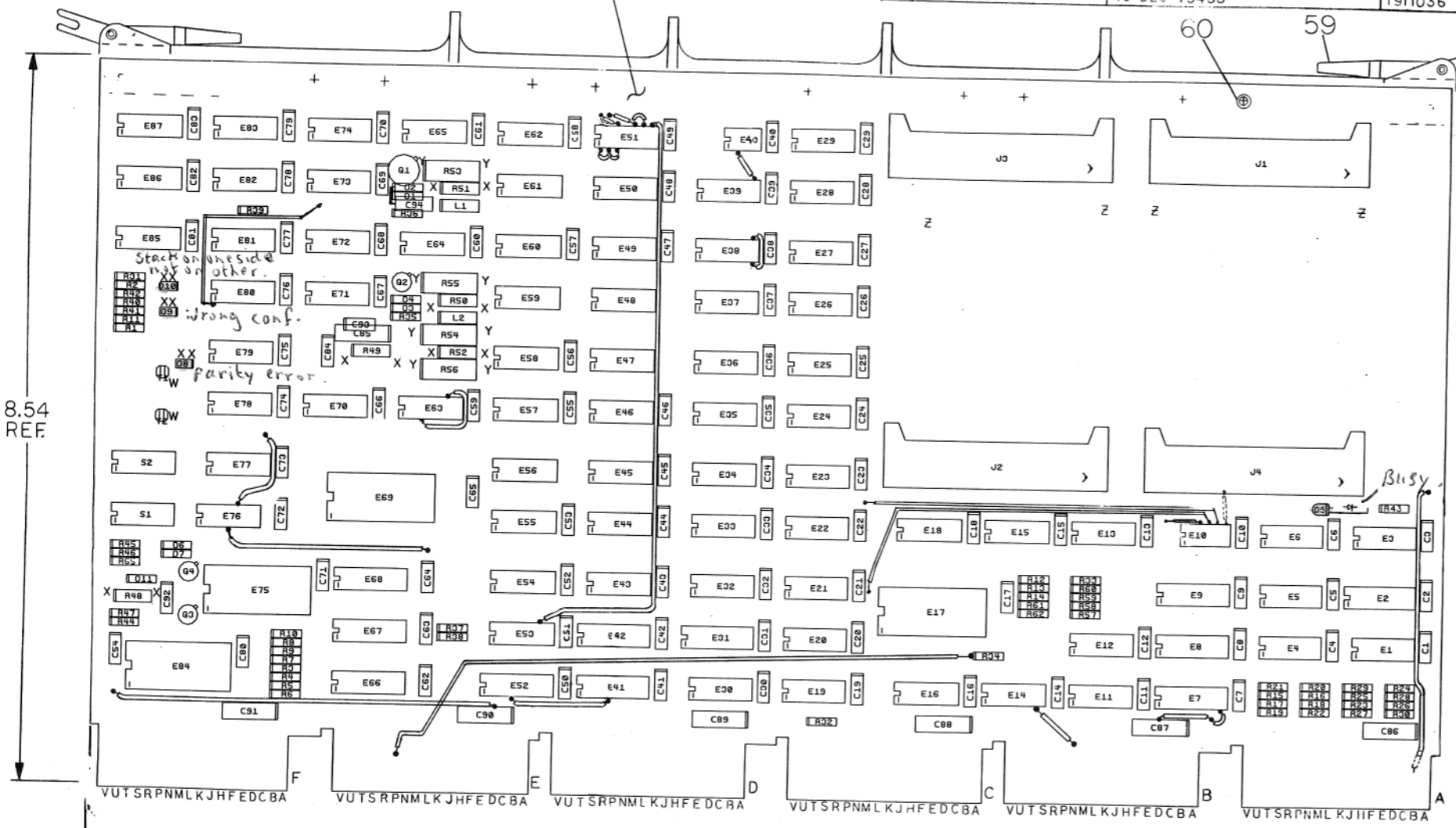
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NOTES:

1-0-8718 MSC 2

2	E86, E51	IC DEC 74S40	1910541	54
1	E67	IC DEC 74S133	1911983	55
1	E14	IC DEC 74S140	1910546	56
1	E2	IC DEC 74187	23-C65A2-01	57
2	TP1, TP2	SPLIT LUGS	9006735	58
1		HANDLE ASSEMBLY	1210711-2	59
12		EYELET (HANDLE)	9006732	60
15		WIRE #30 AWG BUSS (RETROFIT)	9105740-55	61
1	E10	IC DEC 75453	1911036	62

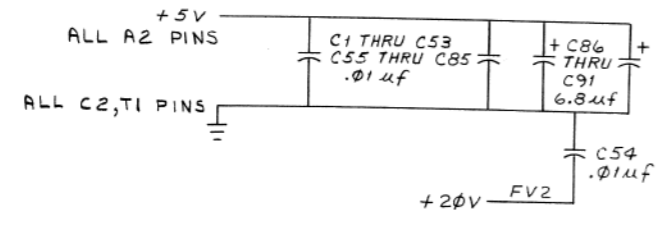
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REF		X-Y COORDINATE HOLE LOCATION	K-CO-M8148-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M8148-0-5	2
REF		MODULE ECO HISTORY	B-MH-M8148-0-6	3
1		ETCHED CIRCUIT BOARD	5011289	4
84	C1 THRU C84	CAPACITOR .01uf 100V 20%	1001610-01	5
7	C85 THRU C91	CAPACITOR 6.8uf 35V 10%	1005306	6
1	C92	CAPACITOR 1000PF 100V 5%	1000042-00	7
2	C93, C94	CAPACITOR 270PF 100V 5%	1000022	8
6	D1, D2, D3, D4, D6, D7	DIODE DEC 777 SWITCHING DIODE	1103041	9
4	D8 THRU D10, D5	DIODE LIGHT EMITTING MV5054-1	1110324	10
1	D11	DIODE ZENER IN 746A 3V	1104860	11
4	J1, J2, J3, J4	CONNECTOR 3M #3432 40 PIN	1209941-01	12
34	R1 THRU R34	RESISTOR 1/4W 1K 5%	1300365	13
3	R35, R36, R37	RESISTOR 1/4W 330 OHM 5%	1300295	14
1	R38	RESISTOR 1/4W 680 OHM 5%	1301424	15
1	R39	RESISTOR 1/4W 470 OHM 5%	1300316	16
4	R40 THRU R43	RESISTOR 1/4W 220 OHM 5%	1300271	17
1	R44	RESISTOR 1/4W 560 OHM 5%	1301890	18
3	R45, R46, R47	RESISTOR 1/4W 20K 5%	1302391	19
1	R48	RESISTOR 1/2W 750 OHM 5%	1300354	20
4	R49 THRU R52	RESISTOR 1/2W 470 OHM 5%	1300315	21
4	R53 THRU R56	RESISTOR 1W 120 OHM 5%	1301838	22
6	R57 THRU R62	RESISTOR 1/8W 1.1K OHM 1%	1302645	23
1	R65	RESISTOR 1/4W 2K 5%	1302388	24
3	Q1, Q2, Q3	TRANSISTOR DEC 3009B	1503100	25
1	Q4	TRANSISTOR DEC 6534D	1503409	26
2	L1, L2	INDUCTOR 100uh	1610662	27
4	E47, E48, E59, E61	DELAY LINE	1611243	28
2	S1, S2	SWITCH 7 POS	1211164-03	29
2		SWITCH COVER	1211284-03	30
9	E22 THRU E29, E36	IC DEC 8640	1911469	31
1	E11	IC DEC 74H04	1909931	32
2	E3, E6	IC DEC 7400	1905575	33
1	E12	IC DEC 74H01-1	1909849	34
4	E34, E35, E37, E38	IC DEC 82S62	1911291	35
2	E85, E87	IC DEC 74S74	1910544	36
1	E78	IC DEC 74H00	1909056	37
4	E17, E69, E75, E84	IC DEC 74S181	1910531	38
1	E68	IC DEC 74S158	1910549	39
11	E13, E43, E45, E56, E57, E58, E60, E62, E65, E77, E49	IC DEC 74S04	1910534	40
12	E32, E33, E39, E44, E46, E54, E55, E63, E72, E73, E74, E79	IC DEC 74S64	1910542	41
1	E5	IC DEC 7404	1909686	42
2	E5C, E70	IC DEC 74S10	1910536	43
1	E21	IC DEC 74S11	1910537	44
2	E80, E81	IC DEC 74S22	1910540	45
5	E41, E42, E52, E66, E31	IC DEC 7475	1909050	46
2	E1, E4	IC DEC 8242	1909712	47
4	E16, E30, E53, E71	IC DEC 74S00	1910532	48
1	E40	IC DEC 75451	1910406	49
2	E20, E82	IC DEC 7408	1910155	50
3	E19, E64, E76	IC DEC 8885	1910649	51
2	E15, E18	IC DEC 74H50	1909060	52
3	E7, E8, E9	IC DEC 74S151	1910956	53



IC TYPE	GND	+5V
DEC 75451	4	8
DEC 74187	8	16
DEC 74S181	12	24
DEC 74S158	8	16
DEC 74S151	8	16
DEC 74S133	8	16
DEC 8640	1	8
DEC 7475	12	5

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS



7/19/75  
T. NORTHROP  
MB148-00003 C  
3/2/75  
TOM NORTHROP  
8/17/75  
Ren Van...  
MB148-00002 B  
1-16-75  
Northrop  
MB148-00001 A  
1-16-75  
Northrop

FIRST USED ON OPTION MODEL MJ11

ETCH BOARD REV A

DRN: J. Vincent DATE: 10-23-74  
CHK'D: R. K DATE: 12/6/74  
ENG: J. Vincent DATE: 12/5/74  
PRJ. ENG: J. Vincent DATE: 12/5/74  
PRD. J. Vincent DATE: 11/17/74

REVISIONS  
CHK CHANGE NO. REV

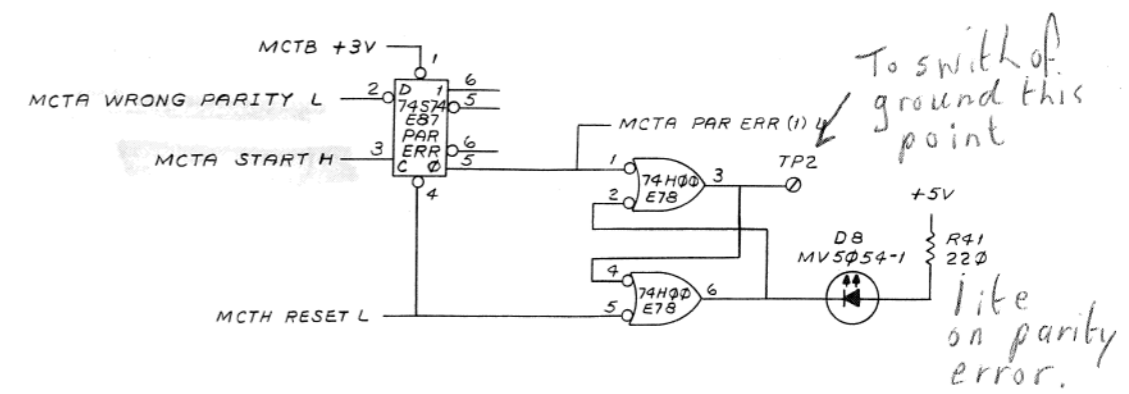
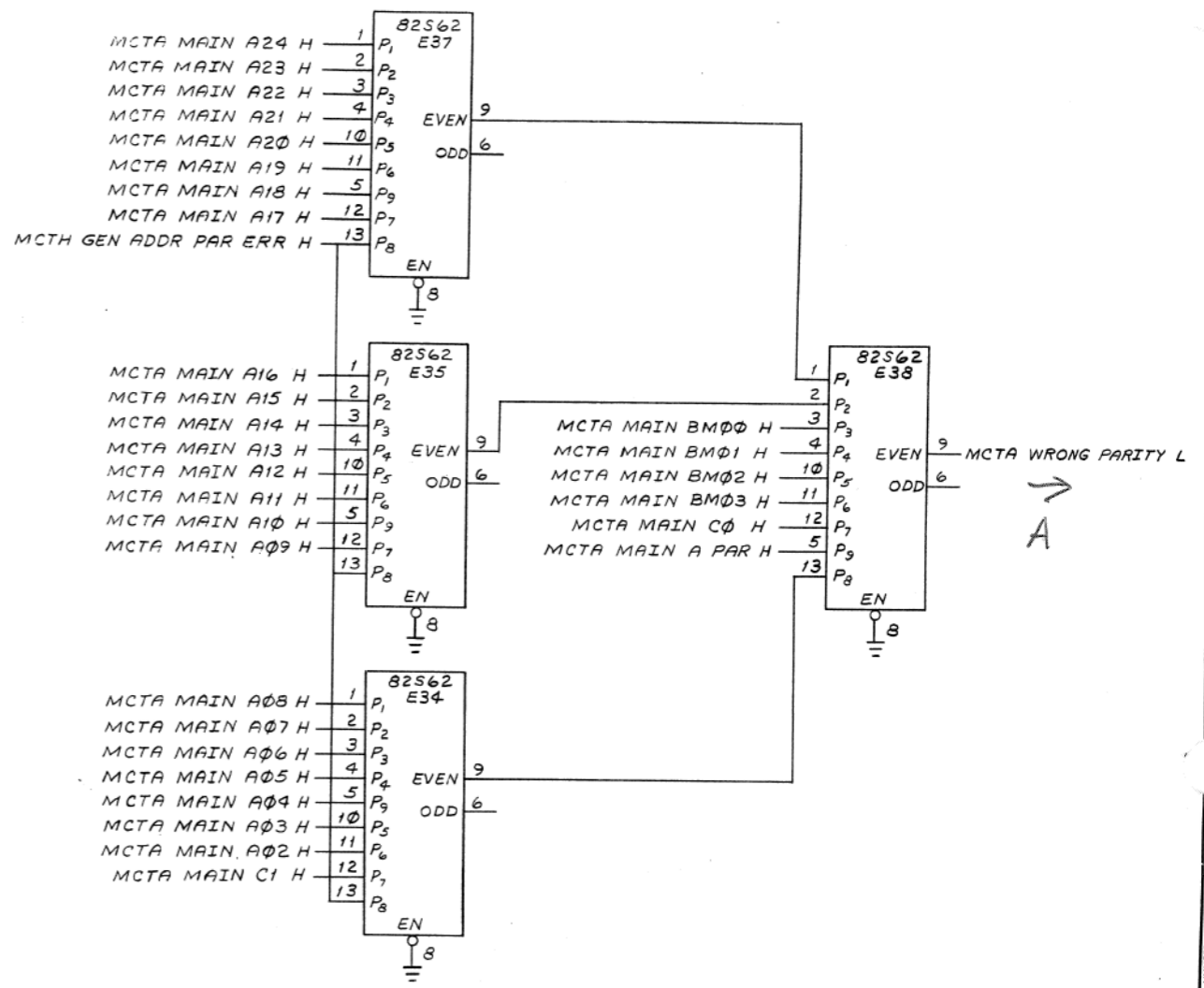
DEC NO. EIA NO. DEC NO. EIA NO.

SEMICONDUCTOR CONVERSION CHART

SCALE: 1 OF 2  
SHEET: 1 OF 2

digital EQUIPMENT CORPORATION  
TITLE: MEMORY CONTROL & TIMING (MCT)  
SIZE CODE: DCS M8148-0-1  
NUMBER: 1  
REV: C

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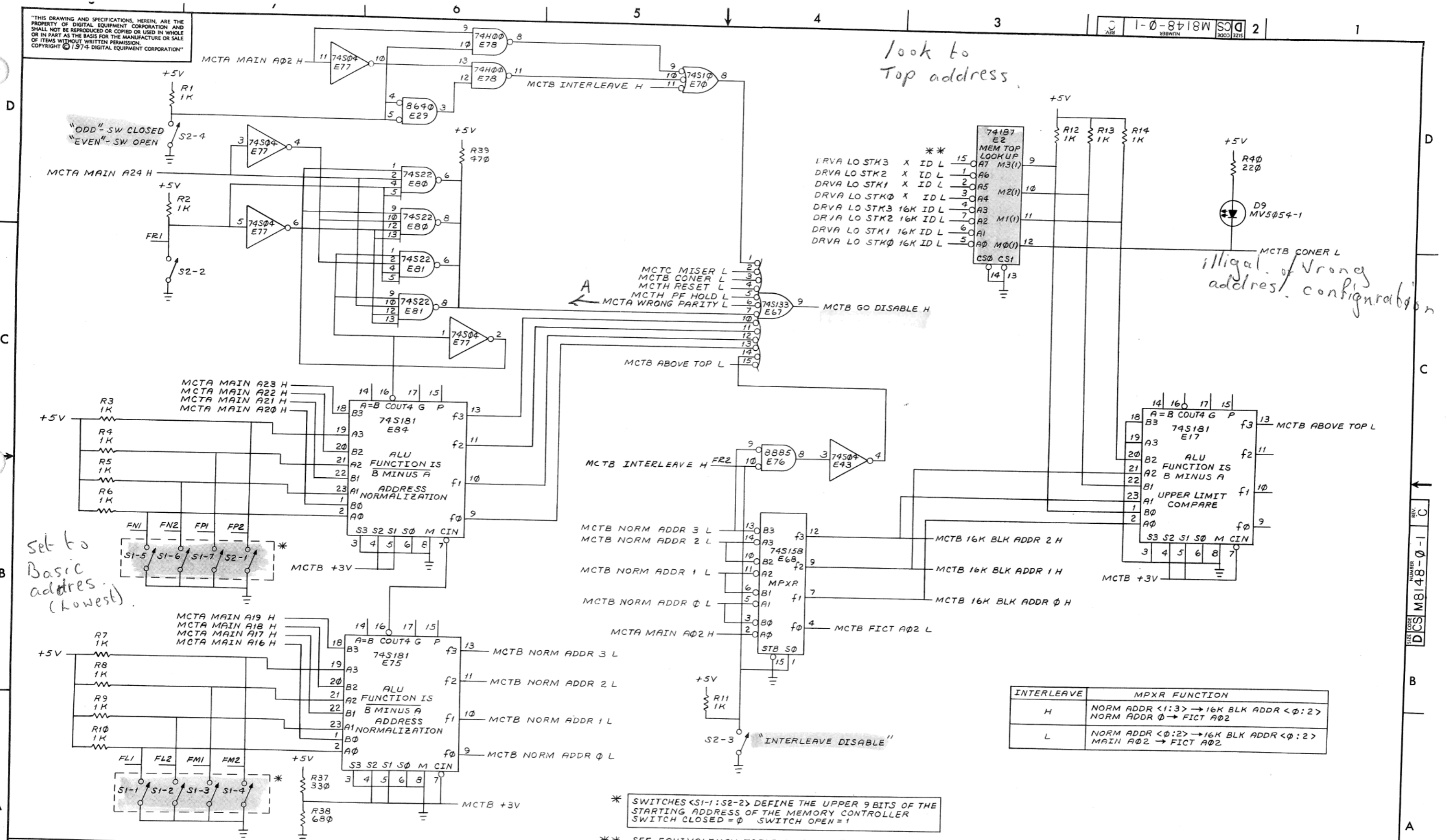
MEMORY BUS INTERFACE AND ADDRESS PARITY CHECKER

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	MEMORY CONTROL AND TIMING (MCTA)	SIZE CODE	D CS	NUMBER	M8148-0-1	REV.	C
SCALE	1/1	SHEET	2 OF 9	DIST.			

REV. C  
NUMBER DCS M8148-0-1

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look to Top address

illegal / wrong address configuration

set to Basic address (lowest)

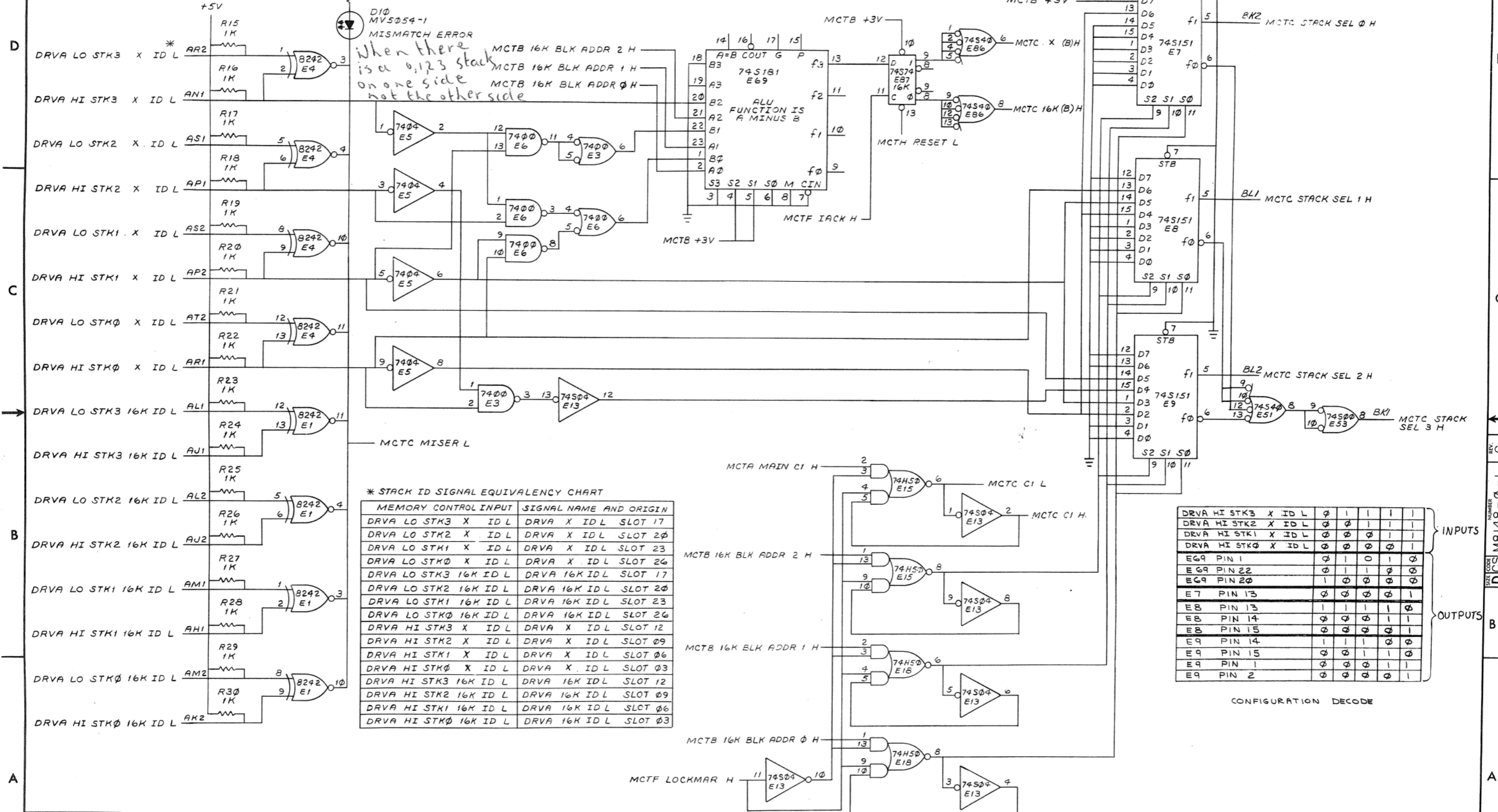
INTERLEAVE	MPXR FUNCTION
H	NORM ADDR <1:3> → 16K BLK ADDR <φ:2> NORM ADDR φ → FICT Aφ2
L	NORM ADDR <φ:2> → 16K BLK ADDR <φ:2> MAIN Aφ2 → FICT Aφ2

\* SWITCHES <S1-1 : S2-2> DEFINE THE UPPER 9 BITS OF THE STARTING ADDRESS OF THE MEMORY CONTROLLER SWITCH CLOSED = φ SWITCH OPEN = 1  
\*\* SEE EQUIVALENCY TABLE ON MCTC FOR SIGNAL SOURCE

REVISIONS		
CHK	CHANGE NO.	REV.



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\* STACK ID SIGNAL EQUIVALENCY CHART

MEMORY CONTROL INPUT	SIGNAL NAME AND ORIGIN
DRVA LO STK3 X ID L	DRVA X ID L SLOT 17
DRVA LO STK2 X ID L	DRVA X ID L SLOT 20
DRVA LO STK1 X ID L	DRVA X ID L SLOT 23
DRVA LO STK0 X ID L	DRVA X ID L SLOT 26
DRVA LO STK3 16K ID L	DRVA 16K ID L SLOT 17
DRVA LO STK2 16K ID L	DRVA 16K ID L SLOT 20
DRVA LO STK1 16K ID L	DRVA 16K ID L SLOT 23
DRVA LO STK0 16K ID L	DRVA 16K ID L SLOT 26
DRVA HI STK3 X ID L	DRVA X ID L SLOT 12
DRVA HI STK2 X ID L	DRVA X ID L SLOT 09
DRVA HI STK1 X ID L	DRVA X ID L SLOT 06
DRVA HI STK0 X ID L	DRVA X ID L SLOT 03
DRVA HI STK3 16K ID L	DRVA 16K ID L SLOT 12
DRVA HI STK2 16K ID L	DRVA 16K ID L SLOT 09
DRVA HI STK1 16K ID L	DRVA 16K ID L SLOT 06
DRVA HI STK0 16K ID L	DRVA 16K ID L SLOT 03

INPUTS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DRVA HI STK3 X ID L	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DRVA HI STK2 X ID L	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
DRVA HI STK1 X ID L	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
DRVA HI STK0 X ID L	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
EG9 PIN 1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
EG9 PIN 22	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
EG9 PIN 20	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0
E7 PIN 13	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
E8 PIN 13	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
E8 PIN 14	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
E8 PIN 15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
E9 PIN 14	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
E9 PIN 15	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
E9 PIN 1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
E9 PIN 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CONFIGURATION DECODE

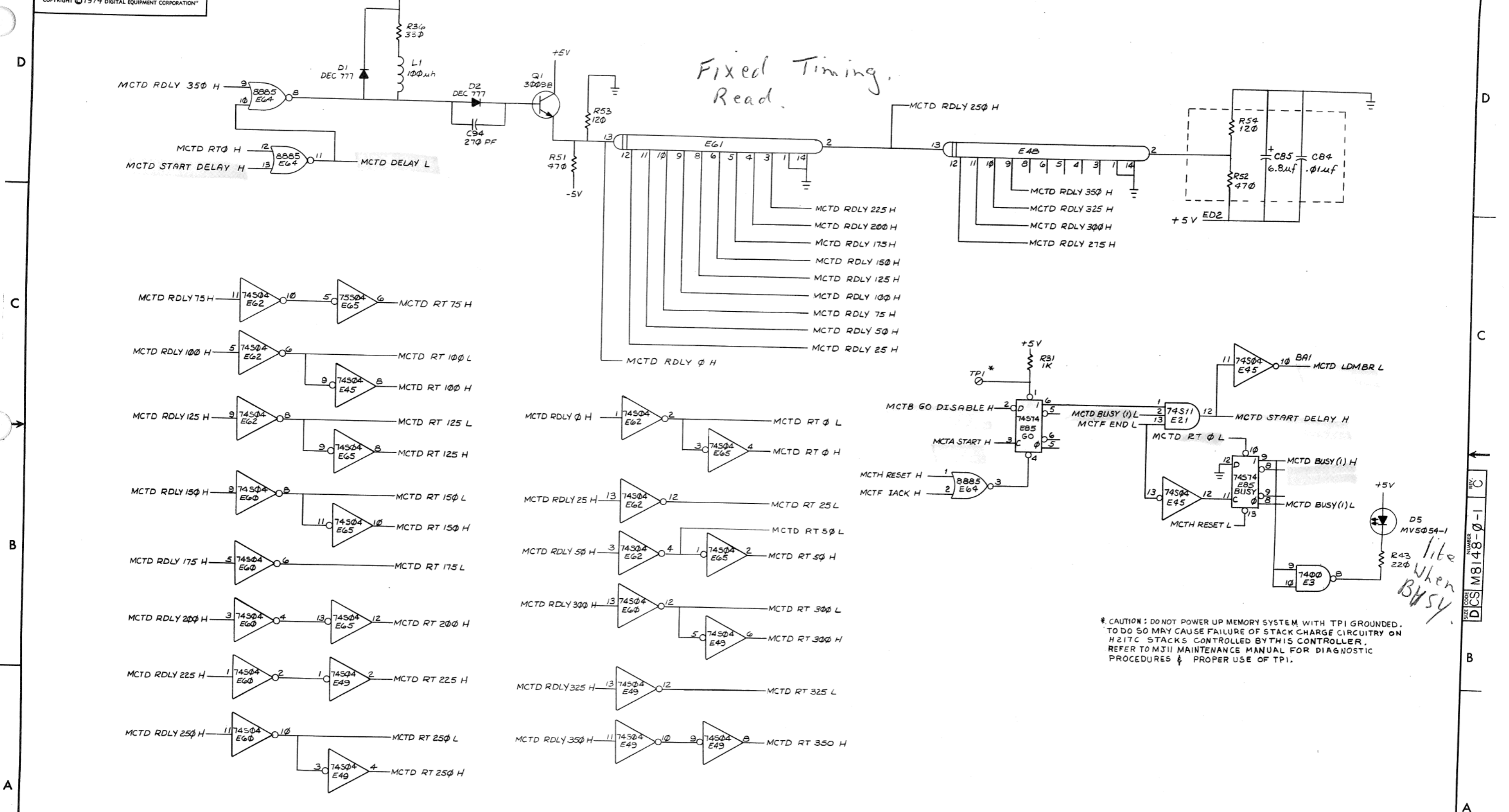
REVISIONS

CHK	CHANGE NO.	REV.

REV. C  
NUMBER M8148-0-1  
SIZE CODE DCS

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Fixed Timing.  
Read.



\* CAUTION: DO NOT POWER UP MEMORY SYSTEM WITH TPI GROUND. TO DO SO MAY CAUSE FAILURE OF STACK CHARGE CIRCUITRY ON H217C STACKS CONTROLLED BY THIS CONTROLLER. REFER TO M311 MAINTENANCE MANUAL FOR DIAGNOSTIC PROCEDURES & PROPER USE OF TPI.

libe  
when  
Busy.

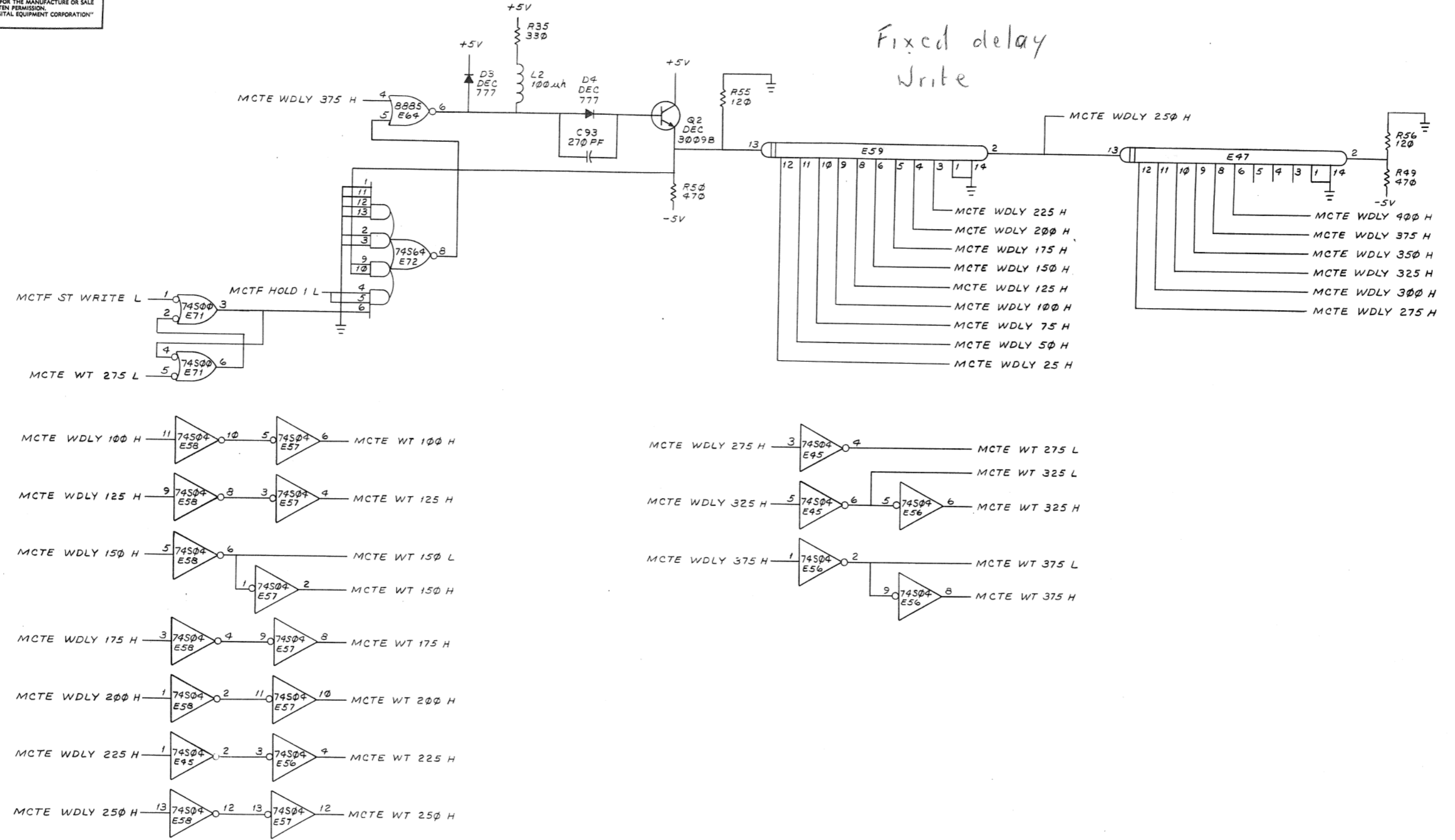
REVISIONS		
CHK	CHANGE NO.	REV.

READ TIMING GENERATOR

TITLE	MEMORY CONTROL AND TIMING (MCTD)	SIZE CODE	DCS	NUMBER	M8148-0-1	REV.	C
SCALE	1/1	SHEET	5	OF 9	DIST.		

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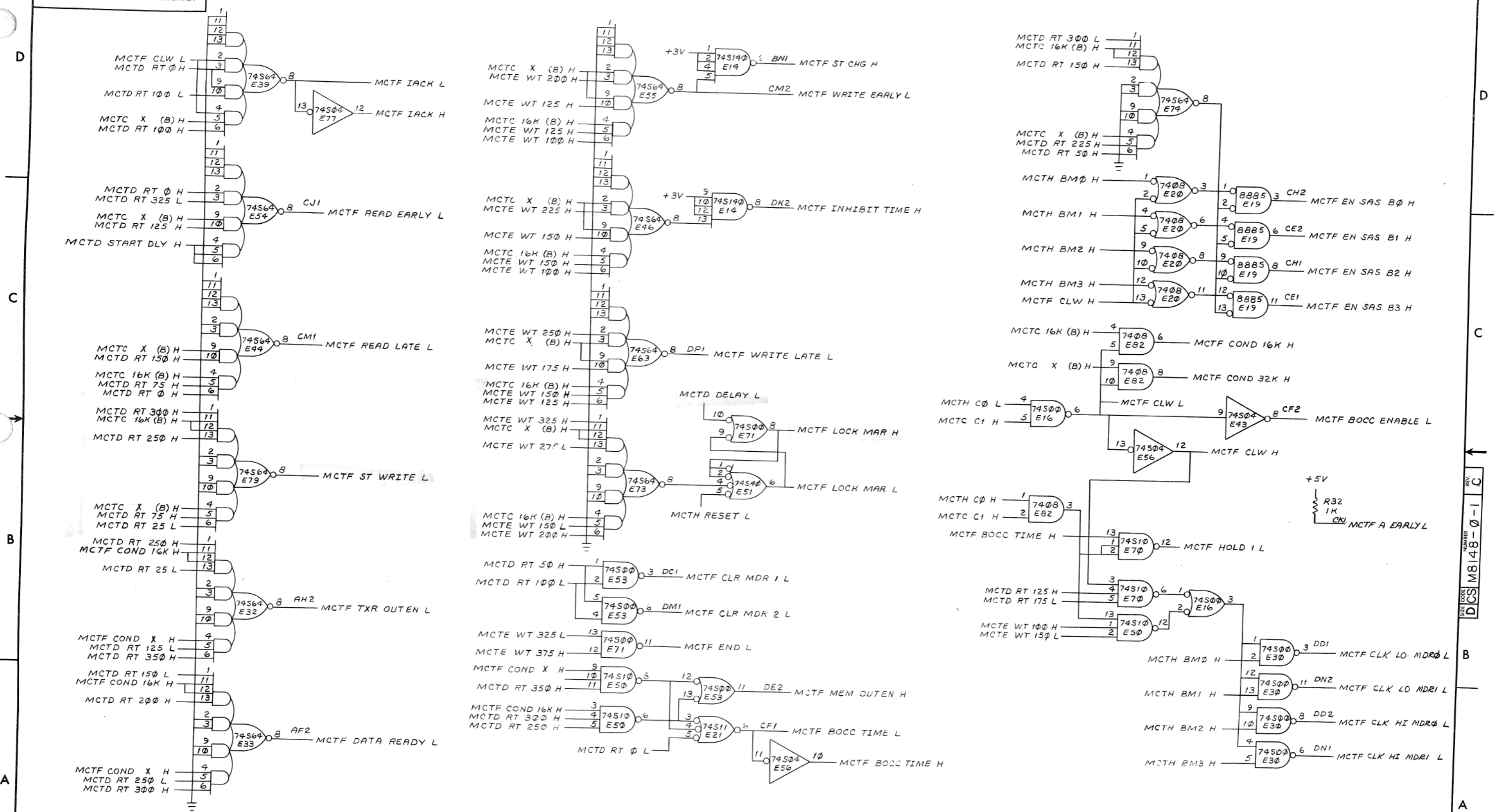
Fixed delay  
Write



REVISIONS		
CHK	CHANGE NO.	REV.

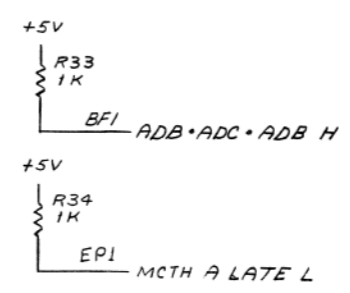
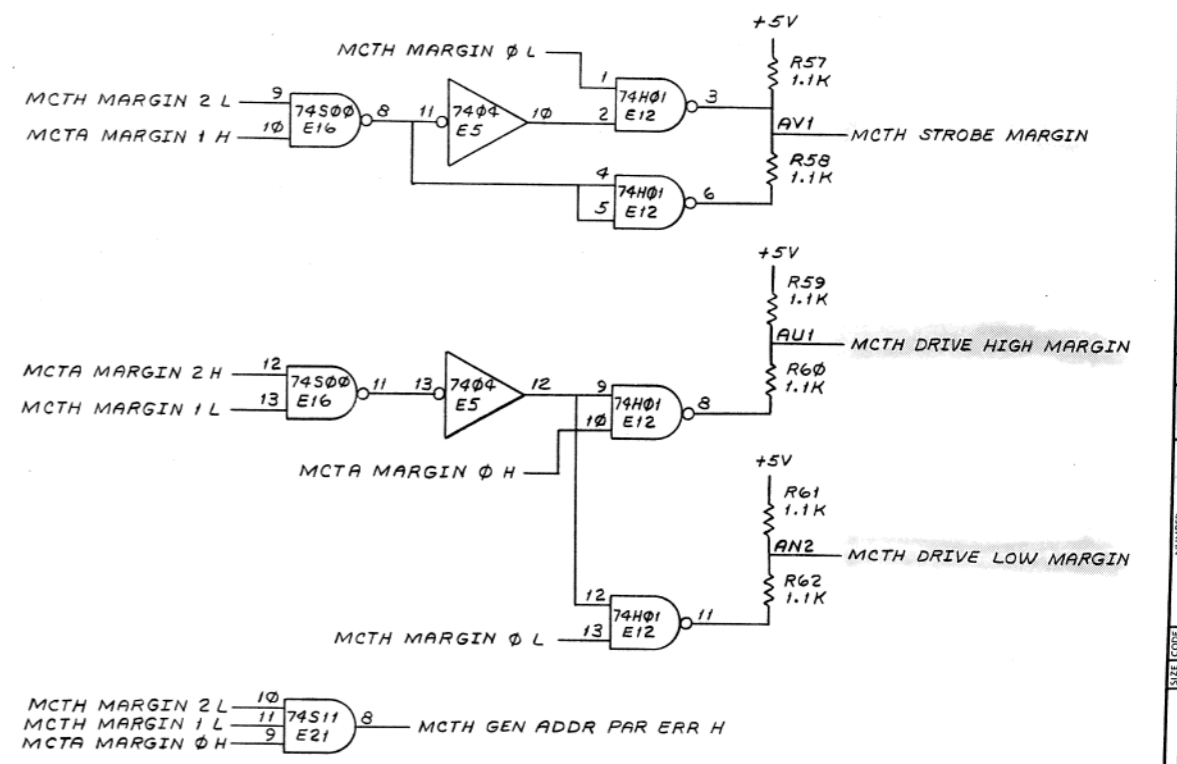
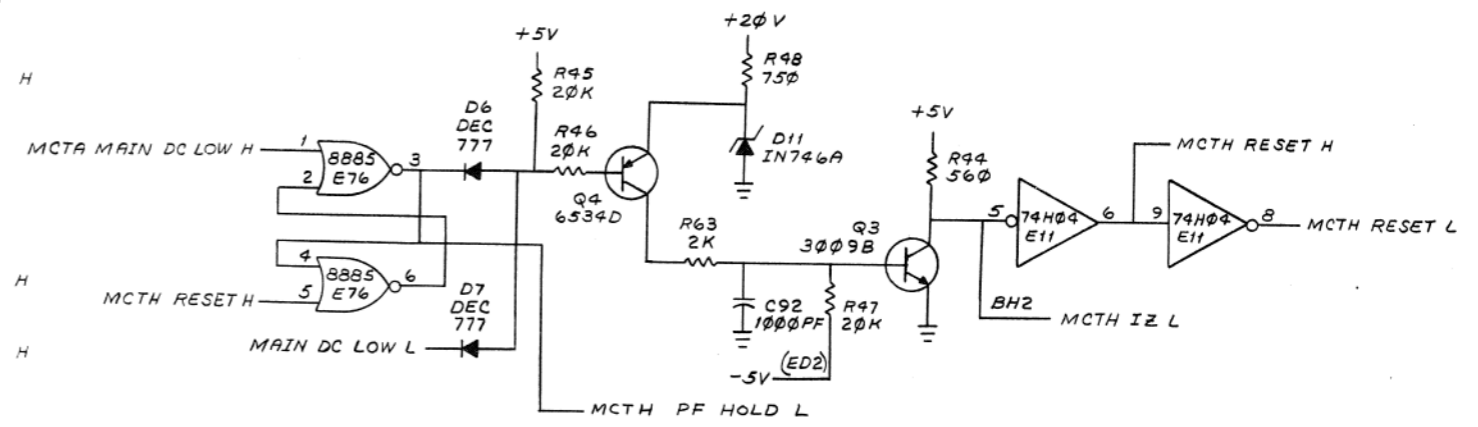
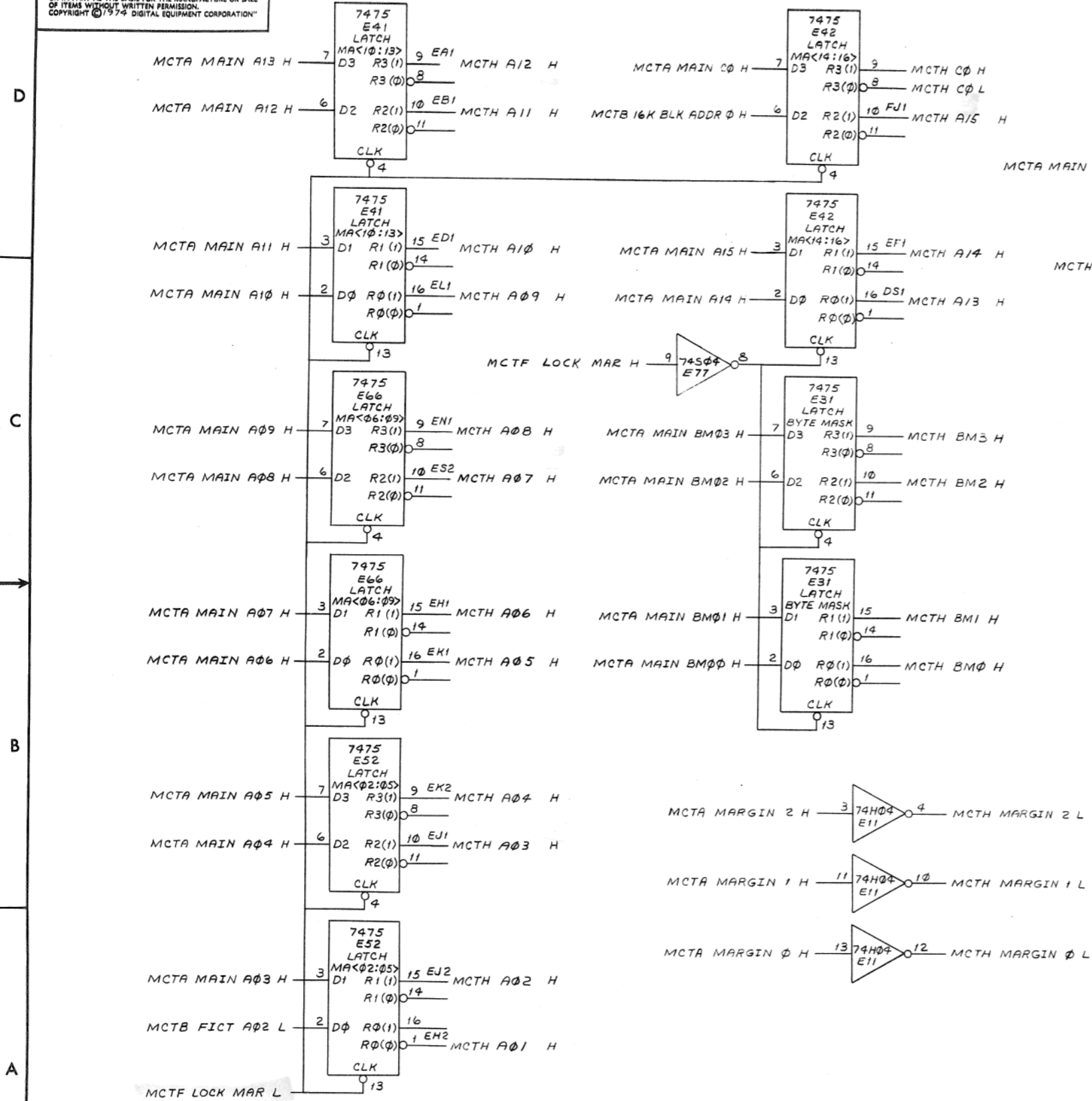
REV. 1-0-8+18W DCS M8148-0-1 C

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REVISIONS		
CHK	CHANGE NO.	REV.

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
MEMORY CONTROL AND TIMING (MCTH)	DCS	M8148-0-1	C
SCALE	SHEET	8 OF 9	DIST.

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x=32k

ROM INPUTS

ROM OUTPUTS

DRVA LO STK 3	X	ID	L	H	H	H	H	H	H	H	L	H	H	H	L	L	L
DRVA LO STK 2	X	ID	L	H	H	H	H	H	H	L	L	H	L	L	H	L	L
DRVA LO STK 1	X	ID	L	H	H	H	H	H	L	L	L	L	H	L	H	L	L
DRVA LO STK 0	X	ID	L	H	H	H	L	L	L	L	L	L	H	L	H	H	L
DRVA LO STK 3	16K	ID	L	H	H	L	H	H	H	L	L	H	H	H	H	H	H
DRVA LO STK 2	16K	ID	L	H	H	L	L	H	H	L	L	H	L	L	L	L	L
DRVA LO STK 1	16K	ID	L	H	L	L	L	H	L	L	L	L	L	L	L	L	L
DRVA LO STK 0	16K	ID	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
E3 PIN 9				L	H	L	H	H	H	H	L	H	L	L	H	L	L
E3 PIN 10				L	L	H	H	L	H	L	H	H	L	L	L	L	H
E3 PIN 11				L	L	L	L	L	L	H	H	L	L	H	H	H	H
E3 PIN 12 (CON EN L)				H	H	H	H	H	H	H	H	H	H	H	H	H	H

NOTE: ALL OTHER COMBINATIONS OF ROM INPUTS RESULT IN ALL OUTPUT PINS LOW

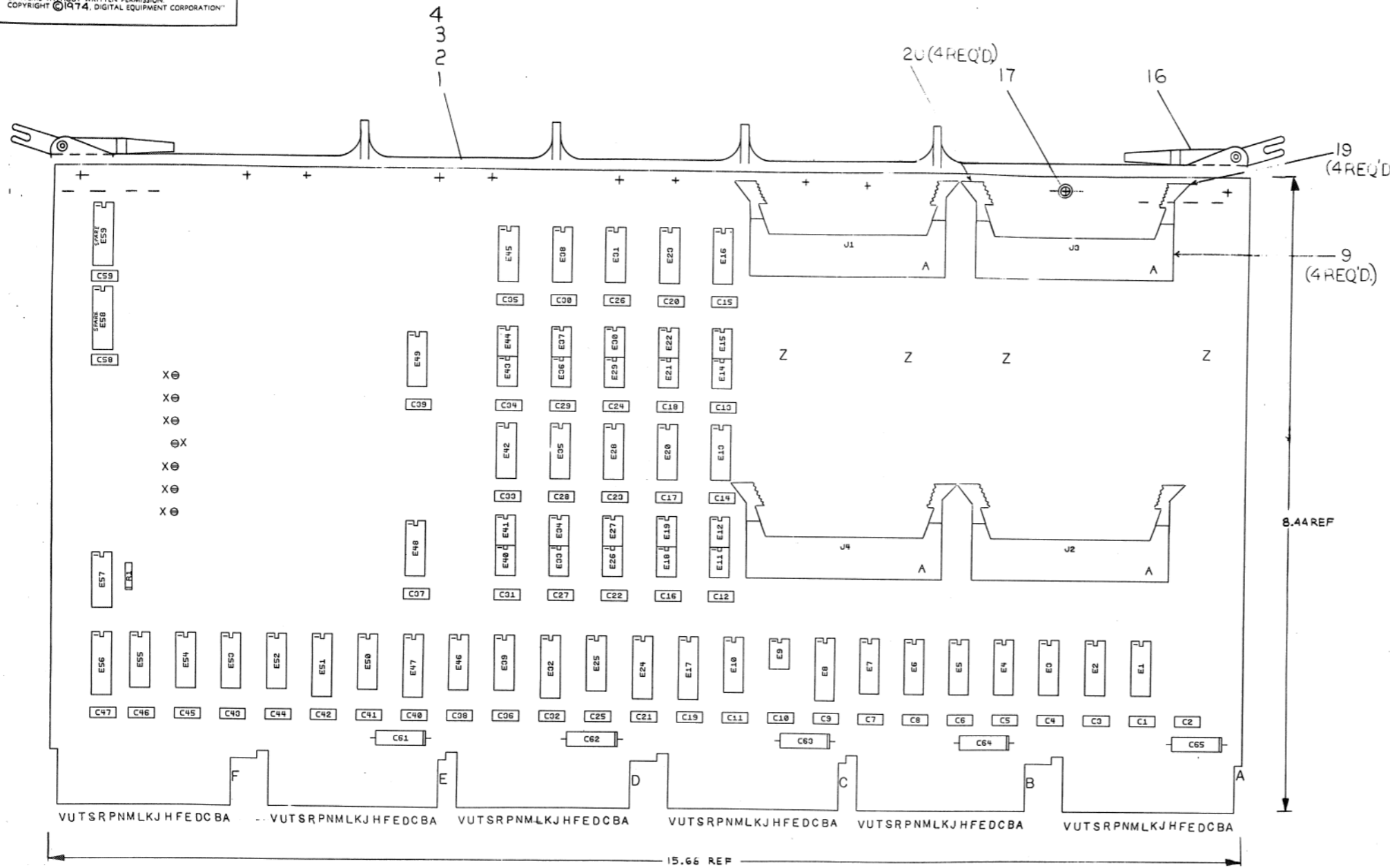
TRUTH TABLE FOR MEM TOP LOOKUP ROM [E3 - MCTB]

REVISIONS		
CHK	CHANGE NO.	REV.

REV. C  
DRAWING NUMBER  
DCS M6148-0-1

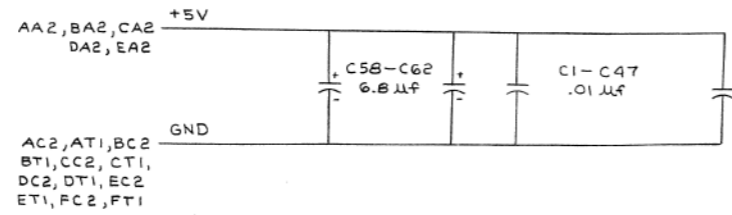
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NOTES: C58 & C59 ARE SPARES



REF	DESCRIPTION	PART NO.	ITEM NO.
REF	X-Y COORDINATE HOLE LOCATION	K-CO-M8149-2-4	1
REF	ASSY/DRILL HOLE LAYOUT	D-AH-M8149-0-5	2
REF	MODULE ECO HISTORY	B-MH-M8149-0-5	3
1	ETCHED CIRCUIT BOARD	5011290	4
5	C61-C65	CAP 6.8 MFD 35V 10%	5
47	C1-C47	CAP .01 MFD 100V	6
1	R1	RES 1K 1/4W 5%	7
7		SPLIT LUG	8
4	J1 THRU J4	RT. ANGLE HEADER, 40 PIN	9
7	E8, E17, E24, E32, E47, E51, E56	IC DEC. 745174	10
10	E2, E3, E5, E6, E25, E29, E50, E52, E54, E57	IC DEC. 74H01-1	11
20	E11, E12, E14, E15, E18, E19, E21, E22, E26, E27, E29, E30, E33, E34, E36, E37, E40, E41, E43, E44	IC DEC. 75452	12
9	E1, E4, E7, E10, E46, E48, E49, E55, E53	IC DEC. 74904	13
10	E13, E16, E20, E23, E28, E31, E35, E38, E42, E45	IC D.E.C. 8640	14
1	E9	IC D.E.C. 75453	15
1		HANDLE ASSY	16
12		EYELETS, G5-47	17
			18
4		RT. ANGLE HEADER 40 PIN LATCH LEFT	19
4		RT. ANGLE HEADER 40 PIN LATCH RIGHT	20

IC DEC	QTY	REF
IC DEC 75453	4	8
IC DEC 8640	1	8
IC DEC 75452	4	8
IC DEC 745174	8	16
IC TYPE	GND	+5V



REV	DATE	BY	CHK	CHANGE NO.
1	12/11/73	E. CLARK		
2	1/23/74			
3	1/23/74			
4	1/23/74			
5	1/23/74			
6	1/23/74			
7	1/23/74			

FIRST USED ON OPTION MODEL  
11/70

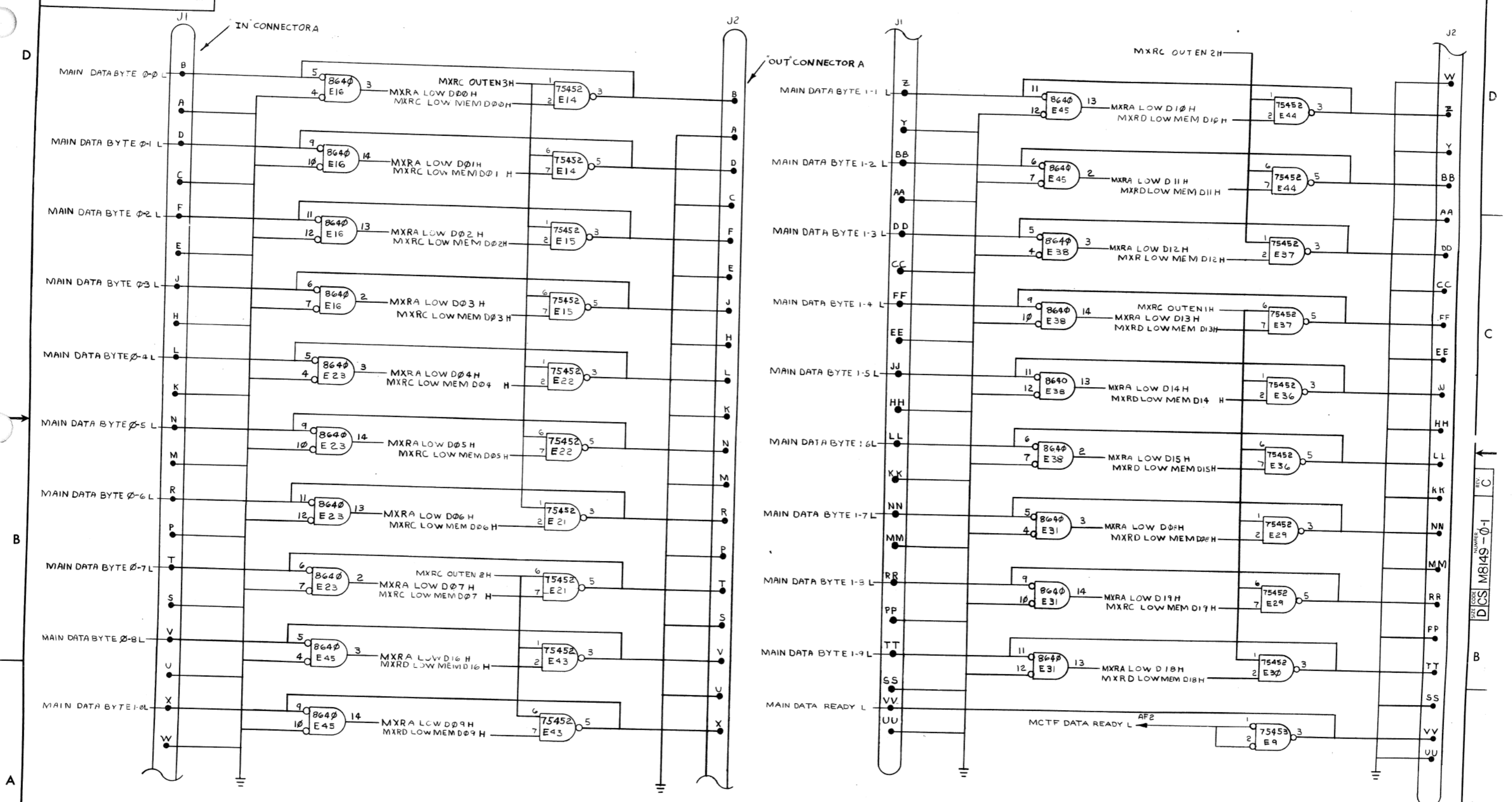
DEC NO.	EIA NO.	DEC NO.	EIA NO.

DRN	Shallen	DATE	11/3/74
CHK'D		DATE	12/2/74
ENG		DATE	12/16/74
PRG. ENG.		DATE	12/16/74
PROD.		DATE	12/16/74
NEXT HIGHER ASSY			
MJI1-AY			
SCALE	1/1	SIZE CODE	D
SHEET	1 OF 5	DIST.	

digital EQUIPMENT CORPORATION  
TITLE: MEMORY TRANS-CEIVER CARD (MXR)  
NUMBER: DCS M8149-0-1  
REV. C

SEMICONDUCTOR CONVERSION CHART

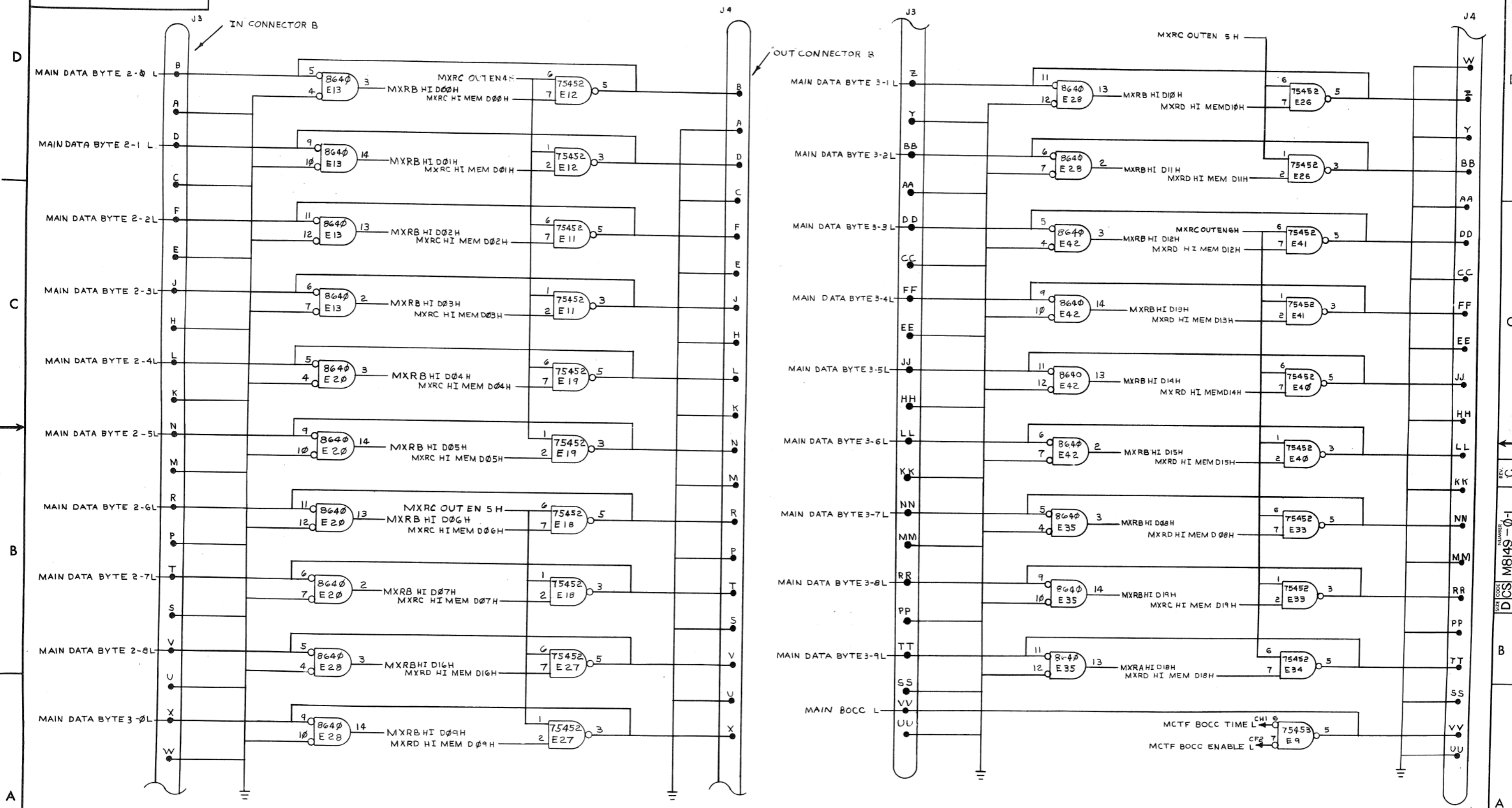
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REVISIONS	
CHK	CHANGE NO



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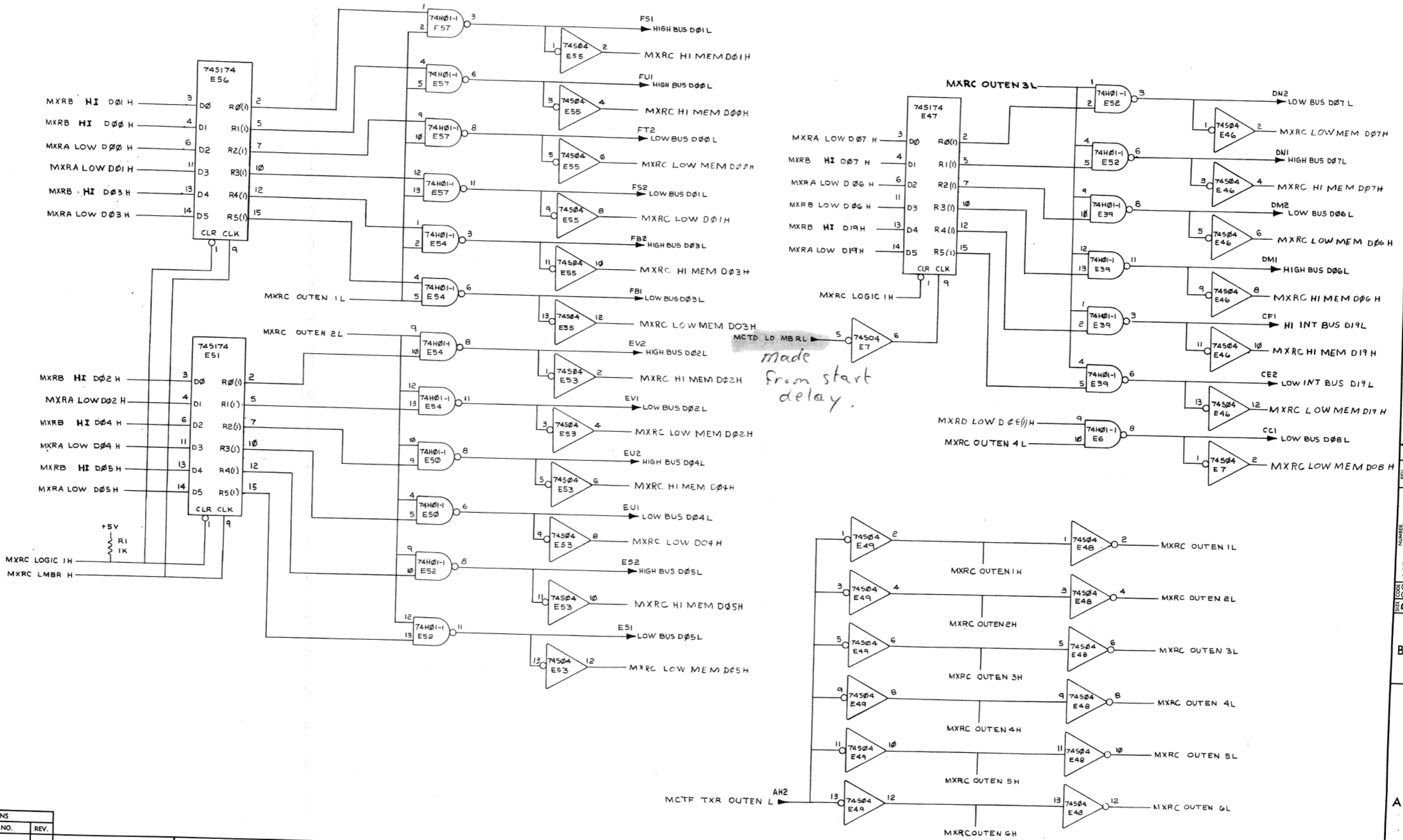


REVISIONS		
CHK	CHANGE NO.	REV.

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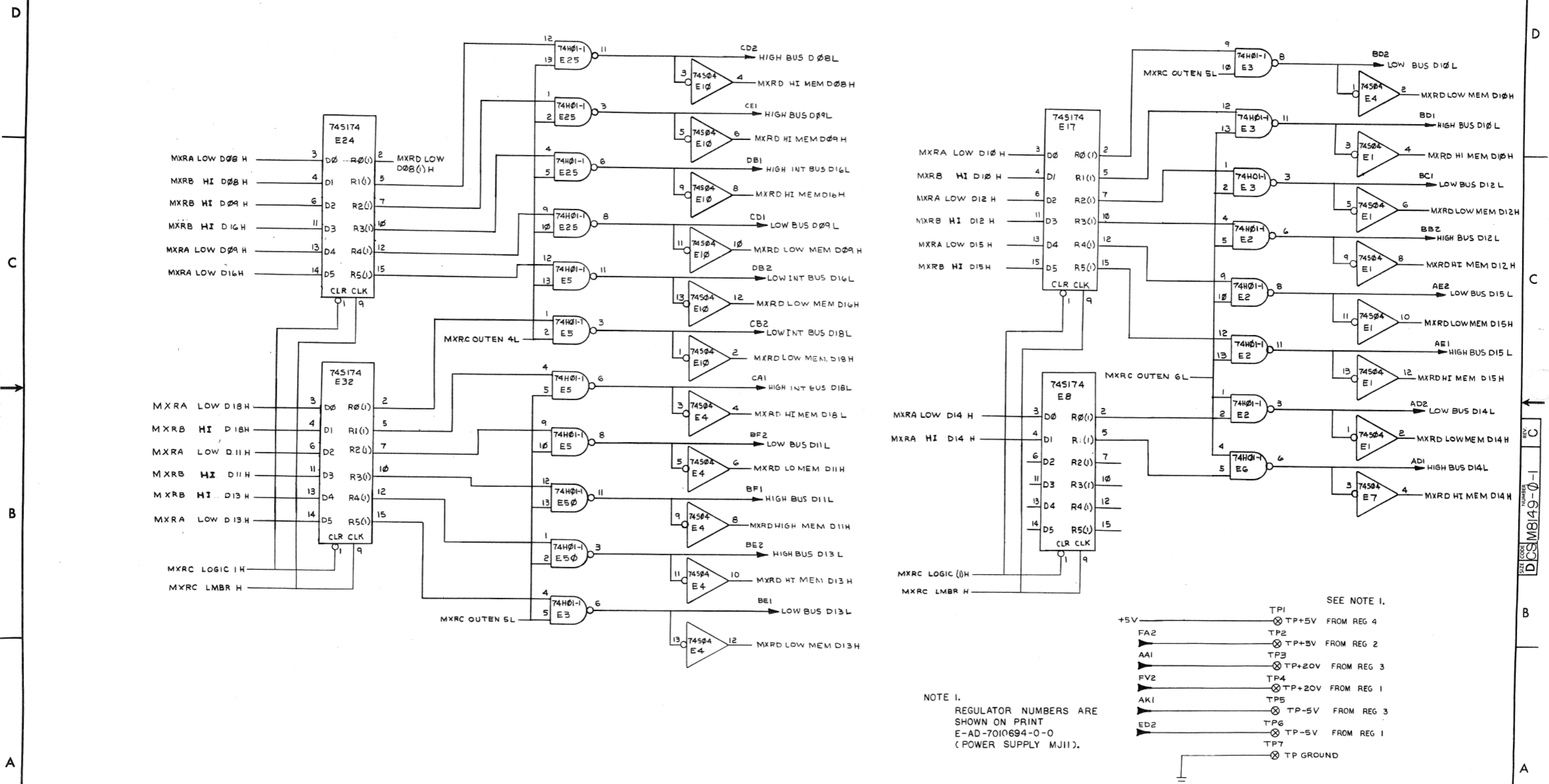
D  
C  
B  
A

D  
C  
B  
A

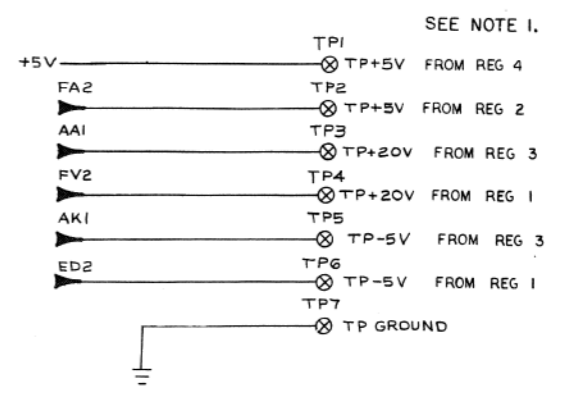


REVISIONS		
CHK	CHANGE NO.	REV.

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NOTE 1.  
REGULATOR NUMBERS ARE SHOWN ON PRINT  
E-AD-7010694-0-0  
(POWER SUPPLY MJ11).



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	MEMORY (MXRD)	SIZE CODE	NUMBER	REV.
TRANSCEIVER CARD		D	CS M8149-0-1	C
SCALE	---	SHEET	5 OF 5	DIST.