

PAGE REVISION CONTROL SHEET


SH NO.	PAGE REVISIONS										REMARKS
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1	A	B	C								
2	A	B	C								
3	A	B	C								
4	A	B	C								
5	A	B	C								
6	A	B	C								
7	A	B	C								
8	A	B	C								
9	A	B	C								
10	A	B	C								

DATE	ENG.	ETCH REV.	ECD NO.	ORIG.
9/27/73	Mod	B	00001	
11/16/73	Mod	B	00002	

FIRST USED ON OPTION/MODEL
MM11 - U

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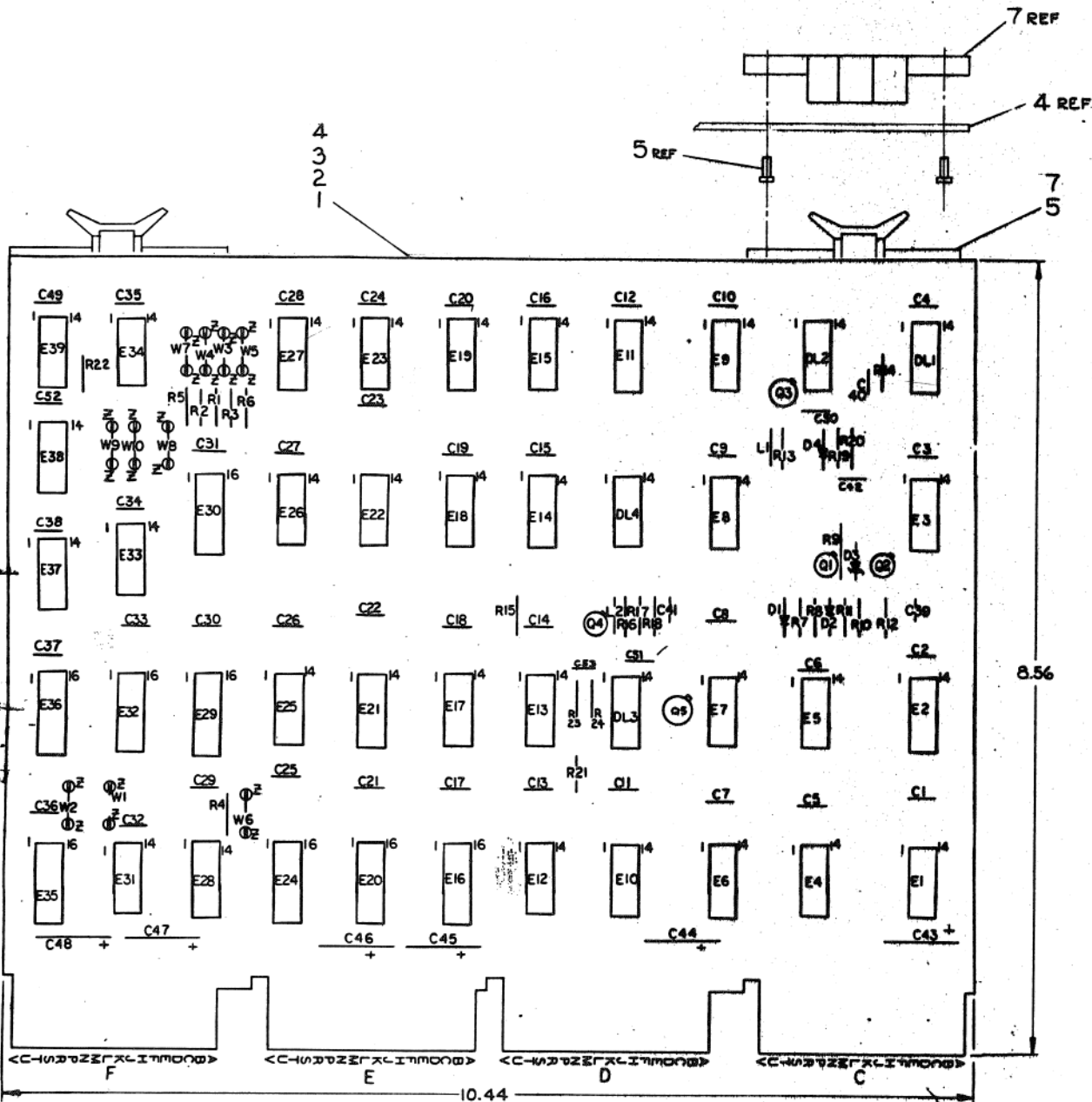
DRN. W. MAJOR	DATE 5/10/73	 EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
CHK'D W. MAJOR	DATE 5/10/73	
ENG. D. Dunbar	DATE 5/10/73	
PROJ. ENG. D. Dunbar	DATE 5/10/73	
PROD. R. Schmitt	DATE 5/10/73	
TITLE: 16K UNIBUS TIMING		

NEXT HIGHER ASSY.
B-DD-MM-11-U

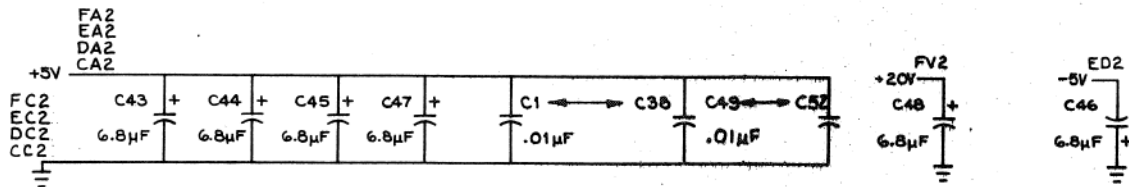
SIZE	CODE	NUMBER	REV.
B	CS	M8293-Ø-1	C

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NOTES: 1. UNLESS OTHERWISE SPECIFIED: RESISTANCE IS IN OHMS, CAPACITANCE IS IN MICROFARADS.



7483	12	5
7485	8	16
380	1	8
7475	12	5
IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTS ARE STATED ABOVE		
IC PIN LOCATIONS		



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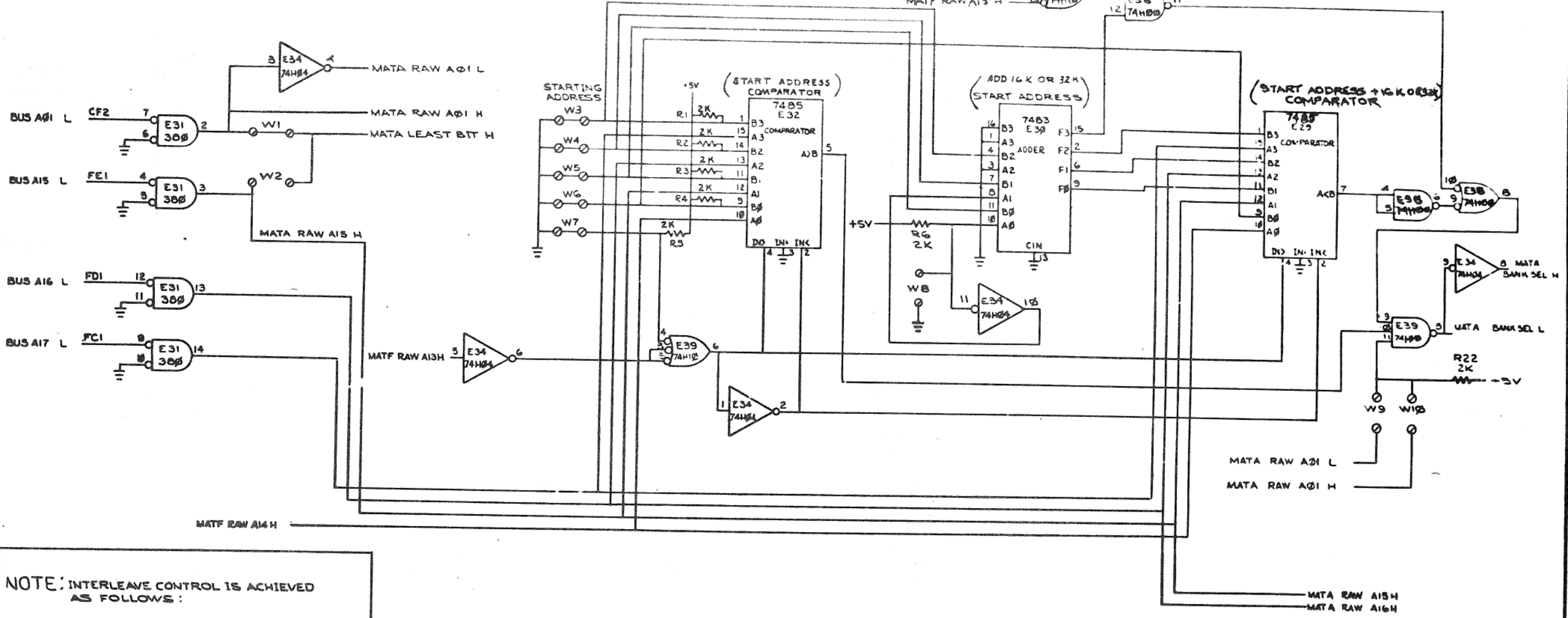
DEC FORM NO. DRD-135A

REF	XY COORDINATE	HOLE LOCATION	K-CO-M8293-0-4	1
REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M8293-0-5		2
REF	MODULE ECO HISTORY	B-MH-M8293-0-6		3
1	ETCHED CIRCUIT BOARD	5010473		4
8	EYELET GS-4-7	9006732		5
20	SPLIT LUGS	9006735		6
4	HANDLE FLIP-CHIP MAGENTA	9008337-6		7
2	C40, C41	CAP 82 PF 100V ±5% DM	1000015	8
1	C39	CAP 1000 PF 100V ±5% DM	1000042	9
43	C1 → 38, 42, 49-52	CAP .01 μF 50V ±20%	1001610	10
6	C43 → 48	CAP 6.8 μF 35V ±10% S, TANT	1005306	11
1	D3	DIODE 1N746A 3.6V ±5% ZENER	1104860	12
3	D1, 2, 4	DIODE D672	1105275	13
3	R13, 14, 18	RES 100 1/4 W 5%	1300229	14
1	R17	RES 120 1/4 W 5%	1300247	15
1	R9	RES 750 1/2 W 5%	1300354	16
1	R16	RES 1K 1/4 W 5%	1300365	17
10	R1 → 6, 10, 21, 15, 22	RES 2K 1/4 W 5%	1302388	18
3	R7, 11, 8	RES 20K 1/4 W 5%	1302391	19
2	R19, 12	RES 560 1/4 W 5%	1301890	20
1	R20	RES 33K 1/4 W 10%	1300510	21
1	Q1	TRANSISTOR DEC 6534 D	1503409	22
4	Q2, 3, 4, 5	TRANSISTOR DEC 3009 B	1503100	23
2	L1, 2	INDUCTOR 100 μH	1610662	24
4	DL1, 2, 3, 4	DELAY LINE 250 NS, TAPPED	1611243	25
1	E28	IC DEC 74H40	1905586	26
5	E20, 24, 16, 36, 35	IC DEC 7475	1909050	27
6	E15, 8, 26, 18, 37, 38	IC DEC 74H00	1909056	28
4	E14, 19, 1, 39	IC DEC 74H10	1909057	29
2	E21, 33	IC DEC 74H50	1909060	30
2	E11, 25	IC DEC 74H53	1909062	31
2	E23, 27	IC DEC 74H55	1909063	32
6	E31, 4, 6, 17, 7, 5	IC DEC 380	1909485	33
4	E9, 22, 13, 34	IC DEC 74H04	1909931	34
1	E30	IC DEC 7483	1909932	35
2	E29, 32	IC DEC 7485	1910224	36
2	E3, 10	IC DEC 8885	1910649	37
2	E2, 12	IC DEC 7427	1910878	38
2	R23, 24	RES 330 1/4 W 5%	1300298	39
1	C53	CAP 120 PF 100V ±5% D.M.	1000018	40

FIRST USED ON OPTION MODEL		PARTS LIST	
MMII-U		ETCH BOARD REV B	
DRN. B. VALENTINE	DATE 1-29-73	digital EQUIPMENT CORPORATION	
CHK'D. W. MAJOR	DATE 5/10/73	MAYNARD, MASSACHUSETTS	
ENG. D. SHOLAN	DATE 5/16/73	TITLE 16K UNIBUS TIMING	
PRD. ENG. R. SCHUBERT	DATE 5/19/73	REV. C	
PROD. R. SCHUBERT	DATE 5/10/73	NEXT HIGHER ASSY B-DD-MMII-U	
DEC NO.	EIA NO.	DEC NO.	EIA NO.
SEMICONDUCTOR CONVERSION CHART			
SCALE	OF 12	DIST.	

DEVICE SELECTION

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NOTE: INTERLEAVE CONTROL IS ACHIEVED AS FOLLOWS:

- a) NON-INTERLEAVED
W1 IN
W2, W6, W7 IN; W3, W4, W5 OUT
- b) INTERLEAVED
W1 OUT
W2, W6 IN
W3 IN } ONE MEMORY
W4, W5 OUT }
W7 OUT } THE OTHER MEMORY
W3, W4 IN }

STARTING ADDRESS FOR THE COMBINED INTERLEAVED MEMORY IS THE SAME AS FOR THE NON-INTERLEAVED CASE (W3, W4, W5, W6, W7 MUST BE CUT THE SAME FOR BOTH INTERLEAVED MEMORIES) BUT THE INTERLEAVED MAX ADDRESS IS INCREASED BY 16K (10000000).

NON-INTERLEAVED START ADDRESS	W3	W4	W5	W6	W7	NON-INTERLEAVED MAX ADDRESS
000000 (0K)	0 IN	0 IN	0 IN	0 IN	0 IN	077776
020000 (4K)	0 IN	0 IN	0 IN	0 IN	1 OUT	117776
040000 (8K)	0	0	0	1	0	137776
060000 (12K)	0	0	0	1	1	157776
100000 (16K)	0	0	1	0	0	177776
120000 (20K)	0	0	1	0	1	217776
140000 (24K)	0	0	1	1	0	237776
160000 (28K)	0	0	1	1	1	257776
200000 (32K)	0	1	0	0	0	277776
220000 (36K)	0	1	0	0	1	317776
240000 (40K)	0	1	0	1	0	337776
260000 (44K)	0	1	0	1	1	357776
300000 (48K)	0	1	1	0	0	377776
320000 (52K)	0	1	1	0	1	417776
340000 (56K)	0	1	1	1	0	437776
360000 (60K)	0	1	1	1	1	457776
400000 (64K)	1	0	0	0	0	477776

* THE MEMORY WILL NOT RESPOND TO BUS ADDRESSES BETWEEN 124-128K

	W3	W4	W5	W6	W7	
420000 (68K)	0	0	0	0	1	517776
440000 (72K)	0	0	0	1	0	537776
460000 (76K)	1	0	0	1	1	557776
500000 (80K)	1	0	1	0	0	577776
520000 (84K)	1	0	1	0	1	617776
540000 (88K)	1	0	1	1	0	637776
560000 (92K)	1	0	1	1	1	657776
600000 (96K)	1	1	0	0	0	677776
620000 (100K)	1	1	0	0	1	717776
640000 (104K)	1	1	0	1	0	737776
660000 (108K)	1	1	0	1	1	757776
700000 (112K)	1	1	1	0	0	757776
720000 (116K)	1	1	1	0	1	757776
740000 (120K)	1	1	1	1	0	757776

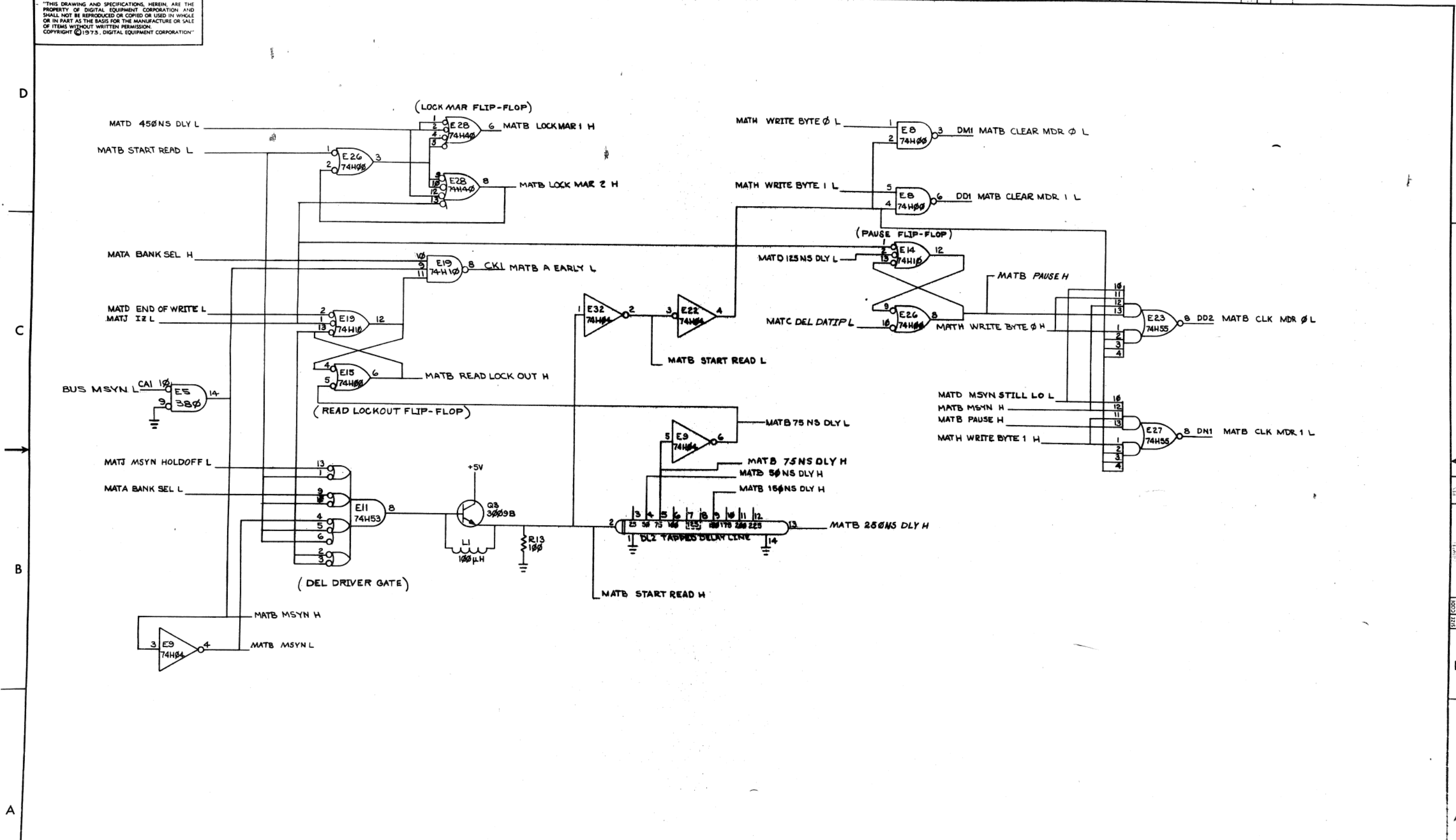
DEVICE SELECTION LOGIC

REV	CHK	CHANGE NO	REV

DCS M8293-0-1

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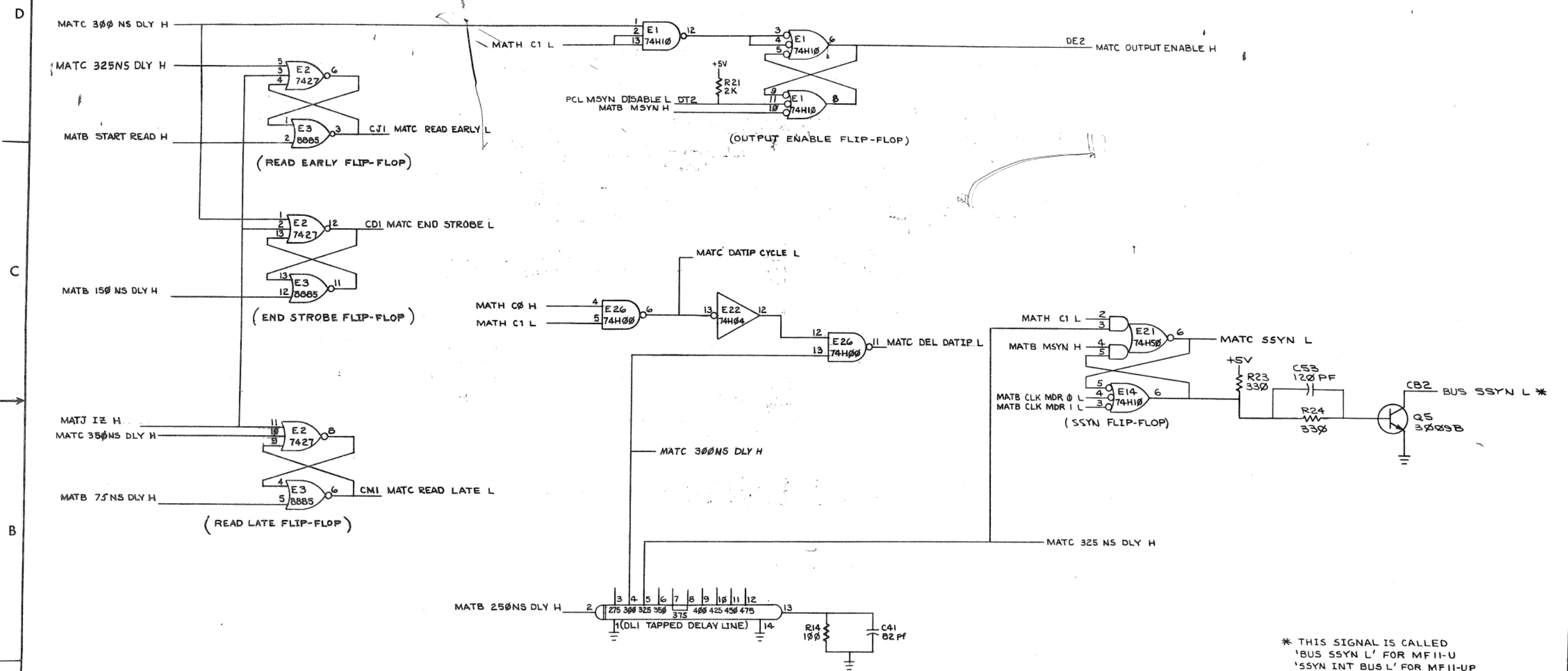
1-0-2628... 2



REVISIONS		
CHK	CHANGE NO	REV

READ START TIMING
 UNIBUS TIMING
 MATE
 DCS M8293

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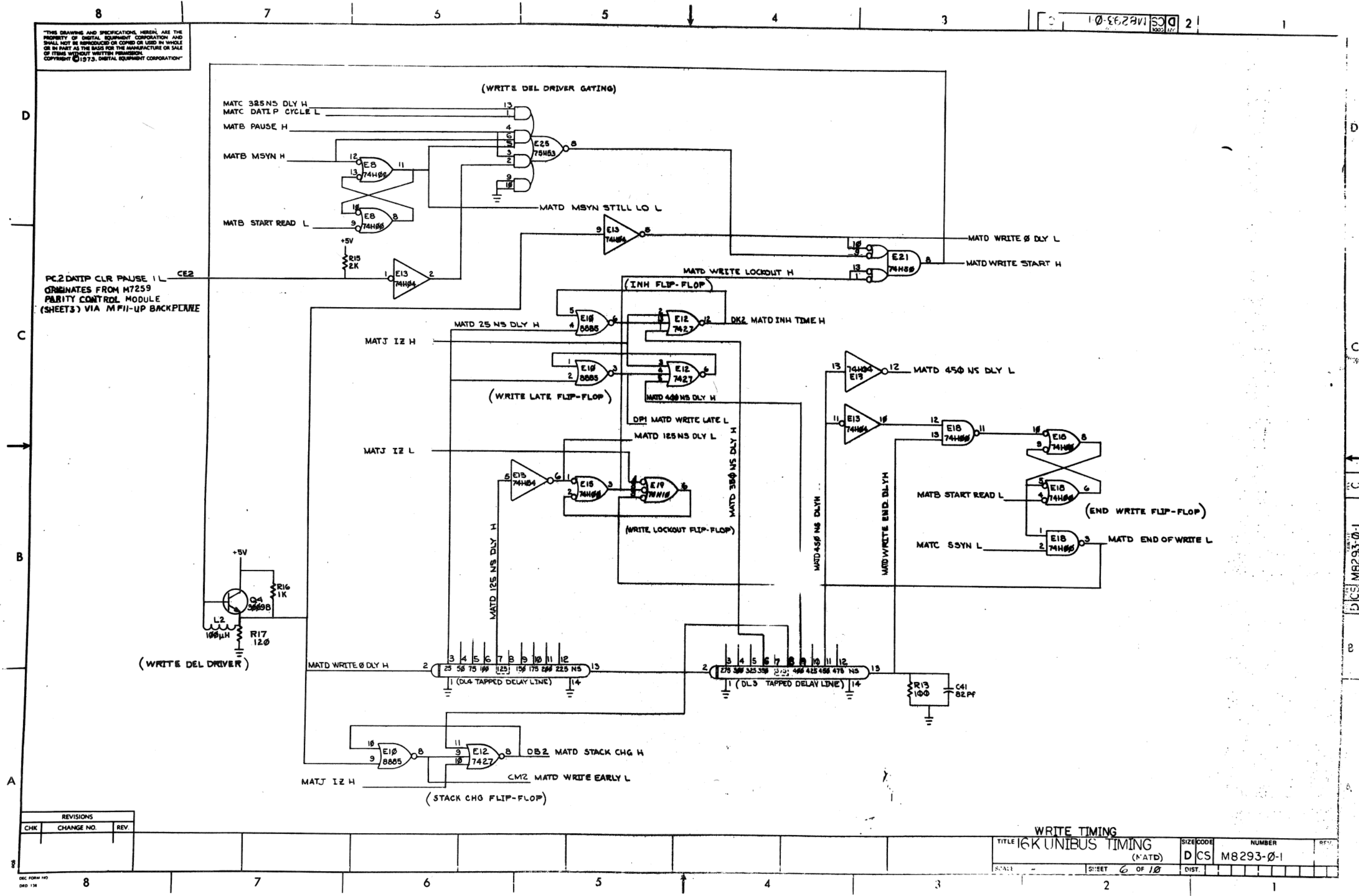


* THIS SIGNAL IS CALLED 'BUS SSYN L' FOR MF11-U 'SSYN INT BUS L' FOR MF11-UP

REVISIONS		
CHK	CHANGE NO	REV

TITLE		SIZE CODE	NUMBER	REV.
CLOCK UNIBUS TIMING (MATC)		DCS	M8293-0-1	C
SCALE	SHEET	OF		
	5	70		

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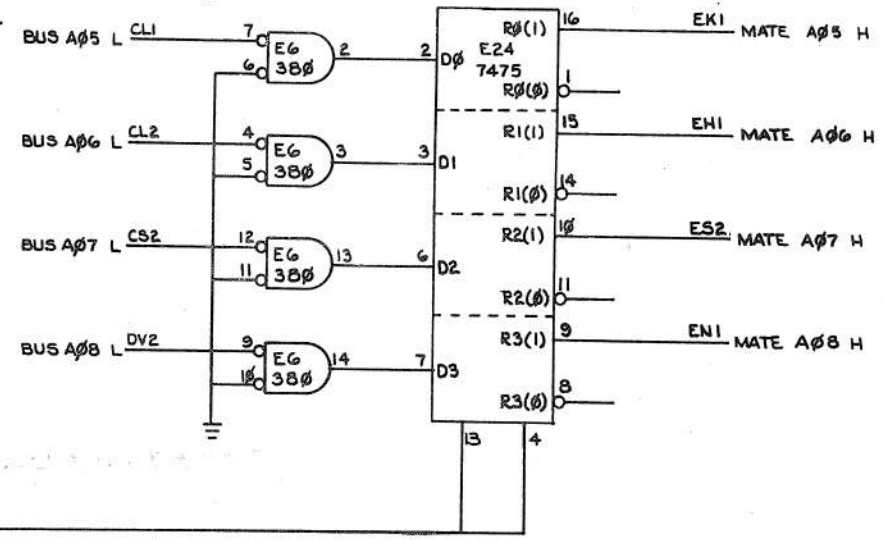
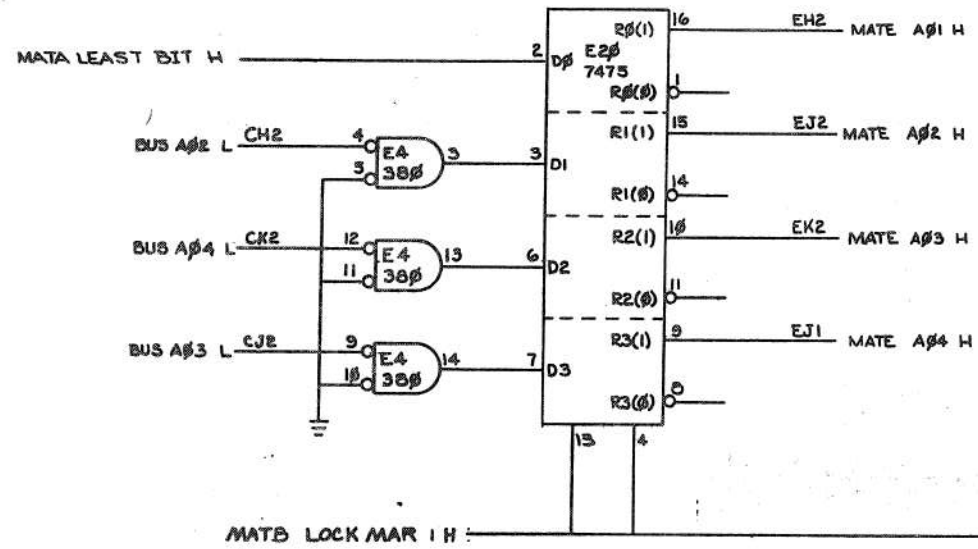


REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		WRITE TIMING		SIZE CODE		NUMBER		REV.	
16K UNIBUS TIMING		(MATD)		DCS		M8293-0-1			
SCALE		SHEET 6 OF 10		DIST.					

DCS M8293-0-1

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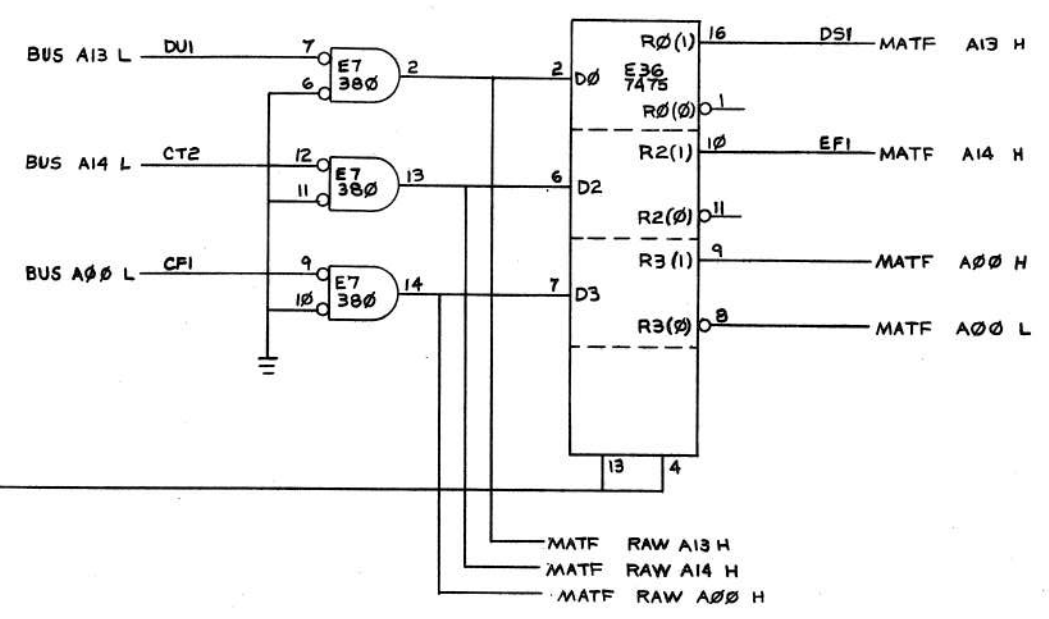
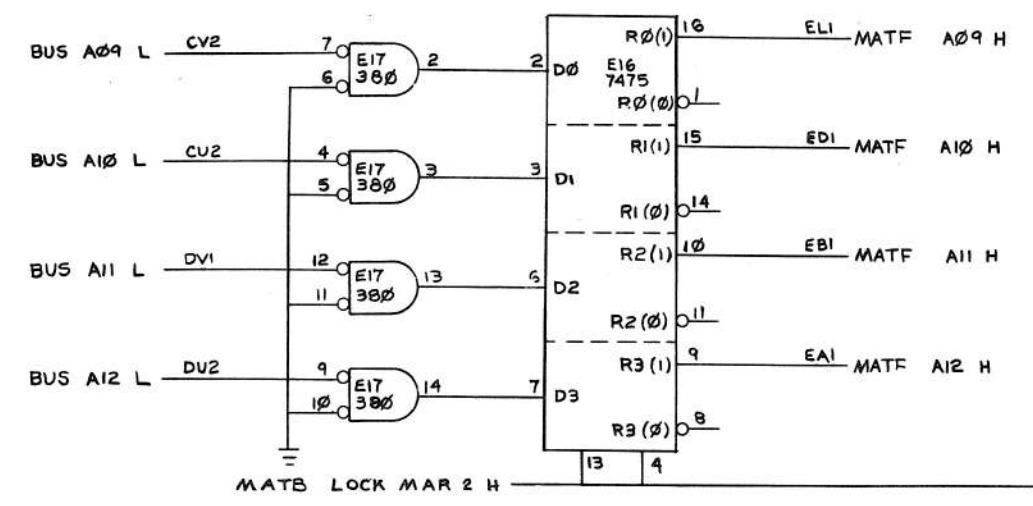


REVISIONS		
CHK	CHANGE NO	REV.

TITLE		SIZE CODE	NUMBER	REV.
A01-A08 LATCHES		DCS	M8293-0-1	C
SUBTITLE		DIST	DATE	
16k UNIBUS TIMING (MATE)			7 05 73	

DCS M8293-0-1

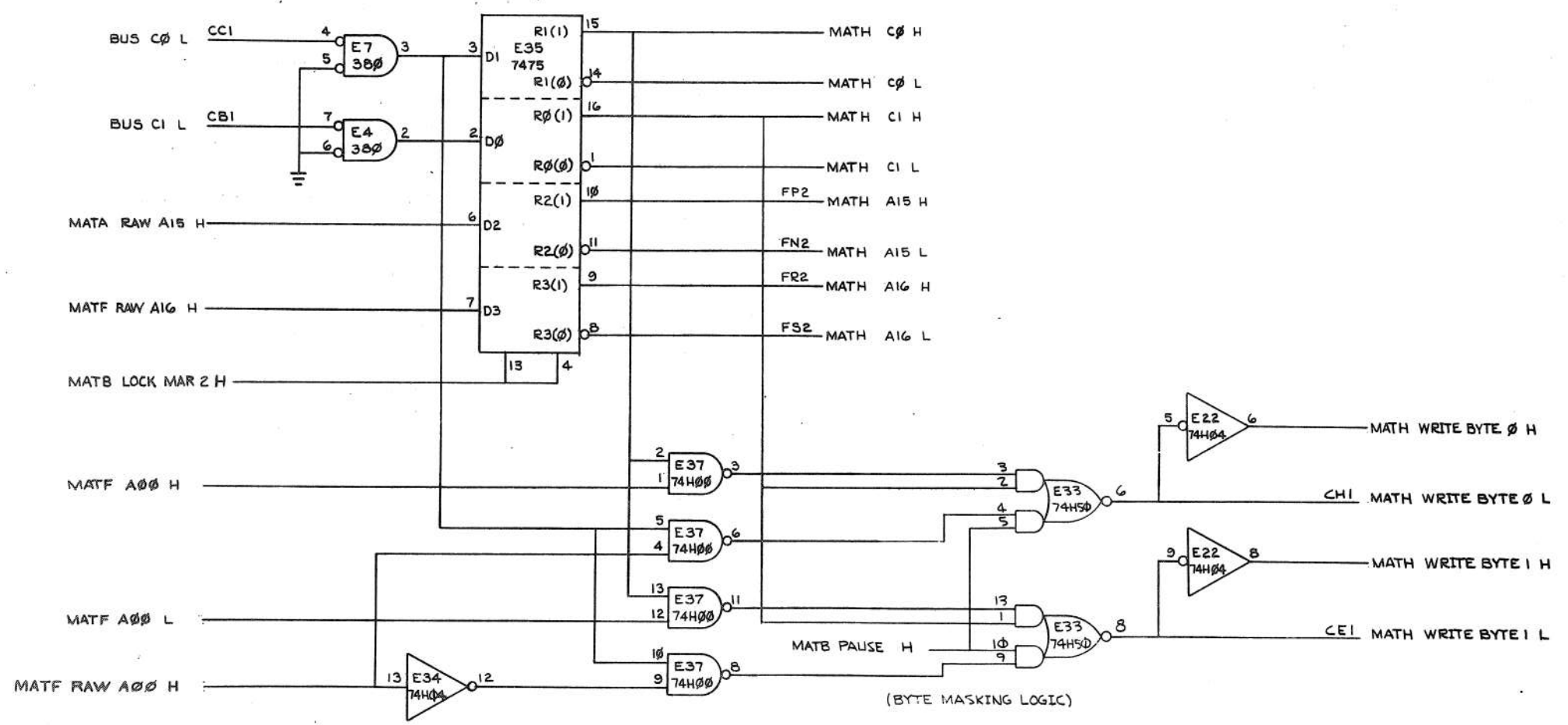
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D
C
B
A

D
C
B
A

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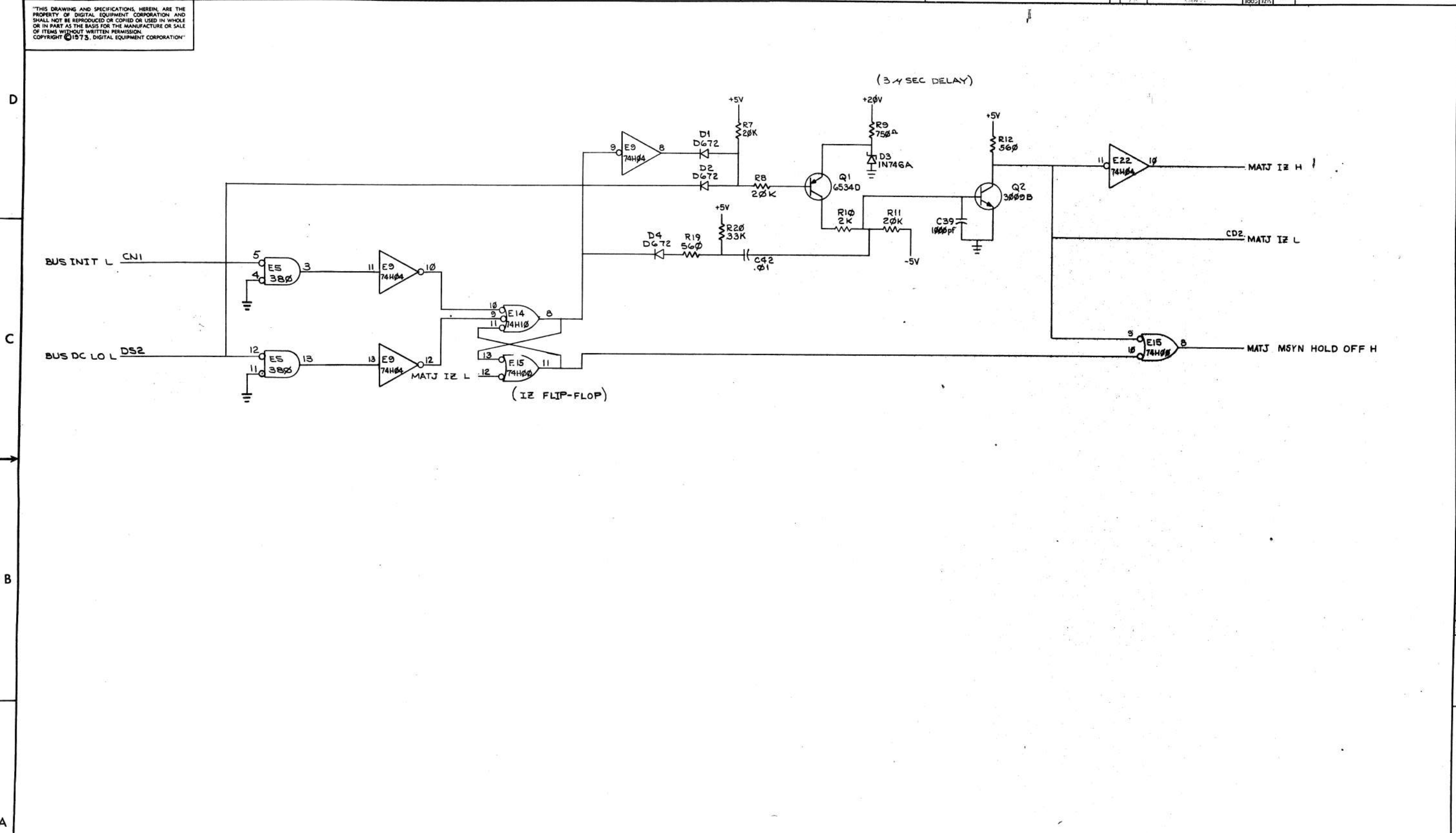


REVISIONS		
CHK	CHANGE NO	REV.

DCS M8293-0-1

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DCS M8293-0-1 2



REVISIONS		
CHK	CHANGE NO.	REV.

TITLE: INIT & DCLO INITIALIZING		SIZE: DCS	NUMBER: M8293-0-1	REV. C
TITLE: 16K UNIBUS TIMING (MATJ)		SCALE: ---	SHEET: 10 OF 10	DIST.:

DCS M8293-0-1 C