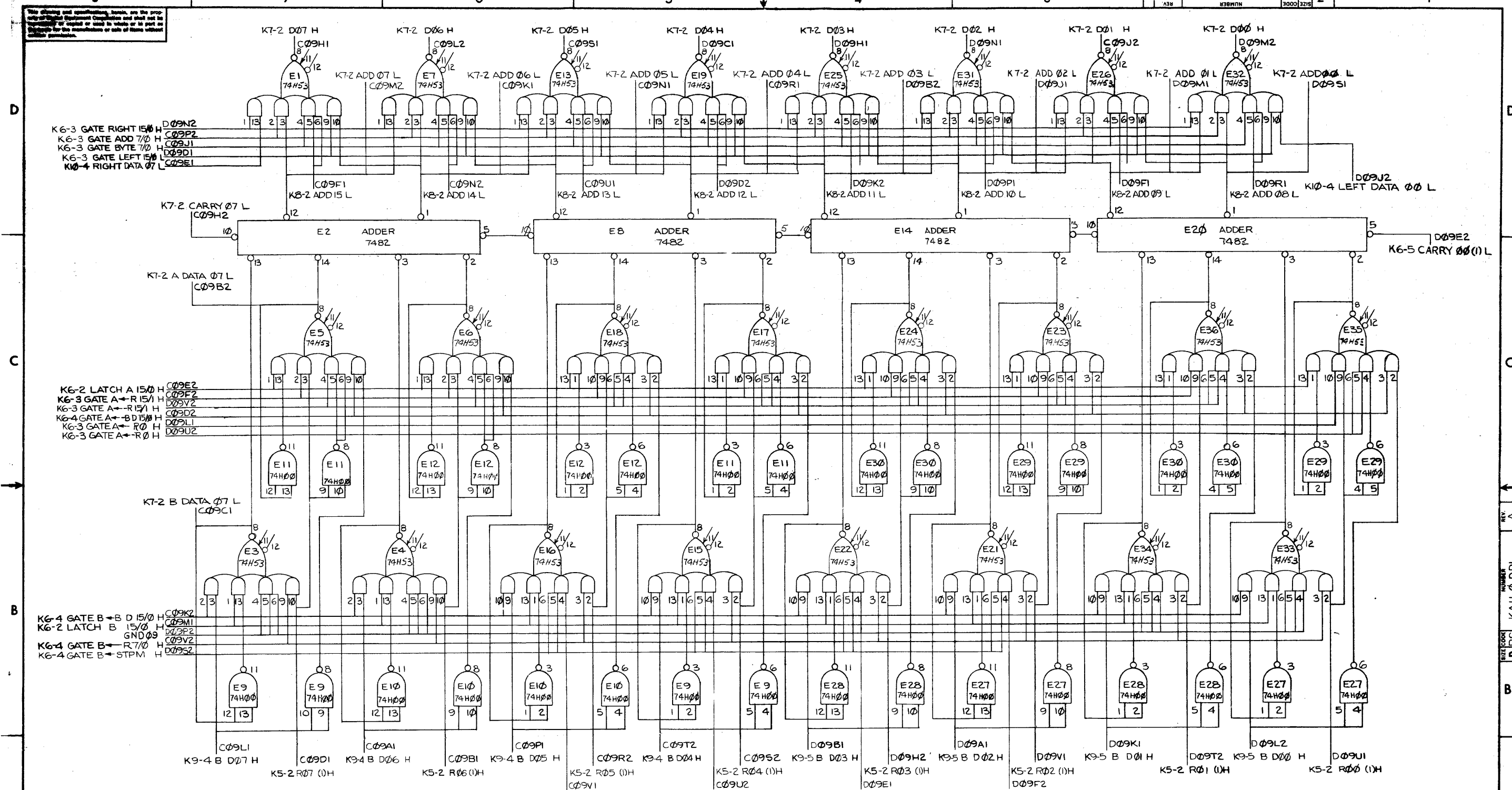


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REV	NO	DATE	BY
1	1	12-21-69	J.P.P.
2	1	1-21-70	J.P.P.

FIRST USED ON OPTION MODEL PDP11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED				
DIMENSION IN INCHES				
TOLERANCES				
DECIMALS: FRACTIONS: ANGLES				
± .005 ± .1/64 ± 9°				
FINAL SURFACE QUALITY				
REMOVE BURRS AND BREAK SHARP CORNERS				
MATERIAL	NEXT HIGHER ASSY			
FINISH	SCALE NONE			
SHEET 2 OF 2		DST.		

PARTS LIST		EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS	
TITLE		DATA PATHS I	
M224		K7-2	
SIZE CODE	NUMBER	REV.	
DBS	KAI1-0-DPI	PA	

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PARTS REFERENCE

ITEM NO	DRAWING REFERENCE	DESCRIPTION	PART NUMBER	QUANTITY
1	E1E3-E7, E13, E15-E19, E21-E26, E31-E36	DEC 74H53N	IC 1909062	24
2	E2, E8, E4, E20	DEC 7482N	IC 1905584	4
3	E9-E12, E27-E30	DEC 74H00N	IC 1909057	8
4	C1-C36	.01 MFD, 100V, 20%	CAP 1001610	36
5	C37, C38	6.8 MFD, 35V, 20%	CAP 1000067	2

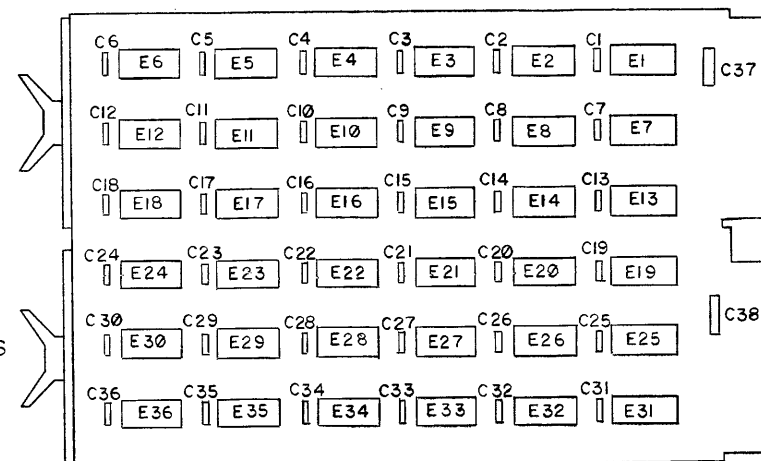
NOTES:

- PIN NOTATION THROUGHOUT IS ORDERED UPON MODULE PLACEMENT IN THE KAI1 PROCESSOR. MODULE REFERENCE ALONE IS OBTAINED BY DELETING THE NUMBER (SLOT LOCATION) AFTER THE FIRST LETTER, AND CONVERTING THE FIRST LETTER ACCORDING TO THE PIN NOMENCLATURE CHART AT RIGHT.
- ALL SIGNALS THAT HAVE MODULE PINS ARE SO NOTED; MULTIPLE NOTATIONS OF THE SAME SIGNALS WITHIN A MODULE HAVE THE PIN NOTED ON EACH. AN INPUT SIGNAL IS NOTED ONLY ONCE PER SHEET UNLESS SEPERATE PINS ARE USED; MULTIPLE INPUTS ARE CONNECTED. DATA FLOW IS FROM THE BOTTOM TO THE TOP.
- PROCESSOR SIGNAL SOURCE NOTATION (K10-2, FOR EXAMPLE) IDENTIFIES THE SIGNAL SOURCE (PRINT AND MODULE). THE FIRST NUMBER AFTER THE K INDICATES THE MODULE PRINT SET, WHILE THE SECOND INDICATES THE SHEET WITHIN THE SET. IF ON A PRINT, THE FIRST NUMBER OF THE K PREFIXES COINCIDE FOR A SIGNAL NAME AND THE PRINT (SEE TITLE BLOCK), THE SIGNAL IS GENERATED ON THE MODULE. A DIFFERENCE IN THE FIRST NUMBER OF THE K PREFIXES INDICATES A SIGNAL GENERATED OFF THE MODULE. SIGNALS WITH A "BUS" PREFIX REPRESENT A "WIRED OR" SITUATION, AND MULTIPLE SOURCES FOR THE SIGNAL CAN EXIST.
- DETAILS ON COMPONENTS ARE NOTED IN THE PARTS REFERENCE, PLACEMENT IS NOTED IN THE COMPONENT PLACEMENT DIAGRAM.
- GND AND +5V ARE USUALLY PIN 7 AND PIN 14, RESPECTIVELY. EXCEPTIONS ARE:

IC TYPE	GND	+5V
DEC 7481	PIN 10	PIN 4
DEC 7482	PIN 11	PIN 4
8251	PIN 8	PIN 16
DEC 8271	PIN 8	PIN 16
DEC 380	PIN 1	PIN 8
DEC 384	PIN 1	PIN 8

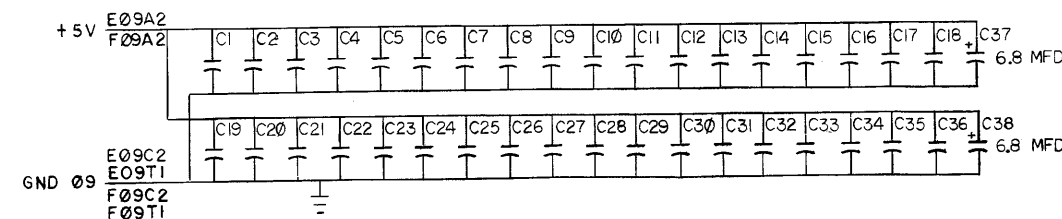
- UNLESS OTHERWISE NOTED: RESISTANCE IS IN OHMS; CAPACITANCE IS IN PICOFARADS. CAPACITORS WITHOUT ANY NOTED VALUES ARE .01 MFD.

COMPONENT PLACEMENT



PIN NOMENCLATURE

MODULE	PROCESSOR
A	E
B	F



REVISIONS

CHK	CHANGE NO.	REV
	1	A

J. O'LOUGHLIN
 6-2-70

FIRST USED ON OPTION/MODEL PDP 11	QTY.	DESCRIPTION	PART NO.	ITEM NO.
UNLESS OTHERWISE SPECIFIED				
UNLESS OTHERWISE SPECIFIED				
DIMENSION IN INCHES				
TOLERANCES				
DECIMALS FRACTIONS ANGLES				
= .005 = 1/64 = 0°30'				
FINAL SURFACE QUALITY				
REMOVE BURRS AND BREAK SHARP CORNERS				
MATERIAL				
FINISH				
NEXT HIGHER ASSY				
SCALE				
SHEET OF 2				
DATE 3-2-70 DATE 3-6-70 DATE 3-6-70 DATE 3/13/70			EQUIPMENT CORPORATION WARDEN MASSACHUSETTS DATA PATHS 2 M224 A-M1-KAI1-0 D81 KAI1-0-DP2 K8-1 A	

