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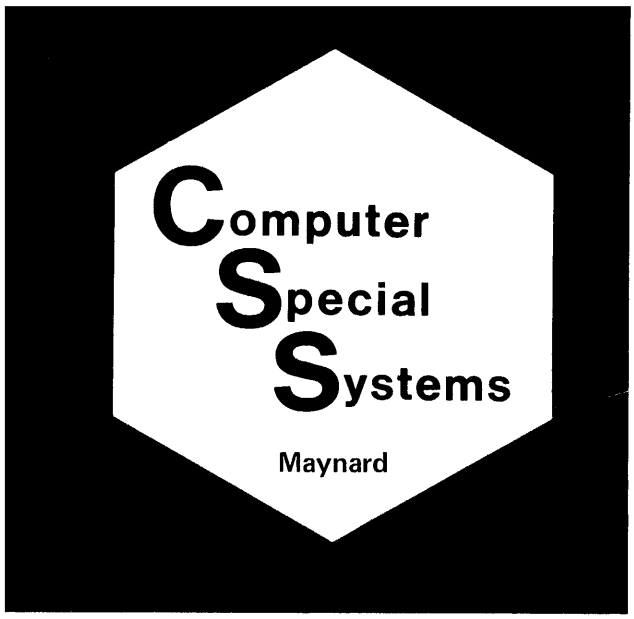
DA11-B
PDP-11 INTERPROCESSOR LINK

OPTION DESCRIPTION
2M-C075A-00



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Computer Special Systems

DA11-B
PDP-11 INTERPROCESSOR LINK

OPTION DESCRIPTION
2M-C075A-00

COMPUTER TYPE PDP-11	**DRAWING SET NO.** DA11-B
PROGRAM NO. MAINDEC-11-DZDRB	**DOCUMENT NO.** YM-C075C-00 (10.4-19) Revision C
DATE OCTOBER 1977	

1st Printing (Rev.) August 1973
2nd Printing January 1974
3rd Printing March 1974
4th Printing December 1974
5th Printing March 1975
6th Printing (Rev.) August 1975
7th Printing September 1976
8th Printing (Rev.) December 1976
9th Printing May 1977
10th Printing October 1977

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PDP-11 INTERPROCESSOR LINK

1.1 GENERAL

The DA11-B Interprocessor Link, designed and manufactured by DIGITAL, provides a means for half-duplex, parallel, DMA (Direct Memory Access) data transfer between two PDP-11 computers.

The DA11-B option consists of two identical sections; each comprises one system unit which mounts in a BA11 Mounting Box associated with each PDP-11 computer.

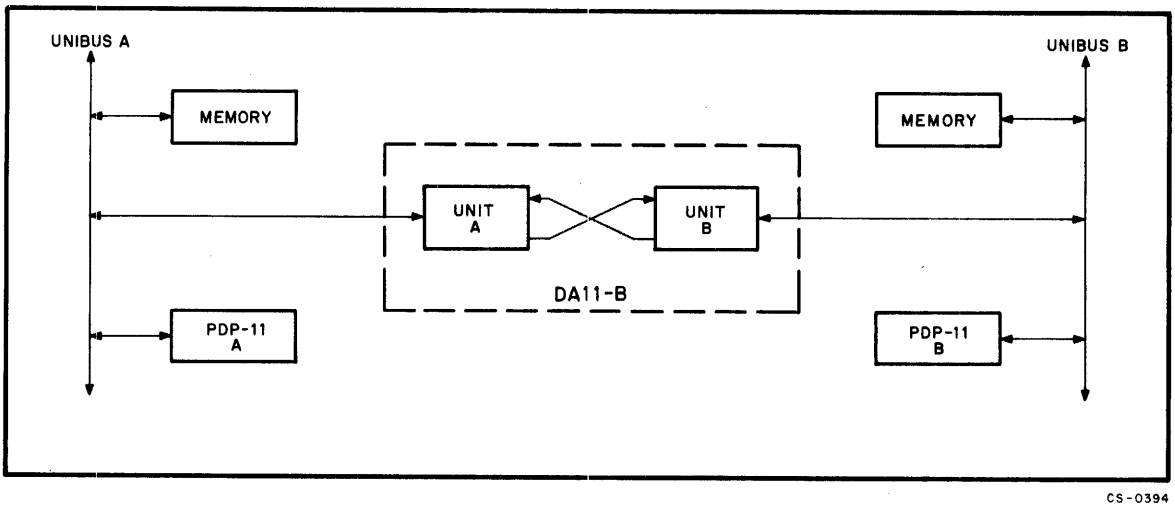

Figure 1-1 System Block Diagram

1.2 OPERATION

Each DA11-B section, consists basically of four registers: Command and Status, Word Count, Bus Address, and Data. Data transfer is initialized under program control and proceeds via Non Processor Request (NPR or DMA), until the entire data block has been transferred. A transfer sequence is as follows:

a. The sending PDP-11 loads its data Starting Address and data block length Word Count.

b. The sending PDP-11 loads the Command/Status register and causes an interrupt in the receiving PDP-11.

c. The receiving PDP-11 responds to the interrupt and loads its Starting Address, Word Count and Command/Status register to initiate the transfer.

d. Transfers continue until completion at which time both PDP-11's receive an interrupt.

Connection between computers is accomplished by BC08R cable assemblies (25 feet standard).

1.3 SPECIFICATIONS*

a. Mechanical:

Units	Two
Logic Panels/Units	One System Unit
Dimensions/Unit	16 in. h, 2-1/4 in. w, 10 in. d
Mounting Prerequisite	BA11-Mounting Box Space

b. Electrical:

Input Power	120/240 Vac ± 10%, 47-63 Hz
Current (at 5 V)	4.3 A
Power Dissipation	25 W
Heat Dissipation	82 Btu/hr
Module Type	M-Series
Logic Levels	TTL

c. Operational:

Data Transfers	
Word Size	16-bits
Method	Direct Memory Access (DMA or NPR) or word transfer
Modes of Operation	
Size	Word or Block
Direction	Send or Receive
Hardware Prerequisites	Two 4K PDP-11 Computers with Multi-Level priority
Unibus	
Bus Load	One Unit load/each bus
Interrupt Vector	Same as DR11-B (124 for first unit)
Register Address	Same as DR11-B (772410 for first unit)
BR Level	Same as DR11-B (BR5 hardwired)
Unit Separation Distance	
25-foot Cables	Model DA11-BD (Standard)
50-foot Cables	Model DA11-BE (Optional)

SECTION 2
INSTALLATION

2.1 SITE CONSIDERATIONS

The DA11-B Interprocessor Link comprises two identical sections; each consists of one System Unit. Each section mounts in a BA11 Mounting Box and interfaces to one of the two PDP-11 computers in the system. Environmental requirements are the same as those specified for the PDP-11 computer system.

2.2 CABLES

Connection between the DA11-B and the two PDP-11 Unibuses is accomplished by means of standard PDP-11 Unibus cables (BC11A) or M920 Jumper Cards. The DA11-B sections connect together by means of BC08R cables supplied by Digital. Cable definitions for the DA11-B and slot locations are shown in Figure 2-1.

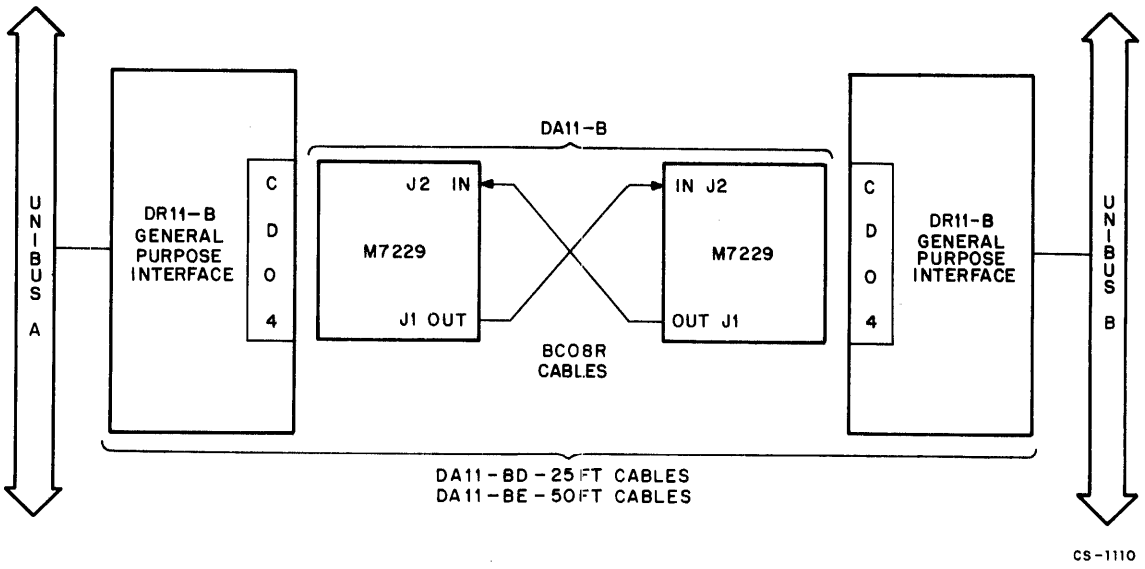

Figure 2-1 DA11-B Cable Layout

2.3 PHYSICAL DESCRIPTION

Each section of the DA11-B contains a standard DR11-B general purpose, direct memory access buffer to the PDP-11. In addition, an M7229 module is provided which plugs into user

connection slots CD04. This module permits back-to-back operation of the DR11-B's between the two processor Unibuses. Two cables supplied by Digital connect the DA11-B sections together. The cables terminate with Berg connectors and plug into the M7229 module.

2.4 INITIAL OPERATION

The following Checkout and Acceptance Test Procedures are performed in-house prior to shipment of the DA11-B option. It is suggested that they be performed again at the customers site, as an initial on-site turn-on procedure.

2.4.1 Checkout Procedure

With the M7229 module card removed from slots CD04 of the DR11-B and the M968 DR11-B Test Board removed from the normal location (AB02) and inserted in CD04, the DR11-B portion of the DA11-B may be tested as a standard DR11-B, using the MAINDEC-11-DZDRB diagnostic program. Each DR11-B must be connected and tested before the two are combined in the back-to-back DR11-B interface of the DA11-B option. Once the DR11-B's are operating correctly, the complete DA11-B option can be connected as shown in the operational configuration (Figure 2-1) and exercised using the MAINDEC-11-DZDRB Diagnostic Program. The system satisfies the requirements of the Acceptance Test when the DA11-B portion of the diagnostic program runs to completion without error.

NOTE

For operation of the DA11-B option, the M968 DR11-B Test Board must be inserted in slots AB02 of each DR11-B.

2.4.2 Acceptance Procedure

The Checkout Procedure also serves as the Acceptance Procedure for this device.

2.5 RELATED LITERATURE

The following DEC publications contain material which supplements the information in this Option Description:

a. PDP-11 Peripherals Handbook

b. Logic Handbook

c. DR11-B/DA11-B Manual EKDR11BTM

d. PDP-11 Multiple-Processor System Options

SECTION 3
OPERATION AND PROGRAMMING

3.1 HARDWARE REGISTERS

This section presents a detailed description of the four registers associated with each processor used with the DA11-B option. These four registers are assigned bus addresses and can be read or loaded (with the exceptions noted) using any instruction that refers to the assigned address.

Signal INIT is the signal produced by power up, power down, the RESET instruction or the START switch on the console; R/W specifies Read/Write. Figure 3-1 shows the register assignments.

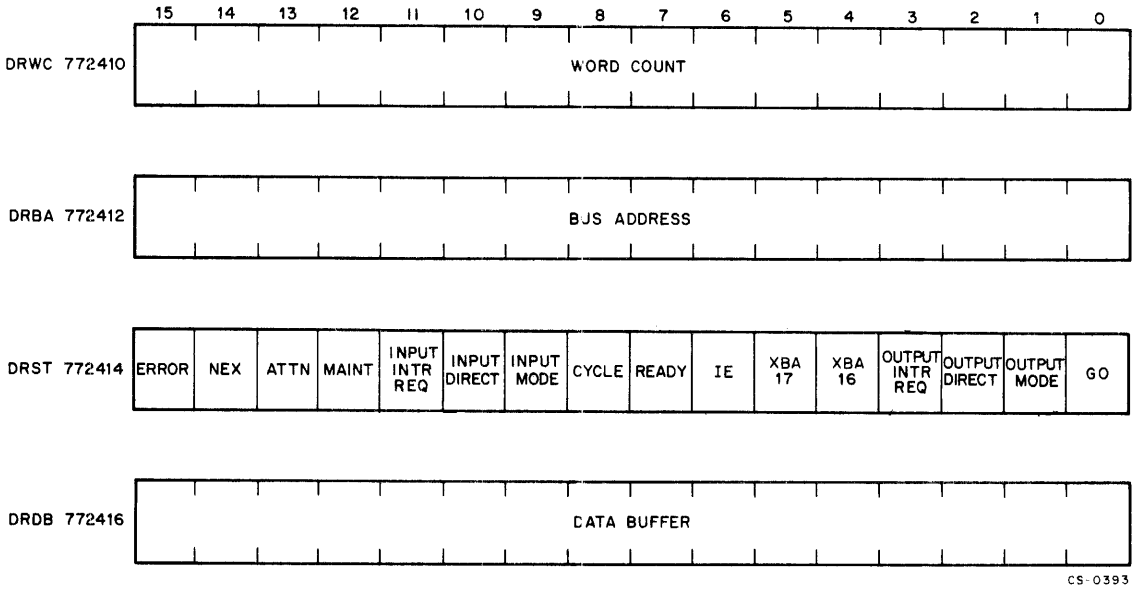

Figure 3-1 DA11-B Register Assignments

3.1.1 Status And Command Register (DRST)

The DRST is a 16-bit register used for issuing commands and providing status for both the control and the companion computer. Each bit is discussed individually in this section. The interrelationship of the DRST bits for each processor is shown in Figure 3-2.

NOTE

OUTPUT INTR REQ 0, OUTPUT DIRECT and OUTPUT MODE (bits 03, 02, and 01, respectively) of the DA11-B become FUNCT 3, FUNCT 2, and FUNCT 1 respectively, in DR11-B literature. In DA11-B notation, OUTPUT INTR REQ, OUTPUT DIRECT and OUTPUT MODE of the control computer become INPUT INTR REQ, INPUT DIRECT and INPUT MODE respectively in the companion computer. The MAINT bit (bit-12) is for maintenance configuration (M968 test board in slots CD04 of the DR11-B).

3.1.1.1 ERROR (Bit 15) - The ERROR bit is read-only, and specifies an error condition when:

a. The DR11-B has attempted to address non-existent memory (also indicated by NEX Bit 14), or

b. When the companion computer has asserted ATTN (Bit 13) because of either an Input Interrupt Request or an Initialize pulse (refer to the description of bit 13), or

c. The test module is not inserted in slot AB02 or CD04 of the DR11-B, or

d. The Bus Address register DRBA has overflowed by incrementing from all 1's to all 0's.

ERROR sets READY (Bit 7) and causes an interrupt if INTERRUPT ENABLE (Bit 6) is set.

The ERROR bit is cleared by removing the condition(s) that caused it to set:

e. NEX is cleared by loading Bit 14 with a zero

f. ATTN is cleared automatically by the companion computer

g. Insert the test module in slots AB02 for normal operation or slots DC04 for diagnostic tests

h. Reload the Bus Address register DRBA.

3.1.1.2 NEX (Bit-14) - NEX (NON EXISTENT MEMORY) is a read/write to 0-bit. The non-existent memory condition specifies that, as Unibus master, the DA11-B did not receive a SSYN response within 20μs following assertion of MSYN. NEX sets ERROR (Bit 15), READY (Bit 7), and causes an interrupt request if IE (Bit 6) has been set. This bit is cleared by INIT or by loading a zero; it cannot be loaded with a one.

3.1.1.3 ATTN (Bit 13) - The ATTN (ATTENTION) bit is read-only; it reads the state of the ATTN signal from the companion computer. When the companion computer is requesting an interprocessor interrupt, the 500 ns ATTN pulse is generated by the companion's INTERRUPT REQUEST (Bit 11). An ATTN pulse is also generated whenever INIT is asserted on the companion computer's bus. If caused by INIT, the ATTN pulse may be as long as 20 ms. Because the ATTN signal is a pulse, it should be ignored by the interprocessor programs.

ATTN sets ERROR and is set and cleared automatically by the DA11-B Link.

3.1.1.4 MAINT (Bit-12) - The MAINT bit is read/write; it is used exclusively with diagnostic programs and is cleared by INIT (Chapter 5 in the DR11-B Maintenance Manual).

3.1.1.5 INPUT INTR REQ (Bit-11) - The INPUT INTR REQ bit is a read-only status bit which reads the status of the OUTPUT INTR REQ bit of the companion computer. When set, the bit specifies that an interprocessor interrupt has been requested by the companion computer.

Setting this bit also sets READY (Bit-7) and causes an Interrupt Request if IE (Bit-6) has been set.

3.1.1.6 INPUT DIRECT (Bit-10) - The INPUT DIRECT bit is read-only and reads the status of the OUTPUT DIRECT bit of the companion computer. The transfer direction is specified as follows:

INPUT DIRECT	Companion Computer Is:
0	Transmitter
1	Receiver

3.1.1.7 INPUT MODE (Bit-9) - INPUT MODE is a read-only status bit for reading the status of the OUTPUT MODE bit of the companion computer. This bit specifies the mode in which the interprocessor link is to be used as follows:

INPUT MODE	Mode
0	Block
1	Word

3.1.1.8 CYCLE (Bit-8) - The read/write CYCLE bit primes bus cycles. If it is set when GO is issued, an immediate bus cycle occurs. It is cleared at the beginning of the bus cycle and by INIT. CYCLE is also set whenever the companion computer requests a bus cycle via CYCLE REQUEST A or B and is cleared when the cycle begins.

3.1.1.9 READY (Bit-7) - The read-only READY bit specifies that the DR11-B is ready to accept a new command. When set, READY forces the DR11-B to release control of the Unibus and inhibits further DMA cycles. This bit is set by INIT, ERROR (Bit-15), or Word Count Overflow and is cleared by GO (Bit-0). Note that READY must be cleared prior to initiating the block transfer. When set, READY causes an interrupt request if IE (Bit 6) has been set.

3.1.1.10 IE (Bit-6) - The read/write IE bit enables an interrupt to occur when either ERROR or READY is asserted, or when INPUT INTR REQ is posted from the companion computer. This bit is cleared by INIT.

3.1.1.11 XBA17, XBA16 (Bits 5 and 4) - These two read/write extended bus address bits (17 and 16) are used with DRBA to specify A<17:01> in direct memory transfers. XBA17 and XBA16 do not increment when DRBA overflows; instead, ERROR is set.

3.1.1.12 OUTPUT INTR REQ (Bit-3) FUNCT 3 - OUTPUT INTR REQ is a read/write bit that is used to send an interrupt request to the companion computer.

When set, this bit sets INPUT INTR REQ and READY in the companion computer and causes an Interrupt Request in the other computer if its INTERRUPT ENABLE has been set. This bit is cleared by INIT.

3.1.1.13 OUTPUT DIRECT (Bit-2) FUNCT 2 - OUTPUT DIRECT is a read/write bit which specifies to the companion computer that the initiating computer is requesting to transmit (0) or receive (1). During the subsequent block transfer, this bit must be in the opposite state to INPUT DIRECT (Bit-10). This bit is cleared by INIT.

3.1.1.14 OUTPUT MODE (Bit-1) FUNCT 2 - The read/write OUTPUT MODE bit specifies to the companion computer (through INPUT MODE) that either a word or block transfer is taking place. A zero specifies a block transfer and a one a word transfer. OUTPUT MODE is not used in any way by the DA11-B control logic but is simply displayed in the companion computer. It may be used by the interprocessor programs to keep track of the progress of the cross-communications dialog that precedes a block transfer and also to note that a block transfer is in progress. This bit is cleared by INIT.

3.1.1.15 GO (Bit-0) - The write-only GO bit causes a pulse to initiate the first DMA cycle in the block transfer. When set in conjunction with CYCLE (Bit-8), this bit causes the first cycle to occur in this computer if this DR11-B is the transmitter. When set alone, it causes the first cycle to occur in the companion computer if that DR11-B is the transmitter. Note that both DIRECTION bits should be set properly before issuing the GO command.

This bit always reads as a zero. When set, this bit clears READY (Bit-7).

3.1.2 Word Count Register (DRWC)

The DRWC is a 16-bit read/write register. It is initially loaded with the 2's complement of the number of transfers to be made and increments toward zero after each bus cycle. When the overflow occurs (all 1's to all 0's), the READY bit of DRST sets and bus cycles cease. DRWC is cleared by INIT.

NOTE

DRWC is a word register; do not use byte instructions when loading this register.

3.1.3 Bus Address Register (DRBA)

The DRBA is a 15-bit read/write register. Bit-0, corresponding to address line A00, is set permanently to 0. With XBA16 and 17 in DRST, DRBA specifies BUS A<17:01> in direct bus access. The register is incremented by two following each bus cycle, advancing the address to the next sequential word location on the bus. If DRBA (corresponding to A<15:01>) overflows (all 1's to all 0's) the ERROR bit in DRST sets. This error condition (BAOF) is cleared by loading DRBA or by INIT.

NOTE

DRBA is word register; do not use byte instructions when loading this register.

The DRBA is cleared by INIT. Overflow does not increment the extended address bits XBA16 and 17, therefore, the maximum block that can be transferred is 32K words.

3.1.4 Data Buffer Register (DRDB)

The DRDB is a 16-bit word register, which can be loaded under program control, and is used to buffer information when transferring data from one computer to the other. The output lines of this register are buffered; the inputs, however, are not. These lines, therefore, must be held until the data is transferred to the memory of the receiving computer.

The Data Buffer DRDB performs two separate functions in the Interprocessor channel. In Word mode, DRDB is used as a 16-bit addressable register to transfer information between computers under program control. In Block mode, DRDB serves as a temporary storage register that holds the word being transferred under NPR control.

3.1.4.1 Word Mode - During program controlled transfers, DRDB is a write/only register for data transmitted to the companion computer and a read/only register for data received. Because only a single flip-flop register exists for each direction, data must be maintained in DRDB until

read by the companion computer. The cross interrupt facility in DRST should be used in conjunction with DRDB to pass parameters between computers as illustrated in the following example: Assume Processor A is sending a file header to Processor B.

Processor A		Processor B
Load DRDB with the first word		
Set: OUTPUT INTR REQ DRST 3		
OUTPUT Mode DRST 1		(New Message)
.	Interrupt B	Enter Interrupt Service Routine
.		Read DRST
.		Read DRDB
.		Set OUTPUT INTR REQ DRST 3
.		.
(Message .	Interrupt A	.
Received)		.
Enter Interrupt Service Routing		.
Load DRDB with second word		.
Clear, then set OUTPUT INTR REQ DRST 3		
	Interrupt B	.
.		.
.		.
repeat		repeat

3.1.4.2 Block Mode - During block transfers under NPR control, DRDB temporarily stores the word read by the transmitter until it is written into memory by the receiver. Because this sequence of operations is transparent to the program, DRDB must not be used for Word mode transfers until the block transfer has completed. If DRDB is loaded by the program during a block transfer, incorrect data may be transmitted between computers. This register is cleared by INIT.

NOTE

DRDB is a word register; do not use byte instructions when loading this register.

3.2 REGISTER ADDRESS ASSIGNMENT

Register address assignments for the DA11-B are the same as for the DR11-B option. Whenever both standard DR11-B's and DA11-B's exist in a given system, the DR11-B's should be assigned first. Four register address complements are reserved. Additional DR11-B's and/or DA11-B's may be installed with addresses assigned in the User Address Space. Table 3-1 lists the reserved register address assignments.

Table 3-1
DR11-B/DA11-B Register Address Assignments

Register	Unit Address (Octal)			
	Unit 1	Unit 2	Unit 3	Unit 4
DRWC	772410	772430	772450	772470
DRBA	772412	772432	772452	772472
DRST	772414	772434	772454	772474
DRDB	772416	772436	772456	772476

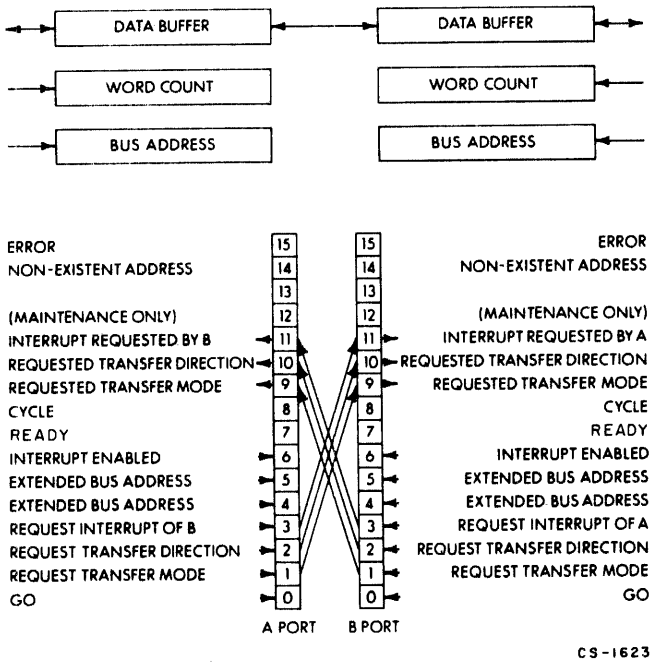

Figure 3-2 Control and Data Transfer Between the A Port and B Port of A Unibus Link

3.3 VECTOR ADDRESS ASSIGNMENTS

Vector address assignments for the DA11-B are the same as for the DR11-B option. Whenever both standard DR11-B's and DA11-B's exist in a given system, the DR11-B's should be assigned first. The first unit is assigned vector address 124_8. Subsequent units are user assigned in the floating vector address space beginning at 300_8.

NOTE

The DA11-B requires only one vector; however, it must be of the form $XX4_8$.

3.3.1 Interrupt Flags

Table 3-2 lists the bits set in DRST following an interrupt request. If several interrupt conditions occur simultaneously, DRST contains the Inclusive-OR of all the bits listed in the table for all pending requests.

Table 3-2
DA11-B Interrupt Flags

	DRST Bit				
Interrupt Caused By:	15 ERROR	14 NEX	13 ATTN	11 INPUT INTR REQ	07 READY
Non-Existent Memory address from DR11-B.	1	1	0	0	1
INIT pulse asserted on companion computer's bus.	1*	0	1*	0	1
Test module not inserted.	1	0	0	0	1
DRBA overflow.	1	0	0	0	1

*Asserted for duration of pulse only.

Table 3-2 (Cont.)
DA11-B Interrupt Flags

Interrupt Caused By:	DRST Bit 15 ERROR	14 NEX	13 ATTN	11 INPUT INTR REQ	07 READY
Input interrupt request from companion computer.	0	0	0	1	1
DRWC overflow indicating block transfer complete.	0	0	0	0	1

*Asserted for duration of pulse only.

3.4 PROGRAMMING

The DA11-B provides four modes of operation: SEND and RECEIVE with WORD or BLOCK data transfers. Either processor may initiate a transfer. The four modes are specified by the states of the function bits of the DRST. With the appropriate function bits enabled, the transfer is initiated by GO of the DRST. After a transfer operation is complete, the DRST function bits should be cleared.

Processor contention, when each is attempting to initiate a transfer, must be resolved by the software. The clearing of the function bits following each transfer facilitates this function.

3.4.1 Initialization

Prior to the initiation of data transfers between two computers connected by the DA11-B option, both systems must be initialized and have their respective Interrupt Enable bits set (Bit-6) in the DRST.

3.4.2 Send Mode

To send information from one processor to the other, the sequence in the sending processor is as follows:

a. Set the DRWC to the 2's complement of the number of transfers to take place.

b. Set the DRBA to the starting address in memory from where data transfers are to occur.

c. Configure the DRST register as follows:

   1. Set OUTPUT INTR REQ - Bit-03, which will interrupt the companion computer;
   2. Clear OUTPUT DIRECT - Bit-02, to specify if a SEND Mode;
   3. Set OUTPUT MODE - Bit-01, for a WORD transfer or clear Bit-01 for a BLOCK transfer;
   4. Set GO, Bit-00.

The interrupted Computer should respond to the interrupt by interrogating the INPUT INTR REQ, INPUT DIRECT, and INPUT MODE Status bits of its DRST to determine if the transmission is to SEND or RECEIVE, WORD or BLOCK. The program should then set up the appropriate DRWC and DRBA after which FUNCT 2 and GO (of the DRST) should be set, specifying that the interrupted computer may receive from its companion computer and that the transfer sequence may proceed.

3.4.3 Receive Mode

For a processor to request information from its companion, the procedure is the same as for SEND, except OUTPUT DIRECT is set to "1" to specify that it is initiating a RECEIVE operation. The Interrupted Computer must respond to the interrupt by setting, in addition to the GO bit, the CYCLE bit (bit 08) in its DRST. This is necessary to cause the first transfer cycle to take place in the Interrupted Computer. Note that in this case, OUTPUT DIRECT of the Interrupted Computer's DRST remains zero, indicating that it is sending to the initiating computer.

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

Because the DA11-B Interprocessor Link design is based upon the DR11-B General Purpose DMA Interface, its operation is defined primarily by the DR11-B. It is assumed that the reader is familiar with the nomenclature used in the DR11-B Maintenance Manual; the same terminology is used here to describe the DA11-B.

The DA11-B Link operates as a half-duplex communications channel; although the channel is capable of transmitting data in both directions, it transmits in only one direction at a time. The following description generally refers to one-way data flow; it should be understood, however, that information can also flow in the opposite direction.

4.2 OPERATING MODES

The DA11-B operates in two modes: Word and Block. In Word Mode, information can be passed between computers one word at a time by interrupt driven program commands. When in Block Mode, the link transmits blocks of consecutive locations from the memory in one computer to the memory of the other using the DMA (NPR) facility in each machine. The block transfer is, then, transparent to the programs in the two computers.

Each computer has independent program control of its own interface. Therefore, the programs in the two machines must cooperate in establishing the channel direction and in priming the Word Count and Bus Address registers in their respective DR11 interfaces. The Word Mode is used primarily to pass information relating to this channel set-up operation prior to a Block Transfer. However, it is not restricted to this function; the Word Mode can also be used to transfer any other types of parameters between the computers so long as a DMA transfer is not in progress.

4.3 BLOCK DIAGRAM

Figure 4-1 is a simplified block diagram of the complete inter-processor DMA communications system. Two separate channels exist through the link in opposite directions. However, because the link operates as a half-duplex device, only one channel is active at a time.

The Data Buffer register (DRDB) is connected through the link to the bus data multiplexer in the opposite computer. In Word Mode, DRDB can be loaded with a full 16-bit word by the program on one side and read by the program in the other computer. In Block Mode, DRDB serves as temporary storage for the word being transferred via NPR control.

The Control and Status registers (DRST) are cross-coupled via three bits in each direction. When DRST <3:1 > are loaded on one side, the information appears in DRST <11:9 >in the opposite computer. These bits also connect to the DA11-B control logic in each interface to define the following operations:

Signal	Transmitter	Receiver
Interrupt Request	DRST 3	DRST11
Direction	DRST 2	DRST 10
Mode	DRST 1	DRST 9

The DA11-B control logic is cross-coupled to activate interrupt requests and coordinate the NPR cyles on each Unibus.

4.4 CROSS INTERRUPT CONNECTION

Figure 4-2 shows the block diagram of the cross-interrupt connection in one direction; an identical circuit exists in the opposite direction. When DRST 3 is set in one computer, a binary "one" appears in DRST 11 of the opposite interface. At the same time,the M7229 Module generates a 500 ns pulse on the ATTN line into the receiving DR11-B. This pulse sets the Ready flag (bit-7) (the pulse also appears briefly on the ATTN flag (Bit-13). If INTERRUPT ENABLE (Bit-6) of the receiver has been previously set, setting READY produces an Interrupt Request to the processor on the receiver's bus. (Note that READY also produces

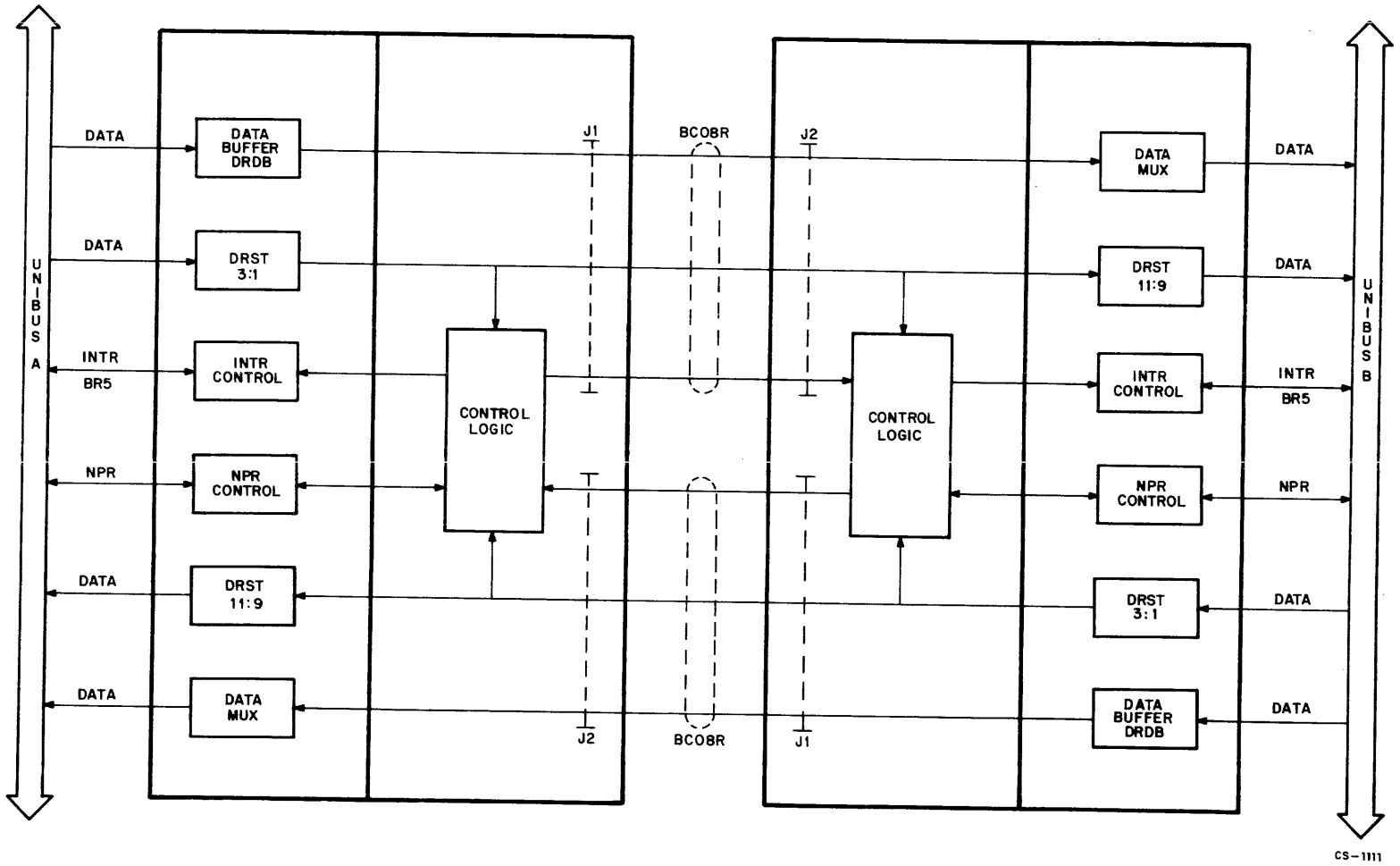

Figure 4-1 DMA Interprocessor Channel Functional Block Diagram

interrupt requests because of other conditions as described in Section Three). When the interrupt service routine responds to the request, it can identify the interrupt as originating from the companion computer by inspecting DRST 11.

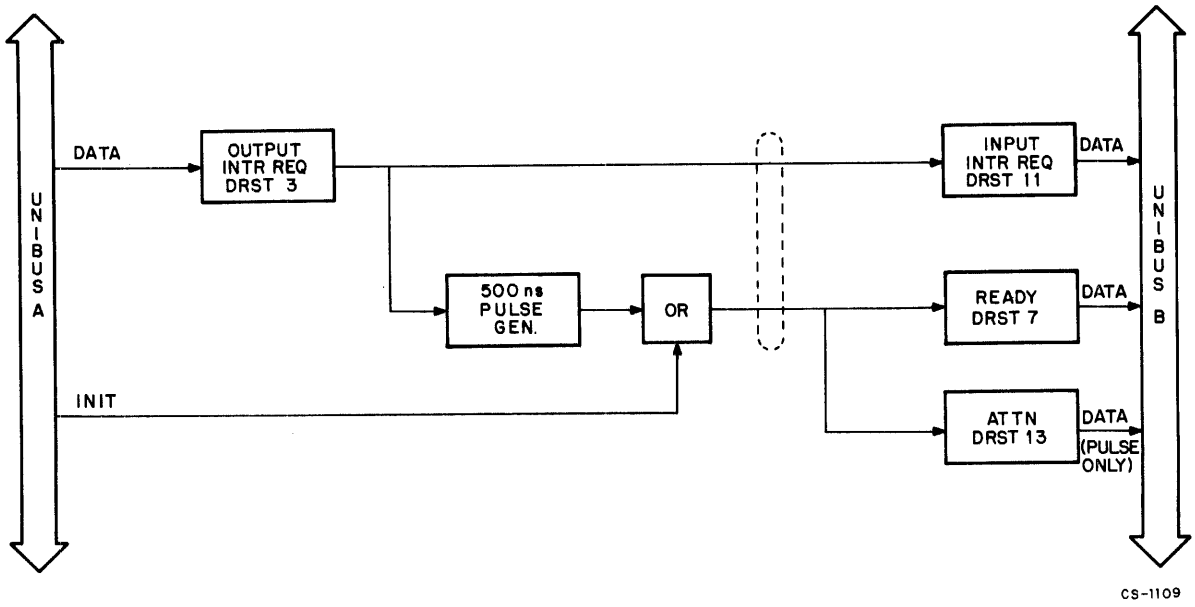

Figure 4-2 Cross Interrupt Block Diagram

When one of the processors issues an INIT pulse to clear the devices on its bus (including its DR11-B), the INIT pulse is transmitted to the other computer where it sets READY and causes an interrupt request as described previously. Note that an INIT command will abort a Block Mode transfer because it clears all the DR11-B registers on its bus; the link, therefore, cannot be used when INIT is asserted.

Figure 4-3 is the block diagram of the control circuits that interlock alternating NPR cycles on the appropriate buses during Block Mode transfers. Two factors must be taken into account in starting the NPR transfer. First, a program in either computer may request the transfer operation and, second, the data may flow in either direction. (Figure 4-3 actually shows only the circuits required to establish a transfer from Unibus A to Unibus B, duplicate circuits exist for the other direction).

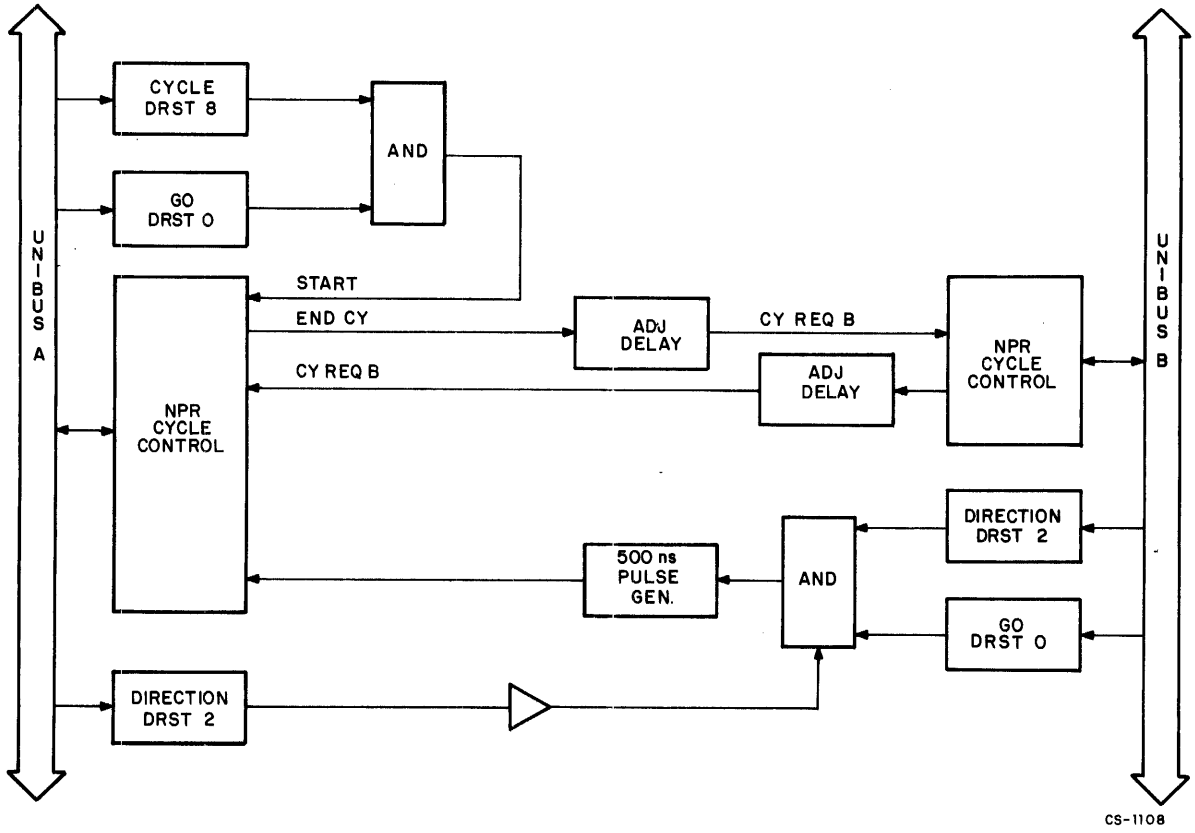

Figure 4-3 NPR Interlocking Control Block Diagram

The NPR Cycles always occur in pairs, i.e., one on each bus. The first cycle is a DATI (read from memory) by the transmitter (Unibus A in Figure 4-3). The second cycle is a DATO (write into memory) by the receiver (Unibus B). These alternating cycle pairs repeat until the entire block has been transmitted. The control circuits illustrated in Figure 4-3 perform the following: the circuits associated with the "GO" commands (DRST 0) in conjunction with the programming procedure described below, generate the first NPR cycle by the transmitter and the END CYCLE circuits produce all subsequent NPR cycles required by the block transfer.

The programming procedure that initiates a block transfer is as follows:

a. The requesting computer sets up the Word Count and Bus Address registers in its associated DR11-B. It then loads the following information into its Status register:

1. GO (Bit-0) is set to a "1" to clear READY (Bit-7).

2. MODE (Bit-1) is cleared to a "0" to specify Block Mode.
3. DIRECTION (Bit-2) is cleared to a "0" to specify Transmit, or set to a "1" to indicate Receive.
4. INT REQ (Bit-3) is set to a "1" to interrupt the other computer.

b. Upon receiving the interrupt, the requested computer sets up its Word Count and Bus Address registers and loads its Status register as follows:
1. MODE (Bit-1) is cleared to a "0" to indicate Block Mode.
2. DIRECTION (Bit-2) is set or cleared to indicate direction. Note that the state of this flag must be opposite to the Direction flag in the requesting computer.
3. If the requested computer is the receiver (Processor B), it sets GO (Bit-0) to generate a GO pulse that is passed through the M7229 module as CYCLE REQUEST A to the transmitter or
4. If the requested computer is the transmitter (Processor A), it sets both GO (Bit-0) and CYCLE (Bit-8) to generate a START command to its own NPR cycle control circuit.

When the transmitter has read the data word from its memory and loaded it into its data buffer DRDB, its NPR cycle control logic generates an END CYCLE pulse. This pulse is stretched by an adjustable delay and sent as CYCLE REQUEST B to the receiving computer. The trailing edge of the stretched pulse triggers an NPR cycle that writes the data word into the receiver's memory. The termination of the write cycle likewise produces an END CYCLE pulse to initiate the next read operation in the transmitter. This alternating sequence continues until the Word Count registers overflow and halt the block transfer.

The interval between successive NPR cycles on a Unibus is equal to the sum of the two adjustable delay times plus the time to request and accomplish the two NPR cycles. Each delay is adjustable from approximately 5 to 50 μs. Therefore, the interval between NPR requests to one of the processors can be adjusted over the range of approximately 10 to 100 μs yielding interprocessor data rates of 10K to 100K words per second. If a higher rate is desired, the capacitor in the adjustable delay circuit can be reduced in value to shorten the delay. The maximum interprocessor data rate is one half the cycle rate of the memories being addressed.

SECTION 5
MAINTENANCE

5.1 MAINTENANCE TECHNIQUES

The DA11-B requires two PDP-11 processors to checkout and diagnose interprocessor communication. The two DR11-B's within the DA11-B are standard. If the interfaces to the DR11-B's which simulate the user device are disconnected, and the M968 test board is inserted in slots CD04 of the DR11-B system units, then each DR11-B may be tested as a stand-alone option. Refer to the DR11-B/DA11-B Maintenance Manual EKDR11BTM, Section 5.

5.2 REQUIRED DIAGNOSTICS

The following diagnostic program completely checks operation of the DA11-B system.

Title	DEC Number
DR11-B Diagnostic	MAINDEC-11-DZDRB

SECTION 6
SUGGESTED SPARE MODULES

6.1 MODULES

Table 6-1 lists the DA11-B module complement by type, function, and quantity in use.

Table 6-1
Spare Module List

DEC Type No.	Function	No. In Use
M112	2-Input NOR Gates	1
M113	2-Input NAND Gates	1
M116	4-Input NOR Gates	1
M208	8-Bit Buffer/Shift Register	1
M239	Three 4-Bit Counter/Register	1
M611	High Speed Power Inverter	1
M796	Unibus Master Control	1
M7219	RC11 Bus Interface	1
M7229	DR11-B Interface	1
M7821	Interrupt Control Module	1

APPENDIX A
ALTERATION OF PRIORITY INTERRUPT LEVEL

A.1 GENERAL

The DR11-B's used in the DA11-B option are factory wired to interrupt at priority level five. Changing this level involves rewiring the BR request line, the BG IN (Bus Grant), and BG OUT. In the following lists, the Bus Grant Lines not in use must remain jumpered between Unibus In (Slots AB01) and Unibus Out (Slots AB04). First, remove priority level five as follows:

Step	Procedure	Location		
1	Remove BUS BR 5 L.	E02P1	to	B01C1
2	Remove BUS BG4 IN H.	B01B1	to	E02E1
3	Remove BUS BG5 OUT H.	E02A1	to	B04B1
4	Add BUS BG5 H.	B01B1	to	B04B1

Then, add the selected priority level, as indicated in Paragraphs A.2 through A.4.

A.2 LEVEL FOUR

For level four perform the following:

Step	Procedure	Location		
1	Remove BUS BG4 H.	B01E2	to	B04E2
2	Add BUS BG4 IN H.	B01E2	to	E02E1
3	Add BUS BG4 OUT H.	E02A1	to	B04E2
4	Add BUS BR4 L.	E02P1	to	B01D2

A.3 LEVEL SIX

For level six perform the following:

Step	Procedure	Location		
1	Remove BUS BG6 H.	B01A1	to	B04A1
2	Add BUS BG6 IN H.	B01A1	to	E02E1
3	Add BUS BG6 OUT H.	E02A1	to	B04A1
4	Add BUS BR6L.	E02P1	to	A01U2

A.4 LEVEL SEVEN

For level seven perform the following:

Step	Procedure	Location		
1	Remove BUS BG7 H.	A01V1	to	A04V1
2	Add BUS BG7 IN H.	A01V1	to	E02E1
3	Add BUS BG7 OUT H.	E02A1	to	A04V1
4	Add BUS BR7 L.	E02P1	to	A01T2

APPENDIX B
ADJUSTING THE INTERPROCESSOR TRANSFER RATE

B.1 GENERAL

The DA11-B provides the capability for adjusting the rate of interprocessor data transfer and consequently regulating the NPR transfer loading of the system. For a heavily loaded NPR system, the DA11-B may be slowed down, so as to provide more service time to the other NPR devices (i.e., disks). The user, therefore, can adjust his DA11-B to provide the optimum data throughput balance for his individual need and configuration.

B.2 TRANSFER TIMING

When one unit of the DA11-B completes a data transfer, the END CYCLE pulse is generated. END CYCLE triggers an adjustable one-shot multivibrator delay which is gated through the cable connected to the companion unit. The trailing edge of the pulse output from the one-shot, initiates a cycle request which starts a bus cycle in the companion computer. When the bus cycle in the companion computer is complete, END CYCLE is generated (also through a one-shot) to the first DA11-B unit and the process repeats. The one-shots, i.e., one in each DA11-B interface section are adjustable from 1.5 μs to 850 μs. These delays are factory set to 15 μs. To summarize, the time between the completion of a bus transfer on one CPU bus and the request for a bus transfer on the other CPU bus is adjustable from 1.5 μs to 850 μs, controlling the frequency of interprocessor data transfers.

B.3 TRANSFER TIMING ADJUSTMENT

Perform the following to adjust transfer timing:

a. Load and run the Interprocessor Link portion of the DR11-B diagnostic program MAINDEC-11-DZDRB

b. With an oscilloscope, observe the END CYCLE pulse generated by one of the DR11-B's at the System Unit back-plane slot C04 pin B1.

c. Starting with both potentiometers set for the minimum interval between pulses, adjust first one control and then the other to achieve the desired rate:

Adjustment	Approximate Pulse Interval
Both set to minimum	15 μs
Adjust first potentiometer	50 μs maximum
Adjust second potentiometer	85 μs maximum

If a different adjustment range is desired, remove capacitor C8 from both M7229 modules and replace with the required value:

C8	Approximate Range
200 pF	1.5 to 8.5 μs
2000 pF	15 to 85 μs (factory value)
.02 pF	150 to 850 μs

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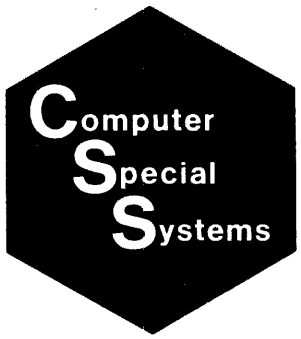
SHIPPING LIST

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION
1		DR11-B Logic Units including all modules	2
2	M7229	Modules	2
3	BC08R	Cables (two cables of appropriate length)	2
4		Unibus cable set (as required)	1
5	YM-C075C-00	Option Description (10.4-19C)	1
6	DA11-B	Engineering Drawing Set	1
7	DR11-B	Engineering Drawing Set	1
8	MAINDEC-11-DZDRB	DR11-B/DA11-B Diagnostic Program on Binary Tape	1
9	MAINDEC-11-DZDRB	DR11-B/DA11-B Diagnostic Program Listing	1
10	DECSPEC-11-AWYAX	DECX/11 Diagnostic Program on Binary Tape	1
11	DECSPEC-11-AWYAX	DECX/11 Diagnostic Program Listing	1
12	EKDR11BTM	DR11-B/DA11-B Manual	1

TITLE	DOCUMENT NUMBER	REV.
DA11-B PDP-11 INTERPROCESSOR LINK	YM-C075C-00 (10.4-19)	C



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