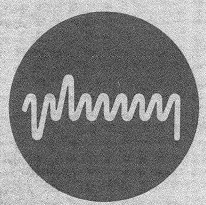
# PM-1116 B
# Core Memory
# Manual



**Plessey**
**Microsystems**

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Microsystems

# CAUTION

READ BEFORE INSTALLING MODULE

DAMAGE TO MODULE OR TO HOST EQUIPMENT
COULD RESULT FROM IMPROPER INSTALLATION.

**READ THE INSTALLATION SECTION OF THE MANUAL.**

- Use address strapping plugs – not jumper wires.
- Verify that address strapping is correct.
- Verify that power is off.
- Insert card only into slots as designated in manual.
- Verify that card is correctly aligned.
- Verify that polarizing keys line up properly.
- Verify that card is completely seated.
- Check that fans and air stream are unobstructed.

# PM-1116 B
# Core Memory
# Manual

February 1977 - Revision -





| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 0-0 |

FORM 000021

# Preface

*This manual provides the information needed to install, operate, maintain, and troubleshoot the PM-1116B core memory manufactured by Plessey Microsystems, Irvine, California.*

*The reader is assumed to have a basic knowledge of digital computer theory and an understanding of the PDP-11 computer in which the PM-1116B is used.*



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## SECTION 5 - MAINTENANCE AND TROUBLESHOOTING





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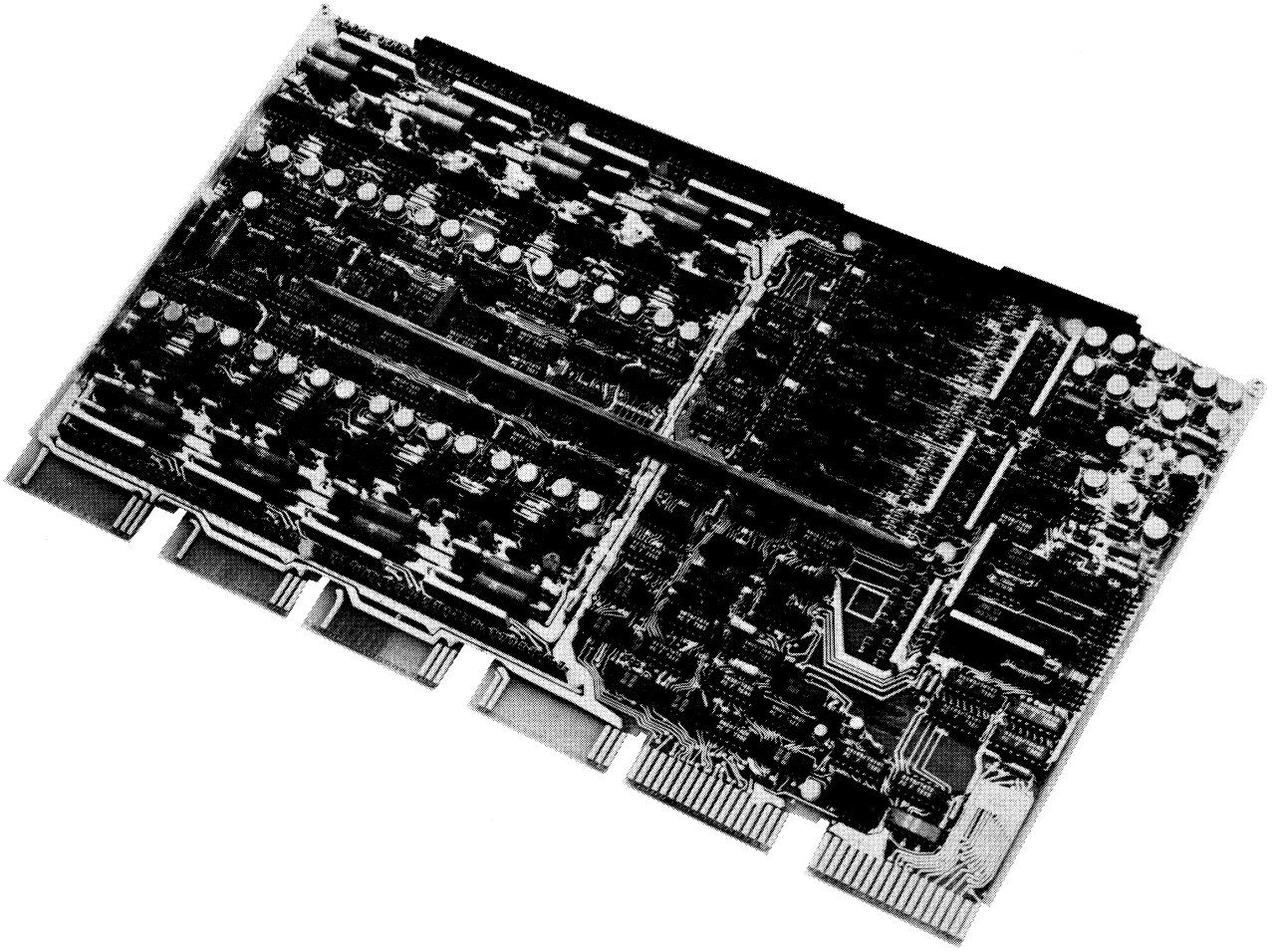

PM-1116B CORE MEMORY



| SIZE | CODE IDENT NO. | DWG NO. |
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| A | 52648 | MA 700945 |
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# Section 1
# General Information

## 1.1 INTRODUCTION

This manual provides the information needed to install, operate, maintain and troubleshoot the PM-1116B core memory manufactured by Plessey Microsystems, Irvine, California.

The material is arranged into five sections as follows:

Section 1 - GENERAL INFORMATION. This section contains a brief functional description of the PM-1116B and a description of the physical specifications of the memory.

Section 2 - INSTALLATION. This section explains the requirements and procedures for equipment installation. Address selection and memory interleaving are described.

Section 3 - FUNCTIONAL DESCRIPTION. This section contains a detailed functional description of the PM-1116B including addressing, timing and control circuits, drive and sink switches, data loop circuitry, and current source generator.

Section 4 - THEORY OF OPERATION. This section contains a circuit logic description of the PM-1116B memory.

Section 5 - MAINTENANCE AND TROUBLESHOOTING. This section describes maintenance and troubleshooting procedures.

Appendix - The appendix contains the parts list, logic diagrams, and assembly drawing required for a complete understanding of the unit.

## 1.2 GENERAL DESCRIPTION

The PM-1116B memory has a maximum capacity of 16384 words of 16 bits per word. It is designed to operate in Digital Equipment Corporation (DEC) PDP-11/05, 11/10, 11/35, 11/40 or 11/45 computers.* It can also be mounted in the PDP-11/04 and 11/34 computers with the 10 1/2" or 21" chassis where -15V at 6A minimum is supplied. The PM-1116B cannot be installed in the 5 1/4" chassis PDP-11/04 or 11/34.

* DEC, PDP and Unibus are registered trademarks of Digital Equipment Corporation.

The PM-1116B may be operated with, or in place of, the DEC model MM11-L in applications where -15V at 6 amps is provided.

### 1.2.1 CAPACITY

The PM-1116B has a storage capacity of 16384 words of 16 bits per word. The storage capacity of the computer may be expanded by adding more memory modules.

### 1.2.2 ACCESS TIME

The access time of the PM-1116B is 350ns maximum. Access time is defined as the time from when MSYN initiates the memory cycle to the time when all data lines are stable on the Unibus.

### 1.2.3 CYCLE TIME

The cycle time of the memory is 900ns maximum. Cycle time is defined as the time from when an MSYN is accepted by the memory to the time when the memory is ready to accept another MSYN.

## 1.3 FUNCTIONAL DESCRIPTION

The PM-1116B operates in several different modes including full word read-restore and clear-write, byte read-restore and clear-write, and read-pause. These modes are determined by the state of address Bit AØØ and control lines CØ and C1. The modes of operation are described in detail in Section 3; a brief description of each mode is contained in the following text.

Read-Restore (DATI): In this mode the memory reads data at a specified location, presents the data to the Unibus, and then restores the data into its original location.

Clear-Write (DATO): In this mode the memory clears a specified core location and then writes data from the data bus into that location.

Clear-Write Byte (DATOB): In this mode the memory performs a read-restore on one byte of data and a clear-write on the other byte of data.

Read-Pause (DATIP): During the DATIP mode the memory reads data from a specified address and waits for a DATO or DATOB operation. The logic in the memory is set such that the memory will skip the clear cycle of the clear-write operation and proceed to write new data into the location.



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|---|---|---|
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### 1.3.1 INTERFACE SIGNALS

Input signals to the memory are as follows:

| Signal Name | Function |
|---|---|
| AØØ-A17 | Address Lines |
| DØØ-D15 | Data Lines |
| CØ, C1 | Control Lines |
| MSYNL | Master Sync |
| INIT | Initialize |
| DCLO | DC Power OK |

Output signals from the memory are as follows:

| Signal Name | Function |
|---|---|
| DØØ-D15 | Data Lines |
| SSYN | Slave Sync |

## 1.4 PHYSICAL SPECIFICATIONS

The PM-1116B memory system assembly consists of an electronics board and a stack assembly. The stack assembly is a 16384 x 16 bit, 3-D, 3 wire (common sense/inhibit) core matrix arranged in a planar configuration of thirty-two 64 x 128 core arrays. The stack assembly also contains decoding diodes; it plugs directly into the back of the electronics card.

The memory assembly occupies only two backplane slots: the electronics card plugs into one slot and the adjacent slot is covered by the stack which does not require backplane connection.

Table 1-1 shows the general specifications of the PM-1116B memory.

| CHARACTERISTIC | SPECIFICATION |
|---|---|
| Cycle Time | 900ns |
| Access Time | 350ns |
| Interface Signal Levels:<br><br>High (inactive)<br>Low (active) | <br><br>+2.4V to +5.0V<br>0V to +0.8V |
| Operating Temperature<br>Non-operating Temperature | 0°C to +50°C<br>-40°C to +85°C |
| Operating Altitude<br>Non-operating Altitude | -1000 ft. to +10,000 ft.<br>40,000 ft. |
| Operating Humidity | 10% to 90% without condensation |
| Mechanical Shock | Housed in its shipping container in accordance with MIL-STD-810B method 516, procedure V. |
| Non-operating Thermal Shock | ±25°C per hour maximum |
| Mechanical Dimensions:<br><br>Width<br>Depth<br>Thickness | <br><br>15.687 inches<br>8.96 inches<br>0.78 inches |
| Component Height Limit:<br><br>Conductive<br>Non-Conductive | <br><br>.343<br>.375 |

Table 1-1: General Specifications

### 1.4.1 POWER REQUIREMENTS

The PM-1116B memory module requires the same DC voltages as the DEC MM11-L memory. Table 1-2 shows the voltage and current requirements. The power requirements shown are average and worst-case values for non-interleaved operation at 25°C.

| VOLTAGE | STANDBY CURRENT | OPERATING CURRENT | |
|---|---|---|---|
| | | TYPICAL | WORST CASE |
| +5V | 2.1A | 2.7A | 3.3A |
| -15V | .3A | 2.8A | 5.3A |

Table 1-2: Power Requirements

Power for the module is routed via connector pins as follows:

| Voltage | Pins |
|---|---|
| +5V | CA2, DA2, EA2, FA2 |
| -15V | CB2, DB2, EB2, FB2 |
| GND | CC2, DC2, EC2, FC2, CT1, DT1, ET1, FT1 |

# Section 2

# Installation and Operation

This section provides information for the installation and operation of the PM-1116B memory system. It also lists the various options available with the memory and explains their incorporation into the memory systems.

## 2.1 UNPACKING AND INSPECTION

The PM-1116B memory is shipped in a special packing carton designed to keep the board from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the memory requires reshipment.

To unpack the memory, remove any packing materials and visually inspect for physical damage. Check all hardware attaching the stack to the electronic board.

## 2.2 ASSEMBLY PART NUMBERS

The following numbers are used to identify the PM-1116B memory assemblies:

| Assembly Part Number | Assembly |
|---|---|
| 700945 | Top Assembly |
| 700944 | Board Assembly |
| 700298-100 | Stack Assembly |

## 2.3 MEMORY INSTALLATION

The PM-1116B is directly interchangeable with the DEC MM11-L memory and can be plugged directly into the same backplane with or in place of it.

The PM-1116B is also interchangeable with the DEC MM11-C and MM11-D where adequate -15V power is supplied. The PM-1116B can be installed in any Plessey or DEC backplane that provides 6A or more -15V power with standard Unibus or modified Unibus memory connections.

The PM-1116B memory will operate in the following backplane units:

- DEC DD11-D, DD11-C double and single systems unit modified Unibus backplanes including the DD11-D and DD11-C series such as the DD11-PK, DD11-CK, and DD11-DK backplanes.
- PM-D11/SPC-1 and -2, double and single systems unit modified Unibus backplanes.
- PM-F11/SPC and F11/SPC-1, double and single systems unit standard Unibus backplanes.
- PM-F11 double systems unit standard Unibus backplane.

The PM-1116B can be installed in any DEC backplane slot specified for MM11-D, MM11-C or MM11-L memory. For installation in Plessey backplanes refer to the appropriate backplane manual. Unibus pin assignments are listed in Table 2-1. For further installation information, refer to *Memory Installation Guide*, document number 700434.

## 2.4 ADDRESS STRAPPING

Each memory must be strapped to respond to specific address locations. Since all memory select lines are common on the Unibus address strapping is necessary in order to access only one memory at one time.

The address strapping plug is designated TB1. It is a 16 pin IC socket and is located next to P1-A interface pin connector on the component side. Pin 1 is at the lower left hand side of the address strapping plug. Table 2-2 shows the jumper locations for memory strapping.

## 2.5 INTERLEAVE OPTION

The PM-1116B memories can be interleaved to speed data transfer times. This section describes interleaving and explains how to interleave two memories.

The memory, which always acts as a slave, takes approximately 900ns to complete a cycle once accessed. Since the memory is self-contained with address registers data registers and timing & control circuitry, it does not require connection to the Unibus for the entire cycle. Each memory unit attached to the Unibus releases the Unibus in less than 600ns after it has been accessed. The Unibus is then free for exchanging communications between devices, however the memory last accessed is still running and will not respond to a request on the Unibus for another 300ns until it completes its internal cycling.

| MEMORY CONNECTOR SECTION A | | | | | |
|---|---|---|---|---|---|
| PIN NO. | UNIBUS SIGNAL NAME STANDARD | MODIFIED | PIN NO. | UNIBUS SIGNAL NAME STANDARD | MODIFIED |
| A1 | INITL | INITL | A2 | +5V | +5V |
| C1 | DØØL | DØØL | C2 | GND | GND |
| D1 | DØ2L | DØ2L | D2 | DØ1L | DØ1L |
| E1 | DØ4L | DØ4L | E2 | DØ3L | DØ3L |
| F1 | DØ6L | DØ6L | F2 | DØ5L | DØ5L |
| H1 | DØ8L | DØ8L | H2 | DØ7L | DØ7L |
| J1 | D1ØL | D1ØL | J2 | DØ9L | DØ9L |
| K1 | D12L | D12L | K2 | D11L | D11L |
| L1 | D14L | D14L | L2 | D13L | D13L |
| T1 | GND | GND | M2 | D15L | D15L |

| MEMORY CONNECTOR SECTION D | | | | | |
|---|---|---|---|---|---|
| PIN NO. | UNIBUS SIGNAL NAME STANDARD | MODIFIED | PIN NO. | UNIBUS SIGNAL NAME STANDARD | MODIFIED |
| A1 | +5V | +5V | A2 | +5V | +5V |
| B1 | -15V | -15V | B2 | -15V | -15V |
| C1 | GND | GND | C2 | GND | GND |
| | | | K2 | BG7 IN | BG7 IN |
| | | | L2 | BG7 OUT | BG7 OUT |
| | | | M2 | BG6 IN | BG6 IN |
| | | | N2 | BG6 OUT | BG6 OUT |
| | | | P2 | BG5 IN | BG5 IN |
| | | | R2 | BG5 OUT | BG5 OUT |
| | | | S2 | BG4 IN | BG4 IN |
| T1 | GND | GND | T2 | BG4 OUT | BG4 OUT |

| MEMORY CONNECTOR SECTION B | | | | |
|---|---|---|---|---|
| PIN NO. | UNIBUS SIGNAL NAME STANDARD | MODIFIED | PIN NO. | UNIBUS SIGNAL NAME STANDARD | MODIFIED |
| | | | A2 | GND | GND |
| | | | C2 | GND | GND |
| F1 | ACLØL | ACLØL | F2 | DCLØL | DCLØL |
| H1 | AØ1L | AØ1L | H2 | AØØL | AØØL |
| J1 | AØ3L | AØ3L | J2 | AØ2L | AØ2L |
| K1 | AØ5L | AØ5L | K2 | AØ4L | AØ4L |
| L1 | AØ7L | AØ7L | L2 | AØ6L | AØ6L |
| M1 | AØ9L | AØ9L | M2 | AØ8L | AØ8L |
| N1 | A11L | A11L | N2 | A1ØL | A1ØL |
| P1 | A13L | A13L | P2 | A12L | A12L |
| R1 | A15L | A15L | R2 | A14L | A14L |
| S1 | A17L | A17L | S2 | A16L | A16L |
| T1 | GND | GND | T2 | C1L | C1L |
| U1 | SSYNL | SSYNL | U2 | CØL | CØL |
| V1 | MSYNL | MSYNL | | | |

| MEMORY CONNECTOR SECTIONS C, E, & F | | | | | |
|---|---|---|---|---|---|
| PIN NO. | UNIBUS SIGNAL NAME STANDARD | MODIFIED | PIN NO. | UNIBUS SIGNAL NAME STANDARD | MODIFIED |
| | | | A2 | +5V | +5V |
| | | | B2 | -15V | -15V |
| | | | C2 | GND | GND |
| T1 | GND | GND | T2 | GND | GND |

NOTE: Unibus signals not connected on the memory are not listed.

Table 2-1: **Standard Unibus and Modified Unibus Pin Assignments**

| | ADDRESS BLOCK | STRAPPING PLUG NUMBER | JUMPER PINS 4-16 | 4-15 | 4-14 | 4-13 | 4-12 | 4-11 | 4-10 | 4-9 | 2-3 | 7-8 | 6-7 | 1-2 | 2-7 | 4-5 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 - 16K | 700066-136 | X | X | X | X | | | | | X | X | | | | |
| | 4K - 20K | 700066-137 | | X | X | X | X | | | | X | X | | | | |
| | 8K - 24K | 700066-138 | | | X | X | X | X | | | X | X | | | | |
| | 12K - 28K | 700066-139 | | | | X | X | X | X | | X | X | | | | |
| * | 16K - 32K | 700066-140 | | | | | X | X | X | X | X | X | | | | |
| | 24K - 40K | 700066-162 | | X | | | | | X | | X | | | | X | |
| | 32K - 48K | 700066-141 | X | X | X | X | | | | | X | | X | | | |
| | 40K - 56K | 700066-163 | | | | X | | X | | | X | | | | X | |
| | 48K - 64K | 700066-142 | | | | | X | X | X | X | X | | X | | | |
| ** | 56K - 72K | 700066-164 | | | | | | | | X | | | | | X | X |
| | 64K - 80K | 700066-143 | X | X | X | X | | | | | | X | | X | | |
| | 72K - 88K | 700066-165 | | | X | | X | | | | | | | X | X | |
| | 80K - 96K | 700066-144 | | | | | X | X | X | X | | X | | X | | |
| | 88K - 104K | 700066-166 | | X | | | | | X | | | | | X | X | |
| | 96K - 112K | 700066-145 | X | X | X | X | | | | | | | X | X | | |
| | 104K - 120K | 700066-167 | | | | X | | X | | | | | | X | X | |
| | 112K - 128K | 700066-146 | | | | | X | X | X | X | | | X | X | | |

* NOTE: For 16K-31K operation, install jumper W1. See Figure 4-1.

** NOTE: For 56K-72K operation, remove jumper from S to R (U14-12) and install from S to T. Also install a 1K ± 5% 1/4 watt resistor between U19-4 and U43-8 (+5V). See Figure 4-1.

Table 2-2: Jumper Locations for Memory Strapping

Assume that a Unibus master is reading from contiguous locations in memory. The device accesses memory and receives stored data in less than 400ns. The memory releases the Unibus after 600ns but is not ready for the device to read the next address location for another 300ns. The device normally must wait 300ns until the memory completes its cycle. However, if two modules are interleaved the next address location is located in a different memory module. The second memory module is not cycling and therefore ready to accept a request. Thus the device can access the next memory module immediately after the Unibus is released by the first memory. When two memories are interleaved, one responds to all the even locations and the other responds to all the odd locations in an address block.

This arrangement enables the Unibus master to read or write in each memory in 600ns effective cycle time. This means that a device that takes 3 minutes to access an address block without interleaving will take only 2 minutes if that address block is interleaved. Figure 2-1 illustrates the time saving feature of the interleave option.

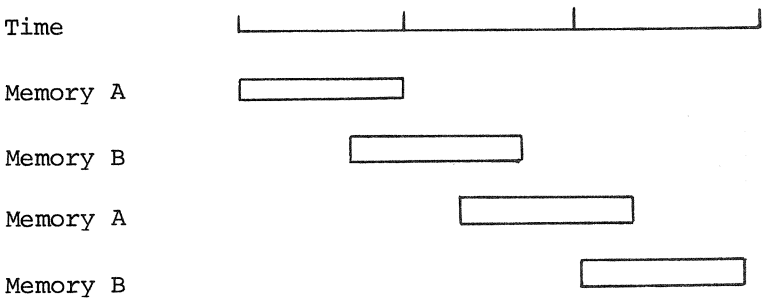


Figure 2-1: Interleave Memory Timing

Two separate memories of equal capacity must be used for interleaving. Memory cannot be interleaved on the same board. Memories of different speeds or from different sources, such as Plessey or DEC or others, can be used together providing they are of the same capacity.

To enable the 16K interleave option, the least significant word address bit, AØ1, and the most significant address bit, A15, are interchanged on the board, as illustrated in Figure 2-2.

No special address strapping plugs are used with the interleave option. If two memories are to be interleaved from Ø to 32K, for example, one memory is assigned the Ø-16K address block and the other memory is assigned the 16K-32K block. By interchanging address A15 and AØ1, one memory is set to respond to odd addresses and the other memory to even addresses.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
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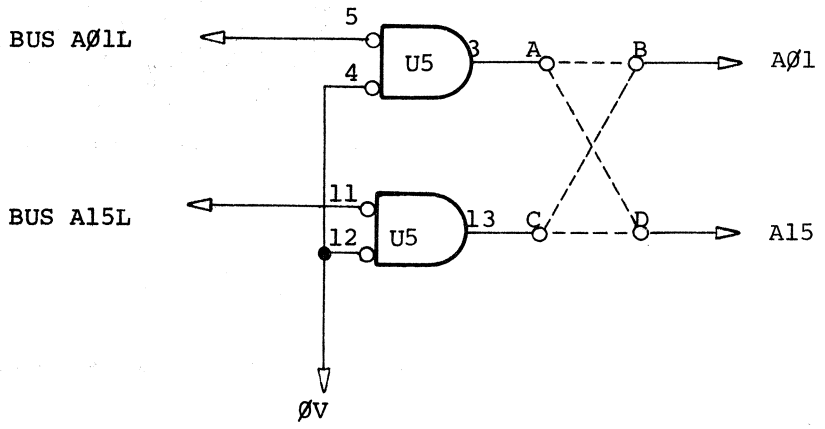



JUMPER POSITIONS

| | | |
|---|---|---|
| Normal | A to B | C to D |
| 16K Inter-leave | A to D | C to B |

Figure 2-2: Interleave Instructions



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 2-6 |

When memory modules are interleaved, two modules are frequently operating simultaneously causing the power requirement to be increased as shown in Table 2-3.

| VOLTAGE | STANDBY CURRENT* | OPERATING CURRENT |
|---|---|---|
| +5V | 4.2A | 6.ØA |
| -15V | Ø.6A | 8.ØA |

*Standby current must also be supplied for the remaining memories.

Table 2-3: Power Requirements for Two Interleaved Memories

# Section 3

# Functional Description

## 3.1 INTRODUCTION

This section describes the operation of the PM-1116B memory system. Figure 3-1 contains an overall block diagram of the system. The diagram shows the relationship between the stack, timing and control, addressing, sink and drive switches, current sources and data loop circuits.

## 3.2 DATA TRANSFER SEQUENCE

This subsection describes the data transfer sequence between the memory and the central processor and I/O devices.

The memory receives commands, address, and data information from the Unibus. The bus master places address and control information on the Unibus lines, waits 150ns to allow for bus delay and memory internal decode delay, and then initiates master sync (MSYNL).

The memory decodes the address information from the bus and if it does not fall within the memory's address, MSYNL is blocked. The memory is not accessed and therefore remains in a stand-by state.

When a memory is selected, it sets its internal memory busy flip-flop to indicate that it is cycling and that it will not accept further commands until its present cycle is completed.

For a read cycle (DATI), when data is available, the memory places the data on the bus and asserts SSYN. After the bus master receives SSYN, it waits 75ns to allow for the maximum bus delay and then strobes data and clears MSYNL. The memory receives the cleared MSYNL and clears SSYN.

After a 75ns delay the bus master removes address and control lines from the bus. The bus is now free and may be taken by another device. All devices must go through the priority arbitration circuit at the processor in order to gain control of the bus.

The memory is still cycling at this point and cannot be accessed until it finishes its present cycle. MSYNL can be asserted while the memory is in cycle. When the memory completes its present cycle, the memory busy flip-flop is reset, enabling the memory to accept another command from the Unibus.

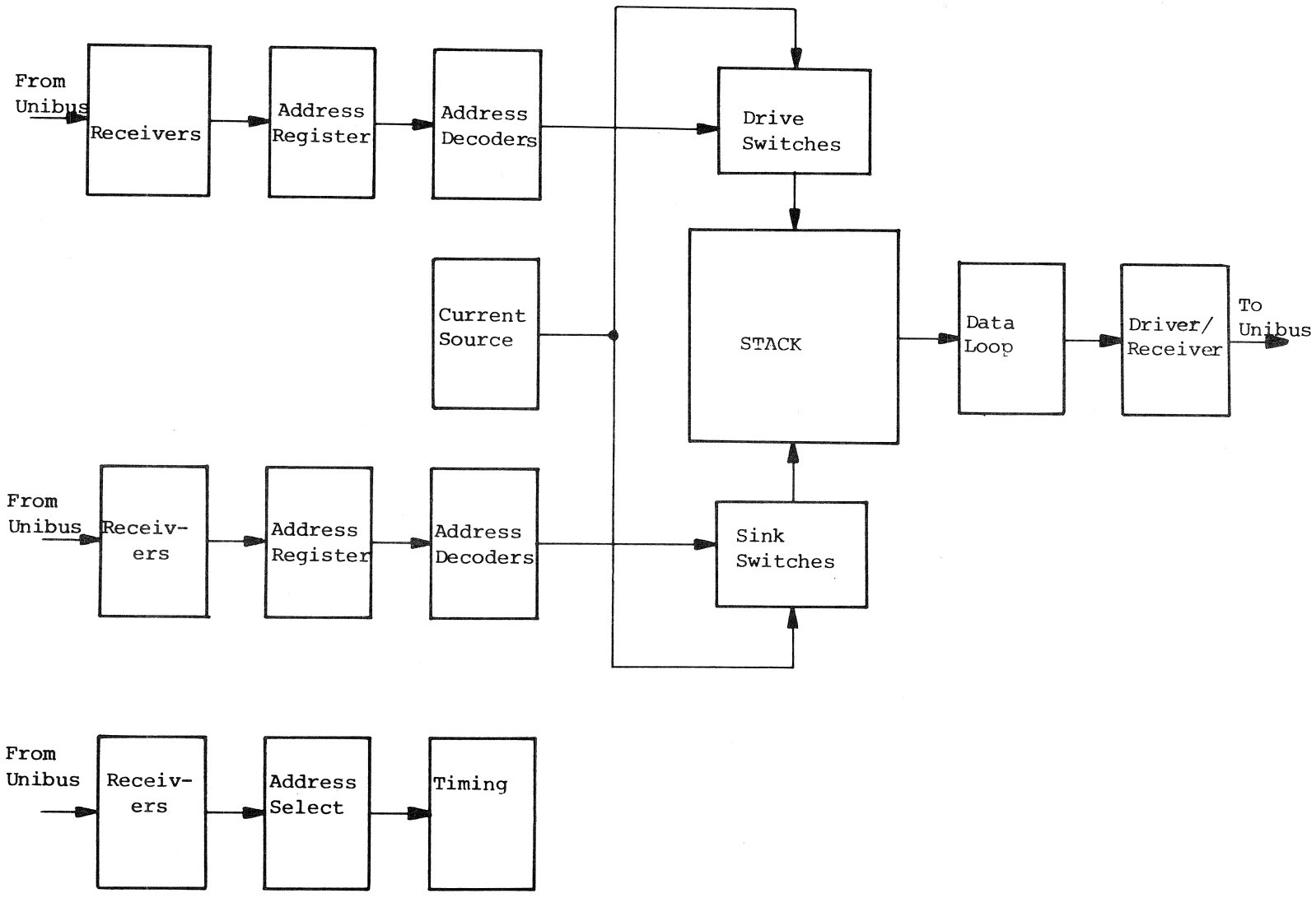



Figure 3-1: Memory Block Diagram

For a write cycle (DATO), the memory asserts SSYN after it strobes data from the bus into its data registers. The bus is released but the memory must finish its present cycle before being accessed again.

## 3.3 INTERFACE SIGNALS

The memory interface signals and their functions are described in the following paragraphs. Interface timing is shown in Figure 3-2.

MASTER SYNC (MSYNL): MSYNL is an input signal which initiates a memory cycle when the following conditions are met:

- Memory is not busy.
- The address falls within the memory block.
- SSYN from the previous cycle has been cleared.

SLAVE SYNC (SSYNL): SSYNL is output from the memory as an acknowledgment to the bus master in response to MSYNL.

DATA LINES (DØØL-D15L): The 16 data lines are used to transfer information between the memory and the master device. Data input to the memory and data output from the memory are transferred on the same lines.

ADDRESS LINES (AØØL-A17L): The address lines are used by the master device to select a particular memory location. AØØ, the least significant bit, is used to decode upper or lower byte during a byte mode operation. AØ1-A14 are used to decode one location within a 16K address block. A15-A17 are used to decode the 16K address block.

DC LINE (DCLO): This signal emanates from the power supply and is wired from the power connector card slot to the Unibus on all system units. It remains cleared as long as all DC voltages are within specified limits. If an out of tolerance voltage condition occurs, DCLO is asserted by the power supply. The PM-1116B core memory uses the DCLO signal to inhibit further operations.

## 3.4 MODES OF OPERATION

The two control lines CØ and C1 in conjunction with address bit AØØ are used to select one of five modes of operation. Table 3-1 shows the five modes. The operational modes are described in the following subsections.

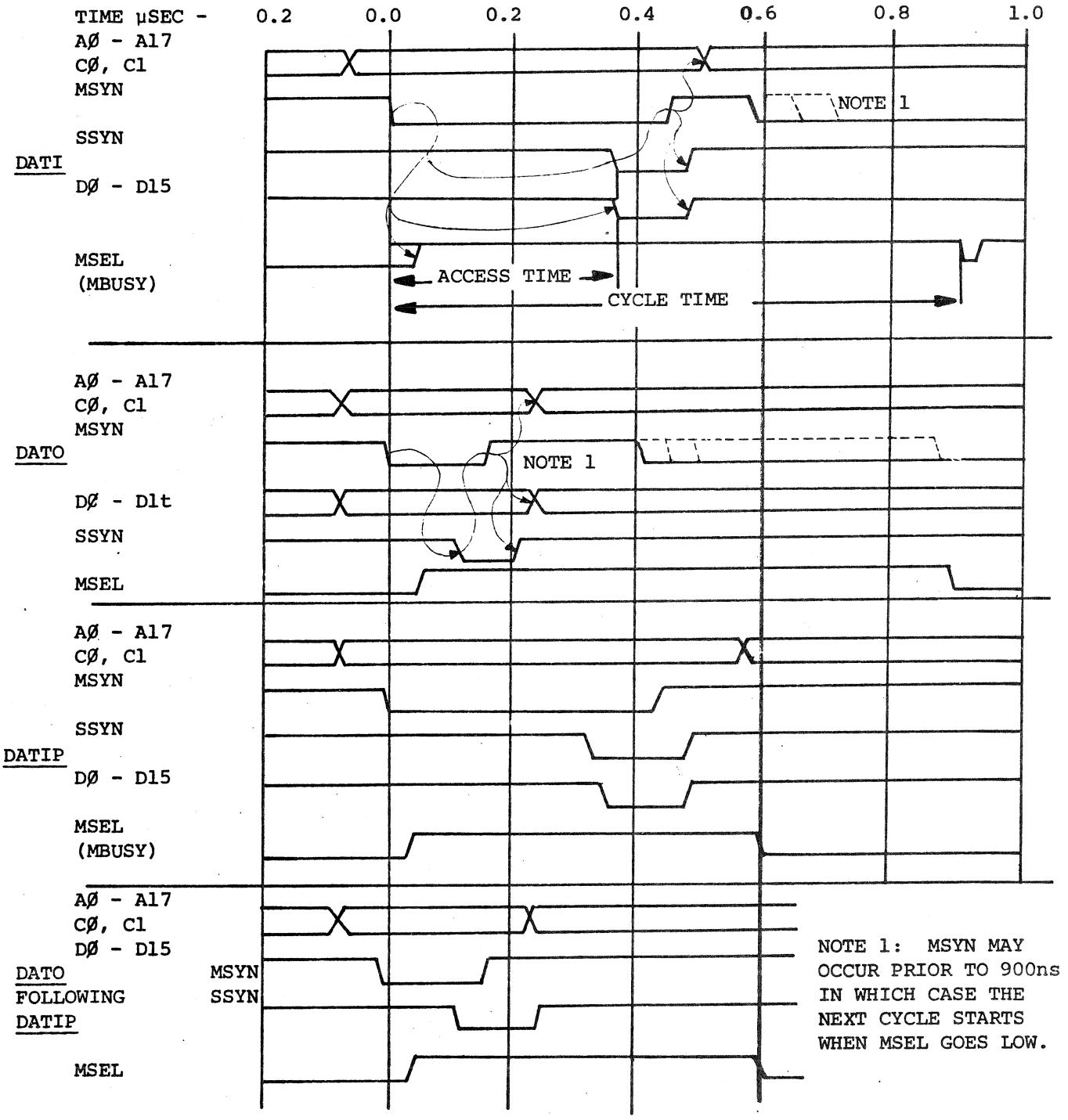



Figure 3-2: **Interface Timing Diagram**



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 3-4 |

| Operation | Command | Control Lines | | Address Line |
|---|---|---|---|---|
| | | CØ | C1 | AØ (LSB) |
| Read-restore | DATI | High | High | x |
| Read-pause | DATIP | Low | High | x |
| Clear-write | DATO | High | Low | x |
| Clear-write byte Ø<br>Read-restore byte 1 | DATOB Ø | Low | Low | High |
| Clear-write byte 1<br>Read-restore byte Ø | DATOB 1 | Low | Low | Low |

NOTES: 1. High state is defined as inactive state (+2.V to +5V). Low state is defined as active state (0V to +0.8V).
2. DATIP command must be followed by DATO or DATOB.
3. X indicates that the value is irrelevant.

Table 3-1: Memory System Modes of Operation

### 3.4.1 READ-RESTORE (DATI)

This is a conventional read-restore cycle. During the first half cycle, the memory reads the data from the selected core location and transfers it to the data bus; it then restores the data back into the same memory location during the write half cycle. This last step is necessary because the core memory is a destructive read-out device. During the read half cycle, the memory strobes the data from the selected location into its data registers and then puts it on the Unibus data lines. During the second part of the cycle, write half cycle, the memory restores the data back into the same memory location from the data registers.

### 3.4.2 READ-PAUSE (DATIP)

In this mode, the memory performs only the read half cycle and then pauses until accessed again. Since the data is destroyed whenever the memory reads from a particular memory location, it must be restored. However, sometimes it is not advantageous to restore the information immediately after reading because the same memory location is going to have new data written into it. By performing a read-pause cycle followed by a write cycle, the restore (write) half cycle from the first cycle and the clear (read) half cycle of the preceding cycle are bypassed. This decreases the total memory cycle by a factor of two. Because no restore cycle is used a read-pause cycle must always be followed by a write cycle (DATO or DATOB) on the same address location or the data will be destroyed.

### 3.4.3 CLEAR-WRITE (DATO)

This is a conventional clear-write cycle. The memory first performs the clear half cycle to clear the selected cores. This clear operation is identical to a read operation except that the data is not read. (Sense amp strobe is inhibited.) The memory then strobes data from the Unibus data lines into its data register, and performs the write half cycle. Whenever a clear-write (DATO) follows a read-pause (DATIP), the memory skips the clear half cycle and proceeds immediately with the write half cycle.

### 3.4.4 CLEAR-WRITE BYTE (DATOB)

The Unibus master under certain conditions may wish to write new data onto one byte only. The memory executes this request by performing a read-restore on one byte and a clear-write on the other byte.

The clear-write byte cycle is similar to a clear-write cycle except that one byte is transferred from the data bus into the memory data register instead of the full two byte word.

Address bit AØØ determines if the lower byte (DØ-D7) or the upper byte (D8-15) is to be transferred. A read-restore cycle is performed on the unselected byte, but the memory does not transfer the data onto the Unibus.

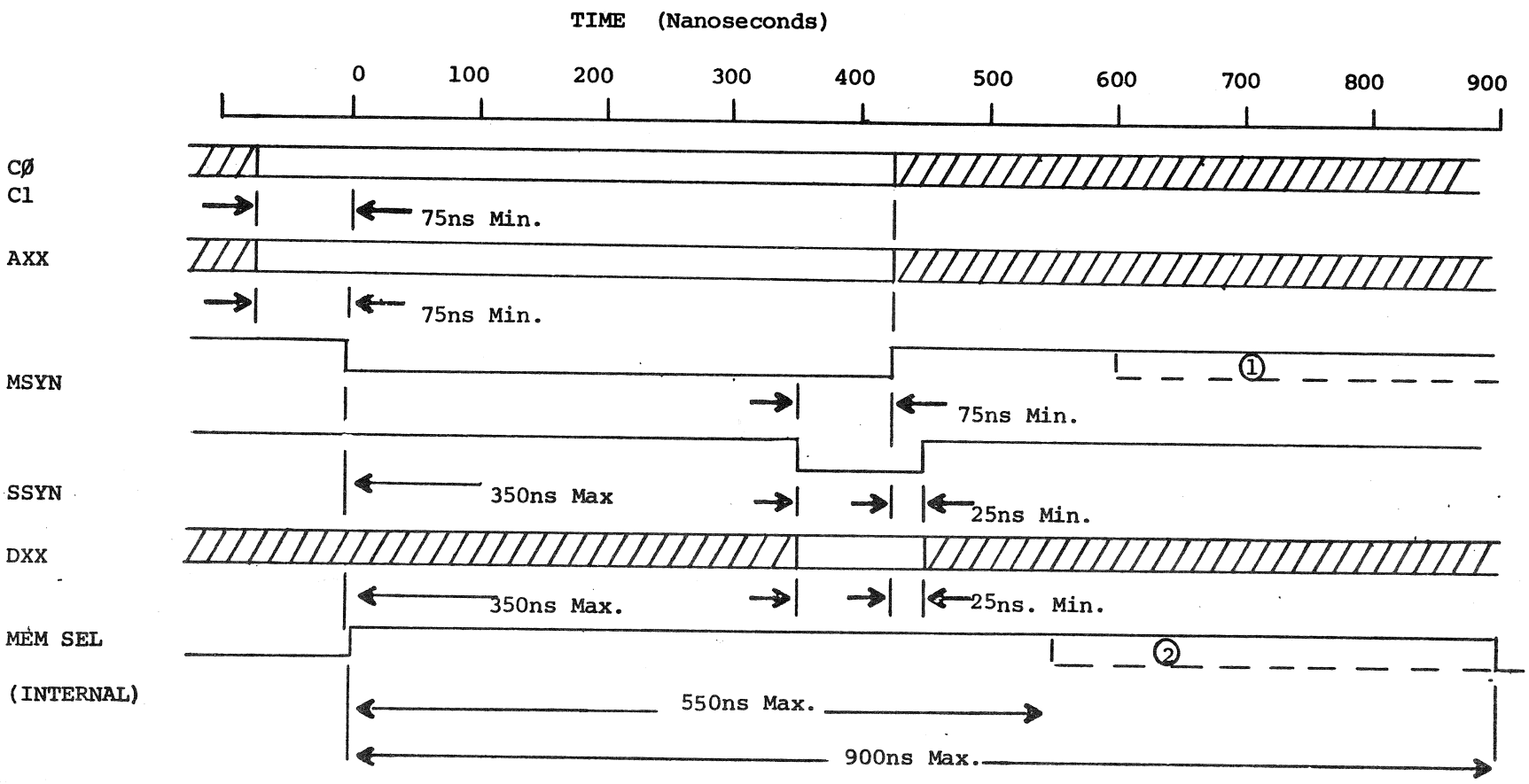
## 3.5 TIMING AND CONTROL

The master sync command (MSYNL) from the Unibus initiates the read timing for the memory card. Normally read timing is followed by write timing except for the cycle following a read-pause mode where only write timing is generated.

Timing for read and write cycles is shown in Figures 3-3 and 3-4. Timing and control functions for the various modes of operation are explained in the following:

Read-Restore Cycle (DATI)

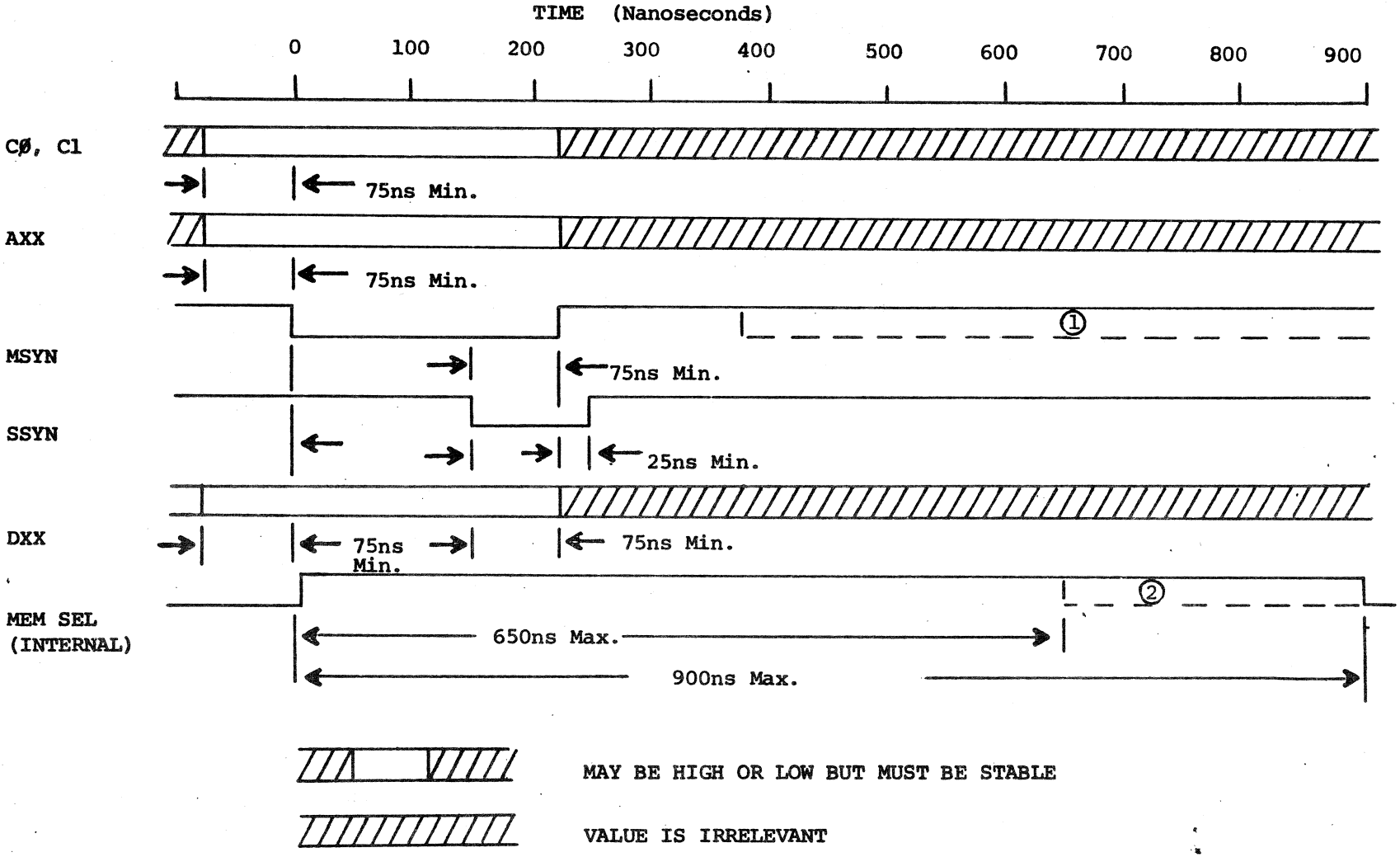
1. Read timing followed by write timing is generated.
2. Data registers (CLRØ and CLR1) are cleared at the beginning of the cycle.
3. Sense amplifier strobes are generated for both bytes.
4. Slave sync pulse (BUS SSYNL) is sent to the processor at sense amplifier strobe timing.
5. Data out is strobed onto the Unibus for both bytes.




1 MSYN MAY BE ASSERTED BEFORE 900ns; MEMORY WILL RESPOND WHEN READY.

2 THESE TIMES ARE FOR DATIP CYCLE.

Figure 3-3: DATI and DATIP Timing




1 MSYN MAY BE ASSERTED BEFORE 900ns; MEMORY WILL RESPOND WHEN READY.

2 THIS TIME FOR A DATO OR DATOB FOLLOWING A DATIP.

Figure 3-4: DATO and DATOB Timing

Read-Pause Cycle (DATIP)

1. Read timing is generated.
2. Data registers are cleared.
3. Sense amplifier strobes are generated for both bytes.
4. Slave sync is sent at sense amp strobe timing.
5. Pause flip-flop is set and data out is strobed onto the Unibus.

Clear-Write Cycle (DATO)

1. Read timing followed by write timing is generated.
2. Data registers are cleared.
3. Data is loaded from the data bus into the memory data registers for both bytes.
4. Slave sync is sent after the data registers are loaded from the data bus.

Clear-Write Byte (DATOB)

1. Read timing followed by write timing is generated.
2. Data registers are cleared.
3. Address bit AØØ is examined. Byte flip-flop is set depending on the state of AØØ.
4. Data is loaded into the data registers only for the byte that performs the clear-write.
5. Slave sync is sent after the data registers have been loaded.
6. Sense amp strobe is generated but is inhibited for the byte that performs a clear-write.

Operation Following A Read-Pause Cycle

1. Write timing is generated.
2. Slave sync is sent at the beginning of the cycle with CLK2H.
3. Pause flip-flop is reset.
4. In byte mode, the data that was read during the previous read-pause cycle is restored to only one byte while the memory performs a write on the other byte.

## 3.6 STACK ASSEMBLY

The PM-1116B stack assembly is a 16384 x 16 bit 3-D, 3-wire (common sense/ inhibit) core matrix arranged in a planar configuration of thirty two 64 x 128 core arrays. The stack assembly, which also contains decoding diodes, plugs directly into the back of the memory card to form the memory card assembly.

Each dimension carries 8 drive and 16 sink switches with two diodes per line. There are two sense/inhibit lines for each bit. Each sense/inhibit line threads through 8192 cores for a total of 16384 cores.

The sense/inhibit lines are terminated with two 150 ohm resistors to ground at the sense amplifier and 75 ohms at the inhibit switch. The array is driven with positive Y and negative X current during a read operation and with negative Y, positive X and negative inhibit current during the write operation. This arrangement of the core array permits the "shared drive" scheme used with the PM-1116B memory. This minimizes the number of components used and thus improves the system reliability. See subsection 3.7.3 for more details.

## 3.7 X AND Y CURRENT DRIVE CIRCUITRY

The X and Y current drive scheme used in the PM-1116B memory card may be broadly divided into three basic sections:

- Address registers and decoders
- Current regulators
- Current switches

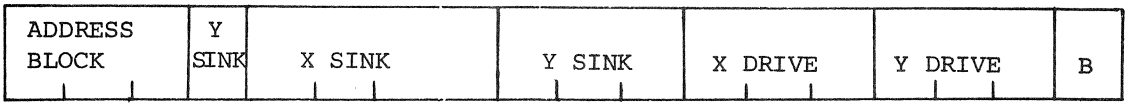
### 3.7.1 ADDRESS REGISTERS AND DECODERS

The address registers store the address information from the Unibus address lines BUS AØØ through BUS A17. This information is available at the beginning of each cycle. The address registers retain this information until the beginning of another cycle in the memory.

The address decoders convert the address information in the address registers to actual core locations as seen by the memory. However, address bit AØØ is used only for selection of byte Ø or byte 1 during a byte mode (DATOB) and is not used for memory address locations.

Figure 3-5 shows the data format for the address word. Address bits AØ1, AØ2 and AØ3 are used to select one of eight Y drive switches and address bits AØ7, AØ8, AØ9, and A14 are used to select one of sixteen Y sink switches. Address bits AØ4, AØ5, and AØ6 are used to select one of eight X drive switches and address bits A1Ø, A11, A12, and A13 are used to select one of sixteen X sink switches.

When the memory system is interleaved, address bit A15 is interchanged with address bit AØ1 at the input of the memory board. Since address bit AØ1 is the least significant bit for address locations, it serves as a mean to locate all even address locations in one memory and all odd address locations in another memory.




ADDRESS BLOCK - Selects one 16K address block.
Y SINK - Selects one of sixteen Y sink switches.
X SINK - Selects one of sixteen X sink switches.
X DRIVE - Selects one of eight X drive switches.
Y DRIVE - Selects one of eight Y drive switches.
B - Byte select for byte mode operations.

Figure 3-5 : Address Data Format

### 3.7.2 CURRENT REGULATOR

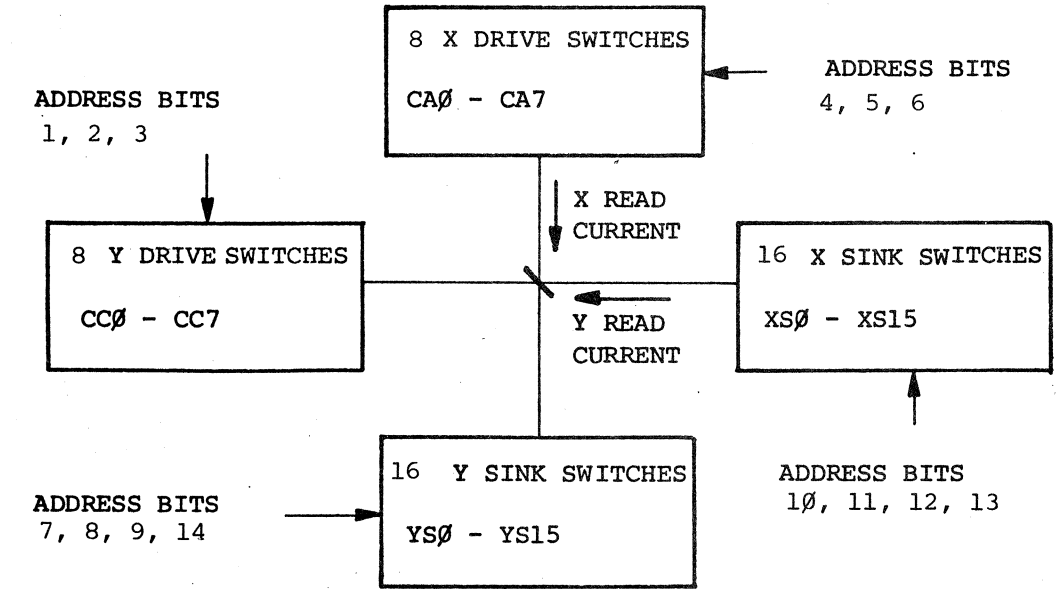
The current regulator section consists of the two regulated current sources + I STAB and - I STAB. Both sources drain current from +20V supply and sink to ground (OV). The +I STAB source is used to drive positive current into the stack required by Y-read and X-write operations. Both + I STAB and - I STAB sources are regulated against a common reference voltage that is controlled by a thermistor which changes its resistance with temperature changes and causes the drive currents to compensate for the changes in temperature. The drive current is factory set at 385ma at 25°C.

### 3.7.3 CURRENT SWITCHES

The current switches may be functionally separated into two categories; the drive switches and the sink switches. However, all the current switches (including the inhibit switches) used in the PM-1116B memory system are similar in electrical design. They contain a floating transformer coupled transistor as the switch. The decoders, when activated by the timing pulses, draw current through the primary winding which induces current in the secondary winding across the base/emitter of the transistor causing it to turn on.

One unique feature of the drive organization is the "shared-drive" scheme. In this design approach, the current switch that drives Y read current pulse is also used to drive Y write current pulses. Thus, by using the "shared-drive" scheme, the memory uses only half the drive switches that are used by the conventional design approach. The "shared-drive" scheme is illustrated in Figure 3-6.

READ HALF CYCLE




WRITE HALF CYCLE

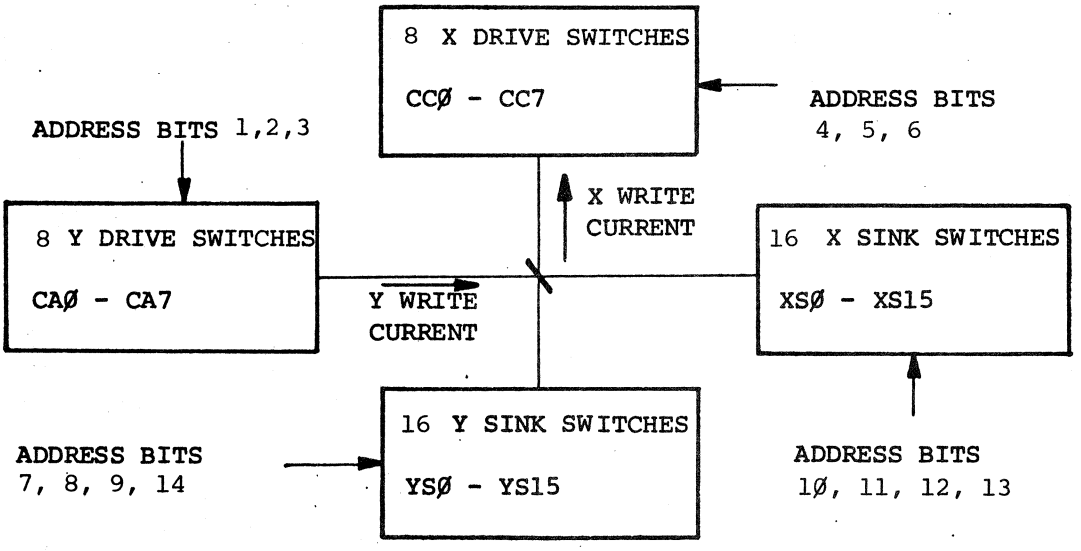



Figure 3-6 : **Shared Drive Scheme**



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 3-12 |

FORM 000021

## 3.8 DATA LOOP CIRCUITRY

The data loop circuitry consists of the receiver, data register, sense amplifier, inhibit driver and output driver. The description of the timing signals for the data loop is contained in Section 4.

The PM-1116B core stack contains two 8K sense/inhibit loops for each bit. This makes it necessary to decode which sense/inhibit loop is being accessed. In order to accomplish this, each 8K sense loop is connected to its own sense amplifier and inhibit driver. Address bit A14 is used to decode between the upper and lower 8K sense/inhibit loops.

During a clear-write cycle, the data registers are first reset, then data is strobed in from the Unibus. For the second half cycle, the memory performs a write with the data in the data registers controlling the inhibit drivers. If a Ø is to be written, the inhibit driver is turned on. The inhibit current opposes the Y write current thereby leaving the core in its cleared state (Ø state). If a 1 is to be written, the inhibit driver is turned off causing a full current pulse to be applied to the core, switching it to the one state. Data registers are reset at the beginning of each cycle except the cycle following a read-pause cycle.

The sense amplifier IC is referenced to a specific threshold voltage (VTH) and when the timing strobe is applied, it will cause its output to set to either a one or a zero. A zero output which did not exceed the threshold voltage during the strobe timing will leave the data register in the reset state. A one signal will exceed the threshold voltage thereby setting the data register.

The threshold voltage for the sense amplifier IC is approximately 18 millivolts and is generated by the resistor voltage divider network from the +5V supply.

## 3.9 INHIBIT DRIVERS

The basic function of the inhibit drivers is to supply half current pulse at the selected core location such as to oppose the Y current pulse and thereby inhibit the core from switching.

In order for the inhibit driver to counteract the write-pulse current, inhibit current must pass through the selected core in the same direction as the read current pulse.

The inhibit drivers circuits used in the PM-1116B memory system are floating transformer coupled transistor switches. Primary current flows in the transformer only when the data register is in its reset state (Ø state) when inhibit timing signal is activated.

# Section 4

# Theory of Operation

This section describes the logic diagrams for the PM-1116B memory. Appendix C contains the logic diagrams which are referenced by sheet number at the beginning of each subsection.

## 4.1 ADDRESS STRAPPING CIRCUIT (SHEET 1)

Master sync (BUS MSYNL) from the processor initiates the memory cycle. The memory can respond to a BUS MSYNL only if it is strapped to the address block addressed by the processor.

Address strapping plug TB1 is used to strap the memory to the address blocks. Table 2-2 shows the jumper configurations for plug TB1.

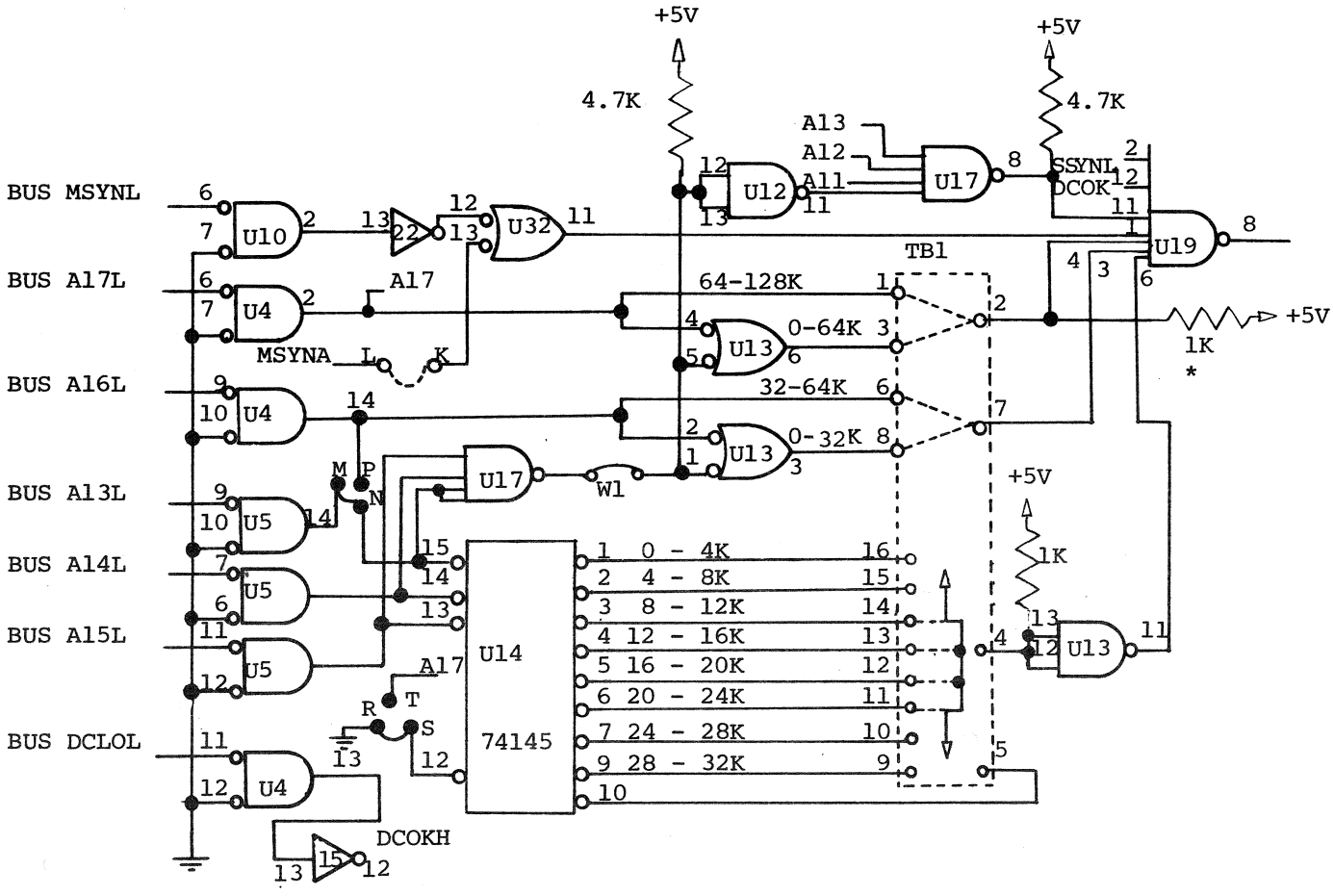
The address strapping circuit is shown in Figure 4-1.

Address lines A13-A15 are decoded by decoder U14. Address blocks up to 32K are decoded in 4K increments. Address blocks up to 64K may be decoded in 8K increments. To enable the decoding up to 64K, cut the etch from N to M and add a jumper from N to P.

Processors that do not have the memory management option can address 32K words. The top 4K word locations are reserved for peripheral and register addresses and the user has only 28K of program instead of the full 32K.

### 31K Option

The PM-1116B provides the user with the option to reserve 1K of memory for I/O instead of the normal 4K. To enable this option, the W1 jumper must be installed as shown in Figure 4-1 and the memory strapped as 16K-32K. This allows the memory to respond to addresses between 16K and 31K instead of between 16K and 28K. No I/O devices may be assigned addresses between 28K and 31K; only the upper 1K from 31K to 32K may be used.




NOTE: For strapping plugs 700066-162 through 600077-167. Remove jumper from N to M and install between N to P.

NOTE: Insert W1 for 31K operation. For 56K-72K operation remove jumper between R and S and install between S and T. Use 700066-164 strapping plug.

* Also install 1K ±5%, 1/4 W resistor between U19-4 and U3-8 (+5V).

Figure 4-1: Address Strapping Circuit

## 4.2 MEMORY INITIATE TIMING CIRCUIT (SHEET 1)

All timing signals are generated by CLK1H and CLK2H. Figure 4-2 shows the timing circuit.

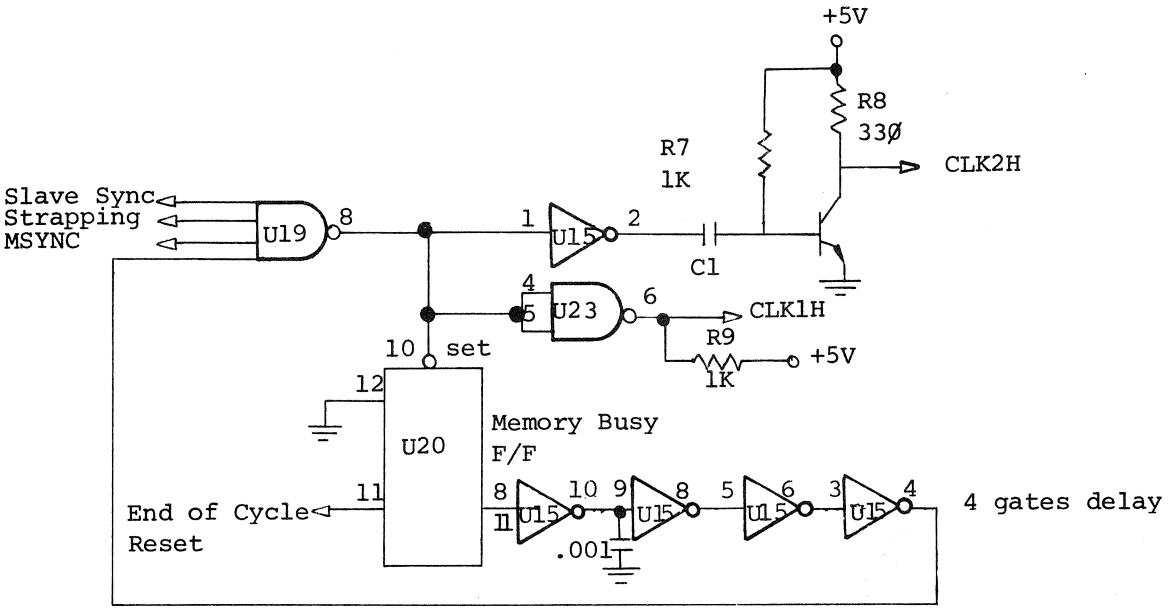



Figure 4-2: Memory Timing Circuit

When the bus master initiates a master sync pulse, if the memory is strapped to the memory block addressed by the processor, and if the slave sync signal is cleared (SSYNC flip-flop is reset), and if the memory is not cycling (memory busy flip-flop is reset, $\overline{Q}$ output = high) then U19 output goes low.

U19 output causes memory busy flip-flop U20 to go low. After a four gate delay U19 input is set low forcing its output back to a high forming clock pulse CLK1H. CLK2H is formed by the trailing edge of CLK1H.

The memory busy flip-flop U20, sheet 1/3C is set at the beginning of the cycle at U20-10. Once U20 is set, it will block the memory at U19-5 to inhibit any further access into the memory until the cycle is complete. U20-11 resets U20 flip-flop at the end of the cycle. The function of the four inverters (U15-74HØ4) from U20-8 to U19-5 is to create a time delay for the width of the clock pulse CLK1H at U22-4.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-3 |

4.2.1 READ HALF CYCLE TIMING

The read half cycle timing source is shown in Figure 4-3. Read half cycle timing is initiated by CLK1H for each memory cycle except the cycle following a read-pause (DATIP). A DATIP cycle must always be directly followed by a write cycle or a write byte cycle on the same address.

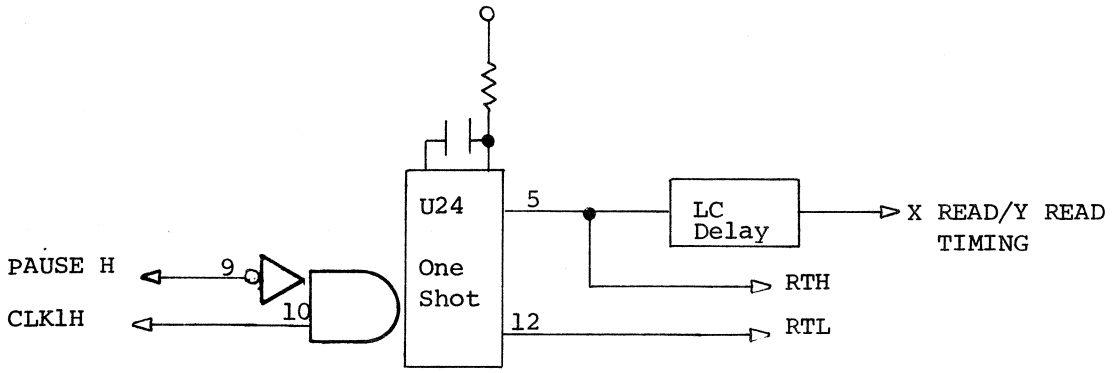



Figure 4-3: Read Half Cycle Timing

One shot (U24) output RTH is lab set to 300ns.

4.2.2 WRITE HALF CYCLE TIMING

Write half cycle timing is shown in Figure 4-4. One-shot U26 output WTH is lab set to 300ns. Write timing is followed by either read timing (PAUSEL = high) or by CLK2H (PAUSEH = high).



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-4 |

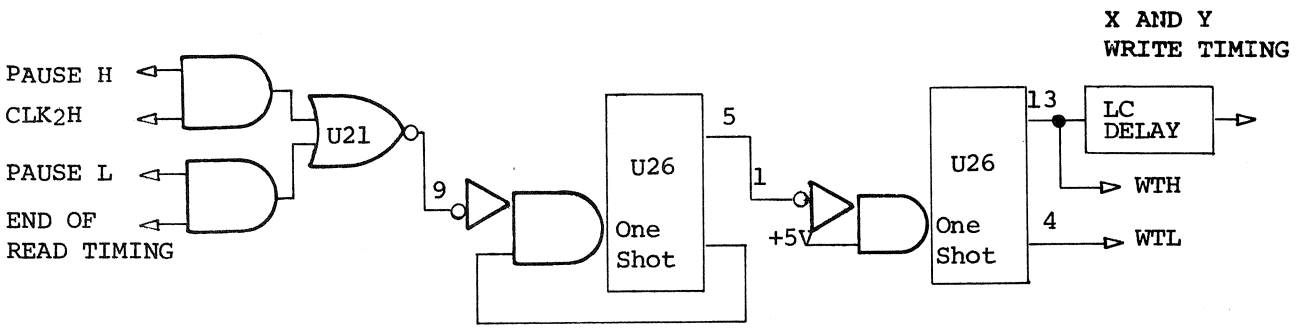



Figure 4-4: Write Half Cycle Timing

4.2.3 READ-PAUSE TIMING

Read-pause timing is generated as function of the read-pause flip-flop as shown in Figure 4-5.

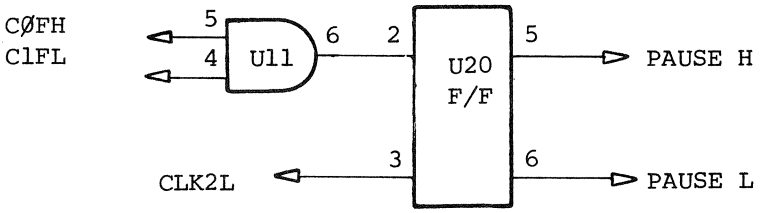



Figure 4-5: Read-Pause Flip-Flop



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-5 |

U20 is a D-type positive edge flip-flop. During read-pause mode (CØFH and ClFL both high), PAUSEH output at pin 5 of U20 is set high by the trailing edge of the CLK2L timing pulse. The trailing edge of CLK2L occurs 130ns after TØ (see internal timing diagram, Figure 5-1). The pause flip-flop is reset at the trailing edge of CLK2L for all modes except read-pause.

During the read-pause cycle, end of cycle one-shot U24-2 triggers 360ns after time TØ with PAUSE high at the trailing edge of RTH. See schematic diagram 700295, sheet 1/B3.

For the cycle following a read-pause, the pause flip-flop does the following:

- Inhibits read-timing (U24-9)
- Enables write timing with CLK2H (U21-9)
- The end of cycle reset one-shot U24-2 is triggered 130ns after time TØ with RTH high and PAUSEH low.
- During a byte mode operation, clear data register pulse (CLRØL or CLRlL) is inhibited or enabled depending upon the state of address bit Ø as shown in Figure 4-6.
- PAUSEL = low (U32-5 sheet 2/6B) inhibits X and Y sink switches from turning on with CLKlH. Since read timing is also inhibited X and Y sink switches turn on with WTL (Ull-9).

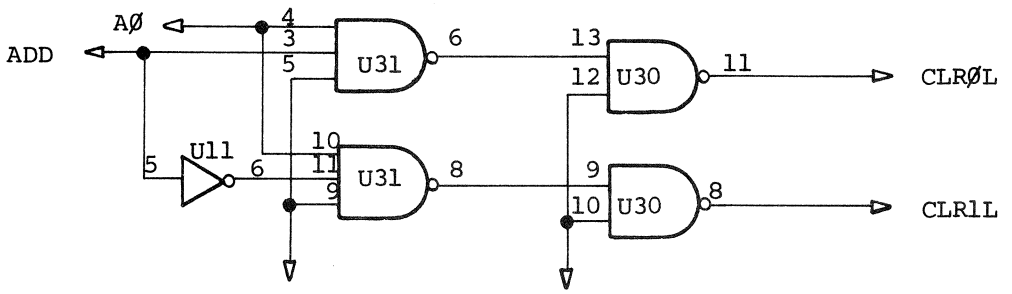



Figure 4-6: Byte Selection Following a Read-Pause Operation

### 4.2.4 SENSE AMPLIFIER STROBE TIMING

Sense amplifier strobe is generated as shown in Figure 4-7.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-6 |

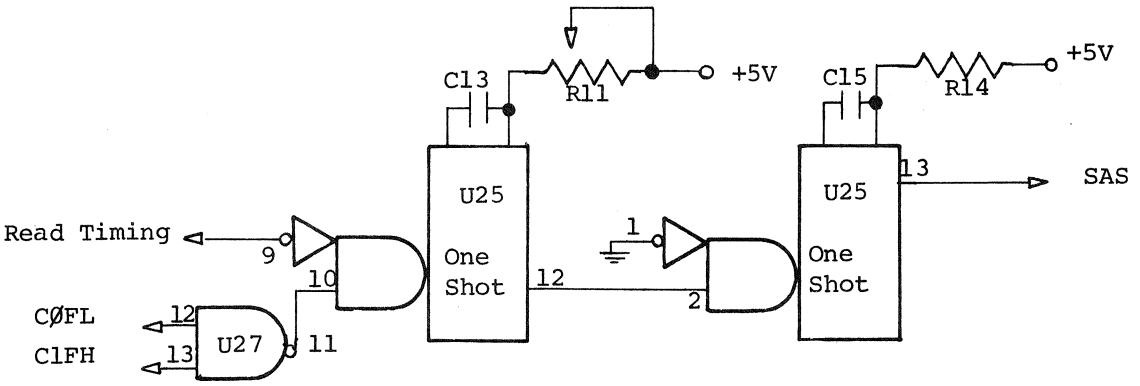



Figure 4-7: Sense Amplifier Strobe Timing

SAS is inhibited in clear-write mode when CØFH and C1FL are both high. It is enabled for all other modes. The pulse width of the strobe is a function of R14 and C15. Strobe timing is a function of C13 and variable resistor R11. The sense amplifier strobe is set with reference to the X read pulse measured at the stack input.

## 4.3 BYTE MODE OF OPERATION (SHEETS 1 AND 2)

The two byte modes of operation are generated as shown in Table 4-1.

| MODE | CONTROL LINES CØ | C1 | ADDRESS BIT ØØ | FUNCTION |
|---|---|---|---|---|
| DATOB Ø | L | L | H | Clear-Write Byte Ø<br>Read-Restore Byte 1 |
| DATOB 1 | L | L | L | Clear-Write Byte 1<br>Read-Restore Byte Ø |

NOTE: All signal levels are measured at the Unibus.

Table 4-1: Byte Mode Selection

Byte Ø is defined as data bits DØ-D7.
Byte 1 is defined as data bits D8-D15.

Figure 4-8 illustrates the byte flip-flop.

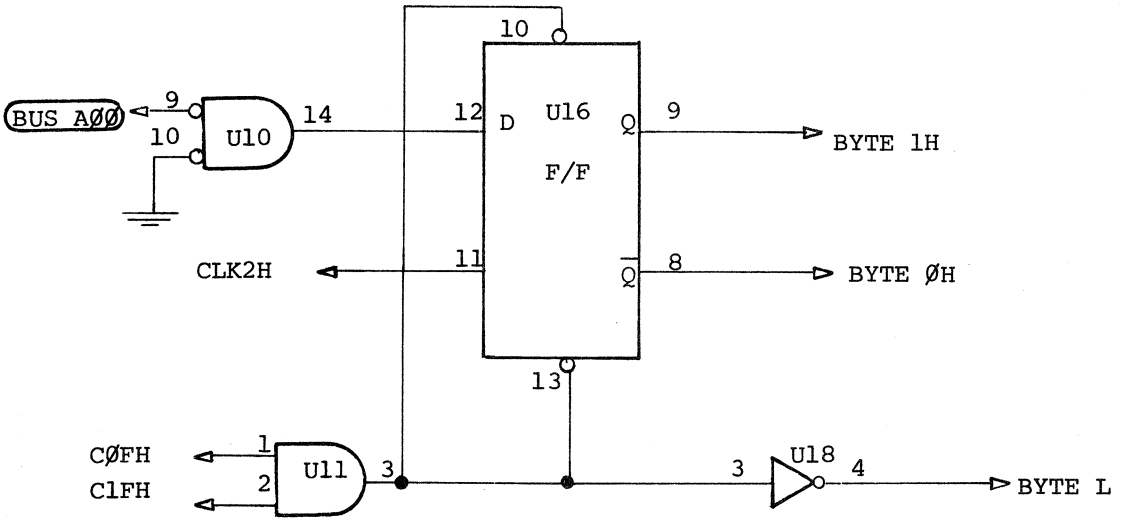



Figure 4-8: Byte Flip-Flop

The byte circuit operates as follows:

For all modes other than byte mode, clear and preset inputs of U16 flip-flop are set low (BYTEL = high). Q and $\overline{Q}$ outputs of byte flip-flop are both high (BYTE ØH = high and BYTE 1H = high). Byte circuits are shown in Figure 4-9.

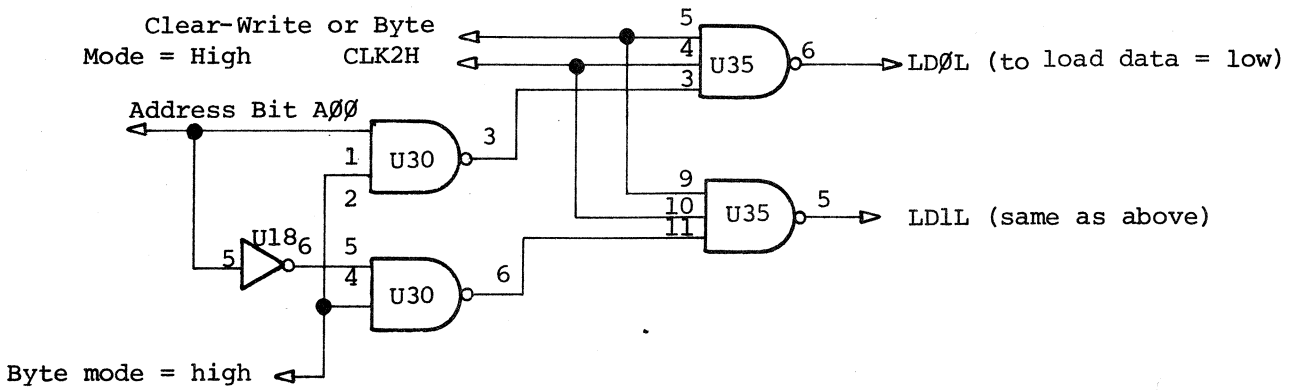



Figure 4-9: Byte Circuits (Continued)



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-8 |

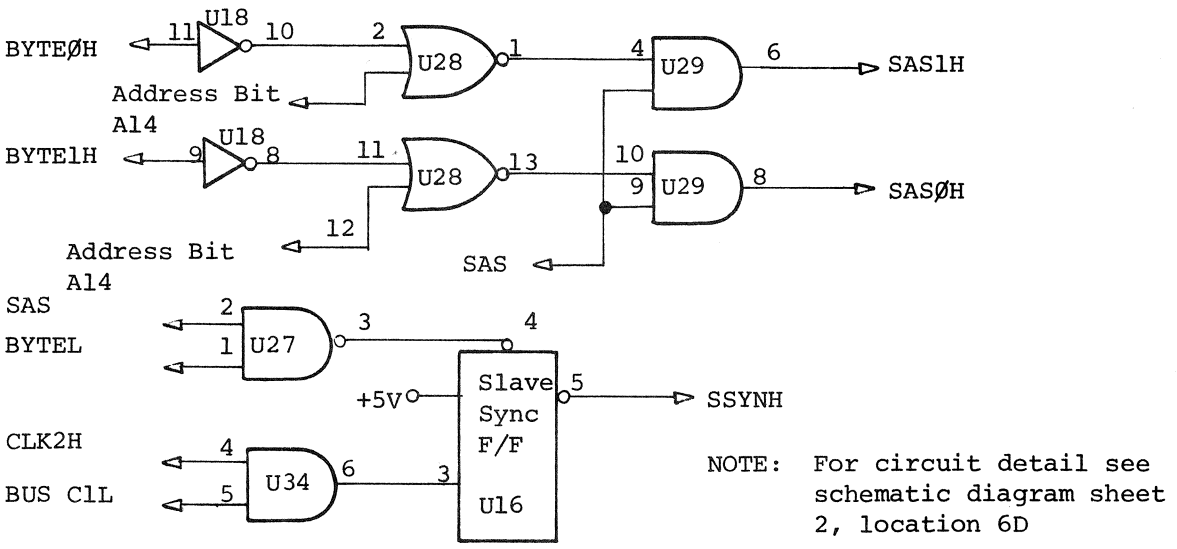



Figure 4-9: Byte Circuits

During non-byte operation both sense amp strobes are enabled (BYTEØH and BYTE1H = high). BYTEL = high enables the slave sync flip-flop which is set by CLK2H with BUS C1L = C1 = high. Also during byte mode, the clear and preset inputs of U16 flip-flop are high.

Table 4-2 illustrates the various functions of the byte mode cycle.

| MODE | FUNCTIONS |
|---|---|
| DATOB Ø<br><br>CLEAR-WRITE BYTE Ø,<br><br>READ-RESTORE BYTE 1 | 1. SAS for byte Ø is inhibited.<br>2. SAS for byte 1 is enabled.<br>3. Load data byte Ø (LDØH) enabled.<br>4. Load data byte 1 (LD1H) inhibited.<br>5. For the cycle following a read-pause only: clear data register byte Ø (CLRØ) enabled and clear data register byte 1 (CLR1) inhibited. |
| DATOB 1<br><br>CLEAR-WRITE BYTE 1,<br><br>READ-RESTORE BYTE Ø | 1. SAS for byte Ø is enabled.<br>2. SAS for byte 1 is inhibited.<br>3. Load data byte Ø (LDØH) inhibited.<br>4. Load data byte 1 (LD1H) enabled.<br>5. For the cycle following a read-pause only: clear data register byte Ø (CLRØ) is inhibited and clear data register byte 1 (CLR1) is enabled. |

Table 4-2: Byte Mode Functions



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-9 |

## 4.4 SLAVE SYNC CIRCUIT (SHEET 2)

Slave sync is an acknowledgement pulse from the memory to the processor in response to a master sync pulse.

Slave sync circuit is shown in Figure 4-10.

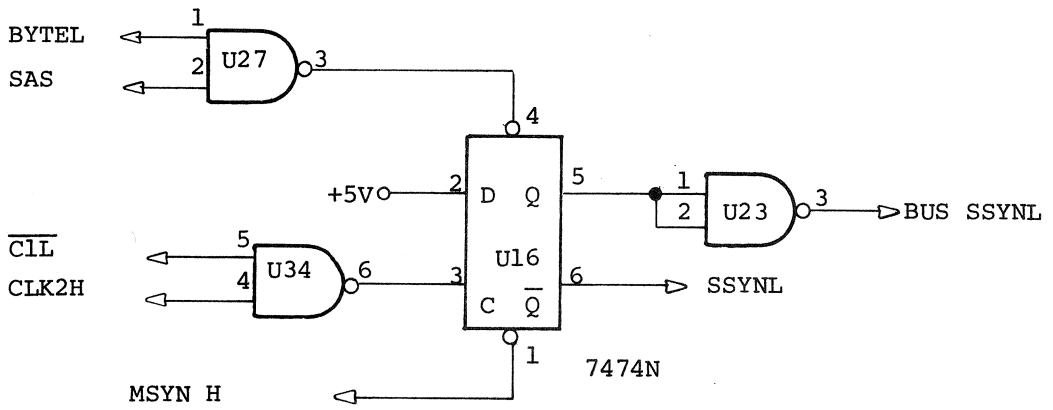



Figure 4-10: Slave Sync Circuit

U16 is a D-type positive edge triggered flip-flop. It is set with sense amplifier strobe during a read-restore (DATI) or a read-pause (DATIP) when BYTEL = high and SAS is enabled. During a clear-write (DATO) or a clear-write byte (DATOB) it is set at the beginning of the cycle with CLK2H. (See internal timing diagram Figure 5-1.)

The slave sync flip-flop is reset each cycle with the trailing edge of master sync pulse. U23 output driver is an open collector driver SN7438.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-10 |

## 4.5 POWER FAIL - DC LOW SIGNAL (DCLOL) (SHEET 2)

BUS DCLOL signal is the Unibus power fail indicator. It remains high (+5V) as long as all power supplies (processor and peripherals) are within their specified limits. It will go low (OV) whenever DC voltages are out of their specified limits. This line is wired on the Unibus. DCLOL is also used during power on sequence to inhibit the memory from starting the cycle before all the DC voltages are within their specification.

DCLOL circuit is shown in Figure 4-11.

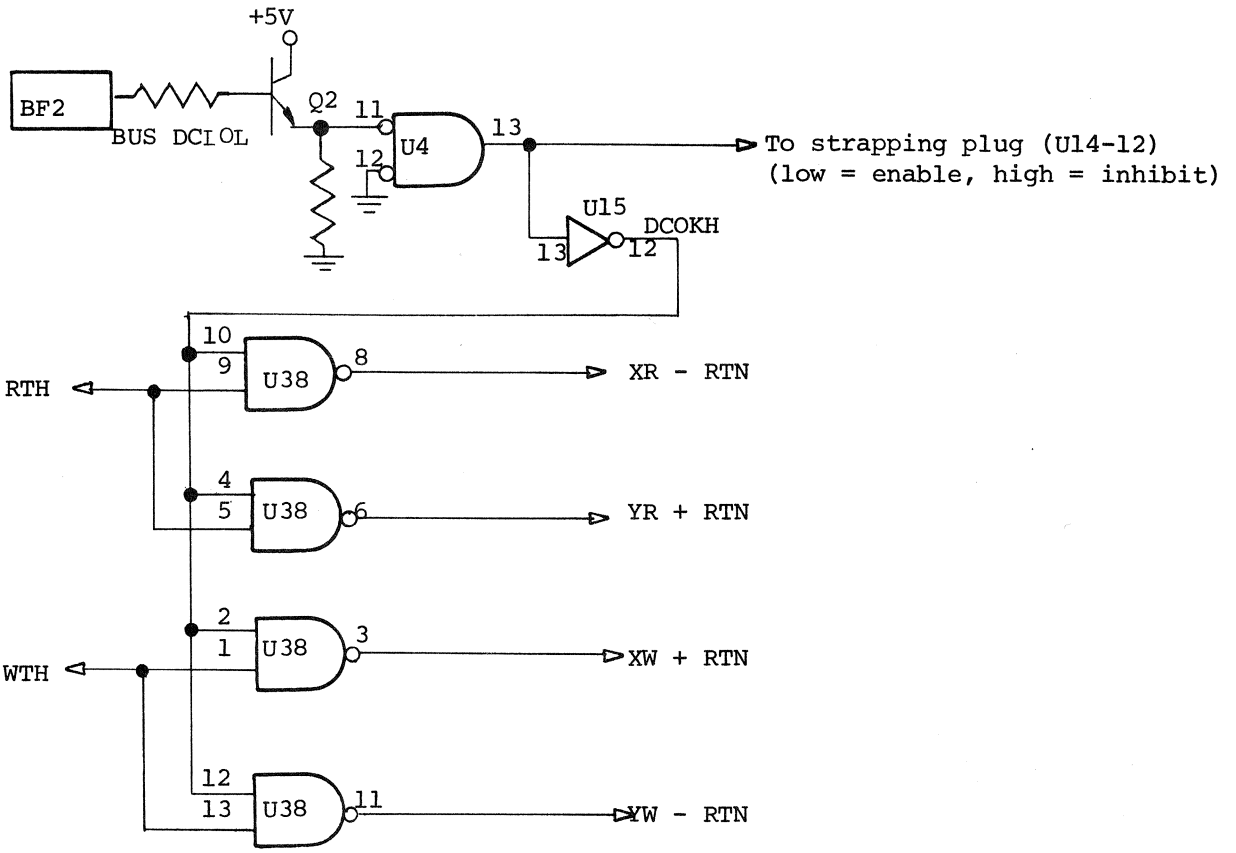



Figure 4-11: DCLO Circuit

When the memory power supply is first turned on, BUS DCLOL line is held at ground level (ØV). It remains at this level until both the +5V and the -15V supplies are within their specifications.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-11 |

BUS DCLOL = low inhibits current path from the Y sink switches to the -15V supply during read half cycle (YR-RTN) and to the +5V supply during write half cycle (YW-RTN). It also blocks the X sink switches to the +5V supply during read half cycle (XR-RTN) and to the -15V supply during write half cycle (XR+RTN).

BUS DCLOL low forces address strapping decoder IC (U14-12) high. This blocks memory initiate gates U19-6 and U13-11 blocking the memory from responding to any further commands from the Unibus.

## 4.6 MEMORY INITILIZE - BUS INITL (SHEET 1)

The BUS INITL Unibus signal is a memory reset pulse from the processor. Memory path is illustrated in Figure 4-12.

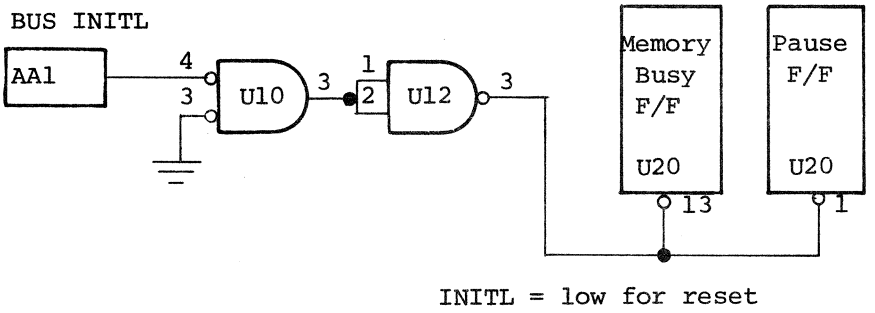



Figure 4-12: Memory Initialize Circuit

## 4.7 X AND Y CURRENT LOOP (SHEET 2)

Figure 4-13 contains a block diagram of the X and Y read current loop. Figure 4-14 contains a block diagram of the X and Y write current loop. The main elements of the current loop are the current source, X and Y sink and drive switches and balun transformers.

### Read Current Path

During the read half cycle, the half current pulse for the selected X line flows from the -15V supply through the XR+YW current source (Q16-Q19). The path continues through one of eight drive switches (QU12, QU13) which is decoded using address bits AØ1, AØ2, and AØ3. The selected line CCØ-CC7 enters the stack at E41-E48. The path exits the stack at one of sixteen X sink switches XSØ-XS15 (E1-E16) which is decoded using address bits A1Ø, A11, A12, and A13.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-12 |

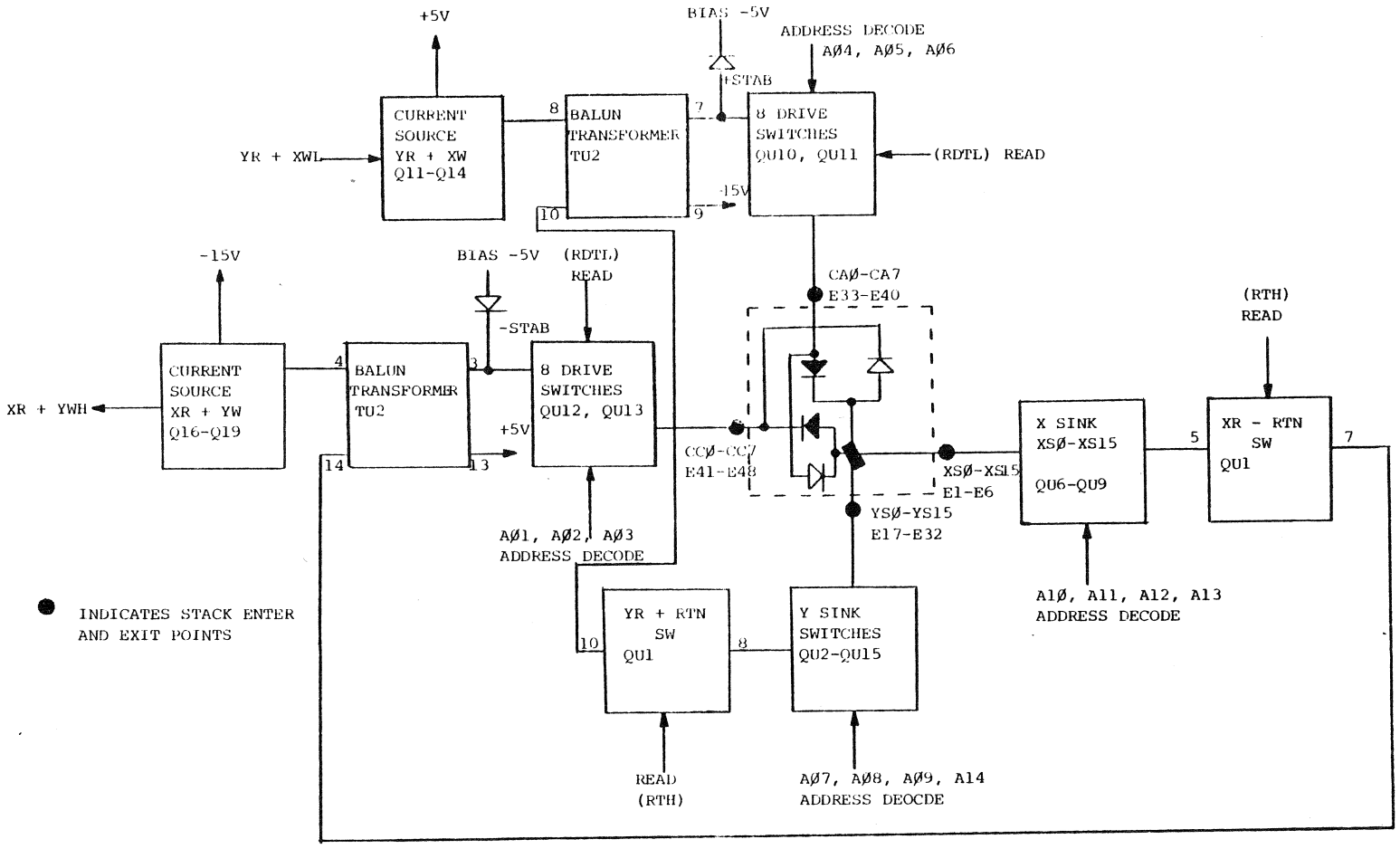



Figure 4-13: X and Y Read Current Paths

| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV | SHEET |
| | — | 4-13 |

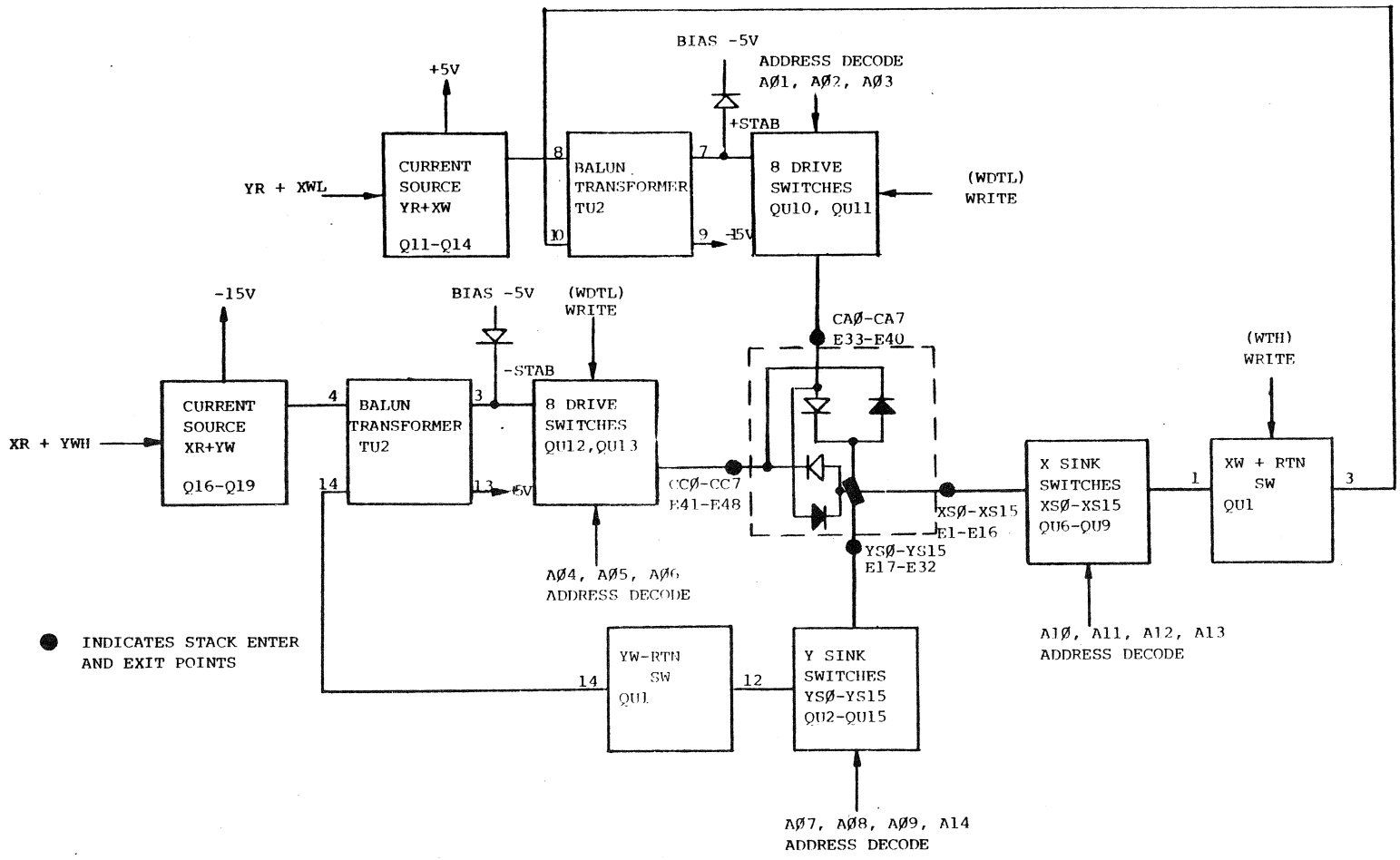



Figure 4-14: X and Y Write Current Paths

The current path completes its circuit through read switch XR-RTN (QU1,5,7) and the X-Y balun transformer (TU12,13,14) to the +5V supply.

The half current pulse for the selected Y line flows from the +5V supply through the YR+XW current source (Q11-Q14). The path continues via one of eight drive switches (QU10 and QU11) which is decoded using address bits AØ4, AØ5, and AØ6. The selected line CAØ-CA7 enters the stack at E33-E40. The path exits the stack at one of sixteen Y sink switches YSØ-YS15 (E16-E32) which is decoded using address bits AØ7, AØ8, AØ9, and A14. The current path completes its circuit through read switch YR-TRTN (QU1,8,10) and the X-Y balun transformer (TU2,10,9) to the -15V supply.

Write Current Path

During the write half cycle, the half current pulse for the selected X line flows from the +5V supply through the YR+XW current source (Q11-Q14). The path continues through one of eight drive switches (QU10 and QU11) which is decoded using address bits AØ1, AØ2, and AØ3. The selected line CAØ-CA7 enters the stack at E41-E48. The path exits the stack at one of sixteen X sink switches XSØ-XS15 (E1-E16) which is decoded using address bits A1Ø, A11, A12, and A13. The current path completes its circuit through write switch XW+RTN, QU1-1-3 and the X-Y balun transformer (TU2-10-9) to the -15V supply.

The half current pulse for the selected Y line flows from the -15V supply through the XR-YW current source (Q16-Q19). The path continues via one of eight drive switches (QU1 and QU13) which is decoded using address bits AØ4, AØ5, and AØ6. The selected line CCØ-CC7 enters the stack at E41-E48. The path exits the stack at one of sixteen Y sink switches YSØ-YS15 (E17-E32) which is decoded using address bits AØ7, AØ8, AØ9, and A14. The current path completes its circuit through write switch YW-RTN (QU1-12-14) and the X-Y balun transformer (U2-14-13) to the +5V supply.

### 4.7.1 X AND Y CURRENT SOURCE

The current source circuits provide the read and write half currents for the selected X and Y lines. Optimum core switching requires current pulses of precise amplitude, shape and duration. X and Y current amplitude is factory set to 385mA at 25°C with a time duration of 300ns.

Figure 4-15 shows a typical current source. Current flows from -STAB through balun transformer T1 via Q7-Q12 to the -15V supply. When XR-YWH goes low it causes Q6 and Q5 to go on and Q7 off. This inhibits any current from flowing through Q8-Q12. XR+YWH signal high causes Q6 and Q5 to turn off and Q7 to turn on. This turns on Q8-Q12.

Current amplitude is controlled by transistors Q1-Q4. Thermistor RT controls current flow to compensate for any temperature variation at the memory card. Resistor R1 controls current flow through both current sources. Resistor R2 controls current flow through transistors Q7-Q12.

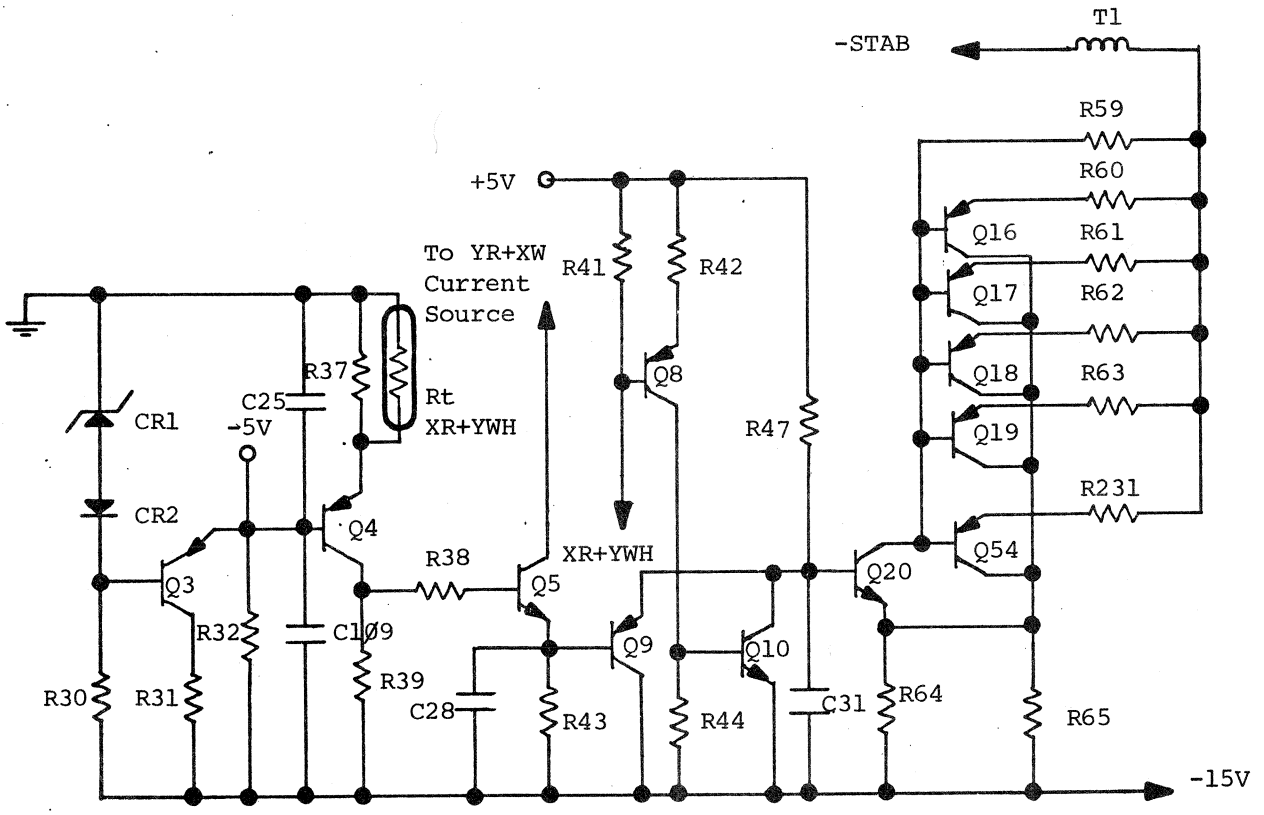



Figure 4-15 Typical Current Source (X Read + Y Write)

4.7.2 X AND Y SINK SWITCHES (SHEET 3)

The PM-1116B contains 16 X sink switches designated XSØ-XS15 and 16 Y sink switches designated YSØ-YS15.

The 16 X sink switches together with 8 drive switches select one of 128 X lines. The 16 Y sink switches together with 8 drive switches select one of 128 Y lines. The X and Y sink switch circuits are identical. A typical sink switch circuit is shown in Figure 4-16.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-16 |

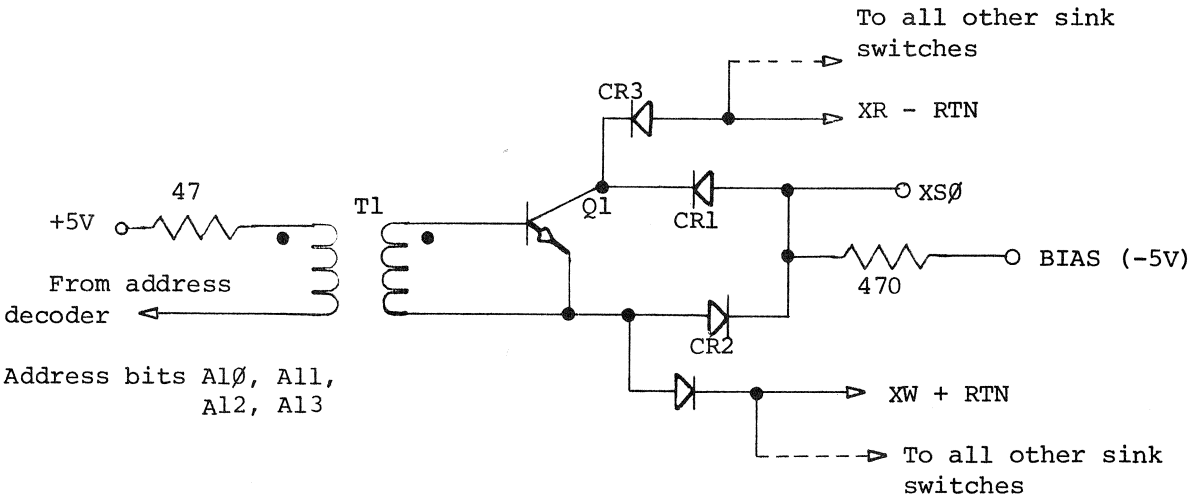



Figure 4-16: X Sink Switch Circuit

A 74145 address decoder is used to decode one of sixteen X or Y sink switches. When one of the X sink switches is selected, the primary winding of transformer T1 is grounded. This causes current to flow from the +5V supply through a 47 ohm current limiting resistor and through the primary winding of T1 to ground. This causes Q1 to be turned on.

During the read half cycle, current sinks in the negative direction from the stack through CR3, Q1 and CR1 to the return path. During the write half cycle, current sinks in the positive direction from the stack through CR2, Q1 and CR4 to the return path.

Address bits 1Ø, 11, 12, and 13 are used to select one of sixteen X sink switches. Address bits 7, 8, 9, and 14 are used to select one of sixteen Y sink switches. X and Y sink decode charts are contained in Tables 5-3 and 5-4.

### 4.7.3 X AND Y DRIVE SWITCHES (SHEET 3)

The PM-1116B contains 16 drive switches designated CAØ through CA7 and CCØ through CC7. They are used in conjunction with the X and Y sink switches in a "shared drive" scheme which minimizes the number of components used in the system and increases reliability while decreasing power consumption.

Figure 4-17 illustrates the shared drive circuit.

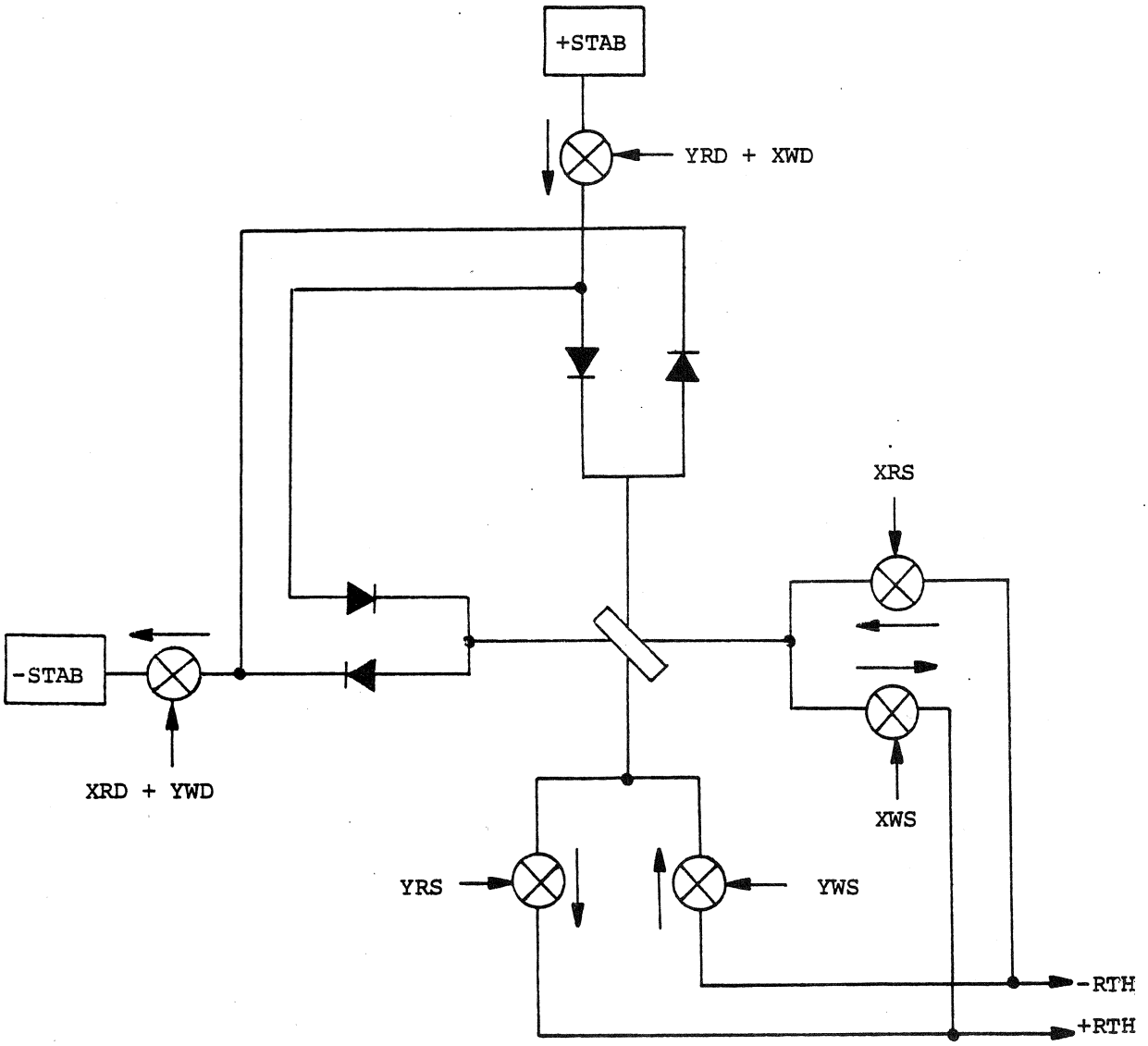



Figure 4-17: Shared Drive Circuit



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV - | SHEET 4-18 |

Figure 4-18 contains typical CA and CC drive switches.

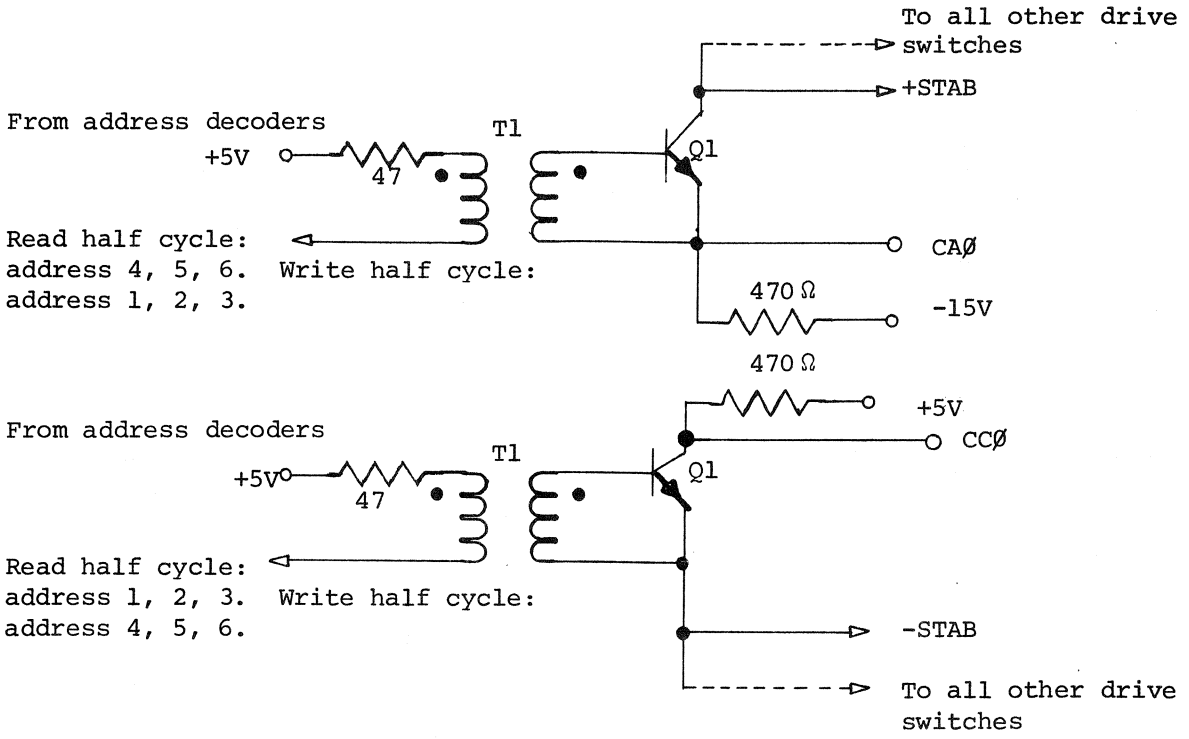



Figure 4-18: Typical Drive Switches

During a read half cycle, one of the CAØ-CA7 drive switches is used to drive current to the selected Y line in conjunction with the selected Y sink switch. During the write half cycle, one of the CCØ-CC7 drive switches is used to drive current to the selected X line in conjunction with the selected X sink switch.

Address bits AØ1, AØ2 and AØ3 are used to select one of eight CCØ-CC7 drive switches during the read half cycle and one of eight CAØ-CA7 drive switches during the write half cycle.

Address bits AØ4, AØ5, and AØ6 are used to select one of eight CAØ-CA7 drive switches during the read half cycle and one of eight CCØ-CC7 drive switches during the write half cycle.

X and Y drive switch decode charts are contained in Tables 5-5 and 5-6.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-19 |

## 4.8 DATA LOOP CIRCUIT (SHEET 4-7)

Data to and from the memory card is transferred on the same Unibus lines. The 16 data-in and data-out lines are designated BUS DØØL through BUS D15L. All Unibus lines are active low (ØV) and inactive high (+3V). This allows all devices including the processor to connect to the Unibus lines in parallel.

Figure 4-19 shows the data loop circuit. An SN7438 open collector NAND gate functions as a Unibus transmitter. The receiver used is a Signetics 8T380 with an input high threshold noise of 1.8V minimum.

Timing signals DOSØH (byte Ø) and DOS1H (byte 1) are used to strobe data from the memory to the Unibus. Timing signals LDØL (byte Ø) and LD1L (byte 1) are used to strobe data from the Unibus to the memory.

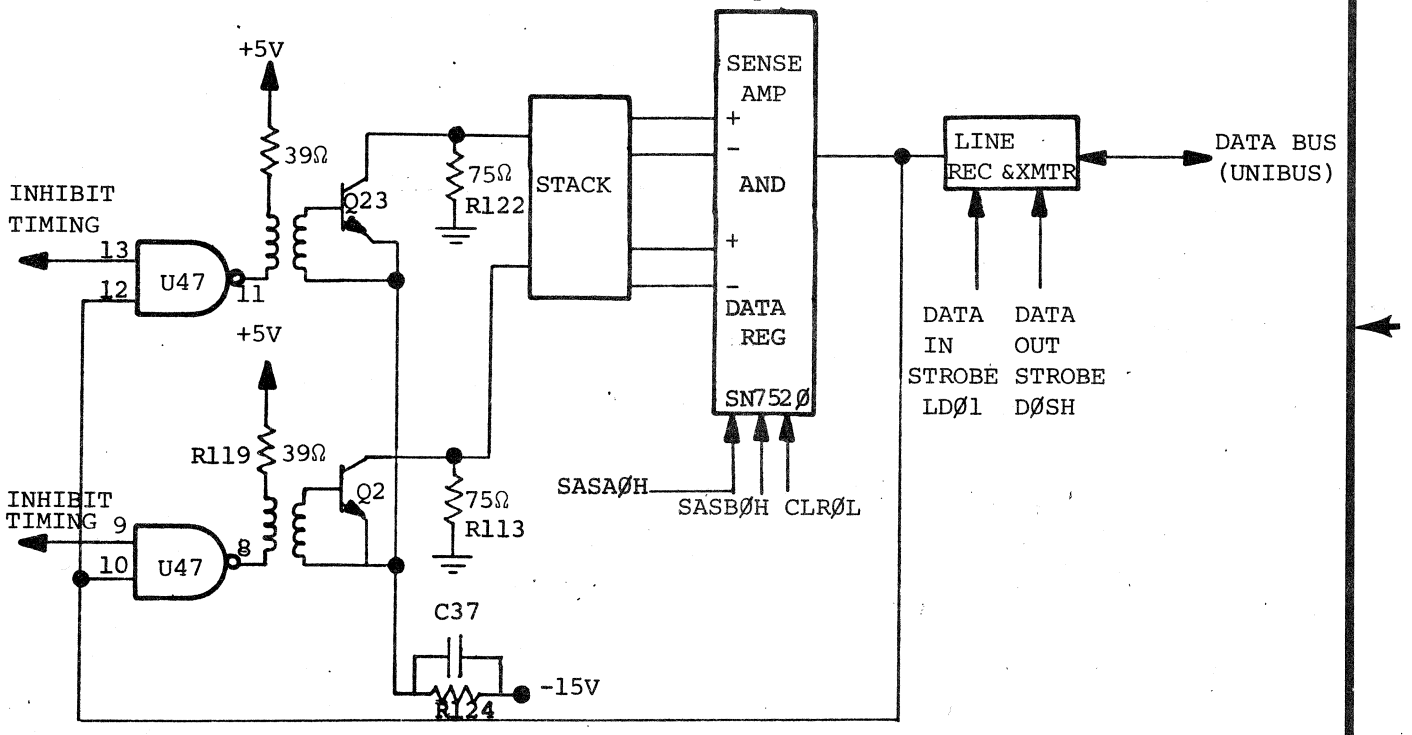



Figure 4-19 Data Loop Circuit

For a clear-write operation during the first half cycle the sense amplifier strobe is inhibited for both lower and upper 8K sense (SASAØH and SASA1H). The data register is cleared at the beginning of the cycle with CLRØL and CLR1L. The data is strobed from the Unibus lines into the memory data registers with timing signals LDØL and LD1L.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 4-20 |

During the second half cycle, the data register controls one input for both inhibit driver gates. The other input is the timing pulse ITAØH or ITA1H which is a function of address bit A14. Address bit A14 low (active) indicates that the memory is addressed in the upper 8K stack; ITAØH is enabled and ITA1H is inhibited. Address bit A14 high (inactive) indicates that the memory is addressed in the lower 8K stack; ITAØH is inhibited and ITA1H is enabled. When the inhibit driver is on, it opposes X and Y currents and causes a zero to be written into the core. When the inhibit driver is off, it enables X and Y currents and causes a one to be written into the core.

For a read-restore mode during the first half cycle, sense amplifier strobe is a function of address bit A14. Address bit A14 low inhibits SASA1H and SASB1H and enables SASAØH and SASBØH.

### 4.8.1 INHIBIT DRIVER CIRCUIT (SHEETS 4-7)

The PM-1116B uses 32 inhibit drivers, one for each 8K sense/inhibit loop or two per bit.

The function of the inhibit driver is to drive current with the same amplitude but in the opposite direction from the write current in all Y lines. This will cancel out the write current in the selected Y line.

To enable writing a 1 in the desired bit, the inhibit driver is turned off, allowing X and Y half-currents to switch the selected core to the one state.

The cores are always cleared to the zero state during the read half cycle. To enable writing a zero in the desired core, inhibit driver is turned on, causing current to flow in the opposite direction of the Y current and thus inhibiting a core switch-over. This causes the selected core to remain in its zero state.

Figure 4-20 illustrates a typical inhibit driver circuit.

Inhibit current flows from the -15V supply through R1 and Q1 into the inhibit/sense stack loop. Q1 is turned on during the inhibit timing (write timing pulse WTH) only if data register $\overline{Q}$ output is high. (Pin 12 or 14 on sense amp IC 7520).

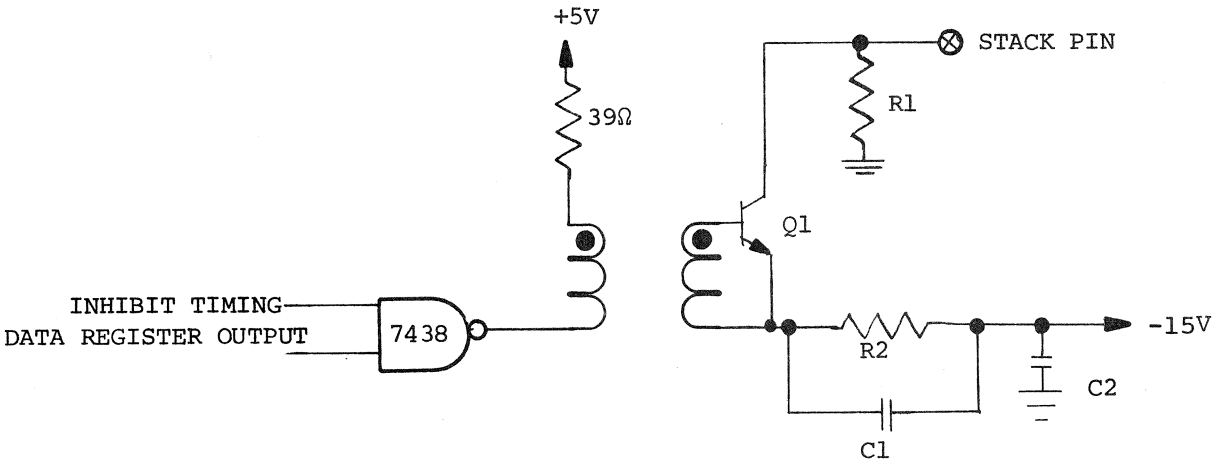



Figure 4-20: Typical Inhibit Driver Circuit

4.8.2 SENSE AMPLIFIER (SHEETS 4-7)

The sense amp IC SN7520 consists of dual differential amplifiers and a threshold voltage input plus the data register latch. The threshold voltage determines the switching level of the sense amplifier. VTH voltage is approximately +4V. This voltage is obtained from the +5V supply through register voltage divider. (See schematic diagram sheet 4 A/5.)

The reference voltage VTH is brought into the threshold inputs (pins 4 and 5) through another resistor voltage divider. The threshold voltage between pins 4 and 5 is approximately 18mv.

The sense amp is an open-loop high gain linear amplifier. Whenever the differential voltage between its inputs (pins 2 and 3 or pins 6 and 7) exceeds the threshold voltage (18mv), the amplifier goes into saturation (switched to a high). If the differential voltage does not exceed the threshold voltage, the amplifier remains in its off state (switched to a zero).

Another section of the sense amp IC consists of the data register latch and the sense amplifier strobe input gate. The data register latch is cleared at the beginning of each cycle with CLR signal. The two sense amp strobed at pins 11 and 15 (SASA and SASB) are a function of address bit A14. They select between the lower and the upper 8K sense loops.

A typical sense amplifier circuit is shown in Figure 4-21.

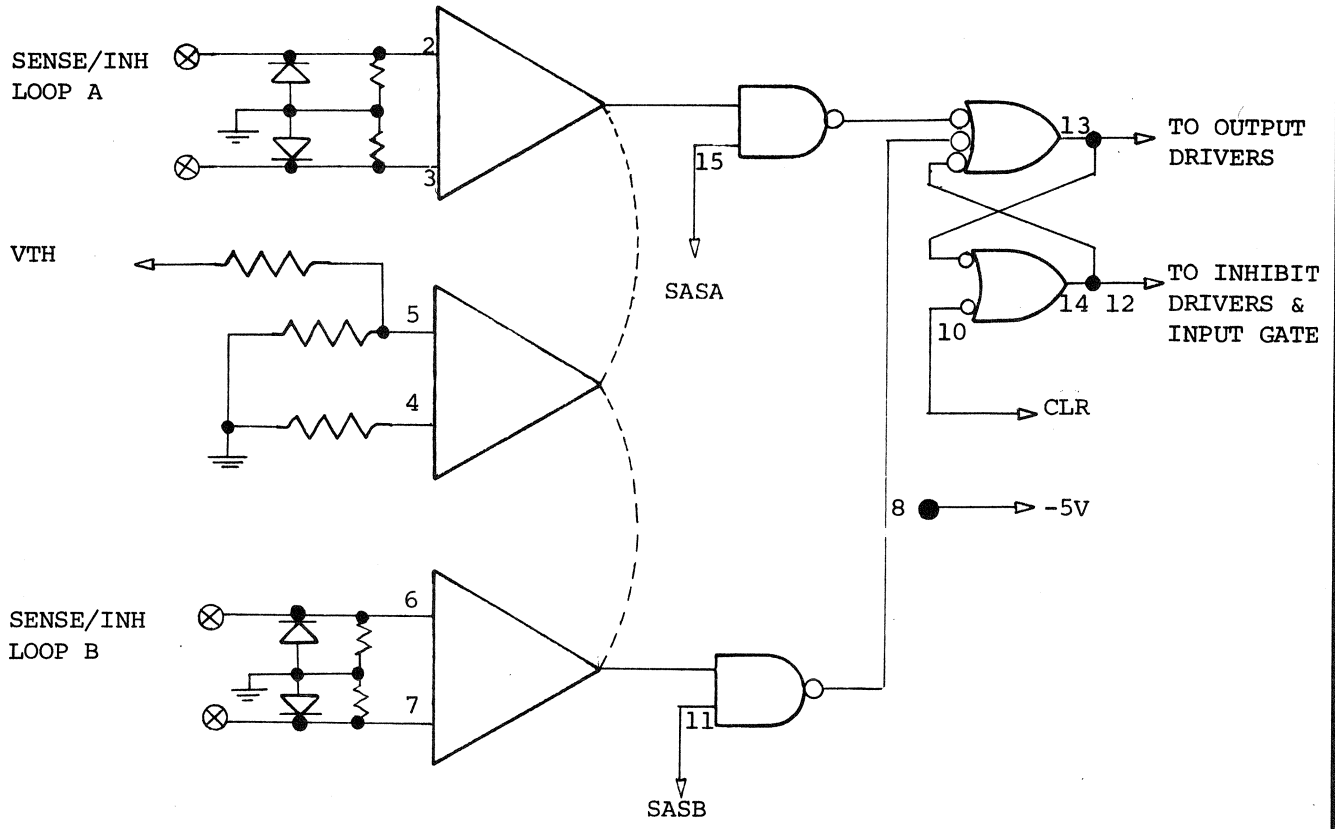



Figure 4-21: Typical Sense Amplifier Circuit

The diode pin in each loop provides the current path for the inhibit current pulse during the write half cycle. The resistor pin in each input terminates the sense/inhibit loop. The sense/inhibit loop measures approximately 16 ohms between pins 2 and 3 or 6 and 7. DC resistance between pins 2, 3, 6, or 7 to ground when the diodes are back biased is approximately 40 ohms and when the diodes are forward biased is approximately 14 ohms.

The DC resistance of both diodes in the forward bias direction must be the same so that the inhibit current is divided equally when flowing through the sense/ inhibit loop.

# Section 5

# Maintenance and Troubleshooting

This section contains maintenance and troubleshooting information. The logic description in Section 4 and the drawings in the appendix are provided for further reference.

## 5.1 PRINTED CIRCUIT BOARD CLEANING

The printed circuit contacts should be cleaned when dust or dirt has built up on the surfaces. Instant Contact Cleaner, alcohol, and freon have been approved for cleaning contacts. When printed circuit contacts must be cleaned, hold the card so the contacts are pointed down and thoroughly saturate the contact area. While the contacts are still wet, scrub with a soft natural bristle brush.

CAUTION

Under no circumstances should an eraser or other abrasive be used on gold plated contacts.

To remove dust from printed circuit boards, a soft brush should be used. Clear, oil-free, pressurized air (5 psi max) can be sprayed over the board.

CAUTION

Do not spray pressurized air directly inside the core matrices.

## 5.2 STACK REPAIR

With the exception of stack diodes, modules and terminating Unibus, which may be replaced in the field, repair of the stack assembly is not recommended. If a stack is faulty, replace it with a new stack assembly.

## 5.3 STACK REMOVAL AND INSTALLATION

Stack removal consists of removing the stack from the board assembly. The stack itself should not be disassembled. The stack is removed by first removing the nuts from the 4-40 screws holding the stack on the board; then carefully spreading the pinned side. Be careful not to excessively bend the board or the stack subassemblies.

To install the stack onto the board assembly, first orient the connectors on each subassembly to be sure that they are aligned. Then carefully insert the stack connectors into the board connectors. Check that the pins are exactly aligned before compressing the two subassemblies in order to prevent bending the board. Insert until the stack standoff makes contact with the components board, then insert the mounting screws.

## 5.4 REPAIRS - GENERAL

Discrepancies in memory system operation are, in general, one of the following types:

- Operation failures, which are caused by faulty reference control, input logic, or timing.
- Partial data word failures which are caused by faulty drive and sink switches, drive control, memory register, inhibit driver, stack decoding logic or line driver circuits.

If no definite failure pattern is apparent, adjusting power supply voltages $\pm$5% about nominal might help to cause a "hard" failure.

NOTE: It is strongly recommended that all assemblies requiring repair be returned to the factory for rework. All returned units should be accompanied with a detailed description of the failure.

## 5.5 PM-1116B INTERNAL TIMING SET-UP

The following timing signals are initially set at the factory. Refer to internal timing diagram, Figure 5-1, and internal timing figures in Appendix A.

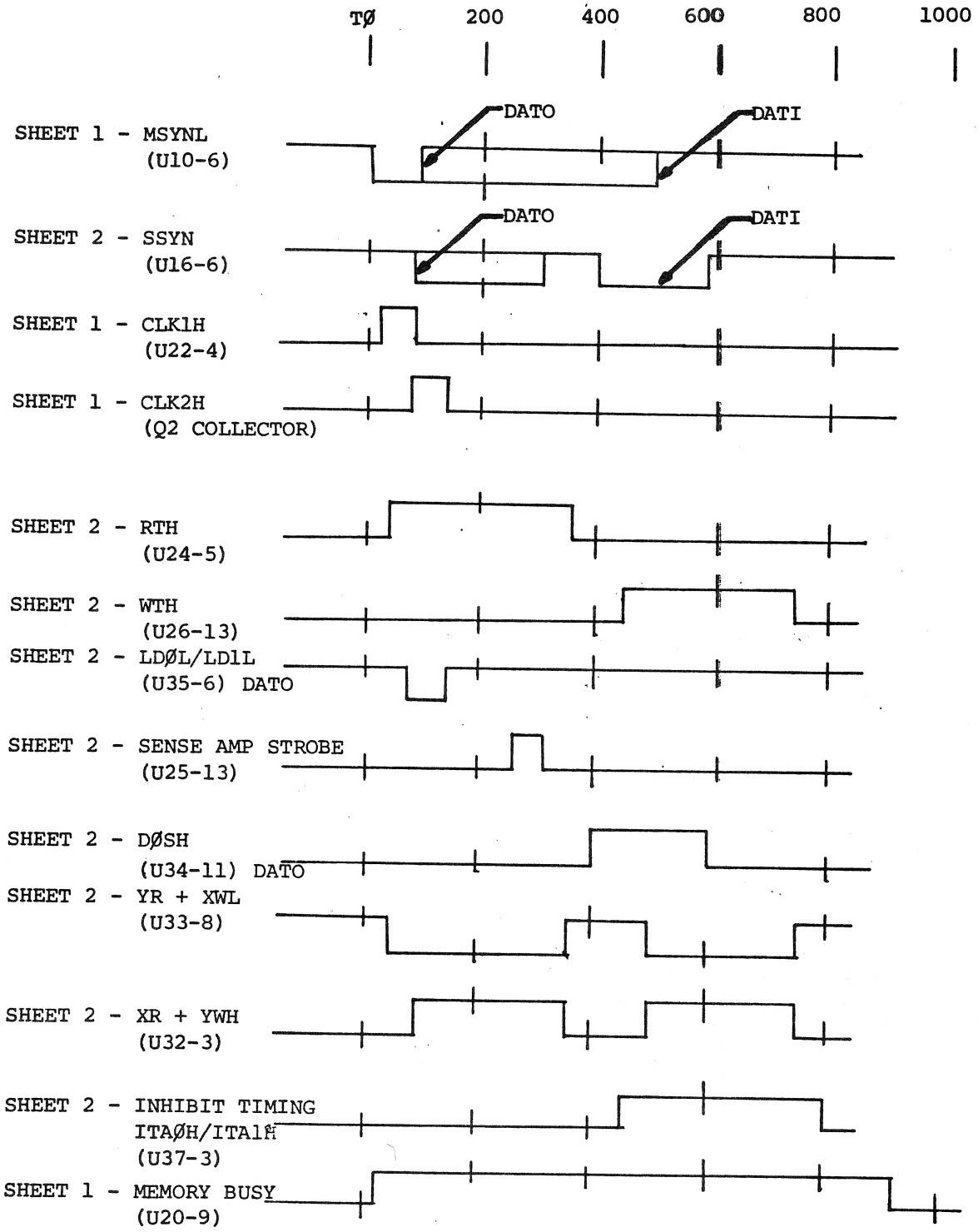



Figure 5-1: Internal Timing Diagram



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 5-3 |

Read Timing Pulse - RTH (Sheet 2/7B)

The RTH timing pulse is monitored at the output of the read timing one-shot U24-5. RTH pulse width is set at 320ns ± 10ns with its leading edge at 50ns ± 10ns. Pulse width is varied by changing the overall value of U24 timing resistor R16. Select values for R16 from the following: 11K, 12K, 15K, 18K, 20K, 22K, 27K, and 33K ohms.

Write Timing Pulse - WTH (Sheet 2/7B)

The WTH timing pulse is monitored at the output of the timing one-shot U26-13. WTH pulse width is set at 300ns ± 10ns with its leading edge at 450ns ± 10ns. Pulse width is varied by changing the overall value of U26 timing resistor R18. Select values for R18 from the following: 11K, 12K, 15K, 18K, 20K, 22K, 27K, and 33K ohms.

Sense Amplifier Strobe - SAS (Sheet 2/7D)

The SAS pulse is monitored at the output of the SAS one-shot U25-13. The leading edge is set at 130ns from the OV level of X read pulse CAØ measured at the stack connector pin. The pulse width of SAS should be 50ns ± 10ns. It is varied using trimmer pot R11 at U25-7.

Monitor all other timing signals listed in the internal timing diagram, Figure 5-1. Tolerance for all timing signals is ± 10ns.

## 5.6 X-Y CURRENT SET-UP

After initial memory warm up install a current probe P6021 or equivalent through the two loops at the back of the stack. With the current probe switch set at 2mA/mV and the scope at 50mV/cm input (scope is set at 100ma per division). Read 385ma ± 5ma at the flat top of both X and Y pulses. Read only the first pulses and invert them if necessary. X and Y current pulses are depicted in Figure 5-2.

To adjust Y read current pulse vary the value of R48 in parallel with R49. To adjust X read current vary the value of R64 in parallel with R39. Select values for R48 and R64 from the following to obtain 390ma of current in the X and Y drive lines: 82, 100, 120, 150, 180, and 220 ohms. To adjust amplitude of both Y read and X read current pulses vary the value of R229 in parallel with R39.

To control the amplitude of X and Y currents for memory margin testing an external potentiometer is connected across plug P1. Plug P1 is a three pin plug located on the component side of the memory board assembly. The plug is shown on schematic sheet 2/3A.

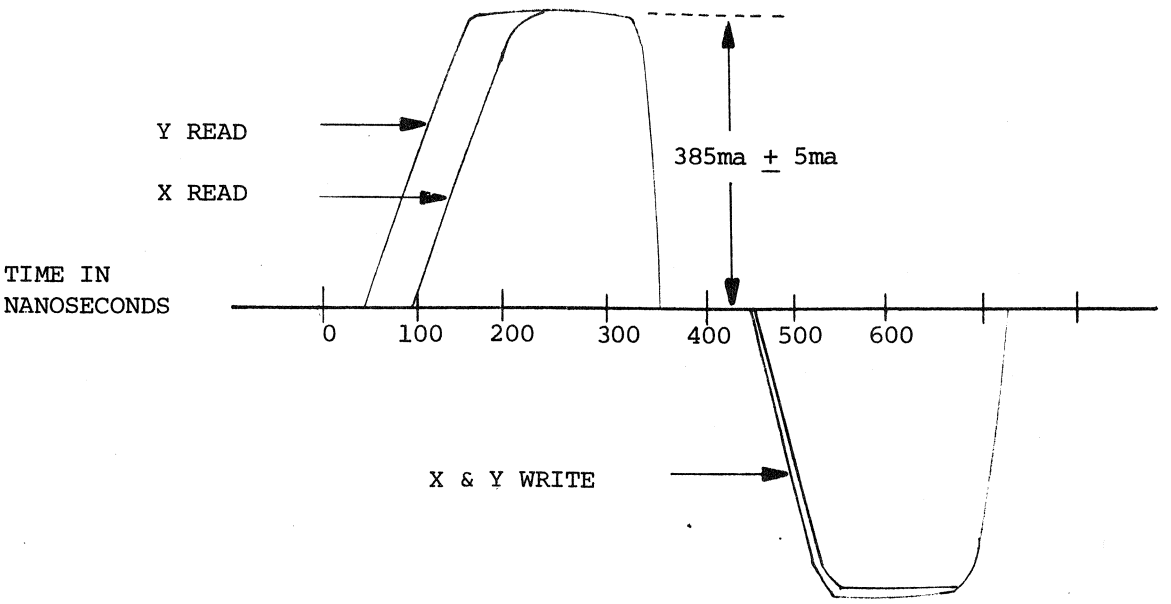



Figure 5-2: X & Y Current Pulses

## 5.7 TROUBLESHOOTING PROCEDURE

In order to detect a malfunction in the memory card it is necessary first to isolate the general area of the memory that causes the malfunction; then in a step by step manner to isolate the exact location of the failure.

All interface lines including the power supply voltages must be present and verified. Figure 5-3 outlines all interface lines to and from the memory system.

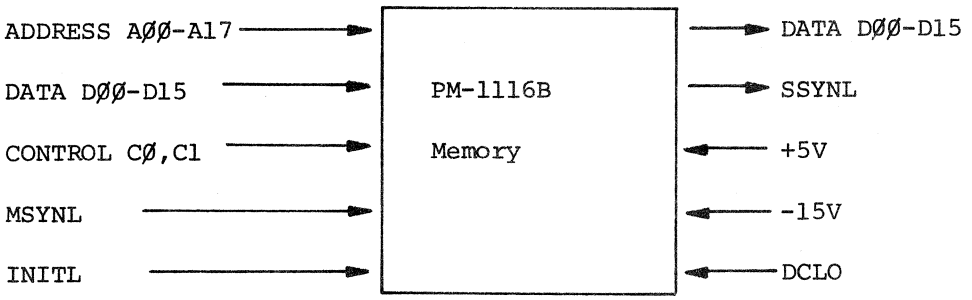



Figure 5-3: Interface Lines

BUS MSYNL is the memory initiate command. Before the memory can respond to a MSYNL command the following conditions must be fulfilled:

- Address strapping jumpers must be set to match the address presented on the data bus (U19-3,4,6, and 11 must be high).
- The memory must complete its present cycle before it is ready to accept another MSYNL command.
- The slave sync (SSYNL) signal from the previous cycle must be cleared.
- BUS DCLO should be high (inactive). BUS DCLO inhibits any access to the memory. DCLOL is monitored at U15-12.
- BUS INITL should be high (inactive). It is monitored at U12-3.

Timing and Control Signals

Once the memory is accessed, all timing and control functions should be checked and verified. Figure 5-4 shows the timing and control signals, Table 5-1 lists the signals and their functions.

Check the presence of CLK2H by monitoring the Q2 collector. The absence of CLK2H indicates that the above conditions were not met.

If CLK2H is present, the next step in the troubleshooting procedure is to monitor X and Y current pulses using a current probe.

X & Y Current Check

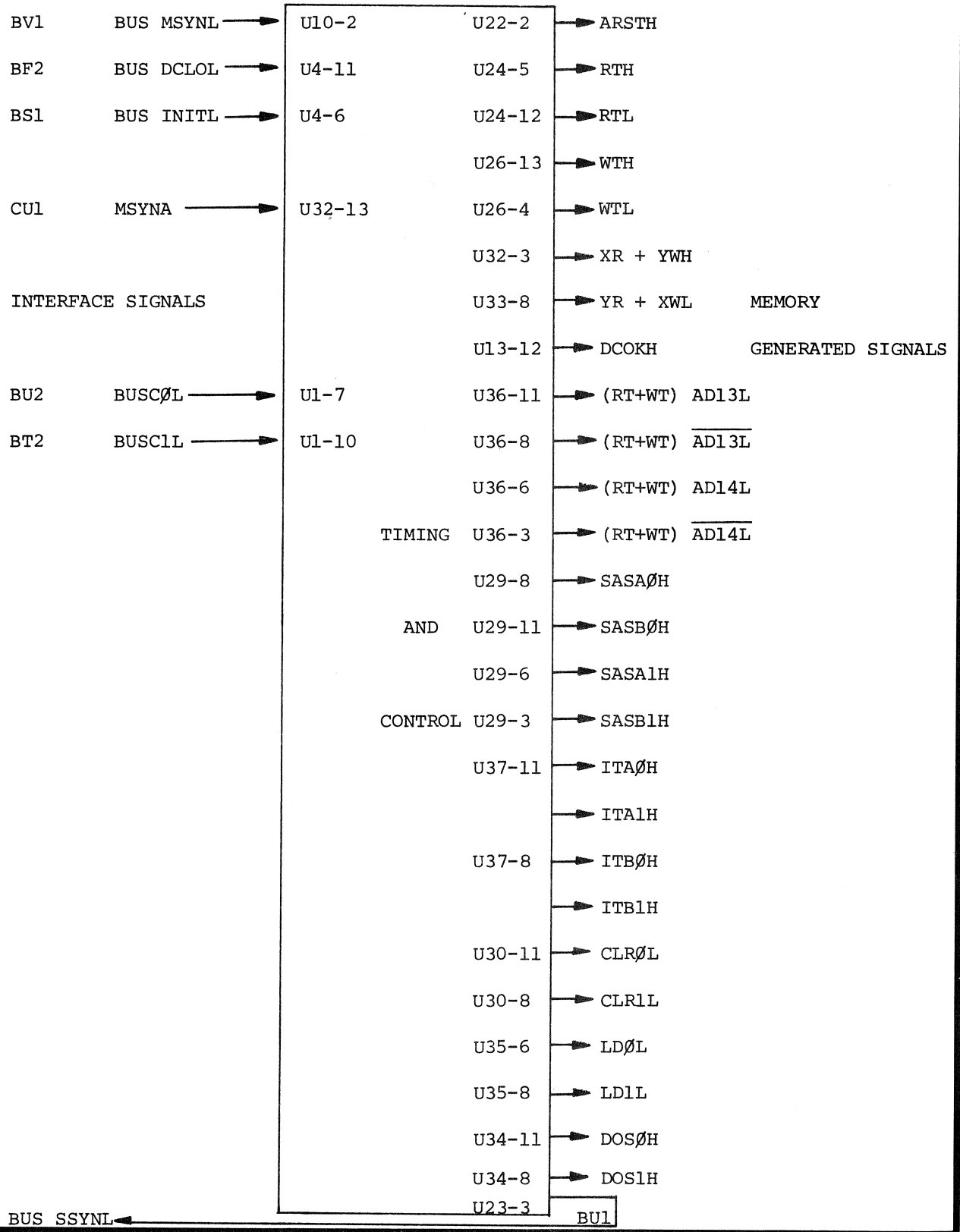
In order to check the X and Y current pulses, a current probe should be installed through the two loops provided in the back of the stack assembly. Both X and Y amplitude should be between 380ma and 390ma at 25°C. Verify that X read pulse is delayed from Y read pulse by approximately 50ns.

To adjust X and Y current amplitude, see Section 5.6.



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 5-6 |

Figure 5-4: PM-1116B Timing and Control Chart






| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET 5-7 |

FORM 000021

Table 5-1: Timing and Control Signal Functions

All signal names ending with the letter H indicate that they are high when active and low when inactive. All signal names ending with the letter L indicate that they are low when active and high when inactive.

| SIGNAL NAME | FUNCTION |
|---|---|
| ARSTH | Address register strobe pulse |
| RTH, RTL | Read timing |
| WTH, WTL | Write timing |
| XR + YWH | X read or Y write pulse to current source |
| YR + XWL | Y read or X write pulse to current source |
| DCOKH | DC current OK |
| (RT + WT) AD13L | X sink timing |
| (RT + WT) AD14L | Y sink timing |
| SASAØH, SASBØH | Sense amp strobe lower 8K sense/inhibit |
| SASA1H, SASB1H | Sense amp strobe upper 8K sense/inhibit |
| ITAØH, ITBØH | Inhibit timing lower 8K sense/inhibit |
| ITA1H, ITB1H | Inhibit timing upper 8K sense/inhibit |
| CLRØL, CLR1L | Data register reset byte Ø and byte 1 |
| LDØL, LD1L | Data-in strobe byte Ø and byte 1 |
| DOSØH, DOS1H | Data-out strobe byte Ø and byte 1 |
| SSYNL | Slave sync pulse |
| MSYNL | Master sync pulse |
| DCLOL | DC Line |
| INITL | Memory initialize |
| MSYNA | Not used |
| CØL, C1L | Control lines |

Address Strapping

To verify that the memory is strapped correctly and that the address strapping circuit is functioning properly, use the following procedure:

1. Insert address strapping plug TB1 in the memory card.

2. Using the information in Table 2-2 force Unibus address lines and check gate U19 pins 3, 4, and 6. All should be high.

3. Verify that jumper W1 is out by monitoring U19-11 and U19-12. They should be high except for 31K operation. For 31K operation, install W1 jumper and force address bits A11, A12, A13, A14, and A15 to go low (active). Verify that U17-8 is low.

To verify that the address strapping decoder IC is functioning properly do the following:

1. Verify that U14-12 is low.

2. Remove address strapping plug TB1.

3. Using Table 5-2 force address bits A13, A14, and A15. Check for the correct output level.

| A13 | A14 | A15 | CHECK FOR OUTPUT = LOW AT |
|---|---|---|---|
| L | L | L | U14-1 or TB1-16 |
| L | L | H | U14-2 or TB1-15 |
| L | H | L | U14-3 or TB1-16 |
| H | H | H | U14-4 or TB1-13 |
| H | L | L | U14-5 or TB1-12 |
| H | H | L | U14-7 or TB1-10 |
| H | H | H | U14-9 or TB1-9 |

Table 5-2: Strapping Decoder Outputs

X and Y Drive and Sink Switches

The X and Y drive and sink switches are the gold plated interface connector pins on the stack. An open switch is easily detected by comparison with the other switches. Compare the eight drive switches CAØ-CA7 to each other. Their pulse strap must be identical. Repeat the same comparison test with all eight drive switches CCØ-CC7, all sixteen X sink switches XSØ-XS15, and with all sixteen Y sink switches YSØ-YS15.

X and Y sink and drive switch decode charts are contained in Tables 5-3 through 5-6. L is used to indicate ØV at the decoder input or +3V at the Unibus. H is used in the tables to indicate +3V at the decoder input or ØV at the Unibus.

The procedure for locating a faulty switch is as follows:

1. Monitor any faulty X or Y line. A malfunction superimposes a distorted current wave form.
2. Force all associated address bits high and then low one at a time.
3. Record the address bits and the level which bypassed the error condition.
4. Invert their polarities and use the decode tables to locate the malfunctioning switch.

Current Source

Current amplitude should be set at 390ma at room temperature (25$^{o}$C) for both X read and Y write pulses. Current tracking is 1.3ma/$^{o}$C minimum to 1.6ma/$^{o}$C maximum.

Data Loop Check

The data loop circuit contains several elements which should be checked in case of malfunction; the troubleshooting procedure for each is contained in the following text.

Using the timing charts in the appendix check the following timing signals and verify them.

- Inhibit timing signals
- Sense amplifier strobe
- Data register clear
- Data register load
- VTH (+5V) and 18ms across divider network
- Inhibit driver output
- Inhibit switch output

Ground the data register timing signals CLRØL and CLR1L. This forces the data register Q output high.

The following tables decode the Unibus address to the selected X and Y sink switch.

| ADDRESS BITS AT TESTER OR DECODER INPUT | | | | | | |
|---|---|---|---|---|---|---|
| U41/U42 PIN 15 AD1Ø | U41/U42 PIN 14 AD11 | U41/U42 PIN 13 AD12 | U41/U42 PIN 12 AD13 | X SINK SWITCH SELECTED | STACK PIN LOCATION | DECODER OUTPUT (74145) |
| L | L | L | L | XSØ | E1 | U41-1 |
| H | L | L | L | XS1 | E2 | U41-2 |
| L | H | L | L | XS2 | E3 | U41-3 |
| H | H | L | L | XS3 | E4 | U41-4 |
| L | L | H | L | XS4 | E5 | U41-5 |
| H | L | H | L | XS5 | E6 | U41-6 |
| L | H | H | L | XS6 | E7 | U41-7 |
| H | H | H | L | XS7 | E8 | U41-9 |
| L | L | L | H | XS8 | E9 | U42-1 |
| H | L | L | H | XS9 | E1Ø | U42-2 |
| L | H | L | H | XS1Ø | E11 | U42-3 |
| H | H | L | H | XS11 | E12 | U42-4 |
| L | L | H | H | XS12 | E13 | U42-5 |
| H | L | H | H | XS13 | E14 | U42-6 |
| L | H | H | H | XS14 | E15 | U42-7 |
| H | H | H | H | XS15 | E16 | U42-9 |

NOTE: UNIBUS ADDRESS ASSERTED (LOW) EQUALS "1".

Table 5-3: X Sink Decode Chart

| ADDRESS BITS AT TESTER OR DECODER INPUT | | | | | | |
|---|---|---|---|---|---|---|
| U39/U40 PIN 14 ADØ7 | U39/U40 PIN 15 ADØ8 | U39/U40 PIN 13 ADØ9 | U39/U40 PIN 12 AD14 | Y SINK SWITCH SELECTED | STACK PIN LOCATION | DECODER OUTPUT (74145) |
| L | L | L | L | YSØ | E17 | U39-1 |
| L | H | L | L | YS1 | E18 | U39-2 |
| H | L | L | L | YS2 | E19 | U39-3 |
| H | H | L | L | YS3 | E20 | U39-4 |
| L | L | H | L | YS4 | E21 | U39-5 |
| L | H | H | L | YS5 | E22 | U39-6 |
| H | L | H | L | YS6 | E23 | U39-7 |
| H | H | H | L | YS7 | E24 | U39-9 |
| L | L | L | H | YS8 | E25 | U40-1 |
| L | H | L | H | YS9 | E26 | U40-2 |
| H | L | L | H | YS1Ø | E27 | U40-3 |
| H | H | L | H | YS11 | E28 | U40-4 |
| L | L | H | H | YS12 | E29 | U40-5 |
| L | H | H | H | YS13 | E30 | U40-6 |
| H | L | H | H | YS14 | E31 | U40-7 |
| H | H | H | H | YS15 | E32 | U40-9 |

NOTE: UNIBUS ADDRESS ASSERTED (LOW) EQUALS "1".

Table 5-4: Y Sink Decode Chart

| ADDRESS BITS AT TESTER OR DECODER INPUT | | | | STACK PIN LOCATION | DRIVE SWITCH SELECTED | DECODER OUTPUT (74145) |
|---|---|---|---|---|---|---|
| U45-13 ADØ1 | U45-15 ADØ2 | U45-14 ADØ3 | | | | |
| L | L | L | | E41 | CCØ | U45-1 |
| L | H | L | | E42 | CC1 | U45-2 |
| L | L | H | | E43 | CC2 | U45-3 |
| L | H | H | | E44 | CC3 | U45-4 |
| H | L | L | | E45 | CC4 | U45-5 |
| H | H | L | | E46 | CC5 | U45-6 |
| H | L | H | | E47 | CC6 | U45-7 |
| H | H | H | | E48 | CC7 | U45-9 |

NOTE: CCØ-CC7 (U45-12 = LOW)

| ADDRESS BITS AT TESTER OR DECODER INPUT | | | | STACK PIN LOCATION | DRIVE SWITCH SELECTED | DECODER OUTPUT (74145) |
|---|---|---|---|---|---|---|
| U44-15 ADØ4 | U44-14 ADØ5 | U44-13 ADØ6 | | | | |
| L | L | L | | E33 | CAØ | U44-1 |
| H | L | L | | E34 | CA1 | U44-2 |
| L | H | L | | E35 | CA2 | U44-3 |
| H | H | L | | E36 | CA3 | U44-4 |
| L | L | H | | E37 | CA4 | U44-5 |
| H | L | H | | E38 | CA5 | U44-6 |
| L | H | H | | E39 | CA6 | U44-7 |
| H | H | H | | E40 | CA7 | U44-9 |

NOTE: CAØ-CA7 (U44-12 = LOW)

Table 5-5: Drive Switches Decode Charts
Read Half Cycle

| ADDRESS BITS AT TESTER OR DECODER INPUT | | | | STACK PIN LOCATION | DRIVE SWITCH SELECTED | DECODER OUTPUT (74145) |
|---|---|---|---|---|---|---|
| U46-15 ADØ4 | U46-14 ADØ5 | U46-13 ADØ6 | | | | |
| L | L | L | | E41 | CCØ | U46-1 |
| H | L | L | | E42 | CC1 | U46-2 |
| L | H | L | | E43 | CC2 | U46-3 |
| H | H | L | | E44 | CC3 | U46-4 |
| L | L | H | | E45 | CC4 | U46-5 |
| H | L | H | | E46 | CC5 | U46-6 |
| L | H | H | | E47 | CC6 | U46-7 |
| H | H | H | | E48 | CC7 | U46-9 |

NOTE: CCØ-CC7 (U46-12 = LOW)

| ADDRESS BITS AT TESTER OR DECODER INPUT | | | | STACK PIN LOCATION | DRIVE SWITCH SELECTED | DECODER OUTPUT (74145) |
|---|---|---|---|---|---|---|
| U43-13 ADØ1 | U43-15 ADØ2 | U43-14 ADØ3 | | | | |
| L | L | L | | E33 | CAØ | U43-1 |
| L | H | L | | E34 | CA1 | U43-2 |
| L | L | H | | E35 | CA2 | U43-3 |
| L | H | H | | E36 | CA3 | U43-4 |
| H | L | L | | E37 | CA4 | U43-5 |
| H | H | L | | E38 | CA5 | U43-6 |
| H | L | H | | E39 | CA6 | U43-7 |
| H | H | H | | E40 | CA7 | U43-9 |

NOTE: CAØ-CA7 (U43-12 = LOW)

Table 5-6: Drive Switches Decode Charts
Write Half Cycle

Monitor the sense amplifier input using a differential probe. Force address bit 14 first to a high then to a low and observe inhibit driver output 25 and inhibit switch output 26.

## 5.8 TROUBLESHOOTING CHART

The following chart is provided to aid in determining the cause of specific failures. The left-hand column lists error indications or symptoms and the right-hand column lists possible sources for each symptom.

Troubleshooting Chart

| INDICATION | ACTION |
|---|---|
| Memory is not cycling. (no clock pulse CLK2H at Q2 collector) | 1. Check +5V supply.<br>2. Check strapping plug U19-3, 4, 5, 11, and 12 - should read high.<br>3. Check master sync pulse at U19-1.<br>4. Check memory busy flip-flop output at U19-5 should read high.<br>5. Check slave sync flip-flop output at U19-2 should be high.<br>6. Check BUS DCLOL line. |
| Memory is not cycling (Clock pulse CLK2H - ok) | 1. Check -15V supply.<br>2. Check DCOKH should read high at U38-10, 4, 2, and 12.<br>3. Check read and write timing RTH U24-5 and WTH U26-13. |
| Memory fails to read/write all Ø's | 1. Check inhibit driver circuit.<br>2. Check -15V supply. |
| Memory fails at certain address locations | 1. Force address bits one at a time and record the bits that bypassed the failure.<br>2. Use X and Y sink drive decode charts Tables 5-3 to 5-6 to decode the faulty line.<br>3. Check X, Y sink drive switches and core stack. |
| All bits fail. | 1. Check X-Y current.<br>2. Check sense amp. strobe timing.<br>3. Check -15V supply.<br>4. Check sense amp. strobe threshold voltage. (VTH) |

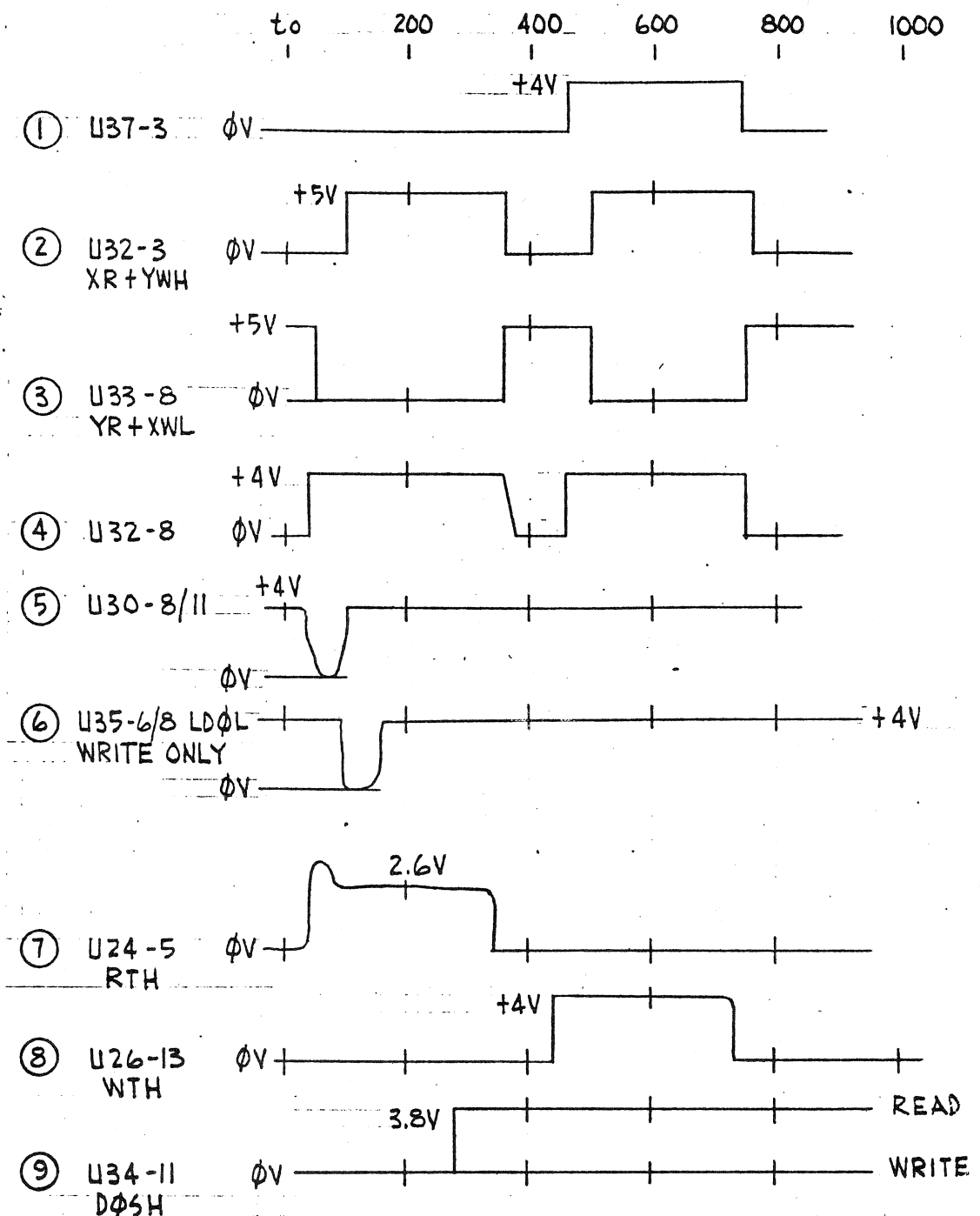
| INDICATION | ACTION |
|---|---|
| All bits fail. | 1. Check X-Y current temperature tracking. |
| Single bit failures. | 1. Check sense amp. strobe timing.<br>2. Check X-Y current pulses.<br>3. Check data circuits for the bits that fail. |
| Memory fails during address as data pattern mode only. | 1. Check address registers inputs. (See schematic diagram sheet 1, locations 6B through 6D). |
| Memory fails during cycle operation or during high or low voltage margin conditions | 1. Check memory busy flip-flop timing.<br>2. Check and verify all timing signals.<br>3. Check X-Y current pulse amplitude. |

# Appendix A

# Internal Timing Charts



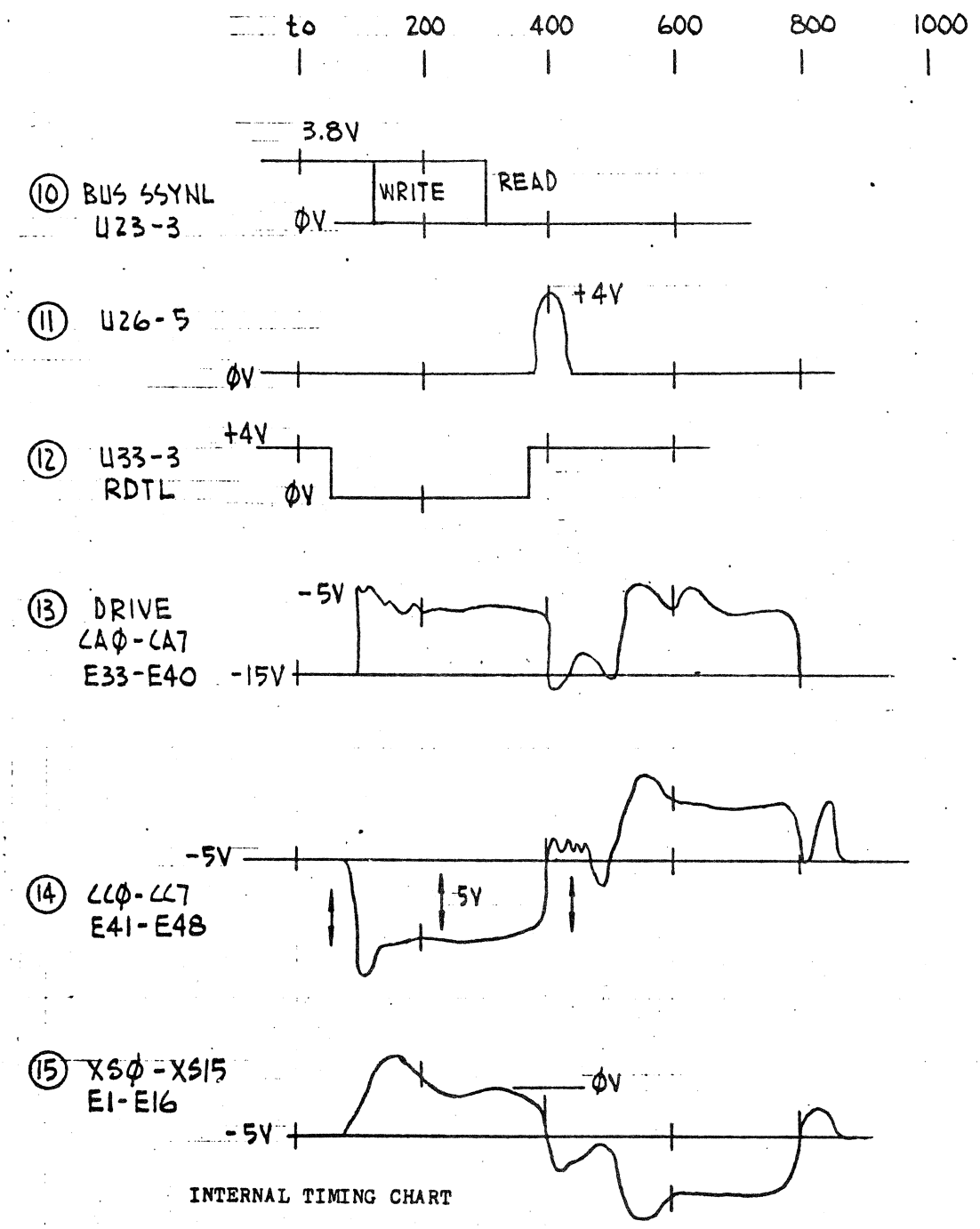
| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET A-1 |




INTERNAL TIMING CHART



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET A-2 |

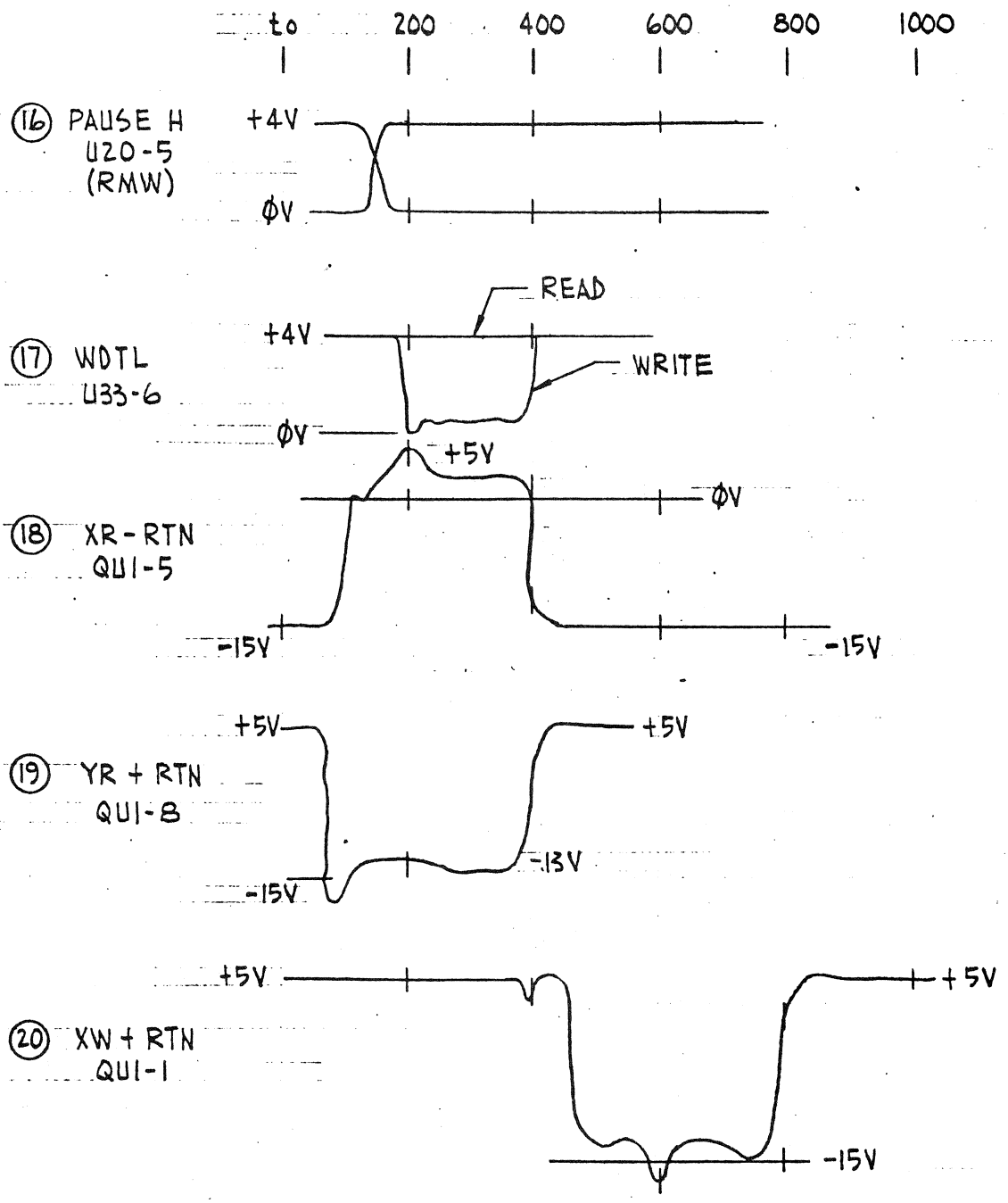



INTERNAL TIMING CHART



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET A-3 |

FORM 000021

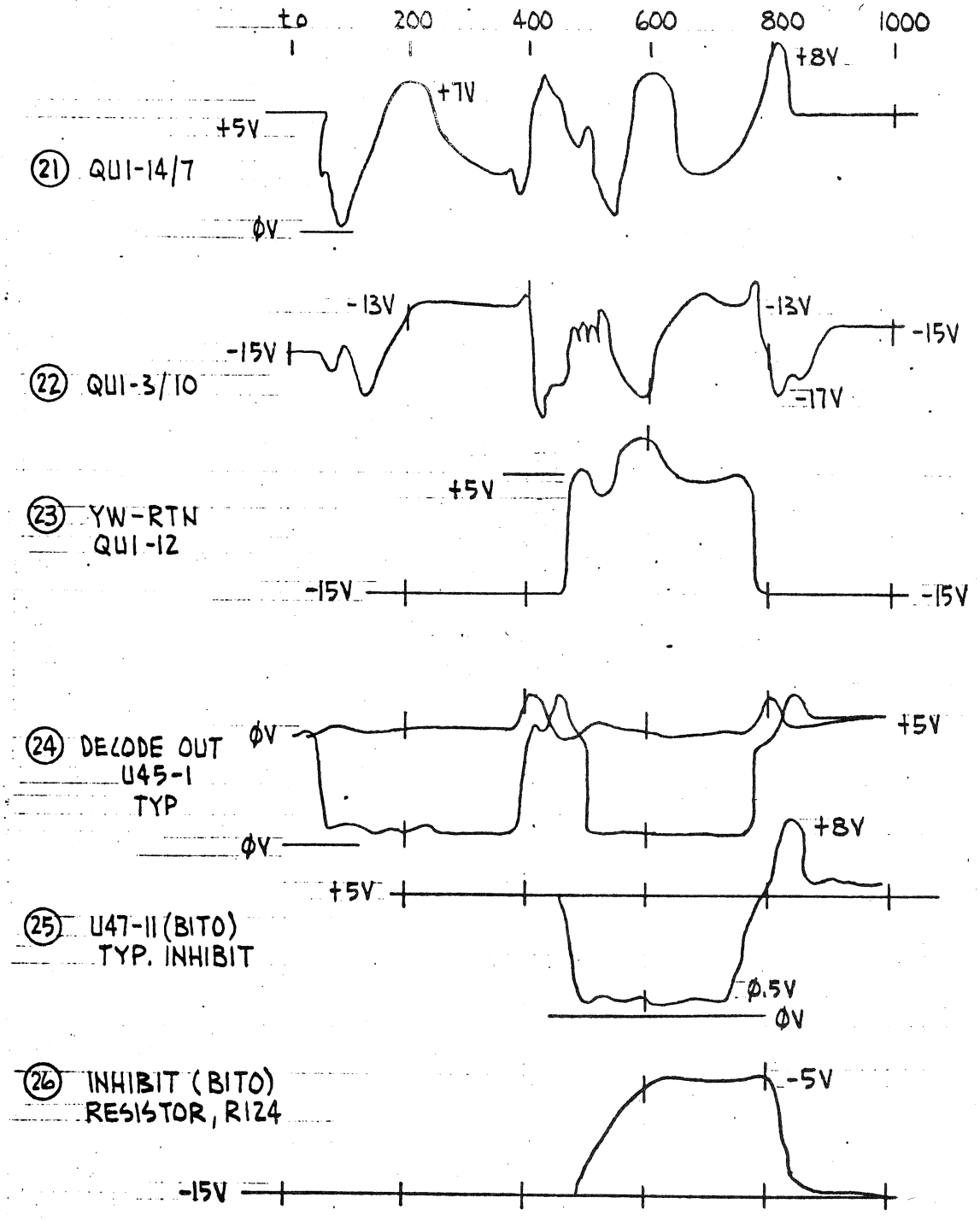



INTERNAL TIMING CHART



| SIZE | CODE IDENT NO | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET A-4 |

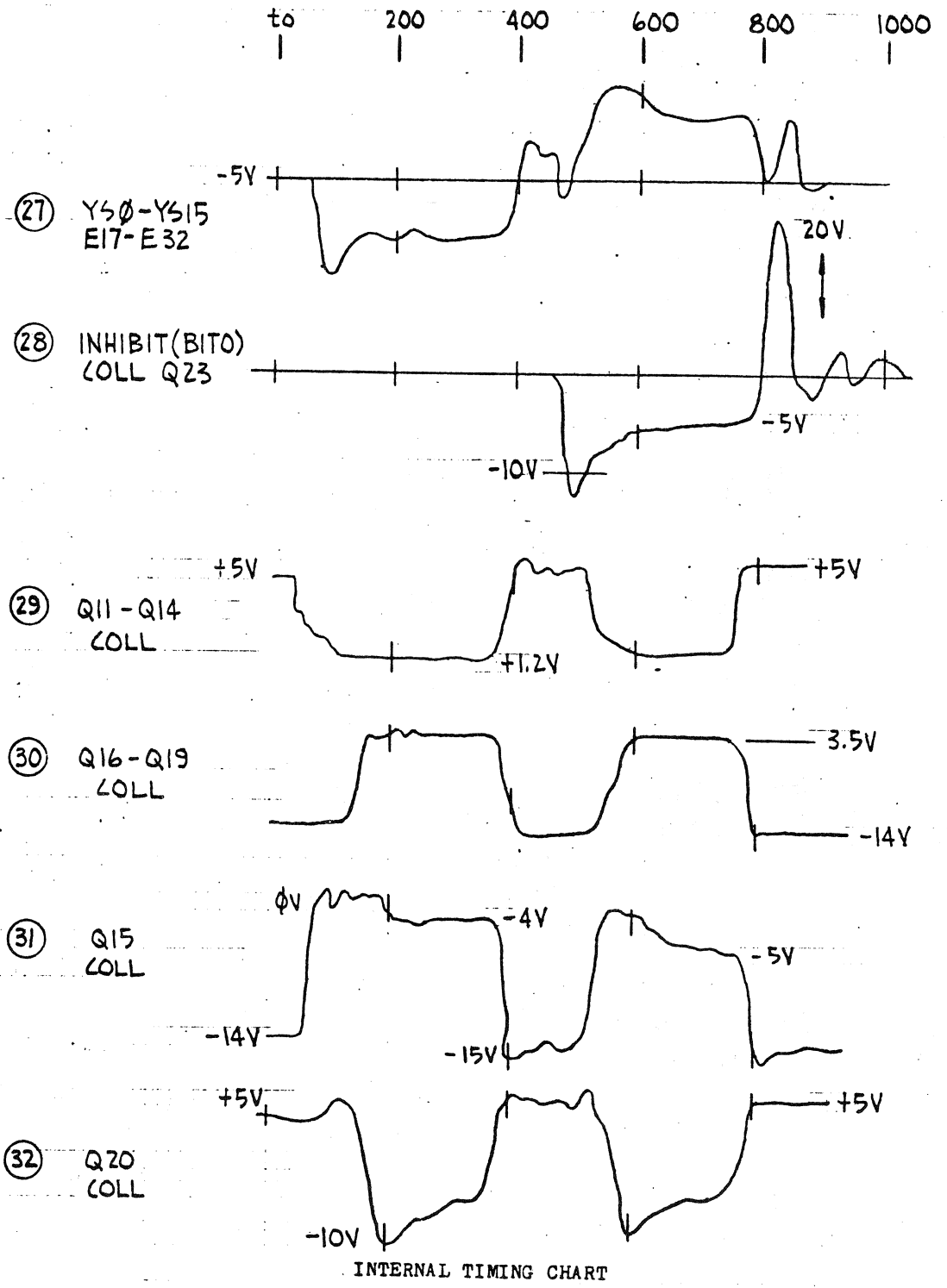
FORM 000021




INTERNAL TIMING CHART



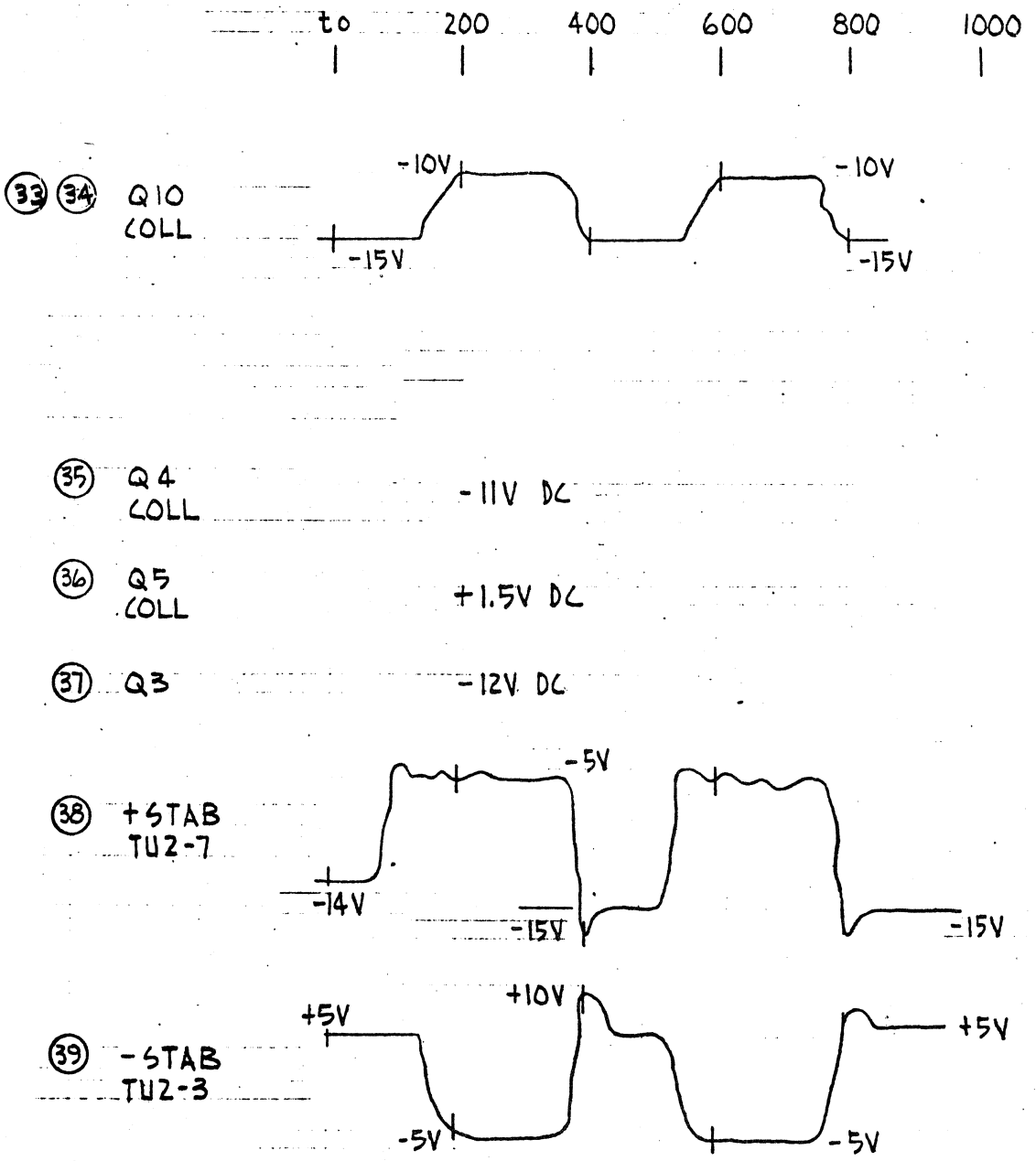
| SIZE | CODE IDENT NO | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET A-5 |




INTERNAL TIMING CHART



| SIZE | CODE IDENT NO | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET A-6 |




INTERNAL TIMING CHART



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET A-7 |

# Appendix B

# Parts List



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET B-1 |

**PARTS LIST** — **Plessey Memories Incorporated**, Santa Ana, California

PREPARED BY: GATES 6-14-76
CHECKED: DWT 6-23-76
RELEASED: RTJ 6-23-76
PARTS LIST NO.: SKPL700944-100
REV LTR: X3
CODE IDENT NO.: 52648
SH 1 OF 10

BOARD ASSEMBLY
MEMORY SYSTEM
PM-1116/B

| LTR | DESCRIPTION | DATE | APPROVED |
|---|---|---|---|
| X1 | REL TO DEV PER ERO 500811 | 6-23-76 | DWT |
| X2 | R9 IS 220Ω WAS 1K | 9-3-76 | [illegible] |
| X3 | ITEM 97 QTY IS 7, WAS 6 | 11-12-76 | DWT [illegible] |

**ENGINEERING RELEASE**
COGNIZANT ENGINEER FOX
NOT FOR FABRICATION UNLESS SIGNED BELOW
DATE

| REFERENCE DESIGNATION | FIND NO. |
|---|---|
| U1,2,3,4,5,10,51,56,61,66 | 11 |
| U12,13,27,30,32,36, | 12 |
| U28 | 13 |
| U15,18,22 | 14 |
| U11,29,33,34,37 | 15 |
| U31,35 | 16 |
| U17 | 17 |
| U19 | 18 |
| U23,38,47,50,52,55,57,60, 62,65,67,70,71,74,75, 78,79,82 | 19 |
| U21 | 20 |
| U16,20 | 21 |
| U6,7,8,9 | 22 |
| U24,25,26 | 23 |
| U14, U39-46 | 24 |
| U48,49,53,54,58,59, 63,64,68,69,72,73,76, 77,80,81 | 25 |
| R127,129,141,143,155,157, 169,171,183,185,197,199, 211,213,225,227 | 27 |
| | 28 |
| R39,40,43 | 29 |
| R37 | 30 |
| R126,128,140,142,154, 156,168,170,182,184, 196,198,210,212,224,226 | 31 |
| R51-54, R60-63, 230, 231 | 32 |
| R2 | 33 |
| R116,117,119,121,130,131, 134,135,144,145,148,149, 158,159,162,163,172,173, 176,177,186,187,190,191, 200,201,204,205,214, 215,218,219 | 35 |
| R26,27,28,29,38,55,57, 66-81,84-99 | 36 |
| R44,50,59 | 37 |
| R13,9 | 38 |
| R8,20,21,41,42,45 | 39 |
| R12,24,33,34,35,36 | 40 |
| R6,7, 25,30 | 41 |
| R22,23 | 42 |
| R46,47 | 43 |
| R1,3,4,5,10,14,19 | 44 |
| R15,17 | 45 |
| R228 | 46 |
| R118,120,122,123,132,133, 136,137,146,147,150,151, 160,161,164,165,174,175, 178,179,188,189,192,193, 202,203,206,207,216, 217,220,221 | 47 |
| R56,58 | 48 |
| R82,83 | 49 |
| R32 | 51 |
| R49,65 | 53 |
| R31 | 55 |
| R232 | 50 |
| R124,125,138,139,152, 153,166,167,180,181,194, 195,208,209,222,223 | 57 |
| R11 | 59 |
| C15 | 61 |
| C13,20 | 62 |
| C30 | 63 |
| C1,16,17,19,28,41,42, 51,52,57,58,63,64,69, 70,75,76,81,82,87, 88 | 64 |
| C14 | 65 |
| C37,38,47,48,53,54, 59,60,65,66,71,72,77, 78,83,84 | 66 |
| C9,10,11,12,27,90-105, 107,108 | 67 |
| C3-8,25,26,29,32,33, 34,35,36,43,44,45,46, 89,106,109 | 68 |
| C23,24,39,40,49,50, 55,56,61,62,67,68, 73,74,79,80,85,86 | 69 |
| Q7,11,12,13,14,21-53 | 71 |
| Q1,2,5,6,10,20 | 72 |
| Q3,4,8,9,15,16,17,18,19,54 | 73 |
| QU1-13 | 75 |
| TU1-22 | 77 |
| RU7-14 | 79 |
| RU1-6,15 | 80 |
| CRU2,4,6,8 | 82 |
| CRU 1,3,5,7,9,10,11,12,13, 14,15,16 | 83 |
| CR2-68 | 84 |
| CR1 | 85 |
| RT1 | 87 |
| L1,2 | 89 |
| TB1 | 91 |
| C110 | 70 |
| RU16, RU17 | 81 |
| R16,18,48,64,229, C2,C31 ARE LAB SET | - |



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET B-2 |

FORM 000021

| REVISION STATUS | NOTE | QTY REQD | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | SPECIFICATION | CODE IDENT NO. | ZONE | FIND NO. | SYM | C/I USAGE | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | C/I CODE | INV ON HAND | PAR | UNIT COST |
| | | 1 | 700943-001 | PRINTED WIRING BOARD | | | | 1 | B | | | | |
| | (12) | 1 | 700066-136 | PLUG, ADDRESS STRAPPING (0-16K) | | | | 2 | B | | | | |
| | | 1 | 700298-100 | CORE MEMORY-PLANAR | | | | 3 | B | | | | |
| | | 1 | 700407 001 | STIFFENER | | | | 4 | B | | | | |
| | | 156 | 86477-2 | RECEPTACLE | AMP | 04618 | | 5 | A | | | | |
| | | 1 | 700369-002 | INSULATOR | | | | 6 | B | | | | |
| | | 2 | MS51957-4 | SCREW, 2-56 X 5/16 | | | | 7 | A | | | | |
| | | 6 | N440-4 | SCREW, 4-40 X 1/4 NYLON BINDER HEAD | WECKESSER | 95987 | | 8 | A | | | | |
| | | 2 | NAS1291C02 | NUT, HEX #2 SELF LOCKING | | | | 9 | A | | | | |
| | | 10 | N-440-X | NUT-HEX | WECKESSER | 95987 | | 10 | A | | | | |
| | | 10 | 136021-381 | QUAD 2-INPUT NOR | | | | 11 | B | | | | |
| | | 6 | SN74H00N | QUAD 2-INPUT NAND | T.I. | 01295 | | 12 | A | | | | |
| | | 1 | SN7402N | QUAD 2-INPUT POSITIVE NOR GATE | T.I. | 01295 | | 13 | A | | | | |
| | | 3 | SN74H04N | HEX INVERTER | T.I. | 01295 | | 14 | A | | | | |
| | | 5 | SN74H08N | QUAD 2-INPUT AND BUFFER | T.I. | 01295 | | 15 | A | | | | |
| | | 2 | SN74H10N | TRIPLE 3-INPUT POSITIVE NAND GATE | T.I. | 01295 | | 16 | A | | | | |
| | | 1 | SN74H20N | DUAL 4-INPUT POSITIVE NAND GATE | T.I. | 01295 | | 17 | A | | | | |
| | | 1 | SN74H30N | 8-INPUT POSITIVE NAND GATE | T.I. | 01295 | | 18 | A | | | | |
| | | 18 | 136000-038 | QUAD 2-INPUT NAND BUFFER GATE O.C. | | | | 19 | B | | | | |
| | | 1 | SN74H51N | DUAL AND/OR INVERTER | T.I. | 01295 | | 20 | A | | | | |
| | | 2 | SN74H74N | DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP | T.I. | 01295 | | 21 | A | | | | |
| | | 4 | SN7475N | QUAD D-FLIP FLOP | T.I. | 01295 | | 22 | A | | | | |
| | | 3 | SN74123N | DUAL 1-SHOT | T.I. | 01295 | | 23 | A | | | | |
| | | 9 | SN74145N | BCD DECODER DRIVER | T.I. | 01295 | | 24 | A | | | | |
| | | 16 | SN7520N | DUAL-CHANNEL SENSE AMPLIFIERS/COMP OUTPUTS | T.I. | 01295 | | 25 | A | | | | |
| | | | | | | | | 26 | | | | | |



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET B-3 |

| ITEM | NOTE | QTY REQD | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | SPECIFICATION | CODE IDENT NO. | ZONE | FIND NO. | SYM | C/I USAGE | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | C/I CODE | INV ON HAND | PAR | MFST CHST |
| | | 16 | RN55D10R0F | RESISTOR, 10Ω, ±1%, 1/8W | CORNING GLASS | 16299 | | 27 | A | | | | |
| | | | | | | | | 28 | | | | | |
| | | 3 | RN55D5620F | 562Ω | | 16299 | | 29 | A | | | | |
| | | 1 | RN55D1001F | 1K | | 16299 | | 30 | A | | | | |
| | | 16 | RN55D2741F | 2.74K, ±1%, 1/8W | CORNING GLASS | 16299 | | 31 | A | | | | |
| | | 10 | RC07GF220J | 22Ω, ±5%, 1/4W | MIL-R-11 | | | 32 | A | | | | |
| | | 1 | RC07GF151J | 150Ω | | | | 33 | A | | | | |
| | | | | | | | | 34 | | | | | |
| | | 32 | RC07GF390J | 39Ω | | | | 35 | A | | | | |
| | | 39 | RC07GF470J | 47Ω | | | | 36 | A | | | | |
| | | 3 | RC07GF101J | 100Ω | | | | 37 | A | | | | |
| X2 | | 2 | RC07GF221J | 220Ω | | | | 38 | A | | | | |
| | | 6 | RC07GF331J | RESISTOR, 330Ω ±5%, 1/4W | MIL-R-11 | | | 39 | A | | | | |
| | | 6 | RC07GF471J | RESISTOR, 470Ω, ±5%, 1/4W | MIL-R-11 | | | 40 | A | | | | |
| X2 | | 4 | RC07GF102J | 1K | | | | 41 | A | | | | |
| | | 2 | RC07GF222J | 2.2K | | | | 42 | A | | | | |
| | | 2 | RC07GF332J | 3.3K | | | | 43 | A | | | | |
| | | 7 | RC07GF472J | 4.7K | | | | 44 | A | | | | |
| | | 2 | RC07GF103J | 10K, ±5%, 1/4W | | | | 45 | A | | | | |
| | | 1 | RN60D46R4F | 46.4Ω, ±1%, 1/4W | | | | 46 | A | | | | |
| | | 32 | RC20GF750J | 75Ω, ±5%, 1/2W | | | | 47 | A | | | | |
| | | 2 | RC20GF221J | 220Ω | | | | 48 | A | | | | |
| | | 2 | RC20GF391J | 390Ω, ±5%, 1/2W | | | | 49 | A | | | | |
| | | 1 | RC07GF681J | 680Ω, ±5%, 1/4W | | | | 50 | A | | | | |
| | | 1 | RC42GF101J | RESISTOR, 100Ω, ±5%, 2W | MIL-R-11 | | | 51 | A | | | | |
| | | | | | | | | 52 | | | | | |



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET B-4 |

| | NOTE | QTY REQD | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | SPECIFICATION | CODE IDENT NO. | ZONE | FIND NO. | SYM | C/I USAGE | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | C/I CODE | INV ON BOARD | PAR | UNIT COST |
| | (14) | 2 | M18-N | RESISTOR, 7.5Ω, ±1%, 2.5W, WW, NI | CF ELECTRONICS | 21551 | | 53 | A | | | | |
| | | | | | | | | 54 | | | | | |
| | | 1 | M30 | 52Ω, ±5%, 5W, WW | CF ELECTRONICS | 21551 | | 55 | A | | | | |
| | | | | | | | | 56 | | | | | |
| | | 16 | M30-N | 12Ω, 5W, ±1%, 5W, WW, NI | CF ELECTRONICS | 21551 | | 57 | A | | | | |
| | | | | | | | | 58 | | | | | |
| | | 1 | 3005P-1-103 | RESISTOR, VARIABLE, 10K, ±10%, 1/2 W, WIREWOUND | BOURNS | 80294 | | 59 | A | | | | |
| | | | | | | | | 60 | | | | | |
| | | 1 | CD15CD100J03 | CAPACITOR, 10 Pf ±5% | CORNELL DUBILIER | 93730 | | 61 | A | | | | |
| | | 2 | CD15ED220J03 | 22Pf | | 93730 | | 62 | A | | | | |
| | | 1 | CD15ED470J03 | 47 Pf | | 93730 | | 63 | A | | | | |
| | | 21 | CD15FD101J03 | 100 Pf | | 93730 | | 64 | A | | | | |
| | | 1 | CD15FD221J03 | CAPACITOR 220 Pf ±5% | CORNELL DUBILIER | 93730 | | 65 | A | | | | |
| | | 16 | K065K272K | CAPACITOR 2700 Pf 200V ± 10% | KEMET | 05397 | | 66 | A | | | | |
| | | 23 | C069B160E 103Z | .01uf 16V +80 -20% | SPRAGUE | 05571 | | 67 | A | | | | |
| | | 21 | 150D 475X 0010A2 | 4.7uf 10V ±20% | SPRAGUE | 05571 | | 68 | A | | | | |
| | | 18 | 150D 156X 0020B2 | CAPACITOR 15uf 20V ± 20% | SPRAGUE | 05571 | | 69 | A | | | | |
| | | 1 | CK05BX102K | CAPACITOR 1000 pf 200V ±10% | MIL-C-11015 | | | 70 | A | | | | |
| | | 38 | 2N3725 | TRANSISTOR | T.I. | 01295 | | 71 | A | | | | |
| | | 6 | 2N2369A | TRANSISTOR | T.I. | 01295 | | 72 | A | | | | |
| | | 10 | 2N2905 | TRANSISTOR | T.I. | 01295 | | 73 | A | | | | |
| | | | | | | | | 74 | | | | | |
| | | 13 | DH3725CN | TRANSISTOR QUAD | NATIONAL SEMI-COND. | 27014 | | 75 | A | | | | |
| | | | | | | | | 76 | | | | | |
| | | 22 | 132300-003 | TRANSFORMER MODULE | | | | 77 | A | | | | |
| | | | | | | | | 78 | | | | | |



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV | SHEET B-5 |

| EQUIP CODE | NOTE | QTY REQD | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | SPECIFICATION | CODE IDENT NO. | ZONE | FIND NO. | SYM | C/I USAGE: C/I CODE | C/I USAGE: INV ON HAND | C/I USAGE: PAR | C/I USAGE: UNIT COST |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 8 | 100013-001 | RESISTOR MODULE, 150Ω | CTS NO 964-2 | 11236 | | 79 | A | | | | |
| | | 7 | 100013-002 | RESISTOR MODULE, 470Ω | CTS NO 964-1 | 11236 | | 80 | A | | | | |
| | | 2 | 100013-008 | RESISTOR MODULE, 47Ω | NAT. ENG. NE7309-C57 | | | 81 | A | | | | |
| | | 4 | 700042-101 | DIODE MODULE, COMMON "C" | | | | 82 | B | | | | |
| | | 12 | 700042-100 | DIODE MODULE, COMMON "A" | | | | 83 | B | | | | |
| | | 67 | 138000-001 | DIODE, HIGH CONDUCTANCE | | | | 84 | A | | | | |
| | | 1 | IN751A | DIODE, ZENER 5.1V | T.I. | 01295 | | 85 | A | | | | |
| | | | | | | | | 86 | | | | | |
| | | 1 | TM-1/4 | THERMISTOR, 1K, ±5% | T.I | 01295 | | 87 | A | | | | |
| | | | | | | | | 88 | | | | | |
| | | 2 | WEE-22 | CHOKE, 22 uh, ±10% | NYTRONICS | 43543 | | 89 | A | | | | |
| | | | | | | | | 90 | | | | | |
| | | 1 | CSA 3100-16B | SOCKET, 16 PIN | S.A.E. | 31514 | | 91 | A | | | | |
| | | AR | 5951 | WIRE, 30 AWG, SOLID COND., KYNAR INSUL., COLOR: WHT | ALPHA WIRE OR EQUIV. | 29172 | | 92 | G | | | | |
| | | | | | | | | 93 | | | | | |
| | | 1 | 700346-001 | BUS BAR (16 CONDUCTOR) | | | | 94 | B | | | | |
| | | 48 | 10079 | TRANSIPAD (TO-5) | MILTON ROSS | 07047 | | 95 | A | | | | |
| | | 6 | 10216 | TRANSIPAD (TO-18) | MILTON ROSS | 07047 | | 96 | A | | | | |
| X3 | | 7 | R-62-3 | BEAD PINS | MOLEX | 27264 | | 97 | | | | | |
| | | 2 | 100330-001 | HANDLE-EXTRACTOR | | | | 98 | B | | | | |
| | | 2 | 700331-001 | SPACER | | | | 99 | B | | | | |
| | | | | | | | | 100 | | | | | |
| | | AR | TYPE 7342 | ELECTRICAL TAPE, 3/8 INCH WIDE | MYSTIK DIV BORDEN CHEM | 88301 | | 101 | A | | | | |



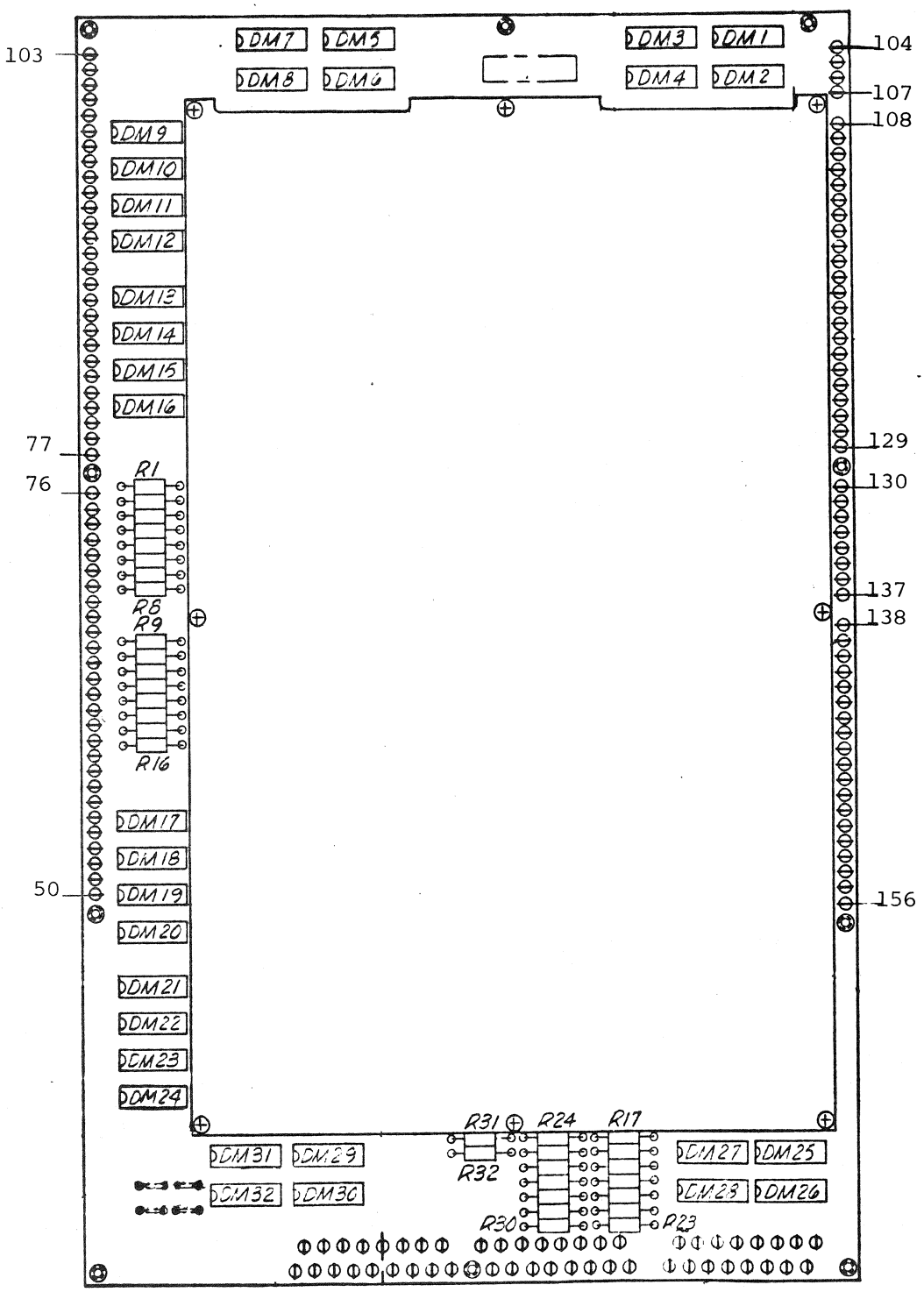
| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV | SHEET B-6 |

# Appendix C

# Schematic Diagrams



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET C-1 |




PM-1116B PLANAR CORE STACK



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET C-2 |

| | | X SINK | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| X DRIVE | 0 | 0 | 4 | 8 | 12 | 16 | 20 | 24 | 28 | 32 | 36 | 40 | 44 | 48 | 52 | 56 | 60 |
| | 1 | 1 | 5 | 9 | 13 | 17 | 21 | 25 | 29 | 33 | 37 | 41 | 45 | 49 | 53 | 57 | 61 |
| | 2 | 34 | 38 | 42 | 46 | 50 | 54 | 58 | 62 | 2 | 6 | 10 | 14 | 18 | 22 | 26 | 30 |
| | 3 | 35 | 39 | 43 | 47 | 51 | 55 | 59 | 63 | 3 | 7 | 11 | 15 | 19 | 23 | 27 | 31 |
| | 4 | 64 | 68 | 72 | 76 | 80 | 84 | 88 | 92 | 96 | 100 | 104 | 108 | 112 | 116 | 120 | 124 |
| | 5 | 65 | 69 | 73 | 77 | 81 | 85 | 89 | 93 | 97 | 101 | 105 | 109 | 113 | 117 | 121 | 125 |
| | 6 | 98 | 102 | 106 | 110 | 114 | 118 | 122 | 126 | 66 | 70 | 74 | 78 | 82 | 86 | 90 | 94 |
| | 7 | 99 | 103 | 107 | 111 | 115 | 119 | 123 | 127 | 67 | 71 | 75 | 79 | 83 | 87 | 91 | 95 |

CORE STACK X LINES

| | | Y SINK | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Y DRIVE | 0 | 0 | 1 | 4 | 5 | 8 | 9 | 12 | 13 |
| | 1 | 16 | 17 | 20 | 21 | 24 | 25 | 28 | 29 |
| | 2 | 2 | 3 | 6 | 7 | 10 | 11 | 14 | 15 |
| | 3 | 18 | 19 | 22 | 23 | 26 | 27 | 30 | 31 |
| | 4 | 32 | 33 | 36 | 37 | 40 | 41 | 44 | 45 |
| | 5 | 48 | 49 | 52 | 53 | 56 | 57 | 60 | 61 |
| | 6 | 34 | 35 | 38 | 39 | 42 | 43 | 46 | 47 |
| | 7 | 50 | 51 | 54 | 55 | 58 | 59 | 62 | 63 |

STACK "A"

| | | Y SINK | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| Y DRIVE | 0 | 64 | 65 | 68 | 69 | 72 | 73 | 76 | 77 |
| | 1 | 80 | 81 | 84 | 85 | 88 | 89 | 92 | 93 |
| | 2 | 66 | 67 | 70 | 71 | 74 | 75 | 78 | 79 |
| | 3 | 82 | 83 | 86 | 87 | 90 | 91 | 94 | 95 |
| | 4 | 96 | 97 | 100 | 101 | 104 | 105 | 108 | 109 |
| | 5 | 112 | 113 | 116 | 117 | 120 | 121 | 124 | 125 |
| | 6 | 98 | 99 | 102 | 103 | 106 | 107 | 110 | 111 |
| | 7 | 114 | 115 | 118 | 119 | 122 | 123 | 126 | 127 |

STACK "B"

CORE STACK Y LINES



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET C-3 |

| PIN NO. | FUNCTION | PIN NO. | FUNCTION | PIN NO. | FUNCTION | PIN NO. | FUNCTION |
|---|---|---|---|---|---|---|---|
| 1 | XS0 | 21 | YS4 | 41 | CC0 | 61 | S9B+ |
| 2 | XS1 | 22 | YS5 | 42 | CC1 | 62 | S9B- |
| 3 | XS2 | 23 | YS6 | 43 | CC2 | 63 | I9B |
| 4 | XS3 | 24 | YS7 | 44 | CC3 | 64 | 0V |
| 5 | XS4 | 25 | YS8 | 45 | CC4 | 65 | S10A+ |
| 6 | XS5 | 26 | YS9 | 46 | CC5 | 66 | S10A- |
| 7 | XS6 | 27 | YS10 | 47 | CC6 | 67 | I10A |
| 8 | XS7 | 28 | YS11 | 48 | CC7 | 68 | S10B+ |
| 9 | XS8 | 29 | YS12 | 49 | BIAS | 69 | S10B- |
| 10 | XS9 | 30 | YS13 | 50 | 0V | 70 | I10B |
| 11 | XS10 | 31 | YS14 | 51 | 0V | 71 | S11A+ |
| 12 | XS11 | 32 | YS15 | 52 | S8A+ | 72 | S11A- |
| 13 | XS12 | 33 | CA0 | 53 | S8A- | 73 | I11A |
| 14 | XS13 | 34 | CA1 | 54 | I8A | 74 | S11B+ |
| 15 | XS14 | 35 | CA2 | 55 | S8B+ | 75 | S11B- |
| 16 | XS15 | 36 | CA3 | 56 | S8B- | 76 | I11B |
| 17 | YS0 | 37 | CA4 | 57 | I8B | 77 | S12A+ |
| 18 | YS1 | 38 | CA5 | 58 | S9A+ | 78 | S12A- |
| 19 | YS2 | 39 | CA6 | 59 | S9A- | 79 | I12A |
| 20 | YS3 | 40 | CA7 | 60 | I9A | 80 | S12B+ |

| PIN NO. | FUNCTION | PIN NO. | FUNCTION | PIN NO. | FUNCTION | PIN NO. | FUNCTION |
|---|---|---|---|---|---|---|---|
| 81 | S12B- | 101 | I15B | 121 | S5B+ | 141 | I2B |
| 82 | I12B | 102 | 0V | 122 | S5B- | 142 | 0V |
| 83 | S13A+ | 103 | 0V | 123 | I5B | 143 | S1A+ |
| 84 | S13A- | 104 | 0V | 124 | S4A+ | 144 | S1A- |
| 85 | I13A | 105 | S7A+ | 125 | S4A- | 145 | I1A |
| 86 | S13B+ | 106 | S7A- | 126 | I4A | 146 | S1B+ |
| 87 | S13B- | 107 | I7A | 127 | S4B+ | 147 | S1B- |
| 88 | I13B | 108 | S7B+ | 128 | S4B- | 148 | I1B |
| 89 | 0V | 109 | S7B- | 129 | I4B | 149 | S0A+ |
| 90 | S14A+ | 110 | I7B | 130 | S3A+ | 150 | S0A- |
| 91 | S14A- | 111 | S6A+ | 131 | S3A- | 151 | I0A |
| 92 | I14A | 112 | S6A- | 132 | I3A | 152 | S0B+ |
| 93 | S14B+ | 113 | I6A | 133 | S3B+ | 153 | S0B- |
| 94 | S14B- | 114 | S6B+ | 134 | S3B- | 154 | I0B |
| 95 | I14B | 115 | S6B- | 135 | I3B | 155 | 0V |
| 96 | S15A+ | 116 | I6B | 136 | S2A+ | 156 | 0V |
| 97 | S15A- | 117 | 0V | 137 | S2A- | | |
| 98 | I15A | 118 | S5A+ | 138 | I2A | | |
| 99 | S15B+ | 119 | S5A- | 139 | S2B+ | | |
| 100 | S15B- | 120 | I5A | 140 | S2B- | | |

PIN FUNCTION CHART



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET C-4 |

CC : Common Cathode

CA : Common Anode

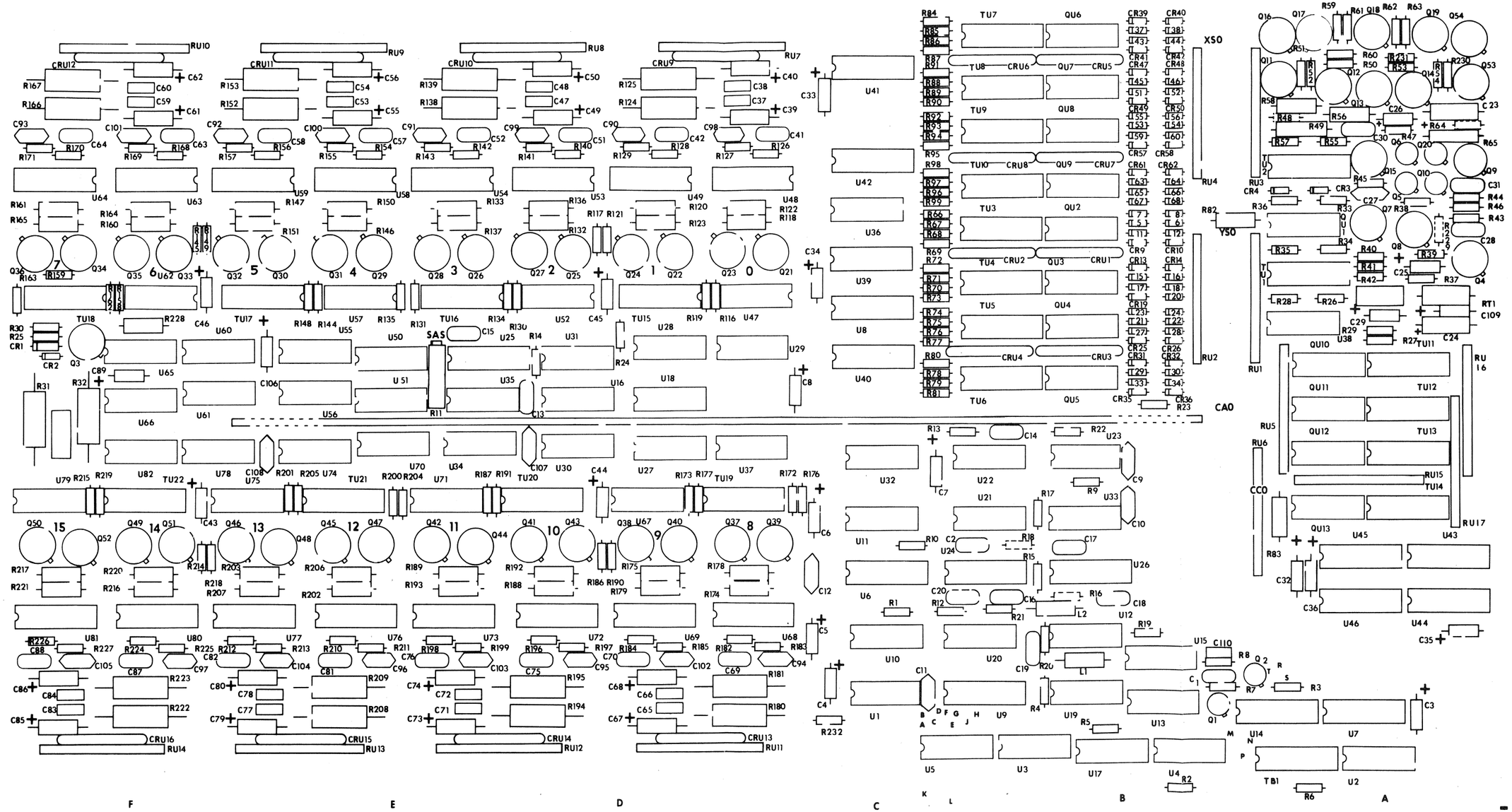
4 6 10 13 no internal connection




TYPICAL DIODE MODULE



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET C-5 |



# Assembly Drawing



| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| A | 52648 | MA 700945 |
| SCALE | REV — | SHEET C-6 |

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | X1 | REL FOR DEV PER ERO 500859 | 8-11-76 | |

| LAST DESIGNATION USED | |
|---|---|
| CAPACITOR | C109 |
| CHOKE | L2 |
| DIODE | CR68 |
| DIODE MODULE | CRU16 |
| INTEGRATED CIRCUIT | U82 |
| RESISTOR | R233 |
| RESISTOR MODULE | RU17 |
| SENSISTOR | RT |
| TRANSISTOR | Q54 |
| TRANSISTOR MODULE | QU13 |
| TRANSFORMER MODULE | TU22 |

| NOT USED | |
|---|---|
| C18, 21, 22, 58 106, 107, 108 | CAPACITOR |
| R109-115, 141, 153 | RESISTOR |
| CR1-4 | DIODE |
| RU1, RU2 | RESISTOR MODULE |
| Q1 | TRANSISTOR |

| AØ | C1 | CØ | MODE | DEFINITION |
|---|---|---|---|---|
| X | H | H | DATI | READ RESTORE |
| X | H | L | DATIP | READ |
| X | L | H | DATO | CLEAR-WRITE |
| H | L | L | DATO BØ | CLEAR WRITE BYTE Ø |
| L | L | L | DATO B1 | CLEAR WRITE BYTE 1 |

A CONNECTOR — COMPONENT SIDE / SOLDER SIDE

| SIDE 1 | | SIDE 2 |
|---|---|---|
| BUS INITL | A | +5V (13) |
| INTR (12) | B | |
| BUS DØØL | C | ØV |
| DØ2L | D | BUS DØ1L |
| DØ4L | E | DØ3L |
| DØ6L | F | DO5L |
| DØ8L | H | DO7L |
| D10L | J | D09L |
| D12L | K | D11L |
| BUS D14L | L | D13L |
| PAL (12) | M | BUS D15L |
| | N | PBL (12) |
| | P | BBSYL |
| | R | SACKL |
| | S | NPRL |
| ØV | T | BR7L |
| | U | BR6L (12) |
| | V | |

B CONNECTOR — COMPONENT SIDE / SOLDER SIDE

| SIDE 1 | | SIDE 2 |
|---|---|---|
| | A | +5V (13) |
| | B | |
| (12) BR5L | C | ØV |
| | D | BR4L (12) |
| | E | |
| ACLOL (12) | F | BUS DCLOL |
| BUS AØ1L | H | AØØL |
| AØ3L | J | AØ2L |
| AØ5L | K | AØ4L |
| AØ7L | L | AØ6L |
| AØ9L | M | AØ8L |
| A11L | N | A10L |
| A13L | P | A12L |
| A15L | R | A14L |
| BUS A17L | S | A16L |
| ØV | T | C1L |
| BUS SSYNL | U | BUS CØL |
| BUS MSYNL | V | |

C,D,E,F CONNECTORS — COMPONENT SIDE / SOLDER SIDE

| SIDE 1 | | SIDE 2 |
|---|---|---|
| (11) | A | +5V |
| | B | -15V |
| | C | ØV |
| | D | |
| | E | |
| | F | |
| | H | |
| | J | |
| | K | (11) |
| | L | |
| | M | |
| | N | |
| | P | |
| | R | |
| | S | |
| ØV | T | (11) |
| (19) BUS MSYNA | U | |
| | V | |

| REF DESIG | GATES USED PER TOTAL | PART NUMBER |
|---|---|---|
| U27 | 3/4 | SN74H10ØN |
| U31 | 2/3 | SN741ØN |
| U33 | 3/4 | SN74-HØ8N |
| U34 | 3/4 | SN74HØ8N |
| U35 | 2/3 | SN741ØN |

| INITIAL ADDRESS | MEMORY SIZE | | TB1 (PIN NUMBERS) 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 6 | 3 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 8K | 4 | X | X | | | | | | | | | | |
| | 16K | 4 | X | X | X | X | | | | | | | | |
| | BOTH | 2 | | | | | | | | | X | | X | |
| | BOTH | 7 | | | | | | | | | | | | |
| 4K | 8K | 4 | | X | X | | | | | | | | | |
| | 16K | 4 | | X | X | X | X | | | | | | | |
| | BOTH | 2 | | | | | | | | | | | X | |
| | BOTH | 7 | | | | | | | | | X | | | |
| 8K | 8K | 4 | | | X | X | | | | | | | | |
| | 16K | 4 | | | X | X | X | X | | | | | | |
| | BOTH | 2 | | | | | | | | | X | | X | |
| | BOTH | 7 | | | | | | | | | | | | |
| 12K | 8K | 4 | | | | X | X | | | | | | | |
| | 16K | 4 | | | | X | X | X | X | | | | | |
| | BOTH | 2 | | | | | | | | | X | | X | |
| | BOTH | 7 | | | | | | | | | | | | |
| 16K | 8K | 4 | | | | | X | X | | | | | | |
| | 16K | 4 | | | | | X | X | X | X | | | | |
| | BOTH | 2 | | | | | | | | | X | | X | |
| | BOTH | 7 | | | | | | | | | | | | |
| 20K | 8K | 4 | | | | | | X | X | | | | | |
| | | 2 | | | | | | | | | X | | X | |
| | | 7 | | | | | | | | | | | | |
| 24K | 8K | 4 | | | | | | | X | X | | | | |
| | | 2 | | | | | | | | | X | | X | |
| | | 7 | | | | | | | | | | | | |

(17) NORMAL OPERATION: JUMPER A TO B, C TO D, E TO F.
8K INTERLEAVE OPERATION: JUMPER A TO D, C TO B.
16K INTERLEAVE OPERATION: JUMPER C TO F, E TO D.

(16) ADD JUMPER W1 FOR 31K OPERATION.
ADD JUMPER W2 FOR MEMORY PROTECTION OPERATION.

(15) FOR 56-72K OPERATION ADD 1K RESISTOR AND USE 700066-164 STRAPPING PLUG.

(14) VALUES ARE LAB SET PER TEST SPEC TS700945

(13) +5V USED FOR TERMINATION ONLY.

(12) SIGNALS ASSIGNED IN UNIBUS BUT NOT USED IN THIS MEMORY.

(11) ON CONNECTOR 'D' ONLY, PIN A IS CONNECTED TO B ON FRONT SIDE (1) & K TO L, M TO N, P TO R, AND S TO T; ON BACK SIDE (2).

(10) EXTERNAL POTENTIOMETER USED TO CONTROL X AND Y DRIVE LINES DURING MEMORY TEST.

9. TRANSFORMER DEVICES NOTED, TU ARE 100003-005
8. TRANSISTOR DEVICES, NOTED, QU, ARE Q2T-3725.
7. ALL TRANSISTORS ARE 2N3725.
6. ALL DIODES ARE 100000
5. CRU1 THRU CRU16 ARE 700042-100.
4. RESISTANCE VALUES ARE IN OHMS ±5%, 1/4W.
3. CAPACITANCE VALUES ARE IN UF +80, -20%.
2. CAPACITANCE TOLERANCE AND VOLTAGES ARE AS FOLLOWS: PF ±5%, 100V; 4.7UF, ±20%, 10V; 15UF, ±20%, 20V.
1. FOR ASSEMBLY DWG SEE 700945.

NOTES: UNLESS OTHERWISE SPECIFIED.

(20) WHEN STRAPPING PLUGS 700066-162 THROUGH 700066-167 ARE USED, REMOVE CIRCUIT (ETCH) FROM M TO N AND ADD JUMPER FROM N TO P. IN ADDITION, FOR 56K-72K (STRAPPING PLUG 700066-164) REMOVE CIRCUIT (ETCH) FROM R TO S AND ADD JUMPER FROM S TO T.

(19) ADD JUMPER 'K' TO L FOR OPERATION OF MSYNA. CAUTION: DO NOT INSTALL THIS JUMPER IF MEMORY IS TO BE INSTALLED INTO A PM-F11/SPC BACKPLANE.

(18) FOR 16K MEMORY, G TO H CONNECTED (ETCH); H TO J IS OPEN. FOR 8K MEMORY, JUMPER J TO H, G TO H IS OPEN (CUT ETCH).

ENGINEERING RELEASE
COGNIZANT ENGINEER FOX
NOT FOR FABRICATION UNLESS SIGNED BELOW
DATE 8-27-76

| | NOTE | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION / MATERIAL | SPEC/SOURCE | CODE IDENT NO. | FIND NO. |
|---|---|---|---|---|---|---|
| | | | | | | 5 |
| | | | | | | 4 |
| | | | | | | 3 |
| | | | | | | 2 |
| | | | | | | 1 |

PARTS LIST

| PART/ASSY NO. & QTY PER ASSY | PART/ASSY REV LTR | NEXT ASSY | USED ON |
|---|---|---|---|
| | SK700945100 | PM1116B | |

APPLICATION

DO NOT SCALE DRAWING

SCREW THREADS PER HANDBOOK H-28
COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM
REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO 250R
ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1
STANDARD HOLE TOLERANCE PER ANSI B32.7
TOLERANCES ON: .XX = ± .02 .XXX = ± .010 ANGLES = ± 0° 30'
INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5
DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH
UNLESS OTHERWISE SPECIFIED

CONTRACT NO.

| | | |
|---|---|---|
| DRAWN | W. Blank | 6 JULY 1976 |
| CHECK | | 8-11-76 |
| ENGR | | |
| PROJ. ENGR | | 8-27-76 |
| PROD. DESIGN | | 8-27-76 |
| OTHER APPROVALS | | |

Plessey Memories Incorporated
Santa Ana, California

DWG TITLE
SCHEMATIC DIAGRAM
MEMORY SYSTEM
16X16 BITS PM-1116B

| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| D | 52648 | SKSD700945 |

SCALE: NONE | SHEET 1 OF 8 | DISTR NO.

SKSD700945 X1

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | | SEE SHEET ONE | | |

BUS CØL BU2 — 136021-381 U1 — CØ(3/C7)
BUS C1L BT2 — 136021-381 U1 — C1(3/C7)
BUS AØ2L BJ2 — 136021-381 U1 — U6 — CØFH(3/C8)(2/C5) CØFL(3/C7) C1FH(2/A5) C1FL(3/C7)(3/C8)(3/D5) ADØ2(4/B3)(4/C8) AD11(4/B6)(4/C6) — SN7475N
BUS A11L BN1 — 136021-381 U1
BUS AØ3L BJ1 — 136021-381 U2 — A11(2/D4)
BUS AØ4L BK2 — 136021-381 U2 — U7 — ADØ3(4/B3)(4/C3) ADØ4(2/C3)(4/B3) ADØ5(4/B3)(2/C3) ADØ6(2/C3)(4/B3) — SN7475N
BUS AØ5L BK1 — 136021-381 U2
BUS AØ6L BL2 — 136021-381 U2
BUS AØ8L BM2 — 136021-381 U3 — ARSTH(2/C1)
BUS AØ7L BL1 — 136021-381 U3
BUS AØ9L BM1 — 136021-381 U3 — U8 — ADØ8(4/B8)(4/C8) ADØ7(4/B8)(4/C8) ADØ9(4/B8) AD1Ø(4/B6)(4/C6) — SN7475N
BUS A1ØL BN2 — 136021-381 U4
BUS A13L BP1 — 136021-381 U5 — A14(2/C6)
BUS A12L BP2 — 136021-381 U3 — A12(2/D4)
BUS A14L BR2 — 136021-381 U5 — A13 — U9 — AD13(3/B5) AD13(3/B5) AD12(2/B6)(4/C6) AD14(3/B5) AD14(3/B5) AD01(4/D3)(4/B3) — SN7475N
BUS AØ1L BH1 — 136021-381 U5
BUS A15L BR1 — 136021-381 U5 — A15(2/C4) A15'(2/C6)
ØV

+5V R1 4.7K — WRITE PROTECT — U10 — 136021-381 — W2 (16)

BUS MSYL BV1 — 136021-381 U10
MSYNA CU1 — K (19)
BUS A17L BS1 — 136021-381 U4 — U13 SN74HØØN
BUS A16L BS2 — 136021-381 U4 — U13 SN74HØØN — A16
A15'(2/B6) — SN74ZØN U17 — W1 (16) — A13
M — P (20) — (2/B6)A14 (2/B6)A15
R — S (20) — ØV
U14 SN71414SN — TB1 — JUMPERS SHOWN ARE FOR 16K MEMORY WITH STARTING ADDRESS OF Ø.

R232 680 — R4 4.7K — (2/B6) A13 (2/B6) A12 (2/C6) A11 — U17 SN74HZØ — (3/D4) SSYNL — R5 4.7K
U12 SN74HØØN — DCOKH (2/B4) — SN74H3Ø U19 — U15 SN74HØØN — C1 1ØØPF — R7 1K — +5V
(3/D3) MSYNH — U22 SN74HØ4N — U32 SN74HØØN
R8 33Ø — U13 SN74HØØN — CLK2L(3/C8) CLK2H(3/A8)(2/A4) — Q2 2N2369A — ØV
MEMORY BUSY
+5V — R233 (15)

+5V — R9 1K — U23 — CLK1H(3/B8) — 136020-038
+5V — R6 1K — U13 SN74HØØN

Q1 2N2369A — R2 150 — R3 4.7K — ØV
BUS DCLOL BF2 — U4 — U15 SN74HØ4N — DCØKH(3/C4)
AA1 BUS INITL — U10 — 136021-381 — U12 SN74HØØN — INITL(3/C8)
BUS AØØL BH2 — U10 — A0(3/C7) BYTE1H(3/D7) BYTE0H(3/D7)
(2/D1) CLK2H — U16 SN74H74 — WTH (3/B7) RTH (3/C7) — U21 SN74H51 — PAUSEH (3/C8) — BYTEL (3/D5) — U18 SN74HØ4N
(2/D6)CØFH (2/D6)C1FH — U11 SN74HØ8N

U22 SN74HØ4N — ARSTH(2/C6)
U20 SN74H74 — U15 SN74HØ4N — C110 .001pf — SN74H04N
C2 — R10 4.7k — U24 SN74123N — H1-2(3/C8)

+5V — C3 4.7 C4 4.7 C5 4.7 C6 4.7 C7 4.7 C8 4.7 C9 .Ø1 C10 .Ø1 C11 .Ø1 C12 .Ø1 — ØV

| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| D | 52648 | SKSD700945 |
| SCALE: NONE | REV X1 | SHEET 2 OF 8 |

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | | SEE SHEET ONE | | |

SN74H04N
SN74H10
SN74H74
SN74123N
SN74H00N
SN74H08N
SN74H08
SN74H51
SN7402N
136020-038
136020-039
2N3725
2N2369A
2N2905

| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| D | 52648 | SKSD700945 |
| SCALE | REV: X1 | SHEET 3 OF 8 |

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | | SEE SHEET ONE | | |

YW-RTN(3/B3)

700042-101

+5V

TU3 QU2 CRU1 CRU2

R66 47 — CR5 — YS0 — E17

R67 47 — CR6 — CR7 — YS1 — E18

R68 47 — CR8 — CR9 — YS2 — E19

R69 47 — CR10 — CR11 — YS3 — E20

R70 47 — CR12 — CR13 — YS4 — E21

R71 47 — CR14 — CR15 — YS5 — E22

R72 47 — CR16 — CR17 — YS6 — E23

R73 47 — CR18 — CR19 — YS7 — E24

TU4 QU3 CRU3 CRU4

R74 47 — CR20 — CR21 — YS8 — E25

R75 47 — CR22 — CR23 — YS9 — E26

R76 47 — CR24 — CR25 — YS10 — E27

R77 47 — CR26 — CR27 — YS11 — E28

R78 47 — CR28 — CR29 — YS12 — E29

R79 47 — CR30 — CR31 — YS13 — E30

R80 47 — CR32 — CR33 — YS14 — E31

R81 47 — CR34 — CR35 — YS15 — E32

TU5 QU4 CRU5 CRU6

TU6 QU5 — 700042-101 — YR+RTN (3/C3)

+5V — U39 — SN74145N

(2/C6) AD08
(2/B6) AD07
(2/B6) AD09
(4/A8)(RT+WT) AD14L

+5V — U40 — SN74145N

(2/C6) AD08
(2/B6) AD07
(2/B6) AD09
(3/B4)(4/C8) (RT+WT) AD14L

BIAS (4/C4) E45

R83 390, ½W — -15V

C32 4.7

+5V R82 390, ½W

+5V — U41 — SN74145N

(2/B6) AD10
(2/C6) AD11
(2/B6) AD12
(3/C4)(4/B6) (RT+WT) AD13L

RU1 470: YS0 YS1 YS7 YS5 YS8 YS10 YS14 YS12

RU2 470: YS3 YS2 YS4 YS6 YS15 YS9 YS11 YS13

+5V — U42 — SN74145N

(2/B6) AD10
(2/C6) AD11
(2/B6) AD12
(RT+WT) AD13L
(3/C4)(4/C6)

C33 4.7 — C34 4.7

XR-RTN(3/C8)

700042-101

+5V

TU7 QU6 CRU5 CRU6

R84 47 — CR37 — X50 — E1

R85 47 — CR38 — CR39 — X51 — E2

R86 47 — CR40 — CR41 — X52 — E3

R87 47 — CR42 — CR43 — X53 — E4

R88 47 — CR44 — CR45 — X54 — E5

R89 47 — CR46 — CR47 — X55 — E6

R90 47 — CR48 — CR49 — X56 — E7

R91 47 — CR50 — CR51 — X57 — E8

TU8 QU7 CRU7 CRU8

R92 47 — CR52 — CR53 — X58 — E9

R93 47 — CR54 — CR55 — X59 — E10

R94 47 — CR56 — CR57 — X510 — E11

R95 47 — CR58 — CR59 — X511 — E12

R96 47 — CR60 — CR61 — X512 — E13

R97 47 — CR62 — CR63 — X513 — E14

R98 47 — CR64 — CR65 — X514 — E15

R99 47 — CR66 — CR67 — X515 — E16

TU9 QU8 CRU9 CRU10

TU10 QU9 — 700042-101 — XW+RTN (3/C8)

+5V — U43 — SN74145N

(2/C6) AD02
(2/C6) AD03
(2/B6) AD01
(3/A5) WDTL

+5V — U44 — SN74145N

(4/C6) AD04
(4/C6) AD05
(4/C6) AD06
(3/A6) RDTL

RU3 470: X51 X50 X55 X57 X59 X511 X513 X515

RU4 470: X53 X52 X54 X56 X58 X510 X512 X514

+5V — U45 — SN74145N

(2/D4) AD02
(2/C6) AD03
(2/B6) AD01
(3/A5) RDTL

+5V — U46 — SN74145N

(2/C6) AD04
(2/B3) AD05
(2/C6) AD06
(2/A5) WDTL

RU15 470: QM12-9 QM13-9 QM13-1 QM12-6 QM13-13 QM12-2 QM12-1 QM13-2

+ STAB(3/B1)

RU16 47

TU11 QU10

CA0 E33
CA1 E34
CA2 E35
CA3 E36
CA4 E37
CA5 E38
CA6 E39
CA7 E40

TU12 QU11

RU5 470

-15V

+5V

RU6 470

RU16 47

TU13 QU12

CC0 E41
CC1 E42
CC2 E43
CC3 E44
CC4 E45
CC5 E46
CC6 E47
CC7 E48

TU14 QU13

-STAB(3/B1)

C35 4.7 — C36 4.7

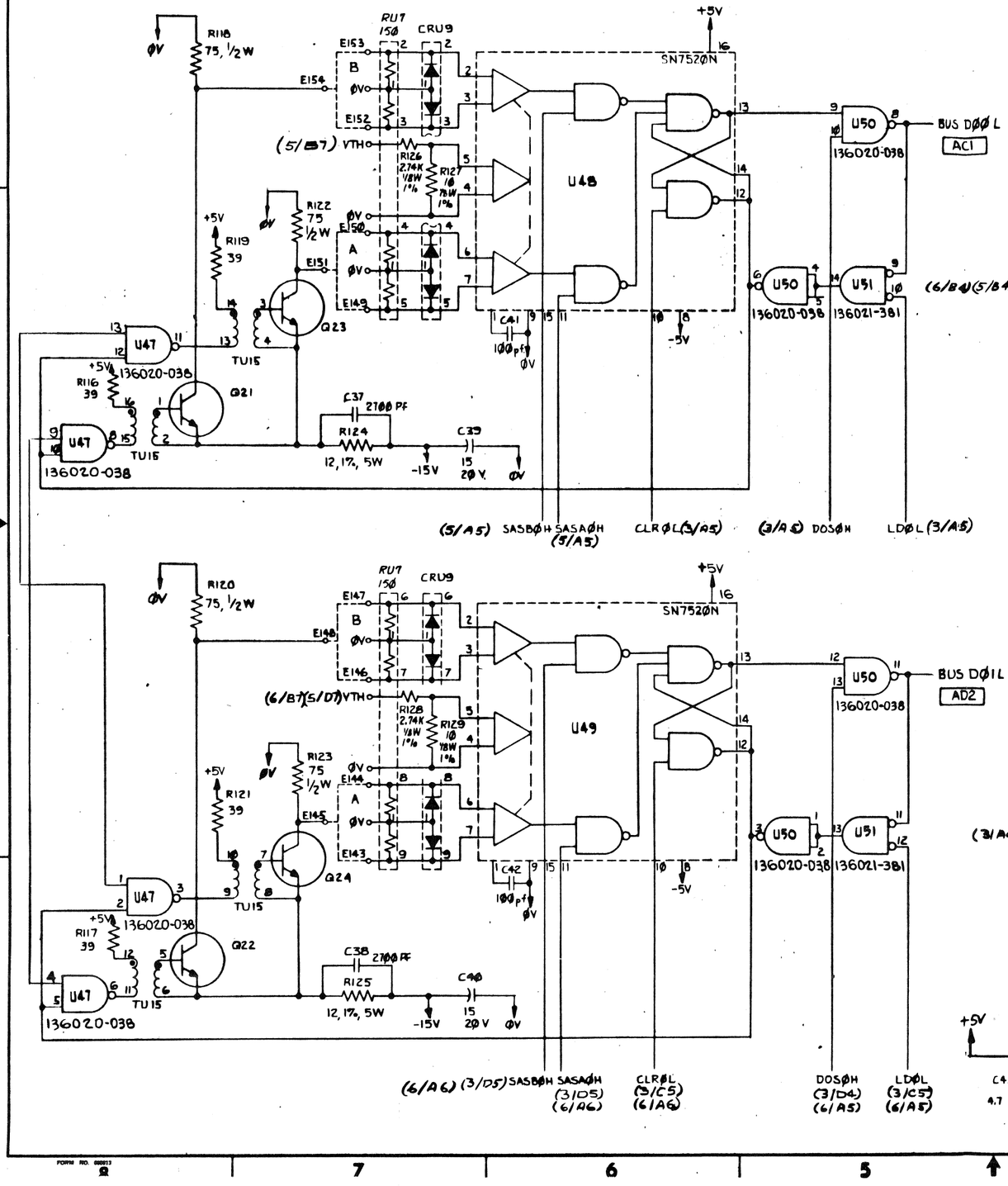
| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| D | 52648 | SKSD700945 |

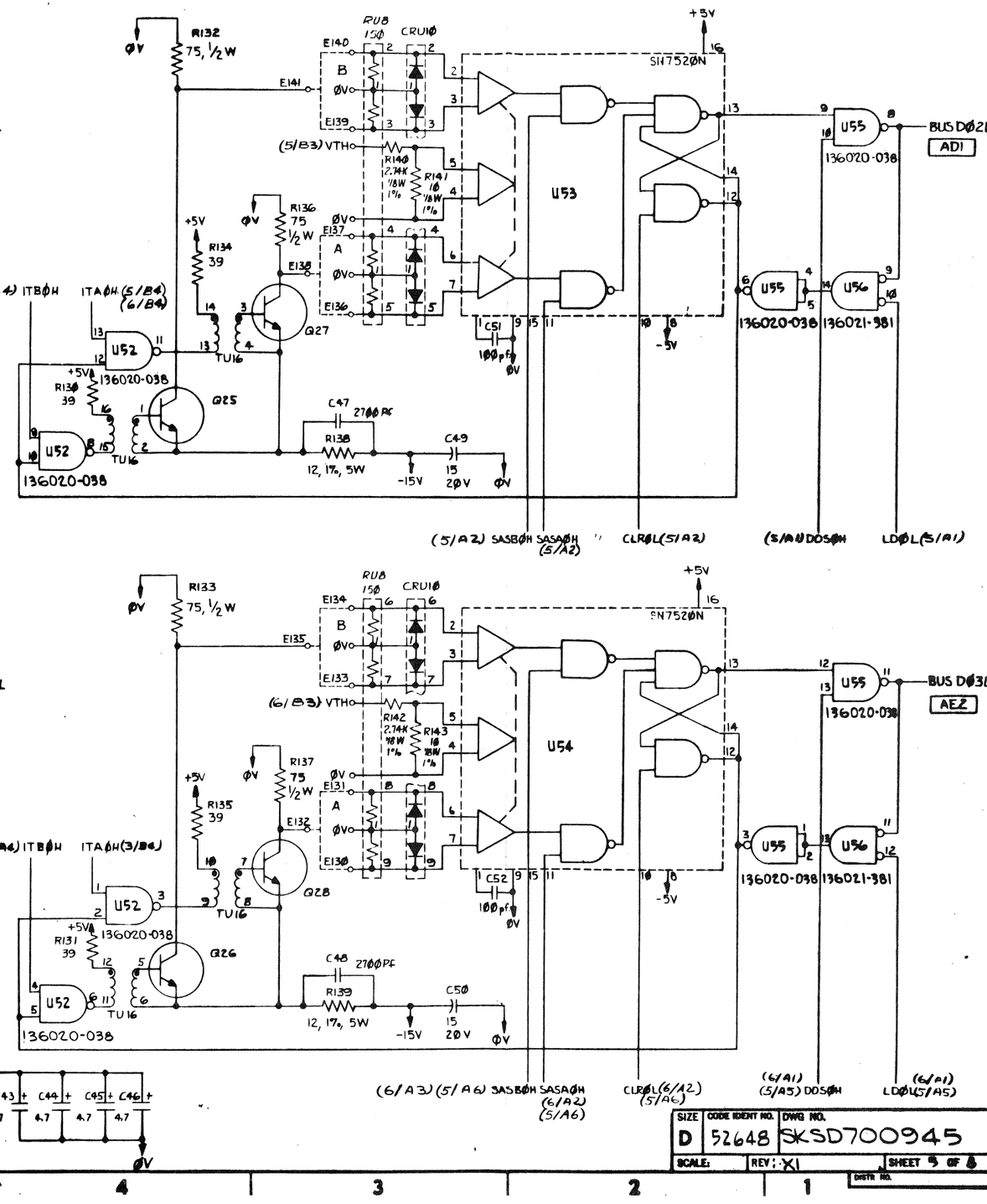
SCALE: — REV: X — SHEET 4 OF 8

DWN BY

C-10

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | | SEE SHEET ONE | | |










| SIZE | CODE IDENT NO. | DWG NO. |
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| D | 52648 | SKSD700945 |
| SCALE: | REV: X1 | SHEET 5 OF 8 |
| | | DISTR NO. |

FORM NO. 600013

| REVISIONS | | | | |
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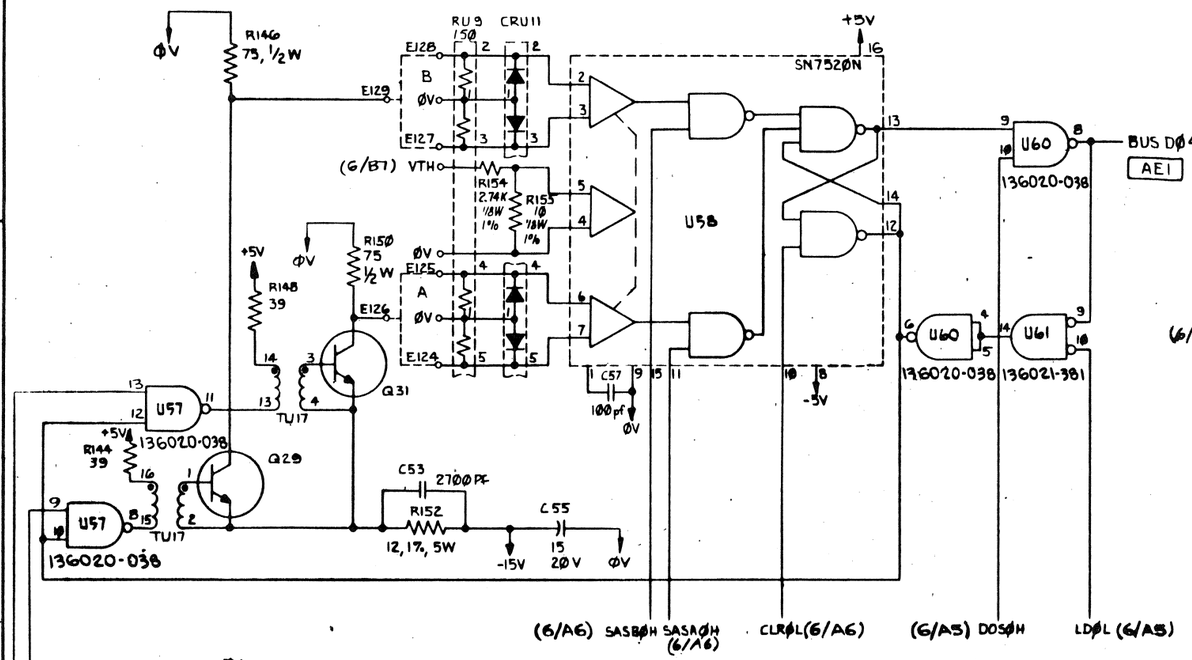
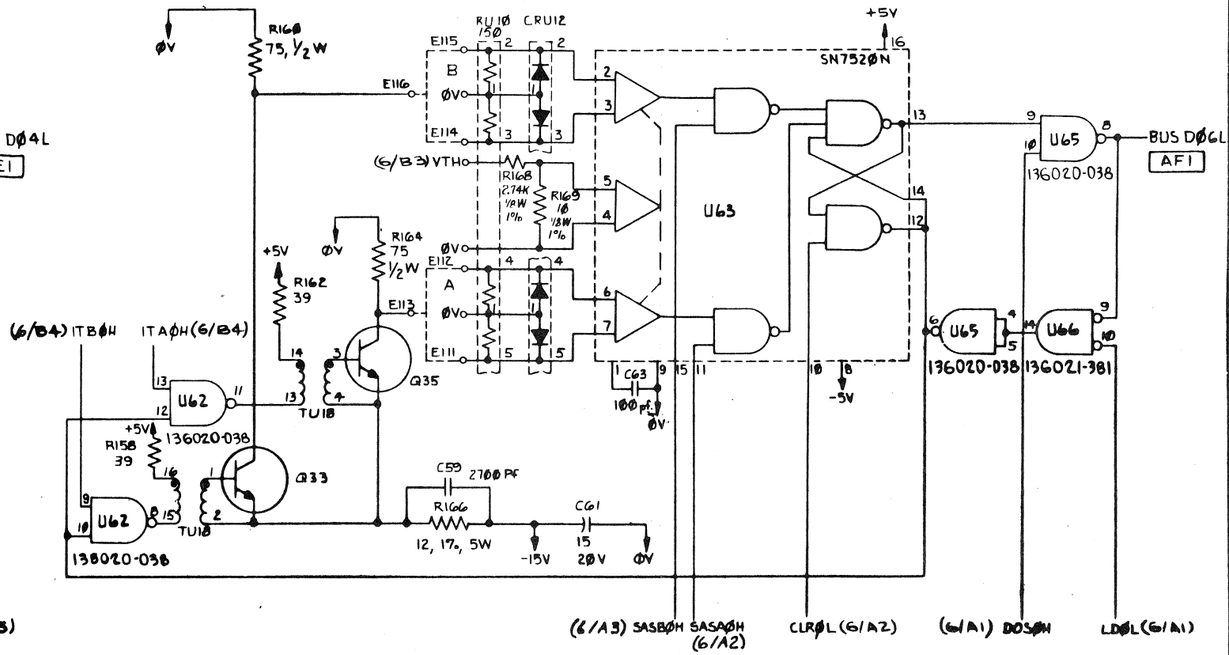
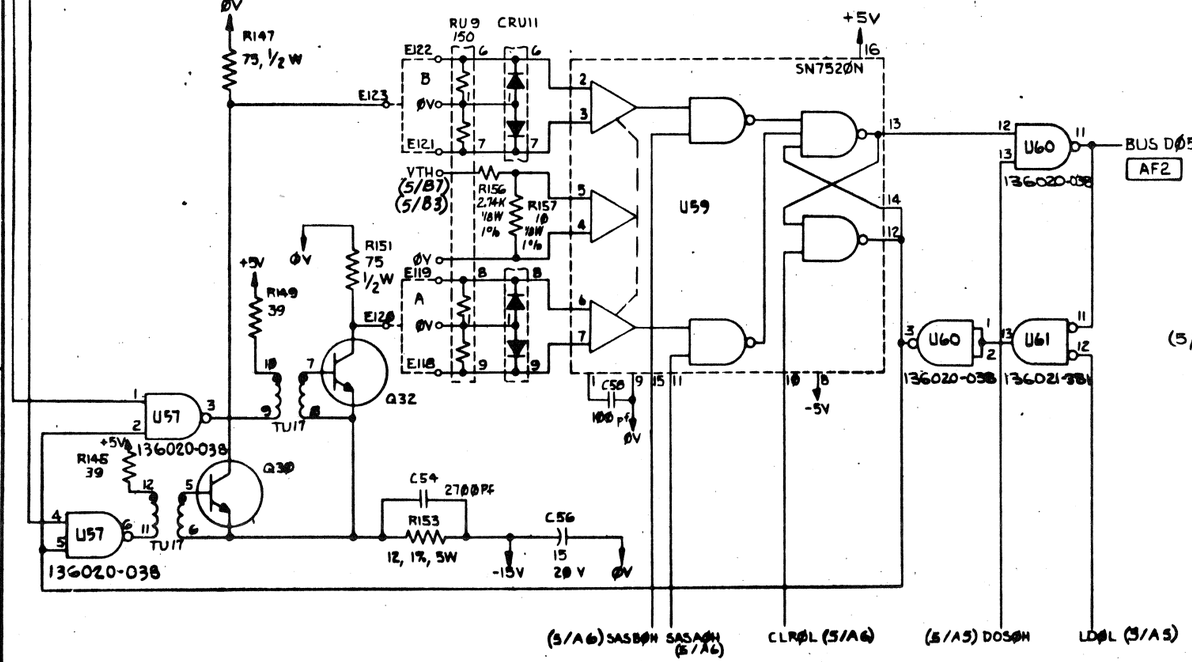
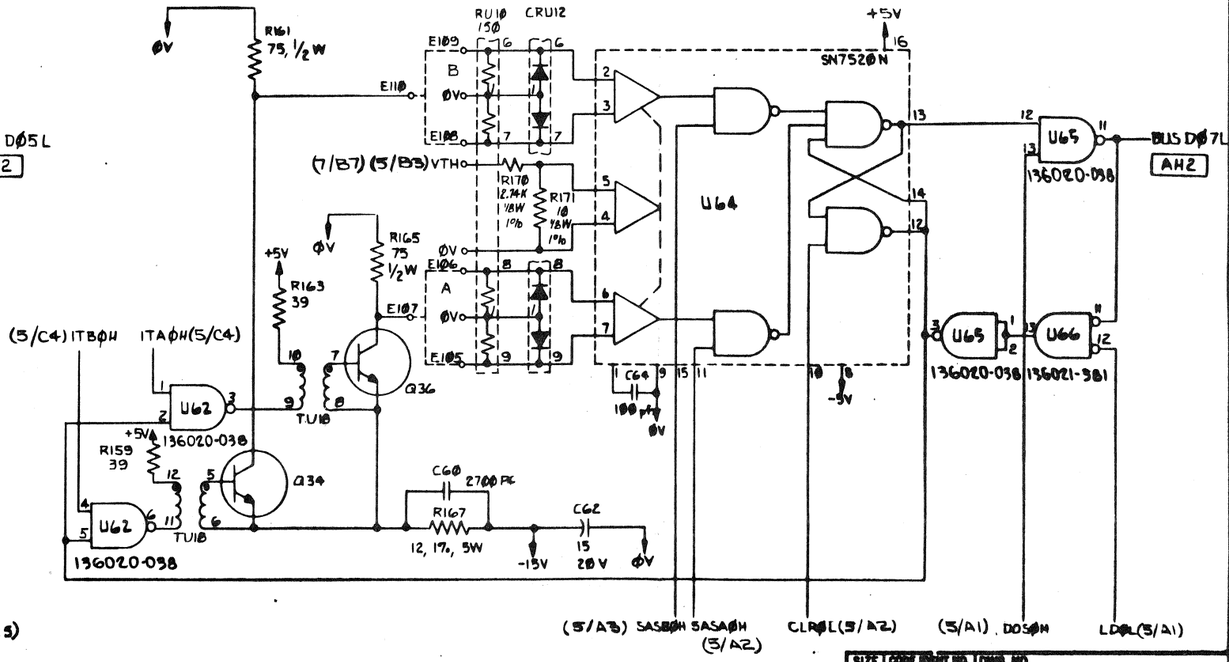
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | | SEE SHEET ONE | | |




| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| D | 52648 | SD700945 |
| SCALE: | REV: X1 | SHEET 6 OF 8 |

| REVISIONS | | | | |
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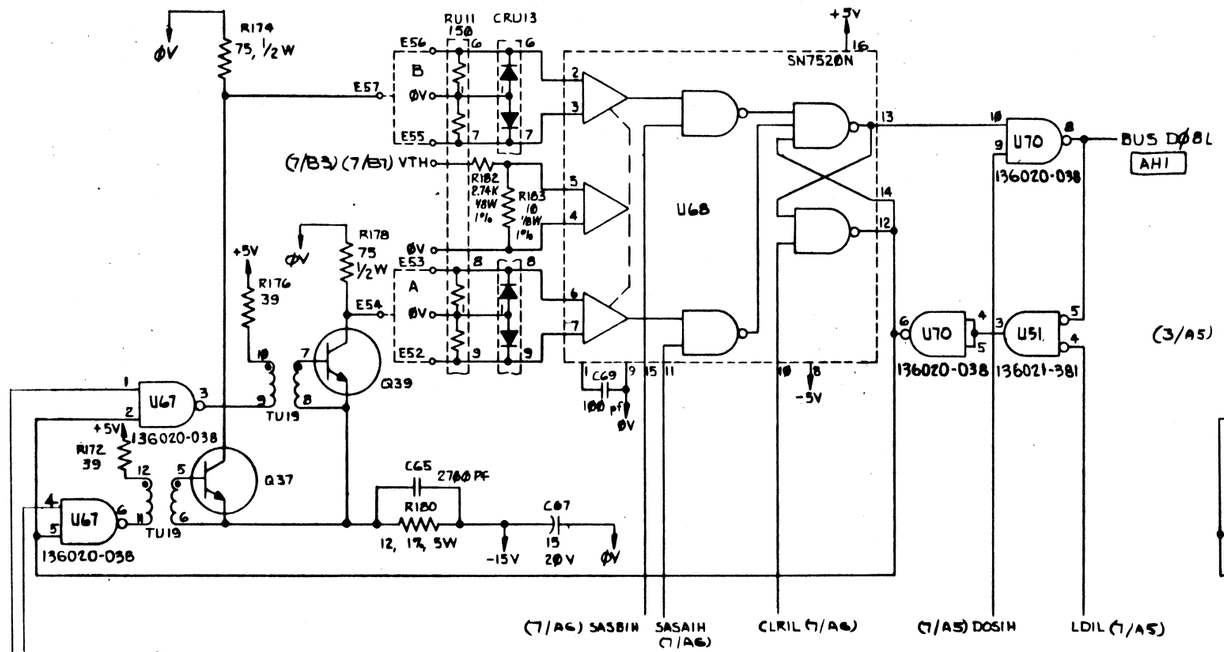
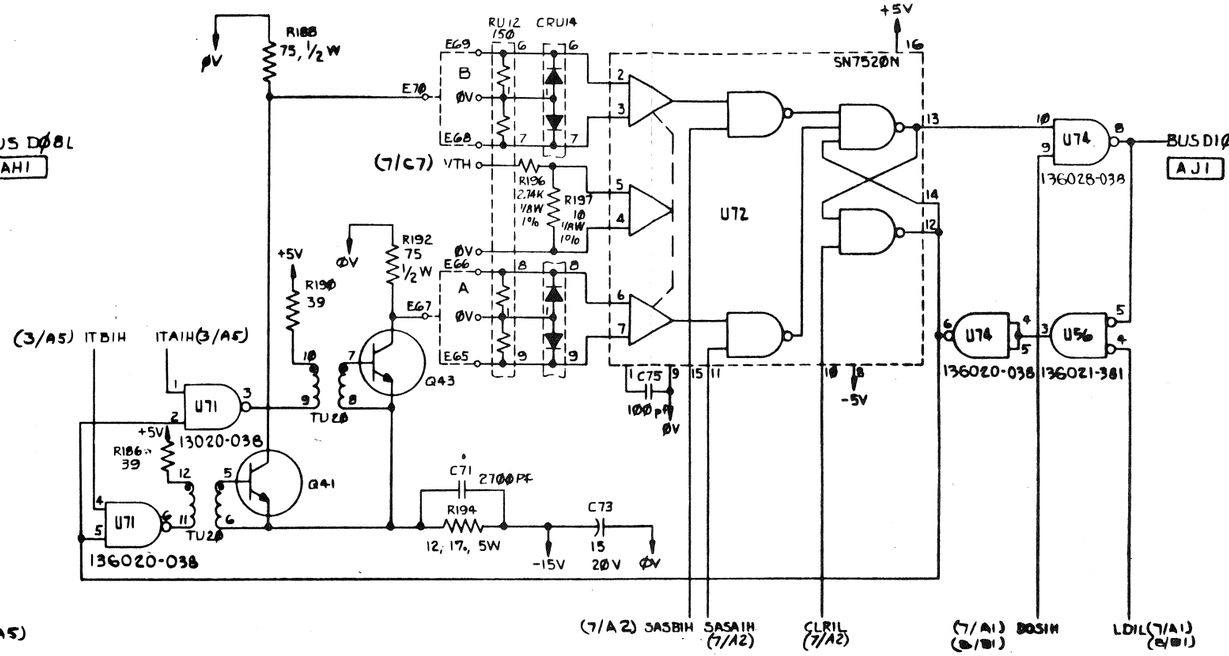
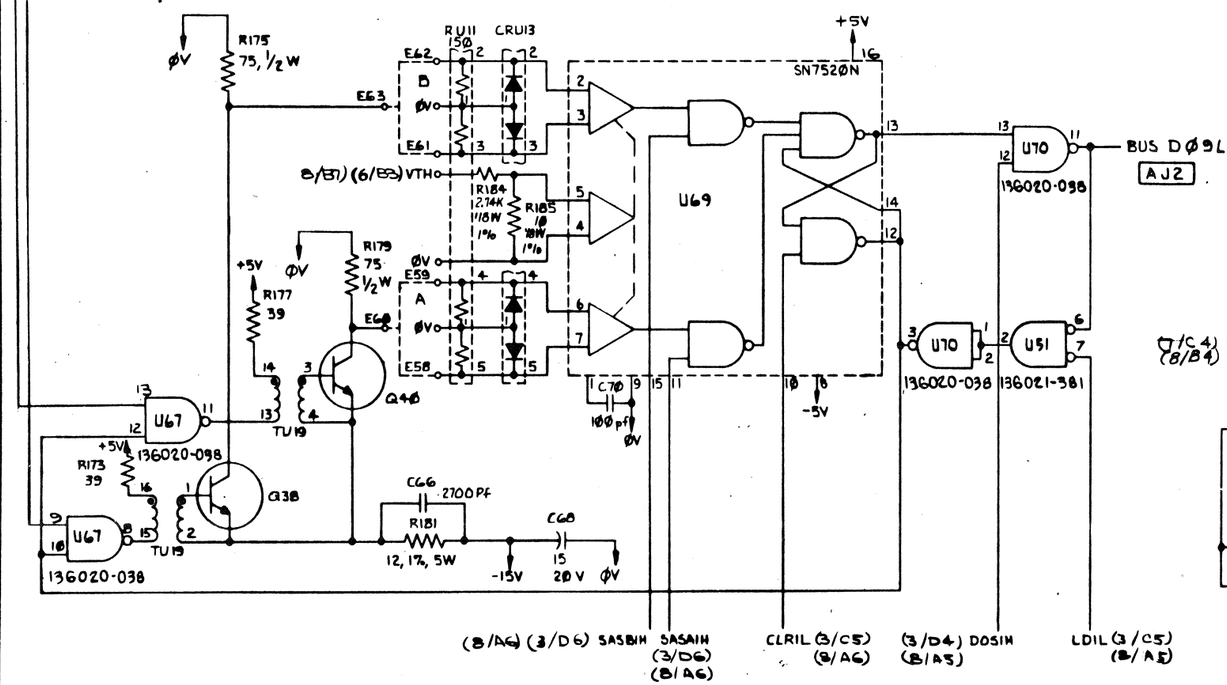
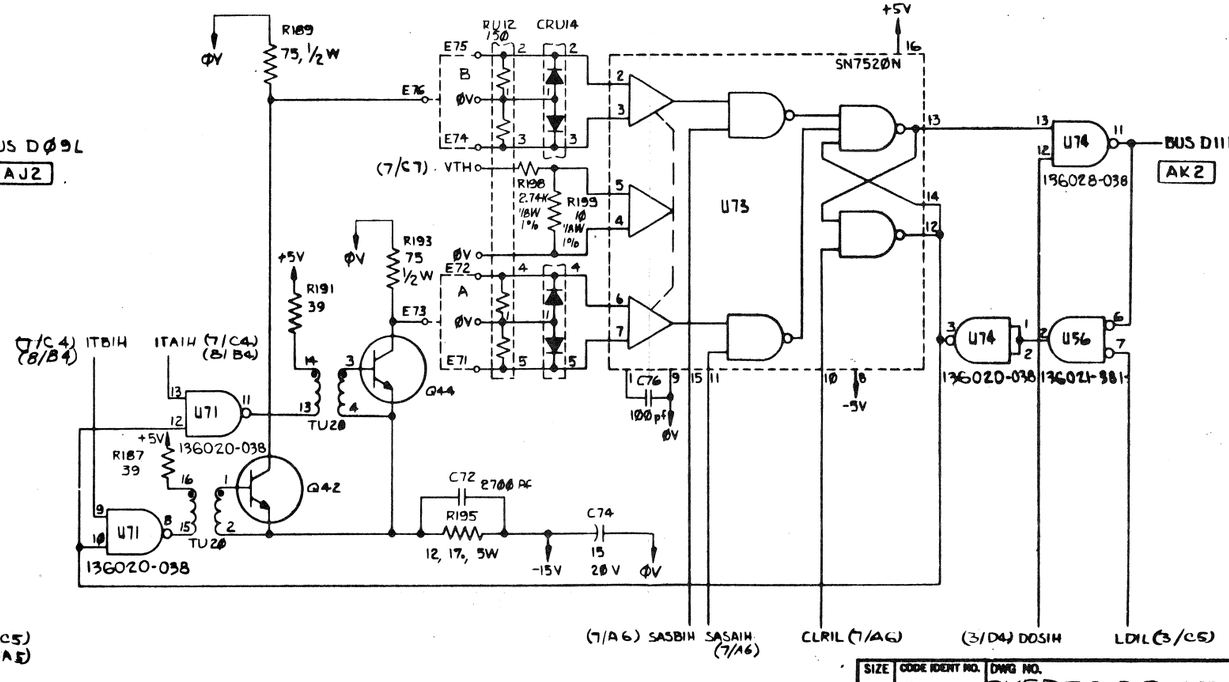
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | | SEE SHEET ONE | | |



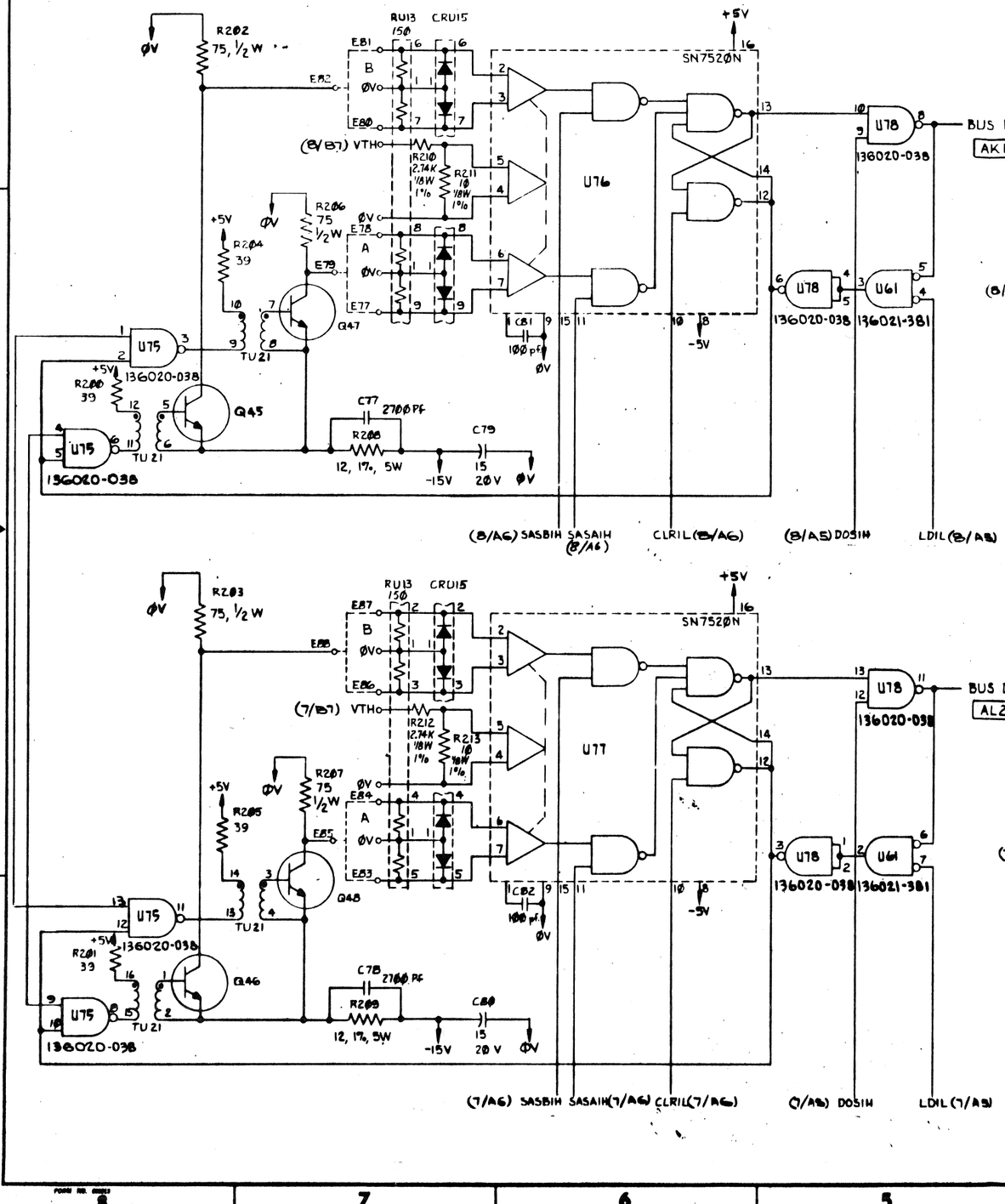



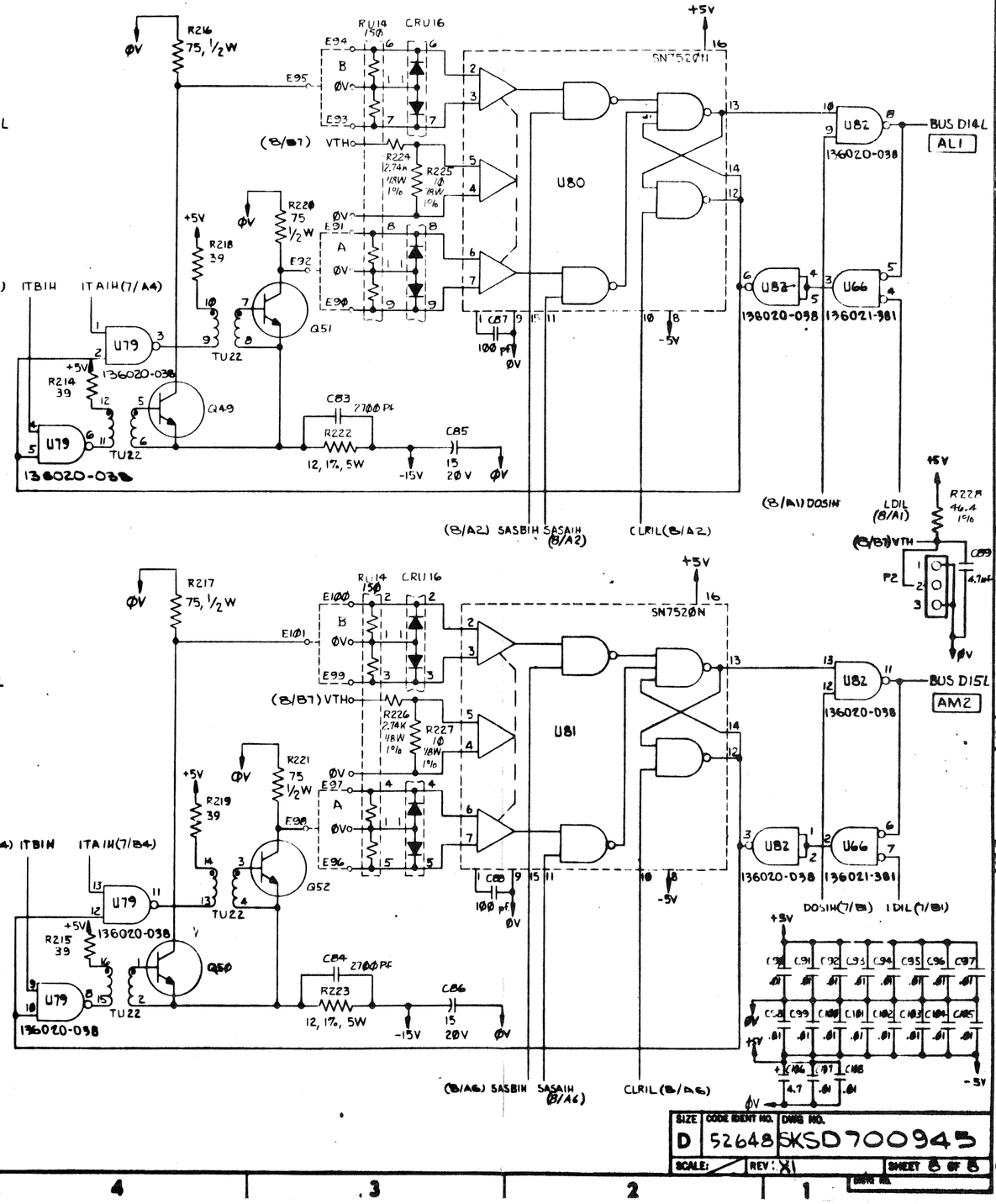




| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| D | 52648 | SKSD700945 |
| SCALE: | REV X1 | SHEET 7 OF 8 |

SKSD700945 X1

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | LTR | DESCRIPTION | DATE | APPROVED |
| | | SEE SHEET ONE | | |










| SIZE | CODE IDENT NO. | DWG NO. |
|---|---|---|
| D | 52648 | SKSD700945 |
| SCALE: | REV: X1 | SHEET 8 OF 8 |

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