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PDP-11/60 installation and operation manual

digital

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PDP-11/60
installation and
operation manual

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

It is the intent of this manual to:

- Detail installation information concerning unpacking, installing, and preparing the PDP-11/60 for normal operation.
- Familiarize users with the purpose and use of the PDP-11/60's hardware, including features, capabilities, and technical characteristics.
- Provide reference data required by operators and hands-on users.
- Describe the operating procedures, illustrating location of operator's controls and indicators.

1.2 SYSTEM DESCRIPTION

Figure 1-1 shows the basic P DP-11S60-XX double-width, low boy corporate cabinet, with the lower front panel removed. On the left is a BA11-P box, which houses the central processor; and, for models with MOS memory, the memory modules. On the right is the BA11-P which normally houses system-configured memory modules.

The PDP-11/60 is packaged in a variety of cabinet types [refer to the *PDP-11/60 Cabinet and Power Supply Manual* (EK-11060-PS-001) for specific configuration information], and may include either the RK05 or RK06 mass storage peripherals; an LA36 terminal is also included. A bootstrap loader and an octal display console are provided to facilitate operator control of the computer.

Figure 1-2 is a basic block diagram of the PDP-11/60.

1.2.1 Unibus

All components of the PDP-11/60 computer system, including peripheral devices, are connected to and communicate with each other by way of a single high-speed bus known as the Unibus. Addresses, data, and control information are sent along the 56 lines of the bus. A detailed description of the Unibus function in the PDP-11/60 can be found in the *PDP-11/60 Computer Manual* (EK-11060-TM-001) or the *PDP-11/60 Processor Handbook* (EB06498).

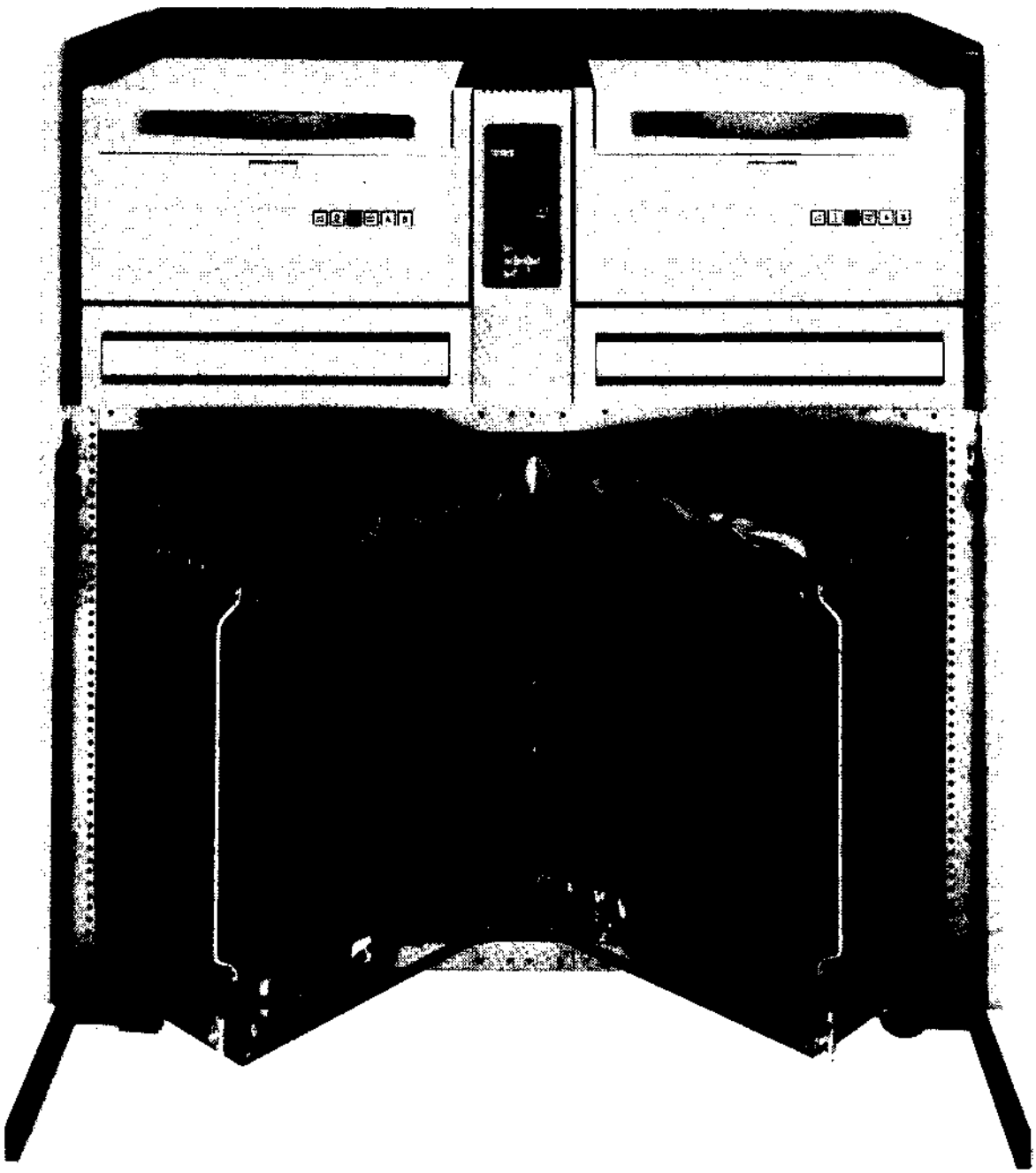

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Figure 1-1 PDP-11/60 Processor Card Cages

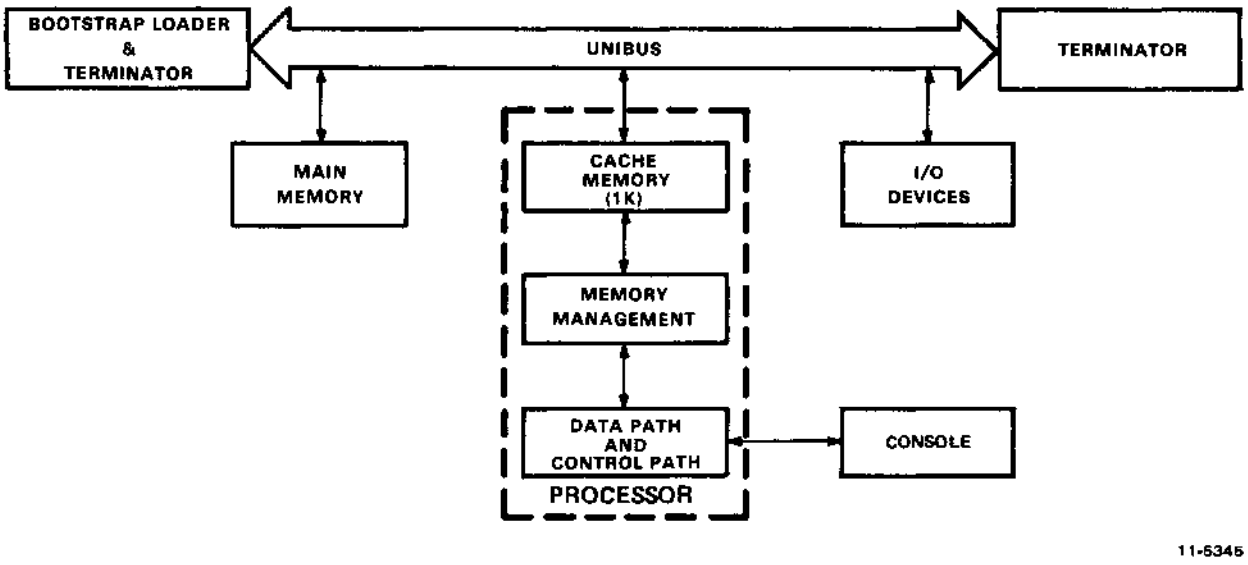

Figure 1-2 PDP-11/60 Basic System Block Diagram

1.2.2 KD11-K Central Processor

The PDP-11/60 central processor consists of six, hex-height logic modules (Figure 1-3). The processor is a functional unit connected to the Unibus that has the following features:

- Basic PDP-11/60 instruction set
- Internal EIS instructions
- Integral floating point instructions
- Cache memory
- Memory management unit
- Programmable stack limit
- Power fail/auto restart
- Four levels of priority interrupt
- Unibus compatibility
- Keypad/numeric display console
- Maintenance features

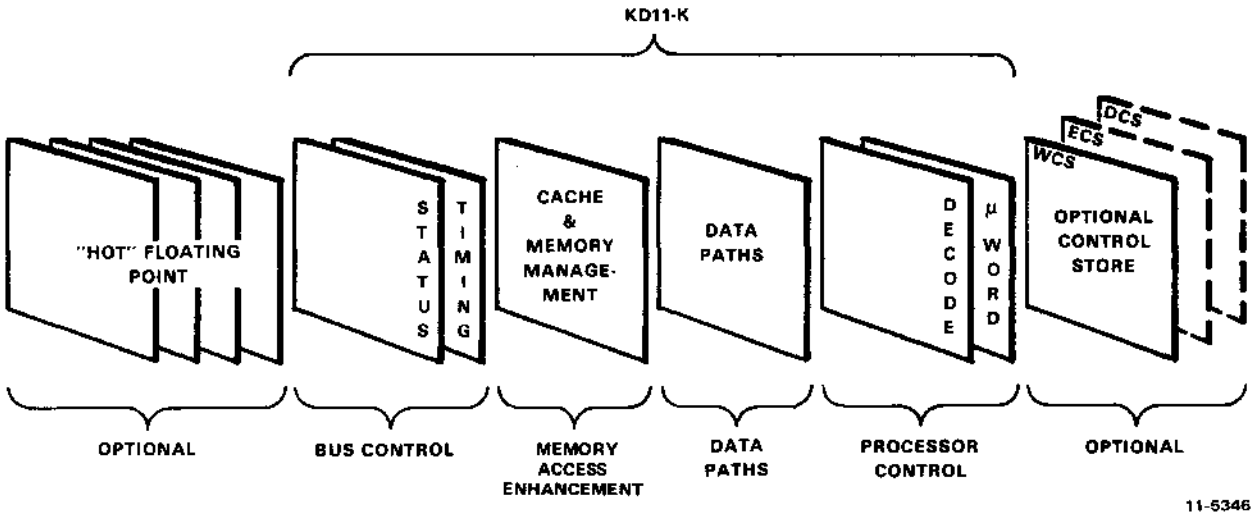

Figure 1-3 PDP-11/60 Processor Physical Partitioning

1.2.3 KY11-P Programmer's Console

The PDP-11/60 console (Figure 1-4) allows direct control of the computer system. It contains a power switch that is used as the master switch for the system. The console is used for starting, stopping, and debugging programs. Lights and switches provide the facilities for monitoring operation, system control, and maintenance. Operating descriptions of all console switches and indicators are provided in Chapter 3 of this manual.

The PDP-11/60 programmer's console provides the following facilities:

- Six-digit octal display for address and data indication.
- Processor state lights:

  RUN
  PROC (Processor)
  USER
  CONSOLE
  BATT (Battery)

- BOOT/RUN/HALT slide switch for power-up action.
- 5-position rotary switch for selection of machine status:

  STD BY
  POWER
  LOCK (Panel Lock)
  R1 (Remote 1)
  R2 (Remote 2)

- Keypad switches (four rows of five switches each, noted below)

  (D)ADRS (Display Address)
  7 (Numeric)
  EXAM (Examine)
  DEP (Deposit)
  HALT/SI (Halt/Single Instruction)
  (L)ADRS (Load Address)
  4 (Numeric)
  5 (Numeric)
  6 (Numeric)
  CONT (Continue)
  (D)SWR, (L)SWR (Display Switch Register, Load Switch Register)
  1 (Numeric)
  2 (Numeric)
  3 (Numeric)
  BOOT (Bootstrap)
  MAINT (Maintenance)
  0 (Numeric)
  DIAG (Diagnostic)
  CNTRL (Control)
  START

For a detailed functional description of the KY11-P programmer's console, refer to the *PDP-11/60 Computer Manual* or the *PDP-11/60 Processor Handbook*.

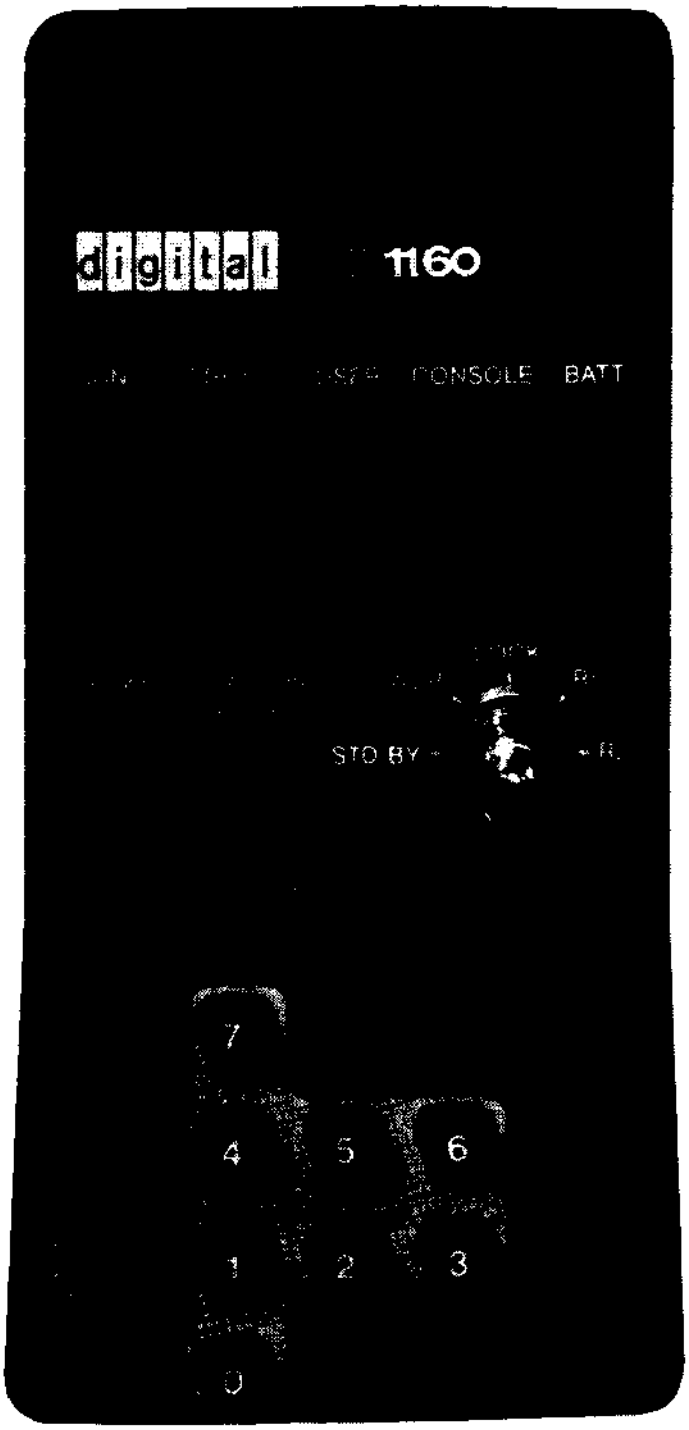

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Figure 1-4 PDP-11/60 Console

1.2.4 Memory

The memory system for the PDP-11/60 consists of a 2048 byte, high-speed, bipolar cache memory physically located within the processor, and up to 256K bytes of Unibus main memory, referred to as backing store.

1.2.4.1 Cache Memory – A cache memory is a small, high-speed memory that maintains a copy of previously selected portions of main memory for faster re-access to instructions and data. The cache memory is physically located within the processor and is both a part of the processor and part of the backing store as shown in Figure 1-5. Cache parameters are defined as follows.

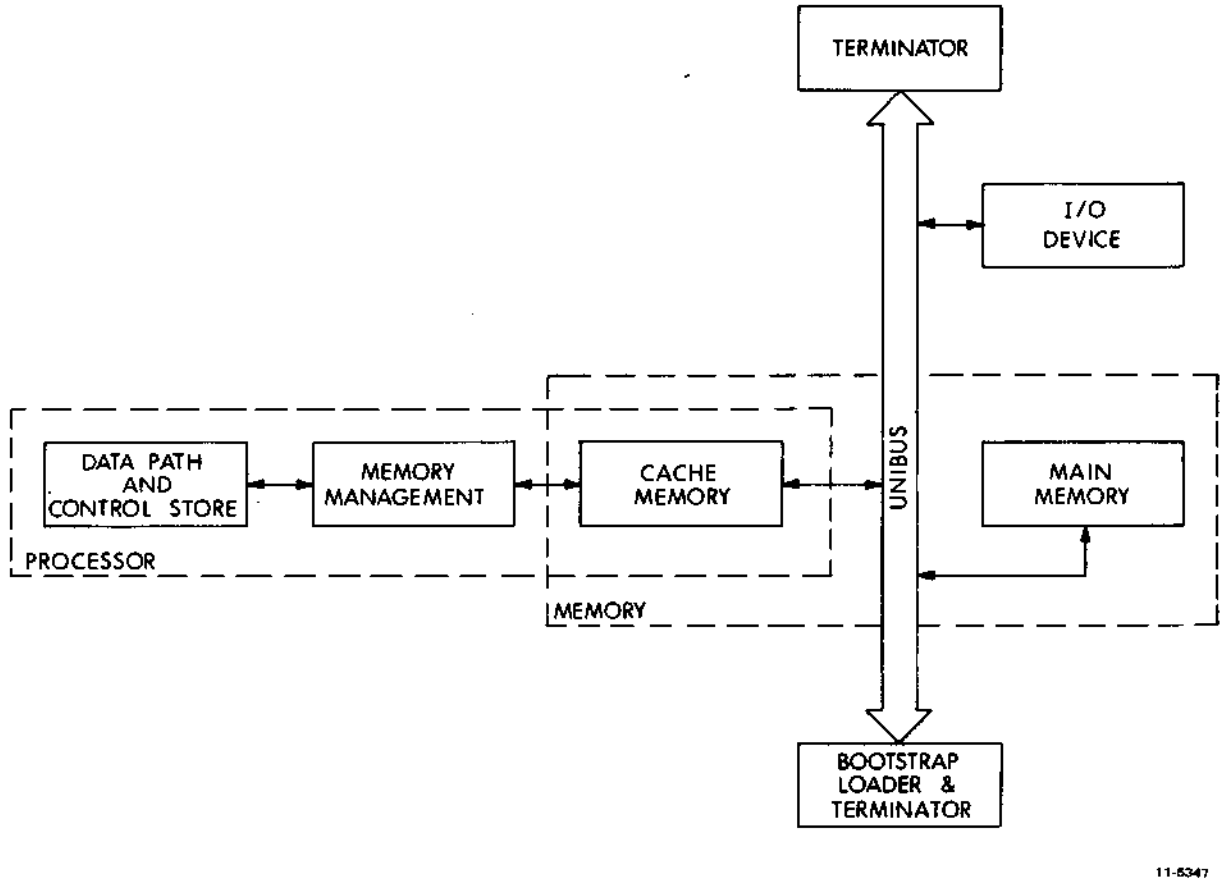


Figure 1-5 Cache Memory System Relationship

Direct mapping address mechanism. This type of mechanism allows each word from main memory only one possible location in cache and, consequently, requires only one address comparison as opposed to the fully associative cache, for example, which requires many address comparisons.

Block size. The PDP-11/60 has a block size of one, which means that every time a fetch to the backing store occurs, only one word is fetched. One word is allocated to cache in the event of a miss.

Set size. The PDP-11/60 has a set size of one, which means that there is one unique location in cache for any given word from backing store. Consequently, if a miss occurs, only one cache location is available for the data to be written into.

Write-through. Write-through is the PDP-11/60 method of handling stale data in main memory. In the write-through method, the data stored in cache is immediately copied into main memory; main memory always has a valid copy of all data.

1.2.4.2 Backing Store Memory – The PDP-11/60 uses Unibus memory and may be configured either for error-correcting MOS or for parity core memories in 64K byte increments. (Refer to the associated memory manual for detailed information.)

MOS Memory
The PDP-11/60 can be supplied with an MF11S-KF memory system. This memory system features single-bit error correction and double-bit error detection. It can be expanded to 128K words (256K bytes) in increments of 64K bytes. 256K bytes occupy two system units of mounting space. Memory addresses cannot be interleaved.

Core Memory
The PDP-11/60 can be supplied with an MF11-WP memory system. This parity memory can be expanded in 32K word (64K byte) increments to a full 256K byte backing store. Address interleave is standard for 128K and 256K byte sizes. 256K bytes occupy four system units of mounting space.

1.2.5 Terminators, Bootstrap Loader

1.2.5.1 M9302 Unibus Terminator – In addition to proper Unibus termination, this device contains logic to aid system throughput. Unheeded grants to peripherals are answered and it is not necessary for the processor to time out to continue system activity. The M9302 terminator is a double-height module (Figure 1-6) and must be installed at the end of the Unibus (furthest from the processor).

1.2.5.2 M9301-YH Bootstrap Loader/Self-Diagnostic/Terminator – The M9301-YH module (Figure 1-7), which is included with the PDP-11/60, provides three functions for the computer system.

1. It contains a read-only memory (ROM) that holds diagnostic routines for verifying computer operation.

2. It contains, also in a ROM, the several bootstrap loader programs for starting up the system.

3. It provides termination resistors for the Unibus.

Diagnostics
The M9301-YH contains diagnostics to check the processor, cache memory, and 28K of main memory in a GO/NO GO mode. This allows the user to detect the general area of a malfunction. Further localization of the malfunction involves examining certain associated registers. Execution of the diagnostics occurs automatically upon loading, but may be disabled by switches on the M9301-YH. It is also possible to inhibit only the memory modifying tests (cache or memory).

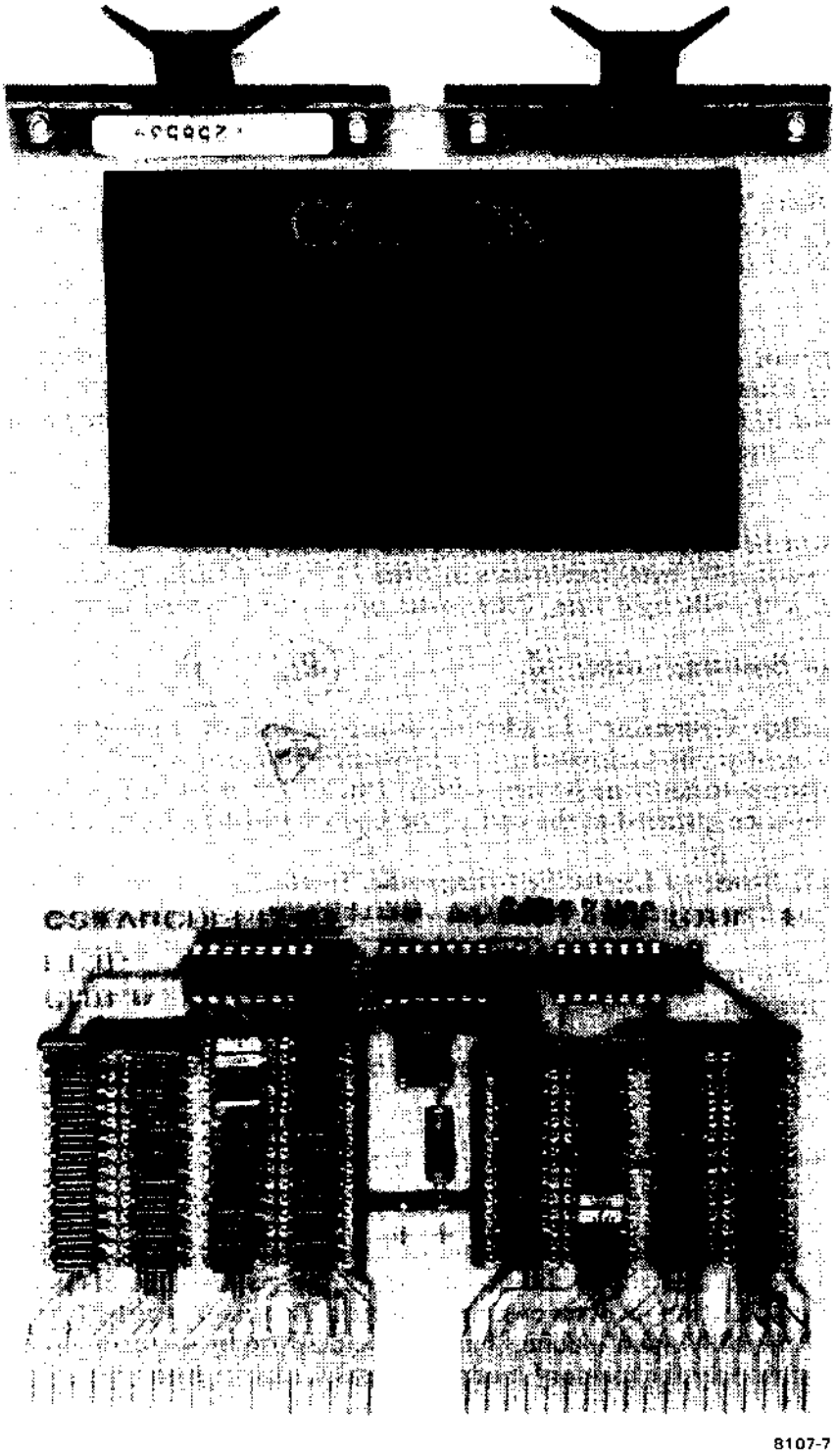


Figure 1-6 M9302 Terminator Module

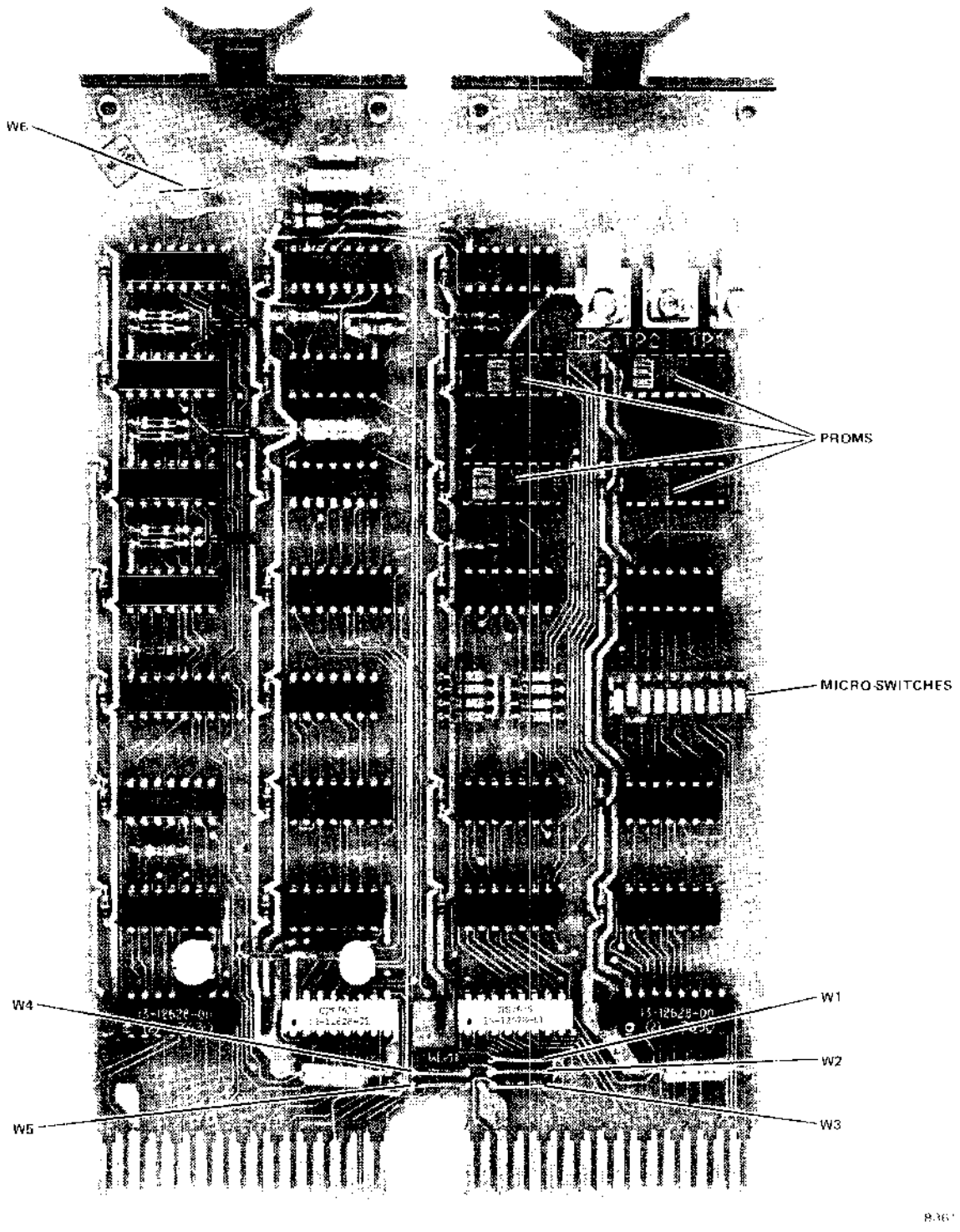


Figure 1-7 M9301-YH Bootstrap/Terminator Module

Bootstrap Loaders
The M9301-YH contains independent bootstrap programs that can bootstrap programs into memory from a selected peripheral device. Through front panel control (CONTROL and BOOT switches pressed simultaneously) or following power-up, the computer can directly execute a bootstrap, without the operator having to manually key in the initial program. The bootstrap program for the peripheral device is determined by switches on the M9301-YH. This is useful in remote applications where no operator is present. For switch settings, refer to Chapter 2, Paragraph 2.5.2.

The inclusion of a bootstrap loader in non-destructible ROM is an important convenience in system operation. Bootstrap programs do not have to be loaded manually into the computer for system initialization. If the device that is normally booted is down, the user can boot from any other device via the console.

The M9301-YH bootstrap loader supports the following devices:

- RK06 dual-access drive.
- RK05 disk drive
- RH11/RP04, RP05, RP06 Massbus controller/disk drive
- RX01 floppy disk drive
- RS04 fixed-head disk drive
- PC11 high-speed reader and punch
- TU10 tape transport
- TU16 magtape transport
- TU56 dual DECtape transport
- RP03 moving head disk

1.2.6 Cabinet Configurations, Backplane, and Power Supply

1.2.6.1 Cabinet Configuration – At the system level, the computer components, with the logic interface for disk controllers, are arranged as noted in Figures 1-8 through 1-15. Expansion space available for the standard PDP-11/60 cabinet configurations is shown in Figures 1-8 through 1-15. For detailed configuration information on the PDP-11/60, refer to the *PDP-11/60 Cabinet and Power Supply Manual*, Document No. EK-11060-SV-XXX, and Table 2-1 of this manual.

1.2.6.2 Backplane – Figure 1-16 shows the layout of the KD11-K processor backplane. Additional space is provided for single module Unibus interfaces. One such space is used for the serial line interface (DL11-W) that connects to the console terminal. Refer to Chapter 4 for additional information on PDP-11/60 backplanes.

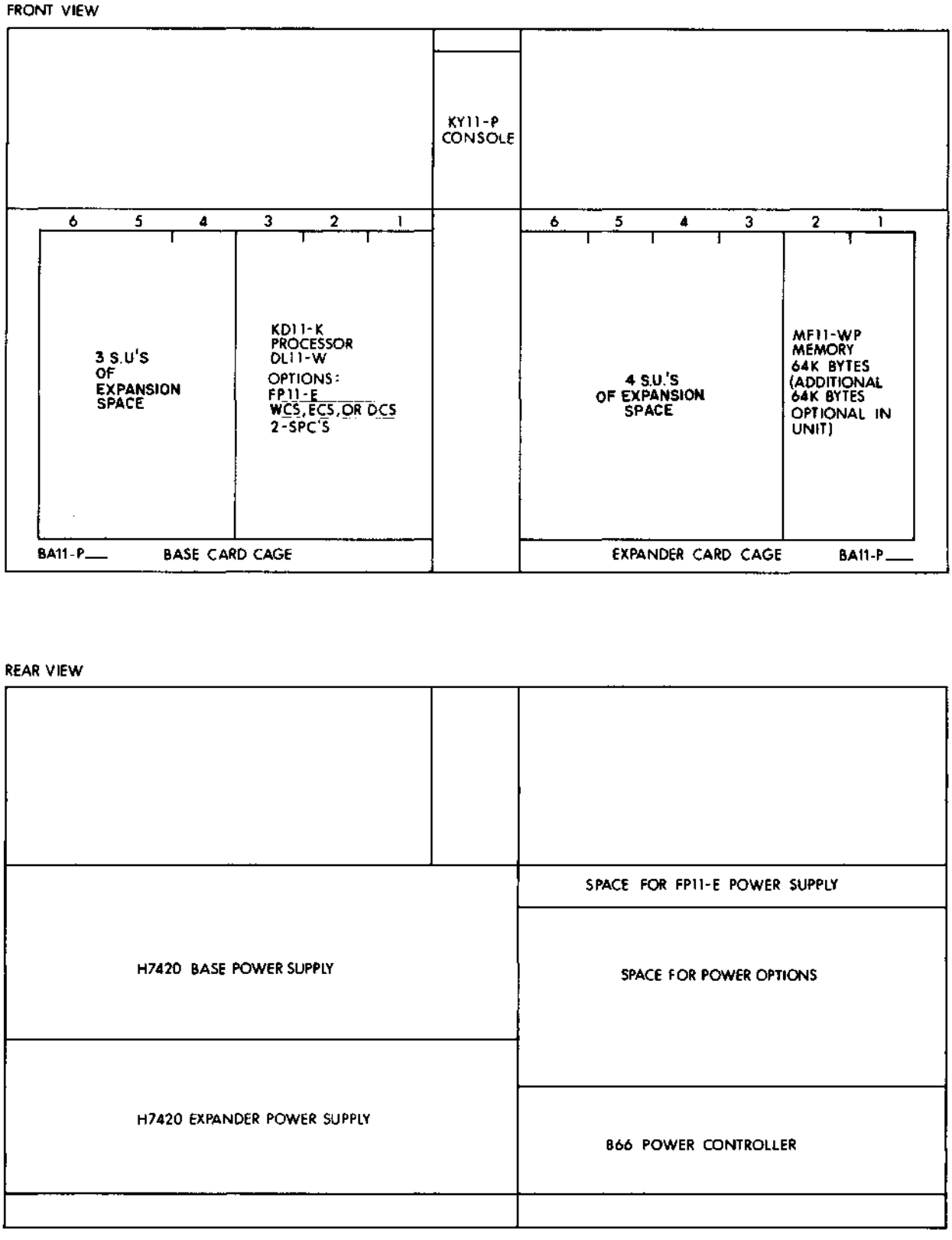


Figure 1-8 PDP-11X60-B Standard Cabinet Configuration

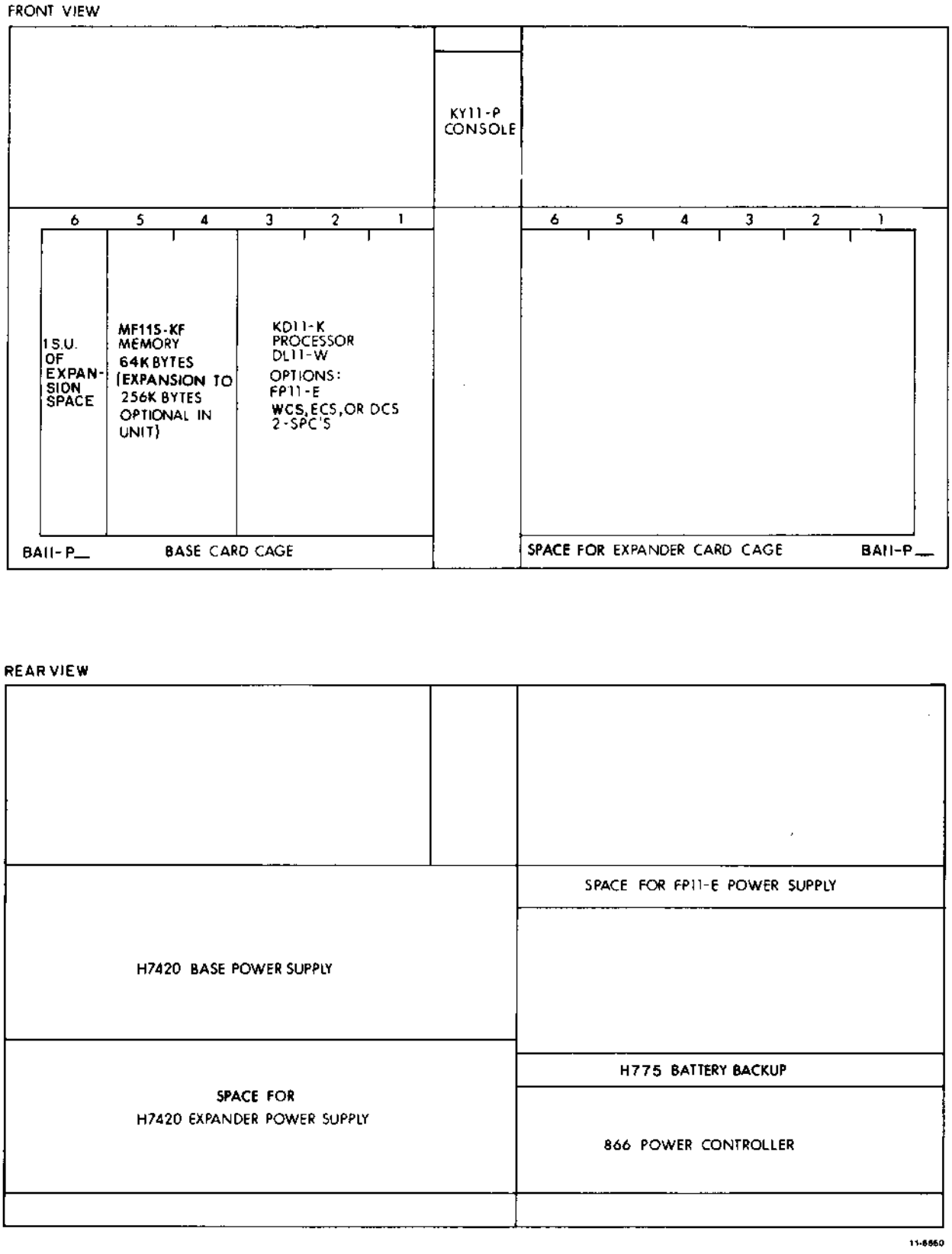


Figure 1-9 PDP-11X60-C Standard Cabinet Configuration

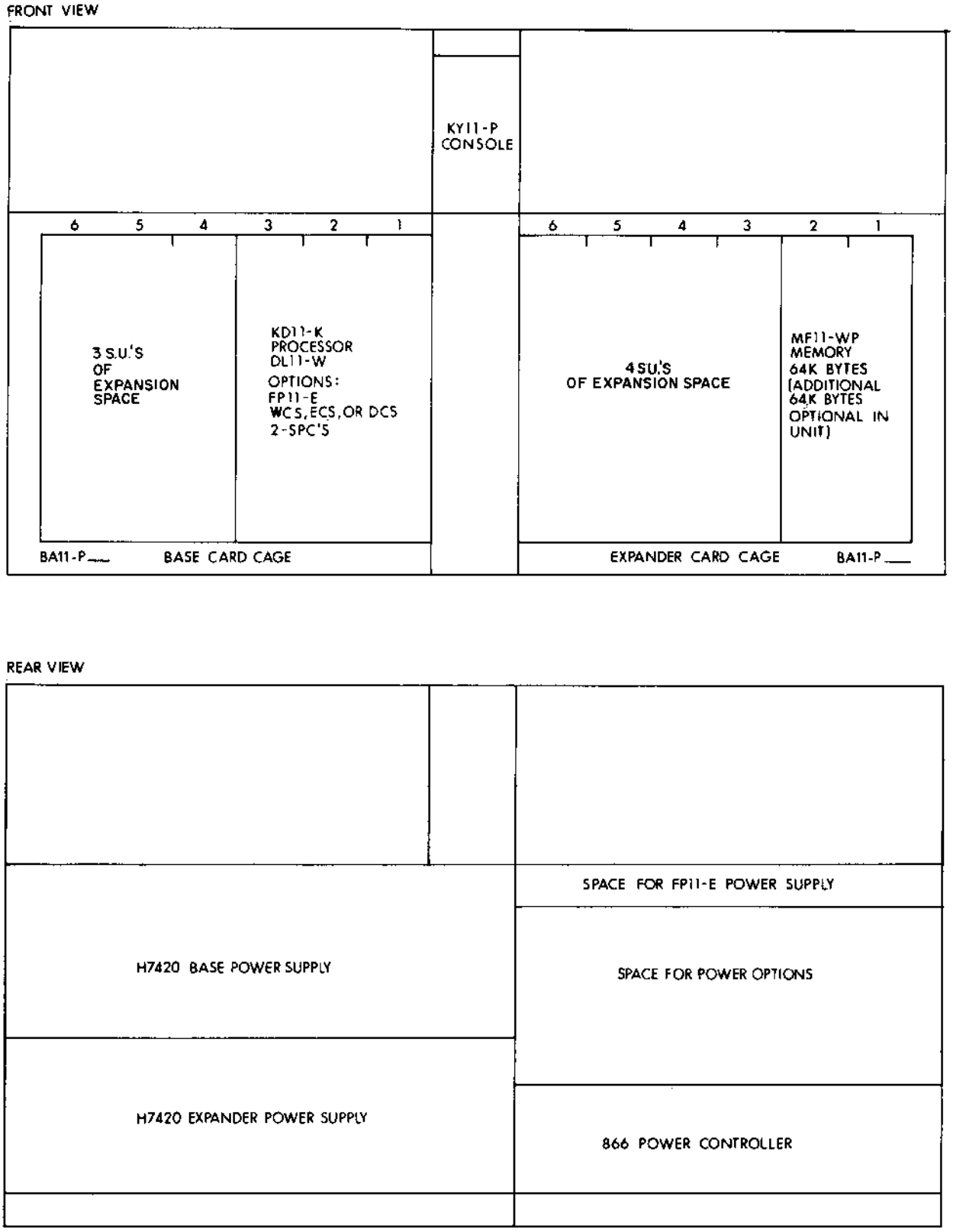


Figure 1-10 PDP-11Y60-B Standard Cabinet Configuration

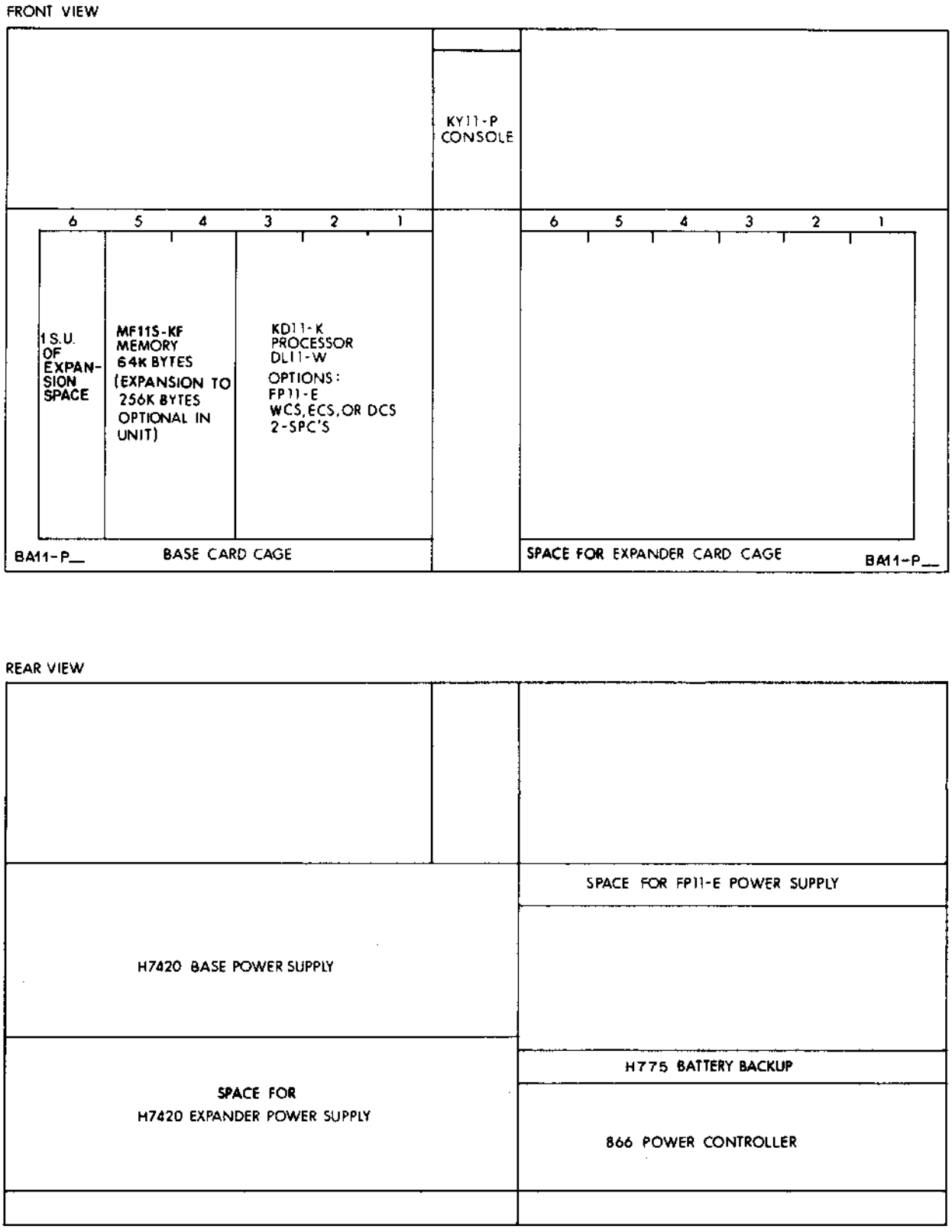


Figure 1-11 PDP-11Y60-C Standard Cabinet Configuration

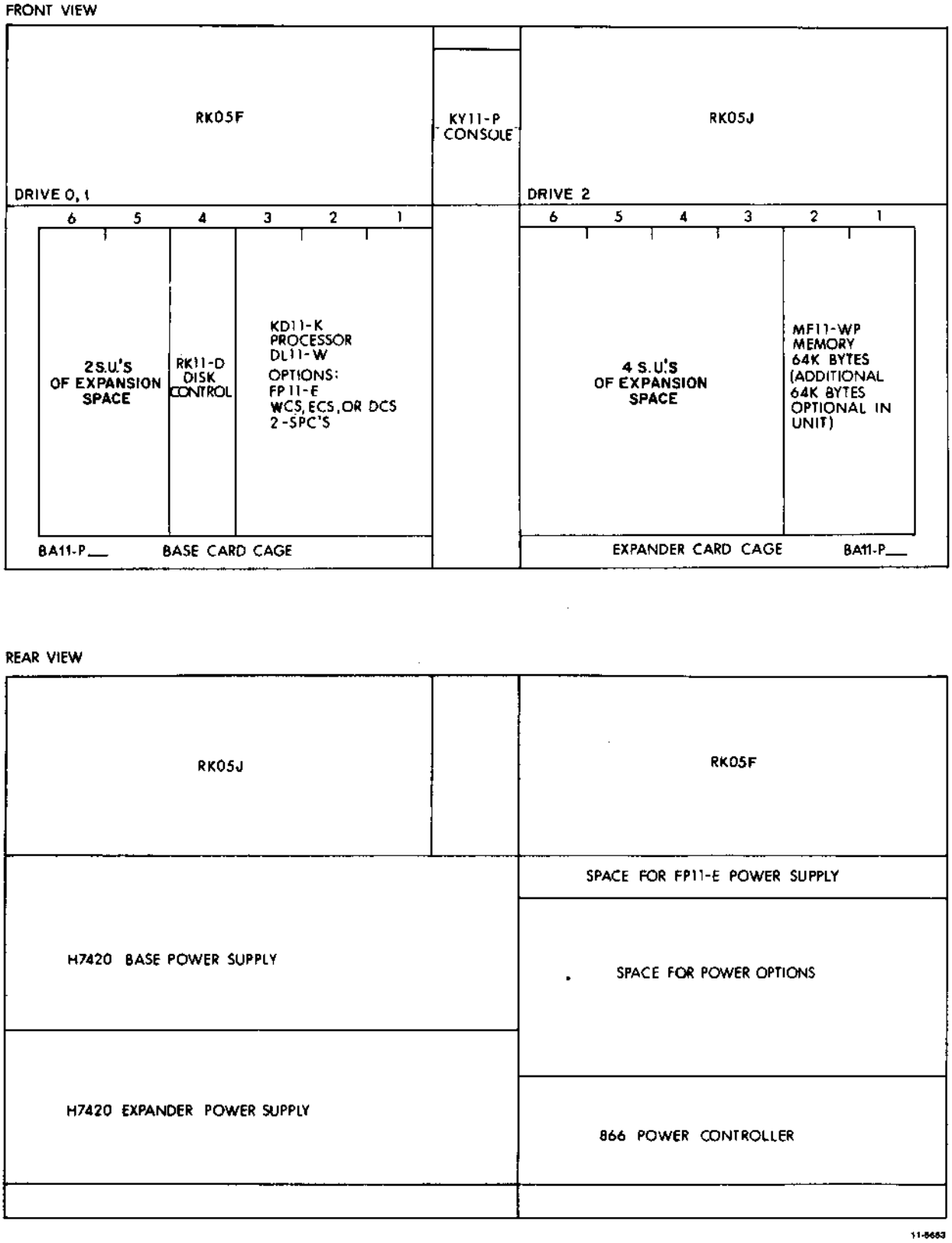


Figure 1-12 PDP-11T60-B Standard Cabinet Configuration

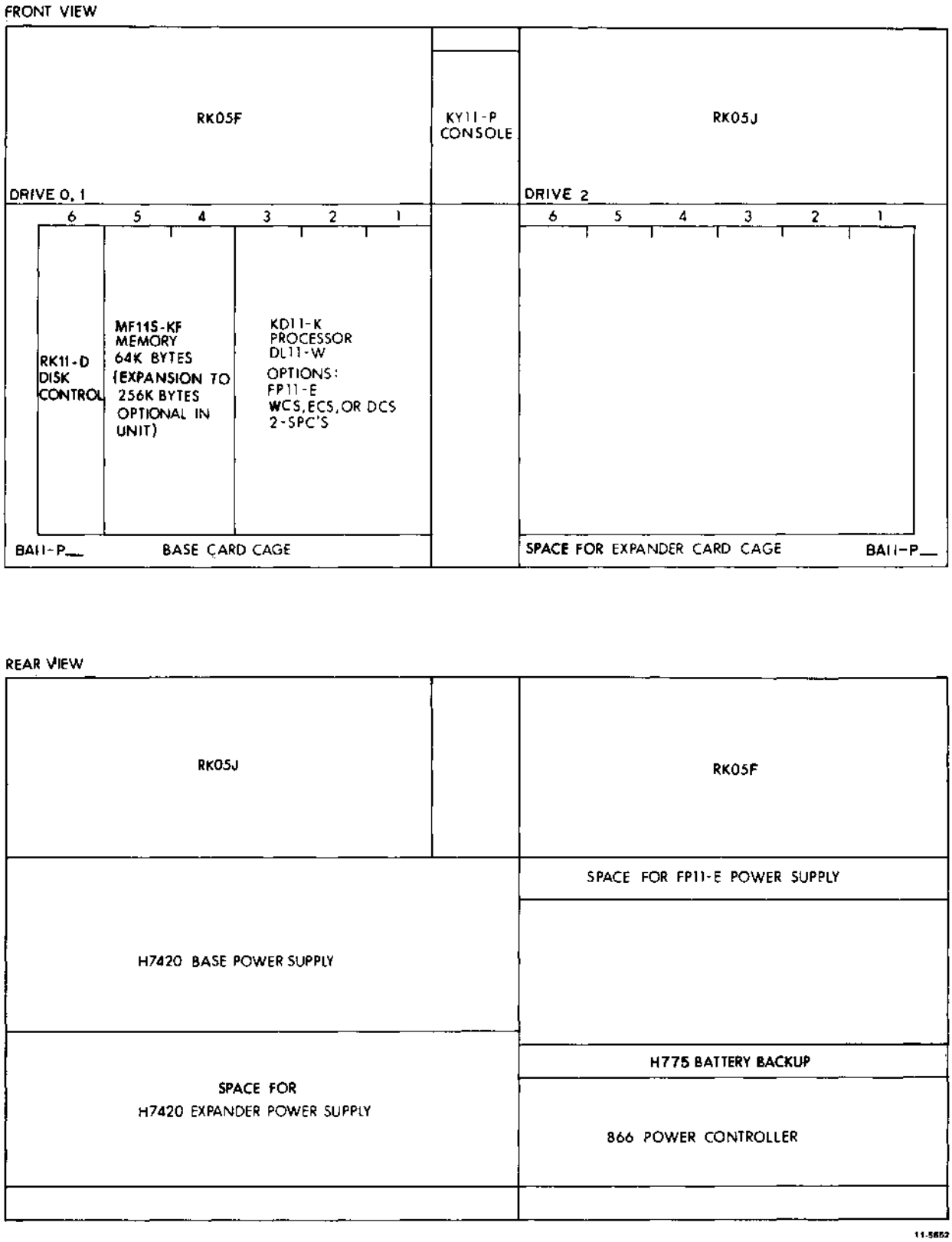


Figure 1-13 PDP-11T60-C Standard Cabinet Configuration

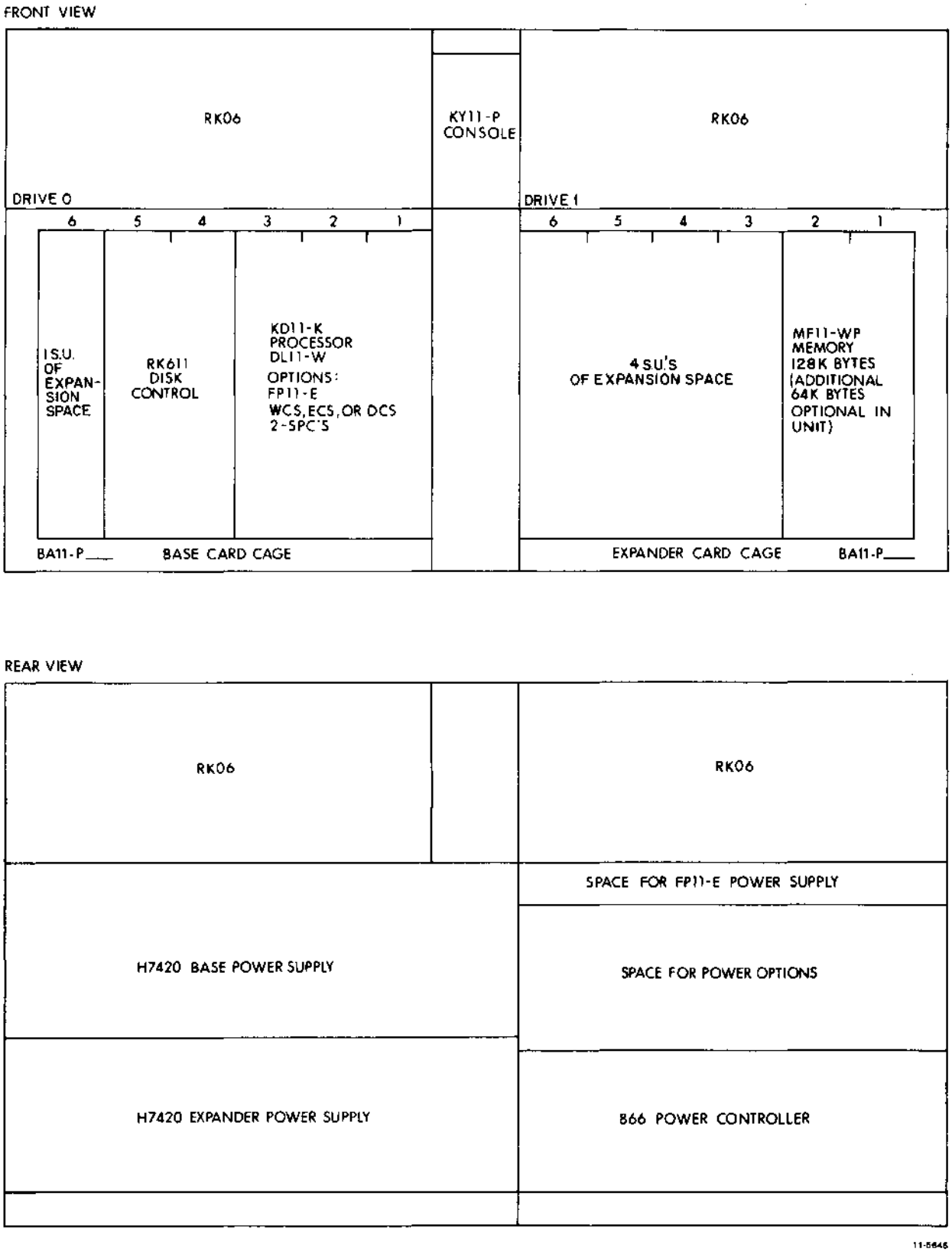


Figure 1-14 PDP-11S60-B Standard Cabinet Configuration

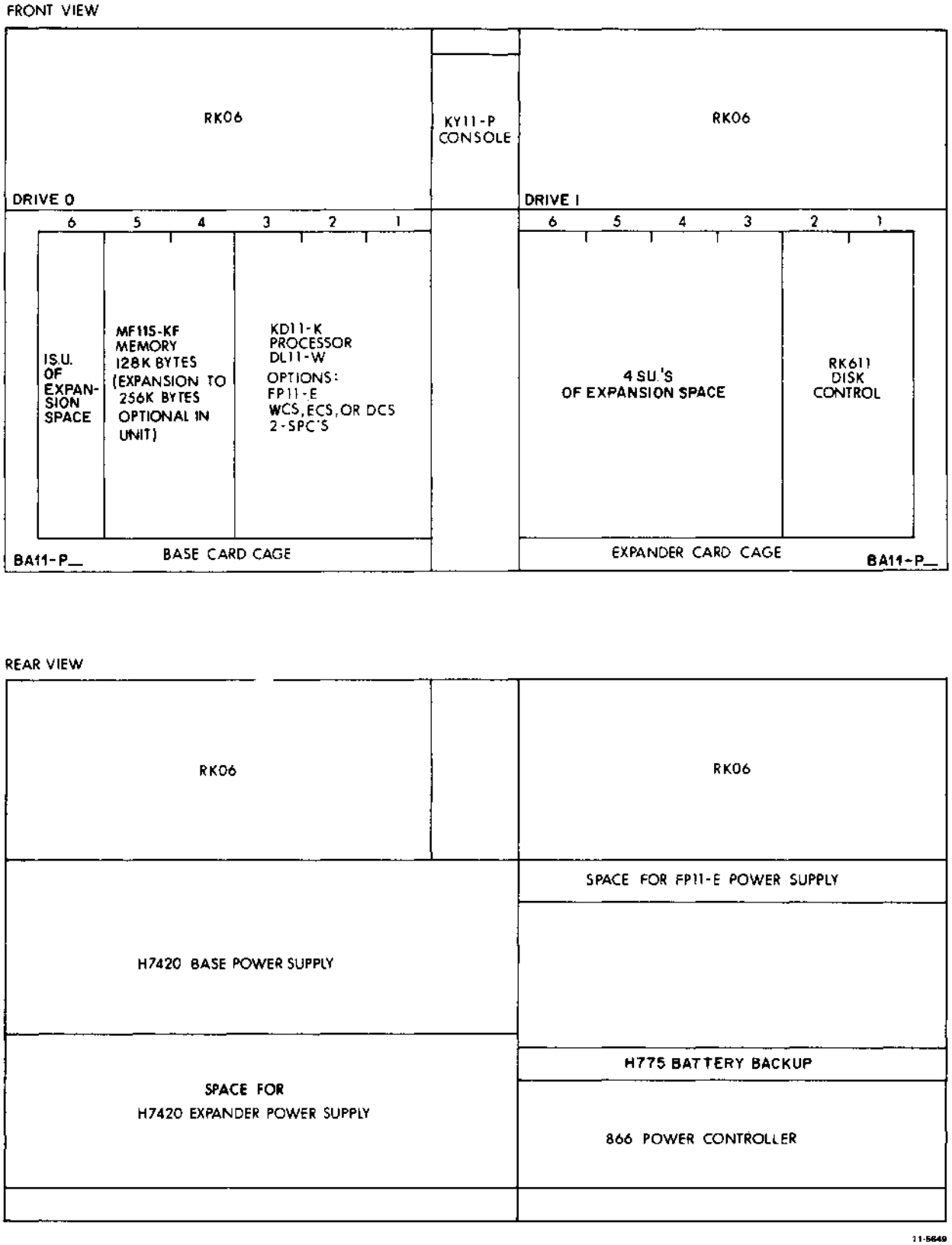


Figure 1-15 PDP-11S60-C Standard Cabinet Configuration

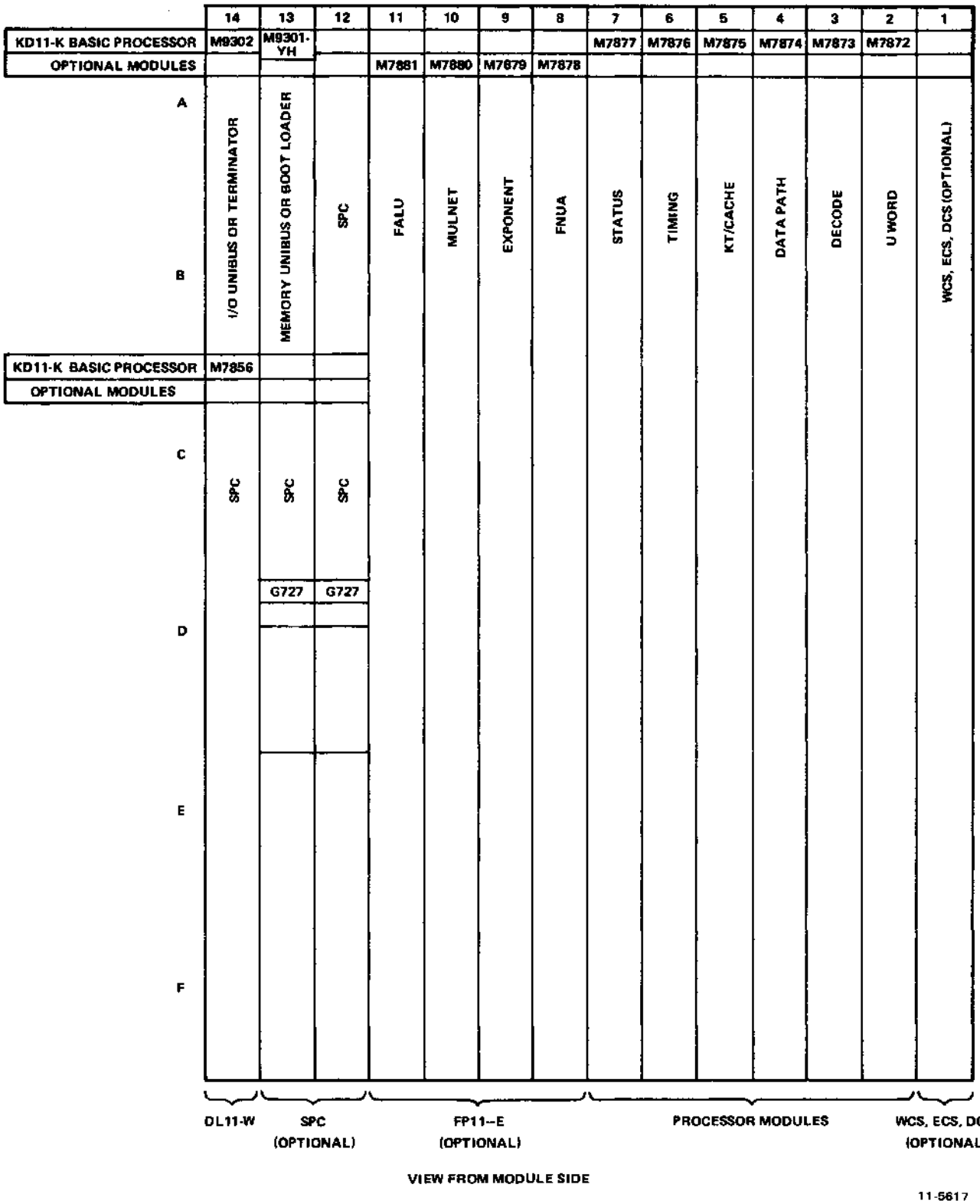


Figure 1-16 PDP-11/60 Processor Backplane

1.2.6.3 Power Supply – AC Power – The 866 power controller is used to control and distribute ac voltage to the power supplies, fans, and other electrical devices that require ac inputs within the system. The 866-D is used with 120 Vac, 3-phase lines. For a detailed description of the 866 power controller, refer to the *PDP-11/60 Cabinet and Power Supply Manual*, Document No. EK-11060-SV.

DC Power – The PDP-11/60 systems utilize one or two H7420 power supplies. Different regulators within these power supplies provide a variety of dc voltages. Table 1-1 shows the voltage distribution.

Table 1-1 PDP-11/60 Voltage Distribution

H7420A Base Power Supply (Upper)					
H754 or H7850 (REG E)	**H781 (REG D)**	**H7440 (REG C)**	**H7440 (REG B)**	**H7440 (REG A)**	**H7420 Supply**
H754 +20 V@8 A –5 V@3 A **H7850** +5 V@4A +12 V@2 A –12 V@0.2 A	+5 V@18 A +15 V@3 A	+5 V@25 A	+5 V@25 A	+5 V@25 A	–15 V@4 A
To SU 4,5,6	Line clock (50/60 Hz) +15 V To slots 12,13,14 and SU 4,5,6 +5 V To slots 6,7,12, 13,14, Console	To SU 4,5,6	To slots 3,4,5	To slots 1,2	To slots 12,13,14 and SU 4,5,6 ac low dc low

Table 1-1 PDP-11/60 Voltage Distribution (Cont)

H7420A Expander Power Supply (Lower)				
H754 (REG L)	**H781 (REG K)**	**H7440 (REG J)**	**H7440 (REG H)**	**H7420 Supply**
+20 V@8 A - 5 V@3 A	+5 V@15 A +15 V@4 A	+5 V@25 A	+5 V@25 A	-15 V@4 A
To all SU	Line Clock (50/60 Hz)	To SU 1.2	To SU 3,4	To all SU
	+15 V To all SU +5 V to SU 5,6			ac low dc low

1.2.7 DL11-W Serial Line Unit/Line Frequency Clock

The DL11-W serial line unit/line frequency clock provides both a line frequency clock and an asynchronous serial line interface. The line frequency clock allows interrupts at intervals of 16 ms or 20 ms determined by either a 60 Hz or 50 Hz line frequency.

The serial line interface converts serial data to parallel or parallel data to serial to provide communication between the PDP-11/60 and an asynchronous serial line, which is connected to a terminal device. The serial line interface has two modes of operation: current loop mode (standard on PDP-11/60) and EIA.

1.2.8 RK05J/RK05F, RK06 Mass Storage Devices

1.2.8.1 RK05J/RK05F – The RK05J and the RK05F disk drives are essentially identical, except that the RK05F has twice the capacity and has a non-removable medium. The RK05F has been designed to appear to the RK11 disk controller as two "logical" RK05J drives, a feature that permits RK05J and RK05F disk drives to be mixed on the same controller. The RK11-D controller is utilized in the PDP-11/60 system.

1.2.8.2 RK06 – The RK06 disk drive is a high performance, medium capacity, mass storage device. The disk cartridge has two platters and four recording surfaces, three surfaces for recording and one for servo control and tracking information. The PDP-11/60 system uses the RK06 disks, controlled by the RK611 disk controller. A summary of specifications for each of the disk subsystems is provided in Chapter 2 of this manual. For a detailed description of the disk subsystems, refer to the appropriate technical manual.

1.2.9 Optional Equipment

The following options can be incorporated to expand system capabilities and meet specific user requirements.

1.2.9.1 FP11-E High-Speed Floating Point Processor – The FP11-E floating point processor is an optional, asynchronous, parallel processor capable of performing high-speed arithmetic calculations. The FP11-E is logically contained on four hex modules that fit into the processor backplane (Figure 1-13). A separate power supply (H7421A) is also supplied with the unit. The FP11-E provides 17 digits of decimal accuracy, does 32-bit single-precision or 64-bit double-precision arithmetic, and contains six 64-bit accumulators.

1.2.9.2 Control Store Options – The writeable control store (KU116-AA) provides a read and modify expansion of 1024 microwords and is suitable for microprogram development and local store.

The extended control store (KU116-AB) is a vehicle for developed customer or DIGITAL applications in nonalterable programmable read only memory (PROM).

The diagnostic control store (KU116-BB) allows the application of microcontrol for diagnostic use within the processor. All of these options are discussed in detail under separate cover.

1.2.9.3 Standard PDP-11 Peripherals – The I/O capabilities of the PDP-11/60 system can be expanded through the implementation of standard PDP-11 peripheral devices. PDP-11 devices include:

- Floppy disk, RX01
- VT52 DECterminal II alphanumeric display
- Tape Drive, TS03
- Tape Transports, TU10, TU16, TU45
- Dispack drive and control units, RJP04, RJP05, and RJP06
- Disk drive with removable cartridge, RK05J
- Disk drive with nonremovable cartridge, RK05F
- Disk drive with removable cartridge, RK06
- High-speed line printers, LA180, LP11, LV11
- Card Readers, CR11, CD11, CM11
- Graphics terminal, GT40
- Synchronous and asynchronous single and multichannel communications interfaces
- DMC-11 microprocessor

1.3 RELATED DOCUMENTS

For detailed information concerning each of the system components, refer to the following documents.

Title	Document Number	Notes
PDP-11/60 Processor Handbook	EB-0649877	Not in Microfiche Library
PDP-11 Peripherals Handbook	EP-PDP11-HB	Not in Microfiche Library
PDP-11/60 Computer Manual	Under Development (EK-11060-TM001)	In Microfiche Library. Available on hard copy.
DL11-W Maintenance Manual	EK-DL11W-MM	In Microfiche Library. Available on hard copy.

Title	Document Number	Notes
M9301 Bootstrap Terminator Maintenance Manual	EK-M9301-MM	In Microfiche Library. Available on hard copy.
PDP-11/60 Cabinet and Power Supply Manual	Under Development (EK-11060-SV)	In Microfiche Library. Available on hard copy.
PDP-11 Family Field Installation and Acceptance Procedure Manual	EK-FS003-1N	Not in Microfiche Library. Hard copy ships with device.
MF11-WP Core Memory Manual	EK-MF11W-MM	In Microfiche Library. Available on hard copy.
MF11S-KF MOS Memory Manual	Under Development (EK-MF11K-TD)	In Microfiche Library. Available on hard copy.
LA36 DECwriter Maintenance Manual	EK-LA36-MM	In Microfiche Library. Available on hard copy.
RK611 Disk Controller Technical Manual	EK-RK611-TD	In Microfiche Library. Available on hard copy.
RK06 Cartridge Disk Drive Technical Manual	EK-RK06-TD	In Microfiche Library. Available on hard copy.
KU116-BB Diagnostic Control Store Manual	EK-M7871-TM	In Microfiche Library. Available on hard copy.

CHAPTER 2
INSTALLATION

2.1 GENERAL

This chapter contains installation information and recommendations to ensure a successful PDP-11/60 installation. Installation of new options in an existing PDP-11/60 system is also described in this chapter.

Customer assistance is provided during site planning, preparation, and installation; the final layout plan should be approved by both the customer and DIGITAL prior to equipment delivery.

Planning considerations should include:

- Shipping and access routes, e.g., door, hall, passageway, elevator restrictions, etc.
- Floor plan layout for equipment.
- Electrical and environmental considerations.
- Fire and safety precautions.
- Storage facilities for accessories and supplies.

Site preparation is dictated by the customer's requirements and can range from providing the required source power to complete construction or remodeling of the selected installation site. Therefore, it is recommended that any and all requirements and restrictions be considered and effected prior to shipment and installation of the equipment.

2.2 SITE PREPARATION

Adequate site planning and preparation simplifies the installation process. DIGITAL sales and field service engineers are available for consultation and planning with customer representatives regarding objectives, course of action, and progress of the installation. The information in this paragraph is provided primarily to permit review of the site planning; use the site configuration worksheet to perform initial site planning.

For more detailed information, refer to the XXX Site Preparation and Planning Guide (where "XXX" stands for a product line, e.g., TELCO, IPG, DECCOM).

2.2.1 Physical Dimensions

The overall dimensions and total weight of a particular system – the dimensions, weight of any optional cabinets, cable lengths, and the number of free-standing peripherals – should be known prior to shipment (refer to Paragraph 2.3).

The route the equipment is to travel from the customer receiving area to the installation site should be studied; measurements of doors, passageways, etc., should be taken to facilitate equipment delivery. All measurements and floor plans should be submitted to the DIGITAL sales engineer and field service to ensure that the equipment is packed to suit the installation site facilities. Any restrictions (such as bends or obstructions in hallways, etc.) should be reported to DIGITAL.

If an elevator is to be used to transfer the PDP-11/60 and its related equipment to the installation site, DIGITAL should be notified of the size and gross weight limitations of the elevator so that the equipment can be shipped accordingly.

The site space requirements are determined by the specific system configuration to be installed and, when applicable, provisions should be made for future expansion. To determine the exact area required for a specific configuration, a machine-room floor plan layout is helpful. When applicable, space should be provided in the machine room for storing tape reels, printer forms, card files, etc. The integration of the work area with the storage area should be considered in relation to the work flow requirements between these areas.

In large installations where test equipment is maintained, DIGITAL recommends that the test equipment storage area be within or adjacent to the machine room.

Operational requirements determine the specific location of the various options and free-standing peripherals of the system. Dimensions, weights, and cable lengths of free-standing peripheral equipment must be known prior to installation – preferably during site preparation and planning. The computer peripherals must not be located at distances where connecting cables exceed maximum limits. The following points should be considered when planning the system layout:

1. Ease of visual observation of I/O devices by operating personnel.

2. Adequate work area for installing tapes, access to console, etc.

3. Space availability for contemplated future expansion.

4. Proximity of the cabinets and peripherals to any humidity-controlling or air-conditioning equipment.

5. Adequate access to equipment (e.g., rear door, etc.) for service personnel.

The final layout will be reviewed by the DIGITAL sales engineer, field service, and in-house engineering personnel to ensure that cable limitations have not been exceeded and that proper clearances have been maintained.

2.2.2 Fire and Safety Precautions

The following fire and safety precautions are presented to aid the customer in maintaining an installation that affords adequate operational safeguards for personnel and system components.

1. If an overhead sprinkler system is used, a dry pipe system is recommended. Upon detection of a fire, this system removes source power to the room and then opens a master valve to fill the room's overhead sprinklers.

2. If the fire detection system is the type that shuts off the power to the installation, a battery-operated emergency light source should be provided.

3. If an automatic carbon dioxide fire protection system is used, an alarm should sound prior to release of the CO_2 to warn personnel in the installation area.

4. If power connections are made beneath the floor of a raised floor installation, waterproof electrical receptacles and connections should be used.

5. An earth ground connection should be provided to protect operating personnel.

To ensure personnel and product safety, consider the following precautions:

1. Observe the caution symbolism on the cabinet containers.

2. If the cabinets are moved up ramps, additional precautions may be necessary if the tilt angle of 10 degrees is exceeded.

3. Refrain from excessively shocking or carelessly handling the cabinets.

4. When moving the cabinets, they should be pushed on the side indicated by the caution symbols, because the casters are locked (Paragraph 2.4.1.3) to facilitate movement in the direction indicated.

2.2.3 Environmental Requirements

An ideal computer room environment has an air distribution system that provides cool, well-filtered, humidified air. The room air pressure should be kept higher than that of adjacent areas to prevent dust infiltration.

2.2.3.1 Humidity and Temperature – The PDP-11/60 specifications are listed in Paragraph 2.3.

2.2.3.2 Air-Conditioning – When used, computer room air-conditioning equipment should conform to the requirements of the *Standard for the Installation of Air-Conditioning and Ventilating Systems (Non-Residential)*, NFPA No. 90A, as well as the requirements of the *Standard for Electronic Computer Systems* , NFPA No. 75.

2.2.3.3 Acoustical Damping – Some peripheral devices (such as line printers and magnetic tape transports) are quite noisy. In installations that use a group of high noise level devices, an acoustically damped ceiling will reduce the noise.

2.2.3.4 Lighting – If CRT peripheral devices are part of the system, the illumination surrounding these peripherals should be reduced to enable the operator to observe the display conveniently.

2.2.3.5 Special Mounting Conditions – If the system will be subjected to rolling, pitching, or vibration of the mounting surface (e.g., aboard ship), the cabinetry should be anchored securely to the installation floor by mounting bolts. Such installations require modifications to the cabinet; arrangements for modifications of this type should be made through DIGITAL's Computer Special Systems Group.

2.2.3.6 Static Electricity – Static electricity can be an annoyance to operating personnel and may affect the operational characteristics of the PDP-11/60 and related peripheral equipment. If carpeting is installed on the computer room floor it should be of a type designed to minimize the effects of static electricity. Flooring consisting of metal panels, or flooring with metal edges, should be adequately grounded.

2.2.4 Electrical Requirements

The PDP-11/60 operates from a nominal 3-phase, 120 V, 50/60 Hz wye configuration or 3-phase, 240 V, 50/60 Hz, ac power source. The primary ac operational voltages should be maintained within the tolerances defined in Paragraph 2.3.

For certain options that use synchronous motors, line voltage tolerance should be maintained within ± 15 percent of the nominal values, and the 50/60 Hz line frequency should not vary more than ±2 Hz.

Primary power to the system should be provided on a line separate from lighting, air-conditioning, etc., so that computer operation will not be affected by voltage transients. The wiring should conform to the following general guidelines:

1. All electrical wiring must conform with the National Electric Code (NEC).

2. The ground terminal on the receptacle is normally a green screw; the neutral terminals are white or silver; the "hot" terminals are brass-colored.

3. Under the NEC (in the U.S. only), the color coding for the neutral wire is either white or gray, and the ground wire is solid green, green with one or more yellow stripes, or bare. There are no specified colors for the "hot" wires.

The PDP-11/60 cabinet grounding point should be connected to the building power transformer ground or the building ground point (Paragraph 2.4.3.1). Direct any questions regarding power requirements and installation wiring to the local DIGITAL sales engineer and/or field service.

2.2.5 Related Documents

The following documents contain information that may be of value during site preparation and planning operations:

1. Plant Engineering Handbook, William Staniar, McGraw-Hill

2. National Electrical Code, NFPA 70*

3. Protection of Electronic Computer/Data Processing Equipment, NFPA 75*

4. Installation of Air-Conditioning and Ventilation Systems (Non-residential), NFPA 90A*

5. Recommended Good Practice for the Maintenance and Use of Portable Fire Extinguishers, NFPA 10A*

6. Installation of Portable Fire Extinguishers, NFPA 10*

7. Lightning Protection Code, NFPA 78*

8. ASHRAE Handbook (American Society of Heating, Refrigeration, and Air-Conditioning Engineers)

9. Computer Talk, Vol. 1, No. 1, 3M Company

10. Computer Decisions, Vol. 2, No. 10

11. ANSI Standard X3.11, 1969

12. ISO Recommendation R 1681, 1970

13. U.L. Handbook No. 478 (Underwriters Laboratories, Inc.)

14. NBFU No. 70 (National Board of Fire Underwriters)

*NFPA standards and publications are available from the National Fire Protection Association, 60 Batterymarch Street, Boston, Massachusetts 02110.

15. EIA Standard RS-232C (Electronics Industries Association)

16. Digital Supplies Catalog (Digital Equipment Corporation)

17. IEEE Standard 142-1972

2.3 SPECIFICATIONS SUMMARY

Table 2-1 summarizes the electrical, mechanical, and environmental specifications of the PDP-11/60 system; and includes configuration information on all the models in the 11/60 family.

2.3.1 Unibus Interface

Specifications for the Unibus devices available to the PDP-11/60 are listed in Appendix A (to be supplied).

2.3.2 Packaging Variations

Because of the variations in the cabinets that are shipped (e.g., completely assembled, frames only, frames with one side panel, etc.), it is necessary for the user to review the available packaging variations and select the appropriate variation for the cabinet configuration(s). The following list gives the packaging variations. The user should review the Packaging Instructions, A-SP-3700241-0-0, for detailed information and/or contact the DIGITAL Commercial Packaging Group.

Packaging Variations

3700241-00	INSTR PKG CORP CAB SGL LB W/END PANELS
3700241-01	INSTR PKG CORP CAB SGL LB 1 FR END
3700241-02	INSTR PKG CORP CAB SGL LB 2 FR END
3700241-03	INSTR PKG CORP CAB SGL LB EXT W/END PANELS
3700241-04	INSTR PKG CORP CAB SGL LB EXT 1 FR END
3700241-05	INSTR PKG CORP CAB SGL LB EXT 2 FR END
3700241-06	INSTR PKG CORP CAB DBL LB W/END PANELS
3700241-07	INSTR PKG CORP CAB DBL LB 1 FR END
3700241-08	INSTR PKG CORP CAB DBL LB 2 FR END
3700241-09	INSTR PKG CORP CAB DBL LB EXT W/END PANELS
3700241-10	INSTR PKG CORP CAB DBL LB EXT 1 FR END
3700241-11	INSTR PKG CORP CAB DBL LB EXT 2 FR END
3700241-12	INSTR PKG CORP CAB SGL HB W/END PANELS
3700241-13	INSTR PKG CORP CAB SGL HB 1 FR END
3700241-14	INSTR PKG CORP CAB SGL HB 2 FR END
3700241-15	INSTR PKG CORP CAB SGL HB EXT W/END PANELS
3700241-16	INSTR PKG CORP CAB SGL HB EXT 1 FR END
3700241-17	INSTR PKG CORP CAB SGL HB EXT 2 FR END
3700241-18	INSTR PKG CORP CAB DBL HB W/END PANELS
3700241-19	INSTR PKG CORP CAB DBL HB 1 FR END
3700241-20	INSTR PKG CORP CAB DBL HB 2 FR END
3700241-21	INSTR PKG CORP CAB DBL HB EXT W/END PANELS
3700241-22	INSTR PKG CORP CAB DBL HB EXT 1 FR END
3700241-23	INSTR PKG CORP CAB DBL HB EXT 2 FR END

NOTES: SGL = Single Width
DBL = Double Width
LB = Low Boy
HB = High Boy
FR = Frame
EXT = Extended

Table 2-1 PDP-11/60 Configurations Data Sheet

Model	Description	Cabinet Style	Size (in/cm) H×W×D	Weight (lbs/kg)	Operating Temp (°C)	Relative Humid (%)	Line Volt/Freq	Logic Card Cages	Amps at +5 V Available	DC Power Supplies	Comments
11X60-BA	11/60W, MF11-WP, DL11-W, 866-D	DWLB	51X47X30 128X118X76	530/241	10 - 40	20 - 80	3 Phase 120 V, 60 Hz	BA11-PA BA11-PE	31.5 40	H7420A (7013050-0) H7420A (7013050-1)	7 S.U.s and 2 Quad SPC Expansion Space Available.
11X60-BB	11/60W, MF11-WP, DL11-W, 866-E	DWLB	51X47X30 128X118X76	530/241	10 - 40	20 - 80	3 Phase 240 V, 50 Hz	BA11-PB BA11-PF	31.5 40	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11X60-BA.
11X60-CA	11/60K, MF11S-KF, DL11-W, H775-BA, 866-D	DWLB	51X47X30 128X118X76	380/172	10 - 40	20 - 80	3 Phase 120 V, 60 Hz	BA11-PK	31.5	H7420A (7013050-8)	1 S.U. and 2 Quad SPC Expansion Space Available in Base Card Cage.
11X60-CB	11/60K, MF11S-KF, DL11-W, H775-BB, 866-E	DWLB	51X47X30 128X118X30	380/172	10 - 40	20 - 80	3 Phase 240 V, 50 Hz	BA11-PL	31.5	H7420B (7013050-10)	Expansion Space Identical to the 11X60-CA. Expander Cage not included.
11Y60-KA	11/60W, MF11-WP, DL11-W, 866-D	DWHB	61X47X30 154X118X76	529/254	10 - 40	20 - 80	3 Phase 120 V, 60 Hz	BA11-PA BA11-PE	31.5 40	H7420A (7013050-0) H7420A (7013050-0)	Expansion Space Identical to the 11X60-BA.
11Y60-KB	11/60W, MF11-WP, DL11-W, 866-E	DWHB	61X47X30 154X118X76	529/254	10 - 40	20 - 80	3 Phase 240 V, 50 Hz	BA11-PB BA11-PF	31.5 40	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11X60-BA.
11Y60-LA	11/60K, MF11-SK, DL11-W, H775-BA, 866-D	DWHB	61X47X30 154X118X76	409/186	10 - 40	20 - 80	3 Phase 120 V, 60 Hz	BA11-PK	31.5	H7420A (7013050-8)	Expansion Space Identical to the 11X60-CA. Expander Cage not included.
11Y60-LB	11/60K, MF11-SK, DL11-W, H775-BB, 866-E	DWHB	61X47X30 154X118X76	409/186	10 - 40	20 - 80	3 Phase 240 V, 50 Hz	BA11-PL	31.5	H7420B (7013050-10)	Expansion Space Identical to the 11X60-CA. Expander Cage not included.
11S60-BA	11/60W, MF11-WP, MM11-WP, DL11-W/LA36-CE, RK611, 2-RK06-AA 866-D	DWLB	51X47X30 128X118X76	930/423	10 - 40	20 - 80	3 Phase 120 V, 60 Hz	BA11-PA BA11-PE	16.5 40	H7420A (7013050-0)	5 S.U.s of Expansion Space Available.
11S60-BB	11/60W, MF11-WP, MM11-WP, DL11-W/LA36-CF, RK611, 2-RK06-AB, 866-E	DWLB	51X47X30 128X118X76	930/423	10 - 40	20 - 80	3 Phase 240 V, 60 Hz	BA11-PB BA11-PF	16.5 40	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11S60-BA.
11S60-BC	11/60W, MF11-WP, MM11-WP, DL11-W/LA36-CH, RK611, 2-RK06-AC, 866-D	DWLB	51X47X30 128X118X76	930/423	10 - 40	20 - 80	3 Phase 120 V, 50 Hz	BA11-PA BA11-PE	16.5 40	H7420A (7013050-0) H7420A (7013050-1)	Expansion Space Identical to the 11S60-BA.
11S60-BD	11/60W, MF11-WP, MM11-WP, DL11-W/LA3-CJ, RK611, 2-RK06-AD, 866-E	DWLB	51X47X30 128X118X76	930/423	10 - 40	20 - 80	3 Phase 240 V, 50 Hz	BA11-PB BA11-PF	16.5 40	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11S60-BA.

NOTE: Maximum heat dissipation: 11X60, 11Y60 - 14,500 Btu/hr; 11S60 - 17,000 BTU/hr; 11T60 - 16,000 Btu/hr.

Table 2-1 PDP-11/60 Configurations Data Sheet (Cont)

Model	Description	Cabinet Style	Size (in/cm) HXWXD	Weight (lbs/kg)	Operating Temp (°C)	Relative Humid (%)	Line Volt/Freq	Logic Card Cages	Amps at +5 V Available	DC Power Supplies	Comments
11S60-CA	11/60K, MF11S-KF, MM11S-KA, DL11-W/LA36-CE, RK611, 2-RK06-AA, H775-BA, 866-D	DWLB	51X47X30 128X118X76	930/423	10 - 40	20 - 80	3 Phase 120 V, 60 Hz	BA11-PK BA11-PE	25 53	H7420A (7013050-8) H7420A (7013050-1)	Expansion Space Identical to the 11S60-BA.
11S60-CB	11/60K, MF11S-KF, MM11S-KA, DL11-W/LA36-CF, H775-BB, RK611/2-RK06-AB, 866-E	DWLB	51X47X30 128X118X76	930/423	10 - 40	20 - 80	3 Phase 240 V, 60 Hz	BA11-PL BA11-PF	25 53	H7420B (7013050-10) H7420B (7013050-3)	Expansion Space Identical to the 11S60-BA.
11S60-CC	11/60K, MF11S-KF, MM11S-KA, DL11-W/LA36-CH, H775-BA, RK611/2-RK06-AC, 866-D	DWLB	51X47X30 128X118X76	930/423	10 - 40	20 - 80	3 Phase 120 V, 50 Hz	BA11-PK BA11-PE	25 53	H7420A (7013050-8) H7420A (7013050-1)	Expansion Space Identical to the 11S60-BA.
11S60-CD	11/60K, MF11S-KF, MM11S-KA, DL11-W/LA36-CJ, H775-BB, RK611/2-RK06-AD, 866-E	DWLB	51X47X30 128X118X76	930/423	10 - 40	20 - 80	3 Phase 240 V, 50 Hz	BA11-PL BA11-PF	25 53	H7420B (7013050-10) H7420B (7013050-3)	Expansion Space Identical to the 11S60-BA.
11T60-BA	11/60W, MF11-WP, 866-D, RK11D/RK05J-AA/ RK05-FA, DL11-W/LA36-CE	DWLB	51X47X30 128X118X76	710/323	10 - 40	20 - 80	3 Phase 120 V, 60 Hz	BA11-PA BA11-PE	22.5 40	H7420A (7013050-0) H7420A (7013050-1)	6 S.U.s of Expansion Space Available.
11T60-BB	11/60W, MF11-WP, 866-E RK11D/RK05J-AB/ RK05-FB, DL11-W/LA36-CF	DWLB	51X47X30 128X118X76	710/323	10 - 40	20 - 80	3 Phase 240 V, 60 Hz	BA11-PB BA11-PF	22.5 40	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11T60-BA.
11T60-BC	11/60W, MF11-WP, 866-D, RK11D/RK05J-AC/ RK05-FC, DL11-W/LA36-CH	DWLB	51X47X30 128X118X76	710/323	10 - 40	20 - 80	3 Phase 120 V, 50 Hz	BA11-PA BA11-PE	22.5 40	H7420A (7013050-0) H7420A (7013050-1)	Expansion Space Identical to the 11T60-BA.

Table 2-1 PDP-11/60 Configurations Data Sheet (Cont)

Model	Description	Cabinet Style	Size (in/cm) HXWXD	Weight (lbs/kg)	Operating Temp (°C)	Relative Humid (%)	Line Volt/Freq	Logic Card Cages	Amps at +5 V Available	DC Power Supplies	Comments
11T60-BD	11/60W, MF11-WP, 866-E, RK11D/RK05J-AD/ RK05-FD, DL11-W/LA36-CJ	DWLB	51X47X30 128X118X76	710/323	10 - 40	20 - 80	3 Phase 240 V, 50 Hz	BA11-PB BA11-PF	22.5 40	H7420B (7013050-2) H7420B (7013050-3)	Expansion Space Identical to the 11T60-BA.
11T60-CA	11/60K, MF11S-KF, 866-D, RK11D/RK05J-AA/ RK05-FA, DL11-W/LA36-CE, H775-BA	DWLB	51X47X30 128X118X76	560/254	10 - 40	20 - 80	3 Phase 120 V, 60 Hz	BA11-PK	6.5	H7420A (7013050-8)	2-Quad SPC Expansion Space Available. Expander Cage not included.
11T60-CB	11/60K, MF11S-KF, 866-E, RK11D/RK05J-AB/ RK05-FB, DL11-W/LA36-CF, H775-BB	DWLB	51X47X30 128X118X76	560/254	10 - 40	20 - 80	3 Phase 240 V, 60 Hz	BA11-PL	6.5	H7420B (7013050-10)	Expansion Space Identical to the 11T60-CA. Expander Cage not included.
11T60-CC	11/60K, MF11S-KF, 866-D, RK11D/RK05J-AC/ RK05-FC, DL11-W/LA36-CH, H775-BA	DWLB	51X47X30 128X118X76	560/254	10 - 40	20 - 80	3 Phase 120 V, 50 Hz	BA11-PK	6.5	H7420A (7013050-8)	Expansion Space Identical to the 11T60-CA. Expander Cage not included.
11T60-CD	11/60K, MF11S-KF, 866-E, RK11D/RK05J-AD/ RK06-FD, DL11-W/LA36-CJ, H775-BB	DWLB	51X47X30 128X118X76	560/254	10 - 40	20 - 80	3 Phase 240 V, 50 Hz	BA11-PL	6.5	H7420B (7013050-10)	Expansion Space Identical to the 11T60-CA. Expander Cage not included.

Table 2-1 PDP-11/60 Configurations Data Sheet (Cont)

Model	Description	Cabinet Style	Size (in/cm) HXWXD	Weight (lbs/kg)	Operating Temp (°C)	Relative Humid (%)	Line Volt/Freq	Logic Card Cages	Amps at +5 V Available	DC Power Supplies	Comments
H9600-AA	Expansion Cabinet with 866-D	DWHB	61X47X30 154X118X76		10 - 40	20 - 80	3 Phase 120 V, 60 Hz				BA11-P Card Cage not included; configured without end panels.
H9600-AB	Expansion Cabinet with 866-E	DWHB	61X47X30 154X118X76		10 - 40	20 - 80	3 Phase 240 V, 50 Hz				BA11-P Card Cage not included; configured without end panels.
H9601-AA	Expansion Cabinet with 866-D	DWLB	51X47X30 128X118X76		10 - 40	20 - 80	3 Phase 120 V, 60 Hz				BA11-P Card Cage not included; configured without end panels.
H9601-AB	Expansion Cabinet with 866-E	DWLB	51X47X30 128X118X76		10 - 40	20 - 80	3 Phase 240 V, 50 Hz				BA11-P Card Cage not included; configured without end panels.
H9602-BA	Expansion Cabinet with 861-D	SWHB	61X27X30 154X70X76		10 - 40	20 - 80	1 Phase 120 V, 60 Hz				BA11-P Card Cage not included; configured without end panels.
H9602-BB	Expansion Cabinet with 866-E	SWHB	61X27X30 154X70X76		10 - 40	20 - 80	1 Phase 240 V, 50 Hz				BA11-P Card Cage not included; configured without end panels.
H9603-BA	Expansion Cabinet with 866-D	SWLB	51X27X30 128X70X76		10 - 40	20 - 80	1 Phase 120 V, 60 Hz				BA11-P Card Cage not included; configured without end panels.
H9603-BB	Expansion Cabinet with 866-E	SWLB	51X27X30 128X70X76		10 - 40	20 - 80	1 Phase 240 V, 50 Hz				BA11-P Card Cage not included; configured without end panels.
H9603-CA	Expansion Cabinet	SWLB	51X27X30 128X70X76				N/A				BA11-P, Power Controller and end panels not included.

2.4 INSTALLATION

The installation procedure for a PDP-11/60 is essentially the same as that for all other PDP-11s. This installation procedure is described in the *PDP-11 Family Field Installation and Acceptance Procedure*, EK-FS003-IN, which should be followed and initialed as shown as the various steps are performed. This paragraph summarizes the PDP-11 family field installation and acceptance procedure; procedures and details that pertain especially to the PDP-11/60 are inserted.

2.4.1 Unpacking/Pre-Installation Procedures

WARNING

Do not uncrate the equipment until the procedures outlined in this paragraph have been completed.

Check the shipment for damage and inventory as described in the PDP-11 Family Field Installation and Acceptance Procedure (EK-FS003-IN), Chapter 2.

Figures 2-1 through 2-4 show packaging considerations provided to ease set-up and installation procedures.

1. Figure 2-1 shows the PDP-11/60 in packaged state. Note that a pallet is not required for shipping. A shock/vibration isolating caster assembly eliminates the need for pallets and allows direct forklifting of the system in transit.

CAUTION

The cabinets will arrive at their destination without shipping skids. Although it is not necessary to use a forklift, if used, it should be inserted from the front or back of a double width cabinet, or from the end of a single width cabinet.

Exercise care when moving cabinets; they may become unstable when tilted more than ten degrees.

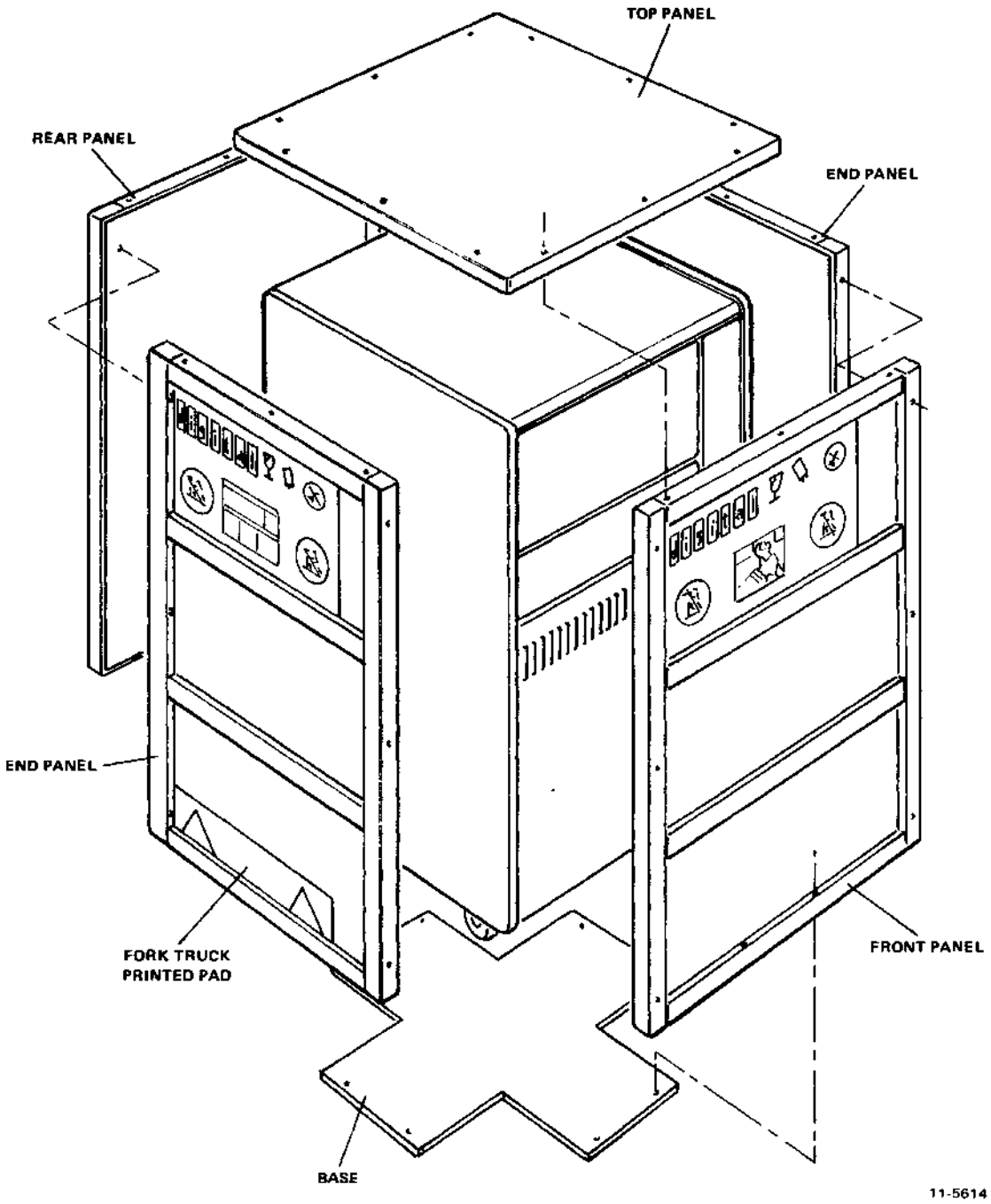


Figure 2-1 Shipping Container for Corporate Cabinet

2. Figure 2-2 shows retracting stabilizer legs in their receded position for normal operation.

NOTE

In this position, a mechanical interlock rod assembly (housed in front corner posts) prevents pulling out sliding devices (for service) prior to pulling out stabilizer legs.

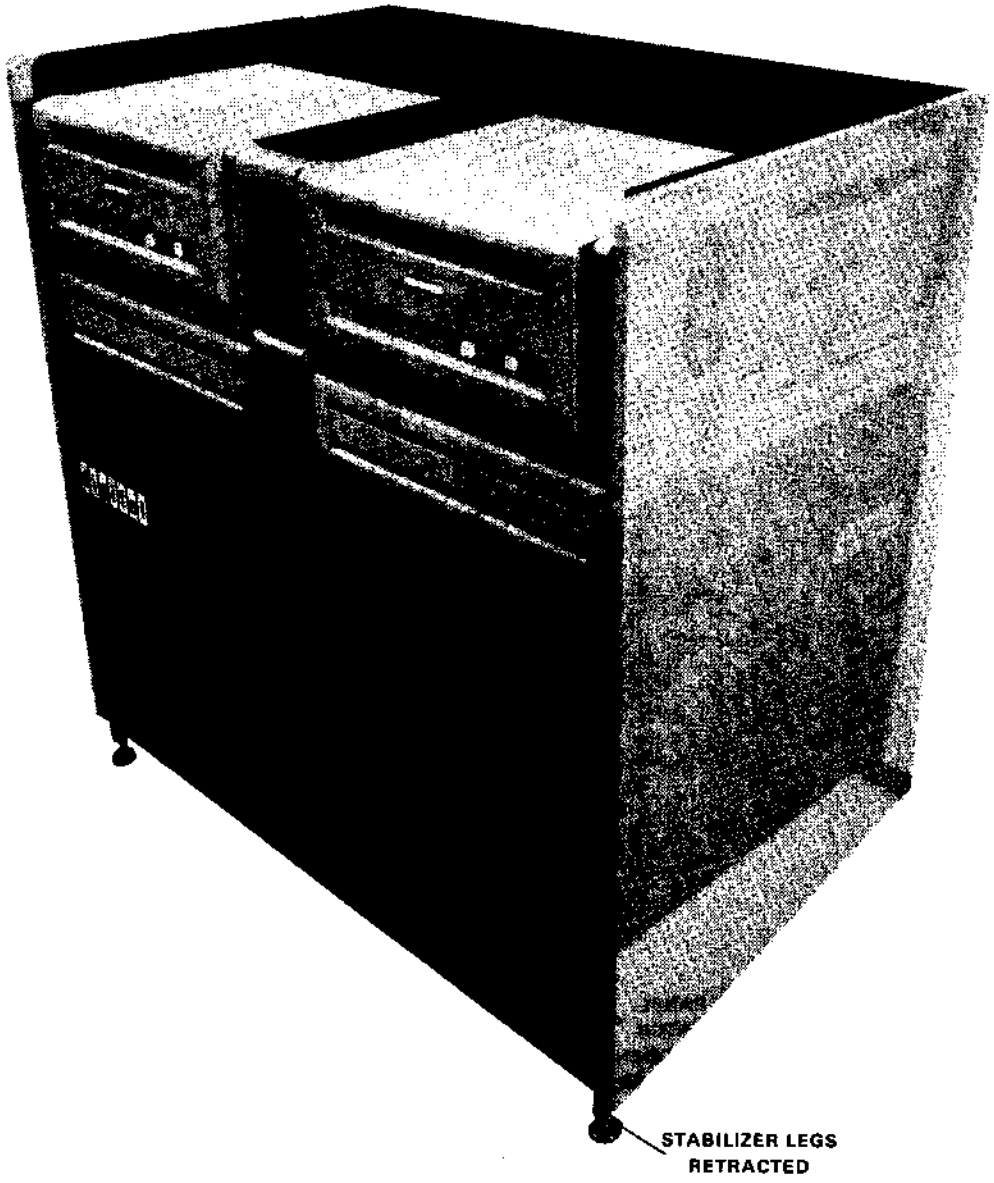


Figure 2-2 PDP-11/60 Normal Operation View

3. Figure 2-3 shows stabilizer legs in their service position.

4. Figure 2-4 shows the PDP-11/60 front view ready for servicing. Note safety latches on the BA11-P (CPU) and BA11-P (Expander) card cages. See Figure 2-3 for location of front panel safety latches. The rear panel needs a restricted release tool (spanner wrench, shipped separately in software box) for opening.

Document any damage and call it to the attention of the customer. If the damage is extensive, report it to the branch service manager or supervisor immediately. DIGITAL is not responsible for shipping damage on systems that are F.O.B. from the manufacturing facility.

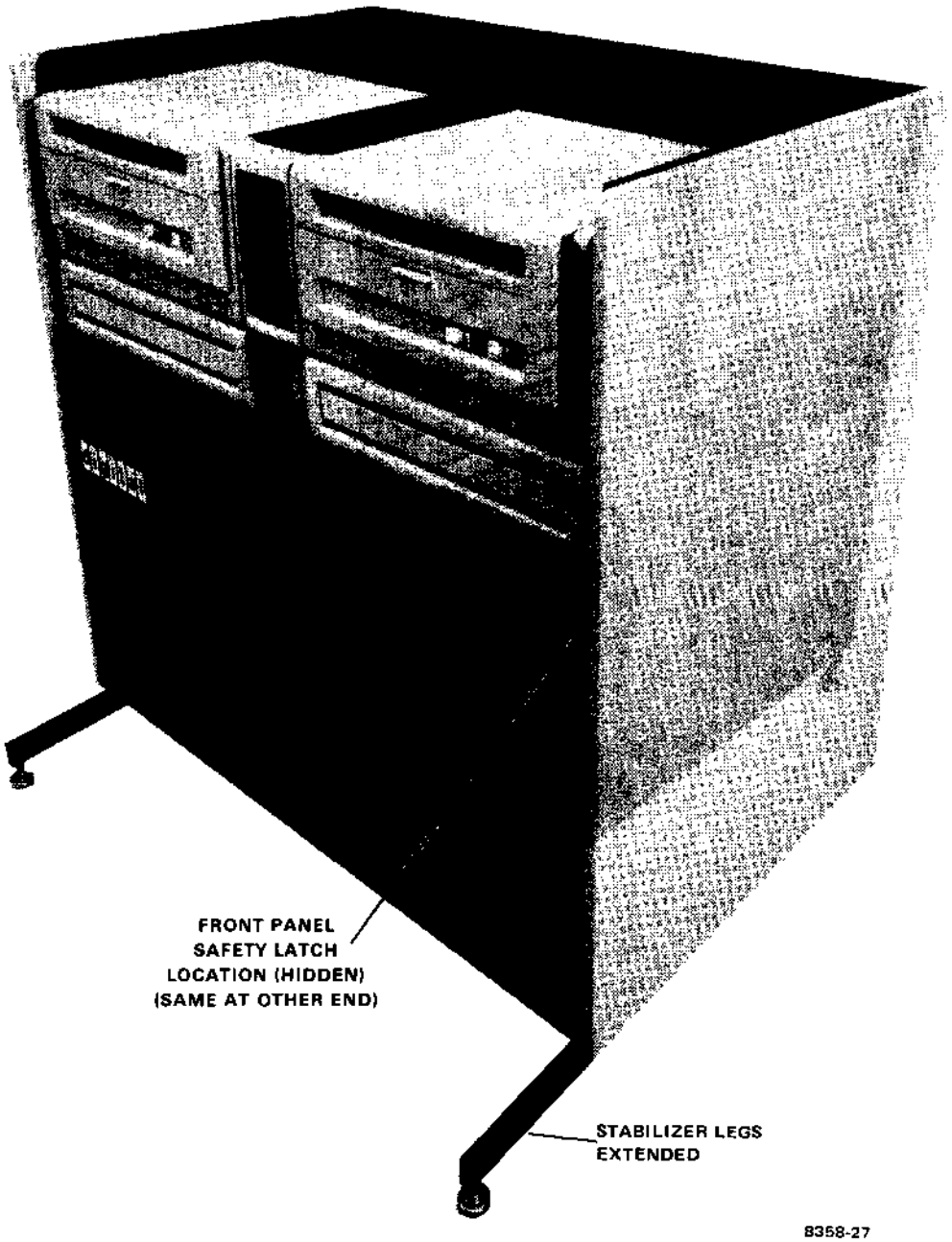
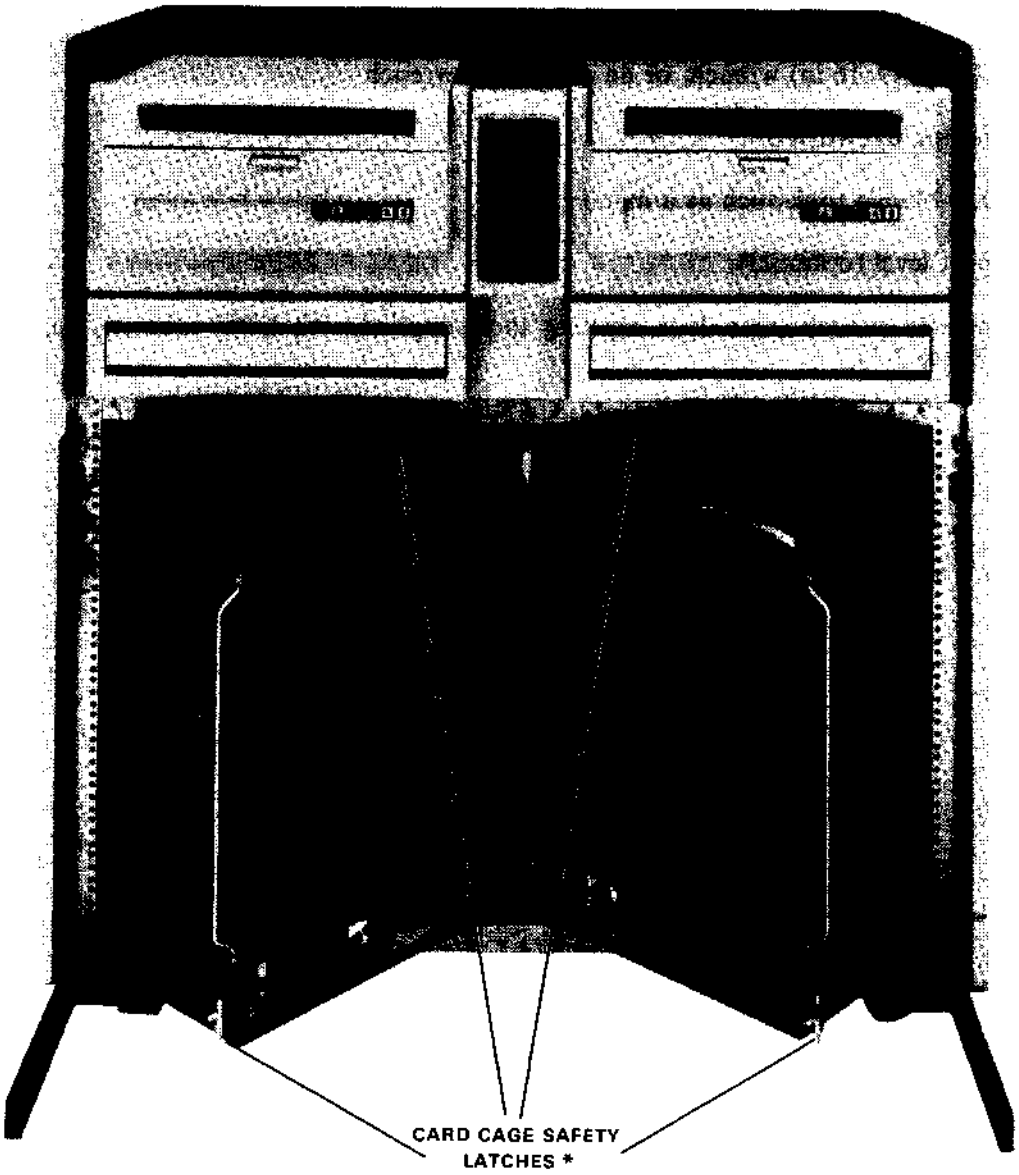


Figure 2-3 PDP-11/60 Sliding Device Loading Position



*THE TOP REAR SAFETY LATCHES ENGAGE WHEN CAGES ARE OPEN AT THEIR MAXIMUM. LATCH MUST BE PULLED DOWN BEFORE CAGE CAN BE OPENED FULLY. OTHERWISE, THE LATCH MAY BREAK WHEN IT HITS THE HORIZONTAL FRAME MEMBER. THESE LATCHES ARE USED TO HOLD THE CAGES OPEN DURING SERVICING.

8358-22

Figure 2-4 PDP-11/60 Ready for Servicing

2.4.1.1 Required Tools – The tools required for unpacking and installation are:

1. 1.11 cm (7/16 in) wrench, or an adjustable wrench
2. 1.43 cm (9/16 in) wrench, or an adjustable wrench
3. Phillips screwdriver
4. Thin bladed tool, such as a metal rule
5. Spirit level (optional)
6. Spanner wrench (rear door opening tool supplied with CPU cabinet), part no. 1213091 (Figure 2-5).

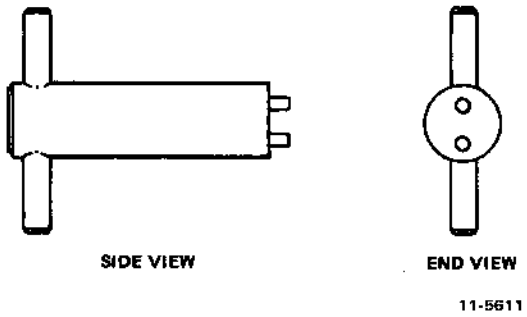


Figure 2-5 Rear Door Opening Tool

2.4.1.2 Unpacking – To unpack the cabinet proceed as follows:

1. Using a 1.11 cm (7/16 in) wrench, unbolt the bottom protector from the crate at the front, back, and sides.
2. Unbolt and remove the front panel of the crate.
3. Slide off the sides, back, and top panels as one piece.

2.4.1.3 Caster Locks – Caster locks, DIGITAL part no. 7417593-0-0, are supplied with each cabinet frame (Figure 2-6). These locks function to facilitate cabinet movement by preventing two of the four casters from swiveling. They also assist in providing cabinet stability by restricting the direction of cabinet movement. These cabinet locks are mounted with hardware and may be removed when it becomes absolutely necessary to move the cabinet during installation. When the cabinet has been installed at its final destination, the locks are to be removed. The locks should be stored with the cabinet if, in the future, the cabinets have to be moved again.

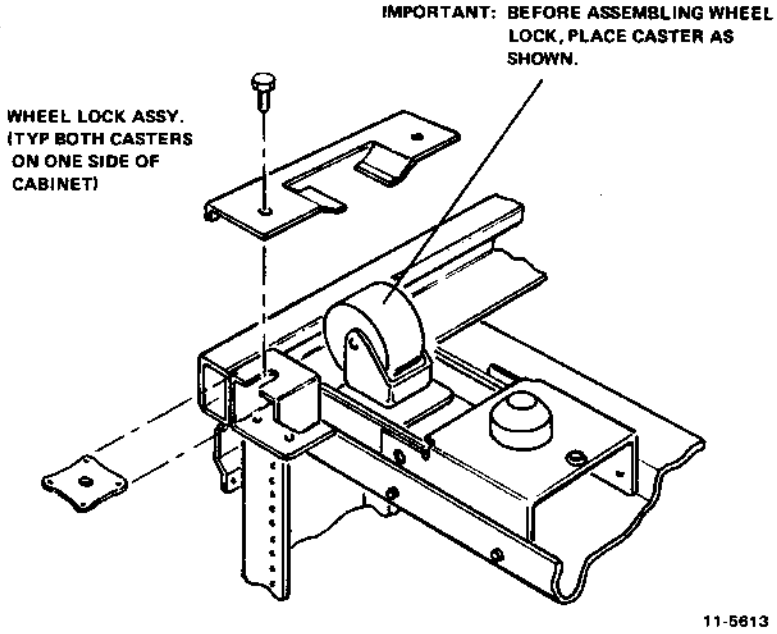


Figure 2-6 Caster Lock Assembly

2.4.1.4 Cabinet Leveling – As a result of weight differentials and self-contained shock mounts, the cabinets have to be leveled before they can be bolted together. Push the cabinets together and use the following procedure for leveling:

1. Install leveler feet in the cabinet frames (Figure 2-7).

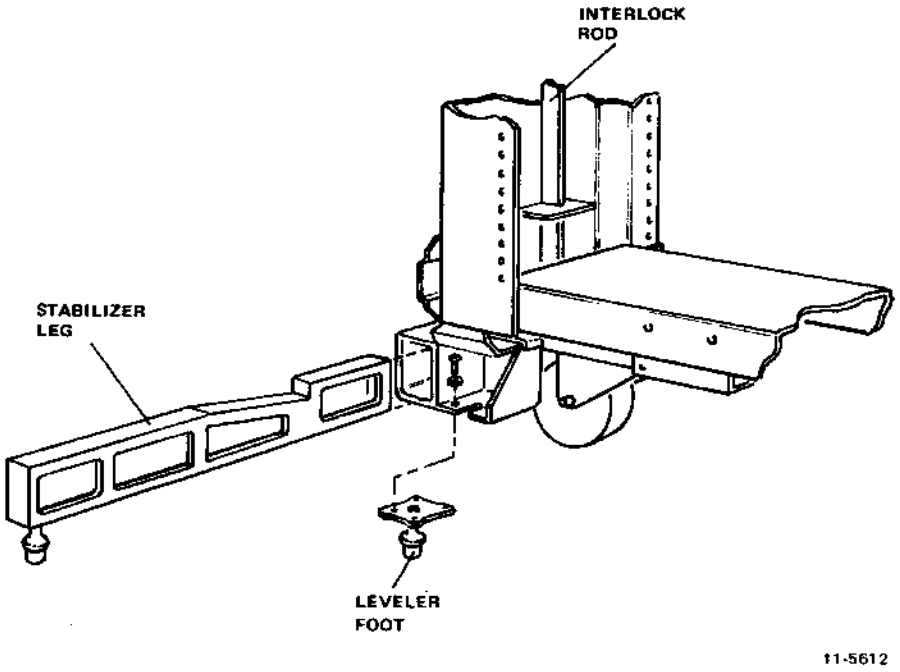


Figure 2-7 Locations of Stabilizer Leg and Leveler Feet

2. Using a 1.43 cm (9/16 in) wrench, lower the leveler feet until all four feet on each cabinet contact the floor.

3. Adjust the highest cabinet until most of its weight is shifted from the casters to the leveler feet. Because of the shock isolating system, the casters will always touch the floor even when all weight from the cabinet has been transferred to the leveler feet.

4. Using a spirit level, adjust the leveler feet until the cabinet is level (optional).

5. Adjust adjoining cabinets to the level of the highest cabinet.

2.4.1.5 PDP-11/60 Initial Set-Up Considerations – The standard PDP-11/60 includes two RK05 disk drives. During shipping these drives are held in place by a bracket (Figure 2-8). The top cover has to be opened in order to remove the shipping bracket. To remove the top cover, enter from the rear and locate the fastener attached to the underside of the top cover (Figure 2-9) (single width cabinet shown, on double width cabinets the fastener is located under the center brace). If access to the fastener is blocked, the fastener was not installed. Release the top cover by turning the fastener 1/4 turn in a counterclockwise direction. Push the top cover forward approximately 1.27 cm (1/2 in). Remove the ground strap. Lift the top cover off from the front of the cabinet. The shipping bracket is removed by unscrewing the two 1/4-20 KEP nuts and washers (Figure 2-8). Remove and discard the bracket. Reinstall the top cover.

2.4.2 Initial Set-Up

Move the equipment to the installation site (refer to Chapter 3 of the *PDP-11 Family Field Installation and Acceptance Procedure*).

NOTE

All optional covers (shipped separately) come with ground straps already attached. A grounding nut, part no. 9008203-01, is used to connect the straps to the cabinet frame. The corporate equipment cabinet has conductive plating, so there is no need to scrape off paint at any ground connection point.

Layout the I/O cables, but do not connect at this time. Check the physical layout with the configuration sheet.

2.4.3 Grounding, Power Checks, and Cabling

The following paragraphs should be used in conjunction with Chapter 4 of the *PDP-11 Family Field Installation and Acceptance Procedure.*

2.4.3.1 Grounding – Grounding for the PDP-11/60 is established through the center conductor of the 5-wire power cable that connects to the customer's ac receptacle, containing the required independent earth ground.

2.4.3.2 AC Power Supply Checks – Check the customer's ac power for proper voltage and phasing.*

*Phasing is not necessary unless enclosed peripherals are equipped with 3-phase motors, i.e., RP04.

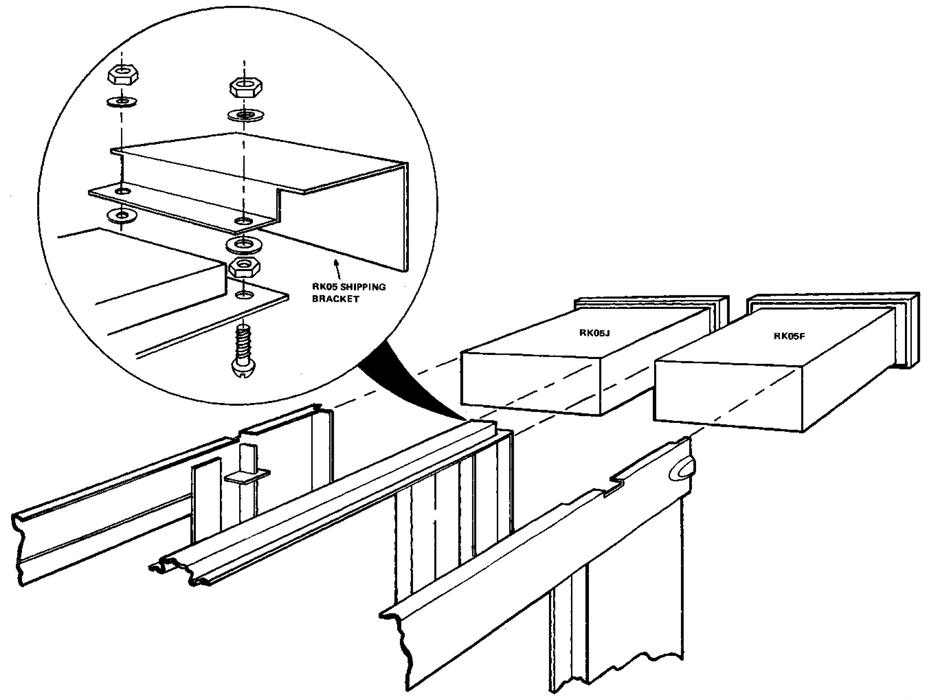


Figure 2-8 PDP-11/60,
RK05 Shipping Bracket Location

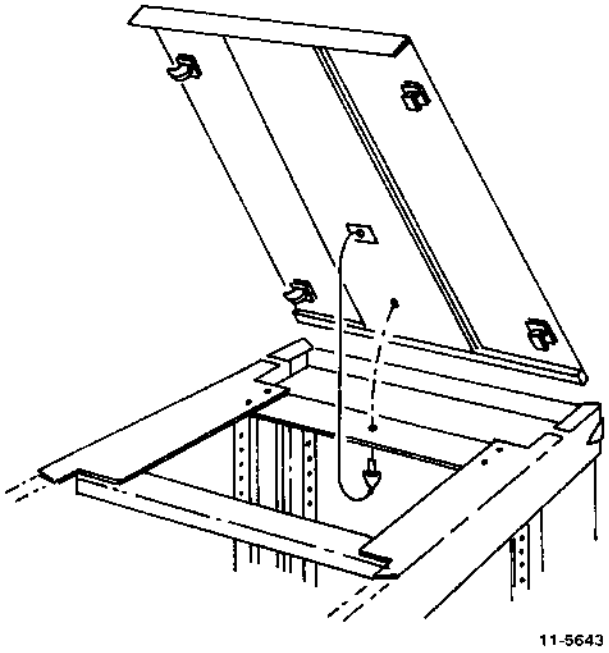


Figure 2-9 Top Cover Fastener

Check that the power receptacles are wired correctly and that ac ground is connected to all ground pins in all power receptacles for the system.

WARNING
It is very important that safety ground be maintained throughout the system to minimize the possibility of injury to personnel and damage to equipment.

Check the customer's ac power as follows:

Refer to Figure 2-10, which shows the ac power receptacle required for the PDP-11/60. Measure the voltage of the three phases and ground, with respect to each other (phase to phase), between each phase and neutral and between each phase and ground. The voltage should be between the limits defined in Paragraph 2.3. Approximately the same voltage should be read between each phase and the earth ground terminal.

2.4.3.3 Equipment Power Checks – Check all ac, dc, and signal cables.

NOTE
The PDP-11/60 power system is described in the PDP-11/60 Cabinet and Power Supply Manual.

Visually inspect all modules for any hardware that may be lodged between them. Check for unplugged cables, bent backplane pins, etc. Turn off the circuit breakers on the 866 controller.

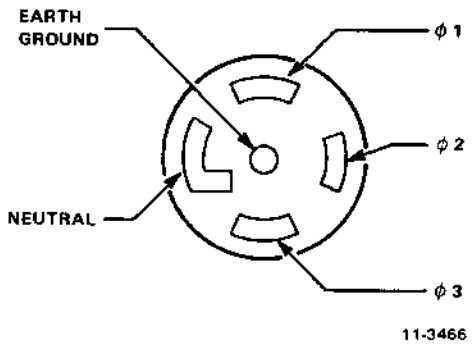


Figure 2-10 NEMA L21-30R Receptacle

Turn off the H7420 circuit breakers on the right side of the upper and lower power supply units.

NOTE
If expansion cabinets are employed in the system, the circuit breakers contained on the power controllers and supplies of these cabinets must also be turned OFF.

Plug all the 866* ac power cables into the customer receptacles.

NOTE
Do not coil or store unused portions of the 866 ac power cable within the PDP-11/60's cabinet.

Put the LOCAL/REMOTE switch on all 866s to the LOCAL position. Turn all 866 circuit breakers ON (main first). Turn the upper H7420 power supply circuit breaker ON; check that all regulator indicators are lit. Perform the same operation for the lower H7420 supply. Turn the LOCAL/REMOTE switch to the REMOTE position; all regulators should turn OFF. Turn the 5-position rotary switch on the console to the POWER position; check that all the regulator indicators are lit.

2.4.3.4 System Cabinet Checks – Starting with the CPU cabinet, perform the following for each cabinet (if expansion cabinets are included) in the system:

1. Check for correct ac voltage output from all the 866 ac outlets; the meter reading between points P and N shown in Figure 2-11 should be 90 to 132 Vac on 120 V systems, and 180 to 264 Vac on 240 V systems. The reading between terminals P and G should be the same as those between P and N.

2. Check that all fans are turning. There are four power supply fans, one for the transformer and three for the regulators, located at the top of each H7420. Two other processor cabinet fans are located beneath the CPU and expander card cages.

*The 240 Vac, 50 Hz version of the 866 can be identified by the 'E' designation on the panel of the controller. 866-E power controls are shipped without a power cable. This cable is connected during installation.

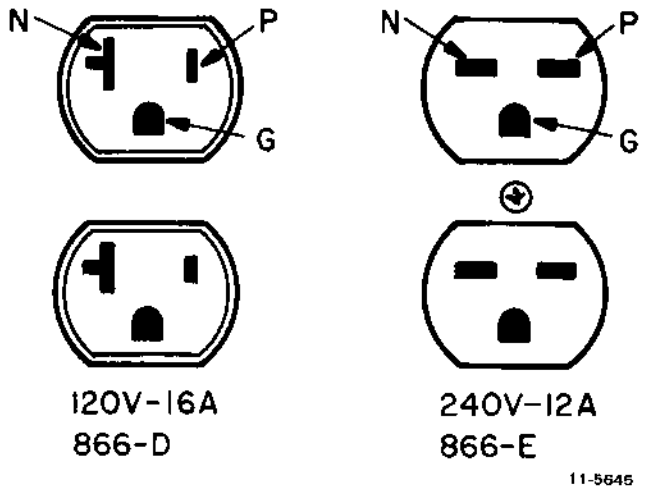


Figure 2-11 866 Power Control Outlets

3. Check card cage dc voltage levels with proper test equipment and adjust to specification. Table 2-2 lists the voltage test points for the CPU.

NOTE

Due to the different memory configurations (MOS/core) available with the PDP-11/60, backplane pin test locations are not listed, but the distribution panel pin numbers are. Refer to the particular memory manual for voltage test points.

4. Turn all ac power circuit breakers to the OFF position.

5. With the LOCAL/REMOTE switches set to the REMOTE position, verify that the remote sensing cables are installed.

6. Check all free standing peripherals.

NOTE

PDP-11/60 peripherals, such as the standard LA36 terminal, must not be connected to the switched outlets on the 866 power controller. These outlets are reserved for devices contained in the PDP-11/60's cabinet.

7. If expansion cabinets are employed, install the Unibus cable(s).

8. Install all peripheral cables.

9. Turn the ac power circuit breakers to the ON position.

Table 2-2 PDP-11/60 Voltage Measurements*

Output	CPU Distribution Panel Pin No.	CPU Backplane Pin	Voltage
Regulator A H7440 +5 V	J3-Pin 1	F02A2	+5 V
Regulator B H7440 +5 V	J3-Pin 2	F03A2	+5 V
Regulator C H7440 +5 V	J9-Pin 1	for SU 4,5, & 6	+5 V
Regulator D H781 +5 V	J6-Pin 1	F06A2	+5 V
Regulator D H781 +15 V	J6-Pin 3	C14U1	+15 V
Regulator E H754 +20 V	J9-Pin 3	for SU 4,5, & 6	+20 V
Regulator E H754 -5 V	J9-Pin 14	for SU 4,5, & 6	-5 V
Upper Supply	J6-Pin 11	F14B2	-15 V
Upper Supply H7420 AC LO	J7-Pin 4	B14F1	≅3.4 V
Upper Supply H7420 DC LO	J7-Pin 3	B14F2	≅3.4 V
Floating Point Supply H7421 Regulator H7441 +5 V (optional)	J4-Pin 3	F08A2	+5 V

*Use a digital voltmeter, Data Technology Model 31 or equivalent. All regulators have their grounds tied together, on the power distribution board, so any ground pin can be used for all measurements.

Table 2-2 PDP-11/60 Voltage Measurements (Cont)

Output	Expander Distribution Pin No.	CPU Backplane Pin	Voltage
Regulator H H7440 +5 V	J11-Pin 1		+5 V
Regulator J H7440 +5 V	J7-Pin 1		+5 V
Regulator K H781 +5 V	J3-Pin 1		+5 V
Regulator K H781 +15 V	J11-Pin 2		+15 V
Regulator L H754 +20 V	J11-Pin 3		+20 V
Regulator L H754 -5 V	J11-Pin 14		-5 V
Lower Supply H7420 -15 V	J11-Pin 13		-15 V
Lower Supply H7420 AC LO	J12-Pin 4		≅3.4 V
Lower Supply H7420 DC LO	J12-Pin 3		≅3.4 V

2.4.3.5 Preliminary System Check – Load all disk and magtape units with scratch packs and tapes.

Since the PDP-11/60 bootstrap module (M9301-YH) contains self-diagnostics, all the preliminary CPU checks listed in Chapter 4 of the *PDP-11 Family Field Installation and Acceptance Procedure* need not be performed; refer to the *M9301 Bootstrap/Terminator Operator/Maintenance Manual* for a detailed description of the self-diagnostics. A brief description of the M9301-YH bootstrap/terminator and its function in the PDP-11/60 is given in Paragraph 2.5.2. Turn on the CPU key and ensure that the power comes up. Check ac/dc low on the Unibus for proper levels (≅3.4 Vdc).

2.5 SYSTEM CHECKOUT

This chapter, used in conjunction with Chapter 5 of the *PDP-11 Family Field Installation and Acceptance Procedure*, is intended to prove the integrity of the PDP-11/60.

It consists of the following operations:

1. Checking the console functions, (Paragraph 2.5.1).
2. Booting the XXDP monitor via the M9301-YH (Paragraph 2.5.2).
3. Running the CPU and applicable peripheral diagnostics.
4. Running the system software exerciser, if available.

When these have been run successfully and the customer has accepted the system, the installation is complete.

No failures are permitted during the CPU, cache, main memory, memory management, Unibus, or (optional) floating point processor diagnostics. The error criteria for peripheral equipment are specified in the *PDP-11 Family Field Installation and Acceptance Procedure.*

Refer to Figure 2-12, which is a detailed installation checkout flowchart. The several steps in this flowchart are explained in the following paragraphs.

2.5.1 Console Functions

Refer to Paragraph 2.5.2.2 for the load address and start procedure using the console for initiating the bootstrap test program. More console operating procedures are contained in Chapter 3. For a detailed functional description of the console, refer to the *KD11-K Processor Technical Description Manual.*

2.5.2 M9301-YH Bootstrap Terminator

The M9301-YH is designed to provide bootstrapping capabilities for the PDP-11/60. In addition to that, the M9301-YH also includes routines that provide basic tests for the CPU, memory, and the cache.

The bootstrap test program has been designed for flexibility of operation. Its functions can be initiated automatically on power-up, by pressing the console "boot" switch, or by a load address and start sequence.

A set of microswitches is located on the M9301 module. They are used by the routines to determine what action is to be taken. Refer to Paragraph 2.5.2.4 for a description of the functions provided by the microswitches.

2.5.2.1 Diagnostic Bootstrap Program Location – Referring to Figure 2-13, all diagnostic tests reside in the first address space: 765 000 – 765 776. All bootstrap loaders reside in the second address space: 773 000 – 773 776.

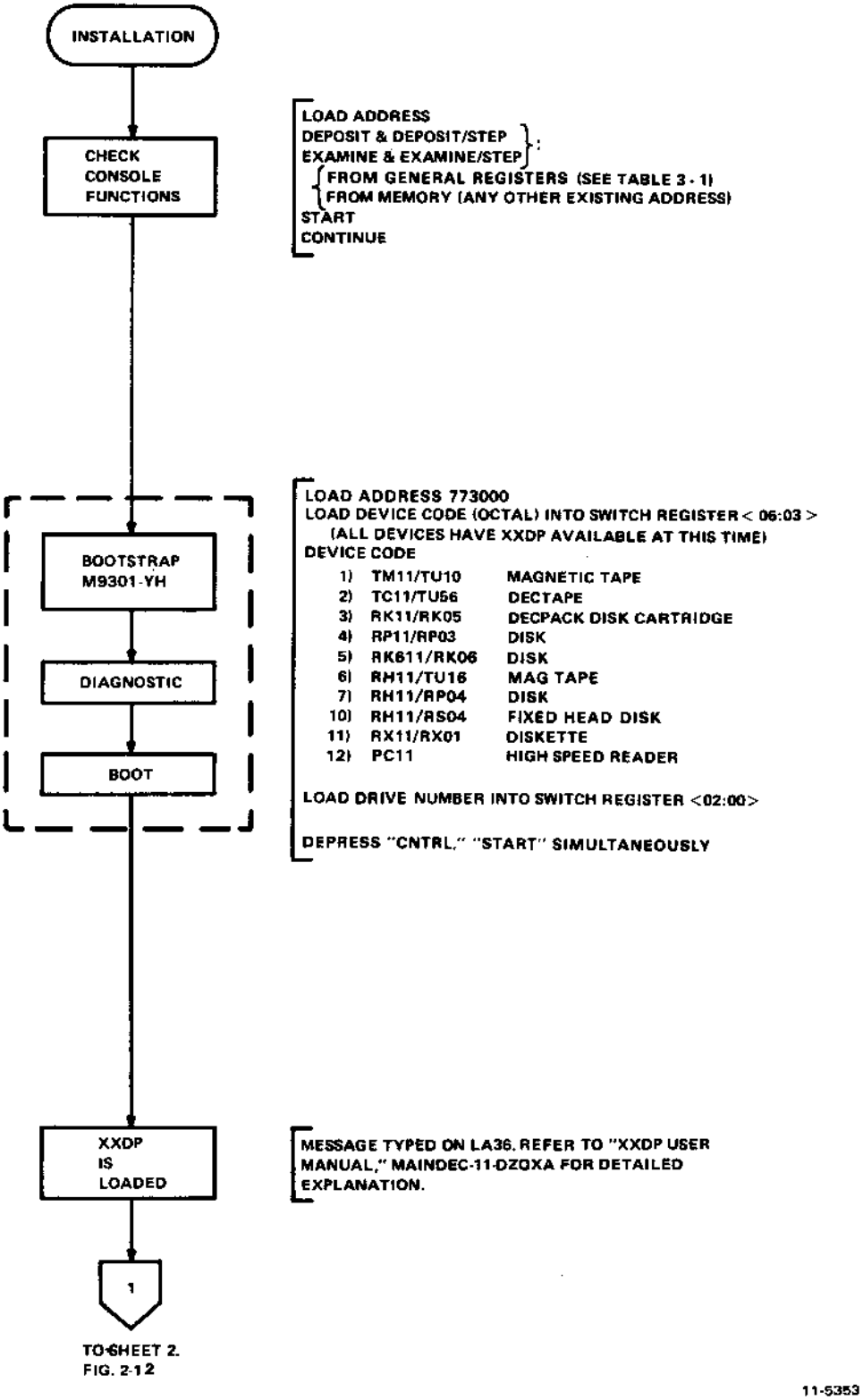


Figure 2-12 System Checkout Flowchart (Sheet 1 of 2)

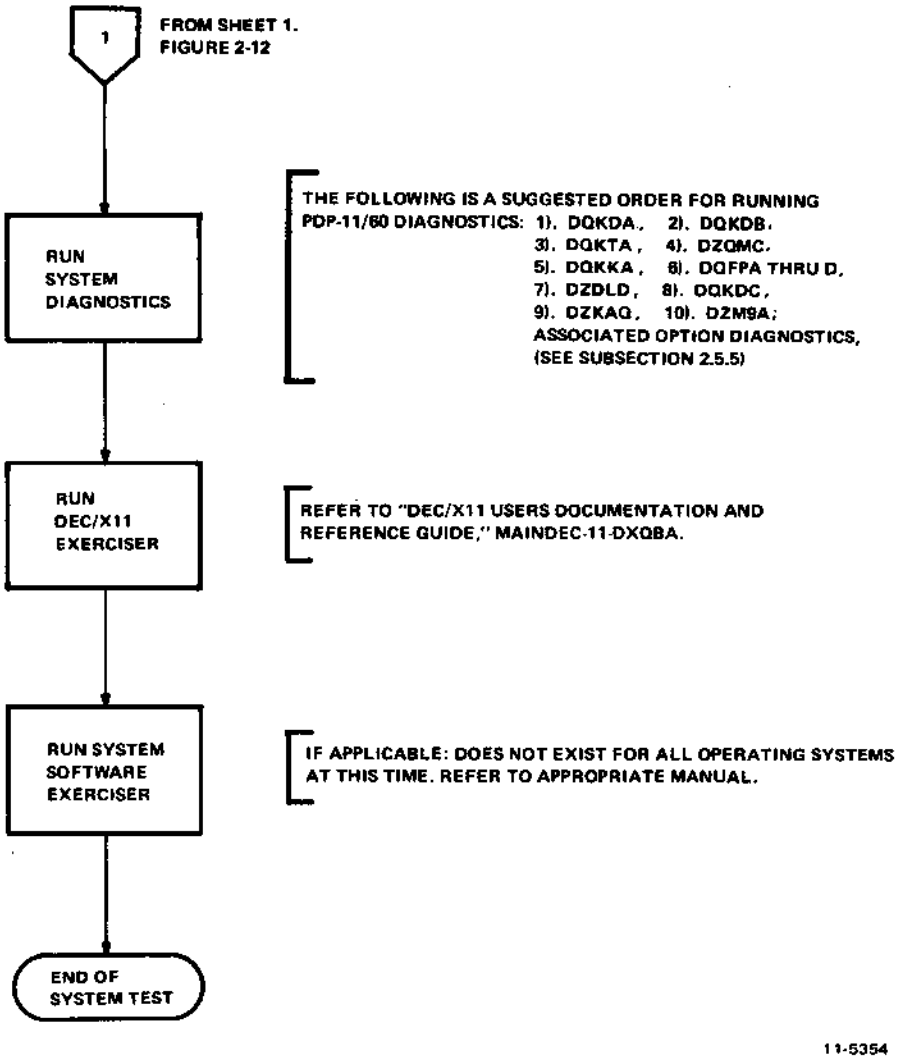


Figure 2-12 System Checkout Flowchart (Sheet 2 of 2)

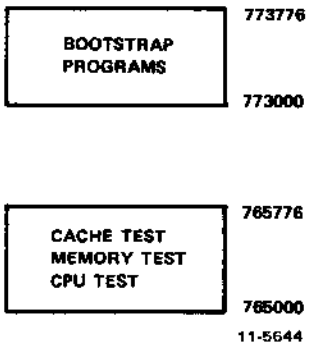


Figure 2-13 M9301-YH Program Memory Map

2.5.2.2 Initiation – The bootstrap test program can be initiated in one of the following ways:

1. Automatically on power up.
2. Pressing the CNTRL and BOOT switches on the console, simultaneously.
3. Load address and start sequence from the console.

Power-Up Start
On the PDP-11/60 there is a 3-position slide switch (BOOT/RUN/HALT) on the console. If this switch is left in the BOOT position and power-up occurs, an automatic booting will occur from the peripheral specified in the microswitches (Paragraph 2.5.2.4). The test routines will be executed prior to booting depending on the setting of microswitches (Paragraph 2.5.2.4).

BOOT Switch
When the CNTRL and BOOT switches on the console are pressed, simultaneously, booting occurs from the peripheral selected in the microswitches. The test routines will be executed depending on the setting of the microswitches (Paragraph 2.5.2.4).

2.5.2.3 Switch Register Loading – When the "load address, start" sequence is used to initiate the bootstrap, the booting will occur either from the default device specified in the microswitches or the device unit specified in the switch register. The procedure is to load address, then load the switch register properly and press control, start.

Starting Address	
773000	PDP-11/60
SWREG (Lo byte)	Function
0	Boot from default device, drive 0
Nonzero	Boot from device and drive number specified in the switch register.

SW REG (6:3) contains the device code (0–12). SW REG (2:0) contains the drive unit number (0–7). The device codes are as follows:

Device Code [SW REG (6:3)]	Device
0	Use the device specified in microswitches
1	TM11/TU10 magtape
2	TC11/TU56 DECtape
3	RK11/RK05 disk
4	RP11/RP03 disk
5	RK611/RK06 disk
6	RH11/TU16 magtape (800 bpu, NRZI)
7	RH11/RP04 disk
10	RH11/RS04 fixed head disk
11	RX11/RX01 diskette
12	PC11 high-speed reader

2.5.2.4 Microswitches, Option Selection – There is a flatpack containing ten microswitches on the M9301. Depending on the setting of these microswitches, the program and the machine take different actions. (The microswitches can be read at UBA 773024.)

Microswitches	Description
10	Used to select processor type if OFF, then PDP-11/70 if ON, then PDP-11/60.
09	If OFF, do not execute any test routines (CPU, cache, memory) If ON, execute test routines (Note: see microswitch 3).
08	If OFF, the ROM bootstrap program will not check the console SW REG before booting. If ON, the ROM bootstrap program will check the console SW REG and will boot accordingly.
07–04	Device code for selecting the device to boot from (default device). (SW4=MSB, SW7=LSB.) **NOTE** **The device codes for selecting the default device from which booting will occur are the same as shown in Paragraph 2.5.2.3, Switch Register Loading. The ten microswitches that are contained on the flatpack are labeled ON and OFF. When setting switches SW4 through SW7, a compliment setting is required. These switches are inverted in hardware; therefore, OFF = 1 and ON = 0.**
03	If OFF, execute memory-modifying tests before booting (Paragraph 2.5.2.5) (JSR, RTS, RTI, memory tests, cache tests). **NOTE** **This microswitch is looked at only if 9 is on.**
02	Switch should be OFF for PDP-11/60; switch should be ON for PDP-11/70 if boot on power up is to be used.
01	If OFF, the low ROM (765000–765776) is disabled. If ON, the low ROM is enabled normal position of SW 01 is ON.

Microswitch option 8* is provided to protect the user against unintentional or nonauthorized setting of the console switch register. Normally, ON power-up (subsequent to power-fail) booting will be done from the device code specified in the microswitches (on M9301 module), provided the console switch register is clear. If the console switch register is not clear, the program will use the code specified in the switch register for selecting the device from which to boot. If the microswitch is left in the OFF position, the bootstrap program will not sense the console switch register; thus eliminating the possibility of attempting to boot from an undesired or nonexistent peripheral in case the console switch register is set randomly.

*Note that on the PDP-11/60 the position of SW8 is irrelevant, because the console switch register is cleared automatically. But if SW8 is OFF, the program will never look at the console switch register, even if a LOAD ADDRESS and START is attempted.

Power-Up Boot/Microswitch Setting Examples

A. TU10 – Set the microswitches as follows:

SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8*	SW9	SW10
ON	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON

On power-up, the system will execute all diagnostics and boot the TU10.

B. RK05 – Set the microswitches as follows:

SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10
ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON

On power-up, the system will boot drive 0 of the RK05 without executing diagnostics.

Refer to Table 2-3 for microswitch settings to select PDP-11/60 peripheral devices.

Table 2-3 M9301-YH Switch Settings for PDP-11/60

Device Name	Code	Microswitch Settings									
		01	02	03	04	05	06	07	08	09*	10
TM11/TU10	1	ON	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON
TC11/TU56	2	ON	OFF	OFF	ON	ON	OFF	ON	ON	ON	ON
RK11/RK05	3	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON
RP11/RP03	4	ON	OFF	OFF	ON	OFF	ON	ON	ON	ON	ON
RK611/RK06	5	ON	OFF	OFF	ON	OFF	ON	OFF	ON	ON	ON
RH11/TU16	6	ON	OFF	OFF	ON	OFF	OFF	ON	ON	ON	ON
RH11/RP04	7	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON
RH11/RS04	10	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON
RX11/RX01	11	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	ON
PC11	12	ON	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON

*If 09 is ON, CPU, cache and memory test routines are executed. If ON, this switch works in conjunction with 03. If 09 is OFF, 03 is ignored. Switch 03, if ON, allows CPU and cache test routines, but disables memory modifying tests.

2.5.2.5 Test Routines in M9301-YH – The M9301-YH has tests to checkout the CPU (instructions), cache, and memory (up to 28K). There are two types of tests.

1. Non-memory modifying tests
2. Memory-modifying tests

The CPU instruction tests are non-memory modifying and are executed prior to booting if microswitch 9 is ON (Paragraph 2.5.2.4).

The memory-modifying tests constitute the tests for RTS, RTI, and JSR instructions; the cache; and the memory. These tests are executed prior to booting if microswitch 09 is ON and microswitch 03 is OFF (Paragraph 2.5.2.4).

CPU Tests
This section consists of several subtests that check the CPU data path and control logic using various instructions.

Main Memory Test
This test checks out the main memory (up to 28K), with the cache disabled. Parity error vector has been set up, hence parity errors, if found, will be detected.

Cache Test
This section has tests to check the cache. The test checks if the cache hits can be obtained all the way through the memory. Also, the data memory of the cache is checked.

2.5.3 Errors
A list of error halts indexed by the address displayed is shown in Table 2-4.

If the bootstrap operation fails as a result of a hardware error in the peripheral device, the program will do a reset instruction and attempt to boot again.

Table 2-4 Error Halts Indexed

Address Displayed	Test Number and Subsystem Under Test
165004	Test 1, Branch Test
165020	Test 2, CLR and Conditional Branch Test
165036	Test 3, DEC and Conditional Branch Test
165052	Test 4, ROR and Conditional Branch Test
165066	Test 5, Conditional Branch Test
165076	Test 6, Conditional Branch Test
165126	Test 7, Register Data Path Test
165136	Test 10, Conditional Branch Test
165154	Test 11, CPU Instruction Test
165172	Test 12, CPU Instruction Test
165202	Test 13, CPU Instruction Test
165210	Test 14, CPU Instruction Test
165224	Test 14, CPU Instruction Test
165246	Test 15, CPU Instruction Test

Table 2-4 Error Halts Indexed (Cont)

Address Displayed	Test Number and Subsystem Under Test
165256	Test 16, Branch Test
165300	Test 16, CPU Instruction Test
165334	Test 17, CPU Instruction Test
165352	Test 20, CPU Instruction Test
165376	Test 21, JSR Test
165406	Test 21, JSR Test
165416	Test 21, RTS Test
165430	Test 21, RTI Test
165436	Test 21, JMP Test
165520	Test 22, Main Memory Data Compare Error
165540	Test 22, Main Memory Data Compare Error no recovery possible from this error
165604	Test 23, Cache Memory Data Compare Error
165614	Test 23, Cache Memory No Hit (pressing continue here will cause boot attempt, forcing cache misses)
165720	Test 24, Cache Memory Data Compare Error
165732	Test 24, Cache Memory No Hit (pressing continue here will cause boot attempt, forcing misses in the cache)
165752	Test 22, 23, or 24, Cache Memory or Main Memory Parity Error. (Examine memory error register 777744 to find out more.) If cache parity error, pressing continue here will cause boot attempt forcing misses in cache.

2.5.4 Operator Action and Error Recovery

If the diagnostic portion of the ROM program detects an error, the processor will halt. The address displayed should be noted. Table 2-4 contains a cross-reference of address displayed versus test number and subsystem under test. For further details, refer to the listing for the ROM program.

Most of the errors described in Table 2-4 are hard failures, and there may be no recovery from them.

If the processor halts in one of the two cache tests, error recovery is possible. When continue is pressed, the program will either attempt to finish the test (165604 or 165720) or force misses in both groups of the cache and attempt to boot with the cache fully disabled (165614, 165732, or 165752).

If the program fails in a uncontrolled manner, it might be due to an unexpected trap to location 4 or 10. If this is suspected, then load the following:

LOC	Contents
4	6
6	0
10	12
12	0

This loading will cause all traps to vectors 4 and 10 to halt the processor at addresses 6 and 12, respectively (with addresses 10 and 14 in the display); the operator can examine the CPU error register at 777766 to get more error information. Bits in CPU EREG are defined as follows:

Bit 02 = Red Zone Stack Limit
Bit 04 = Unibus Timeout
Bit 06 = Odd Address Error

2.5.5 Diagnostics

2.5.5.1 Basic Kits – Four basic diagnostic kits are available for the PDP-11/60:

ZJ011-RB PDP-11/60 Basic Diagnostic Document/Paper Tape Kit
ZJ011-RZ PDP-11/60 Basic Diagnostic Document – Only Kit
ZJ011-PB PDP-11/60 Basic Diagnostic Paper Tape – Only Kit
ZJ011-FR PDP-11/60 Basic Diagnostic Fiche – Only Kit

The diagnostics listed in Table 2-4 are reproduced on all of the XXDP media except cassette. XXDP programs and a DEC/X11 kit are also of interest when using a PDP-11/60.

NOTE
MD-11-DZQMC (0–124K Memory Exerciser Program) should be used with the PDP-11/60s containing MF11-P core memory; MD-11-DZMML (MS11-K Memory Diagnostic) should be used with PDP-11/60s containing MS11-K MOS memory.

When ordering, specify either the desired revision or leave it blank and the latest revision will be sent.

2.5.5.2 Diagnostic Load/Run Procedure – Locate the installation checklist, if available (a computer printout). Compare the configuration key, or transfer sheet, to the installation checklist and check under "RUN" the diagnostics for all options listed as being present in this system. Load and run the diagnostics in the installation checklist that are applicable to the system for the time or number of passes specified.

The diagnostics should be run in the suggested order specified in Figure 2-12 and listed in Table 2-5.

Operating procedures and listings for all diagnostics are contained in the MAINDECs for each program. Operating procedures for the XXDP monitor are described in the *XXDP User Manual*, MAINDEC-11-DZQXA.

Table 2-5 PDP-11/60 Diagnostics

DOC/Order Codes	Title
MAINDEC-11-DQKDA	KD11-K Basic Logic Tests
MAINDEC-11-DQKDB	PDP-11/60 Trap Tests
MAINDEC-11-DQKTA	PDP-11 Memory Management Diagnostic
MAINDEC-11-DZQMC	0–124K Memory Exerciser
MAINDEC-11-DQKKA	PDP-11/60 Cache Diagnostic
MAINDEC-11-DQFPA	PDP-11/60 Floating Point Unit, Basic Instruction Tests
MAINDEC-11-DQFPB	PDP-11/60 Floating Point Advanced Instruction Tests
MAINDEC-11-DQFPC	PDP-11/60 Floating Point Unit Instruction Exerciser
MAINDEC-11-DQFPD	PDP-11/60 Floating Point ADD/SUB/MUL/DIV Exerciser
MAINDEC-11-DZDLD	DL11-W Diagnostic
MAINDEC-11-DQKDC	PDP-11/60 Series CPU Exerciser
MAINDEC-11-DZKAQ	PDP-11 Power Fail Tests
MAINDEC-11-DZM9A	PDP-11/60 Bootstrap/Terminator (M9301, M9400)
MAINDEC-11-DZKUA	Unibus System Exerciser
MAINDEC-11-DZKUB	Unibus Exerciser Module Diagnostic
MAINDEC-11-DZMML	MS11-K MOS Memory Tests
MAINDEC-11-DQM9A	PDP-11/60, PDP-11/70 ROM Bootstrap/Test Program (Document for listing at M9301-YH)
MAINDEC-11-DQKUA	PDP-11/60 WCS Diagnostic
MAINDEC-11-DQFPE	PDP-11/60 Hot Floating Point Diagnostic
MAINDEC-11-DQKUB	KD11-K Microdiagnostics (DCS Listing and Error Dictionary)

2.5.5.3 DEC/X11 System Exerciser – DEC/X11 is a system exerciser, i.e., it is an operating system that runs all devices in a system, using random data. Any errors are reported.

DEC/X11 must be configured for each individual system. The *DEC/X11 User's Documentation and Reference Guide*, MAINDEC-11-DXQBA, contains all information required to configure and run DEC/X11 and to interpret the results of the tests performed. The XXDP DEC/X11 Programming Card, MAINDEC-11-DZZPA, contains a summary of DEC/X11 features.

Turn to the system exerciser section of installation checklist and prepare to load DEC/X11. The system exerciser checklist numbering sequence begins with IBXXXX. To start the DEC/X11 package, refer to notes at the beginning of the system exerciser section of the installation checklist. Device test module QABM is used for the PDP-11/60.

2.5.6 Summary and Final Acceptance

Go through each chapter of the *PDP-11 Family Field Installation and Acceptance Procedure* and ensure that all areas requiring an initial are so marked. If an initial is missing, investigate that section and complete if necessary.

Ensure that all paperwork is complete. The field service and/or installation reports should reflect any problems/repairs encountered during the installation. After completion, the reports and checklists should be returned to the office.

The installation is now complete. Have the customer sign the field service report reflecting installation activity.

2.6 EXPANSION INSTALLATION

Add-on installation may be:

1. System Unit (SU) options
2. Rack-mounted options
3. Cabinet options

Installation in an existing system consists of:

1. Determination of the best electrical and physical position of the option on the Unibus. Guidelines are supplied in Paragraph 2.6.2 to aid in this determination.

2. Mechanical installation of the option.

2.6.1 Mechanical Installation

1. SUs are mounted in BA11-P boxes. All required information is supplied in the *PDP-11/60 Cabinet and Power Supply Manual.*

2. Refer to Figures 1-8 through 1-15 (configuration diagrams) for the amount of expansion space available in the processor cabinet. Any additional small peripheral controllers (SPCs) should be mounted with other I/O devices in the system, because of the potential cable congestion problem that may arise from the PDP-11/60's requirement to build the memory and I/O Unibus on separate cables.

3. Instructions for installation of rack-mounted and cabinet options are contained in their respective manuals.

2.6.2 System Configuration (Unibus)

NOTE

System configuration is a function not only of the variables mentioned below, but also of size, available space, and power distribution. These factors are not discussed here, but must be taken into consideration when a system is reconfigured.

System configuration as defined here is a function of two variables:

1. The tolerance of each device for delays in service (maximum tolerable latency), and
2. The data transfer demand placed by each device on the system.

As the demand of device X increases, it increases the time that device Y must wait for service. The order in which devices are serviced depends on:

1. Their assigned priority, in descending order: NPR, BR7, BR6, BR5, BR4.

2. Within each priority, the order in which they are placed on the Unibus (electrical position).

The definitions that follow are taken from the glossary of the Unibus specification:

Latency is the delay between the time that a device initiates a transaction and the time that it receives a response.

Thus, if a device requests the use of the data section of the bus, is granted the use of the bus, and then receives the negation of BBSY (signifying that the previous master has released the data section of the bus), then latency is the delay between the assertion of the request and the receipt of the negation of BBSY by the requesting device.

Maximum Tolerable NPR Data Transfer Latency is the longest time that a device may be refused bus mastership before it loses data. It affects only devices that transfer data in a constant stream, e.g., a disk.

Maximum Tolerable BR Interrupt Latency is the longest time the computer can take to service an interrupt before the requesting device loses its data. The service time includes the execution of all higher priority interrupts and programs that may be pending, plus the time spent in the interrupt subroutine of the device in question.

From the preceding, general rules for configuration may be stated as follows ("behind" means farther from the processor):

1. In general, BR devices should be placed physically behind NPR devices; thus, the propagation delay of fast NPR devices is reduced and transfers are faster. For convenience, however, some BR devices are sometimes placed before NPR devices, e.g., DL11-W/LA36 is first on the Unibus in the PDP-11/60 (slot 14 of the processor backplane.)

2. Buffered devices (Category 2: Figure 2-15 for definition) should be placed physically behind unbuffered devices (Category 1: Figure 2-15).

3. In either category, devices with higher transfer speed rates should be placed ahead of devices with lower speed rates.

4. Less used devices may be placed behind devices that are accessed more often, if required.

Figure 2-14 shows the optimum placement of NPR Unibus devices in a PDP-11/60 system.

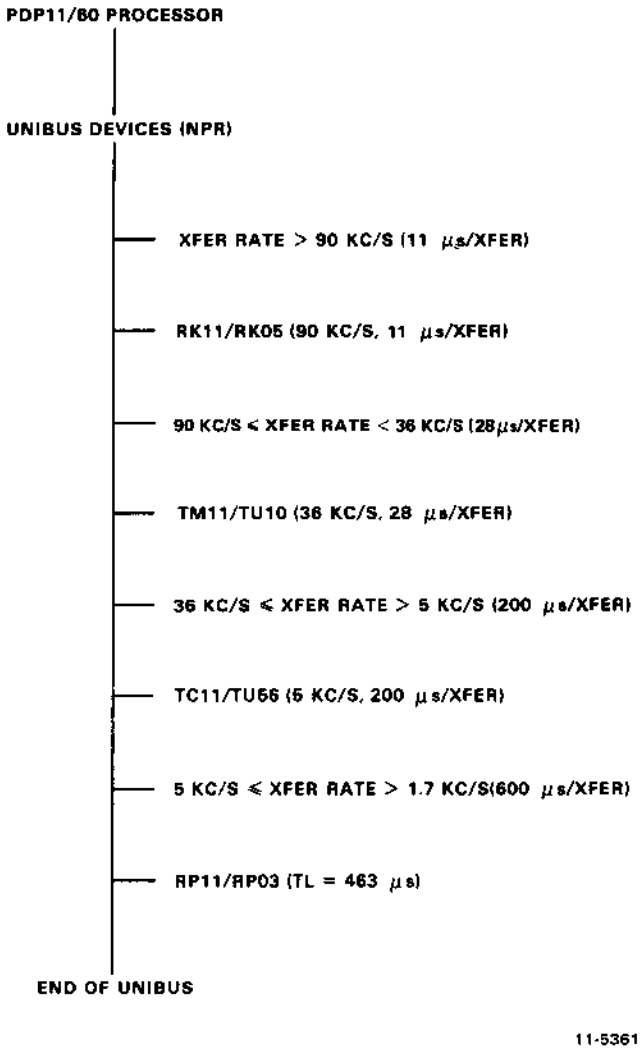


Figure 2-14 PDP-11/60 Unibus Device Placement Example

The flowchart (Figure 2-15) provides an algorithm by which these variables can be combined to produce an optimum Unibus system configuration of both NPR or BR devices. BR devices are placed behind NPR devices with the same data transfer rates, and before NPR devices with slower data transfer rates. The same algorithm is used. This flowchart is intended only as a guideline.

NOTE

The algorithm given in Figure 2-15 suggests the optimum positioning of contending devices on the Unibus. This positioning is not mandatory. If the configuration resulting from the use of this algorithm is not satisfactory, alternative placement of devices should be tried.

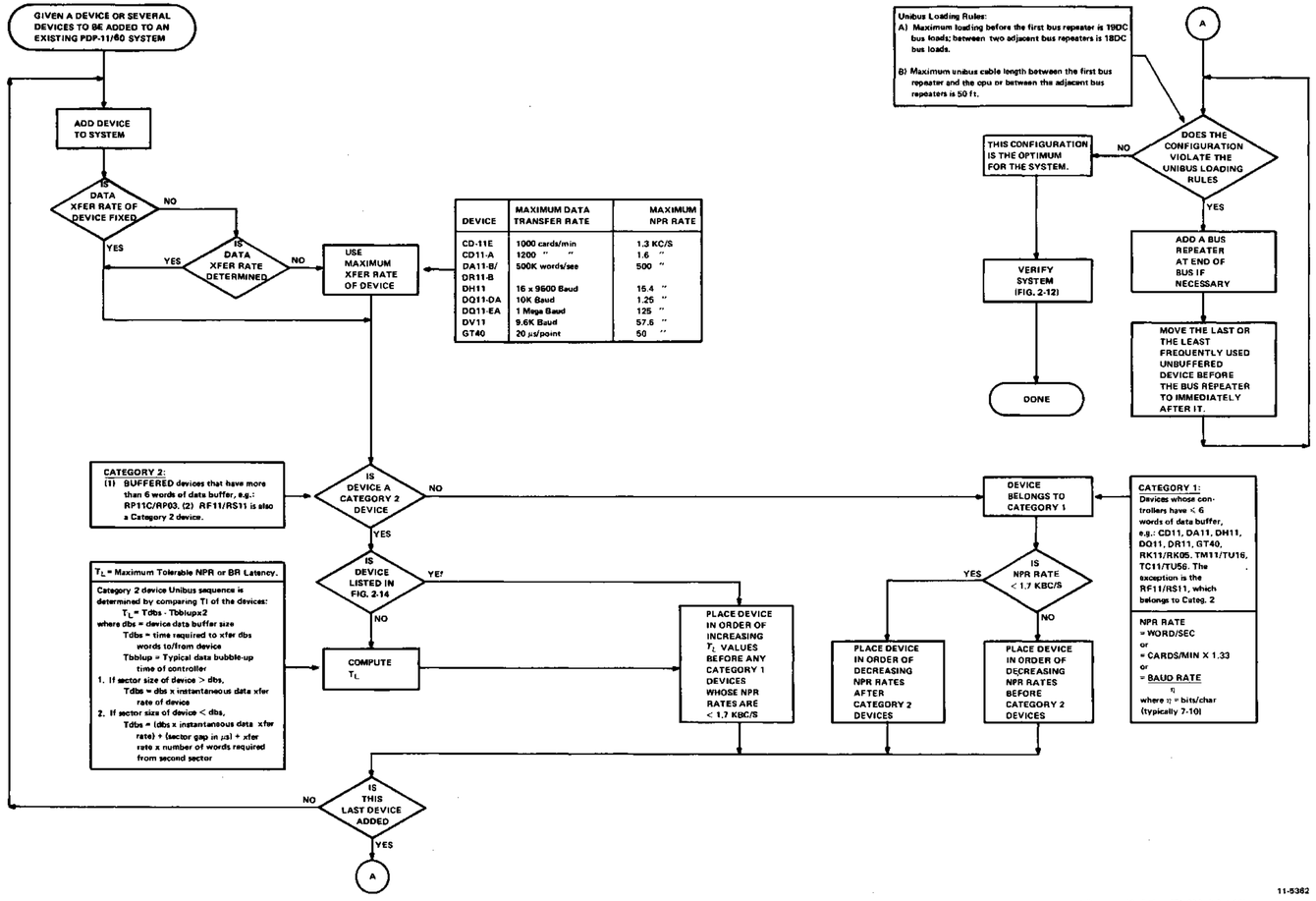


Figure 2-15 PDP-11/60
Unibus Device Placement Flowchart

CHAPTER 3
OPERATION

3.1 INTRODUCTION

This chapter includes all of the information required to operate the PDP-11/60 system. Detailed operational descriptions will be discussed for the following items:

KY11-P Programmers' Console
Power-Up
Starting and Stopping
Functions of Indicators and Switches
Console Internal Registers

Items pertinent for operating the system efficiently will be discussed briefly after the console section. These paragraphs will also include information for locating detailed descriptions.

3.2 KY11-P CONSOLE

The KY11-P programmers' console (Figure 3-1) is used for both computer operation and maintenance. Within the maintenance function, the console supplements other PDP-11/60 features such as single clock, microbreak, processor error log, error status registers, and device-specific macrodiagnostics. Microdiagnostics are also available with the PDP-11/60 via the diagnostic control store (KU116-BB) module.

3.2.1 Functions of Switches and Indicators

3.2.1.1 Octal Display – The octal display is a 6-digit, seven segment display used to display address or data information. The display allows 18 bits (octally coded) to be displayed. For (L)ADRS, (D)ADRS, and HALT/SI functions, decimal points are displayed in conjunction with the octal numerals to indicate that the displayed number is an address versus data. For all other functions, the information is displayed without decimal points. Display of octal digits, when input from the console's numeric keypad, enter from the right and are left shifted.

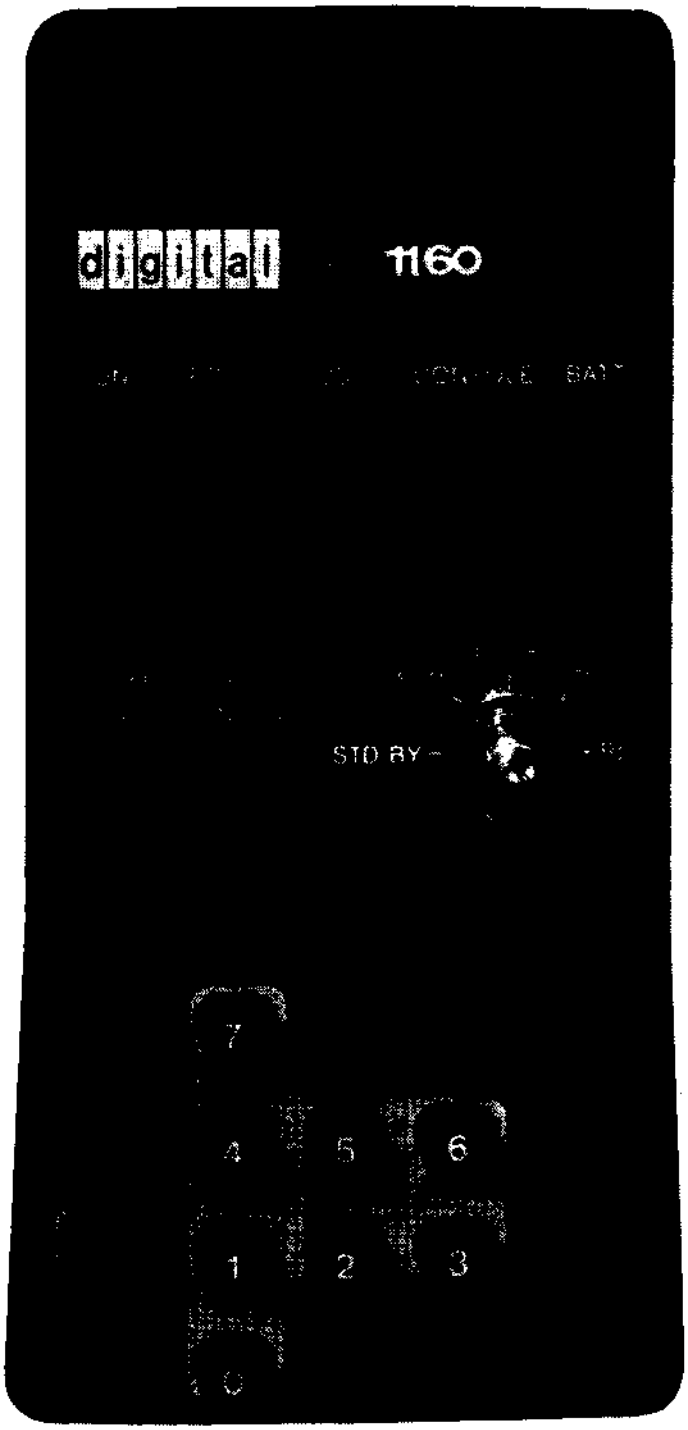
3.2.1.2 Processor State Lights

RUN – If illuminated, indicates that the processor is executing instructions. The light will not remain illuminated during an extended WAIT instruction.

PROC (Processor) – If illuminated, indicates that the processor is the master device and has control of the Unibus.

USER – If illuminated, indicates that the processor is in user mode and certain restrictions on instruction operation and processor status (PS) word loading exist.

CONSOLE – If illuminated, indicates that the processor is in console mode under control of the console keypad switches (manual operation).



8368-2

Figure 3-1 KY11-P Console

BATT (Battery) - Battery monitor indicator. This indicator will function only in machines containing the battery backup option and has the following four states:

OFF – Indicates either no battery present, or battery depletion if battery is present.

ON (continuous) - Indicates that battery is present and is charged.

Flashing (Slow) - Indicates battery is charging.

Flashing (Fast) - Indicates loss of power and battery is discharging while maintaining MOS memory contents.

3.2.1.3 BOOT/RUN/HALT Slide Switch – Power-up action is determined by this switch's position, in conjunction with PANEL LOCK status. If the rotary switch is in LOCK position (deactivating all keypad functions), inadvertent operation of the slide switch has no effect. Upon power-up, the slide switch is treated as if it were in the RUN position, regardless of its physical position. If the battery is depleted (MOS memory system), RUN is altered to a BOOT action.

If the console is not in LOCK position, and power fail occurs, three choices of recovery (BOOT, RUN, and HALT) are available.

BOOT - Power-up to the M9301-YH bootstrap terminator.

RUN - Power-up to location 24, which contains the power-up vector. Note that this action occurs independent of battery status on a MOS memory system.

HALT - Power-up to the console. The CONSOLE light is illuminated and the console keypad switches are active.

3.2.1.4 Rotary Switch
STD BY – Removes dc power from processor and core memory (MOS memory battery charger is still on) and removes dc power from switched outlets (used for peripherals included in the system) on the 866D power controller.

POWER – Applies power to all units. All console controls are operable in console mode.

LOCK – Deactivates all keypad functions. With power switch in LOCK position, the position of the BOOT/RUN/HALT slide switch has no effect when power-up occurs; it is treated as if it were in the RUN position, unless a battery depletion causes BOOT within a system containing MOS memory.

R1 - Local control is deactivated to allow operation from a remote console. The octal display on the console will be blanked.

R2 - Console action is the same as R1.

3.2.1.5 Keypad Switches – The keypad contains twenty switches that are priority encoded into a unique 5-bit code. Simultaneous operation of the keys will allow the operation of the switch with the higher priority. The following paragraphs list the switches in order of their priorities with the highest priority listed first.

0–7 NUMERICS – Activation of any of the numeric keys causes the binary value of that key to be entered into the low-order three bits of the Temporary Switch Register (TMPSW). The previous contents are left shifted three bits. Each 3-bit binary value is displayed in octal. For each additional numeric key pressed, the TMPSW (one of four internal registers) is left-shifted three bits and the octal display is left-shifted one digit. Consequently, a 6-digit octal number is generated as octal digits enter from the right and are left-shifted. Operation of the numerics occurs in both console mode and run mode.

NOTE

The CNTRL (control) key is used in conjunction with some keys to prevent accidental operation of certain functions. When used, the CNTRL key must be pressed first and held down while the other key is pressed. Those keys that are interlocked with the CNTRL key are indicated with an asterisk.

HALT/SI (Halt/Single Instruction – Pressing this switch while the processor is in run mode will halt the processor, between instructions, after outstanding trap sequences and before bus requests. The processor is then put into console mode and the console indicator is illuminated.

The octal display indicates the program counter for both HALT and SINGLE INSTRUCTION functions. Pressing the HALT/SI switch, while in console mode, now causes a single instruction to be executed.

To initialize the system without a program start, it is necessary to press the HALT/SI key while holding the START switch down.

NOTE

The PDP-11/60 differs from other PDP-11 processors regarding the single instruction step function. An operator cannot simply load an address and immediately start single-stepping. To start from an arbitrary address, the program counter (PC) must be loaded using the maintenance key function; one can then single step by pressing the HALT/SI switch. Refer to the MAINT (Maintenance) paragraph for procedures to read from and write into the general-purpose registers.

(D)SWR, *(L)SWR (Display Switch Register, Load Switch Register) – A dual action key, when pressed and not used in conjunction with the CNTRL key the contents of the console switch register (CNSL SWR) are displayed, in both console and run modes.

If this switch is pressed while the CNTRL switch is held, the contents of the TMPSW are loaded into the CNSL SW. The contents of the CNSL SW are displayed. This switch is operative in both console and run modes.

(D)ADRS (Display Address) – Displays the contents of the console address register (CNSL ADRS) and clears the DISLAY LOCK bit, thus enabling the program movements to 777570. Operation occurs in both console and run modes.

NOTE

Console operations are word-ordered operations. If an odd bus address (bit 00 enabled) is used, the odd address is stored in the CNSL ADRS. Examine (EXAM) or deposit (DEP) operations in this address will be treated as word operations (bit 00 ignored).

An EXAM or DEP operation that references a nonexistent address causes the machine to display that address with all the decimal points illuminated. Timeout trap sequences to nonexistent addresses will not be activated.

The following switches are active only in console mode.

(L)ADRS (Load Address) – Pressing this switch transfers the contents of the TMPSW to the CNSL ADRS to be used in subsequent DEP or EXAM operations. The content of the CNSL ADRS is displayed in the octal display and all the decimal points are illuminated.

EXAM (Examine) – Pressing this switch accesses the Unibus address specified in the CNSL ADRS and displays the contents of that address in the octal display. Sequential examines increment the address by two and display the contents of the incremented addresses. This incrementing process is stopped if any other key except numerics is pressed.

DEP (Deposit) – Pressing this switch deposits the contents of the TMPSW at the Unibus address specified by the CNSL ADRS. The CNSL SW is not changed. To deposit data into sequential addresses, all that is necessary is to press the DEP key. This automatically word increments the CNSL ADRS and deposits the data into the incremented address. This process is stopped if any key other than the numeric keys is pressed.

***CONT (Continue)** – Pressing this key allows the processor to leave console mode and continue operation at the present PC location without a BUS INIT. The display is unaltered.

***START** – Pressing this switch begins machine operation at the address (PC) specified by the CNSL ADRS after a BUS INIT signal. Operation occurs only in console mode and the console light is turned off. The display is unaltered.

***BOOT (Bootstrap)** – Pressing this switch will cause a BUS INIT and will start the boot program of the M9301-YH module. The display is unaltered.

***DIAG (Diagnostic)** – Pressing this switch transfers control to the DCS (Diagnostic Control Store) module, if present. Otherwise, the computer enters console mode. The display is unaltered.

***MAINT (Maintenance)** – This key is used to read and write the internal registers. Refer to Paragraph 3.2.5 for procedures for reading and writing general-purpose registers.

3.2.2 Console Internal Registers

The console has the following four internal registers (in the A and B scratchpads) for its own exclusive use. Each is 16 bits wide and has the functions noted below.

3.2.2.1 CNSL CNTL – Console Control, located in the B scratchpad high (R67), is a 16-bit register containing various control bits used in the console microcode. It also contains the upper two bits of the TMPSW, the CNSL SW and CNSL ADRS.

3.2.2.2 CNSL TMPSW – Console temporary switch register, located in the A scratchpad high (R27), is 18 bits wide and is made up of the CNSL TMPSW register and two bits in the control register. The TMPSW is used as a buffer to collect the numerics and is also used for display.

3.2.2.3 CNSL ADRS – Console address register, located in the A scratchpad high (R23), is also 18 bits wide and is composed of the CNSL ADRS register and two bits in the CNSL CNTL to allow 18-bit physical addresses.

3.2.2.4 CNSL SW – Console switch register, located in the A scratchpad high (R26), is also 18 bits wide and is composed of the CNSL SW register and two bits in the CNSL CNTL register. This register has a Unibus address of 777570. If a write is attempted at this address, the data will be written in the CNSL ADRS and then displayed on the console if the DLOCK bit in the CNSL CNTL is not set. This bit is cleared in the (D)ADRS and START functions and set in every other function. (D)ADRS can be used to unlock the display and provide a positive indication of movements by the program to 777570.

3.2.3 Power-Up

Power is turned on by turning the rotary switch to POWER. What occurs after power-up depends on the position of the BOOT/RUN/HALT slide switch prior to the power-up. The slide switch allows three modes of power-up: BOOT, RUN, and HALT.

BOOT – This position allows the system to boot directly from the bootstrap loader (M9301-YH). The boot is accomplished by selecting the device to be bootstrapped by microswitches on the M9301-YH, placing the slide switch in BOOT position and turning the rotary switch to POWER.

RUN – This position allows automatic restart on power-fail recovery. Power-up is to location 24 for automatic restart and occurs except in a MOS memory system where the battery is depleted or absent; in that case, a boot occurs.

HALT – This position allows the use of the console keypad after power-up.

NOTE

To initialize the computer, press the HALT/SI key while holding the START key down. The user should have the slide switch in the desired position, as the slide switch is examined during the initialization. This can be used to clear a hung bus without turning power off.

3.2.4 Starting and Stopping

If it is desired to start a program from a given address, turn the power on after placing the slide switch in the HALT position. The keypad is active and the desired address can be loaded into the TMPSW (and also in the display) by pressing the numeric switches. After checking the desired address as displayed, press the (L)ADRS key. Then press START, holding the CNTRL key down. This starts the program. The CONSOLE light goes out and the RUN light comes on (system is in run mode). The only keys that are active are the numerics, (D)ADRS, D/LSWR, and HALT/SI.

To terminate the execution of a program, press the HALT/SI key. This stops the program, the CON SOLE light comes on, and the RUN light goes out. The system is in console mode and all the keys in the keypad are active. The display contains the PC. In this mode of operation, a single instruction is executed each time the HALT/SI key is pressed.

3.2.5 MOS Configured Systems Power-Down Procedure

To power down systems that are configured with MOS memory (MF11S-KF) the following procedure must be performed:

1. Turn rotary key on console to STD BY.
2. Turn circuit breaker on H775 to OFF.
3. Turn main circuit breaker on 866 to OFF.

3.2.6 Reading and Writing General-Purpose Registers (R0–R7)

The procedures for reading and writing general-purpose registers (GPRs) are as follows. The function codes for the GPRs are listed in Table 3-1.

NOTE

The reading and writing of PDP-11/60 GPRs is not accomplished in the same manner as performed in previous PDP-11s. For example, RO, in previous PDP-11s, could be written into or read from by keying in 777700. To perform the same function in the PDP-11/60, with its calculator style console, a multiple step procedure is required. Refer to the following procedures for reading and writing GPRs.

Table 3-1 GPR Read/Write Function Codes

Register	Read/Write Code
RO	000/200
R1	001/201
R2	002/202
R3	003/203
R4	004/204
R5	005/205
R6	006/206
R7	007/207

3.2.6.1 Read GPR Procedure

CAUTION

Altering any of the internal registers, reserved for maintenance, through the use of the MED procedure, may affect constants used by the processor. Refer to the *PDP-11/60 Computer Manual* for detailed information on the internal registers.

1. Load the TMPSW with the read function code of the register that is desired to be read (Table 3-1).

2. Press the (L)SWR keypad switch while holding in the CNTRL key. This transfers the contents of the TMPSW to the CNSL SW.

3. Press the MAINT key while holding in the CNTRL key. The console display will display the contents of the register specified by the function code in step 1.

3.2.6.2 Write GPR Procedure

1. Load the TMPSW with the write function code of the register that it is desired to write (Table 3-1).

2. Press the (L)SWR key while holding in the CNTRL key. This transfers the contents of the TMPSW to the CNSL SW.

3. Load the TMPSW with the data to be written by pressing the applicable numeric keys.

4. Press the MAINT key while holding in the CNTRL key. The console display will display the data that has been written into the specified register.

3.3 NOTES ON OPERATION

3.3.1 Instruction Set, Addressing Modes, and Programming Techniques

These elements of the PDP-11/60 system remain unchanged from previously developed PDP-11s, and discussions on these subjects can be found in the *PDP-11/60 Processor Handbook*. The following paragraphs briefly introduce the instruction set specifications, and the major instruction formats, with general descriptions of addressing modes used.

3.3.1.1 Addressing Modes – PDP-11 addressing modes include sequential addressing forwards or backwards, address indexing, indirect addressing, 16-bit word addressing, 8-bit byte addressing, and stack addressing. Variable length instruction formatting allows a minimum number of bits to be used for each addressing mode. This results in efficient use of program storage space.

Data stored in memory must be accessed and manipulated. This handling of data is specified by a PDP-11 instruction (MOV, ADD, etc.), which usually indicates:

- The function (operation code)
- A GPR to be used when locating the source operand and/or a GPR to be used when locating the destination operand
- An addressing mode [to specify how the selected register(s) is/are to be used].

3.3.1.2 Instruction Set – The specification for each instruction is shown in the *PDP-11/60 Processor Handbook*. Each specification includes mnemonic, octal code, binary code, a diagram showing the format of the instruction, a symbolic notation describing its execution and the effect of the condition codes, timing information, a description, special comments, and examples.

3.3.2 Programmer's Console Operation Examples

The following procedures implement all of the functions necessary to enter and verify data through the console using simple programs. The end results of the programs are not important; the fact that the programs allow the user to operate each switch/indicator on the console is. Refer to Table 3-2 if console procedures are known.

Table 3-2 Programs Numbers 1 and 2 at a Glance

Program No. 1

Memory		Register	
Loc.	Content	R No.	Content
000	010021	R0	000000
002	000112	R1	000006
004	001000	R2	000000
		R6	000404
		R7	000000

Program No. 2

Memory		Register	
Loc.	Content	R No.	Content
200	062700	R0	000010
202	000010		
204	010037		
206	177570		
210	000000		

3.3.2.1 Memory Loading Procedure for Program No. 1

1. Press numeric key 0. In this program, memory location 000 000 is used as the starting address. Pressing the 0 key, loads the TMPSW and displays the number.

> **NOTE**
> **The processor must be halted if any of the processor state lights are on, other than the CONSOLE indicator. Before proceeding to the next step, ensure that the processor is in console mode. Pressing the HALT/SI key, while the processor is in run mode, will halt the processor and the CONSOLE indicator will light. Repeat Step 1 if this is the case.**

2. Press the (L)ADRS key. Decimal points will appear throughout the 6-digit number. This action causes the 6-digit number to be transferred from the TMPSW to the CNSL ADRS to be used in subsequent EXAM and DEP operations.

3. Press the numeric keys, 0–1–0–0–2–1. Again, loading the TMPSW and displaying the number, visually check the display for correct order of numbers.

4. Press the DEP key. This action deposits the contents of the TMPSW (Step 3) at the Unibus address (Step 1) specified by the CNSL ADRS (Step 2).

5. Press the numeric keys, 0–0–0–1–1–2. Visually check display for correct order.

6. Press the DEP key.

NOTE

Pressing the DEP key, in Step 4, automatically word incremented the CNSL ADRS. (The CNSL ADRS contained all zeros before Step 4's operation, see Steps 1 and 2. Following Step 4's DEP action, it contained address 000002. Following Step 6's DEP action, it contained address 000004.) Therefore, there is no need to perform the load address procedure conducted in Step 1, when the next memory location is required.

7. Press the numeric keys 0–0–1–0–0–0.

8. Press the DEP key.

3.3.2.2 Register Loading Procedure for Program No. 1 – The GPRs, loaded from the console, will contain data or memory address locations that will be used by the program to execute its instructions.

1. Press the numeric keys 2–0–0. (This indicates the write function code for register 0. It will be loaded into the TMPSW and displayed in the octal display.)

2. Press the (L)SWR key while holding in the CNTRL key.

3. Press the numeric key 0, loading the TMPSW and displaying all zeros. (In this program, R0 contains data.)

4. Press the MAINT key while holding in the CNTRL key. (This action deposits the previously entered zeros, Step 3, into R0.)

5. Enter the write function code of register 1 (R1) by pressing numeric keys 2–0–1.

6. Press the (L)SWR key while holding in the CNTRL key. (This action loads the contents of the TMPSW, Step 5, into the CNSL SW; preparing R1 to receive data.)

7. Press numeric key 6. (In this program, R1 contains a memory address.)

8. Press the MAINT key while holding in the CNTRL key.

9. Enter the write function code for R2, by pressing numeric keys 2–0–2 (check that the write function code for R2 is correct by referring to Table 3-1).

10. Press the (L)SWR key while holding in the CNTRL key.

11. Press the numeric key 0, loading the TMPSW and displaying all zeros.

12. Press the MAINT key while holding in the CNTRL key.

13. Enter the write function code for R6, by pressing numeric keys 2–0–6.

14. Press the (L)SWR key while holding in the CNTRL key.

15. Press the numeric keys 4–0–4.

16. Press the MAINT key while holding in the CNTRL key.

3.3.2.3 Memory Checking Procedure for Program No. 1

1. Press the numeric key 0, loading the TMPSW and displaying all zeros.

2. Press the (L)ADRS key, transferring the contents of the TMPSW to the CNSL ADRS.

3. Press the EXAM key. (The contents of memory location 000 000 will be displayed in the octal display. It should be 010021.)

> **NOTE**
> **EXAM operations automatically word increment the CNSL ADRS, in the same manner as DEP operations; see the note following Step 6 in the memory loading procedures.**

4. Press the EXAM key again. The contents of memory location 000002 will be displayed. It should be 000112.

5. Press the EXAM key again. The contents of memory location 000004 will be displayed as 001000.

3.3.2.4 Register Checking Procedure for Program No. 1

1. Press the numeric key 0. This displays all zeros in the octal display, indicating the read function code for R0 (Table 3-1).

2. Press the (L)SWR key while holding the CNTRL key.

3. Press the MAINT key while holding the CNTRL key. The contents of R0 will be displayed as all zeros.

4. Press the numeric key 1, displaying the read function code for R1.

5. Press the (L)SWR key while holding in the CNTRL key.

6. Press the MAINT key while holding in the CNTRL key. The contents of R1 will be displayed as 000006.

7. Perform the same procedure, Steps 1, 2, and 3, for reading the contents of R2 and R6; refer to Table 3-1 for the read function codes of these two registers.

3.3.2.5 Starting Procedure for Program No. 1 – Now that the program has been loaded and verified, perform the following procedure to try to run it.

1. Press numeric key 0, loading the TMPSW and displaying all zeros.

2. Press the (L)ADRS key, transferring the contents of the TMPSW to the CNSL ADRS. Decimal points will be displayed along with the contents of the CNSL ADRS (all zeros).

3. Press the START key while holding in the CNTRL key.

We have just deposited zeros into every memory location, accessible to the user, except for locations 0, 2, 4, 400 and 402 were loaded with zeros and then modified by the error trap. Refer to Figure 3-2 for the contents of these memory addresses and for the "Before" and "After" contents of the GPRS used in this program.

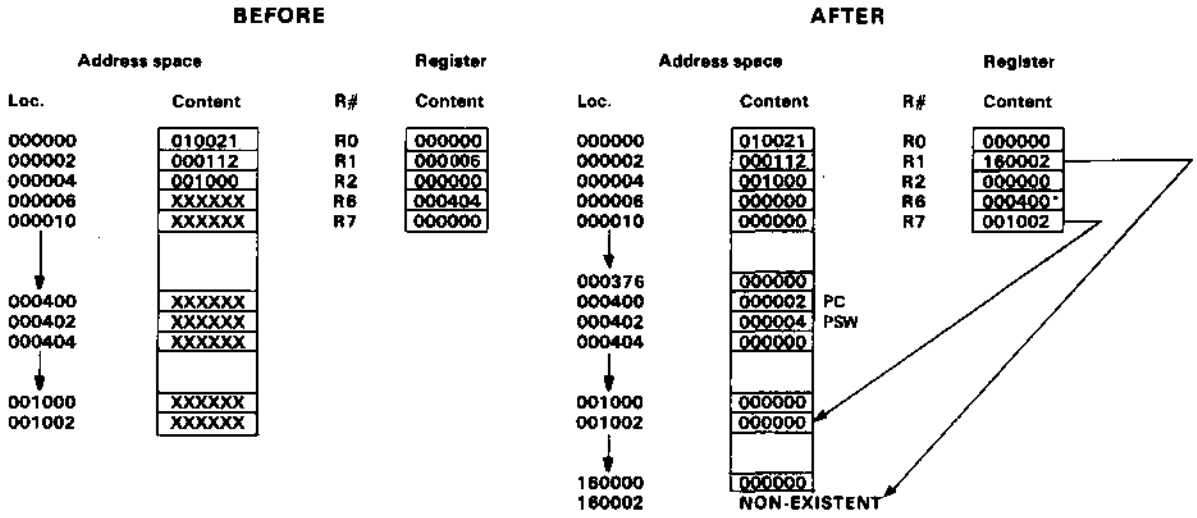


Figure 3-2 Before and After Contents of Memory Addresses and GPRs from Program No. 1

3.3.2.6 Single Step Procedure for Program No. 1 – If the program has already been run, Paragraph 3.3.2.5, reload R1, R6, and R7.

1. Press the numeric keys 2–0–1.
2. Press the (L)SWR key while holding in the CNTRL key.
3. Press the numeric key 6.
4. Press the MAINT key while holding in the CNTRL key.
5. Press the numeric keys 2–0–6.
6. Press the (L)SWR key while holding in the CNTRL key.
7. Press the numeric keys 4–0–4.
8. Press the MAINT key while holding in the CNTRL key.
9. Press the numeric keys 2–0–7.
10. Press the (L)SWR key while holding in the CNTRL key.
11. Press the numeric key 0, loading the TMPSW and displaying all zeros.
12. Press the MAINT key while holding in the CNTRL key.

NOTE

Entering all zeros in R7 (Steps 9, 10, 11, and 12) caused the PC to point at the starting address of our program. This is necessary to single step the instructions of any program.

13. Press the HALT/SI key.

NOTE

The processor has just performed the move instruction (010021) that was contained in memory address 000000, refer to the note preceding Step 13. 0.0.0.0.0.2 will be displayed; this is the address to which the PC is now pointing. When the HALT/SI key is pressed again, the processor will have performed the jump instruction (000112) contained in that memory location. Since the instruction says to jump to the address specified in R2, the PC (R7) will contain all zeros (contents of R2) and the display will contain all zeros.

To determine that the move instruction has been performed, read the contents of R1, (Steps 4, 5, and 6 in Paragraph 3.3.2.4). The contents will have incremented from 000006 to 000014.

3.3.2.7 Continue Procedure for Program No. 1 – This program can be run, in its entirety, from its present location, without beginning at the starting location by pressing the CONT key while holding in the CNTRL key. The same results as shown in Figure 3-2 will occur, as if we had begun at the starting location with the contents of R1 being memory address 000012.

3.3.2.8 Memory Loading Procedure for Program No. 2 – Refer to Table 3-2 if console procedures are known.

1. Press numeric keys 2–0–0.
2. Press the (L)ADRS key.
3. Press numeric keys 0–6–2–7–0–0.
4. Press the DEP key.
5. Press the numeric keys 1–0.
6. Press the DEP key.
7. Press the numeric keys 0–1–0–0–3–7.
8. Press the DEP key.
9. Press the numeric keys 1–7–7–5–7–0.
10. Press the DEP key.
11. Press the numeric key 0.
12. Press the DEP key.

3.3.2.9 Register Loading Procedure for Program No. 2

1. Press the numeric keys 2–0–0.
2. Press the (L)SWR key while holding in the CNTRL key.
3. Press the numeric keys 1–0.
4. Press the MAINT key while holding in the CNTRL key.

3.3.2.10 Memory Checking Procedure for Program No. 2

1. Press numeric keys 2–0–0.
2. Press the (L)ADRS key.
3. Press the EXAM key, 062700 should be displayed.
4. Press the EXAM key, 10 should be displayed.
5. Press the EXAM key, 010037 should be displayed.
6. Press the EXAM key, 177570 should be displayed.
7. Press the EXAM key, all zeros should be displayed.

3.3.2.11 Register Checking Procedure for Program No. 2

1. Press numeric key 0.
2. Press the (L)SWR key while holding in the CNTRL key.
3. Press the MAINT key while holding in the CNTRL key, 000010 should be displayed.

3.3.2.12 Starting Procedure for Program No. 1

1. Press numeric keys 2–0–0.
2. Press the (L)ADRS key.
3. Press the START key while holding in the CNTRL key.

NOTE

The display should contain the next memory address following the last instruction. The last instruction being located in memory address 210; the PC should be pointing at location 212.

4. Press the (D)ADRS key. This action displays the result of the program.

3.3.2.13 Console Switch Register Read/Write* Procedure – The address 177570 is the CNSL SW's Unibus address. To write in this address, from the console, the following procedure must be performed:

1. Load the TMPSW with the data to be written by pressing the applicable numeric keys.
2. Press the (L)SWR key while holding in the CNTRL key.
3. Press the numeric keys 7–7–7–5–7–0.
4. Press the (L)ADRS key.
5. Press the EXAM key.

The number you loaded in Step 1 should be displayed in the octal display. Figure 3-3 is a block diagam of the console registers (TMPSW, CNSL ADRS, CNSL SW, etc.) transfer process. For more detailed programming information, refer to the *PDP-11/60 Processor Handbook*.

*The console switch register cannot be written into via the conventional method (i.e., Load Address, Deposit, etc.). The first two steps of this procedure automatically load the console switch register. Steps 3, 4, and 5 are for reading the register.

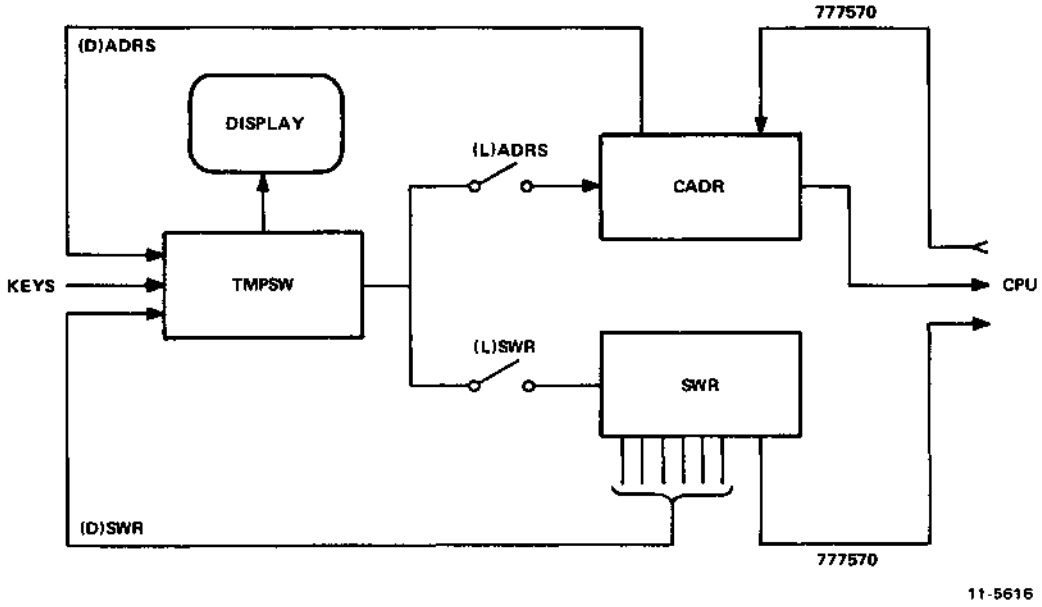


Figure 3-3 Console Registers Flowchart

CHAPTER 4
PDP-11/60 BACKPLANES

This section describes the backplanes of the PDP-11/60. The three backplanes described are the KD11-K Backplane, the MF11-WP Core Memory Backplane, and the MF11S-KF MOS Memory Backplane. An understanding of this section's contents requires that the user have a general knowledge of digital circuitry and a basic understanding of the PDP-11/60 computer. The PDP-11/60 Processor Handbook and the PDP-11 Peripherals Handbook will be valuable as references.

4.1 INTRODUCTION

There are two types of backplanes on the PDP-11/60; the processor backplane and the memory backplane. The KD11-K Processor Backplane is designated 70-12953. This backplane can be accompanied by one of two different memory systems in the 11/60; the MF11S-KF MOS Memory System and the MF11-WP Core Memory System. The MF11S-KF MOS Memory System uses a specially designed DD11-K backplane while the MF11-WP uses a 70-09295 backplane assembly.

Each module, which has its own purpose in the operation of the computer, has its own place on the backplane. Failure to plug a module into the correct slot can lead to a malfunction requiring module replacement. The following paragraphs and figures describe the correct module configurations that should be used with each backplane.

4.2 KD11-K PROCESSOR BACKPLANE

4.2.1 Module Utilization

The KD11-K processor backplane (70-12953) is a 14-slot backplane with each slot containing six two-sided connectors labeled A thru F with A on top. This backplane contains slots for the entire KD11-K processor including cache memory, the optional floating point and control store modules, Unibus cables or terminators, and peripheral controller modules. Figure 4-1 shows the module utilization chart for the KD11-K.

The KD11-K basic processor is contained in slots 2 thru 7 of the processor backplane. The modules are, respectively, the M7872 Microword Module, the M7873 Decode Module, the M7874 Data Path Module, the M7875 KT/Cache Module, the M7876 Timing Module, and the M7877 Status Module. Other basic processor modules include the M9302 Terminator Module in slot 14 rows A and B, the M9301-YH Bootstrap Terminator Module in slot 13 rows A and B, and the M7856 DL11-W Serial Line Unit/Real-Time Clock Module in slot 14 rows C–F.

The main optional modules deal with floating point and control store. The floating point capability of the 11/60 is housed in modules which plug into slots 8 thru 11 of the backplane. The modules are, respectively, the M7878 Floating Point Next Microaddress (FNUA) Module, the M7879 Floating Point Exponent (FLTEXP) Module, the M7880 Multiplying Network (MULNET) Module, and the M7881 Floating Point ALU (FALU) Module. The optional control store modules, of which only one can be used at a time, plug into slot 1 of the backplane. The modules that may be used are either the M7870 Writable Control Store, the M7871 Diagnostic Control Store, or the M7871-YA Extended Control Store.

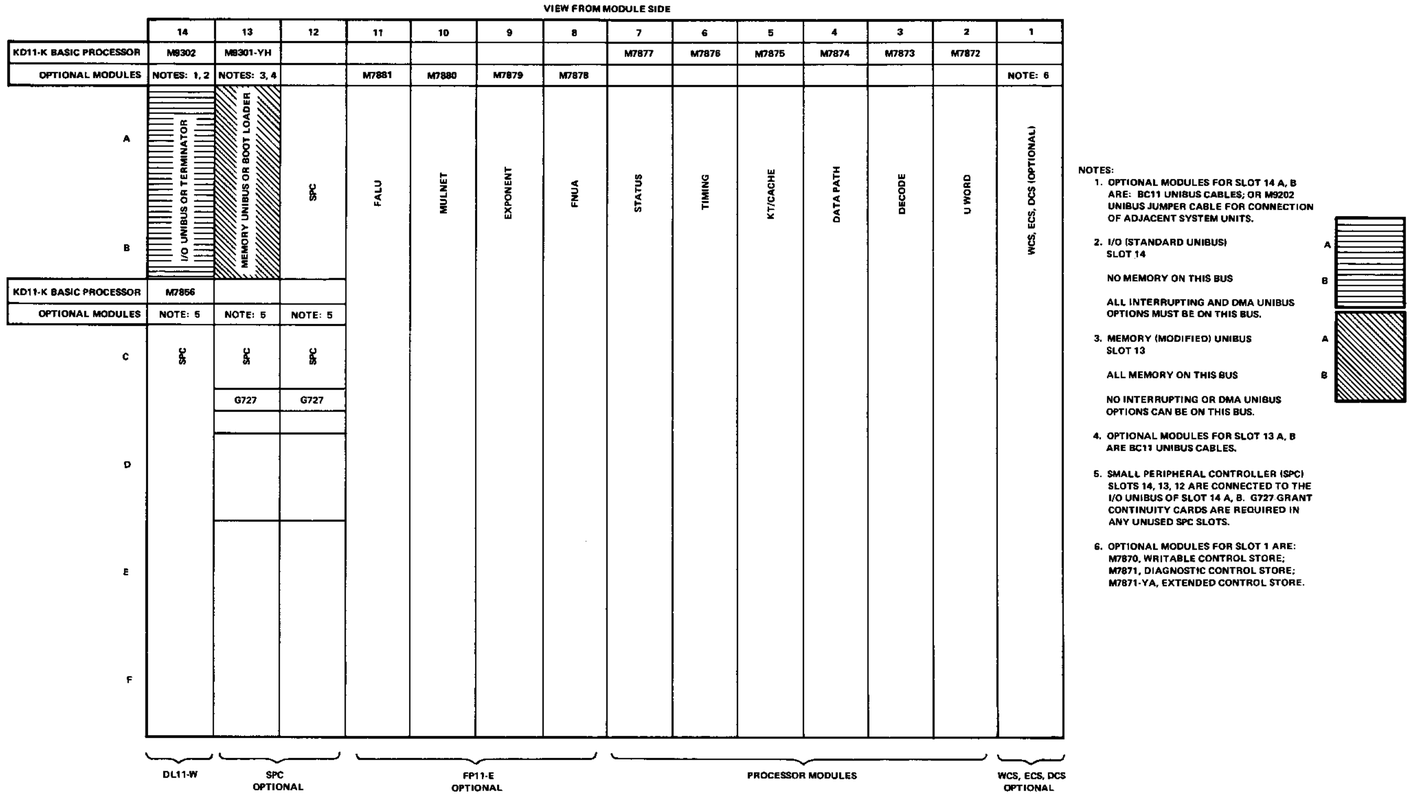


Figure 4-1 KD11-K Module Utilization

Slots 13 and 14 rows A and B can be used as Unibus cable slots if it is not desired to terminate the Unibus at the end of the processor section. Slot 13 is a memory Unibus slot while slot 14 is an I/O Unibus slot. The cables that may be used in slot 14 are a BC11 Unibus cable or a M9202 Unibus jumper cable to connect the adjacent system units. Only the BC11 Unibus cable may be used for this purpose in slot 13.

After the backplane has been configured with the above required and optional modules, the leftover slots in 12, 13, and 14 may be used for any Small Peripheral Controller (SPC) Modules. The modules in the SPC family of options have common backplane pinning and can therefore be installed in any slot designated SPC. The slots into which they are plugged are connected to the I/O Unibus of slot 14 rows A and B. If the SPC slots are not used for SPC modules, then G727 Bus Grant Modules must be inserted in the vacant slots.

4.2.2 Backplane Wiring

Sometimes the wiring etched into the back of the backplane isn't enough to interconnect the various modules. In these cases, external wire wraps connecting the pins on the backside of the backplane must be used. Some of these wires are machine wrapped at manufacturing time. Others must be added as various options are added. For a listing of wire wrap placements refer to the wire list, K-WL-KD11-K-1.

DC power is supplied to the backplane from the base (upper) H7420 power supply. From the H7420 it is routed over power harness 70-12926 through five regulators to solder points on the Power Distribution Board (54-12478), which is located on the top of the backplane (Ref. D-CS-BA11-P-3). Harnesses that are plugged into connectors on the Power Distribution Board then carry power to solder points on the back of the backplane (Ref. Print D-IA-70-12953-0-0). For more information concerning power supply to the backplane refer to the PDP-11/60 Cabinet and Power Supply Manual.

4.2.3 Backplane Pins On Slot 12

MOS power discharged signal on D07V2 comes from power distribution board, on wire listing it is called DISCHARGED L. On the module it is tied to +5 via 1K.

Knowledge of required voltages is needed when putting hex height SPCs in Slot 12. Many pins are not tied in, for instance the following pins are not used:

A12 B2	B12 A1
A12 N1	B12 B1
A12 P1	B12 B2
A12 R1	B12 D1
A12 S1	B12 E1
A12 U1	B12 E2
A12 V1	B12 U1
A12 V2	B12 V2

The following hex height SPCs cannot utilize Slot 12: DF11, DFC11 and all Communication Controllers.

4.3 MF11S-KF MOS MEMORY BACKPLANE

4.3.1 Module Utilization

A MF11S-KF MOS Memory System contains 32K words with single-bit error correction and double-bit error detection. The system can accommodate four of these 32K word modules in one DD11-K backplane. This provides a maximum of 128K words.

The DD11-K MOS Memory Backplane is a 9-slot backplane. Each slot is made up of six connectors labeled A thru F. The modules which plug into these slots contain memory arrays and controllers as well as Unibus cables and terminators. Figure 4-2 shows the MF11S-KF backplane module utilization.

The M7984 MOS memory array module will fit in slots 4 thru 7 of the DD11-K backplane. The M7983 Controller, however, must be placed in slot 8. The array slots are dedicated according to memory size. The first 32K of memory is plugged in slot 7, the second in slot 6, the third in slot 5, and the fourth in slot 4. Slot 1 must be used for the Unibus cable-in jumper. Slot 9 must contain either a Unibus cable-out jumper or a terminator.

NOTE

When the MF11S-K memory is used in the PDP-11/60, small peripheral controllers (SPCs) cannot be used in the DD11-K backplane.

4.3.2 Backplane Wiring

For a listing of MF11S-KF backplane wire wrap placements refer to print K-WL-7013542-0-1.

4.4 MF11-WP CORE MEMORY BACKPLANE

4.4.1 Module Utilization

A MF11-WP Core Memory System provides 32,768 (32K) 18-bit words including two parity bits per word. The 11/60 can accommodate up to four of these systems. One backplane can accommodate up to 64K words, or two systems. Another backplane can be added, though, to bring the total capacity up to 128K words.

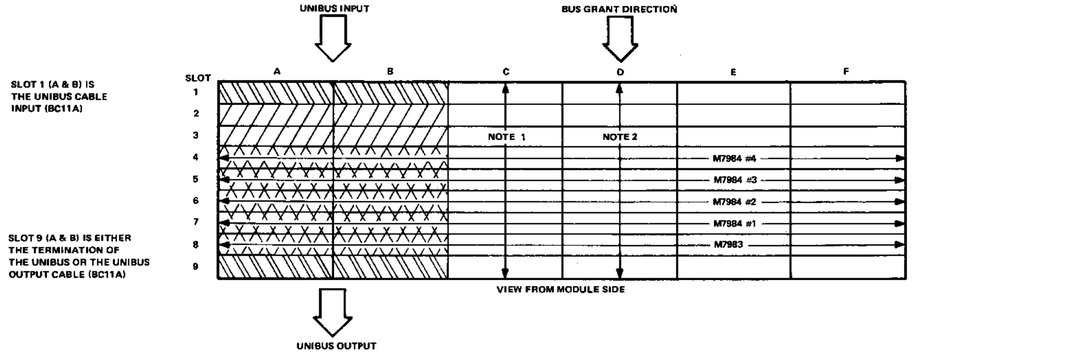
The MF11-WP Core Memory Backplane Assembly (70-09295) is a 9-slot backplane. Each slot is made up of six connectors labeled A thru F. The modules which plug into these slots contain either the physical cores or their supporting logic including drivers, inhibitors, sensors, timers and parity controllers. Figure 4-3 shows the module utilization chart for the MF11-WP.

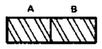
Each memory system consists of a M8294 32K Unibus Timing and Control Module, a G116 Sense/Inhibit Module, a H224C Memory Stack Module and a G236 X/Y Driver Module. If only one 32K system is used then these modules are plugged into slots 9, 8, 7, and 6, respectively. If a second 32K system is used the modules are plugged into slots 1, 3, 4, and 5, respectively.

The presence of some modules are required regardless of whether one or two systems are being plugged into the backplane. The M7259 Parity Control Module must be plugged into the backplane. The M7259 Parity Control Module must be plugged into slot 12 rows A and B. A BC11-A Unibus cable is plugged into slot 1 rows A and B. If the memory system is to be the last device on the Unibus then a M930 Terminator is inserted in slot 9 rows A and B. If the MF11-WP is not the last device on the bus, a M9302 Unibus jumper cable or a BC11-A Unibus cable must be inserted in that slot to continue the Unibus.

4.4.2 Backplane Wiring

For a listing of MF11-WP backplane wire wrap placements refer to print D-AD-7009295-0-0.



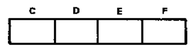


STANDARD UNIBUS
(SLOT 1 & 9)

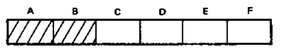
DUAL MODULES WHICH PLUG INTO STANDARD UNIBUS SLOTS ONLY:
BC11A UNIBUS CABLE
M9302 SACK/TERM (NOTE 5)
M920 (NOTE 4)
M930 (NOTE 5)
M9202 (NOTE 4)

MODIFIED UNIBUS
(SLOT 2 & 3)

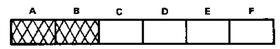
DUAL MODULES WHICH PLUG INTO THE MODIFIED UNIBUS ONLY:
M9301 BOOT/TERM
M9306 TERM.
M7850 PARITY CONT.



SMALL PERIPHERAL CONTROLLER
(SLOT 1-9)
ANY S.P.C. OPTION (N/A ON 11/60).



HEX MODULE WITH MODIFIED UNIBUS SIGNALS
(SLOTS 2 & 3)



MS11-K INT. BUS
(SLOTS 4-8)

HEX MODULES WHICH PLUG INTO INT BUS SLOTS ONLY:
M7893 MF11S-K CONTROLLER
SLOT 8 ONLY
M7984 MS11KA ARRAY MODULE

SLOT 7	1ST	32K
SLOT 6	2ND	32K
SLOT 5	3RD	32K
SLOT 4	4TH	32K

IF A 16K INCREMENT IS REQUIRED, THEN AN MS11-KB MUST BE AT THE TOP OF EXISTING MEMORY. THERE CAN ONLY BE ONE MS11K-B IN A SYSTEM.

NOTES:
1. G727 REQUIRED IN ANY UNUSED SPC SLOT (CONNECTOR D) TO PROVIDE BUS GRANT CONTINUITY.
2. GRANT DIRECTION IS SLOT 1 TO SLOT 9.
3. USE M9202 TO INTERCONNECT SYSTEM UNITS INSTEAD OF M920. M9202 IS A 2 FT. UNIBUS JUMPER CABLE USED TO DISTRIBUTE UNIBUS LOADING.
4. M9302 (SACK/TERM) AND M930 (TERM) MUST NEVER BE INSTALLED IN ANY SLOT OTHER THAN SLOT 9 (A & B). POWER SUPPLY VOLTAGE WILL BE SHORTED OUT IF THESE TERMINATORS ARE MOUNTED IN THE MODIFIED UNIBUS SLOTS.
5. MODIFIED UNIBUS SECTION CARRIES CORE AND MOS MEMORY VOLTAGE TAILS AND MEMORY PARITY CONTROL SIGNALS INSTEAD OF BUS GRANT AND SOME GND SIGNALS THAT ARE CONTAINED IN STANDARD UNIBUS SLOTS.
6. THE +5 V AND GROUND PINS ON CONNECTORS A & B, SLOTS 2 THRU 8, THAT CAN BE USED BY HEX MODULES OTHER THAN THE MF11S-K SYSTEM ARE:
   +5 V: —AA2, BA2
   GND: —AC2, BC2, AT1, BT1

MA-0545

Figure 4-2 MF11S-KF Module Utilization

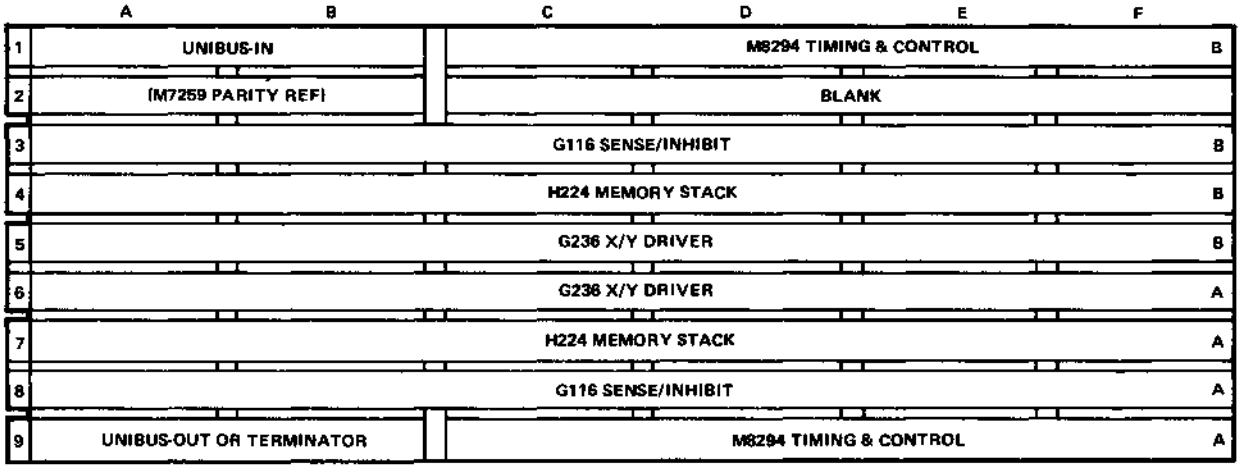


Figure 4-3 MF11-WP Module Utilization

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