EK-KD11Z-TM-001

PDP-11/44 System Technical Manual

digital

EK-KD11Z-TM-001

PDP-11/44
System Technical Manual

digital equipment corporation • maynard, massachusetts

First Edition, December 1980

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

CONTENTS

FIGURES

TABLES

PREFACE

The PDP-11/44 is a midrange computer system which is available in a standard configuration and is expandable by the user to conform to specific user requirements.

This manual defines the standard system and provides the information required to unpack and install the system in a cabinet, and to wire the system for operation. This manual also gives a detailed functional description of the KD11-Z Central Processor used in the PDP-11/44.

Chapter 1, Introduction – Includes a general description of the PDP-11/44 system and the modules supplied with the unit. The chapter also describes the features and capability of the system, the available options, and the equipment specifications, including the power supply.

Chapter 2, Operation – Describes the front panel controls and indicators, the console commands available, and register bit assignments.

Chapter 3, Configuration – Provides the module current requirements and information on placement in the processor backplane, and the switch and jumper lead information required to configure the modules for specific requirements.

Chapter 4, Installation – Provides the information necessary to prepare the installation area, to connect the unit to ac power and to mount the unit into a PDP-11/44 system cabinet or standard 48.26 cm (19 in) cabinet.

Chapter 5, Removal/Replacement Procedures – Describes the procedures required to remove and replace the main units and assemblies and to install additional backplanes for expansion of the system functions.

Chapter 6, Detailed Functional Description – Describes each of the major logic elements of the KD11-Z Central Processor.

CHAPTER 1
INTRODUCTION

The PDP-11/44 processor consists of CPU modules, memory modules, and interface modules enclosed in the BA11-AA or BA11-AB mounting box. The box includes a front control panel and power supply. The mounting box can be installed in a standard 48.26 cm (19 in) rack or cabinet or in a DIGITAL system cabinet.

The PDP-11X44 system consists of the PDP-11/44 processor mounted into the 100 cm (40 in) low-profile, top-loading H9642 cabinet. This cabinet conforms in style to other DIGITAL PDP-11 peripheral unit cabinets.

Figure 1-1 shows several typical PDP-11X44 system configurations that include disk drive units and magnetic tape units. The PDP-11X44 cabinet attaches to the RL02 and RK07 Disk Drive Units and to the TS11 Magnetic Tape Unit.

1.1 GENERAL

The PDP-11/44 and the PDP-11X44 are medium range, general purpose computer systems which operate with 16-bit data words and provide 22 bits for memory addressing. A total of one megabyte of main memory can be included with the system in increments of 256K bytes. The system includes the complete instruction set of the PDP-11/70 processor except for the FD MAINT INST instruction. Two additional instructions, Move From Processor Type (MFPT) and Call to Supervisor Mode (CSM), are included.

The systems also include an 8K byte cache memory and the extended instruction set (EIS). A microprocessor interprets the ASCII codes from the console terminal and allows the functions previously performed at the console switches to be initiated at the console terminal.

A floating-point processor and a commercial instruction set processor are available as options with the system.

The PDP-11X44 system includes a dual TU58 DECtape II cartridge tape unit used to load diagnostic programs and to update software. The following operating software systems are compatible with the PDP-11/44 and PDP-11X44 systems.

Software	Version	Software	Version
RT-11	V4.0	CTS-500	V5.0
RSX-11M	V3.2	DSM-11	V2.0
RSX-11S	V3.2	TRAX	V2.0
RSX-11M+	V1.0	COBOL-11	V4B
RSTS/E	V7.0	MACRO-11	V4.0

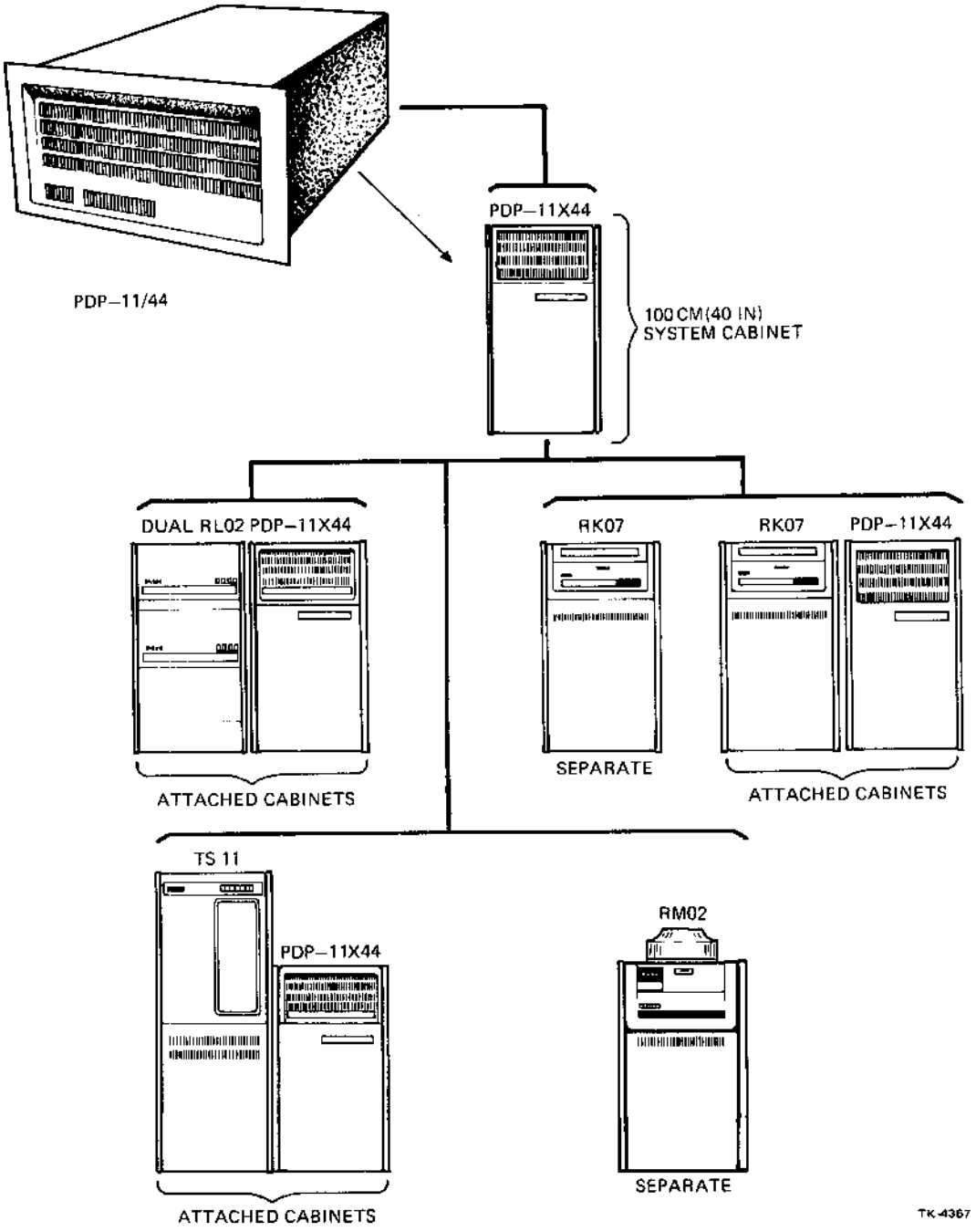


Figure 1-1 PDP-11/44 System Configurations

1.2 EQUIPMENT DESCRIPTION

The PDP-11/44 and PDP-11X44 processor systems are available to operate with either 120 Vac or 240 Vac input power. Table 1-1 lists and describes the components included with each system.

Table 1-1 Processor System Designations

Designation	Description
PDP-11/44-CA	Contains a CPU, 256K bytes of ECC MOS memory, two EIA serial line units, one for the console terminal and one for the TU58 tape transport (not included), BA11-AA mounting box with cabinet, mounting slides and a filter distribution panel. Operates with 120 Vac input power.
PDP-11/44-CB	Same as PDP-11/44-CA except the mounting box is a BA11-AB wired for 240 Vac input power.
PDP-11X44-CA	Same as PDP-11/44-CA except the BA11-AA mounting box is installed in an H9642 system cabinet which includes a dual TU58 tape unit and power control unit for 120 Vac input power.
PDP-11X44-CB	Same as PDP-11X44-CA except it is wired for 240 Vac input power.

1.2.1 PDP-11/44-CA, -CB Processor System

The PDP-11/44-CA, -CB processors are supplied in the BA11-AA, -AB mounting box shown in Figure 1-2. The mounting box contains a 14-slot (column) backplane assembly with the system modules installed, a fan assembly, and an H7140-AA, -AB power supply assembly. The fan assembly contains three fans and provides cooling for the modules and power supply. The fans are mounted on a slide, for ease of removal, and are powered by the power supply. A bezel is attached to the front of the mounting box and contains a control panel and ventilating slots for air circulation. An open-cell foam filter is located directly behind the front bezel and may be easily removed for cleaning.

A control panel, located on the lower section of the front bezel, contains a keyswitch, panel switch, and indicators to select and indicate operating conditions. A removable top and bottom cover is also supplied with the mounting box.

Attached to each side of the mounting box is a slide index plate which allows the unit to be rotated to a vertical position, when the unit is mounted in a cabinet, onto the slides that are provided with the unit. The slide index plates are released by the side pawl retractors also located on each side of the unit, toward the front.

The BA11-AA, -AB box provides a 14-slot CPU backplane and 29 card guides at the front and rear of the unit to allow additional modules to be installed. One DD11-DK 9-slot, double-system unit and one DD11-K single-system unit or three DD11-CK single-system units may be installed and connected directly to the power supply by the cables and connectors attached to the system units. These system units provide additional mounting space for I/O device options.

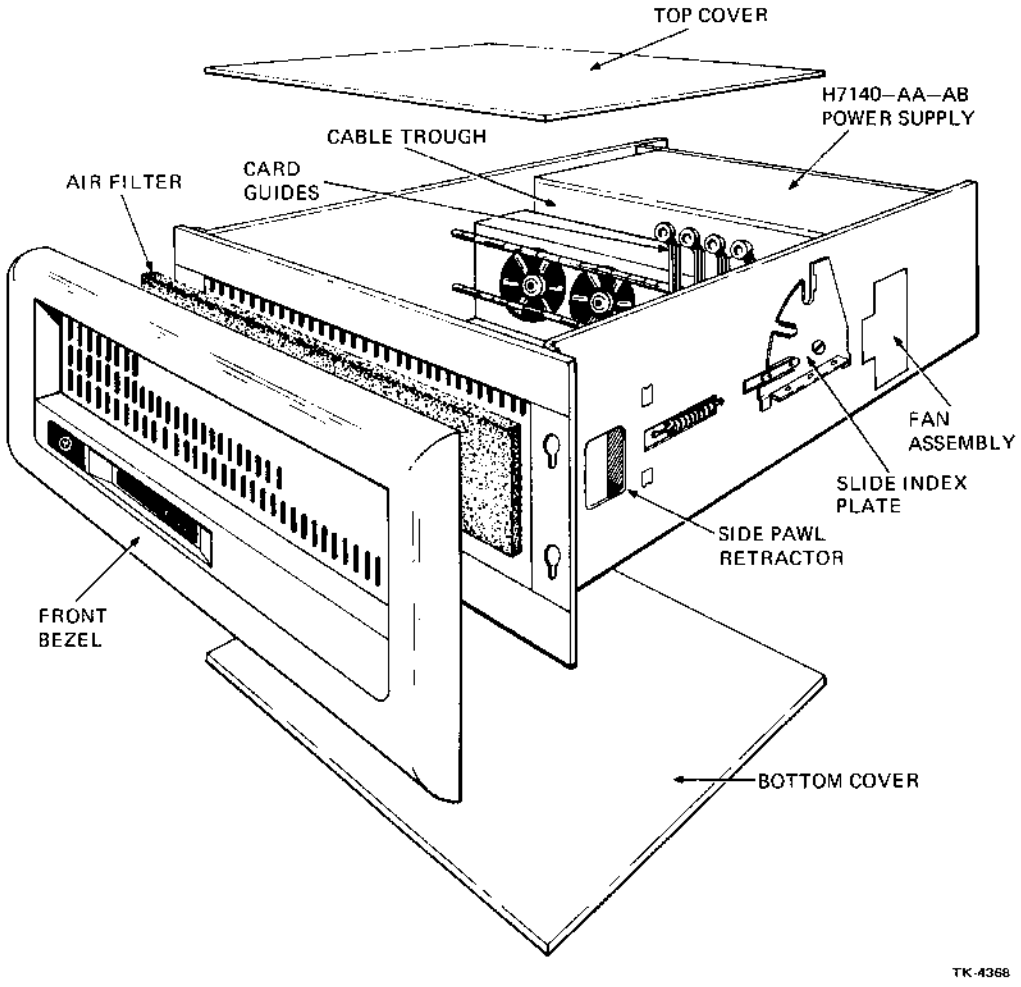


Figure 1-2 PDP-11/44-CA, -CB in Mounting Box

1.2.2 PDP-11X44 Processor System

The PDP-11X44-CA, -CB consists of the components described for the PDP-11/44-CA, -CB which are mounted in a system cabinet as shown on the frontispiece. Mounted below the front bezel is a dual TU58 tape unit which enables the loading of diagnostic programs from cassettes and provides data storage for up to 256K bytes of information.

The BA11-AA, -AB mounting box is attached to the top of the cabinet and can be released and tilted vertically for servicing. When tilted, the mounting box is supported by two gas springs. A hinged panel is provided at the front and the rear of the cabinet to allow access to the power controller unit provided with the cabinet, to the battery backup unit which is supplied as an option, and to the I/O connector panel.

1.2.3 Standard Hardware Components

Table 1-2 lists the standard hardware supplied with each PDP-11/44 system.

Table 1-2 PDP-11/44 Standard Hardware Components

Quantity	Description
1	KD11-Z Central Processor consisting of: (M7090) Console Interface Module (M7094) Data Path Module (M7095) Control Module (M7096) Multifunction Module (M7098) UNIBUS Interface Module
1	MS11-MB ECC MOS Memory (256K bytes)
1	8K byte cache memory on hex-height module (M7097).
1	BA11-AA (120 Vac) or BA11-AB (240 Vac) mounting box with power supply and DD11-DK backplane (70-16502)
1	M9302 UNIBUS Terminator Module
1	M9642 Cabinet (PDP-11/X44-CA, -CB only)
1	TU58 Dual Tape Drive (PDP-11/X44-CA, -CB only)
1	872-D Power Controller Unit (PDP-11/X44-CA, -CB only)
1	I/O Connector Panel

1.2.4 Hardware Options

The standard PDP-11/44 system capabilities can be expanded with the installation of several available hardware options which are listed in Table 1-3.

1.3 EQUIPMENT SPECIFICATIONS

The following paragraphs contain the mechanical/environmental specifications for the PDP-11/44 and PDP-11X44 equipment. Detailed specifications for the peripheral devices supplied with these units are contained in the user's guide associated with the device.

Table 1-3 Hardware Options

Designation	Description
MS11-MB	256K bytes ECC memory on hex-height module
MS11-MC	Same as MS11-MB except 512K bytes on two hex-height modules
MS11-MD	Same as MS11-MB except 758K bytes
FP11-F	Floating-point processor on hex-height module (M7093)
KE44-A	Commercial instruction set processor on a quad-height module (M7091) and hex-height module (M7092)
H7750-BA	Battery backup unit 120 Vac/60 Hz, 240 Vac/50 Hz
H7750-BD	Same as H7750-BA except for 240 Vac/50 Hz
TU58-CA	Dual cassette tape transport
BA11-AE, -AF	Expander box for PDP-11/44 system expansion; includes power supply

1.3.1 PDP-11/44 System Specifications

Table 1-4 lists the equipment specifications for the basic PDP-11/44 unit. When the system is operated with a TU58 DECtape II option, the specifications will be similar to those listed in Table 1-5 for the PDP-11X44 system.

Table 1-4 PDP-11/44-CA, -CB Equipment Specifications

Characteristic	Description
Mechanical	
Overall dimensions (with front bezel)	70.15 cm long × 48.26 cm wide × 26.34 cm high (27.62 in long × 19 in wide × 10.37 in high)
Weight	
Unpacked	32.66 kg (72 lb)
Packed	36.2 kg (80 lb)

Table 1-4 PDP-11/44-CA, -CB Equipment Specifications (Cont)

Characteristics	Description
Environmental*	
Temperature	
Operating	5° C to 50° C (41° F to 122° F)
Nonoperating	–40° C to 66° C (–40° F to 151° F)
Humidity	
Operating	10% to 95% relative (RH) with a maximum wet bulb of 32° C (90° F) and a minimum dew point of 2° C (36° F)
Nonoperating	50% relative (RH) or less to 95% (RH) or less with a maximum wet bulb of 46° C (115° F)
Vibration	
Operating	5 to 22 Hz: 0.01 in DA; 22 to 500 Hz: 0.25 Gpk. Sweep rate of 1.0 octave/min. All three axes.
Nonoperating (PDP-11/44 packed for shipment)	Vertical Axis Random Vibration: 1.4 Grms overall from 10 to 300 Hz; duration: 1 h. Longitudinal & Lateral Axis Random Vibration: 0.68 Grms overall from 10 to 200 Hz; duration: 1 h. each
Altitude	
Operating	0 to 2.4 km (8000 ft)
Nonoperating	9.1 km (30000 ft)
Shock	
Operating	10 Gpk for 10 ms (+3 ms), 1/2 sine wave, vertical axis only
Nonoperating	Flat drop for a 6 in height, 3 drops total (vertical direction only)

*The operating temperature and humidity for PDP-11/44 systems, which include magnetic tape units, disk units, or card readers, is the same as defined in Table 1-5 for the PDP-11X44 system.

1.3.2 PDP-11X44 System Specifications

Table 1-5 lists the equipment specifications for the PDP-11X44 system including the TU58.

Table 1-5 PDP-11X44-CA, -CB Equipment Specifications

Characteristic	Description
Mechanical	
Cabinet dimensions	76.2 cm long × 54.29 cm wide × 100.33 cm high (30 in long × 21.38 in wide × 39.5 in high) (not including leveling feet)
Weight	
Unpacked	140.6 kg (310 lb)
Packed	181 kg (400 lb)
Environmental	
Temperature	
Operating	10° C to 40° C (50° F to 104° F)
Nonoperating	–40° C to 66° C (–40° C to 151° F)
Humidity	
Operating	10% to 90% relative (RH) with a maximum wet bulb of 28° C (82° F) and a minimum dew point of 2° C (36° F)
Nonoperating	50% relative (RH) or less to 95% (RH) or less with a maximum wet bulb of 46° C (115° F)
Vibration	
Operating	5 to 22 Hz: 0.01 in DA; 22 to 500 Hz: 0.25 Gpk. Sweep rate of 1.0 octave/min. All three axes.
Nonoperating (PDP-11X44 packed for shipment)	Vertical Axis Random Vibration: 1.4 Grms overall from 10 to 300 Hz; duration: 1 h. Longitudinal & Lateral Axis Random Vibration: 0.68 Grms overall from 10 to 200 Hz; duration: 1 h each
Altitude	
Operating	0 to 2.4 km (8000 ft)
Nonoperating	9.1 km (30000 ft)
Shock	
Operating	10 Gpk for 10 ms (+3 ms), 1/2 sine wave, vertical axis only
Nonoperating	Flat drop from a 6 in height, 3 drops total (vertical direction only)

1.3.3 H7140-AA, -AB Power Supply Electrical Specifications

Table 1-6 lists the electrical specifications of the H7140-AA, -AB power supplies.

Table 1-6 H7140-AA, -AB Power Supply Specifications

Characteristics	Description
H7140-AA	
Line voltage	90 Vrms – 128 Vrms, single-phase, two-wire and ground (120 Vrms nominal)
Frequency	47–63 Hz
Current (ac)	15 A (rms) maximum at 120 Vac 55 A (peak) maximum at 120 Vac
Power factor	Greater than 0.60 at full output load and low input voltage (90 V)
Inrush current	65 A peak at 128 Vrms for 1/2 cycle, followed by repetitive peaks of decreasing amplitude for an additional 8 cycles of the input voltage
Power	1350 W with maximum load applied at nominal voltage output
Overvoltage condition	Can withstand input overvoltage of 150 Vrms for one second
Noise transient	
Low-energy transients	300 V peak voltage spike* containing not more than 0.2 Ws of energy per spike
High-energy transients	1 KV peak voltage spike* containing not more than 2.5 Ws of energy per spike
Conducted noise	CW-10 KHz to 30 MHz, 3 Vrms
Radiated noise	RF field strength: 10 KHz to 30 MHz, 1 V/M 30 MHz to 1 GHz, 10 V/m
H7140-AB	
Line voltage	180 Vrms – 256 Vrms, single-phase, two-wire and ground (240 Vrms nominal)
Frequency	47–63 Hz
Current (ac)	9 A (rms) maximum at 240 Vac 33 A (peak) maximum at 240 Vac

Table 1-6 H7140-AA, -AB Power Supply Specifications (Cont)

Characteristics	Description
Power factor	Greater than 0.60 at full output load and low input voltage (180 V)
Inrush current	130 A peak at 256 Vrms for 1/2 cycle, followed by repetitive peaks of decreasing amplitude for an additional 8 cycles of the input voltage
Power	1350 W with maximum load applied at nominal voltage output
Overvoltage condition	Input overvoltage of 300 Vrms for one second
Noise transient	
Low-energy transients	300 V peak voltage spike* containing not more than 0.2 Ws of energy per spike
High-energy transients	1 KV peak voltage spike* containing not more than 2.5 Ws of energy per spike
Conducted noise	CW – 10 KHz to 300 MHz, 3 Vrms
Radiated noise	RF field strength – 10 KHz to 30 MHz, 1 V/M 30 MHz to 1 GHz, 10 V/m

*A spike is a voltage transient of either polarity and of either common or differential mode, with a rise time (10% to 90%) of 0.1 μs or less, and a fall time (to 10%) of 10 μs or more. The average power of spikes should not exceed 0.5 W.

1.4 SYSTEM DESCRIPTION

Figure 1-3 is a block diagram of a typical PDP-11/44 system which consists of a console terminal, modem, TU58 tape unit and selected options. The PDP-11/44 processor incorporates the complete instruction set used in the PDP-11/70 processor series and two additional instructions, MFPT and CSM.

The main memory (MS11-L) of the PDP-11/44 is addressed by a 22-bit physical address extension (PAX) bus which provides access to over 4 million bytes. In addition, the PDP-11/44 enables memory to be placed on the UNIBUS. This memory resides in the top 124K words of physical address space. The processor can perform transfers to and from the UNIBUS memory independently of main memory transfers. DMA devices making a reference to an address allocated to UNIBUS memory will never access main memory and, therefore, such transfers are not cached.

The PDP-11/44 includes a high-speed cache memory that buffers words between the processor and main memory. The cache stores those memory locations that will most likely be accessed by the executing program. The program can be executed quickly by accessing the high-speed cache and must slow down only occasionally for main memory operations.

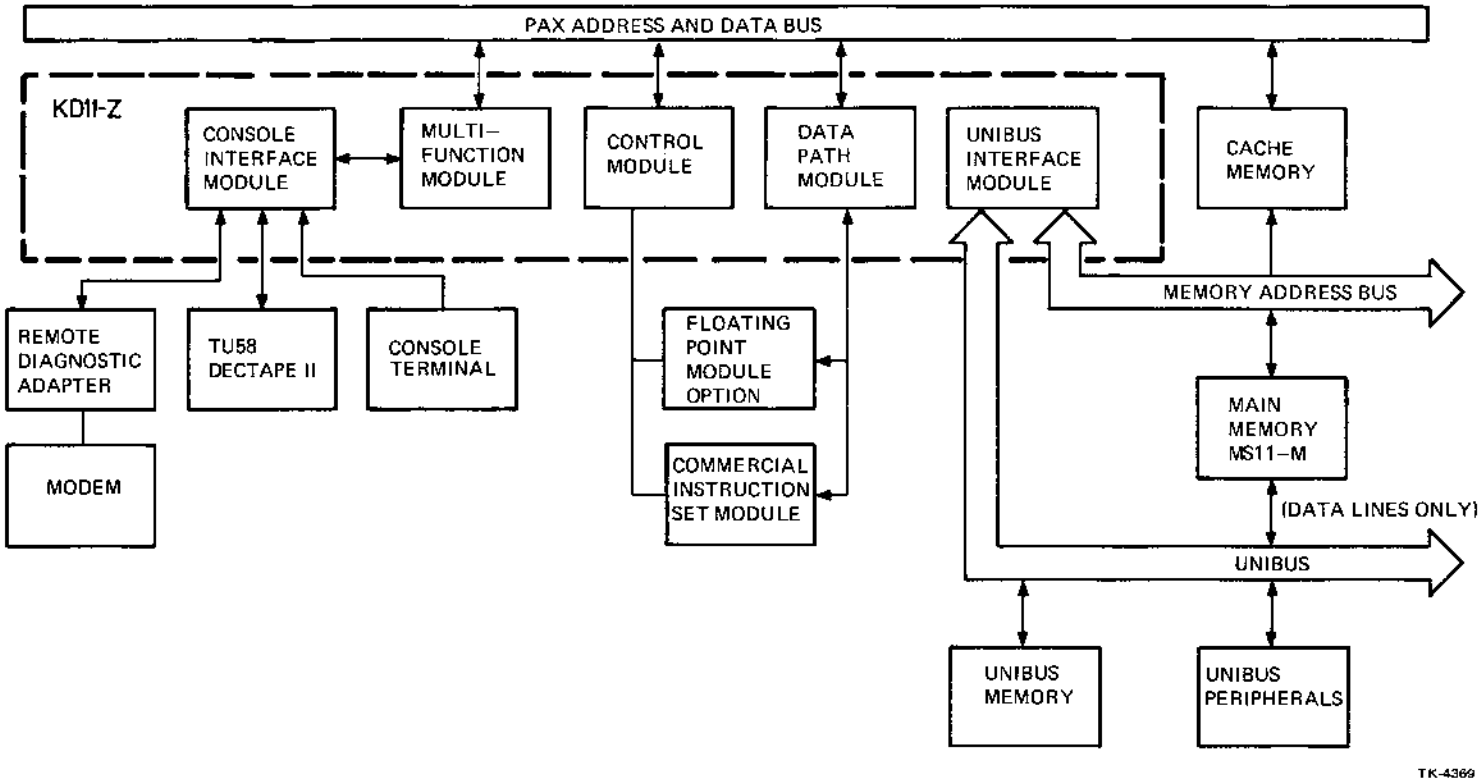


Figure 1-3 Typical PDP-11/44 System and Selected Options

The memory management system of the PDP-11/44 provides the address relocation and memory protection facilities required in a multiprogramming system. This system enables several user programs to be located simultaneously in memory. Memory management includes three mapping schemes: 16-bit, 18-bit, or 22-bit. Mapping converts the 16-bit, processor-generated virtual address to a physical address. A separate mapping scheme, the UNIBUS map, converts 18-bit UNIBUS addresses to 22-bit memory addresses. This allows devices on the UNIBUS to communicate with main memory via nonprocessor requests (NPRs).

The memory management system permits instructions or pure code to be mapped into physical memory separately from data. When this feature is enabled, instructions, index values and immediate operands are mapped through instruction (I) space. Data, or words that can be modified, are mapped through data (D) space. The I/D space facility is enabled under software control. When it is disabled, all memory references are mapped through instruction space.

The internal communication of the PDP-11/44 processor (KD11-Z) is through a 16-bit data bus and a 22-bit PAX bus. Communication between the processor and main memory is through the extended UNIBUS (EUB) and the data lines of the UNIBUS. The UNIBUS provides the path for transfers between the processor and its associated main memory, the peripherals, or the memory on the UNIBUS. The UNIBUS interface module (UBI) controls the information transfers to and from the PAX bus, the EUB, and the UNIBUS.

The multifunction module (MFM) consists of an 8085 microprocessor and the logic necessary to enable the execution of the console command set in the CPU. The 8085 software contains diagnostic programs to test logic and data paths.

In addition to the standard features of the PDP-11/44, the commercial instruction set processor (CISP) and floating-point processor (FPP) can be installed in dedicated slots of the backplane.

The following paragraphs provide a brief description of each of the standard and optional components of the PDP-11/44 system.

1.4.1 KD11-Z Central Processor

The KD11-Z central processor is comprised of four hex-height modules (M7094, M7095, M7096, and M7098) and one double-height module (M7090). The following provides a brief description of each.

1.4.1.1 Data Path Module (M7094) – The data path module contains the data path logic and the memory management logic. The data path performs arithmetic and logic processing, shifting of 8-, 16-, and 32-bit data formats, byte swapping and sign extension of data, storage of general register data, and storage of status information. Data comes from or goes to the CIS and floating-point options via the A-multiplexer (AMUX) bus of the data path. The memory management section of this module performs address relocation and contains several of the memory management registers.

1.4.1.2 Control Module (M7095) – The control module contains the control store programmable read-only memories (PROMs) and associated logic required to decode and execute PDP-11 instructions. It also contains the system clock, power-fail/autorestart logic, boot control logic and trap handling logic.

1.4.1.3 Multifunction Module (M7096) – The multifunction module (MFM) contains an 8085 microprocessor, two serial line ports, a line clock and related logic. The microprocessor allows the system terminal to be used as a programmer's console. The 8085 software routines enable the execution of the console commands discussed in Chapter 2. The serial line port used for the system terminal also serves as a remote diagnostic serial port. The second serial line port of the MFM supports a TU58 tape unit or can be used with other serial line devices.

1.4.1.4 UNIBUS Interface Module (M7098) – The UNIBUS interface module (UBI) provides the logic which enables the processor to access the UNIBUS. It also includes bus arbitration logic for interrupts and NPRs, the boot circuits which allow booting of up to four devices, and buffers for the PAX data lines to and from the processor. The UNIBUS map contained on the module allows direct memory access (DMA) transfers between main memory and peripherals on the UNIBUS. The UBI also controls the operations of the EUB.

1.4.1.5 Console Interface Module (M7090) – The console interface module (CIM) links the central processor to the console terminal, TU58 tape drives and the remote diagnostic unit. Signals between the processor and these units are buffered by the CIM to provide noise and static immunity and are converted to the proper voltage levels. The CIM also has voltage monitoring circuitry which can detect over or under voltage conditions of the power supply at the processor backplane.

1.4.2 MOS Memory

The MOS memory (MS11-M) provides 256K bytes on each module. A maximum of four modules can be installed in the PDP-11/44 system. Each memory module consists of a single hex-height module (M8722) that contains the UNIBUS/extended UNIBUS interface, timing and control logic, error correcting code (ECC) logic and a MOS storage array. The module also contains circuitry for ECC initialization and memory refresh, and a control and status register (CSR). The MS11-M also provides address interleaving for improved speed of operation.

1.4.3 KK11-B Cache Memory

The KK11-B cache increases system performance by decreasing processor-to-memory read-access time. The cache is an 8K byte, high-speed RAM which is used to store the most commonly accessed memory locations. It is contained on a single hex-height module (M7097) and is organized as a directly mapped cache with a write-through facility.

1.4.4 UNIBUS Terminator (M9302)

The M9302 terminator is a double-height module that must be installed in all PDP-11/44 systems at the end of the UNIBUS furthest from the processor. This module contains terminating resistors and logic.

1.4.5 Optional Modules and Devices

The following options can be used with the PDP-11/44 to expand the system's capabilities.

1.4.5.1 FP11-F Floating-Point Processor – The FP11-F is contained on a single hex-height module (M7093) and allows floating-point operations to be executed with greater speed than equivalent software routines. The floating-point instructions provide for both single-precision (32-bit) and double-precision (64-bit) operands.

1.4.5.2 KE44-A Commercial Instruction Set (CIS) Processor – The KE44-A is contained on one quad-height module (M7091) and one hex-height module (M7092). It enables the KD11-Z to execute the PDP-11 commercial instruction set which provides for manipulation of byte strings, character handling and decimal arithmetic operations.

1.4.5.3 TU58 DECtape II – The TU58 is a random-access, fixed-length block, mass-storage tape system. It uses DIGITAL preformatted tape cartridges which have a storage capacity of 256K bytes of data in 512-byte blocks. There are 256 blocks on each of the two tracks. The tape cartridges are miniature reel-to-reel packages containing 42.7 m (140 ft) of 3.81 mm, (0.150 in) wide tape. The TU58 interfaces to the processor through the CIM module and through the serial line unit (SLU) on the multifunction module.

1.4.5.4 Standard PDP-11 Peripheral Devices – The I/O capabilities of the PDP-11/44 can be expanded through the use of PDP-11 peripheral devices such as card readers, alphanumeric display terminals, lineprinters, teletypewriters or high-speed paper tape readers. Available storage devices include magnetic tapes and disk memories.

1.5 RELATED DOCUMENTS

Table 1-7 lists the manuals and publications that contain information related to the installation and operation of the PDP-11/44 processor system. This information is available from the locations listed in the following paragraphs.

Table 1-7 Related Publications

Title	Document Number
BA11-AA,-AB Mounting Box and Power System Technical Manual	EK-BA11A-TM
FP11-F Floating-Point Technical Manual	EK-FP11F-TM
KE44-A CISP Technical Manual	EK-KE44A-TM
MS11-M MOS Memory User's Guide	EK-MS11M-UG
PDP-11 Peripherals Handbook	EB-07667-20/78
PDP-11/04/34A/44/60/70 Processor Handbook	EB-17716-18/79
Terminals and Communications Handbook	EB-07666-20/78
TU58 DECtape II Technical Manual	EK-OTU58-UG
BA11-A Box Assembly Field Maintenance Print Set	MP00832
11/44 System Field Maintenance Print Set	MP00809
PDP-11/44 Unit Assembly (IPB)	EK-01144-IP
BA11-A Unit Assembly (IPB)	EK-BA11A-IP
H7140 Power Supply (IPB)	EK-H7140-IP

1.5.1 DIGITAL Personnel Ordering

Additional copies of this document and printed copies of the documents listed may be obtained from:

Digital Equipment Corporation
444 Whitney Street
Northboro, Massachusetts 01532
ATTN: Printing and Circulation Services (NR2/M15)
Customer Services Section

1.5.2 Customer Ordering Information

Purchase orders for supplies and accessories should be forwarded to:

Digital Equipment Corporation
Accessories and Supplies Group
Cotton Road
Nashua, New Hampshire 03060

Contact your local sales office or call DIGITAL Direct Catalog Sales toll-free 800-258-1710 from 8:30 a.m. to 5:00 p.m. eastern standard time (U.S. customers only). New Hampshire, Alaska and Hawaii customers should dial (603)-884-6660. Terms and conditions include net 30 days and F.O.B. DIGITAL plant. Freight charges will be prepaid by DIGITAL and added to the invoice. Minimum order is $35.00. Minimum does not apply when full payment is submitted with an order. Checks and money orders should be made out to Digital Equipment Corporation.

CHAPTER 2
OPERATION

This chapter describes the hardware characteristics of the PDP-11/44 system and includes the addresses assigned to the internal registers and detailed descriptions of the register bit functions. Additional information is contained in the *PDP-11 Processor Handbook 1979/80* or the latest edition.

User programs for the PDP-11/44 can be developed using the information in this chapter and the information contained in the software operating system documents.

2.1 FRONT CONTROL PANEL

The operator's control panel (Figure 2-1) is located on the lower section of the front bezel.

Table 2-1 lists and describes the functions of the front panel controls and indicators.

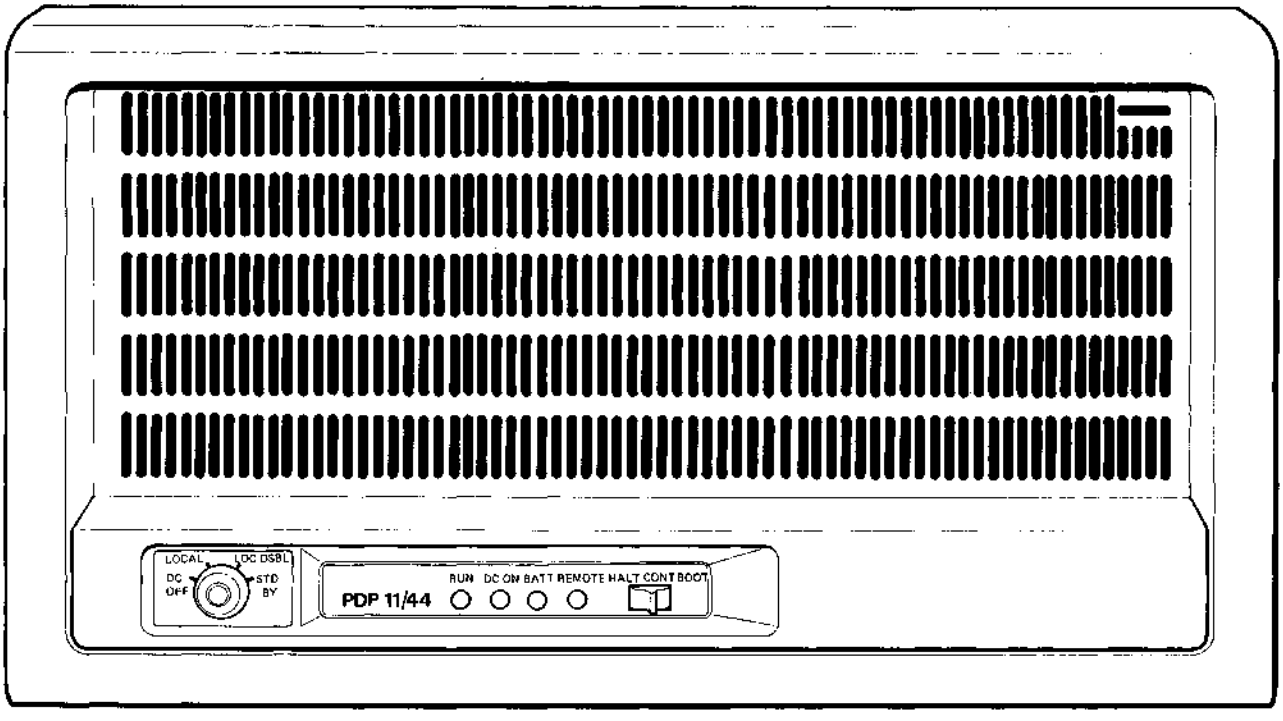


Figure 2-1 Front Control Panel

Table 2-1 Front Panel Switches and Indicators

Description	Status	Function
Power (4-position rotary keyswitch)		
DC OFF		The dc power is removed from the system and cooling fans are off. The DC OFF position does not remove ac power from the system. The ac power is removed only by disconnecting the line cord.
LOCAL		Normal ON position. The dc power is applied to logic and fans are on. The system terminal can be used in console mode or program I/O mode. The HALT position of the toggle switch is disabled.
LOC DSBL		Local disable. Normal power is applied to the system. Console mode is disabled but the console terminal can operate in program I/O mode.
STD BY		Standby. Main dc power (+5V, +15V, −15V) is off. Memory voltages are present and fans remain on.
HALT/CONT/BOOT (3-position toggle switch)		
HALT		The CPU program is stopped.
CONT		Continue. The CPU program is continued.
BOOT		A momentary position which enables the bootstrap program. When the toggle switch is released, it returns to the CONT position.
Indicators		
RUN	On	Processor is executing instructions.
	Off	Processor has halted.
DC ON	On	Indicates dc power is present and all voltages are within specified levels.
	Blinking (5 Hz)	Indicates one or more of the voltages is not within specified levels.
	Off	The dc power is off.

Table 2-1 Front Panel Switches and Indicators (Cont)

Description	Status	Function
BATT	On	Battery is present and charged to 90% or greater capacity. Used only when the battery backup unit (H7750) is installed.
	Slow Blinking	Battery is at less than 90% capacity and is charging.
	Fast Blinking	The ac power has failed, discharging, memory contents are valid.
	Off	Battery is fully discharged or not present and memory contents will be destroyed when the ac power fails.
REMOTE	On	CPU is under control of the remote diagnostic unit.
	Off	CPU is not being accessed by the remote diagnostic unit.

2.2 CONSOLE COMMANDS

The following paragraphs provide a description of the PDP-11/44 console commands and brief examples of their use. The system terminal can be used to input console commands only when the system is in console mode. Console mode can be entered in either of two ways:

1. The processor halting, or
2. The user typing the console break character, control P (^ P).

When the system is not in the console mode, it is in the program I/O mode, and data to or from the terminal is controlled by the software currently being executed.

The commands that can be performed in the console mode are listed in Table 2-2.

NOTE

All addresses specified in a console command are assumed to be 22-bit physical addresses and all data transfers are 16-bit word transfers.

2.2.1 Special Functions

In the descriptions of each console command, several expressions, special characters, and qualifiers are used. Angle brackets, ⟨N⟩, are used to denote category names. For example, the category name ⟨ADDRESS⟩ is used in an expression to represent any valid address. In an actual command, an address (e.g., 17775604) would be typed in place of the category name. Table 2-3 lists and describes the terms and characters used in the syntax expressions.

Square brackets, [N], surrounding an expression in a command description indicate that the expression is optional and is not required to issue a valid command.

Table 2-2 Console Mode Commands

Command	Designation	Command	Designation
ADDER	A	INITIALIZE	I
BOOT	B	MICROSTEP	M
CONTINUE	C	SINGLE-INSTRUCTION STEP	N
DEPOSIT	D	REPEAT	R
EXAMINE	E	START	S
FILL	F	SELF-TEST	T
HALT	H	BINARY LOAD/UNLOAD	X

Table 2-3 Console Command Terms and Characters

Name	Description
⟨SP⟩	One space
⟨COUNT⟩	A numeric count in octal
⟨ADDRESS⟩	An address argument in octal
⟨DATA⟩	A data argument in octal
⟨QUALIFIER⟩	A command modifier
⟨INPUT-PROMPT⟩	The console's prompt string (>>>)
⟨CR⟩	Carriage return
⟨LF⟩	Line feed

2.2.1.1 Console Command Qualifiers – Several of the console commands can be modified by typing qualifiers. Qualifiers expand the capability of commands by providing a number of options. All qualifiers are optional and are not required to issue a valid command. A qualifier always begins with a slash (/). Table 2-4 lists the qualifiers and describes their functions.

2.2.1.2 Special Address Field Characters – The special characters used in the ⟨ADDRESS⟩ field of a command to modify the address argument are listed and defined in Table 2-5.

2.2.1.3 Control Characters – A number of control characters are available to the user. Table 2-6 lists control characters and functions.

Table 2-4 Console Command Qualifiers

Qualifier	Function
/G	A general register qualifier that provides a method of specifying a general register as the address argument. In the examine or deposit command, an E or D can be typed followed by the /G qualifier and the register number (0 to 17_8), rather than the full 22-bit address (eight octal digits).
/N	This qualifier permits examine or deposit commands to be performed on sequential addresses without issuing a new command for each address. The /N qualifier has an associated qualifier value ⟨COUNT⟩, which specifies the number of sequential operations to be performed. The syntax for the /N qualifier is: /N [:⟨COUNT⟩] The actual number of operations to be performed can be expressed as: the initial operation (1) plus ⟨COUNT - 1⟩ additional operations. The default condition for ⟨COUNT⟩ is one.
/M	This qualifier allows a machine-dependent register to be specified as the address argument similar to the /G qualifier that specifies a general register. The address of each machine-dependent register is defined as follows: **Address** **Register** 0 Floating-Point Data 1 CIS Micro PC (CPC) 2 CIS Data 3 CPU Data 4 CPU Micro PC (MPC) 5 Cache Data 6 CPU Error Register 7 MFM Data 10 UNIBUS Data 11 Signal Register
/TB	The take bus qualifier is a maintenance feature which allows the console to perform bus transfers even though the bus may be hung.
/CB	The cache bypass qualifier allows main memory transfers to be performed even though cache is turned on and the transfer would normally result in a cache hit. This only inhibits a hit for the current command.
/E	This qualifier specifies test-extensive and is used only with the self-test (T) command.
/A	This qualifier specifies test-extensive-APT and is used only with the self-test (T) command for manufacturing use.

Table 2-5 Special Address Field Characters

Character	Function
+	The plus sign in the ⟨ADDRESS⟩ field of a command will cause the last address used to be incremented by two and used as the address argument of the command. If the /G or /M qualifier is also specified in the command, the last address is incremented by 1.
−	The minus sign in the ⟨ADDRESS⟩ field of a command will cause the last address to be decremented (by two) and used as the address argument of the command. If the /G or /M qualifier is also specified in the command, the last address is incremented by 1.
@	The "at" sign in the ⟨ADDRESS⟩ field of a command will cause the command to use the last data as the address argument. The "at" sign may be used following an indirect addressing chain of instructions.
*	The asterisk in the ⟨ADDRESS⟩ field of a command will cause the command to use the last address as the address argument.
SW	The letters SW in the ⟨ADDRESS⟩ field of a command will cause the command to use the address of the switch register as the address argument. This may be used with examine or deposit commands. **NOTE** **When accessing the switch register by its UNIBUS address, 17 777 570, only a read operation can be performed.**

Table 2-6 Control Characters

Control Character	Echo	Function
⟨CTRL-C⟩	^ C	Causes all the repetitive console operations to be aborted.
⟨CTRL-O⟩	^ O	Alternately suppresses and continues the display of data at the terminal. While the display is suppressed, the operation continues but no results are printed. An error or the end of the command will cancel the effect of the control character.
⟨CTRL-P⟩	^ P	Initiates the console mode if the keyswitch is in the LOCAL position.

Table 2-6 Control Characters (Cont)

Control Character	Echo	Function
⟨CTRL-Q⟩	^ Q	Restarts the terminal output that was suspended by CTRL-S.
⟨CTRL-S⟩	^ S	Suspends the terminal output until CTRL-Q is typed. No output is lost.
⟨CTRL-U⟩	^ U	Cancels the current input line and discards it.
⟨RUBOUT⟩ OR ⟨DELETE⟩		Deletes the last character typed on the terminal. The terminal responds to the first RUBOUT by echoing a backslash (\) and the character being deleted. Successive RUBOUT will only echo the character being deleted. If the user attempts to rubout beyond the start of the command, the RUBOUT will continue to echo the first character of the input string. The first character typed by the user that is not a RUBOUT will result in the terminal echoing a backslash (\) and the new character being entered. As an example, if the user types: ⟩⟩⟩E⟨SP⟩17713⟨RUBOUT⟩⟨RUBOUT⟩65000⟨CR⟩ the displayed echo will be: ⟩⟩⟩E17713\31\65000 which is equivalent to the user deleting the entire line by control character CTRL-U, then typing the following: ⟩⟩⟩E⟨SP⟩17765000⟨CR⟩

2.2.2 ADDER Command

This command prints the 16-bit result of the current address pointer and the last data examined plus 2. This command can be used to calculate the effective address for an instruction using mode 6, register 7 or mode 7, register 7.

The syntax for the ADDER command is as follows:

A⟨CR⟩

The following are examples of the ADDER command.

```
001000      016767      MOV       2000,3000
001002      000774
001004      001772
001006      000000      HALT
```

```
E 1000⟨CR⟩
00001000 016767

E⟨CR⟩
00001002 000774

A⟨CR⟩
002000

E⟨CR⟩
000001004 001772

A⟨CR⟩
003000

E⟨CR⟩
00001006 000000
```

2.2.3 BOOT COMMAND

The syntax for the BOOT command is as follows:

B [⟨SP⟩⟨DEVICE-IDENTIFIER⟩] ⟨CR⟩

The BOOT command can be performed only if the processor is halted. When typing B⟨CR⟩ without the optional device code, a default boot is performed depending on the setup of the boot switches located on the UNIBUS interface (UBI) module (M7098). The optional device identifier is a two-character code which identifies the peripheral bootstrap to be performed. Device codes for some typical peripherals are listed in Table 2-7.

The device identifier may also include the unit number of the peripheral (e.g., DK1 boots RK05 unit number 1). If a unit number is not typed, the default number is 0.

When the BOOT command is issued, the device code typed is compared to the device identifiers of the boot ROMs. If the device is not supported by the boot ROMs (i.e., no device match), the console will respond with the console prompt ()))). If the device is supported or if no device code was typed (default boot), an initialize is issued. The priority bits of the processor status word are set to 7 and the carry bit is set or cleared, depending on the setting of the boot switches. If the carry bit is cleared, the ROM diagnostic programs will be performed prior to the initiation of the bootstrap program for the specified device. General register 0 is loaded with the unit number, or with zero if none is typed. The PC is then loaded with the starting address of the boot program. If a device code was not typed, the PC is loaded with the starting address indicated by the boot switches. Once the PC is loaded, the processor is started and the system enters program I/O mode.

Table 2-7 Device Bootstrap Identifiers

Device Identifier	Device	Device Identifier	Device
CT	TA11	DY	RX02
DB	RP04/05/06 RM02/03	MM	TU16/E16(TM02/03)
DD	TU58	MS	TS04
DK	RK03/05/05J (Units 2)	MT	TU10/TE10/TS03
DL	RL01	PR	PC05 (High-Speed Reader)
DM	RK06/07	TT	ASR33 (Low-Speed Reader)
DP	RP02/03	XM	DMC-11
DS	RS03/04	XW	DUP-11
DT	TU55/56	XU	DU11
DX	RX01	XL	DL11

The following are examples of BOOT command.

)))B ⟨CR⟩	Perform the default boot.
)))B ⟨SP⟩ DK1 ⟨CR⟩	Boot the RK05, Unit 1.

Up to four devices can be selected for program loading. To determine the value of the starting address selected by the switch pack E28 on the UBI module and the devices which are controlled by a bootstrap ROM, perform the following procedure:

1. Examine address 773024 and evaluate the response as follows:

   165 XYZ = Boot to Console Mode
   173 XYZ = Boot to selected device

   The remaining three octal digits (XYZ) can be separated into the binary values associated with the E58 switch positions as follows:

Switch	S3	S4	S5	S6	S7	S8	S9	S10
Value	x	x	x	y	y	y	z	z
		$0–7_8$			$0–7_8$		$0,2,4$ or 6_8	

Binary 1 = On
Binary 0 = Off

2. To identify the device bootstrap ROMs that are installed, initiate the diagnostic program MAINDEC CZM9B or examine the following five addresses and compare the response with the device ROM identification numbers listed in Table 2-8.

17776774	(CPU diagnostic ROM)
17773000	(Device ROM 1)
17773200	(Device ROM 2)
17773400	(Device ROM 3)
17773600	(Device ROM 4)

A 177776 response will indicate the continuation of a ROM diagnostic program to an additional ROM.

An XXX777 response will indicate a ROM failure or no ROM present at the addressed location.

2.2.4 CONTINUE Command

The syntax for the CONTINUE command is as follows:

C ⟨CR⟩

If the processor was halted when the CONTINUE command was initiated, the processor will begin operating and the system will enter the program I/O mode. If the processor was running when the CONTINUE command was initiated, the system will only enter the program I/O mode.

Table 2-8 Bootstrap ROM Identifiers

Octal ID	Device ROM	Octal ID	Device ROM
041460	PDP-11/44 Diagnostic	050122	ASR33 (Low-Speed Reader)
041524	TA11		
042104	TU58	054114	
042113	RK03/05/05J	177776	DL11
042113	TU55/56	177776	
042114	RL01		
042115	RK06/07	054115	
042120	RP02/03	177776	DMC-11
042120	RP04/05/06	177776	
042120	RM02/03		
042123	RS03/04	054125	
042130	RX01	177776	DU11
042131	RX02	177776	
046515	TU16/45/77/TE16		
046523	TS04	054127	
046524	TU10, TE10, TS03	177776	DUP-11
050122	PC05 (High-Speed Reader)	177776	

2.2.5 DEPOSIT Command

The syntax for the DEPOSIT command is as follows:

D [⟨QUALIFIER⟩]⟨SP⟩⟨ADDRESS⟩⟨SP⟩⟨DATA⟩⟨CR⟩

The DEPOSIT command will deposit ⟨DATA⟩ into the ⟨ADDRESS⟩ specified. The address space will depend upon the qualifiers specified with the command.

Initiating deposits while the processor is running is illegal unless the deposit is to the console switch register (D⟨SP⟩SW⟨SP⟩⟨DATA⟩⟨CR⟩). Since the switch register is internal to the console, the qualifiers /TB and /CB would be useless.

Table 2-9 lists the qualifiers that can be used with the DEPOSIT command.

The ⟨ADDRESS⟩ in the DEPOSIT command can be a one-to eight-digit octal number, SW or any of the special address characters (+, −, *, @). The ⟨DATA⟩ in the command can be a one-to six-digit octal number.

Upon completion of the deposit, the console will respond with the console prompt (⟩⟩⟩).

The following are examples of the DEPOSIT command.

⟩⟩⟩D⟨SP⟩1000⟨SP⟩5	Deposits 5 into location 1000.
⟩⟩⟩D⟨SP⟩+⟨SP⟩776	Deposits 776 into last address +2. If preceded by above example, then data would be deposited into location 1002.
⟩⟩⟩D⟨SP⟩*⟨SP⟩400	Deposits 400 into last address. If preceded by above example, then data would be deposited into location 1002.
⟩⟩⟩D/M⟨SP⟩4⟨SP⟩240	Deposits 240 into the processor micro PC.
⟩⟩⟩D/G/N:5⟨SP⟩0⟨SP⟩35	Deposits 35 into the next 5 general registers starting with R0.

2.2.6 EXAMINE Command

The syntax for the EXAMINE command is as follows:

E [[⟨QUALIFIER⟩]⟨SP⟩⟨ADDRESS⟩]⟨CR⟩]

Examines are legal while the processor is running. The console will respond to the examine command by printing the eight-digit physical address examined followed by the six-digit octal data contained in that location. This will occur unless the printout is inhibited by a control character. Upon completion of the examine, the console will respond with the console prompt (⟩⟩⟩).

The qualifiers that can be used with the EXAMINE command are listed in Table 2-10.

The ⟨ADDRESS⟩ in the EXAMINE command can be a one- to eight-digit octal number, SW or any of the special address characters (+, −, *, @). The ⟨ADDRESS⟩ in the EXAMINE command is optional. If none is typed, the last address is incremented by 2 or 1 if the /G or /M qualifier is used.

Table 2-9 Deposit Command Qualifiers

Qualifiers	Function
/G	Enables deposits into the general registers without typing the full eight-digit octal address. The qualifiers /N, /TB or /CB can be used in conjunction with the /G qualifier.
/M	The only machine-dependent register that can be deposited into is the CPU micro PC register (address 00000004). The data deposited into this register will be used as the next processor micro PC.
/N	Allows deposits into sequential locations.
/TB	The take bus qualifier is used for maintenance purposes only.
/CB	Using the cache bypass qualifier may cause a cache invalidate if the address specified is in cache.

Table 2-10 Examine Command Qualifiers

Qualifier	Function
/G	Enables the general registers to be examined without typing the full eight-digit octal address. The qualfiiers /N, /TB, /CB can be used in conjunction with the /G qualifier.
/M	Allows the machine-dependent registers to be examined. The qualifiers /N, /TB or /CB can be used in conjunction with the /M qualifier.
/N	Allows examines of sequential locations.
/TB	The take bus qualifier is used for maintenance purposes only.
/CB	Using the cache bypass qualifier may cause a cache invalidate if the address specified is in cache.

The following are examples of the EXAMINE command.

```
)))E⟨SP⟩1000⟨CR⟩
00001000 002625
```
Examine location 1000.

```
)))E⟨CR⟩
00001002 005646
```
Examine the next location. An equivalent command would be: E⟨SP⟩+⟨CR⟩.

```
)))E/G⟨SP⟩7⟨CR⟩
17777707 001514
```
Examine the PC.

```
)))E⟨SP⟩@⟨CR⟩
00001514 012737
```
Now examine the location pointed to by the PC (i.e., use the last data for the new address).

```
)))E/M/N:5⟨SP⟩0⟨CR⟩
00000000 130260
```
Examine the next 5 machine-dependent registers starting with the machine-dependent register 0.

```
00000001 177777
00000002 177777
00000003 177777
00000004 000010
```

2.2.7 FILL Command

The syntax for the FILL command is as follows:

F[⟨SP⟩⟨COUNT⟩]⟨CR⟩

The console will send ⟨COUNT⟩ null characters after each ⟨CR⟩ before any further transmissions. When a power failure occurs, the ⟨COUNT⟩ will be cleared.

The FILL command sets the fill count to the value typed in the ⟨COUNT⟩ field, where ⟨COUNT⟩ is a one- to six-digit octal number. However, the maximum fill count is 17 (octal). If the ⟨COUNT⟩ entered is greater than 17, then the fill count is set to 17. If no ⟨COUNT⟩ is entered, the fill count is set to zero. Also, on powerup, the fill count is set to zero. Upon completion of the FILL command, the console responds with the console prompt ()))). The FILL command causes the ⟨COUNT⟩ number of null characters to be echoed following a ⟨CR⟩.

The following are examples of the FILL command.

```
)))F⟨SP⟩4⟨CR⟩
```
Set fill count to 4. Subsequent carriage returns will be followed by 4 null characters generated by the MFM module as shown below.

```
)))E⟨SP⟩1000⟨CR⟩⟨NULL⟩⟨NULL⟩⟨NULL⟩⟨NULL⟩⟨LF⟩
00001000 002625 ⟨CR⟩⟨NULL⟩⟨NULL⟩⟨NULL⟩⟨NULL⟩⟨LF⟩
```

```
)))F⟨CR⟩
```
Resets the fill count to 0.

2.2.8 HALT Command

The syntax for the HALT command is as follows:

H⟨CR⟩

The HALT command initiates a halt by asserting the CPU halt request. If the request is honored and the clock is stopped, the console examines register R7 (the PC), then prints 17777707 and the updated PC value. If the processor does not halt within 600 ms, an error message is printed.

If the processor is halted when the HALT command is issued, the halt request is not asserted and the console responds with the console prompt (>>>). No error message is issued.

The following are examples of the HALT command.

```
>>>H⟨CR⟩
17777707 001000 ⟨CR⟩
```

Halt the CPU and print the contents of R7.

```
>>>H⟨CR⟩
>>>
```

Since the processor is already halted, this command is ignored.

2.2.9 INITIALIZE Command

The syntax for the INITIALIZE command is as follows:

I⟨CR⟩

The INITIALIZE command is valid only if the processor is halted. Upon receiving a valid INITIALIZE command, the console issues a UNIBUS initialize. The console then issues the console prompt (>>>).

2.2.10 MICROSTEP Command

The syntax for the MICROSTEP command is as follows:

M[⟨SP⟩⟨COUNT⟩]⟨CR⟩

The CPU is allowed to execute the number of microinstructions specified by the ⟨COUNT⟩ value. If no count is specified, one microinstruction is performed.

The MICROSTEP command is valid only if the processor is halted. The ⟨COUNT⟩, if specified, is a one- to six-digit octal number. The command will cause the console to perform an initial microinstruction plus ⟨COUNT⟩-1 additional microinstructions. For each microstep, the console enables the processor clock for one cycle, examines the micro PC register, and prints the register address (00000004) and contents of the PC register.

The count is decremented after each microinstruction is performed. When the count equals 0, the console will print out the last micro PC and the console prompt (>>>). The console is then in the spacebar step mode and an additional microinstruction is performed each time the spacebar is pressed. When no count is specified, the console enters spacebar step mode after the first microinstruction is performed.

The following is an example of the MICROSTEP command:

```
)))M⟨SP⟩3⟨CR⟩                    Perform 3 microinstructions
00000004 000010
00000004 000015
00000004 000210
)))                              The console is now in the spacebar step mode and another mi-
                                 croinstruction can be executed by pressing the spacebar.
```

Execution of the MICROSTEP command causes the address of the CPU micro PC (00000004) and the contents of that location to be printed. This is the default printout for the MICROSTEP command. Other machine-dependent registers may be monitored during microstepping. The following example illustrates this capability.

```
)))M⟨CR⟩
00000004 000015
)))E/M⟨SP⟩10⟨CR⟩
00000010 000777
)))00000010 000000               This command executes one microstep; sets the console into
                                 the spacebar step mode. The second command 10 examines
                                 the machine register 10 (UNIBUS data) and changes the
                                 default printout. Pressing the spacebar will then cause anoth-
                                 er microstep to be performed and the new contents of ma-
                                 chine register 10 to be printed.
```

2.2.11 SINGLE-INSTRUCTION-STEP Command

The syntax for the SINGLE-INSTRUCTION-STEP command is as follows:

N[⟨SP⟩⟨COUNT⟩]⟨CR⟩

The SINGLE-INSTRUCTION-STEP command is valid only if the processor is halted. The ⟨COUNT⟩, if specified, is a one- to six-digit octal number. This command will cause the console to perform an initial instruction plus ⟨COUNT⟩-1 additional instructions. For each instruction step, the console enables the processor clock for one instruction, examines the PC, and prints its address (17777707) and contents.

The count is decremented after each instruction step is performed. When the count equals 0, the console will print out the last PC and the console prompt ()))). The console is then in spacebar step mode and an additional instruction step can be performed by pressing the spacebar. When no count is specified, the console enters spacebar step mode after the first instruction step is performed.

The following is an example of the SINGLE-INSTRUCTION-STEP command:

```
)))N⟨SP⟩3⟨CR⟩                    Perform 3 single-instruction steps.
17777707 001000
17777707 001002
17777707 001004
)))                              The console is now in spacebar step mode and another instruc-
                                 tion can be performed by pressing the spacebar.
```

2.2.12 START Command

The syntax for the START command is as follows:

S[⟨SP⟩⟨DATA⟩]⟨CR⟩

The START command is valid only if the processor is halted. The ⟨DATA⟩, if specified, is a one- to six-digit octal number that is deposited into the PC when the command is performed. The console responds to a valid START command by issuing an initialize and depositing data into the PC. If no data is specified, the PC is unchanged. Following the initialize and deposit, the processor continues and the system enters the program I/O mode.

The following are examples of the START command.

)))S⟨SP⟩1000⟨CR⟩	Deposits 1000 into the PC and starts the processor from that location.

The following combination of commands is equivalent to the above command:

)))D/G⟨SP⟩7⟨SP⟩1000⟨CR⟩	Deposits 1000 into the PC.
)))S⟨CR⟩I	Initialize – Continue the processor at current PC (1000).

2.2.13 SELF-TEST Command

The syntax for the SELF-TEST command is as follows:

T[⟨QUALIFIER⟩]⟨CR⟩

The SELF-TEST command is valid while the processor is running only if no qualifiers are specified. If qualifiers are specified, the processor must be halted. The qualifiers that may be used are /E (test-extensive) or /A (test-extensive-APT).

The self-test is executed in response to this command and also upon entry into console mode via ^P or processor halt.

If the self-test is completed without error, the message CONSOLE is printed followed by the console prompt. If the self-test was entered as a result of a processor halt, then the test is run, the PC is examined, the contents are printed, and the console prompt ()))) is printed.

If the T/E or T/A command is entered, additional tests are performed along with the self-test. The console responds to the T/E command by printing CONSOLE-TESTB followed by the console prompt.

NOTE

Caution should be exercised in performing these commands because the T/E and T/A commands modify main memory. The T/A command restarts the processor after execution of the command.

If any of the tests being performed detect an error, the appropriate error message is printed and the test program will loop on the error.

2.2.14 BINARY LOAD/UNLOAD Command

The syntax for the BINARY LOAD command is as follows:

X⟨SP⟩⟨ADDRESS⟩⟨SP⟩⟨COUNT⟩⟨CR⟩⟨COMMAND CHECKSUM⟩
⟨DATA⟩⟨LOAD CHECKSUM⟩

The syntax for the BINARY UNLOAD command is:

X⟨SP⟩⟨ADDRESS⟩⟨SP⟩⟨COUNT⟩⟨CR⟩⟨COMMAND CHECKSUM⟩

NOTE
Bit 15 of the ⟨COUNT⟩ field indicates direction control (1=UNLOAD, 0=LOAD).

The BINARY LOAD/UNLOAD command enables strings of bytes of binary data to be read from or written into memory. The number of binary bytes is represented by the ⟨COUNT⟩ field. The console does not perform byte transfers. The load or unload command is executed by assembling the bytes into words before performing the transfer. Since only word transfers are supported, the ⟨COUNT⟩ field must represent an even number.

During the BINARY LOAD command, the processor cannot process control characters typed by the user since the binary data contains similar characters. To prevent the BINARY LOAD command from being initiated erroneously, the command is terminated by a special ⟨CHECKSUM⟩ character.

During either the BINARY LOAD/UNLOAD command, the checksum is calculated in a similar manner. The command checksum is a binary byte of data that represents the 2's complement of the sum of the ASCII characters that comprise the command string, including ⟨CR⟩. As the command string is read by the console, each character is added to a memory location, which is initially set to 0. If no errors occur, the result of the addition will be zero. If the checksum is correct, the console echoes the prompt string but remains in binary mode. If the command is a binary load, the echo of the input data is suppressed. If the checksum is incorrect, an error is reported. The command checksum is not loaded into memory and does not cause the ⟨COUNT⟩ to be decremented.

In the BINARY LOAD command, a binary string of data of length ⟨COUNT⟩ + 1 will be sent to the console once the requester receives the input prompt which indicates the console's acceptance of the command. The console will sequentially deposit all but the last byte into memory, starting at ⟨ADDRESS⟩. As the console receives the binary data, it calculates the load checksum. Similar to the command checksum, the load checksum is a binary byte of data which when added to the total checksum, should yield a zero result. Once the ⟨COUNT⟩ is exhausted, the load checksum is sent by the console. If an error is encountered during the load or checksum, the error is reported. If no errors occur, the console will respond with the console prompt.

In the BINARY UNLOAD command, the console processes the command and checks the checksum. If the checksum is correct, the console responds with the input prompt followed by a string of bytes, which is the binary data requested. As each binary byte is sent from the console, the 2's complement is added to a byte, initially set to zero. This byte will be sent upon completion of the command and it is followed by the input prompt. The receiver of the unloaded data can now check to ensure that all bytes were correctly received.

2.2.15 REPEAT Command

The syntax for the REPEAT command is as follows:

R⟨SP⟩(COMMAND)⟨CR⟩

This command will repeatedly execute the EXAMINE or DEPOSIT command and is terminated by the control character CTRL-C (∧C).

2.2.16 Summary of Errors

When an error is detected during the performance of a console command, the errors listed in Table 2-11 may be reported by the console.

Table 2-11 Summary of Errors

Character	Definition
?01	Syntax error, illegal command.
?11	Illegal internal processor register designated using /M qualifier.
?15	Command is illegal while processor is running.
?20	Transfer error. The console tried to examine or deposit but failed due to memory time-out or parity error.
?21	Halt error. The console tried to halt the processor but failed.
?22	CPU hung. As opposed to ?20, the console directed the processor to initiate a transfer, but the transfer was never started.
?30	Checksum error. In executing a BINARY LOAD/UNLOAD command, a checksum error occurred.
?81	Checksum error. In executing the self-test, the console control store was found to have a checksum error in PROM 1.
?82	Checksum error. In executing the self-test, the console control store was found to have a checksum error in PROM 2.
?85	Error in read/write test for console RAM.
?A7	Halt/continue test of test/extensive failed.
?A8	PAX data bus test of test/extensive failed.
?A9	PAX address test of test/extensive failed.
?AA	Switch register test of test/extensive failed.

2.2.17 Summary of Commands
Table 2-12 is a list of the console commmands, special characters, modifiers and qualifiers.

2.3 PDP-11/44 REGISTERS
The upper 4K of the physical address space is assigned to the CPU registers and I/O device registers. Table 2-13 lists some of the registers and their associated addresses.

2.3.1 CPU Registers
The CPU contains several registers which can be used to store processor status information, error information and interrupt requests. Eight general purpose registers are also included to be used as accumulators, counters, index registers, or for other programming functions.

Table 2-12 Console Command Summary

Syntax	Command
B [⟨SP⟩ ⟨DEVICE IDENTIFIER⟩] ⟨CR⟩	BOOT
C ⟨CR⟩	CONTINUE
D [⟨QUALIFIERS⟩]⟨SP⟩⟨ADDRESS⟩⟨SP⟩⟨DATA⟩ ⟨CR⟩	DEPOSIT
E [⟨QUALIFIERS⟩⟨SP⟩⟨ADDRESS⟩] ⟨CR⟩	EXAMINE
F [⟨SP⟩ ⟨COUNT⟩] ⟨CR⟩	FILL
H ⟨CR⟩	HALT
I ⟨CR⟩	INITIALIZE
M [⟨SP⟩ ⟨COUNT⟩] ⟨CR⟩	MICROSTEP
N [⟨SP⟩ ⟨DATA⟩] ⟨CR⟩	SINGLE-INSTRUCTION STEP
S [⟨SP⟩ ⟨DATA⟩] ⟨CR⟩	START
T [⟨QUALIFIER⟩] ⟨CR⟩	SELF-TEST
Λ ⟨CR⟩	ADDER
R ⟨COMMAND⟩ ⟨CR⟩	REPEAT

Special Characters	Function
Control C	Causes the aborting of all repetitive console operations.
Control O	Enables/disables terminal output.
Control P	Forces entry into console mode if keyswitch is in LOCAL position. Programs in operation will continue, however, no I/O operations to a terminal can occur by program until the program I/O mode is reentered.
Control U	Deletes entire line currently being typed.
Control S	Stops terminal output.
Control Q	Starts terminal output.

Address Modifiers

+	Autoincrement
−	Autodecrement
*	Use last address
@	Use last data as address
SW	Switch register

Qualifiers

/G	General register
/N:⟨COUNT⟩	Multiple operations
/M	Machine-dependent registers
/TB	Take bus
/CB	Cache bypass
/E	Test-extensive
/A	Test-extensive-APT

Table 2-13 PDP-11/44 CPU and I/O Device Register Address

Address	Register
17 777 776	Processor Status Word (PSW)
17 777 772	Program Interrupt Request (PIRQ)
17 777 766	CPU Error
17 777 744,46,50,52,54	Cache Registers
17 777 707 – 17 777 700	CPU General Registers
17 777 676 – 17 777 660	User Data PAR, Reg. 0–7
17 777 656 – 17 777 640	User Instruction PAR, Reg. 0–7
17 777 636 – 17 777 620	User Data PDR, Reg. 0–7
17 777 616 – 17 777 600	User Instruction PDR, Reg. 0–7
17 777 576	MM Status Register 2 (SR2)
17 777 574	MM Status Register 1 (SR1)
17 777 572	MM Status Register 0 (SR0)
17 777 566 – 17 777 560	Console Terminal SLU
17 77x xx0 – 17 76x xx0	TU58 DECtape SLUs
17 777 570	Switch Register
17 777 516	MM Status Register 3 (SR3)
17 772 376 – 17 772 360	Kernel Data PAR, Reg. 0–7
17 772 356 – 17 772 340	Kernel Instruction PAR, Reg. 0–7
17 772 336 – 17 772 320	Kernel Data PDR, Reg. 0–7
17 772 316 – 17 772 300	Kernel Instruction PDR, Reg. 0–7
17 772 276 – 17 772 260	Supervisor Data PAR, Reg. 0–7
17 772 256 – 17 772 240	Supervisor Instruction PAR, Reg. 0–7
17 772 236 – 17 772 220	Supervisor Data PDR, Reg. 0–7
17 772 216 – 17 772 200	Supervisor Instruction PDR, Reg. 0–7
17 770 372 – 17 770 200	Map Registers

2.3.1.1 Processor Status Word (PSW) – The format of the processor status word (PSW) register is shown on Figure 2-2. Table 2-14 lists the functions of the PSW bits.

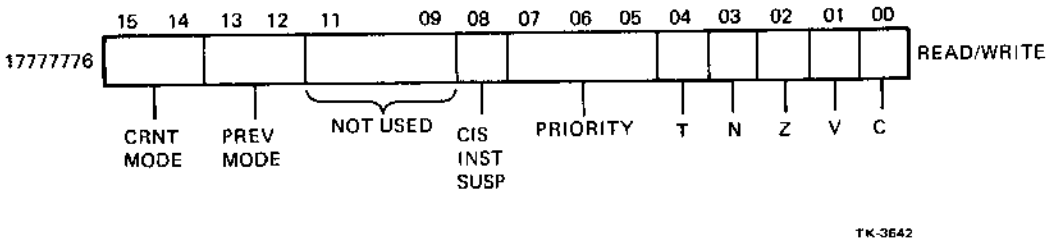


Figure 2-2 PSW Register Format

Table 2-14 Processor Status Word Register Bit Descriptions

Bit	Description
15:14	Current Mode – These bits specify the current processor mode as follows: 00 – The processor is in kernel mode and all operations are legal. 01 – The processor is in supervisor mode. A HALT instruction will trap to location 4 and the instructions RESET and SET PRIORITY LEVEL (SPL) are treated as a NO OPERATION (NOP). 10 – An illegal mode. If memory management is enabled, a memory management abort occurs. 11 – The processor is in user mode. A HALT instruction will trap to location 4 and the instructions RESET and SPL are treated as a NOP.
13:12	Previous Mode – Specify the previous processor mode, prior to the last trap, interrupt or loading of the PSW. The modes are the same as defined for the current mode (bits 15:14).
11:09	Not used.
08	CIS Instruction Suspension – This bit is set to 1 when a CIS instruction is entered and cleared when the instruction is completed. If this bit is set when an interrupt occurs, it indicates that the instruction was not completed and must be continued upon return from the interrupt. If this bit is set, the T-bit cannot be set. This prevents looping in trace trap mode.
07:05	Priority – These bits specify the current level of the processor priority. The central processor operates at any of eight levels of priority, 0–7. When the CPU is operating at level 7, an external device cannot interrupt it with a request for service. The central processor must be operating at a lower priority than the priority of the external device's request in order for the interruption to take effect. The eight processor levels provide an interrupt mask, which can be altered through use of the set priority level (SPL) instruction. This instruction can be used only by the kernel mode and allows a kernel mode program to alter the central processor's priority without affecting the rest of the processor status word.
04:00	Condition Codes – The condition codes contain information which occurred as a result of the previous CPU operation. The bits are defined as follows: T (04) Trap – Set to 1 or cleared under program control. When set, a processor trap will occur through location 14 on completion of instruction execution and a new processor status word will be loaded. This bit is useful for debugging programs by providing a method of tracing the execution of programs.

Table 2-14 Processor Status Word Register Bit Descriptions (Cont)

Bit	Description	
	N (03)	Negative – Set to 1 if the result of the last data manipulation was negative.
	Z (02)	Zero – Set to 1 if the result of the last data manipulation was zero.
	V (01)	Overflow – Set if the result of the last data manipulation caused an overflow.
	C (00)	Carry – Set if the last data manipulation produced a carry bit.

2.3.1.2 Program Interrupt Request Register – System software may request an interrupt by setting one of bits (PIR) 15:09 for PIR7–PIR1 in the program interrupt request (PIRQ) register. The hardware sets bits 07:05 and 03:01 to the encoded value of the highest PIR bit set. Bits 07:05 allow the program interrupt active (PIA) field to be moved into the processor status word register and set the processor priority to the level of the request honored. This disables all requests on the same level or below. Bits 03:01 can be used as an index constant in branching to an interrupt service routine for the appropriate priority level request.

When a priority interrupt request is granted, the processor traps to location 240. A new PC is taken from location 240 and a new PSW from location 242. The interrupt service routine must queue requests within a priority level and clear the PIR bit before the interrupt is dropped.

Figure 2-3 shows the bit assignments of the PIRQ and Table 2-15 lists the functions of the bits.

2.3.1.3 Error Register – This register identifies the source of the abort or trap that used the vector at location 4. Bits 07:04, bit 02 and bit 00 are cleared when the CPU error register is written; the remaining bits are software transparent and are accessible only when the console has control. Figure 2-4 descriptions are listed in Table 2-16.

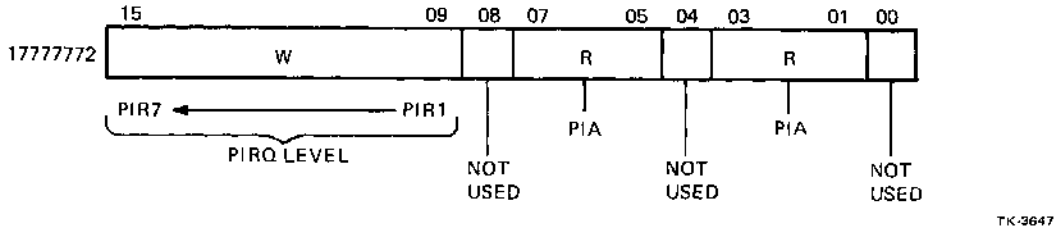


Figure 2-3 PIRQ Register Format

Table 2-15 Processor Interrupt Request Register Bit Descriptions

Bit	Description
15:09	PIR7–PIR1 – Seven program interrupt request bits which may be set to request an interrupt at a given priority level.
08	Not used.
07:05, 03:01	PIA – Program interrupt active bit, which is the encoded value of the highest PIR bit set.
04	Not used.
00	Not used.

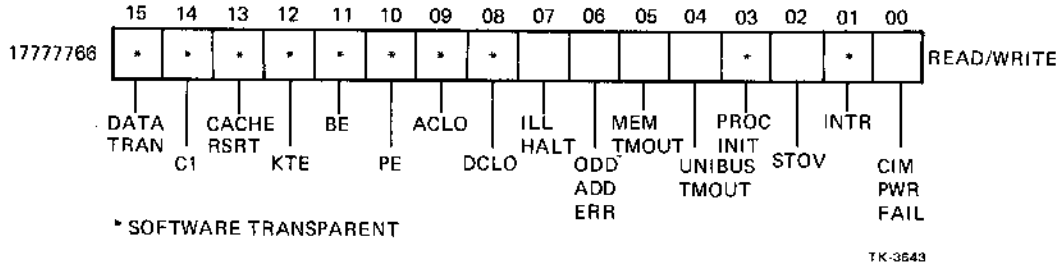


Figure 2-4 CPU Error Register Format

Table 2-16 Error Register Bit Descriptions

Bit	Description
15	Data Transfer – This bit monitors the DATA TRAN line of the processor. When clear, this bit indicates the processor is initiating a data transfer on the UNIBUS.
14	C1 – This bit is set to 1 when the UNIBUS control signal BUS C1 is asserted, indicating a DATO or DATOB transfer is being performed.
13	Cache Restart – This bit, when set to 1, indicates that the cache has generated the signal necessary to restart the processor clock.
12	KTE – This bit, when set to 1, indicates that one of the memory management errors (nonresident, page length or read-only abort) has occurred.

Table 2-16 Error Register Bit Descriptions (Cont)

Bit	Description
11	Bus Error – This bit, when set to 1, indicates that the processor has attempted to access nonexistent memory, odd address during word reference or there was no response on the UNIBUS within approximately 20 μs.
10	Parity Error – This bit, when set to 1, indicates that the processor has received a memory parity error.
09	AC LO – This bit, when set to 1, indicates that UNIBUS AC LO is asserted. This signal is not latched and, therefore, bit 09 is not affected by a processor INIT.
08	DC LO – This bit, when set to 1, indicates that UNIBUS DC LO is asserted. This signal is not latched and, therefore, bit 08 is not affected by a processor INIT.
07	Illegal Halt – This bit is set to 1 when a halt instruction is attempted when the processor is in user or supervisor mode.
06	Odd Address Error – This bit is set to 1 when the program attempts a word reference on an odd address.
05	Memory Time-Out – This bit is set to 1 when the program attempts to read a word from a nonexistent memory location. This does not include UNIBUS addresses.
04	UNIBUS Time-Out – This bit is set to 1 when there is no response on the UNIBUS within approximately 20 μs.
03	Processor Initialize – This bit monitors the processor initialize signal.
02	Stack Overflow – This bit is set to 1 when the kernel hardware stack is less than octal 400.
01	Interrupt – This bit is set when the PAX interrupt line is asserted.
00	CIM Power Failure – This bit, when set to 1, indicates that dc power to the machine has exceeded voltage tolerance limits for a period of 1.5 μs or greater.

2.3.1.4 General Registers – The CPU contains several 16-bit general registers that can be used as accumulators, index registers, autoincrement registers, autodecrement registers or as stack pointers for temporary storage of data. A few of these registers are used for special purposes. Register 7 (R7) is used as the program counter (PC) and contains the address of the next instruction to be executed. R6 is generally used as the processor stack pointer (SP) if the processor is in kernel mode. If the processor is in supervisor or user mode, R16 or R17 is used as the processor stack pointer, respectively. Table 2-17 lists the general registers and their addresses and functions.

Table 2-17 General Register Addresses

Address	Function
17 177 705 – 17 177 700	R5-R0, General Purpose Registers
17 777 706	R6, Kernel Mode Stack Pointer
17 777 707	R7, Program Counter
17 777 710	R10, Temporary Storage
17 777 711	R11, Unused
17 777 715 – 17 777 712	R15-R12, Temporary Storage
17 777 716	R16, Supervisor Mode Stack Pointer
17 777 717	R17, User Mode Stack Pointer

2.3.2 Multifunction Module Register

The multifunction module (MFM) contains two serial line units (SLUs) which provide the interface ports between the serial line devices and the PDP-11/44 processor. The SLU can be connected to a console terminal, to the TU58 tape unit, or to a remote diagnostic facility. The console terminal operates as a standard I/O device or as a programmer's console to access and load registers within the CPU.

2.3.2.1 Console Terminal Receiver Control/Status Register (RCSR) – Figure 2-5 shows the format of the console terminal receiver control/status register (RCSR) and Table 2-18 lists and describes the functions of the bits.

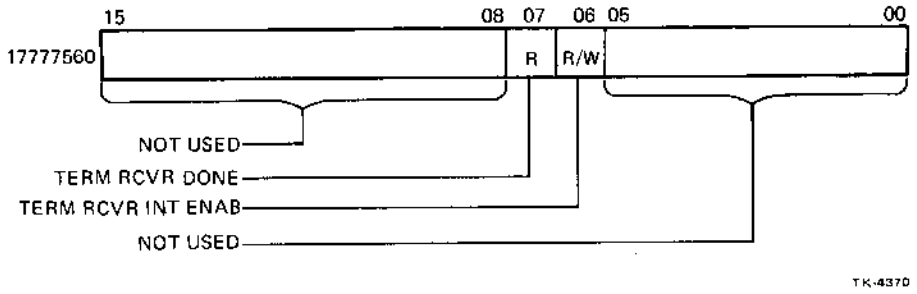


Figure 2-5 Console Terminal RCSR Format

Table 2-18 Console Terminal RCSR Bit Descriptions

Bit	Description
15:08	Not used.
07	Terminal Receiver Done – A read-only bit that is set to 1 during the program I/O mode when a complete character is contained in the console terminal RBUF. Cleared when the RBUF is addressed and when an initialize operation occurs.
06	Terminal Receiver Interrupt Enable – A read/write bit, set to 1 to allow the interrupt sequence to be initiated when the RCVR DONE bit is set.
05:00	Not used.

2.3.2.2 Console Terminal, Receiver Data Buffer (RBUF) – Figure 2-6 shows the format of the console terminal receiver data buffer register and Table 2-19 lists and describes the function of the bits.

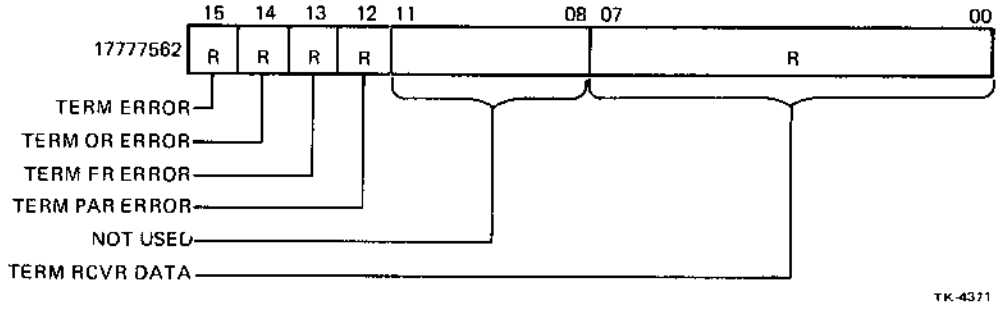


Figure 2-6 Console Terminal RBUF Format

Table 2-19 Console Terminal RBUF Bit Descriptions

Bit	Description
15	Terminal Error – A read-only bit that is set to 1 when the TERM OR ERROR (bit 14), the TERM FR ERROR (bit 13), or the TERM PAR ERROR (bit 12) is set to 1. Cleared by an initialize operation or by the reception of new and correct data.

Table 2-19 Console Terminal RBUF Descriptions (Cont)

Bit	Description
14	Terminal Overrun Error – A read-only bit that is set to 1 if the character in the RBUF has not been read before another character is received. Cleared by an initialize operation or when the RBUF is emptied.
13	Terminal Framing Error – A read-only bit that is set to 1 when the character read does not include a valid stop bit(s). Cleared when a valid character is received. This bit may indicate an error in transmission or the reception of a "break" character.
12	Terminal Parity Error – A read-only bit that is set to 1 when the parity of the data in the RBUF is incorrect relative to the parity mode selected. This indicates an error in transmission. Cleared when the parity of the next character is validated.
11:08	Not used.
07:00	Terminal Receiver Data – Read-only bits that is the data character that was read from the terminal.

2.3.2.3 Console Terminal Transmitter Control/Status Register (XCSR) – Figure 2-7 shows the format of the console terminal transmitter control and status register (XCSR) and Table 2-20 lists the function of the bits.

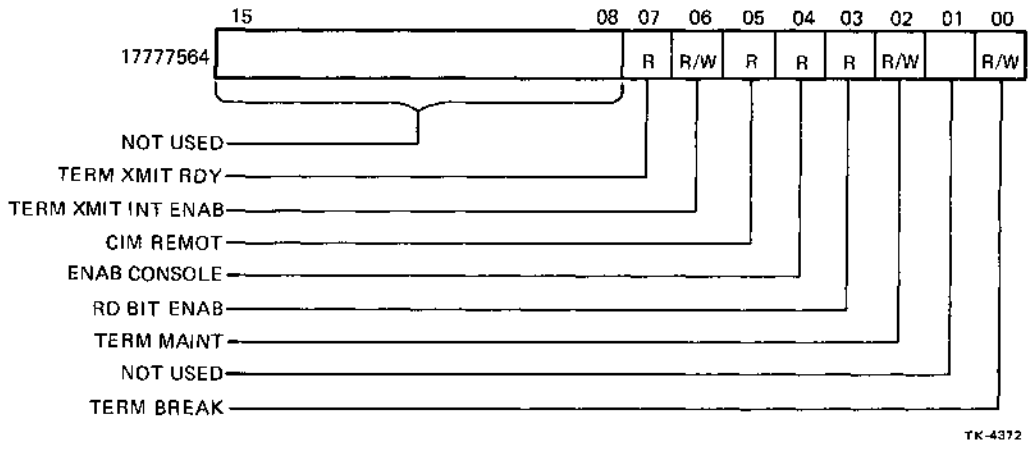


Figure 2-7 Console Terminal XCSR Format

Table 2-20 Console Terminal XCSR Bit Descriptions

Bit	Description
15:08	Not used.
07	Terminal Transmitter Ready – A read-only bit that is set to 1 when the console terminal XBUF register is ready to accept a character or when an initialize operation occurs. It initiates the interrupt sequence if the TERM XMIT INT ENB (bit 06) is set to 1. Cleared when the XBUF receives a character.
06	Terminal Transmitter Interrupt Enable – A read/write bit that is set to 1, by the program to enable the interrupt sequence to be initiated if the TERM XMIT RDY (bit 07) is set to 1. Cleared by program or by the initialize sequence.
05	Console Interface Remote – A read-only bit that is set to 1 when the CPU is operating in the remote diagnostic mode.
04	Enable Console – A read-only bit that is set to 1 by the program to indicate that the CPU is operating in the console mode.
03	Remote Diagnostic Bits Enable – A read-only bit set by switch S2 (E79) on the MFM module. When the switch is on, the status of bits 04 and 05 is entered into this register and when the switch is off, the bits will be zeros.
02	Terminal Maintenance – A read/write bit which, when set to 1 by the program, will cause a closed loop test of the console terminal UART. The serial output of the XBUF will be returned to serial input of the RBUF. The data transfer rate will be at the baud rate of the transmitter. Cleared by an initialize operation or by the program.
00	Terminal Break – A read/write bit that is set to 1 by the program and causes the transmission of a continuous space character. This will cause a framing error (bit 13) of the RBUF to be set. Cleared by the program or by an initialize sequence. Can be disabled permanently by removing the jumper lead W5 on the MFM module.

2.3.2.4 Console Terminal Transmitter Buffer Register (XBUF) – Figure 2-8 shows the format of the console terminal transmitter buffer register (XBUF) and Table 2-21 lists the function of the bits.

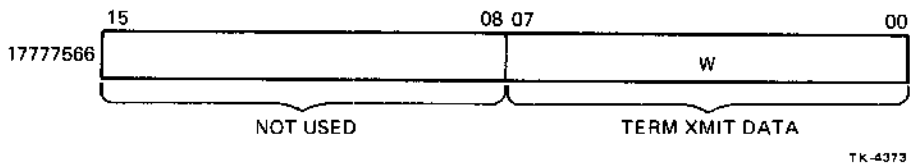


Figure 2-8 Console Terminal XBUF Format

Table 2-21 Console Terminal (XBUF) Bit Descriptions

Bit	Description
15:08	Not used.
07:00	Terminal Transmitter Data – These are write-only bits which form the data character to be transferred to the console terminal.

2.3.2.5 TU58 Receiver Control/Status Register (RCSR) – Figure 2-9 shows the format of the TU58 receiver control/status register (RCSR) and Table 2-22 lists the function of the bits. The typical addresses assigned to the TU58 registers are from 17776500 to 17776506.

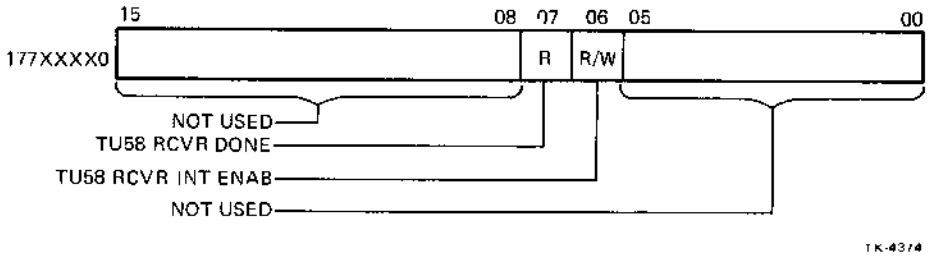


Figure 2-9 TU58 RCSR Format

Table 2-22 TU58 RCSR Bit Descriptions

Bit	Description
15:08	Not used.
07	TU58 Receiver Done – A read-only bit that is set to 1 during the program I/O mode only when a complete character is contained in the TU58 RBUF. Cleared when the TU58 RBUF is addressed or when an initialize operation occurs. Initiates the interrupt sequence when the TU58 RCVR INT ENAB bit (06) is set to 1.
06	TU58 RCVR Interrupt Enable – A read/write bit which is set to 1 by the program to allow the interrupt sequence to be initiated by the TU58 RCVR DONE bit (07).
05:00	Not used.

2.3.2.6 TU58 Receiver Buffer Register (RBUF) – Figure 2-10 shows the format of the TU58 receiver buffer register (RBUF) and Table 2-23 lists the function of the bits.

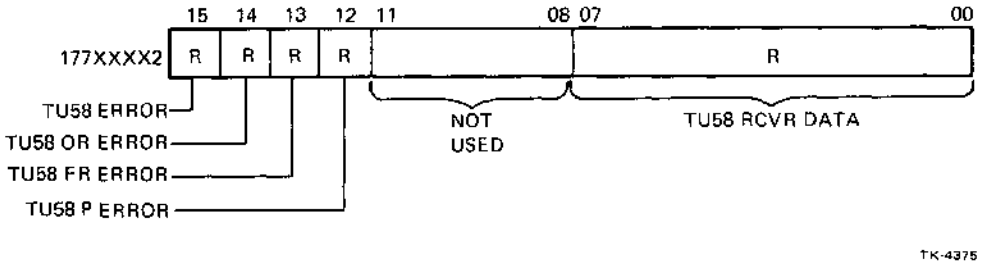


Figure 2-10 TU58 RBUF Format

Table 2-23 TU58 RBUF Bit Descriptions

Bit	Description
15	TU58 Error – A read-only bit that is set to 1 when the TU58 OR ERROR (bit 14), TU58 FR ERROR (bit 13), or the TU58 PAR ERROR (bit 12) is set to 1. Cleared by an initialize operation or by the reception of new and correct data.
14	TU58 Overrun Error – A read-only bit that is set to 1 if the character in the RBUF has not been read before another character is received. Cleared by an initialize operation or when the RBUF is emptied.
13	TU58 Framing Error – A read-only bit that is set to 1 when the character read in the RBUF does not have a valid stop bit(s). Cleared when a valid character is received. This bit may indicate an error in transmission or the reception of a "break" character.
12	TU58 Parity Error – A read-only bit that is set to 1 when the parity of the character read in the RBUF is incorrect relative to the parity mode selected. Cleared when the parity of the next character is validated.
11:08	Not used.
07:00	TU58 Received Data – These are read-only bits that form the data character received from the TU58.

2.3.2.7 TU58 Transmitter Control/Status Register (XCSR) – Figure 2-11 shows the format of the TU58 transmitter control/status register (XCSR) and Table 2-24 lists the functions of the bits.

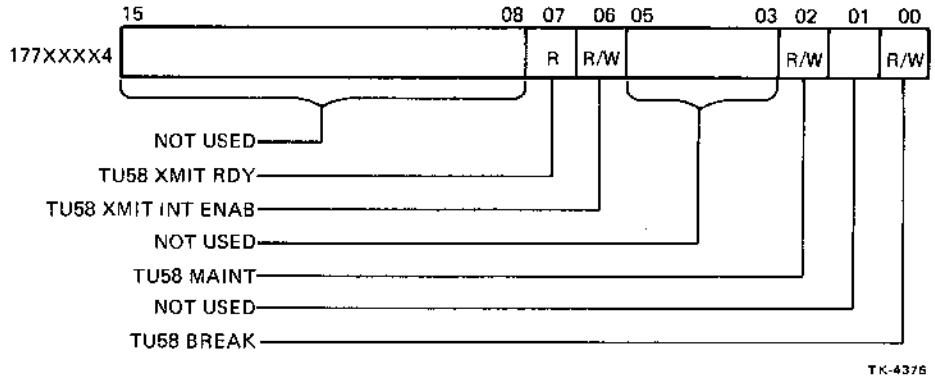


Figure 2-11 TU58 XCSR Format

Table 2-24 TU58 XCSR Bit Descriptions

Bit	Description
15:08	Not used.
07	TU58 Transmitter Ready – A read-only bit that is set to 1 when the TU58 XBUF is ready to accept a character or when an initialize operation occurs. Setting the bit initiates an interrupt sequence if the TU58 XMIT ENAB (bit 06) is set to 1. Cleared when a character is written into the XBUF.
06	TU58 Transmitter Interrupt Enable – A read/write bit that is set to 1 by the program. Enables the interrupt sequence to be initiated if the TU58 XMIT RDY (bit 07) is set to 1. Cleared by the program or by the initialize sequence.
05:03	TU58 Maintenance – A read/write bit that when set to 1 by the program will cause a closed loop test of the TU58 UART. The serial output of the transmitter will be returned to the serial input of the receiver. The data transfer rate will be the baud rate of the transmitter. Cleared by the program or by an initialize operation.
01	Not used.
00	TU58 Break – A read/write bit that is set to 1 by the program and that causes a space character to be continuously transmitted to the TU58. Cleared by the program or by an initialize sequence. The break function can be permanently disabled by removing jumper lead W10 on the MFM module.

2.3.2.8 TU58 Transmitter Data Buffer (XBUF) Register – Figure 2-12 shows the format of the TU58 transmitter buffer register (XBUF) and Table 2-25 lists the functions of the bits.

2.3.2.9 Signal Register – The signal register provides information about the operational status of the MFM module and CPU. Figure 2-13 shows the format of the signal register and Table 2-26 lists the function of the bits.

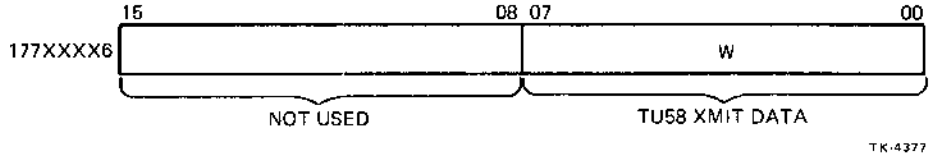


Figure 2-12 TU58 XBUF Format

Table 2-25 TU58 XBUF Bit Descriptions

Bit	Description
15:08	Not used.
07:00	TU58 Transmitter Data – These are write-only bits that form the data character to be transferred to the TU58.

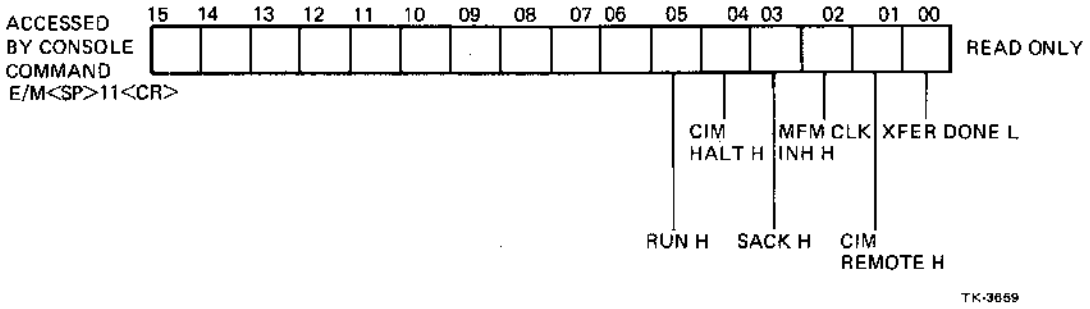


Figure 2-13 Signal Register Format

Table 2-26 Signal Register Bit Descriptions

Bit	Description
15:06	Not used.
05	Run – Set to 1 to indicate that the processor is executing instructions.
04	Console Interface Module Halt – Set to 1 to indicate that the toggle switch on the control panel of the PDP-11/44 is in the HALT position.
03	Selection Acknowledge – Set to 1 to indicate that a device has acknowledged the bus grant.
02	Multifunction Module Clock Inhibit – Set to 1 when the MFM is inhibiting the operation of the CPU clock.
01	Console Interface Module Remote – Set to 1 when the CPU is operating in the remote mode.
00	Transfer Done – Not used.

2.3.2.10 Line Time Clock Control/Status Register (LKS) – Figure 2-14 shows the format of the Line Time Clock Control Status Register (LKS) and Table 2-27 lists the functions of the bits.

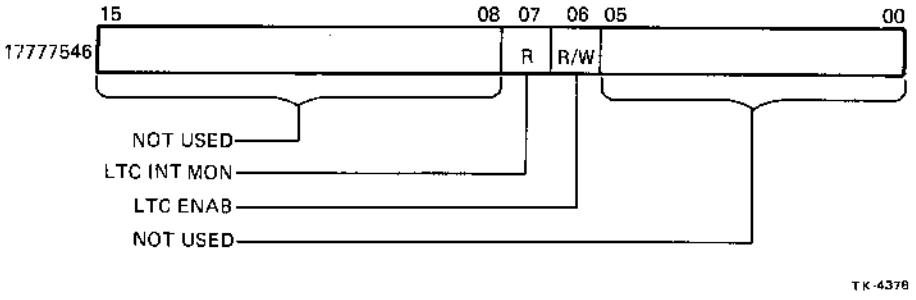


Figure 2-14 Line Time Clock (TCSR) Format

Table 2-27 Line Time Clock LKS, Bit Descriptions

Bit	Description
15:08	Not used.
07	Line Time Clock Monitor – A read-only bit set to 1 for each cycle of the ac voltage and cleared by the program. Provides an interrupt request at an interval of 16.66 ms for the 60 Hz version and 20 ms for the 50 Hz version. Also set during the initialize sequence.
06	Line Time Clock Interrupt Enable A read-write bit set to 1 by the program to allow the interrupt sequence to be initiated when the LTC MON (bit 07) is set.
05:00	Not used.

2.3.3 Cache Memory I/O, Page Registers

The cache memory module (KK11-B) contains several registers that are used to store data information, error indications, and control and status information.

2.3.3.1 Cache Memory Data Register (CDR) – The cache memory data register (CDR) is loaded from the 16-bit data array section of the cache RAM when a read-access occurs to main memory. Figure 2-15 shows the CDR format and Table 2-28 lists the functions of the bits.

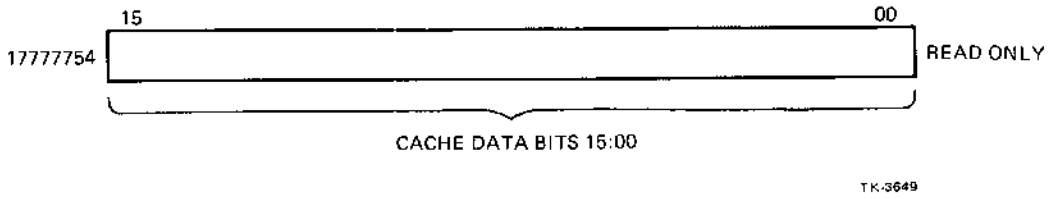


Figure 2-15 Cache CDR Format

Table 2-28 Cache CDR Bit Descriptions

Bit	Description
15:00	These bits are read-only and are loaded from the 16-bit data array section of the cache RAM on every read-access to main memory, except the top 256K bytes. This register can be used with the hit-on-destination-only bit to aid the cache diagnostics in identifying failures in the data section of the cache array.

2.3.3.2 Cache Hit Register (CHR) – The cache hit register (CHR) is a dual-purpose register used as an address match register when written and as a tag address/hit register when read. Figure 2-16 shows the CHR format and Table 2-29 lists the functions of the bits.

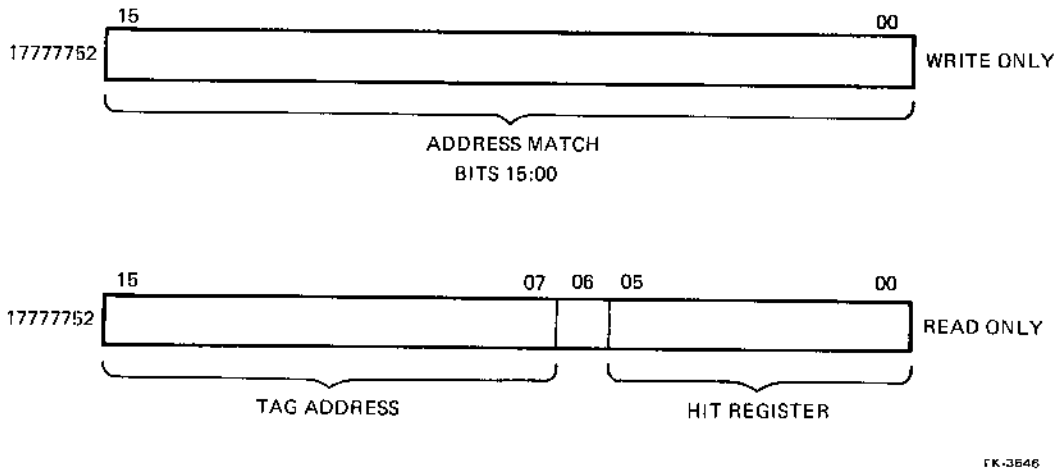


Figure 2-16 Cache CHR Format

Table 2-29 Cache CHR Bit Descriptions

Bit	Description
15:00	Address Match Bits 15:00 – These write-only bits correspond to bits 15:00 of the address match register. Bits 21:16 of the address match register are contained in the cache maintenance register. When bits 21:00 of the address match register are the same as memory address lines 21:00, bit 3 of the CMR is set, a sync pulse is provided to a user-accessible test point and the address match LED is lite. When bit 4 of the CMR is set, the processor clock is stopped. When bit 2 of the CMR is set, the processor is halted.
15:07	Tag Address – These read-only bits contain the nine tag store memory bits of the last main memory access. When used in conjunction with bits 01 and 00 of the cache maintenance register, the tag address bits will allow cache diagnostics to read the tag field of any location in the array.
06	Not used.
05:00	Hit Register – These read-only bits indicate the number of read and write cache hits on the last processor accesses to non-I/O page memory. These bits flow from the LSB to MSB of the field with a 1 indicating a hit and a 0 indicating a miss.

2.3.3.3 Cache Maintenance Register (CMR) – The cache maintenance register (CMR) is a dual-purpose register. The high byte is used as an address match register when written and contains maintenance bits when read. The lower byte contains read/write maintenance bits. Figure 2-17 shows the format of the CMR and Table 2-30 lists the function of the bits.

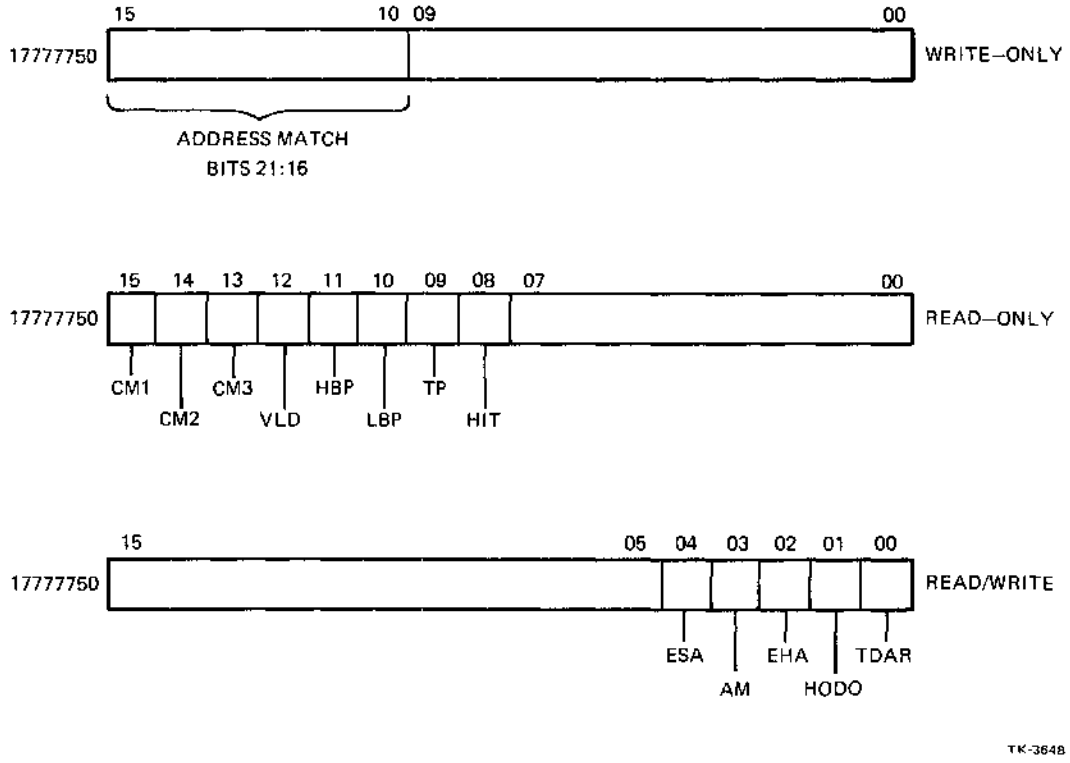


Figure 2-17 Cache CMR Format

Table 2-30 Cache CMR Bit Descriptions

Bit	Description
15:10	Address Match Bits 21:16 – These write-only bits correspond to bits 21:16 of the address match register. Bits 15:00 of the address match register are contained in the cache hit register. When bits 21:00 of the address match register are the same as memory address lines 21:00, a sync pulse is provided to a user-accessible test point.
15:13	Compare 3:1 – These read-only bits represent the value of the compare lines of the cache hit detect logic. when these bits are set, it indicates that the 9-bit tag field currently being read matches the upper 9 bits of the PAX address (bits 21:13).
12	Valid – This read-only bit, when set, indicates that the word currently being read from cache is a valid copy of a backing store location.

Table 2-30 Cache CMR Bit Descriptions (Cont)

Bit	Description
11:09	High Parity, Low Parity, Tag Parity – These read-only bits indicate the parity of the high byte of the data field, low byte of the data field, and the tag field, respectively.
08	Hit – This read-only bit, when set, indicates that all the conditions necessary for a processor-read hit have been met.
04	Enable Stop Action – This read/write bit, when set, will cause the processor clock to stop when a cache parity error or address match condition is detected.
03	Address Matched – This read/write bit is set when the 22-bit address match register is equal to the 22-bit PAX address.
02	Enable Halt Action – This read/write bit, when set, will cause a processor halt upon detection of a cache parity error or address match condition.
01	Hit on Destination Only – This read/write bit, when set, causes the cache to be enabled only during the destination memory access portion of an instruction. Read hits and updates will occur only during the final destination access.
00	Tag Data from Address Match Register – This read/write bit, when set, enables the tag field of the cache to be written with data from bits 08:00 of the address match register. When this bit is set, all cache writes will cause the valid bit to be cleared in that location.

2.3.3.4 Cache Control/Status Register (CCSR) – Figure 2-18 shows the format of the cache (CCSR) and Table 2-31 lists the functions of the bits.

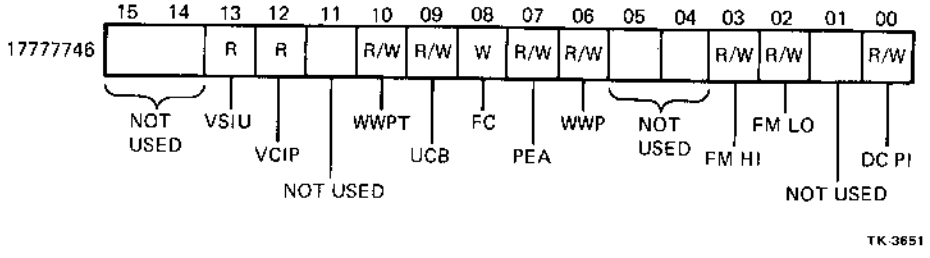


Figure 2-18 Cache CCSR Format

Table 2-31 Cache CCSR Bit Descriptions

Bit	Description
15:14	Not used.
13	Valid Store in Use – This read-only bit controls which set of valid store bits is currently being used to determine the validity of the contents of the tag store memory. When this bit is set to 1, valid bit B is in use; when clear, bit A is in use. This bit is complemented each time the cache is flushed.
12	Valid Clear in Progress – This read-only bit, when set, indicates that the cache is currently in the process of clearing a valid store set. A cache clear cycle is initiated on powerup and when the flush cache bit is set.
11	Not used.
10	Write Wrong Parity Tag – This read/write bit, when set, causes tag parity bits to be written with wrong parity on processor read misses and write hits. This will cause a parity error to occur on the next access to that location. This feature is used by the cache diagnostic programs.
09	Unconditional Cache Bypass – This read/write bit, when set, will force all memory references by the processor to go to main memory. Read or write hits will result in invalidation of those locations in cache, and misses will not change the contents.
08	Flush Cache – This write-only bit, when set, will cause the entire contents of the cache to be declared invalid.
07	Parity Error Abort – This read/write bit controls the response of cache to a parity error. When this bit is set, a cache parity error will cause a force miss and an abort to occur. When cleared, this bit inhibits the abort and enables an interrupt to parity error vector 114. All cache parity errors result in force misses.
06	Write Wrong Parity Data – This read/write bit, when set, causes high and low parity bytes to be written with wrong parity on all updates (processor read misses and write hits). This will cause a cache parity error to occur on the next access to that location. This feature is used in the cache diagnostic programs.
05-04	Not used.
03	Force Miss High – This read/write bit, when set, causes a forced miss on CPU reads where bit 12 of the location's address is a 1. This bit can also be set by a toggle switch (S1) on the cache board. When switch S1 is returned to the cache-on position, bit 03 remains set until cleared by the program or by an initialization.

Table 2-31 Cache CCSR Bit Descriptions (Cont)

Bit	Description
02	Force Miss Low – This read/write bit, when set, causes a forced miss on CPU read operations when bit 12 of the location's address is a 0. This bit can also be set by a toggle switch (S2) on the cache board. When switch S2 is returned to the cache-on position, bit 02 remains set until cleared by the program or by an initialization. Setting both bits 03 and 02 will cause all CPU read operations to be misses thereby effectively disabling the cache.
01	Not used.
00	Disable Cache Parity Interrupt – This read/write bit, when set, overrides the cleared condition of the parity error abort bit (bit 07), thereby disabling the interrupt to location 114. The following shows the relationship between bits 00 and 07 and the effect on cache parity errors.

Bit 07	Bit 00	Result
0	0	Interrupt to location 114 and force miss
0	1	Force miss only
1	0/1	Abort and force miss

2.3.3.5 Cache Error Register (CME) – Figure 2-19 shows the format of the cache CME register and Table 2-32 lists the functions of the bits.

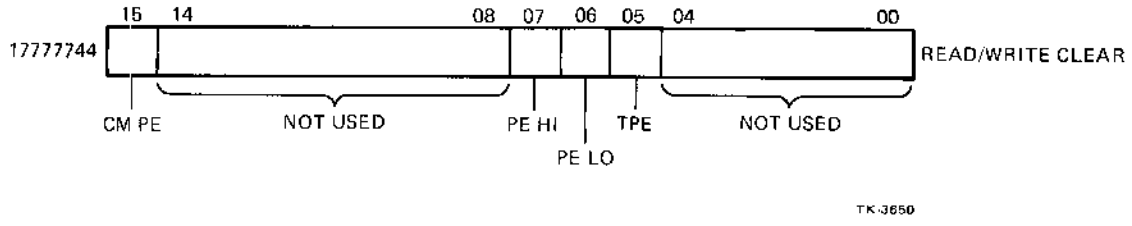


Figure 2-19 Cache CME Format

Table 2-32 Cache CME Bit Descriptions

Bit	Description
15	Cache Memory Parity Error - This bit is set if a cache parity error is detected while the cache parity abort bit (control register bit 07) is set or if a memory parity error occurs. If this bit is set, the cache will force a miss. This bit is cleared by any write to the cache memory error register or by a console INIT.
14:08	Not used.
07	Parity Error High Byte – Set to 1 when a parity error occurs in the high byte of data and the PEA (bit 07) of the CSSR is set to 1. If the cycle is not aborted (PEA = 0), bit 06:05 of the CME will also be set by this error. All parity bits are cleared by a write operation to the CME or by a console INIT.
06	Parity Error Low Byte – Set to 1 when a parity error occurs in the low byte of the cache data, and the PEA (bit 07) of the CCSR is set to 1. If the cycle is not aborted (PEA = 0), bits 07 and 05 will also be set to 1 by this error.
05	Tag Parity Error – Set to 1 when a parity error occurs in the tag address field of the CHR, and the PEA (bit 07) of the CCSR is set to 1. If the cycle is not aborted (PEA = 0), bits 06 and 07 of the CME will also be set to 1. All parity bits are cleared by a write operation to the CME or by a console INIT.
04:00	Not used.

2.3.4 Memory Management Registers

The 16-bit virtual address is translated to a 22-bit physical address by the memory management function. Four status registers, 48-page address registers (PAR), and 48-page descriptor registers (PDR) are associated with the memory management.

2.3.4.1 Status Register 0 (SR0) – Memory management status register 0 (SR0) contains error flags, the page number whose reference caused the abort and various status flags. The format of SR0 is shown in Figure 2-20 and bit descriptions are listed in Table 2-33.

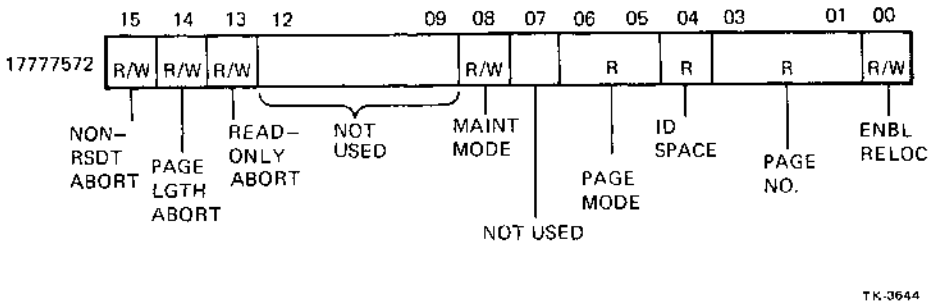


Figure 2-20 Memory Management SR0 Format

Table 2-33 SR0 Bit Descriptions

Bit	Description
15:13	Error Flags – These error bits are prioritized; i.e., flags to the right are less significant and are ignored if a flag to the left is present. For example, a nonresident fault service routine would ignore page length and access control faults.
15	Nonresident Abort – This bit is set to 1 when an attempt to access a page with an access control field (ACF) key equal to 0. It is also set if there is an attempt to use memory relocation with a processor mode of 2.
14	Page Length Abort – This bit is set to 1 if there is an attempt to access a location in a page with a block number (virtual address bits 12:06) that is outside the area authorized by the page length field (PLF) of the page descriptor register (PDR) for that page. It is also set if there is an attempt to use memory relocation with a processor mode of 2. Bits 15 and 14 can be set simultaneously by the same access attempt.
13	Read-Only Abort – This bit is set if there is an attempt to write in a read-only page. Read-only pages have an access key of 1.
12:09	Not used.
08	Maintenance/Destination Mode – This bit, when set, specifies that only destination mode references will be relocated using memory management. This bit is used for diagnostic purposes only.
07	Not used.
06:05	Page Mode – These bits indicate the processor mode (kernel/supervisor/user) associated with the page causing the abort; kernel = 00, supervisor = 01, user = 11, illegal mode = 10. If an illegal mode is specified, bits 15 and 14 will be set.
04	I/D SPACE – This bit indicates the type of address space (I or D) the memory management was using when the fault occurred; 0 = I space, 1 = D space.
03:01	Page Number – These bits contain the page number of the reference causing a memory management fault.
00	Enable Relocation – When this bit is set, all addresses are relocated. When this bit is clear, the memory management facility is inoperative and addresses are not relocated or protected.

2.3.4.2 Status Register SR1 – The format of memory management status register 1 (SR1) is shown in Figure 2-21. SR1 records any autoincrement/decrement of the general purpose register, including explicit references through the PC. SR1 is cleared at the beginning of the fetch cycles for each instruction. Whenever a general purpose register is either autoincremented or autodecremented, the register number and the amount in 2's complement notation by which the register was modified are written into SR1. A single operand instruction will only set the lower byte with the source register change and the upper byte with the destination register change. Table 2-34 describes each of the bits in the SR1.

2.3.4.3 Status Register SR2 – The status register SR2 is loaded with the value of the program counter at the beginning of the fetch cycle of each instruction.

At the beginning of an interrupt, SR2 contains the address trap vector, the T bit, parity traps, odd address, parity and time-out aborts. Figure 2-22 shows the format of SR2 and Table 2-35 lists the function of the bits.

2.3.4.4 Status Register SR3 – Figure 2-23 shows the format of SR3 and Table 2-36 describes the bits.

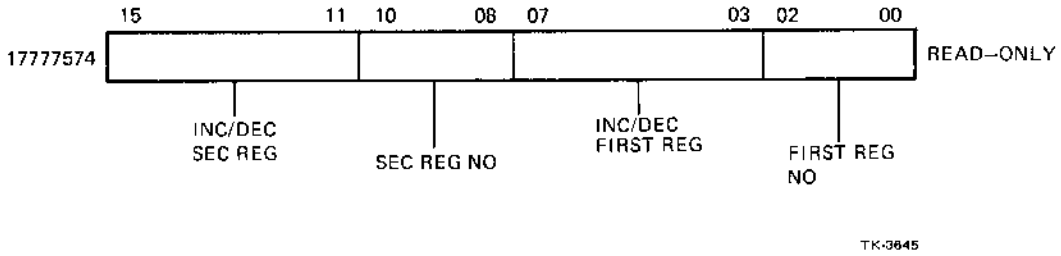


Figure 2-21 Memory Management SR1 Format

Table 2-34 SR1 Bit Descriptions

Bit	Description
15:11	Increment/Decrement Second Register – The 2's complement value of the incrementing or decrementing of the second general register.
10:08	Second Register Number – The octal value of the second general register number (octal 0 for register 0).
07:03	Increment/Decrement First Register – The 2's complement value that is a result of the incrementing or decrementing of the first general register.
02:00	First Register Number – The octal value of the first general register.

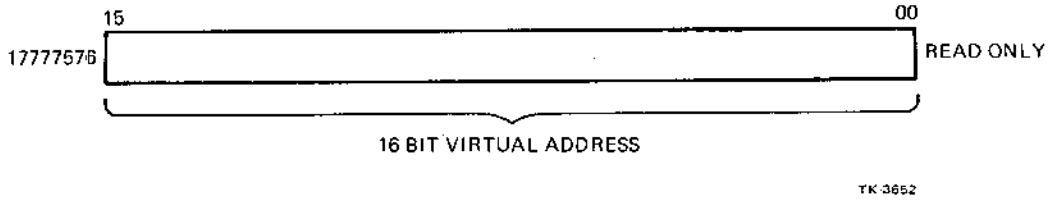


Figure 2-22 Memory Management SR2 Format

Table 2-35 SR2 Bit Description

Bit	Description
15:00	Virtual Address – Read-only bits that are the virtual address at the beginning of the fetch cycle of each instruction.

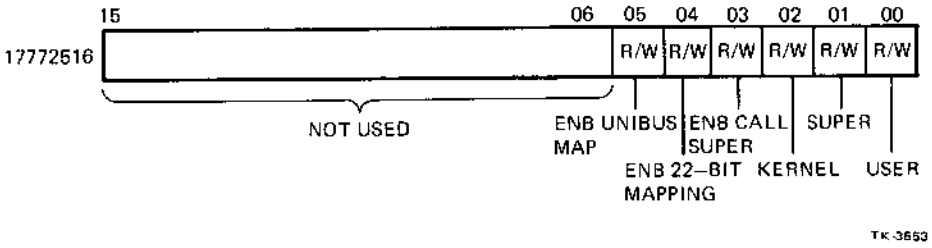


Figure 2-23 Memory Management SR3 Format

Table 2-36 SR3 Bit Descriptions

Bit	Description
15:06	Not used.
05	Enable UNIBUS Map – Set to 1 by program control to enable the UNIBUS map which converts 18-bit UNIBUS addresses to 22-bit memory addresses.
04	Enable 22-Bit Mapping – Set to 1 by program control to enable 22-bit mapping when the ENBL RELOC (bit 01) of SR0 is set to 1. When cleared to 0, 18-bit mapping is enabled.

Table 2-36 SR3 Bit Descriptions (Cont)

Bit	Description
03	Enable Call Supervisor – Set to 1 by program to enable the CALL TO SUPERVISOR MODE instruction to be performed.
02	Kernel – Set to 1 by program control to enable kernel mode D space.
01	Supervisor – Set to 1 by program control to enable supervisor mode D space.
00	User – Set to 1 by program control to enable data space in the user mode. When data space is disabled, all references use the instruction (I) space registers. When D space is enabled, either the I space or the D space registers are used.

2.3.4.5 Page Address Registers (PAR) – The page address registers (PAR) contain the 16-bit page address field that specifies the base address of the page as a block number in physical memory. Figure 2-24 shows the format of a PAR and Table 2-37 describes the bits.

2.3.4.6 Page Descriptor Register (PDR) – The page descriptor registers (PDRs) contain information relative to page expansion, page length and access control. There are six sets of eight PDRs which are allocated in the same manner as the PARs. The addresses of these registers are listed in Table 2-38. The format of the PDR is shown in Figure 2-25 and bit descriptions are listed in Table 2-39.

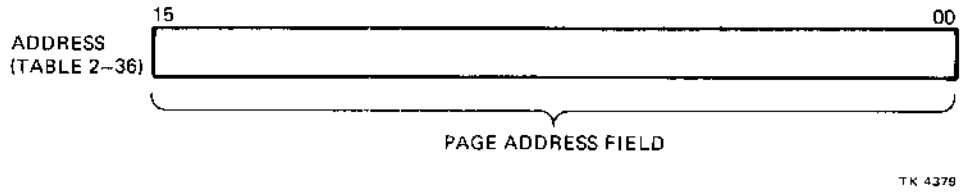


Figure 2-24 Memory Management PAR Format

Table 2-37 PAR Bit Description

Bit	Description
15:00	Page Address Field – Read/write bits that are the page address field. There are six sets of eight PARs, one set each for kernel data space, kernel instruction space, supervisor data space, supervisor instruction space, user data space and user instruction space. The addresses of these registers are listed in Table 2-38.

Table 2-38 PAR/PDR UNIBUS Addresses

I Space			D Space		
No.	PAR	PDR	No.	PAR	PDR
		Kernel			
0	17 772 340	17 772 300	0	17 772 360	17 772 320
1	17 772 342	17 772 302	1	17 772 362	17 772 322
2	17 772 344	17 772 304	2	17 772 364	17 772 324
3	17 772 346	17 772 306	3	17 772 366	17 772 326
4	17 772 350	17 772 310	4	17 772 370	17 772 330
5	17 772 352	17 772 312	5	17 772 372	17 772 332
6	17 772 354	17 772 314	6	17 772 374	17 772 334
7	17 772 356	17 772 316	7	17 772 376	17 772 336
		Supervisor			
0	17 772 240	17 772 200	0	17 772 260	17 772 220
1	17 772 242	17 772 202	1	17 772 262	17 772 222
2	17 772 244	17 772 204	2	17 772 264	17 772 224
3	17 772 246	17 772 206	3	17 772 266	17 772 226
4	17 772 250	17 772 210	4	17 772 270	17 772 230
5	17 772 252	17 772 212	5	17 772 272	17 772 232
6	17 772 254	17 772 214	6	17 772 274	17 772 234
7	17 772 256	17 772 216	7	17 772 276	17 772 236
		User			
0	17 772 640	17 772 600	0	17 772 660	17 772 620
1	17 772 642	17 772 602	1	17 772 662	17 772 622
2	17 772 644	17 772 604	2	17 772 664	17 772 624
3	17 772 646	17 772 606	3	17 772 666	17 772 626
4	17 772 650	17 772 610	4	17 772 670	17 772 630
5	17 772 652	17 772 612	5	17 772 672	17 772 632
6	17 772 654	17 772 614	6	17 772 674	17 772 634
7	17 772 656	17 772 616	7	17 772 676	17 772 636

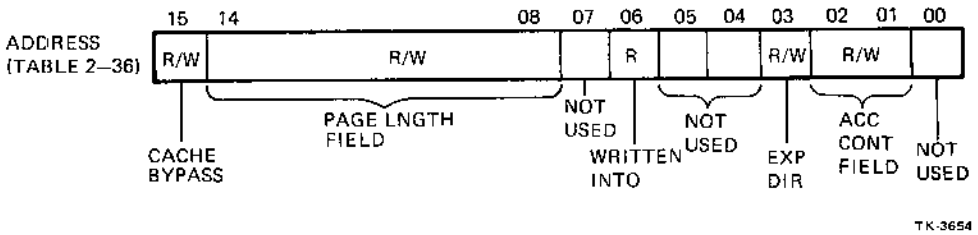


Figure 2-25 Memory Management PDR Format

Table 2-39 PDR Bit Descriptions

Bit	Description
15	Cache Bypass – When set to 1 by the program, this bit will cause all references to this page to bypass the cache memory and directly access the main memory.
14:08	Page Length Field – Specifies the octal number of 32-word blocks in the current page. The block number of the virtual address is compared to the page length field to detect length errors. An error occurs when expanding upwards if the block number is greater than the page length field, and when expanding downwards if the block number is less than the page length field.
07	Not used.
06	Page Written Into – This bit is set to 1 to indicate to the program that the page being accessed was modified since the PAR or PDR was loaded. This bit is used in applications that involve disk swapping and memory overlays. It determines which pages have been modified and must be saved in their new form, and which pages have not been modified and can be overlaid and not saved.
05:04	Not used.
03	Expansion Direction – Specifies the direction in which a page is authorized to expand. When cleared to 0, the page expands upward from relative 0 by adding blocks with higher memory addresses. When set to 1, the page expands downward from block number 177_8 or 127_{10} by adding blocks with lower addresses. Upward expansion is usually used for program space while downward expansion is used for stack space.
02:01	Access Control Field – A two-bit field which defines the access rights for the addressed page as follows:

Bit 02	Bit 01	Function
0	0	Nonresident – abort all accesses
0	1	Read-only – abort all attempts to write
1	0	Unused – abort all accesses
1	1	Read/write – read or write allowed, no trap or abort occurs

00	Not used.

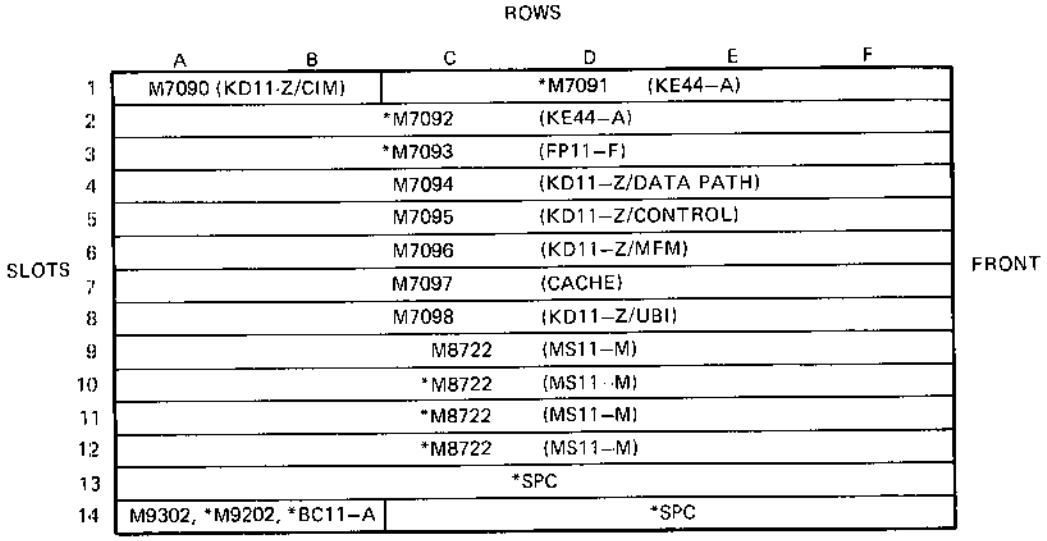
CHAPTER 3
CPU CONFIGURATION

The BA11-AA, -AB mounting box contains a 6-row, 14-column CPU backplane which is dedicated to the PDP-11/44 system modules. Space is provided within the mounting box to allow the installation of additional backplanes.

Some of the installed system modules contain switches and jumper leads which must be set or configured for particular system applications.

3.1 PROCESSOR BACKPLANE ASSIGNMENTS

Figure 3-1 shows the location of the modules within the system backplane. Row A is positioned toward the rear of the mounting box where the power supply is mounted. The asterisked (*) modules are optional and are not supplied with the basic system. Table 3-1 lists and describes the standard modules supplied with the system, and Table 3-2 lists the modules that are available as options.



*MODULE OPTIONS AVAILABLE (TABLE 3–2)

NOTES:

1. A G727, G7270 CARD IS REQUIRED IN ROW D OF ANY UNUSED SPC SLOT TO PROVIDE BUS GRANT CONTINUITY.
2. A G7273 CARD IS REQUIRED IN ROW C AND D OR ANY UNUSED SPC SLOT TO PROVIDE BUS GRANT CONTINUITY.
3. MODULES ARE INSERTED WITH COMPONENT SIDE TOWARD RIGHT SIDE OF BACKPLANE.

TK-4380

Figure 3-1 Backplane Module Locations

Table 3-1 Standard CPU Backplane Modules

Function	Description
CPU Modules	
KD11-Z	M7090 – Console Interface Module (CIM) M7094 – Data Path Module M7095 – Control Module M7096 – Multifunction Module (MFM) M7097 – Cache Memory Module M7098 – UNIBUS Interface Module (UBI)
Memory	
MS11-MB option	M8722 – 256 KB ECC MOS Memory
UNIBUS	M9302 – Bus Terminator Module

Table 3-2 Optional CPU Backplane Modules

Function	Description
Commercial Instruction Set Processor KE44-A	M7091 – Control Module M7092 – Data Path Module
Floating-Point Processor FP11-F	M7093 – Floating-Point Processor Module
Memory Expansion	
MS11-MC	Two M8722 Modules – a total of 512 KB of ECC MOS memory
MS11-MD	Three M8722 Modules – a total of 768 KB ECC MOS memory
UNIBUS Cable Assembly	BC11-A – connects the UNIBUS of the CPU backplane to a remote backplane
Bus Grant Continuity	G727, G7270, G7273 modules – inserted into unused slots to continue bus grant continuity

3.1.1 Backplane Assembly Pin Designations

The system backplane assembly consists of connector blocks mounted to a metal frame. The top of the backplane contains slots into which the module contacts are inserted. The bottom of the backplane provides the wirewrap pins. Figure 3-2 shows the wiring side of the system backplane that contains 14 slots (columns) and 6 rows (A–F). With the mounting box tilted to its servicing position, row F will be located at the top of the assembly and slot 1 (column) will be located at the right side when facing the wirewrap pins. Each slot has 36 pins associated with the slot connectors and a pin is identified by the row, slot, pin designation, and side of the pin row where it is located as shown.

Table 3-3 lists the voltages and signals supplied by connector P1. Table 3-4 lists the voltages distributed to the connector pins of the backplane and Table 3-5 lists the ground lead distribution.

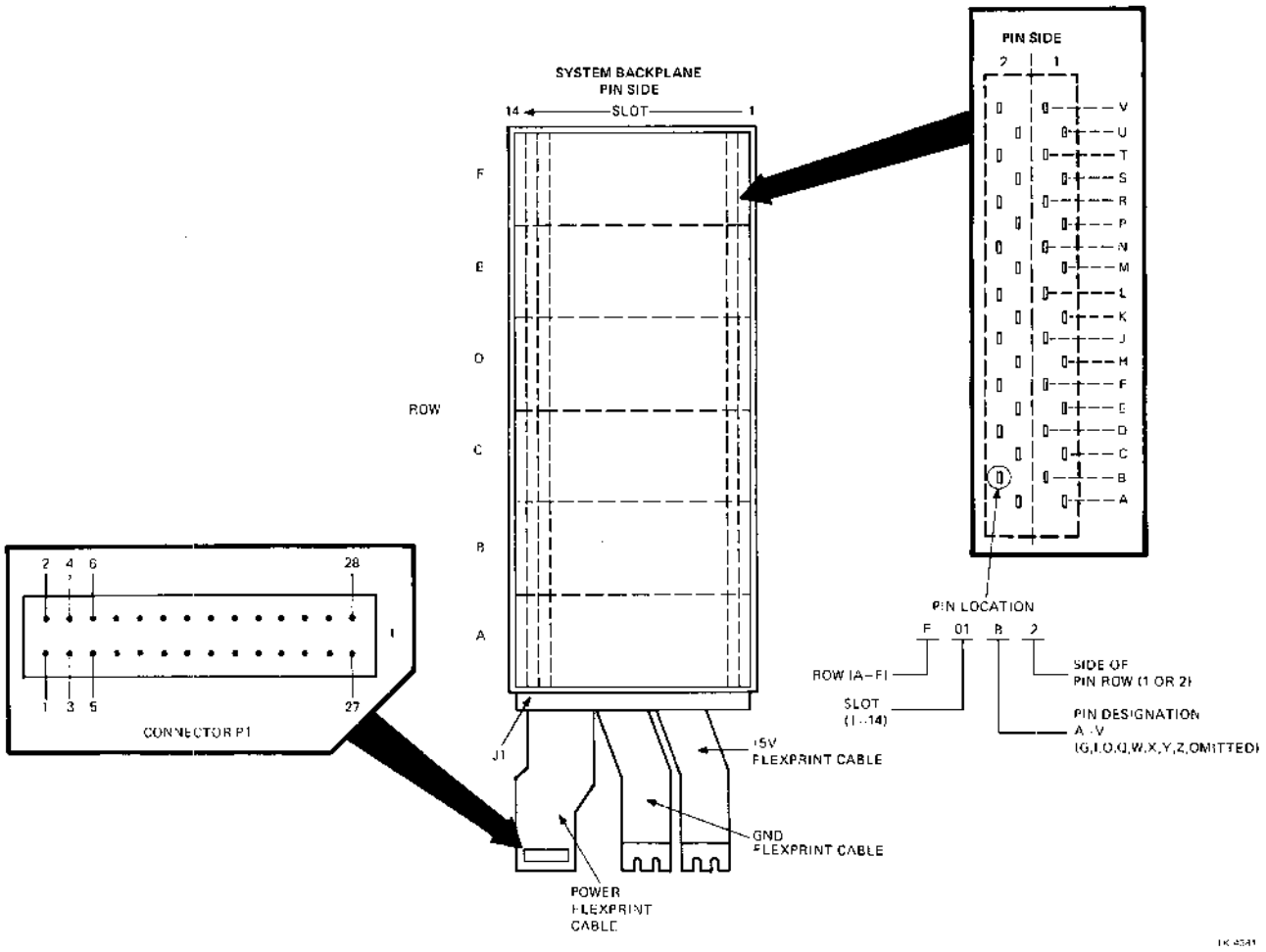


Figure 3-2 Backplane Assembly, Pin Designations

Table 3-3 CPU Backplane Connector P1, Signals and Voltages

Pin	Function
1–10	+5 VB
11–16	+12 VB
17, 18	−12 VB
19	LTC
20	BUS ACLO L
21	BOOT ENAB L
22	BUS DCLO L
23	GND SENSE
24	+5 SENSE
25, 27	−15 V
26, 28	+15 V

Table 3-4 CPU Backplane Voltage Distribution

Voltage	Connector Pin	Voltage	Connector Pin
+12	A01R1 A09R1 – A12R1	+5	B01B1, B09B1 – B012B1 B09D1 – B012D1
+12 VB	J1-11 to J1-15	+5 VB	J1-1 – J1-10
+15	B01C2 C06U1, C12U1 – C14U1 J1 – 26 – J1 – 28	−12	A01S1, A09S1 – A12S1
		−12 VB	J1-17, J1-18
+5	A01A2 – A014A2 A01V1 – A08V1 B01A2 – B14A2 C01A2 – C14A2 C01V1 – C08V1 J2-1, J1-24	−15 V	B01T1 C12B2 – C14B2 D12B2 – D14B2 E12B2 – E14B2 F12B2 – F14B2 J1-25, J1-27
+5–1	D01A2 – D14A2 D01V1, D02V1 E01A2 – E14A2 F01A2 – F14A2 F01V1 – F08V1		

Table 3-5 CPU Backplane Ground Distribution

Ground	Connector Pin	Ground	Connector Pin
GND 01	A01C2, A01T1 B01C1, B01T2 C01C2, C01T1 D01C2, D01T1 E01C2, E01T1 F01C2, F01T1 J00123	GND 08	A08C2, A08T1 B08C2, B08T1 C08C2, C08T1 D08C2, D08T1 E08C2, E08T1 F08C2, F08T1
GND 02	A02C2, A02T1 B02C2, B02T1 C02C2, C02T1 E02C2, E02T1 F02C2, F02T1	GND 09	A09C2, A09T1 B09C2, B09T1 C09C2, C09T1 D09C2, D09T1 E09C2, E09T1 F09C2, F09T1
GND 03	A03C2, A03T1 B03C2, B03T1 C03C2, C03T1 D03C2, D03T1 E03C2, E03T1 F03C2, F03T1	GND 10	A10C2, A10T1 B10C2, B10T1 C10C2, C10T1 D10C2, D10T1 E10C2, E10T1 F10C2, F10T1
GND 04	A04C2, A04T1 B04C2, B04T1 C04C2, C04T1 D04C2, D04T1 E04C2, E04T1 F04C2, F04T1	GND 11	A11C2, A11T1 B11C2, B11T1 C11C2, C11T1 D11C2, D11T1 E11C2, E11T1 F11C2, F11T1
GND 05	A05C2, A05T1 B05C2, B05T1 C05C2, C05T1 D05C2, D05T1 E05C2, E05T1 F05C2, F05T1	GND 12	A12C2, A12T1 B12C2, B12T1 C12C2, B12T1 D12C2, D12T1 E12C2, E12T1 F12C2, F12T1
GND 06	A06C2, A06T1 B06C2, B06T1 C06C2, C06T1 D06C2, D06T1 E06C2, E06T1 F06C2, F06T1	GND 13	A13C2, A13T1 B13C2, B13T1 C13C2, C13T1 D13C2, D13T1 E13A2, E13C2, E13T1 F13C2, F13T1, F13J2
GND 07	A07C2, A07T1 B07C2, B07T1 C07C2, C07T1 D07C2, D07T1 E07C2, E07T1 F07C2, F07T1	GND 14	A14B2, A14C2, A14N1, A14P1, A14R1, A14S1, A14T1, A14V1 B14B2, B14C2, B14D1, B14E1, B14T1, B14V2 F14C2, F14T1, F14J2

3.1.2 Module Contact Designations

Figure 3-3 shows the contact designations for a hex-height module. The contact designations for single-, double-, and quad-height modules will be similar starting with row A and proceeding to the maximum number of rows. When components are mounted on the module, they will be located on side 1.

3.1.3 SPC Module Installation

Slot 13, rows A through F, and slot 14, rows C through F of the system backplane, are allocated to the installation of small peripheral control (SPC) modules. The SPC modules provide control for the transfer of data between the CPU and peripheral devices. Slot 13 can contain a hex-height SPC module and slot 14 can contain a quad-height module. If no module is installed in an SPC slot, a G727 module must be inserted in row D to maintain the bus grant continuity of the backplane.

Some SPC modules allow block data transfers to or from a device without processor intervention. These modules use a nonprocessor grant (NPG) line of the UNIBUS to initiate the data transfers. The NPG line continuity is maintained by jumper wires wrapped to pins on the backplane.

When a module with NPG capability is installed in an SPC location, the jumper lead between pins A1 and B1 of row C must be removed. Figure 3-4 shows the location of the jumper wires on the backplane.

NOTE

When the NPG module is removed or when a module without the NPG capability is installed, the jumper lead must be connected to maintain the signal continuity.

Table 3-6 identifies the signals on the connector pins of row C through row D of the SPC locations. The XX designation in the "Pin" column of the table is slot 13 or 14 unless otherwise indicated.

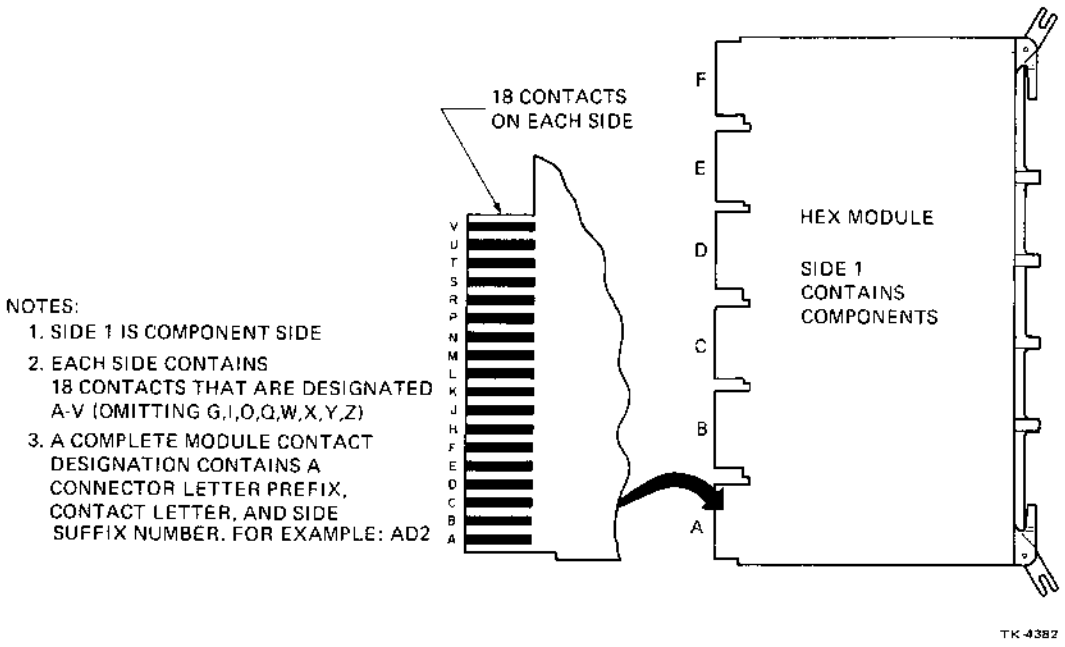


Figure 3-3 Module Contact Designations

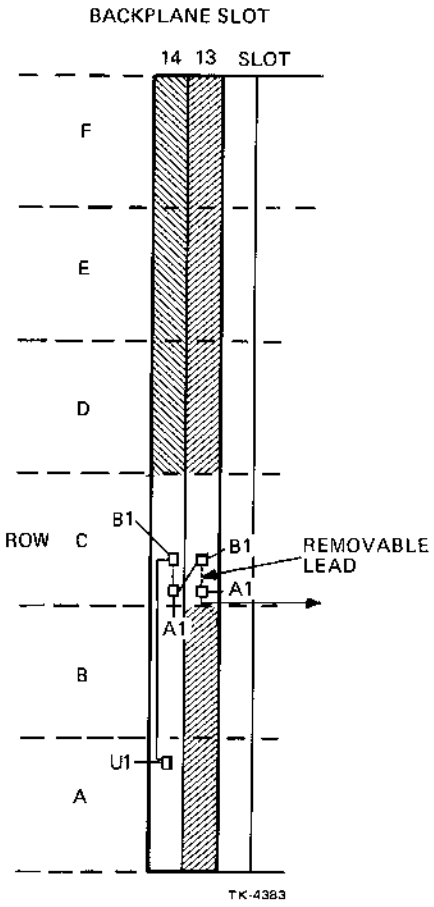


Figure 3-4 SPC Slots, NPG Jumper Lead Locations

3.2 MODULE CURRENT REQUIREMENTS

Table 3-7 lists the typical current requirements of the modules which can be inserted into the CPU backplane.

3.2.1 DC Power Requirements

The H7140-AA, -AB provides the dc power to the modules installed in the CPU backplane and any additional SPC backplane assemblies. The total amount of current available at the dc outputs of the power supply must be considered when installing additional modules to ensure that adequate power is available.

Table 3-6 SPC Location, Signal Identification

Pin	Signal Mnemonic	Pin	Signal Mnemonic
C(XX)A1		F1	SEL 0
A1	BUS NPG H (IN)	F2	BUS BR5 L
A2	+5 V	H1	IN
B1	−15 V	H2	BUS BR4 L
B2	BUS PA L	J1	SEL 2
C1	GND	J2	BR OUT
C2	LTC	K1	OUT H
D1	BUS D15 L	K2	UBA BG7 OUT H
D2		L1	BUS INIT L
E1	BUS D14 L	L2	BUS BG7A H
E2		M1	
F1	BUS D13 L	M2	MFM BG6 OUT
F2	BUS D11 L	N1	INT A
H1	BUS D12 L	N2	BUS BG6A H
H2	INT B	P1	
J1	BUS D10 L	P2	UBA BG5 OUT H
J2		R1	
K1	BUS D09 L	R2	BUS BG5A H
K2	INT ENB L	S1	
L1	BUS D08 L	S2	MFM BG4 OUT H
L2		T1	
M1	BUS D07 L	T2	BUS BG4A H
M2	BUS DCLO L	U1	
N1	BUS D04 L	U2	BG IN
N2		V1	SSYN IN H
P1	BUS D05 L	V2	BG OUT
P2		E(XX)A1	
R1	BUS D01 L	A1	
R2	BUS PB L	A2	SSYN IN H
S1	BUS D00 L	B2	
S2		C1	BUS A12 L
T1	BUS D03 L	C2	
T2		D1	BUS A17 L
U1	BUS D02 L	D2	BUS A15 L
U2		E1	BUS MSYN L
V1	BUS D06 L	E2	BUS A16 L
V2		F1	BUS A02 L
D(XX)A1		F2	BUS C1 L
A1		H1	BUS A01 L
A2		H2	BUS A00 L
B1	SEL 6	J1	BUS SSYN L
C1		J2	BUS CO L
C2	OUT LOW	K1	BUS A14 L
D1	BUS BR7 L	K2	BUS A13 L
D2	SEL 4	L1	BUS A11 L
E1	BUS BRG L	L2	
E2		M1	IN

Table 3-6 SPC Location Signal Identification (Cont)

Pin	Signal Mnemonic	Pin	Signal Mnemonic
M2	OUT H	F2	
N1	OUT LOW	H1	
N2	BUS A08 L	H2	INT ENB B
P1	BUS A10 L	J1	BUS NPR L
P2	BUS A07 L	J2	
R1	BUS A09 L	K1	
R2	SEL 4	K2	INT B
S1	SEL 6	L1	
S2	SEL 0	L2	F13L2 (F14L2)
T1		M1	BUS INTR L
T2	SEL 2	M2	F13M2 (F14M2)
U1	BUS A06 L	N1	F13N1 (F14N1)
U2	BUS A04 L	N2	
V1	BUS A05 L	P1	BR OUT
V2	BUS A06 L	P2	F13P2 (F14P2)
F(XX)A1	BR OUT	R1	F13L2 (F14L2)
A2		R2	F13N1 (F14N1)
B1	BG IN	S1	F13M2 (F14M2)
B2		S2	F13P2 (F14P2)
C1		T1	
C2		T2	BUS SACK L
D1	BUS BBSY	U1	INT A
D2	F13N1 (F14N1)	U2	BR OUT
E1	F13V2 (F14V2)	V1	INT ENB B
E2		V2	F13V2 (F14V2)
F1			

3.2.2 H7140-AA, -AB DC Power Output

Table 3-8 lists the total current supplied from the H7140-AA, -AB power supply. The current output of the +5.1 V output is derated by the amount of current required by the +15 V and −15 V outputs according to the following formula:

$$I_{+5.1\ V} = 120 - 5\ [(I_{+15\ V} - 1) + (I_{-15\ V} - 1)]$$

The maximum current supplied at the +5.1 Vdc output is 120 A with 1 A or less drawn from each of the +15 Vdc and −15 Vdc outputs. The minimum current available at the +5.1 Vdc output is 100 A where maximum current of 3 A is supplied at both the +15 Vdc and −15 Vdc outputs.

Table 3-9 lists some of the UNIBUS options that are available for use in the PDP-11/44 systems and the typical −15 V and +15 Vdc power requirements of the modules. Refer to the *PDP-11 Peripherals Handbook* and the *Terminals and Communications Handbook* for more detailed information on these options.

Table 3-7 CPU Module Current Requirements

Option (Modules)	DC Current +5.1 V	+12 V	−12 V	+5.1 BB
KD11-Z				
M7090	0.5 A			
M7094	7.5 A			
M7095	7.5 A			
M7096	5.0 A			
M7098	7.0 A			
KK11-B (M7097)	6.5 A			
FP11-F (M7093)	7.0 A			
KE44-A				
M7091	3.1 A			
M7092	6.0 A			
MS11-MB (M8722-BA)	4.8 A	1. A	50 mA	1.5 A
M9302	1.5 A			

Table 3-8 H7140-AA, -AB Power Supply Maximum Output Current

DC Outputs	Current in Amperes
+5.1 V*	120
+15 V	3
−15 V	3
+5.1 BB	10 (battery backup)
+12 V	5
−12 V	1

*Derated by the current drawn at the +15 and −15 Vdc outputs

3.3 MODULE SWITCHES, JUMPERS AND INDICATORS

Several of the modules provided with the PDP-11/44 system contain switches and jumper leads which must be set and configured for specific system requirements. The description of the switch and jumper lead configurations for the memory modules (M8722) is contained in the *MS11-M MOS Memory User's Guide*. Configuration information for the optional modules is contained in the respective documents listed in Table 1-2.

Table 3-9 −15 V, +15 Vdc Option Power Requirements

Option Designation	Current Requirements (Amperes) +15 Vdc	−15 Vdc
DH11-AD	0.40	0.65
DH11-AE	0.10	0.34
DL11-E	0.05	0.15
DL11-WA	0.05	0.15
DL11-WB	0.05	0.15
DMC11-DA	0.03	0.31
DMC11-FA	0.03	0.31
DMC11-MA	0.18	0.46
DMC11-MD	0.18	0.46
DUP11-DA	0.08	0.08
DV11-AA	0.60	1.00
DZ11-A	0.10	0.13
DZ11-B	0.10	0.13
DZ11-C	0.12	0.40
DZ11-D	0.12	0.40
DZ11-E	0.20	0.26
DZ11-F	0.24	0.80
RJM02, RJP06, TJE16, TJU77	0.00	0.40
RK711-PA	0.18	0.40
RL11-AK, RL211-AK	0.50	0.50

3.3.1 Console Interface Module (M7090)

The console interface module (CIM) (Figure 3-5) contains 21 jumper lead locations and a light-emitting diode (LED) indicator. The jumpers are used to select transmission methods for compatibility between the CPU and the console terminal, the CPU and the TU58 tape unit, and the CPU and the remote diagnostic unit. The jumper leads as shown in Figure 3-5 select RS-232-C transmission mode for SLU1 (console terminal) and SLU2 (TU58 tape unit).

3.3.1.1 Console Terminal Configurations – The console terminal cable attaches to connector J2. The following methods of data transmission are selectable.

1. 20 mA current loop: active or passive mode
2. Electronic Industries Association (EIA) Standard: RS-232C, RS-423 and RS-422

Table 3-10 lists the jumper lead configuration for the 20 mA interface and Table 3-11 for the EIA interface.

3.3.1.2 TU58 DECtape II Configuration – The TU58 DECtape II device cable attaches to connector J4. Table 3-12 lists the jumper lead configuration for selecting the EIA transmission mode.

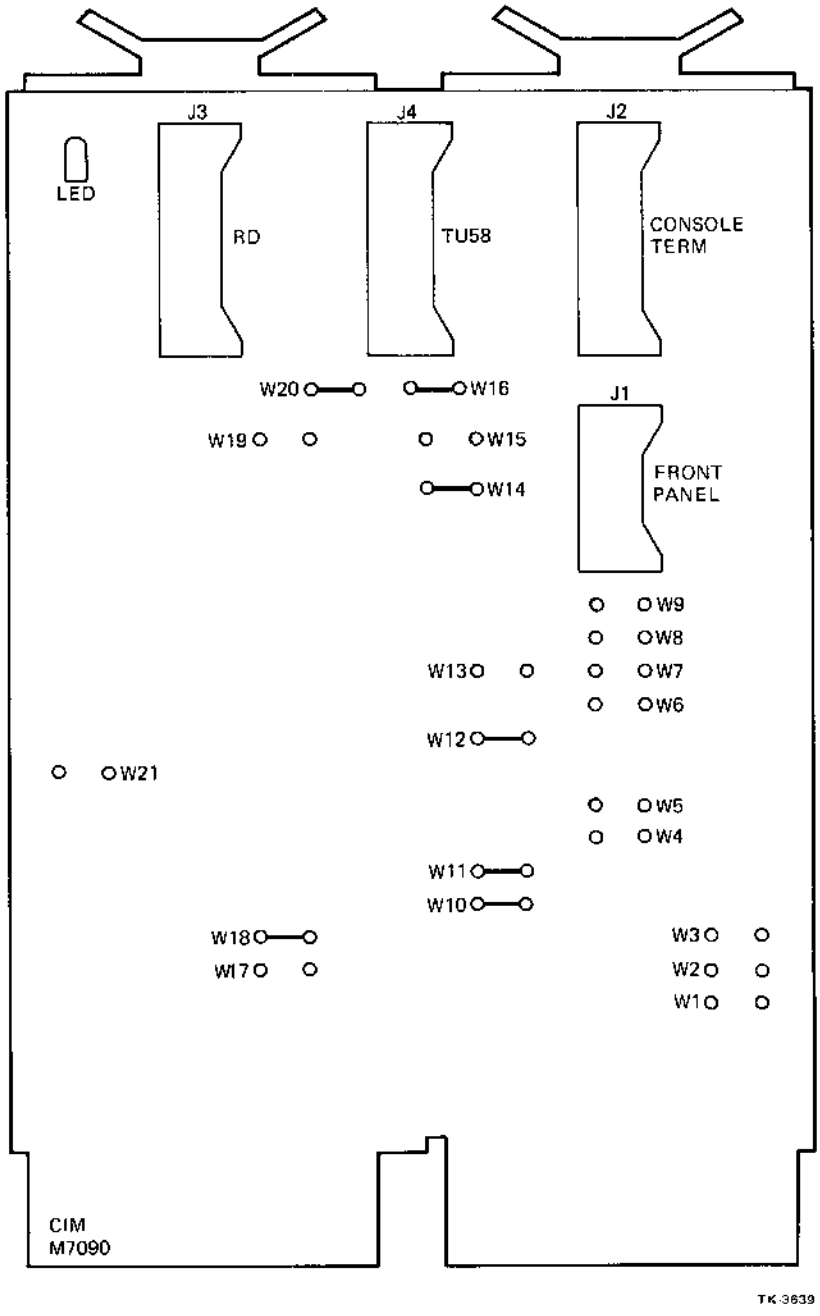


Figure 3-5 CIM Jumper Lead Locations, Connectors and LED Indicator

Table 3-10 Console Terminal Configuration, 20 mA Interface

Mode	Jumper Leads*						
Transmitter	**W4**	**W5**	**W6**	**W7**	**W13**		
Active	Out	In	In	Out	In		
Passive	In	Out	Out	In	Out		
EIA device	Out	Out	Out	Out	Out		
Receiver	**W1**	**W2**	**W3**	**W8**	**W9**	**W17**	**W18**
Active	In	Out	In	Out	In	In	Out
Passive	Out	In	Out	In	Out	In	Out
EIA device	Out	Out	Out	Out	Out	Out	In

*Jumper lead W11 should always be installed except for module testing. When 20 mA operation is selected, jumper leads W12, W15, W16, W19 and W20 may remain installed.

Table 3-11 Console Terminal Configuration, EIA Interface

Mode	Jumper Leads							
	W12	**W15**	**W16**	**W17**	**W18**	**W19**	**W20**	**W1–W9, W13**
RS-232C	In	Out	In	Out	In	Out	In	Out
RS-423	Out	Out	In	Out	In	Out	In	Out
RS-422	Out	In	Out	Out	In	In	Out	Out

Table 3-12 TU58 DECtape II, EIA Configuration

Mode	Jumper Lead W14
RS-232C	In
RS-423	Out

3.3.1.3 Remote Diagnosis Configuration – The remote diagnostic cable attaches to connector J3. When jumper lead W21 is not installed, the remote diagnostic unit has control of the CPU when the front panel switch is set to either the LOCAL or LOC DSBL position. When jumper lead W21 is installed, the remote diagnostic unit cannot take control of the CPU if the front panel switch is in the LOC DSBL position.

3.3.1.4 Voltage Monitoring – The voltage monitoring circuits detect over or under voltage conditions. Jumper lead W10, when IN, enables the 12 V supply voltages to be monitored. When jumper W10 is OUT, the 12 V supply voltages are not monitored.

3.3.1.5 LED Indicator – The LED indicator lights when EIA data transmission to the console terminal has occurred in both directions.

3.3.2 Multifunction Module (M7096)

The multifunction module (Figure 3-6) contains a LED indicator, 14 jumper lead locations and 4 switch packs. The LED on the module is a self-test command indicator which lights at the beginning of a self-test command and is extinguished after the completion of the test.

3.3.2.1 Console Terminal Jumper Leads Selections – Table 3-13 lists the configuration and functions of the console terminal jumper leads on the multifunction module.

Table 3-13 MFM Console Terminal Jumper Lead Configuration

Jumper Lead	Function
W1	When in, address decode for the console terminal is enabled.
W4	When in, the receiver error bits (15:12) of the console terminal receiver buffer register are enabled. When out, the error bits are read as zero.
W5	When in, the break bit (bit 0) of the console terminal transmitter status register (RBUF) is enabled and can be set or cleared. When out, the break bit is disabled and will remain clear.
W6	When in, console terminal receiver parity detection is enabled and parity will be generated. If W4 is in, the parity error bit (bit 12) of the terminal receiver buffer register (XBUF) will be set on a parity error. When W6 is out, parity detection and generation is disabled and the parity error bit will remain cleared.
W7 and W8	These jumpers specify the character length for the console terminal UART, as follows:

Jumper Leads	5 Bits	6 Bits	7 Bits	8 Bits
W7	In	In	Out	Out
W8	In	Out	In	Out

W9	When in, odd parity will be generated and checked, if jumper W6 is also in. When W9 is out, even parity will be generated and checked, if jumper W6 is in.

3.3.2.2 MFM Console Terminal Baud Rate Selection – Table 3-14 lists the positions of switch pack E6 on the MFM to select the baud rate of the console terminal. The location of E6 is shown in Figure 3-6. Switch S1 of E6 selects the stop bit: ON is one stop bit; OFF is two stop bits. The OFF position will also select 1.5 stop bits if a 5-bit character is selected by jumper leads W7 and W8 (Table 3-13).

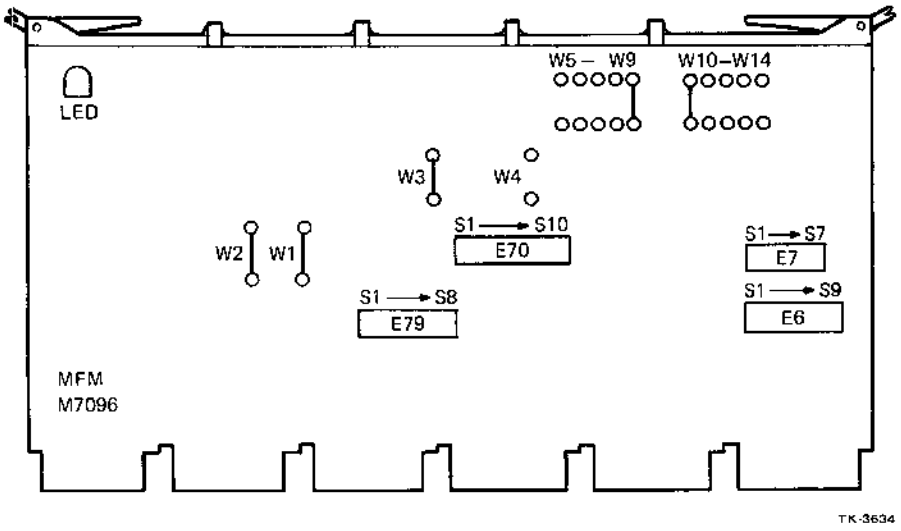


Figure 3-6 MFM Jumper Lead Locations Switches and LED Indicator

Table 3-14 MFM Console Terminal Baud Rate Selection

	Switch Pack E6			
Receiver Switch Locations	**2**	**3**	**4**	**5**
Transmitter Switch Locations	**6**	**7**	**8**	**9**
Baud Rate*				
50	On	On	On	On
75	On	On	On	Off
110	On	On	Off	On
134.5	On	On	Off	Off
150	On	Off	On	On
200	On	Off	On	Off
300	On	Off	Off	On
600	On	Off	Off	Off
1200	Off	On	On	On
1800	Off	On	On	Off
2000	Off	On	Off	On
2400	Off	On	Off	Off
3600	Off	Off	On	On
4800	Off	Off	On	Off
9600	Off	Off	Off	On
19200	Off	Off	Off	Off

*When the processor is placed in the remote mode of operation, the console baud rate defaults to 19200 baud.

3.3.2.3 MFM TU58 DECtape II Jumper Leads – Table 3-15 lists the jumper leads that select the operating parameters of the TU58 tape unit.

3.3.2.4 MFM TU58 Baud Rate Selection – Switches S1 through S6 of switch pack E7 are used to select the baud rates of the TU58 transmitter and receiver. The location of E7 is shown in Figure 3-6. Switch S7 of E7 selects the stop bit: ON is one stop bit; OFF is two stop bits. The OFF position will also select 1.5 stop bits if a 5-bit character is selected by jumper leads W12 and W13 (Table 3-15). Switch position S2 through S6 should only be set to the combinations shown in Table 3-16. The baud rate for the transmitter and receiver can be different.

3.3.2.5 MFM TU58 Device Address Selection – The switch pack at location E70 contains switches S1 through S10 and is used to select the base address of the TU58 tape unit from 17760000 to 17777777. Figure 3-7 shows the address bits affected by the switch settings.

3.3.2.6 TU58 Vector Address Selection – The switch pack at location E79 contains switches S1 through S8. Switch S1, when ON, enables the TU58 address to be decoded. Switch S2 is related to console terminal operation. Switches S3 through S8 are used to set the TU58 vector address from 0 to 770 (octal). The recommended vector address for use with DIGITAL software is 300. The transmitter vector equals the receiver vector plus 4. Figure 3-8 shows the correspondence between the switch positions and the TU58 vector address.

Table 3-15 MFM TU58 Jumper Lead Configurations

Jumper Lead	Function
W3	When in, the receiver error bits (15:12) of the TU58 receiver buffer register are enabled. When out, the error bits are read as zero.
W10	When in, the break bit (bit 0) of the TU58 transmitter status register is enabled and can be set or cleared. When out, the break bit is disabled and will remain clear.
W11	When in, TU58 receiver parity detection is enabled and parity will be generated. If W3 is in, the parity error bit (bit 12) of the TU58 receiver buffer register will be set on a parity error. When W11 is out, parity detection and generation is disabled and the parity error bit will remain cleared.
W12 and W13	These jumpers specify the character length for the TU58 UART, as follows:

Jumper Leads	5 Bits	6 Bits	7 Bits	8 Bits
W12	In	In	Out	Out
W13	In	Out	In	Out

W14	When in, odd parity will be generated and checked, if jumper W11 is also in. When W14 is out, even parity will be generated and checked, if jumper W11 is in.

An example of the switch positions required to select a vector address of 300 is as follows:

S8 to S6 = OFF
S5, S4 = ON
S3 = OFF

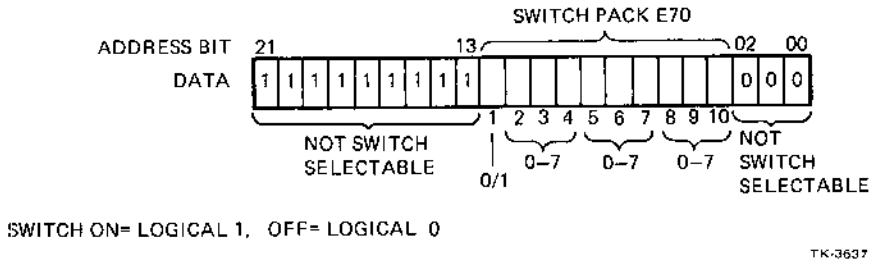


Figure 3-7 TU58 Device Address Selection

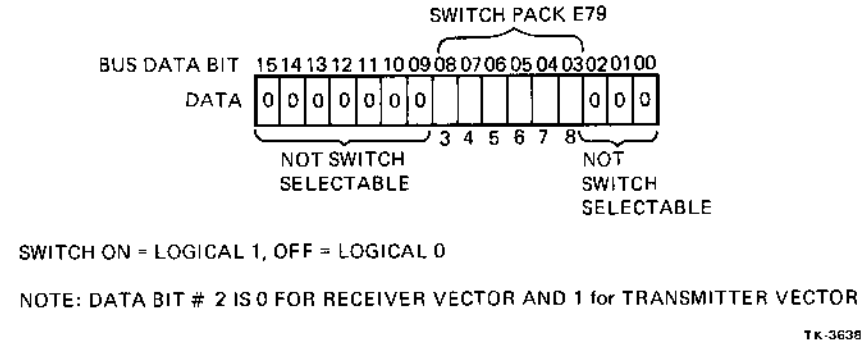


Figure 3-8 TU58 Vector Address Selection

Table 3-16 TU58 Baud Rate Selection (Switch Pack E7 *)

Receiver Switch **Transmitter Switch**	**1** **4**	**2** **5**	**3** **6**
Baud Rate 38,400	ON	OFF	OFF
9600	OFF	ON	OFF
Same baud rate as selected for the console terminal	OFF	OFF	ON

*Switch S7 is not used

3.3.2.7 Line Time Clock Enable/Disable – Jumper lead location W2 on the MFM module controls the operation of the line time clock as listed in Table 3-17.

3.3.3 UNIBUS Interface Module (M7098)

The UNIBUS interface (UBI) module shown in Figure 3-9 contains 14 jumper lead locations and one switch pack at location E28.

3.3.3.1 UBI Jumper Leads and Memory Page Selection – Table 3-18 lists the function of the jumper leads on the UBI module.

Jumper leads W12–W8 and W7–W3 specify the lower and upper limit, respectively, of a set of UNIBUS addresses not mapped to main memory (asserted on the UNIBUS only). Except for the I/O page, every UNIBUS address not in this set is mapped to main memory (asserted on the memory bus) by the UNIBUS map. Devices on the UNIBUS should be addressed only in unmapped or I/O page address space.

When the upper and lower limits are set to the same octal bank (page) number, every non-I/O page address is mapped to main memory.

Table 3-19 lists the jumper lead selections for the lower limit of the set of unmapped addresses. UNIBUS addresses from zero to just below this limit are mapped to main memory. The octal bank number in this table is the first bank of the unmapped set, except when the lower and upper limits are set to the same bank number, in which case only the I/O page is unmapped.

Table 3-17 Line Time Clock Operation

W2	Line Time Clock Address
In	Enable decode
Out	Disable decode

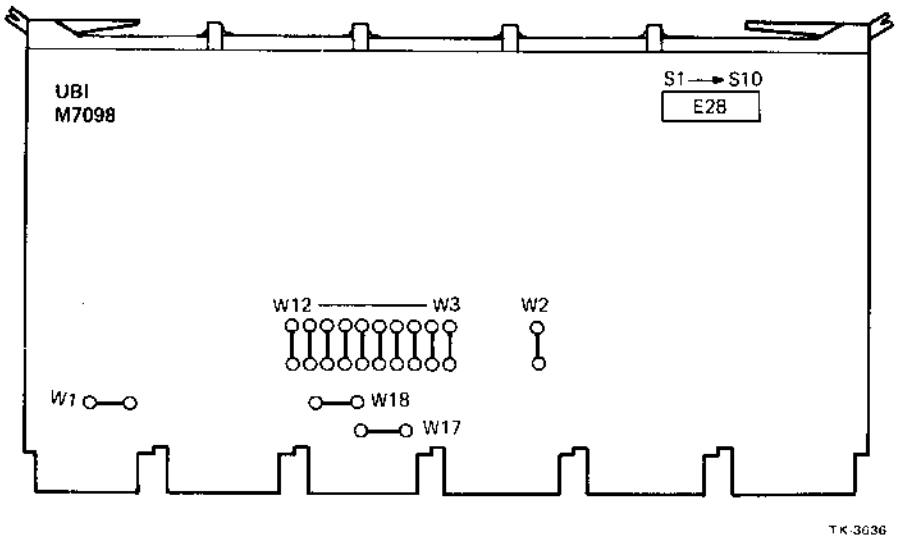


Figure 3-9 UBI Module, Switch and Jumper Lead Locations

Table 3-18 UBI Module Jumper Lead Functions

Jumper Lead	Function
W1	When in, enables parity error abort
W2	When in, enables diagnostic ROM
W3–W7	UNIBUS map page number, upper limit
W8–W12	UNIBUS map page number, lower limit
W17, W18	Always in

Table 3-19 UNIBUS Map Jumper Leads, Lower Limit

Lowest Address In Unmapped Set	Decimal K Words	Octal Bank	Jumper Leads* W12	W11	W10	W9	W8
None	124	37	O	O	O	O	O
740 000	120	36	I	O	O	O	O
720 000	116	35	O	I	O	O	O
700 000	112	34	I	I	O	O	O
660 000	108	33	O	O	I	O	O
640 000	104	32	I	O	I	O	O
620 000	100	31	O	I	I	O	O
600 000	96	30	I	I	I	O	O
560 000	92	27	O	O	O	I	O
540 000	88	26	I	O	O	I	O
520 000	84	25	O	I	O	I	O
500 000	80	24	I	I	O	I	O
460 000	76	23	O	O	I	I	O
440 000	72	22	I	O	I	I	O
420 000	68	21	O	I	I	I	O
400 000	64	20	I	I	I	I	O
360 000	60	17	O	O	O	O	I
340 000	56	16	I	O	O	O	I
320 000	52	15	O	I	O	O	I
300 000	48	14	I	I	O	O	I
260 000	44	13	O	O	I	O	I
240 000	40	12	I	O	I	O	I
220 000	36	11	O	I	I	O	I
200 000	32	10	I	I	I	O	I
160 000	28	7	O	O	O	I	I
140 000	24	6	I	O	O	I	I
120 000	20	5	O	I	O	I	I
100 000	16	4	I	I	O	I	I
60 000	12	3	O	O	I	I	I
40 000	8	2	I	O	I	I	I
20 000	4	1	O	I	I	I	I
0	0	0	I	I	I	I	I

*1 = IN
O = OUT

Table 3-20 lists the jumper selections for the upper limit of the set of unmapped addresses. UNIBUS addresses above this limit and below 760 000 are mapped to main memory. The octal bank number in this table is the first mapped bank after the unmapped set, except when it is bank 37, the I/O page (always unmapped).

Table 3-20 UNIBUS Map Jumper Lead, Upper Limit

Highest Address In Unmapped Set	Decimal K Words	Octal Bank	Jumper Leads* W7	W6	W5	W4	W3
757 777	124	37	O	O	O	O	O
737 777	120	36	I	O	O	O	O
717 777	116	35	O	I	O	O	O
677 777	112	34	I	I	O	O	O
657 777	108	33	O	O	I	O	O
637 777	104	32	I	O	I	O	O
617 777	100	31	O	I	I	O	O
577 777	96	30	I	I	I	O	O
557 777	92	27	O	O	O	I	O
537 777	88	26	I	O	O	I	O
517 777	84	25	O	I	O	I	O
477 777	80	24	I	I	O	I	O
457 777	76	23	O	O	I	I	O
437 777	72	23	O	O	I	I	O
417 777	68	21	O	I	I	I	O
377 777	64	20	I	I	I	I	O
357 777	60	17	O	O	O	O	I
337 777	56	16	I	O	O	O	I
317 777	52	15	O	I	O	O	I
277 777	48	14	I	I	O	O	I
257 777	44	13	O	O	I	O	I
237 777	40	12	I	O	I	O	I
217 777	36	11	O	I	I	O	I
177 777	32	10	I	I	I	O	I
157 777	28	7	O	O	O	I	I
137 777	24	6	I	O	O	I	I
117 777	20	5	O	I	O	I	I
77 777	16	4	I	I	O	I	I
57 777	12	3	O	O	I	I	I
37 777	8	2	I	O	I	I	I
17 777	4	1	O	I	I	I	I
None	0	0	I	I	I	I	I

*I = IN
O = OUT

The following example describes the jumper selections for 3 pages (12 decimal K words) of UNIBUS device addresses immediately following the I/O page.

1. Page (bank) 37 is the I/O page; therefore, the three pages to be unmapped are 34, 35, and 36.

2. Read jumper settings for W12 through W8 from the lower limit (Table 3-19) at bank 34, the first unmapped bank: W12 = in, W11 = in, W10 = out, W9 = out, and W8 = out.

3. Read jumper settings for W7 through W3 from the upper limit (Table 3-20) at bank 37, the next bank after the unmapped set desired (34, 35, and 36): W7 = out, W6 = out, W5 = out, W4 = out, and W3 = out.

Notice that the upper limit "Decimal K Words" amount minus the lower limit "Decimal K Words" amount is equal to 12K words. This is the size of the area desired.

3.3.3.2 Diagnostic and Bootstrap Loader ROMs – The UBI module provides five 16-pin, dual in-line package (DIP) sockets for the installation of a CPU diagnostic ROM and four device bootstrap loader ROMs. If selected, the CPU diagnostic ROM checks the CPU, main memory, and cache when power is initially applied to the system or when a device bootstrap is initiated.

The device bootstrap loader ROMs contain device-independent bootstrap programs that enable the loading of information from a selected peripheral device into main memory. One or two bootstrap programs may be contained in a particular ROM; however, some devices may require two or more ROMs to contain their particular bootstrap programs. Table 3-23 lists the part numbers for the available device bootstrap ROMs.

A bootstrap operation using the UBI module boot logic can be initiated by any one of the following actions.

1. Pressing the front panel toggle switch to the boot position.

2. Typing the bootstrap command at the console terminal when in console mode.

3. Powering up the system.

The actual bootstrap operation performed can be a boot to the console mode (with or without diagnostics) or a boot to a selected device bootstrap ROM (with or without diagnostics). Switches S1 through S10 at location E28 of the UBI module control the boot operation as follows.

Switch S1 determines the upper three digits of the bootstrap starting address.

S1 = On (Boot to the console mode)

S1 = Off (Boot selected device ROM)

Switch S2 controls the operation of the internal bootstrap logic.

S2 = On (Internal UBI boot logic is enabled.)

S2 = Off (Internal UBI boot logic is disabled.
This allows an external auxillary boot device to be used.)

Switches S3 through S10 are bits (08:01) of the bootstrap starting address. Table 3-21 lists the location of the CPU diagnostic ROM and bootstrap loader ROMs and the starting address associated with each one. The selection of the first device starting address determines whether the CPU diagnostic will be performed before the bootstrap program is performed. The second devices listed in the table are for selecting a second device bootstrap program contained in the same ROM as the first device bootstrap program.

Table 3-21 CPU Diagnostic and Bootstrap Loader, ROM Addresses

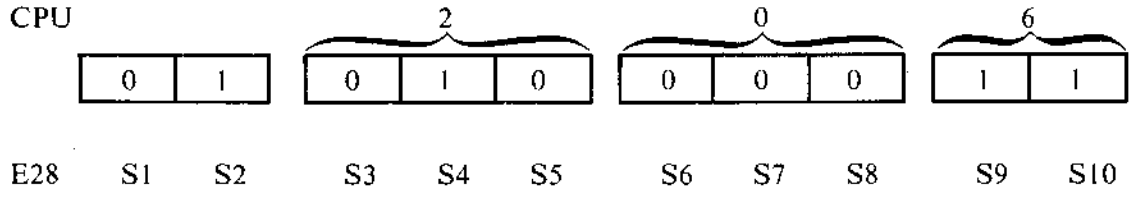
ROM Location	CPU Diagnostic	First Device Address	S3-10 Second Device Address 23-755A9	Second Device 23-756A9 23-760A9	Multiple ROM Device* Unit0	Unit1
CPU Diagnostic (E58)	No	0144				
	Yes	0020				
Device 1 (E48)	No	0004	0050	0034	004	030
	Yes	0006	0052	0036	006	032
Device 2 (E49)	No	0204	0250	0234	204	230
	Yes	0206	0252	0236	206	232
Device 3 (E50)	No	0404	0450	0434		
	Yes	0406	0452	0436		
Device 4 (E59)	No	0604	0650	0634		
	Yes	0606	0652	0636		

*The DMC-11, DU-11, and DUP-11 use multiple ROMs. Table 3-23 lists the ROM part numbers.

The position of the bootstrap ROMs on the module must be sequential, starting with BT1 and progressing to BT4 as listed in Table 3-22. The IC location is indicated on the module etch.

To select an RL01 installed in the second ROM location (E49) and run the CPU diagnostic program, set the switches as described in the following example.

RL01 ROM in location E49
Run diagnostics and then boot RL01



0 = OFF
1 = ON

Table 3-23 lists the part numbers for the available bootstrap ROMs. Some of the ROMs contain more than one device program. The bootstrap loaders for the communication devices DL11, DMC-11, DU11 and DUP-11 are supplied in three ROMs for each device.

Table 3-22 Bootstrap ROM Locations

IC Location	Bootstrap ROM
E48	Device 1
E49	Device 2
E50	Device 3
E59	Device 4

Table 3-23 Device ROM Part Numbers

Device	ROM Part Number	Device	ROM Part Number
ASR33	23-760A9	RL01	23-751A9
DL11	23-926A9	RP02/03	23-755A9
	23-927A9		
	23-928A9	RP04/05/06	23-755A9
DMC-11	23-862A9	RS03/04	23-759A9
	23-863A9		
	23-864A9	RX01	23-753A9
DU-11	23-868A9	RX02	23-811A9
	23-869A9		
	23-870A9	TS04	23-764A9
		TU10, TE10, TS03	23-758A9
DUP-11	23-865A9	TU16, 45, 77, TE16	23-757A9
	23-866A9		
	23-867A9	TU55/56	23-756A9
PC05	23-760A9	TU58	23-765A9
RK03/05	23-756A9	TU60	23-761A9
RK06/07	23-752A9		

3.3.4 Cache Memory Module (M7097)

The cache memory module, shown in Figure 3-10, contains three LED indicators, two toggle switches and two jumper lead locations.

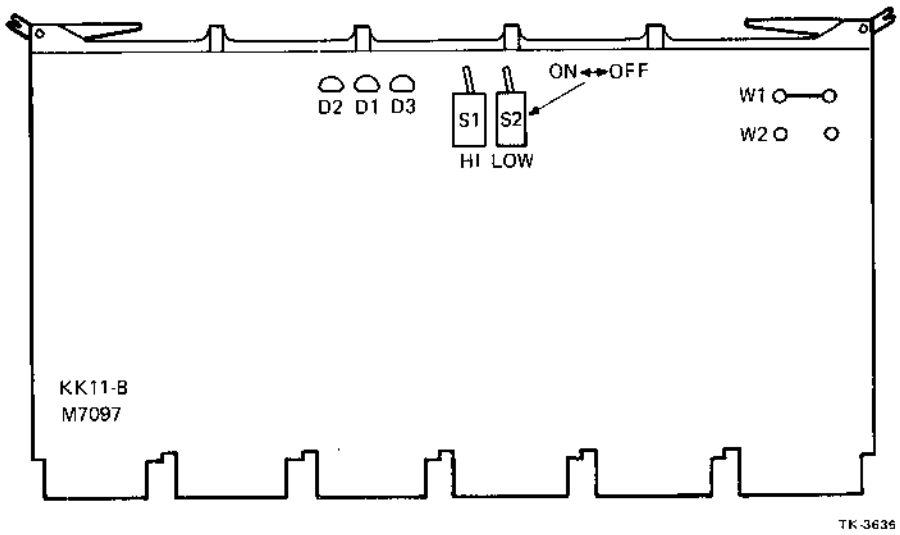


Figure 3-10 Cache Memory Module, Switches, LED Indicators and Jumper Lead Locations

3.3.4.1 LED Indicator Functions – Table 3-24 lists the functions of the LED indicators.

3.3.4.2 Multiport Memory Selection – Jumpers W1 and W2 are provided to accommodate multiported memory. In the PDP-11/44 (without multiported memory), jumper W1 should be in and jumper W2 should be out. In systems using multiport memory, jumper W1 is out and jumper W2 is in.

When on, switches S1 and S2 will force misses to the high and low cache address space, respectively. The switch is on when the lever is positioned to the left, toward the LED indicators.

3.3.5 Control Module (M7095)
The control module contains a toggle switch, S1, (Figure 3-11) that is used to enable or disable the bootstrap operation on power-up.

Table 3-24 Cache Module, LED Indicator Functions

LED	Function
D3	Parity error
D1	Hit
D2	Address MATCHED

– MEM 31/5/85

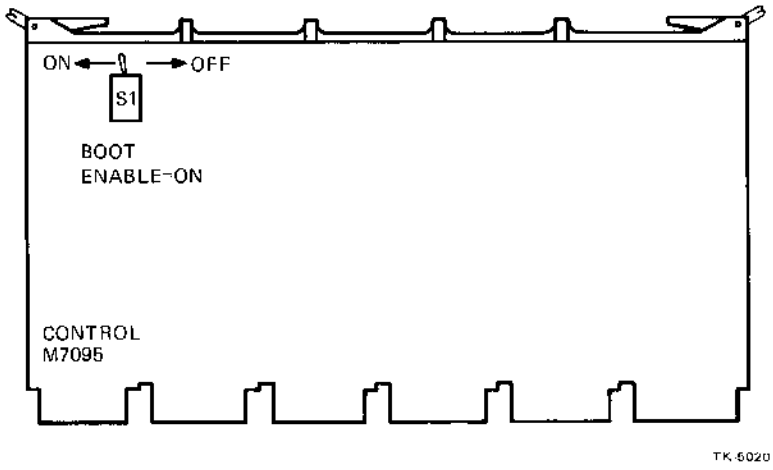


Figure 3-11 Control Module, Bootstrap Control Switch

CHAPTER 4
INSTALLATION

The PDP-11/44 and PDP-11X44 systems and peripheral devices can be operated in most contaminant-free environments such as offices, laboratories or light manufacturing areas. However, to ensure reliable operation, certain environmental conditions are recommended.

4.1 SITE CONSIDERATIONS

The computer equipment should be operated in an environment that is controlled by an air-conditioning system which provides temperature controlled, filtered air at the specified levels of humidity. The air-conditioning system should also increase the air pressure in the computer area to prevent the infiltration of dust and other contaminants from adjacent areas.

The air-conditioning equipment should conform to the requirements of the Standard for the Installation of Air-Conditioning and Ventilating Systems (Non-Residential), N.F.P.A. No. 90A, as well as the requirements of the Standard for Electronic Computer Systems, N.F.P.A. No. 75.

4.1.1 Temperature and Humidity

Temperature cycling and thermal gradients can induce changes in materials which will affect the performance of the system. High temperatures also increase the rate of deterioration of materials. An environment of high absolute humidity can cause dimensional changes in paper tapes, lineprinter papers and cards. Low humidity can produce static electricity, resulting in dust accumulation on magnetic tape and disk devices, which will adversely affect the system operation.

The PDP-11/44 systems are designed to operate in a temperature range of 5° to 50° C (41° to 122° F) at a relative humidity of 10 to 95 percent without condensation. System configurations that use I/O devices, such as magnetic tape units, card readers, disks, etc., require an operating temperature range from 10° to 40° C (50° to 104° F) at a relative humidity of 40 to 66 percent without condensation. The nominal operating conditions for a system configuration are a temperature of 20° C (70° F) and a relative humidity of 45 percent.

4.1.2 Acoustical Dampening

Some peripheral devices such as character printers, lineprinters and magnetic tape transports generate noise when operating. When many of these units are located in an area, sound absorbent materials may be used to reduce the noise level. Sound absorbent ceiling materials are available and antistatic carpets may be installed. In addition, the wall areas may be covered with drapes or other suitable material which will reduce the reflected noise.

4.1.3 Lighting

When video displays (CRTs) are used with the system, a reduced lighting level at the site will prevent excessive reflection from the face of the CRT and enable the display to be viewed more easily by the operator. The light levels may be controlled by dimmers or by the installation of translucent materials between the light source and the surrounding areas.

4.1.4 Static Electricity

The PDP-11/44 and related cabinets should be adequately grounded to prevent the effects of static electricity from interfering with the equipment operation. Static charges can be reduced by maintaining the relative humidity of the room at the specified 45 percent nominal value. Antistatic carpeting is also available to minimize the static charges generated. When raised floors are used at the computer installation, the framing of the floor panels should be adequately grounded.

4.1.5 Shock and Vibration

When the PDP-11/44 units are to be installed at locations subjected to excessive shock and vibration, special cabinet mounting hardware may be required. Contact your local DIGITAL sales representative for information related to special environmental conditions.

4.1.6 Electrical Interference

Several types of electrical interference may be indigenous to the site location and may require special filtering to prevent equipment malfunctions.

The interference transmitted through the air is electromagnetic interference (EMI) and may be caused by TV and radio waves, radar transmissions, lightning discharges, ignition systems and power line transmissions. Interference may also be transmitted through the ac power lines. If the interference is suspected to be causing problems with the operation of the equipment, shielding may be required, or filtering of the ac power to the site. Contact your local DIGITAL sales office or field service representative for information related to interference problems.

4.2 UNPACKING

The system equipment, associated devices, and cabinets are packed and shipped in reinforced cartons and are protected internally by foam inserts and polyethylene bags. Accessories and supplies such as documentation, magnetic tape or disks, and connecting cables and hardware are packed in separate containers. Before unpacking any carton, remove the packing list from the container and check that the items ordered are listed. When the items are unpacked, use the list to check that all the items are in the package. The unpacking information for consoles, printers, disk drives and magnetic tape is contained in the user's guide supplied with each device.

NOTE

Retain the packing materials and shipping containers in the event reshipping is required.

4.2.1 PDP-11/44-CA, -CB Unit Removal

The PDP-11/44-CA and CB units are packed in reinforced cartons and protected by foam inserts and a polyethylene bag as shown in Figure 4-1. To remove the unit from the container, perform the following procedure.

CAUTION

The PDP-11/44-CA, -CB units weigh approximately 34 kg (75 lbs). Use care when lifting the unit from the carton.

1. Open the leaves of the outer carton by cutting the tape at the seams.
2. Remove the inner carton from the foam protector.
3. Open the leaves of the inner carton by cutting the tape at the seams.
4. Remove the side and rear protectors.
5. Remove the unit from the polyethylene bag.
6. Remove the bezel protector.
7. Inspect the unit for visible damage and ensure that the contents are complete.

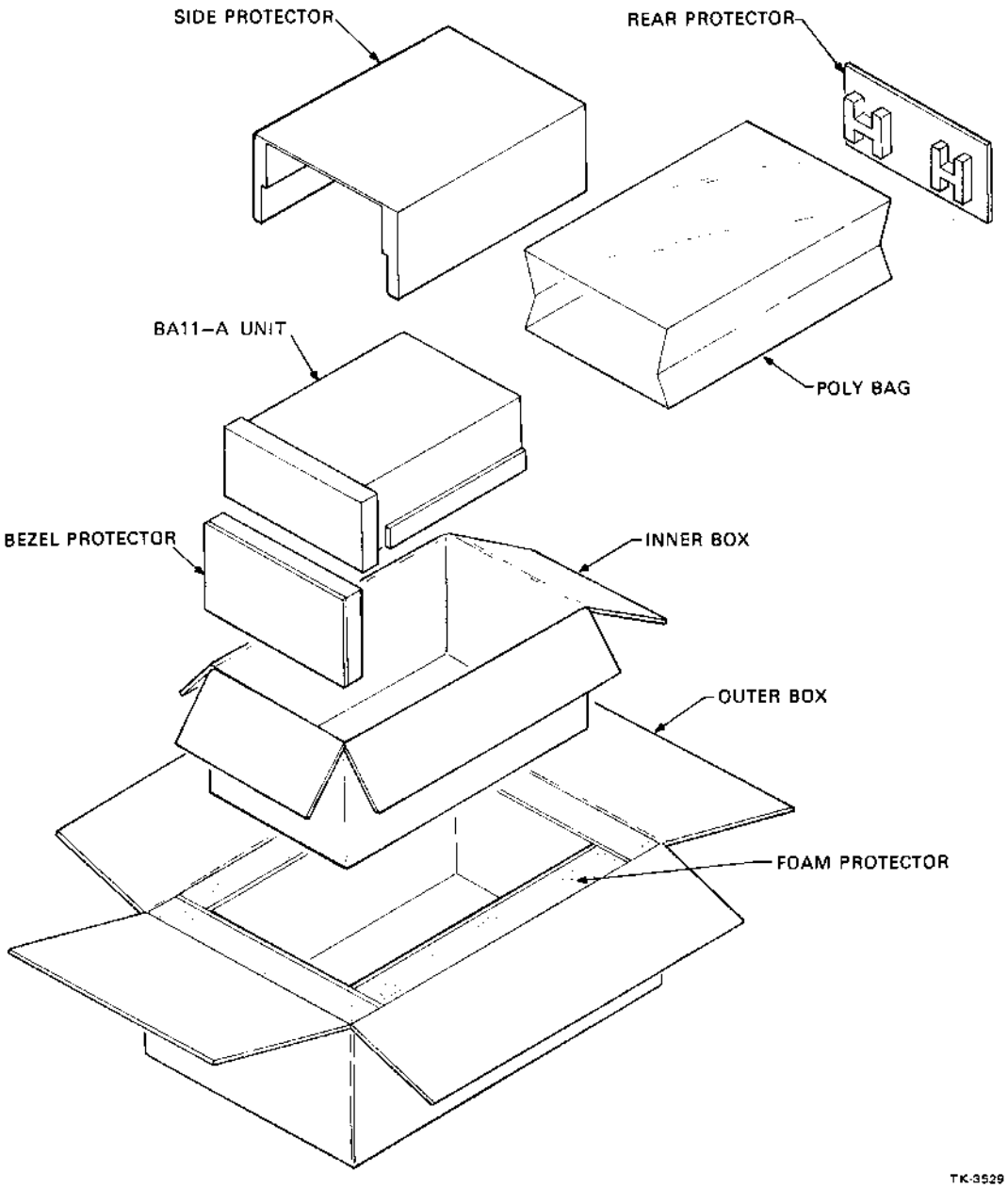


Figure 4-1 PDP-11/44 Unit Unpacking

4.2.2 PDP-11X44-CA, -CB Cabinet Removal

The PDP-11X44-CA, -CB units are attached to a wooden base, covered with a polyethylene bag and enclosed by a carton as shown in Figure 4-2. To remove the unit, perform the following procedure.

1. Cut the polyester straps that secure the carton and unit to the base.
2. Slide the carton up and away from the unit.
3. Remove the polyethylene bag from the unit.
4. Remove the bolts that hold the bottom of the unit to the wooden base.
5. Remove the unit from the wooden base and set the unit in its operating location.
6. Attach the stabilizer feet to the bottom of the unit.

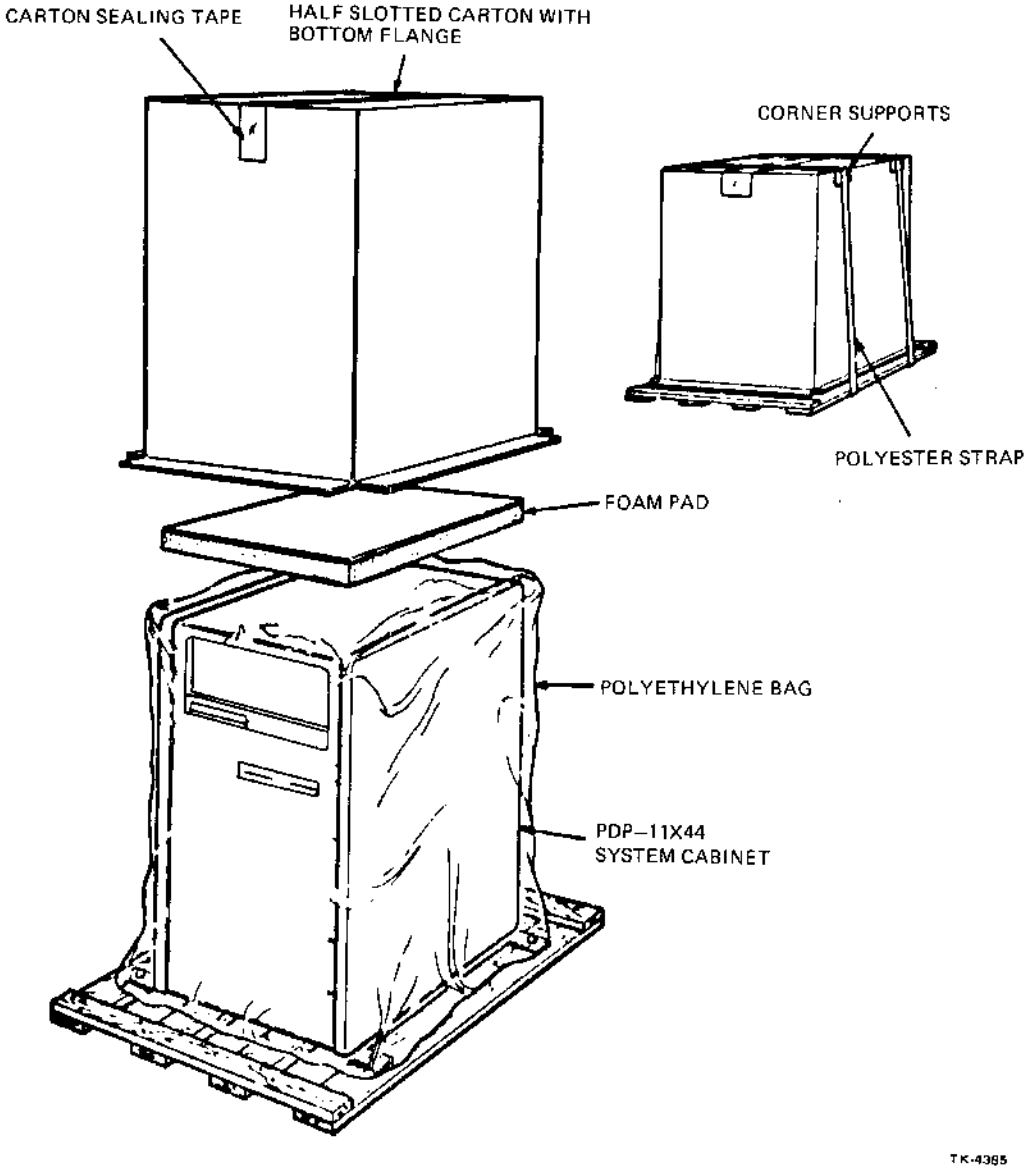


Figure 4-2 PDP-11X44 Cabinet Unpacking

4.2.2.1 Shipping Restraint Removal – Two types of shipping restraint are used in the PDP-11X44 cabinet. The type of restraint used can be determined by the configuration of the top cover as shown in Figure 4-3. In the type A configuration, the box is secured in the cabinet by two shipping brackets and screws. In the type B configuration, the shipping restraint and release mechanism are one unit which does not have to be removed. To disengage the type B release mechanism, refer to Paragraph 5.1.1, steps 6 and 11.

To remove the shipping restraint in the type A configuration, perform the following procedure.

1. Open the front and rear doors of the cabinet. Use a 4mm (5/32 in) hex wrench to release the door fasteners (Figure 4-4).

2. Slide the retractable hinge pin down until the top of the rear door is released.

3. Tilt the top of the door away from the cabinet and lift the door until the lower hinge pin is removed from the hole in the lower right bracket.

4. Remove the rear door.

5. Remove and retain the two 1/4-20 screws and washers that attach the right bracket to the cabinet frame.

6. Retain the right bracket.

7. Remove and retain the two 1/4-20 screws and washers that attach the left bracket to the cabinet frame.

8. Retain the bracket.

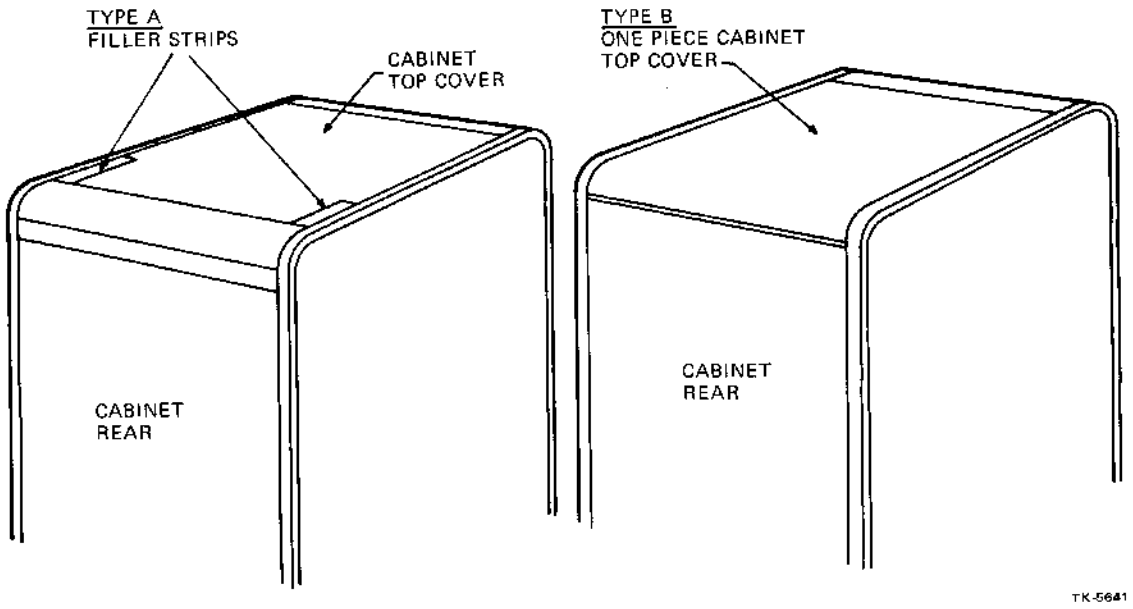


Figure 4-3 PDP-11X44 Cabinet Type Identification

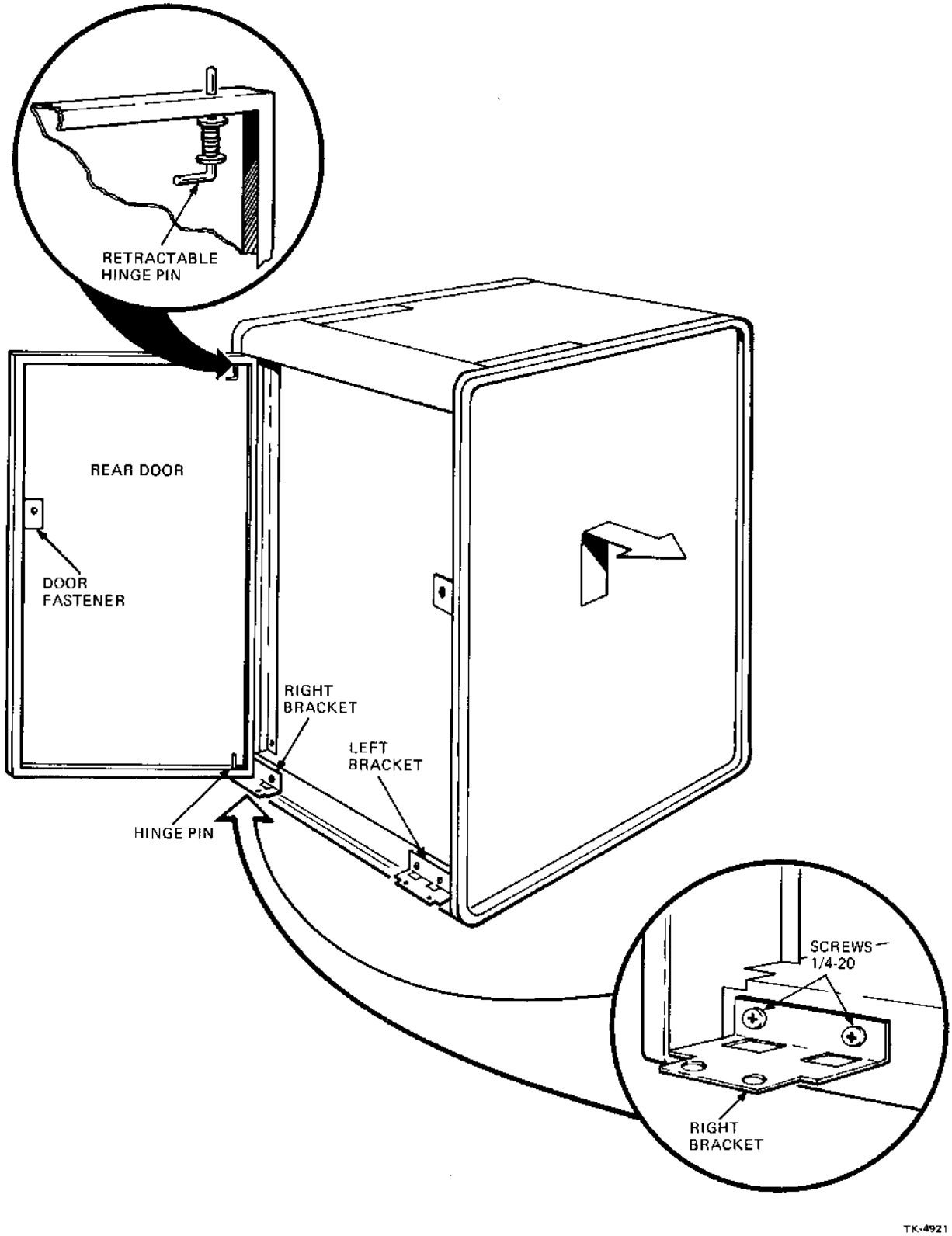


Figure 4-4 Left and Right Side Panel Removal

9. Grasp the left side panel by the ends at the front and rear of the cabinet and lift up approximately 2.5 cm (1 in) to disengage the panel and pull the panel away from the cabinet to remove it.

NOTE

A ground lead is attached to the panel and will restrict the movement of the panel away from the cabinet. Do not remove the lead.

10. Perform step 9 to remove the right side panel from the cabinet.

11. Remove the 10-32 screw and washer that is inserted through the shipping bracket and into the mounting box at the left and right side of the cabinet (Figure 4-5).

12. Replace the left and right side panels that were removed in steps 9 and 10.

13. Replace the brackets that were removed in steps 5 and 7.

14. Tilt the rear door and insert the lower hinge pin into the hole of the bracket closest to the right side panel.

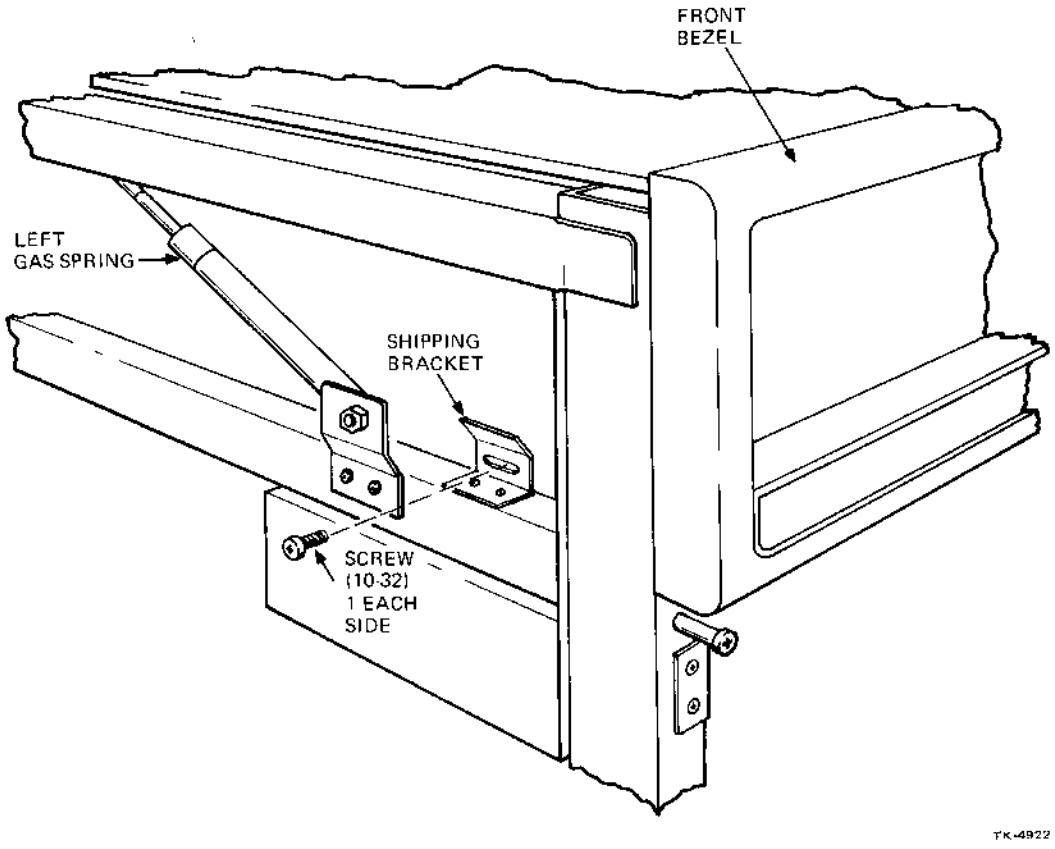


Figure 4-5 Shipping Bracket Location

15. Move the top of the rear door toward its mounting position while holding the retractable hinge pin downward.

16. Release the retractable hinge pin when the pin is aligned with the hole in the top of the cabinet frame.

17. Close the front and rear doors of the cabinet.

4.3 EQUIPMENT DIMENSIONS

Figure 4-6 shows the overall dimensions of the PDP-11/44 unit. The unit will occupy a 26.7 cm (10-1/2 inch) vertical space within a rack or cabinet.

Figure 4-7 shows the overall dimensions of the PDP-11X44 unit. This system is enclosed within a standard system cabinet. When additional units are included in the system configuration, refer to the respective user's guide for the space requirements of each cabinet.

4.4 AC INPUT POWER REQUIREMENTS

The ac input power to the PDP-11/44 system equipment should be supplied by a separate power circuit which is dedicated only to the system.

Table 4-1 lists the power requirements for the four basic system configurations. Any additional equipment installed into the cabinet of the PDP-11X44-CA, -CB system or modules installed into the mounting box may increase the power consumption. Refer to the respective user's guide for the power requirements of the peripheral devices that are supplied with the system.

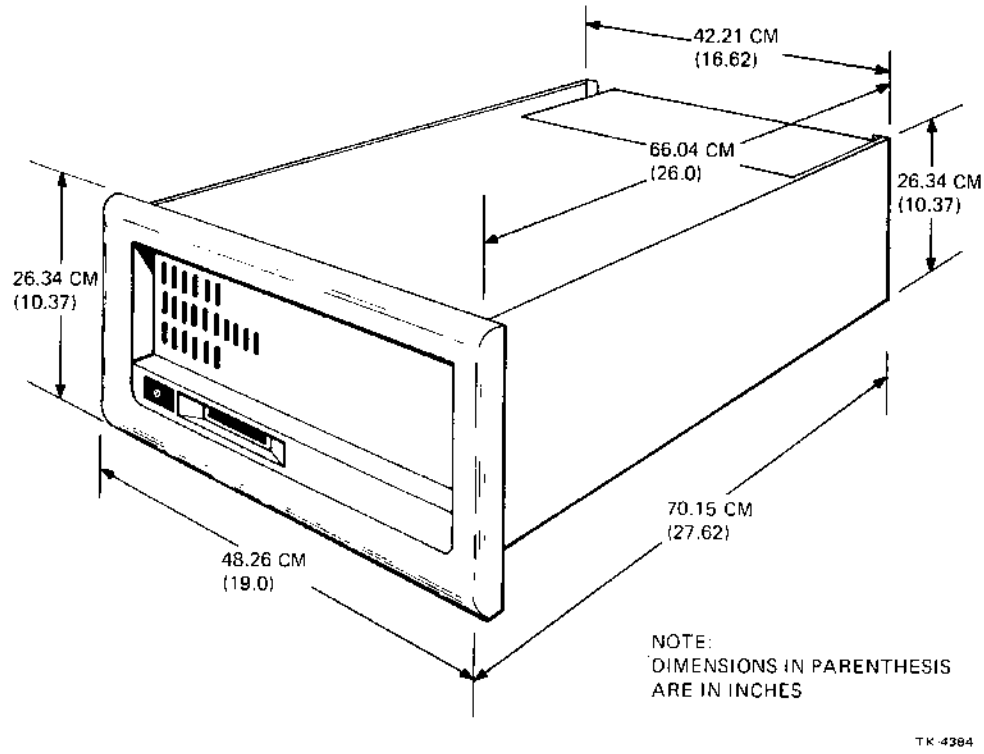


Figure 4-6 PDP-11/44 Unit Dimensions

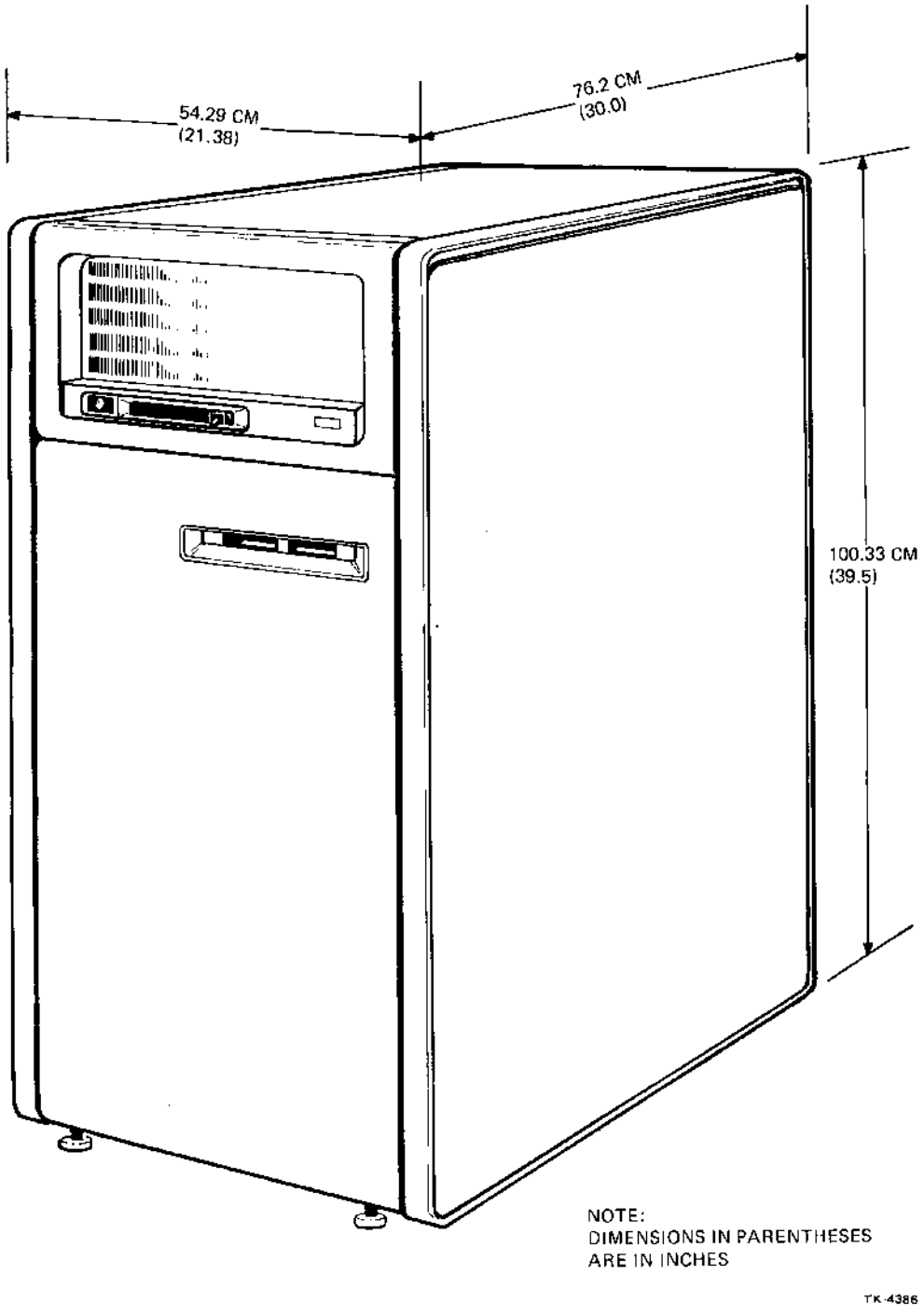


Figure 4-7 PDP-11X44 System Cabinet Dimensions

Table 4-1 System AC Input Power Requirements
System Designation

	PDP-11/44-CA PDP-11X44-CA	PDP-11/44-CB PDP-11X44-CB
AC Voltage Tolerance	90–128 V	180–256 V
Frequency Tolerance	47–63 Hz	47–63 Hz
Phase(s)	1	1
Steady State Current (RMS)	16 A rms max load	9.5 A rms max load
Surge Current	65 A peak	130 A peak
Surge Duration	1/2 cycle	1/2 cycle

4.4.1 Power Connections (AC)

The PDP-11/44-CA, -CB units are supplied with a 2.74 m (9 ft) line cord attached to the rear of the unit. Figure 4-8 shows the ac line cord circuit breaker and connectors. The line cord plug may be connected to an 872-D, -E power controller unit (or equivalent) or directly to the ac power receptacle at the site location. Figure 4-9 shows the type of connector plugs and receptacles used and the DIGITAL part numbers for the connectors. The color of the cable wires connected to the plug is also indicated. The NEMA 5-20 P plug is attached to the PDP-11/44-CA (120 Vac) cable and the NEMA 6-15 P is attached to the PDP-11/44-CB cable. The NEMA 5-20 R and 6-15 R are dual receptacle outlets which can be installed within a wall outlet box or a power distribution unit.

Mounted at the lower rear of the PDP-11X44-CA, -CB cabinet is a power controller unit which controls and distributes the ac power to the units within the cabinet. The PDP-11X44-CA contains an 872-D (120 Vac) power controller, and the PDP-11X44-CB contains an 872-E (240 Vac) power controller. Each controller is supplied with a 4.57 m (15 ft) cord and plug which connects to a receptacle at the site location. Figure 4-10 shows the connector configurations and DIGITAL part numbers for the plugs and receptacles.

4.4.2 System Grounding

The PDP-11/44 and PDP-11X44 systems are commonly grounded to the main power lines through the ac power cord. All units which are part of the system should be connected to a separate and common ac power distribution source to ensure the integrity of the grounding network. If a grounding problem is evident, the potential of the cabinet or mounting box grounds may be checked by connecting a voltmeter between two cabinet frames or between the cabinet frames and the BA11-A mounting box. To ensure positive grounding between the cabinets of the system, it is recommended that a grounding strap or cable be attached in common to each of the cabinet frames. Contact your local DIGITAL field service office for information related to grounding problems.

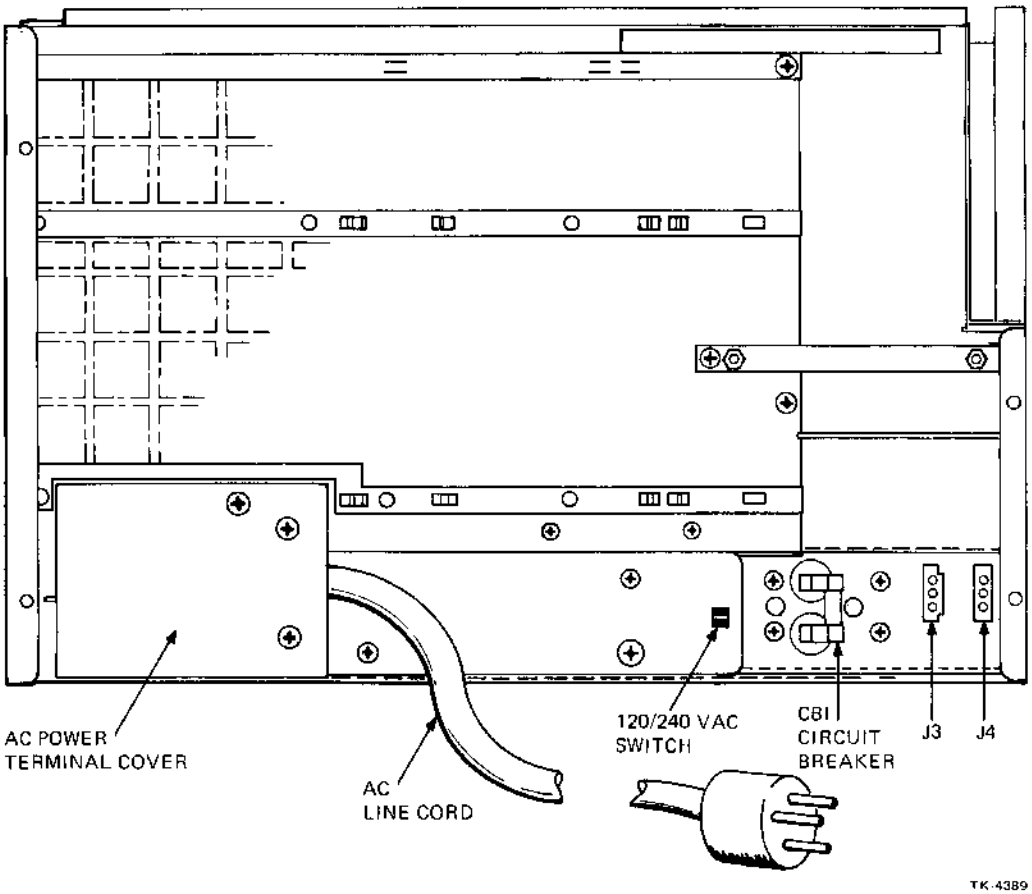
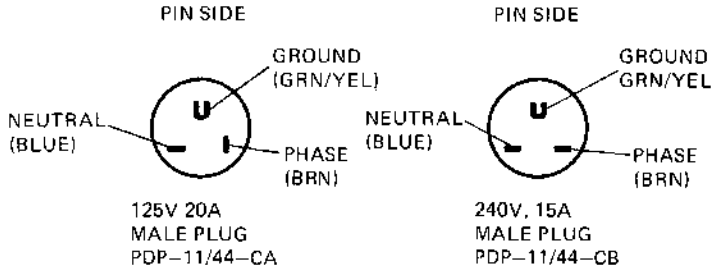


Figure 4-8 Mounting Box Rear Panel Components

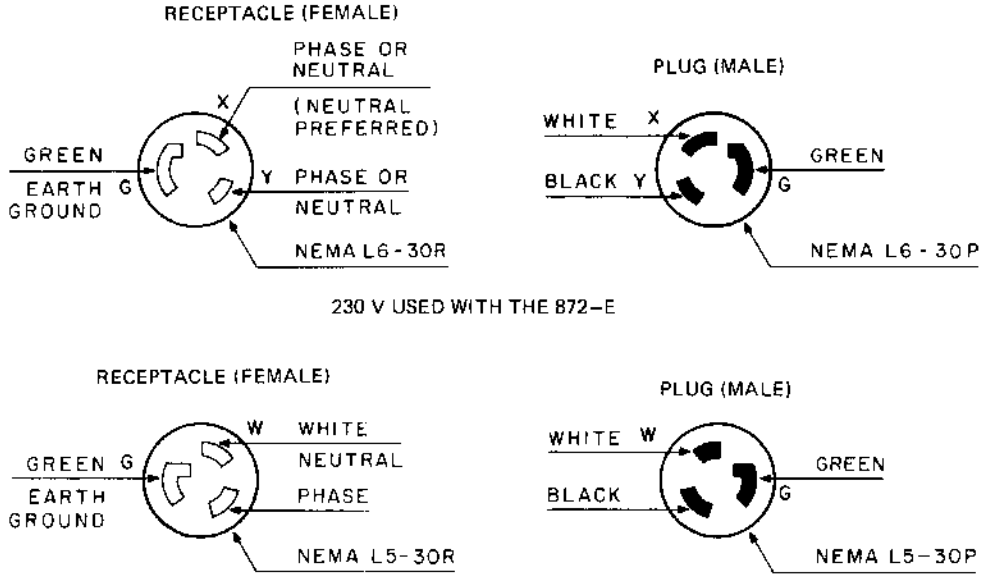


NEMA * DESIGNATION	POWER RATING	DIGITAL PART NO.
5–20 P	125V, 20A	12–15183–00
5–20 R		12–12265–00 * *
6–15 P	240V, 15A	90–08853–00
6–15 R		12–11204–01 * *

* P = PLUG
R = RECEPTACLE
* * DUAL RECEPTACLE OUTLET

TK-4390

Figure 4-9 PDP-11/44-CA, -CB AC Connector Specifications



CONNECTOR SPECIFICATIONS

MODEL NUMBER	POWER	RATING	PLUG NEMA CODE	RECEPTACLE (SUPPLIED BY CUSTOMER)	
				NEMA CODE	DEC PART NO.
872-D	115 V	30 A	L5-30P	L5-30R	12-11194
872-E	230 V	20 A	L6-30R	L6-30R	12-11191

TK-4391

Figure 4-10 872-D, -E Power Controller Input Power Specifications

4.5 BA11-AA, -AB MOUNTING BOX INSTALLATION

The BA11-AA, -AB mounting box is designed to be installed within a standard 48.26 cm (19 in) rack or cabinet on slide mounting assemblies as shown in Figure 4-11.

A slide kit is available (part number 70-18133) and includes one each of the following items: left and right index plates and mounting hardware; left and right slide assembly and mounting hardware.

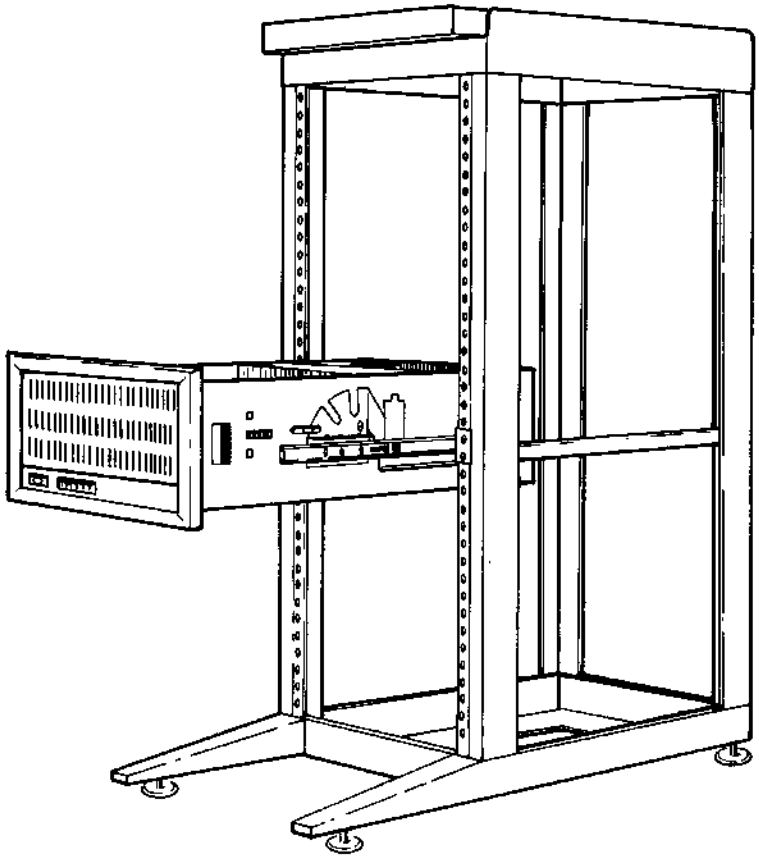


Figure 4-11 Mounting Box in H961 Cabinet

4.5.1 Index Plate Mounting

The index plates supplied with the kit are mounted onto the sides of the BA11-AA, -AB mounting box and permit the box to be tilted on the slides for servicing. To install the index plates refer to Figure 4-12 and perform the following procedures.

1. Position the right index plate onto the pawl as shown. The index plate mounting tab protrudes away from the side of the box.
2. Insert the pivot screw and tighten with a screwdriver.
3. Ensure that the index plate rotates freely when the locking pawl is released.
4. Perform steps 1 and 3 using the left index plate.

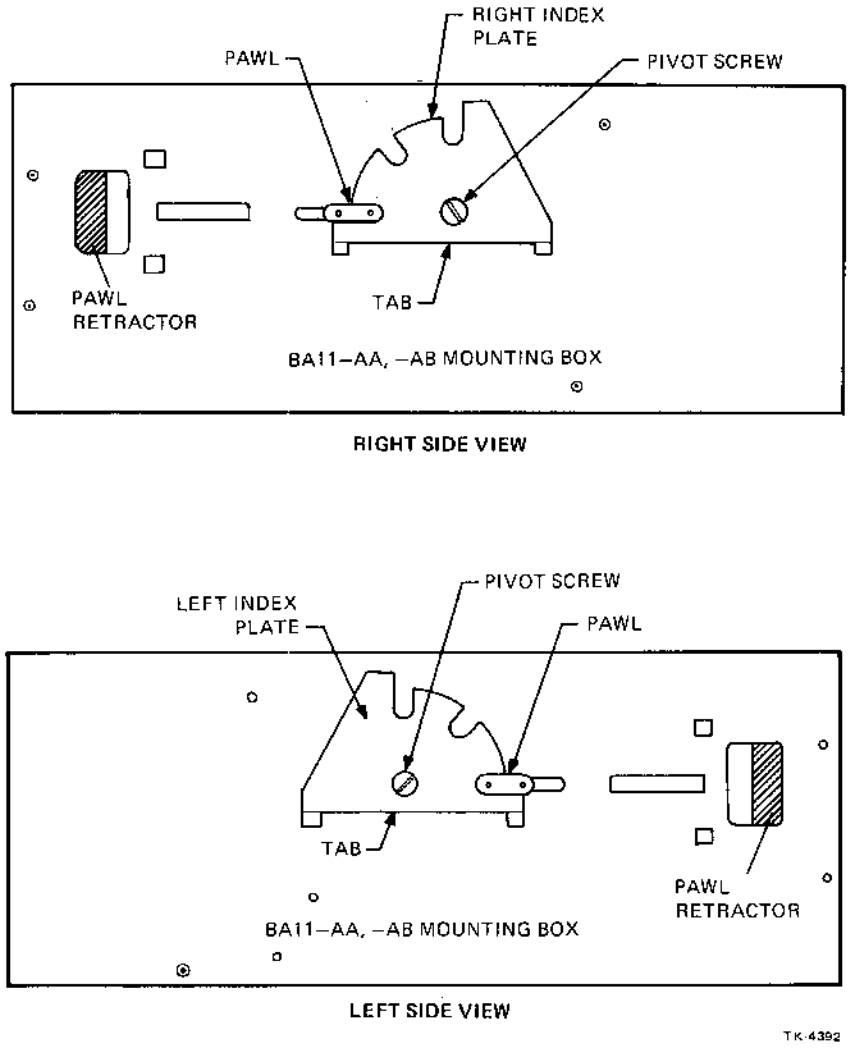


Figure 4-12 BA11-AA, -AB Mounting Box Index Plate Installation

4.5.2 Slide Assembly Mounting

One of two types of slide assemblies is provided with the slide kit option: a single-channel slide set or a double-channel slide set. Figure 4-13 shows each type mounted to the BA11-AA, -AB unit and fully extended from the cabinet. The mounting location of the slides will vary depending on the type of slide. Figure 4-14 shows a typical H961 standard cabinet with the PDP-11/44-CA, -CB unit. The mounting location holes of the single-channel slides for each 26.67 cm (10.5 in) unit are indicated in Figure 4-14. When installing double-channel slides, the hole location numbers will be decreased by two for the same mounting position of the unit.

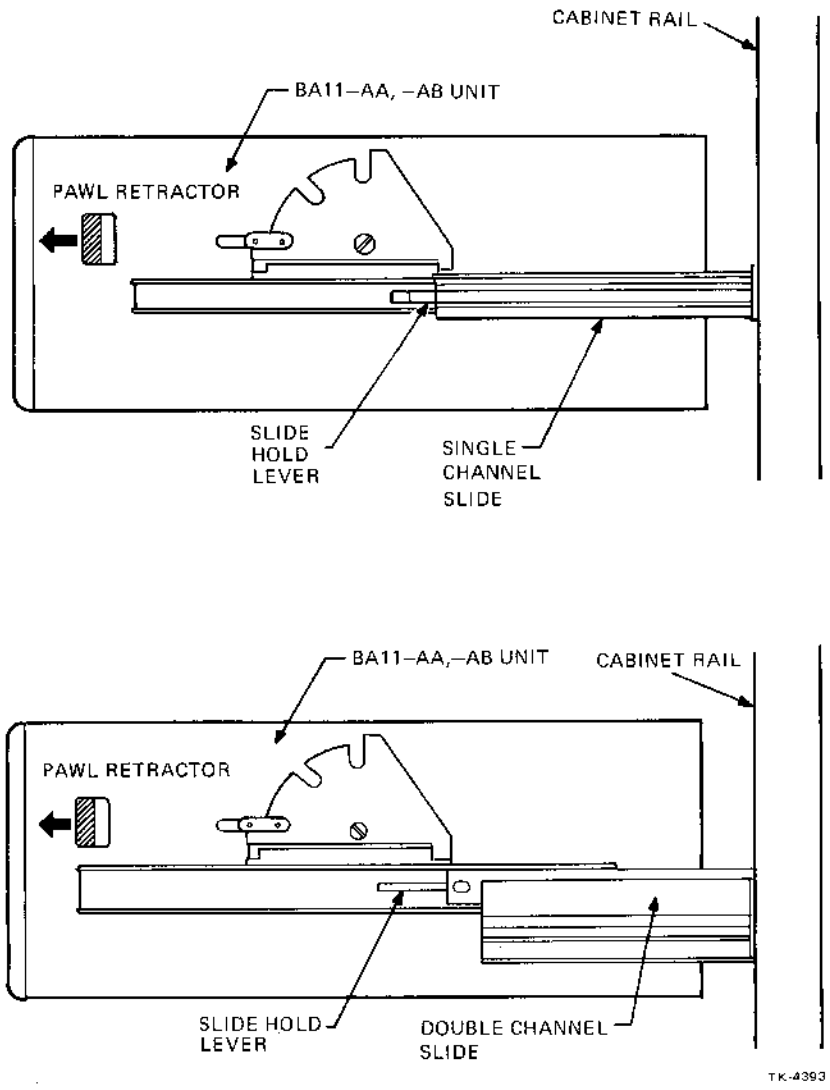


Figure 4-13 Single- and Double-Channel Slide Assemblies

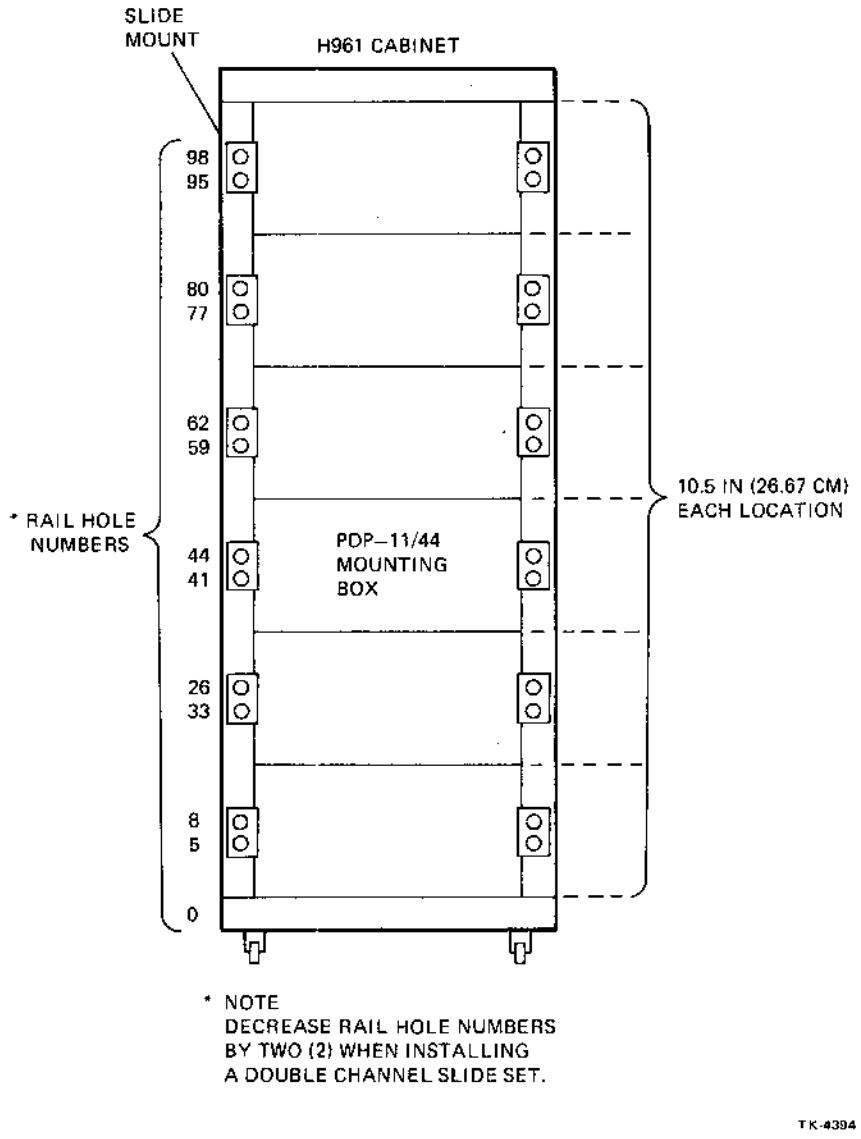


Figure 4-14 H961 Cabinet Slide Mounting Locations

Figure 4-15 shows the hardware and installation of a single-channel slide assembly. The double-channel slide assembly is mounted in a similar manner. To install the slide, perform the following procedure.

1. Position the left slide against the left front and left rear cabinet rail as shown.

2. Insert one 10-32 screw and washer through the top hole in the slide bracket, through the hole in the front rail and into the top threaded hole in the nut plate. Do not tighten.

3. Perform steps 1 and 2 at the left rear rail of the cabinet.

4. Insert one 10-32 screw and washer through the second hole from the bottom in the slide bracket, through the hole in the front rail and into the nut plate. Do not tighten in the front rail.

5. Perform step 4 at the left rear rail of the cabinet.

6. Insert one 10-32 screw and washer through the third hole from the bottom in the slide bracket. Tighten the three screws in the front rail.

7. Perform step 6 at the left rear rail of the cabinet.

8. Perform steps 1 through 7 to install the remaining slide onto the right side of the cabinet.

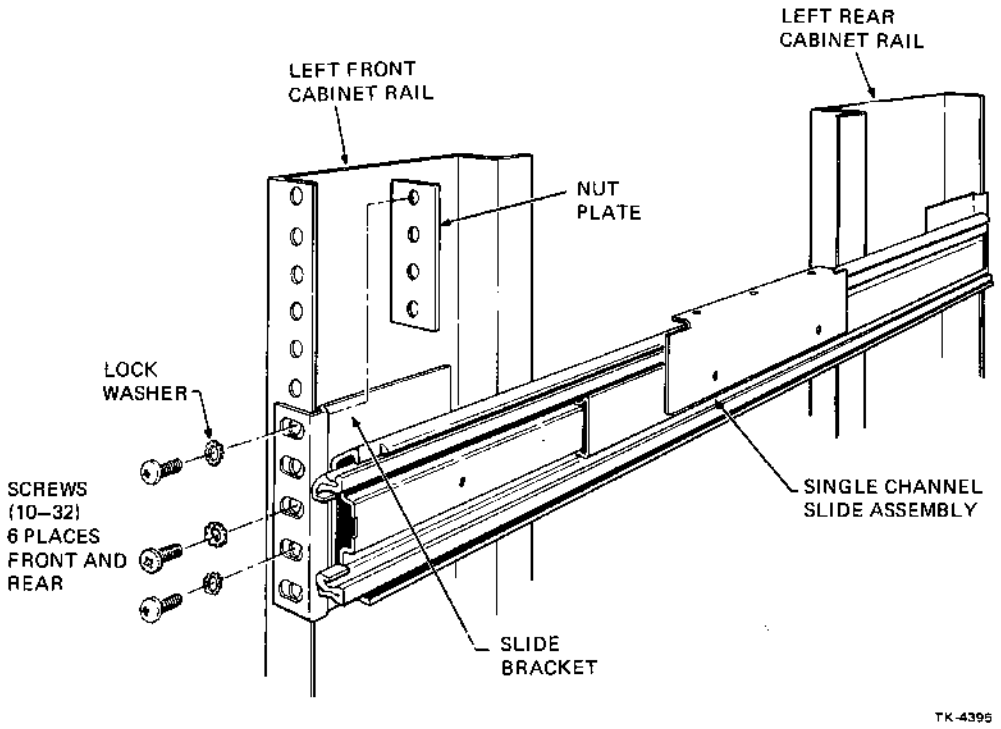


Figure 4-15 Cabinet Slide Installation

4.5.3 Mounting Box to Slide Installation

Figure 4-16 shows the method and hardware used to install the mounting box onto the slide mounting bracket. Perform the following procedure.

1. Extend the left and right slide channels to their maximum position at the front of the cabinet. When fully extended, the channels will be held in place by the slide hold lever shown on Figure 4-13.

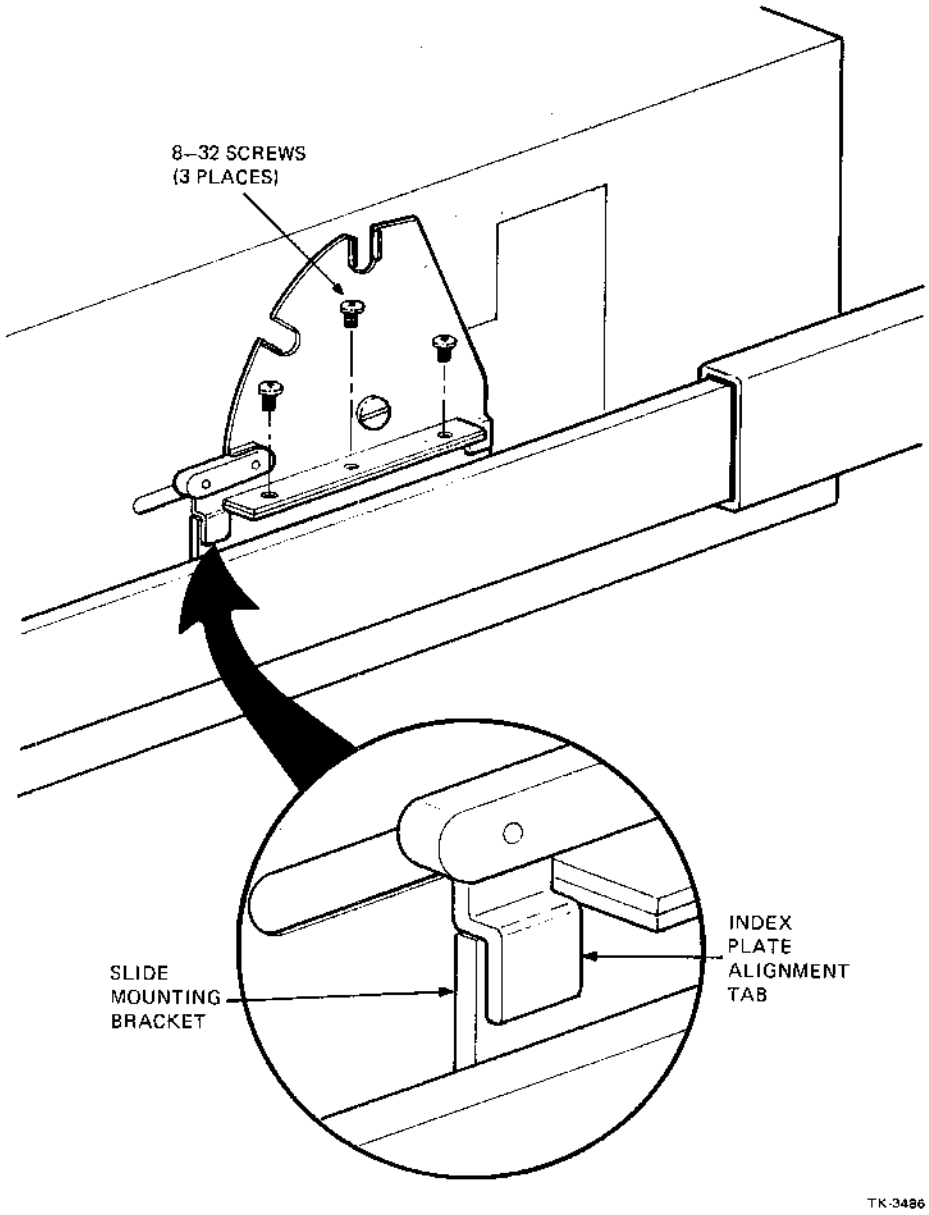


Figure 4-16 Mounting Box to Slide Installation

2. Carefully lift the mounting box over and above the extended slides and set the index plate over the slide mounting bracket on each side of the box. The index plate alignment tabs will engage the sides of the slide mounting bracket.

NOTE

When the slides are fully extended, it may be necessary to force the ends of the slides inward toward the sides of the mounting box.

3. Insert the three 8-32 screws through the left index plate tab and into the threaded holes of the slide mounting bracket.

4. Perform step 3 for the right index plate.

4.6 PDP-11X44 SYSTEM CABINET INSTALLATION

The PDP-11X44-CA, -CB system cabinet is supplied with four rollers on the bottom frame and four leveler feet. The cabinet can be positioned alone or attached to another H9640 series cabinet. When operating alone, a stabilizer bar (option no. H9544-MJ) must be attached to the rear of the unit to prevent the cabinet from tilting when the BA11-AA, -AB box is raised to the servicing position.

4.6.1 Base Stabilizer Installation

Figure 4-17 shows the mounting position and hardware used to install the base stabilizer onto the PDP-11X44 system cabinet. To mount the stabilizer, perform the following procedure.

1. Position the left and right coupler over the collars on the base stabilizer as shown.
2. Slide the stabilizer under the rear of the cabinet and align the mounting holes.
3. Insert the mounting bolt and washer, through the plate, through the slot in the frame, and into the threaded hole of the coupler. Do not tighten.

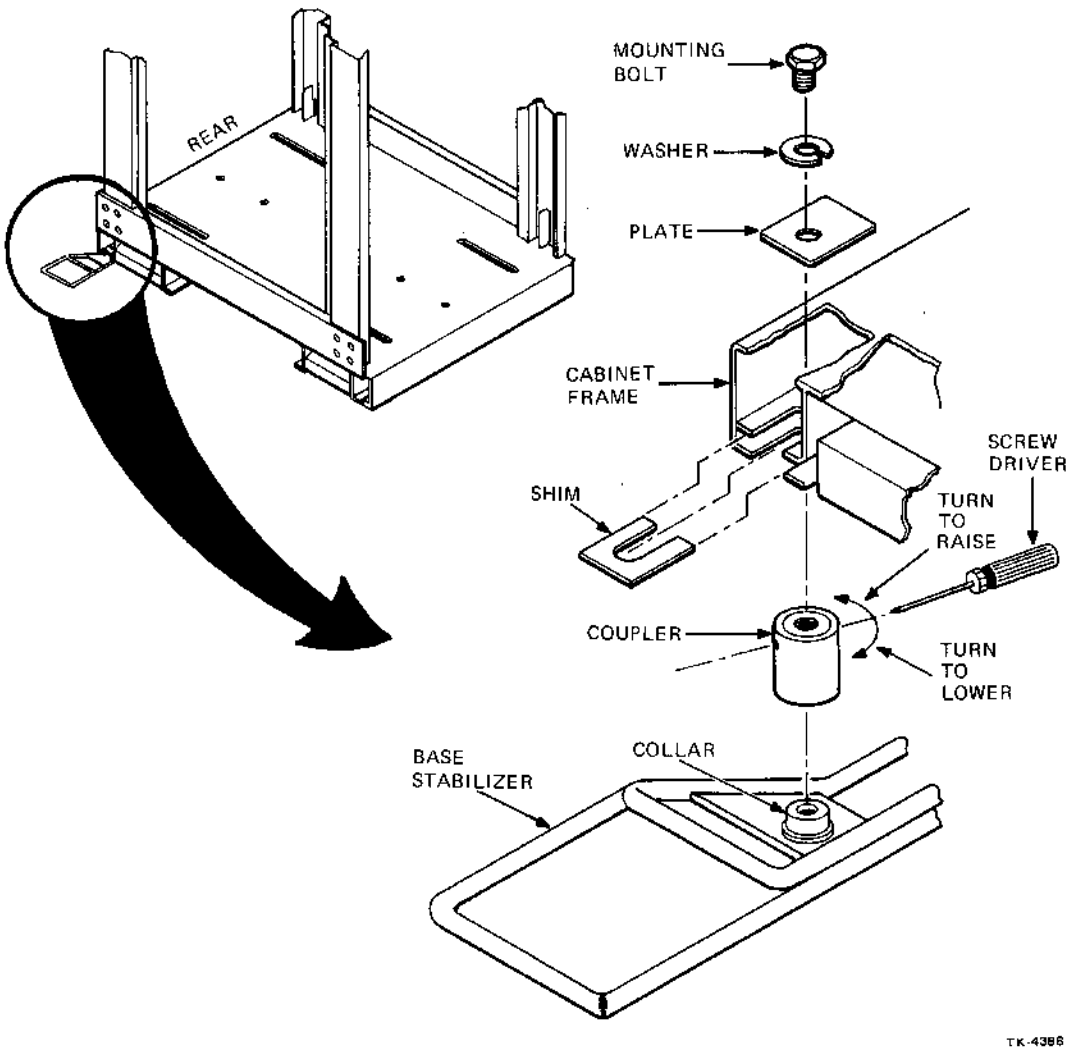


Figure 4-17 Cabinet Stabilizer Mounting

4. To level the cabinet turn the coupler by inserting the shank of a screwdriver through the hole, in the direction desired.

5. Insert the shim into the location as shown.

6. Tighten the mounting screw with a 13/16 in box-end wrench while holding the coupler in position with the screwdriver.

4.6.2 Servicing Area

The rear door of the PDP-11X44 system cabinet can be opened to gain access to the 872-D, -E power controller, the connectors attached to the I/O panel, and the rear panel of the BA11-AA, -AE mounting box. Figure 4-18 shows the service area clearance at the rear of the cabinet to permit the opening of the door and access to the internal units. The clearance also prevents the obstruction of air flow through the cabinet.

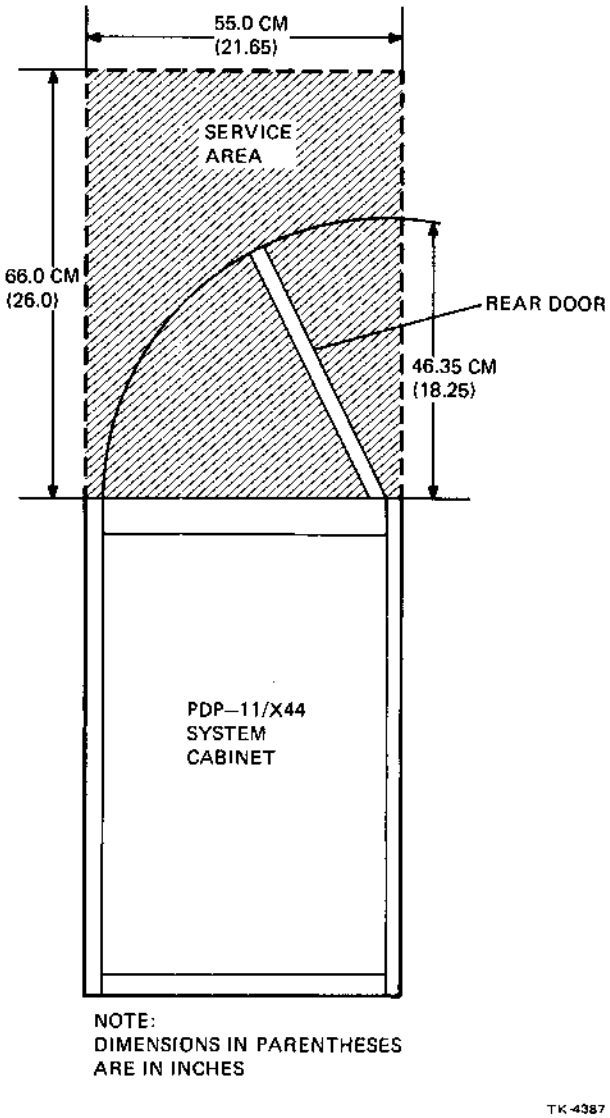


Figure 4-18 PDP-11X44 System Cabinet Service Area

4.7 CABLE ROUTING

The power and signal cables routed between assemblies within a cabinet and externally between cabinets should be properly secured away from sharp objects. Cables connected between cabinets should be protected from damage by routing through a channel or by covering with protective padding. The ac power cables and signal cables should be routed separately from each other to prevent the possibility of signal interference.

4.7.1 Mounting Box Cable Routing

The cable assemblies that are attached to connectors on the modules are routed between the rear card guides through the cable trough directly behind the card guides and through the trough on the left side of the power supply. Figure 4-19 shows the position of the rear card guides and cable troughs.

4.7.2 PDP-11X44 Cabinet Cable Routing

Figure 4-20 shows the routing of the cables at the rear of the system cabinet. The UNIBUS cable is folded and clamped at the rear of the power supply as shown. All other cables such as the console terminal cable from the I/O panel should be clamped to the cabinet channels. The length of all cables should be adequate to allow the mounting box to be raised for servicing without causing cable strain. Nylon tiewraps can be used to secure the cables to cabinet channels.

4.8 POWER CHECKS

The system contains several indicators that can be used to check the ac and dc power to the system. The 872-D, -E Power Controller unit contains an ac indicator that lights when ac power is applied. The control panel of the BA11-A box also contains a DC ON indicator that displays the status of the dc voltage from the power supply.

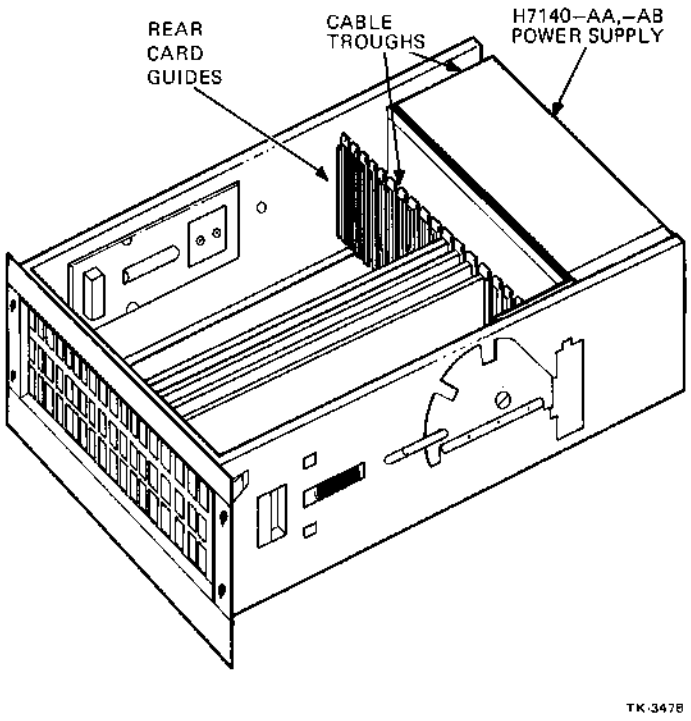


Figure 4-19 BA11-A Cable Routing Locations

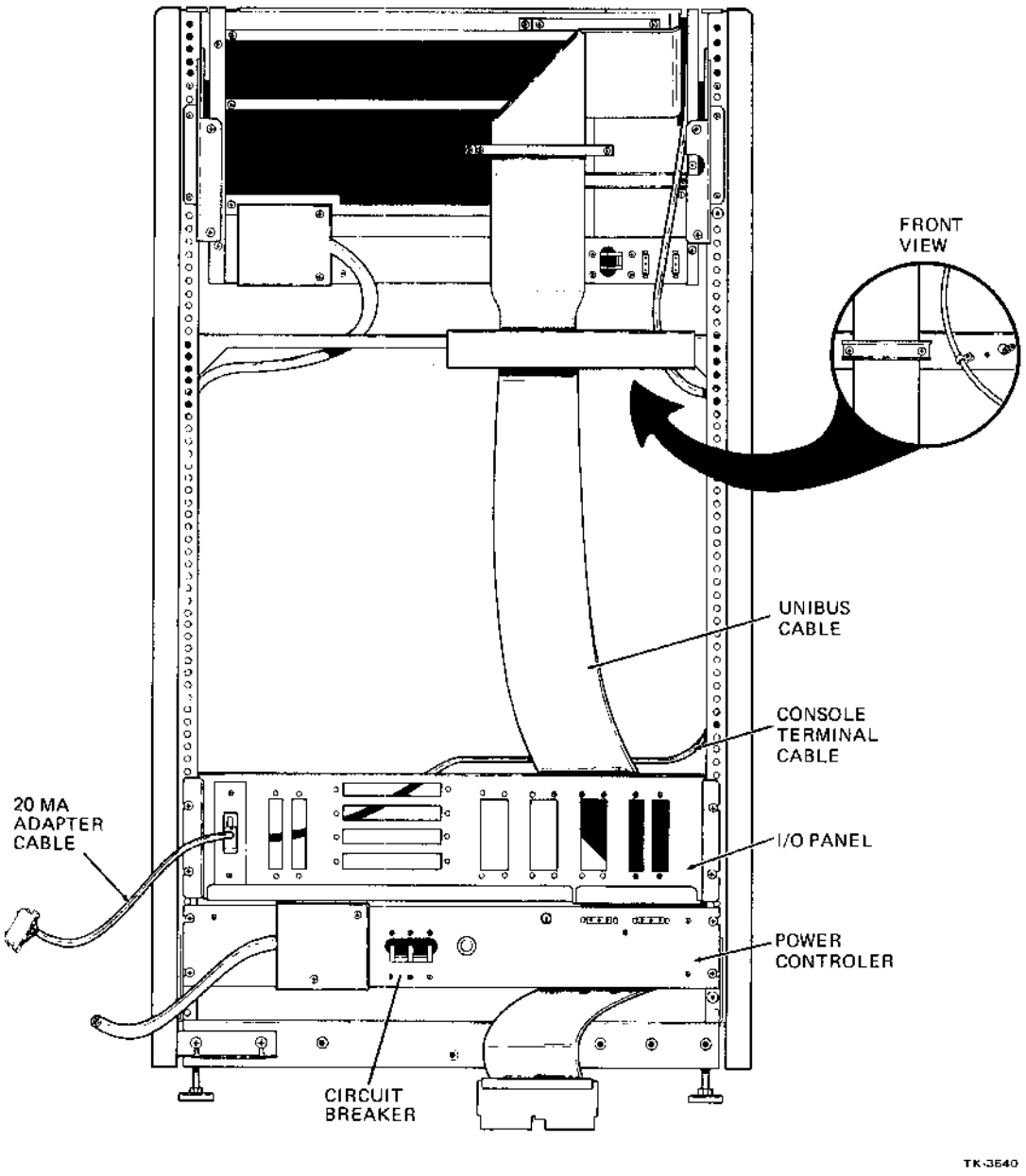


Figure 4-20 PDP-11X44 Cabinet Cable Routing

4.8.1 AC Power Distribution

The ac power in the PDP-11/44 system cabinet is distributed from the 872-D, -E Power Controller or a similar power controller unit. The 872-D, -E unit contains three dual-switched ac receptacles and one dual receptacle that is not switched. The ac power to the switched receptacles is controlled by the LOCAL/OFF/REMOTE switch on the 872-D, -E control panel, or by the keyswitch on the front panel of the mounting box if the LOCAL/OFF/REMOTE switch is in the REMOTE position.

4.8.1.1 Initial AC Power Checks

To check the ac power, perform the following steps.

1. Ensure that the keyswitch on the control panel of the mounting box is in the LOCAL, LOC DSBL or STD BY position.

2. Check that the ac indicator, on the control panel of the 872-D, -E unit, is lighted.

3. If the indicator is not lighted, check the main ac power outlet to ensure that ac voltage is present.

4. If the indicator is lighted, check that the MAIN POWER circuit breaker on the 872-D, -E unit is in the ON position (1).

5. Check that the LOCAL-ON/OFF/REMOTE-ON switch on the POWER CONTROLLER is in the LOCAL-ON or REMOTE-ON position.

6. If in the REMOTE-ON position, set the switch to the LOCAL-ON position.

7. If the ac power is not applied, remove connector P1 or P2 from the dc power control bus on the power control unit.

8. If pin 1 of P1 is open to ground, check the continuity of the power control cable between connector P1 and P2.

9. Remove connector P1 from J3 on the rear of the PDP-11/44 mounting box.

10. If pin 1 of J3 is open to ground, the mounting box wiring is defective.

11. If pin 2 of P1 in step 7 is grounded, an overtemperature condition exists in a unit within the system cabinet or peripheral cabinet.

4.8.2 DC Power Distribution

The dc voltages from the power supply are distributed to the CPU backplane and to any optional backplanes in the mounting box. The DC ON indicator on the control panel of the PDP-11/44 mounting box monitors the dc voltages and provides a visual indication of power failures.

4.8.2.1 DC Power Checks – To check the dc power, perform the following steps.

1. Perform steps 1 through 5 of paragraph 4.8.1.1

2. Measure the +5 V CPU backplane voltage at the connector end of the flexprint cable shown in Figure 4-21.

CAUTION

When measuring the +5 V bus voltage, do not short the +5 V bus and ground bus together.

3. Measure the remaining backplane voltages at connector P1 of the power flexprint cable shown in Figure 4-21. Table 4-2 indicates the voltage and signal connections on P1.

4. If a dc voltage failure is evident, remove and replace the H7140-AA, -AB power supply as described in paragraph 5.4 of this manual.

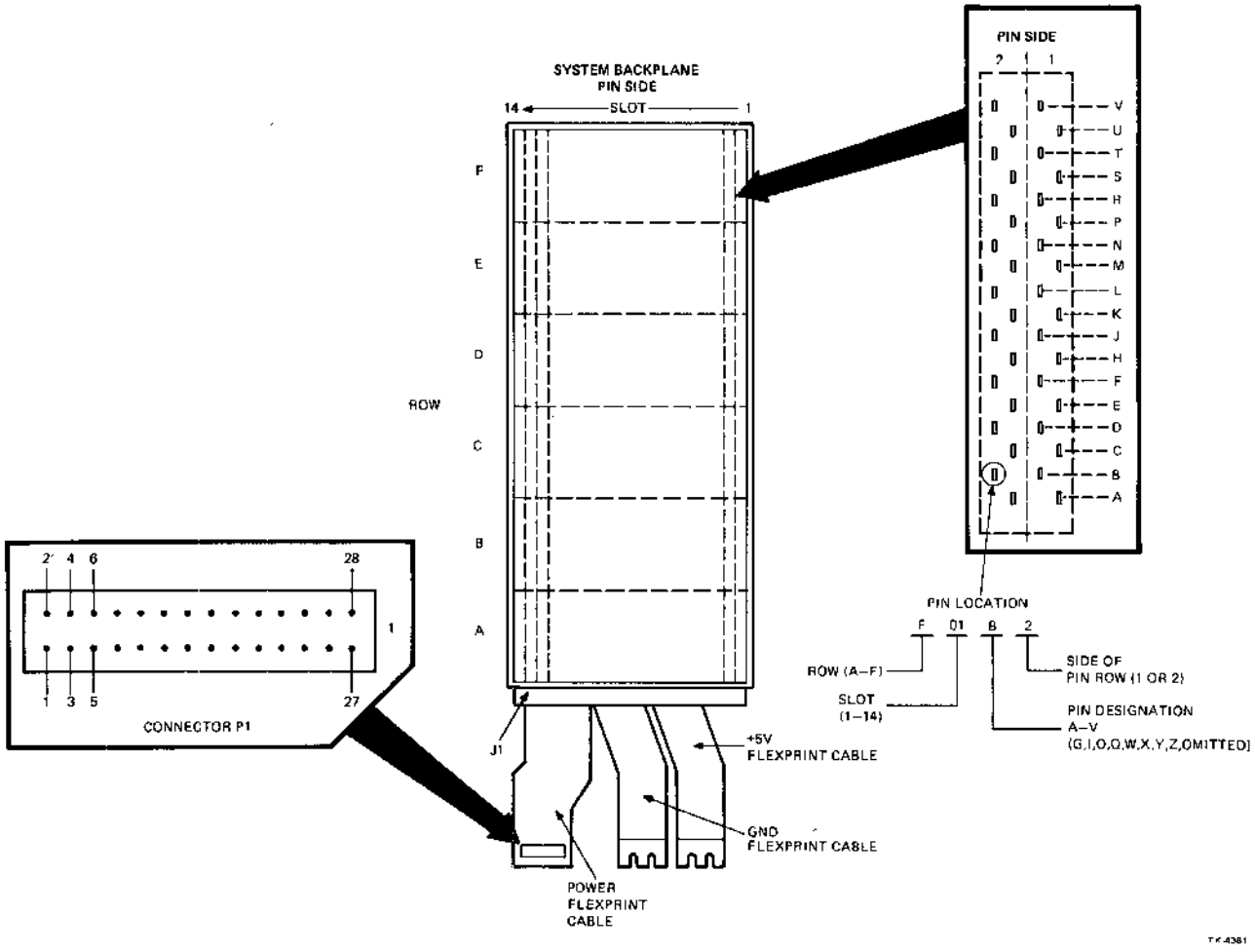


Figure 4-21 Backplane Assembly, Pin Designations

Table 4-2 CPU Backplane Connector P1, Signals and Voltages

Pin	Function
1-10	+5 B
11-16	+12 VB
17, 18	−12 VB
19	LTC
20	BUS ACLO L
21	BOOT ENAB L
22	BUS DCLO L
23	GND SENSE
24	+5 SENSE
25, 27	−15
26,28	+15

4.9 SYSTEM EVALUATION

The PDP-11/44 system can be evaluated by a series of diagnostic exerciser programs. These programs detect and isolate system failures where they occur.

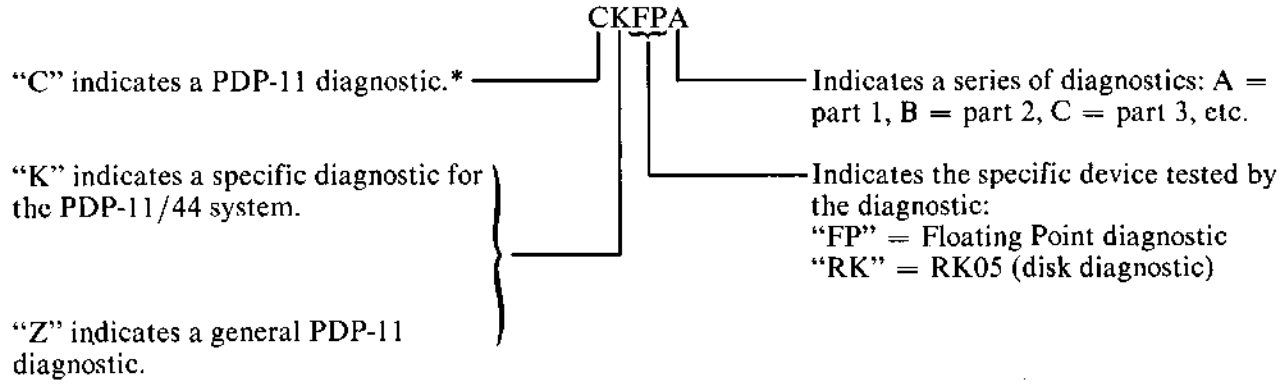
Two basic types of diagnostics are associated with the system, external and internal. The external diagnostics are loaded and executed under XXD04. The internal diagnostic programs are contained in ROMs located on the UBI and MFM modules.

4.9.1 MAINDEC Diagnostic Programs

The MAINDEC diagnostics are external programs which are listed in Table 4-3. These programs are loaded and executed with the MAINDEC diagnostic package XXDP+. This package includes monitor programs, device driver programs and utility programs for the CPU and peripheral devices.

Diagnostics 1 through 11 should be executed in the sequence as listed to obtain the proper results. Each diagnostic test assumes the successful completion of the preceding test.

4.9.1.1 Diagnostic Designations – The designations assigned to the PDP-11 family of diagnostic programs are described as follows.



* Not used on diagnostic disk pack or on magnetic tape.

The "xy" designation that appears after the MAINDEC diagnostic listing on the table contains the following information.

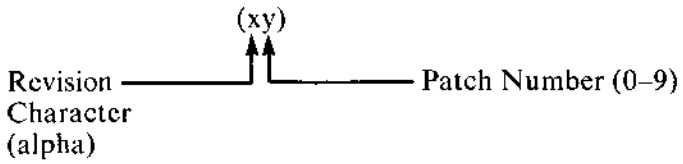


Table 4-3 PDP-11/44 MAINDEC Diagnostic Programs

MAINDEC Diagnostic	Operating Sequence	Title
CKK FA ⟨xy⟩	1	11/44 Diagnostic ROM*
CKK AA ⟨xy⟩	2	11/44 CPU/EIS
CKK AB ⟨xy⟩	3	11/44 Traps
CKK TA ⟨xy⟩	4	11/44 Mem. Mgt. Prt A
CKK TB ⟨xy⟩	5	11/44 Mem. Mgt. Prt B
CZM 9B ⟨xy⟩	6	M9312/11/44 UBI Boot
CKK UA ⟨xy⟩	7	11/44 UBI Map
CKK KA ⟨xy⟩	8	11/44 KK11-B Cache
CZM SD ⟨xy⟩	9	MSL-M/L Memory
CZD LD ⟨xy⟩	10	DL11-W/MFM SLU
CKK AC ⟨xy⟩	11	11/44 Power Fail
CKF PA ⟨xy⟩	12	FP11-F Part A
CKF PB ⟨xy⟩	13	FP11-F Part B
CKF PC ⟨xy⟩	14	FP11-F Part C
CZK EE ⟨xy⟩	15	PDP-11 CIS Instr. Exerciser
CZK UA ⟨xy⟩	16	UNIBUS Systems Exerciser Diag.
CZK UB ⟨xy⟩	17	UNIBUS Exerciser Module

*Included with the M7098 UBI module.

4.9.2 Internal Diagnostic Programs

The internal diagnostics consist of the PDP-11/44 diagnostics contained in the CPU diagnostic ROM located on the UBI module and the console diagnostics contained in a ROM on the MFM module. The CPU diagnostic, if selected (refer to Paragraph 3.3.3.2), is initiated by one of the following actions:

1. Pressing the front panel toggle switch to the BOOT position.
2. Typing the bootstrap command at the console when in the console mode.
3. Powering up the system with switch S1 on control module in the ON position (powerup boot enabled.)

Table 4-4 lists the LOOP/HALT addresses and the test that failed the CPU diagnostic. When a failing test is in a loop, enter console mode and halt the CPU with a halt command from the console. The console will then print the LOOP address.

The console diagnostic is initiated by one of the following actions:

1. When the CPU is halted except by a HALT command from the console.
2. When entering console mode using a ^P command.
3. When using the T or T/E command when in console mode.

Table 4-4 CPU Diagnostic ROM Error Indicators

Loop/Halt Address	Test No.*	Sequence or Instruction Failure
165070	1	Unconditional branch
165106	2	CIR, mode 0, BMI, BVS, BHI, BLT, BLOS
165122	3	DEC, mode 0, BPL, BEQ, BGE, BLE
165134	4	ROR, mode 0, BUC, BHIS, BNE
165172	5	Register data path
165202	6	ROL, BCC, BLK
165220	7	ADD, INC, COM, BCS, BLE
165240	10	BOR, DEC, BIS, ADD, BLO
165246	11	COM, BLOS
165260	11	BIC, BGT, BLE
165302	12	SWAB, CMP, BIT, BNE BGT
165312	13	MOVB, BPL
165334	13	SOB, CIR, TST, BNE
165346	14	JSR
165356	14	Push onto stack failed
165366	14	RTS
165400	14	RTI
165406	14	JMP
165526	15	Main memory data error WO/cache
165550	15	Main memory data error WO/cache
165634	16	No hit in cache**
165652	16	No hit in cache**
165664	15 or 16	Parity error
165702	Any test	Hardware trap to 4 (check stack)

*Tests 1-14 loop on error. Tests 15-16 halt on error.

** Cache memory may be manually disabled by switches S1 and S2 on the cache memory module.

CHAPTER 5
REMOVAL/REPLACEMENT PROCEDURES

The PDP-11/44 system is designed to permit units and assemblies to be easily removed and replaced. This section includes the removal and replacement procedures for the BA11-AA, -AB mounting box, the H7140-AA, -AB power supply, and the fan assembly. For detailed removal and replacement procedures related to other units supplied with the system, refer to the appropriate manuals supplied.

5.1 BA11-AA, -AB MOUNTING BOX IN SYSTEM CABINET

In the PDP-11X44 system, the BA11-AA, -AB mounting box is located at the top of the system cabinet. Two types of release mechanisms are in use to allow the BA11-A mounting box to be raised to the servicing position in the PDP-11X44 cabinet. The type of mechanism that the cabinet contains can be identified by the top cover configuration as shown in Figure 5-1. The cabinet with the type A release has filler strips located at the rear of the unit. The cabinet with the type B release has a one piece top cover.

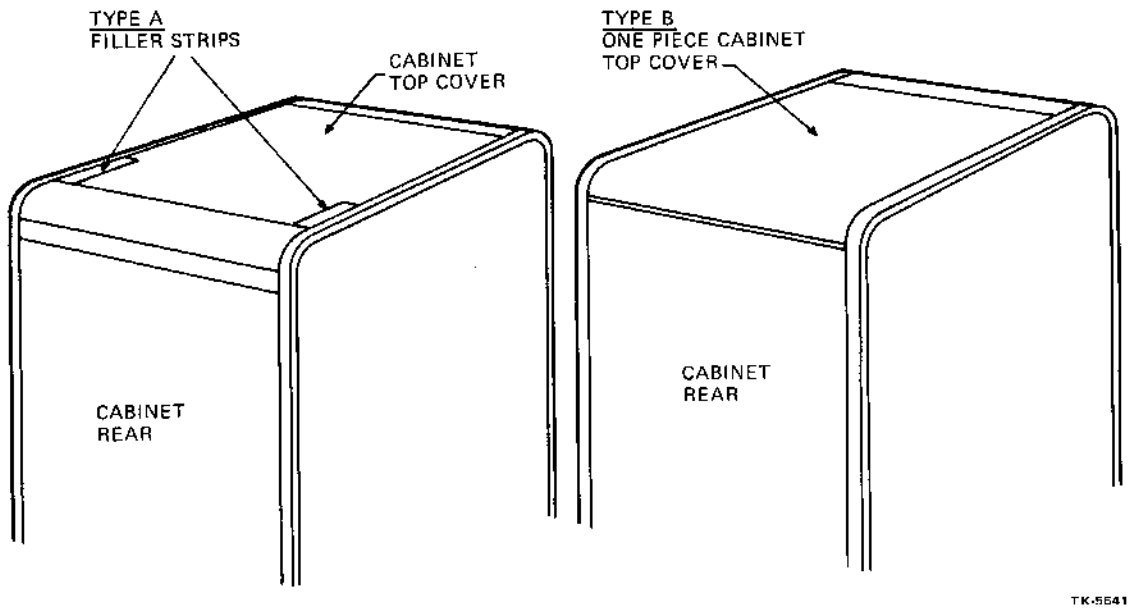


Figure 5-1 PDP-11X44 Cabinet Type Identification

5.1.1 Mounting Box Removal

To remove the BA11-AA, -AB mounting box from the PDP-11X44 system cabinet, perform the following procedure.

1. Open the rear door of the cabinet. Use a 4mm (5/32 in) hex wrench to release the door fastener.

2. Remove the ac power from the power controller by setting the circuit breaker in the down (0) position (Figure 4-20).

3. Remove the BA11-AA, -AB power cord plug from the nonswitched receptacle at the rear of the power controller.

4. Cut or release any fasteners used to secure the power cord to the cabinet frame.

5. If the release mechanism is type A (Paragraph 5.1), insert the blade of a small screwdriver into the hole behind the slot which is located at the top, right side of the front bezel.

   a. Release the latch which holds the mounting box by sliding the screwdriver in the direction shown in Figure 5-2.

   b. Raise the front of the mounting box until the unit is approximately at a 45° angle with the top of the cabinet.

   c. Loosen the four (10-32) screws which hold the cover brackets to the left and right sides of the mounting box (Figure 5-3). Do not remove the screws.

   d. Remove the top cover.

   e. Lower the front of the mounting box until it is in the normal position and the latch engages.

6. If the release mechanism is type B, remove the screw (10-32) that secures the top cover ground lead to the back of the cabinet frame (Figure 5-4).

   a. Use a slot head screwdriver to release the two captive screws that secure the back of the top cover to the cabinet.

   b. Raise the back of the top cover so the pins are released from the spring latch at the front of the cover.

   c. Remove the top cover.

7. Disconnect all bus and I/O cable connectors attached to the modules within the unit.

8. At the rear of the BA11-AA, -AB box, remove and retain the two 1/4 inch nuts used to secure the cable clamp bar to the power supply (Figure 4-20).

9. Remove the cables from the cable trough in the BA11-AA, -AB mounting box and feed the cables toward the back of the cabinet and away from the mounting box.

10. If the release mechanism is type A, release the latch (Figure 5-2) and raise the front of the mounting box.

11. If the release mechanism is type B, locate the left and right slide latches on the angle brackets attached to each side of the BA11-AA, -AB mounting box (Figure 5-5).

    a. Slide the latches, in the direction shown, to release the latch from the holding pin.

12. Raise the front of the mounting box to the maintenance position shown in Figure 5-6 and raise the safety lever to hold the mounting box.

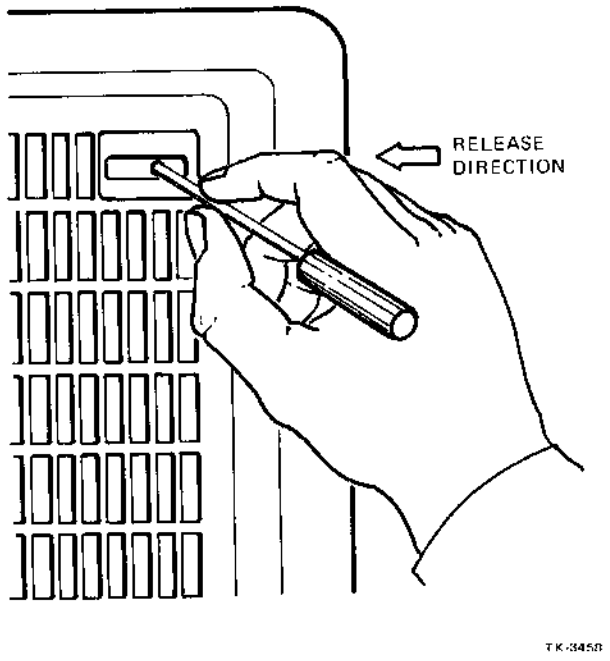


Figure 5-2 PDP-11X44 Type A Cabinet Mounting Box Release Lever

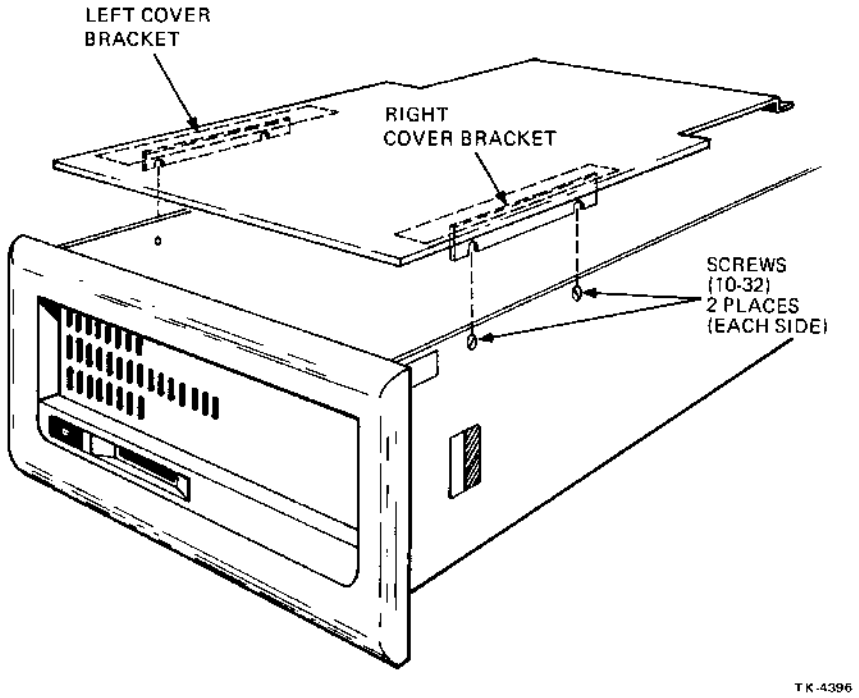


Figure 5-3 PDP-11X44 Top Cover Mounting (Type A)

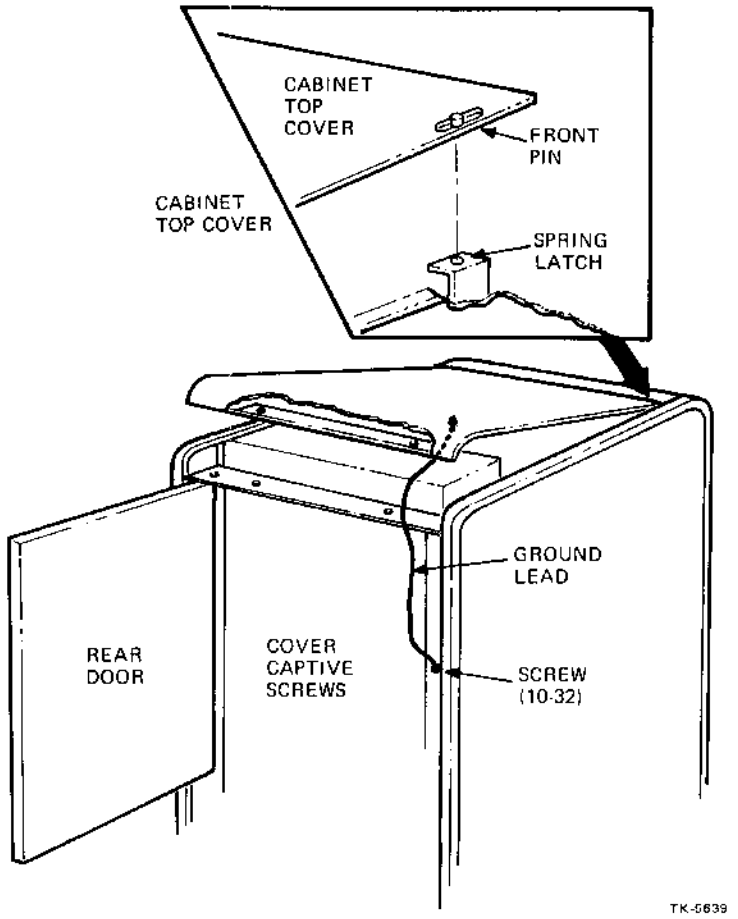


Figure 5-4 PDP-11X44 Cabinet Top Cover Mounting (Type B)

WARNING

When the gas springs are removed, the safety lever cannot support the weight of the BA11-A mounting box. The box should be supported by a field service person while servicing is continued.

13. Remove the retaining clip from the upper ball connectors of the gas spring on the left and right interface bracket (Figure 5-7). Use needle-nose pliers to help the clip removal.

14. Remove the retaining clip from the lower ball connectors of the gas spring on the left and right side of the cabinet.

15. Support the mounting box.

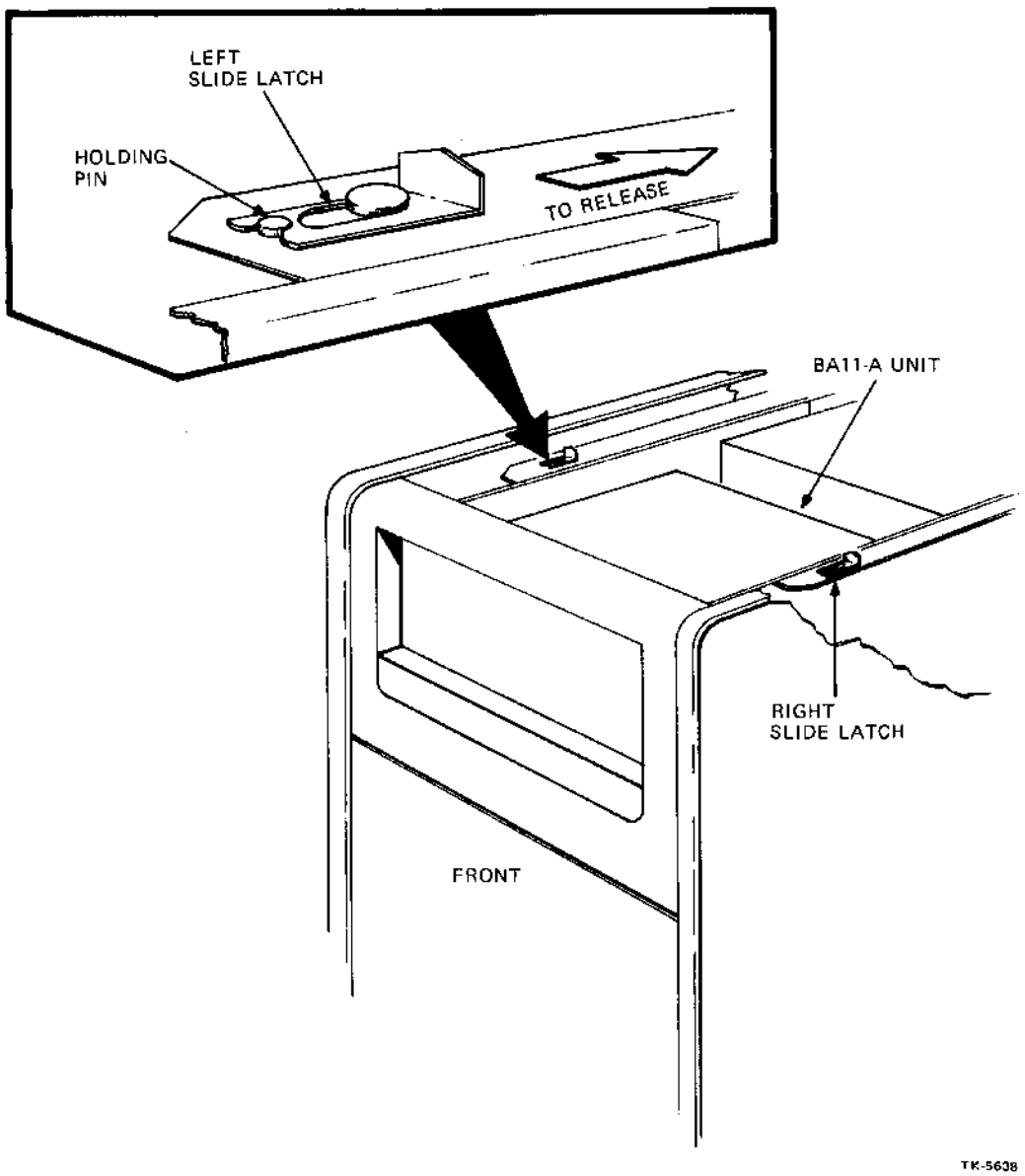


Figure 5-5 PDP-11X44 Cabinet, Slide Latch Locations

16. Remove the ball connectors from the studs on the right side of the cabinet by inserting a screwdriver blade between the ball connector and the ball stud mounting surface.

17. Remove the ball connectors from the studs on the left side of the cabinet using the procedure described in step 16.

18. At the rear of the cabinet remove the four 10-32 screws and washers (two on each side near the top of the mounting box facing toward the center of the cabinet) which secure the pivot bracket to the cabinet frame on the left and right side of the cabinet (Figure 5-7). These screws can not be reached once the box is lowered.

19. At the front of the cabinet, while supporting the weight of the box, lower the safety lever, and lower the mounting box to its normal position (Figure 5-6).

NOTE

When the gas springs have been removed, the mounting box is not properly supported. If not properly supported, it can fall causing possible personal injury.

20. At the rear of the cabinet, remove and retain the two 10-32 screws and washers on the left and right side of the cabinet which secure the pivot bracket to the mounting box (Figure 5-7).

21. Grasp the bottom of the mounting box at the front and rear and gently slide the box toward the front of the cabinet. Lift the back of the mounting box and slide the box forward and away from the cabinet frame.

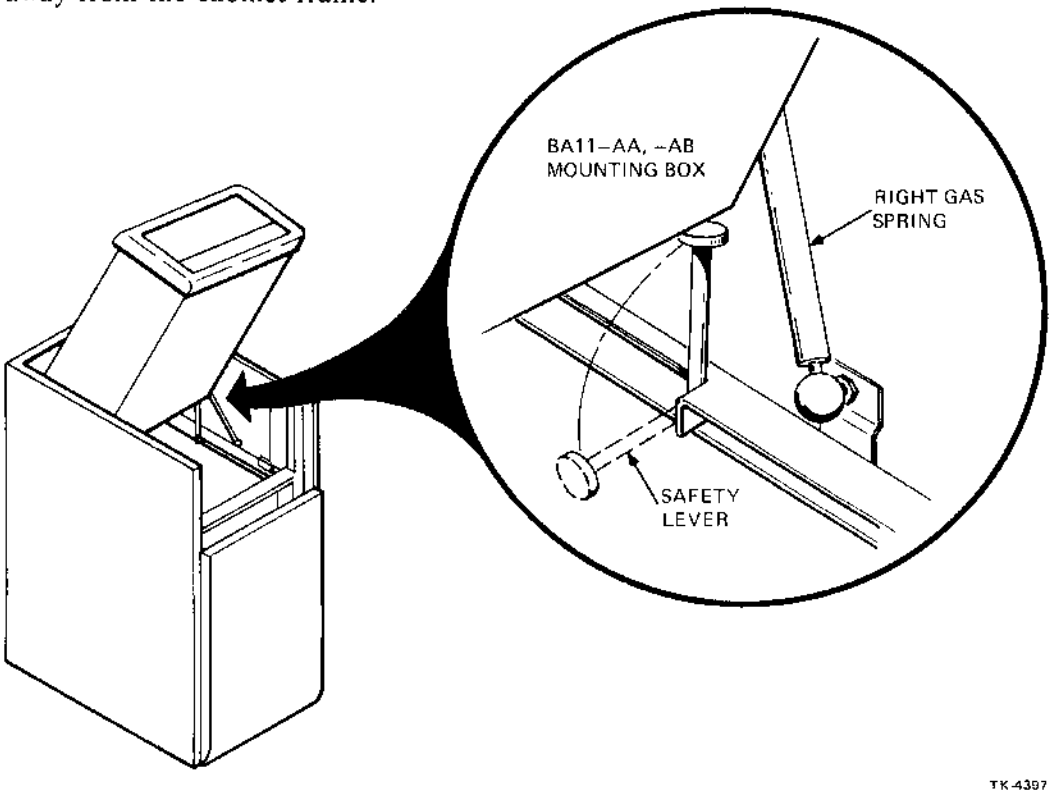


Figure 5-6 PDP-11X44 Cabinet Safety Lever

CAUTION

Removal of the mounting box requires two people due to its weight, with one person lifting from the left side and one person lifting from the right side of the cabinet.

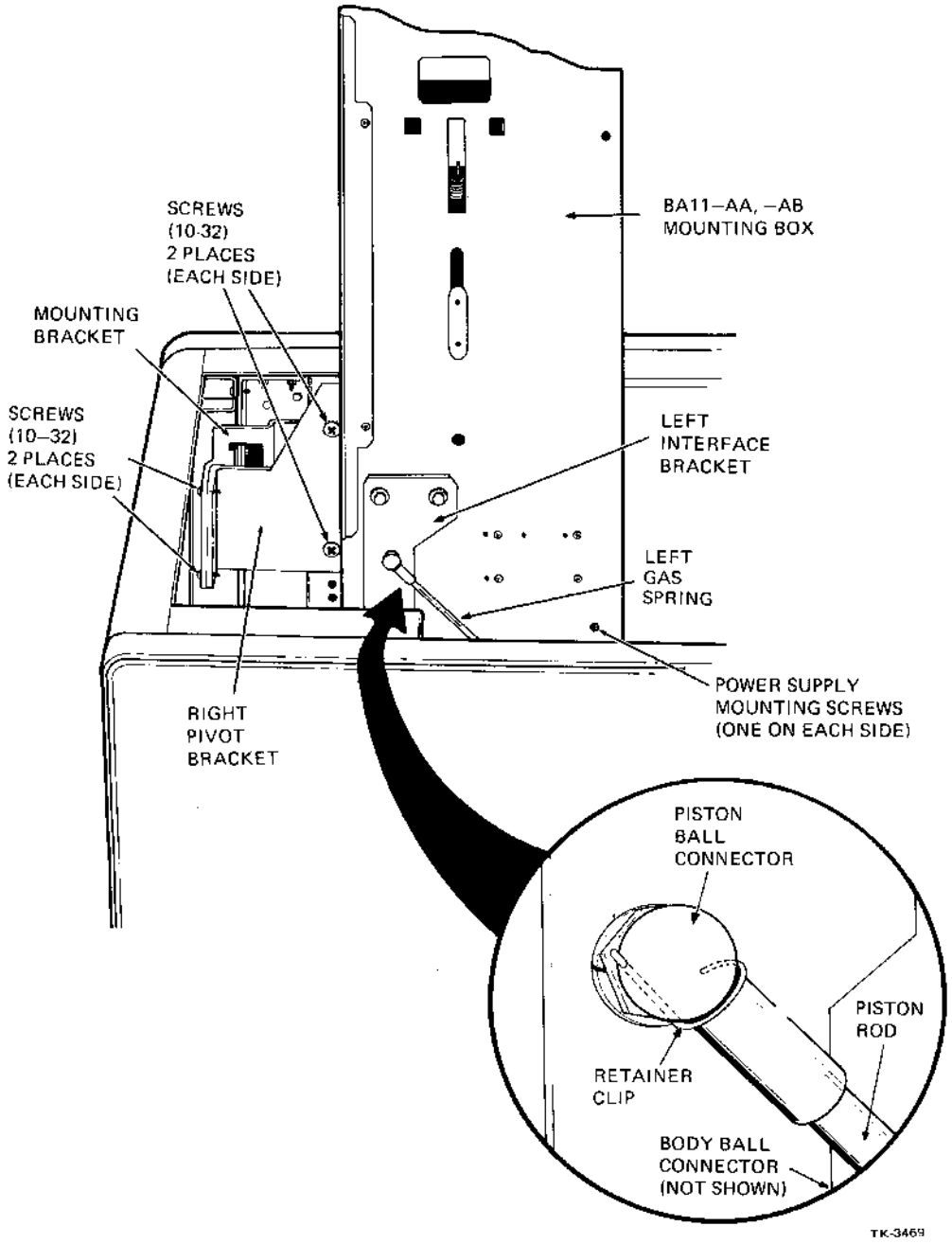


Figure 5-7 PDP-11X44 Cabinet Mounting Box Hardware

5.1.2 Interface Bracket Removal/Installation

If the mounting box to be installed does not have the interface and pivot bracket mounted on each side, remove the brackets from the box to be replaced and install using the following procedure.

1. Using a 1/2 in open- or box-end wrench, remove the two 5/16-24 bolts and the 5/16-24 ball stud located on the left and right side of the mounting box (Figure 5-8).

2. Remove the two bracket assemblies and, using the hardware previously removed, install onto the left and right side of the replacement mounting box. Do not tighten bolts.

3. Align the top of the interface bracket parallel with the top of the mounting box and at the dimension shown in Figure 5-8.

4. Tighten the two 5/16-24 bolts and the ball stud.

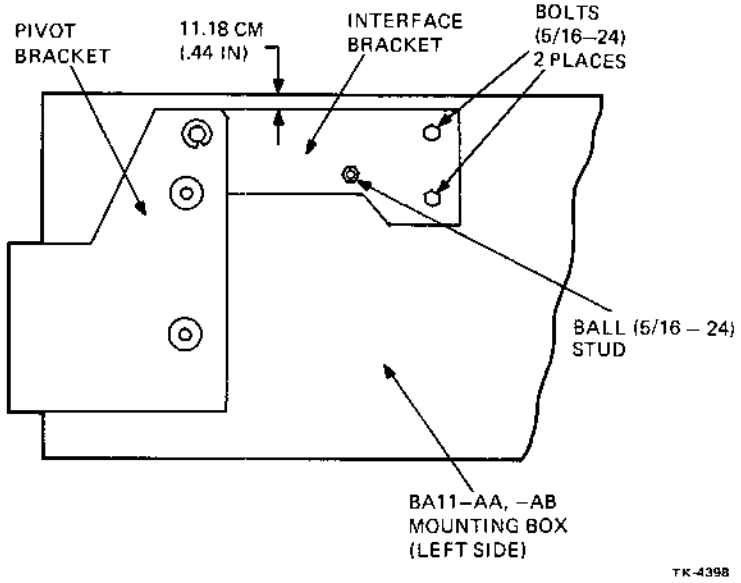


Figure 5-8 Interface Bracket Mounting

5.1.3 Mounting Box Replacement

Perform the following procedure to install the BA11-AA, -AB mounting box in the PDP-11X44 system cabinet.

CAUTION

Installation of the mounting box requires two people due to its weight, with one person lifting from the left side and one person lifting from the right side of the cabinet.

1. Grasp the bottom of the mounting box at the front and rear and position the box on the support rails (see Figure 4-4) with the front of the unit extending away from the front of the system cabinet.

2. Slide the mounting box toward the rear of the unit while lifting the rear of the box to clear the ball stud (Figure 5-8).

3. At the rear of the cabinet, install the two 10-32 screws and washers, removed in step 20 of Paragraph 5.1.1, in the angle part of the left and right interface bracket (Figure 5-7). Do not tighten the screws.

WARNING

When the gas springs are removed, the safety lever cannot support the weight of the BA11-A mounting box. The box should be supported by a field service person while servicing is continued.

4. Raise the front of the mounting box to the position shown in Figure 5-7, raise the stop lever and hold the mounting box in position.

5. Replace the two 10-32 interface bracket screws and washers, removed in step 18 of Paragraph 5.1.1, into the left and right cabinet frame (Figure 5-7).

NOTE

It may be necessary to shift the position of the mounting box in a direction that will cause the holes of the interface bracket to be properly aligned with cabinet frame holes.

6. Tighten the screws installed in step 5.

7. Replace both gas springs, removed in Paragraph 5.1.1, snapping the lower ball connectors on first and then the upper ball connectors.

8. Install the four retaining clips removed in Paragraph 5.1.1.

9. Lower the stop lever and lower the mounting box to its normal operating position.

10. Route the cables removed in step 9 of Paragraph 5.1.1 through the cable trough.

11. Insert the cable connectors removed in step 7 of Paragraph 5.1.1.

12. Install the cable clamp removed in step 8 of Paragraph 5.1.1.

13. Release the mounting box latch as described in steps 5 and 6 of Paragraph 5.1.1.

14. Raise the front of the mounting box as described in steps 5 and 6 of Paragraph 5.1.1.

15. Install the top cover onto the mounting box and tighten the screws which were released in step 5 or 6 of Paragraph 5.1.1.

16. Lower the front of the unit to its normal operating position and engage the latch.

5.2 BA11-AA, -AB SLIDE MOUNTED REMOVAL/REPLACEMENT

Refer to Chapter 4 for the installation of the BA11-AA, -AB mounting box on slide assemblies.

5.3 FAN ASSEMBLY

The fan assembly is installed on the right side of the BA11-AA, -AB mounting box and can easily be removed for servicing. The assembly contains three fans, each of which can be removed and replaced.

5.3.1 Fan Assembly Removal/Replacement

Perform the following procedure to remove the fan assembly and fans.

1. Remove the ac power from the BA11-AA, -AB mounting box by removing the ac power cord plug from its receptacle.

2a. In the PDP-11X44 system cabinet, perform steps 5, 6 and 11 of paragraph 5.1.1.

2b. If the mounting box is installed on slides in a cabinet, insert a screwdriver blade into the hole behind the slot which is located at the top, right side of the front bezel (Figure 5-9).

3. Release the latch which holds the mounting box by sliding the screwdriver in the direction shown.

4a. In the PDP-11X44 system, raise the front of the mounting box to its maintenance position and raise the safety lever (Figure 5-6).

4b. If the mounting box is installed on slides, pull the front of the box until the slide hold levers are engaged (Figure 4-13).

4c. Release the pawl retractors on each side of the mounting box and tilt the box 90° to the maintenance position.

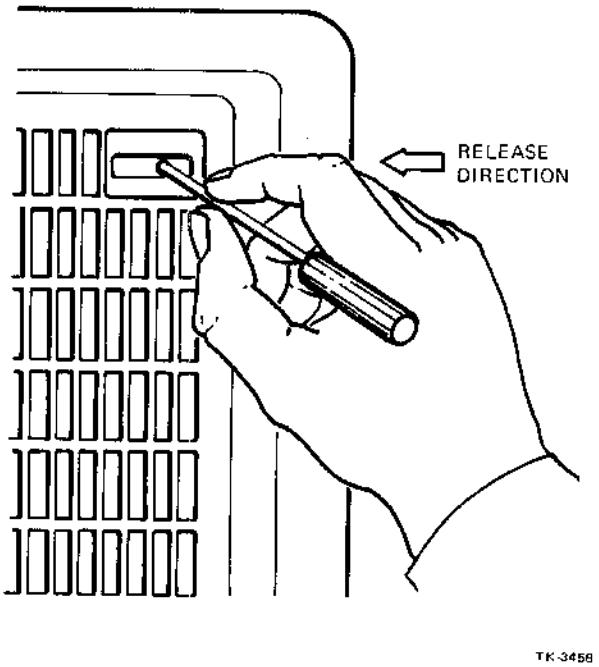


Figure 5-9 Mounting Box Release Lever

5. Remove the two 6-32 screws which secure the fan assembly to the side of the box (Figure 5-10).

6. Slide the fan assembly away from the side of the box approximately 5 cm (2 in) and disconnect connector P1 from J1.

7. Continue to slide the assembly away from the box.

NOTE

Any of the three fans can be replaced by disconnecting the power plug on the fan and removing the four 6-32 mounting screws which secure the fans to the slide. Use only the specified replacement fan and mount the new fan to assembly using the hardware removed.

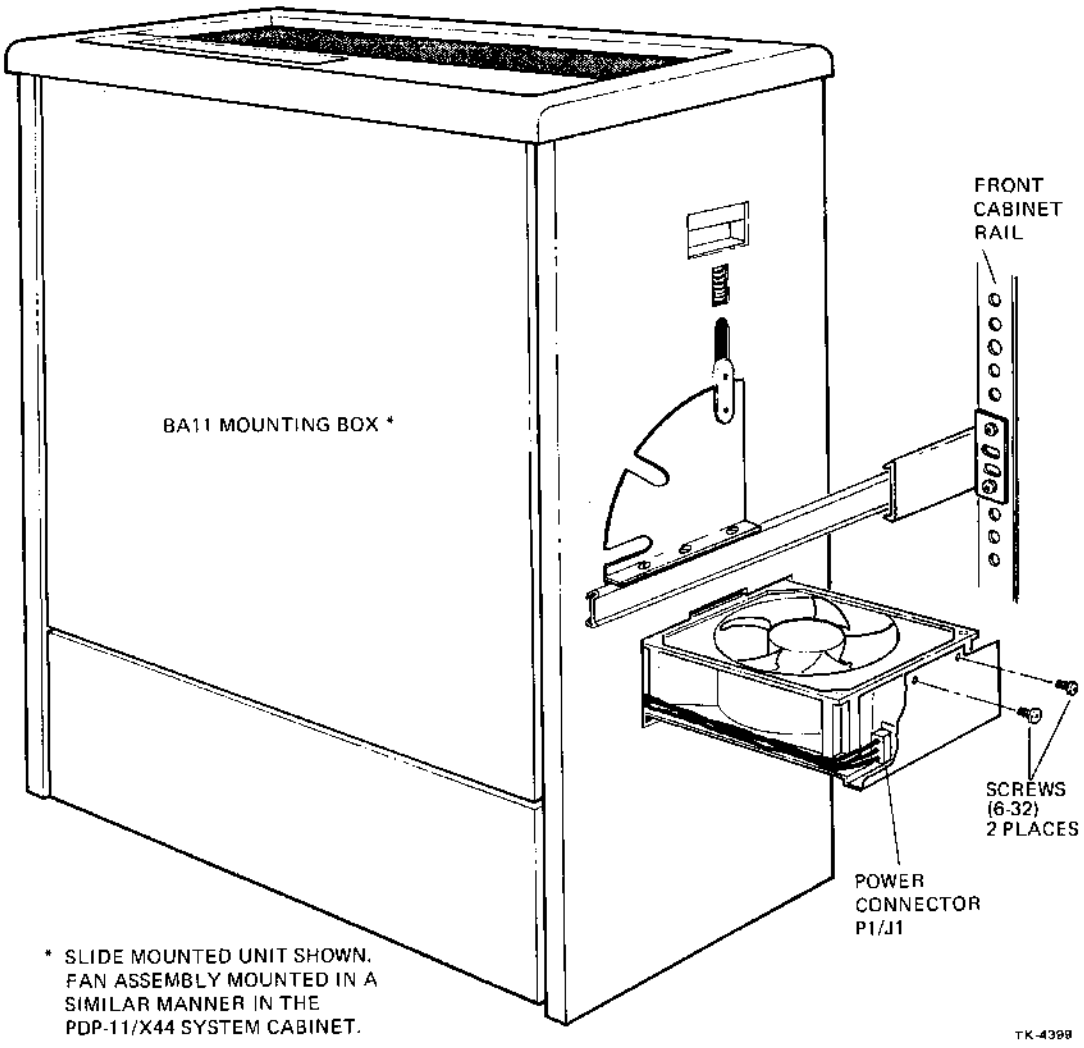


Figure 5-10 Fan Assembly Removal

8. To replace the fan assembly, perform the instructions described in steps 5, 6, and 7 in the reverse order and reset the mounting box in its normal operating position.

NOTE

The slide holding levers (Figure 4-13) must be released by pressing inward before the slides will retract.

5.4 H7140-AA, -AB POWER SUPPLY REMOVAL/REPLACEMENT

Before removing the power supply assembly from the mounting box, remove the power cord plug of the power supply from the ac power distribution connector. To remove and replace the power supply, perform the following procedure.

5.4.1 Power Supply Removal

1. From the rear of the cabinet, remove and retain the two 8-32 screws located in each of the two chassis angles at the rear of the mounting box (Figure 5-11).

2. Perform steps 1 through 4 of Paragraph 5.3.1

3. Remove and retain the four 6-32 screws that secure the bottom cover to the mounting box (Figure 5-12). Remove the cover.

4. Remove and retain the four 6-32 screws that secure the cover plate to the bottom of the power supply assembly. Remove the cover.

5. Remove and retain the 10-32 screw that secures the ground lead to the ground bus (Figure 5-13).

6. Loosen the two 3/8 in nuts on the clamp that holds the ground flex print cable to the ground bus bar.

7. Loosen the two 3/8 in nuts on the clamp that holds the +5 V flex print cable to the +5 V bus bar.

8. Slide the ground and +5 V flex print cables away from the clamps and bend up toward the backplane.

9. Remove the power flex print connector P1 from power supply connector J11 and bend up toward the backplane.

10. Remove connector P3 of the CIM cable assembly from connector J1 of the power supply. Move the tabs on each side of J1 to release P3 (Figure 5-14).

11. Remove the 3/8 in nut that secures the ground lead of connector P3, removed in step 10, to the chassis ground stud.

12. If one or more additional backplanes are mounted in the box, remove the connectors attached to J2, J3 and J4 of the power distribution board. Remove the backplane connectors from P2, P3 and P4 of the power distribution harness.

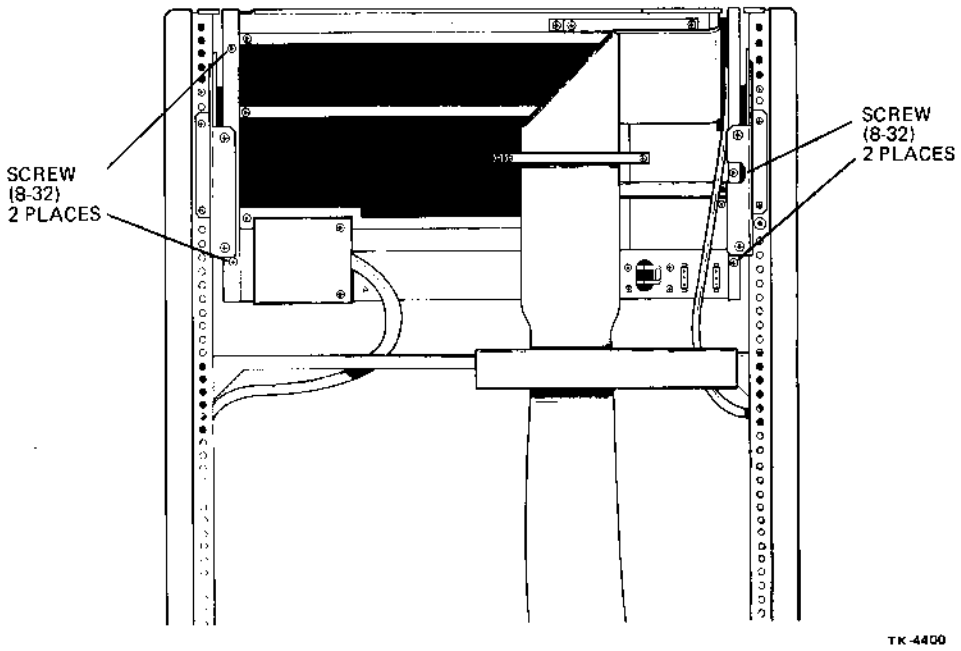


Figure 5-11 Power Supply Assembly, Rear Mounting Screws

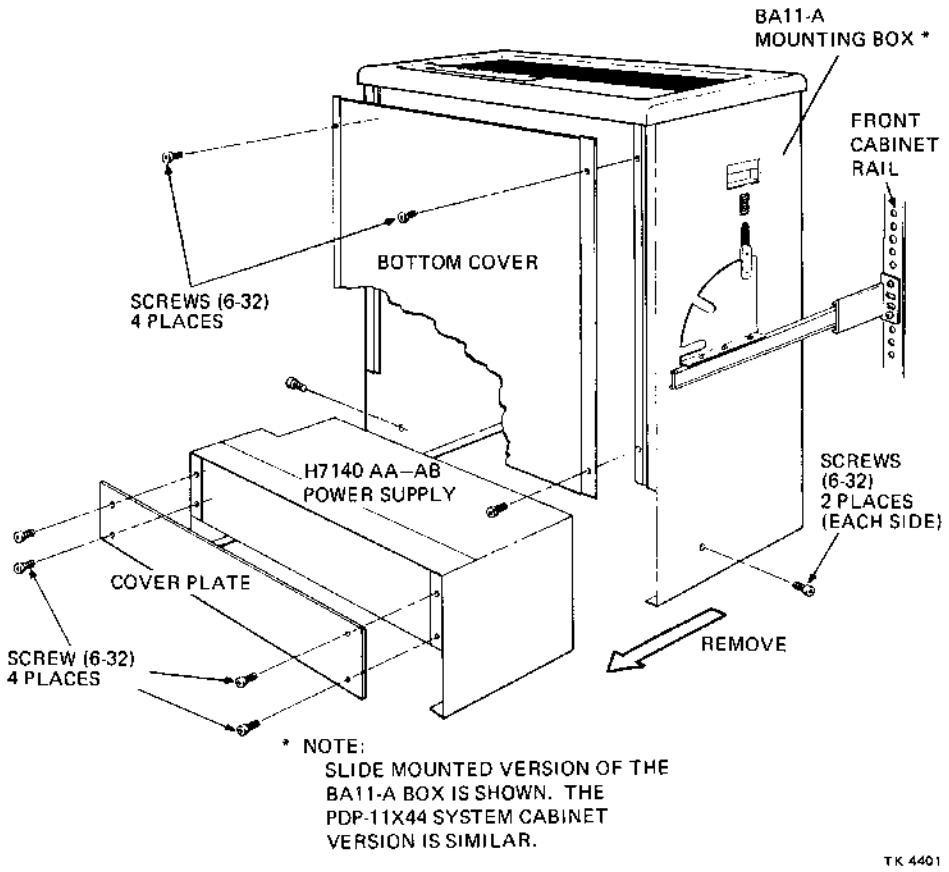


Figure 5-12 Power Supply Assembly Removal

13. In a slide mounted installation, remove and retain the 8-32 screws located on each side of the mounting box, toward the rear (Figure 5-12).

14. In a PDP-11X44 installation, remove and retain the 8-32 screws located on each side of the mounting box, toward the rear (Figure 5-7).

CAUTION
The H7140 power supply assembly will tend to slide forward when the screws in step 14 are removed.

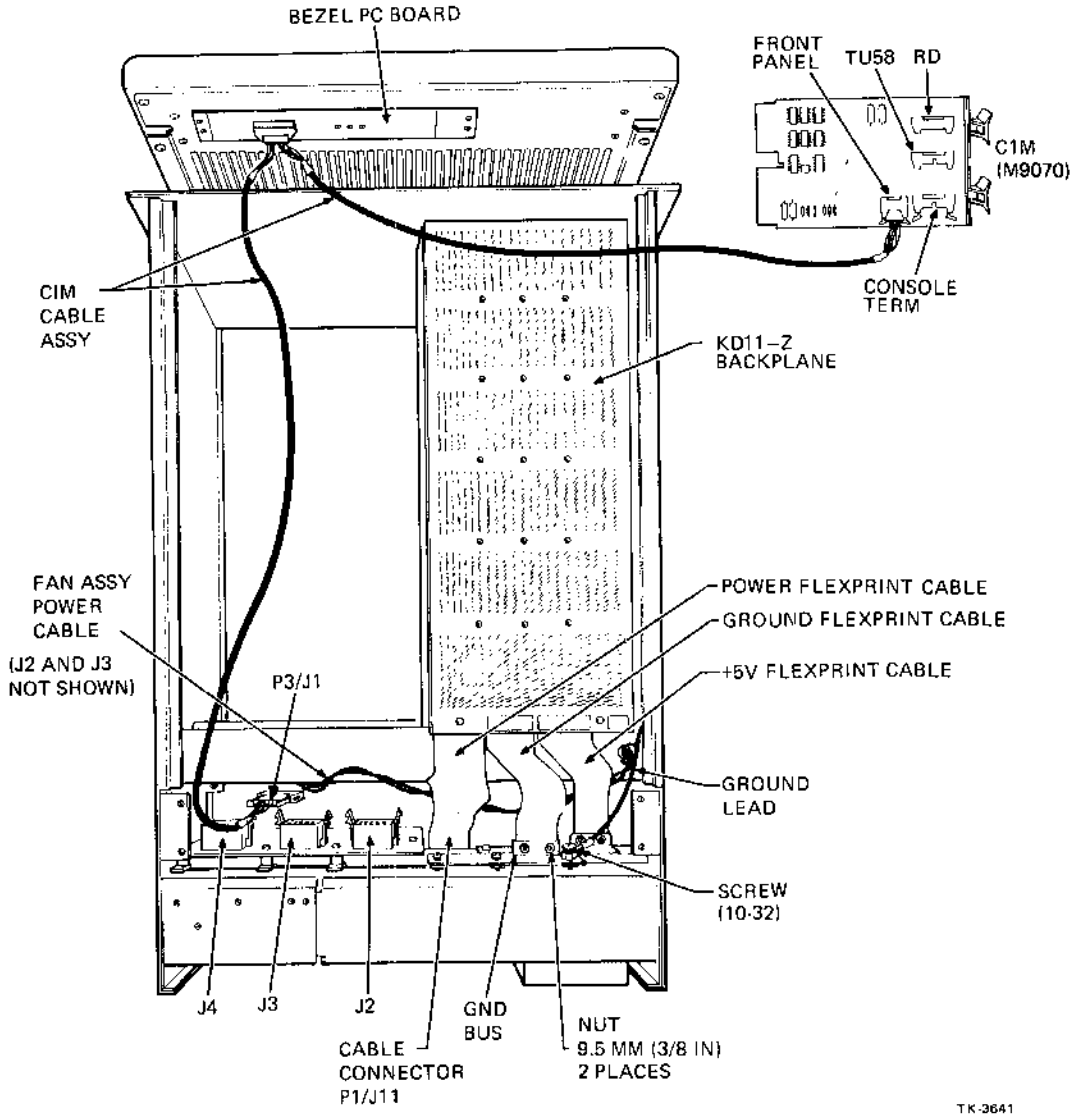


Figure 5-13 Power Lead Connections

15. Slide the power supply assembly forward approximately 5 cm (2 in) and disconnect the fan assembly power cable shown in Figure 5-13 from connectors J2 and J3 (not shown) on the power supply PC board.

16. Slide the power supply assembly from the mounting box (Figure 5-12) and away from the cabinet.

5.4.2 Power Supply Replacement

1. With the mounting box in the maintenance position, slide the power supply into the mounting box chassis.

NOTE

When the power supply assembly is being inserted, check that the I/O and bus cables are properly positioned and do not interfere with the power supply installation. Before the supply is fully inserted, connect the fan assembly power leads that were removed in step 15 of Paragraph 5.4.1.

2. Replace the 8-32 screws removed in step 13 or 14 of Paragraph 5.4.1.

3. Replace the backplane connectors removed in step 12 of Paragraph 5.4.1.

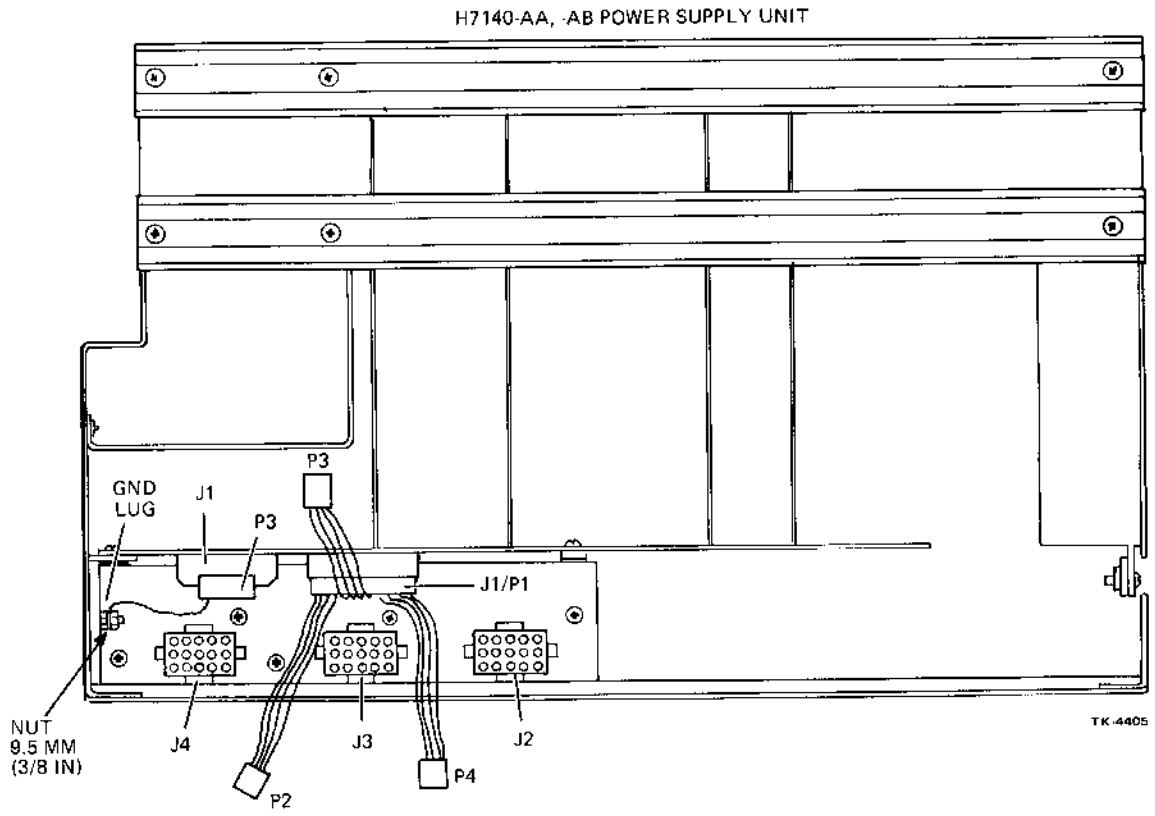


Figure 5-14 Power Distribution Panel and Connectors

4. Replace the ground lead removed in step 11 of Paragraph 5.4.1.

5. Replace connector P3 removed in step 10 of Paragraph 5.4.1.

6. Replace the power flex print cable connector removed in step 9 of Paragraph 5.4.1.

7. Replace the +5 V and ground flex print cables removed in steps 8, 7 and 6 of Paragraph 5.4.1.

8. Replace the ground lead removed in step 5 of Paragraph 5.4.1.

9. Replace the cover plate removed in step 4 of Paragraph 5.4.1.

10. Replace the bottom cover removed in step 3 of Paragaraph 5.4.1.

11a. In the PDP-11X44 system, release the safety lever and lower the mounting box and engage the latch.

11b. If the mounting box is installed on slides, release the slide hold levers on each side slide rail and slide the mounting box into the cabinet until the front latch engages.

12. From the rear of the cabinet, replace the four 8-32 screws removed in step 1 of Paragraph 5.4.1.

5.5 OPTIONAL BACKPLANE ASSEMBLIES

Two types of backplane assemblies are available for installation in the BA11-A mounting box. The DD11-CK backplane is a single system unit and the DD11-DK is a double system unit. The backplane assemblies are shown in Figure 5-15 and consist of module connector blocks that are mounted in a metal frame. The connector block pins are prewired for the PDP-11 bus signals and for the dc power and ground. Table 5-1 lists the slot columns and rows available in each backplane.

The backplane assemblies are installed within the mounting box in the area adjacent to the CPU backplane. The dc power is supplied to the backplane through a wire harness and connectors that mate with the power supply connectors. Table 5-2 lists the maximum number of each type of backplane which can be installed.

Table 5-1 Optional Backplane Assemblies

Designation	Type	Slot Columns	Rows	Modules
DD11-CK	Single	4	6	2 quad-height and 2 quad/hex-height
DD11-DK	Double	9	6	2 quad-height and 7 quad/hex-height

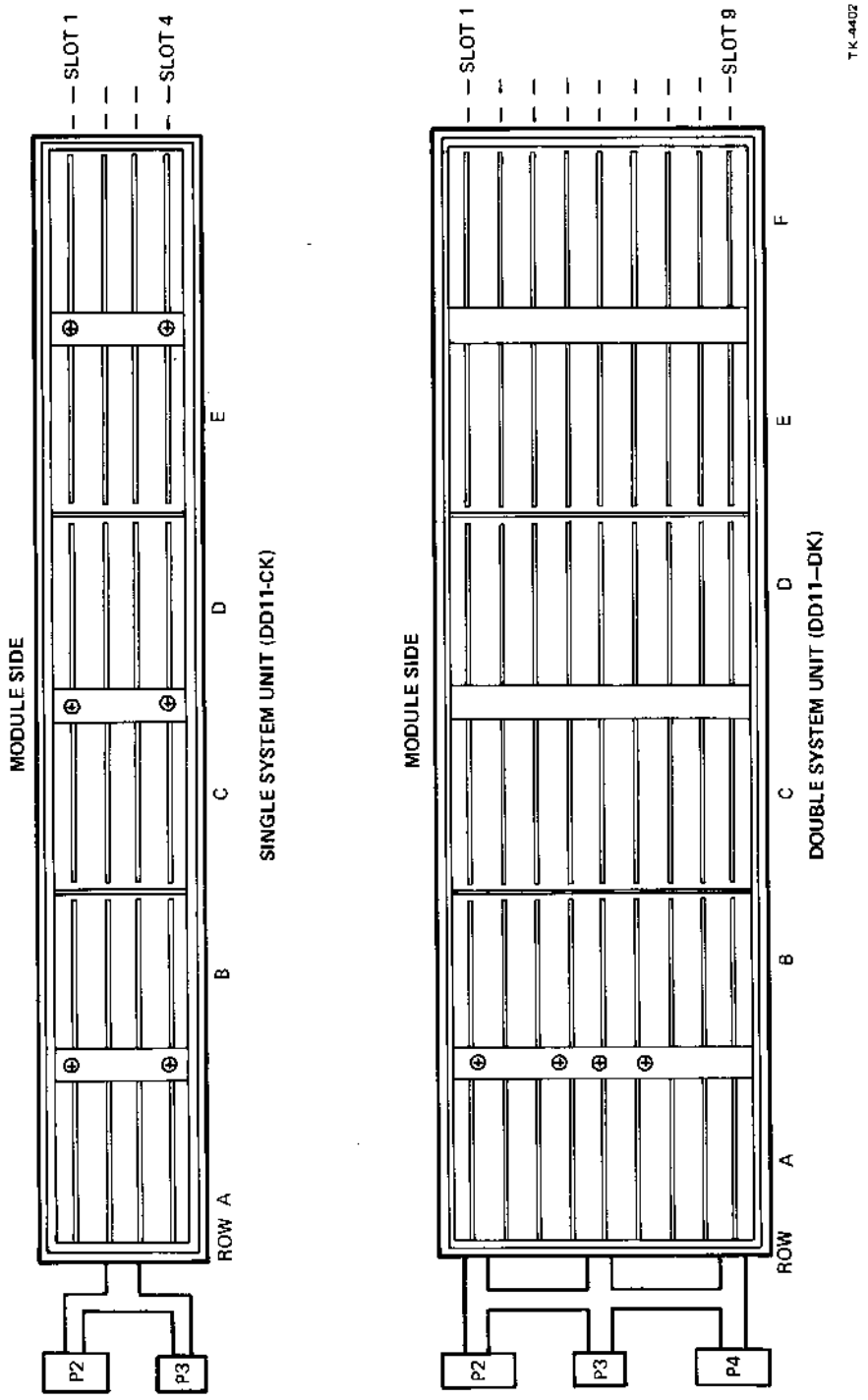


Figure 5-15 Optional Backplane Assemblies

Table 5-2 Backplane Assembly Types

Option Number	Total Slot Columns
One DD11-DK	9
One DD11-CK and One DD11-DK	13
Three DD11-CK	12

5.5.1 Optional Backplane Configurations

Figure 5-16 shows three configurations of the DD11-CK (4 slot) and DD11-DK (9 slot) backplanes installed in the mounting box.

5.5.2 Backplane Assembly Installation

To install the DD11-CK or DD11-DK backplane assembly, perform the following procedures.

1. In the PDP-11X44 system cabinet, perform steps 1 through 3 and steps 5 through 9 of Paragraph 5.1.1.

2a. If the mounting box is installed on slides, insert a screwdriver blade into the hole behind the slot which is located at the right side of the bezel (Figure 5-9).

2b. Pull the front of the box until the slide hold levers are engaged (Figure 4-13).

2c. Release the pawl retractors on each side of the mounting box and tilt the box 90° to the maintenance position.

3. Remove and retain the four 6-32 screws that secure the bottom cover to the mounting box (Figure 5-12). Remove cover.

4. Remove and retain the four 6-32 screws that secure the cover plate to the bottom of the power supply assembly. Remove the cover.

5. Position the backplane assembly on the mounting rails so that the tapped holes in the rails are aligned with the backplane mounting holes (Figure 5-17).

NOTE

The backplane harness includes a ground lead with a lug attached which must be installed under the mounting screw.

6. Install the four 8-32 screws that are supplied with the backplane assembly. Do not tighten the screws.

7. Lower the mounting box to its normal horizontal position and insert a hex-height module into the module guides that are aligned with the slot columns on each side of the backplane assembly (Figure 5-18).

NOTE

The backplane assembly can be shifted in position to enable the module connectors to be properly aligned with the module slots.

8. Raise the mounting box to the maintenance position and tighten the four 8-32 screws that were installed in step 6.

9. Install the backplane wiring harness connectors P2, P3 and P4 into the power distribution connectors J5, J4 and J6, respectively. For the DD11-CK backplane assembly, install connector P2 and P3 into connectors J5 and J4, respectively (Figure 5-14).

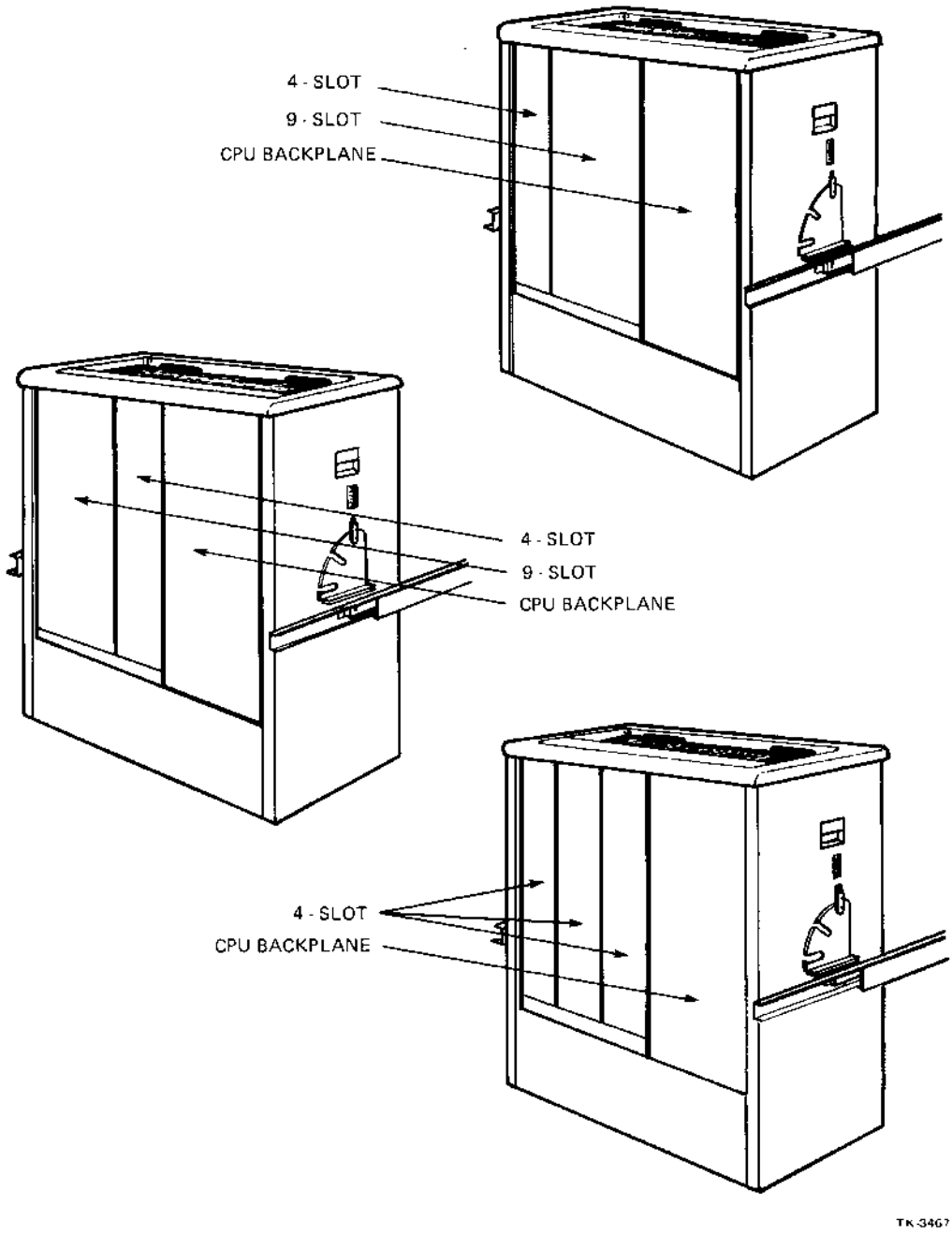


Figure 5-16 Optional Backplane Configurations

10. Replace the bottom cover and cover plate removed in steps 3 and 4.

11. Lower the mounting box to its normal operating position.

12. Remove the hex modules used for alignment in step 7.

13. Install the UNIBUS jumper module, SPC modules and UNIBUS terminator modules.

14. In the PDP-11X44 system cabinet, perform steps 15 and 16 of Paragraph 5.1.3.

15. In the PDP-11/44 slide mounted system, replace the top cover of the mounting box using the four 6-32 screws.

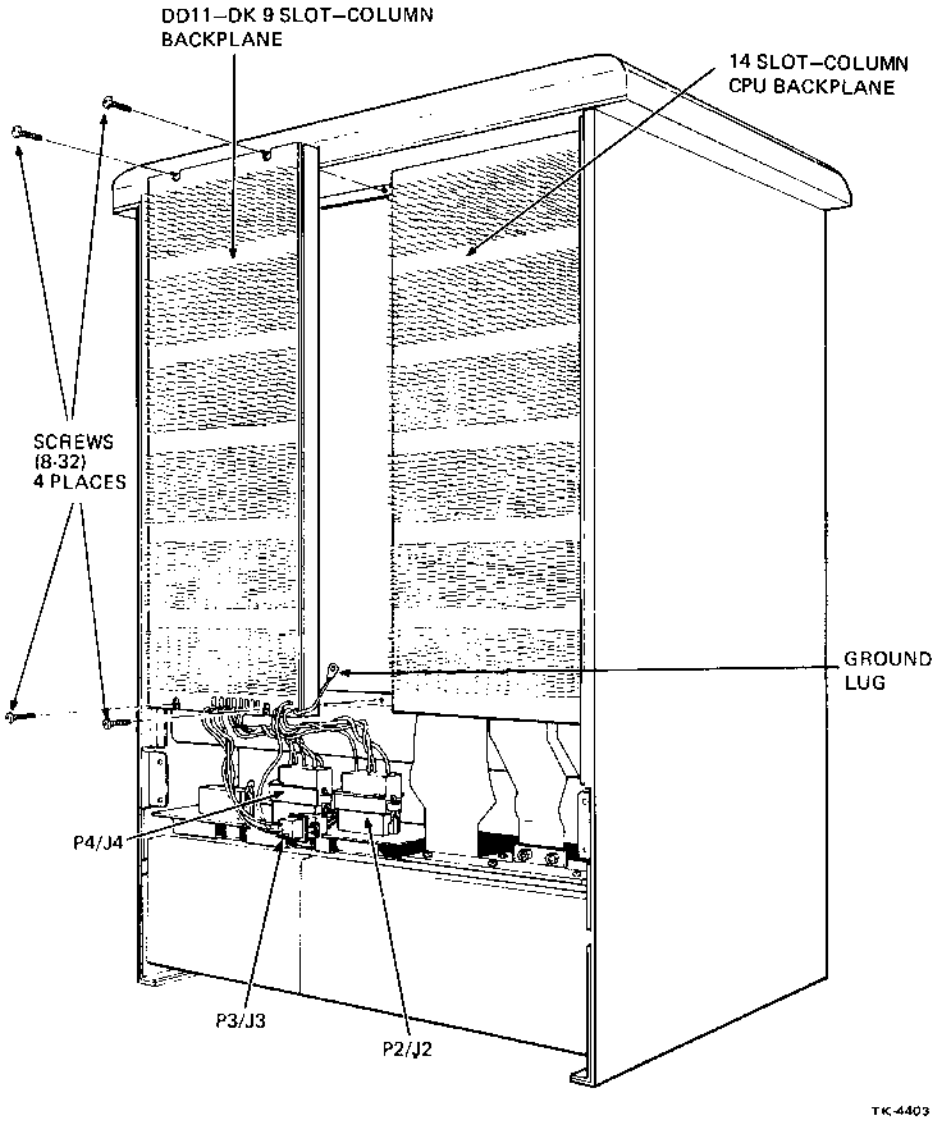


Figure 5-17 Backplane Assembly Mounting

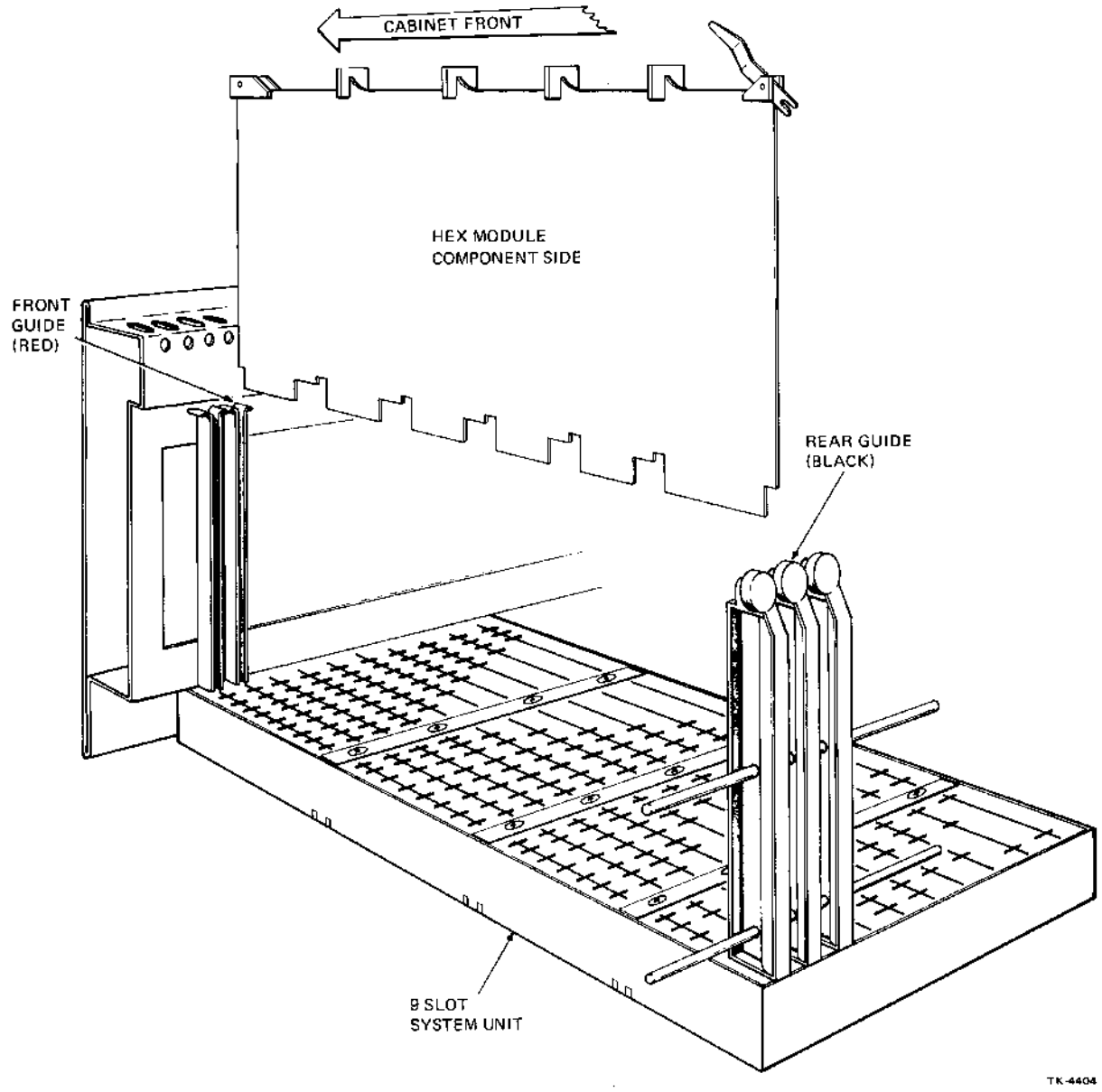


Figure 5-18 Backplane Assembly Alignment

5.5.3 Backplane Connector Assignments

The connectors in the backplane are classified into three categories: standard UNIBUS, modified UNIBUS, and small peripheral control (SPC) connectors. Particular areas of the backplane are reserved for the different types of connectors as shown in Figure 5-19.

The standard UNIBUS connectors contain all the UNIBUS connections. Sections A and B of slot 1 are the beginning of the UNIBUS in the DD1-CK and DD11-DK and should be occupied by the BC11-A UNIBUS cable since they are expander backplanes. Sections A and B of slot 9 in the DD11-DK or of slot 4 in the DD11-CK are the end of the UNIBUS on the backplane. These sections should be occupied by the BC11-A UNIBUS cable or a terminator module.

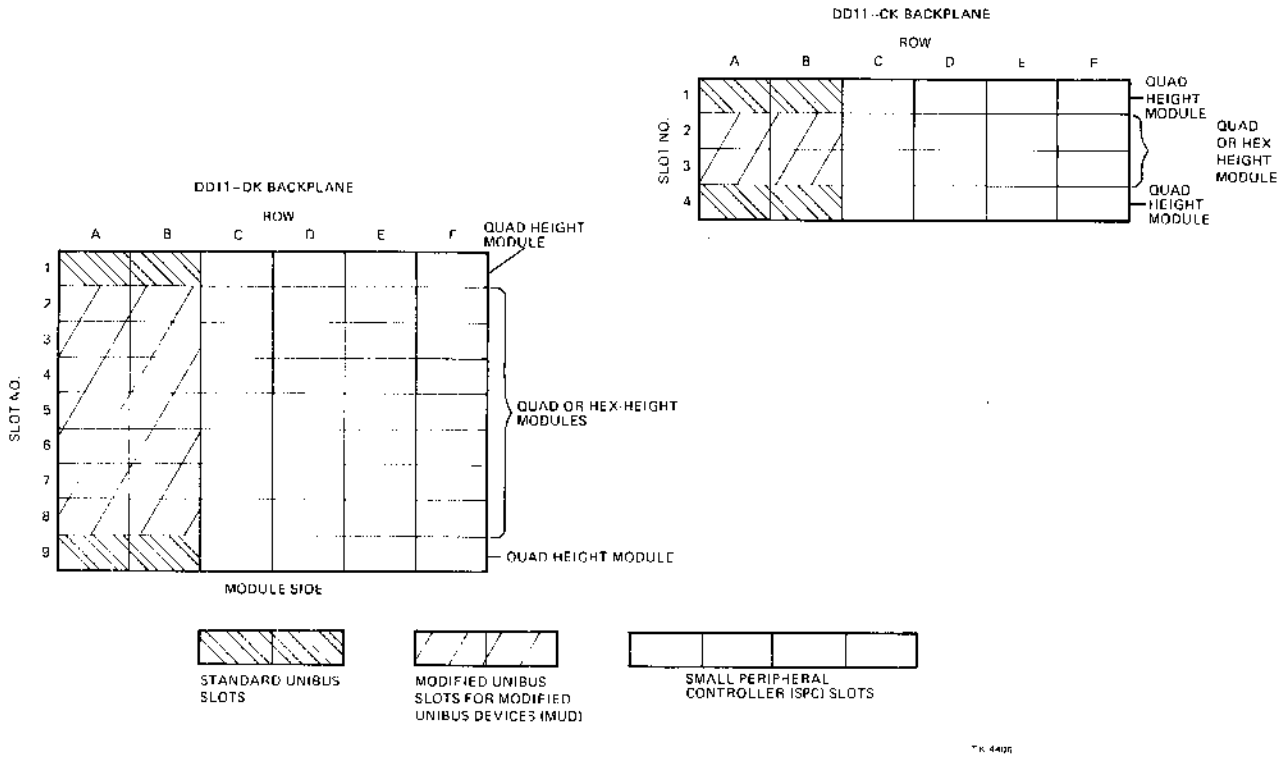


Figure 5-19 Optional Backplane Slot Assignments

5.5.4 NPG and BG Jumper Lead Routing

The NPG line is the UNIBUS grant line for devices that perform data transfers without processor intervention. Continuity of the NPG line is provided by wirewrap jumpers on the backplane. When an NPR device is placed in a slot, the corresponding jumper wire from pin CA1 to pin CB1 of that slot must be removed. The routing of the NPG signal through the backplane is shown in Figure 5-20. Grant priority decreases from slot 1 to slot 9 in the DD11-DK (slot 1 has the highest priority and slot 9 has the lowest).

NOTE

If an NPR device is removed from a slot, the jumper wire from CA1 to CB1 must be reconnected.

The bus grant lines (BG4:BG7) for devices requiring processor intervention during data transfers are routed through each small peripheral control section in slot D. Each of the four grant signals is routed on a separate line. Grant priority for each level decreases from slot 1 to slot 9.

NOTE

A bus grant jumper card (G727 G7270, or G7273) must be placed in connector D of any unoccupied SPC section. If an SPC section is left open, bus grant continuity will be lost.

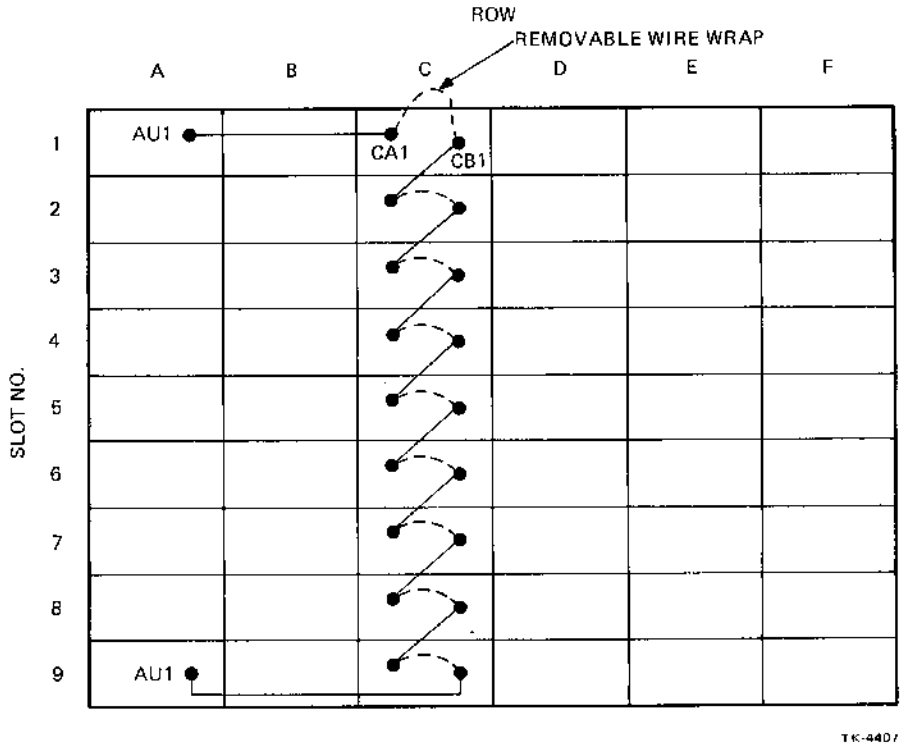


Figure 5-20 NPG Jumper Leads Routing

5.5.5 Standard and Modified Backplane Locations

Figure 5-21 shows the pin designations of the standard and modified UNIBUS connectors. The modified UNIBUS differs from the standard UNIBUS in that certain pins have been redesignated. Some ground connections, BUS GRANT signals, and the NPG signal have been removed from the modified UNIBUS and have been redesignated with core memory voltage pins, battery backup voltage pins for MOS memory, parity signal pins, several reserved pins, and test point pins.

Dual-height modules that are standard UNIBUS compatible must not be placed in the modified UNIBUS sections.

5.5.6 SPC Backplane Locations

The small peripheral control sections (C, D, E and F) collectively contain all the UNIBUS lines as well as power voltages (+5 V, +15 V, −15 V). These sections can be used by hex-height or quad-height modules containing the control logic for peripheral devices. Figure 5-22 shows the pin designations for the SPC connectors.

5.5.7 Backplane Power Connections

Power is supplied to the backplane via a wire harness that connects to the power distribution board with the power supply. The wires run from the backplane to a set of Mate-N-Lok connectors that run directly into the distribution board.

The power harness from the DD11-DK contains two large connectors (15-pin Mate-N-Lok) and one small connector (6-pin Mate-N-Lok). The DD11-CK backplane has only one 15-pin connector and one 6-pin connector. The connector pin locations are shown in Figure 5-23 and the signal assignments for each pin are listed in Table 5-3 (DD11-CK) and Table 5-4 (DD11-DK).

STANDARD UNIBUS PIN DESIGNATIONS

Side / Pin	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	BG6 H	+5V
B	INTR L	GND	BG5 H	GND
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	GND	BR4 L
E	D04 L	D03 L	GND	BG4 H
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	GND	PB L	A11 L	A10 L
P	GND	BBSY L	A13 L	A12 L
R	GND	SACK L	A15 L	A14 L
S	GND	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	NPG H	BR6 L	SSYN L	C0 L
V	BG7 SO	GND	MSYN L	GND

MODIFIED UNIBUS PIN DESIGNATIONS

SIDE / PIN	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	RESV PIN	+5V
B	INTR L	TP	RESV PIN	TP
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	+5 BAT	BR4 L
E	D04 L	D03 L	INT SSYN	PAR DET
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	PAR P1	PB L	A11 L	A10 L
P	PAR P0	BBSY L	A13 L	A12 L
R	+15 BAT	SACK L	A15 L	A14 L
S	-15 BAT	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	+20 (CORE)	BR6 L	SSYN L	C0 L
V	+20 (CORE)	+20 (CORE)	MSYN L	-5 (CORE)

NOTE: INDICATES A REDESIGNATED PIN.

TK-4409

Figure 5-21 Standard and Modified Backplane Pin Assignments

SIDE / PIN	ROW C		ROW D		ROW E		ROW F	
	1	2	1	2	1	2	1	2
A	NPG (IN)	+5V	TP	+5V	GND A	+5V	ABG OUT	+5V
B	NPG (OUT)	-15V	TP	-15V	ASSYN IN H	-15V	ABG IN	-15V
C	PA L	GND	A SEL 6	GND	A12 L	GND	SSYN L	GND
D	LTC	D15 L	A OUT LOW	BR7 L	A17 L	A15 L	BBSY L	FO1 N1
E	TP	D14 L	A SEL 4	BR6 L	MSYN L	A16 L	FO1 V2	D02 L
F	TP	D13 L	A SEL 0	BR5 L	A02 L	C1 L	D05 L	D06 L
H	D11 L	D12 L	A IN	BR4 L	A01 L	A00 L	D07 L	A INT ENB B
J	A INT B	D10 L	A SEL 2	A BR OUT	SSYN L	C0 L	NPR L	GND A
K	TP	D09 L	A OUT	BG7 SO	A14 L	A13 L	D08 L	A INT B
L	A INT ENBB	D08 L	INIT L	BG7 OUT	A11 L	TP	D03 L	FO1 L2
M	TP	D07 L	AINT ENBA	BG6 SO	AIN	AOUT HIGH	INTR L	FO1 M2
N	DC LO	D04 L	A INT A	BG6 OUT	A OUT LOW	A08 L	FO1 N1	D04 L
P	HALT REQ	D05 L	TP	BG5 S0	A10 L	A07 L	ABR OUT	FO1 P2
R	HALT GRT	D01 L	TP	BG5 OUT	A09 L	ASEL 4	FO1 L2	FO1 N1
S	PB L	D00 L	TP	BG4 S0	ASEL 6	ASEL 0	FO1 M2	FO1 P2
T	GND	D03 L	GND	BG4 OUT	GND	ASEL 2	GND	SACK L
U	+15/+8	D02 L	TP	ABG IN	A06 L	A04 L	A INT A	ABR OUT
V	AC LO	D06 L	ASSYN IN H	ABG OUT	A05 L	A03 L	A INT ENB A	FO1 FO1

TK-4410

Figure 5-22 SPC Backplane Pin Assignments

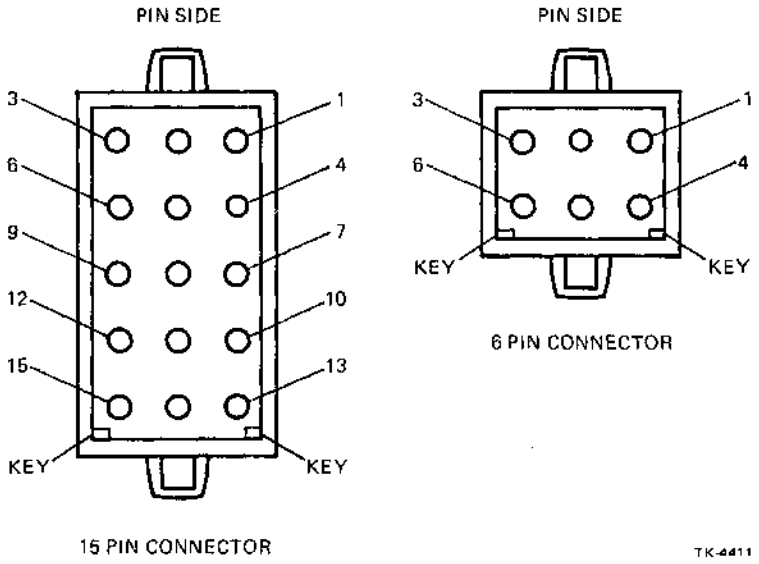


Figure 5-23 Backplane Power Connector Pin Designations

Table 5-3 Power Connector Signal Assignments for DD11-CK

Pin	Signal	Wire Gauge	Color
	15-Pin Mate-N-Lok Connector		
1	+5 V	14	Red
2	+15 V	18	Gray
3	+20 V	18	Orange
4	+5 V	14	Red
5	Spare (not connected)	–	–
6	+15 B	18	Green
7	Ground	14	Black
8	Ground	14	Black
9	Spare (not connected)	–	–
10	Spare (not connected)	–	–
11	Spare (not connected)	–	–
12	+5 B	14	Red
13	−15 V	18	Blue
14	−5 V	18	Brown
15	−15 B	18	White
	6-Pin Mate-N-Lok Connector		
1	LO GND	14	Black
2	LTC (line clock)	18	Brown
3	DC LO	18	Violet
4	AC LO	18	Yellow
5	Spare (not connected)	–	–
6	Spare (not connected)	–	–

Table 5-4 Power Connector Signal Assignments for DD11-DK

Pin	Signal	Wire Gauge	Color
	15-Pin Mate-N-Lok Connector 1		
1	+5 V	14	Red
2	+15 V	18	Gray
3	+20 V	14	Orange
4	+5 V	14	Red
5	Spare (not connected)	–	–
6	Spare (not connected)	–	–
7	Spare (not connected)	–	–
8	Ground	14	Black
9	Ground	14	Black
10	Spare (not connected)	–	–
11	Spare (not connected)	–	–
12	+5 B	14	Red
13	Spare (not connected)	–	–
14	−5 V	18	Brown
15	Spare (not connected)	–	–
	15-Pin Mate-N-Lok Connector 2		
1	+5 V	14	Red
2	Spare (not connected)	–	–
3	+20 V	14	Orange
4	+5 V	14	Red
5	Spare (not connected)	–	–
6	+15 B	18	White
7	Spare (not connected)	–	–
8	Ground	14	Black
9	Ground	14	Black
10	Spare (not connected)	–	–
11	Spare (not connected)	–	–
12	Spare (not connected)	–	–
13	−15 V	18	Blue
14	Spare (not connected)	–	–
15	−15 B	18	Green
	6-Pin Mate-N-Lok Connector		
1	LO GND	14	Black
2	LTC (line clock)	18	Brown
3	DC LO	18	Violet
4	AC LO	18	Yellow
5	Spare (not connected)	–	–
6	Spare (not connected)	–	–

CHAPTER 6
DETAILED FUNCTIONAL DESCRIPTION

6.1 INTRODUCTION
This chapter describes the major logic elements of the KD11-Z central processor used in the PDP-11/44. References to pages in the print set are made in the figures and text where applicable.

6.2 CONTROL STORE
Execution of each PDP-11 instruction requires the performance of a sequence of operations. The sequence is controlled by the microprogram contained in the PROM control store (K2-6,7,8,13). The KD11-Z control store provides storage for 1K of 56-bit microinstructions. Every microinstruction comprises 23 fields which control particular functions in the processor. Figure 6-1 illustrates the format of the KD11-Z microinstruction and the significance of each field value.

6.2.1 MicroPC Generation
The address of the current microinstruction (microPC) can be generated from a number of sources. Refer to Figure 6-2. The two major sources of the microPC lines (K2-6 MPC 10:00 H) are the central processor and the console processor. The signals from the central processor and console processor are wire ORed but only one group of signals is enabled at any particular time.

The console processor can generate a particular microPC by writing the address onto the PAX data bus and generating K3-2 MFM LOAD MPC L. This signal clocks the PAX data bits into a flip-flop and enables that data onto the MPC lines (K2-6 MPC 10:00H). In addition, the console processor can read the current microPC via the PAX data bus by generating K3-4 FORCE CPU MPC L.

Under normal conditions, the central processor generates the address of the microinstruction. The signal K3-2 MFM LOAD MPC L is false and the CPU MPC line drivers are enabled by the signal K2-9 ENAB CPU MPC L. The next address field (CS 00:10) of the current microinstruction will specify the microPC. Control store bits 00:10 generate MPC bits 10:00, respectively. However, several signals are wire ORed with the MPC lines to enable branching at specific points within the microprogram. Branches are enabled in the following situations.

Branch on Micro Test – The BUT ENABLE field of the microinstruction (CS 36:39) selects certain signals or groups of signals to be ORed with MPC bits 07:00. The microPC will be altered to reflect the status of those signal lines being tested.

Instruction Decode – The instruction decode logic generates signals which are wire ORed with MPC bits 07:00. When enabled, the instruction decode logic can cause branching within the microprogram. The microbranch address will depend on the instruction, mode, and operands specified.

Power Restart – Power restart will force the MPC lines to be cleared by an initialize signal (K2-11 PROC INIT H). The power up circuit (K2-2) will then enable MPC bit 00, forcing the processor to perform the power up routine beginning at microprogram address 001.

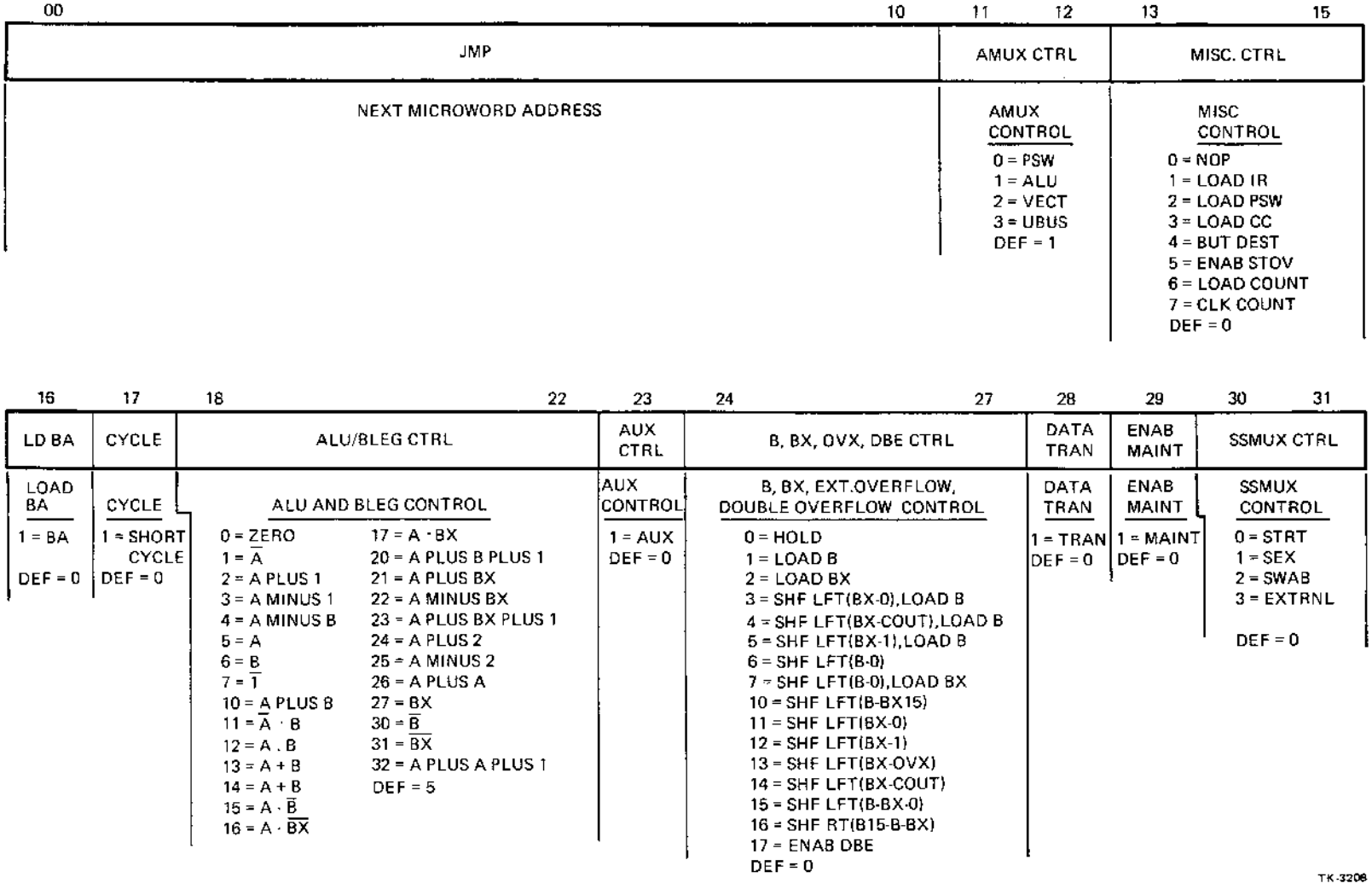


Figure 6-1 KD11-Z Microinstruction Format (Sheet 1 of 2)

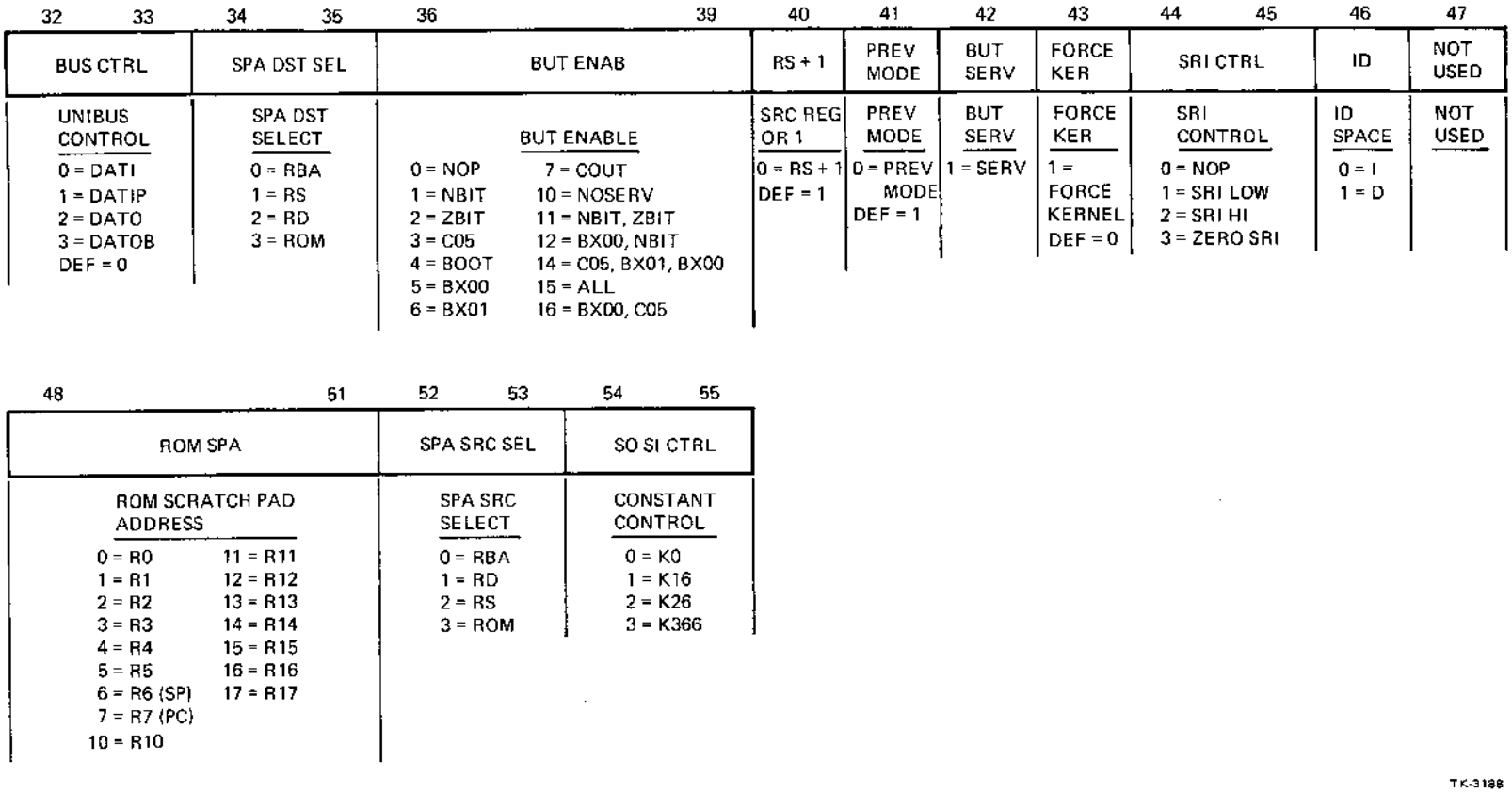


Figure 6-1 KD11-Z Microinstruction Format (Sheet 2 of 2)

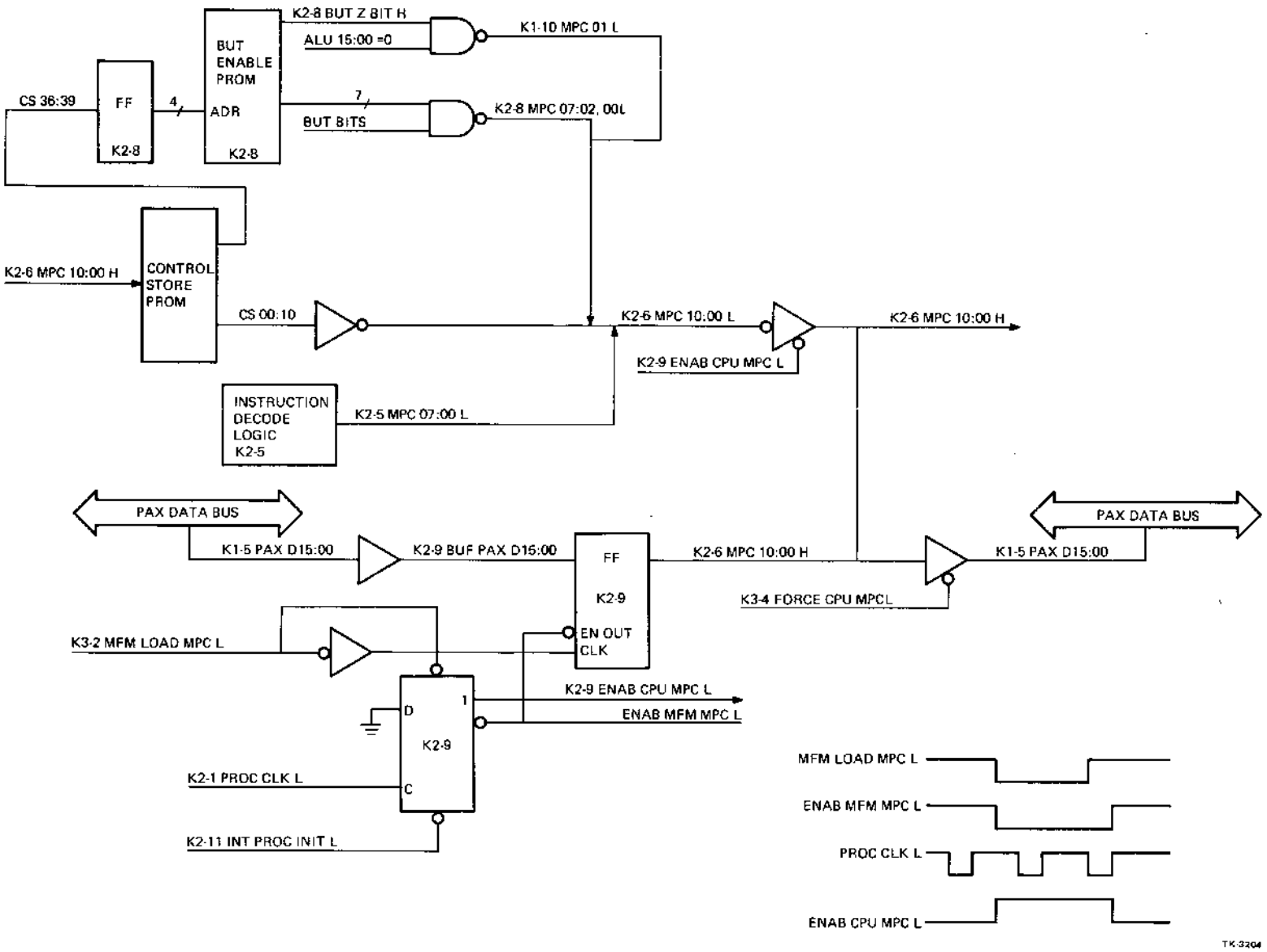


Figure 6-2 MicroPC Generation

Trap Decode – The processor enters the service microstate when CS bit 42 is enabled (K2-8 BUT SERVICE 1 (H) is generated). The service logic (K2-2) can then monitor various trap conditions and enable MPC bit 00. This causes a branch to a microroutine which initiates an error macroroutine. The error routine pushes and pops the PC and PSW on or off the processor stack.

6.3 DATA PATH

The data path (Figure 6-3) provides the logic required for arithmetic and logic processing (ALU), shifting of 8, 16, and 32-bit data formats (ALU B-leg logic), byte swapping and sign extention of data (SSMUX), storage of general register data (scratch pad memory), and storage of status information (processor status word). The following paragraphs describe each major element of the data path.

6.3.1 Arithmetic Logic Unit (ALU)

The ALU (Figure 6-4) is the main processing element of the data path. It performs arithmetic (with full carry look-ahead) or logic operations on 16-bit operands. The ALU is physically divided into four 4-bit slices (K1-1 through K1-4). Operations performed by the ALU are specified by the ALU/BLEG CTRL field (CS 18:22) of the current microinstruction or by the auxiliary control logic.

When bit 23 of the microinstruction equals 1, the signal K2-7 AUX CONTROL (1) H is generated and the auxiliary ALU control PROMs (K2-4) are enabled. The ALU operation will then be a direct function of the current PDP-11 instruction being executed. Refer to the auxiliary control description. If the auxiliary control bit (CS 23) is not set, the ALU function is defined explicitly by CS 18:22, as shown in Figure 6-1.

The data sources for the A input of the ALU are the scratch pad memory and KT multiplexer (KT MUX). These sources are wire ORed to generate the signals SP 15:00 (1) H. The internal address decode logic (K1-10) generates K1-10 ENAB KT MUX L which enables the KT MUX and disables the scratchpad memory. The KT MUX and scratchpad are thereby prevented from driving the SP lines at the same time. The data source for the B input of the ALU is the B-leg multiplexer (BMUX). The BMUX can select the BX register, B register, +1, or zero. Refer to paragraph 6.3.2.

The data outputs of the ALU (ALU 15:00 H) are input to one leg of the ALU multiplexer (AMUX) and the condition code logic (K1-10). The generate and propagate outputs of each ALU slice are input to the look ahead carry generator. This circuit enables the carry to be anticipated across the four ALU slices.

6.3.2 ALU B-Leg Logic

The B leg of the ALU (Figure 6-5) consists of three components: the B-leg multiplexer (BMUX), the B register (B REG) and the BX register (BX REG). Each of these components is divided into four 4-bit slices (K1-1 through K1-4).

The BMUX selects the data source for the B input of the ALU. The BMUX can select the B REG, BX REG, or the constants 1 and 0, depending on the value of the BMUX control lines, as follows.

K2-7 BLEG 01 H	K2-7 BLEG 00 H	BMUX OUTPUT (DP BLEG 15:00 H)
0	0	BREG 15:00 (1) H
0	1	BXREG 15:00 (1) H
1	0	0
1	1	DP BLEG 15:01 = 0, DP BLEG 00 =K2-3 PLUS ONE H

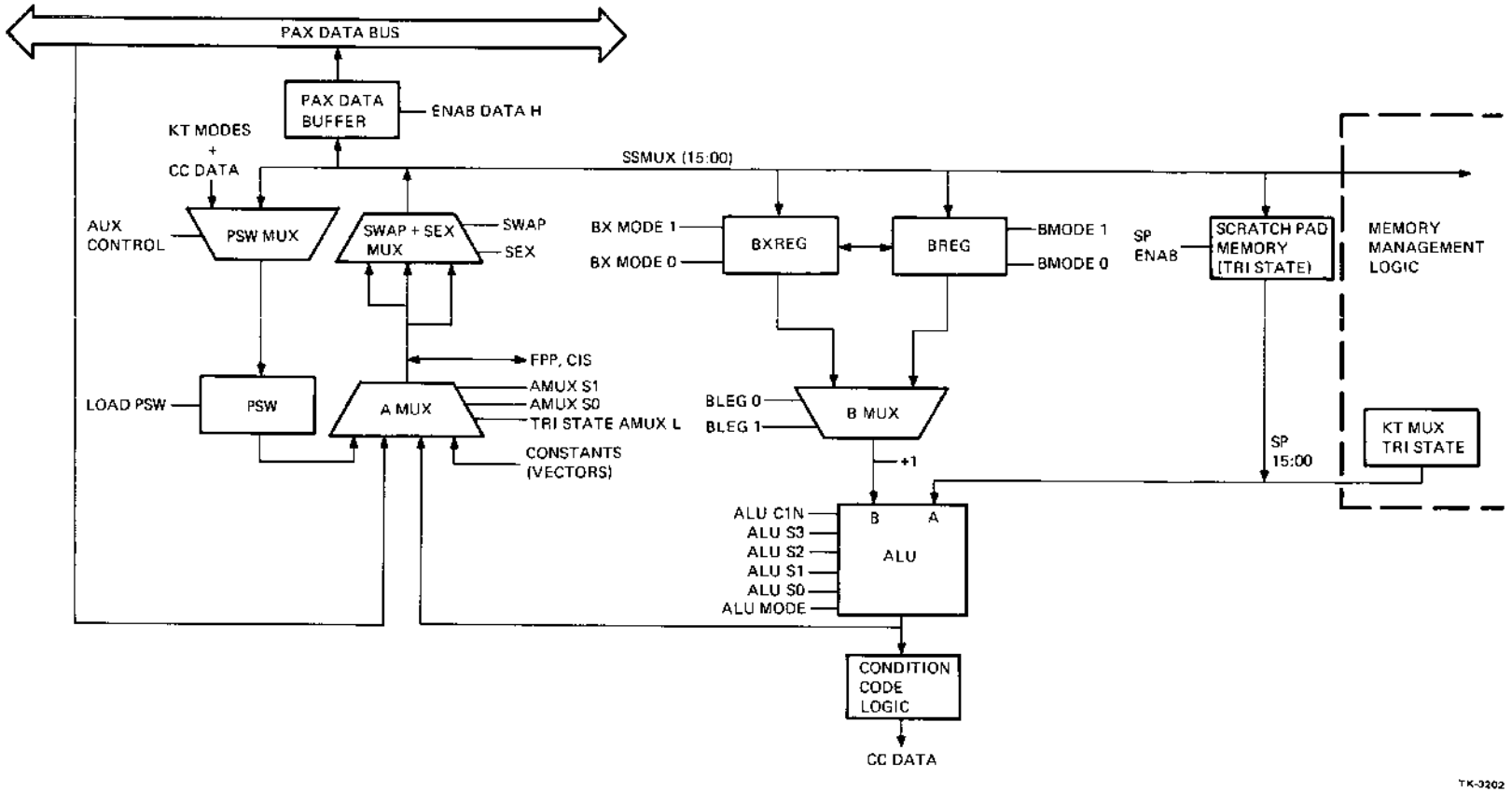


Figure 6-3 Data Path Block Diagram

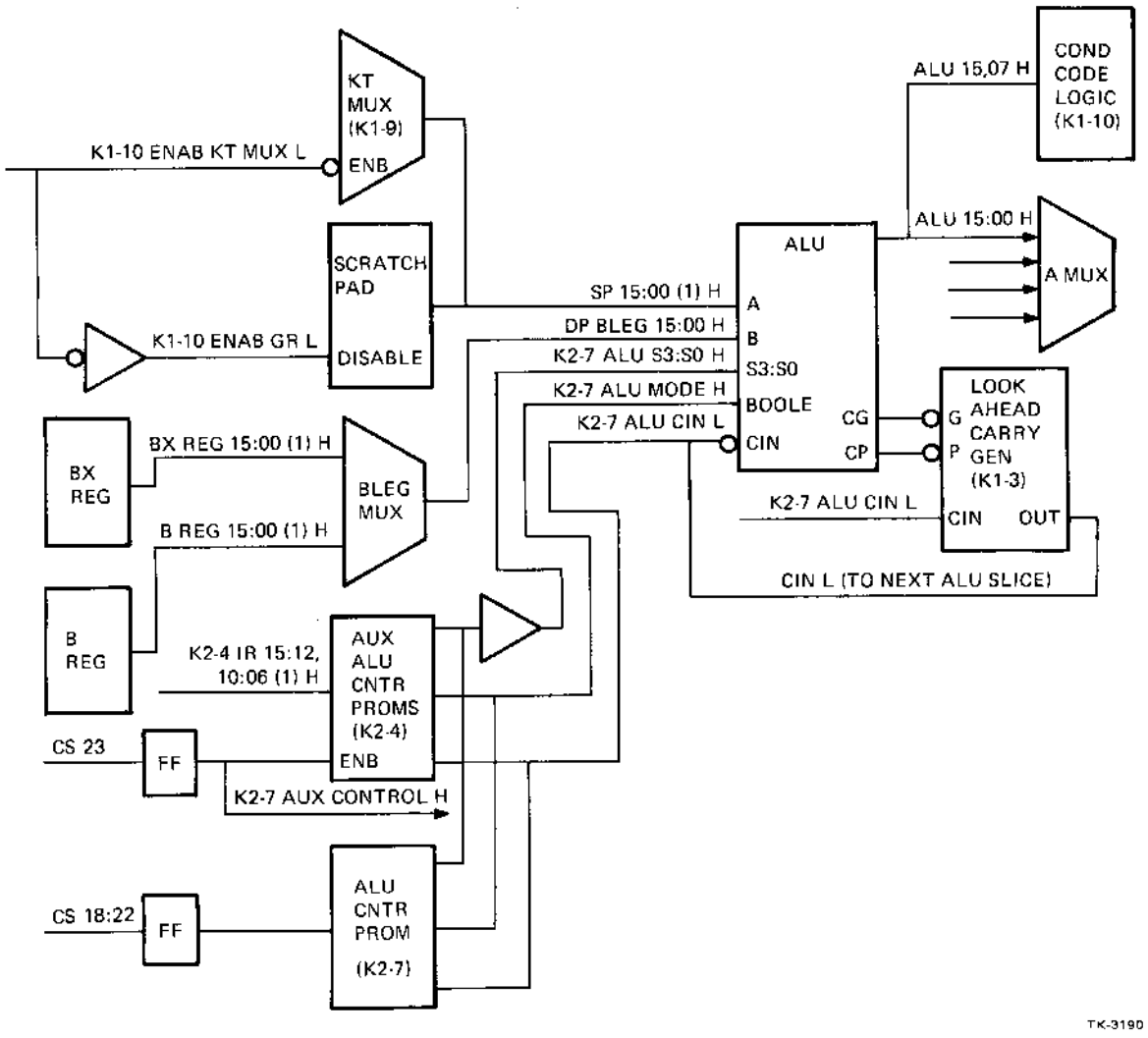


Figure 6-4 Arithmetic Logic Unit

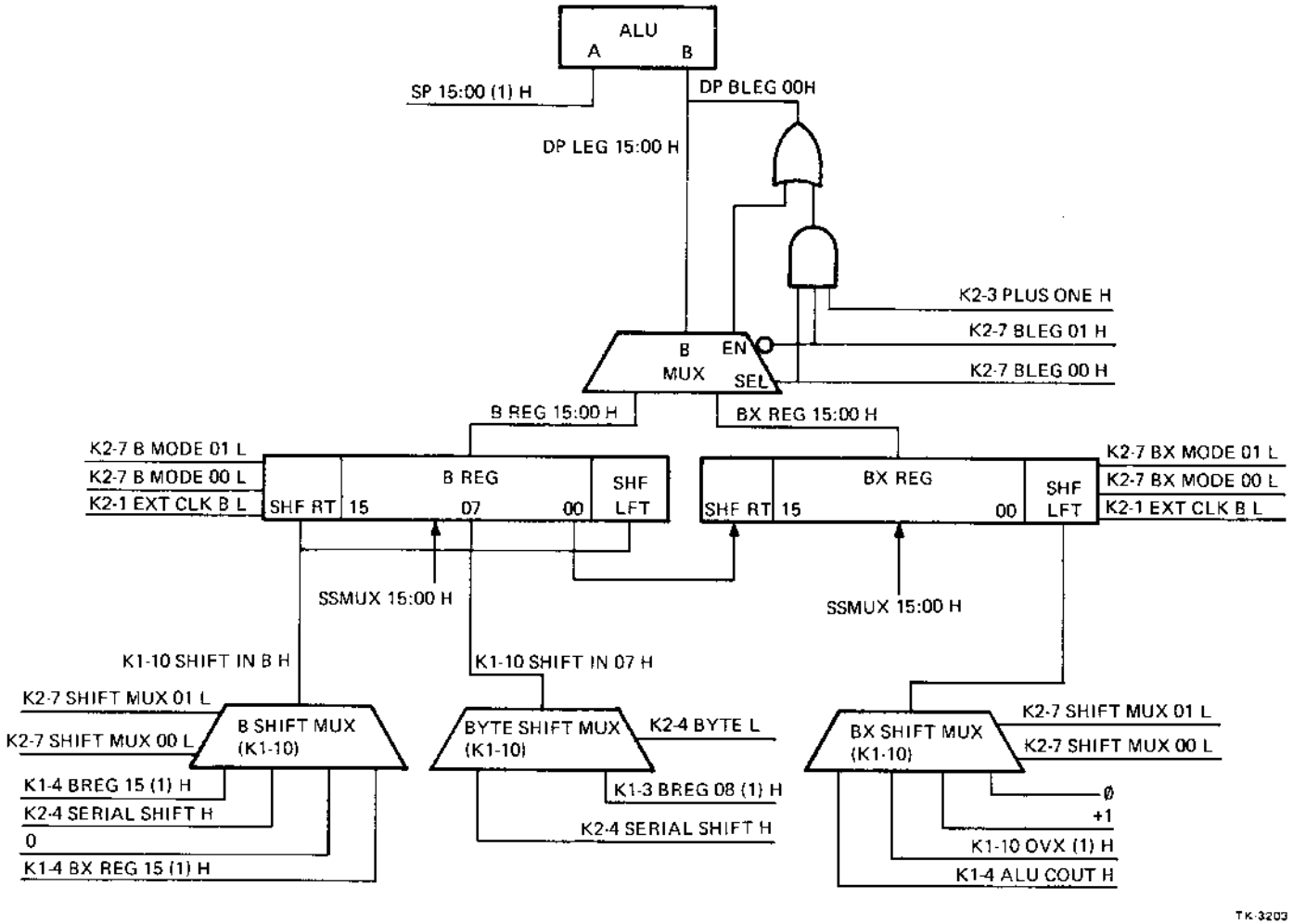


Figure 6-5 ALU B-Leg Logic

The constants 1 and 0 are generated during autoincrement and autodecrement operations. During either operation, if a word instruction is being performed, the specified register is incremented or decremented by two; if a byte operation is being performed, the register is incremented or decremented by one.

The ALU uses the signal K2-8 ALU CIN L to increment or decrement the A-leg input by one. The B-leg input must provide the constant 1 or 0 to obtain the correct autoincrement or autodecrement result. The constant 0 is generated by disabling the BMUX output. The constant 1 is generated by disabling the BMX output and ORing BMUX bit 0 with the signal K2-3 PLUS ONE H. This signal is true when the contents of the specified register are to be incremented or decremented by two.

The B REG and BX REG are 16-bit general purpose registers that can be shifted right or left by a single bit. Both registers can also be parallel loaded with data from the swap sign extend multiplexer (SSMUX). The BREG and BXREG have separate pairs of mode control lines (Figure 6-5) but they perform the same functions, as follows.

Mode 01	**Mode 00**		**Function**
L	L	Hold	Contents of register do not change.
L	H	Shift Right	Contents are shifted right one bit.
H	L	Shift Left	Contents are shifted left one bit.
H	H	Parallel Load	Data from SSMUX is loaded into the register and appears at its output.

Each register can be shifted as a 16-bit word or the registers can be combined and shifted as a 32-bit word. When the B REG and BX REG are used in conjunction, the B REG represents the upper 16 bits. The B REG can also be shifted as an 8-bit byte. The signal K1-10 SHIFT IN B H is fed into both serial shift inputs (SHF RT and SHF LFT) of the B REG. This signal is generated by the B SHIFT multiplexer. The B SHIFT MUX can select B REG bit 15, BX REG bit 15, 0, or K2-4 SERIAL SHIFT H as the serial input for either a right of left shift. To allow the byte shift function of the B REG, bit 07 of the B REG is loaded with the signal K1-10 SHIFT IN 07 H (generated by the BYTE SHIFT multiplexer). During a byte operation, the BYTE SHIFT MUX selects K2-4 SERIAL SHIFT H to be directly input into bit 07 of the B REG. During a word instruction, the signal K1-3 B REG 08 (1) H is input to bit 07.

As previously mentioned, the BX register can also be shifted to the right or left. During a shift right, the BX register contents are moved one place toward the least significant position and BX REG bit 15 is loaded with B REG bit 00. Thus, for all right shifts, the BX REG represents the low-order 16 bits of a 32-bit word. During a shift left, the register contents are shifted toward the most significant bit position and BX REG bit 00 is loaded with the signal K1-10 SHIFT IN BX H, generated by the BX SHIFT MUX. The BX SHIFT MUX can select K1-4 ALU COUT H, the output of the EIS overflow detection logic (K1-10 OUX (1) H), 1 or 0 as the serial input for a left shift.

The shift capabilities of the B register and BX register are used during the performance of a number of instructions. The following briefly describes the shifting requirements for the ASL, ASR, ROL, ROR, ASH, and ASHC instructions.

1. Arithmetic Shift Left (ASL) – Shifts all bits of the destination left one place. The low-order bit is loaded with a 0. The C bit of the status word is loaded from the high-order bit of the destination. ASL performs a signed multiplication of the destination by two, with overflow indication.

2. Arithmetic Shift Right (ASR) – Shifts all bits of the destination right one place. The high-order bit is duplicated. The C bit is loaded from the low-order bit of the destination. ASR performs signed division of the destination by two.

3. Rotate Left (ROL or ROLB, depending on whether a word or byte operation) – Rotates all bits of the destination left one place. The high-order bit is loaded into the C bit of the status word, and the previous contents of the C bit are loaded into the low-order bit of the destination.

4. Rotate Right (ROR or RORB) – Rotates all bits of the destination right one place. The low-order bit is loaded into the C bit, and the previous contents of the C bit are loaded into the high-order bit of the destination.

5. Arithmetic Shift (ASH) – Shifts the contents of the register right or left the number of times specified by the source operand. The shift count is taken as the low-order six bits of the source operand. This number ranges from −32 to +31. Negative is a right shift and positive is a left shift.

6. Arithmetic Shift Combined (ASHC) – Treats the contents of the register and register ORed with one (R+1) as one 32-bit word. R+1 (bits 15:00) and R (bits 31:16) are shifted right or left the number of times specified by the shift count. The shift count is taken as the low-order six bits of the source operand. This number ranges from −32 to +31. Negative is a right shift and positive is a left shift. When the register chosen is an odd number, the register and the register ORed with one are the same. In this case, the right shift becomes a rotate. The 16-bit word is rotated right the number of bits specified by the shift count.

NOTE

When R is an even-numbered register, R+1 will be the next highest register. If R is an odd-numbered register, R+1 will be the same register. For example, if R = R4, then R+1 = R5; if R = R5, then R+1 = R5.

Figure 6-6 illustrates the operations performed by the shift and rotate instruction.

6.3.3 ALU Multiplexer (AMUX)

The AMUX enables the selection of one of four sources as the input data for the SSMUX. The AMUX can select data which is external to the processor (K1-5 PAX D 15:00 H) or internal data from the ALU, PSW, or constants. The AMUX output can also be placed in a high impedance state. This allows data from the floating point processor or commercial instruction set processor to be input to the data path via the AMUX lines. The output enable lines of the AMUX are controlled by the console processor on the multifunction module. When the console processor generates K3-4 FORCE CPU DATA L, the AMUX output is enabled and one of the four AMUX sources can be input to the SSMUX. When the console processor generates K3-4 FREE BUS H, the signal TRI STATE AMUX L is asserted low and the AMUX outputs are placed in the high impedance state.

When the AMUX outputs are enabled, one of the following four inputs will be selected:

a. PAX data (K1-5 PAX D15:00)
b. Constant inputs (K2-2 C7:C1 H) used to generate vectors
c. ALU inputs (ALU 15:00 H)
d. Processor status word (PSW) inputs

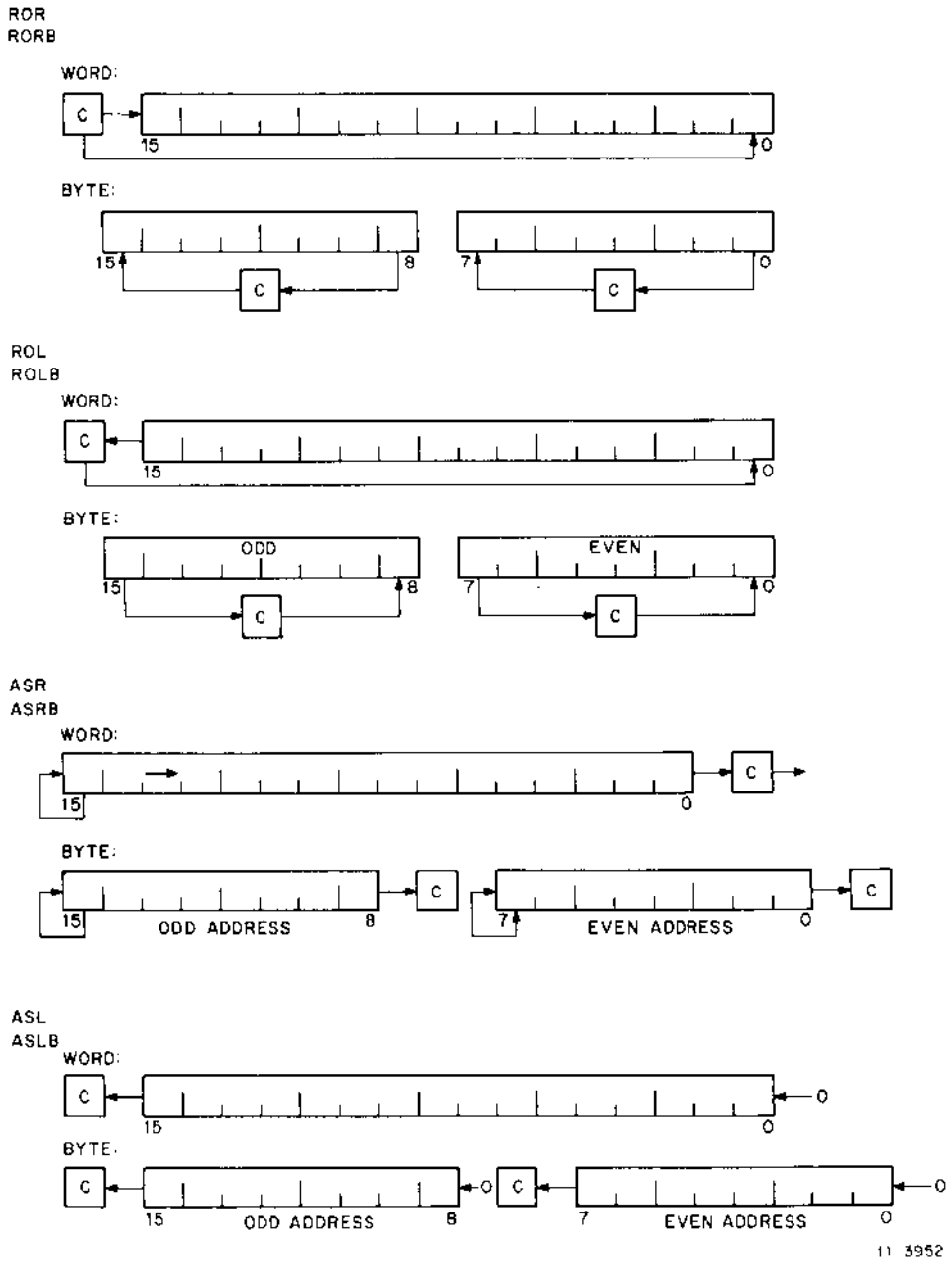


Figure 6-6 Rotate Instructions

6.3.4 Swap Sign Extend Multiplexer (SSMUX)

The SSMUX provides the capability of changing the format of the data before it is output from the data path or routed to another portion of the data path. The value of the two multiplexer select lines determine which of the following functions will be performed by the SSMUX.

K2-7 SWAP H	K2-7 SEX H	SSMUX Function
0	0	Data is passed through the SSMUX unchanged.
0	1	The sign bit of the low byte (K1-2 AMUX 07 H) is extended into the entire word.
1	0	The low and high bytes of the word are swapped.
1	1	The low and high bytes are swapped and then the sign bit of the new low byte (previously the high byte) is extended into the entire word.

The SSMUX input comes from the AMUX lines (AMUX 15:00). These signal lines can be generated by the AMUX or by the floating point or commercial instruction set (CIS) options. The output of the SSMUX goes to other sections of the data path (PSW, B leg, and scratchpad memory) and to the memory management system. The SSMUX output can also be routed to the rest of the computer system via the PAX data bus.

6.3.5 Scratchpad Memory

The scratchpad (Figure 6-7) consists of a 16-word by 16-bit random access memory. The scratchpad is divided into four 4-bit slices, shown on prints K1-1 through K1-4. The 16 scratchpad registers can be used for temporary storage or as general purpose registers specified during instruction execution. The following lists the scratchpad registers and their normal use.

Register Number	Description
R0	General Purpose Registers
R1	
R2	
R3	
R4	
R5	
R6	Kernel Mode Stack Pointer
R7	Program Counter
R8	Temporary Storage
R11	Unused
R12	Temporary Storage
R13	Temporary Storage
R14	Temporary Storage
R15	Temporary Storage
R16	Supervisor Mode Stack Pointer
R17	User Mode Stack Pointer

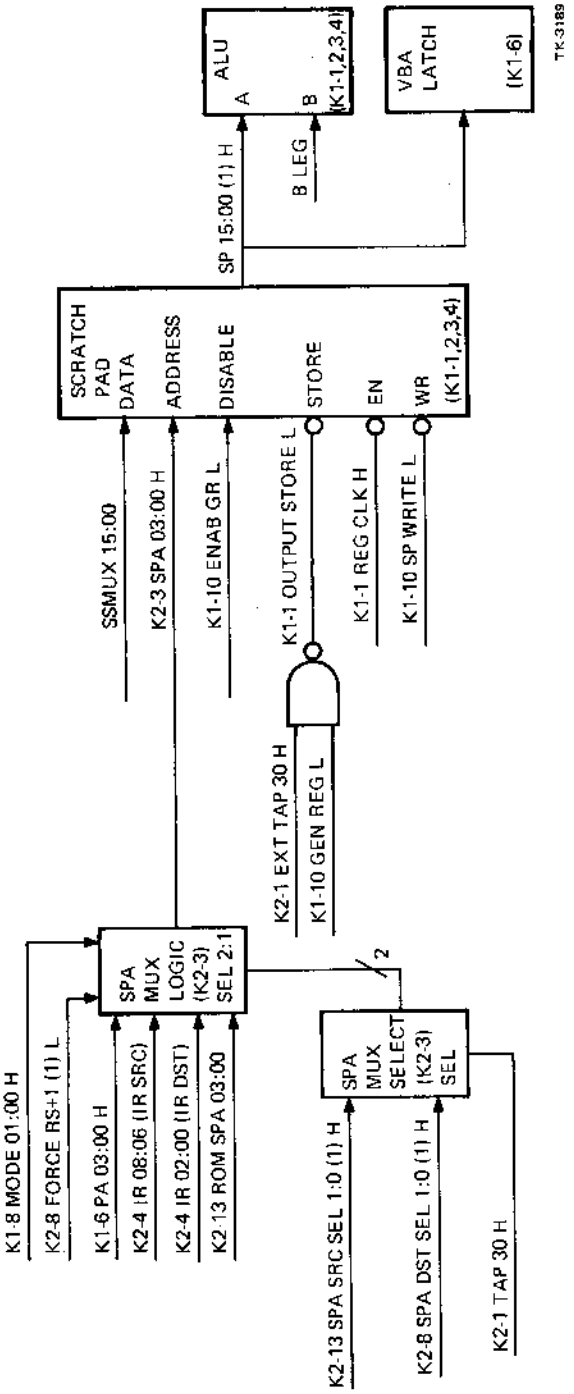


Figure 6-7 Scratchpad Logic

The scratchpad address (K2-3 SPA 03:00) is generated by the scratchpad address multiplexer (SPAM). The SPAM can select one of the following four address sources depending on the value of the multiplexer select lines;

Physical Address Bus (K1-6 PA 03:00 H)
Instruction Register Source Field (K2-4 IR 08:06)
Instruction Register Destination Field (K2-4 IR 02:00)
Control Store ROM SPA Field (K2-13 ROM SPA 03:00)

Note that scratchpad address R6 is forced to R16 when the memory management system is in user mode and the address is specified by the instruction register or the control store.

The select lines for the SPAM are also generated by a multiplexer. During the first half of the machine cycle, the signal K2-1 TAP 30 H is not asserted and the multiplexer selects K2-8 SPA SRC SEL 1:0 (1) H as the source for the SPAM select lines. During the second half of the machine cycle K2-8 SPA DST SEL 1:0 H is selected as the source. These two sources are generated by two fields of the micro-instruction: SPA SRC SEL (CS 52:53) and SPA DST SEL (CS 34:35).

6.3.5.1 Scratchpad Operation – The scratchpad registers can be read or written under program control, or the scratchpad memory can be disabled with its output placed in a high impedance state. Since the scratchpad output is wire ORed with the output of the KT MUX, the scratchpad must be disabled when the KT MUX is enabled. The output of the scratchpad (SP 15:00 (1) H) is fed into the A input of the ALU and the UBA latch. The following descriptions of the read and write operations assume the scratchpad memory is enabled (K1-10 ENAB GR L asserted low). Figure 6-8 shows the timing relationships of the read and write operations.

Read Operation – In a read operation, the scratchpad register is addressed during the first half of the machine cycle and the contents of the register are latched on the scratchpad output lines during the second half of the cycle. When the signal K2-1 EXT TAP 30 H goes low, the output store signal (K1-1 OUTPUT STORE L) goes high. This sets up the scratch pad for a read operation from the addressed register. When TAP 30 goes high and output store signal is enabled low, the contents of the addressed register are latched on the output of the scratchpad memory (SP 15:00 (1) H). The data can then be read for the remainder of the machine cycle. The outputs will not be affected by any modifications to the SPM address lines until TAP 30 goes low at the beginning of the next cycle.

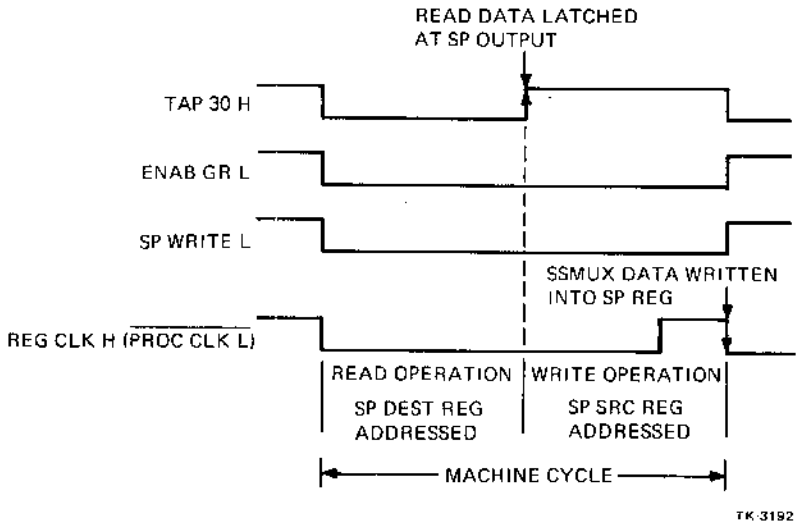


Figure 6-8 Scratchpad Timing

Write Operation – A write operation can occur during the second half of the machine cycle (TAP 30 H asserted high) if the write enable signal (K1-10 SP WRITE L) is asserted low. On the high to low transition of the clock signal (K1-1 REG CLK H), data from the SSMUX is loaded into the addressed scratchpad register. If the instruction is performing a byte operation, bits 15:08 of the scratchpad are not written.

6.3.6 Processor Status Word (PSW)

The processor status word is a 16-bit register (3 bits are unused) which contains the current and previous memory management modes, an indication of CIS instruction suspension, the current processor priority, a processor trap bit and the condition code results of the previous operation. The following lists the name and use of each PSW bit.

PSW Bit	Name	Use
15:14	Memory Management Current Mode	Contain the current memory management mode.
13:12	Memory Management Previous Mode	Contain the previous memory management mode.
11:09	Unused	
08	CIS Instruction Suspension	This bit, when set, indicates that a CIS instruction has been suspended by an interrupt and must be continued upon return from the interrupt. Setting this bit also inhibits a trace trap.
07:05	Priority	Set the processor priority.
04	Trace	When this bit is set, the processor traps to the trace vector. Used for program debugging.
03	N	Set when the result of the last data manipulation is negative.
02	Z	Set when the result of the last data manipulation is zero.
01	V	Set when the result of the last data manipulation produces an overflow.
00	C	Set when the result of the last data manipulation produces a carry from the most-significant bit.

The PSW is composed of flip-flops (Figure 6-9) which are all clocked by K2-1 EXT CLK B L, provided the proper control signal is enabled. The enabling signals are generated by the control store or the internal address decode PROM. All of the PSW bits can be loaded from the SSMUX. However, the previous memory management mode bits (13:12) and the condition code bits (03:00) can be loaded from alternative sources via the PSW multiplexer.

When the control store generates K2-8 FORCE KERNEL (1) H the PSWMUX selects PSW bits 15:14 as the source of the previous mode bits. When the force kernel line is not enabled, the PSWMUX selects SSMUX bits 13:12.

When the internal address decode logic generates K1-10 LOAD PSWL, the PSWMUX selects the SSMUX as the source for bits 03:00 of the PSW. The condition code bits (K1-10 CC N,Z,V,C) are loaded into the PSW only if the address decode does not generate the LOAD PSW line and the control store generates the auxiliary control signal (K2-7 AUX CONTROL L).

6.4 INSTRUCTION DECODE

The instruction decode circuitry consists of a set of PAX data buffers which pass the instruction to the instruction register where it is loaded on the rising edge of PROC CLK L (K2-4). From the instruction register, the information is passed to three programmable logic arrays (PLA) and several AUX control PROMS where it is decoded and used to generate the next microinstruction (MPC). The three PLAs handle the bulk of the instruction decoding while the AUX control is used when the instruction takes the form of Y ← X OP B or where the microcode does not contain enough information to properly execute the instruction.

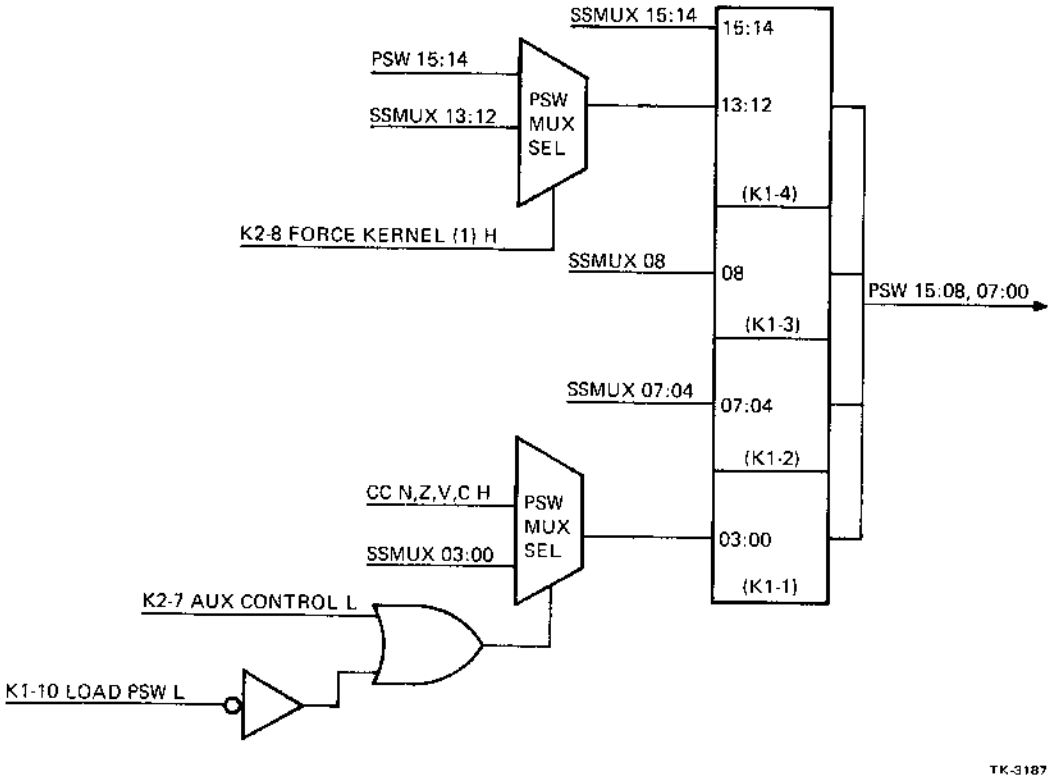


Figure 6-9 PSW Logic

The outputs of the instruction decode PLAs are wire ORed with the microprogram lines (MPC 07:00). These lines help create the address to the control store. After the control store has been addressed, the outputs of the control store are latched and routed to the other CPU modules where they control the operation of the ALU, BUS routing, scratch pad addressing and other base machine functions including the creation of the next MPC address.

The three PLAs used to decode the PDP-11 instruction set respond to several enabling conditions. Two of these enabling conditions are signals generated by the control store (K2-6). One signal is K2-4 IR DECODE (1) H. This signal indicates that the instruction register was loaded in the last microstate and the instruction is ready to be decoded. The other signal is K2-6 BUT DEST L, which is a microcode signal that indicates a branch on microtest. When this line is asserted and the instruction remains constant, it allows different microvectors to be asserted using the same instruction. This ability to keep the same instruction and change the microvector is very useful because it allows one set of micro routines to service several similar instructions without duplicating microcode. For example, a double operand instruction can be routed through a common fetch routine and, after the operands are fetched, each instruction can be executed by its own handler. Thus, MOV and ADD instructions may have some common microcode.

6.4.1 Instruction Classes

The instructions are loosely divided into three groups with each group being decoded by one PLA.

1. Double operand and branch instructions
2. Single operand instructions
3. Miscellaneous instructions (WAIT, HALT, etc.)

6.4.1.1 Double Operand and Branch Instructions – All branch instructions and most double operand instructions are decoded by one PLA (K2-5, E116).

Branch Instructions – A branch instruction, along with the status of the condition code bits K1-1 C, V, Z and N BIT (1) H, will enable the different branches used in the PDP-11 instruction set.

If the branch is true then a vector to microaddress 210 is executed. This vector will create a new PC for the branch. If the branch fails, the microprogram returns to instruction fetch. When a branch is decoded, signal K2-5 BRNSRV H is generated which creates a pseudo BUT NO SERVE condition. If a branch is false, this signal helps to decrease the time needed to execute the instruction by allowing the processor to skip the service state during an instruction fetch if no interrupt or trap is waiting to be serviced.

Floating-Point Instructions – If the FP11-F floating-point option is installed and input FP11-F ATTACHED L is asserted, all floating-point instructions will be forced to microaddress 50. If the floating-point option is not installed, a reserved instruction trap will occur (K2-5 IRCODE 00 L).

Double Operand Instructions – Inputs K2-4 08:15 (1) H, K2-6 BUT DEST L, IR DECODE (1) H, and destination mode (pin 20, E116) are used to decode double operand instructions. The outputs of the PLA are wire ORed to MPC 07:03 lines. K2-5 MOV L is asserted if a move instruction is decoded. Whenever it is desired to place the destination mode of the current instruction on the MPC lines, pin 10 of E116 (K2-5) is asserted, which through its associated logic places the destination mode on MPC line 02:00. PDP-11 instruction source and destination modes are usually brought out in this manner to cause a microbranch for every mode. The outputs for various double operand instructions are as follows.

Instruction Type	MPC 3	MPC 4	MPC 5	MPC 6	MPC 7
MOV (SMO:DMO)	0	0	0	0	1
DOP NON-MOD (SMO:DMO)	1	1	1	0	1
SUB (SMO:DMO)	0	0	1	0	1
MUL or DIV	0	1	0	0	1
ASH or ASHC	0	1	0	0	1
SOB	0	1	1	0	1
XOR	0	0	1	0	0

6.4.1.2 Single Operand Instructions – Most of the single operand and some double operand instructions are decoded on one PLA (K2-5, E115). The inputs and outputs of this PLA are similar to that of the double operand and branch decode PLA with one exception. K1-4 P.C. USER H is used to detect if the previous processor mode and the current processor mode in the PSW are both USER. When this condition is detected, K1-4 P.C. USER H is asserted and provides execute-only protection as acknowledged by the MFPI instruction. An MFPI instruction, which occurs when K1-4 P.C. USER H is asserted, will automatically relocate through D space, thus preventing unauthorized access to program code.

The output for various single operand instructions are as follows.

Instruction Type	MPC 3	MPC 4	MPC 5	MPC 6
SOP Modify	0	1	0	1
SOP Non-modify	0	1	1	1
NEG	1	0	1	1
Rotate/Shift	1	1	1	1
JSR	1	0	1	1
JMP	0	1	0	0
MARK	0	1	0	0
SWAB	1	1	0	0
MFPI (D)	0	0	0	1
MTPI (D)	1	0	0	1
*DOP MOD (SMO:DMO) (ADD, BIC, BIS)	0	0	1	1

*Double operand instruction.

6.4.1.3 Miscellaneous Instructions – Miscellaneous instructions such as HALT, WAIT, SET and CLEAR condition codes, along with trap and interrupt instructions, are decoded by this PLA (K2-5, E100). This PLA also generates most of the IR codes and K2-5 CPU HALT REQUEST H. The outputs generated by the various instructions are as follows.

Instruction	MPC 0	MPC 1	MPC 2	MPC 3
RESET	1	1	0	0
RTI/RTT	0	1	1	1
SET CC	1	1	1	0
CLR CC	0	1	1	0
RTS	0	0	1	0
WAIT	0	0	1	1
CSM (Call-to-supervisor mode)	1	1	1	1
HALT	K2-5 CPU HLT RQST L			

Instruction	IRC 00	IRC 01	IRC 02
HLT	0	0	0
JMP/JSR	0	1	0
EMT	1	0	1
TRAP	0	1	1
IOT	0	0	1
BPT	1	1	0
Reserved	1	0	0

Input K2-2 USER + SUPER H detects the absence of kernel mode for certain instructions. K2-10 EN CALL SUPER H allows the call to supervisor mode (CSM) instruction to be executed.

6.4.2 Miscellaneous Decoding for Reset Instruction and T Bit

PROM E88 K2-5 and associated gating are used to decode reset, return to interrupt (RTI) and return to interrupt no trace trap (RTT) instructions. When these instructions are decoded three possible signals are generated.

1. K2-5 DISABLE LOAD PRW H – This signal prevents the loading of the processor priority bits when the CPU is not in the kernel mode. It is generated during the RTI (T) instruction when the CPU is in the user or supervisor modes.

2. K2-5 ENAB T BIT H – This signal simply enables the T bit trap for RTI instructions when asserted and disables it for RTT instructions when not asserted.

3. K2-5 START RESET H – This signal will cause a UNIBUS INIT to be generated for 150 ms when a RESET instruction with the CPU in kernel mode is detected. A RESET in the user or supervisor mode is no-oped. When the CPU is not in a power clear mode, the UNIBUS INIT is performed by a one-shot (K2-11, E9).

6.4.3 ALU Auxilliary Control

The AUX control logic (K2-4) consists of a three PROMs (E68, E46, E43) which are used to determine the ALU operation to be performed when an instruction takes the form of X ← Y OP B. The Y designates a scratchpad register and the X designates either the B REG or a scratch pad register.

The AUX DOP PROM (E68) decodes double operand instructions, and is enabled when K2-7 AUX CONTROL (1) H is asserted and K2-4 IR 12-14 = 0 L is not asserted. The following table gives the output of the PROM as a function of the instruction being performed. (B represents the B register, A represents any scratchpad register, and F represents the ALU output.)

Instruction	ALU Function	Outputs D00	D01	D02	D03	D04	D05	D06	D07
MOV (B)	F=A	0	1	0	1	0	0	0	0
COMP (B)	F=A minus B	0	0	0	0	1	0	0	1
ADD	F=A plus B	0	0	1	0	0	1	1	0
SUB	F=A minus B	0	0	0	0	1	0	0	1
BIT (B)	F=A . B	0	0	0	1	0	0	1	0
BIC (B)	F=A . B	0	0	0	1	1	0	1	1
BIS (B)	F=A + B	0	0	0	1	1	0	0	0
XOR	F=A + B	0	0	0	1	1	0	0	1

The AUX SOP PROM (E46) decodes single operand instructions, and is enabled when K2-7 AUX CONTROL (1) H is asserted and K2-4 IR 12-14 = 0 H is asserted. The following table gives the outputs of the PROM as a function of the instruction being decoded.

Instruction	ALU Function	Outputs D07	D06	D05	D04	D03	D02	D01	D00
SWAB	F=A	0	1	0	1	0	0	0	0
CLR (B)	F=ZERO	0	1	0	1	0	0	1	1
COM (B)	F=A	0	1	0	1	1	1	1	1
INC (B)	F=A plus 1	0	1	0	0	1	1	1	1
DEC (B)	F=A minus 1	0	1	1	0	0	0	0	0
NEG B	F=A minus B	0	0	0	0	1	0	0	1
ADC (B)	*F=A plus C BIT (0)	0	1	0	1	0	0	0	0
	F=A plus C BIT (1)	0	1	0	0	1	1	1	1
SBC (B)	*F=A minus C BIT (0)	0	1	0	1	0	0	0	0
	F=A minus C BIT (1)	0	1	1	0	0	0	0	0
TST (B)	F=A	0	1	0	1	0	0	0	0
ROR (B)	F=B	0	0	0	1	1	0	1	0
ROL (B)	F=B	0	0	0	1	1	0	1	0
ASR (B)	F=B	0	0	0	1	1	0	1	0
ASL (B)	F=B	0	0	0	1	1	0	1	0
MARK	N/A	0	1	0	1	0	0	1	1
MFRI (D)	F=A	0	1	0	1	0	0	0	0
MTPI (D)	F=A	0	1	0	1	0	0	0	0
MFPS	F=A	0	1	0	1	0	0	0	0
MTBS	F=A	0	1	0	1	0	0	1	1
SXT	F=NBIT (0)	0	1	0	1	0	0	1	1
	F=NBIT (1)	0	1	0	1	1	1	0	0

Auxiliary control signals are also necessary for performing rotate and shift instructions. The ROTATE/SHIFT PROM (E43) decodes these instructions and generates the control signals necessary to shift the contents of the B REG. Inputs K1-1 B REG 00 (1) H, K1-10 CC N H, and K1-1 CBIT (1) H also determine the K2-4 SERIAL SHIFT H and K2-4 ROT C BIT H signals. The SERIAL SHIFT H signal is sent to the B SHIFT MUX where it is used in determining K1-10 SHIFT IN B H. SERIAL SHIFT is also sent to the BYTE SHIFT MUX where it is used in determining K1-10 SHIFT IN 07 H when just a byte of data is shifted. K2-4 ROT C BIT (1) H is used in the calculation of the new carry condition (condition code PROM K1-10, E42). Note that for all rotate and shift operations, the AUX control is performed on the B ← B step before each X ← Y OP B step previously mentioned. This is done to allow the condition codes to be set up without slowing the processor.

6.5 DATA TRANSFER LOGIC

6.5.1 UNIBUS Transfer Logic

All data transfers on the UNIBUS are controlled by the bus transfer logic on print K4-1. This logic monitors the status of the UNIBUS (Bus Busy), controls the bus control lines BBSY, MSYN, C0 and C1, and also detects parity errors, bus errors, memory management errors and odd address errors.

6.5.1.1 Processor Clock Inhibit – All processor data transfers on the UNIBUS are started by K2-7 BUF DATA TRAN (1) H. When a data transfer is started, it is necessary to stop the system clock. The clock is stopped by K2-1 EXT TAP 30 H, K4-1 ABORT RESTART L (not asserted), and E102 pin 12 (K4-1) being ANDed to create K4-1 TRAN INH L. K4-1 TRAN INH L then asserts K4-2 INH L which stops the clock.

6.5.1.2 UNIBUS Synchronization – The synchronization logic shown in Figure 6-10 determines whether the processor or some other device will control the UNIBUS. Flip-flop E116 (K4-1) and its associated logic determines whether or not the bus is in use. When BUS IN USE H is asserted at the set input of E116, the bus is in use. Each of the inputs on E122 and E100 that combine to create BUS IN USE H, monitors a specific set of bus conditions.

NPR (K4-2 NPR H)	A UNIBUS peripheral has asserted a nonprocessor request (NPR) and wishes to gain control of the bus immediately.
BBSY (K4-1 BBSY H)	Another UNIBUS device already has control of the bus and is asserting a bus busy (BBSY).
NPG (K4-2 NPG (1) H)	An NPR device has gained control of the UNIBUS and the processor has issued a nonprocessor request grant (NPG). The condition may exist where the NPR device has already recognized the NPG and has dropped its NPR signal, while not yet having asserted a SACK or BBSY.
NO SACK L (K4-2 NO SACK L)	A device has requested control of the UNIBUS. The processor has issued a grant, and the device has returned SACK L, causing NO SACK L to go high. The condition may exist where only SACK L remains on the UNIBUS for a period of time before the peripheral asserts BBSY.

TAKE BUS H (K2-9 TAKE BUS H)	Gives unconditional control of the UNIBUS to the MFM (console module).
DATIP (0) L (K4-1 DATIP (0) L)	When this input is true, all of the above signals are overridden. It indicates that the processor is performing a DATIP (read/modify/write) operation, and has control of the UNIBUS (BBSY asserted). NPR devices may, however, be granted control, but must wait until the processor releases BBSY before asserting theirs. (DATIP operations dictate worst-case bus latencies for NPR devices.) The DATIP flip-flop (E95) is clocked with the assertion of CPU MSYN (1) H during a DATIP cycle. It is cleared out by the following cycle which must be a DATO (B).

If none of the above bus-in-use conditions exist, the E116 flip-flop on K4-1 can be set when K4-1 GET BUS H is asserted. K4-1 GET BUS H is asserted by K2-7 BUF DATA TRAN (1) H and remains asserted until K4-1 GET BUS H goes low followed by the assertion of K2-1 EXT TAP 30 H. Setting E116 starts the data transfer.

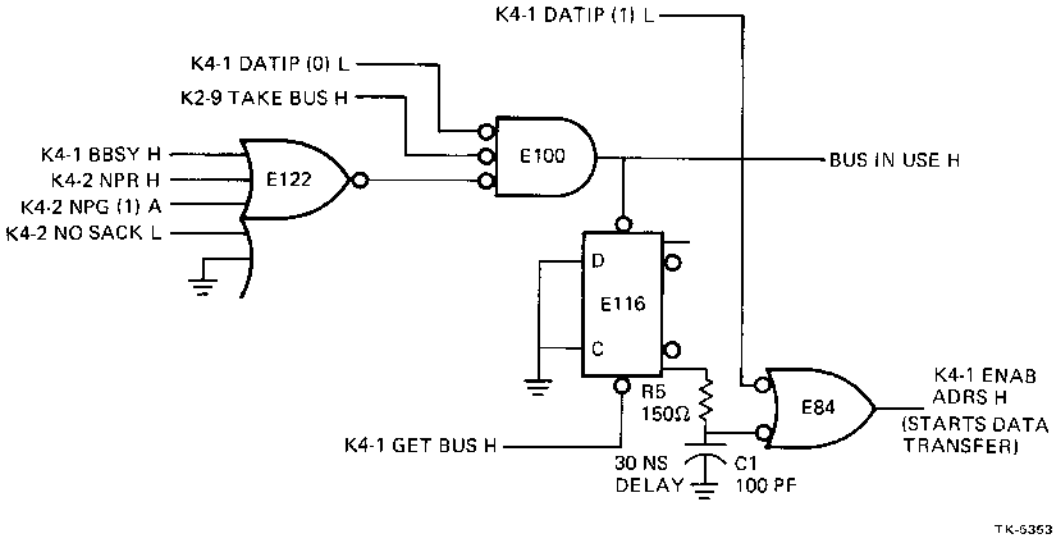


Figure 6-10 UNIBUS Synchronizer

6.5.1.3 Bus Control – When flip-flop E116 is set, the bus transfer circuitry begins a UNIBUS data transfer by asserting K4-1 ENAB ADRS H which begins the following actions.

1. Enables the bus address drivers
2. Enables bus busy driver (K4-1)

3. Enables the bus control signals BUS C0 and BUS CI, which determine the kind of transfer being performed

C1	C0	Operation
0	0	DATI
0	1	DATIP
1	0	DATO
1	1	DATOB

The actual condition of these control lines is determined by K2-8 BUF C0 (1) H and K2-8 BUF C1 (1) H.

4. Enables the bus data drivers if the operation being performed is a DATO.

K4-1 ENAB ADRS H is asserted 30 ns after E116 is set by K4-1 GET BUS H being asserted and BUS IN USE H being negated. The delay is created by R5 and C1. The PAX address is then passed to the UNIBUS or memory bus (EUB) as determined by flip-flop E81 (K4-3) and K1-11 UPPER 128K L. At this time, BUS BBSY L is also asserted.

6.5.1.4 Generation of MSYN and MSYN/SSYN Timeout – The logic in Figure 6-11 is used to generate MSYN and MSYN/SSYN timeout. The generation of MSYN begins with the assertion of K4-1 ENAB ADRS H. When this signal is asserted, it is sent down serial delay line E127 which generates K4-1 DLY ENAB H. There are two possible time delays inserted, depending on the type of instruction being executed. If the instruction is a standard PDP-11 instruction, the delay will be 40 ns. This delay allows the address lines to settle and gives the cache memory enough time to recognize the address on the PAX lines. The other delay, 160 ns, is used if the commercial instruction set (CIS) option is installed and a CIS instruction is being executed. This time delay is inserted to allow the address to be transfered through the additional logic associated with the CIS option.

When K4-1 DLY ENAB H is asserted, it is ANDed with K3-2 START TRN H, which is asserted 90 ns into the current cycle, and with the output of E102 pin 4, which is always high at the beginning of short cycles, to create K4-1 START TRAN L. K4-1 START TRAN L is then fed into serial delay E86 which is used to develop the timing necessary to complete the generation of CPU MSYN.

When K4-1 START TRAN L is asserted, the direct clear on CPU MSYN flip-flop (E95) is removed. K4-1 CACHE GATE H is asserted 45 ns after K4-1 START TRAN L is asserted. This signal, along with K1-11 UPPER 128K L, is used to determine if the address is a UNIBUS or memory bus (EUB) address. Approximately 90 ns after K4-1 START TRAN L is asserted, K4-1 STROBE CACHE H is asserted for approximately 15 ns. This signal strobes cache and if a cache hit is registered, CACHE RESTART L is asserted. CACHE RESTART L restarts the system clock and clears the CPU MSYN flip-flop (E95). This series of events cancels the remainder of the DATA TRAN cycle because a bus transfer is no longer needed. If a cache miss occurs, CACHE RESTART L is not asserted and CPU MSYN one-shot (E97) is armed. After the MSYN one-shot is armed, K4-1 CPU MSYN (1) H is asserted and fires the MSYN one-shot. The low going pulse of the MYSN one-shot readies the MSYN/SSYN timeout flip-flop (E115). If K4-3 SSYN H is not asserted by the time the MSYN one-shot times out, the MSYN/SSYN timeout flip-flop is set and K4-1 TO (1) H and K4-1 TO (1) L are asserted and signal a timeout. Normally, however, K4-3 SSYN H will be asserted and complete the transfer before the MSYN one-shot times out. During the next microcycle, START TRAN H will be negated and direct clear the MSYN one-shot.

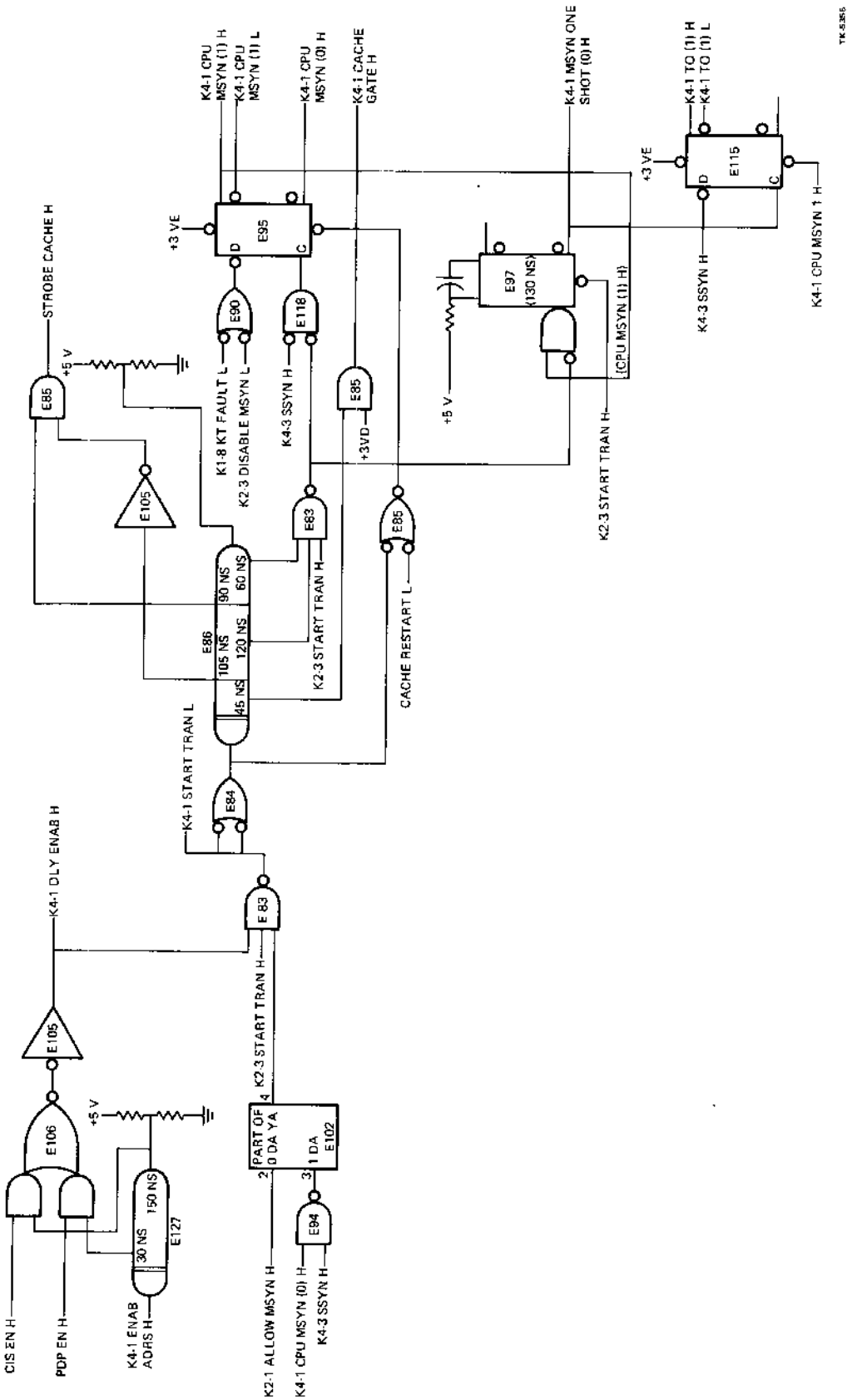


Figure 6-11 Generation of MSYN and MSYN/SSYN Timeout

When a DATI or DATIP operation is performed, it is necessary to delay the MSYN cycle (MSYN long cycle) to allow for the creation of the relocated physical address. This is done by selecting ALLOW MSYN H (E102) as one of the signals used to generate K4-1 START TRAN L. ALLOW MSYN H is delayed 90 ns before it is asserted, allowing enough time to create the relocated physical address.

6.5.1.5 Restarting Processor Clock – The processor clock can be restarted by the following conditions.

1. A cache HIT-CACHE RESTART L is asserted and restarts the clock.

2. An error condition exists. If an odd address, parity, timeout, or KT error has occured, ABORT RESTART L is asserted and negates K4-1 TRN INH L which negates K4-2 INH L and restarts the clock.

3. Completion of data transfer. The clock is restarted at the end of a data transfer cycle by clearing pin 12 of multiplexer E102, which negates K4-1 TRAN INH L, which negates K4-2 INH L, and restarts the clock.

On DATI and DATIP operations, when K4-3 SSYN H is asserted at E84 (K4-1 CPU MSYN (1) H is already asserted), the outgoing signal is deskewed (Figure 6-12) a nominal 75 ns to allow for worst-case bus transit and receiver times. The signal is deskewed 140 ns when a CIS instruction is in use. This is to allow for additional delay created by the CIS processor. Note that a parity error which asserts K4-1 PB H will not allow the clock to restart.

On DATO and DATOB cycles, it is not necessary to deskew the output of E84, therefore, it is passed directly to E102 to negate K4-1 TRAN INH L and start the clock.

6.5.2 Bus Arbitration

The PDP-11/44, like other PDP-11 processors, responds to bus requests (BRs) and nonprocessor requests (NPRs) issued by the different UNIBUS devices (CPU, peripheral devices). These requests have an established priority that determines which request is serviced next. The requests in descending order of priority are NPR, BR7, BR6, BR5, and BR4.

The bus arbitration logic of the PDP-11/44 recognizes a software controlled request, programmed interrupt request (PIRQ), which is initiated by the software to schedule certain tasks, such as, housekeeping functions. This request, along with the priority level of the processor, and the current highest BR level are arbitrated by the bus arbitration logic and use of the bus granted to one.

6.5.2.1 Bus Requests – Bus requests are handled by the logic on K4-2. The BRs are received and clocked into holding register E101 by the positive transition of EXT CLK C L. The output of the holding register is then passed to the arbitration PLA (E82) where it is compared with the processor priority level (PSW 07:05) and the PIRQ priority level (PIA 3:1). After the requests have been arbitrated by the PLA, one of three actions will take place.

1. No Action – This indicates the processor has the highest priority level.

2. Issue a PIRQ Grant – The PIRQ request has the highest priority level.

3. Issue a Bus Grant – The BR has the highest priority level and a BG at the same level is issued by asserting the proper input to E92 and BG + HLT H.

Because a BR can cause a program interrupt, it may be serviced only after the completion of the current instruction cycle.

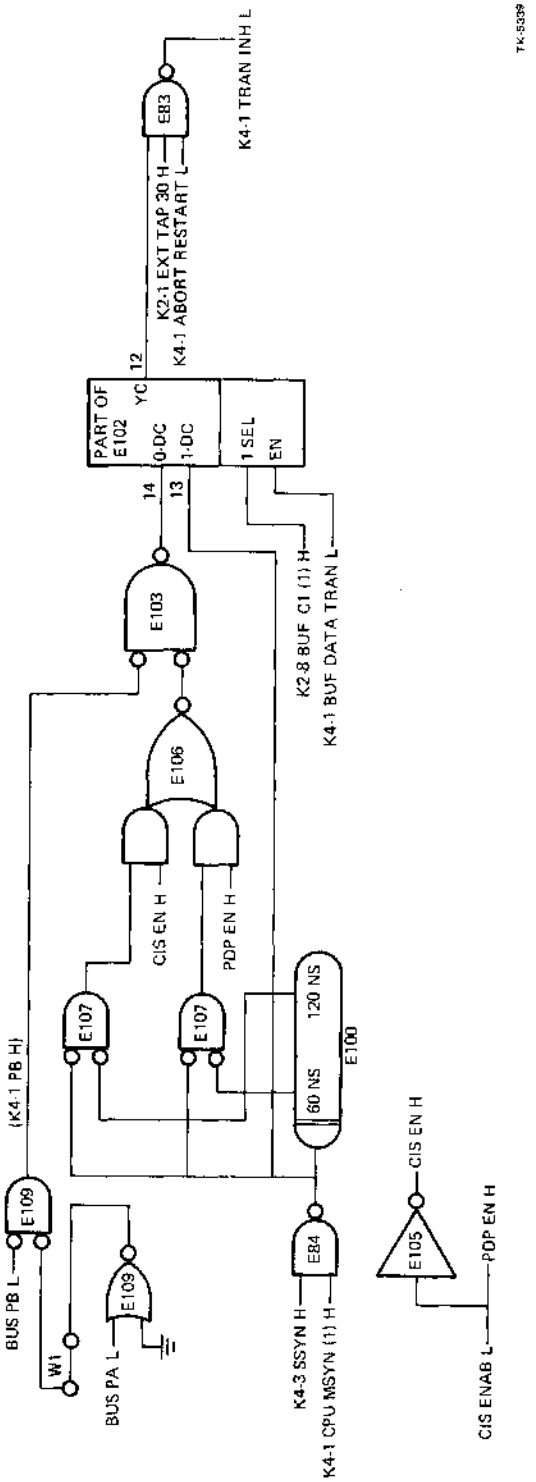


Figure 6-12 Deskew Logic

If no halt requests or traps are pending, then K2-2 ENAB GRANTS H is asserted and ANDed with BG + HLT II to halt the clock by causing K4-2 INH L to be asserted. This combined signal is also used to set the enable BG flip-flop (E113). The issuing of grants is controlled by the request synchronization logic.

6.5.2.2 Request Synchronization – The request synchronization logic of Figure 6-13 is used to determine whether a BG or a nonprocessor grant (NPG) is to be enabled.

Flip-flop E116 acts as the synchronizer between BRs and NPRs. During the service state of the microprogram, K2-8 BUT SERVICE (1) H is asserted. If there are no NPGs on the bus, K4-2 NPG (0) H is asserted, the console has not stopped the clock, and MFM CLK INH L is not asserted, then the output of E47 goes high. This allows E116 to be cleared if there are no NPRs present. If SACK is not asserted, then E124-8 goes high, clocks E113 and enables the proper BG. During the acceptance sequence, the clock is stopped.

The request synchronization logic allows an NPR to be granted use of the bus anytime the bus is not in an arbitration sequence; that is, BUS SACK L is not asserted, thus allowing any DMA traffic to be processed at this time. When BUS NPR L is asserted, E116 will be set if a competing BG has not already cleared the flip-flop. If SACK is not asserted, E124-11 goes high and clocks E113 which causes BUS NPG H to be asserted. While NPG is asserted, no further bus grants are honored.

6.5.2.3 SACK Timeout – The SACK timeout logic of Figure 6-14 is used to determine if SACK has been generated by the device receiving either the BG or NPG.

The generation of BUS SACK L from the device requesting use of the bus direct clears both halves of E113 (K4-2). E113 pin 6 goes high, and clocks SACK return flip-flop E114 which stops the system clock and clears request latch E101. When BUS SACK L is negated, K4-2 NO SACK L is asserted and clears the SACK return flip-flop E114 which restarts the system clock and allows a new arbitration for the bus.

The SACK timeout circuitry consists of one-shot E97 and its associated logic. One-shot E97 monitors the BG and NPG lines. If BUS SACK L is not asserted in 20 μs to acknowledge the grant, one-shot E97 times out and clears the grant itself. This is done either to avoid hanging the processor on nonexistent devices or when the BR is removed by the interrupting device before the grant could be accepted.

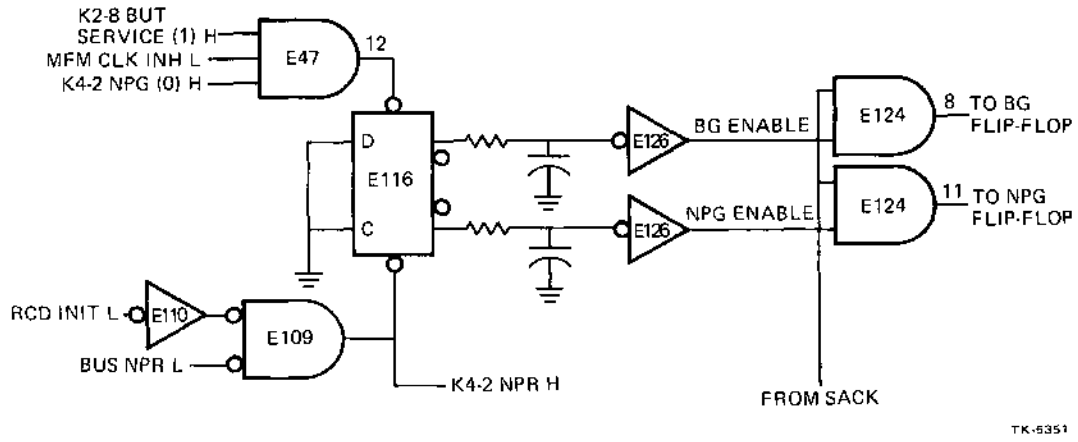


Figure 6-13 Request Synchronization

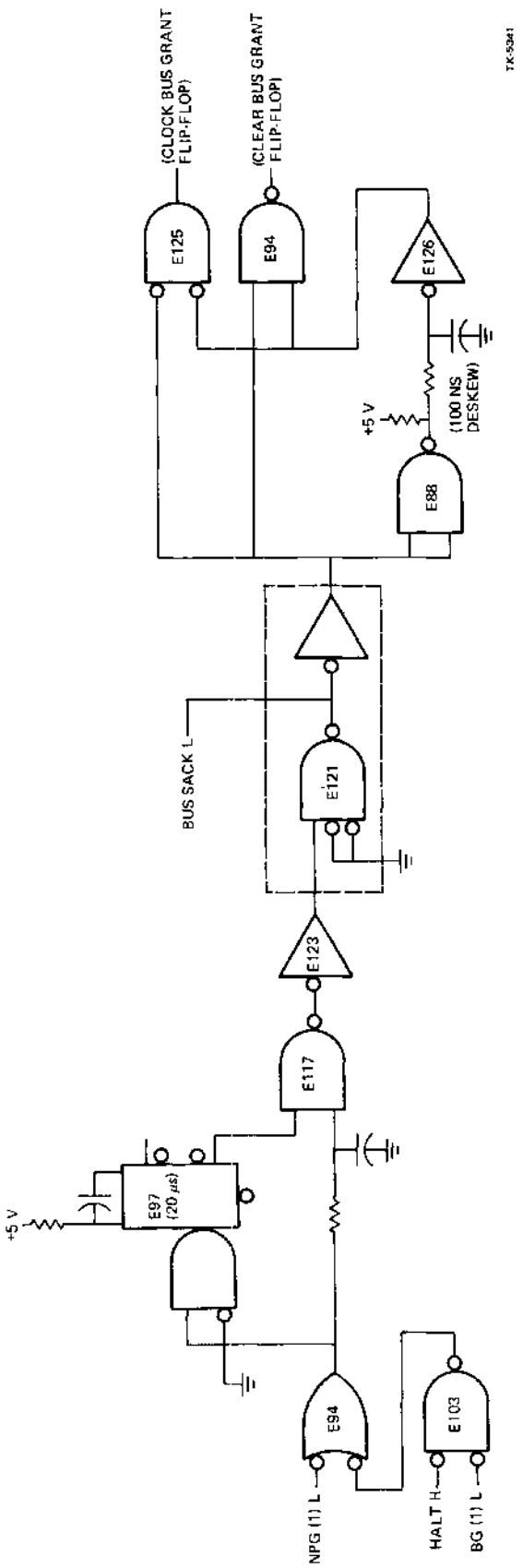


Figure 6-14 SACK Timeout

6.5.2.4 Program Interrupt Request (PIRQ) – The program interrupt request register is described in paragraph 2.3.1.2.

The PIRQ logic is located on K2-10. The PIRQ consists of E69, E15 and PROM E6. The PIRQ is loaded via BUF PAX D 15:9 with the assertion of K1-10 LOAD PRIH L and on the rising edge of PROC CLK L. PROM E6 is a priority encoder which takes the highest priority level (0-7) and changes it to a three digit octal value, PIA 3:1.

The bus arbitration logic (K4-2) issues a PIRQ grant by asserting K4-2 PIRQ GRANT L. This causes MPC 00 L and INT VECTOR L (K2-2) to be asserted when the next service state is entered. The trap service PLA (E99) asserts the PIRQ vector 240 which is strobed into the processor during the trap handling microsequence. The PIRQ vector 240 is put onto the SSMUX lines by the assertion of INT VECTOR L (K1-10) so the vector can be read by the processor.

6.5.3 Error Logic

The data transfer error logic in Figure 6-15 is used to log the four different types of errors that may occur during a CPU data transfer. The following are the four types of errors.

1. Bus error
2. Odd address error
3. Parity errors – memory read and cache
4. KT errors

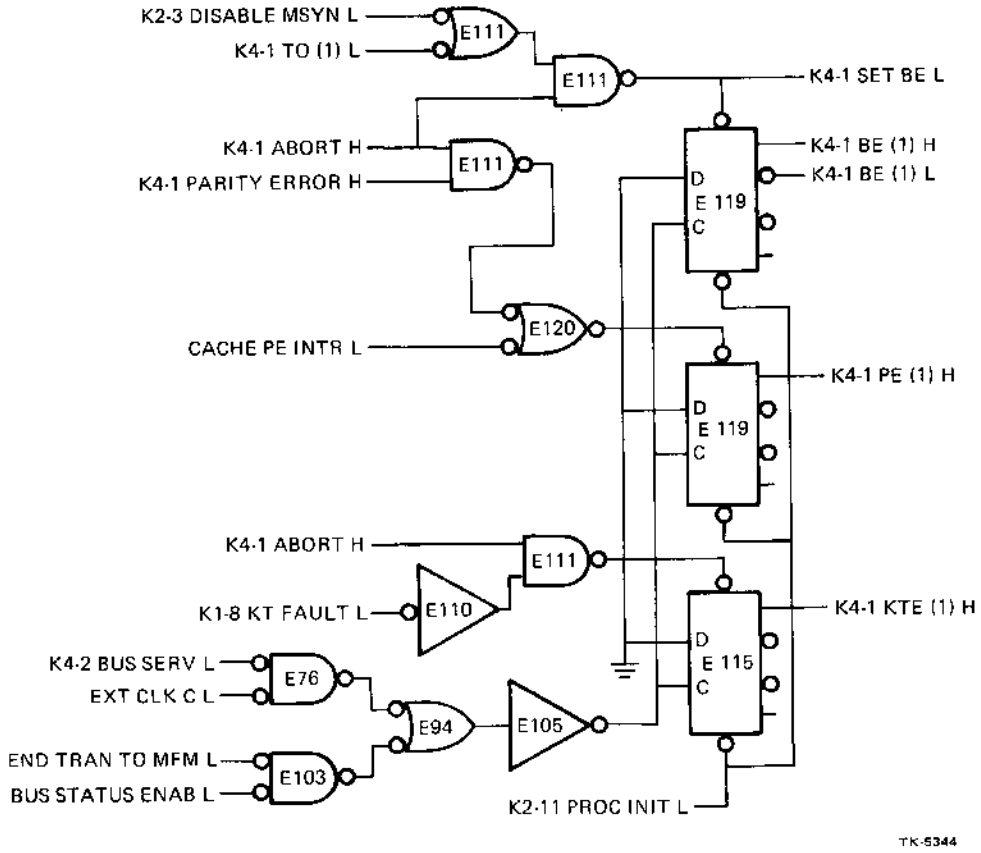


Figure 6-15 Transfer Error Logic

When any of these errors are detected, with the exception of a cache parity error, and the appropriate signal is asserted, ABORT H and ABORT RESTART L are asserted. Figure 6-16 shows the logic used to generate ABORT H and ABORT RESTART L. ABORT H is a pulse approximately 15 ns in duration that clocks the errors into flip-flops E115 and E119 where they are logged. ABORT H also clears the next MPC address latches (K2-6, K2-8) which forces the CPU into a trap service state and sets the appropriate bits in the CPU error register (K2-11). Approximately 100 ns after ABORT H is asserted, ABORT RESTART L is asserted and restarts the system clock. Restarting the system clock causes the CPU to service the trap condition created by the specific error or errors. The trap vector is generated by the trap service PLA (K2-2).

The error signals and the error conditions that cause them are shown in Table 6-1.

The error logic may be cleared by:

1. a processor INIT
2. a console read of the error register
3. servicing the error.

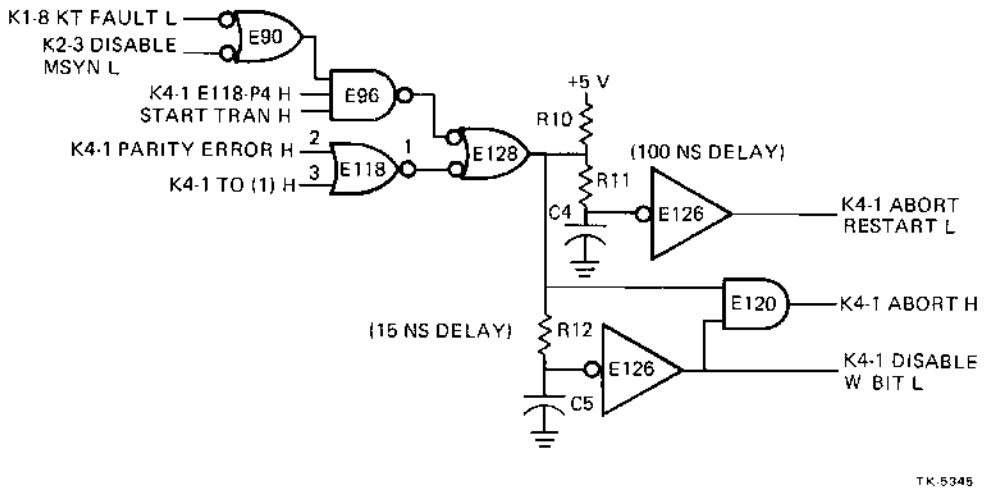


Figure 6-16 Generation of ABORT RESTART L and ABORT H

6.5.4 Cache Interface

An 8K byte direct-mapped cache memory reduces the average memory cycle time in the PDP-11/44 to a minimum. For an explanation of how the cache memory operates, refer to paragraph 6.12, KK11-B Cache.

6.6 SYSTEM CLOCK

The system clock (K2-1) on the PDP-11/44 generates all the timing signals to which the processor is synchronized. This allows an orderly execution of the various functions performed by the processor. The clock consists of a delay line (E3) and associated logic (E2, E13, E21, E22) that is used to create the positive feedback necessary for the clock to sustain oscillation. The various timing signals are taken from the different taps on the delay line.

Table 6-1 Error Logic Outputs

Error Signal	Error Condition
K4-1 BE (1) H	SSYN was not returned in time and the SSYN timeout one-shot (E97) times out, clocks flip-flop E115 and asserts K4-1 TO (1) H.
	An odd address error is detected and K2-3 DISABLE MSYN L is asserted.
K4-1 PE (1) H	A memory read parity error is detected and K4-1 PARITY ERROR H is asserted.
	A cache memory parity error is detected and CACHE PE INTR L is asserted. This signal does not generate ABORT H or ABORT RESTART L. This error is serviced at the end of the current instruction cycle.
K4-1 KTE (1) H	A nonresident, read only, or page length violation is detected and K1-8 KT FAULT L is asserted.

When power is applied to the clock, and if none of the clock disable signals are asserted (K42 INH L, K2-11 INT PROC INIT L, MAN CLK ENAB L), the clock will start running. The length of the operating cycle will be either 180 ns or 240 ns. The normal cycle, or short cycle, for the processor is 180 ns. The 240 ns cycle, or the long cycle, is used when a DATO or DATOB is being performed, or in situations where the condition code must be determined before an operation can be performed. The long cycle is selected by K2-6 LONG CYCLE L being asserted.

The basic timing signals generated by the clock are shown in Figures 6-17 and 6-18 in relationship to the delay line input (E3). The rising edge of PROC CLK L is designated as T0 because it is at this time that the execution of the next microinstruction begins. The other signals created from these basic signals are the following.

1. EXT CLK A L, EXT CLK B L, EXT CLK C L – These timing signals are logically identical to PROC CLK L. These separate signals are sent to the various modules. These signals are used so that loading will be equalized and edge skews minimized.

2. PROC CLK H – is the inverse of PROC CLK L.

3. EXT TAP 30 H – is identical to TAP 30 H.

4. EXT TAP 90 L – is the inverse of TAP 90 H.

5. ALLOW MSYN H – is generated by the ANDing of TAP 30 H, TAP 90 H, TAP 120 H or by RELOCATE H not being asserted. This signal delays the memory cycle until the PAX ADRS is loaded during a DATI or DATIP operation.

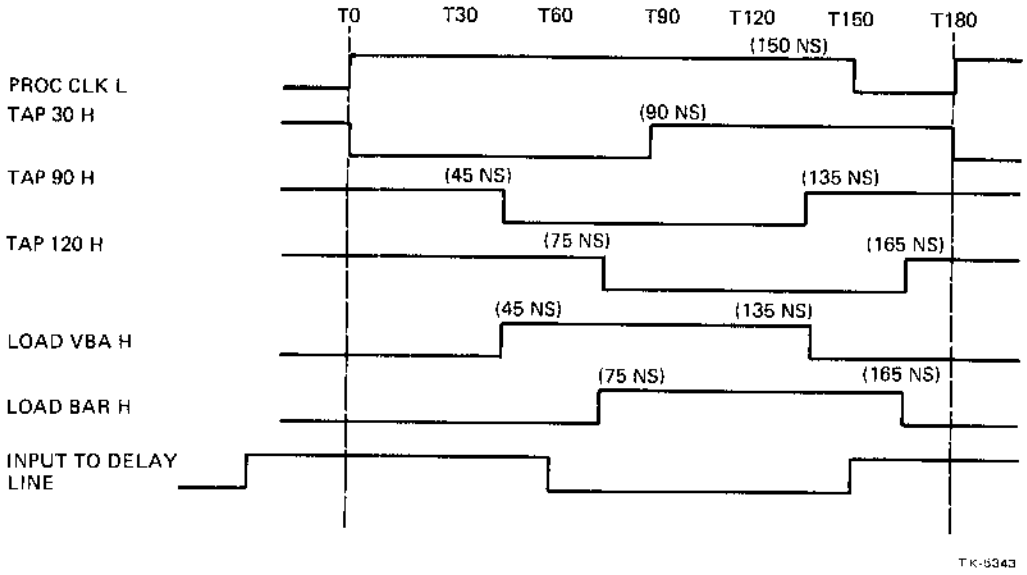


Figure 6-17 PDP-11/44 System Clock Short Cycle Timing Diagram

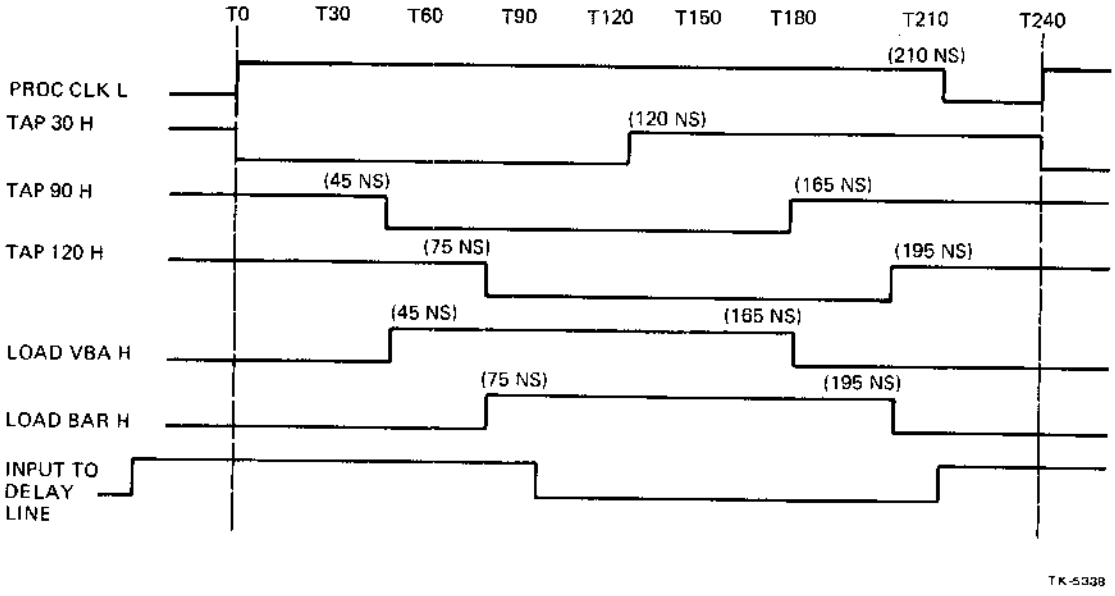


Figure 6-18 PDP-11/44 System Clock Long Cycle Timing Diagram

The clock may be stopped by asserting one of three signals.

1. MAN CLK ENAB L – This signal disables the clock and allows it to be manually stepped by the assertion of MAN CLK L. Any TTL-compatible waveform may be used to single-step the clock.

2. INT PROC INIT L – This signal will stop the clock when asserted.

3. INH L – This signal stops the clock when asserted. This signal indicates a bus cycle is in progress and can be overridden by CACHE RESTART L which restarts the clock.

Figure 6-19 shows a memory cycle in which the system clock is stopped.

The system clock is turned off by the appropriate signal under the following conditions.

1. During a BUS INIT that is not caused by a RESET
2. During the INIT portion of the power-up routine
3. During the INIT portion of the power-down routine
4. During a RESET
5. During a BUT service arbitration delay
6. During a priority interrupt
7. While BUS SACK is asserted by an interrupting device (not for NPRs)
8. During bus data transfers
9. After a HALT instruction is executed
10. When the console processor generates a clock inhibit signal
11. When the manual clock is enabled

6.7 POWER FAIL/AUTO RESTART

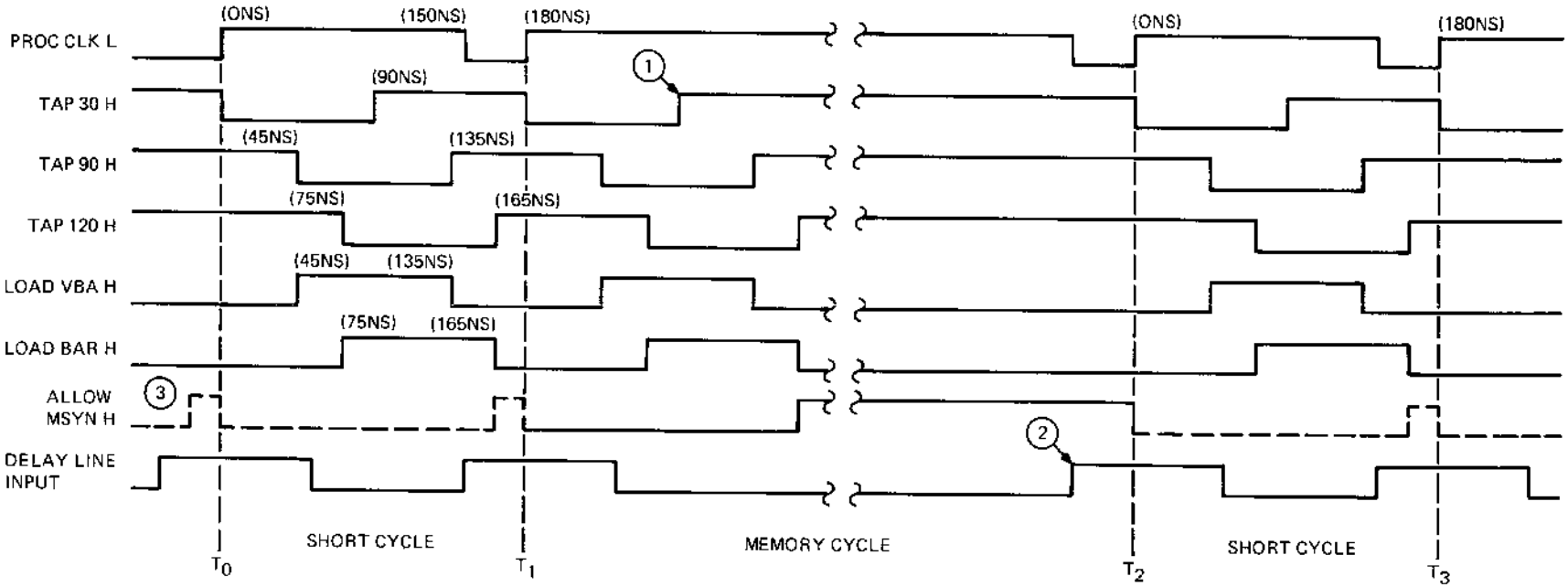
The PDP-11/44 power fail/auto restart circuitry (K2-2) serves the following purposes.

1. Initializes the microprogram, the UNIBUS control, and the UNIBUS to a known state immediately after power is applied to the computer.

2. Notifies the microprogram of an impending power failure.

3. Prevents the processor from responding to an impending power failure for 2 ms after initial startup.

The actual power fail/auto restart sequences are microprogram routines. The operation of the power fail/auto restart circiutry depends on the proper sequencing of two bus signals: AC LO and DC LO. Because of the electrical properties of the UNIBUS drivers and receivers, the entire computer system must be powered up for the machine to operate. Therefore, the processor is notified of a power failure in peripherals, as well as in its own ac source.



NOTES:

1. CLOCK INHIBITED
2. CLOCK RESTARTED
3. IF THE MEMORY CYCLE IS A NON-RELOCATED CYCLE ALLOW MSYN H IS ALWAYS ASSERTED.

TK-4476

Figure 6-19 PDP-11/44 System Clock Timing Diagram with Memory Cycle

The notification of power status of any PDP-11 system component is transmitted from each device by the signals BUS AC LO L and BUS DC LO L (K2-2). The power-up sequence (Figure 6-20) shows that BUS DC LO L is unasserted before BUS AC LO L is unasserted. When BUS DC LO L is not asserted, it is assumed that the power in every component of the system is sufficient to operate. When BUS AC LO L is not asserted, there is sufficient stored energy in the regulator capacitors of the power supply to operate the computer for 5 ms, should power be shut down immediately.

As ac power is removed, BUS AC LO L is asserted by the power supply, warning the processor of an impending power failure. When BUS DC LO is asserted, it must be assumed that the computer system can no longer operate predictably. Memories manufactured by DIGITAL use BUS DC LO L as a switched signal, turning them off even if power is still available. Time $\Delta t2$ (Figure 6-20) is the time delay between the assertion of BUS AC LO L and the assertion of BUS DC LO L; this time delay must be greater than 5 ms. This allows for power to be rapidly cycled on and off. According to PDP-11 specifications, on system start up, a minimum of 2 ms run time is guaranteed before a power fail trap occurs, even if the line power is removed simultaneous with the beginning of the power-up sequence. After the power fail trap occurs, a minimum of 2 ms run time is guaranteed before the system shuts down. Given the tolerance permitted in the timing circuitry used in most equipment, $\Delta t2$ must be greater than 5 ms.

When a pending power fail is sensed, a program trap occurs, causing the present contents of the PC (R7) and the PSW to be pushed onto the memory stack, as determined by the contents of R6 (stack pointer register). The PSW is then loaded with the contents of location 26_8 and R7 with the contents of 24_8. Processing is continued with the new R7 and PSW. The user's program must prepare for the impending power failure by storing away volatile registers and reloading location 24_8 and 26_8 with a power-up vector. This vector points to the beginning of a restart routine.

When power is restored, the processor loads the PC (R7) with the contents of location 24_8 and the PSW with the contents of location 26_8. After loading these registers, the user's program presumably will prepare locations 24_8 and 26_8 for another power failure. If the HLT RQST L input is asserted by an external switch closure, the processor powers up through locations 24_8 and 26_8 and halts.

Schematics for the power fail, auto restart, and bus reset logic are on K2-2. One-shot E9 generates a 150-ms processor INIT pulse as soon as BUS DC LO L is negated after power is applied to the processor. This pulse is used to initialize the processor by asserting K2-2 PWR CLR L which asserts the various initialize signals on K2-11. At the end of 150 ms, the PUP one-shot (E10) is fired if BUS DC LO L is not asserted and the processor begins the PC and PSW load routine. The PUP one-shot generates a 2-ms pulse, during which the assertion of BUS AC LO L is ignored.

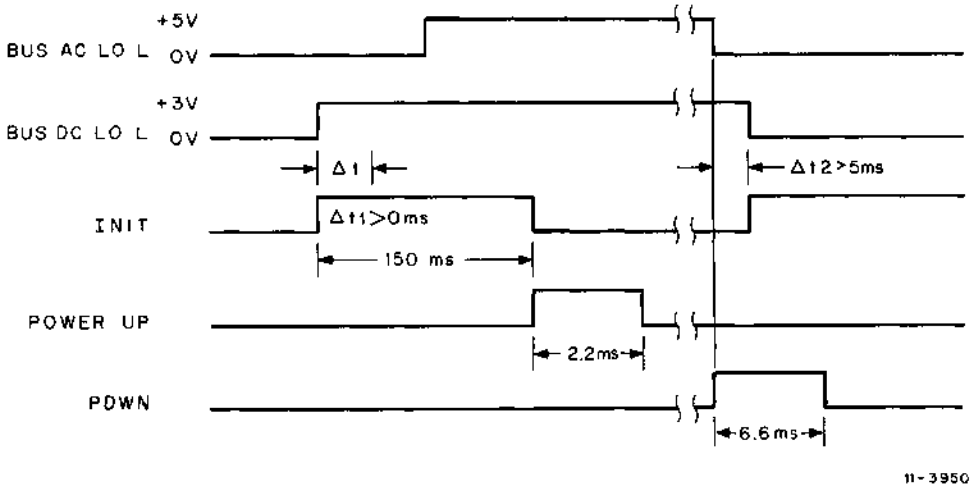


Figure 6-20 BUS AC LO and BUS DC LO Timing Diagram

The triggering of the 150-ms INIT one-shot (E9) also resets the POWER INIT flip-flop (E51). Setting this flip-flop forces the control store to run the power-up routine beginning at microPC address 001. It is this routine that reads location 24_8 and 26_8 for the new PC and PSW.

After PUP has timed out, the assertion of BUS AC LO L would fire the PDWN one-shot (E10). Upon entering the next service microcode state, K2-2 PFAIL H is latched into E112 (K4-2), causing a power fail trap to be recognized by the microprogram on entering the next service state. Various traps are arbitrated by the BUT service PLA (E99).

If a momentary power failure causes the assertion of BUS AC LO L but does not cause the assertion of BUS DC LO L, the processor will restart when the PDWN one-shot times out, retriggering the INIT one-shot.

CIM BOOT H is used to initiate a power fail sequence from the front panel boot switch. During the power failure initiated by the front panel boot switch, BUT BOOT H (K2-8) is asserted which forces the microcode to execute a boot routine which fetches the new PC from location 773024_8. A power failure initiated by a remote bootstrap module, such as an M9312, will also assert BUT BOOT H, causing a boot power-up sequence to occur.

6.8 MEMORY MANAGEMENT

Memory management is used to relocate a 16-bit virtual address, if necessary, and transmit the 22-bit physical address to the UNIBUS (refer to paragraph 6.9, Unibus Map), cache memory, or main memory. Address modification is the main function of memory management. The modification of addresses is called relocation because it consists of adding a fixed constant to a virtual address to create a physical address.

Memory management also allows the user to protect one section of memory from access by programs located in another section. Memory management divides memory into individual sections called pages. Each page has a protection or access key associated with it that defines the type of access allowed on that particular page. With the memory management unit, a page can be keyed nonresident (memory neither readable nor writable) or read-only (no write operations to memory). These two types of protection, in association with other features, enable the user to develop a secure operating system.

It is often desirable to load a program into one area of physical memory and execute it as if it were located in another area of memory, for example, when several user programs are simultaneously stored in memory. When any one program is running, it must be accessed by the processor as if it were located in the set of addresses beginning at 0. This process is called relocation. When the processor accesses virtual bus address 0, a base address is added to it and the relocated 0 location of the program is accessed. Typically this base address is added to all references while the program is running. A different base address is used for each of the other programs in memory.

Memory management specifies relocation on a page basis, which allows a large program to be loaded into nonadjacent pages in memory. This capability eliminates the need to shuffle programs to accommodate a new one. It also minimizes unusable memory fragments, thus allowing more users to be loaded into a specific memory size.

A program and its data can occupy as many as 16 pages in the memory. The size of each page may vary and can be any multiple of 32 words up to 4096 words in length. This feature allows small areas of memory to be protected (stacks, buffers, etc.), and also allows the last page of program, exceeding 4K words, to be of adequate length to protect and relocate the remainder of the program. As a result, the memory fragmentation problem inherent with fixed-length pages is eliminated. The base address of each page can be any multiple of 32 words in the physical address space, thus ensuring efficient use of main memory. The variable page length also allows the pages to be dynamically changed at run time.

Memory management provides three separate sets of pages for use in the processor's kernel, supervisor, and user modes. These sets of pages increase system protection by physically isolating user programs from service supervisor programs and the kernel program. The service programs are also separated from the kernel program. Separate relocation register sets greatly reduce the time necessary to switch context between mapping. The three sets of registers also aid the user in designing an operating system that has clearly defined communications, is modular, and is more easily debugged and maintained.

The virtual bus address space is further divided, within each of the kernel, supervisor, and user pages, into instruction space and data space (I and D space). I space contains code, that is, any word that is part of the program such as instructions, index words and immediate operands. D space contains information that can be modified, such as data buffers.

By using this feature, memory management can relocate data and instruction references with separate base address values. Therefore it is possible to have a user program of 64K words consisting of 32K of instructions and 32K of data.

6.8.1 Relocation

When memory management is enabled, the normal 16-bit direct-byte address is no longer interpreted as a direct physical address (PA) but as a virtual bus address (VBA) containing information to be used in constructing a new 22-bit PA. The information contained in the VBA is combined with relocation information contained in the page address register (PAR) to make a 22-bit PA. Using memory management, memory can be dynamically allocated in pages composed of from 1 to 128 blocks of 32 words each.

The starting PA for each page is a multiple of 32 words, and each page has a maximum size of 4096 words. Pages may be located anywhere within the PA space. The set of 16 PARs to be used to create the PA is determined by the current mode of operation of the CPU (kernel, supervisor, or user).

6.8.1.1 Address Mapping – All addresses with memory relocation enabled reference information in either instruction (I) space or data (D) space. I space and D space each have eight PARs in each mode of CPU operation. Using register SR3, the operating system may select to disable D space and map all references through I space, or to use both I and D space.

The basic information needed for the construction of a PA comes from the VBA, which is illustrated in Figure 6-21, and the appropriate PAR set.

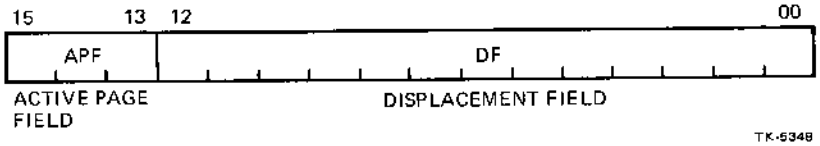


Figure 6-21 Interpretation of VBA

The VBA consists of:

1. The Active Page Field (APF) – This 3-bit field determines which of the eight PARs will form the PA.

2. The Displacement Field (DF) – This 13-bit field contains an address relative to the beginning of a page. This permits page lengths of up to 4K words. The DF is further subdivided into two fields as shown in Figure 6-22.

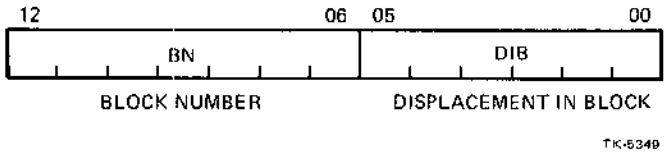


Figure 6-22 Displacement Field

The displacement field consists of:

1. The Block Number (BN) – This 7-bit field is interpreted as the block number within the current page.

2. The Displacement in Block (DIB) – This 6-bit field contains the displacement within the block referred to by the block number (BN).

The remainder of the information needed to construct the PA comes from the 16-bit page address field (PAF) which is contained in the PAR and specifies the starting address of the memory page. The PAF is actually a block number in the physical memory, for example, PAF=3 indicates a starting address of 96(3 × 32) words in physical memory.

The formation of the PA is illustrated in Figure 6-23.

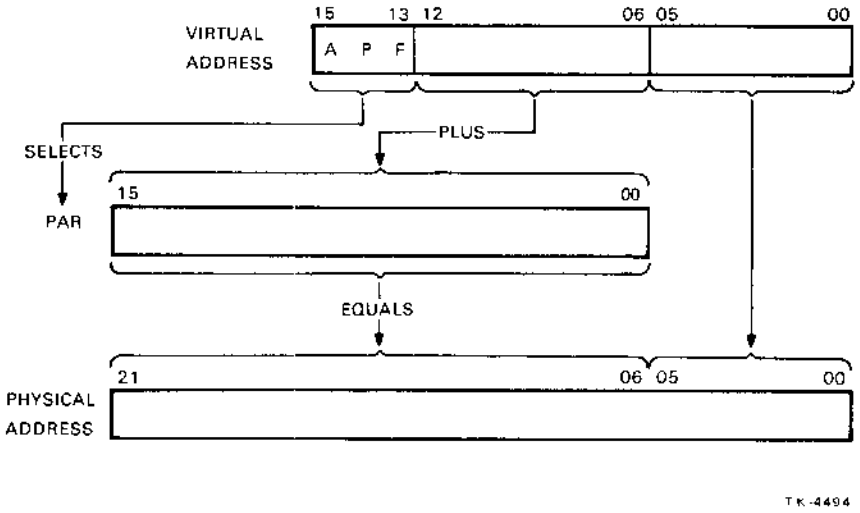


Figure 6-23 Construction of PA

The logical sequence involved in constructing a PA is as follows.

1. Select a set of PARs, depending on the space being referenced (I or D).
2. The APF of the VBA is used to select a PAR (PAR0–PAR7).
3. The PAF of the selected PAR contains the starting address of the currently active page as a block number in physical memory.
4. The block number (BN) from the VBA is added to the PAF to yield the number of the physical block in memory which will contain the PA being constructed.
5. The displacement in block (DIB) from the displacement field (DF) of the VBA is joined to the physical block number to yield a 22-bit PA.

6.8.1.2 Address Translation – Address translation is done from the VBA (Figure 6-24) which is created by latching the scratchpad outputs into the memory management (KT) buffer (K1-6, E77, E91, E106) on the falling edge of LOAD VBA H. K1-8 RELOCATE H, K2-10 E22 BITS 11 and K2-8 D SPACE H are also latched into the KT buffer at this time. These signals are used to enable the memory management logic, and to determine the address mode.

Table 6-2 shows which of these signals will be asserted for a particular address mapping mode.

16-Bit Mapping – Refer to Figure 6-25. In 16-bit mapping, the PA space consists of 28K memory locations (PA = 00000 000 – 00 157 777) and the 4K peripheral page (PA = 17 760 000 – 17 777 777).

Physical addresses 00 160 000 – 17 577 777 cannot be generated when using 16-bit mapping.

Refer to Figure 6-26. A 16-bit VBA is the PA if bits 15:13 are not equal to 111. In this case bits 21:16 of the PA are made zeros and bits 15:00 of the PA are the same as bits 15:00 of the VBA. If bits 15:13 of the VBA are equal to 111, then a reference to the peripheral page is intended by the program and bits 21:16 of the PA are set to 1 and bits 15:00 are the same as the VBA.

Table 6-2 Address Mapping Modes

Address Mode	D Space H	Relocate H	E22 Bits H
16-bit I space	X*	0	X
18-bit I space	0	1	0
18-bit D space	1	1	0
22-bit I space	0	1	1
22-bit D space	1	1	1

*Does not matter.

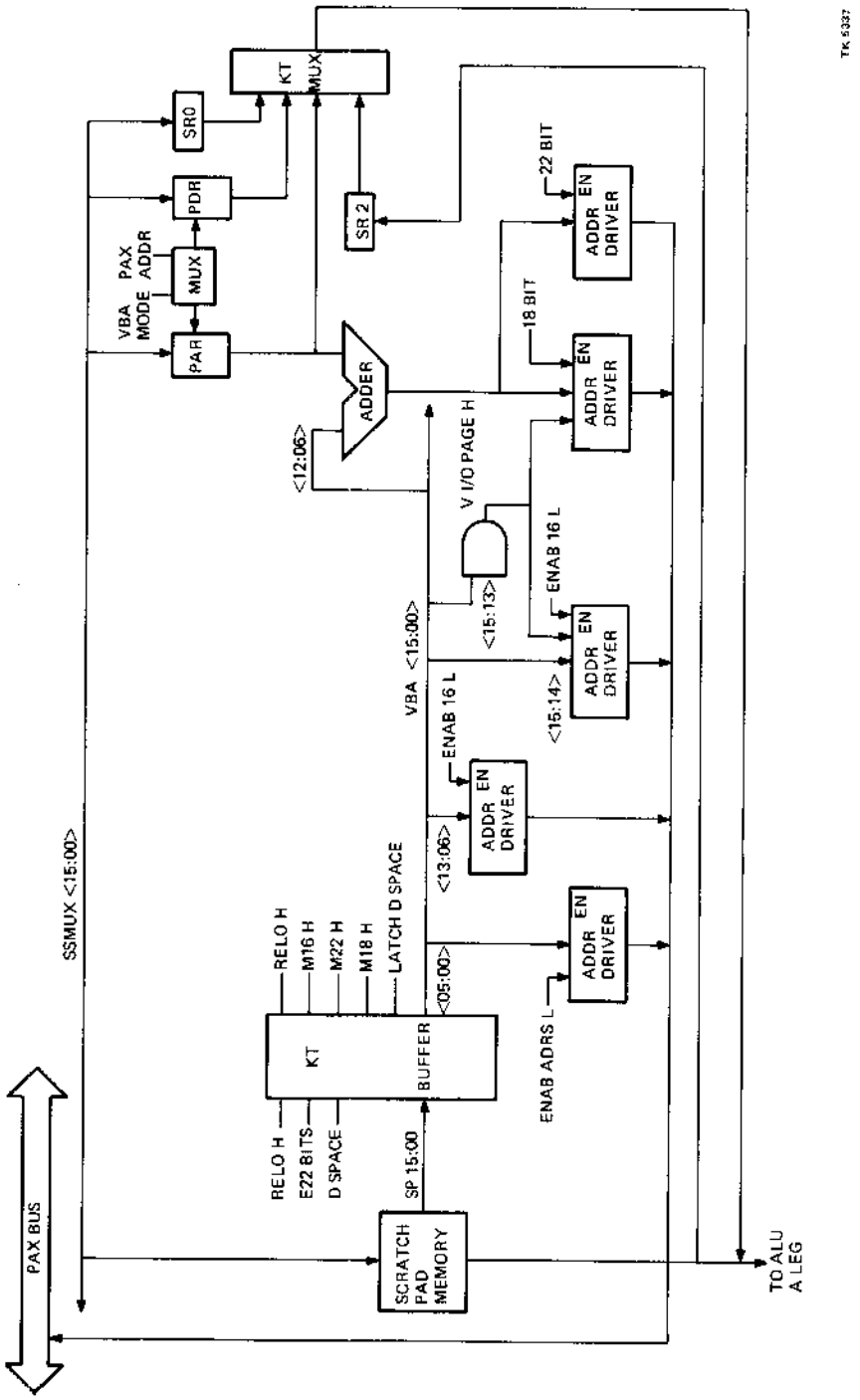


Figure 6-24 Memory Management Block Diagram

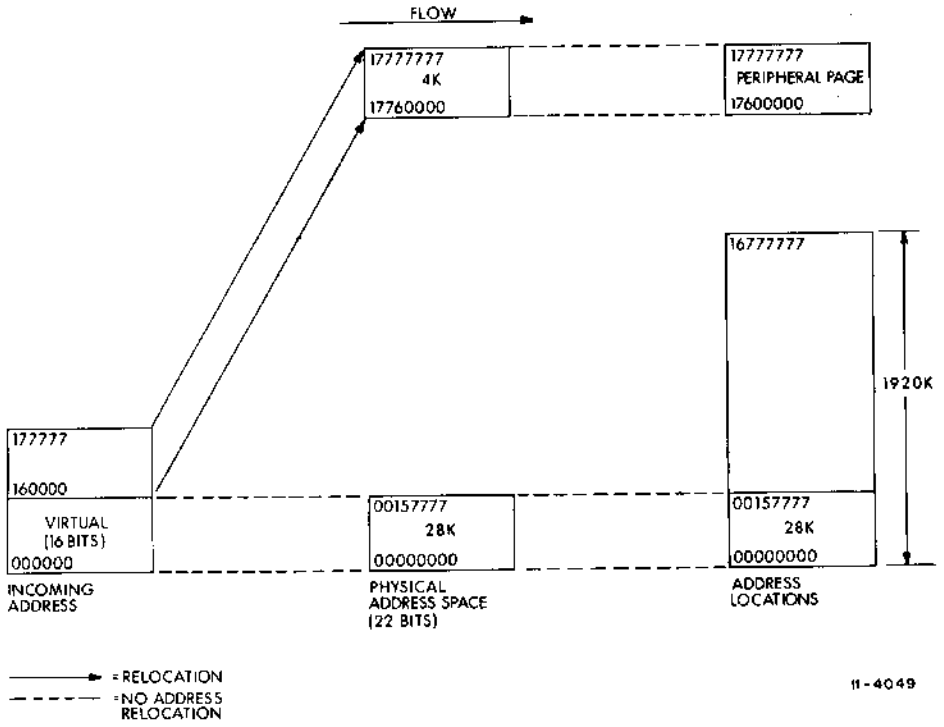


Figure 6-25 16-Bit Mapping

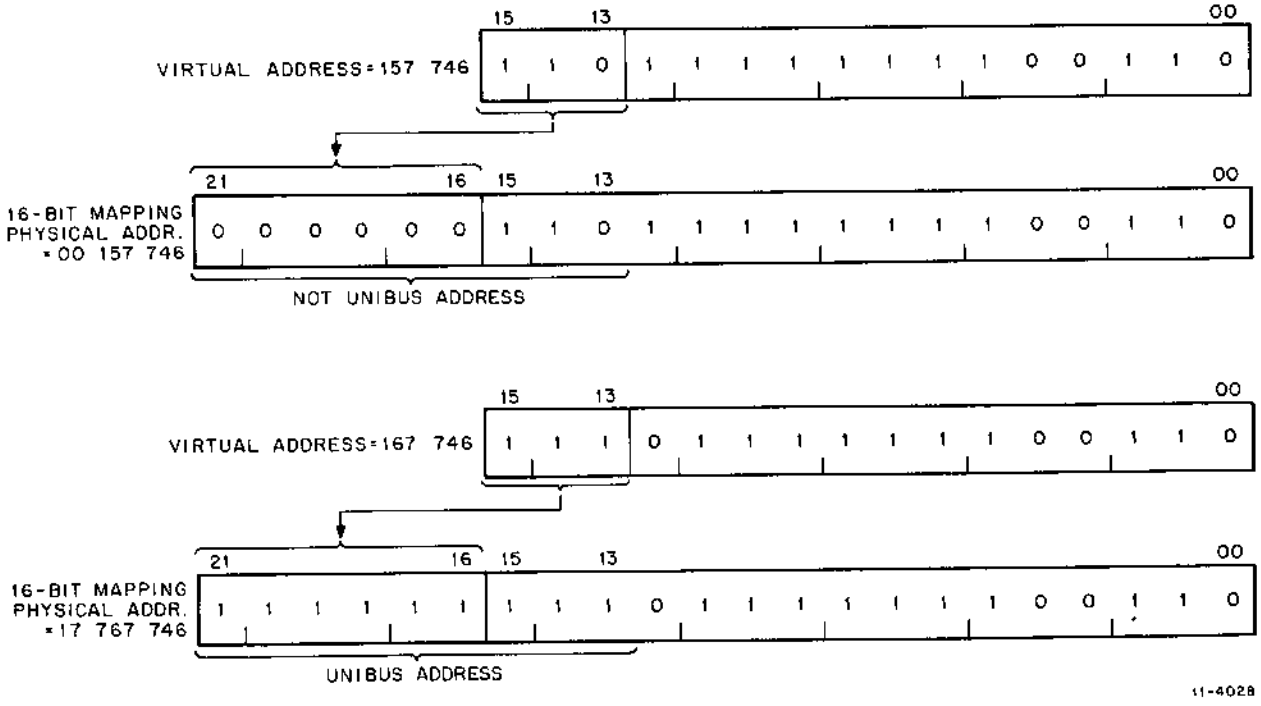


Figure 6-26 16-Bit Mapping: Generation of PA

16-bit mapping is enabled by K1-6 M16 (1) H being asserted. VBA 15:00 are latched into E71, E94 (K1-6) and E93 (K1-11) on the falling edge of LOAD BAR H and are then driven onto the PAX address lines. This action causes a one-to-one transfer of VBA 15:00 to PAX 15:00, and PAX 21:16 are set to 0 if VBA 15:13 are not all ones. If VBA 15:13 are all ones, then K1-6 V I/O PAGE is asserted and PAX 21:16 are forced to ones. This action causes a reference to the I/O page which is contained in the upper 4K of memory.

18-Bit Mapping – Refer to Figure 6-27. In 18-bit mapping the VBA is added to the selected PAF to generate the PA. This address mode has a range of 128K. The PA space consists of 124K (00 000 000 – 00 757 777) and the 4K peripheral page (17760000 – 17777777).

18-bit mapping is enabled by the assertion of K1-6 RELO (1) H and K1-6 M18 (1) H. As in 16-bit mapping, VBA 05:00 are directly driven onto the PAX address lines via E71 (K1-6). VBA 15:13 are used to select a PAR (PAR 0-7) which is then added to VBA 12:06 by high speed adders E98, E99, E113 (K1-11). Bits 15:12 of the PAR are not used in 18-bit mapping. The sum of PAR 11:00 and VBA 12:06 create PA 21:06 which is then driven onto the PAX address lines by E95 and E104. If bits 17:13 are all ones, a reference to the peripheral page is intended by the program: E116 detects this condition and forces PA 21:18 to ones. If bits 17:13 are not all ones then E116 will force PA 21:18 to 0.

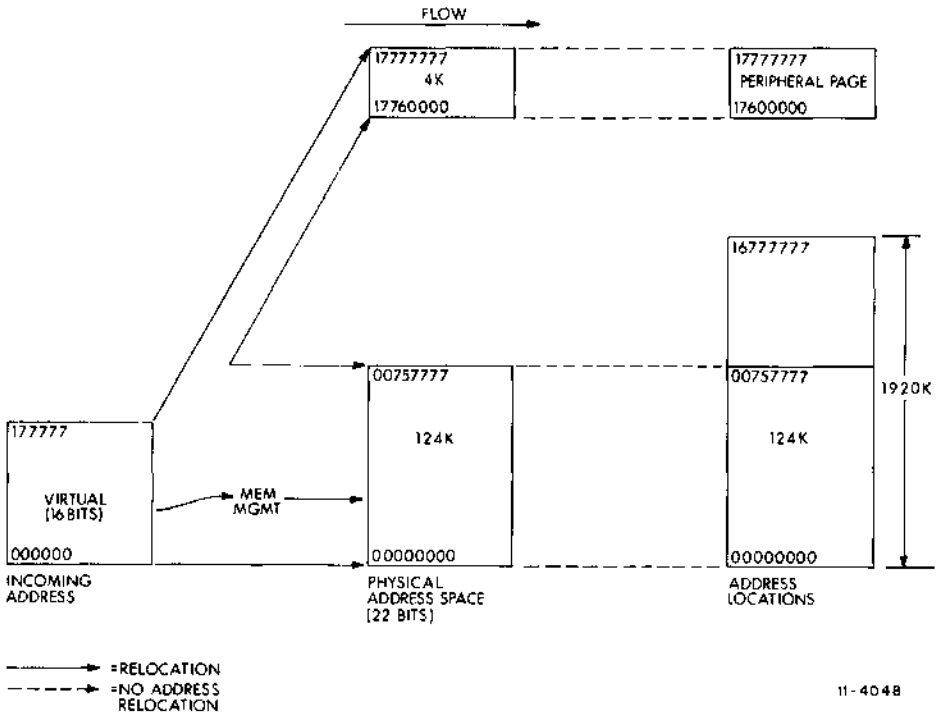


Figure 6-27 18-Bit Mapping

Figure 6-28 illustrates an 18-bit PA that is not a UNIBUS reference, that is, bits 17:13 are not all ones. In this case bits 21:18 of the PA are set to zeros, which causes a memory reference.

Figure 6-29 illustrates an 18-bit relocated address that is a UNIBUS reference, that is, bits 17:13 are all ones. In this case bits 21:18 of the PA are changed to ones, which causes a UNIBUS reference.

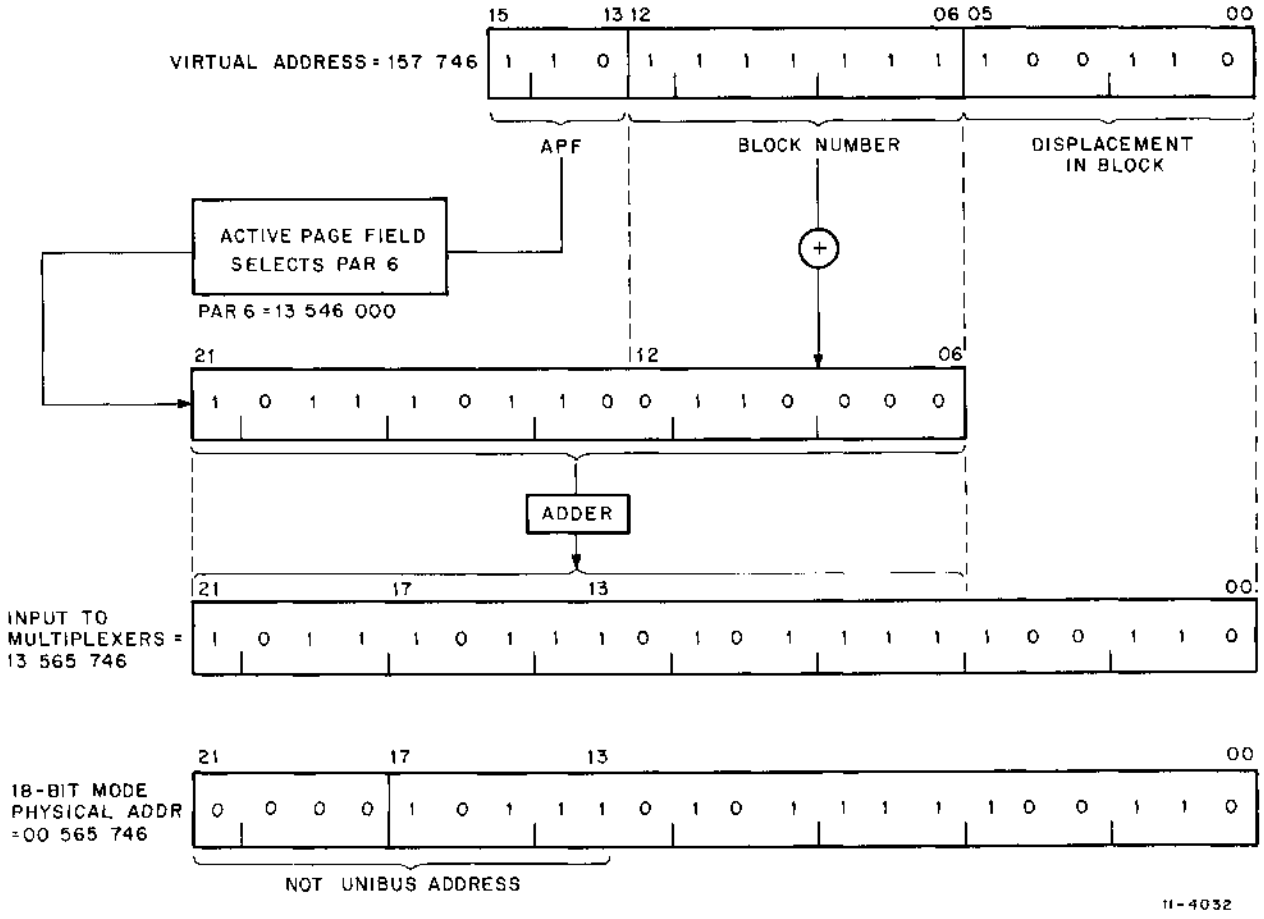


Figure 6-28 18-Bit Mapping: Memory Address

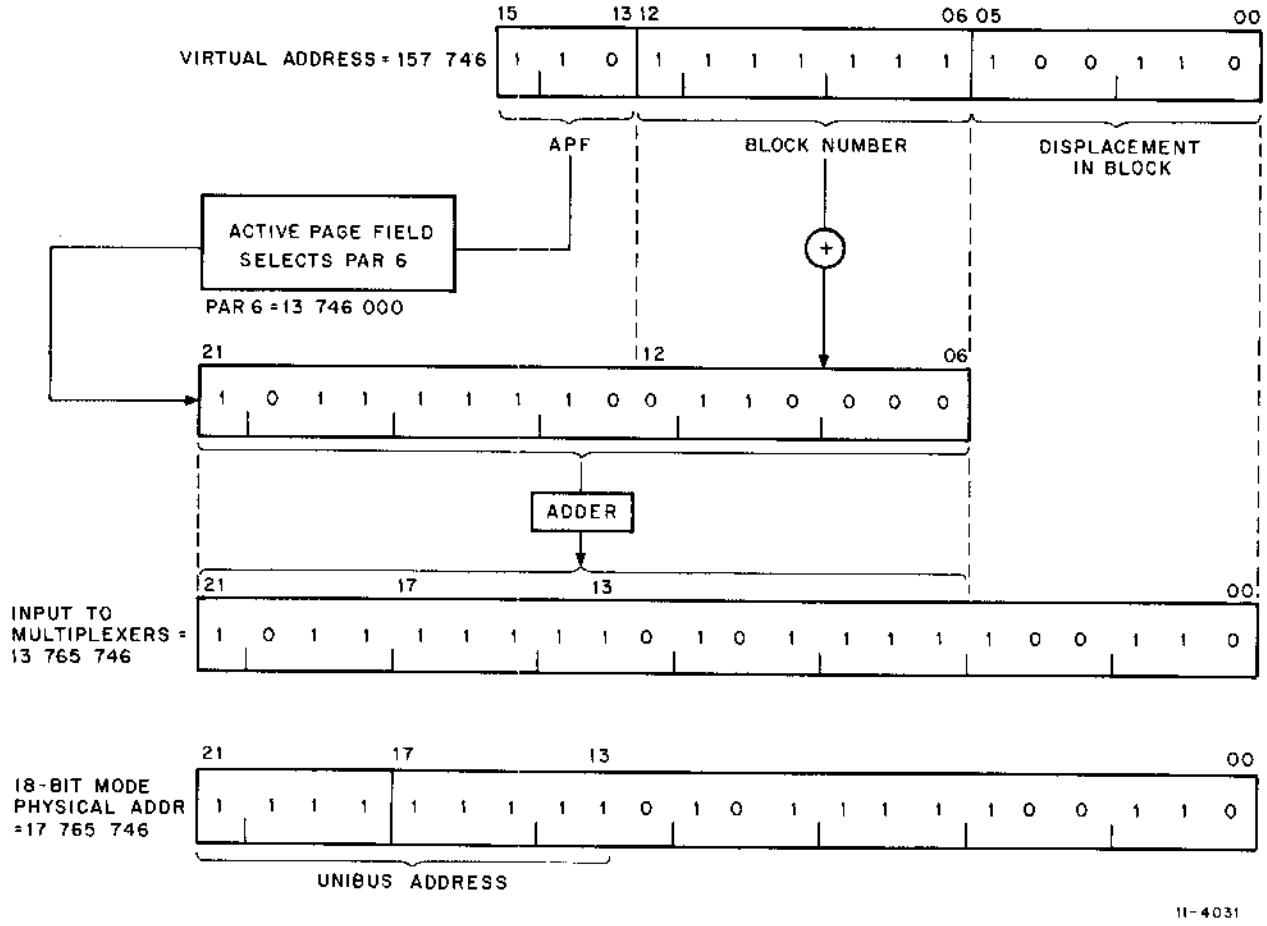


Figure 6-29 18-Bit Mapping: UNIBUS Address

22-Bit Mapping – Refer to Figures 6-30 and 6-31. In 22-bit mapping the VBA is relocated in the same manner as 18-bit mapping, but the relocated address becomes the PA without modification. Thus, all PAs from 00 000 000 – 17 777 777 can be generated.

Addresses 17 760 000 – 17 777 777 are UNIBUS I/O page references. Addresses 00 000 000 – 16 777 777 are memory addresses. The top 124K of addresses 17 000 000 – 17 757 777 may be used to access memory via the UNIBUS map (paragraph 6.9).

22-bit relocation is enabled by the assertion of K1-6 RELO (1) H and M22 (1) H. As with 18-bit relocation, VBA 05:00 are used to make PA 05:00 and driven onto PAX address 05:00. VBA 15:13 are used to select a PAR which contains a base constant. The 16 bits of the PAR are added to VBA 12:06 by adders E98, E99, E113, E122, and carry generator E110. The output of the adders create PA 21:06 which are driven onto the PAX address lines by E95 and E115. If a reference to a UNIBUS address is made, PA 21:18 all ones, K1-11 UPPER 128K L will be asserted and passed to the UNIBUS map logic (paragraph 6.9).

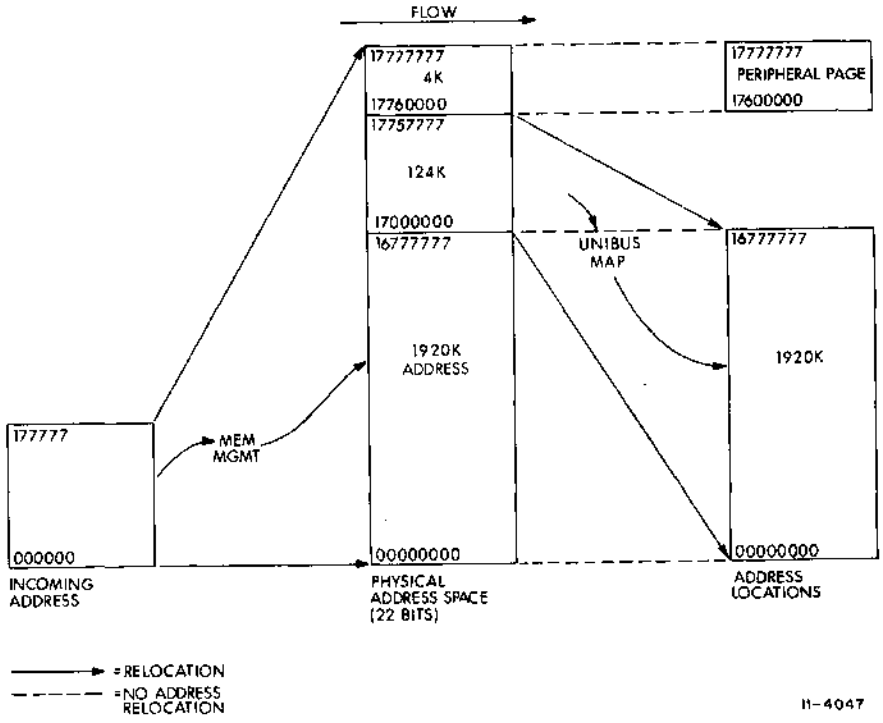


Figure 6-30 22-Bit Mapping

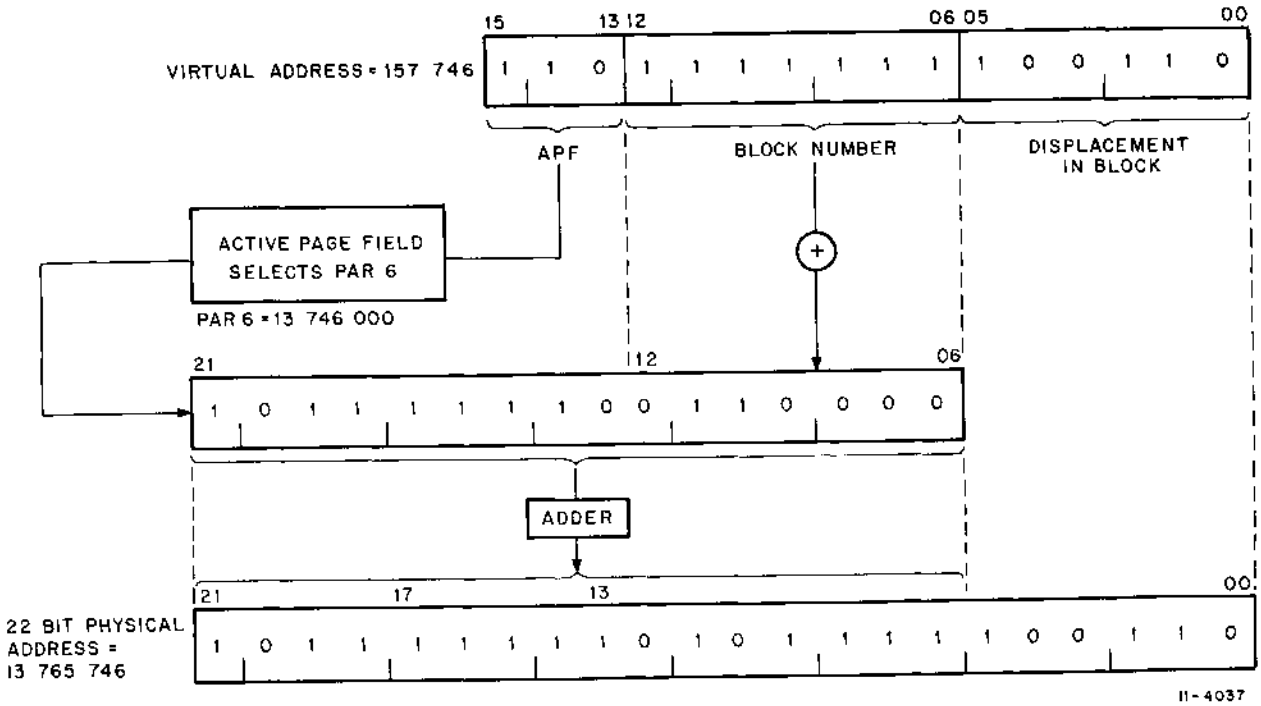


Figure 6-31 22-Bit Address Mapping

6.8.2 Protection

A timesharing system performs multiprogramming; it allows several programs to reside in memory simultaneously, and to operate sequentially. Access to these programs and the memory space they occupy must be strictly defined and controlled. Several types of protection must be afforded a timesharing system.

1. User programs must not be allowed to expand beyond allocated space, unless authorized by the system.

2. Users must be prevented from modifying common subroutines and algorithms that are resident for all users.

3. Users must be prevented from gaining control of or modifying the operating system software.

The memory management logic provides the hardware facilities to implement all of the above types of memory protection.

6.8.3 Page Address Registers (PAR)

The page address registers (K1-7) contain the constant or base address which memory management adds to the VBA to create a 22-bit physical address. The forty-eight 16-bit PARs are made up of four 256 × 4 random-access memories, E69, E59, E58, E66. These registers can be either read or written.

Address selection is done via a multiplexer made up of E97 and E105. K1-10 PAR + PDR L is used to select the inputs used to address the PARs. During memory management relocation, K1-10 PAR + PDR L is not asserted. K1-9 PSEL 05:00 are created from VBA 15:13, MODE 01:00 (processor mode), and LATCH D SPACE. VBA 15:13 determine which PAR, 0-7, is to be used. MODE 01:00 selects which set of PARs, user, supervisor, or kernel will be used. LATCH D SPACE selects I space or D space. Figure 6-32 shows the allocation of the PARs. When a PAR is going to be written, examined by the console, or read by the program, K1-10 PAR + PDR L is asserted and PAX/A08, 06, 04:01 are used to create K1-9 PSEL 05:00. K1-10 PAR + PDR L is generated by PLA E114. Data on the SSMUX will then be written into the selected PAR on the falling edge of EXT CLK B L. Whether the high byte or the low byte or both high and low bytes will be written is determined by K1-10 LOAD PARH L and K1-10 LOAD PARL L which are used to enable the write inputs to the PARs.

6.8.4 Page Descriptor Registers (PDR)

In addition to its relocation function, memory management has supervisory or memory protection functions which are determined by the contents of the PDR.

The PDR is read at the same time as its corresponding PAR during relocation and contains all the information required for the supervisory or memory protection functions. Figure 6-33 shows the PDR.

Access Control Field (ACF)

This 2-bit field, occupying bits 2:1 of the PDR, contains the access rights to a particular page. The keys specify the manner in which a page may be accessed and whether or not a particular access should result in an abort of the current operation. In the context of access control, the term "write" is used to indicate the action of any instruction which modifies the contents of any addressable word.

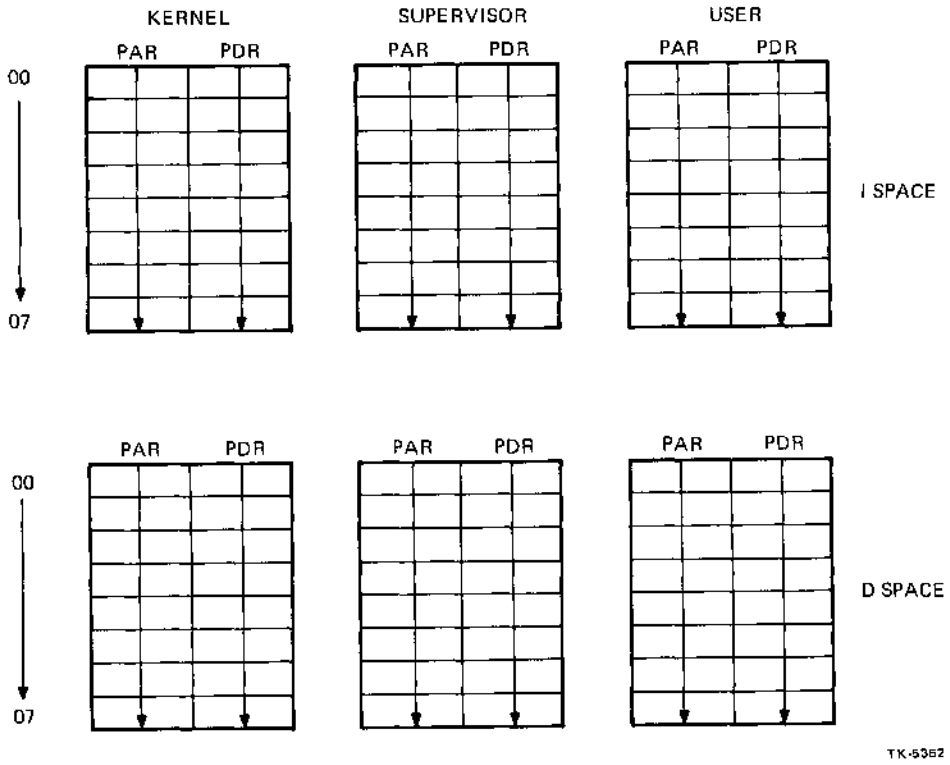


Figure 6-32 Memory Management Relocation Registers

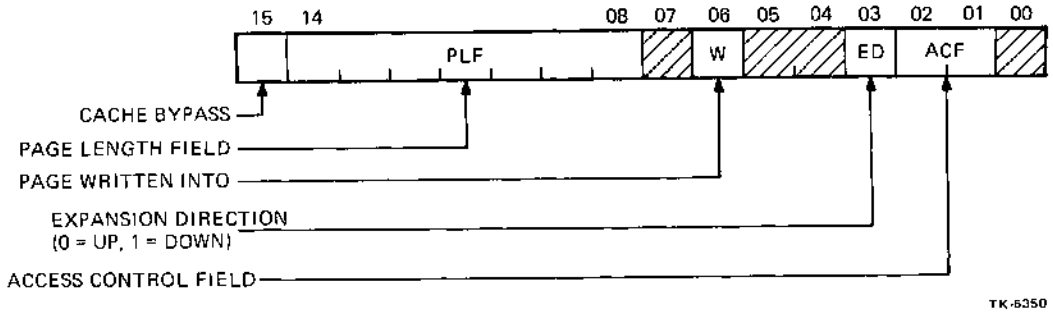


Figure 6-33 Page Descriptor Register

The access control keys are the following.

ACF	Description	Function
00	nonresident	abort all accesses
01	read only	abort all write attempts
10	illegal mode	abort all accesses
11	read/write	read or write allowed

It should be noted that the use of I space in conjunction with read-only access provides the user with another form of protection, Execute Only.

Expansion Direction (ED)
Bit 3 of the PDR specifies the direction the page is to expand. If ED = 0, the page expands upward from block number 0 to include blocks with higher addresses (Figure 6-34). If ED = 1, the page expands downward from block number 177_8 to include blocks with lower addresses (Figure 6-35).

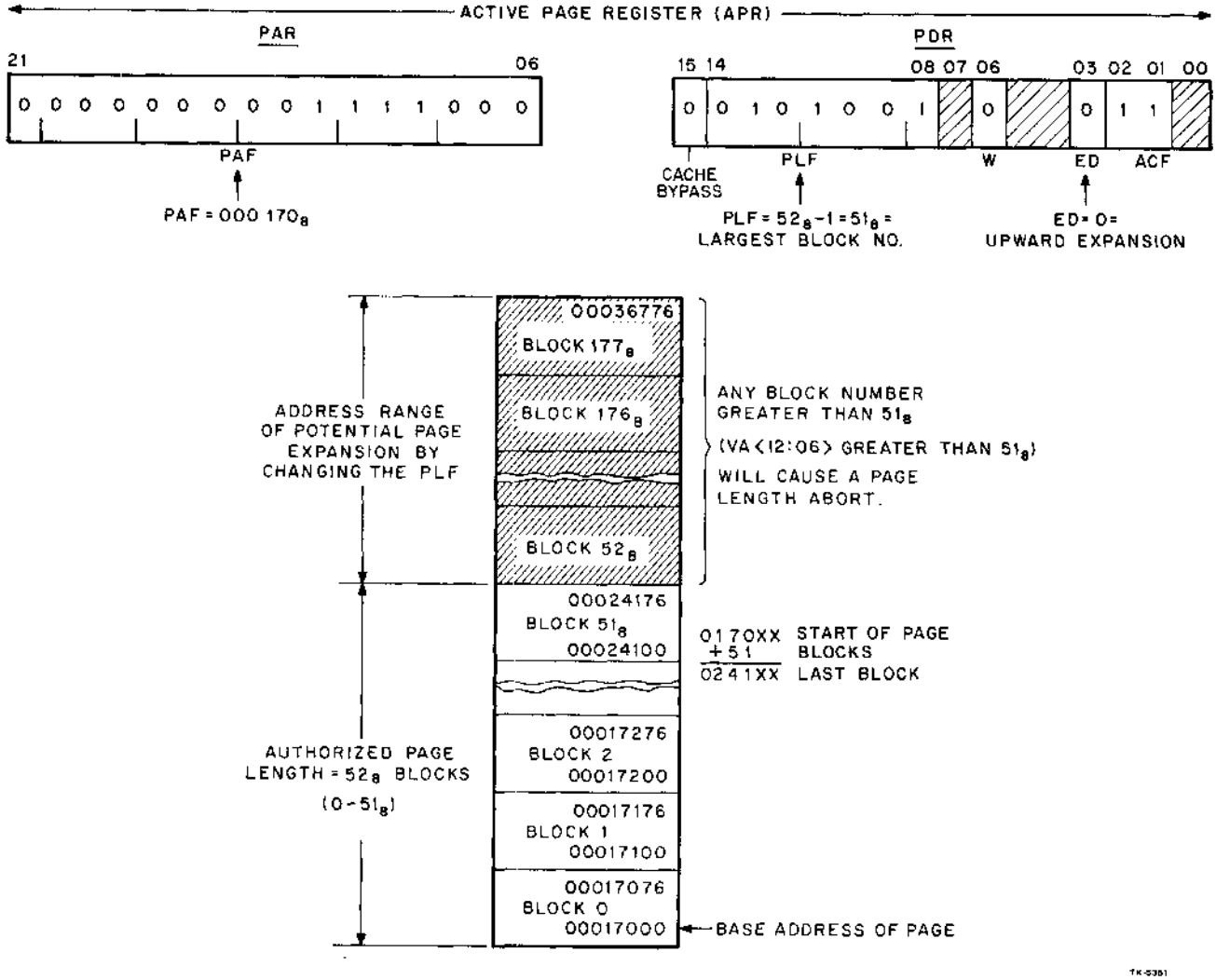


Figure 6-34 Upward Expansion

Upward expansion is typically used for program space, and downward expansion for stack space.

Written Into (W)
The W bit, bit 6, indicates whether or not the specified page has been modified (written into) since either the PAR or PDR was loaded (W = 1 is affirmative). The W bit is useful in applications which involve disk swapping and memory overlays. It is used to determine which pages have been modified and must be saved in their new form, and which pages have not been modified and can be simply overlayed.

The W bit is reset to 0 whenever the PAR or PDR associated with it is written into.

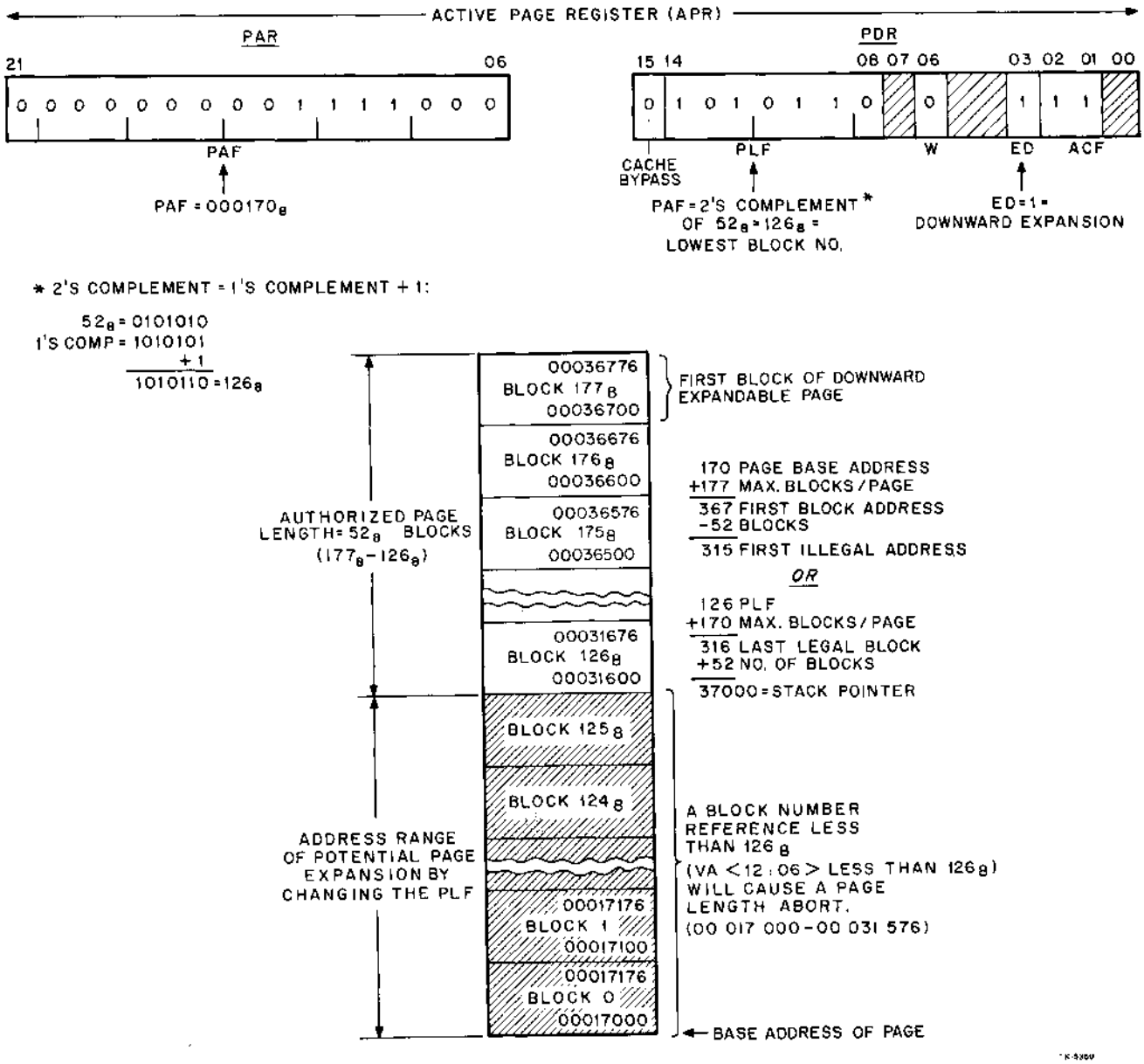


Figure 6-35 Downward Expansion

Page Length Field (PLF)
The 7-bit field occupying bits 14:08 of the PDR specifies the block number (BN) which makes up the boundary of that page. The BN of the VBA is compared against the PLF to detect page length errors.

An error occurs when expanding upward if the BN is greater than the PLF, and when expanding downward if the BN is less than the PLF.

The PDRs are made up of 256 × 4 RAMs E68, E70, E67, and 256 × 1 RAM E87 on K1-7. The PDRs are addressed in the same way as the PARs. They are written in the same manner as the PARs except that K1-10 LOAD PDRH L and K1-10 LOAD PDRL L are used to enable the write inputs to E68, E70 and E67. E87 and latch E89 are used for the W bit. The write enable signal is generated whenever a page of a PAR or PDR is written into. K1-9 WRITE WBIT H, K1-1 REG CLK H, and K1-6 PAX CI H are ANDed together by E109 to create this signal.

6.8.5 Memory Management Fault Logic

The memory management fault logic (K1-8) is used to notify the operating system of a memory management error, such as an attempt to access a nonresident page. The error logic consists of comparators E81 and E92 and PROM E84. PROM E84 generates four errors which are determined by the existing input conditions. A list of the inputs and their description is contained in Table 6-3. Table 6-4 lists the outputs of the PROM and their description.

Table 6-3 Memory Management Fault PROM Inputs

Input Signal	Description
BUF DATA TRAN (1) H	When asserted, a bus data transfer is in progress.
UBUS C1, C0	Used to determine the type of data transfer being done (DATI, DATIP, DATO, DATOB).
KT DISABLE MSYN L	Disables the memory management logic when the data transfer is an odd address (byte address). The memory management logic uses only word references.
MODE 01, 00	These two signals give the operating mode of the processor (kernel, supervisor, or user).
ACF2, ACF1	These are the access control bits from the PDR and are used to notify the fault logic of the type of access the program has to the specific page.
Comparator E92 Output	Used with ED to determine if a page length error has occurred.
ED	Expansion direction bit of the PDR used to determine if page expansion is up or down.
Chip Enable	Allows the memory management fault PROM to be enabled only during a relocated bus transfer.

Table 6-4 Memory Management Fault PROM Outputs

Output	Description
RO	Indicates a write access was attempted to a read-only page.
PL	Indicates an attempt to address a memory location outside the specified page boundaries or the PSW contains an illegal processor mode.
NR	Indicates an attempt to access a nonresident page.
MAINT	Used for memory management maintenance purposes. Allows the user to prevent relocation on the destination portion of a memory cycle.
KT FAULT L	Used to signal that a memory management fault has occurred. Selects the multiplexer input to SR0 15:13, 08. Starts the abort function.

Comparators E81 and E92, along with the expansion direction bit from the PDR, are used to determine if a page length error has occurred. The comparators compare VBA 12:06 with the page length field in the PDR (bits 14:08) to determine if the VBA page address is greater than, equal to, or less than the PDR page length field. If the expansion direction of the page is up, then VBA 12:06 must be less than or equal to the PLF or a page length error occurs. If the expansion direction is down, then VBA 12:06 must be greater than or equal to the PLF or a page length error occurs.

When a memory management error is detected K1-8 KT FAULT L is asserted, which selects PROM E84 outputs as the inputs to SR0 15:13, 08, along with aborting the data transfer that was in progress. The output of E100 is clocked into SR0 15:14, 08 (E111) by K1-1 REG CLK H ANDed with K2-7 BUF DATA TRAN (1) H and either K1-8 KT FAULT L or LOAD SR0H L. LOAD SR0H L allows the upper byte of SR0 to be loaded from the SSMUX and K1-8 KT FAULT L loads SR0 with a hardware-generated error condition. When any one of SR0 bits 15:13, 08 is set, K1-8 ERROR H is asserted which locks out any other attempts to change the contents of SR0. The register cannot be reloaded until it has been cleared manually and K1-8 ERROR H is negated.

6.8.6 I and D Space

The concept of I and D space is used in mapping information into separate physical memory segments depending on whether the information is considered instructions (I) or data (D). In PDP-11 architecture all instruction fetches, immediate mode operands, absolute addresses, and index words are located in I space; any other memory reference that does not fit into these categories is located in D space. In the PDP-11/44 separate PARs and PDRs are used for I and D space relocations (Figure 6-32). Bits 02:00 of SR3 enable D space for each of the three processor operating modes: bit 00 user, bit 01 supervisor, bit 02 kernel. The hardware then selects the correct register set. If D space is not enabled for a particular operating mode, all references are then relocated through I space.

The use of I and D space allows programs to exist in two virtual segments and effectively doubles the addresses available to the user from 32K words to 64K words.

6.9 UNIBUS MAP

The UNIBUS map is the interface between the UNIBUS and main memory. It responds as a slave device to UNIBUS signals and converts 18-bit UNIBUS addresses to 22-bit memory addresses.

The top 4K word addresses of the 128K UNIBUS addresses are reserved for the CPU and I/O registers and are called the peripherals page (Figure 6-36). The lower 124K addresses are used by the UNIBUS map to reference physical memory.

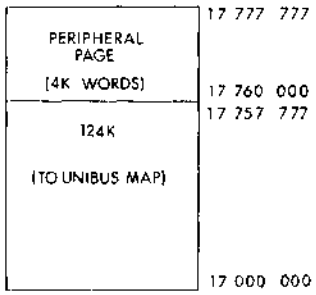


Figure 6-36 UNIBUS Address Space

The UNIBUS map is made up of a 21-bit adder (K4-8) and 32 mapping registers (K4-6) which may be written or read. These registers are 21 bits wide and require two UNIBUS transactions for each read or write. Therefore, 64 addresses are allotted to them on the I/O page (Table 6-5). It should be noted that the last mapping register (addresses 17 770 374 and 17 770 376) can be read and written, but cannot be used to map UNIBUS addresses because it would be used by addresses in the range of the peripherals page (17 760 000 – 17 777 777).

The UNIBUS map does relocation by adding one of 31 UNIBUS map registers, which contain a relocation constant, to the 18-bit UNIBUS address to create a 22-bit physical address (PA) which is used to reference physical memory. When the UNIBUS map is disabled its operation is transparent to the user and the incoming UNIBUS address is used to reference the first 124K of physical memory.

Figure 6-37 shows a block diagram of the UNIBUS map and its associated control logic.

6.9.1 Map Control

The map control logic (K4-4) is used to control the reading and the writing of the 32 map registers and consists of UNIBUS map and boot address decode PLA (E45), a delay line (E69), and associated read/write and buffer control logic. PLA E45 decodes the UNIBUS address to determine if a read or write of the map registers is intended and asserts the appropriate signal, MAP WRITE L or MAP READ L. MAP WRITE L and MAP READ L are used to generate MAP R/W L. MAP R/W L is used to accomplish the following during a read or write of the map registers.

1. Assert DISALLOW MEM MSYN. This keeps MSYN, intended for the map registers, from being sent to main memory.

2. Asserts the input of delay line E69 which is used to generate UBI SSYN L (approximately 120 ns after MAP R/W L is asserted), and MAP SSYN H which is used to negate WRITE MAP L.

3. Assert MAP CE L which is the chip-enabling signal for the map registers.

Table 6-5 Access to Unibus Map Registers

Register No.	UNIBUS Address Read or Write		UNIBUS Address for Memory Reference
	HI	LO	
0	17 770 200,	02	17 000 000 – 17 017 777
1	17 770 204,	06	17 020 000 – 17 037 777
2	17 770 210,	12	17 040 000 – 17 057 777
3	17 770 214,	16	17 060 000 – 17 077 777
4	17 770 220,	22	17 100 000 – 17 117 777
5	17 770 224,	26	17 120 000 – 17 137 777
6	17 770 230,	32	17 140 000 – 17 157 777
7	17 770 234,	36	17 160 000 – 17 177 777
10	17 770 240,	42	17 200 000 – 17 217 777
11	17 770 244,	46	17 220 000 – 17 237 777
12	17 770 250,	52	17 240 000 – 17 257 777
13	17 770 254,	56	17 260 000 – 17 277 777
14	17 770 260,	62	17 300 000 - 17 317 777
15	17 770 264,	66	17 320 000 – 17 337 777
16	17 770 270,	72	17 340 000 – 17 357 777
17	17 770 274,	76	17 360 000 – 17 377 777
20	17 770 300,	02	17 400 000 – 17 417 777
21	17 770 304,	06	17 420 000 – 17 437 777
22	17 770 310,	12	17 440 000 – 17 457 777
23	17 770 314,	16	17 460 000 – 17 477 777
24	17 770 320,	22	17 500 000 – 17 517 777
25	17 770 324,	26	17 520 000 – 17 537 777
26	17 770 330,	32	17 540 000 – 17 557 777
27	17 770 334,	36	17 560 000 – 17 577 777
30	17 770 340,	42	17 600 000 – 17 617 777
31	17 770 344,	46	17 620 000 – 17 637 777
32	17 770 350,	52	17 640 000 – 17 657 777
33	17 770 354,	56	17 660 000 – 17 677 777
34	17 770 360,	62	17 700 000 – 17 717 777
35	17 770 364,	66	17 720 000 – 17 737 777
36	17 770 370,	72	17 740 000 – 17 757 777
*37	17 770 374,	76	17 760 000 – 17 777 777

*Can be read or written into, but not used for mapping.

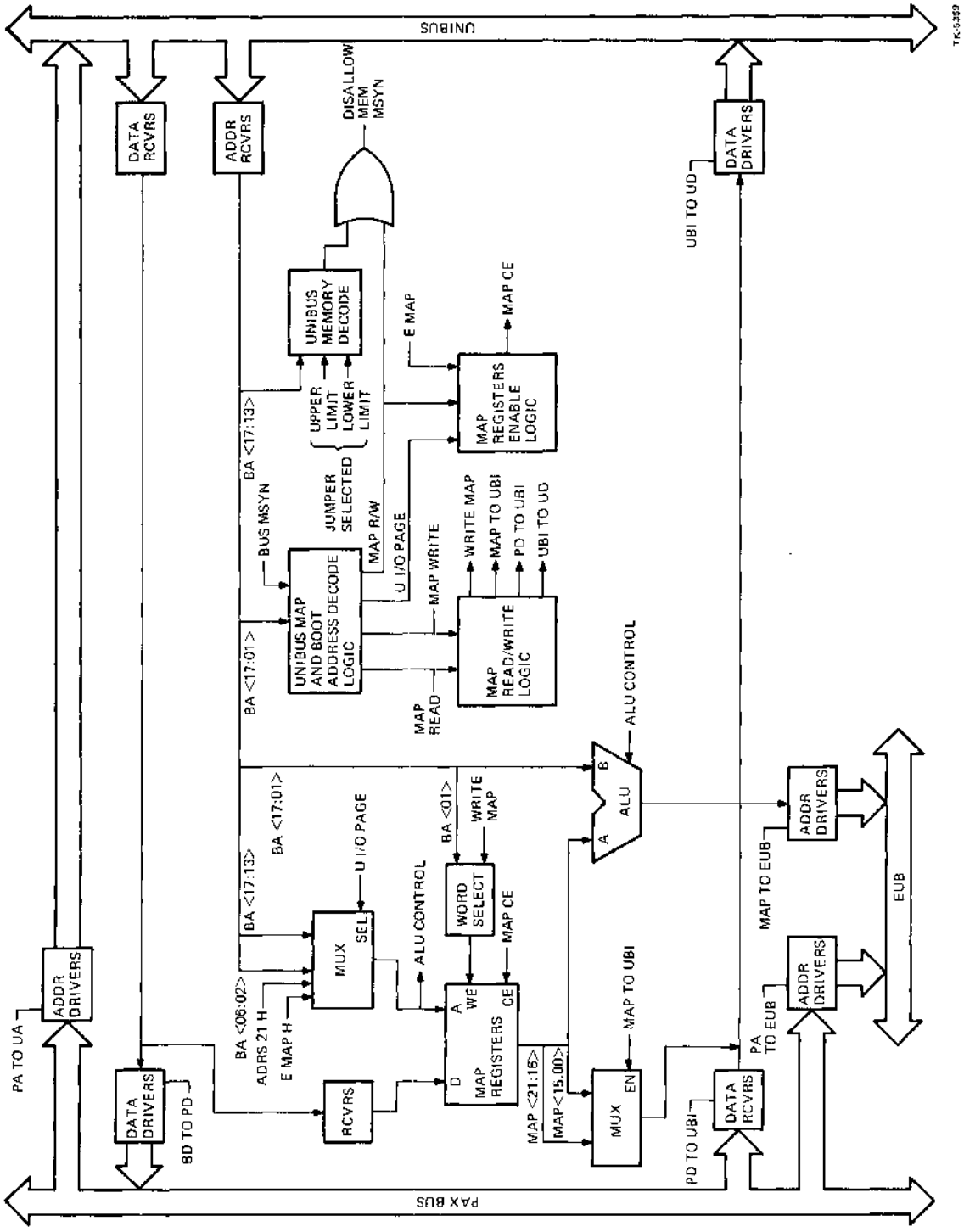


Figure 6-37 UNIBUS Map Block Diagram

The remainder of the map control logic is used to steer the map output to the proper bus during a read operation. Normally PD TO UBI H and PD TO UBI L are asserted and PAX data is passed directly to the UNIBUS drivers. For a map read operation, these signals are negated and MAP TO UBI L is asserted and causes the output of the map registers to be passed to the UNIBUS drivers.

6.9.2 Map Addressing and Relocation

Relocation expands the 18-bit UNIBUS address to the 22-bit main memory address. This allows the UNIBUS to access any location in main memory. This relocation or mapping of addresses is done by adding the contents of one of the mapping registers to bits (12:01) of the incoming UNIBUS address.

All mapping registers in the UNIBUS map are 21 bits wide. A 22nd bit, which is not writeable and is always read as zero, acts as the lowest-order bit for each register. Each register specifies the 21-bit PA of a 4K page residing on any word boundary in memory. The reason for using word boundaries is that the mapping logic does not know if a byte operation is being executed, and if so, what byte is required.

Figure 6-38 illustrates the construction of a PA by the UNIBUS map. Bits (17:13) of the 18-bit UNIBUS address select a map register. The remaining bits (12:00) of the UNIBUS address are used as an offset into the page to which the mapping register is pointing.

When an address is taken off the UNIBUS, the mapping register is automatically selected and the contents read out. That 21-bit address is added to the 12-bit offset in the UNIBUS address to form the PA. This mapping function is very similar to that performed by memory management.

The program controls this process both by selecting the contents of the mapping registers and by its ability to enable and disable the UNIBUS map relocation function.

The UNIBUS map is enabled by the assertion of E MAP H (bit 5 of SR3). The UNIBUS address lines BA (17:00) are received by the map logic. BA 17:13 are selected by the map address multiplexer (E35, 55) to generate the address, RAM A 4:0, to the map registers. The output of the selected register, MAP 21:01 H, is sent to the adder, which is made up of ALUs E35, E46, E33, E44, E37 and carry generators E26, where it is added to BA 12:01 to create MA 21:01. The output of the ALUs, MA 21:01, along with BA 00 and ADRS OUT 21 H, are used to create the PA. These signals are then passed to the memory bus (EUB) via buffers E30, E31, and E43.

When the UNIBUS map is disabled, bits 21:18 of the PA are set to 0 and BA 17:00 are used for bits 17:00 of the PA. This allows the UNIBUS to access the first 24K of main memory.

When a peripherals page address (17 760 000 – 17 777 777) is decoded by the map, U I/O PAGE L is asserted. U I/O PAGE L being asserted forces bits 21:13 of the PA to be set to ones and BA 12:00 are used for bits 12:00 of the PA. This action forces a reference to the upper 4K of physical memory.

6.9.3 Addressing Limits

There are 31 mapping registers which can be accessed by the UNIBUS for relocation. The actual number is determined by two sets of five jumpers (K4-4) which are used to set the upper limit (W3-W7) and the lower limit (W18-W12).

The lower limit jumpers are used to select the first address that will not be mapped to main memory starting at UNIBUS address 0 up to the lower limit. The lower limit allows the UNIBUS space that will be mapped to main memory to be expanded upward from UNIBUS address 0 up to 760 000 in 4K word segments.

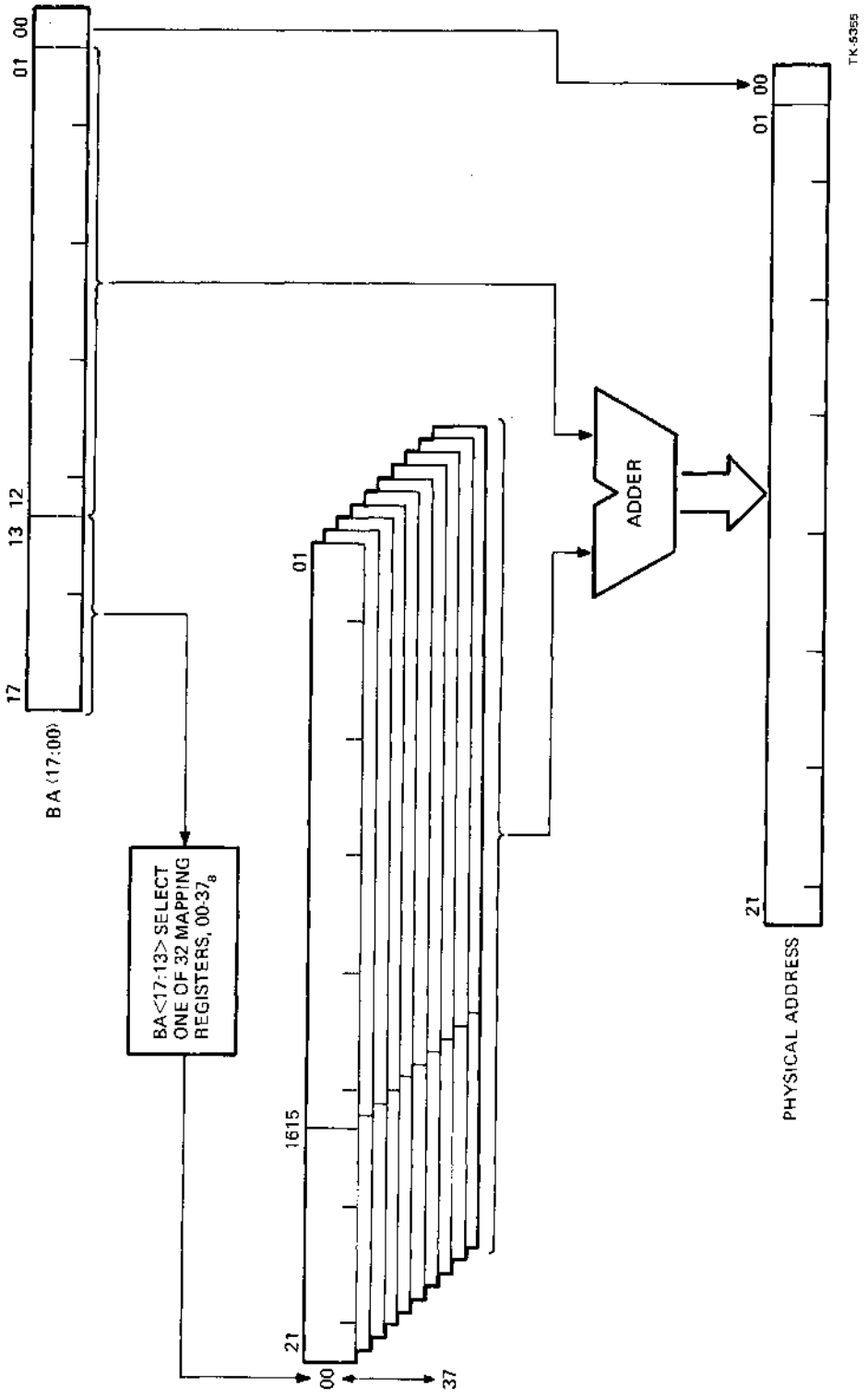


Figure 6-38 Construction of the PA

The upper limit jumpers are used to select the first address that will not be mapped to main memory starting at UNIBUS address 757 776 down to the upper limit. The upper limit allows the UNIBUS space that will be mapped to main memory to be expanded downward from UNIBUS address 760 000 in 4K word segments.

Figure 6-39 shows how the addressing limits affect UNIBUS space. When the upper and lower limits are set to address 0 (0K) or 760 000 (124K) or if the limits overlap (that is, lower limit = 400 000 (64K), upper limit = 417 776 (68K)) all of the UNIBUS space, with the exception of the I/O page, will be passed to main memory.

NOTE

For CPU diagnostics to run properly it is necessary to set both the upper and lower limits to UNIBUS address 0 or 760 000.

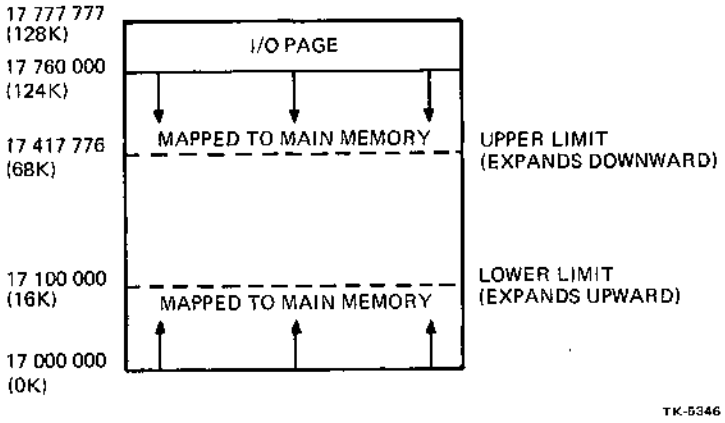


Figure 6-39 UNIBUS Map Addressing Limits

6.10 CONSOLE PROCESSOR

The console processor consists of an 8085 microprocessor and associated logic. The console processor, in conjunction with the console terminal, is used to interpret ASCII characters so they can perform the equivalent functions of the "lights and switches" console of earlier processors.

The console terminal (the LA120 or equivalent used for the system console/programmer console) can be operated in one of two modes.

1. Console Mode – the console is used to perform such functions as: start, halt, deposit, examine, continue, etc. The operation of the console is controlled by the 8085 microprocessor.

2. Program I/O Mode – the console functions as the system console and is controlled by the operating system of the CPU.

For an explanation of the console commands refer to Chapter 2.

Figure 6-40 is a block diagram that shows the addressing and data flow of the console processor.

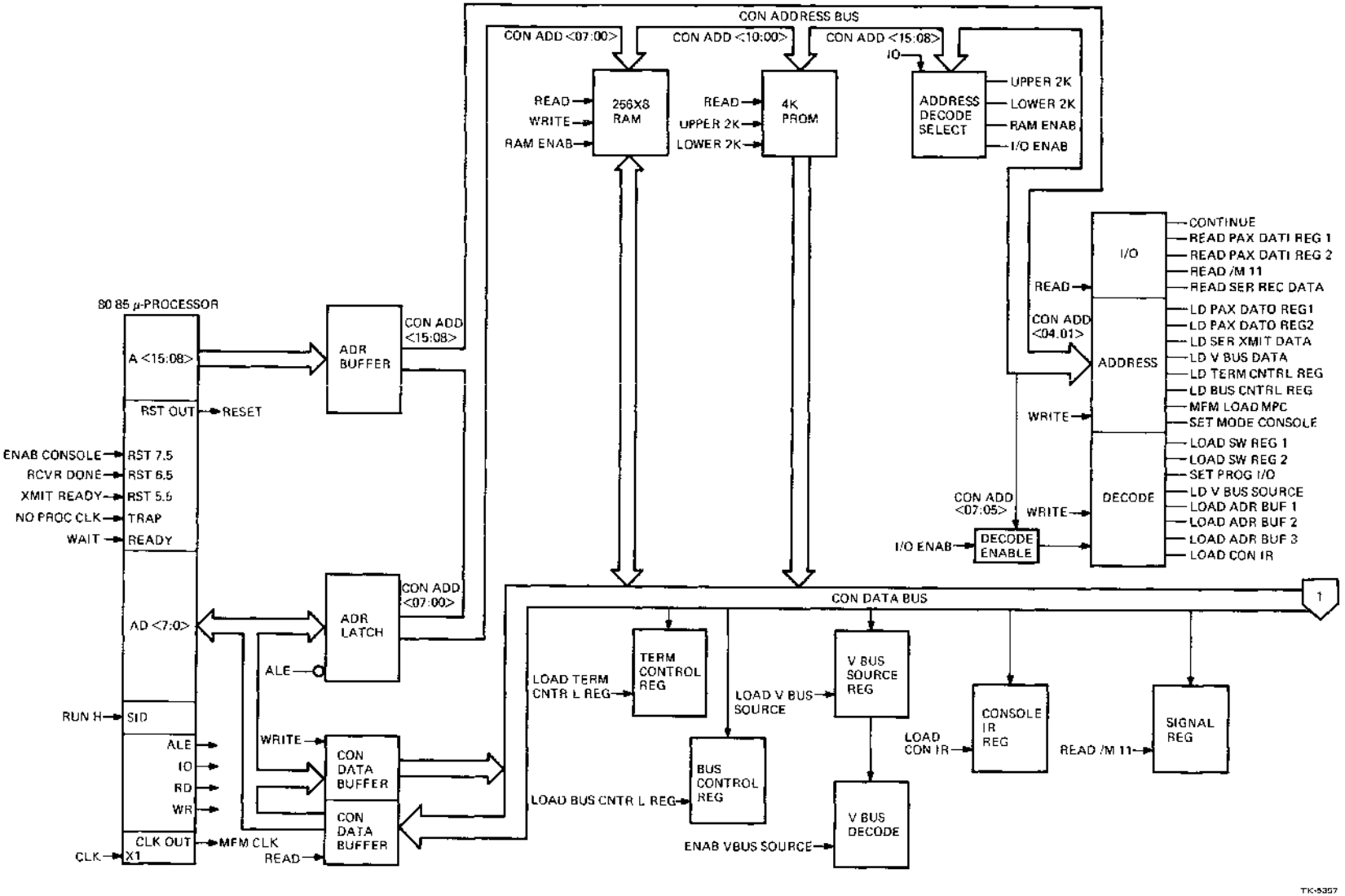


Figure 6-40 Console Processor Block Diagram (Sheet 1 of 2)

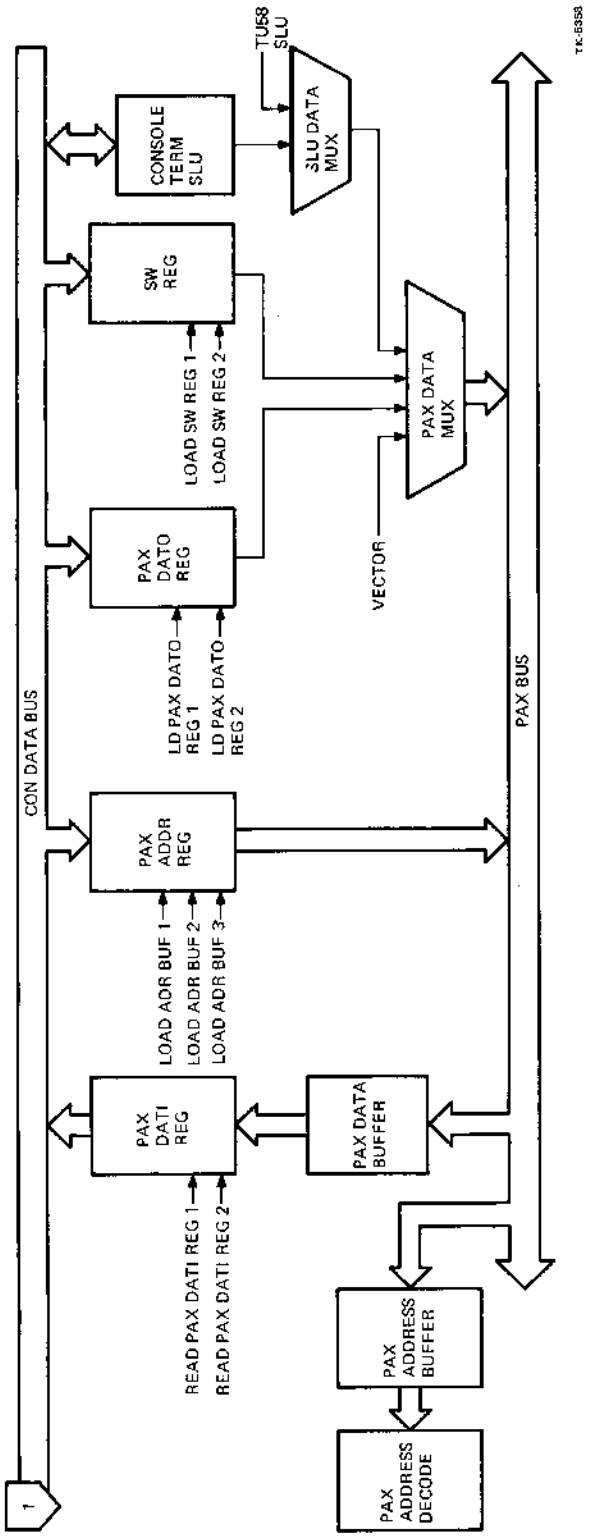


Figure 6-40 Consolc Processor Block Diagram (Sheet 2 of 2)

6.10.1 8085 Addressing

The 8085 microprocessor, as it is used in this application, when addressing a location will do one of two cycles, a read or a write. The 8085 uses a 16-bit address when referencing its program store, random access memory, or I/O locations.

The upper eight bits of the address are direct buffered onto the console address bus. The lower eight bits, because they are multiplexed with data going to or from the 8085, are latched by E123 (K3-2) and then buffered onto the console address bus. the 8085 controls E123 with the address latch enable (ALE) signal.

The following paragraph is an example of an 8085 address as used in the PDP-11/44 console processor.

The upper eight address bits are asserted and buffered onto the console address bus by E127. At the same time the upper eight address bits are asserted, the lower eight bits along with ALE are asserted. After a certain period of time, ALE is negated and AD 07:00 of the 8085 change from address to data lines. A 15:08 and the output of the latch (E123) remain asserted until the beginning of the next address cycle.

When the 8085 asserts an address, the upper eight address bits and the I/O signal from the 8085 are decoded by the address decode select ROM (E126). The address decode select ROM determines whether a program store, RAM, or I/O address has been asserted. The I/O addresses are further decoded by the I/O address decode logic (E100, E102, E103, and E131). The outputs of the I/O address decode logic are used for two different functions:

1. Register load and unload
2. Control functions.

The control functions are implemented by writing to the I/O address that corresponds to the particular function. There is no transfer of data to or from the 8085. Thus, by the 8085 writing to the correct I/O address, the selected control function is implemented. There are five control signals selected by the I/O addresses.

1. SET MODE CONSOLE L – This signal is used to set the console mode flip-flop (K3-6, E62) which enables the console mode operation of the console terminal.

2. Continue – This signal is used to clear the console processor inhibit of the PDP-11/44 CPU clock by initiating a 130-ns continue pulse via one-shot E37 (K3-2). Note that the 8085 has to read from this address, unlike the other four control signals which are written to.

3. SET PROG I/O L – This signal is used to clear the console mode flip-flop (K3-6, E62) and return the console terminal to the program I/O mode.

4. LD VBUS DATA L – This signal enables the selected VBUS source by asserting K3-2 ENAB VBUS SOURCE and then puts the data on the PAX bus. The data on the PAX bus is then trailing-edge clocked into the console's PAX data in register by LD VBUS DATA L.

5. MFM LOAD MPC L – This signal is used to load the next MPC via the console logic. This signal enables the PAX data out multiplexer which puts the data onto the PAX bus. After the data is on the PAX bus it is clocked into the next MPC registers, thereby loading the next MPC.

All other I/O locations addressed by the 8085 involve either the writing or reading of data to or from the console data bus by the 8085.

6.10.2 Console Data Flow

The 8085 microprocessor, as it is used in this application, has only two types of I/O cycles: a read for incoming data and a write for outgoing data. The data going to and coming from the 8085 microprocessor is transferred on the console data bus. Because the number of loads on the console data bus are more than the 8085 can drive, it is necessary to buffer the data entering and leaving the microprocessor via its address/data lines (AD 07:00). Figure 6-40 shows the buffers and the different loads on the console data bus.

When the 8085 is doing a read, it asserts K3-2 READ L (K3-2) which enables the incoming data buffer, E124 (K3-2), and the addressed data source (program store, RAM, I/O locations). The data is read by the 8085 and then K3-2 READ L is negated to complete the read cycle. When the 8085 is going to write data it asserts K3-2 WRITE L which enables the outgoing data buffer and also synchronizes the write operation at the data's destination. When the write cycle is completed (approximately 400 ns), K3-2 WRITE L is negated. The output buffer (E125) is not disabled until 40 ns after K3-2 WRITE L has been negated. This delay is needed to allow for any hold time requirements of the receiving logic. The delay is created by the propagation of K3-2 WRITE L through the gates of E140 (Etch Rev. B - E138) (K3-2) before the output buffer is disabled.

6.10.3 Console-to-PAX Interface

The console-to-PAX interface is the path by which the console processor communicates with the PDP-11/44 processor. The PAX bus is the internal data and address bus of the CPU and is the route by which all information going to or from the PDP-11/44 CPU must pass. The console-to-PAX interface is made up of buffers, registers, and control logic necessary for the console processor to interface with the PAX bus.

The logic for the console-to-PAX interface is located on K3-3 and K3-4 of the print set. The interface consists of an outgoing 24-bit (22-bit address and 2 control bits) PAX address register (E67, E78, E89), an outgoing 16-bit PAX data register (E33, E24), and an incoming 16-bit PAX data register [E56, E42 (Etch Rev. B-E45)]. The control logic consists of flip-flop E110 and gates E12, E13, E15, E130 on K3-3 along with the VBUS and CPU system clock control logic on K3-4. The PDP-11/44 data transfer logic (paragraph 6.5) is used to handle bus arbitration, timing, and detection of data transfer errors. This eliminates the need to duplicate this logic in the console processor.

To understand how the console-to-PAX interface works, an understanding of the various types of deposits and examines, used by the console processor, is needed. (For an explanation of the console commands, refer to paragraph 2.2.) An examine (E) command from the console is executed as follows.

1. Load data out registers with next MPC for MFM data in.
2. Load next MPC register in CPU.
3. Load the outgoing PAX address registers with the address to be examined.
4. Start the CPU clock to do the data transfer.
5. Read PAX DATI register.
6. Check for a transfer error by checking the CPU error register.
7. Convert binary data to ASCII and send to console terminal.

A deposit (D) command is similar to an examine command except that a different MPC is loaded into the CPU and the data to be deposited is loaded into the data out registers. A deposit (D) command from the console is executed as follows.

1. Load data out registers with next MPC for MFM data out.
2. Load next MPC register in CPU.
3. Load outgoing PAX address registers with location of where data is to be deposited.
4. Load data out registers with data.
5. Start CPU clock to do data transfer.
6. Check CPU error register for data transfer error.

A more detailed explanation of how an examine and deposit command functions is contained in the next section, paragraph 6.10.4, Operation During Command Execution.

6.10.4 Operation During Command Execution

The operation of the console processor during command execution is a function of the software contained in the console processor's program store. When doing any type of function that requires the transfer of data to or from the console, some of the control for the data transfer is handled by the CPU data transfer logic. During command execution, the console processor controls the manipulation of data within itself, direct communication with the console terminal, control of the CPU clock and the loading of the next MPC, if required.

A detailed explanation of a deposit command (D) best explains how the console processor functions during command execution.

Deposit 5 into location 1000. This is entered at the console terminal as follows:

D⟨SP⟩ 1000⟨SP⟩5 ⟨CR⟩

The carriage return ⟨CR⟩ at the end of the command tells the console processor that the command is complete and execution can start. The console processor first determines that a deposit is to be done and then converts the address and data from ASCII to binary format and stores this information in RAM. After this conversion is done, the command execution begins. First the console processor selects an internal constant which will be used as the next MPC value in the CPU. When doing a deposit this constant designates that an MFM data out is going to be done by the CPU. The console processor then loads this constant into the PAX DATO registers in two write cycles by the 8085 microprocessor. MFM LOAD MPC L (K3-2) is then asserted by the 8085 to put the MPC value on the PAX bus and clock it into the next MPC registers in the CPU. After the MPC is loaded into the CPU, the console processor sets up for the deposit by loading the PAX ADR registers (three write cycles by 8085) with the address where the data is to be deposited and the PAX DATO registers (two write cycles by 8085) with the data. The console processor also asserts FREE BUS H. This signal puts the PAX bus into a high impedance state and prevents any conflicting data from being on the bus when the transfer begins.

When the setup is complete the console processor is ready to let the CPU take control of the data transfer. This is accomplished by the console processor setting the XFER DONE bit and the WAIT bit in the CON IR (K3-4 E90). By setting the WAIT bit, one-shot E35 is triggered and asserts K3-4 WAIT H which triggers one-shot E37 (K3-2) to start the CPU clock by asserting K3-2 CONTINUE L. The CPU now takes control of the transfer; this is done by the control logic on K3-3 (Figure 6-41). When the CPU clock starts running, TRAN TO MFM L is asserted and direct sets flip-flop E110 as soon as CPU ENAB ADRS H is asserted by the data transfer Logic (K4-1), approximately 60 ns after the clock starts. The PAX address buffers are enabled by E110, when it is set, and put the address on the PAX bus. A short time after CPU ENAB ADRS H is asserted, CPU DATO L is asserted, CPU DATO L is ANDed with TRAN TO MFM L to assert ENAB DATA L. When ENAB DATA L is asserted, the contents of the PAX DATO registers are put on the PAX bus and deposited in the addressed location. When the transfer is complete, TRAN TO MFM L is negated and END TRAN L is asserted. END TRAN L is ANDed with the output of E110 to clear the CON IR and then clocks E110 to clear the flip-flop. Clearing the CON IR clears the wait one-shot and restarts the 8085. Also, at the end of the transfer, the CPU halts and returns control of the CPU clock to the console processor.

When the transfer is completed the console processor checks the CPU error register to see if there was a transfer error. If a transfer error has occurred and the transfer is not completed, the console processor does not know until it checks the CPU error register. This is because the WAIT one-shot will timeout and restart the 8085 in 220 ms if the CPU has not asserted END TRAN L before the one-shot times out.

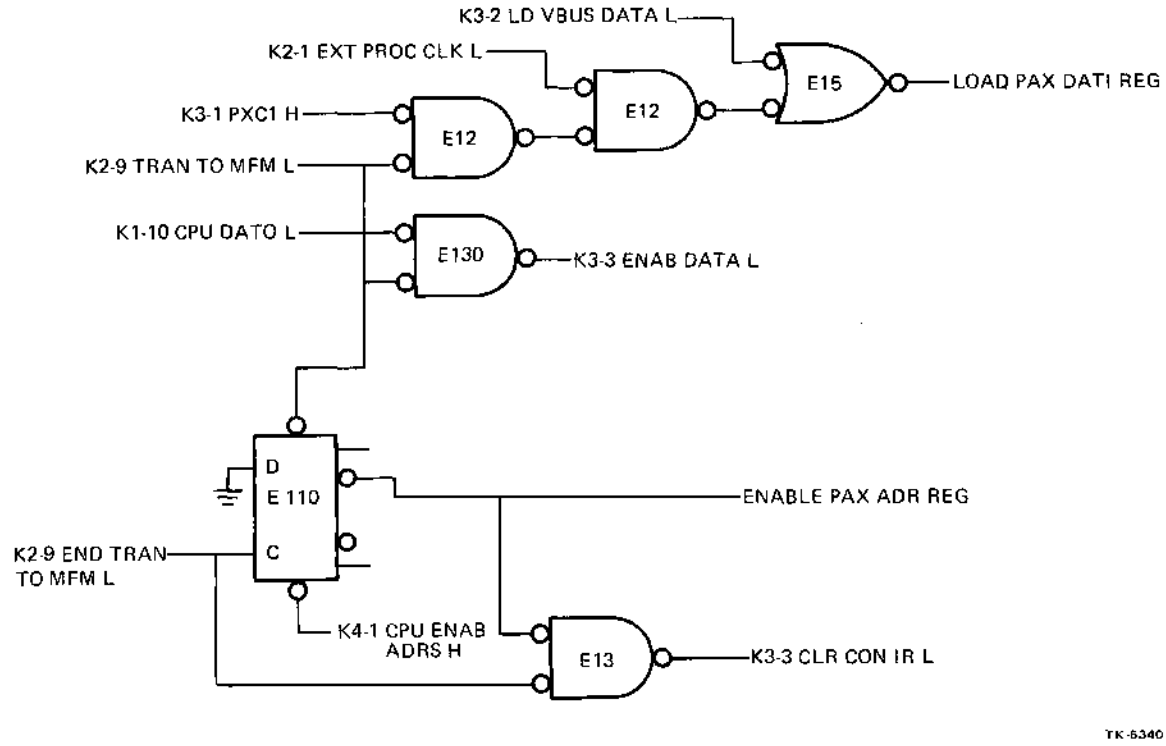


Figure 6-41 Console Processor to PAX, Interface Control Logic

An examine command is similar to a deposit except that there is no data that needs to be loaded into the PAX DATO registers after the MPC constant for an examine has been loaded. Gates E12, E15, and EXT PROC CLK L (Figure 6-41) are used to clock the incoming data into the PAX DATI registers. The console processor, after checking for a transfer error, converts the data and address from binary to ASCII and puts the information out on the console terminal. Note that when examining one of the machine registers it is not necessary to load the PAX address registers because the VBUS register (K3-4, E122, E121) is used to select the source register in the CPU.

For a complete listing of the console commands and their functions refer to paragraph 2.2.

6.11 SERIAL LINE UNITS

The multifunction module (MFM) contains two serial line units (SLUs): a console terminal SLU and a TU58 SLU. The following paragraphs describe each unit separately, except where areas of logic are shared (for example, address and interrupt logic).

6.11.1 Console Terminal SLU

The console terminal SLU (Figure 6-42) provides the I/O port for an LA36 or LA120 serial terminal or equivalent. The console terminal operates in two modes: as the standard system terminal (program I/O mode) or as a programmer's console (console mode). In console mode, the terminal is used in conjunction with the 8085 microprocessor to functionally replace the switch register and light display of the traditional control panel. In this mode, all characters input on the terminal are interpreted as commands to the processor control section or as commands to verify and control the console logic.

In either console or program mode, the console terminal SLU enables the transfer of data between the console processor or CPU (parallel data) and the external terminal (serial data). The major functional area of this unit is a universal asynchronous receiver/transmitter (UART).

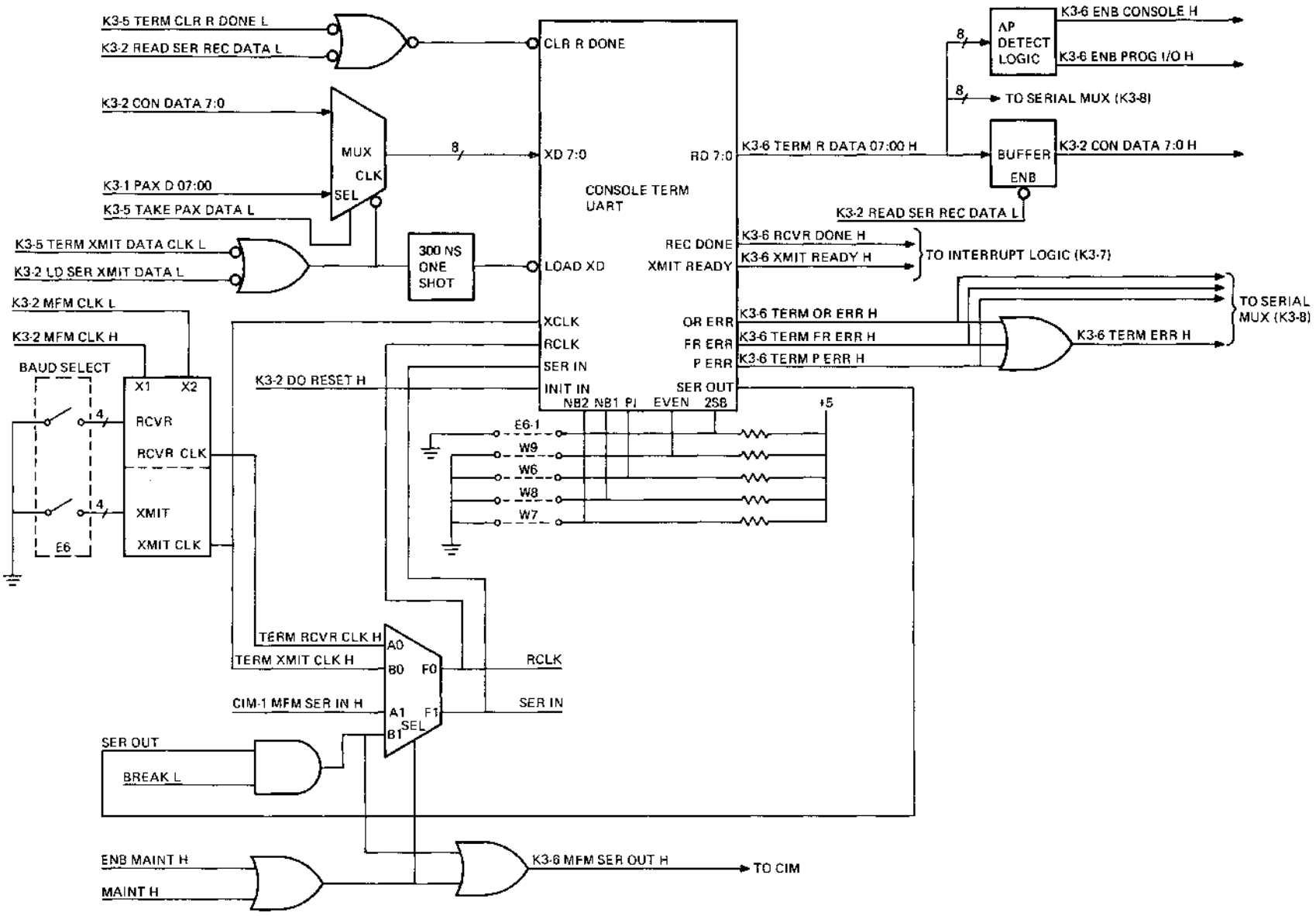


Figure 6-42 Console Terminal SLU

6.11.1.1 Transmitter Operation (Terminal UART) – Parallel data to be transmitted from the processor to the terminal is input to the UART transmit data lines (XD 7:0). The source for the transmit data is a multiplexer which selects either the console data bus (K3-2 CON DATA 7:0) or the PAX data bus (K3-1 PX D 07:00). This multiplexer is clocked under two circumstances:

1. when the central processor performs a DATO operation to the terminal transmitter buffer via the PAX data bus (K3-5 TERM XMIT DATA CLK L is generated), or

2. when the console processor writes data to the terminal via the console data bus (K3-2 LD SER XMIT DATA L is generated).

In both circumstances, the signal that clocks the multiplexer also triggers a 300-ns one-shot which generates the data strobe (K3-6 LD XD L) signal on the UART. The 300-ns one-shot keeps the load signal low for the time period required by the UART transmitter. The parallel-loaded character is converted by the UART to serial data and is output through the SER OUT line of the UART. When the transmitter buffer is emptied, the UART generates the transmit ready line (K3-6 XMIT READY H) indicating a new character can be loaded. The format of the serial character is determined by control inputs to the UART. These inputs can be enabled or disabled by the following jumpers and switch:

Jumper/Switch	**Function**
Jumpers W7 and W8	These jumpers specify the character length as follows:

	5 Bits	**6 Bits**	**7 Bits**	**8 Bits**
W7	In	In	Out	Out
W8	In	Out	In	Out

Jumper W6	Parity is generated and detected when this jumper is in.
Jumper W9	Odd/even parity select. When this jumper and W6 are in, odd parity will be generated and checked.
Switch E6 – Position 1	Stop bit select. This switch position is on for 1 stop bit and off for 2 stop bits. This position is also off for 1.5 stop bits if a 5-bit character length has been selected.

The serial character (K3-6 MFM SER OUT H) is transferred from the MFM to the console interface module (CIM) where it can be output to the terminal. The rate at which the character bits are transmitted (baud rate) is switch selectable. Refer to paragraph 6.11.1.3.

6.11.1.2 Receiver Operation (Terminal UART) – The receiver section of the UART accepts a serial character from terminal for conversion to parallel data. The receiver samples the serial input line (SER IN) at selected edges of the receiver clock (RCLK). The source of data for the serial input line is a multiplexer. During normal operation, the multiplexer selects serial data from the console interface module (CIM–1 MFM SER IN H). In maintenance mode, the multiplexer selects the SER OUT line of the UART. This enables the closed-loop test of the receiver and transmitter.

The receiver enters the data entry state when it detects a mark-to-space (high to low) transition of the serial input line. If the receiver control logic has been set up to detect parity (jumper W6 IN), the receiver checks the parity of the data bits plus the parity bit following the data bits. The receiver compares the parity of these lines with the parity select line (pin 39 of the UART). If the parity of the received character differs from the parity of the UART control logic, the parity error line (K3-6 TERM P ERR H) is asserted and bit 12 of the terminal receiver buffer register is set.

The receiver samples the first stop bit which occurs after the parity bit or after the data bits if no parity is selected. If the stop bit or bits are valid, it indicates that the entire character has been received and shifted into the receiver shift register. The receiver then parallel transfers the contents of the shift register into the receiver data holding register, and sets the data available line (K3-6 RCVR DONE H).

If the receiver samples the first stop bit and it is low, this indicates an invalid stop code. The UART will then generate a framing error signal (K3-6 TERM FR ERR H) which sets bit 13 of the terminal receiver buffer register.

In addition to the parity error and framing error conditions, a third error condition (overrun) is associated with receiver operation. The overrun condition indicates that a new character is being loaded into the UART before the previous character has been read. Under these circumstances, the UART generates K3-6 TERM OR ERR H which sets bit 14 of the terminal receiver buffer register.

The serial character received is converted by the UART to parallel data (K3-6 TERM R DATA 07:00). The central processor can read this data by reading the terminal receiver buffer register. The console processor can read the parallel data via the console data bus (K3-2 CON DATA 07:00 H). Also, the character is decoded to determine if it is the console break character (ASCII ^P). If the character is decoded as ^P (020_8 or 220_8), the console terminal enters console mode.

6.11.1.3 Console Terminal Baud Rate Logic – The baud rates for the console terminal receiver and transmitter are derived from a 5.52960 MHz master oscillator and frequency divider circuits. The oscillator drives the internal clock generator of the 8085 microprocessor (K3-2). The clock output of the 8085 is used to generate two timing signals (K3-2 MFM CLK H and K3-2 MFM CLK L) which are used as the clock inputs of the frequency dividers.

The frequency divide circuits have switch-selectable inputs which determine the receiver and terminal clock frequencies and the corresponding baud rate of each. Table 3-14 lists the switch settings and resulting baud rates.

NOTE
The frequencies required by the UART are 16 times the desired baud rate.

The clock outputs of the two frequency dividers (K3-6 TERM RCLK H and K3-6 TERM XCLK H) are input to a multiplexer. In the normal mode of operation, K3-6 TERM RCLK H is fed into the receiver clock input of the UART and K3-6 TERM XCLK H is fed into the transmitter clock input. In maintenance mode, the multiplexer is selected so that K3-6 TERM XCLK H is fed into both the receiver and transmitter inputs of the UART, thereby ensuring the same baud rate for both.

6.11.2 TU58 SLU

The TU58 SLU (Figure 6-43) provides the I/O port for the TU58 tape unit. Operation of this serial line unit is very similar to that of the console terminal SLU. Serial data transferred to and from the TU58 is converted to parallel data for the central processor. As in the console terminal SLU, the major functional unit is the UART.

6.11.2.1 Transmitter Operation (TU58 UART) – Parallel data from the processor (K3-1 PX D07:00) is loaded into the UART transmitter when the processor performs a DATO to the TU58 transmitter buffer. The address logic generates K3-5 TU58 XBUF WRITE L which triggers a 300-ns one-shot. The output of the one-shot clocks the PAX data latch and keeps the data strobe (K3-7 LD XD TU58 L) low for the time period required by the UART transmitter.

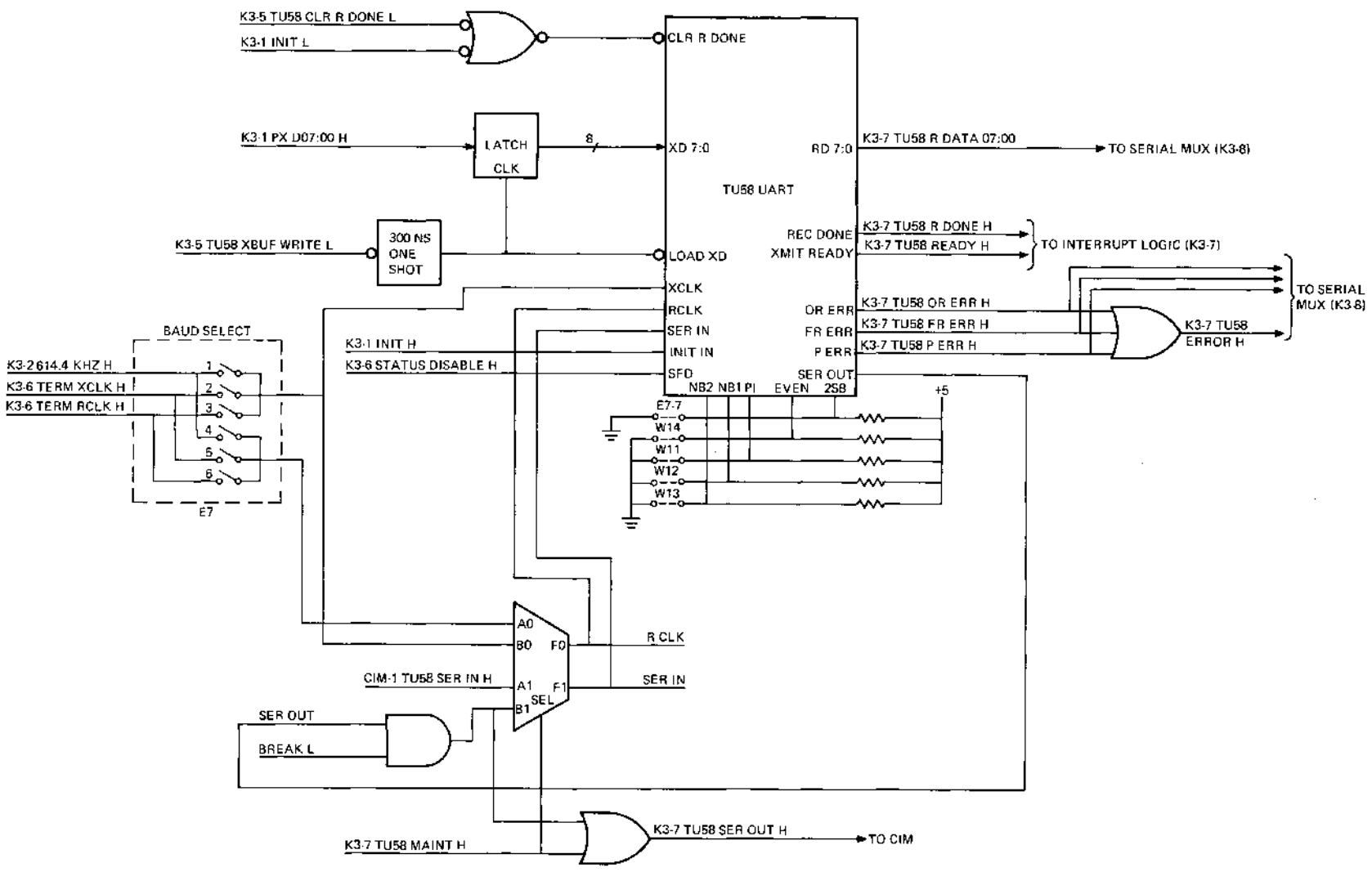


Figure 6-43 TU58 SLU

The parallel data loaded from the PAX data bus is converted by the UART to serial data and transmitted through the SER OUT line of the UART. The serial data (K3-7 TU58 SER OUT H) is transferred from the MFM to the console interface module where it is output to the TU58. The format of the serial data is determined by control inputs to the TU58 UART, which are jumper and switch selectable. The following describes the function of the associated jumpers and switch.

Jumper/Switch	**Function**
Jumpers W12 and W13	These jumpers specify the character length as follows:

	5 Bits	**6 Bits**	**7 Bits**	**8 Bits**
W12	In	In	Out	Out
W13	In	Out	In	Out

Jumper W11	Parity is generated and detected when this jumper is in.
Jumper W14	Odd/even parity select. When this jumper and W11 are in, odd parity will be generated and checked.
Switch E7 – Position 7	Stop bit select. This switch position is on for 1 stop bit and off for 2 stop bits. This position is also off for 1.5 stop bits if a 5-bit character length has been selected.

6.11.2.2 Receiver Operation (TU58 UART) – The receiver accepts serial data TU58 (CIM–1 TU58 SER IN H) from the console interface module. During normal operations the serial TU58 data is selected by a multiplexer as the SER IN source of the UART. In maintenance mode, the multiplexer selects the SER OUT line of the UART as the SER IN source.

The receiver samples the serial input line and enters the data entry state when it detects a mark to space (high to low) transition. If parity detection has been enabled (jumper W11 in), the receiver checks the parity of the data bits plus the parity bit following the data bits. If the checked parity differs from the expected parity, the UART generates K3-7 TU58 P ERR H which sets bit 12 of the TU58 receiver buffer register.

If the receiver samples the stop code and it is valid, the entire character is shifted into the receiver shift register. The receiver then parallel transfers the contents of the shift register into the receiver data holding register, and sets the data available line (K3-7 TU58 R DONE H).

A framing error signal (K3-7 TU58 FR ERR H) is generated if the receiver detects an invalid stop code. This sets bit 13 of the TU58 receiver buffer register. An overrun error signal (K3-7 TU58 OR ERR H) is generated if a new character is being loaded into the UART before the previous character is read.

The serial data received from the TU58 is converted by the UART to parallel data (K3-7 TU58 R DATA 07:00). The central processor can read this data by reading the TU58 receiver buffer register.

6.11.2.3 TU58 Baud Rate Logic – The baud rate for the TU58 receiver and transmitter is derived from a 5.52960 MHz master oscillator and a synchronous counter. The oscillator output is fed into the clock input of the counter. The counter generates K3-2 614.4 KHz H (38.4K baud) which can be selected as the source for the receiver clock and transmitter clock.

K3-2 614.4 KHz H also supplies the input to a divide-by-four counter which generates K3-7 153.6 KHz H (9.6K baud) which can be selected as the source for the receiver clock and the transmitter clock. Note that the frequency used by the UART is 16 times the selected baud rate.

The source for the TU58 baud rate is switch selectable for both the receiver and transmitter. In addition to the standard 38.4K baud and 9.6K baud rates and the console terminal receiver rate can be selected as the source. Table 6-6 lists the switch settings for the possible TU58 baud rates.

Table 6-6 TU58 Baud Rate Selection

Receiver Switch Locations Transmitter Switch Locations	Switch E7 (K3-7) 1 4	 2 5	 3 6
Baud Rate			
38,400	On	Off	Off
9,600	Off	On	Off
Console Terminal Receiver Baud Rate	Off	Off	On

NOTE: Switch positions E7-1 through E7-6 should not be set up in any combination other than those shown in Table 6-6. The baud rate sources for the transmitter and receiver do not have to be the same.

6.11.3 Address Selection

The address selection logic (Figure 6-44) is shared by the console terminal SLU and the TU58 SLU. The PAX address and control lines (PX A21:00, PX C1:C0) are decoded to determine which of nine SLU registers is to be read or written from the central processor. Bit descriptions of each register are provided in paragraph 6.11.4. The address of the console terminal registers and line clock register are fixed as follows.

Address	Console Terminal Register
17777560	Terminal Receiver Status Register
17777562	Terminal Receiver Buffer Register
17777564	Terminal Transmitter Status Register
17777566	Terminal Transmitter Buffer Register
17777546	Line Clock Status Register

NOTE

The console terminal registers can be disabled by removing jumper W1 (K3-5). The line clock register can be disabled by removing jumper W2 (K3-5).

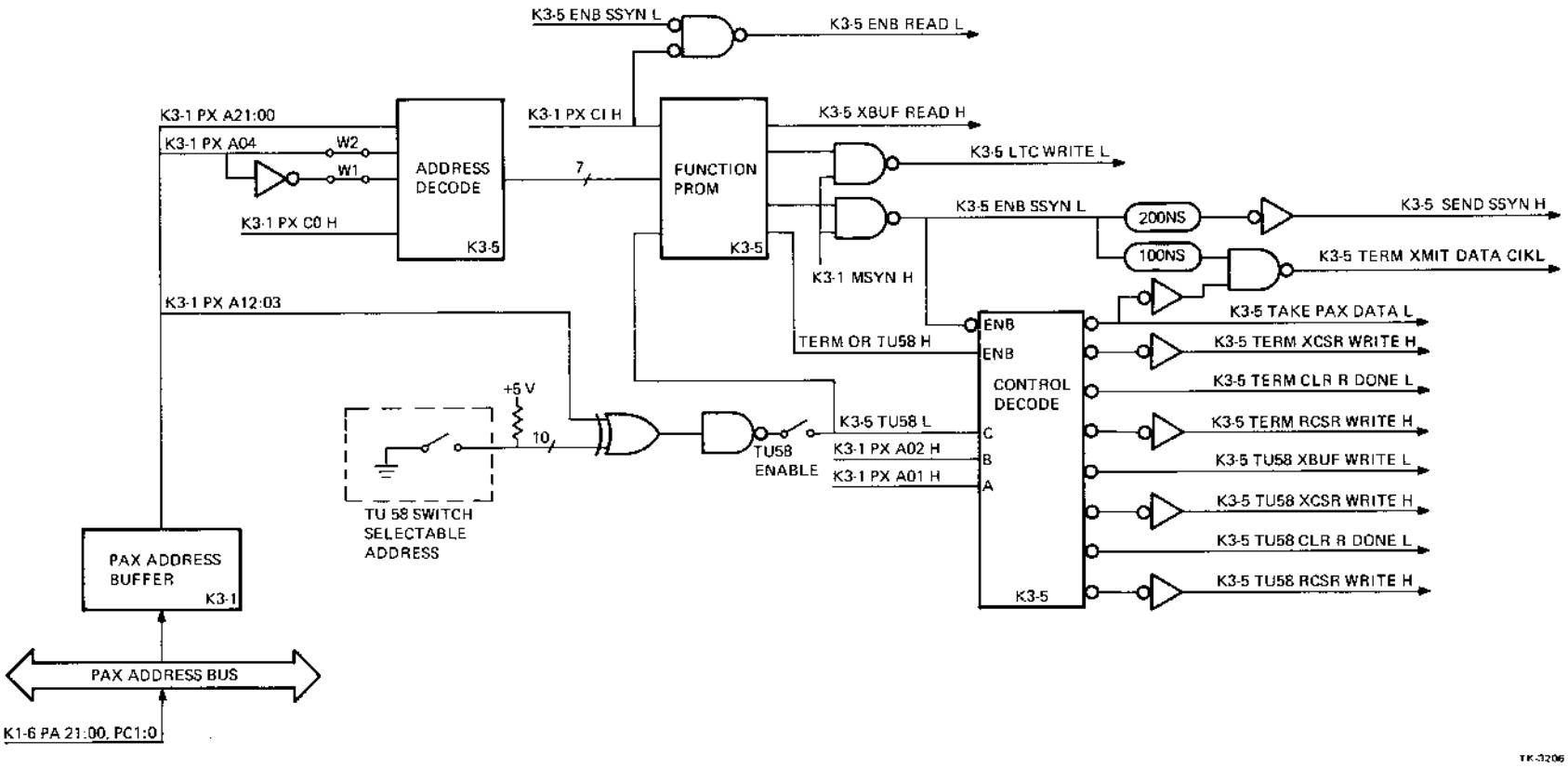


Figure 6-44 Address Selection Logic

The base address of the TU58 registers is switch selectable and falls within the range of 17760000 to 17777770. The base address corresponds to the TU58 receiver status register. The following shows the TU58 register addresses with respect to the selectable base address.

NOTE
Bits 3 through 12 are switch selectable.

Address	TU58 Register
177XXXX0	TU58 Receiver Status Register
177XXXX2	TU58 Receiver Buffer Register
177XXXX4	TU58 Transmitter Status Register
177XXXX6	TU58 Transmitter Buffer Register

The format of the address lines is shown in Figure 6-45. Address lines PX A21:13 must be all ones. This specifies an address within the top 4K address space which is dedicated to device registers. If the first five octal digits of the address are decoded as 1777756X, a terminal register has been selected for the operation. The final octal digit (address line PX A02, PX A01, PX A00) determines which register has been selected and whether a word or byte operation is to be performed. The line clock register is selected if address 17777546 is decoded.

Address lines PX A12:A03 are switch selectable for the TU58 base address. The switches are configured with exclusive OR gates so that when the switch is closed, it will match a one (high) on the associated address line. A match of all the address lines will generate the control line K3-5 TU58 L. This control line can be enabled or disabled by a switch (E79-1). When this switch is closed, the TU58 address decode is enabled. Address lines PX A02:A01 select one of the four TU58 registers.

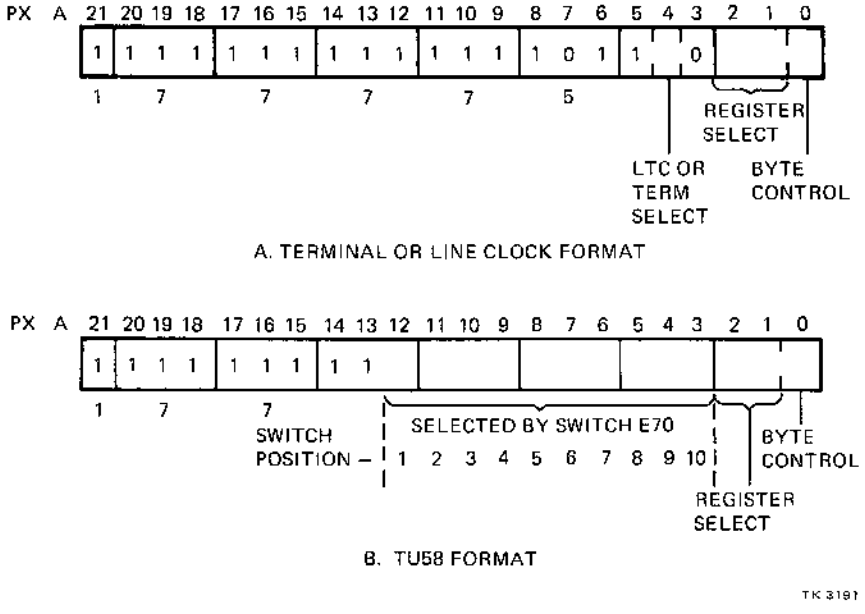


Figure 6-45 SLU Address Format

Three additional lines are input to the address decode logic: K3-1 MSYN H, K3-1 PX C1 H, and K3-1 PX C0 H. The master synchronization line (MSYN) indicates that the processor is bus master and enables the address control lines. The C1 and C0 lines determine the type of operation to be performed:

C1	C0	Type of data transfer
0	0	DATI
0	1	DATIP
1	0	DATO
1	1	DATOB

The address selection logic generates a number of control signals which affect the SLU registers. The following provides a brief description of each signal.

Control Signal	Destination	Function
K3-5 ENAB READ L	K3-8	Selects the serial data input to the PAX data multiplexer. This allows one of the terminal or TU58 registers to be read onto the PAX data bus.
K3-5 XBUF READ H	K3-8	Disables the multiplexers so that all zeros will be read when a DATI or DATIP is performed on the terminal transmitter buffer register.
K3-5 LTC WRITE L	K3-8	Clocks PAX data bit 06 into the LTC interrupt enable flip-flop, and clocks data bit 7 (only when zero) into the line clock monitor flip-flop.
K3-5 TERM XMIT DATA CLK L	K3-6	This signal is a 100-ns low pulse which is used to clock the terminal transmitter data multiplexer and the terminal UART transmitter buffer.
K3-5 TAKE PAX DATA L	K3-6	Selects the PAX data input to the terminal transmitter data multiplexer.
K3-5 SEND SSYN H	K3-1	Returns PAX SSYN to the processor on a valid address selection.
K3-5 TERM XCSR WRITE H	K3-6	Clocks PAX data bits 06, 02, and 00 into terminal transmitter status register bits 06, 02, and 00, respectively.
K3-5 TERM CLR R DONE L	K3-6, K3-8	Generated when the terminal receiver buffer register is read, indicating that a new character may be loaded into the receiver. This signal generates CLR R DONE on the terminal UART and also enables the terminal error bits to be read as bits 15:12 of the terminal receiver buffer register.

Control Signal	Destination	Function
K3-5 TERM RCSR WRITE H	K3-6	Clocks PAX data bit 06 into terminal receiver status register bit 06.
K3-5 TU58 XBUF WRITE L	K3-7	Clocks PAX data bits 07:00 into the TU58 transmitter buffer register.
K3-5 TU58 XCSR WRITE H	K3-7	Clocks PAX data bits 06, 02, and 00 into the TU58 transmitter status register bits 06, 02, and 00, respectively.
K3-5 TU58 CLR R DONE L	K3-7, K3-8	Generated when the TU58 receiver buffer register is addressed, indicating that a new character may be loaded into the receiver. This signal generates CLR R DONE on the TU58 UART and also enables the TU58 error bits to be read as bits 15:12 of the TU58 receiver buffer register.
K3-5 TU58 RCSR WRITE H	K3-7	Clocks PAX data bit 06 into TU58 receiver status register bit 06.

Each of the address control signals are used to read or write bits in the TU58 and terminal registers. The format and bit descriptions of the registers are described in paragraph 6.11.4.

6.11.4 Console Terminal and TU58 Register Descriptions

This section provides the format and bit descriptions of each device register associated with the console terminal and TU58 serial line units and the line clock. Each of these bits are fed into the serial multiplexer (K3-8). The address decode logic controls which SLU register will be selected by the serial multiplexer. The output of the serial line data multiplexer (K3-8 SER D 15:00 H) is fed into the PAX data multiplexer (K3-9). When the address decode logic detects a valid line clock or SLU register address, the serial line data input to the PAX data multiplexer is selected and the PAX data lines (K3-1 PAX D15:00 H) are enabled.

6.11.4.1 Terminal Receiver Status Register – The terminal receiver status register (Figure 6-46) provides two bits which monitor the receiver logic and enable an interrupt sequence.

Each of these bits is described in the following paragraphs.

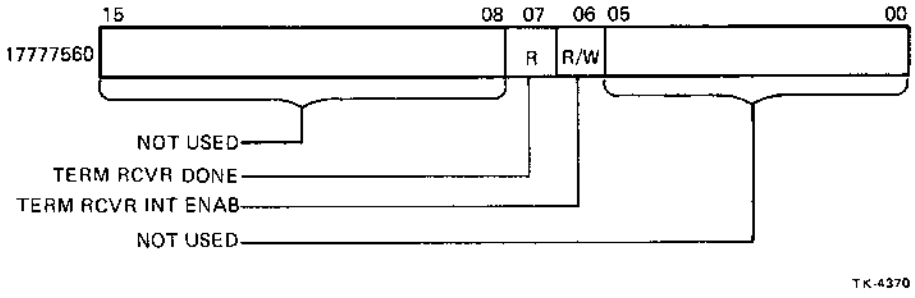


Figure 6-46 Terminal Receiver Status Register

Terminal Receiver Done (Bit 07) – This is a read-only bit which indicates that a full character has been received from the terminal and has been stored in the UART parallel output register. This bit can only be set if the terminal is in program I/O mode. It is inhibited if the character received was an ASCII 020 or 220 (^ P). This character holds the done bit clear and thus prevents further program output.

The done bit is ANDed with the interrupt enable signal (K3-6 TERM REC INT ENA H) to clock the receiver interrupt request flip-flop. Setting of the flip-flop generates K3-6 REQ TERM REC INT H which initiates an interrupt sequence.

This bit is cleared by the signal K3-6 CLR R DONE BUF L which is generated by INIT or by one of the following conditions.

1. The PAX address logic generates K3-5 TERM CLR R DONE L.
2. The console processor address logic generated K3-2 READ SER REC DATA L.

Both conditions indicate that the terminal receiver buffer register was addressed and that a new character may be loaded into the receiver. Either signal will also generate CLR R DONE on the UART.

Terminal Receiver Interrupt Enable (Bit 06) – This is a read/write bit. It enables an interrupt sequence to be initiated when the TERM R DONE bit is set, indicating that a character has been received and is ready for transfer to the PAX data bus. Bit 06 is written when a write operation to the terminal receiver status register is decoded by the address logic. The signal K3-5 TERM RCSR WRITE H clocks PAX data bit 06 (K3-1 PX D06 H) into the interrupt enable flip-flop. This bit is cleared by INIT.

6.11.4.2 Terminal Receiver Buffer Register – The terminal receiver buffer register (Figure 6-47) consists of four error bits and eight data bits associated with the UART receiver.

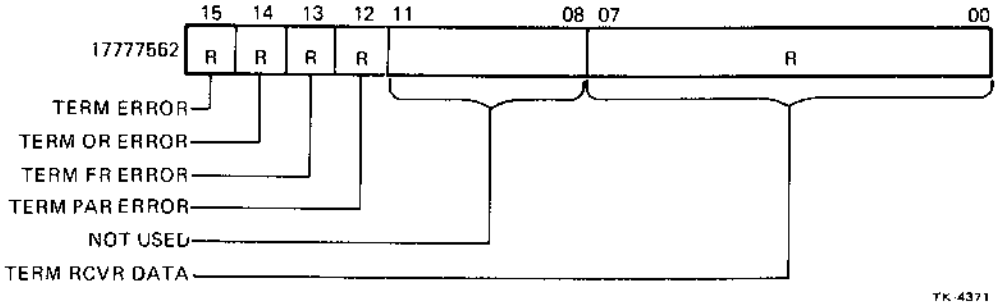


Figure 6-47 Terminal Receiver Buffer Register

Terminal Receiver Error Bits (Bits 15 to 12) – The four error bits of the buffer register are set to indicate improper receiver operation. These bits are read only and can be disabled by removing jumper W4 (shown on print K3-8). Three of the error bits are generated by the UART and the fourth bit (TERM ERROR) is the inclusive-OR of the other three. The error bits are described as follows.

1. Overrun Error (TERM OR ERROR) - Generated by the UART when R DONE was not reset prior to receiving a new character. This indicates that the UART received a new character before the processor read the previous character.

2. Framing Error (TERM FR ERR) – Generated by the UART to indicate that the character read has no stop bit.

3. Parity Error (TERM P ERR) – Generated by the UART to indicate that the parity received does not agree with the parity expected.

4. Terminal Error (TERM ERROR) – Indicates that any one or more of the other three error bits is set.

Each of the error bits is updated when a new character is received. All four bits are cleared on a power-up when DCLO becomes unasserted.

Terminal Receiver Data Bits (Bits 07 to 00) – The receiver buffer is read only and is loaded by the UART. The UART receives the serial data from the terminal, converts it to parallel data and places it on the terminal receiver data lines (K3-6 TERM R DATA 07:00). This data can then be read by the central processor or the console processor.

6.11.4.3 Terminal Transmitter Status Register – The terminal transmitter status register (Figure 6-48) contains both transmitter status information and maintenance information.

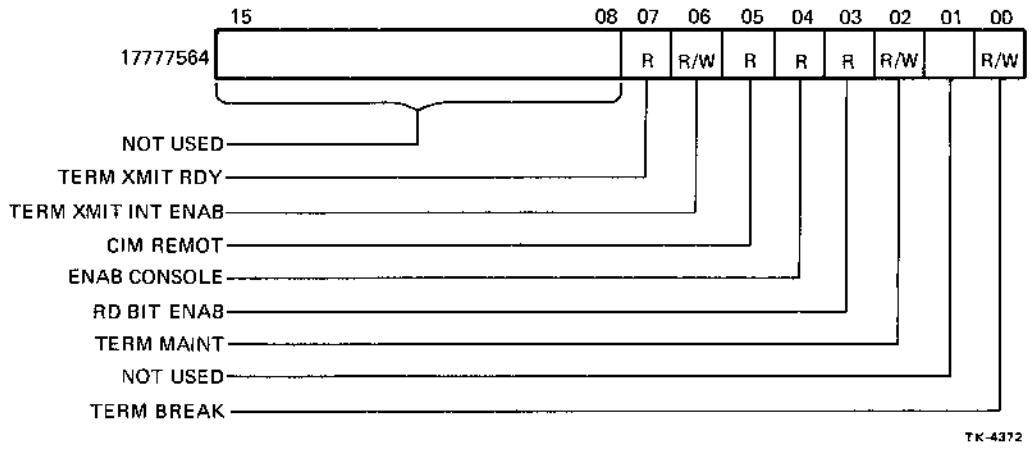


Figure 6-48 Terminal Transmitter Status Register

Terminal Ready (Bit 07) – This is a read-only bit that indicates the terminal transmitter buffer if ready to accept another character from the PAX data bus.

This bit also initiates an interrupt sequence if bit 06 is set. The ready bit is ANDed with the interrupt enable signal (K3-6 TERM XMIT INT ENA H) to clock the transmitter interrupt request flip-flop. Setting of this flip-flop generates K3-6 REQ TERM XMIT INT H which initiates an interrupt sequence.

Bit 07 is set by the initialize signal (K3-1 INIT L) and is the transmitter ready output of the UART, indicating that the transmitter buffer is empty. Terminal ready is cleared by K3-6 LD XD L, which is generated when the transmitter buffer is being loaded with data.

Note that bit 07 can only be set when the terminal is in program I/O mode. If the terminal is in console mode, this bit and the associated interrupt sequence to the processor are inhibited. This enables the console processor to load a character into the transmitter buffer via the console data bus (K3-2 CON DATA 7:0). The signal K3-6 XMIT READY H notifies the console processor that the transmitter buffer is ready.

Terminal Transmitter Interrupt Enable (Bit 06) – This is a read/write bit. Bit 06 enables an interrupt sequence to be initiated when bit 07 (terminal ready) is set, indicating that the terminal transmitter buffer can accept another character. This bit is written when a write operation to the terminal transmitter status register is decoded by the address logic. The signal K3-5 TERM XCSR WRITE H clocks PAX data bit 06 (K3-1 PX D06 H) into the interrupt enable flip-flop. This bit is cleared by INIT.

Console Interface Module Remote (Bit 05) – This bit is read-only and indicates that the system is being operated in the remote diagnosis mode.

Enable Console (Bit 04) – This bit is read-only and indicates that the system terminal is operating in console mode.

Enable Remote Diagnosis Status Bits (Bit 03) – This is a switch-selectable read-only bit. When switch E79-2 is ON (causing bit 03 to be set), bits 05 and 04 are enabled and can be read in the terminal transmitter status register; otherwise these three bits are always zero.

Terminal Maintenance (Bit 02) – This is a read/write bit. When set, a closed loop test of the terminal UART can be performed. The serial output of the transmitter is fed back to the serial input of the receiver. The receiver is forced to run at transmitter speed. This bit is written by clocking PAX data bit 02 (K3-1 PX D02 H) into the TERM MAINT flip-flop. This bit is cleared by INIT and disabled if the terminal is in console mode.

Terminal Break (Bit 00) – This is a read/write bit. When set, a continuous space (low or zero logic level) is transmitted to the terminal. It can be disabled by removing jumper W5. This bit is written by clocking PAX data bit 00 (K3-1 PX D00 H) into the TERM BREAK flip-flop. Bit 00 is cleared by INIT and disabled if the terminal is in console mode.

6.11.4.4 Terminal Transmitter Buffer Register – The terminal transmitter buffer (Figure 6-49) is a write-only register that receives parallel data from the PAX data bus (K3-1 PX D07:00 H) or the console data bus (K3-2 CON DATA 7:0 H).

The parallel data is loaded into the UART for serial conversion and transmission to the terminal. The two data sources for the transmitter buffer are multiplexed. If the signal K3-5 TAKE PAX DATA L is asserted, the PAX data bus is selected as the source.

Two signals can be generated which clock the data from the multiplexer onto the transmit data lines. The signal K3-5 TERM XMIT DATA CLK L is generated by the address decode logic to clock the PAX data lines. The signal K3-2 LD SER XMIT DATA L is generated by the console processor address logic to clock the console data lines. When either of these signals is generated, the resulting clock signal triggers a 300-ns one-shot. The one-shot keeps the data load signal (K3-6 LD XD L) low for the time required by the UART transmitter.

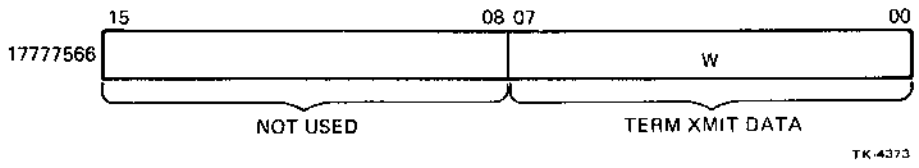


Figure 6-49 Terminal Transmitter Buffer Register

6.11.4.5 Line Clock Status Register – The line clock status register (Figure 6-50) contains two bits associated with line clock operation: an interrupt monitor bit and an interrupt enable bit.

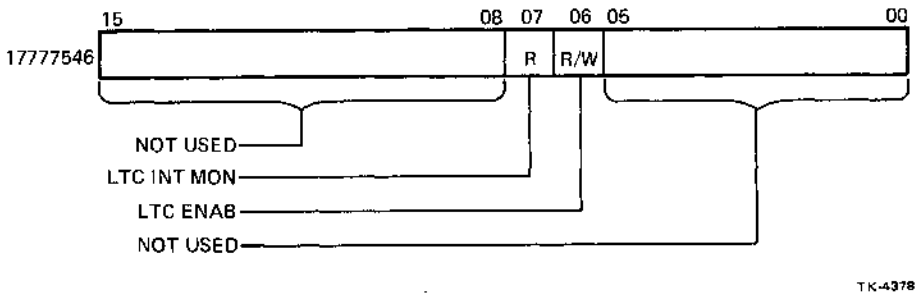


Figure 6-50 Line Clock Status Register

Line Clock Monitor (Bit 07) – This is a read-only bit which provides noninterrupt mode timing information and allows software to measure time intervals.

The LTC interrupt monitor flip-flop is clocked by K3-8 BUS LTC L. This signal is a square wave with the same frequency as the ac power and is generated in the power supply. The line clock monitor bit is set once for each cycle of ac power. The program must clear the bit each time it becomes set, if interrupts are disabled. The program clears the bit by writing the line clock status register with PAX data bit 07 low. This will also disables the line clock interrupt request (K3-8 BR6 REQ L) at the same time if the interrupt has not occurred.

Line Clock Interrupt Enable (Bit 06) – This is a read/write bit which allows the generation of timed interrupt sequences. Interrupt sequences occur at time intervals of 16-2/3 ms (60 Hz) or 20 ms (50 Hz), depending on the frequency of the ac power. This bit is set when the line clock status register is written (K3-5 LTC WRITE L) with PAX data bit 06 high. When bit 06 is set, the direct-clear signal is removed from the interrupt request flip-flop. This enables the interrupt request flip-flop to be set on the next falling edge of K3-8 BUS LTC L. This generates the BR6 interrupt request line and initiates an interrupt sequence.

6.11.4.6 TU58 Receiver Status Register
The TU58 receiver status register (Figure 6-51) provides a receiver done monitor bit and interrupt enable bit for the TU58 receiver logic.

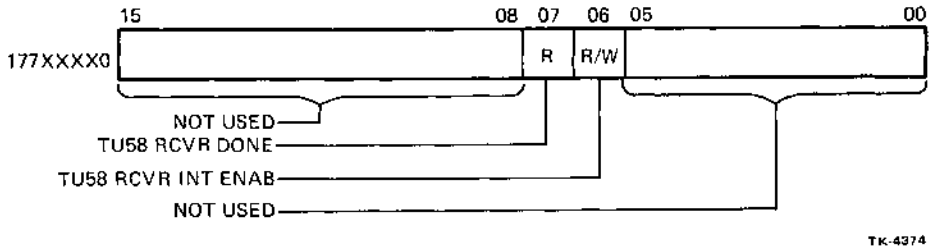


Figure 6-51 TU58 Receiver Status Register

TU58 Receiver Done (Bit 07) – This is a read-only bit which indicates that the UART has received a full character from the TU58. The done bit is ANDed with the interrupt enable signal (K3-7 TU58 REC INT ENA H) to clock the receiver interrupt request flip-flop. This generates K3-7 REQ TU58 REC INT H which initiates an interrupt sequence.

The done bit is cleared by the signal K3-7 TU58 CLR DONE L which generates the CLR R DONE signal on the UART. The clear signal is generated by INIT or by the processor reading the TU58 receiver buffer register (K3-5 TU58 CLR R DONE L is generated). Once the receiver buffer has been read, a new character may be loaded into the receiver.

TU58 Receiver Interrupt Enable (Bit 06) – This is a read/write bit. It enables an interrupt sequence when the TU58 R DONE bit is set, indicating that a character has been received and is ready for transfer to the PAX data bus. This bit is written when the address logic decodes a write operation to the TU58 receiver status register. The signal K3-5 TU58 RCSR WRITE H clocks PAX data bit 06 (K3-1 PX D06 H) into the interrupt enable flip-flop. This bit is cleared by INIT.

6.11.4.7 TU58 Receiver Buffer Register – The TU58 receiver buffer register (Figure 6-52) consists of four error bits and eight data bits associated with the TU58 UART receiver.

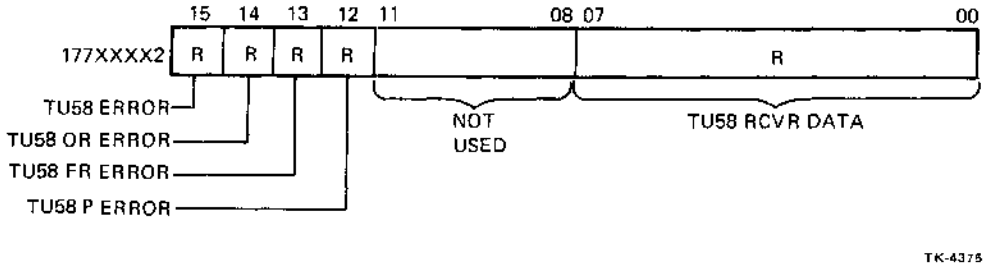


Figure 6-52 TU58 Receiver Buffer Register

TU58 Receiver Error Bits (Bits 15 to 12) – The four error bits of the buffer register are set to indicate improper receiver operation. These bits are read only and can be disabled by removing jumper W3 (shown on print K3-8). Three of the error bits are generated by the UART and the fourth bit (TU58 ERROR) is the inclusive-OR of the other three. The error bits are described as follows.

1. Overrun Error (TU58 OR ERROR) – Generated by the UART when R DONE was not cleared prior to receiving a new character. This indicates that the UART received a new character before the processor read the previous character.

2. Framing Error (TU58 FR ERR) – Generated by the UART to indicate that the character read has no stop bit.

3. Parity Error (TU58 P ERR) – Generated by the UART to indicate that the parity received does not agree with the parity expected.

4. TU58 Error – Indicates that one or more of the other three error bits is set.

Each of the error bits is updated when a new character is received. All four error bits are cleared by INIT.

TU58 Receiver Data Bits (Bits 07 to 00) – The receiver buffer is read only and is loaded by the UART. The UART receives the serial data from the TU58, converts it to parallel data and places it on the TU58 receiver data lines (K3-7 TU58 R DATA 07:00). This data can then be read by the central processor.

6.11.4.8 TU58 Transmitter Status Register – The TU58 transmitter status register (Figure 6-53) contains transmitter status information and maintenance information.

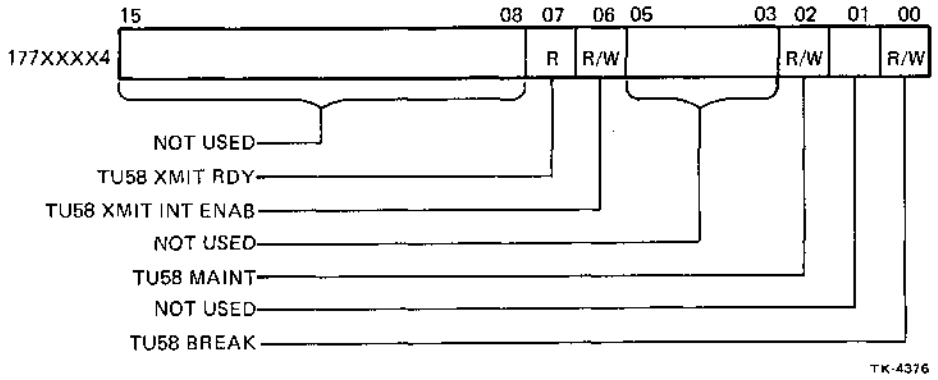


Figure 6-53 TU58 Transmitter Status Register

TU58 Ready (Bit 07) – This is a read-only bit that indicates the TU58 transmitter buffer is ready to accept a character from the PAX data bus. The ready bit initiates an interrupt sequence if bit 06 is set. It is ANDed with the interrupt enable signal (K3-7 TU58 XMIT INT ENAB H) to clock the transmitter interrupt request flip-flop.

Setting of the request flip-flop generates K3-7 REQ TU58 XMIT INT H which intitiates the interrupt sequence.

TU58 Transmitter Interrupt Enable (Bit 06) – This is a read/write bit. It enables an interrupt sequence to be initiated when bit 07 (TU58 READY) is set. Bit 06 is written when the address logic decodes a write operation to the TU58 transmitter status register. The signal K3-5 TU58 XCSR WRITE H clocks PAX data bit 06 (K3-1 PX D06 H) into the interrupt enable flip-flop. This bit is cleared by INIT.

TU58 Maintenance (Bit 02) – This is a read/write bit. When set, a closed loop test of the TU58 UART can be performed. The serial output of transmitter is fed back to the serial input of the receiver and the receiver is forced to run at transmitter speed. This bit is written by clocking PAX data bit 02 (K3-1 PX D02 H) into the TU58 MAINT flip-flop. This bit is cleared by INIT.

TU58 Break (Bit 00) – This is a read/write bit. When set, a continuous space is transmitted to the TU58. It can be disabled by removing jumper W10. This bit is written by clocking PAX data bit 00 (K3-1 PX D00 H) into the TU58 BREAK flip-flop. Bit 00 is cleared by INIT.

6.11.4.9 TU58 Transmitter Buffer Register – The TU58 transmitter buffer (Figure 6-54) is a write-only register that receives parallel data from the PAX data bus (K3-1 PX D07:00 H).

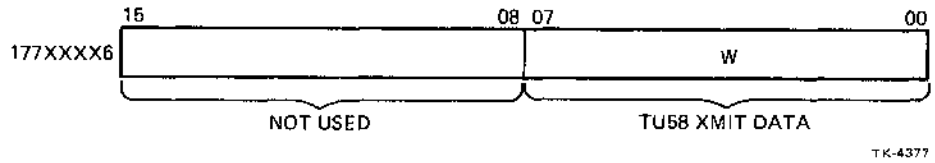


Figure 6-54 TU58 Transmitter Buffer Register

The parallel data is loaded when the processor writes the transmitter buffer. The address decode logic generates K3-5 TU58 XBUF WRITE L that clocks the PAX data latch and triggers a 300 ns one-shot. The one-shot keeps the data load signal (K3-7 LD XD TU58 L) low for the time required by UART transmitter. The parallel data is then converted for serial transmission to the TU58.

6.11.5 Interrupt Request Logic

The interrupt request logic enables the console terminal SLU, TU58 SLU, and line clock to interrupt the processor and initiate a service routine. Each of these devices will direct the processor to the correct routine by sending an appropriate vector. The following are the vectors corresponding to each device interrupt.

Device	Vector
Line Clock	100
Terminal Receiver	060
Terminal Transmitter	064
TU58 Receiver	000–777
TU58 Transmitter	Receiver vector plus 4

The line clock and terminal vectors are fixed. The TU58 receiver and transmitter vectors are switch selectable.

The terminal and TU58 interrupts are generated on bus request level 4 (BR4). The line time clock generates an interrupt on bus request level 6 (BR6). Each of the two bus request lines (K3-7 BR4 REQ L and K3-8 BR6 REQ L) are fed into UNIBUS control chips (DC013).

The UNIBUS control chip asserts the bus request if the interrupt logic is not already the master. The bus requests are sent to the processor arbitration logic (K4-2). The processor arbitrates the request and returns a bus grant (K3-1 BUS BG6 IN H or K3-1 BUS BG4 IN H) if no device of higher priority is making a request.

The UNBIUS control chip receives the grant and decides whether to accept it or pass it on. If a request is made before the grant is received, the control chip accepts the grant and asserts K3-8 BG SACK L. However, if a nonprocessor request (NPR) is also being made, the control chip does not execute an interrupt sequence upon receiving the grant.

The processor responds to SACK by dropping the bus grant. Removal of the bus grant causes the UNIBUS control chip to drop SACK and generate a MASTER signal. The MASTER signal is ANDed with K2-8 BUT SERVICE (1) H to place the vector on the PAX data bus. The processor clocks in the vector, returns PAX SSYN L, and begins running the microcode routine corresponding to that vector. The MASTER signal is also routed back to the MASTER CLR input of the control chip. This enables the control chip to drop MASTER when it receives PAX SSYN from the processor.

Note that the vector is transferred to the PAX data bus via the PAX data multiplexer (K3-9). The vector bits (K3-8 VECTOR D8:D2 H) are generated by the vector multiplexer (K3-8) and used as one source of the PAX data multiplexer. The MASTER signal of the control chip is ANDed with the BUT SERVICE signal of the processor to produce K3-8 ENAB VECTOR L. This signal causes the PAX data multiplexer to select the vector bits and enables the PAX data lines (K3-1 PAX D15:00 H).

6.11.5.1 Arbitration Between Terminal and TU58 Interrupts – As previously mentioned, the TU58 and terminal SLUs both interrupt on bus request level 4. Therefore, the interrupt request logic (Figure 6-55) must arbitrate between simultaneous interrupts. The order of priority for these interrupts is the following.

Highest	TU58 Receiver
	TU58 Transmitter
	TERM Receiver
Lowest	TERM Transmitter

As an example of interrupt arbitration, consider simultaneous requests by the TU58 receiver (K3-7 REQ TU58 REC INT H) and the terminal transmitter (K3-6 REQ TERM XMIT INT H). The two requests are clocked into the interrupt request latch by the arbitration control logic. Since the TU58 request has higher priority, the priority encode PROM will generate the following signals.

K3-7 ANY REC INT L
K3-7 TU58 REC INT L
ANY INT L

The signal K3-7 ANY REC INT L is an input to bit 02 of the vector multiplexer and generates a zero in that bit position. ANY INT L clocks the bus request flip-flop which generates K3-7 BR4 REQ L. The signal K3-7 TU58 REC INT L clears the TU58 interrupt request (K3-7 REQ TU58 REC INT H) and is also fed into the clear bus request and rearbitrate logic. Rearbitration occurs if the TU58 receiver interrupt enable bit is cleared or a character is transmitted before the bus request is granted. The bus request flip-flop is cleared and the interrupt request latch is clocked again. The signals generated by the priority encode PROM depend on the current interrupt requests. Under normal conditions, the rearbitration occurs when the MASTER signal is unasserted in response to PAX SSYN becoming asserted.

6.12 KK11-B CACHE

The KK11-B Cache Memory is an integral part of the PDP-11/44 processor and is designed to increase the CPU performance by decreasing the CPU-to-memory read-access time. It is an 8K-byte high-speed RAM memory organized as a direct-mapped cache with write-through. Figure 6-56 shows a block diagram of the KK11-B cache.

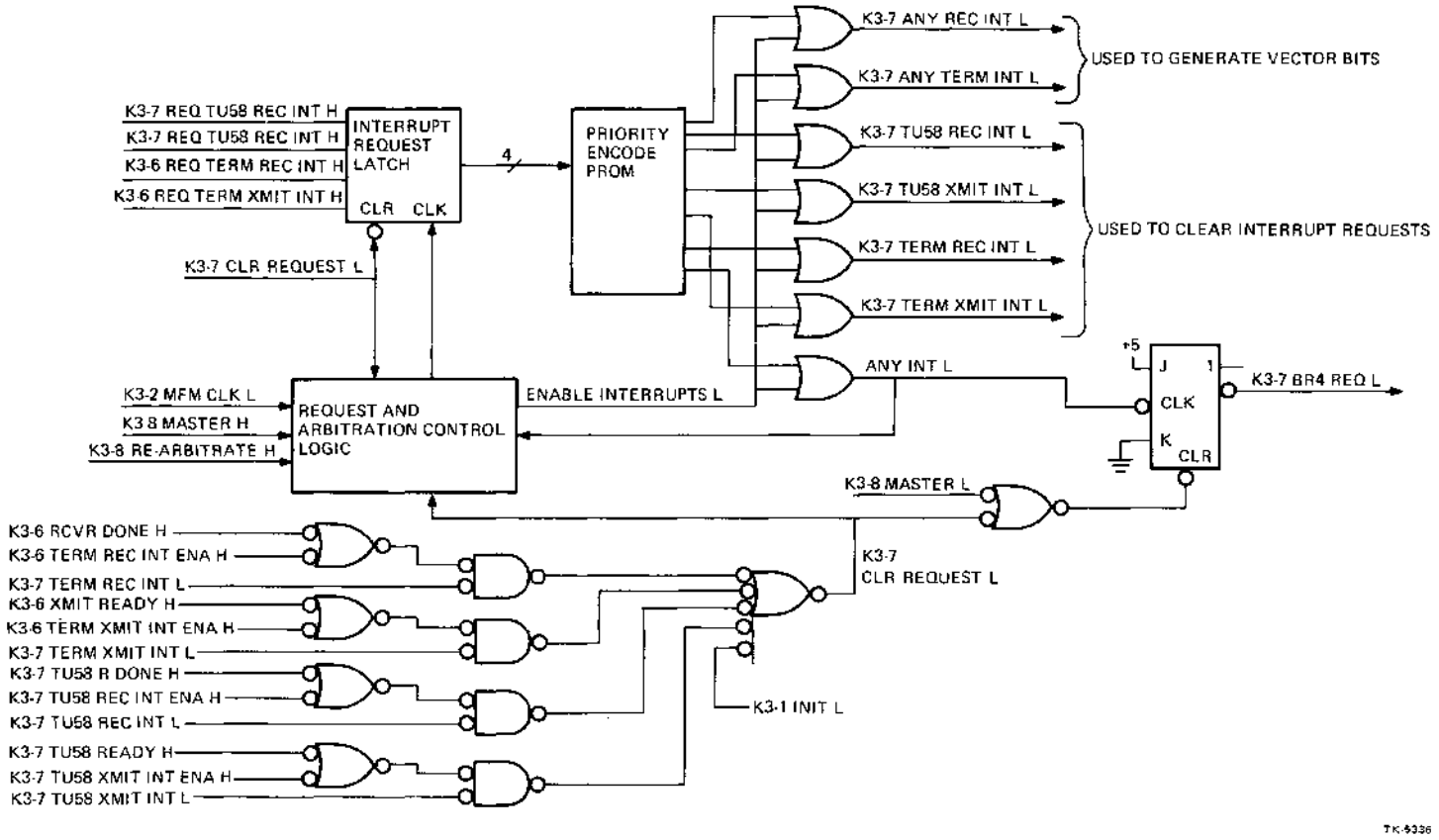


Figure 6-55 Terminal and TU58 Interrupt Arbitration Logic

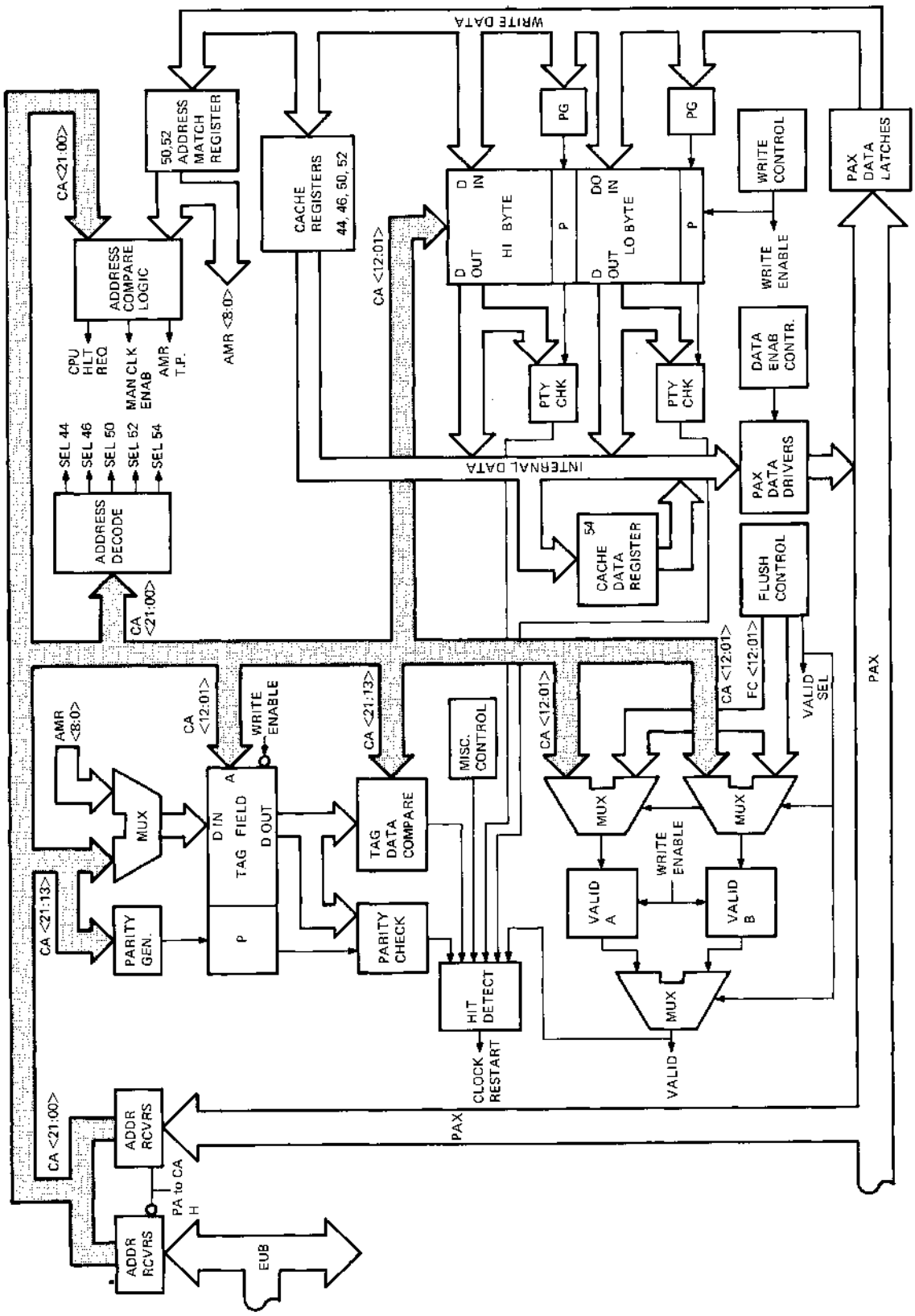


Figure 6-56 KK11-B Cache Memory Block Diagram

The KK11-B cache operates as an associative memory in parallel with main memory and is connected to the CPU via the PAX lines. When the CPU is performing a DATI from main memory, the cache memory is first checked to see if it contains the requested data. If the data is in cache memory (a read hit), the data transfer from main memory is discontinued and the data in cache is sent to the CPU via the PAX data lines. If the data is not in cache memory (a read miss), the data transfer is completed, with cache memory performing a write-through to update itself. When the CPU performs a DATO to main memory, the cache updates itself if the addressed location is presently in cache. DMA (direct memory access) and data transfers from the UNIBUS are monitored by the cache and result in the invalidation of cached locations. Only CPU transfers to main memory are cached. Memory located on the UNIBUS will not be cached.

6.12.1 Memory Organization

The KK11-B cache is an 8K-byte direct-mapping cache with write-through. A direct-mapping cache allows each main memory address only one possible location in cache.

Each address is divided into two fields: the index field and the tag field (Figure 6-57). The index field specifies the cache locations in which the tag and data are stored. The stored tag field is then compared to the tag of the requested word to determine if there is a cache hit.

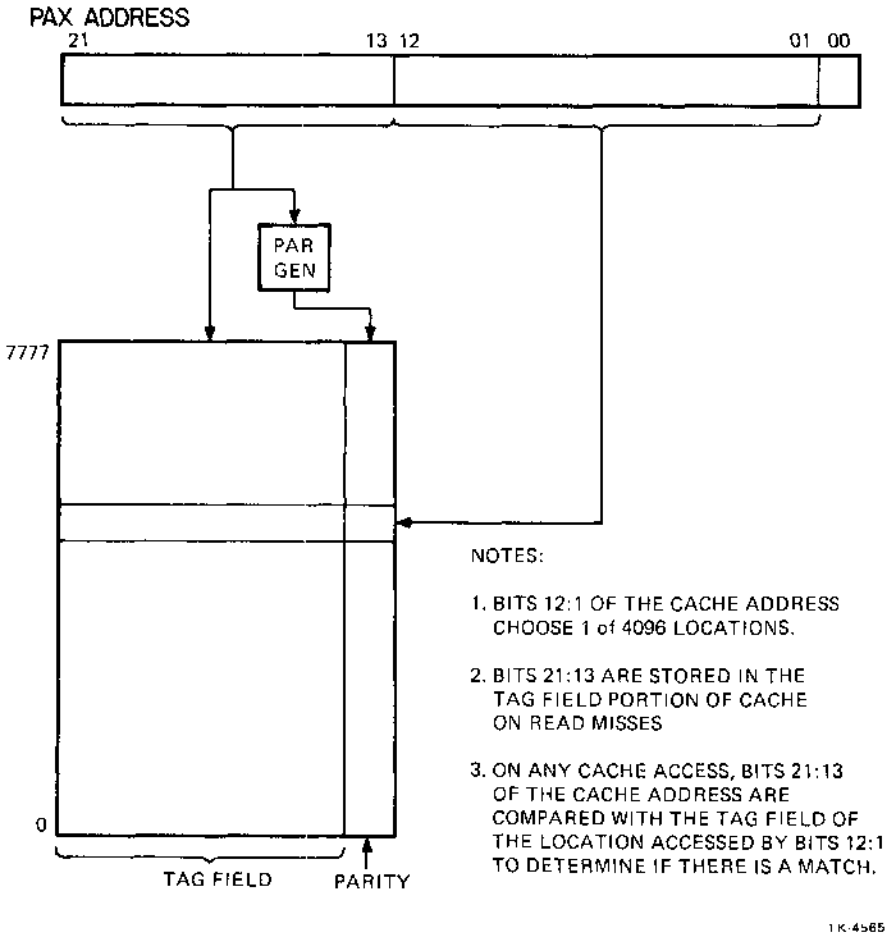


Figure 6-57 Cache Memory Addressing

The KK11-B Cache Memory consists of thirty 4096 × 1 static MOS RAM chips. The organization of these chips is shown in Figure 6-58. The cache memory is divided into three basic segments.

TAG	Consists of nine tag field bits plus one parity bit.
VALID	Consists of two bits; one bit is active while the other bit is cleared. The two bits allow a fast flush of cache by switching to the set of valid bits previously cleared.
DATA	Consists of two 8-bit bytes plus a parity bit for each byte.

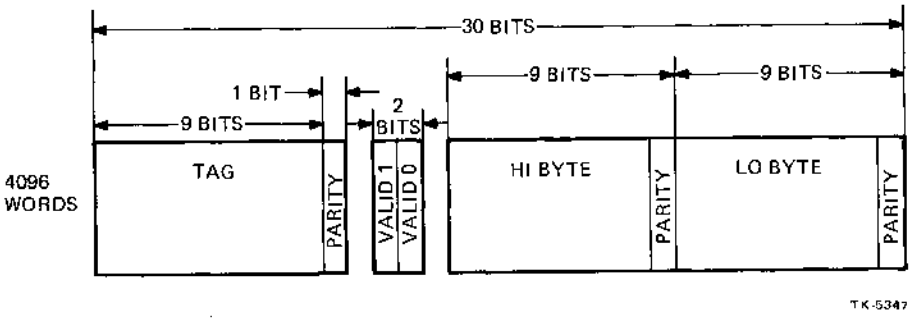


Figure 6-58 Cache Memory Organization

6.12.2 Interface Logic

The KK11-B cache interface logic consists of the PAX address and EUB address buffers located on K7-3 and the PAX data buffers and latches on K7-2, along with several control and timing signals. A detailed explanation of the PAX address, EUB address, and PAX data logic is contained in paragraphs 6.12.3, Address Logic, and 6.12.4, Data Control.

The following describes the cache interface signals.

PAX A21:00 H	These 22 lines are the physical address bits taken directly from the physical address register (BA) in the CPU. The cache looks at these address lines whenever the CPU starts a memory transfer.
EUB A21:00 L	These 22 lines are the memory address bus. The cache looks at these lines by default if the processor is not currently transferring data. The cache looks at these lines to watch for any DMA traffic that might result in invalidations of a cached location.
PAX D15:00 H	These 16 lines are the main CPU data bus. This bus connects the CPU data path and control section, the multifunction module, the UNIBUS interface and the cache. If the cache is providing data to the CPU, it comes over this bus. If the cache is updating itself via a READ MISS or WRITE HIT, the data is also on this bus.
EUB C0, C1 L	These two lines are the memory bus control lines. They work in the same manner as the UNIBUS control lines. The cache monitors these lines to determine the type and direction of transfer taking place.

EUB MSYN L EUB SSYN L	These two lines are the memory master SYNC and memory slave SYNC lines. They work in the same manner as the UNIBUS MSYN and SSYN lines. These lines are isolated from the UNIBUS lines to reduce loading. The cache monitors these lines to determine when memory has been accessed.
PAX SSYN L	This line is used by the various I/O page registers within the CPU (including cache) that communicate over the PAX data bus. This line works like BUS SSYN and is used to inform the processor that the data should only appear on the PAX data bus and not the UNIBUS data lines.
BUS PB L	This is the only UNIBUS line that the cache is connected to. The cache looks at this line to see if a memory read resulted in a parity error. This line is driven by the cache to cause the CPU to abort and trap on a cache parity error if the appropriate control bits have been set in the cache control registers.
PROC INIT L	This line is used by the cache to initialize its internal registers and also flush both valid bits. This signal is asserted on power-up or by the initialize command from the console.
ENAB ADRS H	This line is issued by the CPU as soon as it has successfully arbitrated for the bus. This signal is the first indication to the cache that the CPU is about to transfer data. On receiving this signal, the cache immediately switches from its standby mode of watching for I/O traffic on the memory address bus (EUB A21:00 L) to its fast-access mode where it looks at the processor physical address bus (PAX A21:00). This address bus will stablize the earliest in the cycle and hence give the cache the earliest possible address setup time.
UPPER 128 K L	This signal is generated by the CPU when the address on the PAX address lines (PAX A21:00) is within the range of the upper 128K of address space. Since this space is allocated to the UNIBUS address and I/O page group, it is of special interest to the cache. It tells the cache not to store any of the data that appears in this address range.
BUF C1 (1) H	This signal, which is generated by the data transfer logic of the CPU, gives the cache the earliest possible indication of the direction of the transfer about to take place, that is, DATO or DATI.
START TRAN L	This signal actually initiates the cache cycle. When the cache sees this signal it knows that the PAX address lines (PAX A21:00) are now stable. The leading edge of this signal is the point from which the cache access time is measured.

CACHE GATE H	This signal is derived by the CPU from START TRAN delayed by 45 ns. CACHE GATE is used by the cache in conjunction with START TRAN to control address switching and data enabling circuits.
STROBE CACHE H	This is a 15-ns wide pulse issued by the CPU 90 ns after the assertion of START TRAN. The cache uses this pulse to strobe its read hit logic to determine if the cycle is a cache read hit.
CACHE RESTART L	This signal is issued by the cache if the STROBE CACHE signal resulted in a read hit. The cache drives this line to restart the processor clock and inhibit the data transfer from main memory.
EXT CLK C L	This signal is a buffered version of PROC CLK, the main CPU clock. The cache uses this signal in various places to clock data from the CPU.
FAULT H	This signal is generated by the CPU when an odd address fault or memory management fault is detected. The cache uses this line to abort a cache read hit sequence on the occurrence of either of these errors.
CACHE PE INTR H	This signal is issued by the cache to direct-set the parity error flip-flop in the CPU if a cache parity error is detected. The CPU traps the parity error after the instruction is executed.
CACHE BYPASS H	This signal is issued by the CPU if one of three conditions exists. 1. If the memory management page address register currently in use has the cache bypass bit 15 true. 2. If the operator specifies an examine operation with cache bypass. 3. On detection of the destination access of an ASRB instruction, this feature is used in certain multiported memory applications. These three actions result in the cache forcing a miss condition if that location is currently cached and disallows the read update that would normally follow a miss.
FREE BUS H	This signal is issued by the console logic to disable all devices from driving data onto the PAX data bus. This action is used by certain maintenance commands issued by the operator.
FORCE CACHE DATA L	This signal is used by the console in conjunction with FREE BUS to allow the console to see the internal data bus in the cache during special console maintenance operations.

ENAB MAINT (1) H	This signal is issued by the CPU during the final destination memory reference of an instruction to allow the cache and memory management diagnostics to test these devices without affecting the fetching of the instructions in the diagnostic itself.
CPU HALT REQUEST L	The address match register in the cache can be set to allow the cache to halt the CPU on recognition of a unique 22-bit address. The cache asserts CPU HALT REQUEST L as soon as the selected address appears in the cache, if the appropriate maintenance bits are set. This line can also be driven by the parity detect logic on the cache to halt the processor after an instruction that caused a cache parity error.
MAN CLK ENAB L	This line is used in a manner similar to CPU HALT REQUEST. The cache can be set up to stop the processor clock on recognition of a 22 bit address. MAN CLK ENAB is a wire-ORed line that can be driven by the cache or the console to stop the CPU clock. This line can also be driven by the parity detect logic on the CACHE to stop the clock on a cache parity error.

6.12.3 Address Logic

The KK11-B cache address control logic (K7-3) selects the bus, PAX address or EUB address, that drives the internal cache address lines CA 21:00. Three basic conditions determine which set of address lines are selected to drive the cache address lines.

1. When the CPU is performing a data transfer, the PAX address lines are the point at which the 22-bit physical address will stabilize earliest. Therefore, when a data transfer is in progress, the cache will want to monitor the PAX address lines to see if it contains the requested data.

2. When a DMA transfer is in progress, the UNIBUS address generated by the DMA device is mapped to main memory via the UNIBUS map. Because of this, the PAX address lines will not show any DMA activity. For the cache to monitor DMA traffic, it must look at the EUB address lines.

3. When the CPU performs a data transfer to UNIBUS address space (upper 128K of main memory address space), the address on the PAX address lines may not be the same as the address on the EUB address lines. This condition is called "wraparound" and will be explained later.

Because the cache does not know when a UNIBUS device is accessing main memory (DMA), the cache address multiplexer (K7-3), by default, looks at the EUB address lines. When the CPU is performing a data transfer, the cache address multiplexer looks at the PAX address lines.

The control logic for the cache address multiplexer consists of E1, E2, E13, E23, and E59 located on K7-3 (Figure 6-59). This logic is used to generate the signals PA TO CA L and PA TO CA H. When PA TO CA L and PA TO CA H are not asserted (the default state), the EUB address lines are driven onto cache address lines CA 21:00. When the CPU starts a data transfer, ENAB ADRS H is asserted which asserts PA TO CA L and PA TO CA H. These two signals being asserted selects the PAX address lines and drives them onto the cache address lines CA 21:00.

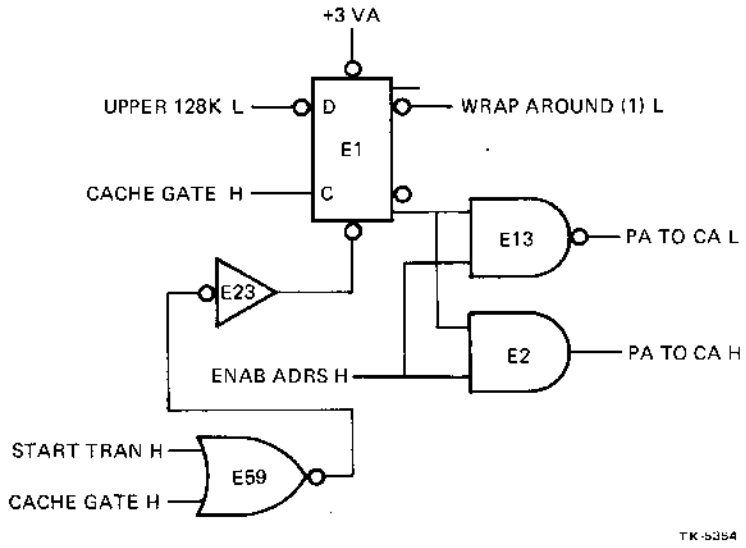


Figure 6-59 Cache Address Multiplexer Control Logic

One exception to the function of the cache address multiplexer is the special wraparound condition that can exist when the CPU is performing a data transfer to UNIBUS address space (upper 128K) with the UNIBUS map enabled. (For an explanation of how the UNIBUS map functions, refer to paragraph 6.9.) Due to the nature of the UNIBUS map, any address that appears on the UNIBUS is mapped into main memory via the map relocation registers when relocation is enabled. This also includes references to the UNIBUS address space made by the CPU when 22-bit relocation is enabled by memory management. Because of mapping of the PAX address by the UNIBUS map, the address on the EUB may not be the same as the original PAX address. This action is called "wraparound" because the original PAX address is wrapped around to main memory via the UNIBUS.

The circuitry that controls the wraparound action (K7-3) is shown in Figure 6-59. This circuit detects references to UNIBUS address space (upper 128K) by the CPU. When the CPU starts a data transfer, START TRAN H and ENAB ADRS H will switch the cache address multiplexer to the PAX address lines and START TRAN H removes the direct-clear from flip-flop E1. A minimum of 45 ns after ENAB ADRS H is asserted, CACHE GATE H will be asserted. CACHE GATE H clocks flip-flop E1 to determine if the address is in the upper 128K of physical address space. (If the address is not in the upper 128K of address space, signal PA TOP 128K L will not be asserted. Therefore, flip-flop E1 will be held clear and the address multiplexer will continue to look at the PAX address lines.) When the address is in the upper 128K of the physical address space, PA TOP 128K L will be asserted thus signifying a reference to UNIBUS address space. When CACHE GATE H clocks flip-flop E1 and UPPER 128K L is asserted, the flip-flop will be set and change the multiplexer so it is looking at the EUB address lines.

The output of E1 is labeled WRAPAROUND and is used elsewhere in the cache to force a cache miss condition to occur because the wraparound condition violates cache read hit timing. WRAPAROUND is also used to enable/disable the data array (K7-5 and K7-6).

6.12.4 Data Control

The cache data control logic (K7-2) can be divided into two parts:

1. Write data latching
2. Read data enable

6.12.4.1 Write Data Latching – The write data circuit is used when writing data from the PAX data bus into the cache array. When writing into the cache array, the data that is on the PAX data bus must be latched up for approximately 70 ns after the leading edge of PROC CLK L. This action provides the hold time required by the cache array when writing into it.

The write data circuit can be divided into two parts:

1. Transparent data latches E68 and E95
2. Latch control circuit E6, E31, and E33

The outputs of the transparent data latches, when the hold input is not asserted, will follow the data at their inputs. When writing into the cache array, BUF CACHE GATE L will be asserted and remove the preset from E6, which does not allow LATCH DATA L to be asserted. Approximately 45 ns after BUF CACHE GATE L is asserted, EXT CLK C L will be asserted, clocking flip-flop E6 and asserting LATCH DATA L which latches the data on the PAX data bus into latches E68 and E95. The latch will stay set until cleared by the negation of BUF CACHE GATE L which happens no less than 75 ns after the leading edge of EXT CLK C L. This circuit gives the necessary data hold times when the cache is being written into. The clearing of the latch is also controlled by I/O REG L. This signal is generated on K7-11 and is the result of a reference to a cache register. This input to the data latch flip-flop guarantees that data on the input to the cache registers will be true up to 100 ns after the clock enable inputs are negated.

6.12.4.2 Read Data Enable – The read data circuit consists of the data drivers and control logic used when reading data from the cache. There is also a maintenance control allowing access to cache via the console for maintenance purposes.

The drivers (E85, E87) are used to drive the requested cache data onto the PAX data bus for use by the CPU. Because of the relatively slow enable time of the data drivers as compared to their data-in to data-out time, the data enable circuit has been designed to enable the drivers as soon as possible during a cache read cycle. Three different conditions result in the cache data drivers being enabled so that the cache data is driven onto the PAX data bus.

1. A read of one of the five cache registers – When the address decode logic on K7-11 recognizes one of the addresses of one of the five cache registers, it asserts I/O REG READ H. If FREE BUS H is not asserted, the data drivers will be enabled via E18, E5 and E16 and will put the internal data onto the PAX data bus.

2. Cache READ HITs – To allow the data as much time as possible to propagate into the CPU and its options, the read data enable circuit has been designed to assume that all read accesses to cache will result in read hits. The control logic works as follows.

   START TRAN L is asserted by the CPU a minimum of 30 ns after the PAX address lines have stabilized. The assertion of START TRAN L clocks flip-flop E3 to determine if the data transfer is a DATO or a DATI. The data input to the flip-flop, BUF C1 H, provides the direction of the data transfer. If BUF C1 H is not asserted, a DATI cycle (when flip-flop E3 is clocked), ENAB DATA H, will be asserted, and, if FREE BUS H is not asserted, the data drivers E85 and E87 will be enabled. At this point it has not been determined if the read access is a hit or not. Approximately 85 ns after the assertion of START TRAN L, the inputs to the hit-detect logic have stabilized. The STROBE CACHE pulse is generated 90 ns after START TRAN L is asserted. If it is a read hit then CACHE RESTART is asserted and the CPU clock is restarted which results in START TRAN L being negated. (For a detailed explanation of a data transfer refer to paragraph 6.5.) START TRAN L is negated after the cache data has been clocked into the CPU. START TRAN L is then ANDed with BUF CACHE GATE H which clears flip-flop E3 and disables the data drivers.

If the read access to cache had resulted in a cache miss, the sequence will remain the same up to the STROBE CACHE pulse. As soon as the cache determines the read access was a miss, CLR ENAB DATA L is asserted and flip-flop E3 is cleared, disabling the data drivers.

3. Cache maintenance from the console – FREE BUS H and MFM FORCE CACHE DATA L are used by the console to override all drivers on the PAX data bus and to examine certain data in the cache, thus allowing the console visibility into the cache.

6.12.5 Cache Array

6.12.5.1 Data Section – The cache data section of the cache memory array, K7-5 and K7-6, consists of sixteen 4096 × 1 RAMs. The RAMs are addressed by CA 12:01 and the data inputs are the write data lines, WRT D 15:00, found in the data control logic, K7-2. Each byte of the data array can be written independently as determined by the write control logic (K7-1). The two write pulses, WRITE LO BYTE L and WRITE HI BYTE L, are generated by this logic. The output of the RAMs are enabled by the assertion of POWER ENABLE L, generated by AND gate E16 on K7-5. POWER ENABLE L is used to take advantage of the stand-by power-down feature of the RAM chips, thereby reducing the amount of power drawn by the data section of the cache array.

6.12.5.2 Tag Section – The tag section of the cache array, K7-4, consists of nine 4096 × 1 static MOS RAMs. Unlike the data section, the output of the tag RAMs is permanently enabled because the output of the tag field must be available during DMA transfers to determine if a DMA DATO cycle will result in the invalidation of a cache location.

The data input to the tag field is controlled by a multiplexer (E97, E100, E103) which selects one of two data inputs. This aids in diagnosing a problem in the tag field. During normal operation TDAR L is not asserted, thus gating CA 21:13 onto TAG WRT D 21:13. TDAR (tag data from address register) is a bit in the cache maintenance that, when set, asserts TDAR L and causes the multiplexer to gate AMR 08:00 onto TAG WRT D 21:13. Since the address match register (AMR) can be directly loaded by the diagnostic and the tag field can be read through the cache bit register, the diagnostic can isolate a failure in the tag section of cache.

The KK11-B cache has independent parity generation and checking for the cache data (high byte, low byte) and tag sections. The parity logic (K7-7) consists of three parity generators (E76, 81, 102) which generate the even parity used by cache. Each of the three parity generators has an extra input, from the cache control register, that allows the writing of wrong parity for diagnostic purposes. The outputs of the parity RAMs (E111, E110, E109) are read back in parallel with the rest of the cache array and are checked by three parity checkers (E79, E101, E58). The outputs of the parity checkers are ORed together to generate RAM PE H if a parity error exists. This signal and its components are clocked into the cache error register, E47, every time there is a read access to a valid cache location. (For a description of the bits in the cache error register refer to paragraph 2.3.3.5.) When a parity error is detected and RAM PE H is asserted, the clock input to the cache error register, E47, is inhibited by the assertion of CACHE PE L, thus saving the contents of the register for use by error recovery and logging routines. The cache error register can be cleared by a write operation to the register, a processor initialization which occurs on power-up, or by a console INIT command.

6.12.6 Cache Flush Control

The cache flush control selects which valid control set, A or B, will be used by cache while alternately clearing the other set, or it may do a cache flush which clears both sets of valid bits simultaneously. The cache flush logic (K7-8) can be activated by software by setting bit 8 in the cache control register, or by the assertion of PROC INIT on power-up, or a console initialize command.

Three flip-flops, E39 A, E39 B and E38 A, control the operation of the cache flush logic. On power-up, BUF PROC INIT L is asserted for 150 ns after AC LO is negated. This signal direct-sets both sections of E39, clears the flush counter E26, E43, and E54, clears the flush done flip-flop E38 B, and inhibits the delay line oscillator E52 and E53. With the direct setting of E39 B, both the direct-set and clear inputs of E38 A are asserted causing VALID A SEL L and VALID B SEL L to be unasserted and allowing both the valid A and valid B bits to be cleared by the flush counter.

When BUF PROC INIT L is negated, the oscillator starts to run, thereby beginning the cache flush. For 45 ns the oscillator generates FLUSH CLK H, which is the write enable to the valid RAMs, causing location 0 to be written. The flush counter is incremented 15 ns after FLUSH CLK H is negated and, 120 ns later, FLUSH CLK H is asserted, writes the next location, and the cycle repeats. (Figure 6-60 shows the cache flush timing.) E38 B is clocked 4095 cycles later by the carry output of E26 which sets the flip-flop, stopping the oscillator and clearing E39 A and B. With E39 B cleared, the direct-set and clear inputs of E38 A are unasserted. Since the clear input to E38 A is connected through an RC delay, the input is unasserted last, thereby clearing the flip-flop and selecting valid set A.

A cache flush sequence can also be invoked by setting bit 8 in the cache control register. This results in clearing the counters and flush done flip-flop. When the DATO to the cache control register is completed, E39 A is clocked set. This is the valid clear in progress (VCIP) flip-flop which releases the hold on the flush oscillator to start the flush sequence. Every time the cache flush bit is set, E38 A is complemented which causes the current valid set to be deselected and cleared while the previously cleared valid set is nonselected for immediate use. If a second flush command is issued before the last has finished (less than 800 μs), then valid clear in progress will still be set and will cause a one to be clocked into E39 B. This results in the direct-clear and set inputs being negated. The net result is if two flush commands are issued less than 800 μs apart, both valid sets are deselected and cleared, leaving the cache inoperative until completion of the double flush.

6.12.7 Valid Control Logic

The valid control logic (K7-9) consists of two 4096 $\times$ 1 RAMs and their associated input multiplexers. The input multiplexers are used to gate either CA 12:01 or CNT 12:01 to the address inputs of the valid A or B RAMs, and also to select the source for the write pulse and data inputs.

If the valid A set is selected, VALID A SEL L asserted, then its multiplexer is switched to look at the cache address lines CA 12:01, the write valid input from the write control logic, and the data input from K7-9 VALID DATA H. Valid set B, at this time, is either in the process of being flushed or it is clear and idle waiting for the next flush command to switch it into the in-use state. The data input to a VALID RAM is 0 if it is being flushed, or it is VALID DATA H.

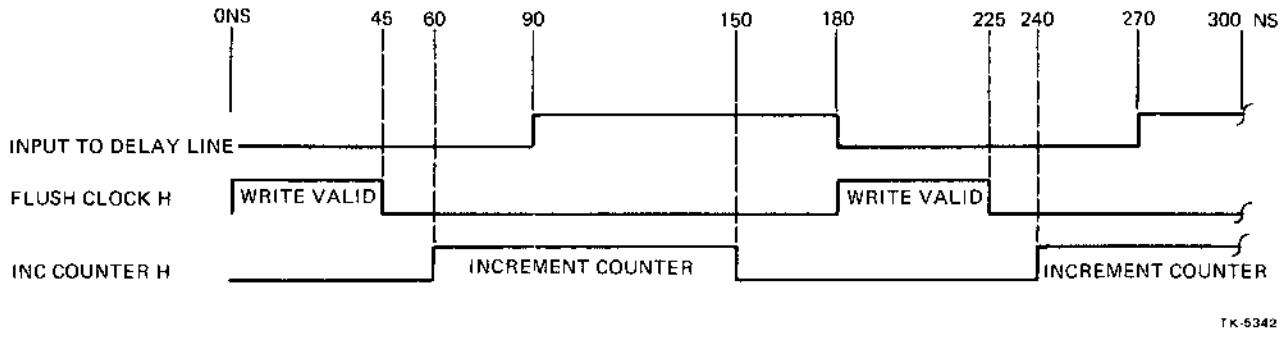


Figure 6-60 Cache Flush Timing Diagram

VALID DATA H is asserted when there is a CPU transfer to all but the upper 128K of address space, WRAPAROUND L not asserted. VALID DATA H will not be asserted if a cache bypass is in effect, BYPASS L asserted, or if the tag field is being tested by a diagnostic, TDAR L asserted. The output of the valid A RAM is routed through both multiplexers such that if a double flush is in progress (both sets of valid bits being cleared at once), VALID H will be held unasserted to keep the cache inoperative until the double flush is completed.

6.12.8 Write Control Logic

The algorithm used in the write control logic (K7-1) of the KK11-B cache is standard for a direct-mapped single-block single-set cache. Table 6-7 shows the response of the cache to different types of cycles and accesses (DMA or CPU).

As can be seen from Table 6-7 the cache will be written on four different occasions.

1. CPU DATI misses to main memory with cache bypass disabled (update).
2. CPU DATI hits to main memory with cache bypass enabled (invalidate).
3. CPU DATO hits to main memory (invalidate or update).
4. DMA DATO hits to main memory (invalidate).

The write control logic (K7-1) determines if a cache write is to be done and, if so, to which parts of the cache array (valid bit, tag field, cache memory high byte, or cache memory low byte).

The write control logic uses two multiplexers, E8 and E10, to select between the different conditions resulting in a cache write. E8 determines if it is a read (DATI) or a write (DATO, DATOB) cycle. E10 determines if it is a CPU or a DMA access. The remainder of the write control logic gives the result of the cache access (hit/miss), selects which section of the cache array is to be written, and generates the write enable pulse required by the cache array RAMs.

The inputs to multiplexer E8 are selected by C1 H to determine if the cycle is a read (DATI) or a write (DATO). If a read cycle is being done, then C1 H is not asserted and the D0 inputs are selected. If a write cycle is being done, C1 H is asserted and the D1 inputs are selected. The outputs of E8 are ENABLE WRITE H and byte selected for a DATOB cycle.

Table 6-7 Cache Read/Write Response

Type of Cycle	DMA		CPU	
	Hit	Miss	Hit	Miss
Read	Nothing	Nothing	Cached	Update
Read Bypass	Nothing	Nothing	Nothing or Invalidate*	Nothing
Write Bypass	Invalidate	Nothing	Invalidate	Nothing
Write	Invalidate	Nothing	Update	Nothing

*This action takes place when using multiported memory, Jumper W2 and W1 out, thereby eliminating the possibility of stale data in cache.

Read Cycle – When a read miss of cache occurs, a cache update is done. A miss condition is detected by AND gate, E7. The inputs to E7 and their functions are as follows.

BYPASS L – If this signal is not asserted then E7 is enabled to determine if the cycle is a read miss.

UPPER 128K L – This signal not asserted means that the address is in main memory space.

UBUS PB L – This signal not asserted means that the backing store reference that could occur, as a result of a cache miss, does not have a parity error.

BUF CACHE GATE H – This signal asserted means that the access to cache is from the CPU.

Cache Hit Flip-Flop – This flip-flop (E6) signals if there was a cache hit or miss on a read or write. The input to E7 from E6 being high tells the cache that the memory access now occurring was a result of a cache miss.

All of the above conditions result in ENABLE WRITE H being asserted. ENABLE WRITE H is sent to the write cycle mutliplexer (E10) which will be described later. If BYPASS L had been asserted, with jumper W1 installed, then ENABLE WRITE H would not be asserted resulting in no action by the cache. With jumper W2 installed and BYPASS L asserted, E7 will be disabled and AND gate E9 enabled to look for CPU HIT (1) H, thus generating ENABLE WRITE H to cause a write cycle for the bypass invalidate sequence.

Write Cycle – The write cycle logic consists of a multiplexer (E10), its input logic, and a pulse generator. The pulse generator is made up of a flip-flop (E42) and a delay line (E32); it is used to generate an accurate write pulse for the RAMs in the cache array. The inputs to the pulse generator are the data input to the flip-flop, which decides if a write cycle is to happen, and the clock input, which decides when the write cycle is to happen. The write cycle multiplexer is switched by BUF CACHE GATE H to determine if the write cycle is from the CPU or DMA traffic. The multiplexer selects the inputs to the pulse generator.

When BUF CACHE GATE H is not asserted the multiplexer selects the output of AND gate E40 as the data input to the pulse generator. The output of E40 will be asserted if C1 L and INTERNAL HIT L are asserted. These conditions indicate a write hit from a DMA device and the currently cached data is to be invalidated. EUB MSYN H and EUB SSYN H are ANDed together to provide the edge needed to clock the write pulse circuit and invalidate the specified location in cache.

If the cycle is a CPU write, then BUF CACHE GATE H will be asserted and switch the multiplexer so that ENABLE WRITE H is the data input to the pulse generator. EUB SSYN H ANDed with PROC CLK H is the clock input to flip-flop E42. PROC CLK H is used so that the cache will be written at the same time the CPU is writing its registers, thereby reducing the possibility of skew problems.

The pulse generator can be disabled by the hit on destination only bit being set in the cache maintenance register. This bit set asserts DISAB CACHE WRITE H which disables the outputs of the write cycle multiplexer, E10. When asserted, this signal remains asserted for all but the final destination access of any instruction. This feature allows diagnostics to test the cache without concern for how the instruction stream affects the write algorithm. This feature should be used with care because it is possible to create stale data in some cases.

The output of the pulse generator is sent directly to the valid logic (K7-9) because it can be written without affecting the rest of the cache array. The rest of the cache array is written only when BUF CACHE GATE H is asserted, indicating a CPU access. The logic that controls which section of the cache array is written consists of gates E13, E16, E22, E30, E46 and section A of multiplexer E8.

When BUF CACHE GATE H is asserted, the gates that generate WRITE TAG L (E46), WRITE HI BYTE L (E30), and WRITE LO BYTE L (E16) are enabled. If the cycle is a read update, all of the cache array will be written. If the cycle is a write update, the output of multiplexer E8 section A will determine if it is a DATO or DATOB. A DATO will write the high byte and low byte while a DATOB will look at CA 00 H to see if the high or low byte is to be written.

6.12.9 Hit Detect Logic

The hit detect logic (K7-10) determines if all the conditions necessary for a CPU READ HIT have been met. The hit detect logic consists of a 13-input NAND gate and its input logic. The signals and their purpose are as follows.

COMPARE 1 H
COMPARE 2 H
COMPARE 3 H

These three input signals are generated by comparators E61 and E57 along with XOR gate E64. This logic compares the tag field selected by CA 12:01 with the upper nine bits of the cache address, CA 21:13, to see if there is a match. When there is a match, all the signals will be asserted.

VALID H

This bit being asserted indicates that the word currently being read out of cache is valid.

TAG PE L
HI BYTE PE L
LO BYTE PE L

These three signals are normally not asserted, indicating that the parity of the word being accessed is correct. Any of these signals being asserted along with VALID H indicates a cache parity error and will force a miss condition.

MAINT DISAB CACHE L

This signal, when asserted, indicates that either a wraparound condition exists or the cache maintenance bit, hit on destination only, is set and the current access is not a destination access. This signal being asserted will cause a cache miss.

MISS HI L
MISS LO L

These two signals are generated from FMHI (1) H and FMLO (1) H (force miss high and force miss low) which can be set from either the cache control register or the two toggle switches mounted on the cache module. When asserted, these signals cause misses to high and low address space, respectively. High cache address space is when cache address bit 12 (CA 12 H) is set and low cache address space is when CA 12 H is not set.

C1 H
BYPASS H

These two signals are ORed (E19) together and must not be asserted to allow a cache hit. Hits are only permitted for read operations (C1 H unasserted) without bypass (BYPASS H unasserted).

FAULT H

This signal must not be asserted to allows hits from cache. This signal is generated by the CPU to indicate an error in the virtual address (odd address error) or an error in the physical address (memory management violation). In either case the CPU has decided to abort the transfer, and this signal is used to cause the cache to do the same.

When all the inputs to E28 are high, CACHE HIT L will be asserted to signify a cache read hit. CACHE HIT L is clocked into the cache hit flip-flop (E42) by STROBE CACHE H and sets the flip-flop. When the cache hit flip-flop is set, CACHE RESTART L is asserted and the CPU clock is restarted so the CPU can clock in the cache data. CACHE RESTART L also holds the CPU master sync flip-flop clear, thus aborting the main memory reference that would occur if the cycle was a cache miss.

CACHE HIT L and STROBE CACHE H are ANDed (E9) to generate CLR ENAB DATA L. This signal is used to disable the cache data drivers when a cache read miss occurs (CACHE HIT L unasserted).

The cache hit register (E73) is used to save the hit/miss sequence for the last six memory references. This register is wired as a shifter and is clocked by STROBE CACHE H ANDed with MAINT DISAB CACHE L. As long as the address is within main memory and the hit on destination only bit of the cache maintenance register is not set, every STROBE CACHE H pulse will shift in the current value of INTERNAL HIT L. This signal reflects both read and write hits. The output of the first stage of the hit register is used to drive a LED, mounted on the cache module, to provide a visual indication of cache hits.

6.12.10 Cache Register Control

The cache register control logic (K7-11) consists of a decoder (E60) and AND gates E62 and E74 which are used to decode the upper part of the cache register addresses 17777740 to 17777756. The outputs of E62, E74 and AND gate E2, which is asserted when EUB MSYN A and START TRAN H are both asserted, are used to enable the decoder (E60). Cache address bits 1:3 (CA 03:01 H) are used to select the particular register addressed. The outputs of the decoder are ORed together (E50, E13, E19) and delayed by an RC network to generate PAX SSYN L. This signal is used by any processor options that communicate over the PAX bus and is the same as BUS SSYN on the UNIBUS. Two other signals are also generated by the outpt of E9: I/O REG READ H which is used to turn the cache data drivers on and put the data on the PAX bus, and I/O REG L which is used to control the write data latch. (Refer to paragraph 6.12.4.) These signals determine whether it is a read or a write to the selected cache register. Some of the outputs of the decoder are ANDed with LOAD HI BYTE L and LOAD LO BYTE L to generate the required load signals for the writable registers.

For a description of each cache register and its bit functions refer to paragraph 2.3.3.

6.12.11 Address Match Logic

The KK11-B cache implements an address match and oscilloscope sync register which can be used by diagnostics to check the address buses within the cache or it can be used by maintenance personnel to provide a convenient oscilloscope sync point for troubleshooting both cache and CPU failures.

The 22-bit address match register (K7-12) consists of three octal registers that can be loaded by a DATO cycle to cache registers 17777750 and 17777752. Once the registers are loaded, comparators E104, E69, E67, E75, and E106, along with XOR gate E64, monitor the cache address lines CA 21:00 for a match with the address match register AMR 21:00. If a match is detected, all eight inputs of AND gate E66 will be asserted, thus generating CA EQUALS AMR L which will direct-set the address match (AM) flip-flop E71. The output of the AM flip-flop is used to drive a LED mounted on the cache module. The direct-set input to the AM flip-flop is also available on the backplane and on terminal points, T.P. 1 and T.P. 2, accessible on the top of the cache module. The AM flip-flop is read/write through the cache maintenance register. Two bits in the cache maintenance register allow the cache to either stop the CPU clock or halt the CPU on an address match condition or a cache parity error. This feature is useful when troubleshooting intermittent cache or system problems. Two AND gates (E21) are used to drive CPU HLT REQ L or MAN CLK ENAB L if the enable halt action or enable stop action bits of the cache maintenance register have been set before an address match or a cache parity error.

6.12.12 Cache Registers

The registers and drivers shown on K7-13 are all driven onto the cache internal data bus, INT D 15:00 H, by their various select signals that are generated by the address decode logic on K7-11. The drivers, when enabled, drive the contents of the selected cache register onto the cache internal data bus which, in turn, is driven onto the PAX data bus during read accesses to the cache registers.

Four octal registers, E86, E99, E98, E89, and a flip-flop E63, are used to save the contents of the addressed section of the cache array and associated internal status on every CPU READ to main memory. These registers are clocked by CLK DATA L which is generated anytime there is a CPU read access to main memory.

PDP-11/44 System Technical Manual
EK-KD11Z-TM-001

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults or errors have you found in the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

_____

☐ Please send me the current copy of the *Technical Documentation Catalog*, which contains information on the remainder of DIGITAL's technical documentation.

Name _____ Street _____
Title _____ City _____
Company _____ State/Country _____
Department _____ Zip _____

Additional copies of this document are available from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA 01532
Attention: Printing and Circulating Service (NR2/M15)
Customer Services Section

Order No. EK-KD11Z-TM-001

Fold Here

Do Not Tear – Fold Here and Staple

digital

No Postage Necessary if Mailed in the United States

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 33 MAYNARD, MA.

POSTAGE WILL BE PAID BY ADDRESSEE

Digital Equipment Corporation
Educational Services Development and Publishing
1925 Andover Street
Tewksbury, MA 01876