WEEK 2 PDP11/40

TIME	MON	TUES	WED	THURS	FRI
0900	INTRO TO μ PROGRAM DEVICE	KD11 FLOWS	KD11 FLOWS & DISPLAY RULES	LOGIC ANALYSIS	LOGIC ANALYSIS
	SUB COMMANDS AND			POWER UP	DATA XFER
1000	BLOCK DIAGRAM USAGE	MICRO BRANCHING	KD11 CONSOLE OPERATIONS	POWER DWN	BR SEQ
				STACK OVFW	NPR SEQ
1100				ODA ERROR	
1200	L U N C H				
1300	U WORD FORMAT & CLOCK CKT ANALYZE	KD11 FLOWS & SINGLE CLOCKING KM11	KD11 FLOWS SERVICE & TRAPS	PROBLEM ISOLATION & BACK PLANE	MM-11 MEMORY
1400					
1500	MUXS & GPR ADRS SWITCH	LAB	LAB	TROUBLE SHOOTING LAB	
1600	INTRO TO KD11 FLOWS				
1700					REVIEW & COURSE CRITIQUE

CORRECTION SHEET

1- CHANGE DOPØ7 (SHEET 8) FLOWS FROM DISPLAY D TO DISPLAY R[SF]

2.- ADD THE TERM BUTØ6 TO CON19 (SHEET 11) FLOWS

3 - REVISE MODULE UTILIZATION KM11A BASIC=F1 OPTION E1

4 - BA MUX LOW ORDER INPUTS ARE REVERSED

5 -

6 -

7 -

8 -

9 -

10 -

11 -

12 -

13 -

14 -

15 -

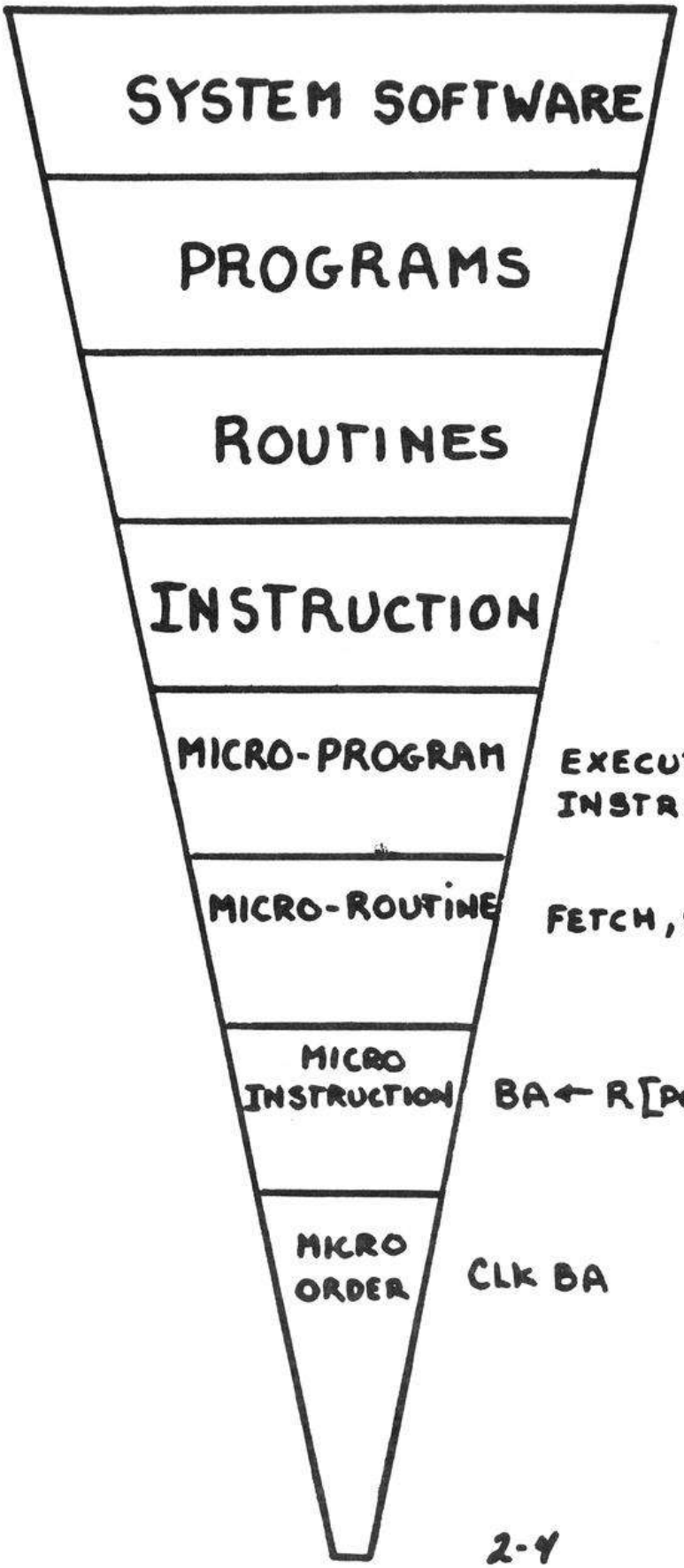
16 -

17 -

18 -

DAY 1

MICRO-PROGRAM INTRODUCTION.



KD11-11A SUBCOMMAND LIST

GENERAL REGISTERS

```
RIF (3:Ø) = ØØ8
          = Ø18
            :
            :
          = 168
RIF (3:Ø) =178
```

```
RA (3:Ø) ←RIF (3:Ø)
 "    "  ← IR (8:6)
 "    "  ← IR (2:Ø)
 "    "  ← BA (3:Ø)

READ ←1
WRITE ←1

R(15:Ø8)←DMUX(15:Ø8)
R(Ø7:ØØ)←DMUX(Ø7:ØØ)
```

ARITHMETIC LOGIC UNIT

```
AM (15:ØØ)←R(15:ØØ)

BIN(15:ØØ)←BREG(15:ØØ)
BIN(15:ØØ)←BCON(15:ØØ)
BIN(15:Ø8)←BREG(15:Ø8)
BIN(Ø7:ØØ)←BREG(Ø7:ØØ)
BIN(15:Ø8)←BREG(Ø7:ØØ)
BIN(Ø7:ØØ)←BREG(15:Ø8)
BIN(15:ØØ)←BREG(Ø7:ØØ)   SEX

BREG(15:ØØ)←DMUX(15:ØØ)
```

```
Ain (7:Ø)——PS (7:Ø)

BCON (15:ØØ)←1
              ←2
              ←4
              ←1Ø
BCON (15:ØØ)←17757Ø

Cin←1    Cin←Ø

ALUout = A PLUS CIN
ALUout = Ā PLUS CIN
ALUout = A PLUS B PLUS CIN
ALUout = A MINUS B
ALUout = B PLUS CIN
```

ALU output

```
D(15:ØØ)←ALUout (15:ØØ)
DMUX(15:ØØ)←D(15:ØØ)
DMUX(15:ØØ)←R(15:ØØ)
DMUX(15:ØØ)←BUS D (15:ØØ)
```

```
DMUX (15:ØØ)←COUT,D (15:Ø1)
PS (7:Ø)←DMUX (7:Ø)
IR (15:ØØ) ←DMUX (15:ØØ)
BA (15:ØØ) ←R(15:ØØ)
BA (15:ØØ) ←ALUout (15:ØØ)
```

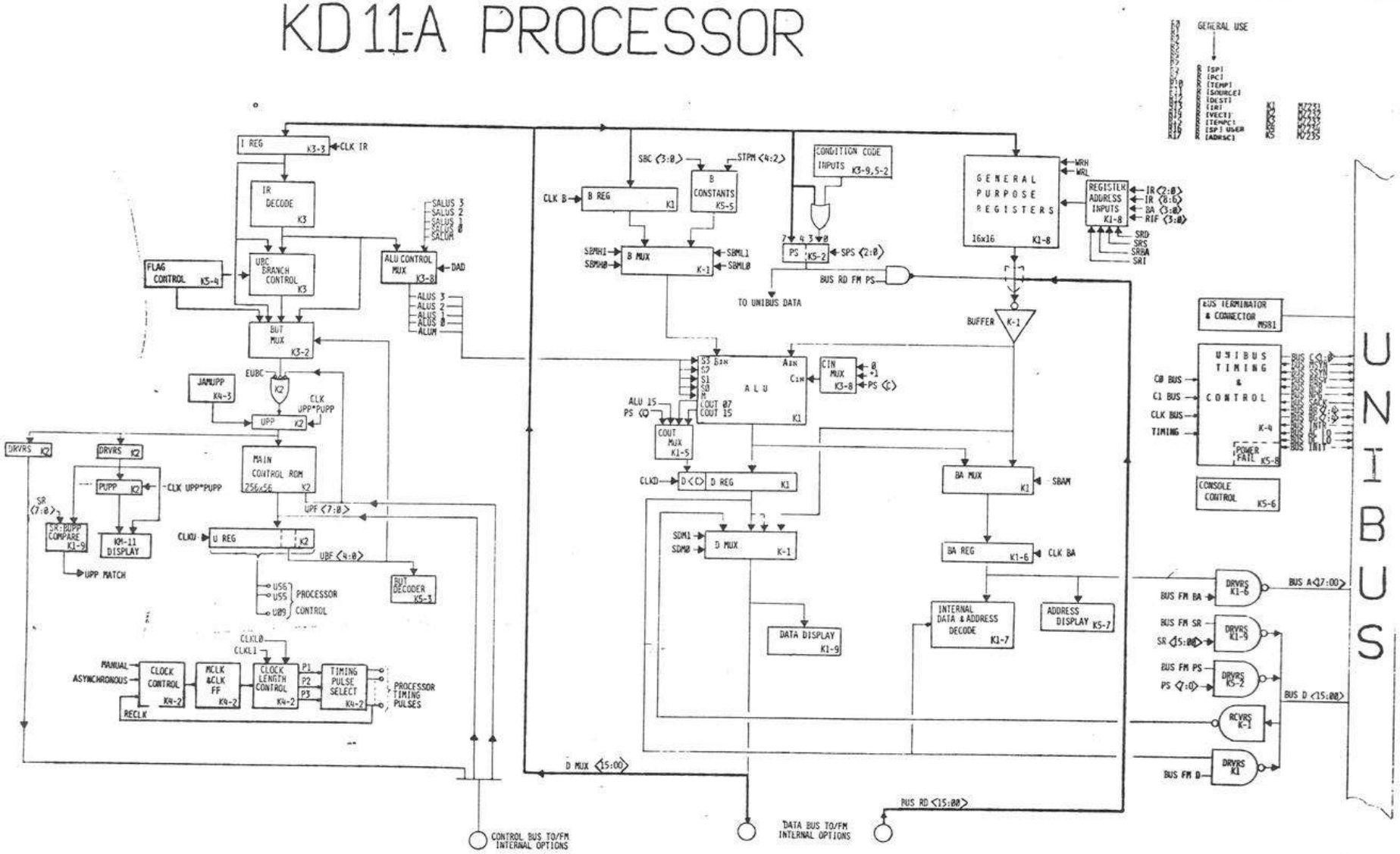
CONTROL AND TIMING

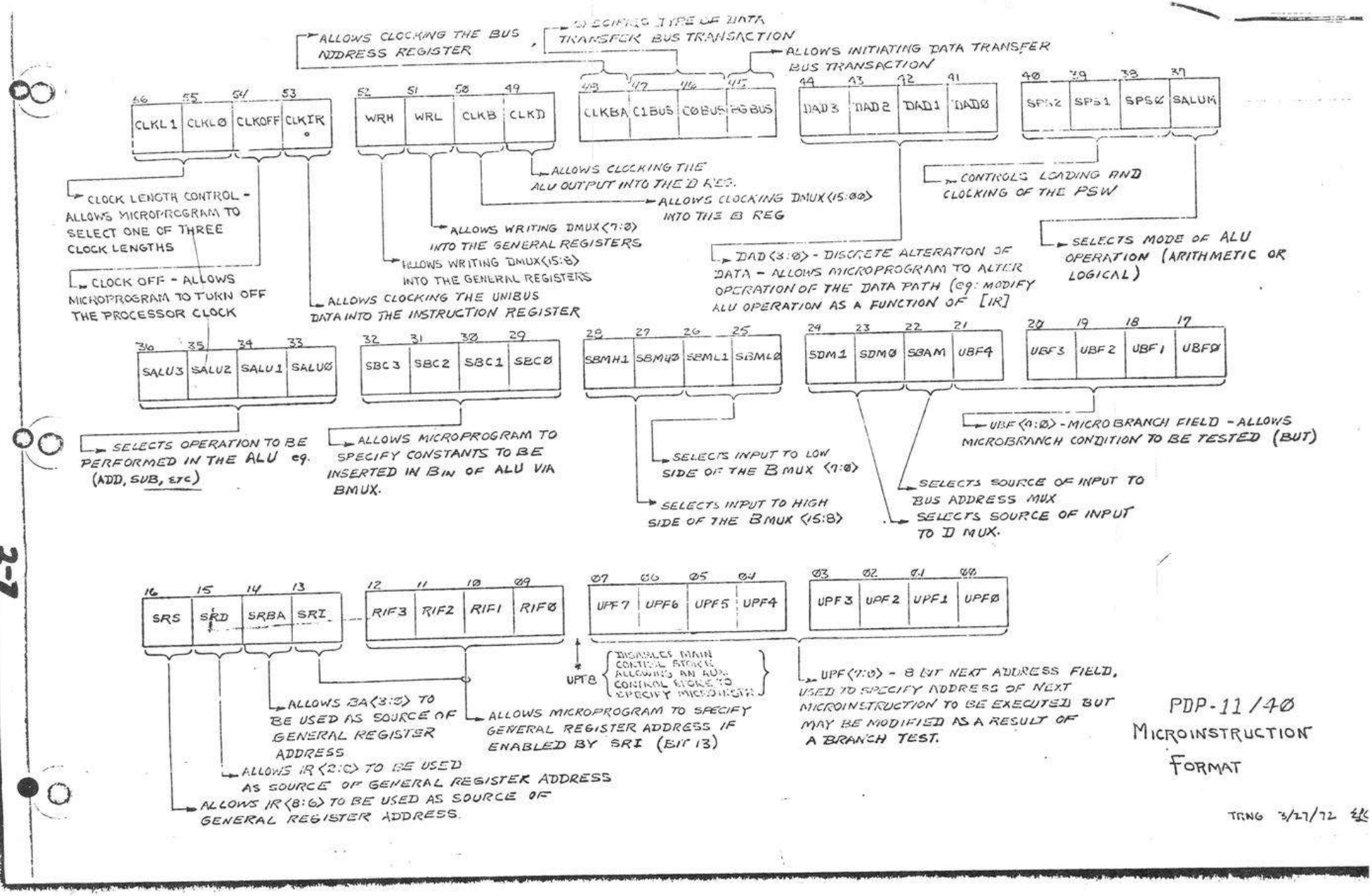
```
BUS C (1:Ø)←Ø
  "    "   ←1
  "    "   ←2
  "    "   ←3
CLKL ←1
 "  " ←2
 "  " ←3
CLKOFF ←1
```

```
BUS BBSY←1
BUS MSYN←1
BUS A (15:ØØ)←BA (15:ØØ)
BUS A (17:16)←ʃ BA (15:13)

BUS D (15:ØØ)←D (15:ØØ)
BUS D (15:ØØ)←Ø,PS (7:Ø)
BUS D (15:ØØ)←SR (15:ØØ)
```

KD11-A PROCESSOR





PDP-11/40 MICROINSTRUCTION FORMAT

TRNG 3/27/72

SUB-COMMAND EXAMPLES

USING THE KD-11 BLOCK DIAGRAM AND THE SUB COMMAND LIST, WRITE THE SUB-COMMAND SETS REQUIRED TO IMPLEMENT THE FOLLOWING

1. BA ← UNI BUS DATA

2. R[6] ← R[6] MINUS 2

ANSWER TO SUB-COMMAND EXAMPLES (2-8)

1. BA ← UNI-BUS DATA

```
                "CLKL1"
                DMUX<15:00> ← BUS D<15:00>
(P1)            B<15:00> ← DMUX<15:00>

                CLKL2
                BMUX<15:00> ← B<15:00>
                BIN<15:00> ← BMUX<15:00>
                AIN = Ø
                CIN = Ø
                ALUOUT = BIN + AIN + CIN
                BAMUX<15:00> ← ALUOUT<15:00>
(P2)            BA<15:00> ← BMUX<15:00>
```

2. R[6] ← R[6] MINUS 2

```
                "CLKL3"
                RIF<3:Ø> ← 6
                RA<3:Ø> ← RIF<3:0>
                READ ← 1
                AIN<15:00> ← R<15:00>
                CIN = Ø
                BCON<15:00> ← 2
                BMUX<15:00> ← BCON<15:00>
                BIN<15:00> ← BMUX<15:00>
                ALUOUT = A MINUS B
(P2)            D<15:00> ← ALUOUT<15:00>
                DMUX<15:00> ← D<15:00>
                R<15:00> ← DMUX<15:00>
(P3)            WRITE ← 1
```

PDP 11/45 MICROINSTRUCTION CODING WORKSHEET

Ø - INACTIVE 1 - ACTIVE

MIKROINSTRUCTION	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1. FET 02 (1)	Ø	1	1	Ø	Ø	Ø	Ø	Ø	1	Ø	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1	Ø	Ø	Ø	Ø	1	Ø	Ø	Ø	1	Ø	1	1	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	1
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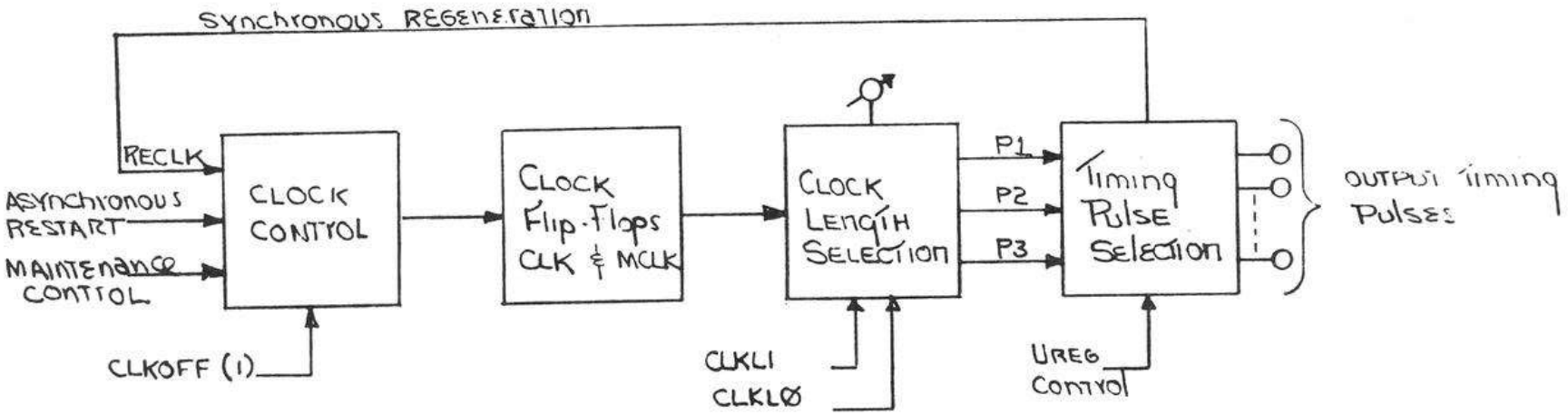
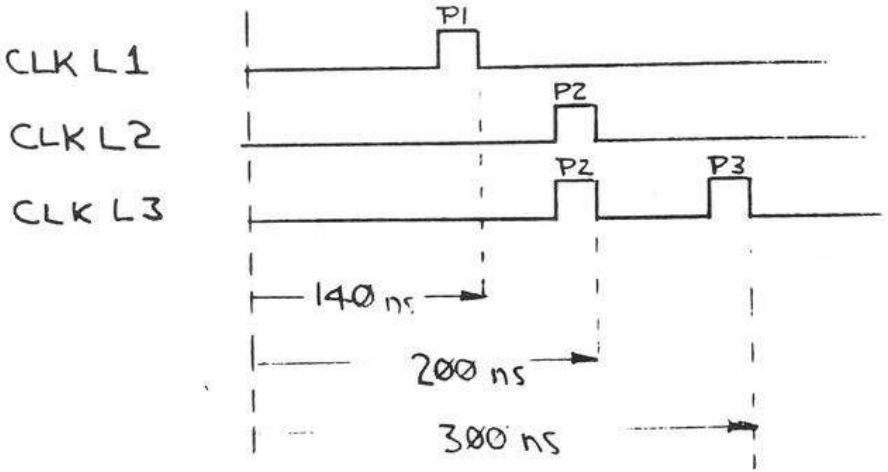
2-10





KDIIIA
Processor Clock
Block Diagram

11-2

BASIC TIMING

PURPOSE:

USED TO GATE INFORMATION INTO REGISTERS AND TO STEP THE MICRO-PROGRAM THRU ITS SEQUENCES:

SELECTION OF CLOCK LENGTH:

THERE ARE THREE UNIQUE CLOCK LENGTHS THAT MAY BE SELECTED BY THE MICRO-PROGRAM. EACH MICRO-WORD WILL SELECT ONE OF THE FOLLOWING CLOCK LENGTHS DEPENDING ON WHAT THAT MICRO-WORD IS TRYING TO DO. THE MICRO-WORD WILL ALWAYS SELECT THE SHORTEST CLOCK LENGTH THAT WILL ACCOMPLISH THE TASK SPECIFIED IN THAT MICRO-WORD.

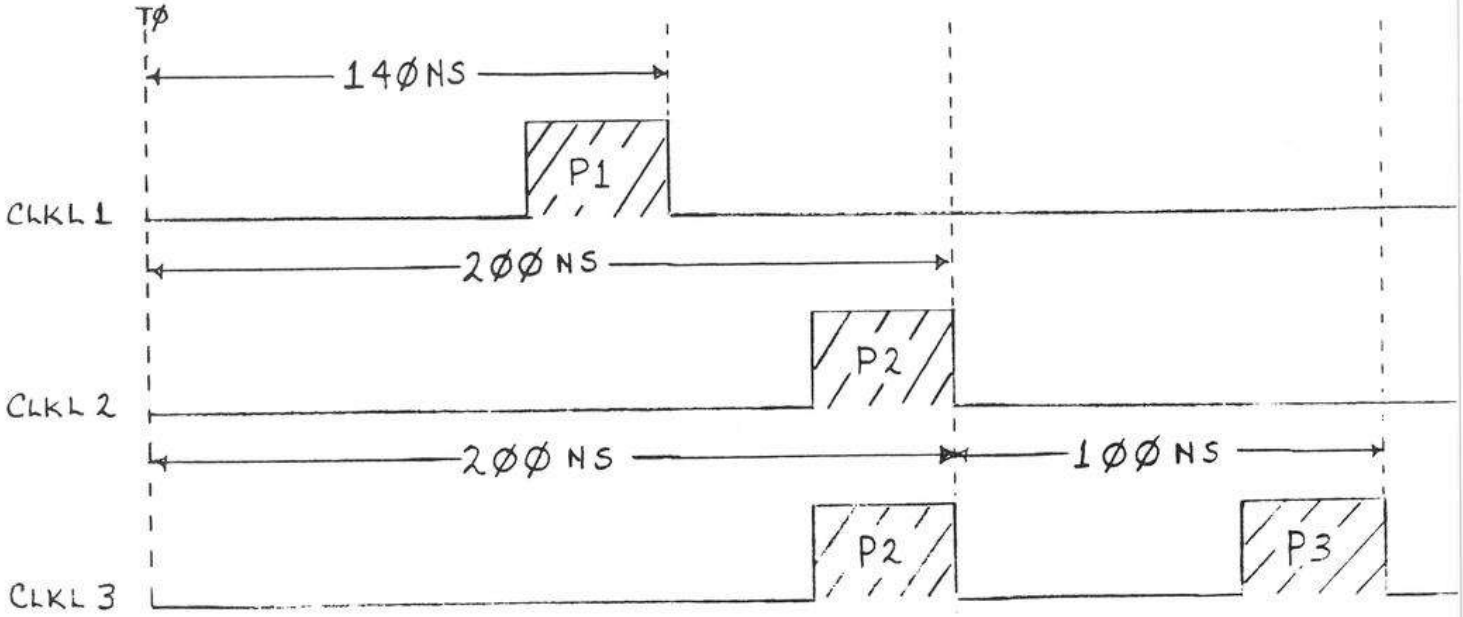
RECYCLING THE CLOCK:

THE CLOCK WILL AUTO-MATICALLY RESTART ITSELF ON THE TRAILING EDGE OF THE LAST CLOCK PULSE PERMITED IN THE PRECEEDING CLOCK CYCLE. RESTART IS ASSUMED UNLESS THE MICRO-WORD CHOOSES TO STOP THE CLOCK (IE DATA BUS CYCLE)

GENERAL RULES FOR CHOOSING CLOCK LENGTHS:

SINCE THE MICRO-PROGRAM CAN BE STEPPED ALONG BY THE PRESENCE OF ANY OF THE THREE CLOCK LENGTHS THE ONLY FACTOR IN SELECTING CLOCK LENGTHS IS WHICH REGISTER IS INVOLVED IN THIS MICRO-WORD EXECUTION CERTAIN REGISTERS REQUIRE PARTICULAR CLOCK LENGTHS TO BECOME ACTIVE. THE FOLLOWING IS THE REQUIRED CLOCK LENGTH THAT WILL ACTIVATE THE REGISTERS.

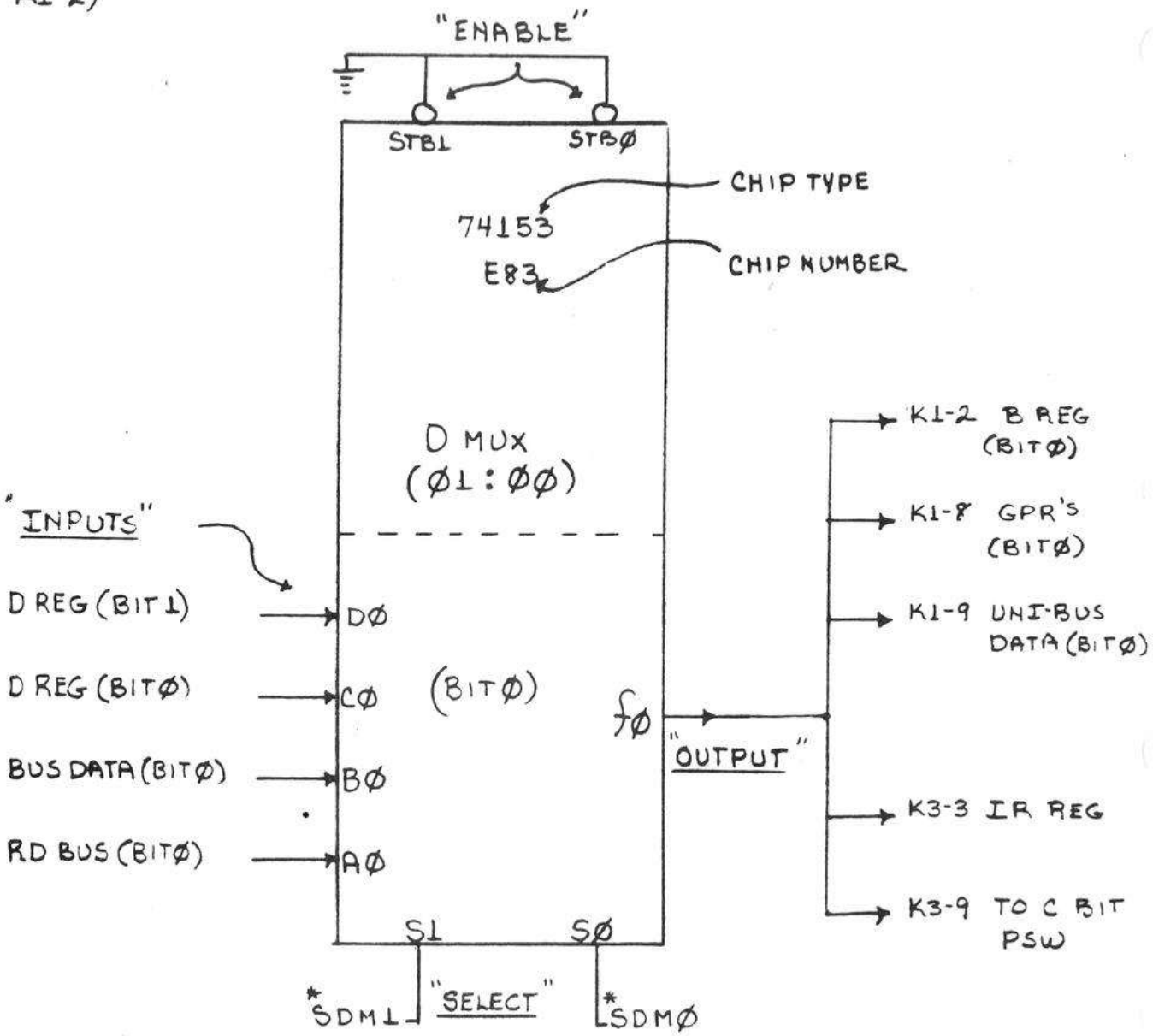
LOADING BA REG	CLKL 1 OR CLKL 2
LOADING D REG	CLKL 2
LOADING GPR REG	CLKL 1 OR CLKL 3
LOADING IREG AND BREG	CLKL 1 OR CLKL 3



NOTE: WHENEVER CLKL3 IS SPECIFIED BY MICRO-WORD P2 AND P3 ARE BOTH AVAILABLE AT CLOCK OUTPUT.

D MULTIPLEXOR

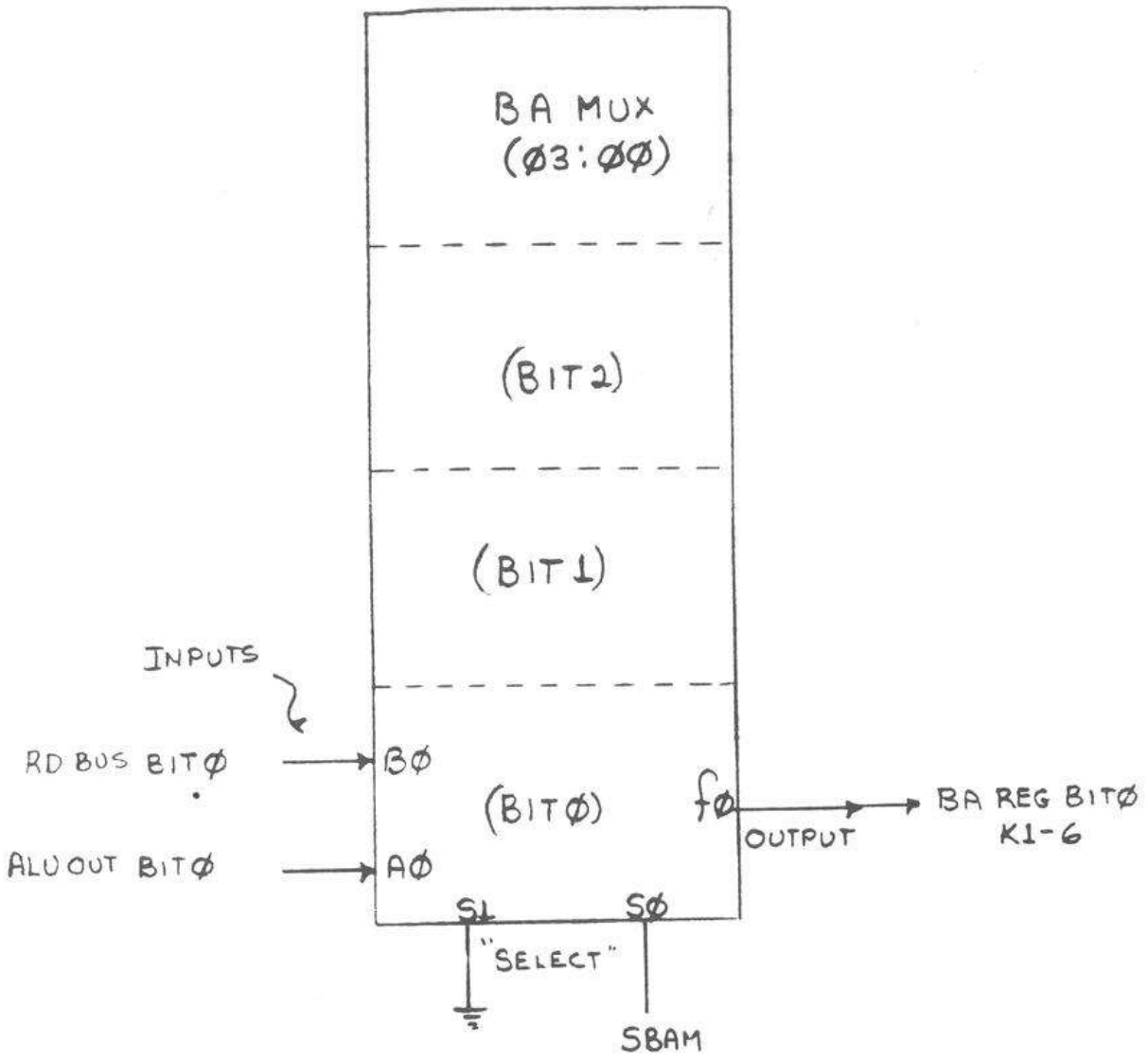
(SHEET K1-2)



S1	SØ	OUTPUT
Ø	Ø	RD BUS BITØ
Ø	1	BUS DATA BITØ
1	Ø	D REG BITØ
1	1	D REG BIT1

* SDM1/SDMØ = SELECT D MUX BITS FROM MICRO-WORD

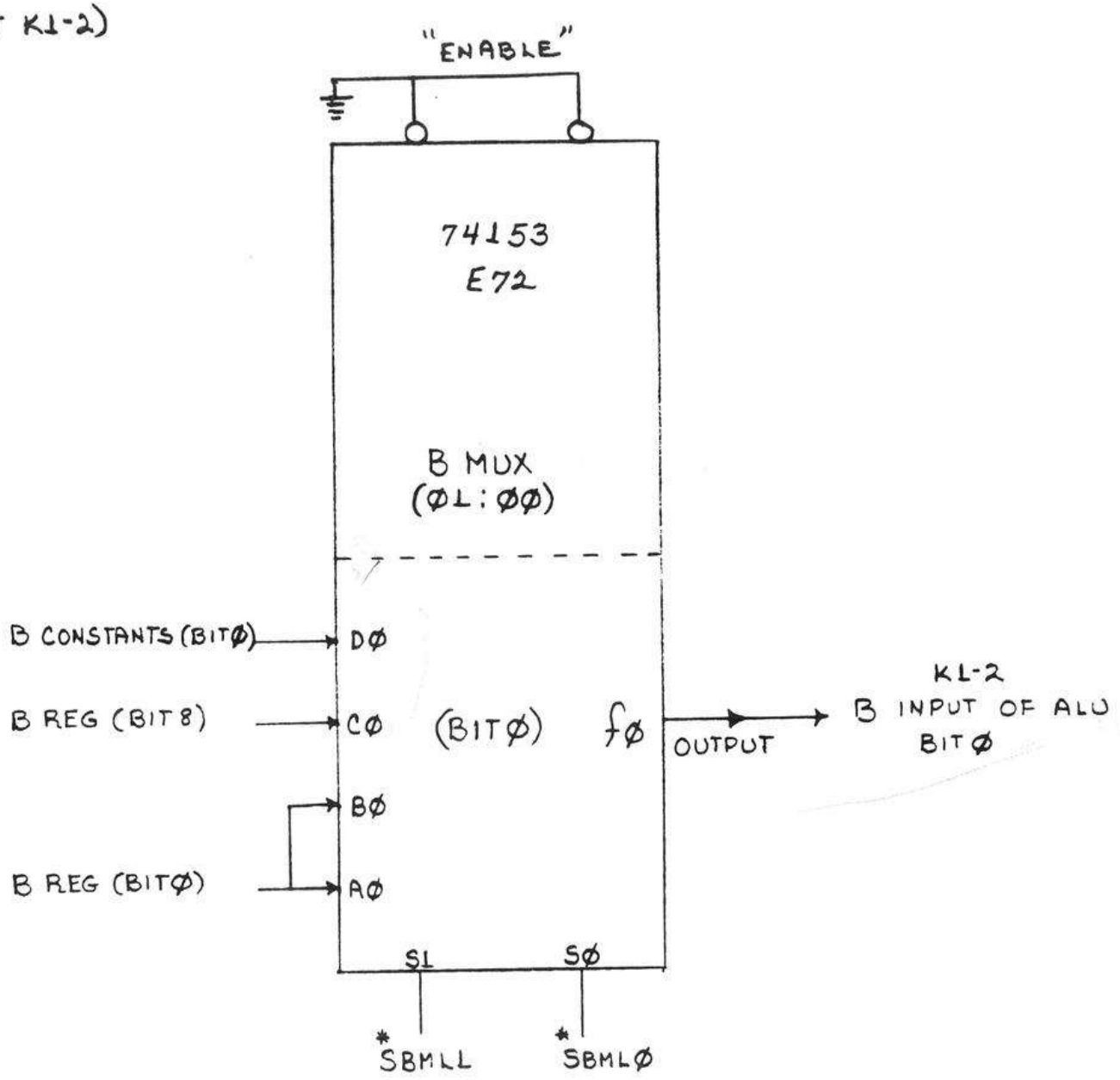
BA MULTIPLEXOR
(SHEET K1-2)



SBAM	OUTPUT
Ø	ALU OUT
1	RD BUS

NOTE: THIS MULTI PLEXOR
HAS NO ENABLE

B MULTIPLEXOR
(SHEET K1-2)

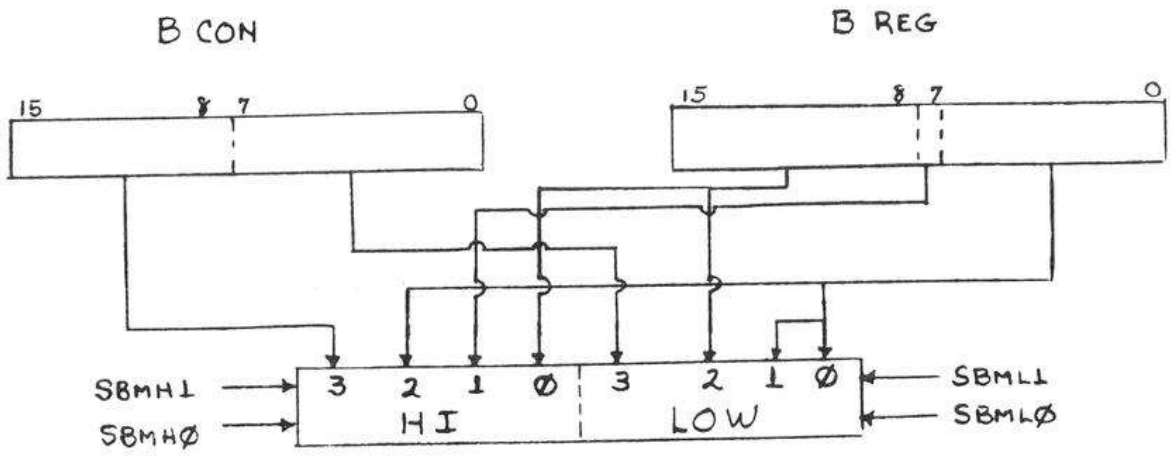


S1	SØ	OUTPUT
Ø	Ø	B REG BITØ
Ø	1	B REG BITØ
1	Ø	B REG BIT 8
1	1	B CONSTANT BITØ

* SBMLL/SBMLØ = SELECT B MUX LO BYTE FROM MICRO-WORD

SBMHL/SBMHØ ARE USED TO CONTROL INPUTS TO BMUX BITS 8→15 SEE SHEET K1-4

B MUX



	SBMH1	SBMHØ	SBML1	SBMLØ	
SBM ØØ	Ø	Ø	Ø	Ø	= B REG TO ALU
SBM Ø2	Ø	Ø	1	Ø	= DUPLICATE UPPER BYTE
SBM Ø5	Ø	1	Ø	1	= SIGN EXTEND
SBM 1Ø	1	Ø	Ø	Ø	= DUPLICATE LOW BYTE
SBM 12	1	Ø	1	Ø	= SWAP BYTES
SBM 17	1	1	1	1	= B CON TO ALU

4. ROM LOCATION ØØ6 SPECIFIES THAT THE _____ REGISTER SHALL BE DISPLAYED IN THE DATA LIGHTS OF THE CONSOLE. (REFER TO UWORD TABLES)

A- IR REGISTER
B- D REGISTER
C- GPR R-14
D- GPR R-13

5. WHICH OF THE BELOW ROM LOCATIONS SPECIFIES CLOCK LENGTH 3, DATI, CLOCK OFF

A. 3Ø6
B. 15Ø
C. Ø4Ø
D. 1Ø1

6. REFER TO OUTPUT OF THE CLOCK ON K4-2. THE SIGNAL PART P END H IS ACTIVE ON

A. P1 + P2 + P3
B. P1 + P3
C. P2 + P3
D. P1 + P2

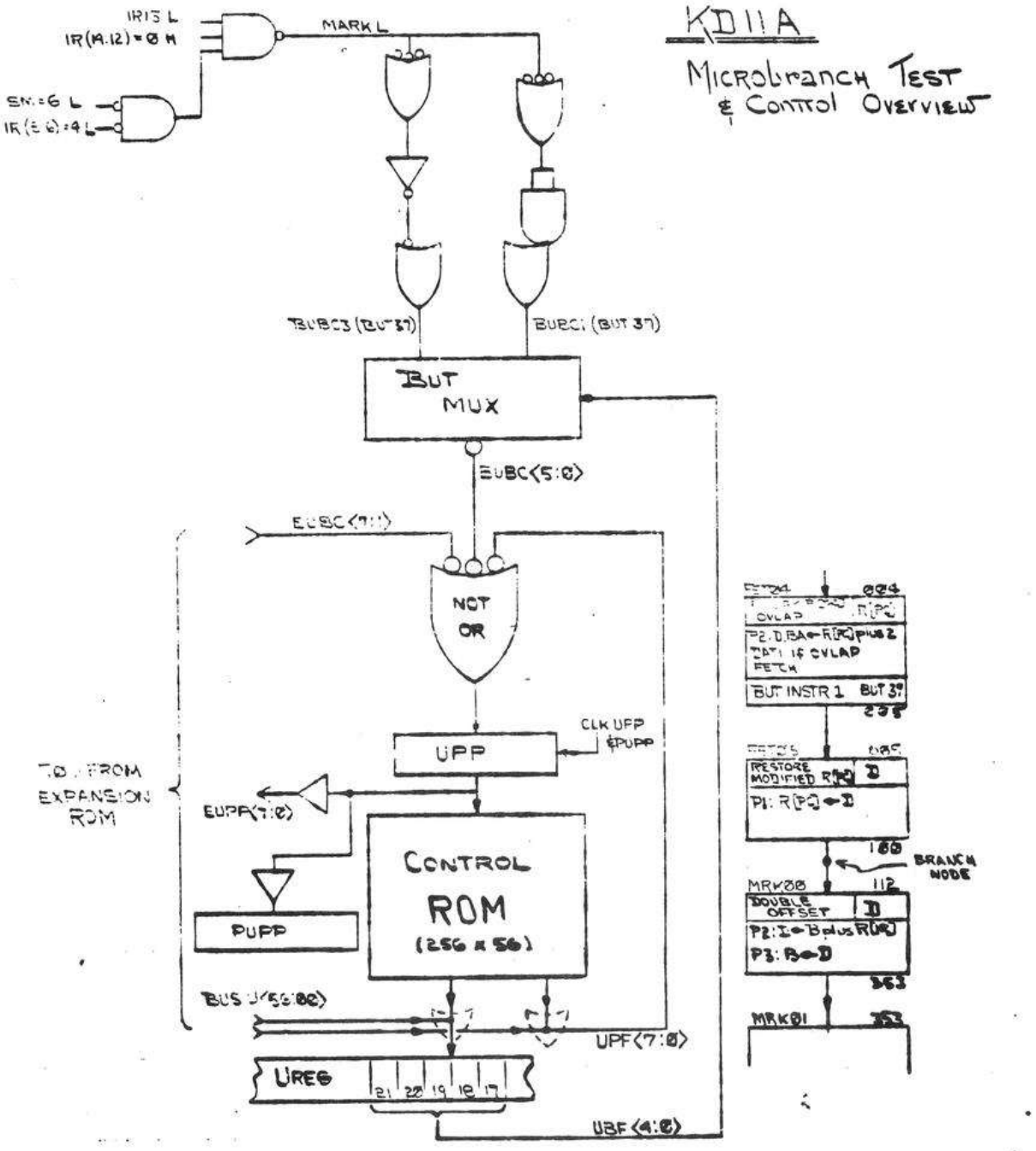
DAY 2

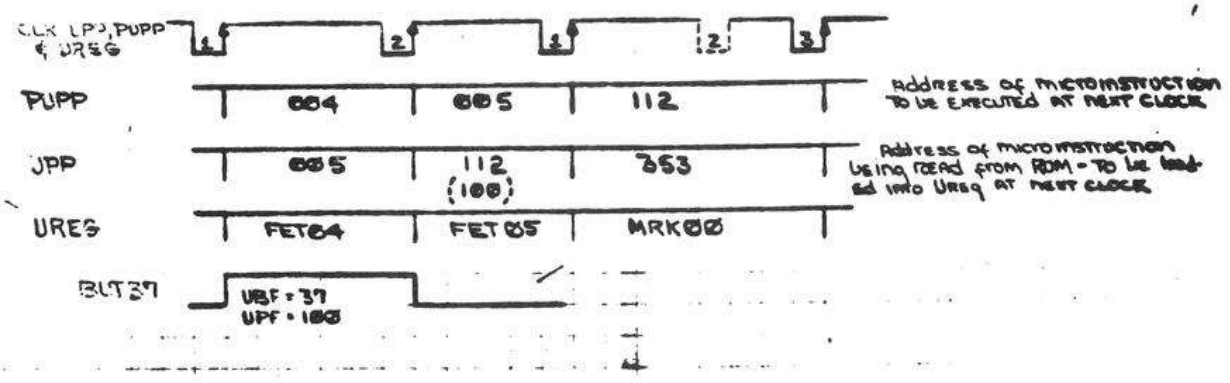
IR = MARK

15	14	13	12	11	10	9	8	7	6	5	0
2	2	2	2	1	1	0	1	0	2	x	x x x x x

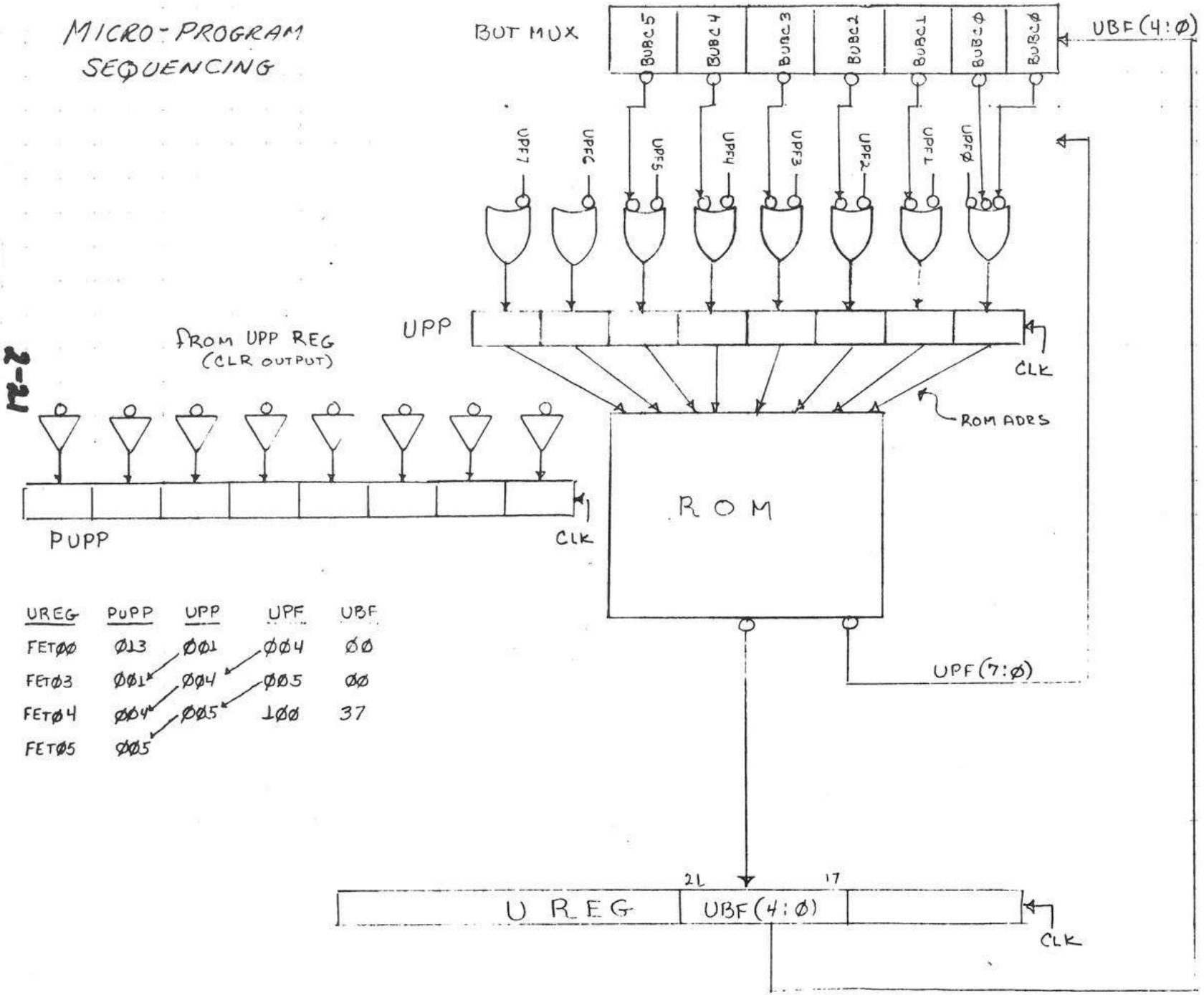
KD11A

Microbranch Test & Control Overview



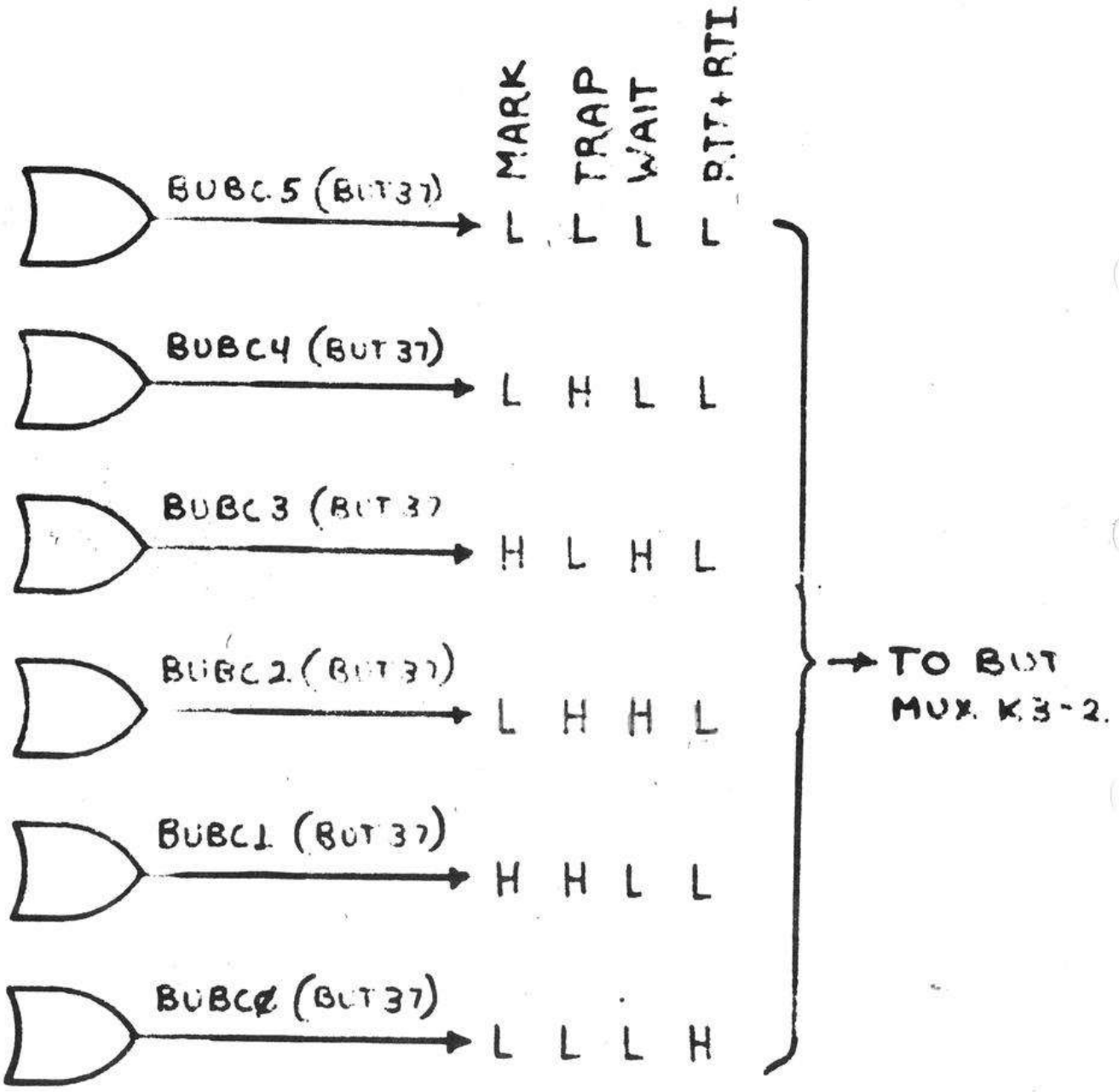


MICRO-PROGRAM SEQUENCING

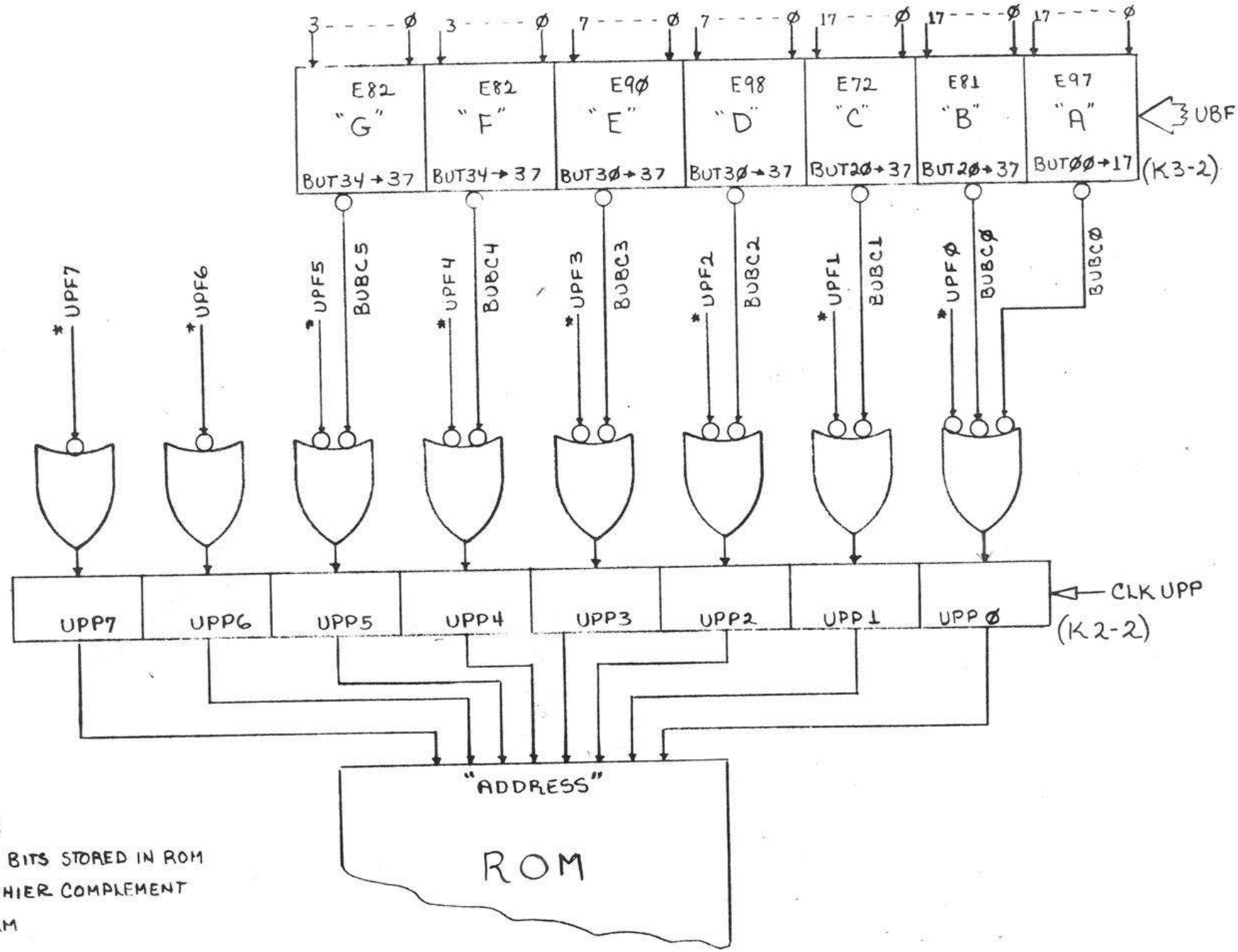


UREG	PUPP	UPP	UPF	UBF
FET00	013	001	004	00
FET03	001	004	005	00
FET04	004	005	100	37
FET05	005			

OUT PUT OF IR
DECODE TO CONTROL BUT MUX [K3-5]



MICRO-BRANCHING

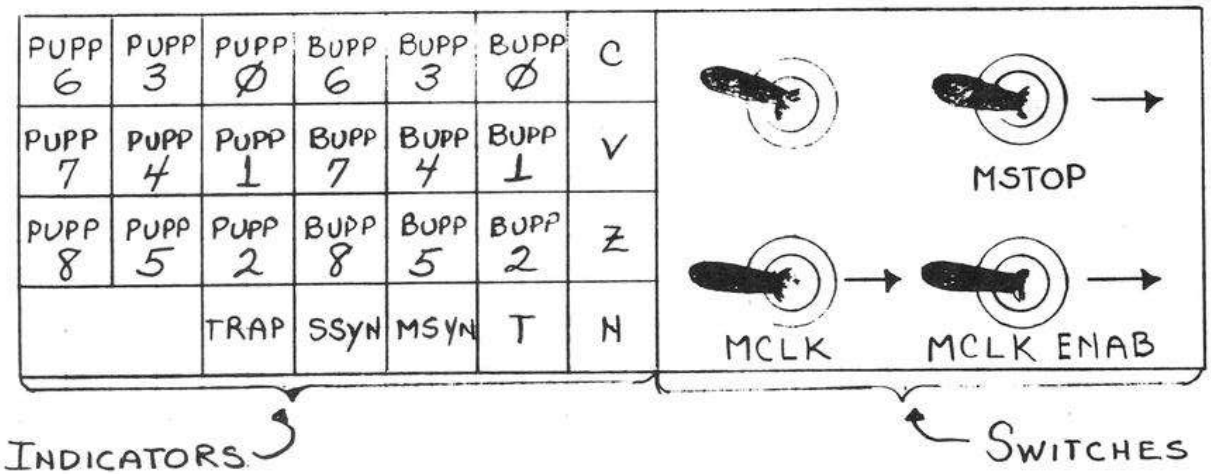


* NOTE:
UPF BITS STORED IN ROM
IN THIER COMPLEMENT
FORM

KD11-A

MAINTENENCE MODULE

{PLUGS INTO SLOT F1 OF KD11A}



PUPP ⟨8:Ø⟩ = ADDRESS OF THE MICRO-INSTRUCTION STORED IN U REG.

BUPP ⟨8:Ø⟩ = ADDRESS OF NEXT MICRO-INSTRUCTION BEING READ OUT

MSTOP = ALLOWS STOPPING THE PROCESSOR WHEN MATCH BUPP = SR ⟨8:Ø⟩

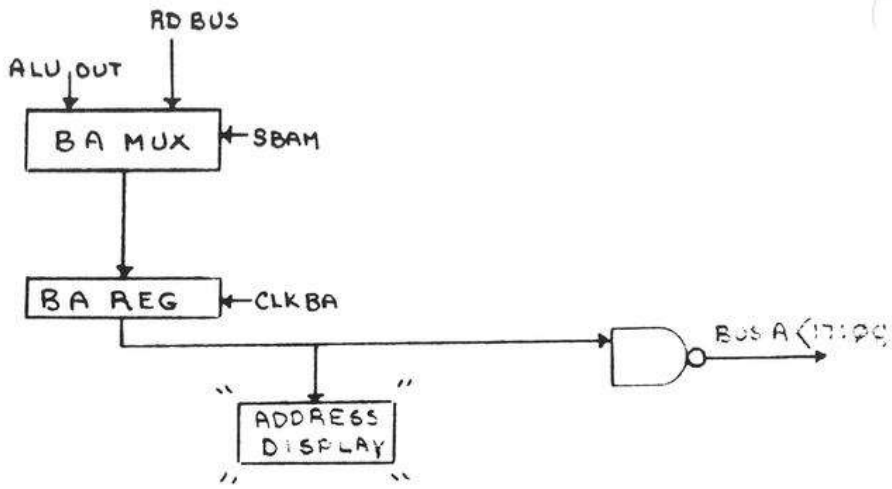
MCLK ENAB = DISABLES PROCESSOR CLOCK AND ALLOWS SINGLE CLOCKING THE MICRO-PROGRAM WITH MCLK SWITCH

MCLK = SINGLE CLOCK SWITCH, EACH TIME ON GENERATES ONE CLOCK CYCLE

DAY 3

Single Clock Display Rules

Address Display

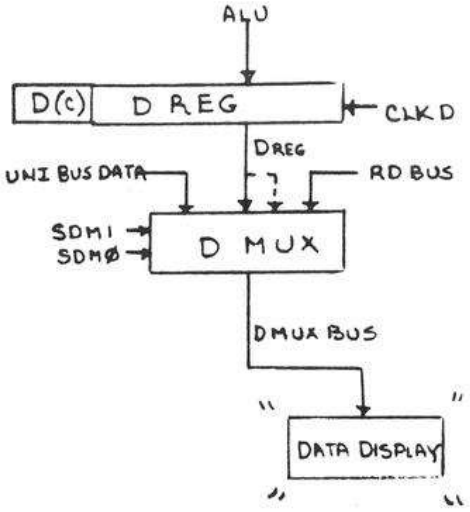


Since Address Display lights are fed directly by contents of BA Reg you need only determine the contents of BA Reg.

Rule:

If micro-word specifies BA ← X, you will not see X in BA nor will X be displayed in the address lights until the next clock pulse. The Address Lights will display the contents of BA Reg established in the last micro-word that altered the contents of BA Reg.

DATA DISPLAY



THE DATA DISPLAY LIGHTS ARE DRIVEN BY THE OUTPUT OF THE D MUX SINCE THE D MUX CAN BE SELECTED TO OUTPUT FROM ONE OF FOUR INPUTS, THE MICRO-WORD FLOWS WILL INDICATE WHICH INPUT LINE IS BEING DISPLAYED THE DATA DISPLAY SOURCE IS INDICATED IN THE SMALL BOX, UPPER RIGHT OF EACH MICRO-WORD OF THE FLOWS.

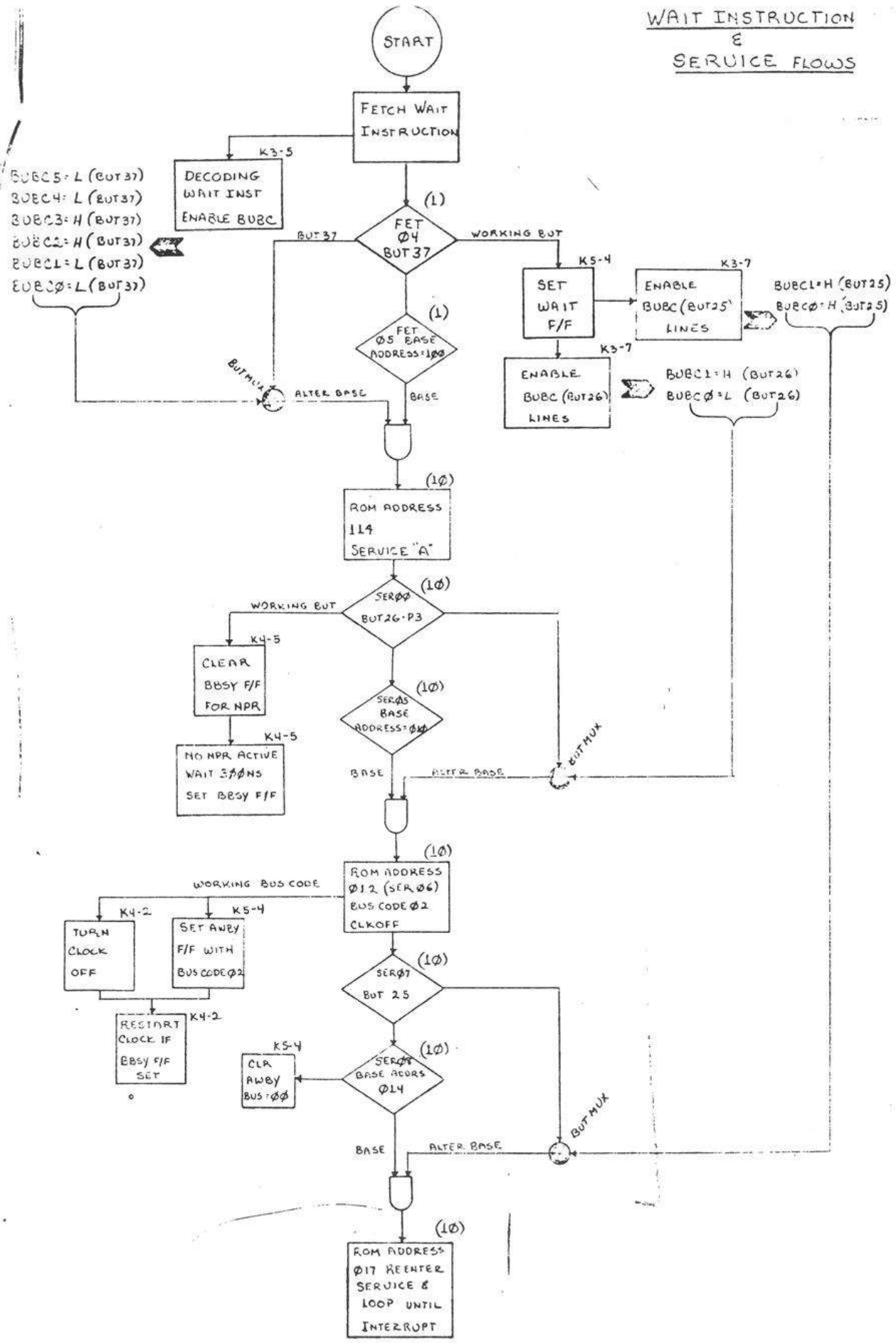
RULES:

IF THE DATA DISPLAY INDICATOR, IN THE MICRO-WORD, SPECIFIES UNI-BUS DATA OR ANY OF THE 16 GPRS, THAT DATA WILL BE DISPLAYED IN THAT MICRO-WORD.

IF THE DATA DISPLAY INDICATOR, IN THE MICRO-WORD, SPECIFIES DISPLAY D AND THAT MICRO-WORD ALSO SPECIFIES D ← X, X WILL NOT BE SEEN IN D NOR WILL IT BE DISPLAYED UNTIL THE NEXT CLOCK PULSE. THE DATA LIGHTS WILL DISPLAY THE VALUE IN D ESTABLISHED IN THE LAST MICRO-WORD THAT ALTERED THE CONTENTS OF D.

IF THE MICRO-WORD SPECIFIES DATI OR DATO, MSYN LIGHT ON THE KM11 MAINTENENCE MODULE WILL NOT LIGHT UNTIL NEXT CLOCK PULSE. YOU WILL NOTE THAT SSYN ON MAINTENENCE MODULE SHOULD ALSO BE LIGHTED WHEN MSYN IS ON.

WAIT INSTRUCTION & SERVICE FLOWS



BUBC1 & BUBCØ TRANSLATOR (K3-7)

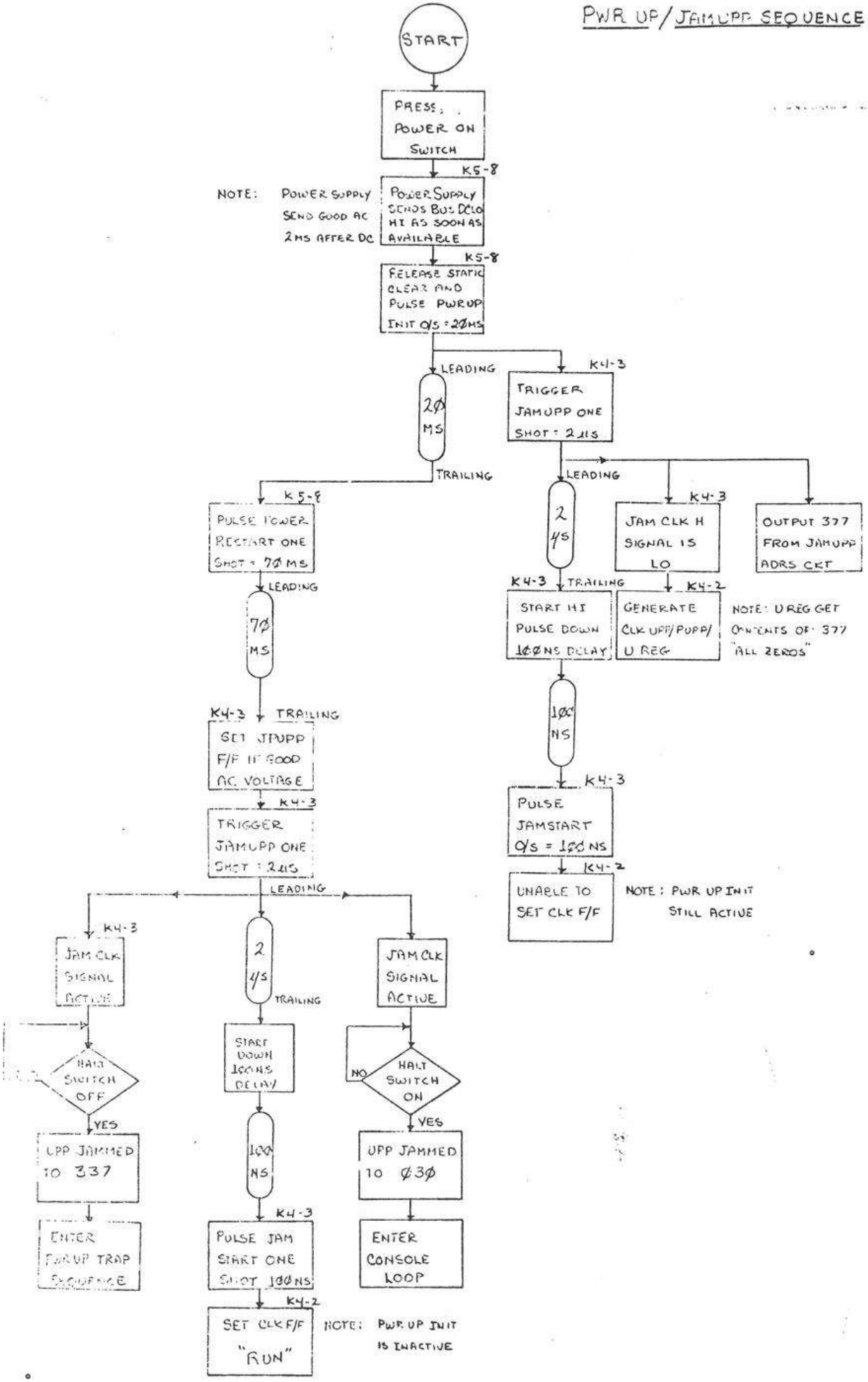
(FOR USE IN SERVICE FLOW)

CONDITION	BUBC1 (BUT26)	BUBCØ (BUT26)	BASE ADDRS	BRANCH ADDRS
BERR PS(T) OVFLW PWRDWN	Lo	Lo	Ø1Ø	Ø1Ø TRAP A
CBR	Lo	Hi	Ø1Ø	Ø11 CONSOLE B
BR+WAIT	Hi	Lo	Ø1Ø	Ø12 SER Ø6
No Rost	Hi	Hi	Ø1Ø	Ø13 FETCH A

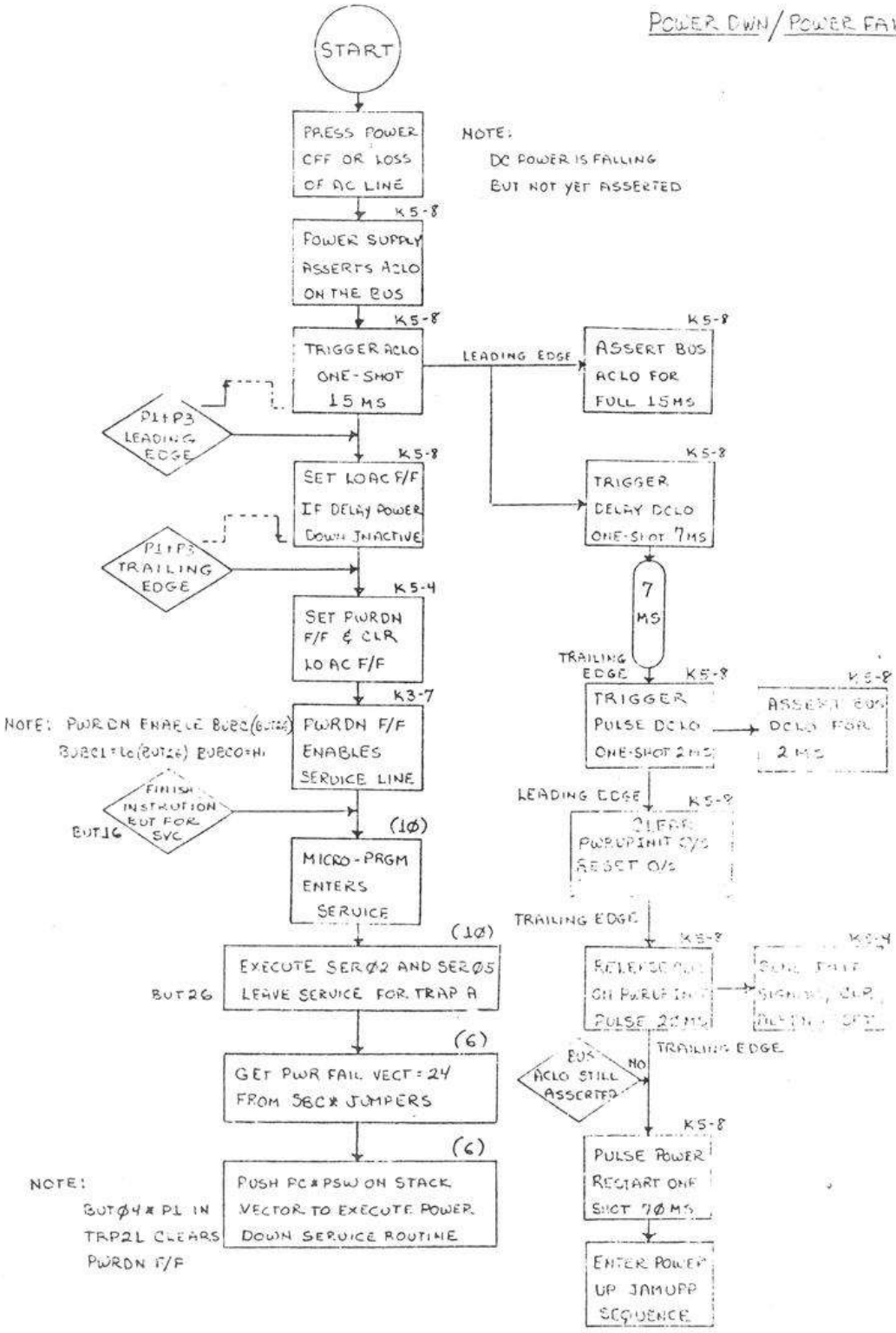
CONDITION	BUBC1 (BUT25)	BUBCØ (BUT25)	BASE ADDRS	BRANCH ADDRS
BR	Lo	Lo	Ø14	Ø14 SER Ø9
WAIT	Hi	Hi	Ø14	Ø17 SERVICE C
No Rost	Hi	Lo	Ø14	Ø16 FETCH C

DAY 4

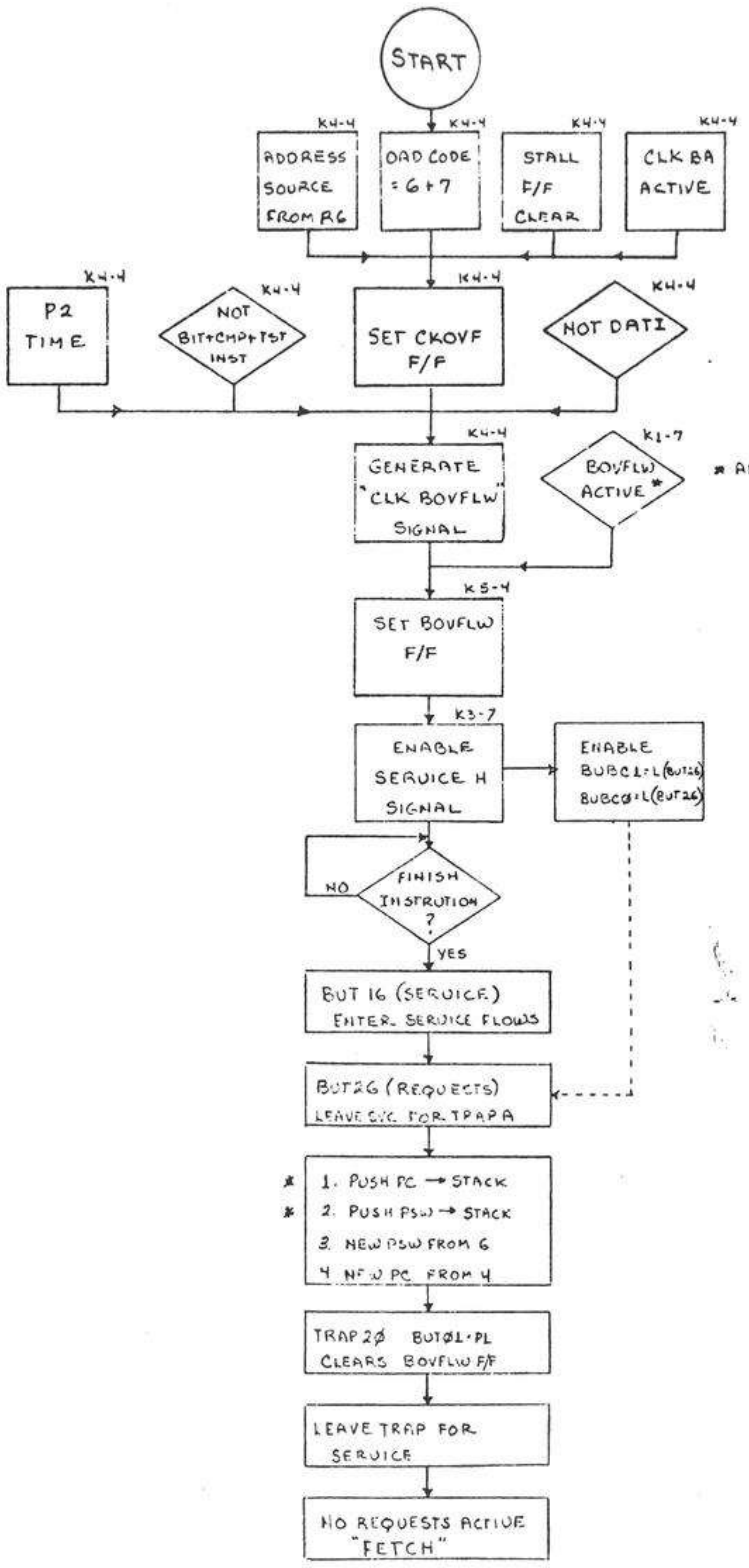
PWR UP/JAMUPP SEQUENCE



POWER DWN/POWER FAIL



YELLOW ZONE STACK OVERFLOW

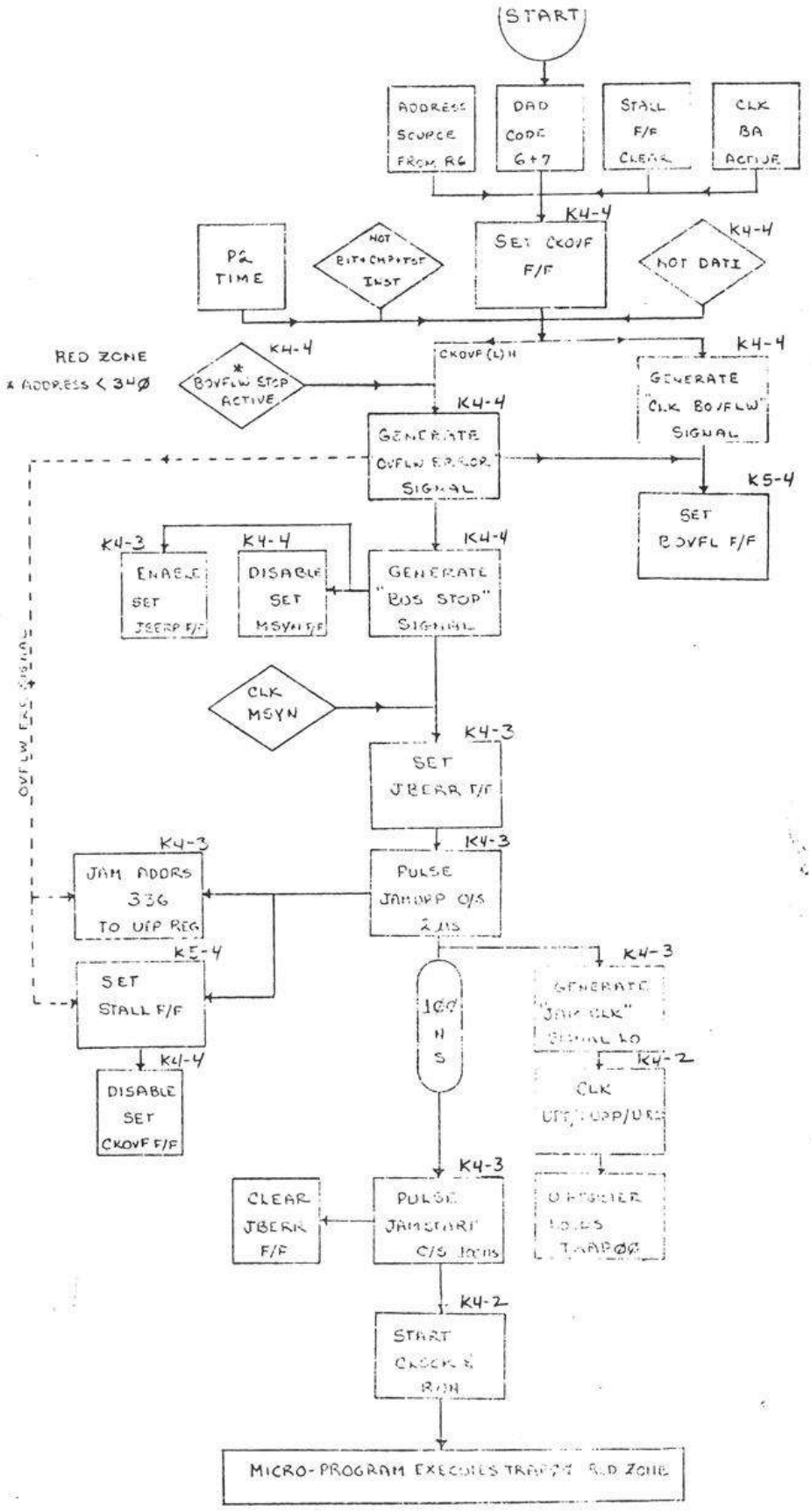


YELLOW ZONE
* ADDRESS < 400 BUT > 336

* NOTE

TWO ADDITIONAL PUSHES ON THE STACK ARE DONE IN THE YELLOW ZONE TRAP ROUTINE AND ARE SENSED BY CKOVF F/F BUT DO NOT MATTER UNLESS A RED ZONE VIOLATION OCCURS DURING YELLOW ZONE PUSH

STACK OVERFLOW



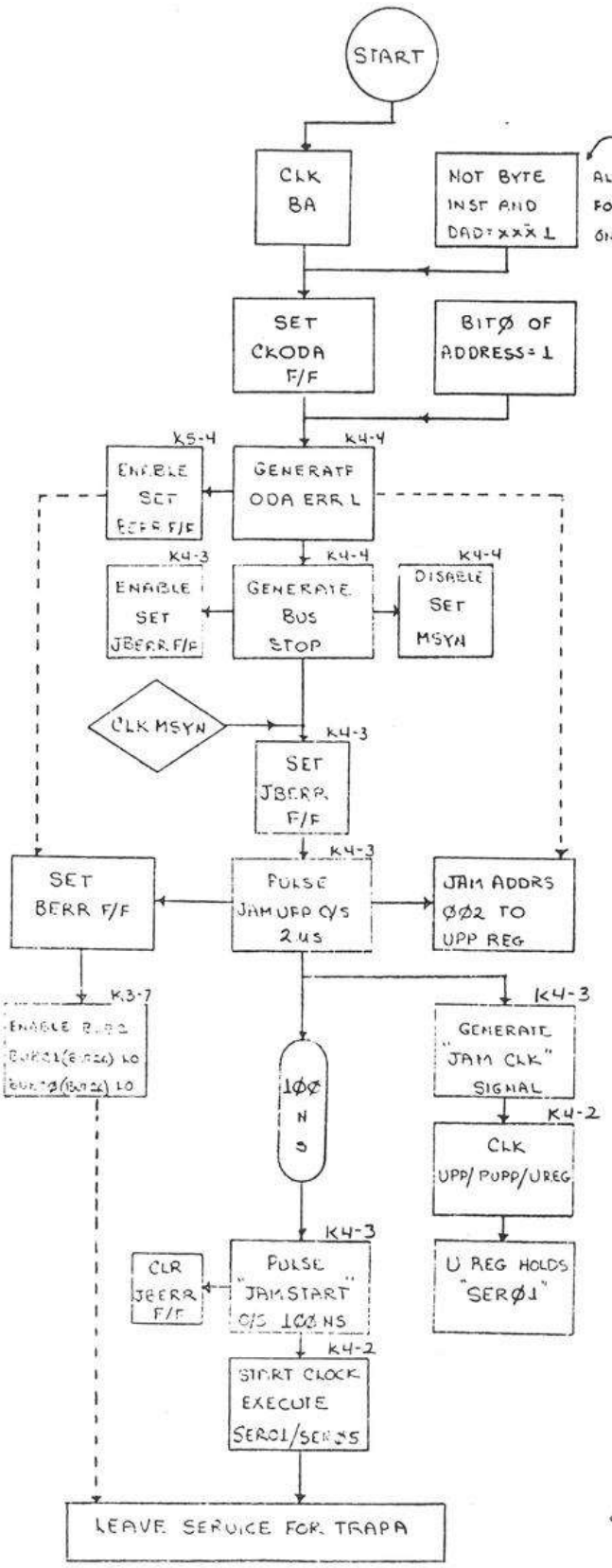
NOTE:

CLKBAIN TRPØ2 CLEARS CKOVF F/F (STAYS CLEAR AS LONG AS STALL F/F SET)

BUTØ1 * PL IN TRP2Ø CLEARS BOVFL F/F

BUTØ4 * PL IN TRP21 CLEARS STALL F/F (ENABLES SENSING OVFLW)

ODD ADDRESS ERROR



NOTE

BERR F/F IS CLEARED BY BUT03 · PL IN TRP16
IF ANOTHER ODA OCCURS UP TO THIS POINT
YOU HAVE A DOUBLE BUS ERROR (DUBBER)

PDP11/40 Quiz
Trouble Isolation

ANALYZE THE PROBLEM SYMPTOMS GIVEN BELOW AND IN EACH CASE, GIVE AT LEAST ONE IC (MODULE NUMBER, CHIP NUMBER AND PIN NUMBER) THAT COULD CAUSE THE PROBLEM.

1. THE CLOCK IS DISABLED BY THE MAINTENENCE BOARD (KM11). YOU POWER UP THE PROCESSOR WITH THE HALT/ENABLE SWITCH IN THE HALT POSITION. UPP IS JAMMED TO ROM LOCATION 337 INSTEAD OF 30.

2. YOU ARE USING MAINT. MODULE TO SINGLE CLOCK THE CONSOLE FUNCTIONS. NO MATTER WHICH SWITCH YOU DEPRESS, YOU DISCOVER THAT ROM ALWAYS STAYS IN THE CONSOLE LOOP (26→46→26→46) ROM WILL NOT GO TO LOCATION 27 WHEN YOU DEPRESS A CONSOLE CONTROL SWITCH.

3. YOU ARE SINGLE CLOCKING THE PROCESSOR TO CHECK OUT THE LOAD ADDRESS SEQUENCE. THE SEQUENCE IS NORMAL UNTIL PUPP GOES TO 051, HERE YOU NOTE THE CONSOLE ADDRESS LIGHTS INDICATE A 17.

4. WHEN SINGLE CLOCKING THE PROCESSOR THRU A HALT INSTRUCTION, YOU HAVE NORMAL INDICATIONS UNTIL PUPP = ØØ5, HERE YOU NOTE THAT UPP GOES TO 114 INSTEAD OF 122, WHICH IS THE REQUIRED SEQUENCE FOR A HALT.

FOR QUESTIONS 5 - 9 ASSUME THAT YOU ARE SINGLE CLOCKING THE SUBTRACT INSTRUCTION SHOWN BELOW:

5ØØ- SUB #2Ø, @ (3)+
5Ø2 - 2Ø
5Ø4 - HALT

R3 = 3ØØØ
3ØØØ = 5ØØØ
5ØØØ = 4Ø

5. IN THE VERY FIRST STEP OF FETCH [FETØ2, LOC 16] WE NOTE THAT THE CONSOLE ADDRESS LIGHTS INDICATE A 3ØØØ INSTEAD OF 5ØØ.

6. NORMAL INDICATION ON THE FIRST THREE ROM STATES BUT WHEN WE CLOCK IN FETØ5, WE NOTE THE CONSOLE DATA LIGHTS INDICATE A 5Ø3

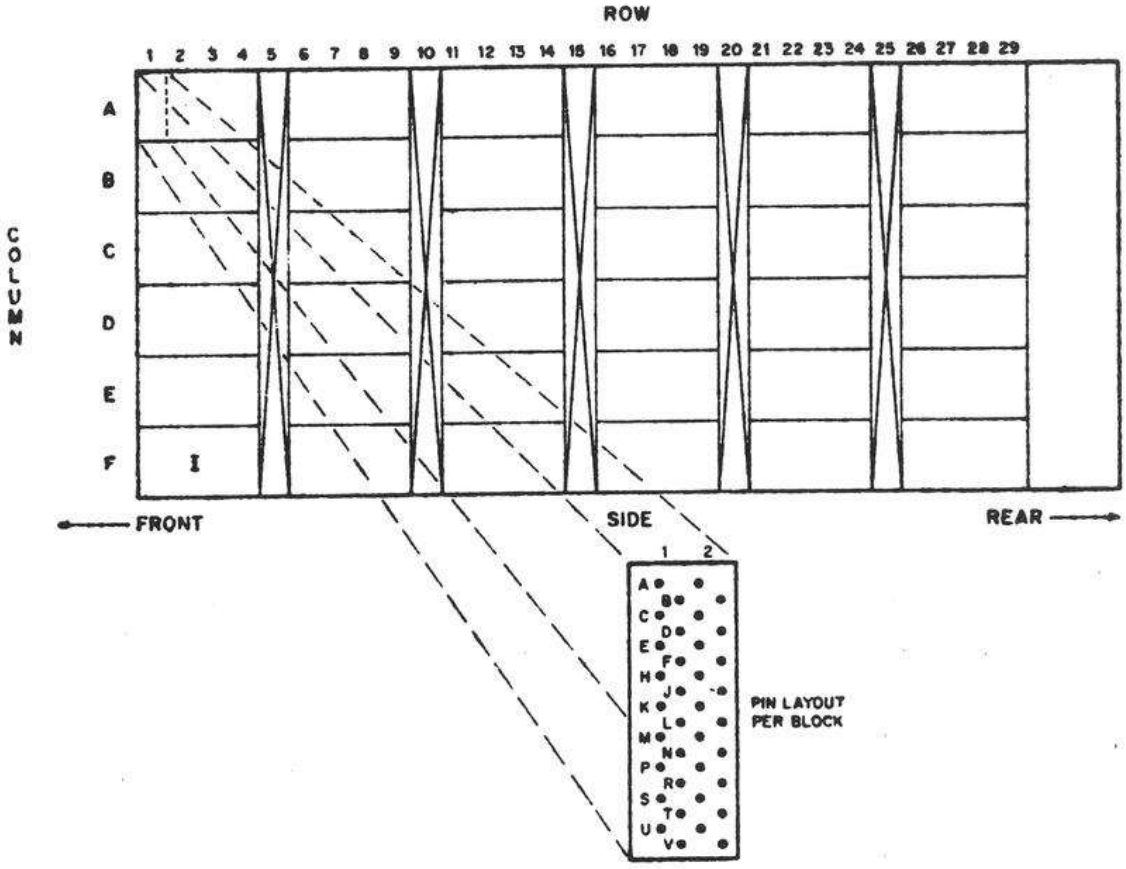
7. NORMAL INDICATIONS UNTIL WE CLOCK IN SRC15 LOC 25Ø. HERE WE NOTE THAT UPP GOES TO 137 INSTEAD OF 162.

8. NORMAL INDICATIONS UNTIL WE CLOCK IN DOP12 LOCATION 367. HERE WE NOTE THE CONSOLE DATA LIGHTS INDICATE A 17

9. IN THE LAST MKRO-WORD DOP20, LOC 375 WE NOTE THAT THE "C" BIT INDICATOR ON THE MAINT MODULE IS LIGHTED.

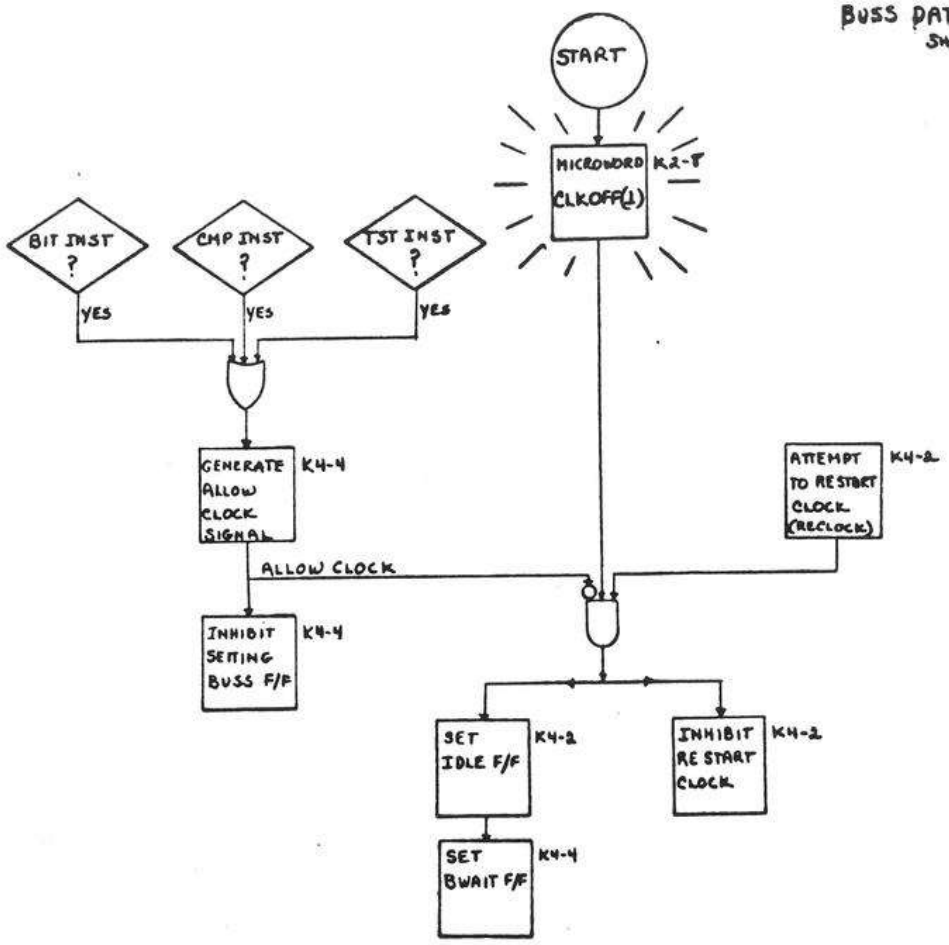
1. JAMUPP PROBLEM
2. BUT PROBLEM
3. SBC PROBLEM
4. IR DECODE PROBLEM
5. GDR ADDRESS SWITCH
6. INSERTED CARRY ON PC UPDATE
7. GETTING FALSE ODD BYTE SIGNAL
8. GETTING ONE'S COMPLEMENT INSTEAD OF TWO'S COMP
9. PSW "C" SHOULD SET IF OVFLW ON SUBTRACT

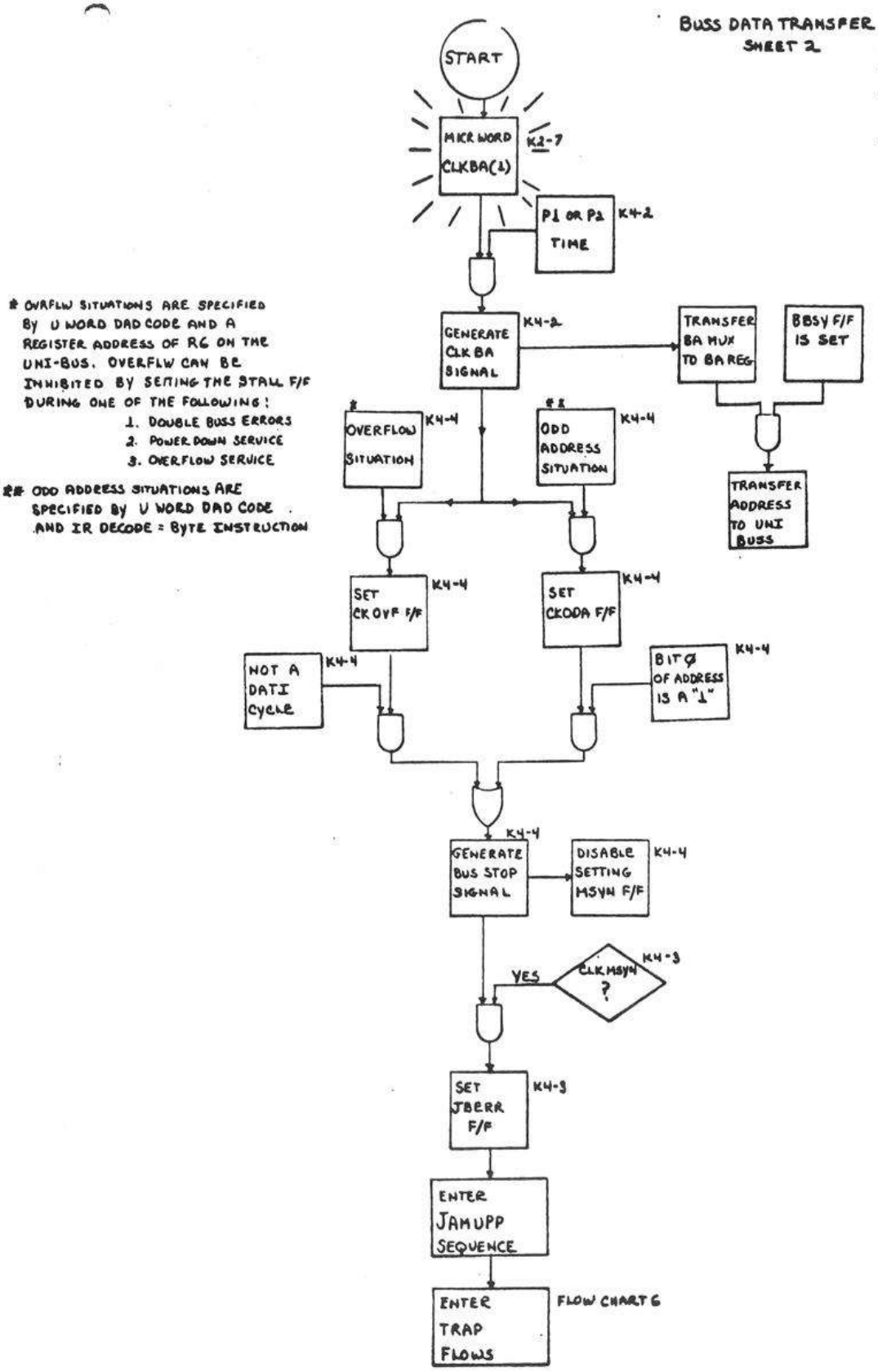
PDP-11 MODULE BLOCK AND PIN LAYOUT



PIN SIDE VIEW

DAY 5

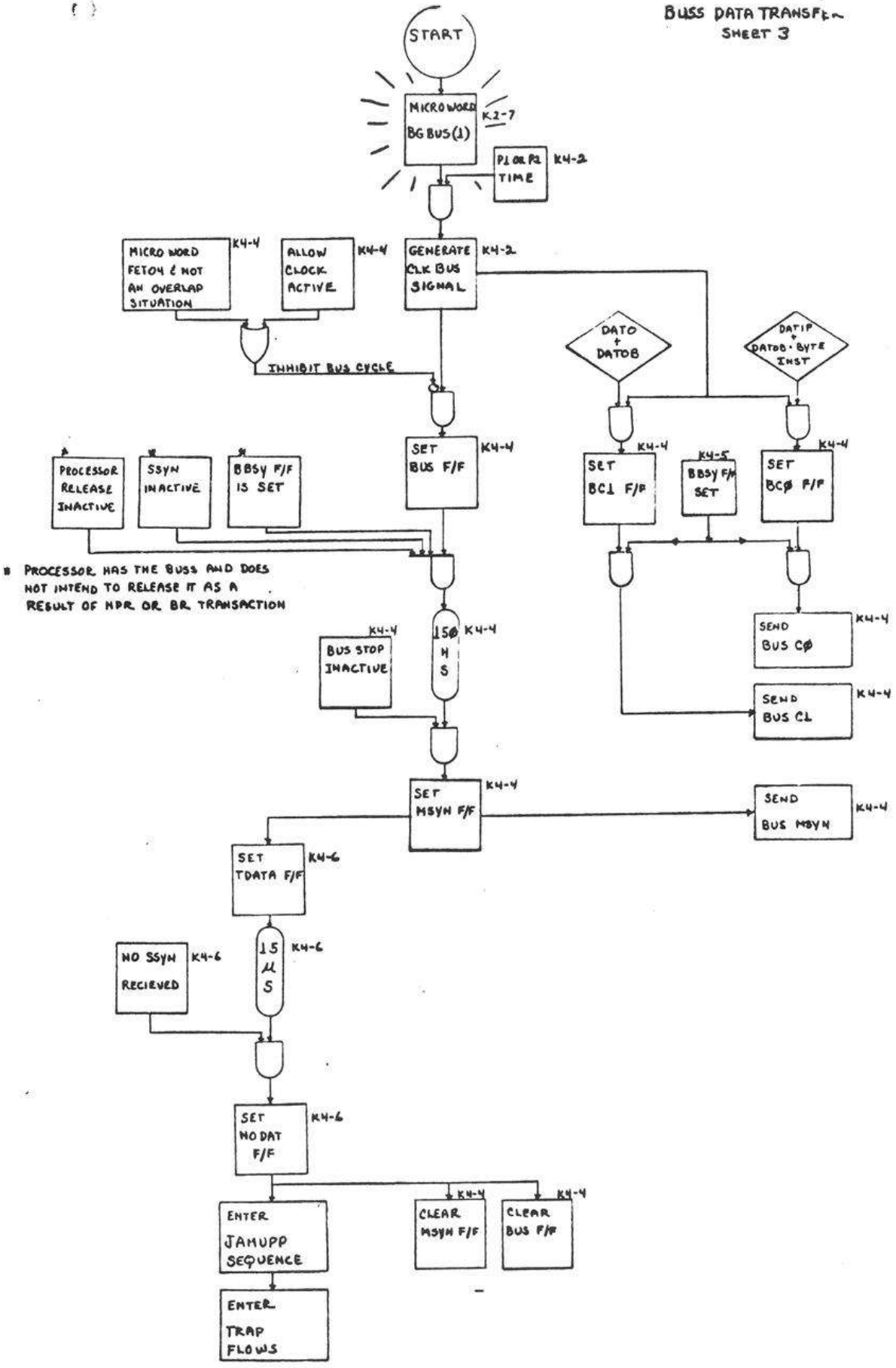

START
MICROWORD CLKOFF(1)
K2-5
BIT INST ?
CMP INST ?
TST INST ?
YES
YES
YES
GENERATE ALLOW CLOCK SIGNAL
K4-4
ATTEMPT TO RESTART CLOCK (RECLOCK)
K4-2
ALLOW CLOCK
INHIBIT SETTING BUSS F/F
K4-4
SET IDLE F/F
K4-2
INHIBIT RE START CLOCK
K4-2
SET BWAIT F/F
K4-4

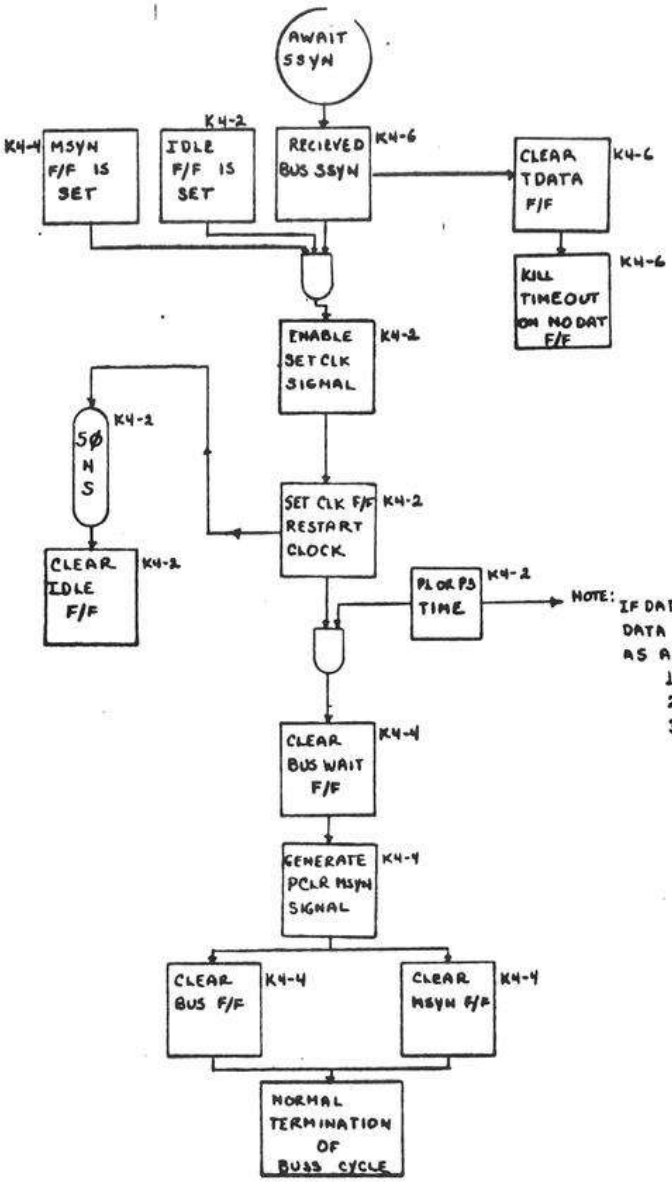


* OVRFLW SITUATIONS ARE SPECIFIED BY U WORD DAD CODE AND A REGISTER ADDRESS OF RG ON THE UNI-BUS. OVERFLW CAN BE INHIBITED BY SETING THE STALL F/F DURING ONE OF THE FOLLOWING:

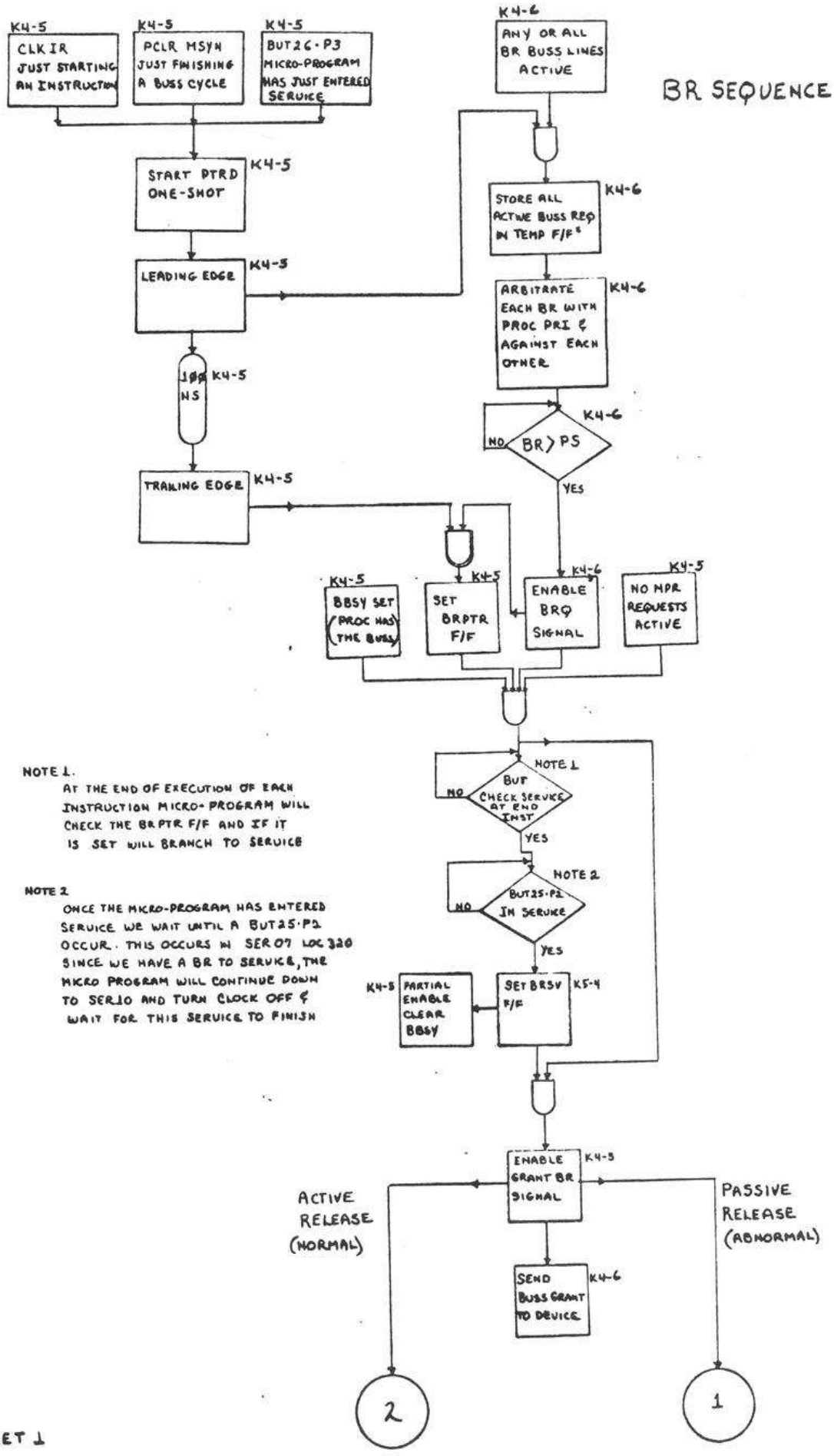
1. DOUBLE BUSS ERRORS
2. POWER DOWN SERVICE
3. OVERFLOW SERVICE

** ODD ADDRESS SITUATIONS ARE SPECIFIED BY U WORD DAD CODE AND IR DECODE = BYTE INSTRUCTION


START
MICRO WORD BG BUS (1)
K2-7
P1 OR P2 TIME
K4-2
MICRO WORD FETCH & NOT AN OVERLAP SITUATION
K4-4
ALLOW CLOCK ACTIVE
K4-4
GENERATE CLK BUS SIGNAL
K4-2
INHIBIT BUS CYCLE
DATO + DATOB
DATIP + DATOB · BYTE INST
PROCESSOR RELEASE INACTIVE
SSYN INACTIVE
BBSY F/F IS SET
SET BUS F/F
K4-4
SET BCL F/F
K4-4
BBSY F/F SET
K4-5
SET BCØ F/F
K4-4
PROCESSOR HAS THE BUSS AND DOES NOT INTEND TO RELEASE IT AS A RESULT OF NPR OR BR TRANSACTION
BUS STOP INACTIVE
K4-4
150 NS
K4-4
SEND BUS CØ
K4-4
SEND BUS CL
K4-4
SET MSYN F/F
K4-4
SEND BUS MSYN
K4-4
SET TDATA F/F
K4-6
NO SSYN RECIEVED
K4-6
15 µS
K4-6
SET NO DAT F/F
K4-6
ENTER JAMUPP SEQUENCE
CLEAR MSYN F/F
K4-4
CLEAR BUS F/F
K4-4
ENTER TRAP FLOWS


AWAIT SSYN
K4-4 MSYN F/F IS SET
K4-2 IDLE F/F IS SET
RECIEVED BUS SSYN K4-6
CLEAR TDATA F/F K4-6
KILL TIMEOUT ON NO DAT F/F K4-6
ENABLE SET CLK SIGNAL K4-2
50 NS K4-2
SET CLK F/F RESTART CLOCK K4-2
CLEAR IDLE F/F K4-2
P1 OR P3 TIME K4-2
NOTE: IF DATIP CYCLE, CLOCK UNI-BUS DATA INTO TEMPORARY STORAGE AS A FUNCTION OF U WORD
1. B REG
2. GPR
3. I REG
CLEAR BUS WAIT F/F K4-4
GENERATE PCLR MSYN SIGNAL K4-4
CLEAR BUS F/F K4-4
CLEAR MSYN F/F K4-4
NORMAL TERMINATION OF BUSS CYCLE

BR SEQUENCE



NOTE 1.

AT THE END OF EXECUTION OF EACH INSTRUCTION MICRO-PROGRAM WILL CHECK THE BRPTR F/F AND IF IT IS SET WILL BRANCH TO SERVICE

NOTE 2

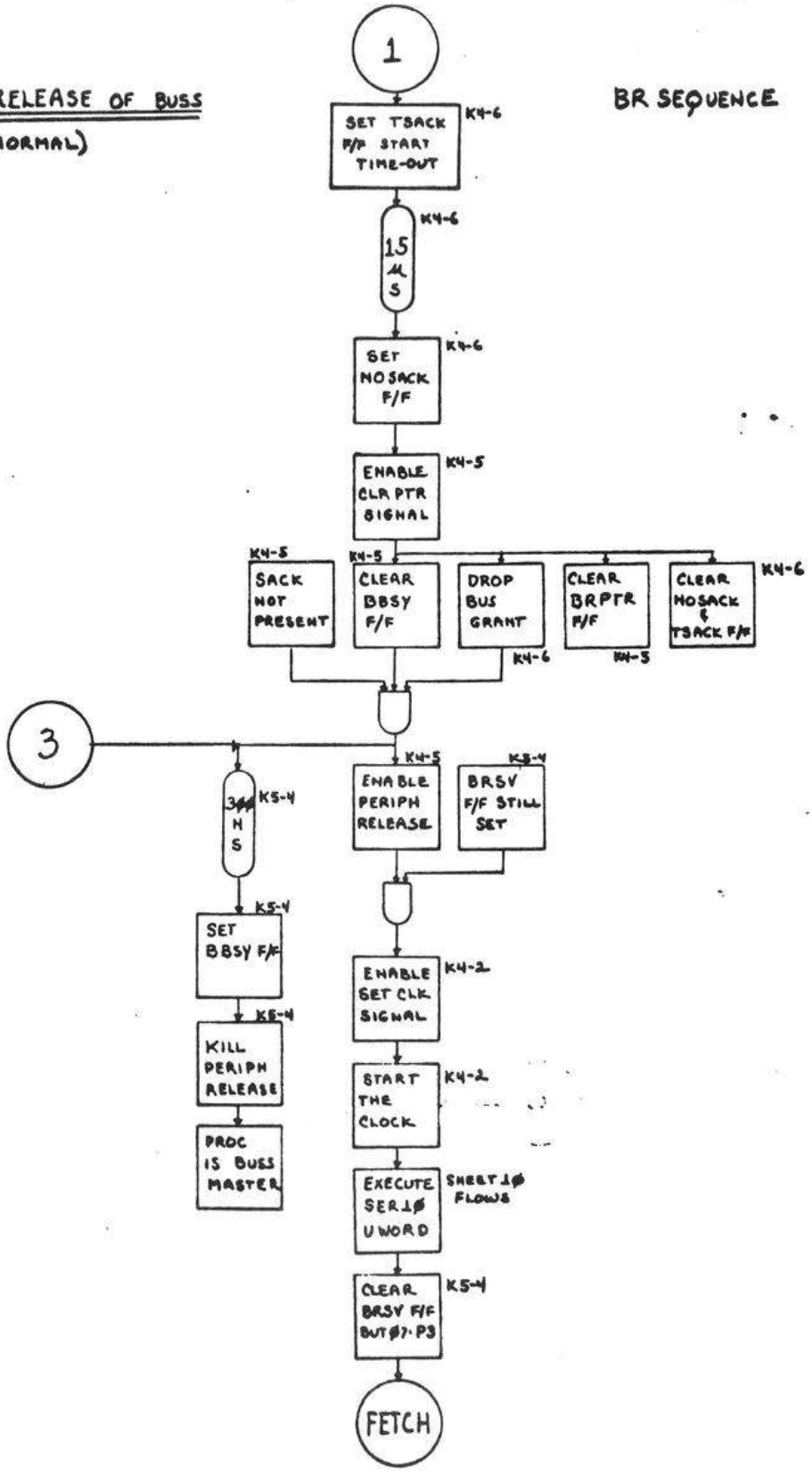
ONCE THE MICRO-PROGRAM HAS ENTERED SERVICE WE WAIT UNTIL A BUT25·P2 OCCUR. THIS OCCURS IN SER07 LOC 320 SINCE WE HAVE A BR TO SERVICE, THE MICRO PROGRAM WILL CONTINUE DOWN TO SER10 AND TURN CLOCK OFF & WAIT FOR THIS SERVICE TO FINISH

SHEET 1

PASSIVE RELEASE OF BUSS

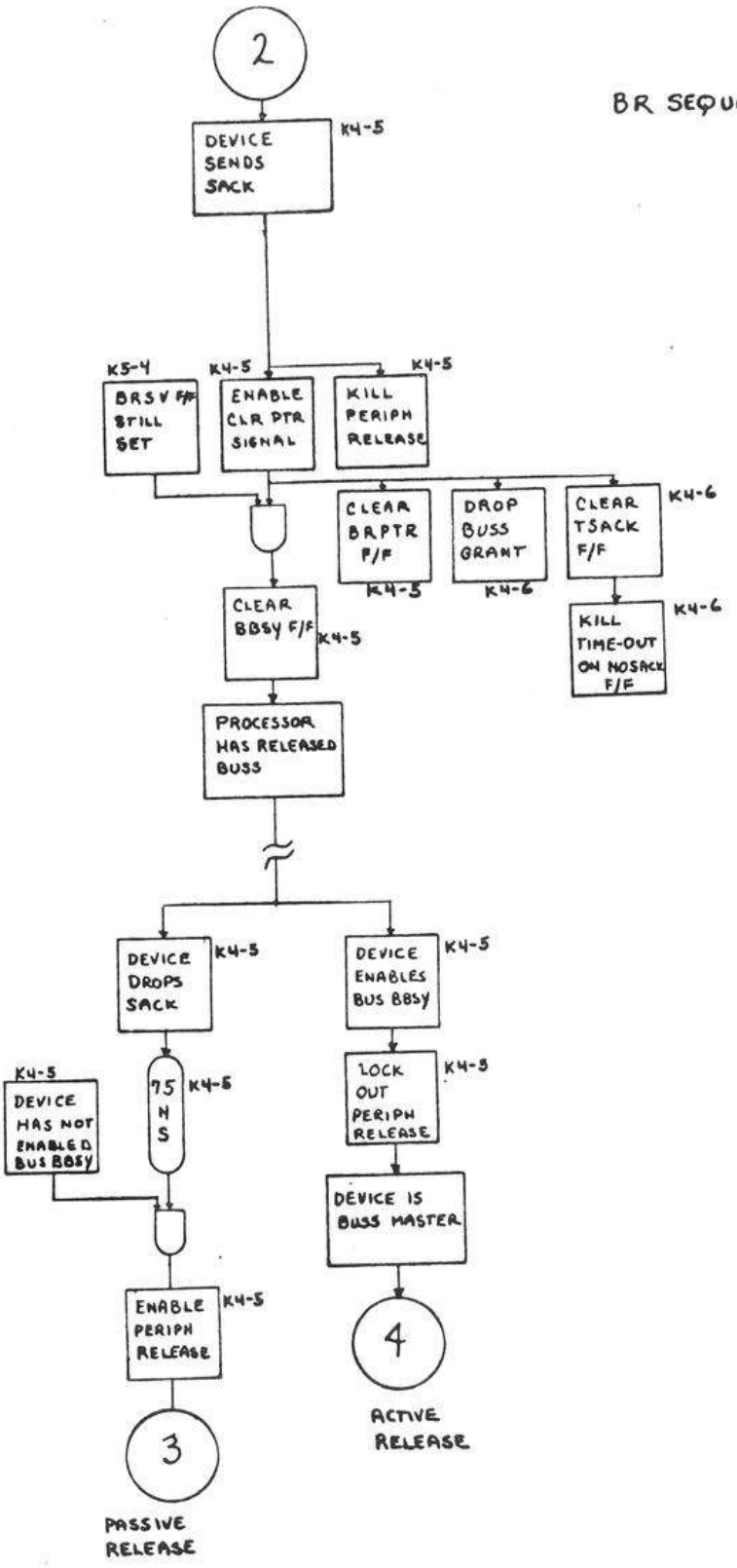
(ABNORMAL)

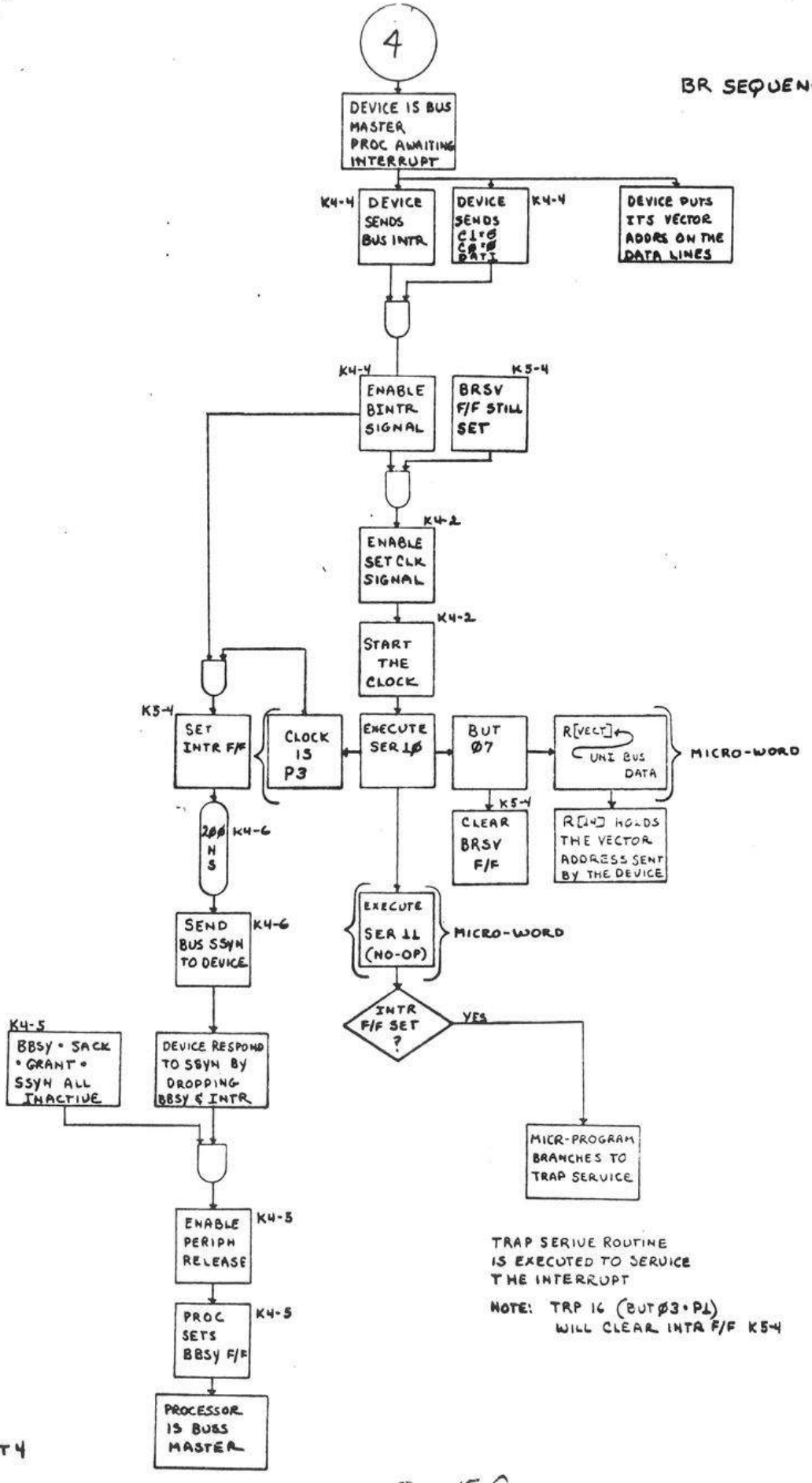
BR SEQUENCE



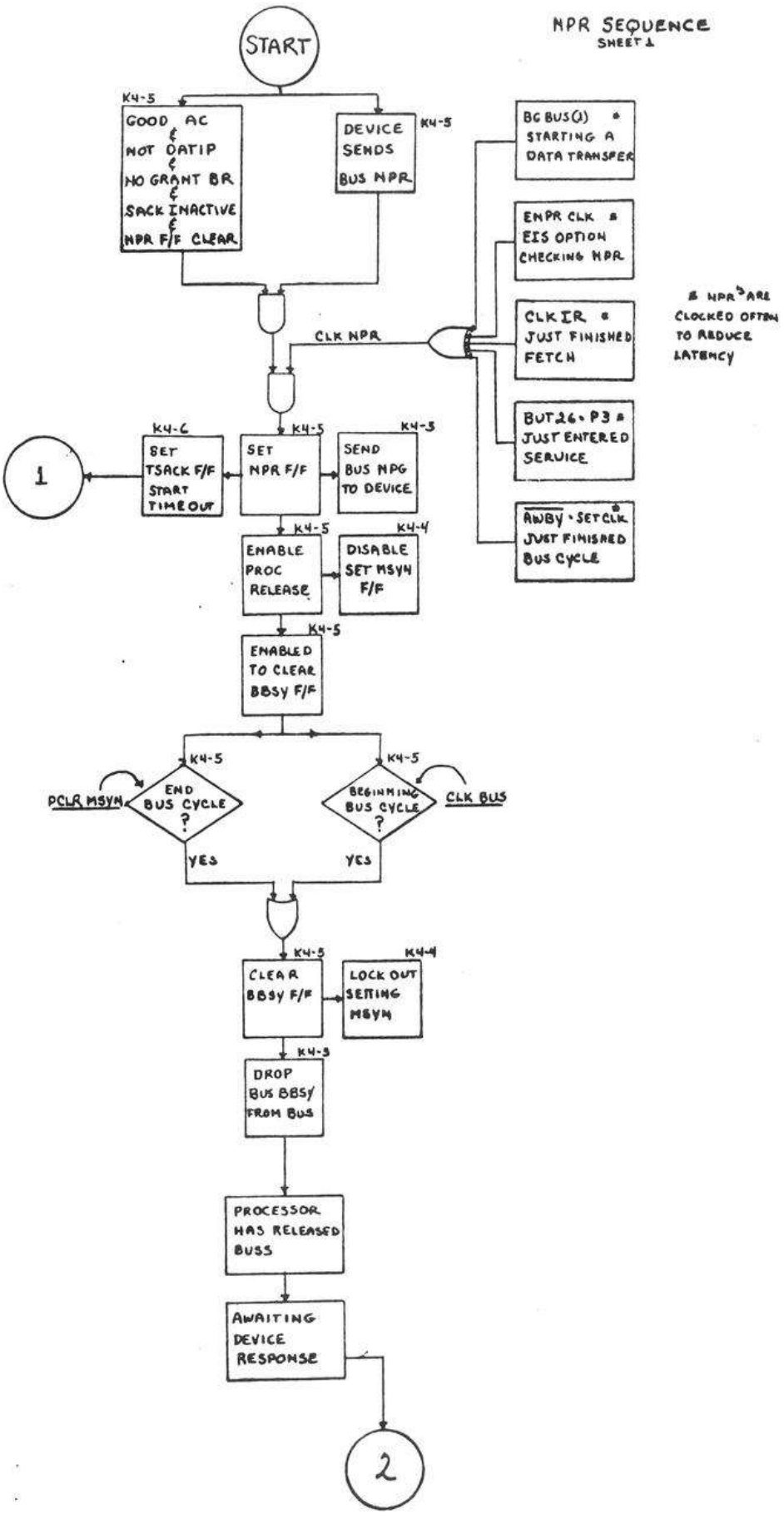
SHEET 2

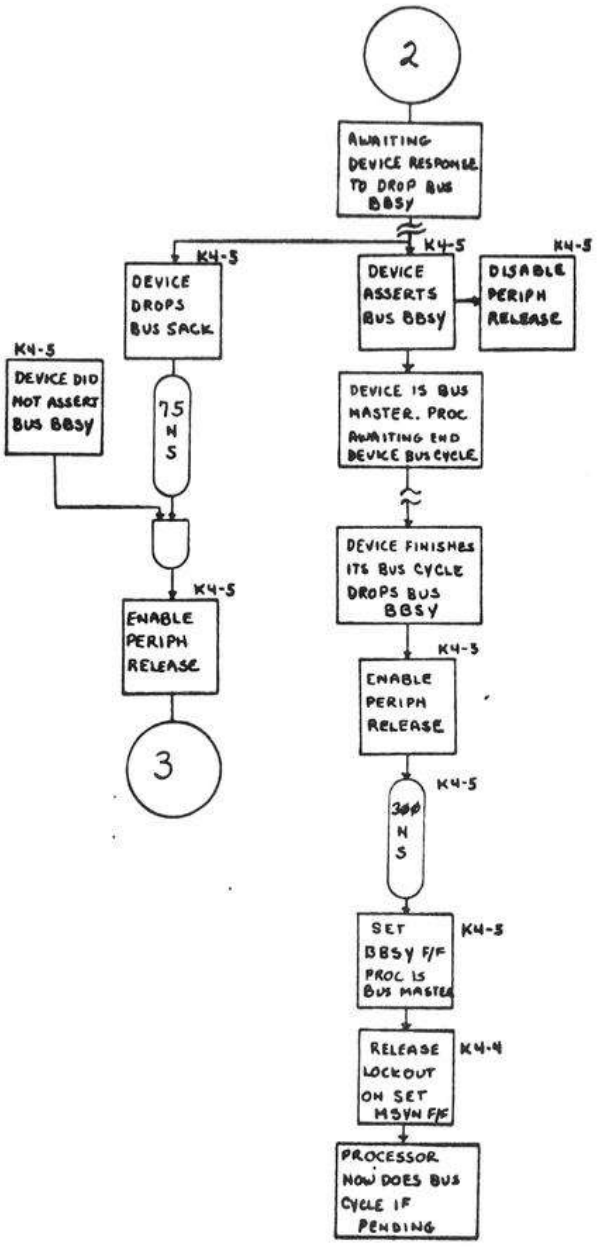
BR SEQUENCE


2
DEVICE SENDS SACK
K4-5
K5-4
BRSV F/F STILL SET
K4-5
ENABLE CLR PTR SIGNAL
K4-5
KILL PERIPH RELEASE
CLEAR BRPTR F/F
K4-5
DROP BUSS GRANT
K4-6
CLEAR TSACK F/F
K4-6
KILL TIME-OUT ON NOSACK F/F
K4-6
CLEAR BBSY F/F
K4-5
PROCESSOR HAS RELEASED BUSS
DEVICE DROPS SACK
K4-5
DEVICE ENABLES BUS BBSY
K4-5
K4-5
DEVICE HAS NOT ENABLED BUS BBSY
75 NS
K4-5
LOCK OUT PERIPH RELEASE
K4-5
DEVICE IS BUSS MASTER
ENABLE PERIPH RELEASE
K4-5
4
ACTIVE RELEASE
3
PASSIVE RELEASE


4
BR SEQUENCE
DEVICE IS BUS MASTER PROC AWAITING INTERRUPT
K4-4
DEVICE SENDS BUS INTR
DEVICE SENDS C1=0 C0=0 BATT
K4-4
DEVICE PUTS ITS VECTOR ADDRS ON THE DATA LINES
K4-4
ENABLE BINTR SIGNAL
K5-4
BRSV F/F STILL SET
K4-2
ENABLE SET CLK SIGNAL
K4-2
START THE CLOCK
K5-4
SET INTR F/F
CLOCK IS P3
EXECUTE SER 1Ø
BUT Ø7
R[VECT] UNI BUS DATA
MICRO-WORD
K5-4
CLEAR BRSV F/F
R[4] HOLDS THE VECTOR ADDRESS SENT BY THE DEVICE
200 NS K4-6
SEND BUS SSYN TO DEVICE K4-6
EXECUTE SER 11 (NO-OP)
MICRO-WORD
INTR F/F SET ?
YES
K4-5
BBSY • SACK • GRANT • SSYN ALL INACTIVE
DEVICE RESPOND TO SSYN BY DROPPING BBSY & INTR
MICR-PROGRAM BRANCHES TO TRAP SERVICE
ENABLE PERIPH RELEASE K4-5
PROC SETS BBSY F/F K4-5
PROCESSOR IS BUSS MASTER
TRAP SERIVE ROUTINE IS EXECUTED TO SERVICE THE INTERRUPT
NOTE: TRP 16 (BUTØ3•P1) WILL CLEAR INTR F/F K5-4
SHEET 4

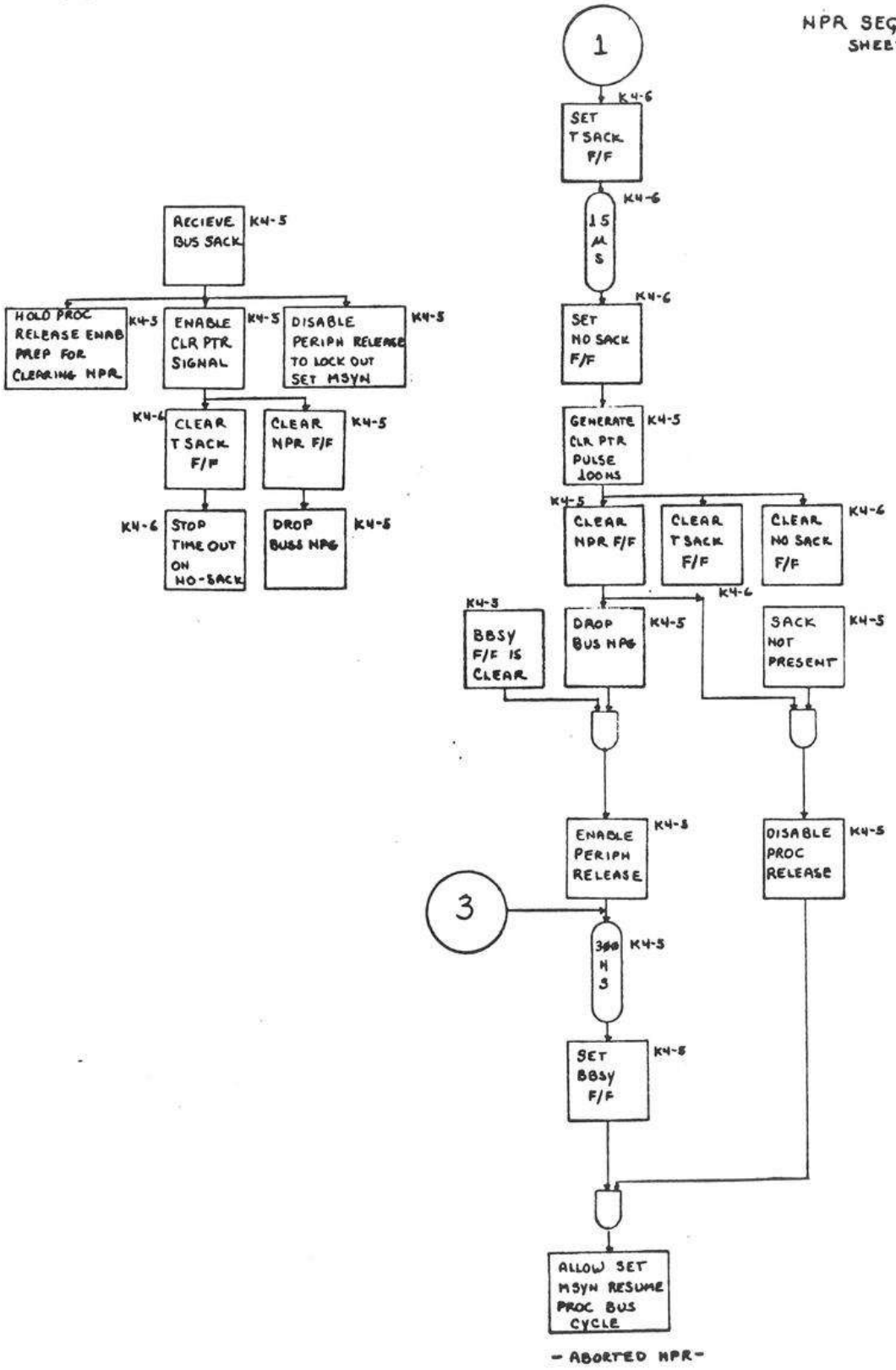
NPR SEQUENCE
SHEET 1





NORMAL TERMINATION

NPR SEQUENCE
SHEET 3



PDP 11/40

WEEK 2

EXAM

1. TO DISPLAY THE UNI-BUS DATA LINES ON THE CONSOLE DATA DISPLAY, BITS U<24:23> OF THE UWORD MUST PROGRAMMED AS:

A. ØØ
B. Ø1
C. 1Ø
D. 11

2. THE MICRO-INSTRUCTION SHOWN BELOW IS BEING EXECUTED. WHAT IS THE STATE OF UREG <16:Ø9> ?

A. ØØ11Ø1Ø1
B. 1ØØ11Ø Ø1
C. ØØØ11ØØ1
D. ØØ1Ø1Ø1Ø

P1: B, R[SOURCE] ← D

3. DURING THE MICRO-INSTRUCTION THAT ENABLES DELIVERING THE RESULTS OF THE INSTRUCTION SHOWN BELOW, WHAT WOULD BE THE STATE OF WRH(1) AND WRL(J) (REFER TO K2-7)

A. H, H
B. H, L
C. L, H
D. L, L

6ØØ MOVB (1), %2

R1 = 5Ø3

4. WHICH OF THE FOLLOWING ELEMENTARY OPERATIONS DICTATES THAT A CLOCK LENGTH OF THREE MUST BE SPECIFIED?

A. D ← R[SP] MINUS 2

B. R[PC] ← D

C. R[SF] ← UNIBUS DATA

D. R[PC] ← R[PC] PLUS 2

5. WHICH OPERATION SHOWN BELOW REQUIRES TWO MICRO-INSTRUCTIONS TO EXECUTE?

A. R[PC] ← R[PC] PLUS 2

B. D ← R[DEST] PLUS UNIBUS DATA

C. B ← R[SOURCE]

D. BA ← R[SF] PLUS B

6. REFER TO K3-2 PRINT. THE MICRO-INSTRUCTION BEING EXECUTED IS ENCODED TO BUT JMP+JSR. WHICH BUT MULTIPLEXOR CHIP IS SELECTED

A. E82

B. E72

C. E81

D. E97

7. THE MICRO-INSTRUCTION PRESENTLY BEING EXECUTED SPECIFIES A CLOCK LENGTH OF THREE. THE NEXT MICRO-INSTRUCTION WILL BE CLOCKED INTO THE UREG AT THE:

A. LEADING EDGE OF P2

B. TRAILING EDGE OF P3

C. LEADING EDGE OF P3

D. TRAILING EDGE OF P2

BEFORE ANSWERING QUESTIONS 8 THRU 10 COMPLETE A MICRO-PROGRAM WORKSHEET FOR THE INSTRUCTION SHOWN BELOW. START AT FETØ2 AND INCLUDE ALL MICRO-INSTRUCTIONS FROM START TO FINISH.

→ 5ØØ - CMP 7Ø2, (3) R2 = 35Ø
5Ø2 - HALT R3 = 5ØØ

8. IF YOU MANUALLY CLOCK THE MICRO-PROGRAM UNTIL PUPP = 267, YOU SHOULD OBSERVE _____ IN THE BUPP LIGHTS OF THE MAINTENENCE MODULE?

A. 266

B. 22Ø

C. 225

D. 224

9. IF YOU MANUALLY CLOCK UNTIL PUPP = 367 YOU SHOULD OBSERVE _____ IN THE DATA LIGHTS ON THE CONSOLE?

A. 020213
B. 060134
C. 160035
D. 160135

10. WHAT SHOULD BE IN THE CONSOLE ADDRESS DISPLAY WHEN PUPP = 161

A. 476
B. 500
C. 502
D. 504

11 YOU ARE MANUALLY CLOCKING THE MICRO-PROGRAM TO VERIFY THE INSTRUCTION SHOWN BELOW. THE NEXT MICRO-WORD EXECUTED AFTER SSL03 SHOULD BE

A. DOP16
B. DOP17
C. DOP18
D. DOP19

INCB %2
R2 = 100

12. DURING EXECUTION OF A ROLB INSTRUCTION, WHICH DATA FACILITY DOES THE ACTUAL SHIFTING?

A. B MUX

B. D MUX

C B REG

D ALU

13. THE INSTRUCTION SHOWN BELOW IS BEING SINGLE CLOCKED. THE BUT INST L IN FETØ4 SHOULD ACTIVATE MICRO-BRANCH CONTROL SIGNALS

A. BUBCØ AND BUBC1

RTS 3

B. BUBC1 AND BUBC2

C. BUBC3 AND BUBC4

D. BUBC2 AND BUBC4

14 REFER TO SHEET 3 OF FLOWS. DURING EXECUTION OF THE MICRO-INSTRUCTION TAGGED DST16, WHAT SHOULD BE THE STATE OF SBMLL AND SBMLØ ON K2-5

A. L, L

B. H, L

C. L, H

D. H, H

15. CONSIDER THE PRINCIPLE OF MICRO-BRANCHING USED IN THE KD-11A. IF A MICRO-WORD HAS A BASE ADDRESS OF 37Ø, HOW MANY ADDRESS PATHS ARE OPEN TO US IN ADDRESSING THE NEXT MICRO-WORD. ASSUME BUT37

A. 2
B. 3
C. 6
D. 8

16. WHEN SINGLE CLOCKING THE MARK INSTRUCTION, YOU STOP THE SEQUENCE WITH PUPP=354. IF YOU SCOPED SDML(1) AND SDMØ(1) ON K2-5 YOU WOULD EXPECT TO OBSERVE

A. HIGH, HIGH
B. LOW, LOW
C. HIGH, LOW
D. LOW, HIGH

17. YOU ARE CHECKING OUT THE DEPOSIT OPERATION BY DEPOSITING ALL ONES INTO LOCATION 5ØØ. YOU MANUALLY CLOCK UNTIL PUPP=67. WHAT SHOULD YOU OBSERVE IN THE CONSOLE ADDRESS DISPLAY?

A. 177777

B. 5ØØ

C. 1775ØØ

D. 17757Ø

18. REFER TO K1-7 PRINT: WHICH OF THE FOLLOWING BUS ADDRESSES WILL THE SIGNAL BOVFL (ENABLE) STOP?

A. 4ØØ

B. 37Ø

C. 35Ø

D. 33Ø

19. THE MICRO-PROGRAM DOES A JAMJPP TO LOC ØØ2 FOR ANY MICRO-INSTRUCTION THAT SPECIFIES A DATA TRANSFER (DATI OR DATO) YOU ARE GETTING PROPER SSYN RESPONSE TO MSYN. TROUBLE HAS BEEN ISOLATED TO THE K4 MODULE. WHICH CHIP

A. E2Ø

B. E56

C. E38

D. E1Ø

20 WHILE CHECKING OUT THE CONSOLE, YOU NOTE THAT YOU CAN EXAMINE REGISTERS BUT CANNOT EXAMINE ANY LOCATION ON THE BUS. YOU SINGLE CLOCK THRU AN EXAMINE OF LOC 500 AND FIND THAT THE MICRO-PROGRAM SKIPS AROUND EXM 06, EXM 07 AND EXM 08 BACK INTO THE CONSOLE LOOP. THE PROBLEM IS MOST LIKELY CHIP

A. E82

B. E98

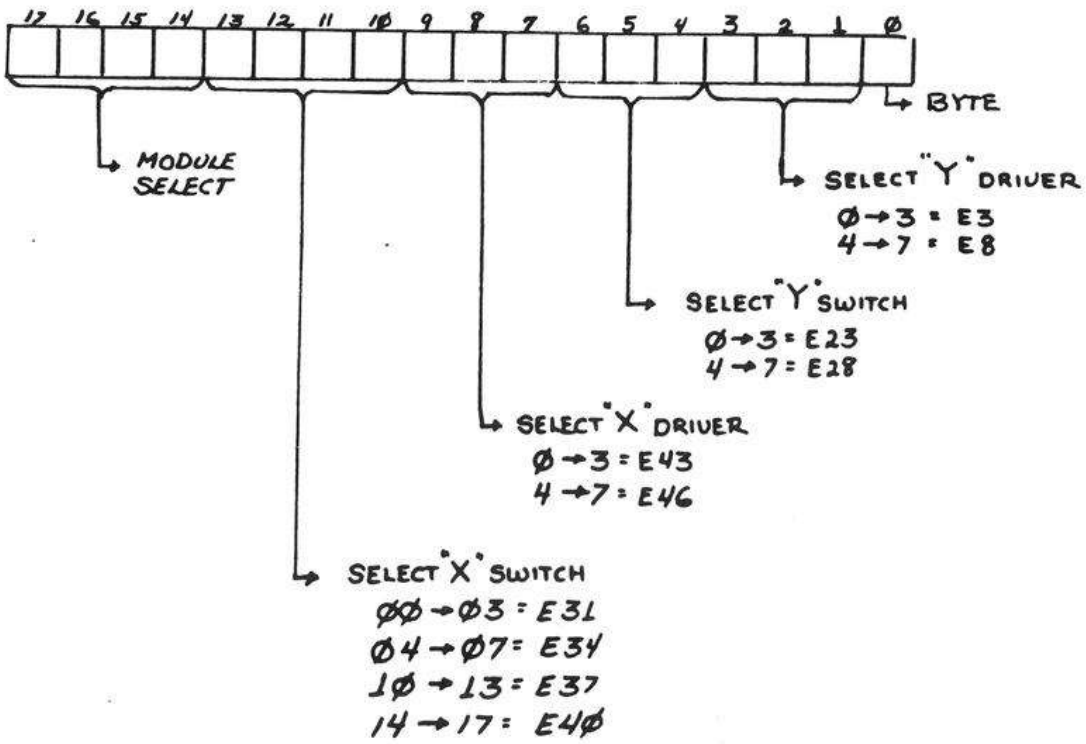
C. E81

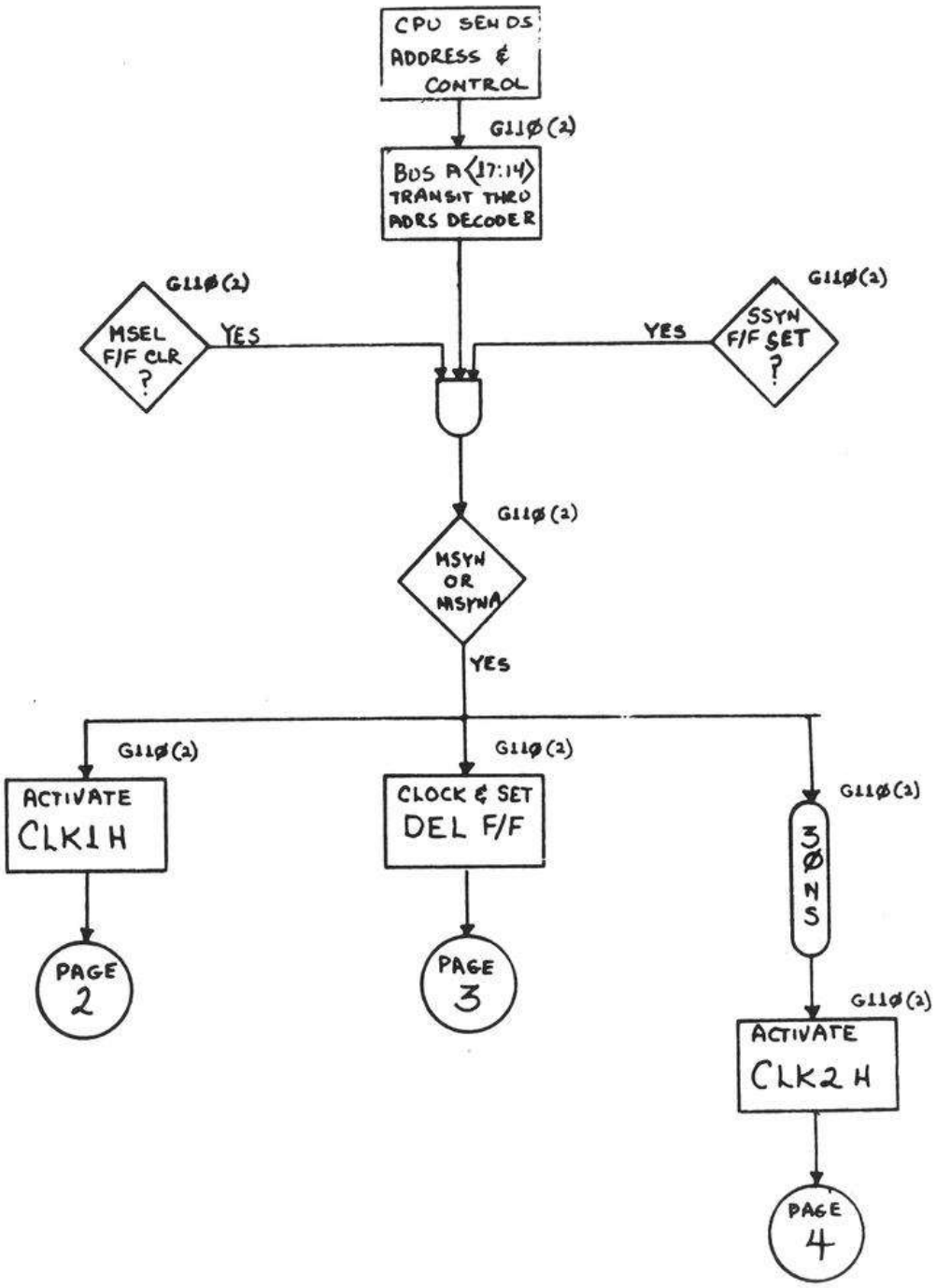
D. E73

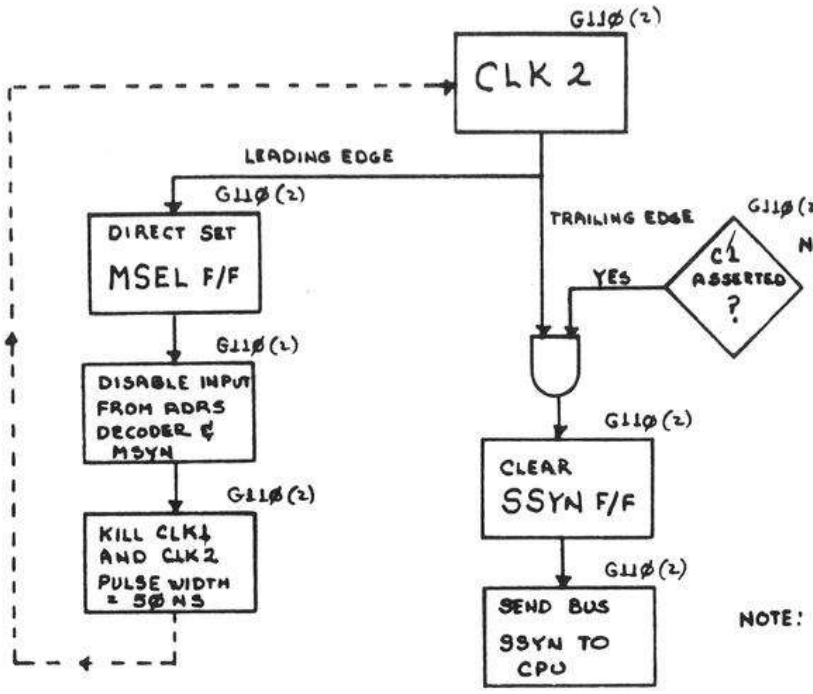
MM-11

MEMORY

MEMORY ADDRESS FORMAT

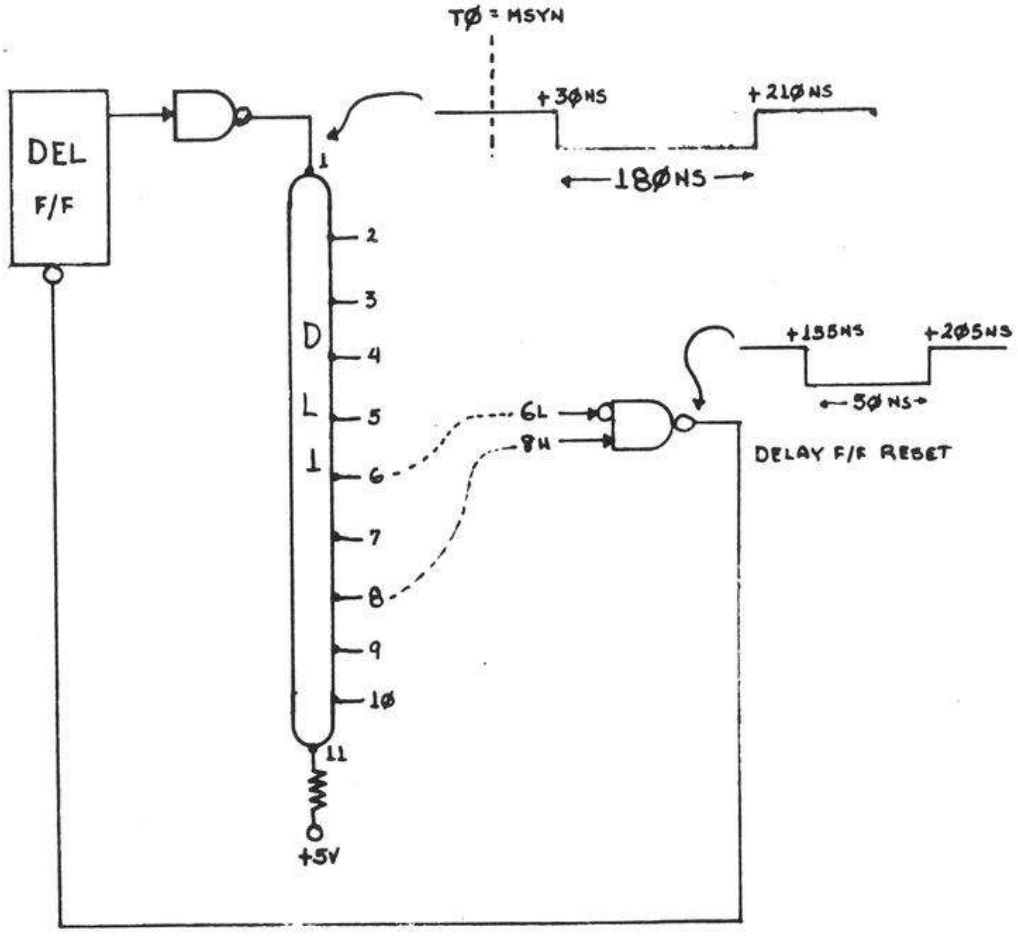



CPU SENDS ADDRESS & CONTROL
G11Ø(2)
BUS A⟨17:14⟩ TRANSIT THRU ADRS DECODER
G11Ø(2)
MSEL F/F CLR ?
YES
G11Ø(2)
SSYN F/F SET ?
YES
G11Ø(2)
MSYN OR MSYNA
YES
G11Ø(2)
ACTIVATE CLK1H
G11Ø(2)
CLOCK & SET DEL F/F
G11Ø(2)
3ØNS
G11Ø(2)
ACTIVATE CLK2H
PAGE 2
PAGE 3
PAGE 4



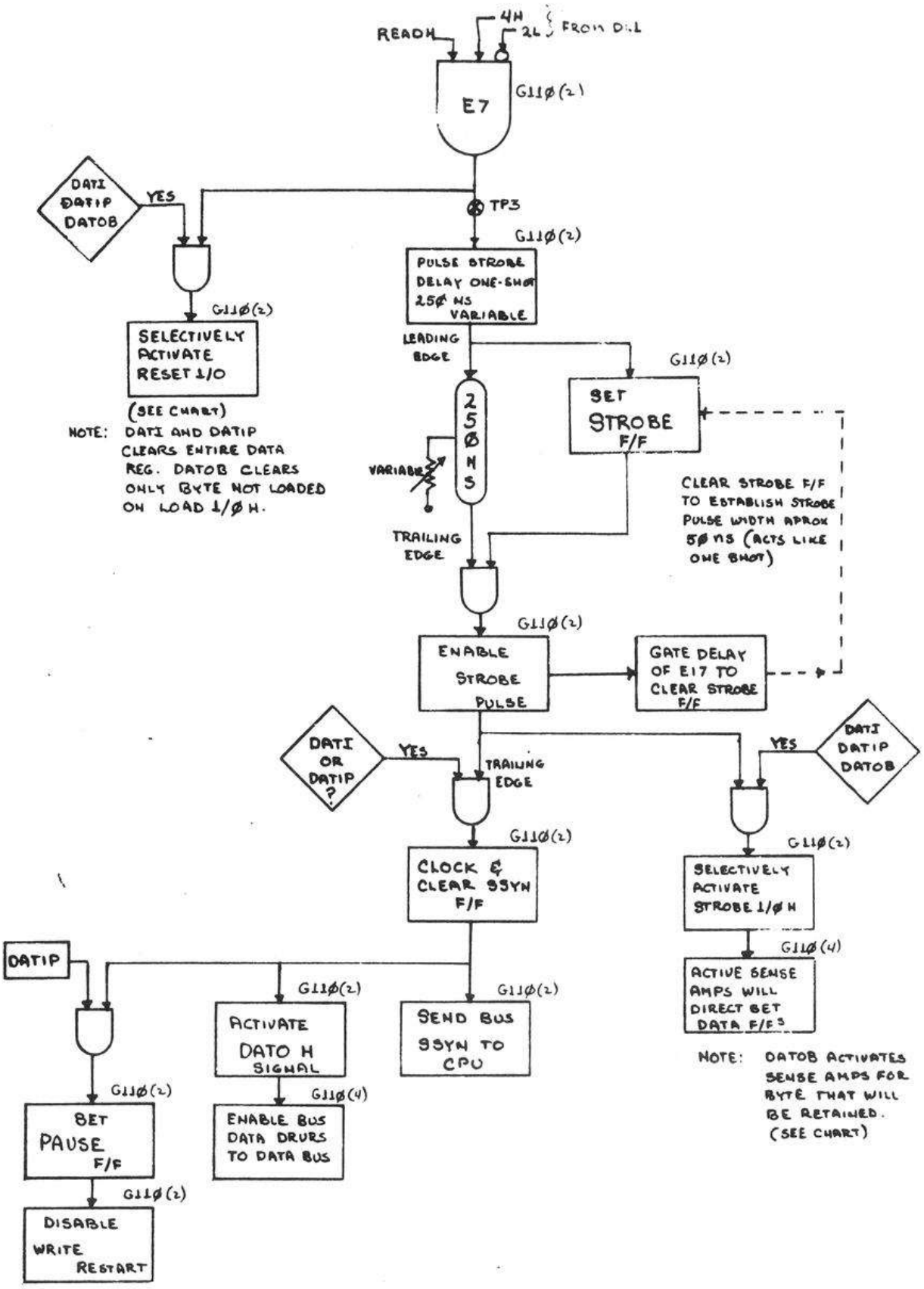
NOTE: IF THIS WERE A DATO OR DATOB, LOAD 1/Ø H ON PAGE 2 WOULD HAVE GATED DATA INTO DATA REG AND BUS SSYN WOULD BE PROPER RESPONSE. NOTE HOW EARLY IN MEM CYCLE SSYN IS SENT ON DATO/DATOB

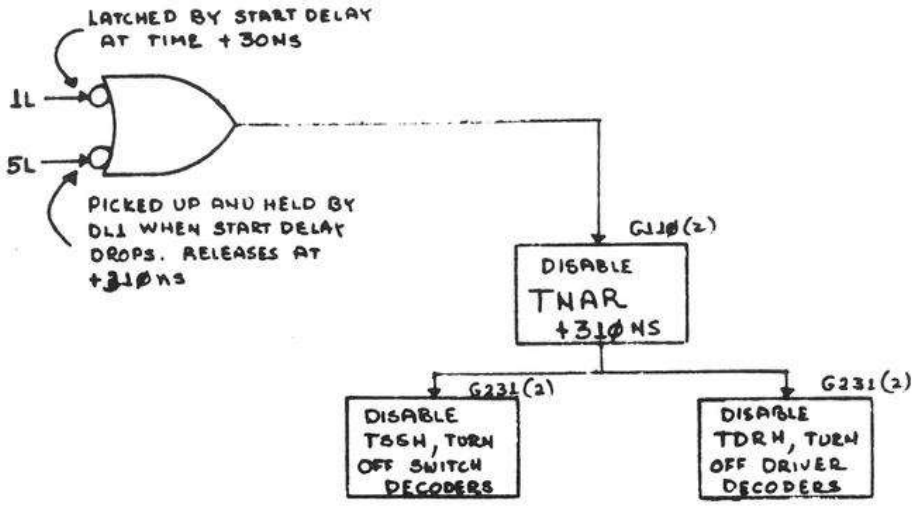
START LO PULSE DOWN DLL COMMENCE TIMING

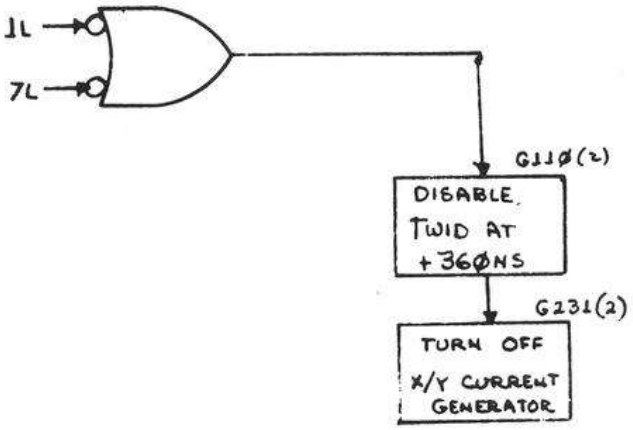


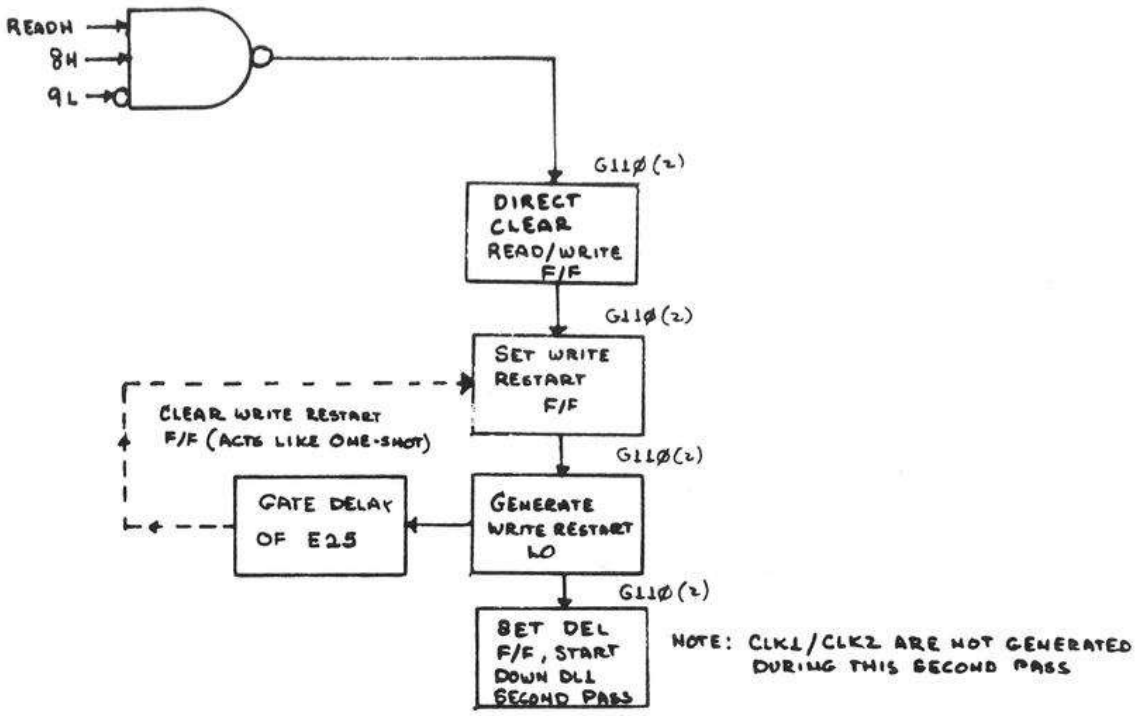
THE PURPOSE OF SHOWING THE ABOVE IS TO ESTABLISH THE RELATIONSHIP BETWEEN THE TIME MSYN (TØ) IS RECIEVED AND THE WAY THE WIDTH OF THE LO PULSE DOWN THE DELAY LINE IS DETERMINED. TO FIND THE APPROXIMATE ELAPSED TIME (REFRENCED TO MSYN) MULTIPLY 25NS X THE TAP NUMBER. THE APPARENT DESCREPENCIES IN TIME ARE CONSUMED IN GATE DELAYS AND RESPONSE TIME.

AS SHOWN, THE WIDTH OF THE LO PULSE COMING DOWN THE DELAY LINE IS ≈ 18ØNS. EACH TAP WILL SEE THIS 18ØNS LO PULSE 25 NS DISPLACED FROM THE PREVIOUS TAP

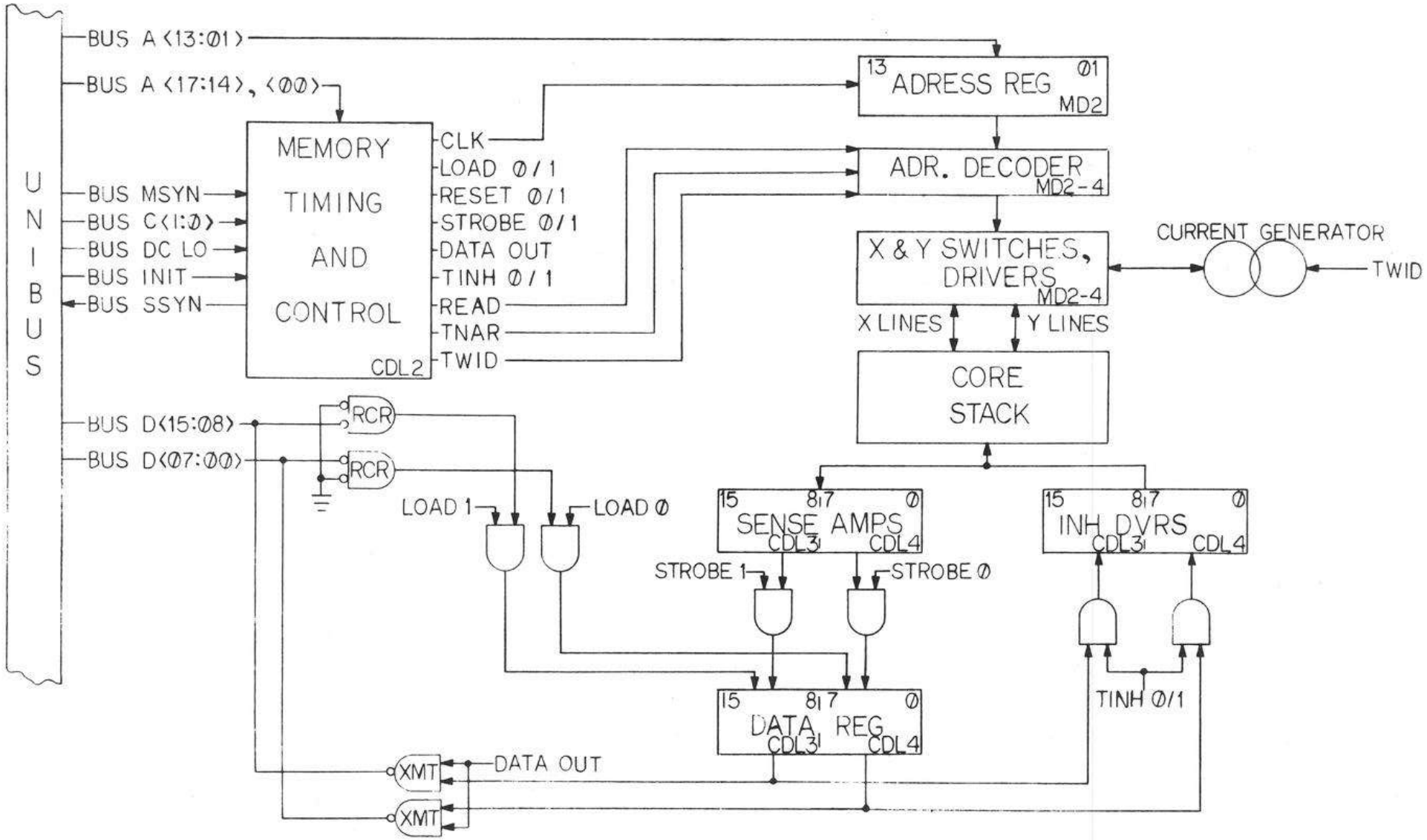

READH
4H
2L
FROM D.L
E7
G11Ø(2)
DATI DATIP DATOB
YES
TP3
G11Ø(2)
PULSE STROBE DELAY ONE-SHOT 25Ø NS VARIABLE
G11Ø(2)
SELECTIVELY ACTIVATE RESET I/O
(SEE CHART)
NOTE: DATI AND DATIP CLEARS ENTIRE DATA REG. DATOB CLEARS ONLY BYTE NOT LOADED ON LOAD I/Ø H.
LEADING EDGE
2 5 Ø N S
VARIABLE
G11Ø(2)
SET STROBE F/F
CLEAR STROBE F/F TO ESTABLISH STROBE PULSE WIDTH APPROX 5Ø NS (ACTS LIKE ONE SHOT)
TRAILING EDGE
G11Ø(2)
ENABLE STROBE PULSE
GATE DELAY OF E17 TO CLEAR STROBE F/F
DATI OR DATIP ?
YES
TRAILING EDGE
YES
DATI DATIP DATOB
G11Ø(2)
CLOCK & CLEAR SSYN F/F
G11Ø(2)
SELECTIVELY ACTIVATE STROBE I/Ø H
G11Ø(4)
ACTIVE SENSE AMPS WILL DIRECT SET DATA F/F'S
NOTE: DATOB ACTIVATES SENSE AMPS FOR BYTE THAT WILL BE RETAINED. (SEE CHART)
DATIP
G11Ø(2)
ACTIVATE DATO H SIGNAL
G11Ø(2)
SEND BUS SSYN TO CPU
G11Ø(2)
SET PAUSE F/F
G11Ø(4)
ENABLE BUS DATA DRVRS TO DATA BUS
G11Ø(2)
DISABLE WRITE RESTART

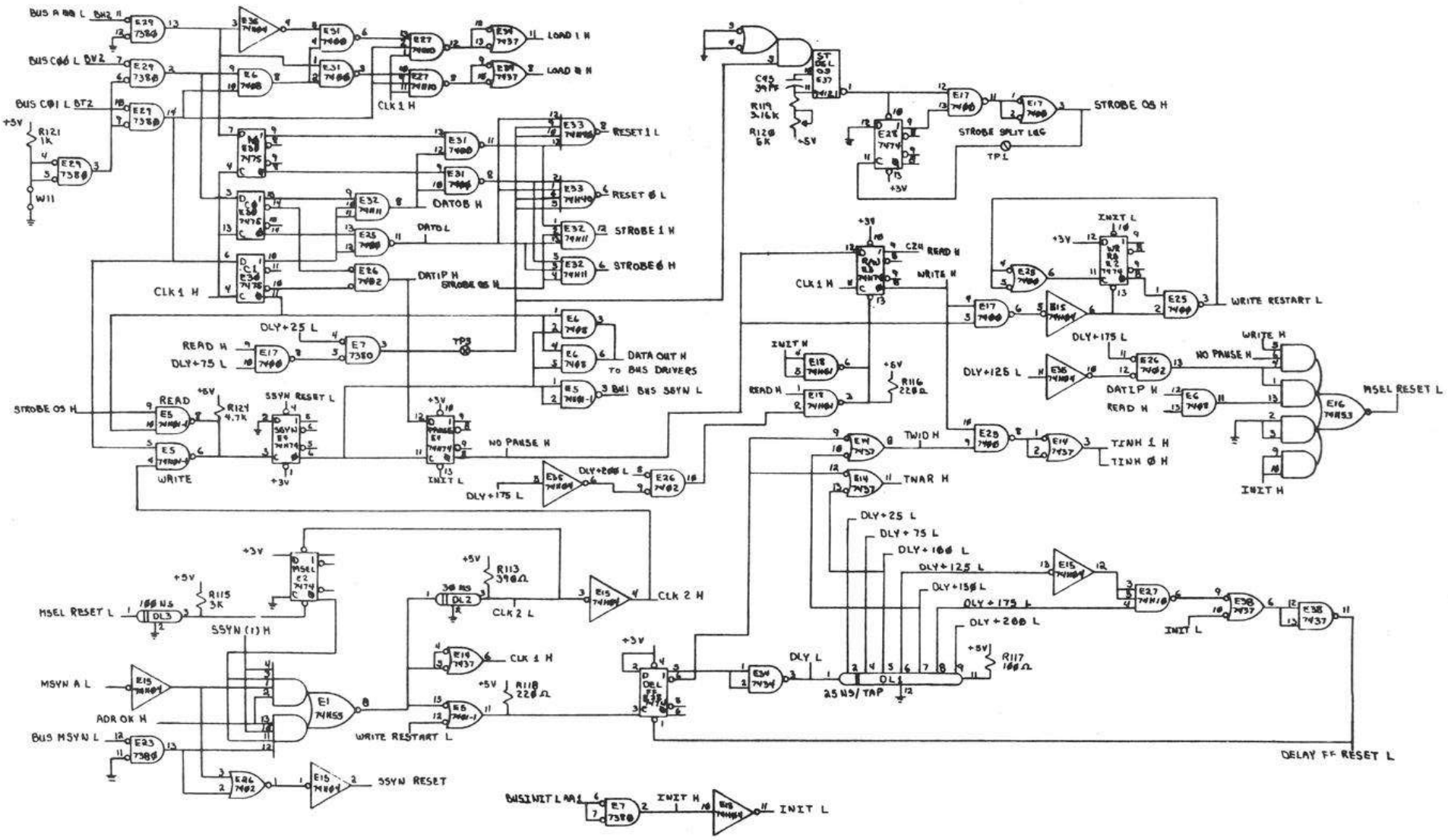

LATCHED BY START DELAY AT TIME +30NS
1L
5L
PICKED UP AND HELD BY DL1 WHEN START DELAY DROPS. RELEASES AT +310NS
G110(2)
DISABLE TNAR +310NS
G231(2)
DISABLE TSGH, TURN OFF SWITCH DECODERS
G231(2)
DISABLE TDRH, TURN OFF DRIVER DECODERS


1L
7L
G110(2)
DISABLE TWID AT +360NS
G231(2)
TURN OFF X/Y CURRENT GENERATOR



A SECOND PASS IS MADE DOWN DLL WITH THE READ/WRITE F/F CLEAR. THIS DOES A WRITE RESTORE AT THE SELECTED LOCATION INHIBIT DRIVERS GO ON WITH TWID AND SENSE AMPS ARE DISABLED DURING THIS PASS.


UNIBUS
BUS A <13:01>
BUS A <17:14>, <00>
BUS MSYN
BUS C<1:0>
BUS DC LO
BUS INIT
BUS SSYN
MEMORY TIMING AND CONTROL
CDL2
CLK
LOAD 0/1
RESET 0/1
STROBE 0/1
DATA OUT
TINH 0/1
READ
TNAR
TWID
13 ADRESS REG 01
MD2
ADR. DECODER
MD2-4
X & Y SWITCHES, DRIVERS
MD2-4
CURRENT GENERATOR
TWID
X LINES
Y LINES
CORE STACK
BUS D<15:08>
BUS D<07:00>
RCR
RCR
LOAD 1
LOAD 0
15 8 7 0
SENSE AMPS
CDL3
CDL4
STROBE 1
STROBE 0
15 8 7 0
INH DVRS
CDL3
CDL4
TINH 0/1
15 8 7 0
DATA REG
CDL3
CDL4
XMT
XMT
DATA OUT


BUS A RR L BA2
BUS C00 L BT2
BUS C01 L BT2
+5V
R121 1K
W11
LOAD 1 H
LOAD 0 H
CLK 1 H
RESET 1 L
RESET 0 L
DATOB H
DATO L
STROBE 1 H
STROBE 0 H
DATIP H
STROBE 05 H
DLY+25 L
READ H
DLY+75 L
TP3
DATA OUT H
TO BUS DRIVERS
BUS SSYN L
STROBE 05 H
READ
WRITE
R124 4.7K
SSYN RESET L
NO PAUSE H
INIT L
DLY+175 L
DLY+200 L
C95 39PF
R119 5.16K
R120 6K
STROBE 05 H
STROBE SPLIT LEG
TP1
C24 READ H
WRITE H
INIT L
WRITE RESTART L
DLY+175 L
DLY+125 L
DATIP H
READ H
WRITE H
NO PAUSE H
MSEL RESET L
INIT H
INIT H
R116 220Ω
TWID H
TINH 1 H
TINH 0 H
TNAR H
DLY+25 L
DLY+75 L
DLY+100 L
DLY+125 L
DLY+150 L
DLY+175 L
DLY+200 L
R117 100Ω
INIT L
DLY L
25 NS/TAP
DELAY FF RESET L
MSEL RESET L
100 NS
R115 3K
SSYN (1) H
R113 390Ω
30 NS
CLK 2 L
CLK 2 H
CLK 1 H
R118 220Ω
WRITE RESTART L
MSYN A L
ADR OK H
BUS MSYN L
SSYN RESET
BUS INIT L BA1
INIT H
INIT L

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