F-87S

PDP-8/S

MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

1st Edition October 1967
2nd Edition March 1968
3rd Edition June 1968
4th Edition August 1969
5th Edition October 1970

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PREFACE

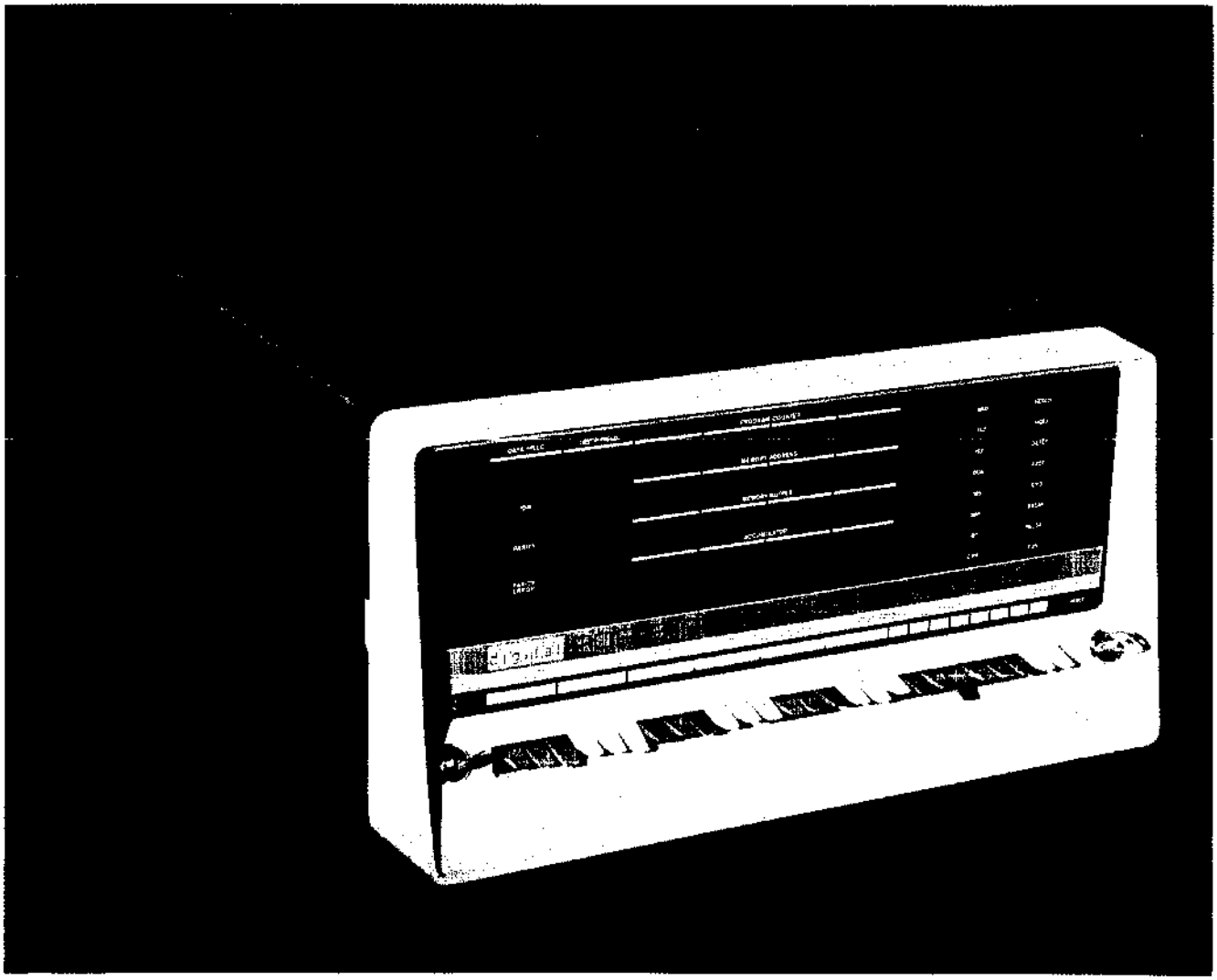
This instruction manual is intended to aid personnel in the operation and maintenance of the PDP-8/S computer. The manual also discusses the operation of the Teletype ASR-33 and describes its control unit, which is of DEC manufacture, but a separate manual is furnished for the device itself.

Chapters 1 through 4 and Appendix A apply to the basic PDP-8/S and Teletype ASR-33. Chapter 1 lists the operating specifications of the system and describes its physical and electrical characteristics. Chapter 2 describes the logical organization of the computer, discusses the number system and instruction formats used by it, explains the use of all controls and indicators on the operator panel, and explains the operation of the ASR-33. Chapter 3 presents a complete detailed description of the system logic, including a discussion of the symbols and notation used in the logic drawings and flow charts. Chapter 4 contains information useful in maintaining the system, including a discussion of maintenance programs, memory alignment and troubleshooting procedures, and in-out bus specifications.

Chapter 5 contains equivalent information on the Data Break (DB8S) and Memory Expansion (MC8S, ME8S, MM8S) options and the additional logic common to both (OMD8S).

Appendix A contains engineering drawings, logic drawings, flow charts, and circuit schematics for the basic PDP-8S and ASR-33 control.

Appendix B contains engineering drawings, logic drawings, flow charts, circuit schematics, and a glossary for the Data Break and Memory Expansion Options.



CHAPTER 1
INTRODUCTION

The PDP-8/S is a small-scale, general-purpose digital computer designed for use as an independent information-handling facility in a larger computer system, or as the control element in a complex processing system. The basic computer consists of a central processor and a memory, and has a Teletype Model 33 Automatic Send/Receive set for input-output. The processor performs all arithmetic, logical and system control functions. Memory operation is based on a read-write cycle, one cycle being executed each time access is requested by the processor.

Interface circuits for the in-out bus allows connection to a variety of peripheral equipment. Every device must detect its own selection code and provide any necessary input gating. In the standard computer all transfers over the in-out bus are under program control, but peripheral equipment can interrupt the program. Optional equipment allows direct data access to the memory for high speed devices such as disc memory.

In the processor all operations on words are serial; the computer uses parallel transfers only for communication between the processor and the memory, the console, or the in-out equipment over the in-out bus. Information handled by processor and memory has the following characteristics.

Word Length	
Processor:	12 bits
Memory:	13 bits including parity bit
Instruction Format	
Memory Reference:	Instruction code, 3 bits Indirect, 1 bit Memory address, 8 bits
Operate Group:	Instruction code, 12 bits
Input-Output:	Instruction code, 12 bits including 6 bit device code
Internal Number System	Binary
Negative Representation	Two's complement
Number Format	Sign, 1 bit; magnitude, 11 bits

All timing is synchronous, but processor and memory operate on separate clocks, which cannot run simultaneously. Thus every time that the processor requests memory access its clock stops; when the memory cycle is complete, the processor restarts. Each processor cycle of 10.5 μs is one word time, the time required to process one word serially. The PDP-8/S uses two types of random access magnetic

core memory having cycle times of 6.3 and 6.5 μs. Instruction execution times differ depending upon the number of processor and memory cycle required, and upon whether a given instruction uses indirect addressing and autoindexing.

The processor must set up all transfers of data to and from the peripheral equipment; but since a device can signal the processor by means of a program interrupt when it requires services, no processor time need be lost in waiting, and processor and peripheral equipment can operate in parallel. The only I/O device supplied with the standard computer is the Teletype Model 33 ASR but it includes keyboard, printer, tape reader and punch. It handles data at the rate of ten 8-bit characters per second.

1.1 PHYSICAL CHARACTERISTICS

The table model is housed in a cabinet but the computer is also available for mounting in a standard 19-in. rack. The computer contains six logic mounting panels, lettered A to F from right to left when viewing it from the front. Each mounting panel can hold forty DEC Flip-Chip plug-in modules numbered from front to back.

The rack-mountable model requires 10-1/2 in. of vertical space in a 19-in. rack. It protrudes 3-3/4 in. at the front of the rack, and slides out 25 in. Physical dimensions of both models are shown in Figures 1-1 through 1-5. The table model weighs 84 lb, and the rack model weighs 200 lb including power equipment. The Teletype ASR 33 has the following dimensions.

Height: 45 in.
Width: 22 in.
Depth: 19 in.
Weight: 100 lb

Intake fans at the back of the table model cool the logic modules by blowing air between them. A PDP-8/S shipped mounted in a DEC rack has three muffin fans on the left side, but the user must supply adequate ventilation for a computer shipped unmounted.

It is recommended that the ambient temperature at the installation be maintained between 70° and 85°F, but it can vary between 32° and 130°F without adverse effect. Although all exposed surfaces are treated to prevent corrosion, exposure to extreme humidity for long periods of time should be avoided.

1.2 ELECTRICAL CHARACTERISTICS

The computer uses standard line power at 115 ± 17 Vac, 60 cycle (±2%), single phase. The rack model uses a standard 728 power supply and a control through which the power switch on the front panel switches ac to a pair of receptacles on the computer backplate. These receptacles are for the power supply and the fans. To switch ac to other supplies or devices from the computer front panel

requires the use of a repeater relay slaved to this switched ac. The power cable uses a Hubbell Twist-Lok connector; both cable and connector are rated at 20 or 30 amp depending upon total system requirements.

The table model has an equivalent power supply mounted on the inside rear of the cabinet, and both it and the fans receive ac through the front panel power switch and a pair of circuit breakers. The power cable uses a standard ac plug with ground and is rated at 15 amp. The teletype must be powered separately.

Current consumption is as follows.

	Processor	Teletype
Line current	3 amp	2.6 amp Turn on surge, 7 amp
Dissipation	100W	140W
Logic voltages		
+10V	0.6 amp	1.2 amp
-15V	5.5 amp	0.5 amp

The dc voltages required by the logic are +10V and -15V. All logic is solid state; transistors and diodes operate on static logic levels of 0 and -3 Vdc (tolerances are 0V to -0.3V and -3.2V to -3.9V). Most logic modules include an internal supply to derive the negative logic level from the -15V input. PDP-8/S logic uses pulse timing almost exclusively. Pulse amplitude from a pulse generating source is +3V from -3V with the same tolerances as levels. Pulses at inverter outputs may be from ground to -3V or vice versa. Pulse widths may be 100 ns or 400 ns depending upon application. Occasionally, an input may be triggered by a positive level transion of 60 ns or less instead of a pulse. Driving voltages for the core memory are nominally -10V to ground and -15V to ground. The statistics given here apply to all modules used in the equipment described in this manual except the transmitter and receiver modules for the teletype; the special voltage requirements for these modules are discussed with the teletype logic.

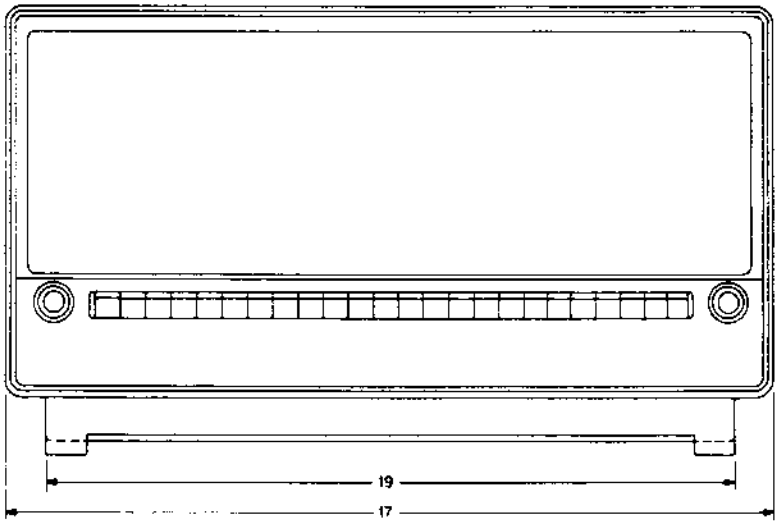


Figure 1-1 Dimensions, Table Model (Front View)

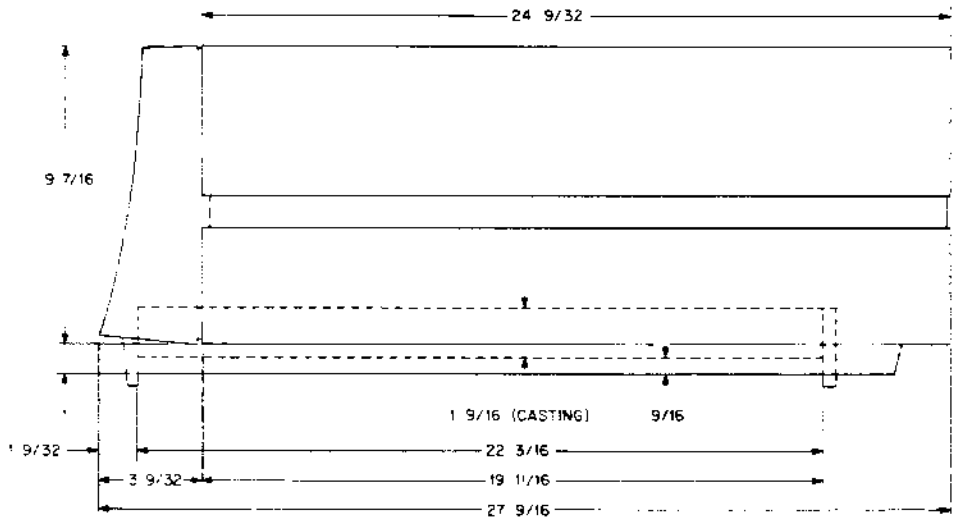


Figure 1-2 Dimensions, Table Model (Side View)

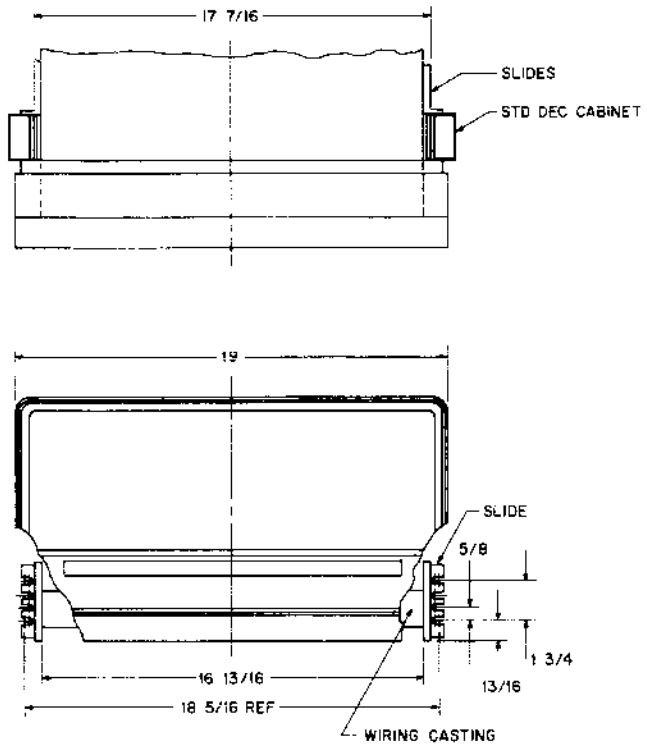


Figure 1-3 Dimensions, PDP-8/S Mounted in Standard DEC Rack

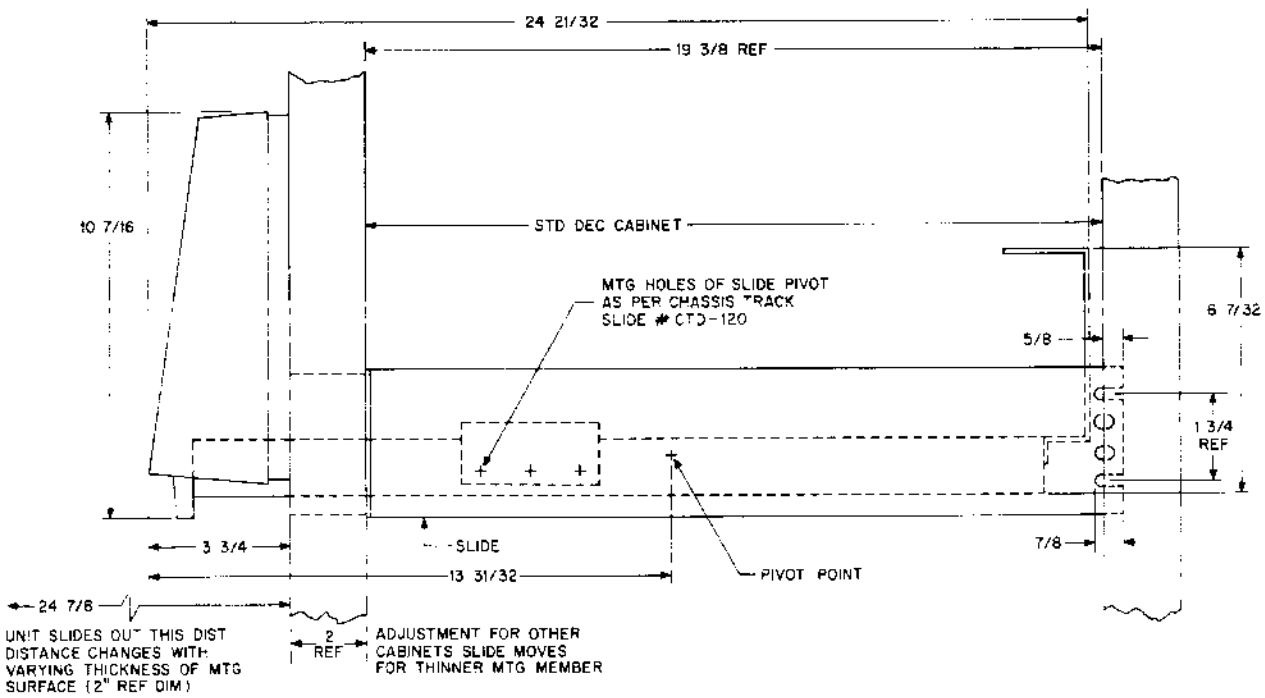


Figure 1-4 Dimensions, PDP-8/S Mounted in Standard DEC Rack

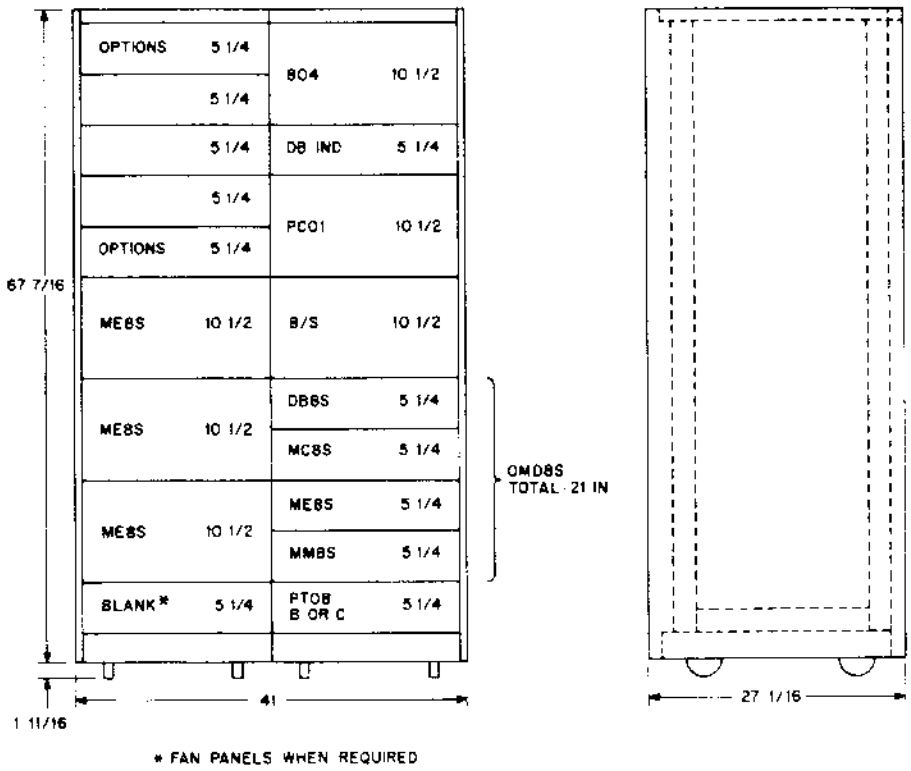


Figure 1-5 Typical Rack Mounted PDP-8/S
with Recommended Option Mounting

CHAPTER 2
SYSTEM OPERATION

Figure 2-1 shows the registers and data flow in the PDP-8/S. The processor is the control unit for the entire system: it governs all peripheral in-out equipment, sequences the program, and performs all arithmetic and logical operations.

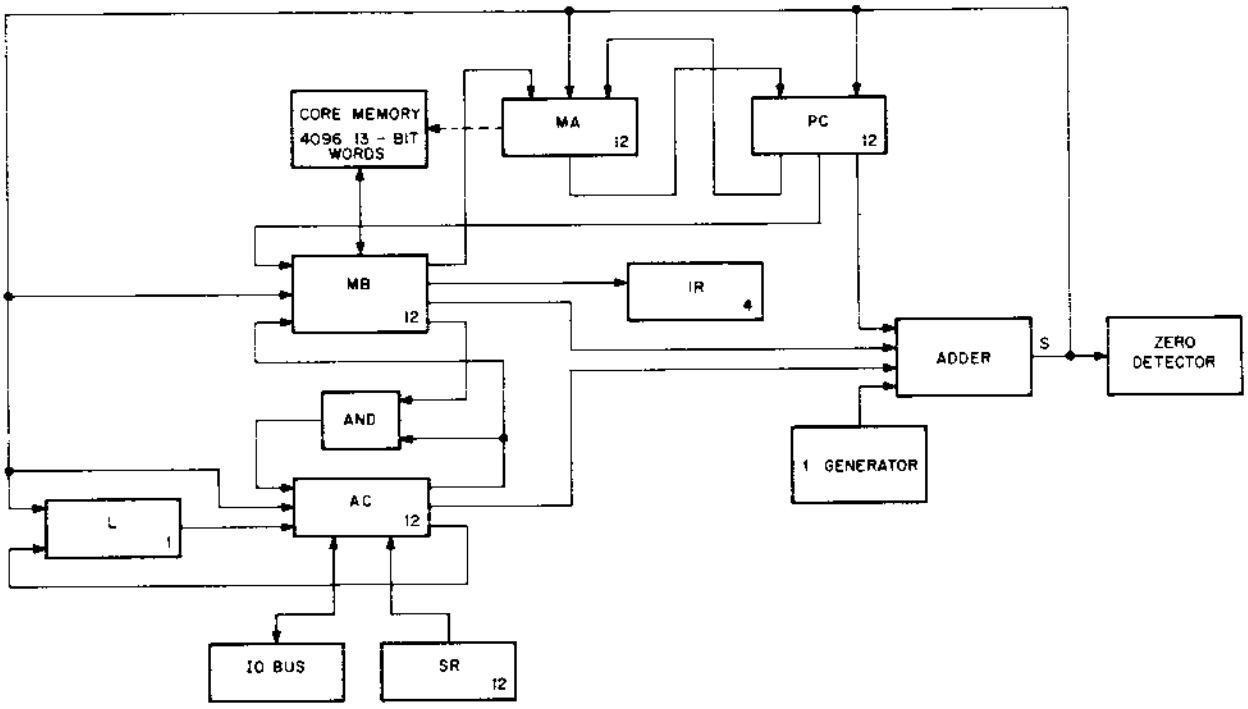


Figure 2-1 PDP-8/S Data Flow

The processor handles words of 12 bits, which are stored in a memory with a capacity of 4096 words. Storage in memory is actually in the form of 13-bit words, the extra bit being an even parity bit for the word. The bits of a word are numbered 0 through 11, left to right, as are the flip-flops in the registers that handle the words. Words are used either as computer instruction in the program, as addresses, or as operands, that is, data for the program.

The processor performs a program by executing instructions retrieved from consecutive memory locations, as counted by the program counter (PC), although the program may alter its own sequence by changing the address in PC, either by indexing (incrementing it by one) an extra time in a test skip instruction or by replacing its contents with the value specified by a jump instruction. To gain access to memory for retrieval or storage, the processor requests a memory cycle and supplies an address from the memory address register (MA). All transfers of data between processor and memory are made through the memory buffer (MB). When a word is retrieved at MB, as an instruction, its left four bits pass to the instruction register (IR), which is decoded to govern the actual execution of the instruction. In a memory reference instruction, the rest of the word in MB supplies address information to MA; otherwise the rest of the word is decoded directly from MB to assist in instruction execution.

The heart of the processor is the memory buffer MB, the accumulator (AC), and a 1-bit serial adder. All transfers between processor and peripheral equipment are made via AC, which is connected to the in-out bus. The accumulator is also connected to the switch register (SR) through which the operator can send data and addresses into the computer from the console. The only parallel transfers that occur in the system are those between MB and memory, between AC and the I/O bus, and from SR to AC. All other operations in the processor are serial: all registers are shift registers, and information is transferred from one register to another by shifting both registers to the right, so that information leaves one register at the right (LSB) and enters the other from the left (MSB). Although not shown in Figure 2-1, the processor can recirculate any of the four main registers whenever its contents must be saved while being transferred.

To produce the logical AND function, the contents of MB and AC are shifted through a simple AND gate, with the result appearing in AC. All other operations on words are performed through the serial adder. The contents of MB and AC are added one bit at a time as the sum is shifted into AC. The adder is also used to increment AC, MB, or PC, to complement AC, and even to detect zero contents in MB or AC for a skip test.

Associated with AC is a 1-bit register, the link (L). The link serves as an overflow flag in addition and when AC is incremented. AC and L can be rotated together, to the left or right, as a single 13-bit register (left rotation is produced by a shortened right shift). The program can also use L to generate products and quotients one bit at a time.

Besides the registers that enter into the regular execution of the program and its instructions, the processor also contains a program interrupt system that allows peripheral devices, a memory parity error or a power failure to interrupt normal program flow. When such an interruption occurs and the interrupt is on (ION), the processor stores the current contents of PC (the address of the next instruction in the program) in location 0000, and executes the instruction in location 0001.

Timing for all operations in processor and memory is supplied by two clocks. Each serial processing of a word is performed in one word time under control of the processor clock. When memory access is required, the processor stops its own clock and triggers a memory cycle, which is executed under control of the memory clock. At the completion of the memory cycle the memory clock stops, and the processor clock restarts to execute another word time.

2.1 PROGRAMMING

The program is a set of instructions used to perform some task and is stored in memory. Each word in memory is identified by an address, 0000-7777 octal. To execute a program, the computer normally retrieves instructions from sequentially increasing locations, but the instructions, themselves, can alter program flow and cause the computer to continue sequential operation from some other location. Table 2-1 is an instruction index.

Table 2-1.
Instruction Index

Mnemonic	Meaning	Octal Code
AND	Logical AND	0xxx
TAD	Twos Add	1xxx
ISZ	Increment and Skip if Zero	2xxx
DCA	Deposit and Clear Accumulator	3xxx
JMS	Jump to Subroutine	4xxx
JMP	Jump	5xxx
IOT	In-out Transfer	6xxx
OPR	Operate	7xxx
	Operate Group	
NOP	No Operation	7000
IAC	Increment Accumulator	7001
RAL	Rotate Accumulator Left	7004
RTL	Rotate Two Left	7006
RAR	Rotate Accumulator Right	7010
RTR	Rotate Two Right	7012
CML	Complement Link	7020
CMA	Complement Accumulator	7040
CIA	Complement and Increment Accumulator	7041
CLL	Clear Link	7100
STL	Set Link	7120
CLA	Clear Accumulator	7200
STA	Set Accumulator	7240
HLT	Halt	7402
OSR	OR Switch Register	7404
SKP	Skip	7410
SML	Skip on Nonzero Link	7420
SZL	Skip on Zero Link	7430
SZA	Skip on Zero Accumulator	7440
SNA	Skip on Nonzero Accumulator	7450
SMA	Skip on Minus Accumulator	7500
SPA	Skip on Positive Accumulator	7510

Table 2-1. (continued)
Instruction Index

Mnemonic	Meaning	Octal Code
CLA	Clear Accumulator	7600
LAS	Load AC Switches	7604
	IOT Group	
ION	Interrupt On	6001
IOF	Interrupt Off	6002
SMP	Skip on No Memory Parity Error	6101
CMP	Clear Memory Parity Error Flag	6104
KSF	Keyboard, Skip on Flag	6031
KCC	Keyboard, Clear Flag	6032
KRS	Keyboard, Read Buffer Static	6034
KRB	Keyboard, Read Buffer	6036
TSF	Teleprinter, Skip on Flag	6041
TCF	Teleprinter, Clear Flag	6042
TPC	Teleprinter, Print Character	6044
TLS	Teleprinter, Load Sequence	6046

2.1.1 Number System

The PDP-8/S uses two's complement, fixed-point conventions to do binary arithmetic. In a word used as a number, bit 0 (the left-most bit) represents the sign denoted by 0 for positive, 1 for negative. In a positive number, the remaining eleven bits are the magnitude in ordinary binary notation. The negative of a number is obtained by taking the two's complement. If x is an n-digit binary number, its two's complement is $2^n - x$, and its one's complement is $(2^n - 1) - x$, or equivalently $(2^n - x) - 1$. Subtracting a number from $2^n - 1$ (from all 1s) is equivalent to performing the logical complement, changing all zeros to ones and all ones to zeros. Therefore, to form the two's complement, take the logical complement (usually referred to merely as the complement) of the entire word including the sign, and add 1 to the result. In a negative number, the sign bit is 1 and the remaining bits are the two's complement of the magnitude.

$+153_{10} = +231_8 =$ 000 010 011 001
0 11

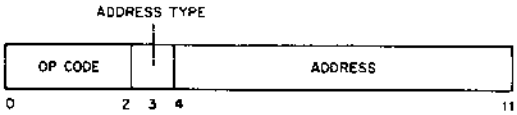
$-153_{10} = -231_8 =$ 111 101 100 111
0 11

Zero is represented by a word containing all 0s; complementing this number produces all 1s, and adding 1 to that produces all 0s again. There is only one zero representation and its sign is positive. Since the numbers are symmetrical in magnitude about a single zero representation, all even numbers both positive and negative end in 0, all odd numbers in 1 (a number all 1s represents -1). Since there are the same number of positive and negative numbers, however, there is one more negative number than there are nonzero positive numbers. This is the most negative number and it cannot be produced by negating any positive number. (The magnitude of the most negative number is one greater than the largest positive number.)

If one's complements were used for negatives, a negative number could be read by attaching significance to the 0s instead of the 1s. In two's complement notation, each number is one greater than the complement of the positive number of the same magnitude, so one can read a negative number by attaching significance to the rightmost 1 and attaching significance to the 0s at the left of it. (The negative number of largest magnitude has a 1 in only the sign position.) In a negative integer, 1s may be discarded at the left, just as leading 0s may be dropped in a positive integer. In a negative fraction, 0s may be discarded at the right as long as only 0s are discarded, the number remains in two's complement form because it still has a 1 that possesses significance. If a portion including the rightmost 1 is discarded, the remaining part of the fraction is now a one's complement. The computer does not keep track of a binary point, so the programmer must adopt a point convention and shift the magnitude of the result to conform to the convention used.

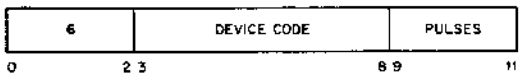
2.1.2 Instruction Format

A computer instruction performs some basic function, such as storing a word in memory or performing an arithmetic or logical operation. If an instruction requires a memory address, the three high-order bits (0 through 2) specify the operation, bit 3 specifies the type of addressing, and the remaining eight bits (4 through 11) specify the effective address or the location to be used in determining the effective address. The effective address is the actual address used to fetch the operand or alter program flow.



The operate and in-out instructions do not require memory addresses. In an operate instruction bits 0 through 2 contain 7, and the remaining bits specify individual operations, so an instruction can be microprogrammed to perform a combination of the various operations. In an in-out instruction,

bits 0 through 2 contain 6, bits 3 through 8 specify the in-out device, and bits 9 through 11 select the timing pulses sent out over the I/O bus. Pulses at the three event times, in order, are selected respectively by 1s in bits 11, 10, and 9.



2.1.3 Addressing

Locations in memory are addressed by the 12-bit octal numbers 0000 to 7777 (0 to 4095 decimal). The instruction format allows only eight bits for an address, so for programming purposes the memory is divided into thirty-two pages, each containing 128 (200_8) locations. The eight address bits in the instruction can select one location out of 256, or a single location from two pages. If bit 4 is 0, bits 5 through 11 are taken as an address in page 0, i.e., the address part of the instruction is taken to represent an address between 0000 and 0177. If bit 4 is 1, bits 5 through 11 are taken as an address in the same page from which the instruction was retrieved. The 12-bit address that is used is the combination of bits 5 through 11 of the instruction word and bits 0 through 4 of the address previously supplied by PC to MA for instruction retrieval.

Bit 3 of the instruction word specifies the type of address contained in bits 4 through 11. If bit 3 is 0, addressing is direct; the effective address is the 12-bit address determined by bits 4 through 11. If bit 3 is 1, addressing is indirect, and the address part of the instruction is taken to specify a location whose contents are to be used as the (12-bit) effective address.

2.1.4 Autoindexing

The program can make use of an automatic indexing feature by indirectly addressing any memory location from 0010 to 0017. Whenever one of these locations is specified by an indirect address, the processor retrieves the contents of the addressed location, indexes the word contained therein, writes the altered word back into memory, and uses the indexed word as the effective address.

2.1.5 Operating Speed

The table 2-2 gives the approximate execution times in microseconds of the various PDP-8/S instructions. Where they are applicable, the longer times that are required for indirect addressing and autoindexing are also given. With each time, the pair of numbers separated by a comma indicates the number of processor and memory cycles required for the instruction.

Table 2-2.
PDP-8/S Instruction Execution Times

			Indirect Addressing		Autoindexing	
AND	32.2	2,2	48.3	3,3	64.4	4,4
TAD	32.2	2,2	48.3	3,3	64.4	4,4
ISZ	48.3	3,3	64.4	4,4	80.5	5,5
DCA	42.7	3,2	58.8	4,3	74.9	5,4
JMS	42.7	3,2	58.8	4,3	74.9	5,4
JMP	26.6	2,1	42.7	3,2	58.8	4,3
IOT	37.1	3,1				
OPR 1	26.6	2,1				
OPR 2	37.1	3,1				

A processor cycle (one word time) requires 10.5 μs if there is no memory request, about 9.8 μs otherwise. The above times are based on a memory cycle of 6.3 μs. The nominal times for the two memory types are 6.3 μs and 6.5 μs, but either type can differ by as much as 100 ns from its nominal value. Moreover, if the optional data channel equipment or expanded memory is added to the computer, the memory cycle time is fixed at 8 μs regardless of stack type. The programmer is advised not to use internal computer timing in place of a real-time clock.

A program interrupt takes 32.2 μs (2,2) in addition to instruction execution time. The first IOT pulse occurs 10.5 μs after the IOT instruction is fetched, and the other two pulses occur at 1-μs intervals thereafter.

2.2 Word Times

Each word time is made up of 14-bit times (numbered 00 through 13) during which the clock generates a string of fourteen bit pulses 750 ns apart. The first 12 pulses perform whatever serial operations are required on one or more 12-bit words. The thirteenth pulse performs most of the individual operations that are required for any instruction (such as an OPR), checks parity, and requests a memory cycle if one is required. When a memory cycle is requested, the processor clock stops, and the memory goes through its cycle controlled by its own clock. Upon completion of the cycle, the processor clock restarts at the fourteenth pulse, which determines the transition to the next word-time. When the computer is stopped by the program or the operator, it does so between the thirteenth and fourteenth bit times, i.e., at time 13 but following completion of the memory cycle if one is requested.

The word-time in which a word is processed depends upon what type of information it represents (an instruction, an address, an operand) and what functions must be performed on it. There are six word-times: fetch, index, defer, execute, end, break. Although the execution of an instruction

begins in fetch time, the program must start in end time, which determines the location of the first instruction and requests a memory cycle to retrieve it. In other words, fetch time does not fetch the instruction. Fetch time processes the instruction just retrieved from memory. It transfers the instruction code to IR for decoding, transfers the address part to MA, and indexes PC so that it will point to the next location.

At the end of fetch time, the processor requests memory access if the instruction is indirectly addressed or requires the retrieval of an operand. If an autoindexing location is indirectly addressed, the processor then enters index time; for any other indirect addressing it enters defer time; in any other situation it goes directly to execute time. In index time the address that has been retrieved is incremented by one and written back in memory. The processor then enters defer time to move the new address to MA and request a memory cycle, if an operand must be retrieved. The actual logical, arithmetic or program control operation specified by the instruction is then performed in execute time, which requests access if an operand must be deposited in memory. In end time the processor determines the location of the next instruction and fetches it. In some cases the execute and end times are simultaneous; if they are not, the processor automatically goes from execute to end time.

After retrieving an instruction, the processor returns to fetch time unless a program interrupt has been requested. In this case the processor enters break time in which it deposits the current contents of PC in location 0000, and then returns to end time to retrieve the instruction in location 0001. There are also three special word times for operations associated with the console: these are used for loading a starting address into PC, depositing a word in memory, or examining the contents of a memory location.

To control the special operations required for in-out, including parallel transfer over the bus, the first bit pulse in execute time of an IOT triggers a string of three special pulses 1 μs apart. Of these, the only pulses actually sent over the bus for use in IOT operations are those specified by the programmer in bits 9 through 11 of the IOT instruction.

2.3 PROCESSOR OPERATION

In the table model of the PDP-8/S, the circuit breakers are mounted on the rear panel with the power supply; the rack mounted model has a power control that includes circuit breakers and usually a power light. All other controls and indicators for the processor and memory are located on the computer front panel. The indicators are on the vertical upper part of the panel; below this is a row of two-position keys and switches with a key-operated rotary switch at each end (switches are alternate action, keys are momentary contact).

The six switches at the left end of the row and the corresponding lights at the top of the panel are for the optional memory expansion. The next 12 switches make up a switch register through which the operator can supply data and addresses to the processor (the up position of a switch represents a 1).

The register can be used in conjunction with some of the operating keys, and its contents can be read into AC by the program. The next six levers are the operating keys. They are off when in the up position, except for DEP (third one from the left) which is off when in the down position. The last two levers are the operating mode switches, which are off when in the down position. Power is applied to the computer by turning clockwise the key-operated POWER switch at the right-hand end of the panel. The similar PANEL LOCK switch at the left-hand end disables the operating keys and switches when turned clockwise (the last eight levers at the right-hand end become inoperative and the switch register is not affected).

When any indicator is lit, the associated flip-flop is in the 1 state or the associated function is true. A few indicators display useful information while the processor is running, but most change too frequently and are therefore discussed in terms of the information they display when the processor has stopped.

2.3.1 Indicators, Operating Keys, and Switches

In the center of the panel there are four rows of indicators that display (from top to bottom) the contents of PC, MA, MB and AC. The extra light at the left-hand end of the bottom row displays the contents of the link. When the computer stops, PC usually holds the address of the next instruction, MA indicates the address of the last memory access, and MB holds the word read from or written into memory.

Indicator	Function
FETCH, INDEX, DEFER, EXEC, END, BREAK	EXEC and END can be on together, but otherwise only one of these lights can be on at a time. The on light indicates the word time the processor has stopped in.
PAUSE	A memory cycle is in progress. This light can stay on long enough to be noticed only if optional data break equipment is occupying the memory most or all of the time, and thus the processor is running little if at all.
RUN	The processor is in normal operation with one instruction following another. When the light goes off, the computer stops.
AND, TAD, ISZ, DCA, JMS, JMP, IOT, OPR	Only one of these can be on at a time. It indicates the instruction being executed or just executed. If the processor stops with BREAK on, or the operator has just loaded an address from the console, the AND light will be on regardless of what instruction was last executed.
ION	The program interrupt system is on, so a parity error or an interrupt request over the in-out bus will cause a program break.
PARITY	Displays the parity bit of the last word read from or written into memory.
PARITY ERROR	Indicates that a word read from memory had incorrect parity.

When the computer executes a HLT, it stops with RUN and PAUSE off, and END and OPR on. The MB lights display the next instruction, the PC and MA lights indicate the address of the next instruction to be executed, i.e., the instruction just retrieved from memory in end time.

Operating Key	Function
START	Pressing this key clears AC, L, MB and the in-out equipment. It turns off ION, PARITY, and PARITY ERROR. It sets the END state, and lights RUN, causing the computer to begin normal operation by retrieving an instruction from the location currently addressed by PC.
LOAD ADD	If RUN is off, pressing this key clears AC. It turns off ION and loads the contents of the switch register into PC, and lights FETCH and AND.
DEP	If RUN is off, lifting this key deposits the contents of the switch register into the memory location currently addressed by PC, increments PC by one, and lights FETCH. At the completion of the operation, the AC and MB lights display the word deposited, PARITY indicates its parity, MA addresses the location into which the word was deposited, and PC contains the next consecutive address.
EXAM	If RUN is off, pressing this key turns off PARITY ERROR, clears AC, displays the contents of the memory location addressed by PC in the MB and PARITY lights. It increments PC by one, and lights FETCH. At the end of the operation MB and PARITY display the word, MA addresses the location that was examined, and PC addresses the next consecutive location.
CONT	Pressing this key lights RUN, causing the computer to begin normal operation in its current state. If RUN is already lit the key has no effect.
STOP	Pressing this key while RUN is lit causes the computer to stop with FETCH lit. At this time the instruction lights indicate which instruction is about to be executed, MB contains the instruction word or operand (or an address if an indirect bit was used) depending on the type of instruction, and PC points to the location one beyond that from which the instruction was retrieved. The MA lights indicate the address from which the last memory word was fetched. They represent either the address of the instruction or the operand (or an address if an indirect bit was used) depending on the type of instruction. The instruction indicators will display the type of instruction.

Operating Switch	Function
SING INST	While this switch is in the up position, the processor stops in fetch time of every instruction that it executes. Hence the operator can run a program one instruction at a time, by turning on this switch, fetching the first instruction by pressing START, and executing each succeeding instruction by pressing CONT. Each time the computer stops, the lights display the same information as when the STOP key is pressed.
SING STEP	While this switch is in the up position, the processor stops at the end of every word-time that it executes. This switch is for maintenance purposes and allows the operator to run a diagnostic routine or other program, one

SING STEP (continued)

step at a time. Operations are begun by pressing START, and each succeeding word-time is initiated by pressing CONT. The reader can determine the information that should be displayed on the panel by consulting the flow charts.

2.4 TELETYPE OPERATION

The teletype provides two-way communication between operator and computer. It is actually four devices: keyboard, printer, reader and punch, which may be operated in various combinations. The equipment operates at speeds up to ten characters per second, with 8-bit characters plus start and stop control signals transmitted serially.

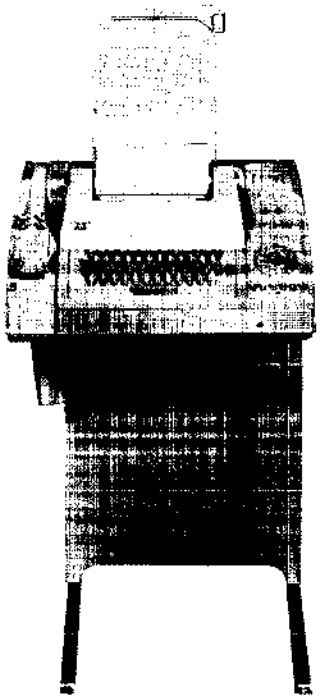


Figure 2-2 Teletype Model ASR 33

Located at the right front right-hand side of the unit is a 3-position rotary switch LINE/OFF/LOCAL. When this switch is set to LOCAL, the entire unit is independent of the computer and the keyboard and printer function together as a normal typewriter. Moreover, turning on the punch allows the operator to punch a tape from the keyboard, and running the reader allows a tape to control the printer (if the punch is also on, it duplicates the tape).

Turning the switch to LINE connects the unit to the computer and separates its input and output functions. Any information transmitted to the computer from the keyboard affects the printer only insofar as the computer sends it back. Turning on the reader places it under program control, and turning on the punch causes it to punch whatever is sent to the printer by the computer.

The only control on the reader is a 3-position switch. When the switch is in the FREE position, the tape can be moved by hand freely through the reader mechanism. The STOP position engages the reader clutch so the tape is stationary but the reader is still off. Turning the switch to START causes the reader to read the tape if the unit is in local, but places it under program control if on line.

The operator controls the punch by means of four pushbuttons. The two on the right turn the punch on and off. Pressing the REL button releases the tape so that it can be moved by hand through the punch mechanism. Pressing B. SP. moves the tape backward one frame so that the operator can delete a frame that is incorrect by using the RUB OUT key (rubout characters are ignored when the tape is read).

The keyboard resembles that of a standard typewriter with four rows of keys and a space bar. The line feed moves the carriage only vertically with a spacing of six lines per inch. The return moves the carriage to the left margin but does not feed a line. To start a new line, the operator must strike both return and line feed. Codes for the characters on the lower parts of the key tops can be transmitted merely by striking the keys. Codes for printable characters on the upper parts (punctuation, ampersand, percent sign) are transmitted by holding down the shift key when striking the character key. Control codes are transmitted by holding down the control key CTRL, while striking the appropriate character key. Codes for all characters listed on the keyboard and some that are not can be transmitted to the computer, but codes for some of the control functions have no effect on the printer when sent back. Table 2-3 lists all codes, their ASCII assignments, and the key combinations required to transmit them. The 8-bit codes are listed below. An asterisk indicates a code that nas no effect on the Model 33. The characters actually contain only seven information bits; the eighth bit may be used for parity, but currently all machines are set up so that the eighth bit is a mark, and thus the codes generated from the keyboard are 200_8 greater than the corresponding ASCII codes.

Table 2-3.
Teletype Code

Octal Code	ASCII Character	Key Combination	Remarks
200	NULL	SHIFT CTRL P	Null
201*	SOM	CTRL A	Start of message
202*	EOA	CTRL B	End of address
203*	EOM	CTRL C	End of message
204	EOT	CTRL EOT	End of transmission; shuts off TWX machines
205	WRU	CTRL WRU	"Who are you?" Triggers "Here is...," at remote station
206*	RU	CTRL RU	"Are you...?"

Table 2-3. (continued)
Teletype Code

Octal Code	ASCII Character	Key Combination	Remarks
207	BELL	CTRL BELL	Rings the bell
210*	FE	CTRL H	Format effector
211	HT	CTRL TAB	Horizontal tab
212	LF	LINE FEED	Line feed
213	VTAB	CTRL VT	Vertical tab
214	FF	CTRL FORM	Form feed
215	CR	RETURN	Carriage return
216*	SO	CTRL N	Shift out
217*	SI	CTRL O	Shift in
220*	DC0	CTRL P	Device control reserved for data line escape
221	DC1	CTRL Q	Turns reader on
222*	DC2	CTRL TAPE	Turns punch on
223	DC3	CTRL XOFF	Turns reader off
224*	DC4	CTRL	Turns punch off
225*	ERR	CTRL U	Error
226*	SYNC	CTRL V	Synchronous idle
227*	LEM	CTRL W	Logical end of media
230*	S0	CTRL X	Separator, information
231*	S1	CTRL Y	Separator, data delimiter
232*	S2	CTRL Z	Separator, words
233*	S3	SHIFT CTRL K	Separator, groups
234*	S4	SHIFT CTRL L	Separator, records
235*	S5	SHIFT CTRL M	Separator, files
236*	S6	SHIFT CTRL N	Separator, miscellaneous
237*	S7	SHIFT CTRL O	Separator, miscellaneous
240	Space	Space bar	
241	!	SHIFT !	
242	"	SHIFT "	
243	#	SHIFT #	
244	$	SHIFT $	
245	%	SHIFT %	

Table 2-3. (continued)
Teletype Code

Octal Code	ASCII Character	Key Combination	Remarks
246	&	SHIFT &	
247	'	SHIFT '	
250	(	SHIFT (	
251	)	SHIFT)	
252	*	SHIFT *	
253	+	SHIFT +	
254	,	,	
255	-	-	
256	.	.	
257	/	/	
260	ø	0	Zero, prints with a slash
261	1	1	
262	2	2	
263	3	3	
264	4	4	
265	5	5	
266	6	6	
267	7	7	
270	8	8	
271	9	9	
272	:	:	
273	;	;	
274	<	SHIFT <	
275	=	SHIFT =	
276	>	SHIFT >	
277	?	SHIFT ?	
300	@	SHIFT @	
301	A	A	
302	B	B	
303	C	C	
304	D	D	

Table 2-3. (continued)
Teletype Code

Octal Code	ASCII Character	Key Combination	Remarks
305	E	E	
306	F	F	
307	G	G	
310	H	H	
311	I	I	
312	J	J	
313	K	K	
314	L	L	
315	M	M	
316	N	N	
317	O	O	
320	P	P	
321	Q	Q	
322	R	R	
323	S	S	
324	T	T	
325	U	U	
326	V	V	
327	W	W	
330	X	X	
331	Y	Y	
332	Z	Z	
333	[	SHIFT K	
334	\	SHIFT L	
335	]	SHIFT M	
336	↑	SHIFT ↑	
337	←	SHIFT ←	
340-373*			Lower case letters; codes cannot be generated from keyboard and should not be used in programs for reasons of compatibility
374	ACK		Acknowledge; code cannot be generated from keyboard and should not be used in programs for reasons of compatibility

Table 2-3. (continued)
Teletype Code

Octal Code	ASC II Character	Key Combination	Remarks
375*	①	ALT MODE	May be used for any desired control purpose
376*	ESC		Escape; code cannot be generated from keyboard and should not be used in programs for reasons of compatibility
377*	DEL	RUB OUT	Delete
		REPT	Causes any other key that is struck to repeat continuously until REPT is released
		HERE IS	In local, punches 20 lines of tape feed
		BRK RLS	Not connected

At the right end of the second row from the bottom is the repeat button (REPT). Pressing this button and striking any character key causes transmission of the corresponding code so long as REPT is held down. Characters that require the shift key may also be repeated in this manner, but there is no repetition of control characters. Pressing HERE IS (top row, right end) with the unit in local punches 20 lines of tape feed.

2.4.1 Tape

The tape moves in the reader from back to front with the feed holes closer to the left-hand edge. To load tape, set the switch to FREE, release the cover guard by opening the latch at the right, place the tape so that the sprocket wheel teeth engage the feed holes, close the cover guard, and set the switch to STOP.

To load tape in the punch, raise the cover, feed the tape manually from the top of the roll into the guide at the back, move the tape through the punch by turning the friction wheel, then close the cover. Turn on the punch with the unit in local and punch about two feet of leader. Code 200 or 377 can be used for leader or trailer. Press the CTRL, SHIFT and P keys to generate 200 (null); press RUB OUT for 377.

2.4.2 Paper

The printer may be either a sprocket feed or friction feed and uses 8-1/2 in. x 11 in. fanfold form paper or 8-1/2 in. roll paper. The roll supply is held in a tray at the back of the unit and printed forms can be torn off against the edge of the glass window in front of the platen. To replace the paper, first remove the upper cover by pressing the cover release button on the right-hand side. To free the remaining old paper for removal, lift the paper guides by pushing the handle marked PUSH at the right of the platen. To insert new paper from the tray, bring it up below the platen at the rear, line up the

holes at the edges of the paper with the sprockets, and press line feed (in local) to draw the paper under the platen.

NOTE

Paper guides and sprockets do not exist on friction feed version.

2.4.3 Ribbon

Replace the ribbon whenever it becomes worn or frayed or the printing becomes too light. Disengage the old ribbon from the ribbon guides on either side of the type block, and remove the reels by lifting the spring clips on the reel spindles and pulling the reels off. Remove the old ribbon from one of the reels and replace the empty reel on one side of the machine; install a new reel on the other side. Push down both reel-spindle spring clips to secure the reels. Unwind the fresh ribbon from the inside of the supply reel, over the guide roller, through the two guides on either side of the type block, out around the other guide roller, and back onto the inside of the takeup reel. Engage the hook on the end of the ribbon over the point of the arrow in the hub. Wind a few turns of the ribbon to make sure that the reversing eyelet has been wound onto the spool. Make sure the ribbon is seated properly and feeds correctly in operation.

2.4.4 Tabs

Each tab mechanism, horizontal and vertical, is a slotted wheel surrounded by a spring on which are mounted a number of tab stops. The slotted wheel for the horizontal tab is mounted on the spacing drum, and the tab can be set by inserting a tab stop in a groove where it catches the tabulator pawl when the type block carriage is in the desired position. With needle nosed pliers, lift the tab stop out of the slot in the wheel against the spring tension. Slide the stop along the spring in the desired direction and reinsert it into the slot at the new location. A stop may be removed from use by turning it so that it does not catch the pawl. The slots in the disc of the vertical tab mechanism allow tabs at any desired lines, but adjacent tabs must be at least an inch apart.

CHAPTER 3
SYSTEM LOGIC

In addition to presenting a detailed description of the logic of the PDP-8/S and the Teletype ASR 33, this chapter explains the organization of the drawings and the conventions used in them that represent that logic.

3.1 DRAWINGS

There is a complete set of electrical drawings, consisting primarily of D-size flow charts and logic drawings (block schematics) that accompany each PDP-8/S. Every drawing is labeled with a DEC drawing number in five parts, such as D-BS-8S-0-14. The first part is a letter indicating the size of the drawing; the second is a mnemonic code indicating the type of drawing; the third is the type code of the equipment (8S for the computer, PT08 for the teletype); the fourth is the drawing serial number (see next paragraph); and the last is a number specifying the individual drawing. If a drawing includes several sheets, both the sheet number and the number of sheets are written at the lower left of the drawing number. If a drawing is revised after being signed by the project engineer, a revision letter is written at the right.

Some typical drawing type codes are BS (block schematic), BD (block diagram), FD (flow diagram), TD (timing diagram), MU (module utilization), ML (master drawing list), PL (parts list), CL (cable list), WL (wiring list). The last four codes are usually A size.

Numbers on drawings of individual circuits are of essentially the same form based on the circuit type number. These are usually B or C size and are drawing type replacement schematic (RS). At the right of the drawing number there may be a letter or number that indicates a revision of the drawing. At the left or below the drawing number, there may be a letter or number that indicates a revision of the printed circuit.

Almost all of the drawings included in this manual are flow diagrams, logic drawings, and circuit schematics. (Appendix 1 describes the other types of engineering drawings and their use.) Drawings in the manual are intended for instruction purposes only, so persons working at the machine should use the prints that accompany the equipment rather than the figures in the manual. Drawings printed in the manual are serial 0, corresponding to the standard production machine. Although every computer is assigned a different serial number, most of the prints accompanying the equipment have drawing serial 0. But if a particular computer differs in some way from the standard machine, those drawings that reflect the difference have the same serial number as the lowest numbered machine that is so modified. Therefore, although the manual drawings are complete for the standard computer, maintenance personnel should use the separate prints for work on the equipment because they show any variations peculiar to the installation.

At the back of this manual the circuit schematics are in order by circuit type number, and the remaining drawings are in order by individual drawing number, i.e., they are ordered by the last part of the drawing number, and it is these individual numbers that are used for reference throughout this chapter. Hence the drawing (D-BS-8S-0-14) mentioned above is variously referred to in the text as print 14 or drawing 14.

3.1.1 Logic Drawings

The logic drawings are block diagrams that show the function of every logic element used in the computer. They also indicate the signal present at any module connector pin that carries a logic signal or some special voltage. The standard power and ground pins (A to C on every module) are not shown. In addition to giving the function of every logic element, the drawings identify every circuit by type number as given in the DEC Logic Handbook followed by the letter for the output pin of the particular part of the circuit used. Below the type number is a location code made up of one digit, one letter and two digits. For example, the location code 1 B29 represents module connector 29 in mounting panel B (all location codes begin with a redundant 1 -- the entire computer is contained in a single group of mounting panels). Pin designations are formed merely by adding the pin letter to the location code. Note 1 B29D. Some modules are double height and have two connectors. On the circuit schematic, A and B preceding the pin letters indicate the upper and lower connectors respectively, but on the logic drawings the prefixes are the appropriate mounting panel letters. Taps (if any) located on the handle end of the module are numbered. In the lettering on the drawings, the numeral 0 has a slash through it (Ø) to distinguish it from letter "O".

By convention, a logic level is regarded as true when negative (-3 Vdc) and false when ground. If a line carries a logic level that represents some logic function X, then the line is labeled X if it is negative when X is true, but is labeled -X (not X) if it is ground when X is true. It is easier to regard pulses as timing functions rather than logic functions, but for consistency a positive-going pulse is regarded as false and the line carrying it is so labeled. These conventions apply to all but the teletype drawings, whose conventions are explained with the description of the teletype in the last section of the chapter.

Figure 3-1 shows the symbols used to represent the logic circuits on the block schematics. Information about these circuits is given in the DEC Logic Handbook, but the system of diamonds and triangles used there to show signal type and polarity is not used here. All blocks are labeled to show logical and/or electrical function, except flip-flops which can easily be recognized by the form of their representation and are named according to their use or the meaning of the information they contain. Logic gates are labeled from the point of view that negative is true. Inputs are at the left of a block, and outputs are at the right or top. Signal names are written slightly above horizontal lines or their extensions.

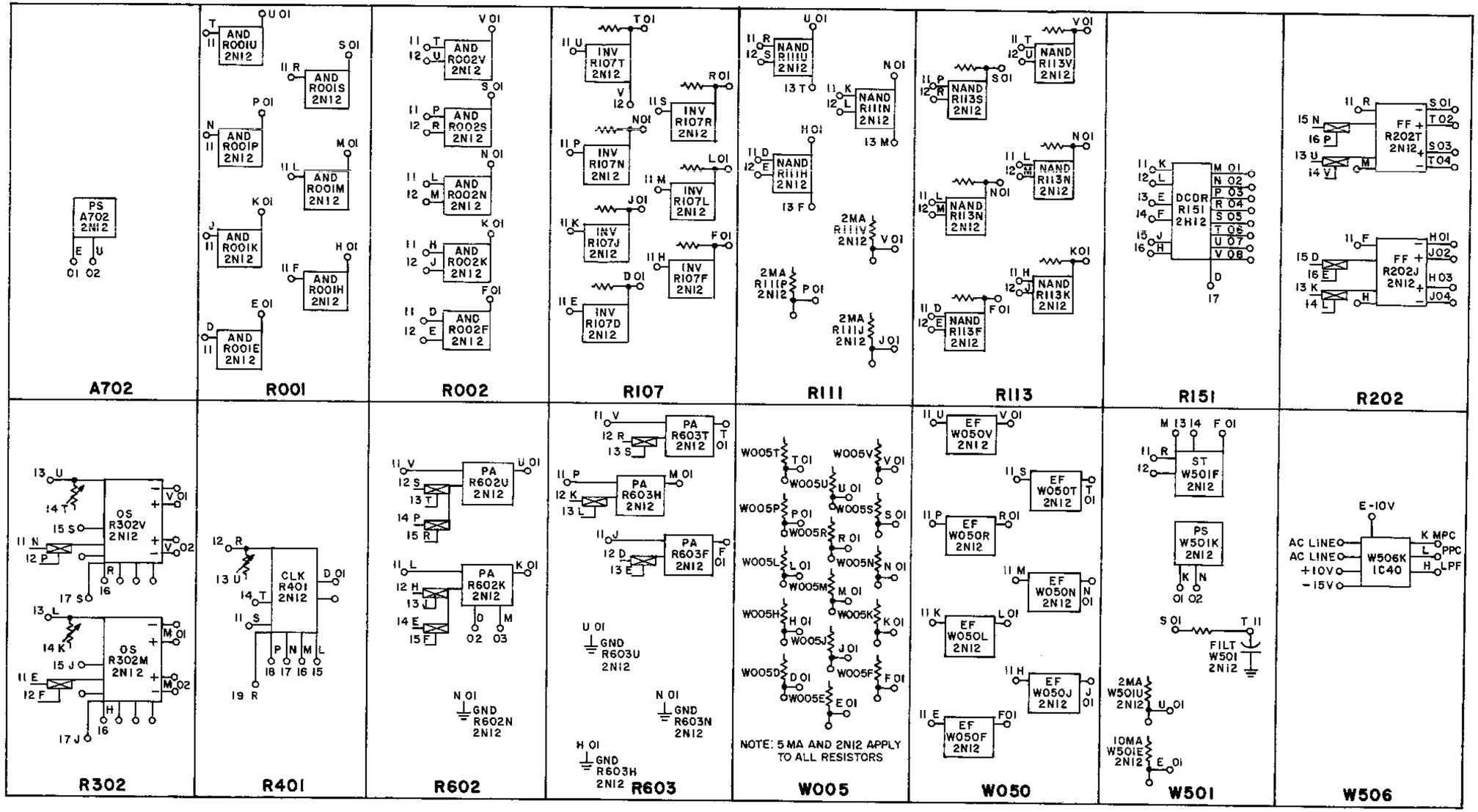


Figure 3-1 Logic Symbols

Each NAND gate actually has two parts, a diode AND gate and an inverter. The nodes shown below the blocks for the R111 gates are points at which other AND gates can be connected in conjunction with the AND part of the R111. The 0 and 1 inputs to the R151 decoder receive signals, wherein a negative level represents the state of a binary source, i.e., if the signal X is applied to pin L, -X must be applied to K. The single output selected by a given input configuration is at ground provided that the enabling input D is also at ground.

The diode-capacitor-diode input gate used with flip-flops, one-shot delays, and pulse amplifiers requires a ground-enabling level, and the triggering input to the DCD gate, as well as direct triggering inputs to the circuits, require positive-going pulses or level changes. The R401 clock produces a pulse train, and a negative enabling level is present at S. PA and clock outputs are positive-going 100-ns pulses, but one of the PAs on R602 produces 400-ns pulses if D and M are jumpered.

If a pulse is applied to both input gates of a flip-flop while both are enabled, the flip-flop complements. A flip-flop can also be set or cleared by grounding its 0 or 1 output, respectively. Note that on the symbol representing a flip-flop (and also the one shot), the output terminals are drawn twice using signs to show the polarities associated with either state of the circuit. They are drawn in such a way to eliminate excessive line crossing in showing the shift connections from one bit of a register to another, and also for ease in recognizing the required state of the flip-flop in cases where connecting lines are drawn directly from its outputs to other circuits on the same print. Nominally, the 1 and 0 outputs are those so labeled on the circuit schematic, these being the ones shown as negative beside the 1 and 0 in the illustration. In the logic drawings, however, the output names are reversed whenever the logical configuration is simplified by doing so.

The W501 is a Schmitt trigger circuit that produces a standardized logic level change from a switch closure. The W506 is a monitor that generates clear levels at power turnon or failure. The remaining circuits illustrated do not take part in the actual logical flow of events. The A702 is a -10V reference supply in the memory, the W005 contains clamped loads, and the W050 contains emitter followers to drive indicators. An emitter follower output is always labeled only by the pin to which it is connected. It never has a logical name.

Occasionally, in the text and flow charts, the location of a circuit on a block schematic is called out by rectangular map coordinates. Each drawing has eight columns numbered from right to left and four rows lettered from bottom to top.

3.1.1.1 Signal Notation. - Signal names are usually mnemonics that indicate the function or meaning of the signal. Composite signals sometimes have short names indicating function, but usually a composite is named by the entire logical function it represents, with a plus sign indicating logical OR and an asterisk indicating AND. Every flip-flop has a name which is also the name of its 1 output; the same

name preceded by a minus sign specifies its 0 output terminal. A minus sign applies only to the term it precedes unless parentheses are used to group terms.

Associated with every register is a shift pulse that shifts the contents of the register to the right and whose name is the name of the register followed by the letters SH. The name of the shift input to the left end of the register is the name of the register preceded by the letters RI "(readin)". Numerals that represent register bits are merely appended to the register name. For example, bit 11 in PC is PC11. Outputs of the flip-flops in some registers are buffered, and the buffer outputs are named by the register name preceded or followed by a B. In the case of MB and the word-time flip-flops, the direct outputs are used only locally (e.g., as the bit-to-bit shift levels in MB), so the flip-flop names are assigned to the buffer outputs rather than the actual outputs of the flip-flop circuit. Therefore, the logic signal WTD is actually the output of an inverter driven from the 0 output of the WTD flip-flop.

With only a few exceptions, the source of any signal, i.e., the drawing that shows its generation, is obvious from its name. Any signal that contains the name of a register is generated on the drawing that shows the register, and any signal that begins with BT originates on the drawing that shows the bit timing. Table 3-1 lists the various mnemonic codes, their meanings and the drawings associated with them.

Table 3-1.
Mnemonic Index

Code	Print	Meaning
A	11	Basic time pulses generated by bit timing
AC	20,10	Accumulator
BT	11	Bit timing
IC	5	Information collector
IO	17	In-out
IR	16	Instruction register
L	20,10	Link
MA	12	Memory address
MB	9	Memory buffer
MEM	22,23 4,18	Memory (8K) Memory (4K)
PC	19	Program counter
S	14	Sum output of adder
WT	13	Word timing

AC and L are shown together on drawing 20, and some of the control signals for both are on print 10. Any composite signal that begins with an instruction mnemonic originates on the instruction register drawing; the parity logic is shown with MB; the skip control flip-flop (SKP) is on print 10; and the various functions originating from console keys and switches are on print 15.

3.1.2 Flow Charts

Drawings 29 and 30 are flow charts of all operations that can be executed by the PDP-8/S and the teletype. These figures show every event, and insofar as possible, show the flow of operations in a manner that is equivalent to the actual gating and timing in the hardware. The terminology is from the logic drawings unless italicized.

Except for connections from one line to another or a return loop, flow in time is always down. A pair of horizontal lines breaking a vertical line indicates a delay; between the lines is listed the delay time, or the condition that must be satisfied to continue the flow. Pulses always appear in ellipses and events or level assertions in rectangles. For more complete correlation with the logic drawings, an empty ellipse indicates a pulse amplifier whose output has no name. A condition written on a line must be satisfied for flow to continue along the line. When several vertical lines branch from a horizontal line, the conditions are written above the vertical lines. To follow the chart, the reader must realize that at any branch point the flow continues on all lines whose gating conditions are satisfied.

In several cases the same event occurs in a number of flow lines, and such an event is often controlled by a composite function which may or may not have a simple mnemonic name. These composite functions seldom appear on a flow line because they are satisfied by the lesser conditions associated with the individual line. In other instances, instruction mnemonics appear as gating conditions, whereas the gating levels in the logic may be the combination of several terms that taken together represent the instruction. In any event, every composite function that appears in the logic drawings with a distinct name (that is not written merely as a combination of all its terms) is written on the chart, usually near that part of the flow in which it plays a role. Note that the logic functions SKIP and OP SKIP are used on the flow charts for convenience only. They do not appear on the logic drawings.

Drawing 30 shows the main flow including all word times and all operations executed from the console. The loop in the upper left-hand corner represents the processor clock, which is always in operation unless the word time has been stopped for a memory cycle. The clock output does not operate the processor, however, unless RUN has been set in one of the lines of flow that originate from console keys, as shown in the upper right. The remainder of the chart shows the many operations that occur at the different word-time pulses in all of the instruction word-times, the break word-time, and the word-times executed for the console functions Load Address, Deposit, and Examine.

The main line is the vertical one at the left, originating in the clock loop. The first horizontal line to the right is merely for a clear function at power turnon or power failure. While RUN is set, the clock output produces the basic A pulses that generate the bit time functions by shifting the timer T. The remaining lines to the right represent the generation of the bit time pulses. The first line represents only the first pulse in each set of fourteen and it is used only for special functions including entry into the in-out sequence, which is shown in a separate flow chart in the lower left on print 29. The special sequence shows the events associated with IOTs for the processor, and the right two-thirds of the drawing contains detailed flow charts of input and output teletype operations.

The pulses triggered in the third line to the right occur only at the first two bit-times and are used only for right rotation. The next line stems from the first twelve bit-times, and it is this set of twelve pulses that controls the processing of full words for all information transfers, addition, logic functions, incrementing, and testing conditions for skips. The next line represents the thirteenth bit time, and its pulse A12 triggers individual events that are required for certain operate instructions, checks parity, checks for overflow in addition, triggers a memory cycle whenever one is required, and stops the computer on a programmed or operator halt. Calling a memory cycle stops the clock, and flow continues to the memory chart in the upper left on print 29. The bottom line represents the final bit time, which controls the selection of the next word time.

Note that in the flow chart all gating conditions are written as logic functions without regard to truth values associated with voltage levels. In other words, an event that occurs in the fetch word-time is gated by WTF, whereas the actual gating level shown in the logic drawings may be a negative level labeled WTF or a ground level labeled -WTF. Similarly, the reader can easily determine whether a level in the logic labeled -X causes an event to occur when X is true or when X is false by consulting the equivalent representation of the logic in the flow chart.

3.2 TIMING

The timing for processor operations is in two parts, the generation of the bit-time pulses to control the sequence of events in each word time, and the selection of the different word-times to control the overall execution of computer instructions, breaks, and console functions.

As can be seen at the top center of the main flow chart (drawing 30) every pulse from the clock complements a flip-flop that is shown at C4 in logic drawing 15. Every time the flip-flop clears, it triggers a series of clear pulses for the logic if the processor power clear level is true. The turnon of this level also clears other control flip-flops, places the computer in fetch time, and resets the timer to its initial state. The PPC level comes from the power monitor, shown at bottom center on drawing 17. This circuit monitors the +10V and -15V logic supplies and the -10V memory reference. It produces power-clear signals for both memory and processor whenever any voltage is not within its proper range. At power turnon, both clear outputs remain at ground until about 50 ms after the last voltage threshold

has been met to allow any motors, solenoids, relays, and the like, to reach operating conditions. Then MPC goes off (-MPC drops to -13V), and about 5 ms later PPC turns off. Whenever any voltage fails to maintain its proper value, the outputs remain negative for 9 to 16 ms, at which time PPC turns on, clearing the processor and 3 to 10 ms later MPC clears memory control.

The power monitor module also contains a low power condition flag (LPC), which can be used to restart the computer automatically, following a power failure. In 3 to 6 ms after any voltage failure LPC sets, and this state change requests a program interrupt if the interrupt is enabled. In this way, before the power-clear levels turn on, the program has at least several milliseconds in which to store the various processor registers in memory and place an appropriate jump in location 0. After the power-clear signals go off (power is restored), LPC clears, restarting the computer at location 0, if the optional auto restart circuit (W501 in 1E5) is in the machine. The auto restart is disabled by removing this module.

3.2.1 Bit Timing

Print 11 shows the clock, the timer or time ring counter T, and logic that decodes the counter to generate the bit time functions and pulses. The clock at the upper left generates a pulse train except when WTS is set to stop the word time for a memory cycle. So long as RUN remains set, the pulse train triggers the A pulses which rotate T to the right. The input gating levels to T0 are reversed from those for the other bits, so each shift places the complement of T6 in T0.

The initial pulse in Load Address, Deposit or Examine resets the timer to its initial state. The RT pulse is applied to the common set input (M) of the last two bits at the right, but the 0 and 1 sides of T5 are reversed, so only T6 is set. All remaining bits are cleared. The same configuration is produced by power clear.

From its initial state with a 1 in T6, the A pulses fill T with 1s from the left until it is all 1s, then 0s come in from the left until it is clear. The generation of bit-time levels from the T-states is shown in the upper left of the flow chart, and the generation of bit time pulses is listed on the logic drawing. A given bit-time level conditions the logic to produce a time pulse having the same number, but the pulse also steps the counter to the next bit time. For example, when T is clear, BT00 is true and the next A-pulse generates A00, but this same pulse sets T0, thus generating BT01. Note that the initial state of the timer actually corresponds to the final bit-time in a processor cycle, so the first pulse is actually A13, which selects the proper word-time to enter. Every A12 should automatically produce this state, but A12 triggers the reset pulse to force the state and prevent any malfunction from disrupting more than one cycle. Note also that the initial pulse in the console operation start clears T6 so that the computer starts at the beginning of a word time. It is assumed that the operator will press the start key only when the timer is in its initial state and hence all other bits are clear.

The logic on the left-hand side of drawing 11 decodes the register for the bit-time levels that serve as gates for the PAs to generate the time pulses. The top PA generates a pulse only at the beginning of each word time, the second PA produces a pair of pulses for the first two bit times. Individual pulses produced during the last two bit times, 12 and 13, and a string of 12 pulses for the basic word processing is produced while BT (00-11) is true. The main string and A12 are combined to produce a string of 13 A(00-12) pulses to control the carry flip-flop during addition. The remaining gates generate two BT levels, each of which is true during part of the basic processing time, to control the transfer of an address to MA after each instruction is fetched (the instruction word specifies only a 7-bit address).

3.2.2 Word Timing

The column of flip-flops at the center of drawing 13 controls the execution of the various word times except for console functions. The third flip-flop from the bottom, AI, specifies whether an instruction addresses an autoindexing location. At the end of each word time, the nets at the left of the flip-flops determine which word time must be entered next, and A13 triggers the transition by clearing any WT flip-flop that is set and setting the appropriate one for the next word time. The direct outputs of the WT flip-flops drive only inverters whose outputs in turn are used for all logic connections; the flip-flop names are applied to these buffered outputs. (The names do not reflect the fact that the signals are buffered.)

The logic net at the left of AI grounds the enabling level for the AI set gate if the left half of MA is clear. Bits 5 through 7 of MB are clear and MB08 is 1. The appearance of this configuration in the fetch time of an instruction that calls for indirect addressing indicates that one of the autoindexing locations, 10-17, is being addressed. Of course AI is set at A12 in any word time in which this particular configuration exists, but its being 1 is used to control the selection of index time only when such selection is possible.

The final pulse in every word time, A13, always clears AI, but it is applied to both set and clear gates of all other flip-flops. The level inputs to the clear gates are grounded and therefore always enabled, but the gating levels for the set inputs come from logic nets that determine which word time the computer must enter next. Since no word time ever follows itself, the set inputs are enabled at only one, or at most, two flip-flops and these must presently be clear. Pulse A13 clears any flip-flop that is presently set, and sets only the ones appropriate to the next word time. State changes in the flip-flops are shown in detail at the bottom of the main flow chart (print 30).

During any word time in which the processor must deposit a word in memory, the net in D3 of print 13 pulls the -WTWR level false. A similar net in B6-7 grounds -WTRD in any word time that must retrieve a word from memory. If either type of memory cycle is necessary, A12 triggers the memory request pulse MP through the PA in the lower left-hand corner of the drawing. This pulse triggers one or the other of the two PAs just to the right to start a read-write or a clear-write memory cycle depending

upon whether reading or writing is required. MR also sets WTS (B3) to stop the word time by stopping the clock. At the end of the memory cycle, the MEMGO level goes false, clearing WTS and allowing the clock to proceed to A13.

The AND gates hung on the outputs of WTS, WTE, and WTF set or clear these flip-flops for various console operations and power clear. The direct set and clear inputs to all of the flip-flops are also used for this purpose. The remaining logic nets at the right-hand and the upper left-hand sides of the drawing generate various composite control levels whose names in all but two cases are written out. WTINCPC at the upper left (D6) gates PC into the adder whenever it must be incremented; WTINCR inputs a 1 to the adder whenever any register is being incremented.

3.3 REGISTERS

The registers in the computer are used in different ways, and their names reflect their use. But regardless of their use they all function in essentially the same way. All are shift registers in which one bit is connected to the next for right shifting. In a few cases, the direct set and clear inputs to the register flip-flops are used either to clear a register or to effect a parallel transfer (as from the switch register to AC), but there is no complicated input gating for producing logical or arithmetic functions or parallel transfers from various sources. Whenever the contents of any register change or are transferred to another register, information is shifted to the right in all registers affected. Information from a register is made available only one bit at a time at the right end (LSB), and information is shifted into a register only one bit at a time at the left end (MSB). A register clears if it has no input while it is shifting, but often the input to a register is its own output, so the contents of the register are recirculated while it is supplying information to some other register. All registers except IR have 12 bits, but AC and the link often function together as a 13-bit register. IR has only four bits.

3.3.1 Instruction Register

The register that holds the instruction code and indirect bit during the execution of each instruction is shown in the upper left-hand side of drawing 16. IR is cleared only in special circumstances, such as at the beginning of a console operation or a program break. After each instruction is fetched from memory, the contents of MB are shifted into IR by the standard 12-bit shift, which therefore leaves the left four bits of the word in IR and drops out the address part at the right.

The R151 at the right decodes the left three IR bits to determine the instruction; one of the decoder outputs is always at ground to specify some instruction except when an Examine or Deposit is being executed. IR03 is combined with the two states of A1 to select indirect addressing with or without autoindexing. At the lower left (A7) the OPR level is combined with the two states of IR03 to determine the operate group. The OP1 level is then further combined with bits from MB to determine the specific operate instruction. The remaining nets generate composite functions to control events common to more

than one instruction or to determine specific conditions within one or more instructions, for example, to determine whether the count is zero in an ISZ (ISZ · ZI) or to determine the circumstances in which PC must be incremented an extra time.

The meanings of the functions generated are obvious except for the rotate levels at the right. ROTR is true during right rotation (OP1 · MB08) when either MB10 is true or the processor is not in the first bit time (BT00 is false). This level gates the A(00-01) pulses for the right shift so there can be at most two shifts. If a 1 is programmed in instruction bit 10, both shifts occur, but if bit 10 is 0 there is only one shift at BT01.

There are no gates for left shifting, so a left rotation is produced by a shortened right shift. AC and L are rotated together, so a complete rotation would require 13 shifts. Since the right shifting for a left rotation occurs on A(00-11), there are at most 12 right shifts (the result is at least one left shift). The shifting is controlled by ROTL which is true during left rotation (OP1 · MB09) when either MB10 is false or BT00 is false. If a 1 is programmed in bit 10 of the instruction, ROTL is true except during BT00, which eliminates one of the 12 right shifts.

3.3.2 Memory Buffer

Because MB is the buffer between processor and memory (print 9), the entire register is cleared at the M pins by a request for a read-write cycle, and the parallel transfer of a word read from memory is effected by memory output pulses that set individual MB bits. Pressing the start key also clears the register. Direct outputs of the MB flip-flops are used only for shift gating within the register; all remote connections use the inverted outputs whose names do not reflect their being buffered from the register bits. An extra set of buffered outputs for the in-out bus supplies both sides of the center six bits for device selection and the 0 sides of all bits for output in a data break (optional equipment).

The two logic nets in the upper left generate the MB shift pulses and the shift inputs to MB00. MB can receive information from PC or AC for deposit in memory, from the adder during an indexing operation, and from itself while it is being made available to IR and MA in fetch time (-WTS holds off the MB level during memory access). Note that the bottom two gates in the enabling net for the shift pulses are satisfied simultaneously in AND, TAD, and JMP, in which the execute and end times are performed together. In these two word times, input is supplied to MB in only three cases (DCA, ISZ, JMS). Otherwise the gates clear MB except when its contents are needed for the instruction (device selection in an IOT, selecting operations in an OPR).

3.3.3 Program Counter

This register (print 19) receives an address from MA during a jump instruction. It receives the output of the adder when it is indexed in fetch time (Examine and Deposit) when it receives address 0001 in break time, and when it receives an address from the switch register via AC and the adder in

Load Address. During end time, it receives the sum from the adder whenever any extra indexing is required (a skip or a JMS), but recirculates itself in all other instructions except JMP in which it receives MA because WTX and WTE are simultaneous.

3.3.4 Memory Address

Drawing 12 shows the register whose 12 bits select one of the 4096 locations in memory during a memory cycle. At the lower right-hand side of drawing is the page zero flip-flop, which is set by the first pulse in fetch time if bit 4 of the instruction is 0. The shift input nets at the left supply the 7-bit address from MB for the first seven fetch pulses, but recirculate the original contents of MA00-04 in the rest of the word time unless PGZ has been set, in which case the input is inhibited and MA will address page 0. MA receives a 12-bit address from MB in defer time, receives PC for a memory access in Examine or Deposit, and recirculates itself while its contents are being transferred to PC in a jump. In end time, except in JMP, it receives an address for the next instruction retrieval from PC, either directly or incremented by one through the adder. The direct inputs are not used, and the register is cleared only when shifted without input in break time.

3.3.5 Accumulator and Link

AC and L, both shown on print 20, have separate control pulses, but the two function together as a 13-bit register when used for addition or rotation. All 12 AC bits are cleared at once by two of the operate instructions, by an IOT, by power clear, and by any console operation except Continue. To load information from the switch register into AC during Load Address (Deposit or OSR) the logic at the top of print 10 generates the SAC pulse which sets individual AC bits through any switches that are on. AND gates tied to the 0 AC outputs allow pulses from the information collector to effect a parallel transfer into AC from the in-out bus. Buffered AC outputs drive the bus for transmission of information to peripheral equipment.

The shift inputs to AC are produced by the net on the upper left-hand side of print 20, and the shift pulses are generated by the logic in the lower left-hand side. Most shifting is produced by the standard set of A(00-11) pulses (although ROTL may eliminate one of these), but there is an additional shift at A12 in the TAD execute time to complete the 13-bit addition, and one or two shifts may be generated at A(00-01) for right rotation.

During a rotate instruction, the link (at the center left of the drawing) receives information from AC, and AC in turn receives it from L. In TAD, L receives the sum and AC receives L. In IAC or CMA, both AC and L receive the adder output but at different times: in IAC, L complements at A12 if the AC incrementing has produced a final carry (has overflowed); AC is complemented through the adder in CMA, but the CMA input to L is redundant and L merely shifts into itself. The word shifted into AC in AND is the bit-by-bit AND function of the contents of MB and AC. AC recirculates itself

while being shifted to MB in Deposit (the Examine shift is redundant), and it receives its original contents through the adder during OP2 while being tested for zero contents.

Print 10 shows the generation of the control pulses for the link. LSH is generated at the same time as ACSH in those instructions that operate on AC and L together, except in IAC and CMA when LSH is at A12 only. In the upper part of the drawing (print 10) is the net that generates set and clear pulses for L in fetch time of those operate instructions that control it. L is cleared by an instruction that calls only for clearing or calls only for complementing and it is now set. It is set if the instruction calls for both clearing and complementing or calls only for complementing and L is now clear.

3.4 CONTROL CIRCUITS

Besides registers and timing logic, the processor contains a serial adder, parity and skip logic, and circuits associated with the console.

3.4.1 Adder

The serial adder (print 14) produces the sum of a pair of numbers one bit at a time. For each step, the circuit uses three inputs: two are bits from summands SX and SY (two numbers to be added), the third is the carry-in from the previous step (the carry into the first step is of course 0). At each step the address produces two outputs, a bit of the sum S, and the carry out C which is stored in CA for the next step. The outputs are generated in exactly the same way as one would when performing pencil and paper addition of binary numbers. S is true (that is, 1) if the sum is odd, if one and only one input is true or all three are true. The carry is true if the sum is 2 or greater, i.e., if any two inputs are true.

The upper net on the left-hand side of print 14 generates the input SX. This input comes from AC in TAD; but in any other case in which addition is actually performed, SX is true only during BT00 and hence has the effect of adding one to the number received as the SY input. BT00 is gated-in during Examine and Deposit to increment PC, and by WTINCR during any other operation that requires incrementing and also in break time to supply address 0001 to PC (there being no SY input at this time). When there is no SX input, the number shifted out at S is identical to that shifted in at SY. This procedure is used to complement AC, to test it for zero, and to transfer it to PC.

The number shifted into SY is from PC during Examine or Deposit, from MB in addition or indexing, and from AC during Load Address or the operate skip group. WTINCPC gates in PC for normal program counting in fetch time and for a skip or JMS in end time. The remaining gates control SY during the operate instructions CMA and IAC. The gates at the bottom bring information from AC (the left gate receives the complement of AC for CMA) except at BT12 when the top gate substitutes L. The CMA link shift is redundant, but in IAC, A12 complements L when there is a carry (overflow). Note that the gate for IAC, which is enabled by MB11, includes the condition -MB06; so when the program calls for both complementing and incrementing (CIA), the adder adds one to the complement (that is, forms the two's complement).

On the lower right-hand side of print 14 is the zero indicator flip-flop ZI, which is set by the final pulse in fetch time. It is then cleared if the sum is ever true in execute time of an ISZ or the operate skip group.

3.4.2 Parity Logic

On the upper left-hand side of the main flow chart is a small isolated flow diagram beginning with MBSH. It indicates that PG is complemented whenever a 1 is shifted into MB, and PT is complemented whenever the bit shifted out of MB is 1. These events occur whenever MB is shifted in any flow line. On print 9, PT is shown at the top and PG at the left-hand side. Both flip-flops start clear so that whenever MB is shifted, PT tests the parity of the word shifted out and PG generates an even parity bit for the word shifted in.

When a write request is made, A12 shifts PG into PB, which is written in memory with MB. For reading, the CMB pulse that clears MB also clears PB, which is then set if a 1 is read from the parity plane. Following the shifting of any word that has been read from memory (at the end of any word time that follows a read memory cycle), PE SET sets the parity error flip-flop PE if PB and PT differ (if the test bit generated from the word differs from the parity bit read from memory). PE can be cleared by an IOT but is cleared otherwise only by power clear, the start pulse, or the examination of a memory location from the console. Note that detection of a parity error does not change the contents of memory: the word read from memory, whether correct or not, is written back into memory before the test is made.

3.4.3 Skip Logic

The SKP flip-flop that is shown near the center of drawing 10 controls incrementing of PC in execute time for skipping. A skip pulse from in-out control sets the flip-flop directly. The large net at the left of the flip-flop generates the skip condition for operate instructions.

A 1 in bit 5 of the instruction tests for negative AC (AC00 set), a 1 in bit 6 tests for zero AC (ZI set), and a 1 in bit 7 tests for L set. The selection is made by three NAND gates associated with the selection bits in the instruction. The output of any gate corresponding to a 0 selection bit must be negative; a gate output can be ground only if the selection bit is 1 and the selected condition is true.

The complete skip condition appears at the ORed outputs of the two NAND gates in B4. Instruction bit 8 specifies whether the skip is to occur when the selected condition is true or false; hence the upper NAND gate receives MB08 and the output of the selection gates, whereas the lower NAND gate receives -MB08 and the inverted output from the selection gates. If a 0 is programmed in bit 8 and any condition selected by bits 5 through 7 is true (making the output of the selection net ground and its inversion negative), then both inputs to the 1F07U gate are negative and the gating level to the set input of SKP is ground. Similarly, if no selected condition is true, the output of the selection

net is negative; in this case if bit 8 is 1, the 1C07U gate receives negative signals at both inputs. Hence if any condition is satisfied and a 0 is programmed in bit 8, or all specified conditions fail of satisfaction and a 1 is programmed in bit 8, then A12 in OP2 execute time sets SKP. The 1 state of this flip-flop causes an extra indexing of PC during end time of an OPR or IOT.

3.4.4 Console

Print 15 shows the inputs to the system from the console, and the RUN flip-flop through which the console keys and switches start and stop the computer. In the upper left is a register of switches that allow information to be loaded into AC by passing the SAC pulse to individual AC bits. Below the register are the operating keys and switches, each of which can place a ground on a control line provided that the console key lock is closed; if the lock is open, the keys and switches are inoperative.

Closure of any key except stop generates a trigger pulse through the Schmitt trigger circuit at the lower right; the inputs from the deposit, however, examine, and load address keys are gated by RUN, so they have no effect while the computer is in operation. For Continue, TP sets RUN. For Start, TP produces a start pulse SP through the PA at the left of RUN provided that the processor is not stopped for a memory cycle. SP clears most of the computer logic through the PAs in the upper right, and its trailing edge sets RUN through a NAND gate 400 ns later.

For Load Address, TP triggers a pair of load pulses (LP and LPA) 1 μs apart (C3). A similar pulse pair is used for Deposit and Examine, but in this case, TP triggers a common first pulse (DP+EP) and the output of the one-shot triggers separate delayed pulses for the two functions. The delayed pulse in any of these three operations sets one of the flip-flops at the left to control its execution (these are the word time flip-flops for console operations). At the end of the single word time, A12 clears the flip-flops and clears RUN through the PA in B5 to stop the computer.

The net at the far left allows A12 to clear RUN in end time of a HLT. The gates at bottom center cause A12 to clear RUN in fetch time if the stop key or single instruction switch is on, but in any word time if the single step switch is on.

The Schmitt trigger and PA on the upper right-hand side of the drawing are for the optional restart feature after power failure. The clearing of the LPC flip-flop in the power monitor triggers the AST pulse, which starts the computer in the same way the trigger pulse does when the start key is pressed (A4).

3.5 MAIN FLOW

Now that the reader has an understanding of the way the registers and the timing and control circuits function, he should have no difficulty in following any instruction or console function in the main flow chart (drawing 30). A discussion of the flow of events in memory access, the special IOT sequence, and teletype input and output (drawing 29) is included with the descriptions of the corresponding logic in the three sections following this one.

3.5.1 Console Operations

Entry into the flow is always made by means of the console keys, as shown on the upper right-hand side of print 30. For Continue the trigger pulse merely sets RUN to start the computer in its present state.

For Load Address, Deposit and Examine, TP triggers pairs of pulses that place the processor in operation for one word time. The first pulse for all three clears AC, WTF and WTE, and resets the timer. LP additionally clears all word time flip-flops, IR and other control flip-flops. Each of the second pulses sets RUN and a flip-flop that controls the word time for the function. EPA also clears PE, whereas DPA and LPA transfer the contents of the switch register to AC.

Below the initiation of the three functions are the word times used by them. In Load Address, the 12 A(00-11) pulses shift the switch register address from AC through the adder to PC, clearing AC in the process. For the other two operations, the pulses shift PC to MA and index PC. For Deposit they also move the switch register word from AC to MB. After the shifting is complete, A12 clears whichever word-time flip-flop has been controlling the operation, clears RUN, and places the processor in fetch time. For the two functions that require memory access, A12 generates MR, which stops the clock by setting WTS and requests the appropriate type of memory cycle: clear-write to deposit information, read-write to retrieve it. In the latter case, the pulse that triggers the memory cycle also clears MB and PB to prepare them for receiving a word from memory.

Pressing the start key causes the computer to begin normal operation by retrieving the instruction in the location addressed by PC. The trigger pulse from the key generates the start pulse provided that a memory cycle is not now in progress. SP places the computer in end time, clears T6 so the clock will start at the beginning of the word time, and together with two more pulses shown in the same flow line, clears the in-out equipment, MB, AC, IR and most of the control flip-flops in the processor. Finally the trailing edge of SP sets RUN to start the clock. Pressing the start key while the computer is running merely restarts it at the location presently addressed by PC, except that it will not interrupt a memory cycle to do so.

After the reestablishment of the proper voltage levels following a power failure, the power monitor level, LPC goes negative, producing AST, which duplicates the action of the trigger pulse produced by pressing the start key.

3.5.2 Instruction Flow

The loop in the upper left-hand corner represents the clock which is always going except during memory access. If action at the console sets RUN, the pulse train from the clock produces the A pulses that sequence the timer to produce the various bit time functions. The flow follows one or more of the lines to the right, depending upon which BT function is true. Insofar as it is practical, the series of events that make up a single word time appear below one another in the drawing.

Events common to all word times are closest to the main vertical line at the left. The first 13 pulses each save the current carry in CA whether an addition is going on or not. A12 sets A1 if an autoindexing configuration exists in the appropriate MA and MB bits, clears RUN if the single step switch is on, resets the timer, and sets the program interrupt request flip-flop if the interrupt system is on and there is either a parity error, a power failure, or an interrupt request over the in-out bus. A13 clears a number of control flip-flops in preparation for the next word time.

The special word times for Load Address, Deposit, and Examine have already been discussed above. Following Start, the processor executes an end time in which it moves PC to MA and requests a read-write cycle to retrieve the first instruction.

3.5.2.1 Fetch. - After an instruction has been brought from memory, A00 sets PGZ in bit 4 of the instruction word is 0. It also turns on the interrupt system if the preceding instruction was an ION. The full set of word processing pulses A(00-11) moves the instruction code and indirect bit to IR and indexes PC. The first seven of these pulses move the address from MB to MA, and the next five then either reestablish the current page number in MA or clear MA00-04, depending on whether PGZ is clear or set. If IR now contains the code for a group 1 OPR, A12 sets or clears L and/or clears AC if these events are specified. A12 also stops the computer if the stop key or single instruction switch is on, triggers PE SET to check the parity of the instruction word, and requests a read-write cycle to get a new address if the instruction is indirectly addressed or to get either a new address or the operand for AND, TAD or ISZ. The condition on the line leading to MR is the general one for any reading or writing, but on this line it is satisfied specifically by the three conditions for fetch, index, and defer time that are written just at the right.

If RUN is still on when the clock restarts, A13 clears WTF, sets ZI for possible use in the instruction, and puts the processor into the next word time. If the instruction indirectly addresses an autoindexing location, A13 sets WTI; for indirect addressing with AI clear, defer time follows. If the instruction is an OPR or an IOT, or uses a direct address, A13 sets WTX; and it also sets WTE if the instruction is an OPI or a directly addressed AND, TAD or JMP.

3.5.2.2 Index. - This word time merely indexes the address contained in MB, checks its parity, and calls a clear-write cycle to put the incremented address back in memory. The processor then enters defer time.

3.5.2.3 Defer. - This word time moves the absolute address from MB to MA, checks its parity, and reads the operand if the instruction is AND, TAD or ISZ. The processor then enters execute time and enters end time simultaneously for an AND, TAD, OPI or JMP.

3.5.2.4 Execute. - For an IOT, A00 triggers the special in-out sequence. For right rotation, A(00-01) shift AC and L together once or twice as required.

The main set of A(00-11) pulses produces whatever transfers are necessary for the six memory reference instructions. For example, TAD shifts MB to the Y adder input, shifts AC to the X input, and shifts the sum through L back into AC. In ISZ, the SX input is true only at BT00, so the number shifted back to MB from the adder is one greater than that shifted from MB to SY. If the adder output is ever true, ZI is cleared. Note that the events shown for JMP are not complete on the WTX line: the return of MA to itself while being moved to PC appears in the WTE line because it is controlled by end time, which is simultaneous with execute time in this instruction.

Any full word operation required for an OPR also appears in the WTX line for the main set of twelve shift pulses. IAC adds one to AC, CMA complements AC through the adder; if both occur together, the adder receives -AC but IAC still makes SX true at BT00. For left rotation, AC and L are shifted right either 11 or 12 times. For the test-skip group, AC is rotated through the adder, ZI being cleared if the sum is ever true.

Following the 12-bit processing, A12 performs whatever additional operations are required to complete the execution of the instruction. In TAD there is an extra addition step through the adder to put the 12-bit result in AC and complement L from its original state on overflow (the adder input at this time is L, which has been shifted through AC). AND, TAD, and ISZ check the parity of the operand retrieved from memory: ISZ, DCA, and JMS write the operand in memory. IAC also complements L on overflow (CMA appears in the gating condition but has no effect). For the skip group A12 clears AC if bit 4 of the instruction is 1, and sets SKP if the specified skip condition has been satisfied. Finally A13 sets WTE if the processor is not already in end time.

3.5.2.5 End. - For an OSR (a 1 in bit 9), A00 transfers the switch register to AC. A(00-11) determine the address for the next instruction retrieval. For a JMS or an ISZ or OPR skip, PC is indexed and the result goes to MA. If there is no skip and the instruction is not a JMP, PC goes to MA. For a JMP the simultaneous execute time is moving the new address from MA to PC, and the MA shift controlled by end time merely reestablishes MA.

A12 clears SKP, clears RUN on an HLT (a 1 in bit 10), and requests a read-write cycle to retrieve the next instruction. When the clock starts again, the processor enters fetch time if there is no interrupt request, but enters break time if PIR is set.

3.5.2.6 Break. - A00 clears IR and turns off the program interrupt by clearing INS and ION (hence the break now in progress cannot be interrupted). A(00-11) clear MA, shift the present program location from PC to MB, and place address 0001 in PC. Then A12 checks the parity of the instruction just retrieved but not executed, and requests a clear-write cycle to save PC in location 0000. The processor then returns to end time automatically to execute the instruction in location 0001.

3.6 MEMORY

The computer may have either of two memories that differ slightly in physical configuration. The so-called 4K memory is shown in prints 18 and 4; prints 22 and 23 are the equivalent drawings for the so-called 8K memory, which is really a 4K memory mounted on 8K planes (6-1/2 planes of 64 x 128 bit mats). Which memory is in a particular machine can be determined merely by checking the location of the stack (the 8K stack is long and thin, and is used in all machines serial 200 and up).

3.6.1 Memory Control

Prints 18 and 22 show the timing and control logic for the two memories, and a flow chart of this logic is on the upper left-hand side of print 29. The logic is the same for both memories, the two prints being identical except for module locations. The basic timing is supplied by the clock and ring counter shown at the bottom. At power turnon, the MPC level from the power monitor clears this counter, and in every memory cycle it shifts through its 12 states (as shown in the flow chart) returning to zero. The clock setting is approximately 2 mc for the 6.3-μs memory, slightly slower for the 6.5-μs memory.

At left center of the print a request pulse for either type of memory cycle temporarily turns on the MEMGO level, enabling the clock. The first shift from the clock sets A, which holds MEMGO on so that the cycle can continue. Before A clears, F is already set so MEMGO continues until the counter is back to zero. At this time it returns to ground, clearing the WTS flip-flop in the word timing logic, and thus restarting the bit timing clock.

The timing signals to the core logic are derived from the counter and the flip-flop made up of the two NAND gates with feedback in the center of the print. This strobe enable flip-flop is set by a request for a read-write cycle, but is cleared by a request for a clear-write cycle. The read level to the core logic is true during the 2 μs while BM is 1 and FM is 0. During the read period, the single counter state in which DM is 1 and EM is 0 generates the strobe pulse provided that the strobe enable flip-flop has been set. This pulse strobes the memory read outputs into MB; thus when the strobe is not enabled, the read portion of a memory cycle serves merely to clear the addressed location. During the write portion of the cycle, the timing logic generates inhibit and write levels, each of 1.5 μs duration, with the latter beginning and ending 0.5 μs after the former. The inhibit is on while AM is 0 and DM is 1, the write is on while BM is 0 and EM is 1.

3.6.2 Core Logic

Block schematics 4 and 23 show the modules associated with the stack. The 4-wire stack has 13 planes with one sense winding and one inhibit winding per plane. Selection of a single location in the 64 x 64 matrix is accomplished by selecting one each from among 64 X-windings and 64 Y-windings. The two prints are identical except for module locations, and each G607 and G608 in the 4K memory

is replaced by a single G609 in the 8K memory. References in the following paragraphs are to the 8K print with the 4K references given parenthetically wherever necessary.

A single Y-winding is selected by decoding MA00-05 in the W108's, shown above and below the stack. The equivalent circuits that decode MA06-11 to select an X-winding are on either side of the stack. The sense circuits are at the extreme left-hand side in the print, and the inhibit logic is at the right. The -10V reference is supplied to tap terminals 1 and 2 on all W108's via the G609's (G608's). The ground read and write levels from memory control are applied to the lower inhibit W108 at the right; this section of the module is actually independent of the inhibit logic, and the associated drivers are used to generate the negative read and write signals applied to the X and Y W108's.

To understand the decoding of MA to select a pair of X- and Y-windings that intersect at a single location, consider the selection of a single Y-winding by the circuits shown above and below the stack. The top W108 decodes MA00-02 to select a single driver whose two outputs are tied together and connected to one end of a set of eight consecutive Y-windings through selection diodes on part of a G609 (G607). The bottom W108 similarly decodes MA03-05 to select a single driver, but here the driver outputs are applied separately to the selection diodes in part of a G609 (G607). There are two diodes per line and each output of each driver is connected through one set of diodes to eight Y-windings, one from each of the eight sets of eight selected by the top W108's. When MA00-05 is 00, the 0 winding is selected by decoding MA00-02 to select windings 0 through 7 and decoding MA03-05 to select the first winding from each set of eight windings, 0, 8, 16,....

MA remains stable throughout a memory cycle so the same pair of drivers remains selected, but current flows only while the read or write signal is true. The read and write signals are connected to opposite pins on the two driver modules, so one acts as a sink whenever the other acts as a source. Consider what happens when WRITE is true, still assuming selection of winding 0. Pin EE is brought to ground and pin EF floats, but the two are connected together, so windings 0 through 7 are connected to ground at one end. In the bottom W108, pin EF is brought to -10V but EE floats. Both outputs are connected to windings 0, 8, 16, ..., but through different sets of diodes, so the floating output has no effect, and the selected windings are brought to -10V at this end. Thus a current of approximately 200 ma flows from the driver in the top W108 through Y-winding 0 to the driver in the bottom W108. Since only one of 15 windings is connected at both ends, there are 14 that are connected at one end but floating at the other and are hence partially selected. Of these, seven are at ground because grounded at the one end, the other seven are at -10V. The 49 remaining Y-windings float.

During read, current flows in the opposite direction because EF in the top W108 is now at -10V, and EE at the bottom is ground while EF floats. The circuits on either side of the stack select a single X-winding in the same manner, with current flowing from right to left during read, from left to right during write.

The combined effect of the read current flowing through the 13 cores at the intersection of the selected X-winding and the selected Y-winding is sufficient to change to 0 any core that is in the 1 state. (It has no effect on those already 0.) Such a state change produces a pulse on the sense winding in the plane that contains the core. The sense windings are connected via the G609 (G608) at the left to the W532 sense amplifiers, contained two per module. These are ac-coupled difference amplifiers with a difference gain of 90 and common mode rejection of 3 to 1. The outputs of each sense amplifier are in turn applied to a G803 ac-coupled rectifying slicer, also contained two per module. If enabled, the strobe produces an output pulse at each slicer that receives a sense signal representing a change from 1 to 0. These output pulses set individual MB bits. If there is no strobe, the net effect of the read is merely to clear the addressed core location.

While write current is flowing, the combined effect on the 13 cores at the intersection of the selected X- and Y-windings is sufficient to change all the cores from 0 to 1 except those in planes that receive inhibit current that acts to oppose the write current. In the upper W108 at the right, the two inhibit levels are applied to both the 0 and 1 inputs of two sets of the decoding diodes, so the drivers are selected entirely by the other eight inputs. Selection is on a negative input, so a given driver supplies inhibit current to prevent the writing of a 1 in any plane that corresponds to an MB bit that is 0. In the lower W108, the inhibit level is applied only to DP and DS and enables those inputs that receive signals from MB or the parity bit PB. The drive select terminals of the W108 are left floating, so the driver outputs switch between ground and -15V. The inhibit windings are connected to the negative driver output terminals and are grounded at the other end so that current flows through the winding into the driver.

The inputs to the lower W108 that receive the read and write levels from memory control are completely isolated from the other inputs, and their drivers act separately as buffers for the signals. The positive outputs are used, but memory control supplies the input levels at ground, so the output is at -15V when the corresponding function is true (when READ is true the read driver is not selected and its positive output is therefore negative). At turn-on the read and write levels must supply 120 ma to the X and Y W108s, 35 ma to each driver at the ground end of a winding, 25 ma to each at the negative end.

3.7 IN-OUT

The IO logic is shown in block schematic 17. IOT instructions use a special sequence that is shown in the flow chart on the lower left-hand side of drawing 29, but IOT events that occur in the main flow are shown in drawing 30. Print 5 shows the signals on the IO bus, with positive and negative pulses shown by open and closed triangles, and levels of the two polarities are shown similarly by diamonds. The signal naming convention has been changed at this point to provide ease of interpretation when dealing with standard PDP-8 options which are used on the PDP-8/S. The inputs from the information

collector listed at the left go directly to AC. The levels from AC and MB listed in the second and third columns are for data output and device selection. The remaining signals are received or generated by the logic shown in print 17.

In the center of that block schematic are a pair of one-shot delays that generate a separate IO pulse train that is parallel to the bit time pulses. In execute time of an IOT, A00 triggers a PA to set the first one-shot, and 1 μs later its transition back to 0 triggers the second one-shot, which also has a period of 1 μs. The IO pulses are derived from the PA output and the 1 outputs of the delays, but they are microprogrammed. Therefore only those called for by the IOT are actually generated. Thus at the lower left a 1 in instruction bit 11 allows the PA output to trigger IOP1. Just above it a 1 in bit 10 produces IOP2 from the output of the first delay. At the top of the drawing the third pulse IOP4 is generated from the second delay if bit 9 is 1.

The gate below the INS flip-flop decodes the device selection portion of an IOT for the code 00, which selects the program interrupt. When PI is selected, IOP1 sets INS; IOP2 clears both it and ION to turn off the interrupt. Setting INS turns on the interrupt by setting ION at the first pulse in the next fetch time. When the interrupt is on, an interrupt signal over the bus or the occurrence of a parity error (upper left) requests a program interrupt by causing A12 to set PIR. An interrupt is also requested by LPC setting as power is failing (C3). Every A13 clears PIR, but the interrupt signal is a level, so every A12 sets it again until the level goes away. When the break is granted, A00 clears both INS and ION to prevent further interruptions.

The other "devices" contained in the processor are the parity and power failure logic. Both are selected by the code 10 which is decoded by the net at the lower right. When this selection is made, IOP1 causes a skip if there is no parity error. IOP2 skips if there is a power failure (i.e., LPC is 1). The output of the parity and power checking nets are ORed with the skip signal from the bus to produce IOSKP, which is gated by IOT at the far left to produce IOSKS, which in turn sets the skip flip-flop (SKP). If IOP4 is programmed, the IOT also clears PE.

The clear pulse shown at the lower right clears all IO equipment only when the start key is pressed and on power clear. A clear AC signal from the bus (upper left corner) produces CAC, the clear pulse for that register.

3.8 TELETYPE

The circuits and bus connections for the teletype control are shown in drawing PT08-A-1. The teletype is actually two separate devices, one for input, the other for output; and all logic for transmission of information between computer and teletype is contained in two modules, a receiver and a transmitter. Since these are separate devices, there are two device selectors: device code 03 selects the receiver, 04 selects the transmitter. The transmitter and receiver also require separate clocks (upper left-hand side of drawing), both set at about 220 Hz (both have periods between 4.5 and 4.6 ms,

but the transmitter clock runs slightly faster than the receiver clock). The transmitter clock is always on, the receiver clock functions only when enabled from the receiver module.

Data transmission between computer and teletype control is in 8-bit characters sent to or taken from AC04-11. AC11 corresponds to the first character bit and the eighth bit (AC04) is always 1. Between the control and the ASR 33, data transmission is in the form of 11-unit characters that are presented serially at 110 bits per second, so one complete character requires 100 ms. Character transmission always begins with a start impulse (space), followed by the eight data bits in order (with 1s represented by marks), and transmission is terminated by a stop impulse (two marks). An idle line marks continuously.

The logic that is internal to the W706 receiver and W707 transmitter modules is shown only in the circuit schematics, and the conventions used are different from those used in the computer block schematics. Here the voltage levels are high and low, where high is defined as any voltage in the range 0.85 to 3.6V, and low is the range of 0 to 0.4V. Voltage dividers at all module inputs and outputs translate the high and low levels to (and from) the computer ground and negative levels. A D-shaped symbol represents an AND gate in which two low inputs produce a high output; the arrow-shaped gate is an OR in which the output is low if either input is high. A circle at any input or output indicates a transition from high to low whenever the circuit function is satisfied, or flip-flop goes to the given state, etc. A flip-flop is defined as being in the 1 state when its 1 output is low. A transition from high to low at the T-input sets the flip-flop if only S is low, clears it if only C is low, but complements it if both are low. The input at the side of a flip-flop has no circle and sets or clears it (whichever the case may be) on a low to high edge.

3.8.1 Input

For the teletype input logic, refer to the circuit schematic of the W706 receiver. The clock input (on the lower left-hand side of the drawing) is the input shown as RCLO on the block schematic. Proceeding clockwise around the circuit schematic, the input at BV is I/O CLEAR, the clear flag input is IOT032, the reader run output is RRE, the flag output is the interrupt signal, the strobed flag output is the skip signal, and the strobe for reading the flag is IOT031. The bit outputs are IC11-04, with bit 8 at the bottom corresponding to IC04. The read strobe for the input shift register is IOT034, and the clock enable output is RCLE.

The serial input from the teletype is at bottom center of the schematic (this is labeled TSO on the block). Whenever a key is struck or a line is read on paper tape, the distributor begins transmission with a space which changes the input from high to low. This enables the receiver clock and the first RCLO sets ACTIVE, whose 0 side transition from high to low sets all bits in the shift register, clears FLAG DLY, and clears READER RUN so that if input is from the reader only a single frame will be read. The 1 state of ACTIVE holds the enabling level to the clock so it will continue throughout the input cycle.

The first clock also sets the frequency divider flip-flop, so that the second pulse, which is centered in the input unit, clears it (see the flow chart in the center of print 29). The low-to-high transition at its 1 output shifts the contents of the register upward and reads the present input into bit 8. Since each input cycle always begins with a space, bit 8 clears. Then each subsequent pair of clocks sets and clears the frequency divider to read another unit of the character into bit 8 and shift up the data that was previously read. At the time the eighth character bit is being read, the 0 resulting from the initial space is in bit 1, so the shift also sets FLAG to request an interrupt, and sets FLAG DLY Once the FLAG DLY flip-flop is set, the next clock sets IN LAST UNIT, and the succeeding one clears ACTIVE and sets STOP 1. Although ACTIVE is now clear, in LAST UNIT holds on the clock enable so the next clock sets STOP 2 and clears STOP 1. With both stop flip-flops set, the final clock clears them both and clears IN LAST UNIT to disable the clock. The final three clocks are not necessary for reception, but they prevent noise on the line from triggering a new input cycle at least for the first one and a half units of the two-unit stop impulse.

The program can determine the source of the interrupt by using an IOT031 to skip on the flag. An IOT that selects teletype input and has 1s in bits 9 and 10 clears AC at IOP2 and loads the character into AC04-11 at IOP4. The inverter through which IOT032 generates the clear signal for AC is shown at the top left-hand side of the schematic for the W707 transmitter module. The same IOT that clears AC also clears FLAG, and sets READER RUN so that another frame will be read if the reader is on.

3.8.2 Output

For the teletype output logic refer to the circuit schematic for the W707 transmitter. The clock input at the lower left is the TCLO input on the block schematic. Proceeding clockwise around the circuit schematic, the power clear input is I/O CLEAR, the clear flag input is IOT042, and the input at BJ is IOT032 which produces the CLR AC pulse at AP. IOT041 strobes the flag and the strobed output causes a skip; the flag output is the interrupt signal and the output line that drives the print selector magnets is labeled PSM on the clock. The data inputs to the shift register are BAC levels 11-04 the last corresponding to bit 8. The pulse that loads the buffer at the bottom right is IOT044, and it always sets ENABLE because pin BS is grounded.

As shown at the top of the output flow chart on the right-hand side of drawing 29, by selectir device code 04 the program can skip on the flag to determine when the transmitter is free, and IOP2 clears the flag. Loading a character into the shift register sets ENABLE, allowing transmission to begin on the next clock provided that the previous transmission is complete. If the program gives the IOT044 while the stop impulse for the previous character is still on the line, the clock continues to transmit that signal and does not begin the new character until both stop flip-flops are set and FLAG DLY is clear.

When transmission does begin the first TCLO sets ACTIVE, which clears LINE to begin transmission with a space. The next clock (which clears STOP 2) sets the frequency divider, so that the

following clock (which clears STOP 1) clears the frequency divider to shift the first bit of the character into LINE for transmission. The shift also clears ENABLE and moves the rest of the character up one bit. Each pair of clocks then alternately sets and clears the frequency divider and moves another bit into LINE for transmission. After the last character bit is transmitted, the next shift moves the 1 originally in ENABLE into LINE to begin transmission of the stop impulse. All bits of the shift register are then clear, so the next clock clears ACTIVE, sets FLAG DLY, and sets FLAG to request an interrupt.

Subsequent clocks then time out the two marks required for the stop, the next clock clearing FLAG DLY and setting STOP 2, and the final one setting STOP 1. A new character can be loaded into the shift register anytime after FLAG is set. After completion of the stop signal, a 1 in ENABLE causes a new transmission cycle to begin. So long as ENABLE is clear, LINE remains set to continue marking the line.

CHAPTER 4
MAINTENANCE

DEC Field Services supplies an up-to-date list of recommended spare parts for the PDP-8/S. The list includes not only module, semiconductor and miscellaneous spares for the computer, but also spares and necessary tools for the teletype. In addition, it is recommended that the user have the following items to maintain the computer and teletype.

Item	Description
Multimeter	Triplett Model 630-NA; Simpson Model 260
Dual-channel oscilloscope	Tektronix 580 series, preferably with delayed sweep trigger facilities
ASR 33 lubricants	Teletype KS7470 oil, KS7471 grease
Lint-free cloths	Cheese cloth or equivalent
Cotton swabs	Q-tips or equivalent
Cleaning fluids	Dupont Freon TF; denatured alcohol
Test cables and probes	Low-capacity probes for the oscilloscope, alligator clips, etc.
Super Filter Kote (aerosol)	Research Products Corp., Madison, Wisconsin

DEC supplies the following manufacturers manuals for lubrication and adjustment procedures and corrective maintenance for the teletype:

Teletype Bulletin 273B:	Model 33 Automatic Send-Receive Teletypewriter Set (ASR), Vols 1 and 2
Teletype Bulletin 1184B	Parts, Model 33 Automatic Send-Receive Teletypewriter Set (ASR)

4.1 MAINTENANCE PROGRAMS

MAINDEC programs permit self-testing of the PDP-8/S for checkout, preventive maintenance, or diagnosing equipment malfunctions. Each MAINDEC package consists of program tapes and a reference document. All documents have the same format, and an outline of this format, as well as the documents and tapes themselves, are available from the DEC PDP-8/S Program Library. In particular, § 1 of the document is an abstract of the program; § 3, 4 and 5 give complete details for loading, starting, and running the program, § 6 § 10 and 11 contain flow charts and the program listing.

The MAINDECs listed below are applicable to the PDP-8/S processor, memory and teletype. In a number of a tape, PB following the slash indicates a paper tape in binary format, PM indicates a paper tape in readin mode format.

	Document No.	Tape No.
Basic Instruction Test	801-1/D	801-1/PM
Instruction Test 1	8S-D01A/D	8S-D01A/PB
Instruction Test 2	8S-D02A/D	8S-D02A/PB
Instruction Test Part 2B	801-2B/D	801-2B/PB
Basic JMP-JMS Test	8S-D03A/D	8S-D03A/PB
Random JMP Test	8S-D04A/D	8S-D04A/PB
Random JMP-JMS Test	8S-D05A/D	8S-D05A/PB
Random DCA Test	8S-D06A/D	8S-D06A/PB
Random ISZ Test	8S-D07A/D	8S-D07A/PB
Memory Checkerboard (two tapes - low and high)	802/D	802/PM
4K Memory Address Test	8S-D11A/D	
Low		8S-D11A/PB 8S-D11A/PM
High		8S-D11J/PB 8S-D11J/PM
4K Sense Amplifier Test	8S-D15A/D	8S-D15A/PB
Extended Memory Control	820-1/D	820-1/PB(?)
Extended Memory Checkerboard	820-2/D	820-2/PB(?)
Memory Power On/Off Test	829/D	829/PB
Teletype Reader Test	810/D	810/PM
Teletype Reader Exerciser	810A/D	810A/PM
Teletype Punch Test	812/D	812/PM
Teleprinter Test	814/D	814/PM

4.2 MEMORY ALIGNMENT

The memory is a very simple coincident current system with only two adjustments. The master current adjustment is the pot on the A702 reference supply. The strobe adjustment is through the R401 located in 1E22 (8K) or 1F36 (4K). Adjusting the clock affects both the width and position of the strobe simultaneously. Note that it also affects total memory cycle time as well as the read, write and inhibit times.

The memory is aligned during the heat test in checkout. Unless the clock and reference supply pots are jarred severely in transit, they should be aligned properly when received. The reference supply voltage is easily measured at the tabs on the handle end of a W108 or G609 (G608 in 4K). This voltage varies with temperature and best tuning is achieved at 130°F, because at this upper spec temperature the shmoo characteristic has a much smaller area. With the machine stabilized at normal room temperature (68°F), the stack operating temperature will be on the order of 73°F.

The temperature compensation thermistor is located on the rear memory stack module. The thermistor on the front module is a spare. Compensation is not linear and causes the tab voltage to move toward zero when the temperature is increased. Nominal voltages are as follows.

Ambient	0°C 32°F	25°C 77°F	54.5C 130°F
Stack			
Ferroxcube	-13.3V	-11.9V	-9.4V
EMI	-13.1V	-11.6V	-9.0V

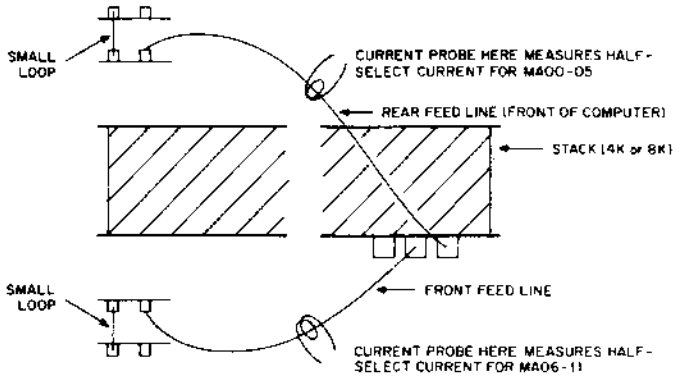
The best place to measure memory timing is the MEMGO signal at 1D36N. The negative level found here represents the memory cycle time, which is nominally 6.3 μs for a Ferroxcube stack, 6.5 μs for an EMI stack*. The value may vary from stack to stack by about 100 ns as it is set by averaging the upper and lower failure points while the machine is in heat. At room temperature, the setting may not necessarily be the average of the room temperature upper and lower failure points, but this is proper as the shmoo of either stack expands in area as the temperature drops.

In any case, the 1 output for any bit measured at the output of a W532 sense amp should be 2V peak (4V peak-to-peak).

4.3 MEMORY TROUBLESHOOTING

4.3.1 X-Y Selection

Failure to select a particular block of locations or even single locations in some fixed pattern of blocks in core generally indicates a bad W108 selection driver. By using a current probe, it is very simple to check all selection drivers with a small program loop. First, rearrange the tab wiring on the handle end of the W108s so that the current regulator on the front stack module is driving the front and rear W108 pairs in parallel.

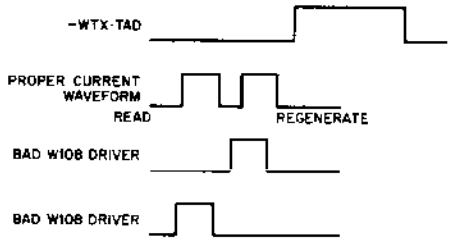


*Room temperature, R401 period coefficient is -0.15% 1°C.

Without using locations 0-7, 10, 20, 30, 40, 50, 60, 70, 100, 200, 300, 400, 500, 600, 700, 1000, 2000, 3000, 4000, 5000, 6000, 7000, put this loop in some area of core that works.

```
        LAS
        DCA .+3
        TAD I .+2
        JMP .-3
0
```

Start the program and place the current probe on the front feed line. Sync scope negative on WTX ·TAD (1A18D) and look at -WTX -TAD (1A18E) with the other scope trace. -WTX ·TAD is a positive waveform. Just prior to its rising edge is a current waveform that represents the address selected by any combination of MA06-11. Run the loop through the 16 combinations, 0-7, 10, 20, 30, 40, 50, 60, 70, on the SR switches. If a driver is failing, a missing current pulse will be observed as shown below.



The W108 can be localized by moving the current probe to the small loop between adjacent waveforms once the bad address combination is found.

Move the current probe to the rear feed line, and repeat the above procedure using addresses on the SR switches of: 100, 200, 300, 400, 500, 600, 700, 1000, 2000, 3000, 4000, 5000, 6000, 7000. This simple procedure checks all drivers in the selection system.

4.3.2 Inhibit Drivers

Place this loop (if runable) in core.

```
        LAS
        DCA .+2
        JMP .-2
```

Set the switch register to all 1s and place a current probe on the feed line from the rear stack module to the first W108 inhibit driver. Sync on WTX ·DCA (1B08R) and observe -WTX ·DCA)1B08S). Turn off

one switch (put a 0 in one bit in the SR word). The current waveform appearing just prior to the negative-going edge of -WTX •DCA is the inhibit current for the bit selected by the switch.

4.3.3 Sense Amplifiers and Slicers

Problems in these circuits generally are accompanied by a parity error indication on the front panel. The first thing to check for is an error that seems to be intermittent and/or is very sensitive to temperature changes.

The following simple loop, which writes the SR switches everywhere in core except where the program resides and allows parity errors to interrupt, is very helpful in tracking a dropout or pickup problem.

Location	Instruction Octal	Instruction Mnemonic	Definition
1	6104	CMP	/Clear PE on parity error /only
2	7200	CLA	
3	5010	JMP 10	
10	6001	ION	/Enable interrupt
11	1022	TAD 22	/Set location counter
12	3023	DCA 23	
13	7604	LAS	/Read pattern from SR
14	3423	DCA I 23	/Store
15	1423	TAD I 23	/Retrieve
16	2023	ISZ 23	/Index counter
17	5013	JMP 13	/Repeat
20	7200	CLA	/Finished, start again
21	5011	JMP 11	
22	0024		
23	0		

The program writes SR in locations 24 through 7777, and reads each location immediately after writing it. A parity error is most likely to occur as a test location is read, i.e., at the TAD in location 15.

Sync scope negative on PE (1E06T). Observe -PE (1E06S). Positive pulses appearing on this train are parity errors. An error occurs on the memory cycle just before the positive-going edge of -PE. Look at -WTX •TAD. The error is occurring here if -PE goes positive approximately 6 μs before the positive-going edge of -WTX •TAD.

A parity error can occur only in data that is read from memory by the processor. By varying the pattern in SR, one may find combinations that increase the frequency of errors. Once the bit has been localized, watch the sense amplifier and slicer behavior just prior to an error. Note that a parasitic oscillation is extremely difficult to observe. Any added capacitance (such as a scope probe) can cure the problem and should be a hint that it is a parasitic.

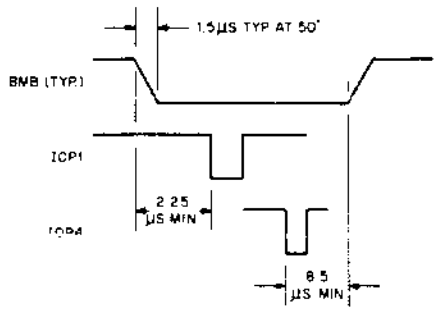
There are two test points on the G803 that are not shown on the logic drawing. These are pin L for inputs J and K and pin S for inputs P and R. The pulse observed here is the slicer action and it shows where slicing begins and ends. Observing the read strobe simultaneously at pin V of any slicer (G803) will aid in adjusting the strobe (memory timing). The strobe should be approximately centered in the slicer test point signal.

4.4 IN-OUT BUS SPECIFICATIONS

The maximum length of the bus including the teletype lines is 50 ft of 92 Ohm coaxial cable. The cables have nine conductors and are fitted with W011 connectors that can be plugged into standard Flip Chip module receptacles. Terminations are required only on the IOP lines, which originate in the computer at B39 pins K, M, and P. A cable terminator (G701) with D664 diodes to ground must be plugged into the spare bus slot in the last device on the bus. The diodes limit overshoot to +0.75V maximum and -0.75V minimum. A G701 terminator is installed in the teletype logic as shipped from DEC. If the teletype is always the last device on the bus, the terminator can be left where it is.

Signals on the bus are as follows.

BMB00-08	Output levels that specify the device address in an IOT. Six pairs of lines represent both 0 and 1 at both 0V and -3V.
Recommended peripheral decoder	W103 with appropriate diodes clipped out
Alternate peripheral decoder	R111 diode gate
Drive available	18 ma maximum at 0V -4.25 ma maximum at -3V
Timing	BMB lines should be used only for strobing by an IOP. They have settled down by BT11 of WTF in the IOT, and they remain static until BT0 of WTE in the IOT. There should thus be no need to worry about slow fall times.
	Typical overshoot on positive-going BMB lines is +2.5V for 200 ns. Overshoots do not affect recommended DEC module types.



BAC00-11

Output levels that supply the contents of AC as data

0V = 1
-3V = 0

Recommended inputs

Level inputs of DCD gates such as in the R203

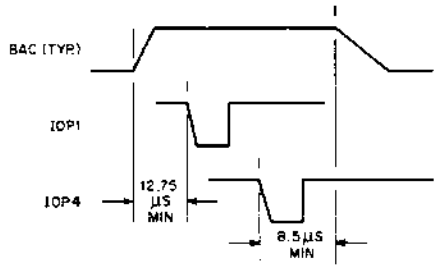
Alternate inputs

R series gates such as R107

Drive available

18 ma maximum at 0V
-8 ma maximum at -3V

Timing



BAC lines can be set up any time prior to an IOT. The shortest time from set up to the earliest IOP is at BT11 of WTE in a TAD. The earliest possible time that BAC lines can change after the latest IOP is at BT12 of WTF in an OPR. Poor fall times on BAC lines need never concern the designer since there is such a large amount of time available prior to the earliest IOP.

Typical overshoot on positive-going BAC lines is +2.5V for 200 ns. Overshoots do not affect recommended DEC module types

IC00-11

Positive input pulses (-3V to ground) that set individual AC bits

Recommended sources

Pulsed outputs, clamped or unclamped, such as R603, R123

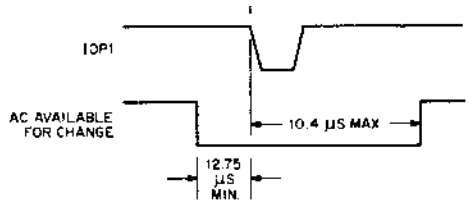
Loading

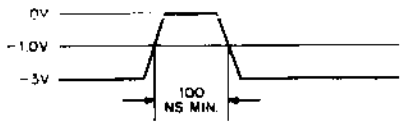
11 ma at 0V in the 8/S
0 ma at -3V in the 8/S

Caution should be exercised when connecting loaded gates to the IC lines as they increase the total drive requirement at 0V.

Timing

Pulses presented to IC lines should originate from an IOP. The maximum time that AC is available for external setting is until the earliest time that AC can be used in the instruction following the IOT. This is BT0 of WTF in an OPR.





The minimum acceptable pulse at the input to the 8/S is as shown here. It is recommended that nominal 400-ns pulses be used at the driving end.

SKIP

Positive input pulse (-3V to ground) that sets the skip control flip-flop from a peripheral device during an IOT.

Recommended sources

Pulsed outputs, clamped or unclamped, such as R603, R123

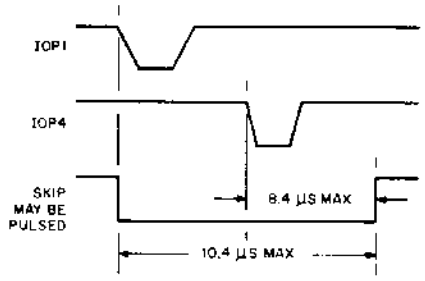
Loading

11 ma at 0V in the 8/S
0 ma at -3V in the 8/S

Caution should be exercised when connecting loaded gates to the skip bus. The total external loading on the bus must not exceed 9 ma.

Timing

Pulses presented to the skip bus should originate from an IOP. The maximum time during which the bus can be pulsed is shown here. The minimum acceptable pulse at the input to the 8/S is the same as shown for IC.



CLEAR AC

Positive input pulse (-3V to ground) that clears AC prior to pulsing the IC lines.

Recommendes sources

Pulsed outputs, clamped or unclamped, such as R603, R123

Loading

20 ma at 0V in the 8/S
0 ma at -3V in the 8/S

External loaded gates cannot be connected to the bus.

Timing

Pulses presented to the clear AC bus should originate from an IOP. The maximum time during which the bus can be pulsed is the same as shown for the skip bus. The minimum acceptable pulse at the input to the 8/S is the same as shown for IC.

I/O CLEAR

Negative output pulses (ground to -3V) that occur when the start key is pressed and when power is turning off or on. The latter two cases generate a burst of pulses.

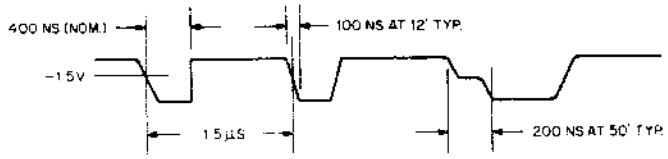
Recommended loads

R107 inverters. If true pulsed lines are required, the PA (R603) pulse input should be driven from an inverter as the rise time of the clear bus pulses cannot be guaranteed less than 60 ns.

Drive available

18 ma maximum at 0V
-1.25 ma maximum at -3V

Timing



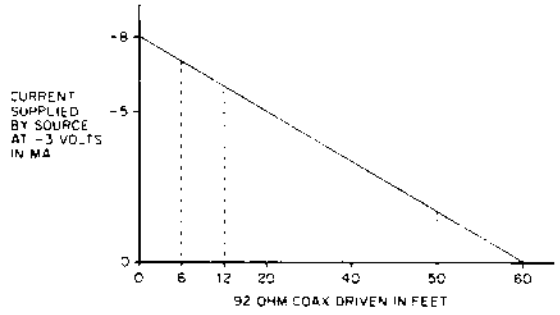
IOP 1, 2, 4

Negative output pulses (ground to -3V) that are the primary source of input-output timing for activating and transferring data to and from peripheral devices.

Recommended loads

W103 pulsed inverter inputs R111, R107, etc.

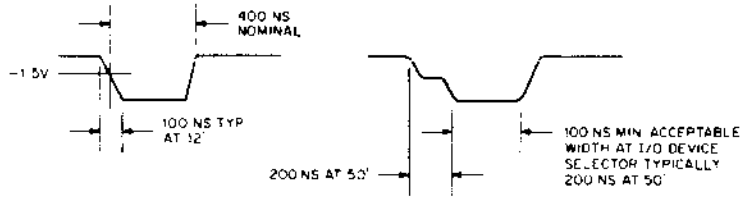
Drive available



72 ma maximum at 0V
-1.25 ma maximum at -3V

The current the IOP lines can supply back into the source at -3V is a function of cable length and a fall time limited to a maximum of 300 ns as shown here.

Timing



INTERRUPT	Level input that causes the computer to interrupt the current program if interrupt synchronization is internally enabled. Bringing the line to ground requests the interrupt; the line is quiescent at -3V.
Recommended inputs	R111, R123, R107, loaded or unloaded
Loading	13 ma at 0V 0 ma at -3V External loads added must not exceed a total of 7 ma.
Timing	The interrupt line is examined at BT12 of WTE in every instruction. The longest possible time the device must wait for an interrupt request to be recognized is 90 μs.

CHAPTER 5
MEMORY EXPANSION AND DATA BREAK OPTIONS

5.1 INTRODUCTION

This chapter contains information required for operation and maintenance of optional equipment for expansion of the PDP-8/S memory and for the data break facility. The options that are covered in this chapter are as follows.

OMD8S	Mounting assembly and control logic for DB8S and MC8S options; interconnections for ME8S options.
MC8S	Memory extension control and additional 4096 word memory
DB8S	Data break facility
ME8S	8192-word memory mounting hardware (accommodates one or two MM8S 4096-word memory modules).

The arrangement of assemblies and interconnecting cables is shown in Figure 5-1.

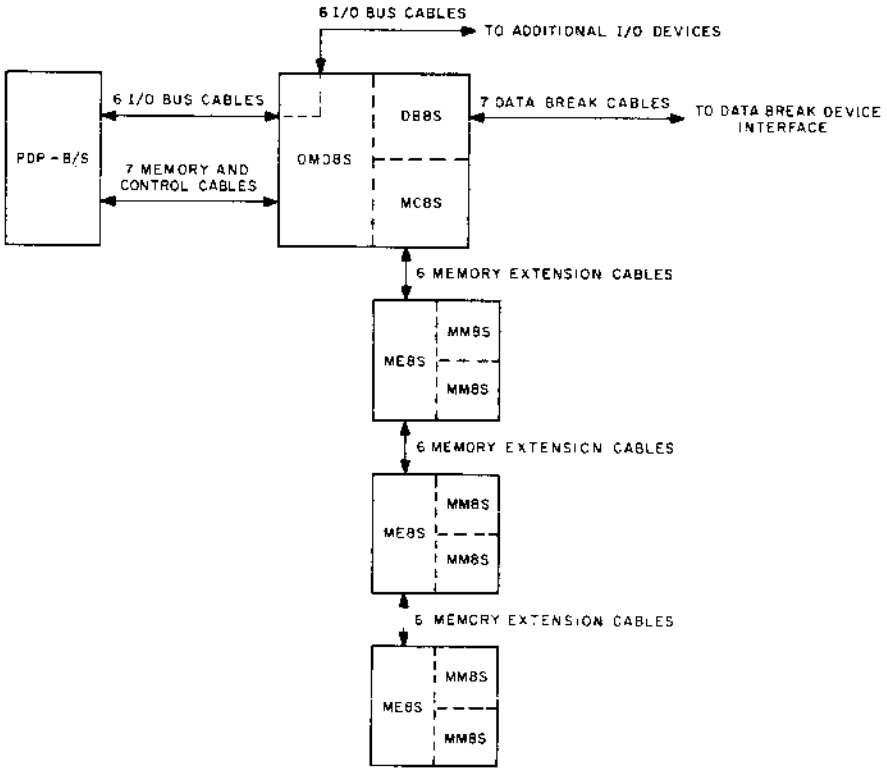


Figure 5-1 Assembly and Cabling Configurations for Memory Expansion and Data Break Options

The OMD8S assembly includes timing control logic and memory bus distribution for the data break option or for memory expansion, or both. In either application, the standard PDP-8S 4096-word memory module (field 0) is removed from its location in the PDP-8/S and installed in the OMD8S assembly. Logic for the MC8S and DB8S options mounts within the OMD8S assembly.

The MC8S provides the first additional 4,096 words of expanded memory (field 1), and includes control and field selection logic that permits expansion of memory up to 32,768 words with ME8S options.

The DB8S Data Break option provides control logic and buffer registers to implement single-cycle or three-cycle data breaks and memory increment data breaks.

ME8S provides rack mounting hardware and interconnections for one or two type MM8S 4096-word memory modules, for memory expansion beyond 8192 words in 4096-word increments. Maximum expansion to 32,768 words requires an OMD8S assembly containing an MC8S and three ME8S assemblies each containing two MM8S memory modules.

5.1.1 Physical Characteristics

This group of options is intended for rack mounting. The OMD8S is a single assembly that occupies 21 vertical inches of a 19-inch rack; it accommodates one DB8S and one MC8S. Mounting dimensions are shown in Figure 5-2. The weights of the OMD8S and its subassemblies are as follows: OMD8S weighs 35 lb; DB8S weighs 2 lb; MC8S weighs 5 lb.

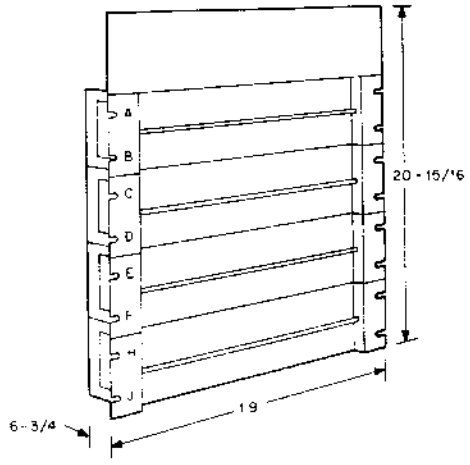


Figure 5-2 OMD8S Assembly Mounting Dimensions

The ME8S option is physically separate from the OMD8S assembly. Dimensions are shown in Figure 5-3. Weight of the ME8S alone is 20 pounds (add 5 pounds for each MM8S memory module).

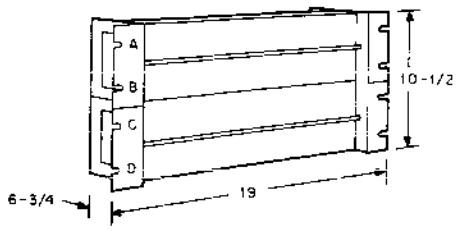


Figure 5-3 ME8S Assembly Mounting Dimensions

Recommended locations for the OMD8S and ME8S assemblies in a rack-mounted installation are shown in Figure 1-5.

Ambient temperature and humidity requirements are the same as the standard PDP-8/S (Chapter 1). Additional forced-air ventilation is not usually required in a typical rack-mounted installation.

5.1.2 Electrical Characteristics

These options obtain dc power from additional DEC Type 728 power supplies. One 728 supplies OMD8S, MC8S, and DB8S. An additional 728 power supply is required for each pair of ME8S units. All dc voltages, logic levels, and pulse characteristics are the same as the standard PDP-8/S.

5.2 SYSTEM OPERATION

5.2.1 Data Flow

Figure 5-4 shows the data flow between the PDP-8/S and the major logic elements of this group of options.

5.2.2 OMD8S Option

The OMD8S option includes modifications to internal PDP-8/S logic for a revised memory timing sequence. Inverters and amplifiers are added for distribution of memory timing, the memory address register output (BMA), and selected processor timing or control signals.

Logic within the OMD8S assembly provides for bussed memory data and address lines (GMA, GMB, SMB) for memory field 0 (removed from the PDP-8/S) and any other memory modules added by MC8S and ME8S options. Data and address bits to and from memory through the DB8S option (when used) are applied to these same bus lines.

The OMD8S assembly provides through-connection of the PDP-8/S I/O bus. (Some of the I/O bus signals are used by the MC8S option.) Connections are also provided for the memory address, data, and control bus lines for plug-in addition of ME8S expansion options. The MC8S and DB8S options, when used, mount directly in the OMD8S assembly and connect to the bus lines by direct internal wiring.

5.2.3 MC8S Option

The MC8S option adds a 4096-word memory module (field 1) and provides the field selection controls required to address memory beyond 4096 words. Three additional memory address bits beyond the 12 bits of the MA register are required to address memory up to 32,768 words.

Field selection bits for instruction words are stored by a 3-bit IF register; field selection bits for deferred operands are stored by a 3-bit DF register. The field selection bits are applied from the appropriate register (according to whether instructions or operands are being fetched) to a decoder which distributes a field selection signal to one of the 4096-word memory modules in the system. Each 4096-word module is considered a field. Field 0 is the original PDP-8/S module removed to the OMD8S, field 1 is the module provided with the MC8S option, fields 2 through 7 are added by ME8S options. The basic memory timing signals (read, write, strobe enable, and inhibit) are applied to all memory modules, but only the module specified by the field selection bits is enabled to operate.

Instruction and data fields must be set up initially by the PDP-8/S console DATA FIELD and INSTR FIELD switches (which are put into operation when the MC8S option is installed) and then kept current by IOT, JMP, or JMS instructions. Two additional registers, SF (save field) and IB (instruction buffer) provide temporary field storage to permit field changes during interrupts or program jumps. Contents of the IF, DF, and SF registers may be read into the accumulator or updated from MB by assigned IOT instructions.

In systems including a DB8S option, the three additional data field bits are provided directly to the field selection decoders by the external equipment during data breaks.

5.2.4 DB8S Option

The DB8S Data Break Facility adds two buffer registers (DBMB and DBMA), a parity generator, and control logic required to stop the normal sequence of instruction fetching and execution and utilize the memory for input or output data transfers. Break cycles can occur singly, interleaved with

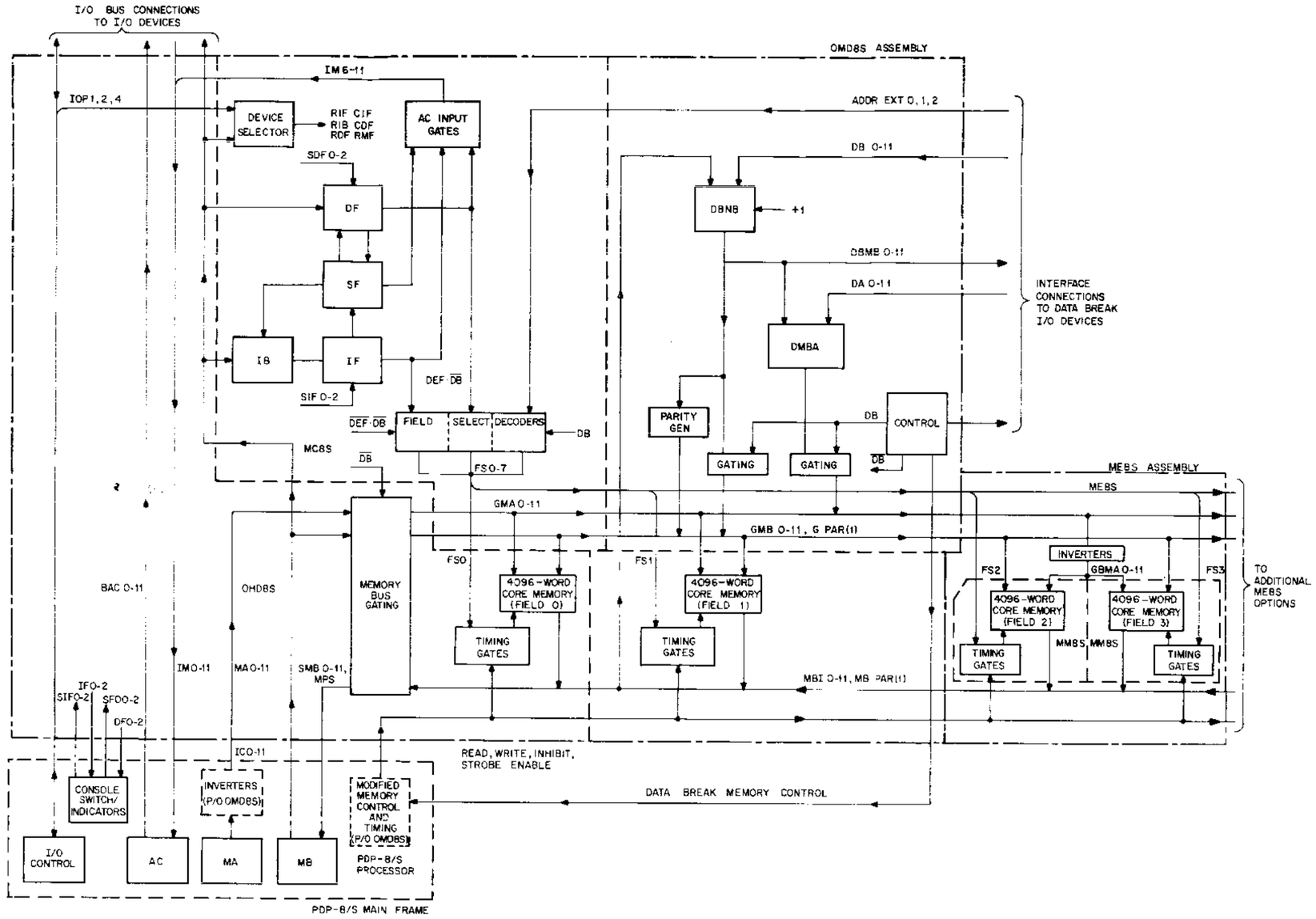


Figure 5-4 OMD8S/MC8S/DB8S/ME8S Data Flow

program steps, or consecutively, for block transfers of large quantities of data. The program counter, instruction register, and MA register are not modified during break cycles; at the conclusion of data break transfers, the normal program resumes.

When a break state is requested, the OMD8S gating disconnects the PDP-8/S MA and MB registers from the memory input, output, and address busses. Addresses and data are obtained instead from the DBMA and DBMB registers of the DB8S option. Two basic types of data break, single-cycle and three-cycle, can be performed by this logic, depending on the facilities of the external equipment. Single-cycle word transfers take 8.0 μs (one memory cycle) and 3-cycle word transfers take 24.0 μs (three memory cycles). An additional 0.5 μs is required for the first and last transfers of a series, and a waiting period of up to 8.0 μs may elapse before the data break suspends normal program operation and starts the first break.

5.2.4.1 Single Cycle Breaks. - In single-cycle data breaks, the external equipment must supply a 12-bit address to the DBMA register and (if memory is expanded) three extended address bits to the MC8S field selection logic. A memory cycle is initiated to transfer data to or from the specified address. For input transfers, the data is entered into buffer register DBMB for transfer to the GMB memory input bus. A parity bit is also generated. For input transfers, memory data from the MBI bus is transferred into DBMB, where it is stored until it can be sampled by the external equipment. Control is then returned to the main program.

Because it requires only one memory cycle per data transfer, the single-cycle break can transfer data as fast as the PDP-8/S memory can operate, for a 125 KHz word rate. The single-cycle break, however, requires the external equipment to supply an updated address for each data transfer from a counting register.

The single-cycle break can also operate in a "memory increment" mode. On request, the DB8S accesses a memory location (specified by an externally supplied address) and adds one to the content of the location.

5.2.4.2 Three-Cycle Breaks. - The three-cycle data break facility eliminates the need for an address register in the device control. The current address and word count are stored instead in core memory locations and are updated automatically after each word transfer. These locations must be in memory field 0. (The data transfer may take place in any memory field, however.) When several devices are connected to this facility, each specifies a different set of core locations for word count and current address, allowing interlaced operation of all devices as long as the combined data rate does not exceed 42 KHz. The three-cycle data break facility performs the following sequence of operations.

a. The device enters a word count address in DBMA. Since this address is always the same for a given device, it can be wired in and does not require a flip-flop register. The word count location must be an even number (DBMA11=0).

b. The content of the word count address is read from memory into DBMB, which included provisions for adding 1 to its least significant stage and propagating the resulting carries. The word count is incremented by DBMB, then restored to the same location. If the word count becomes 0 as a result of the addition, a WC OVERFLOW pulse is transmitted to the device. (To transfer a block of N words, this register is loaded with -N during programmed initialization of the device.) After the block has been fully transferred the WC OVERFLOW pulse signifies completion of the operation.

c. The odd memory location following the word count address (DBMA11 = 1) contains the current address for the ensuing data transfer. This location is read and its contents transferred to both DBMB and DBMA. The incrementing feature of DBMB normally adds one to the current address before it is restored. However, an "increment CA inhibit" signal from the device can prevent this, for operations such as a magnetic tape search cycle. At the end of this second memory cycle the current address is present in DBMA.

In initializing for a block transfer beginning at location A, the current address location is set up by the program to contain A-1.

d. A third memory cycle is initiated, to transfer data to or from the location specified by the content of DBMA. For input transfers, data and a parity bit is entered into DBMB for transfer to the GMB memory input bus. For output transfers, memory data from the MBI bus is transferred to DBMB where it is stored until it can be sampled by the device.

e. In the "memory increment" mode, the content of the current address location is incremented and replaced in memory. No external data transfer takes place.

5.2.5 ME8S Option

The ME8S option provides mounting facilities for one or two 4096-word MM8S memory modules, plus control and timing logic and interconnections. The memory modules are connected to the memory timing, memory address and data bus lines from the OMD8S, and the field selection signals from MC8S. Additional inverters are provided to distribute both polarities of the GMA lines from OMD8S.

Each MM08 memory module consists of a core array, address selection circuits, inhibit selection circuits, sense amplifiers, and memory drivers which are identical with these in the standard PDP-8/S. Only one module at a time is enabled by the MC8S field selection signals.

No distinction is made between memory cycles initiated by the central processor or by the data break option; address lines, data lines, and timing signals operate in the same way regardless of the controlling equipment.

Through plug-in connections are provided on each ME8S assembly for addition of other ME8S units. Up to three ME8S assemblies can be added to a basic PDP-8/S for memory expansion up to 32,768 words.

5.3 OPERATION AND PROGRAMMING

This group of options imposes three changes, as follows, in basic PDP-8/S programming.

a. Memory cycle time increases from approximately 6.3 μs to 8.0 μs, for a small increase in instruction execution time.

b. If memory beyond 4096 words is used, the MC8S field selection logic must be kept current by special assigned IOT instructions.

c. If 3-cycle data breaks are to be permitted, memory locations for word count and current address must be initialized.

5.3.1 Memory Field Selection

Operating and programming information for a PDP-8/S with expanded memory appears in the PDP-8/S Users Handbook which is reproduced in Small Computer Handbook, Doc. No. C-800(1967), published by Digital Equipment Corporation of Maynard, Mass.

5.3.2 Initializing 3-Cycle Data Breaks

To prepare for 3-cycle data breaks, memory locations dedicated to word count and current address must be initialized to desired values. The word count location, WC, is specified by a wired address from the data break device interface. The address must be an even number in field 0. The current address location is WC + 1.

For a transfer of N words, location WC must be present to contain -(N-1). The initial value of current address is at the programmer's convenience. During data break transfers, the current address in location WC + 1 is incremented by the hardware after every word cycle. The memory field to which the 12-bit current address refers is specified by three extended address bits obtained from the device interface.

Normally the current address is incremented during every cycle, but a control line from the device can prevent this.

5.3.3 Indicators, Operating Keys, and Switches

The following indicators and switches are installed on the panel of the standard PDP-8/S, but they are activated only when an MC8S option is installed.

Control or Indicator	Function
DATA FIELD indicators and switches	Indicators display the content of the data field (DF) register. Switches load manual input into DF when LOAD ADDRESS key is pressed. The DF register determines the core memory field for retrieval and storage of data.
INSTR FIELD indicators and switches	Indicators display the content of the instruction field (IF) register. Switches load manual input into DF when LOAD ADDRESS key is pressed. The IF register determines the core memory field from which instructions are to be read.

The DB8S option, installed in the OMD8S assembly, includes a display panel which includes the following indicators:

Indicator	Function
DATA BREAK MB	Display the content of the data break memory buffer (DBMB) register.
PARITY	Indicates the even parity bit generated from the content of the DBMB register.
BRK RQ	Indicates the presence of an external break request. Permits the operator to observe and dismiss a waiting break request before starting the program.

5.4 SYSTEM LOGIC

The following paragraphs contain a detailed description of logic and an analysis of sequential operation for each of the options.

An interconnecting cable diagram and a complete set of logic drawings, flow charts, module utilization charts, and module schematics appears in Appendix C. Drawing numbers, logic symbols and notation, and conventions regarding signal names and logic levels are similar to the standard PDP-8/S drawings in Appendix A.

Flow diagrams are included for the revised memory timing introduced by OMD8S, for the changes in operating sequence and special IOT instructions added by the MC8S, and for the 1- and 3-cycle data breaks. Notation on these flow charts corresponds to that of the main PDP-8/S flow diagram in Appendix A.

A glossary of signal names generated by this group of options appears at the end of Appendix C.

5.5 OMD8S LOGIC

5.5.1 Logic Elements

5.5.1.1 Interconnections and Control Signals. - Control signals from the PDP-8/S processor are supplied to the OMD8S assembly through connector modules. Shown on print D-IC-OMD8S-0-3 are the I/O bus signals, used by the MC8S option and also applied to through connectors for other options. Memory timing signals READ, WRITE, INHIBIT, and STROBE ENABLE are also applied to through connectors for use in ME8S memory expansion assemblies.

Circuits added within the PDP-8/S by module addition or substitution are shown in Print D-BS-OMD8S-0-4. For the most part these circuits provide general purpose timing and control signals used in the MC8S and DB8S options. The control signals are discussed in relation to the functions performed, under the appropriate option description.

Also shown on this print are the drivers which isolate the MA_{0-11} signals from the BMA_{0-11} bus. Logically, MA and BMA are identical.

5.5.1.2 Memory Address Gating (Print D-BS-OMD8S-0-6). - A primary function of the OMD8S logic is to provide bussing systems for memory address, input data, and output data. The bus system includes gating so that either the processor or the data break option can use the memory. It also permits memory expansion by addition of core modules. Memory capacity is expanded easily by connecting all data and control lines to the same busses.

The BMA memory address lines from the processor are gated to the GMA (0) lines as long as the data break facility is not using memory (the DB level is at -3V). The GMA (0) signals, and the GMA (1) signals developed by inverters on the same print, are distributed to memory field 0 in the OMD8S assembly (and also to memory field 1, if a MC8S option is installed). The GMA (0) signals are distributed through connector 1H1 when an ME8S memory expansion option is in the system.

During data breaks, the DB level goes to ground, blocking the BMA gates. The memory address is obtained instead from the DB8S option DBMA lines which are gated to the GMA (0) lines by the DB level on Print D-BS-DB8S-0-5.

5.5.1.3 Memory Read Data Gating (Print D-BS-OMD8S-0-6). - Data from memory, during a read cycle, appears on the MBI bus common to all memory modules and the DB8S option. When a data break is not in effect, DCD gates preceding pulse amplifiers are enabled so that MBI is transmitted to the processor on the SMB_{00-11} lines. During data break memory cycles, the gates are inhibited and the data is instead entered into the data break's DBMB register (Print D-BS-DB8S-0-2).

5.5.1.4 Memory Write Data Gating (Print D-BS-OMD8S-0-7). - Data to all memory modules during write cycles is applied on the GMB bus lines. During processor memory cycles, when the DBB level is at -3V, the processor memory bus output (BMB_{0-11}) is gated to the GMB lines which are distributed internally to memory fields 0 (and 1, if used) and externally through connectors IH5 and IH6 to any ME8S memory extension units. The processor's parity bit, BPAR (1), is gated to the GPAR (1) line, also distributed to all memory modules.

During data breaks, the processor BMB lines are blocked from the GMB bus by the DB level and the DB8S option DBMB lines are gated to the GMB lines. The parity bit, DB PAR (1), is gated to GPAR (1). (See Print D-BS-DB8S-0-5.)

During data breaks, the DBB level is at ground, blocking processor BMB data from the GMB lines. Data from the external device, communicating through the DB8S option, is applied to the GMB (also called DBMB) lines, instead. Connectors IJ7 and IJ8 are used by the external device for this purpose.

5.5.1.5 Memory Control. - Print D-BS-OMD8S-0-4 shows the modified memory control logic that replaces the standard 8K memory control logic shown in Print D-BS-8S-0-22. Basic memory cycle timing is established by a 2 mc clock driving an 8-stage switch-tail ring counter. At power turnon, the MPC level from the power monitor module clears all stages of the counter. A RD RQ or WR RQ pulse enables the clock, which supplies shift pulses to the counter. The MCA(0) and MCH(0) levels keep the clock operating until the counter has shifted through all 16 states and returned to the all-zero condition. During the 8 μs counter cycle, the basic memory timing pulses are generated, as shown in Figure 5-5 and the timing chart at the lower left of Print D-BS-OMD8S-0-4, Sheet 1.

The RD RQ and WR RQ signals may be initiated either through processor memory requests or data break memory requests. The related control logic appears on Print D-BS-OMD8S-0-7.

Processor requests are honored by the P PRQ (permit processor request) pulse, which occurs during A12 provided no break cycles are active. A processor write request (WRS) enables the WR RQ pulse; a read request (RDS) enables a RD RQ pulse.

The RDS or WRS levels also enable the P REQ flip-flop to be set during A12. If a data break is in effect, the P REQ flip-flop stays set, as an indication that the processor requires a memory cycle as soon as the data break releases control. The flip-flop is reset by the WRITE pulse of the first memory cycle data break.

Data break memory cycles are requested by the 1WRRQ, 2WRRQ, 1RDRQ, or 2RDRQ signals. The conditions under which these are generated are discussed in the description of DB8S.

The M DONE pulse occurs every time the clock counter returns to all zeros. Provided that the data break is not active, the P DONE pulse is also generated. P DONE is returned to the processor to restart the main timing chain by resetting the W15 flip-flop. (This is the same function performed by the MEMGO signal in the standard PDP-8/S.)

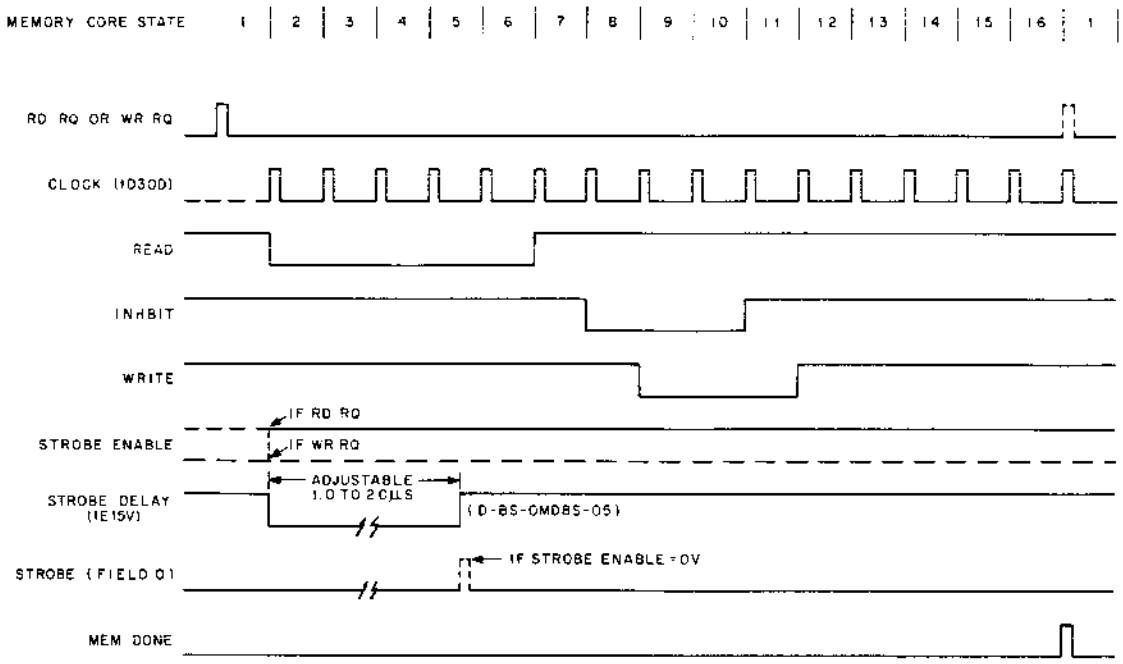


Figure 5-5 OMD8S Memory Timing Diagram

If data break is still in effect, the P DONE pulse is inhibited. The M DONE pulse instead initiates another RD RQ or WR RQ pulse.

5.5.1.6 Field 0 Memory Module. - Field 0 memory logic is shown in Print D-BS-OMD8S-0-5. Operation is essentially identical to the standard PDP-8/S memory module, except for the 8-µs memory cycle introduced by the modified clock system. In addition, the logic shown in the lower left section of the print gates the basic memory timing signals against the FS0 (field select 0) level. If the system contains only the one 4K memory module, FS0 is true at all times. In expanded systems, FS0 is provided by the MC8S option; it is true only when field 0 operation is desired.

5.5.2 OMD8S Sequential Operation

The OMD8S logic has no independent function; it operates with MC8S/ME8S memory expansion, with the DB8S Data Break facility, or both. Sequential functions involving OMD8S logic are discussed under MC8S, DB8S, or ME8S, as applicable.

5.6 MC8S LOGIC

5.6.1 Logic Elements

The MC8S option adds the first additional field of expanded memory (field 1) and includes the registers and control circuits required to assign and update the three additional address bits that address expanded memory systems. Logic is shown in Prints D-BS-MC8S-0-2. Functional elements of the logic are described in the following paragraphs.

5.6.1.1 Field Registers (IF, DF, SF, IB). - This group of registers handles instruction and data field assignments during normal operation, program interrupts, and program jumps. Logic for these registers appears on Print D-BS-MC8S-0-1, Sheet 1. Each of the registers can be loaded from several sources. Figure 5-6 shows the signal sources, the gating levels that select inputs, reset pulses, and the strobe pulses that set selected data into the registers. Timing of the gating, strobe, and reset pulses is discussed in Paragraph 5.6.2.

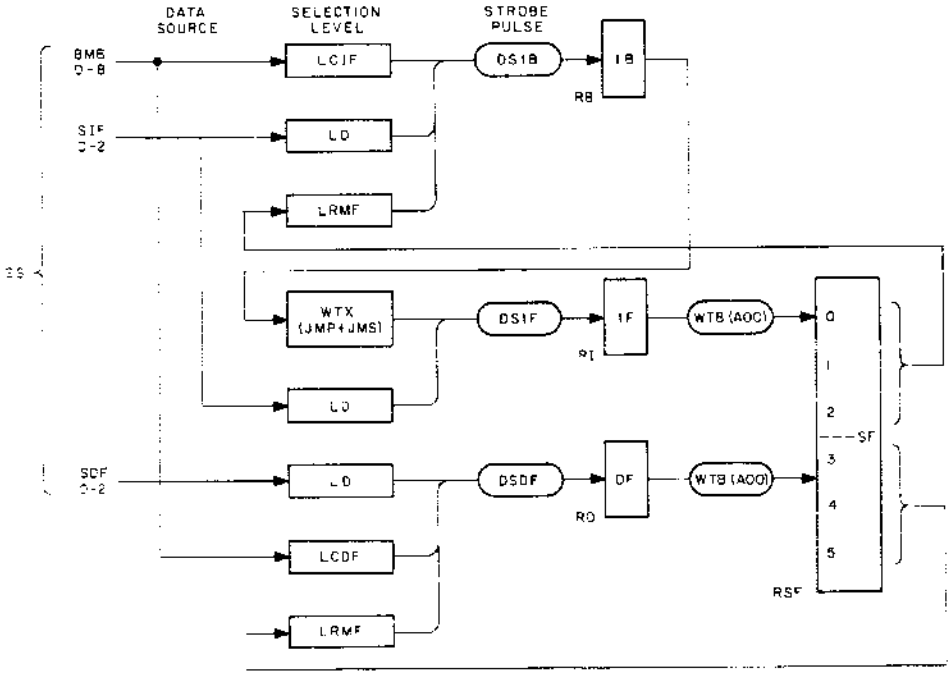


Figure 5-6 MC8S Field Register Data Flow

5.6.1.2 Device Selector. - The IOT instructions which operate the MC8S extension control logic are decoded by a type R111 NAND gate on Print D-BS-MC8S-0-1, Sheet 3. This gate and the R002 diode gate connected to it, decode BMB bits 3 through 5 for the octal combination X2XX and the IOT instruction level to produce a control level called S CDF. This control level, equivalent to 62XX on the BMB bus, is used as the conditioning level for all extended memory control instructions. It is further combined with BMB11 to produce CDF and LCDF signals, with BMB 10 to produce LCIF signals, and with BMB 6-8 to produce RDF, RIB and RIF signals as shown on Sheet 2 of Print D-BS-MC8S-0-1.

5.6.1.3 Field Decoders and Field Select Signals. - The field decoders consist of three type R151 Binary-to-Octal Decoder modules that accept complementary pairs of input levels from the IF, DF, and data break address extension signals, respectively. The enable inputs of the three decoders are driven by networks which determine whether a deferred operand is being fetched or a non-deferred operand is being fetched. In the case of deferred operands, the DF register is enabled; in the case of non-deferred operands, the IF register decoder is enabled. During the break state, the DB8S address extension decoder is enabled. Note that field 0 decoding is forced if the data break is active and the DB8S is not in the BRK (data transfer) state. During the 3-cycle break WC and CA memory cycles, field 0 is required.

Since the MC8S houses both fields 0 and 1 of the memory, field select signals for fields 2 through 7 are generated via R107 buffers connected to the outputs of the field register decoders and distributed through connector slot 1H4. These levels are used only in the ME8S memory extension modules.

5.6.1.4 Interrupt Inhibit. - Interrupts must be prevented between the time a change of instruction field is issued and the time a jump to the new field of memory occurs is accomplished. Logic to accomplish this is added to the 8S processor, as shown in Print D-B-OMD8S-0-4. The inhibit flip-flop, called FR, is initially cleared by a start pulse or power clear pulse (SP + PCP) and is set whenever a change instruction field (CIF) IOT is issued. The resulting positive level at the "0" terminal of the FR flip-flop (-FR) is used to inhibit the NAND gate which sets the PIR flip-flop in the 8S on I/O Print D-BS-8S-0-17. The FR flip-flop is reset as soon as the first JMP or JMS instruction is issued; an interrupt request which arrived during the inhibit time is then recognized.

5.6.1.5 Accumulator Transfer Gating. - The reading of the contents of the SF, IF, and DF registers into the processor via the I/O channel is done by the R123 NAND gates located on Sheet 2 of Print D-BS-MC8S-0-1. During IOP 4 of the appropriate IOT instruction, the contents of one of the three registers is gated onto the input bus to the 8S accumulator.

5.6.1.6 Memory Field 1. - Memory field 1 and its associated electronics are shown on Print D-BS-MC8S-0-2, and it is considered part of the basic MC8S option. The standard memory control signals (READ, WRITE, etc.) are gated against the field select 1 signal (SF1), as shown at the lower left of Print D-BS-MC8S-0-2.

5.6.2 MC8S Sequential Operation

Differences in standard processor operation introduced by the MC8S option are in the DCA, ISZ JMP, and JMS instructions, and in the six IOT instructions assigned to the IF, DF, and SF registers. In addition, word time B is modified in order to set IF and DF into the SF register during interrupts.

Manual operations for these options involve the setting of the content of the DATA FIELD and INSTR FIELD switches into the IF, IB, and DF registers during a load address cycle, and clearing of IF, DF, and IB during a power-on cycle or START switch operation.

The MC8S flow diagram (Print D-FD-MC8S-0-4) shows the logical conditions under which the various strobe and gating pulses are generated.

5.6.2.1 Power On. - The -PPC level generated by the processor power monitor module enables a gate on D-BS-OMD8S-0-4, Sheet 2, to produce the -CLR pulse. The -CLR pulse forces the RI, RD, and RB pulses (Print D-BS-MC8S-0-1, Sheet 1) which reset the IF, DF, and IB registers, respectively. The -CLR pulse also resets the DEF flip-flop on Print D-BS-MC8S-0-1, Sheet 3.

The (SP + PCP) level (initiated by -PPC) resets the FR flip-flop on Print D-BS-OMD8S-0-4, Sheet 1, and also triggers the -RSF pulse (D-BS-OMD8S-0-4, Sheet 2) which resets the SF register.

5.6.2.2 Start Key. - The start key also initiates the (SP + PCP) signal which resets the SF register and the FR flip-flop as described above.

5.6.2.3 Load Address. - When the LOAD ADD key is pressed, the processor LP pulse forces a -CLR pulse, which causes the IF, DF, and IB registers and the DEF flip-flop to be reset as described in Paragraph 5.6.2.1.

After a fixed delay, the processor -LPA pulse sets the LD and RUN flip-flops. The processor then enters LD word time to load the new address from the manual switches into the PC. The LD level

enables a series of input gates on Print D-BS-MC8S-0-1, Sheet 1, that select the DATA FIELD and INSTR FIELD switches as the input sources for the DF, IF, and IB registers.

For the IF register, the LD level gates ones from the INSTR FIELD switches (SIF0 through SIF2) to the level inputs of DCD gates. The DSIF pulse, which occurs during A00 of LD word time, sets ones present at the DCD gates into the register.

Similar gating is used at the input to the DF register. The DATA FIELD switches (SDF0 through 2) are gated to the DCD level inputs by LD; DSDF strobes ones into the register.

For the IB register, LD gates INSTR FIELD switch levels SIF0 through 2 to the input gates; DSIB strobes ones into the register.

The DSIF, DSDF, and DSIB pulses are all forced at the same time by the LID pulse, which occurs during A00 of LD word time (Print MC8S-0-1, Sheet 3).

5.6.2.4 JMP, JMS Instructions. - WTF word time is normal through A13, when the IF register is reset by RI (Print D-BS-CS8S-0-1, Sheet 1).

During A00 of WTX, for both instructions, the content of the IB register (previously loaded by a CIF or RMF instruction) is transferred to the IF register. The WTX (JMP + JMS) level applies ones from the IB register to the level inputs of the DCD gates at the input of the IF register. The DSIF pulse, timed by A00, transfers the ones into the IF register.

At the same time, the FR flip-flop is reset (Print D-BS-OMD8S-0-4, Sheet 1) to permit program interrupts.

The remainder of the execution of these instructions is the same as the normal 8/S instruction flow.

5.6.2.5 Field Register IOT Instructions. - The six special IOT instructions assigned to updating or reading the content of the various field registers are implemented like normal IOT instructions except for certain special functions during WTF and WTX.

a. RIB

WTF for the RIB instruction is like any IOT.

During WTX, the content of the DF register is applied to IM_{6-8} for transfer to the processor AC. This occurs during the RDF pulse, generated during IOP4 when the IOT 623X instruction is detected by the logic on Print D-BS-MC8S-0-1, Sheet 2. Actually, the logic detects only code XX1X on the BMB bus. The SCDF level (Sheet 3 of Print D-BS-MC8S-0-1) represents IOT X2XX, by definition 62XX. The logical result at gate 1J13 (Sheet 1 of Print D-BS-MC8S-0-1) is IOT 621X. Since an IOP4 pulse will not occur unless bits 10 through 12 of IR contain 4_8, the last octal digit need not be decoded.

The remainder of WTX and WTE is the same as any IOT instruction.

b. RIF

WTF for the RIF instruction is like any IOT.

During WTX, the content of the IF register is applied to IM6 through IM8 for transfer to the processor AC. This occurs during the RIF pulse, generated during IOP4 when the IOT 6224 instruction is detected by the logic on Print D-BS-MC8S-0-1. The decoding technique is similar to that of RIB, described above in detail.

c. CIF

WTF for the CIF instruction is normal through A12; the IB register is then reset by RB (Print D-BS-MC8S-0-1, Sheet 1). The RB pulse is enabled during WTF by the LCIF level, shown in Print D-BS-MC8S-0-1, Sheet 3. LCIF indicates that a CIF instruction (IOT 62X2) is present.

During WTX, bits 6 through 8 of the CIF instruction, present on BMB6 through BMB8, are transferred to the IB register. (Since the register was reset during WTF, only ones are transferred.) The LCIF level gates BMB6 through BMB8 to the level inputs of the IB register DCD gates; the DSIB pulse sets ones into the register. DSIB is enabled by the LCIF level and triggered by the IOP2 pulse.

Also during IOP2 of the CIF execution cycle, the FR flip-flop on Print D-BS-OMD8A-0-4, Sheet 1 is set. (See paragraph 5.6.1.4.)

d. CDF

WTF for the CDF instruction is normal through A12. The DF register is then reset by RD (Print D-BS-MC8S-0-1, Sheet 1). The RD pulse is enabled during WTF by the LCDF level, shown in Print D-BS-MC8S-0-1, Sheet 3. LCDF indicates that a CDF instruction (IOT 62X1) is present. It enables the WTF (LCDF + LRMF) level that enables generation of RD during A12 of WTF.

During WTX, bits 6 through 8 of the CDF instruction, present on BMB6 through BMB8, are transferred to the DF register. (Since the register is reset during WTF, only ones are transferred.) The LCDF level gates BMB6 through BMB8 to the level inputs of the DF register DCD gates; the DSDF pulse sets ones into the register. DSDF is triggered by the CDF pulse generated on Sheet 3 of Print D-BS-MC8-0-1, by gating LCDF and the IOP pulse.

e. RMF

WTF for the RMF instruction is normal through A12, when the DF register is reset by RD (Print D-BS-OMD8S-0-1, Sheet 1). The RD pulse is enabled by the WTF (LCD + LRMF) level just as in the CDF instruction.

During WTX, SF_{3-5} are transferred to the DF register, and SF_{0-2} are transferred to the IB register. When IOT 6244 is detected by the decoder on Print D-BS-MC8S-0-1, Sheet 2, the LRMF level is produced. LRMF gates SF_{0-2} to the IB register DCD gate inputs, and also gates SF_{3-5} to the DF register DCD gates SF_{3-5} to the DF register DCD gate inputs.

The DSDF pulse, transfers ones into the DF register, and the DSIB pulse transfers ones into IB register. DSDF is triggered by RMF, which is in turn triggered by the IOP4 pulse when an IOT 624X instruction is present (Print D-BS-MC8S-0-1, Sheet 2). DSIB is triggered by IOP4 when the LRMF level is present.

5.6.2.6 DCA, ISZ Instructions and DEF Flip-Flop. - The DEF flip-flop (Print D-BS-MC8S-0-1, Sheet 3) keeps track of deferred operand fetches. It is set during A00 of every WTD cycle to enable the field-selection decoder driven by the DF register contents.

The DEF flip-flop is normally reset at the end (A13) of the WTD cycle. However, it is left set after the WTD cycle of a DCA or ISZ instruction so that the DF register can specify the memory field during the WTX cycle, when the modified AC or MB contents are being restored in memory.

The DEF flip-flop is reset at the end of a DCA or ISZ instruction's WTE cycle. The DEF flip-flop is also reset by the CLR pulse which occurs during a load-address cycle, a power-on sequence, or during A00 of WTB (at the start of a program interrupt sequence).

5.6.2.7 Program Interrupts and FR Flip-Flop. - When an interrupt is recognized at the end of WTE, the 8/S processor stores the current program count in location 0000 of field 0, and proceeds to an interrupt subroutine at the address specified in location 0001 of field 0. With extended memory, it may also be necessary to store the current instruction and data fields in addition to the program count.

During A13 of every WTE cycle, if the PIR flip-flop is set, WTB is initiated. The SF register is cleared at the same time by -RSF (Print D-BS-OMD8S-0-4, Sheet 2).

During A00 of WTB, the IF and DF registers are transferred to the SF register (Print D-BS-MC8S-0-1, Sheet 1). IF and DF are then reset, as is the IB register. This assures that, during the following memory cycle, the PC content will be written into location 0000 of memory field 0. Reset signals RI, RD, and RB are all triggered by the -CLR pulse generated during A00 of WTB (Print D-BS-OMD8S-0-4, Sheet 2).

Ordinarily, location 0001 of field 0 contains a JMP to the interrupt subroutine entry point, which must also be in field 0. If the instruction subroutine itself is not in field 0, it is necessary to initialize IB by a CIF instruction. A subsequent JMP or JMS instruction automatically transfers the new field from IB to IF.

During an interrupt, the instruction and data fields of the interrupted routine are held in the SF register. They can be restored at the end of the interrupting subroutine by an RMF instruction. If multilevel interrupts are permitted, there must be software provisions for storing the SF register content at each interrupt level.

It is important to prevent interrupts during a change of instruction field. Typically, the new field is set up by a CIF instruction, followed by a JMP (or JMS) that transfers the new field from IB to IF. Sometimes, a few instructions may be inserted between the CIF and the JMP. If an interrupt occurs after the CIF but before the JMP, the program will return to field 0 instead of the field that was active when the interrupt occurred. (IB is reset during WTB, wiping out the field set up by the CIF instruction that preceded the interrupt. When the JMP of the interrupted program is reached, IF is set to field 0.)

For this reason, the FR flip-flop is set during a CIF instruction. (See Print D-BS-OMD8S-0-4, Sheet 1.) It remains set, preventing interrupts, until WTX of the JMP or JMS instruction that sets up a new field and then it is reset.

5.7 DB8S LOGIC

The DB8S data break facility allows one I/O device to transfer information directly into or out of the PDP-8/S core memory. The data break is particularly well-suited for devices which transfer large amounts of information in block form.

Peripheral I/O equipment operating at high speeds can transfer information with the computer through the data break facility more efficiently than through programmed means. The combined maximum transfer rate of the data break facility is over 1.5 million bits per second.

Data breaks are of two basic types: 1-cycle and 3-cycle. In a 1-cycle data break, registers in the device (or device interface) specify the core memory address of each transfer and count the number of transfers to determine the end of data blocks. In the 3-cycle data break, two computer core memory locations perform these functions, simplifying the device interface by omitting two hardware registers.

5.7.1 Logic Elements

Control logic to start the required memory cycles and arrange for data transfers is shown on Print D-BS-DB8S-0-1 (2 sheets). The DBMA and DBMB registers appear on Print D-BS-DB8S-0-2.

5.7.1.1 Memory Request Logic. - Data break control over memory cycle requests is performed by the logic on the left half of Print D-BS-DB8S-0-1, Sheet 1. The 1RDRQ or 1WRRQ signals initiate the first memory request of a data break and also initiate a processor request waiting at the end of a data break period. Both signals occur at the end of a 0.5 μs delay. The 2RDRQ and 2WRRQ signals are generated without delays to enable consecutive memory requests during 3-cycle breaks or 1-cycle block transfers.

5.7.1.2 Parity Generator. - On the right half of Print D-BS-DB8S-0-1, Sheet 1, a group of type B130 3-bit parity circuits monitors the content of the DBMB register at all times and generates an even

parity bit, DB PAR (1). The parity bit is ORed to the memory bus MB PAR (1) line and is written into memory along with each data break data word.

5.7.1.3 Data Break Major State Register. - Four flip-flops on Print D-BS-DB8S-0-1, Sheet 2, control the operating sequence for 1- and 3-cycle breaks. The BRK SYC flip-flop is set and reset at the beginning of every break cycle, including consecutive breaks. For 1-cycle breaks, the BRK flip-flop is set during the first available data break memory cycle, during which the data transfer takes place. For 3-cycle breaks, the WC, CA and BRK flip-flops are set in sequence during three memory cycles. The first cycle, WC, fetches and increments the word count. The second cycle, CA, fetches and (optionally) increments the current data address. Then a BRK cycle performs the data transfer in the appropriate direction. Output levels from these flip-flops condition the control logic to enable the appropriate timing pulses.

5.7.1.4 DBMA Register. - The DBMA register on Print D-BS-DB8S-0-2 is a 12-stage flip-flop register with two sets of inputs. The external address on lines DA_{0-11} is set into the register at the beginning of every break cycle. (The register is first reset by 0 → DBMA; then ones on the DA lines are gated in by DATA ADDRESS → DBMA.) A binary 1 is represented by ground on the DA line.

DBMA also holds the current address during the BRK portion of a 3-cycle break. The current address is jam transferred in at the end of the CA cycle by DBMB ⟶ DBMA.

5.7.1.5 DBMB Register. - DBMB on Print D-BS-DB8S-0-2 is also a 12-stage register with two sets of parallel inputs. During input transfers, it stores external data to be written into memory. The data on the DB_{0-11} lines is jam-transferred in by the DATA ⟶ DBMB pulse. The register also stores memory output data until it can be sampled by the device, and holds the current address until it is transferred to DBMA during 3-cycle breaks. In both cases, the register is reset by 0 → DBMB, then ones on the MBI memory bus are transferred in during memory strobe time. (Binary ones on the MBI bus occur as positive-going pulses.)

DBMB includes ripple carry-propagation logic that operates when the word count and current address are being incremented, or during a single-cycle memory increment break. When any stage changes from 1 to 0, it complements the next higher stage. The +1 → DBMB pulse is injected into DBMB11 to start the process.

The most significant stage, DBMB0, is monitored by logic on Print D-BS-DB8S-0-1, Sheet 1. When stage 0 changes from 1 to 0 during the 3-cycle break's WC period, indicating that the word count has changed from -1 to 0, the WORD COUNT OVERFLOW pulse is generated.

5.7.1.6 Control and Timing Logic. - Control and timing signals appear on Print D-BS-DB8S-0-1, Sheets 1 and 2. Conditions under which the signals are generated are discussed in the following paragraphs.

5.7.2 Standby Condition

The DB8S logic is initialized by the MPC pulse generated by the processor power monitor module. MPC resets the P REQ flip-flop, the data break major state register (BRK SYC, WC, CA, BRK), the WCOF flip-flop, and the DBMA register.

The processor operates in the normal manner as long as no break request is received from the external equipment. When a break request is received, the OMD8S memory gating logic is conditioned so that the processor controls the address, data, and timing bus lines to all memory modules. The DB8S logic then assumes control of memory timing and conditions the memory gating logic in OMD8S to block the processor from the GMA, GMB, and MBI memory bus lines. The DB8S register handles memory addresses and data for the duration of the break cycle. Events during 1- and 3-cycle breaks are discussed in following paragraphs.

5.7.3 Sequential Operation, 1-Cycle Breaks

For 1-cycle breaks, the CYCLE SELECT input line must be held at -3V. Internal timing for this mode of operation is shown in Print D-TD-DB8S-0-3. The left-hand portion of the flow diagram on Print D-FD-DB8S-0-6 shows the logical conditions under which the various strobe and gating pulses are generated.

5.7.3.1 Synchronizing. - The BREAK REQUEST signal from external equipment primes a DCD gate at the input of BRK SYC flip-flop, provided the WC and CA flip-flops are both zero. The break facility can interrupt the processor at either of two times: at the beginning of A11 (before the processor has a chance to demand a memory cycle) or during the WRITE pulse (just before the end of a processor-controlled memory cycle). When either condition is present, the BRK SYC flip-flop is set and the BT1 pulse is generated.

5.7.3.2 BRK State. - The BRK SYC (1) level enables a DCD gate at the input of the BRK flip-flop, provided the 1 CYCLE SELECT line from the external equipment is negative. The BRK flip-flop is set when the DCD gate is pulsed by either the M DONE pulse or A12 (depending on whether BRK SYC was set by the WRITE pulse or A11). The BRK (1) level produces the DB level (Print D-BS-OMD8S-0-1, Sheet 2) which conditions the OMD8S gating for data break utilization of memory modules by blocking the GMA, GMB, and SMB bus lines from the processor.

At the same time (M DONE or A12) a 0.5 μs delay is triggered, after which either the 1RDRQ pulse or the 1WRRQ pulse is generated, according to whether the transfer direction is in or out. One of these pulses triggers logic on Print D-BS-OMD8S-0-7 to produce either the WRRQ or RDRQ pulse. These in turn start the memory clock sequence (Print D-BS-OMD8S-0-4, Sheet 1) described in Paragraph 5.5.1.5.

During the break, the processor clock runs and instruction execution proceeds normally up to the time the processor requires a memory cycle. At A12 time, the processor clock stops and the WTS flip-flop is set. The waiting RDS or WRS signal also enables A12 to set the PREQ flip-flop (Print D-BS-OMD8S-0-7). (As soon as the data break facility is finished with the memory, a memory cycle will be initiated to take care of the waiting request.)

The standard memory signals (READ, WRITE, MEM DONE) are used as timing signals for the transfer of data and addresses between the data break facility and the external equipment. At the start of the memory cycle (BT2A time) the DATA ADDR → DBMA pulse is produced to strobe the DA_{0-11} address lines from the external equipment into the DBMA register. (DBMA will have been cleared by "0 → DBMA" during either an MPC pulse or a preceding memory WRITE pulse.) The DATA ADDR → DBMA pulse also triggers the ADDRESS ACCEPTED pulse to the external equipment. The DBMA register, gated to the GMA memory address lines on Print D-BS-DB8S-0-5, is made available to all fields of memory. If memory is expanded, the external equipment must supply the ADDR EXT 0, 1, and 2 lines to the break-state field selection decoder on Print D-BS-MC8S-0-1, Sheet 2. The BRK (1) level enables this decoder (IF15) and the DB level disables the decoders supplied by the data field and instruction field registers.

The leading edge of the READ pulse triggers 0 → DBMB, which clears the DBMB register.

If the transfer direction is in, the trailing edge of the READ pulse triggers the DATA —J→ DBMB pulse, which sets external data ones into the DBMB register.

If the transfer direction is out, data from the READ portion of the memory cycle, appearing on the MBI memory bus, at strobe time, enters the DBMB register. Ones on the MBI bus set corresponding stages of the register. Memory timing is such that the data is available in the DBMB register about 2.5 μs after the BT2A pulse. If the INCREMENT MB line is at ground during the end of the READ pulse, the +1 → DBMB pulse increments the content of the DBMB register.

During the WRITE portion of the memory cycle, the content of DBMB is restored to memory. The parity generator develops the MB PAR (1) parity bit from the contents of the DBMB register. The parity bit is written into memory along with the data word.

5.7.3.3 End of Break. - At the end of the memory cycle, the M DONE pulse resets the BRK flip-flop. The BRK signal to the external equipment returns to ground.

If the BREAK REQUEST line is still at ground and the processor has not yet stopped for a memory cycle (setting PREQ), the normal instruction execution sequence proceeds.

5.7.3.4 Consecutive Breaks. - If the BREAK REQUEST line stays high for consecutive break cycles, the BRK SYC flip-flop is set again at the end of the BRK time read pulse. Another memory cycle is enabled by the 2RDRQ level (output) or the 2WRWQ level (input). (The corresponding RDRQ or WRRQ pulse is triggered on Print D-BS-OMD8S-0-7 by the BRK cycle's M DONE pulse.) The full BRK cycle is repeated. Consecutive breaks occur in this manner so long as the BREAK REQUEST line is at ground at the end of WRITE time. The external device must supply an updated address at the beginning of each BRK cycle.

5.7.3.5 Delayed Processor Requests. - When -3V on the BREAK REQUEST line indicates that no more breaks are required, control is released to the processor. However, if the PREQ flip-flop is set, the BRK cycle M DONE pulse triggers another 1RDRQ or 1WRRQ pulse, depending on the transfer direction. (the processor RDS enables 1RDRQ, while WRS enables 1WRRQ at this time.) The ensuing memory cycle is used by the processor to complete a memory cycle that was postponed during the data break period. Processor access to the GMA, GMB, and MBI lines is permitted by a false DB level.

The M DONE pulse of this memory cycle triggers a P DONE pulse (Print D-BS-OMD8S-0-7). This resets the processor's WTS flip-flop and starts the clock to resume normal operation.

5.7.3.6 Memory Increment. - During the BRK cycle of either 1- or 3-cycle breaks, with output direction specified and the MEMORY INCREMENT line at ground, the +1 → DBMB pulse increments the content of the DBMB before it is restored to memory. This feature permits a memory location to serve as a counting register without program intervention. A hard-wired address must be provided on the DA_{0-11} lines. For 3-cycle breaks, the current address can be assigned by the program.

5.7.4 Sequential Operation, 3-Cycle Breaks

Internal timing for the 3-cycle break is shown in Print D-TD-DB8S-0-3. For this mode of operation, the CYCLE SELECT line must be at ground. The right-hand portion of the flow diagram (Print D-FD-DB8S-0-6) shows logical conditions for the various strobe and gating signals.

5.7.4.1 Synchronizing. - The start of a 3-cycle break is similar to the 1-cycle break. The BRK SYC flip-flop is set by either A11 time or the trailing edge of a processor memory cycle WRITE pulse. At the following A12 (or M DONE) time, BRK SYC is reset and the WC flip-flop is set, starting the word-count cycle. The processor continues normal operation until a memory cycle is required; then, at A12 time, the PREQ flip-flop is set (Print D-BS-OMD8S-0-7), and the WTS flip-flop is set, stopping the clock.

5.7.4.2 Word Count Cycle. - At the same time that the WC flip-flop is set (A12 or M DONE time), 1RDRQ is generated to start the memory cycle that will fetch the word count for the active device. The device must supply the address of the word count location on the DA_{0-11} lines. (For a single channel, the address may be hard-wired.) The DATA ADDRESS → DBMA pulse sets ones of the address into the DBMA register. (DBMA has been reset by a power clear (MPC) or by 0 → DBMA at the end of the preceding break cycle.) Decoder 1F13 (Print D-BS-MC8S-0-1, Sheet 2) forces the FS0 (field select 0) level, as the word count is assumed to be in memory field 0. Also, the DB level blocks the processor from the OMD8S GMA, GMB, and MBI memory bus lines and connects the DBMA and DBMB registers instead.

The DBMB register is cleared by 0 → DBMB, which occurs at the leading edge of the memory READ pulse. Ones from the addressed word count location enter the register during the memory strobe time.

The current address, in DBMB, is incremented by +1 → DBMB, triggered by the memory READ pulse trailing edge. If a carry is propagated out of DBMB0 (1 changes to 0), the WORD COUNT OVERFLOW pulse is delivered to the device interface, signifying the completion of a block transfer. The WCOF flip-flop is set and reset at this time, bracketing the carry propagation. WORD COUNT OVERFLOW can be generated only while WCOF is set. (It is not generated during an "increment MB" break.)

During the write half of the WC memory cycle, the DBMB register content is restored to memory.

5.7.4.3 Current Address Cycle. - Throughout WC, the 2RDRQ level is held at ground. When the M DONE pulse terminates WC, it also triggers a RDRQ pulse (Print D-BS-OMD8S-0-7), initiating another memory read cycle. M DONE also triggers a +1 → DBMA pulse, which sets bit 11 of the DBMA register. The WC address, always an even number, is still in the DBMA register. Setting DBMA, bit 11 produces WC +1 as the location from which the current address will be obtained. The purpose of the CA cycle is to read this location to obtain the current address for the data transfer. During this memory cycle DBMA (gated to the GMA lines of the OMD8S logic) provides the address. Again, memory field 0 is forced by gate 1F13 (Print D-BS-OMD8S-0-1, Sheet 2).

As in the WC cycle, 0 → DBMB clears the DBMB register and memory data ones are set into DBMB during strobe time. Ordinarily, the current address is incremented by +1 → DBMB, at the end of read time. However, the external equipment may inhibit this by holding the INCREMENT CA line at ground.

During the write portion end of the CA cycle the current address, held in the DBMB register, is restored to memory. At the end of memory WRITE time, the DBMB —J→ DBMA pulse transfers the current address to the DBMA register. (The jam transfer does not require that the DBMA register be reset.)

Since the following BRK cycle will involve a data transfer to or from the external equipment, either a memory read or write cycle will be required. The external equipment must specify the direction of transfer by controlling the TRANS DIR line, negative for "in," ground for "out." Either 2RDRQ or 2WRRQ comes on during CA time, according to the state of the TRANS DIR signal. During the CA time M DONE pulse, either RD RQ or WR RQ (Print D-BS-OMD8S-0-7) initiates the next memory cycle.

5.7.4.4 BRK Cycle. - The memory cycle initiated at the end of CA time addresses the location specified by the content of the DBMA register. In systems with expanded memory, the three ADDR EXT bits must be provided by the external equipment to select the data field. Decoder 1F15 (Print D-BS-MC8S-0-1) is enabled during data breaks so that the ADDR EXT bits are decoded to provide the field selection level.

The data transfer takes place as in a single-cycle break BRK cycle. The DBMB register is cleared. Then for output transfers, the content of the addressed memory location is loaded into DBMB, from which it can be sampled by the external equipment. For input transfers, external data on the DB_{0-11} lines is loaded into DBMB by DATA —J→ DBMB. In either case, the content of DBMB is written into memory at the end of the cycle. The parity generator develops the MB PAR (1) bit to be written into memory along with the data word.

5.7.4.5 End of 3-Cycle Break. - At the end of the BRK time memory cycle, the M DONE pulse resets the BRK flip-flop, provided the BREAK REQUEST line has returned to -3V. The B BRK signal to the external equipment returns to ground. Full control of memory is returned to the processor.

5.7.4.6 Consecutive 3-Cycle Breaks. - If the BREAK REQUEST line stays high, for consecutive break cycles, the BRK SYC flip-flop is set again at the end of the BRK time read pulse. The 2RDRQ level is also produced to enable another word count read cycle. The M DONE pulse then sets the WC flip-flop and triggers RDRQ to start the word count memory cycle. The WC, CA and BRK cycles are repeated. Consecutive breaks occur in this manner as long as the BREAK REQUEST line is at ground at the end of WRITE time.

5.7.4.7 Delayed Processor Requests. - If the PREQ flip-flop is set by the processor during a 3-cycle break, the data break logic develops either 1RDRQ or 1WRRQ at the end of BRK time. The M DONE pulse triggers RDRQ or WRRQ (Print D-BS-OMD8S-0-7), accordingly.

5.8 MEMORY EXTENSION BEYOND 8K WORDS (ME8S and MM8S)

The MC8S memory control logic, housed in the OMD8S option mounting panel, includes the basic 4K of memory removed from the 8S processor (field 0) and an additional 4K of memory which constitutes field one. Fields 2 through 7 are added to the system in pairs through the use of the ME8S memory extension panel. Each ME8S houses an even field and an odd field of memory, interconnected to the memory control and data bus lines as shown in Figure 5-7. Interconnection from a set of connectors located in the OMD8S are bussed to duplicate connectors in the ME8S panel, for through-connection of other ME8S options. The control signal in these bus lines emanate from the OMD8S master memory timing logic. The basic timing signals (read, write, inhibit, and strobe) are sent to all fields of memory whether they are housed in the OMD8S or ME8S. Along with these signals are sent the field select signals generated by the MC8S option. The field select levels are gated locally in each ME8S to produce directed control signals for the field of memory which has been addressed. The GBMA bus carries memory addresses from either the processor or the DB8S data break logic. Similarly, the GMB lines carry data from either the processor MB or from the data break DB MB register. The slice amplifiers of each memory bank drive the BMI and MB PAR(1) busses which return to the OMD8S and are distributed either to the processor or to the data break.

5.8.1 ME8S Logic

Besides providing mounting and interconnections for MM8S memory modules, the ME8S contains inverters which distribute the address lines to the two memory modules. (See Print D-BS-ME8S-0-1.) The GMA lines from the OMD8S are supplied in one polarity only (binary 1 is represented by ground), and the memory address decoders require both polarities. The inverters provide the BGMA (0) and BGMA (1) lines to the memory modules.

ME8S also contains the delay circuits that provide directed strobe delay pulses to the two modules.

5.8.2 MM8S Logic

Each MM8S option includes one 4096-word memory module plus gating to direct the bussed memory timing pulses to the module. All memory modules are, in effect, tied to common address, input data, and output data busses. However, the memory timing pulses are directed by the field selection signals from MC8S so that only one module actually goes through a read-write cycle.

Logic of an even memory field module appears in Print D-BS-MM8S-A-1, and directed timing gates are shown in Print D-BS-MM8S-A-2. The FS EVEN enabling level is hard-wired to the appropriate field select level from MC8S/OMD8S.

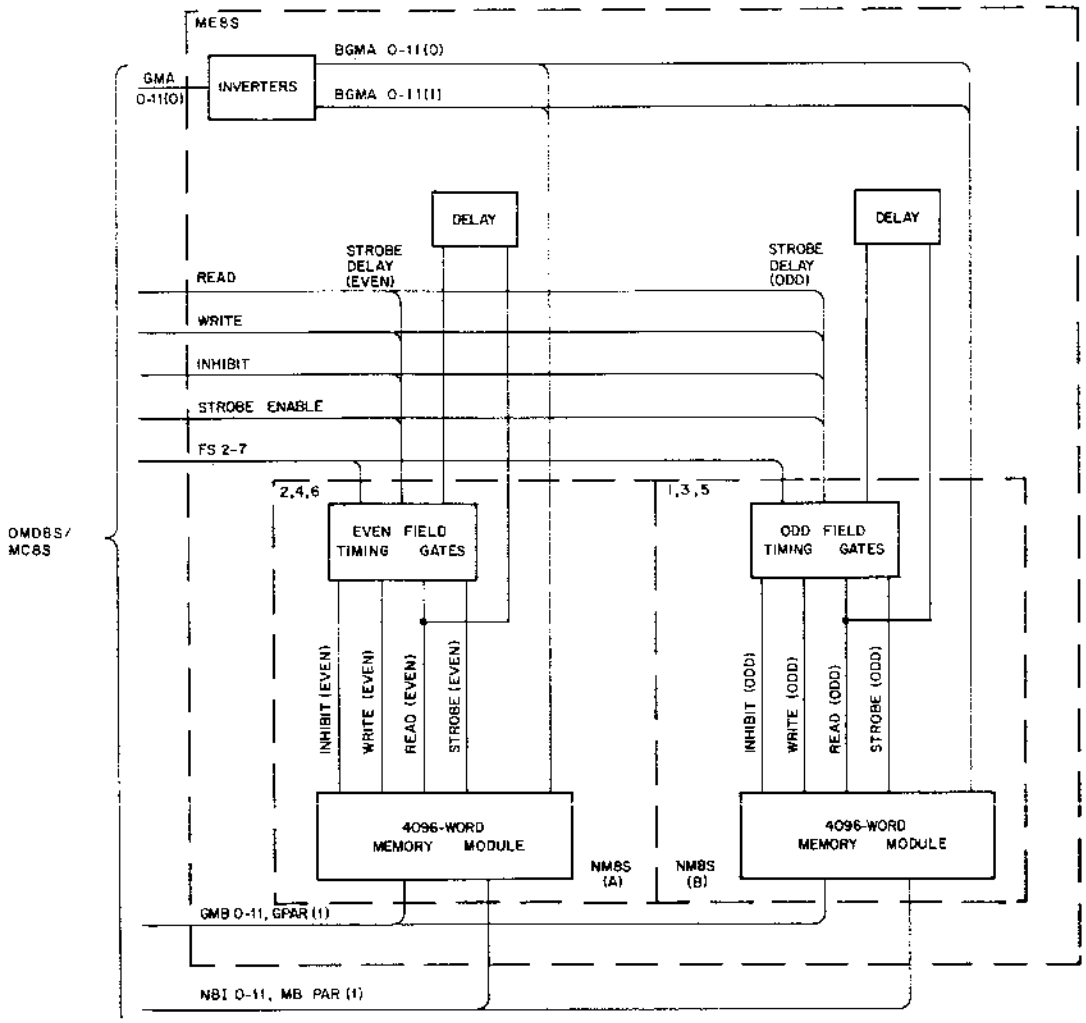


Figure 5-7 ME8S/MM8S Memory Control and Data Distribution

Memory module wiring and timing gates for odd memory fields are shown in Prints D-BS-MM8S-B-1 and D-BS-MM8S-B-2.

5.9 MAINTENANCE

5.9.1 Spare Parts and Test Equipment

DEC Field Services provide an up-to-date list of spare parts for these options. No test equipment or tools other than those listed in Chapter 4 are required.

5.9.2 Maintenance Programs

The maintenance programs listed in Chapter 4 apply to a PDP-8/S with expanded memory as well. Particularly applicable are the Extended Memory Control and Extended Memory Checkerboard tests.

The factory diagnostic program for detailed checkout and debugging of a data break installation requires a logic test fixture that simulates an active data break device. The factory test fixture is not available for use in the field. For field checkout, operate the computer and data break with the associated device, in a simple (and if possible repetitive) operational program. Data flow through the data break logic can be traced with the aid of the timing diagrams provided in this section.

5.9.3 Memory Alignment and Troubleshooting

Since the memory modules used in expanded memory systems are identical to the basic 8K module, the alignment and troubleshooting hints of Chapter 4 apply, except that the memory clock period is increased from 6.5 to 8.0 μs.

5.9.4 Interfacing External Equipment of DB8S Facility

Data and control signals exchanged between the data break facility and associated external equipment are shown in Figure 5-8. External connections are made through W021 cable connector modules. Cables are not supplied. Coaxial 92-ohm cables up to 50 ft long may be used. The following text and timing diagrams define data break operations in terms of the interconnecting signals.

5.9.4.1 Single Cycle Data Breaks. - Single-cycle breaks are used for input data transfers to the computer, output data transfers from the computer, and memory increment data breaks. None of the active processor registers are affected by a data break transfer, and processing continues uninterrupted until a processor memory cycle is required. In case of ties between break requests and processor requests, the break request always wins. Memory increment is a special output data break in which the content of a memory address is read, incremented by 1, and rewritten at the same address.

5.9.4.2 Single-Cycle Input Transfers. - Figure 5-9 illustrates timing of a single-cycle transfer. The address to be affected in core is normally provided by the device interface from a 12-bit flip-flop register (data break address register) which has been preset by programmed transfer from the computer. Typical external registers and control flip-flops supplying information and control signals to the data break facility are shown in Figure 5-10. The input buffer register (IB in Figure 5-10) holds the 12-bit data word to be written into the computer core memory location specified by the address contained in the address register (AR in Figure 5-10). Output terminals of these registers are connected to the DB8S

logic connectors so that ground potential represents binary 1's. A parity bit is generated for all input transfers by the DB8S. Since most devices that transfer data through the data break facility are designed to use either 1-cycle or 3-cycle breaks, but not both, the CYCLE SELECT signal can usually be supplied from a stable source (such as a ground connection or a -3V clamped load resistor) rather than from a bistable device as shown in Figure 5-11. Other portions of the device interface, not shown in Figure 5-11, establish the data word in the input buffer register, set the address into the address register, set the direction flip-flop to indicate an input data transfer, and control the break request flip-flop. These operations can be performed simultaneously or sequentially, but all transients should occur before the data break request is made. Note that the device interface need supply only static levels to the computer, minimizing the synchronizing logic circuits necessary in the device interface.

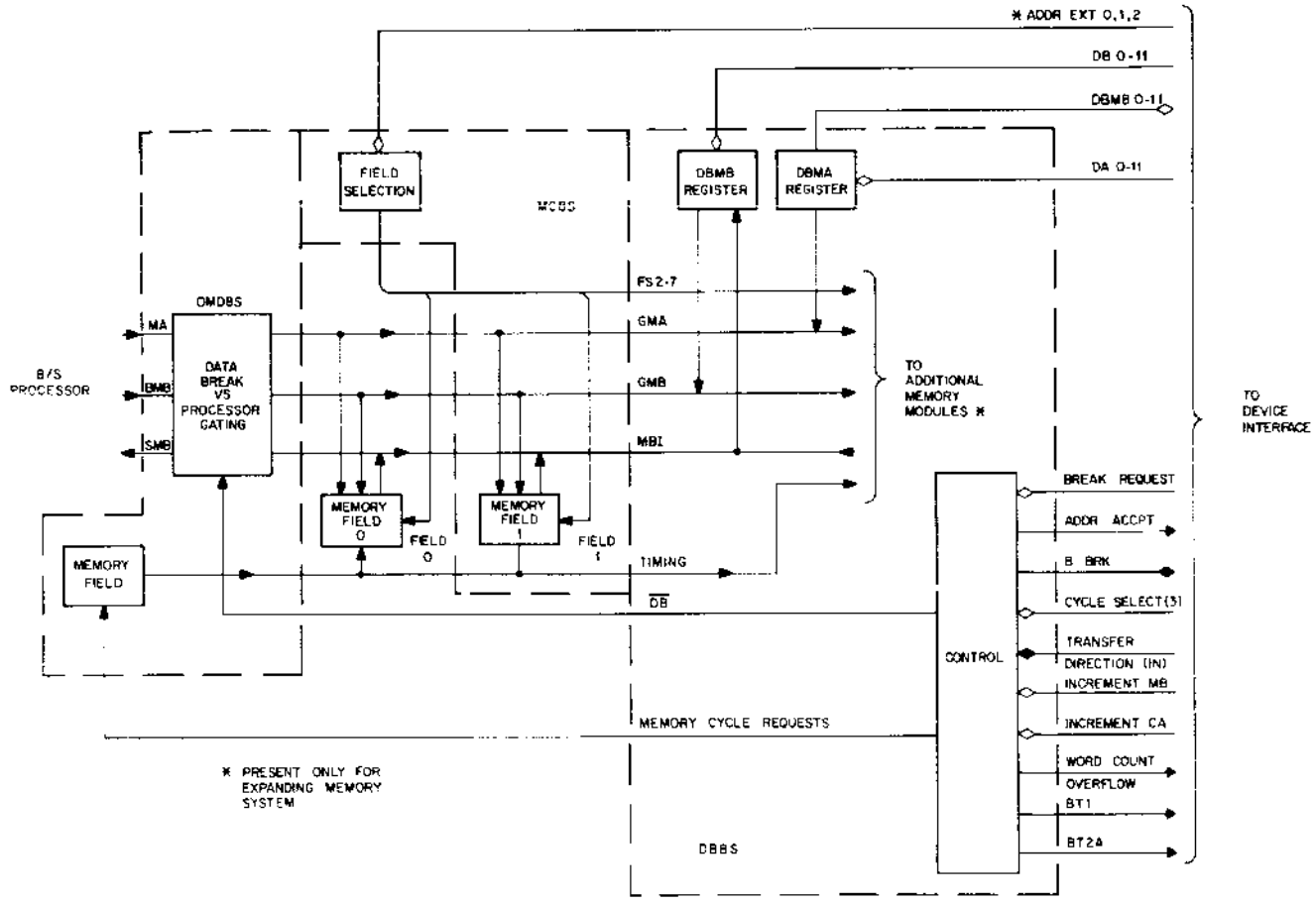


Figure 5-8 DB8S Interface Connections

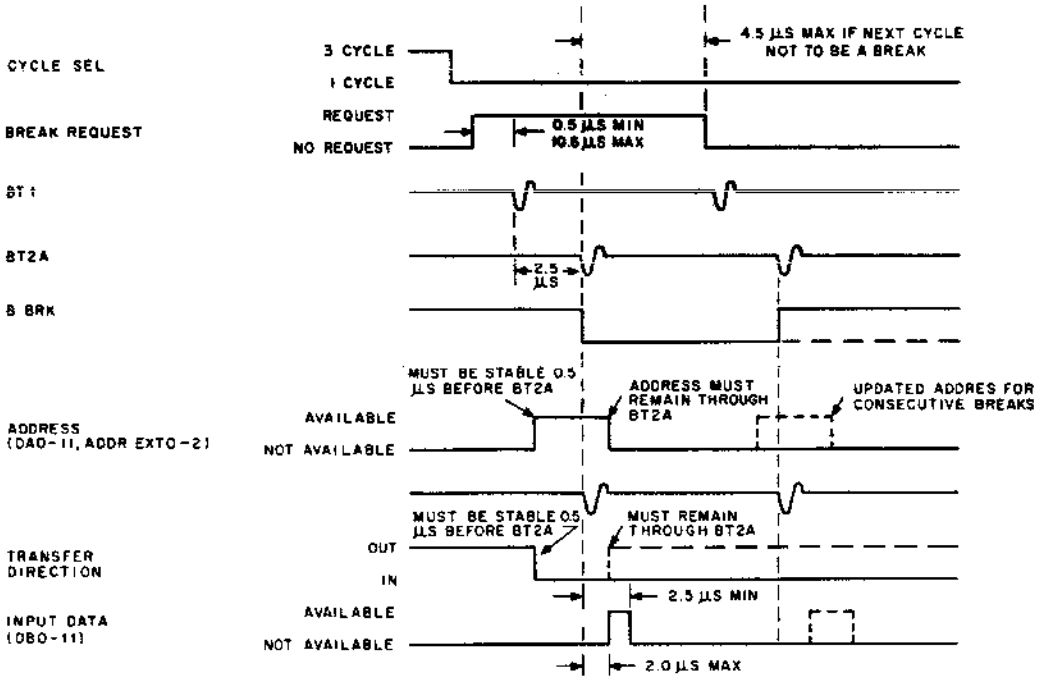


Figure 5-9 Interface Timing, Single Cycle Breaks, Input

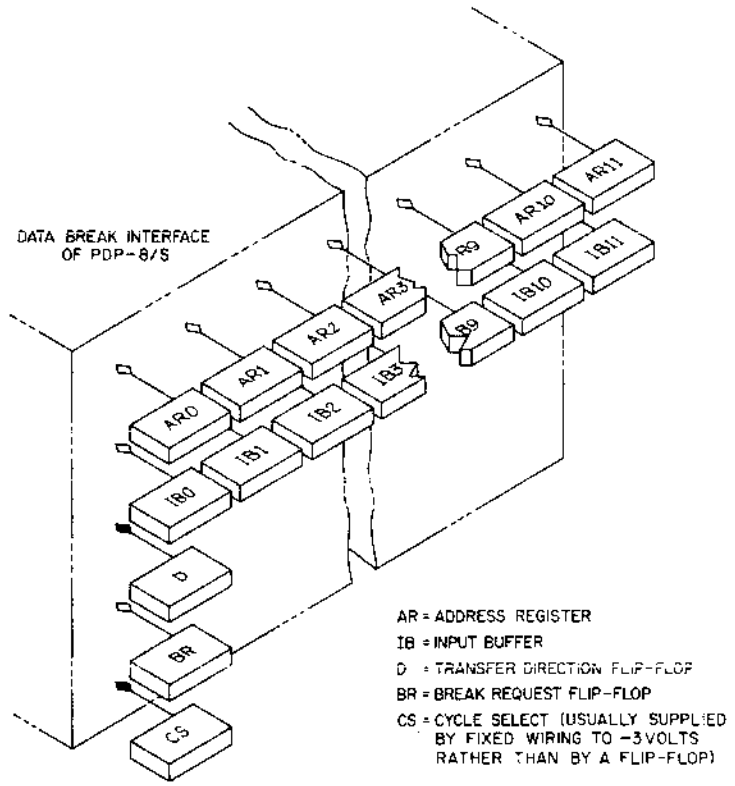


Figure 5-10 Device Interface Logic for Single-Cycle Input Transfer

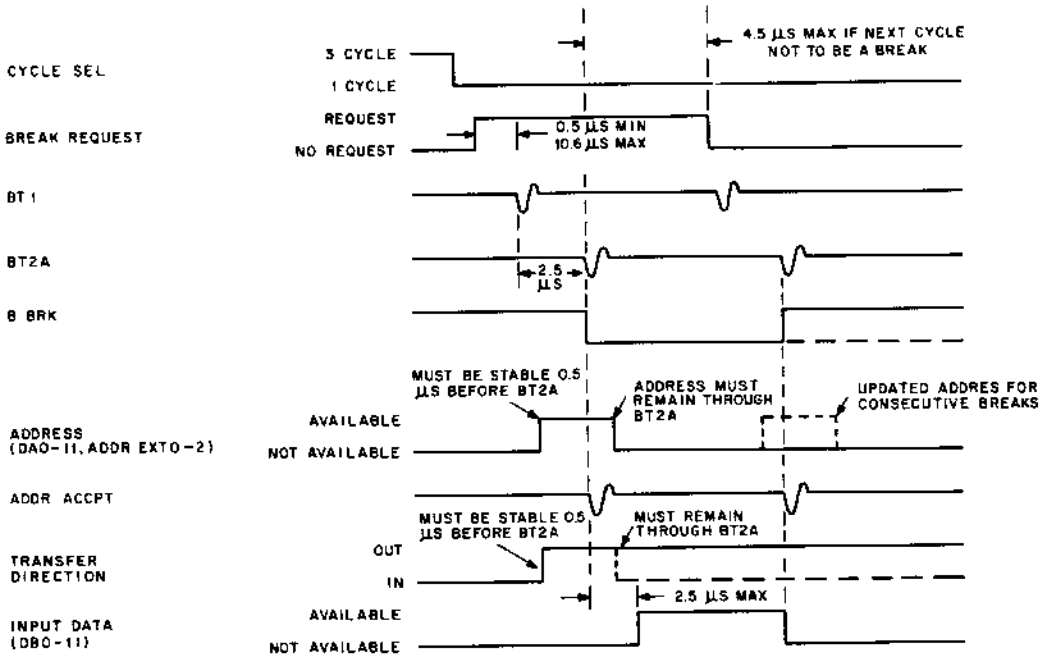


Figure 5-11 Interface Timing, Single-Cycle Breaks, Output

Data break requests are sampled by BTI. (The maximum delay before a break request is sampled is 10.6 µs.) Within 3.0 µs after BTI an ADDR ACCPT (address accepted) pulse is generated to acknowledge receipt of the request, and the break state is entered. The supplied address must be sustained until the address accepted pulse. The address-accepted pulse can be used in the device interface to clear the break request flip-flop, increment the contents of the address register, etc. A 0.5 µs delay allows control of the memory to switch from processor to data break before a memory request is generated. There is also a 0.5 µs delay at completion of the break state to allow control of the memory to return from the data break to the processor. Due to these 0.5 µs delays, the total time for an individual break is 9.0µs. If the break request is present at every BTI time, successive breaks will occur every 8 µs (125 KHz). (The 0.5 µs delay only occurs at the beginning of the first break and at the end of the last break.)

5.9.4.3 Single Cycle Output Data Transfers. - Timing of operations occurring in a 1-cycle output data break is shown in Figure 5-11. Basic logic circuits for a typical device interface used in this type of transfer are shown in Figure 5-12. Address and control signals are similar to those discussed previously for input data transfers, except that the TRANSFER DIRECTION signal must be at ground potential.

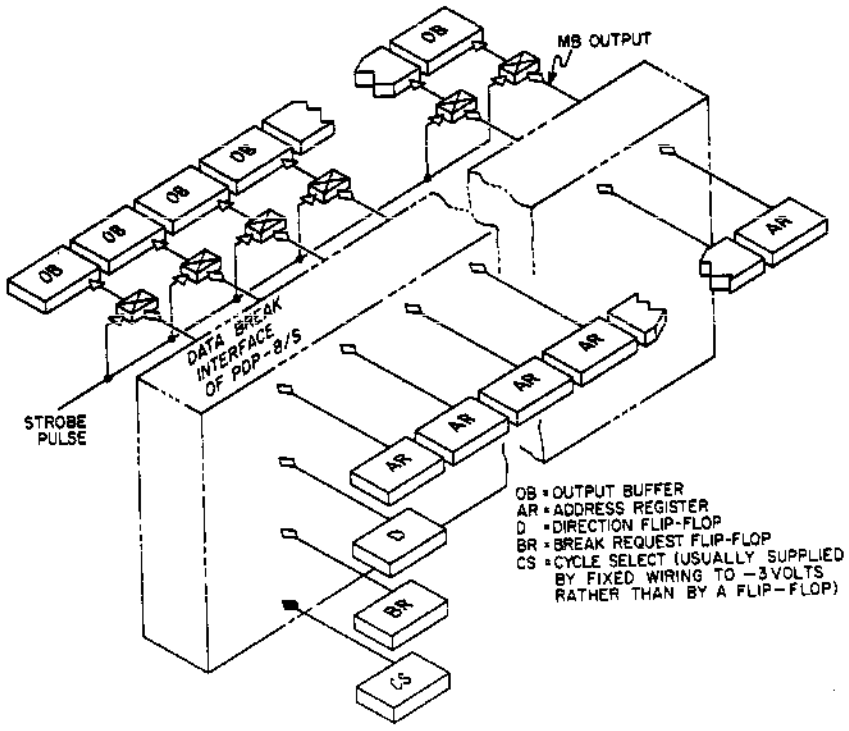


Figure 5-12 Device Interface Logic for Single-Cycle Output Transfer

An output data register (OB in Figure 5-12) is usually required in the device interface to receive the computer information. The device, not the DB8S, controls strobing of data into this register. The device must supply strobe pulses for all data transfers out of the computer (programmed or data break) since circuit configurations and timing characteristics differ in each device.

When the address and data break request are supplied, an ADDR ACCPT pulse is generated as in input data break transfers. At BT2A time, the address supplied to the PDP-8/S is loaded into DBMA, the break state is entered, and the MB is cleared. Not more than 2.5 μs after BT2A, the content of the device-specified core memory address is read and available in DBMB. (This word is automatically rewritten at the same address during the last half of the break cycle and is available for programmed operations when the data break is finished.) Data bit signals (DB_{0-11}) are available as static levels of ground potential for binary 1's and -3V for binary 0's. The DBMB is cleared at BT2A (+1.5 μs) of each break cycle, so the data word is available in the DBMB for approximately 5.5 μs to be strobed by the device interface. The data for the last transfer is available in DBMB until the next break.

Generation of the strobe pulse by the device interface can be synchronized with computer timing through the use of timing pulses BT1 or BT2A, which are available at the computer interface. The strobe pulse should be gated by condition signals that occur only during the break cycle of an output

transfer. Figure 5-13 shows typical logic circuits to effect an output data transfer. In this example, the B break signal and an inverted TRANSFER DIRECTION signal are combined in a diode NAND gate to condition a diode-capacitor-diode gate. A buffered BT2A pulse triggers the DCD gate to produce the strobe pulse. The BT2A pulse determines the timing of the transfer in this example, since the input of the output buffer register has DCD gates. Conventional DCD gates require a minimum setup time of 400 ns, which is adequately provided between the time when data is available in the DBMB and BT2A time. If diode gates or other devices with a setup time of less than 400 ns are used at the input of the output buffer register, the BT1 pulse and a delay, or some other pulse generated by the device interface before BT2A time, can trigger strobe pulse generation. By careful design of the input and output gating, one register can serve as both the input and output buffer register. Most DEC options using the data break facility have only one data buffer register with appropriate gating to allow it to serve as an output buffer when the TRANSFER DIRECTION signal is at ground potential or as an input buffer when the TRANSFER DIRECTION signal is -3V.

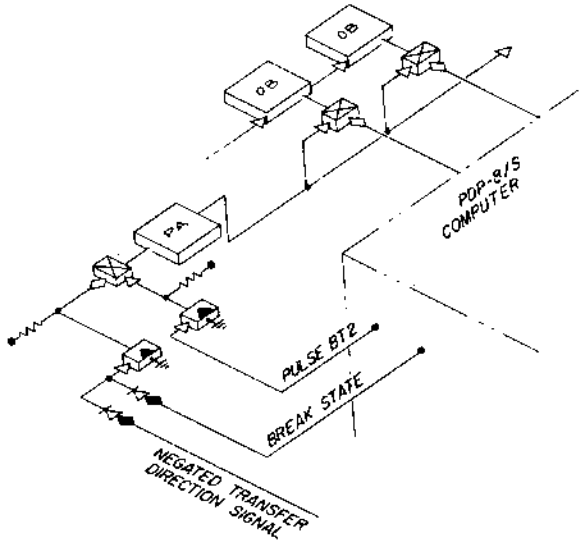


Figure 5-13 Device Interface for Strobing Output Data

5.9.4.4 Memory Increment. - In this type of data break, the content of core memory at a device-specified address is read into the DBMB, is incremented by 1, and is rewritten at the same address within one 8.0 μs cycle. This feature is particularly useful in building a histogram of a series of measurements, such as in pulse-height analysis applications. For example, in a computer-controlled experiment that counts the number of times each value of a parameter is measured, a data break can be requested for each measurement, and the measured value can be used as the core memory address to be incremented (counted). The signal interface for a memory increment data break is similar to an output transfer data break except that the device interface generates an INCREMENT MB signal and does not

generate a strobe pulse (no data transfer occurs between the DB8S and the device). Timing of memory increment operations appear in Figure 5-14, and an example of the logic circuits used by a device interface appears in Figure 5-15.

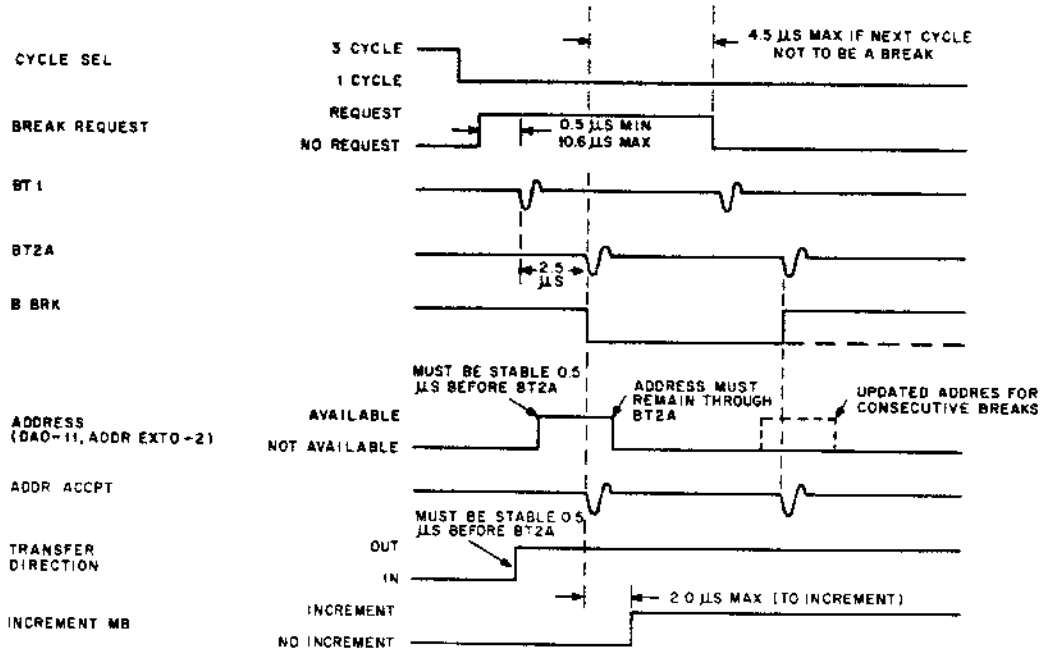


Figure 5-14 Interface Timing, Memory Increment Data Breaks

An interface for a device, using memory increment data breaks, must supply 12 data address lines (DA_{0-11}), a TRANSFER DIRECTION signal, a CYCLE SELECT signal, and a BREAK REQUEST signal to the computer data break facility, as in an output transfer data break. In addition, a ground potential INCREMENT MB signal must be provided no later than 2.0 µs after BT2A time of the break cycle. This signal can be generated in the device interface by ANDing the B BRK DB8S output signal, the output transfer condition of the TRANSFER DIRECTION signal, and the condition signal in the device that indicates that incrementing should take place. When the DB8S receives this INCREMENT MB signal, it adds one to the content of DBMB, at BT2A (+2.5 µs) time, then restores DBMB to memory.

The device interface logic shown in Figure 5-16 samples the most significant bit of the data word (GMB0) to determine whether it overflows when incremented. If GMB0 changes from the 1 to the 0 state when the data word is incremented, this logic requests a program interrupt to allow the program to take some appropriate action, such as incrementing a core memory counter for numbers above 4096, stopping a test to compile the data gathered to the current point in the operation, reinitializing the

addressing, etc. The logic in the figure uses the select code of a programmed data transfer to skip on the overflow condition to determine the cause of a program interrupt, to clear the overflow flip-flop, and to clear the device flag. Note that the devices that use data break transfers almost always use programmed data transfers to start and stop operation of the device, to initialize registers, etc., and do not rely on data break facilities alone to control their operations.

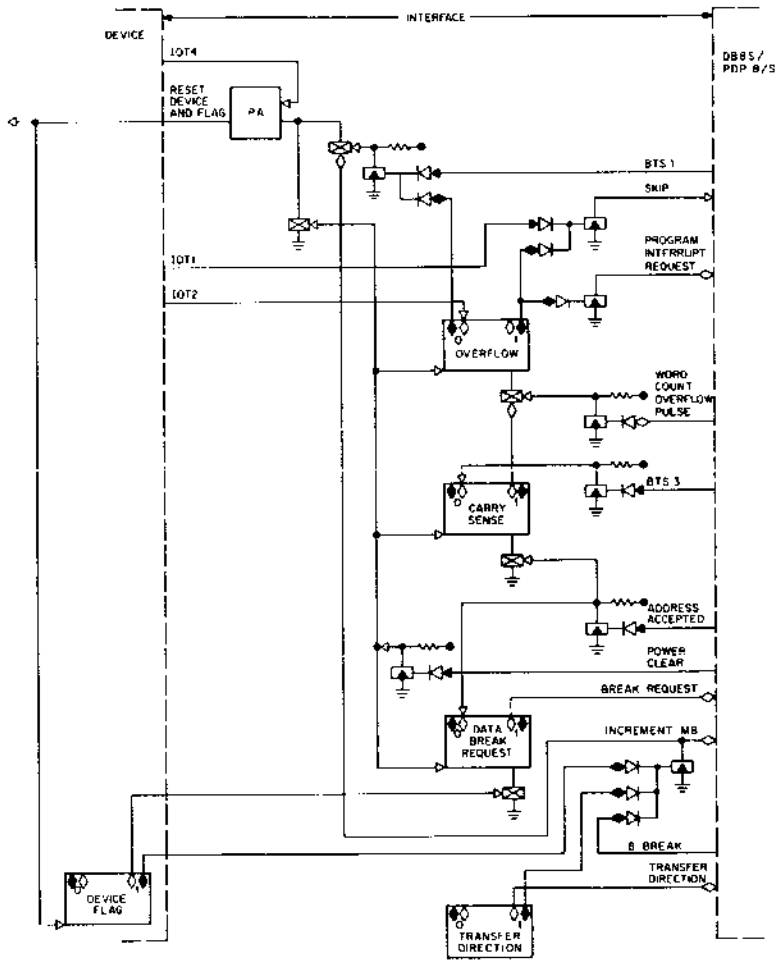


Figure 5-15 Device Interface Logic for Memory Increment Data Break

5.9.4.5 Three Cycle Data Breaks. - Timing of input or output 3-cycle data breaks is shown in Figure 5-16. The 3-cycle break provides an economical method of controlling the flow of data at high speeds between PDP-8/S core memory and fast peripheral devices, e.g., drum, disc, magnetic tapes, and line printers; allowing transfer rates in excess of 40K words per second. The 3-cycle data break facility uses many of the gates and transfer paths of the 1-cycle data break system, but this does not preclude the use of 1-cycle data break devices. Any combination of 3-cycle and 1-cycle data break devices can be used in one system, so long as a multiplexer channel is available for each.

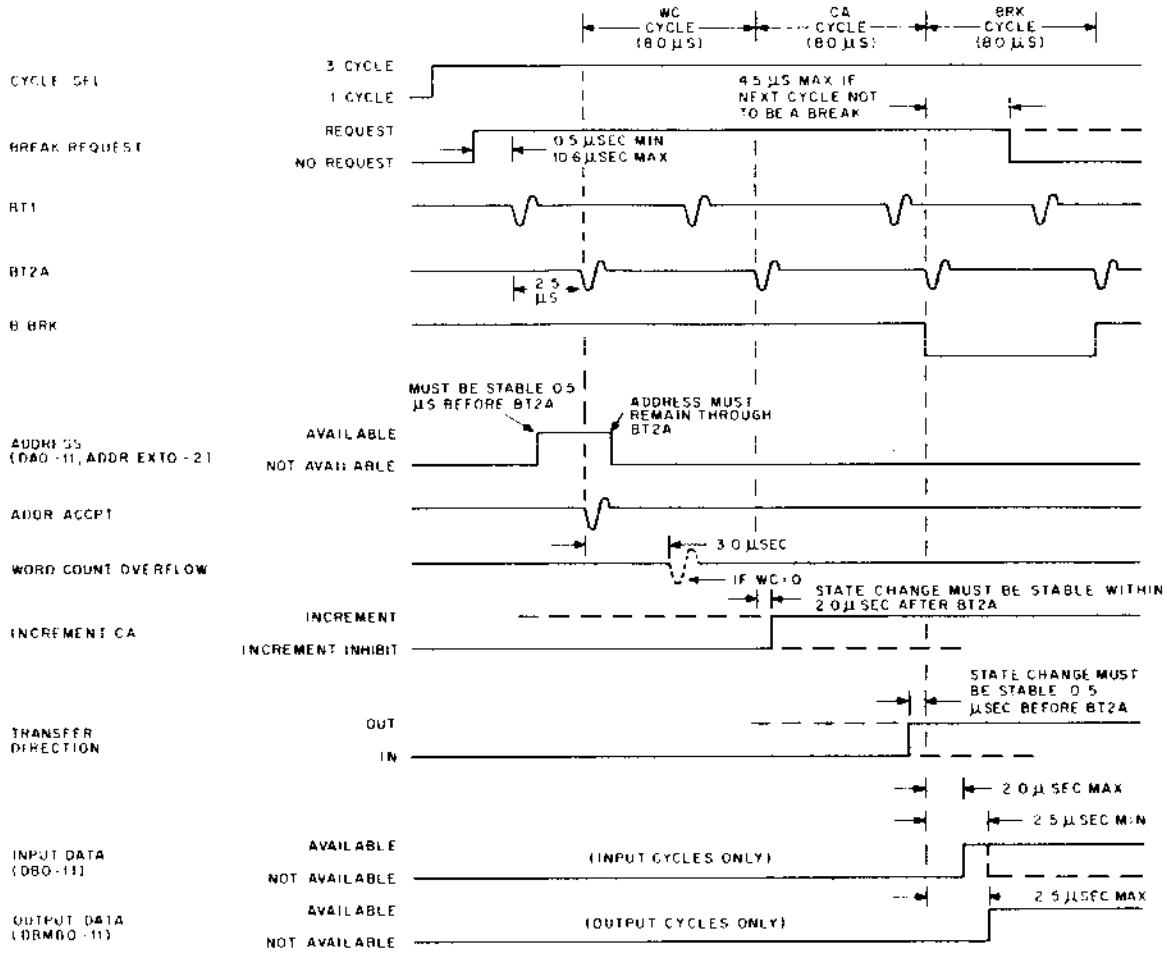


Figure 5-16 Interface Timing, 3-Cycle Breaks

The 3-cycle data break is entered similarly to the 1-cycle data break, except a ground-level CYCLE SELECT signal allows entry to the WC (Word Count) state to increment the fixed core memory location containing the word count. The device requesting the break supplies this address as in the 1-cycle data break, except that this address is fixed and can be supplied by wired ground and -3V signals, rather than from a register. The sole restriction on this address is that it must be an even number (bit 11=0). Following the WC a CA (Current Address) state is entered, in which the core memory location following the WC address is read, incremented by one, restored to memory and used as the transfer address. Then the normal BRK (Break) state is entered to effect the transfer.

Two additional control lines are provided with the 3-cycle data break as follows.

a. WC OVERFLOW. A standard 0.4 µs negative computer output pulse is transmitted to the device when the word count becomes equal to zero.

b. INCREMENT CA INHIBIT. When ground potential, this device-supplied signal inhibits incrementation of the current address word.

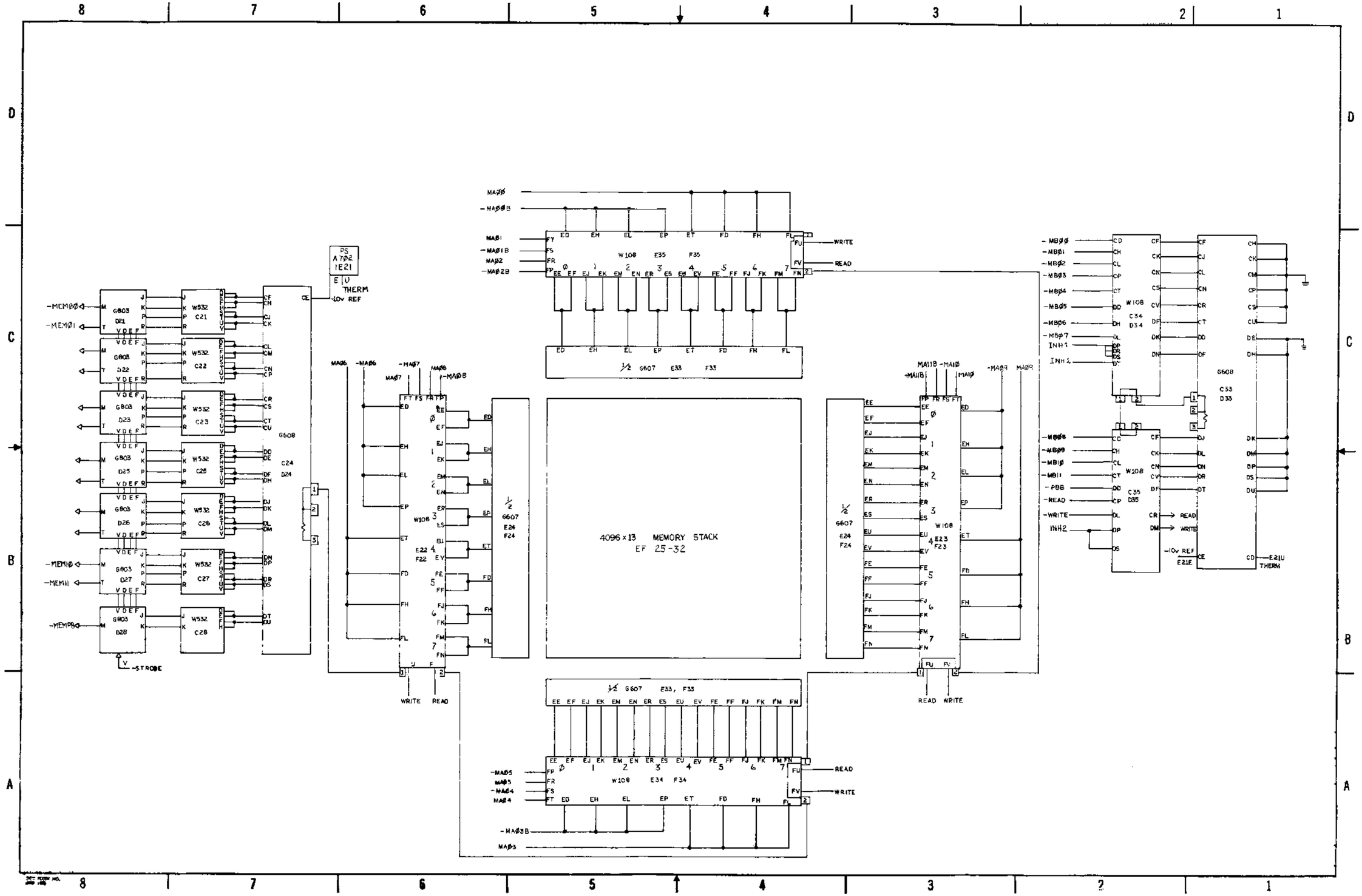
APPENDIX
ENGINEERING DRAWINGS

Reduced copies of the flow charts, logic drawings and circuit schematics are included at the back of this manual. Chapter 3 explains the drawing numbers and the type codes that identify engineering drawings for the PDP-8/S and details the notation and conventions used in the block schematics and flow charts, which are the basis for learning and maintaining the equipment. There are many other engineering drawings, however, used primarily for reference in maintenance.

The master drawing list, A-ML-8S-0, lists the block schematics, flow charts, parts list, module utilization drawings, some assembly drawings, and the drawing index list for the computer. This last drawing, D-DI-8S-0-27, lists all mechanical and electrical drawings for the PDP-8/S including the teletype (sheet 2). Sheet 1 is a map showing the relationship among the various categories of drawings.

Detailed information about the modules that make up the processor and memory is given in the module utilization drawings, D-MU-8S-0-25 for the 8K and D-MU-8S-0-26 for the 4K. Each has two sheets showing the six mounting panels, each panel being divided into 40 sections representing the plugin locations. Above the locations are the type numbers of the modules occupying them. Each location is further partitioned according to the individual circuits (flip-flops, pulse amplifiers, inverters) in the module. Circuits are identified by logical function, using the same signal names that appear on the block schematics. For example, a pulse amplifier is labeled by naming the output pulse; an inverter or diode gate is labeled by the output of the net in which it is used. Clamped loads are identified only by the pins to which they are connected.

The rack mounted model uses a standard 728 power supply and 832 power control, which are shown in the circuit schematics. The power supply, circuit breakers, and ac wiring for the table model are shown in the rear panel assembly drawing, D-AD-7005193-0-0.



Memory Block Diagram (4K) D-BS-8S-0-4

E38

NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
IOØØ	E3D	D	R001/11MA	→
IOØ1	E3F	E	R001/11MA	→
GND		F		
IOØ2	E3J	H	R001/11MA	→
GND		J		
IOØ3	E3L	K	R001/11MA	→
GND		L		
IOØ4	E3N	M	R001/11MA	→
GND		N		
IOØ5	A3T	P	R001/11MA	→
GND		R		
IOØ6	A3R	S	R001/11MA	→
IOØ7	A3N	T	R001/11MA	→
GND		U		
IOØ8	A3L	V	R001/11MA	→

E39

NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
BAC 0(1)	D5F	D	R107/18ma	◇
BAC 1(1)	D5J	E	R107/18ma	◇
GND		F		
BAC 2(1)	D5L	H	R107/18ma	◇
GND		J		
BAC 3(1)	D5N	K	R107/18ma	◇
GND		L		
BAC 4(1)	D5R	M	R107/18ma	◇
GND		N		
BAC 5(1)	D5T	P	R107/18ma	◇
GND		R		
BAC 6(1)	D5F	S	R107/18ma	◇
BAC 7(1)	C5J	T	R107/18ma	◇
GND		U		
BAC 8(1)	C5L	V	R107/18ma	◇

E40

NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
BMBØØ(Ø)	C38D	D	R107/18MA	◆
BMBØ1(Ø)	C38F	E	R107/18MA	◆
GND		F		
BMBØ2(Ø)	C38J	M	R107/18MA	◆
GND		J		
BMBØ3(1)	B37F	K	R107/18ma	◆
GND		L		
BMBØ3(Ø)	B37J	M	R107/18ma	◆
GND		N		
BMBØ4(1)	B37L	P	R107/18ma	◆
GND		R		
BMBØ4(Ø)	B37N	S	R107/18ma	◆
BMBØ5(1)	B37R	T	R107/18ma	◆
GND		U		
BMBØ5(Ø)	B37T	V	R107/18ma	◆

E37

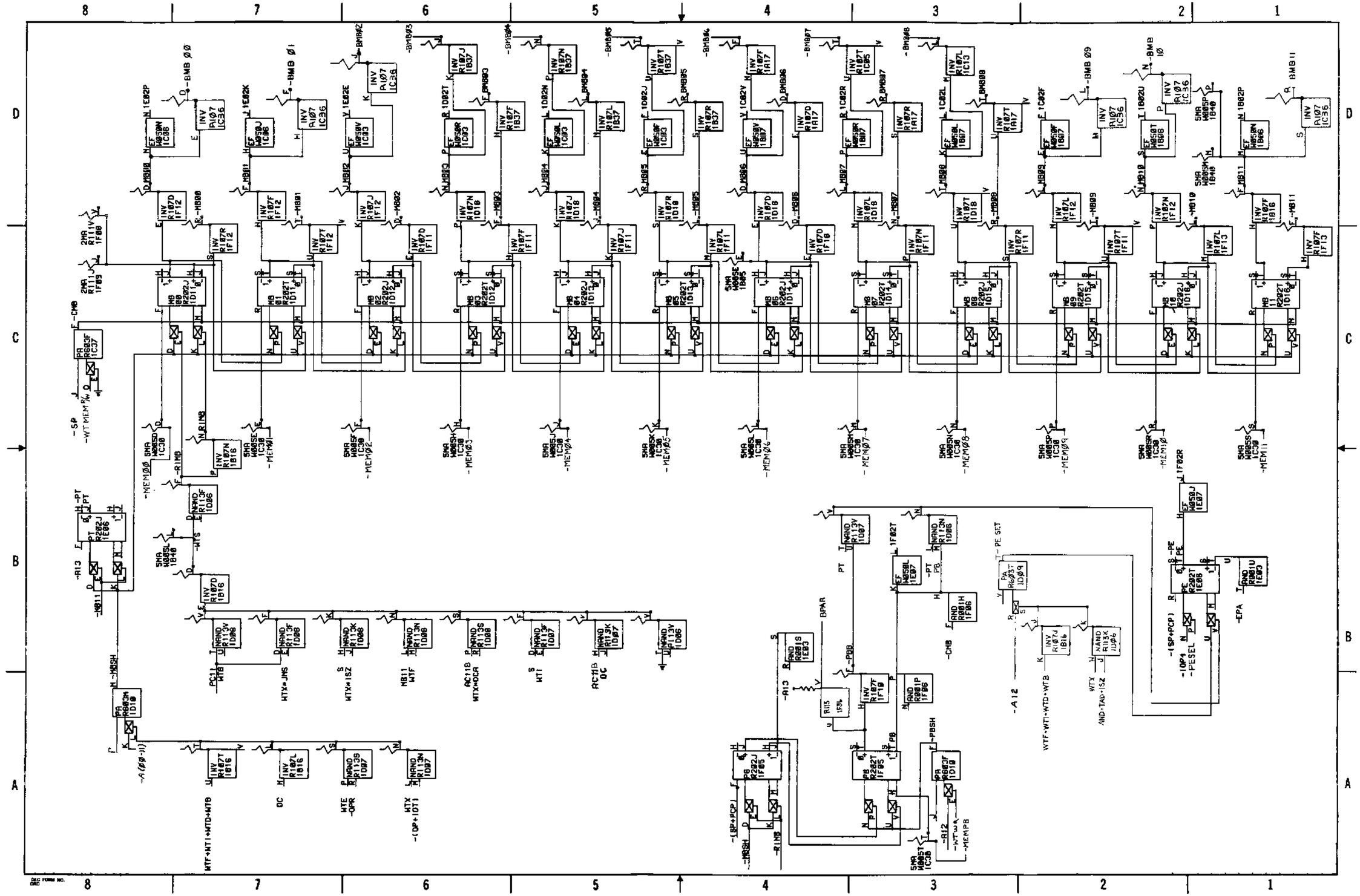
NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
IOØ9	A3J	D	R001/11MA	→
IOIØ	A3F	E	R001/11MA	→
GND		F		
IOII	A3D	H	R001/11MA	→
GND		J		
SKP	A9K	K	R107/11MA	→
GND		L		
INT	A40E	M	R107/11MA	◇
GND		N		
CLRAC	A19R	P	R202/20MA	→
GND		R		
B RUN (1)	B36P	S	R113/18MA	◆
BPAR (1)	F3KV	T	R113/18MA	◇
GND		U		
-LCIF	1C31V	V	R282	

B39

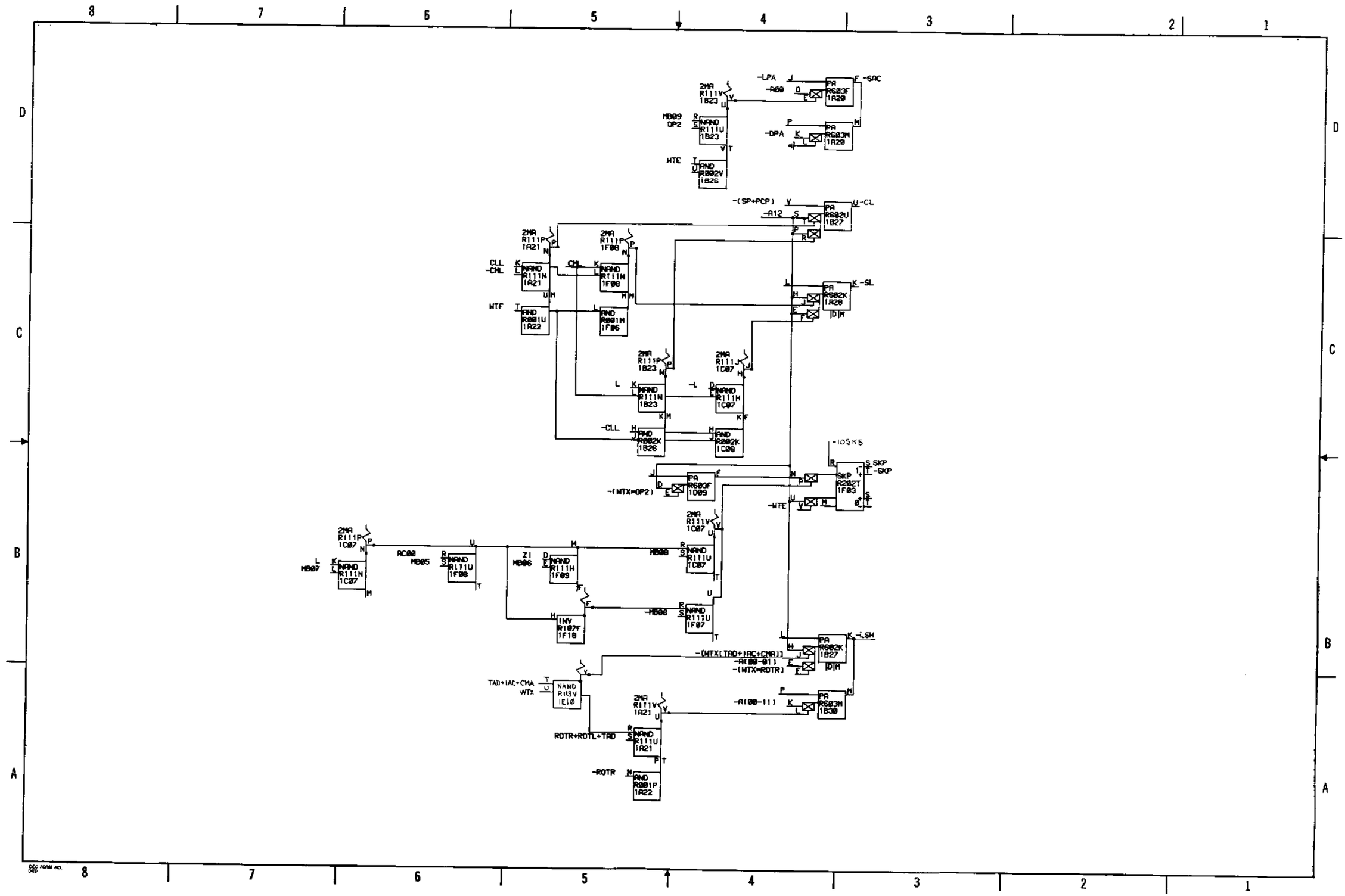
NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
BAC 9(1)	C5N	D	R107/18ma	◇
BAC 10(1)	C5R	E	R107/18ma	◇
GND		F		
BAC 11(1)	C5D	H	R107/18ma	◇
GND		J		
IOP1	A40J	K	4-R107/72MA	→
GND		L		
IOP2	A40H	M	4-R107/72MA	→
GND		N		
IOP4	1B37Ø	P	4-R107/72MA	→
GND		R		
		S		
		T		
GND		U		
B I/O CLEAR	A17L	V	4-R107/72MA	→

D40

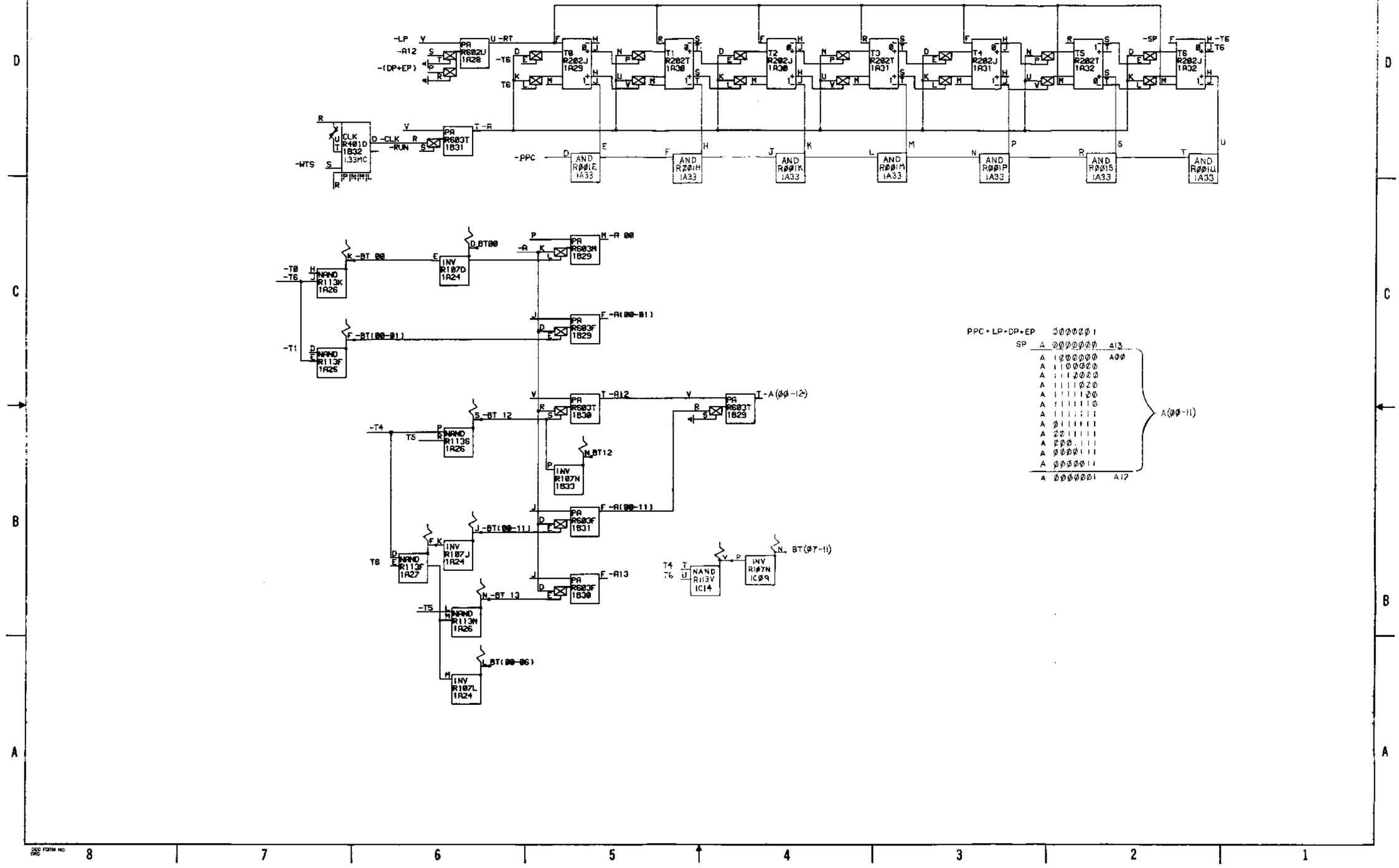
NAME	FROM	PIN	MODULE TYPE/LOAD	ASS.
		A		
		B		
GND		C		
BMBØ3(1)	A17D	D	R107/18ma	◆
BMBØ6(Ø)	A17F	E	R107/18ma	◆
GND		F		
BMBØ7(1)	A17R	H	R107/18ma	◆
GND		J		
BMBØ7(Ø)	C05T	K	R107/18ma	◆
GND		L		
BMBØ8(1)	A17T	M	R107/18ma	◆
GND		N		
BMBØ8(Ø)	C13L	P	R107/18ma	◆
GND		R		
BMBØ9(Ø)	C36L	S	R107/18MA	◆
BMB 10(Ø)	C36N	T	R107/18MA	◆
GND		U		
BMB 11(Ø)	C36R	V	R107/18MA	◆



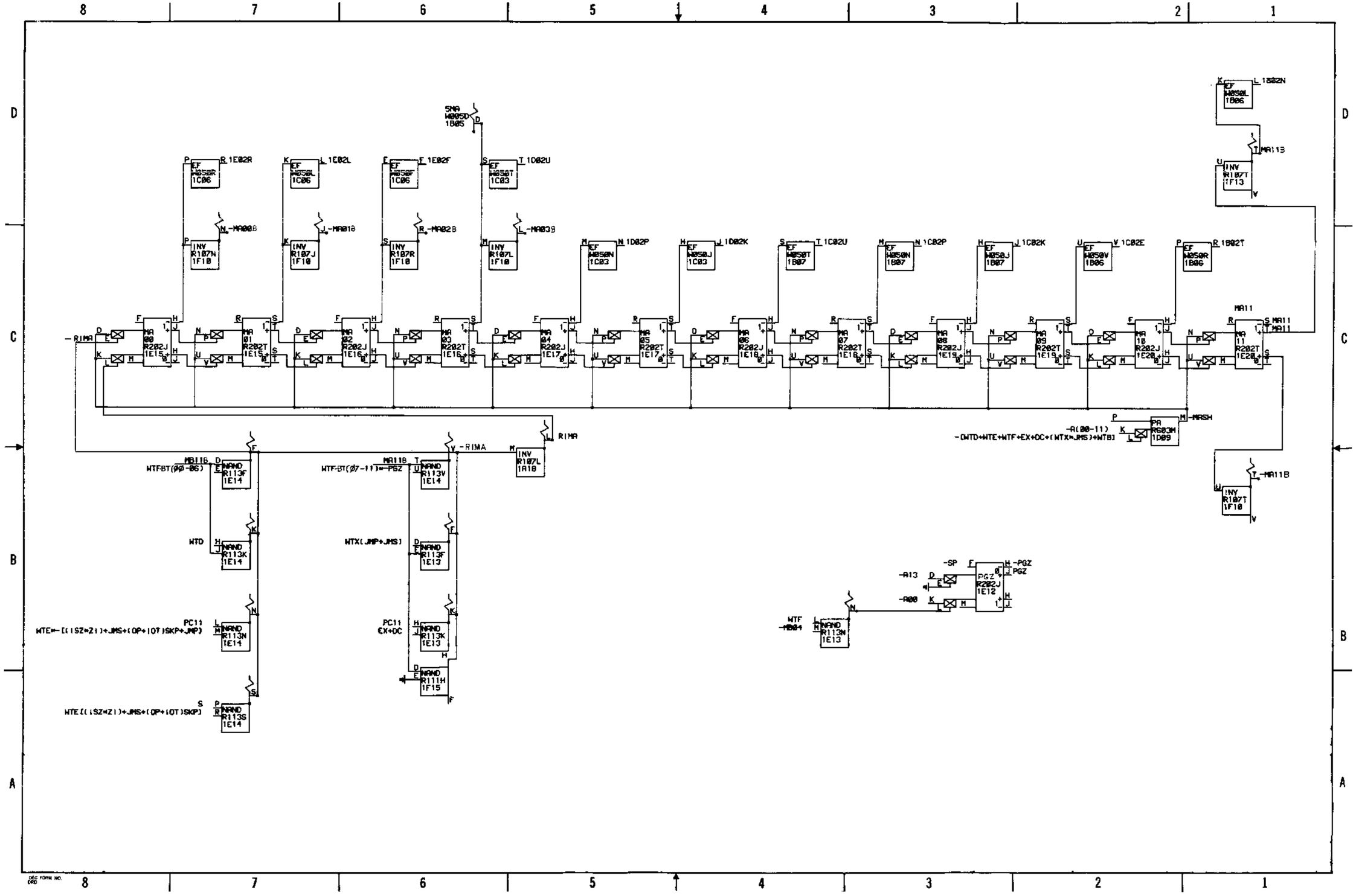
Memory Buffer D-BS-8S-0-9



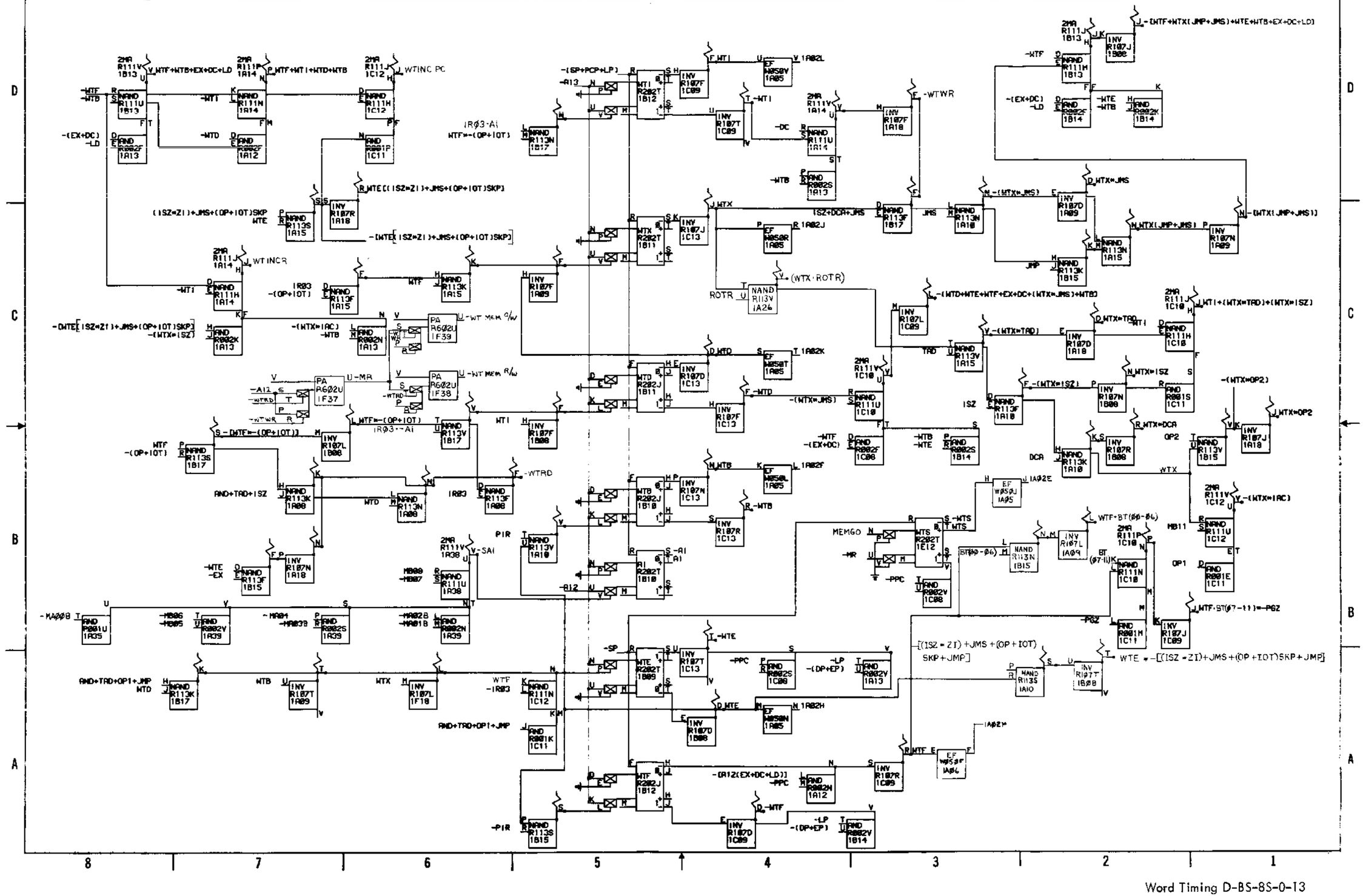
Link and Skip Control D-8S-8S-0-10



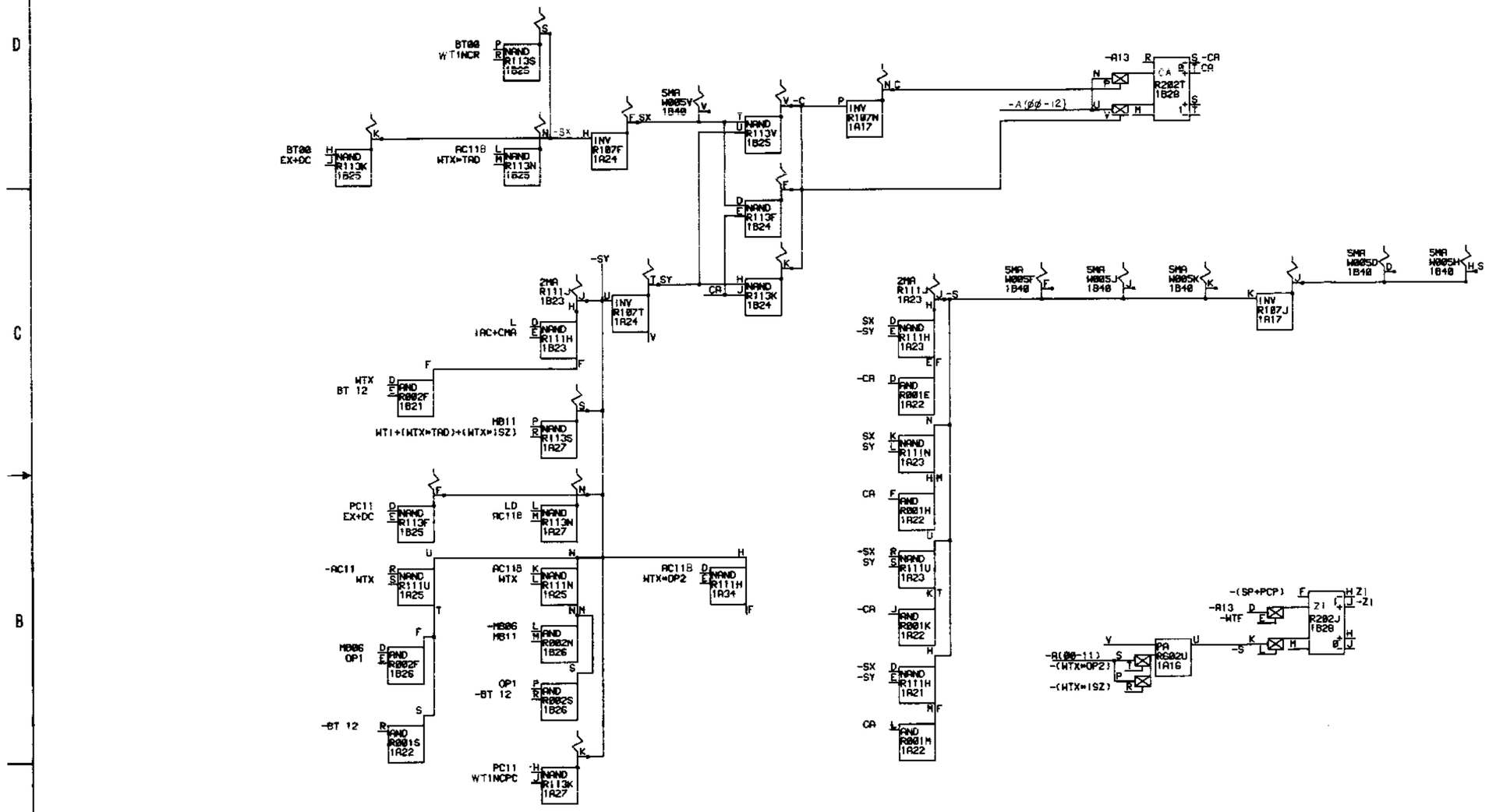
Bit Timing D-BS-8S-0-11



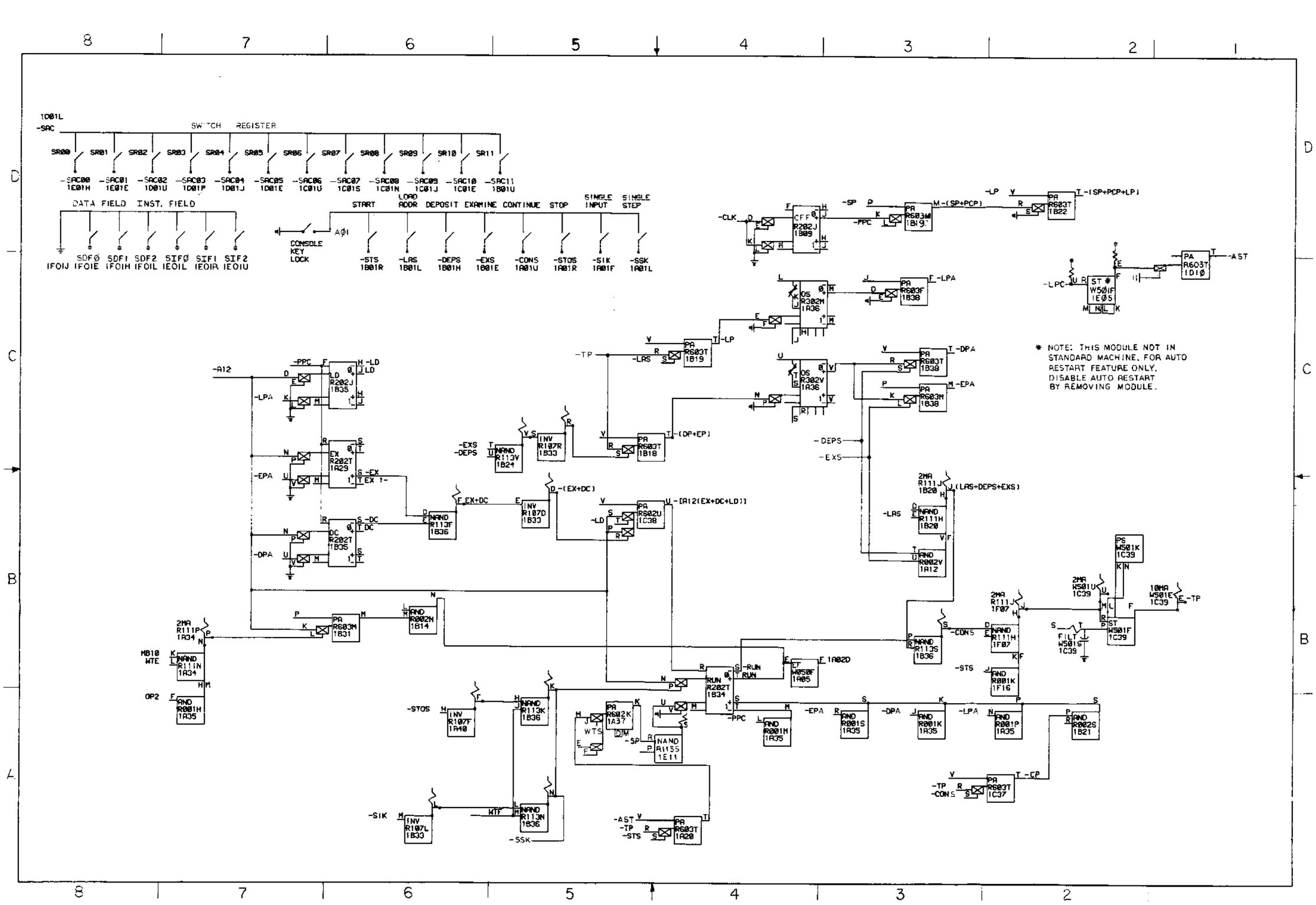
Memory Address D-BS-8S-0-12



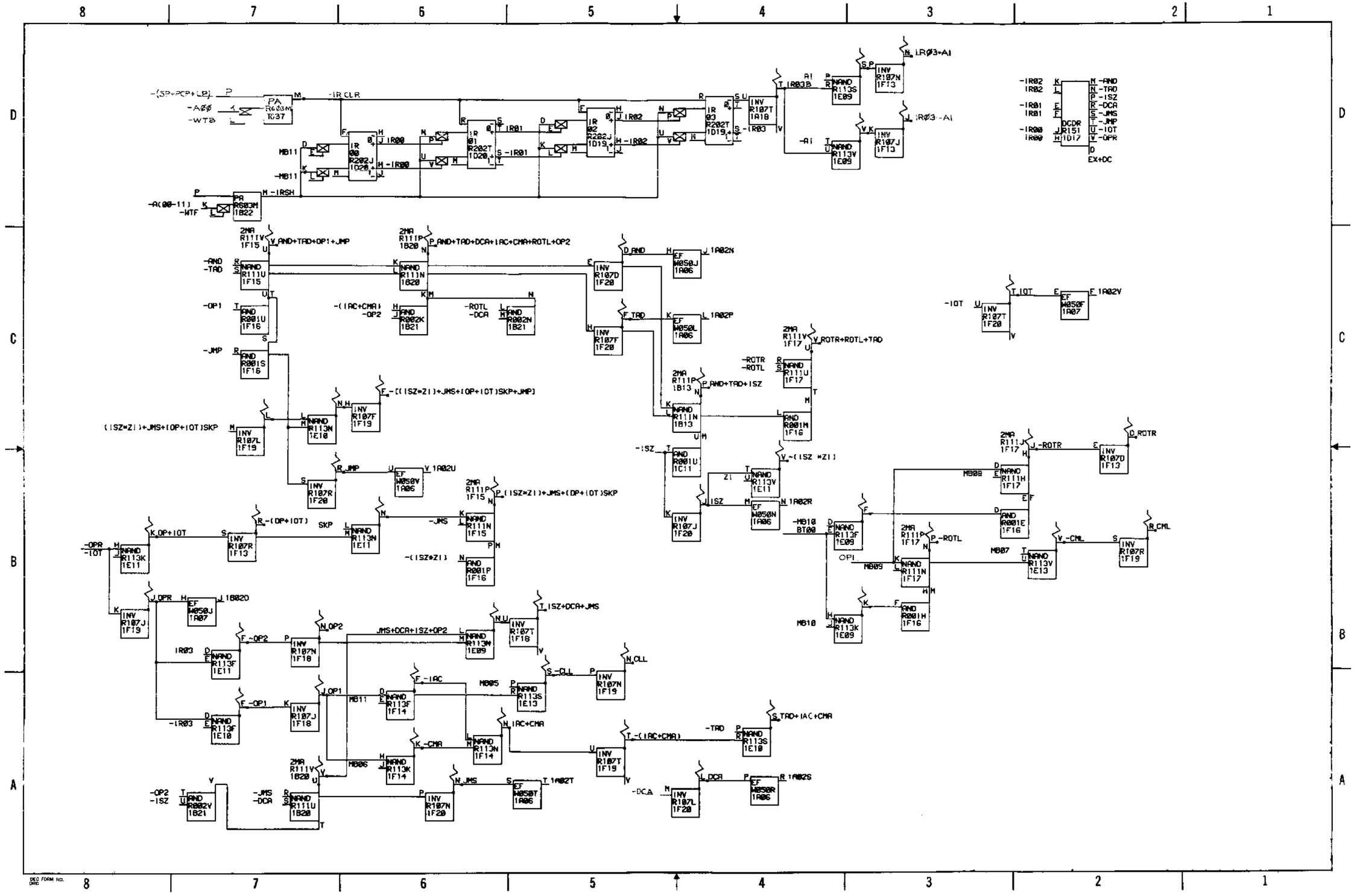
Word Timing D-BS-8S-0-13



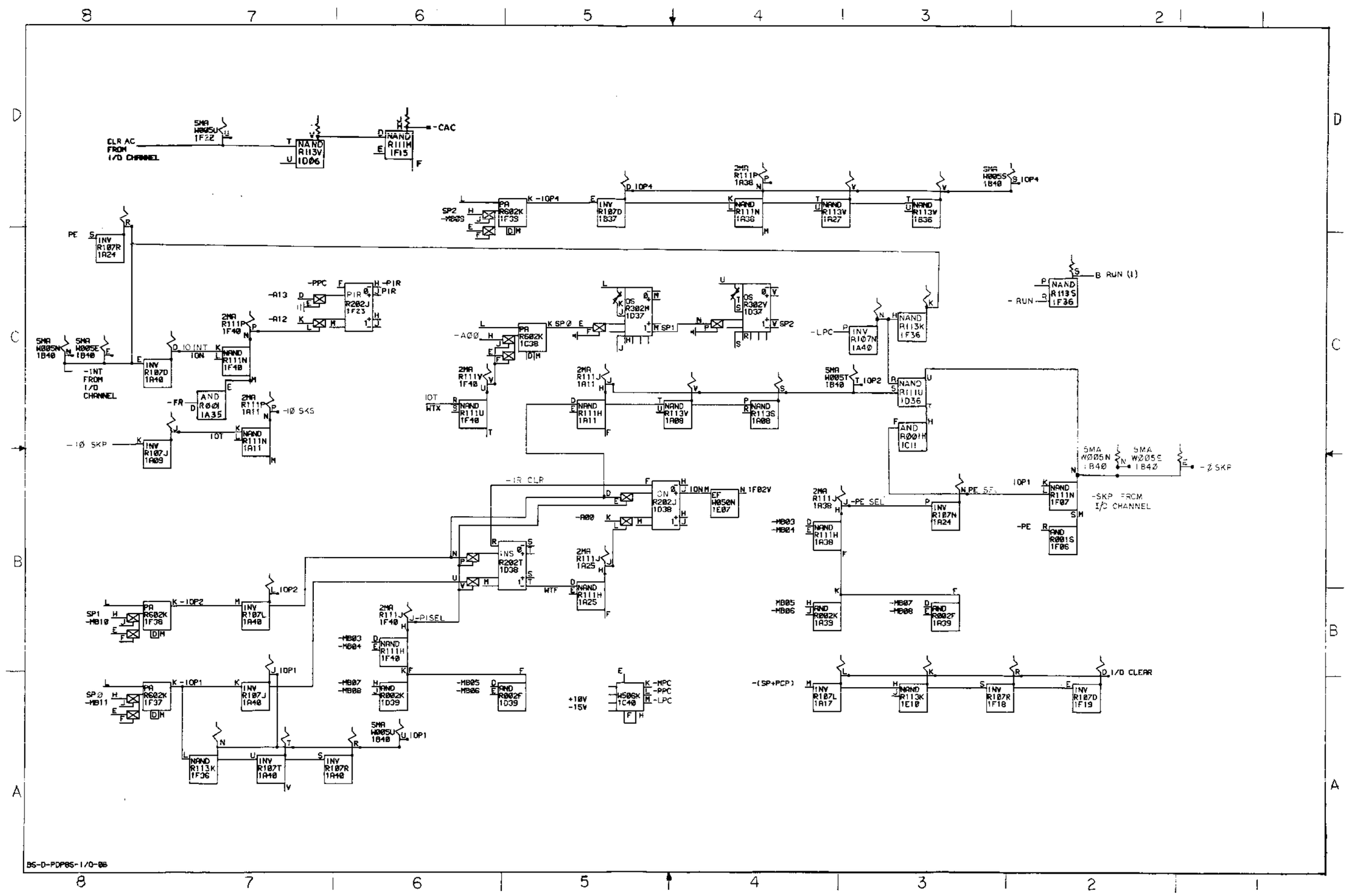
Adder D-BS-8S-0-14

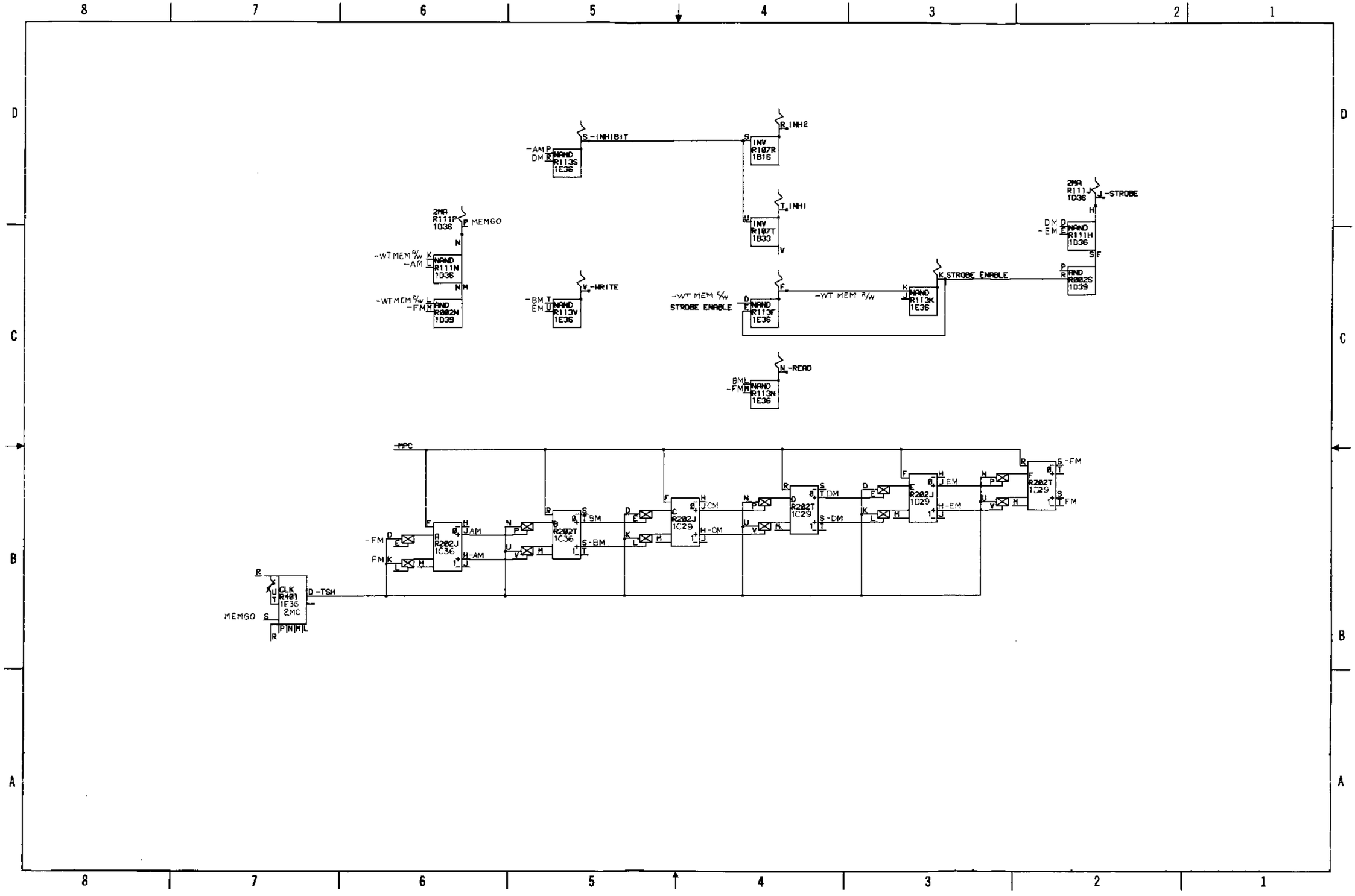


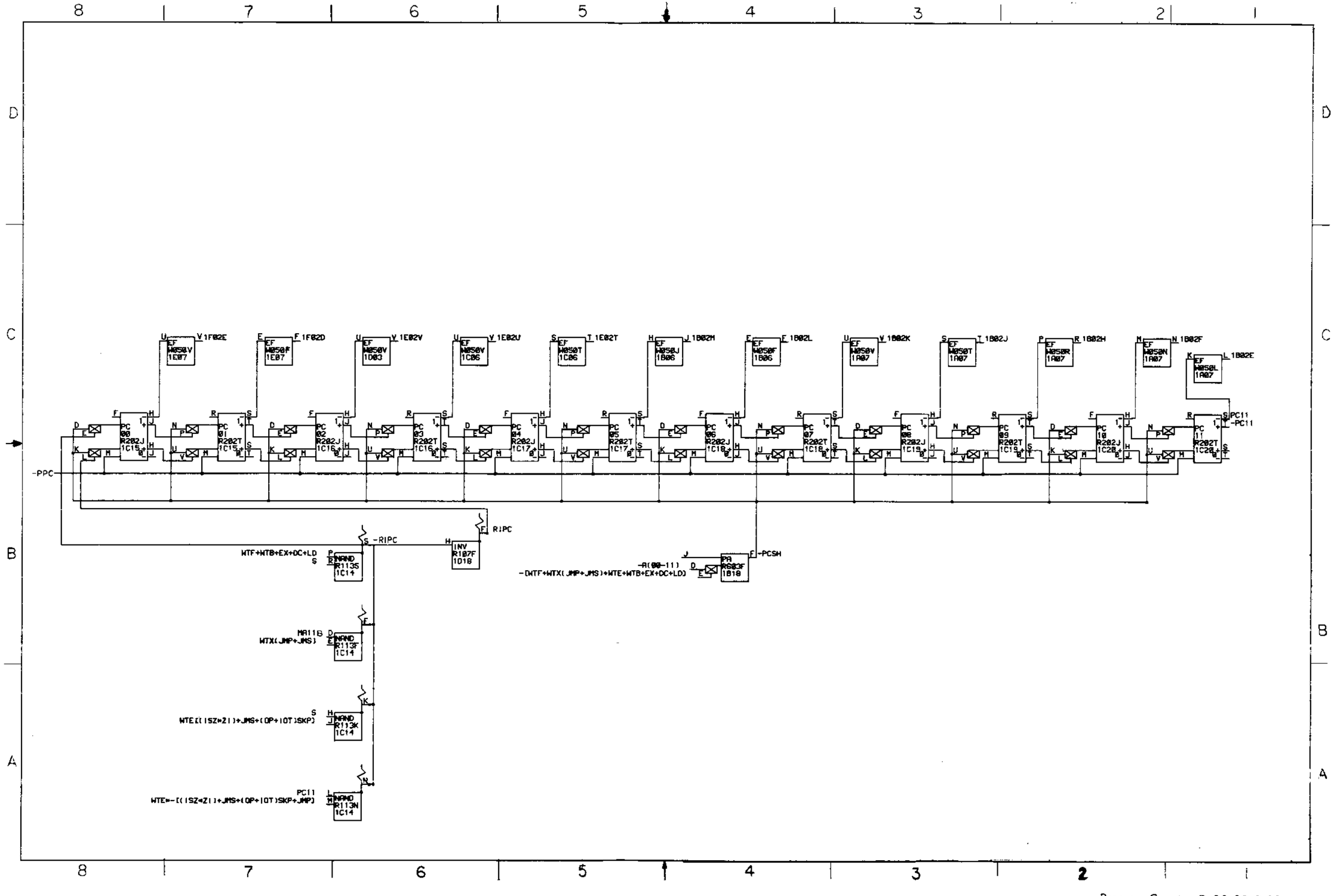
Control D-BS-8S-0-15



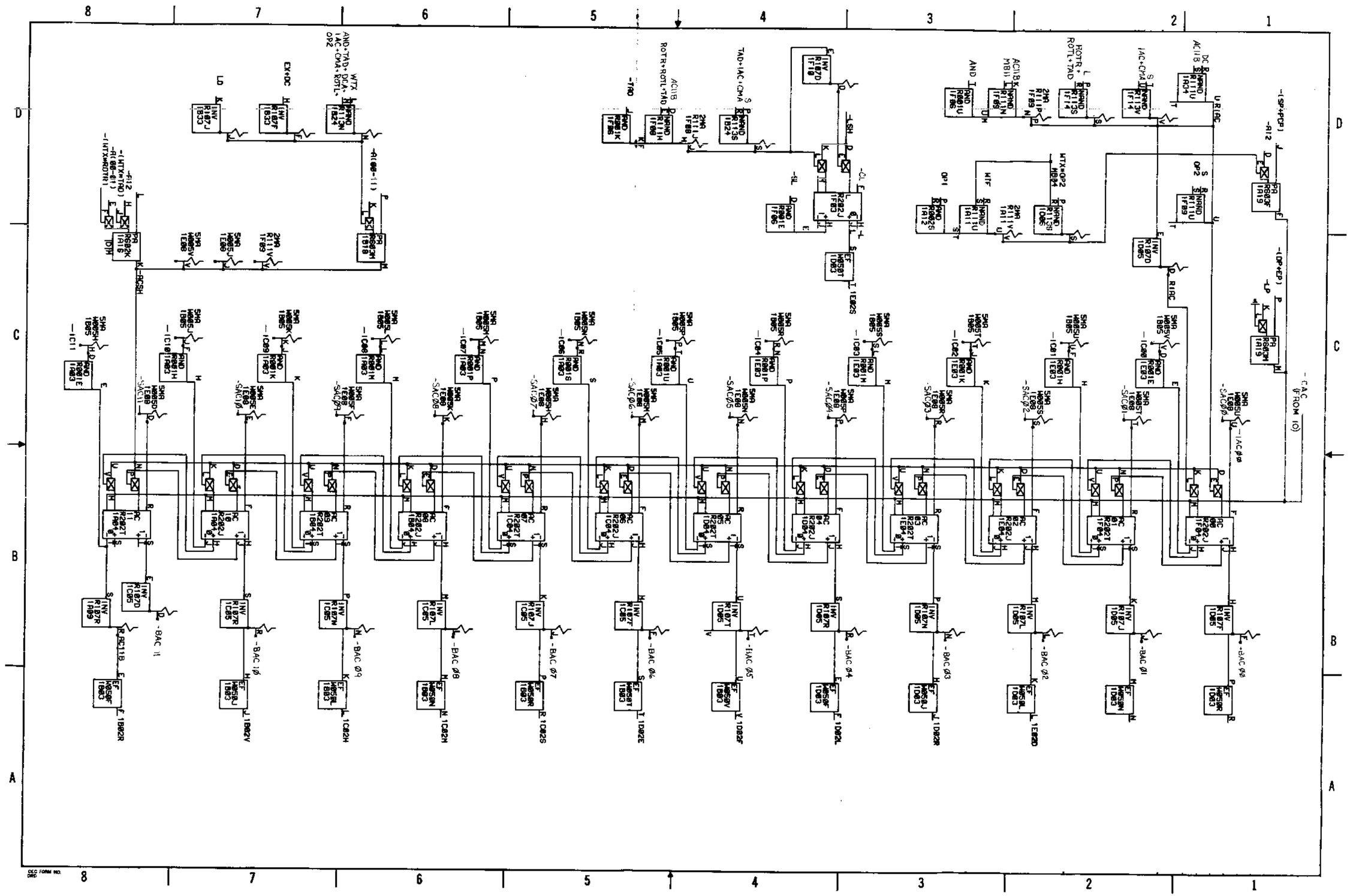
Instruction Register D-BS-8S-0-16


CLR AC FROM I/O CHANNEL
-CAC
PE
-INT FROM I/O CHANNEL
-FR
-Ø SKP
-Ø SKS
-PPC
-PIR
-A13
-A12
-AØØ
SP2
SPØ
SP1
-LPC
B RUN (1)
- RUN
-SKP FROM I/O CHANNEL
-Ø SKP
-PE SEL
-PE
-IR CLR
WTF
IOT
WTX
-(SP+PCP)
I/O CLEAR
+10V
-15V
-MPC
-PPC
-LPC
BS-D-PDP8S-I/O-08

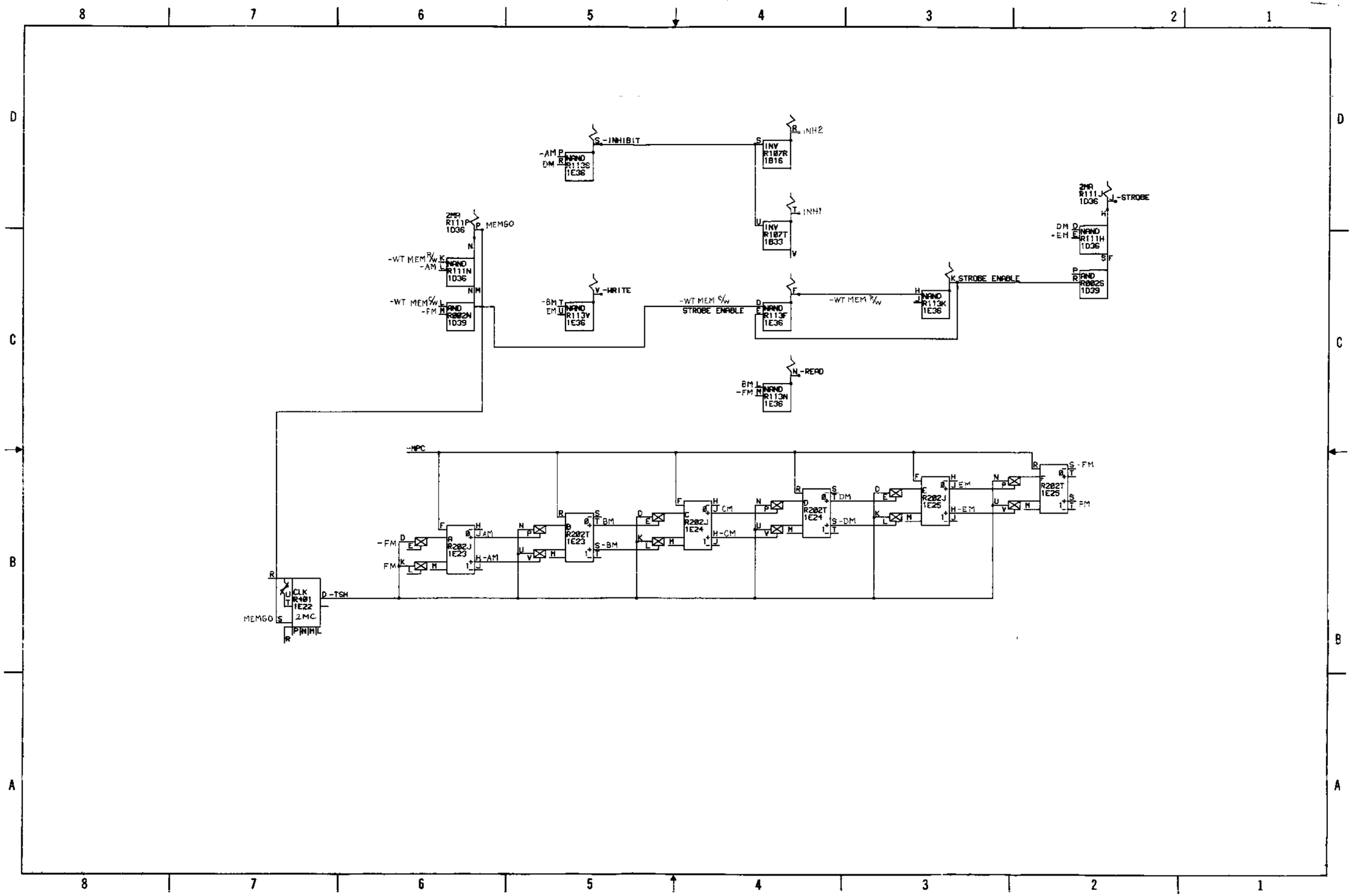

-AMP DM
NAND R113S 1E36
S -INHIBIT
R INH2
INV R107R 1B16
T INH1
INV R107T 1B33
2MA R111P 1D36
P MEMGO
-WT MEM R/W
-AM
NAND R111N 1D36
-WT MEM R/W
-FM
FND R002N 1D39
-BM T
EM U
NAND R113V 1E36
V -WRITE
-WT MEM R/W
STROBE ENABLE
NAND R113F 1E36
-WT MEM R/W
NAND R113K 1E36
K STROBE ENABLE
2MA R111J 1D36
J -STROBE
DM D
-EM E
NAND R111H 1D36
FND R002S 1D39
BML
-FM H
NAND R113N 1E36
N -READ
-MPC
R
CLK R101 1F36 2MC
D -TSH
MEMGO S
P N M L
R
-FM
FM
A R202J 1C36
H-AM
J AM
B R202T 1C36
S-BM
T BM
C R202J 1C29
H-CM
J CM
D R202T 1C29
S-DM
T DM
E R202J 1D29
H-EM
J EM
F R202T 1D29
S-FM
T FM

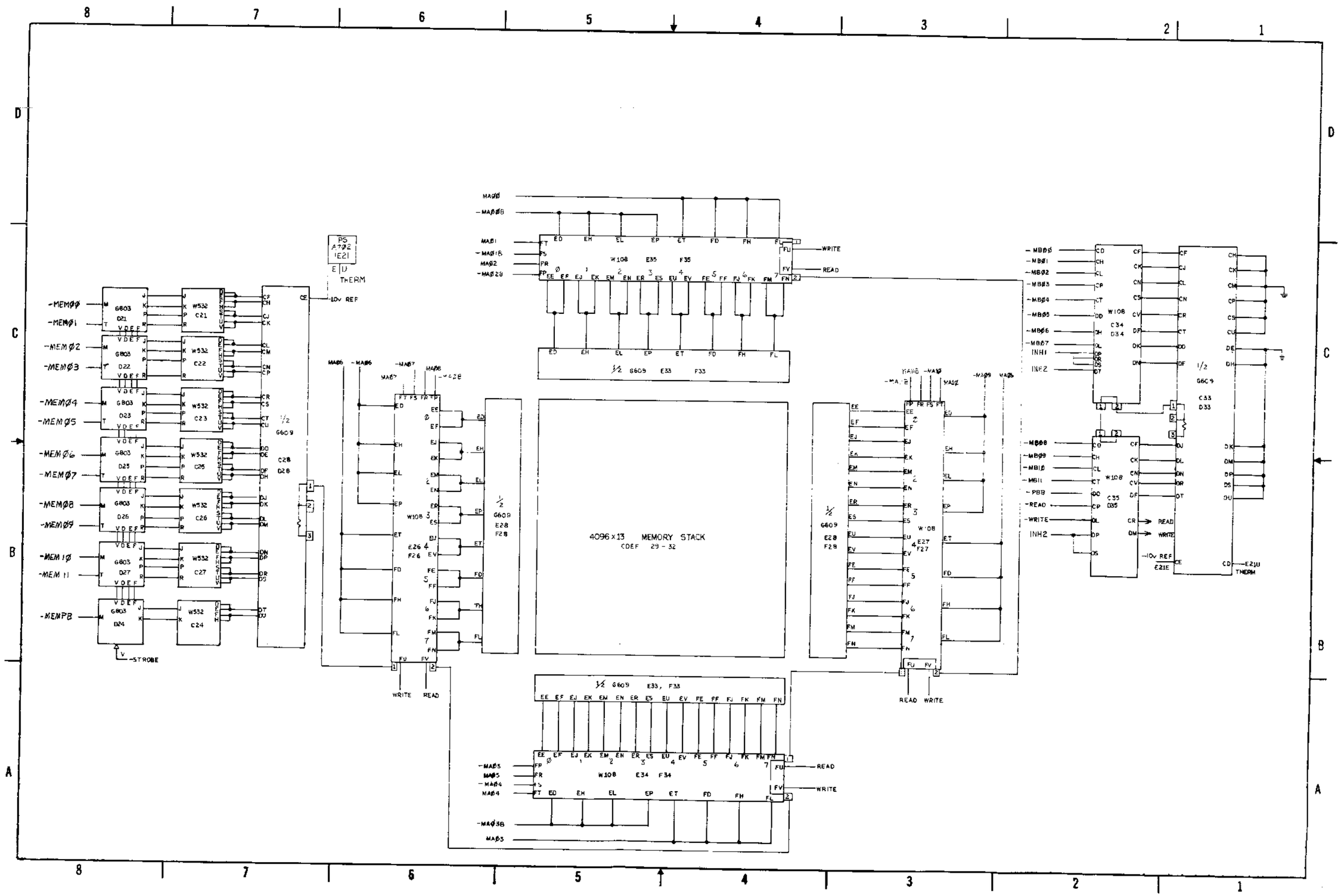


Program Counter D-BS-8S-0-19

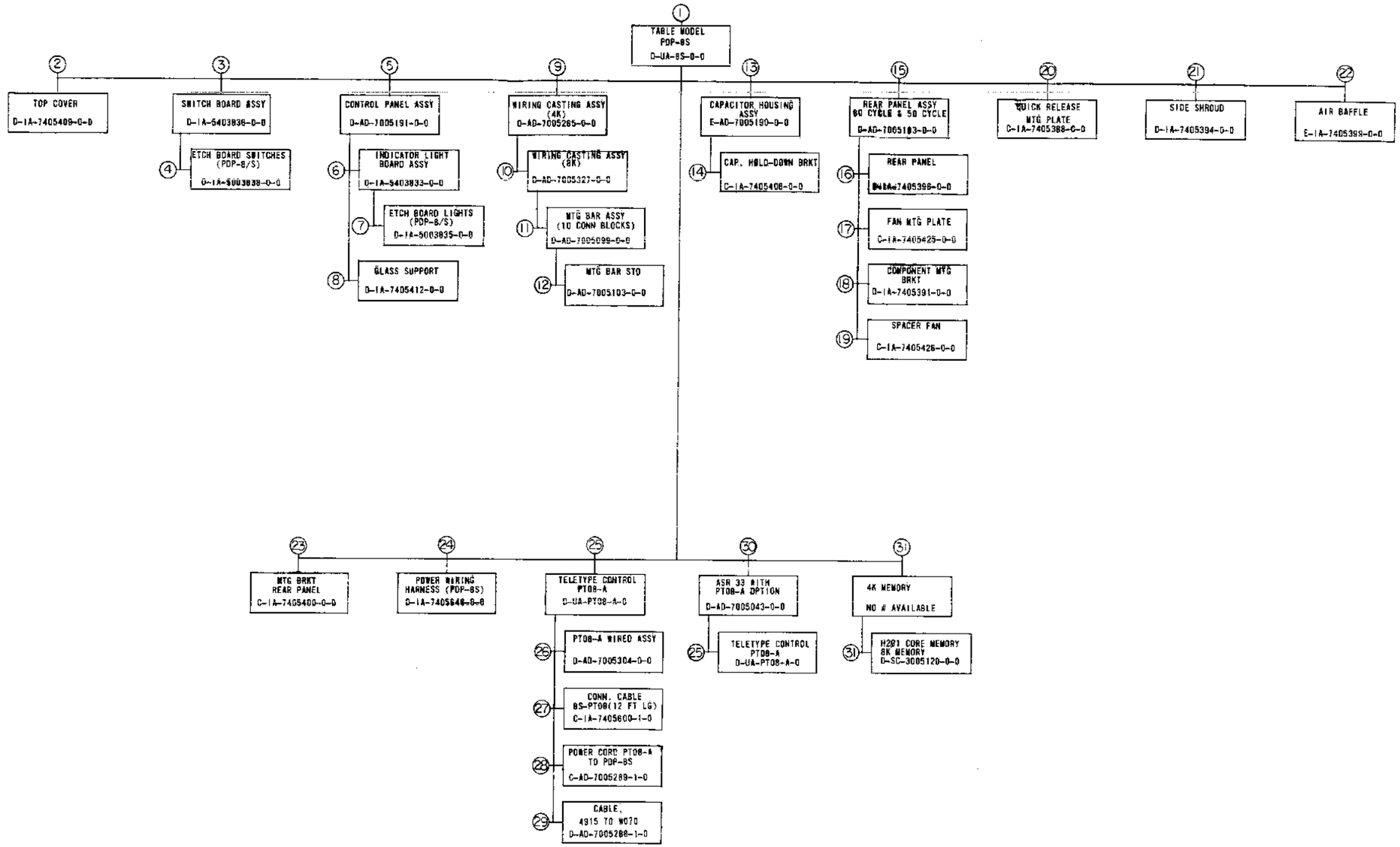


Accumulator D-BS-8S-0-20


-AM
DM
-INHIBIT
INH2
INH1
MEMGO
-WT MEM R/W
-AM
-WT MEM R/W
-FM
-BM
EM
-WRITE
-WT MEM R/W
STROBE ENABLE
-WT MEM R/W
STROBE ENABLE
BM
-FM
-READ
-STROBE
DM
-EM
-MPC
-FM
FM
-TSH
MEMGO
CLK
R401
1E22
2MC
JAM
H-AM
BM
S-BM
JCM
H-CM
DM
S-DM
JEM
H-EM
S-FM
FM



Memory Block Diagram (8K) D-BS-8S-0-23

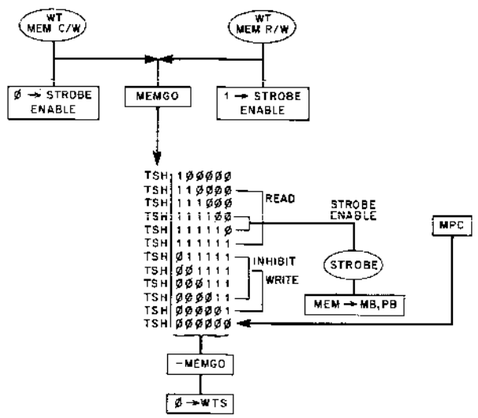

1
TABLE MODEL
PDP-8S
D-UA-8S-0-0
2
TOP COVER
D-1A-7405409-0-0
3
SWITCH BOARD ASSY
D-1A-5003836-0-0
4
ETCH BOARD SWITCHES
(PDP-8/S)
D-1A-5003838-0-0
5
CONTROL PANEL ASSY
D-AD-7005191-0-0
6
INDICATOR LIGHT
BOARD ASSY
D-1A-5003833-0-0
7
ETCH BOARD LIGHTS
(PDP-8/S)
D-1A-5003835-0-0
8
GLASS SUPPORT
D-1A-7405412-0-0
9
WIRING CASTING ASSY
(4K)
D-AD-7005265-0-0
10
WIRING CASTING ASSY
(8K)
D-AD-7005327-0-0
11
MTG BAR ASSY
(10 CONN BLOCKS)
D-AD-7005099-0-0
12
MTG BAR STD
D-AD-7005103-0-0
13
CAPACITOR HOUSING
ASSY
E-AD-7005190-0-0
14
CAP. HOLD-DOWN BRKT
C-1A-7405408-0-0
15
REAR PANEL ASSY
60 CYCLE & 50 CYCLE
D-AD-7005183-0-0
16
REAR PANEL
D-1A-7405398-0-0
17
FAN MTG PLATE
C-1A-7405425-0-0
18
COMPONENT MTG
BRKT
D-1A-7405391-0-0
19
SPACER FAN
C-1A-7405426-0-0
20
QUICK RELEASE
MTG PLATE
C-1A-7405388-C-0
21
SIDE SHROUD
D-1A-7405394-0-0
22
AIR BAFFLE
E-1A-7405399-0-0
23
MTG BRKT
REAR PANEL
C-1A-7405400-0-0
24
POWER WIRING
HARNESS (PDP-8S)
D-1A-7405648-8-0
25
TELETYPE CONTROL
PT08-A
D-UA-PT08-A-0
26
PT08-A WIRED ASSY
D-AD-7005304-0-0
27
CONN. CABLE
8S-PT08(12 FT LG)
C-1A-7405800-1-0
28
POWER CORD PT08-A
TO PDP-8S
C-AD-7005288-1-0
29
CABLE,
4915 TO W070
D-AD-7005288-1-0
30
ASR 33 WITH
PT08-A OPTION
D-AD-7005043-0-0
25
TELETYPE CONTROL
PT08-A
D-UA-PT08-A-0
31
4K MEMORY
NO # AVAILABLE
31
H281 CORE MEMORY
8K MEMORY
D-SC-3005120-0-0

MECHANICAL			DEPT. USAGE		
FIND NO	DESCRIPTION	PART NO.	PROD	CUST	F/C
1	TABLE MODEL PDP-8S	D-UA-8S-0-0			
	TABLE MODEL PDP-8S (P.L.)	A-PL-8S-0-0			
	GUIDE, TOP COVER	B-MD-7405405-0-0			
	SHIELD, FILTER CIRCUIT	C-MD-7405589-0-0			
	SIDE BRKT, SHROUD	B-MD-7405402-0-0			
	SPACER, SHROUD	B-MD-7405401-0-0			
	COVER, BOTTOM	D-MD-7405404-0-0			
	AIR EXHAUST	D-MD-7405397-0-0			
	FOOT, REAR	B-MD-7405403-0-0			
	POSITIONING PLATE	B-MD-7405410-0-0			
	BEZEL CASTING REWORK	D-MD-7405414-0-0			
	SIDE POS. PLACE	A-MD-7406190-0-0			
2	TOP COVER	D-IA-7405409-0-0			
3	SWITCH BOARD ASSY	D-IA-5403836-0-0			
	SPACER#2 SWITCH BOARD	C-MD-5503902-0-0			
	ROCKER TO SWITCH	D-SC-7405229-8-0			
	ROCKER TO SWITCH	D-SC-7405229-9-0			
	ROCKER TO SWITCH	D-SC-7405229-6-0			
	SPACER#1 SWITCH BOARD	C-MD-5503839-0-0			
4	ETCH BOARD, SWITCHES	D-IA-5003836-0-0			
	EPOXY BOARD	1405020-0-0			
	PRINTED CIRCUIT LAYOUT	5003836-0-2			
5	CONTROL PANEL ASSY	D-AD-7005191-0-0			
	CONTROL PANEL ASSY (P.L.)	A-PL-7005191-0-0			
	SILK SCREEN-STEP#1(GRAY)	C-SS-7405621-0-0			
	SILK SCREEN-STEP#2(RUS.ORN.)	C-SS-7405622-0-0			
	SILK SCREEN-STEP#3(BURNT ORN)	C-SS-7405623-0-0			
	SILK SCREEN-STEP#4(BLK)	C-SS-7405289-0-0			
	GLASS PANEL	D-MD-7005191-0-0			
6	INDICATOR LIGHT BOARD ASSY	D-IA-5403833-0-0			
7	ETCH BOARD LIGHTS(PDP-8S)	D-IA-5003835-0-0			
	EPOXY BOARD	1405019-0-0			
	PRINTED CIRCUIT LAYOUT	5003835-0-2			
8	GLASS SUPPORT	D-IA-7405412-0-0			
9	WIRING CASTING ASS'Y (4K)	D-AD-7005285-0-0			
	WIRING CASTING ASS'Y (4K)(P.L.)	A-PL-7005285-0-0			
	WIRING CASTING REWORK	E-MD-7405413-0-0			
	WIRED ASSY CASTING (C.P.)	A-CP-8S-0-31			
	WIRE LIST PDP-8S (8K)	K-WL-8S-0-21			
10	WIRING CASTING ASSY(8K)	D-AD-7005327-0-0			
	WIRING CASTING ASS'Y(8K)(P.L.)	A-PL-7005327-0-0			
	WIRING CASTING REWORK	E-MD-7405413-0-0			
	WIRED ASSY CASTING (C.P.)	A-CP-8S-0-31			
	WIRE LIST PDP-8S (8K)	K-WL-8S-0-21			
11	MTG BAR ASSY (10 CONN. BLOCKS)	D-AC-7005099-0-0			
	MTG BAR ASS'Y (10 CONN BLOCKS)	A-PL-7005099-0-0			
12	MTG BAR STD	D-AD-7005103-0-0			
	MTG BAR	D-MD-7405035-0-0			
13	CAPACITOR HOUSING ASSY	E-AD-7005190-0-0			
	CAPACITOR HOUSING ASS'Y (PL)	A-PL-7005190-0-0			
	JUMPER (BLK)	D-IA-7405360-2-0			
	JUMPER (BLK)	D-IA-7405360-4-0			
	JUMPER (RED)	D-IA-7405360-5-0			
	JUMPER (BLU)	D-IA-7405360-1-0			
	CONN WIRE (BLU)	D-IA-7405359-2-0			
	CONN WIRE (BLK)	D-IA-7405359-1-0			
	CONN WIRE (RED)	D-IA-7405359-3-0			
	CAP CONTAINER	D-MD-7405407-0-0			
	JUMPER (BLU)	D-IA-7405360-3-0			
14	CAP, HOLD-DOWN BRKT.	C-IA-7405408-0-0			

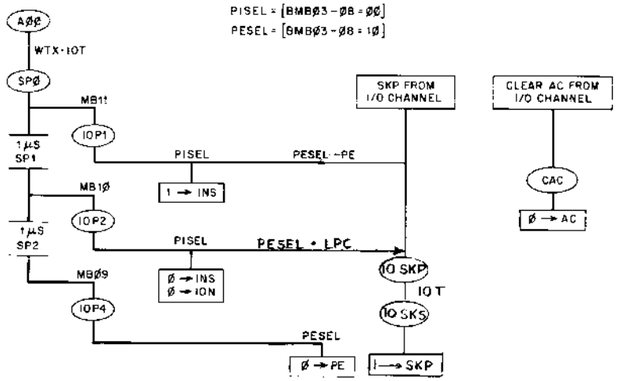
MECHANICAL			DEPT. USAGE		
FIND NO	DESCRIPTION	PART NO.	PROD	CUST	F/C
15	REAR PANEL ASSY 50 & 60 CYCLE	D-AD-7005193-0-0			
	REAR PANEL ASSY 50 & 60 CYCLE	A-PL-7005193-0-0			
	SUPPORT GUSSET (L.H.)	C-MD-7405395-1-0			
	PIVOT BRKT	B-MD-7405393-0-0			
	TOP COVER STOP	B-MD-7405392-0-0			
	SUPPORT GUSSET (R.H.)	C-MD-7405395-2-0			
	FAN SCREEN	C-MD-7405388-0-0			
	MARG CHK SCRTCHCALS	C-SS-10801			
	PROTECTION COVER	B-MD-7404508-0-0			
	(TRANSFORMER CHK LABEL (50 CYCLES ONLY)	SS-100105-1			
	INPUT POWER LABEL (60 CYCLES)	SS-100104-1			
16	REAR PANEL	E-IA-7405386-0-0			
17	FAN MTG PLATE	C-IA-7405425-0-0			
18	COMPONENT MTG PLATE	D-IA-7405391-0-0			
19	SPACER, FAN	C-IA-7405426-0-0			
20	QUICK RELEASE MTG PLATE	C-IA-7405388-0-0			
21	SIDE SHROUD	D-IA-7405394-0-0			
	SIDE SHROUD(L.H.)	D-IA-7405394-1-0			
	SIDE SHROUD(R.H.)	D-IA-7405394-2-0			
22	AIR BAFFLE	E-IA-7405399-0-0			
23	MTG BRKT, REAR PANEL	C-IA-7405400-0-0			
24	POWER WIRING HARNESS	D-IA-7405648-0-0			
25	TELETYPE CONTROL PT08-A	D-UA-PT08-A-0			
	TELETYPE CONTROL PT08-A (PL)	A-PL-PT08-A-0			
	1943 MTG PANEL LABEL	SS-100153-1			
	LEFT END PANEL	C-MD-1943-0-1-0-2			
26	PT08 WIRED ASSEMBLY	D-AD-7005304-0-0			
	PT08 WIRED ASSEMBLY (PL)	A-PL-7005304-0-0			
	1943 FRAME CAST REWORK	C-MD-7405531-0-0			
27	CONN CABLE 8S-PT08	C-IA-7405600-1-0			
28	POWER CORD PT08-A TO POP8S	C-AD-7005209-1-0			
	POWER CORD PT08-A TO PDP-8S (PL)	A-PL-7005209-0-0			
29	CABLE 4915 TO W870	D-AD-7005288-1-0			
	CABLE 4915 TO W870 (PL)	A-PL-7005288-0-0			
30	ASR TTY WITH PT08-A OPTION	D-AD-7005043-0-0			
	ASR TTY WITH PT08-A OPTION (PL)	A-PL-7005043-0-0			
	ASR 33 TELETYPE STAND (REWORK)	C-MD-7405529-0-0			
	PROTECTION PLATE ASR 33	1405292-0-0			
31	4K MEMORY	NO # AVAILABLE			
31	H281 MEMORY (8K)	D-SC-3005120-0-0			

ELECTRICAL					
FIND NO	DESCRIPTION	PART NO.	PROD	CUST	F/C
1	TABLE MODEL PDP-8S(4K)	A-WL-8S-0			
	WIRING CASTING ASS'Y	D-AD-7005285-0-0			
	WIRING CASTING ASS'Y	A-PL-7005285-0-0			
	WIRE LIST PDP-8S	K-WL-8S-0-8			
	MEMORY BLOCK DIAGRAM	D-BS-8S-0-4			
	PDP8S BLOCK DIAGRAM	D-BD-8S-0-2			
	KEYS SWITCHES TIMING DIAGRAM	D-TD-8S-0-1			
	TIMING DIAGRAM	D-TD-8S-0-3			
	MB	D-BS-8S-0-9			
	ACCNT	D-BS-8S-0-10			
	BTG	D-BS-8S-0-11			
	MA	D-BS-8S-0-12			
	WORD TIME GEN.	D-BS-8S-0-13			
	ADDER	D-BS-8S-0-14			
	CONTROL	D-BS-8S-0-15			
	IR	D-BS-8S-0-16			
	I/O	D-BS-8S-0-17			
	MEMORY	D-BS-8S-0-18			
	P.C. REGISTER	D-BS-8S-0-19			
	ACCUMULATOR	D-BS-8S-0-20			
	IO CABLE SCHEDULES	D-CL-8S-0-5			
	MEMORY BLOCK MU(4K)	D-MU-8S-0-26			
	MEMORY BLOCK MU(4K)	A-PL-8S-0-26			
1	TABLE MODEL PDP-8S(8K)	A-WL-8S-0			
	WIRING CASTING ASSY	D-AD-7005327-0-0			
	WIRE LIST PDP-8S(8K)	K-WL-8S-0-21			
	MEMORY BLOCK DIAGRAM(8K)	D-BS-8S-0-23			
	PDP-8S BLOCK DIAGRAM	D-BD-8S-0-2			
	KEYS SWITCHES TIMING DIAGRAM	D-TD-8S-0-1			
	TIMING DIAGRAM	D-TD-8S-0-3			
	MB	D-BS-8S-0-9			
	ACCNT	D-BS-8S-0-10			
	BTG	D-BS-8S-0-11			
	MA	D-BS-8S-0-12			
	WORD TIME GEN	D-BS-8S-0-13			
	ADDER	D-BS-8S-0-14			
	CONTROL	D-BS-8S-0-15			
	IR	D-BS-8S-0-16			
	I/O	D-BS-8S-0-17			
	MEMORY (8K)	D-BS-8S-0-22			
	P.C. REGISTER	D-BS-8S-0-18			
	ACCUMULATOR	D-BS-8S-0-20			
	MEMORY BLOCK MU(8K)	D-MU-8S-0-25			
	MEMORY BLOCK MU(8K)	A-PL-8S-0-25			
	IO CABLE SCHEDULES				
	CABLE INTERFACE PDP-8/S	D-IC-8S-0-32			
15	REAR PANEL ASS'Y (SH 3 OF 3)	C-AD-7005193-0-0			
25	TELETYPE CONTROL PT08-A	A-WL-PT08-A-0			
	(MTG IN TELETYPE)				
	TELETYPE CONTROL PT08 LOGIC	D-BS-PT08-A-1			
	MODULE LOCATION TYPE PT08	D-MD-PT08-A-2			
	MODULE LOCATION TYPE PT08	A-PL-PT08-A-2			
	WIRING LIST TYPE PT08	A-WL-PT08-A-3			
	PT08-A WIRED ASSEMBLY	C-AD-7005304-0-0			
	TELETYPE MOD (ASR-33)	D-IC-7605185-0-0			
31	4K MEMORY	NO # AVAILABLE			
31	H281 MEMORY (8K MEMORY)	D-SC-3005120-0-0			

MEMORY



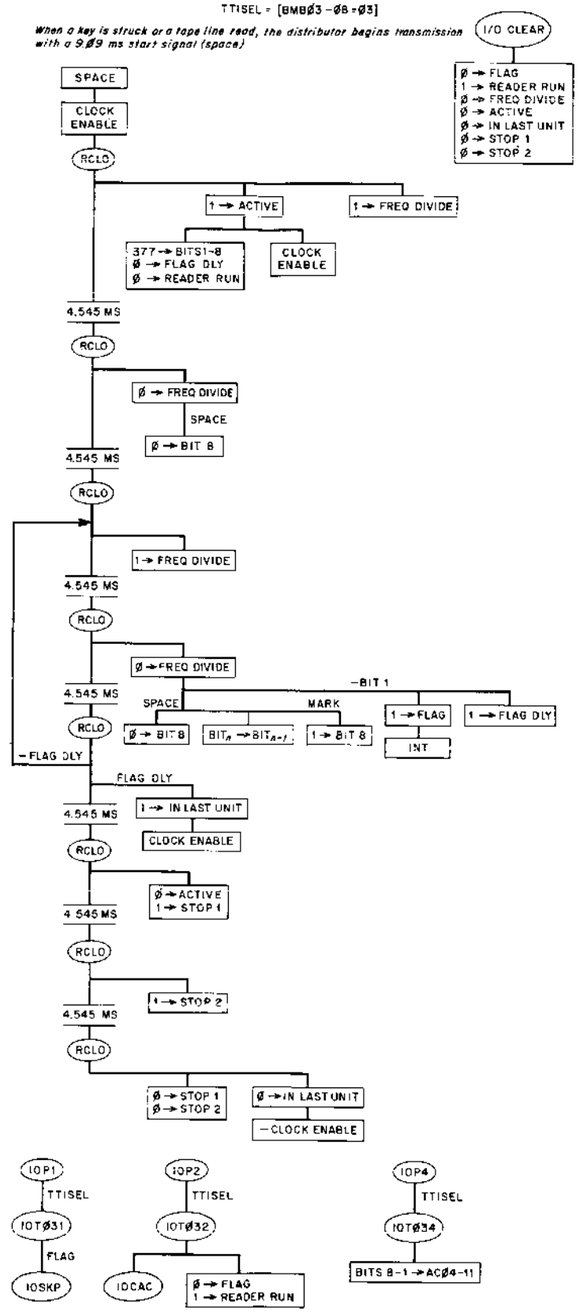
IN-OUT



TTI

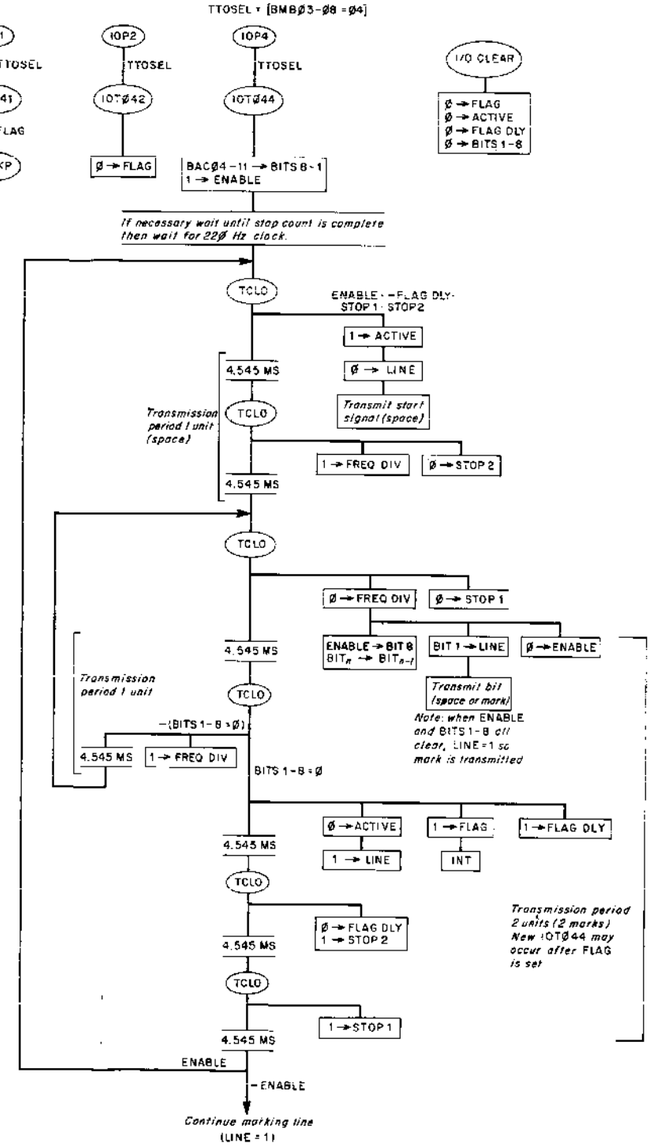
TTISEL = [BMBØ3-ØB=Ø3]

When a key is struck or a tape line read, the distributor begins transmission with a 9.09 ms start signal (space)

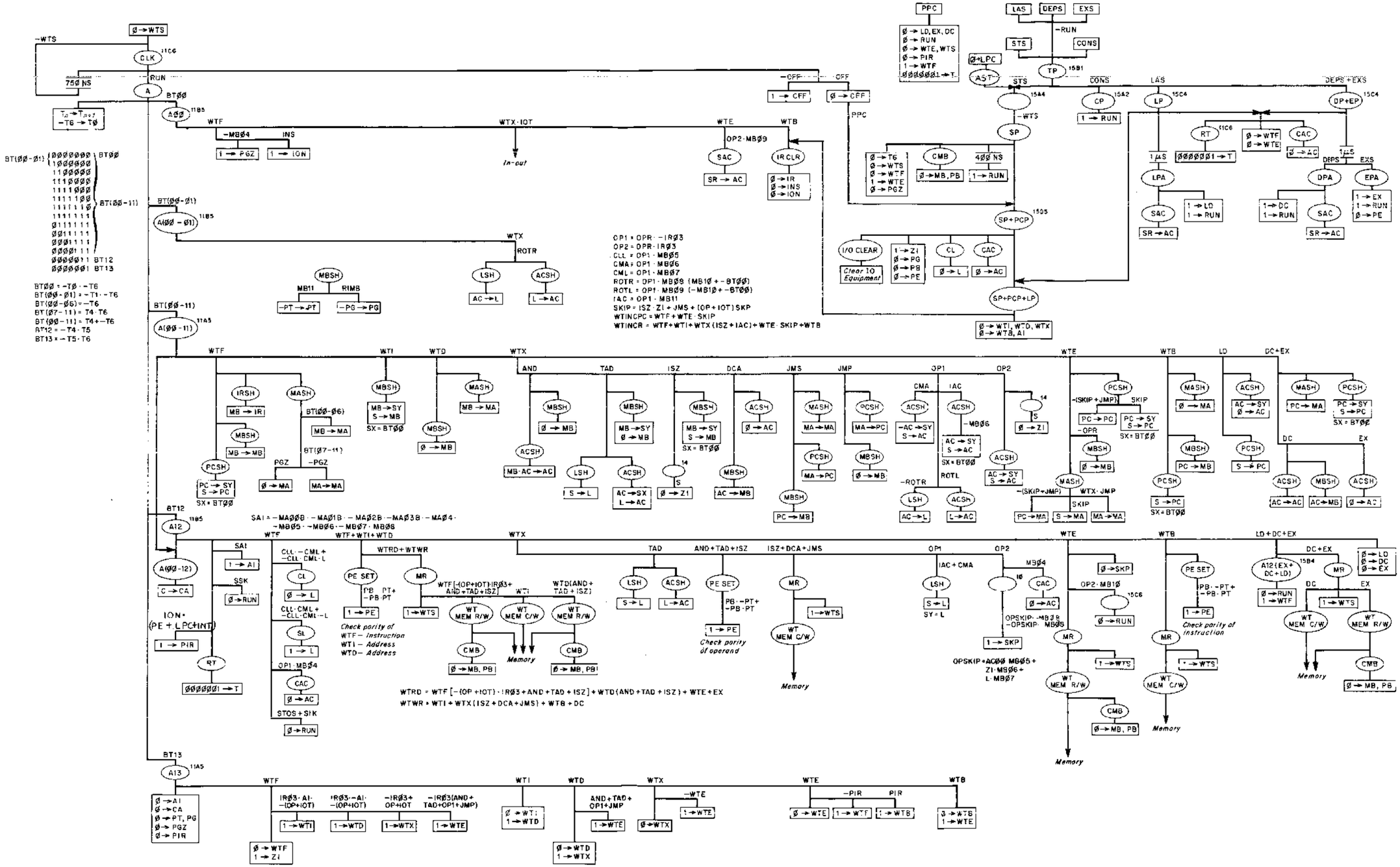


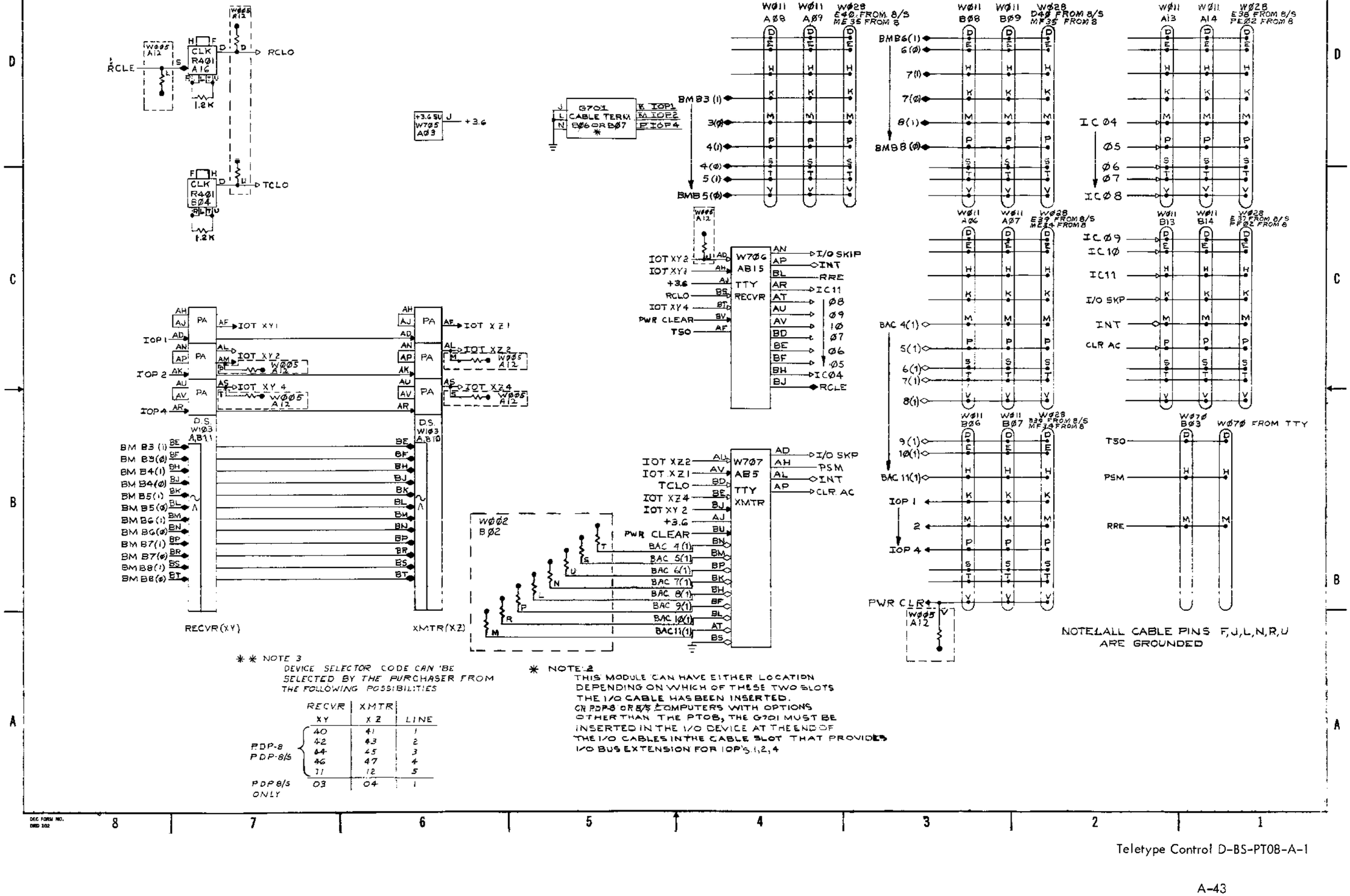
TTO

TTOSEL = [BMBØ3-ØB=Ø4]



Memory and In-out Flow D-FD-8S-0-29


Ø → WTS
CLK
RUN
750 NS
A
BTØØ
AØØ
WTF
WTX·IOT
WTE
WTB
OP2·MBØ9
SAC
SR → AC
IR CLR
Ø → IR
Ø → INS
Ø → ION
1 → PGZ
1 → ION
In-out
-CFF
1 → CFF
Ø → CFF
PPC
Ø → LD, EX, DC
Ø → RUN
Ø → WTE, WTS
Ø → PIR
1 → WTF
Ø → T6
Ø → WTS
Ø → WTF
1 → WTE
Ø → PGZ
CMB
Ø → MB, PB
4ØØ NS
1 → RUN
SP
SP+PCP
SP+PCP+LP
Ø → WT, WTD, WTX
Ø → WTA, AI
I/O CLEAR
Clear IO Equipment
1 → ZI
Ø → PG
Ø → PB
Ø → PE
CL
Ø → L
CAC
Ø → AC
LAS
DEPS
EXS
STS
CONS
-RUN
Ø → LPC
AST
TP
CP
1 → RUN
LP
DP+EP
LPA
SAC
SR → AC
1 → LD
1 → RUN
DPA
EPA
1 → DC
1 → RUN
1 → EX
1 → RUN
Ø → PE
RT
Ø → WTF
Ø → WTE
Ø → AC
ØØØØØØ1 → T
1 μS
DEPS
EXS
BT(ØØ-Ø1)
BTØØ
BT(ØØ-11)
ØØØØØØØØ
1ØØØØØØØ
11ØØØØØØ
111ØØØØØ
1111ØØØØ
11111ØØØ
111111ØØ
1111111Ø
11111111
Ø1111111
ØØ111111
ØØØ11111
ØØØØ1111
ØØØØØ111
ØØØØØØ11 BT12
ØØØØØØØ1 BT13
BTØØ = -TØ · -T6
BT(ØØ-Ø1) = -T1 · -T6
BT(ØØ-Ø6) = -T6
BT(Ø7-11) = T4·T6
BT(ØØ-11) = T4+-T6
BT12 = -T4·T5
BT13 = -T5·T6
A(ØØ-Ø1)
A(ØØ-11)
WTX
ROTR
MBSH
MB11
RIMB
-PT → PT
-PG → PG
LSH
ACSH
AC → L
L → AC
OP1 = OPR · -IRØ3
OP2 = OPR · IRØ3
CLL = OP1 · MBØ5
CMA = OP1 · MBØ6
CML = OP1 · MBØ7
ROTR = OP1 · MBØ8 (MB1Ø + -BTØØ)
ROTL = OP1 · MBØ9 (-MB1Ø + -BTØØ)
IAC = OP1 · MB11
SKIP = ISZ · ZI + JMS + (OP + IOT) SKP
WTINCPC = WTF + WTE · SKIP
WTINCR = WTF + WTI + WTX (ISZ + IAC) + WTE · SKIP + WTB
WTF
WTI
WTD
WTX
AND
TAD
ISZ
DCA
JMS
JMP
OP1
OP2
WTE
WTB
LD
DC+EX
IRSH
MASH
MB → IR
MBSH
MB → MB
PCSH
PC → SY
S → PC
SX = BTØØ
BT(ØØ-Ø6)
MB → MA
BT(Ø7-11)
PGZ
-PGZ
Ø → MA
MA → MA
MB → SY
S → MB
Ø → MB
MB → MA
ACSH
MB·AC → AC
! S → L
AC → SX
L → AC
14
S
Ø → ZI
AC → MB
Ø → AC
MA → MA
MA → PC
PC → MB
-AC → SY
S → AC
CMA
IAC
-MBØ6
AC → SY
S → AC
SX = BTØØ
ROTL
-ROTR
AC → L
L → AC
-(SKIP+JMP)
SKIP
PC → PC
PC → SY
S → PC
-OPR
WTX·JMP
PC → MA
S → MA
MA → MA
Ø → MA
AC → SY
Ø → AC
PC → MB
S → PC
AC → AC
AC → MB
Ø → AC
PC → MA
DC
EX
Ø → LD
Ø → DC
Ø → EX
BT12
A12
A(ØØ-12)
C → CA
SSK
Ø → RUN
ION·(PE + LPCHNT)
1 → PIR
RT
ØØØØØØØ1 → T
SAI
1 → AI
CLL·-CML+-CLL·CML·-L
CL
Ø → L
CLL·CML+-CLL·CML·-L
SL
1 → L
OP1·MBØ4
CAC
Ø → AC
STOS+SIK
Ø → RUN
WTF+WTI+WTD
WTRD+WTWR
PE SET
PB·-PT+-PB·PT
1 → PE
MR
1 → WTS
Check parity of WTF – Instruction
WTI – Address
WTD – Address
WT MEM R/W
WT MEM C/W
CMB
Ø → MB, PB
Memory
WTRD = WTF [-(OP+IOT)·IRØ3+AND+TAD+ISZ] + WTD(AND+TAD+ISZ) + WTE+EX
WTWR = WTI + WTX(ISZ+DCA+JMS) + WTB + DC
TAD
AND+TAD+ISZ
ISZ+DCA+JMS
OP1
OP2
IAC+CMA
LSH
S → L
SY = L
MBØ4
16
CAC
Ø → AC
1 → SKP
OPSKIP·-MBØ8·-OPSKIP·MBØ9
OPSKIP·ACØØ MBØ5+ZI·MBØ6+L·MBØ7
Ø → SKP
OP2·MB1Ø
15C6
Ø → RUN
PB·-PT+-PB·PT
Check parity of instruction
LD+DC+EX
DC+EX
A12(EX+DC+LD)
15B4
Ø → RUN
1 → WTF
Ø → LD
Ø → DC
Ø → EX
SAI = -MAØØ8 · -MAØ1B · -MAØ2B · -MAØ38 · -MAØ4 · -MBØ5 · -MBØ6 · -MBØ7 · MBØ8
A13
BT13
Ø → AI
Ø → CA
Ø → PT, PG
Ø → PGZ
Ø → PIR
-IRØ3·AI·-(OP+IOT)
1 → WTI
Ø → WTF
1 → ZI
-IRØ3·-AI·-(OP+IOT)
1 → WTD
-IRØ3+OP+IOT
1 → WTX
-IRØ3(AND+TAD+OP1+JMP)
1 → WTE
Ø → WTI
1 → WTD
Ø → WTD
1 → WTX
AND+TAD+OP1+JMP
1 → WTE
-WTE
Ø → WTX
-PIR
PIR
Ø → WTE
1 → WTF
1 → WTB
3 → ATB
1 → WTE



** NOTE 3
DEVICE SELECTOR CODE CAN BE SELECTED BY THE PURCHASER FROM THE FOLLOWING POSSIBILITIES

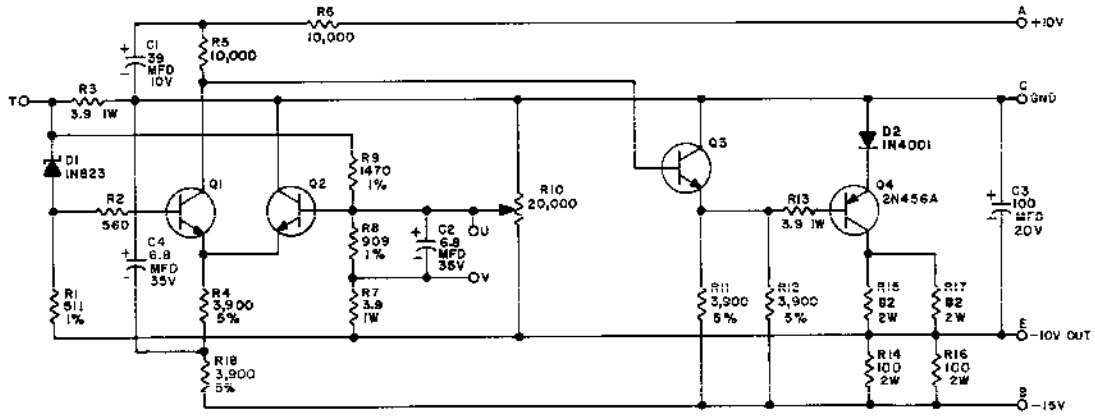
	RECVR XY	XMTR XZ	LINE
PDP-8 PDP-8/S	40	41	1
	42	43	2
	44	45	3
	46	47	4
	11	12	5
PDP 8/S ONLY	03	04	1

* NOTE 2
THIS MODULE CAN HAVE EITHER LOCATION DEPENDING ON WHICH OF THESE TWO SLOTS THE I/O CABLE HAS BEEN INSERTED. ON PDP-8 OR 8/S COMPUTERS WITH OPTIONS OTHER THAN THE PT08, THE G701 MUST BE INSERTED IN THE I/O DEVICE AT THE END OF THE I/O CABLES IN THE CABLE SLOT THAT PROVIDES I/O BUS EXTENSION FOR IOP'S 1,2,4

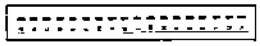
NOTE ALL CABLE PINS F,J,L,N,R,U ARE GROUNDED

DEC FORM NO. DRD 102

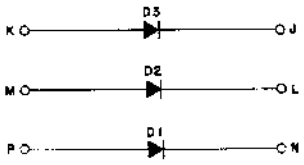
Teletype Control D-BS-PT08-A-1



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
3.9 RESISTORS ARE IRC BWH OR EQUIV.
1% RESISTORS ARE METAL FILM, 100PPM/°C
TRANSISTORS ARE DEC2219
R10 IS A #275P

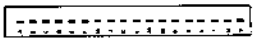


Reference Supply A702-0-1-B

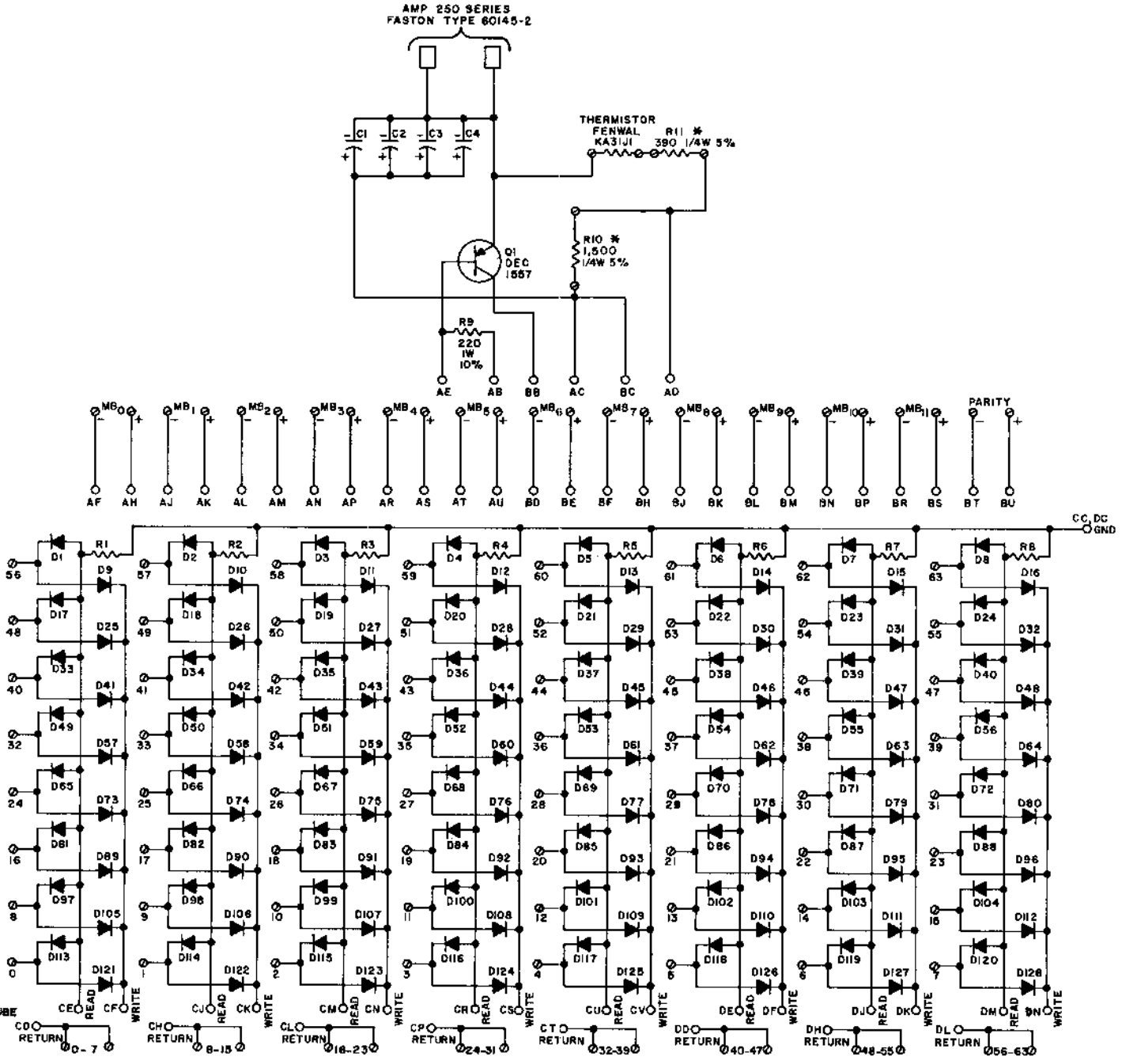


UNLESS OTHERWISE INDICATED:
DIODES ARE D664

USE THE ETCH BOARD OF THE R001

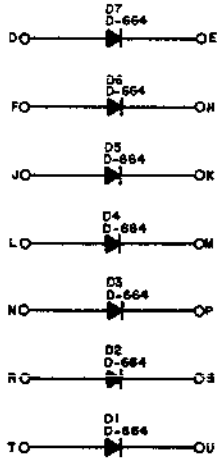


Cable Terminator G701

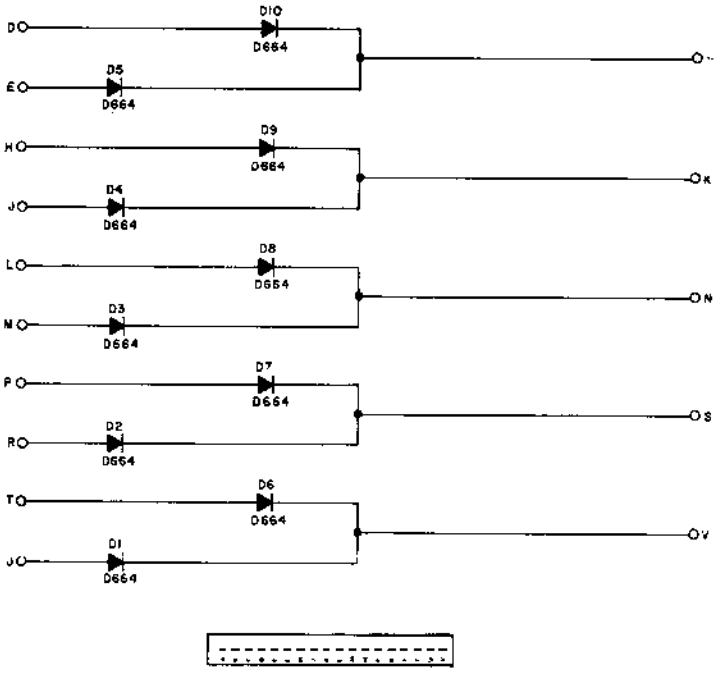


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 4,700; 1/4W; 5%
DIODES ARE D671
CAPACITORS ARE 50MFD 50V GMV
⌀ INDICATES SPLIT LUGS
* VALUES SHOWN ARE FOR FERROXCUBE
R11 IS 100Ω AND R10 IS 2700Ω
FOR EMI

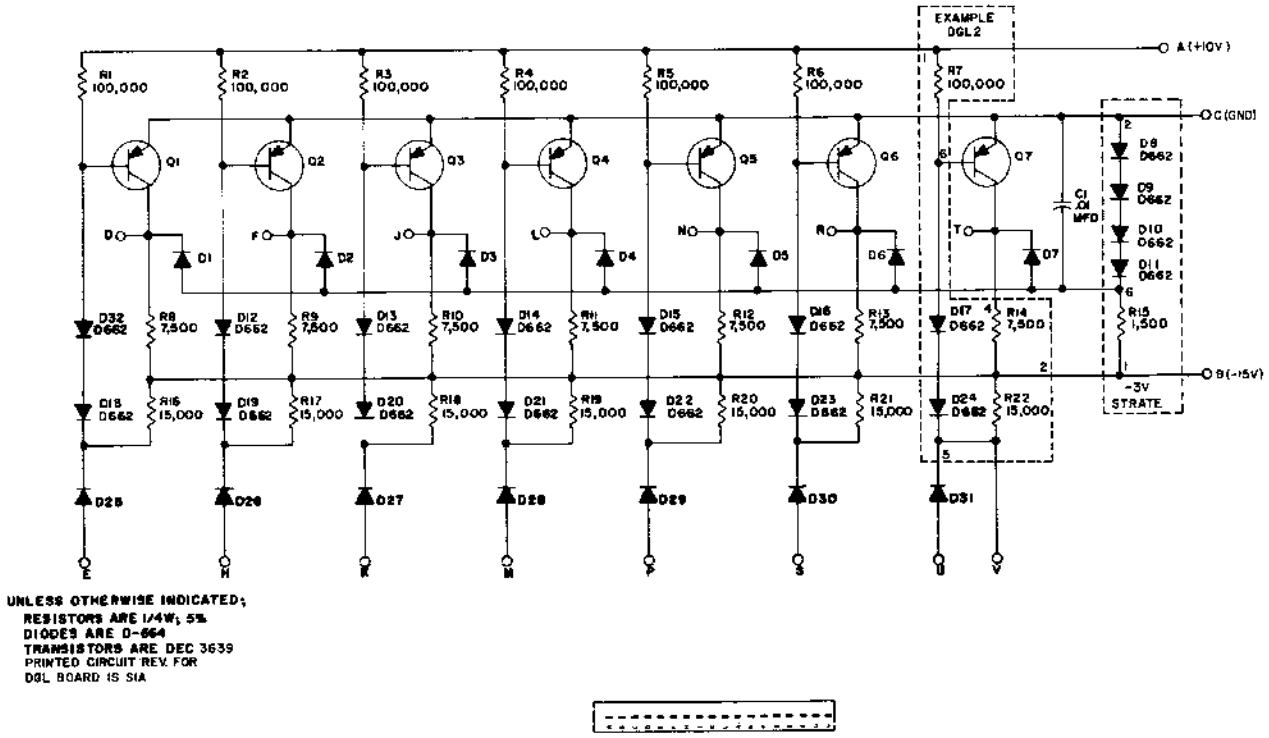
Memory Mounting Board G609



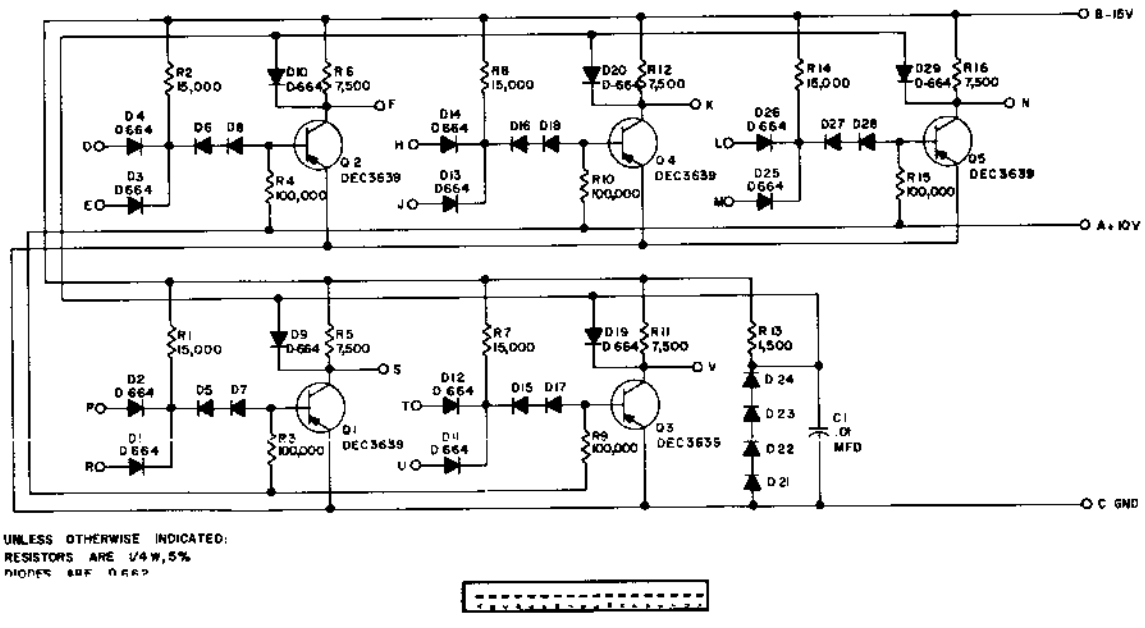
Diode R001-1



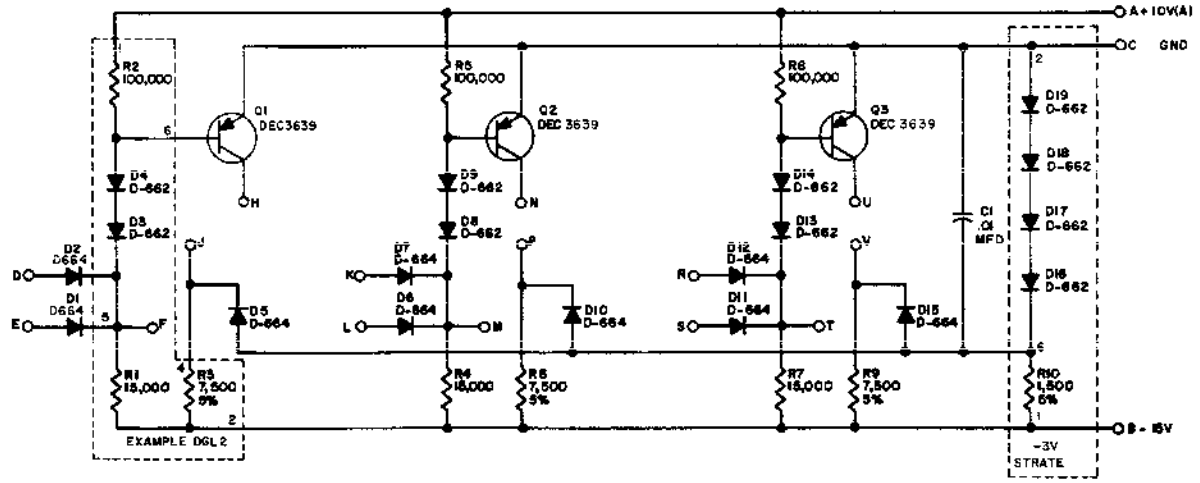
Diode R002-0-1-A



Inverter R107-0-1-E

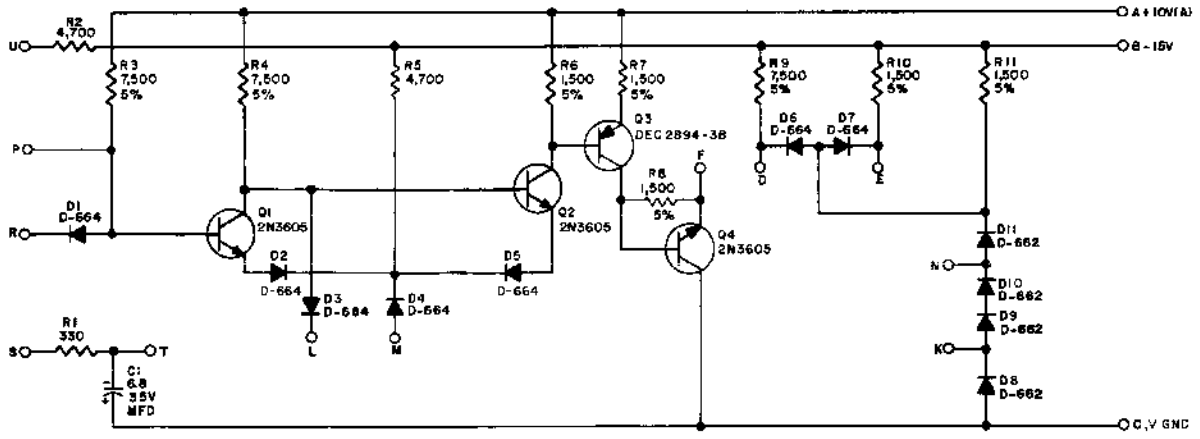


Diode Gate R113



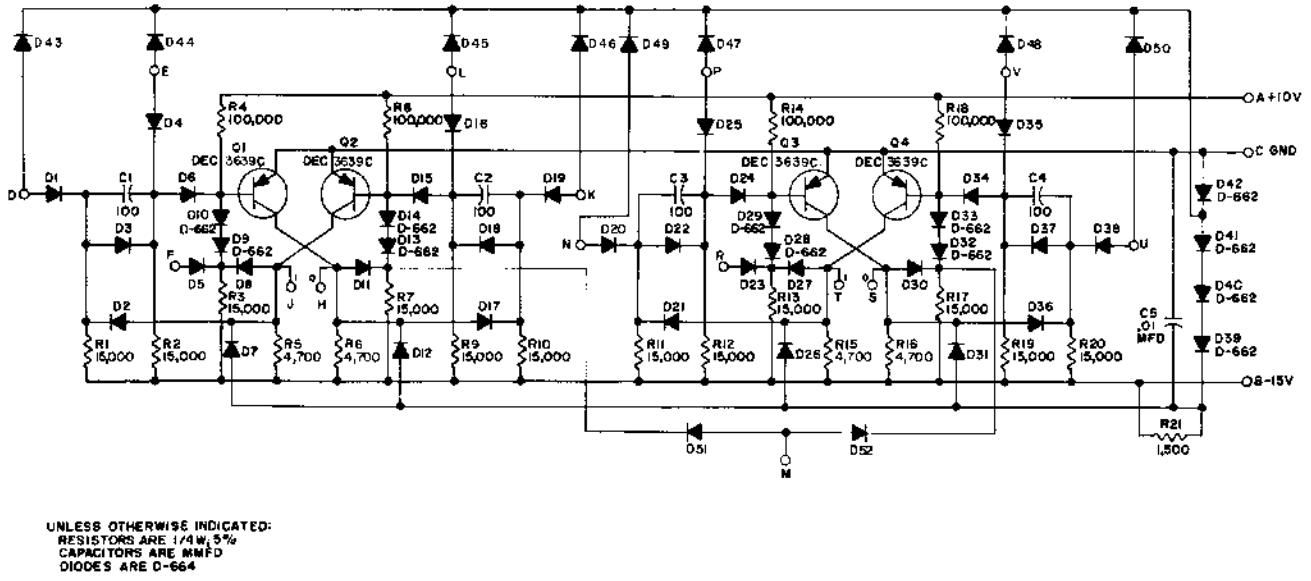
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%.
PRINTED CIRCUIT REV. FOR
DGL BOARD IS 51A

Diode Gate R111-0-1-E

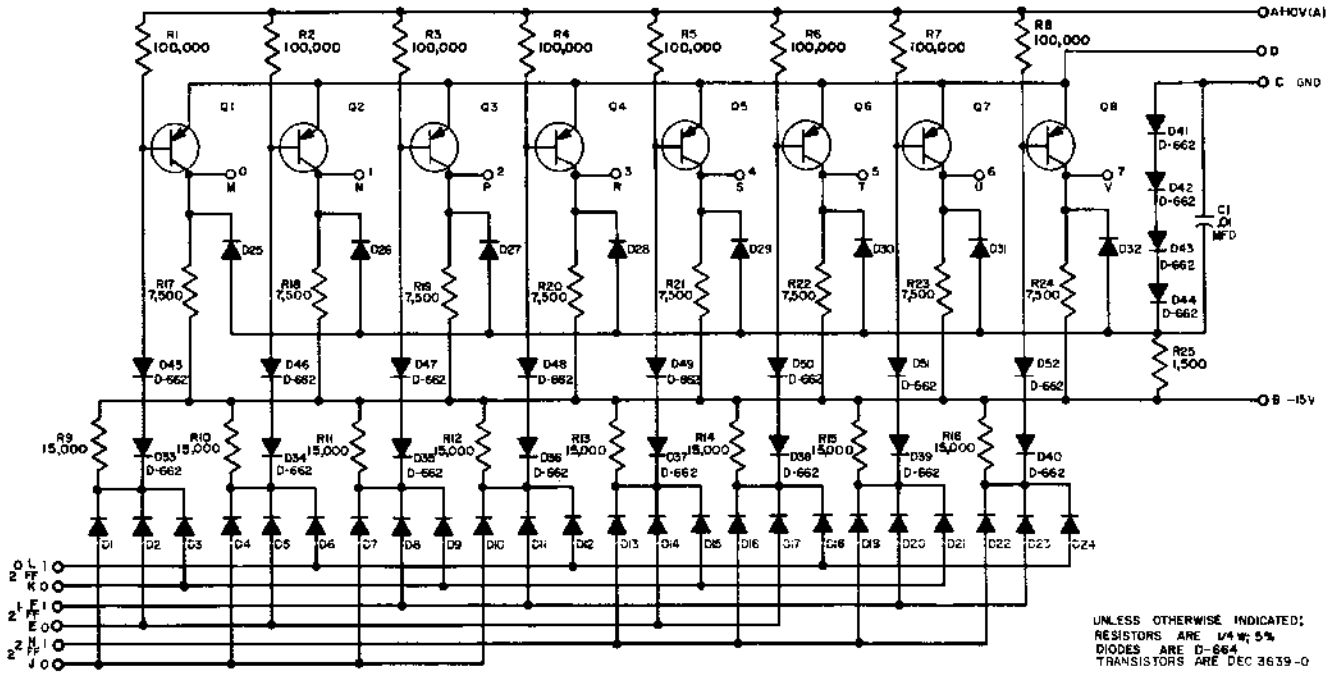


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%

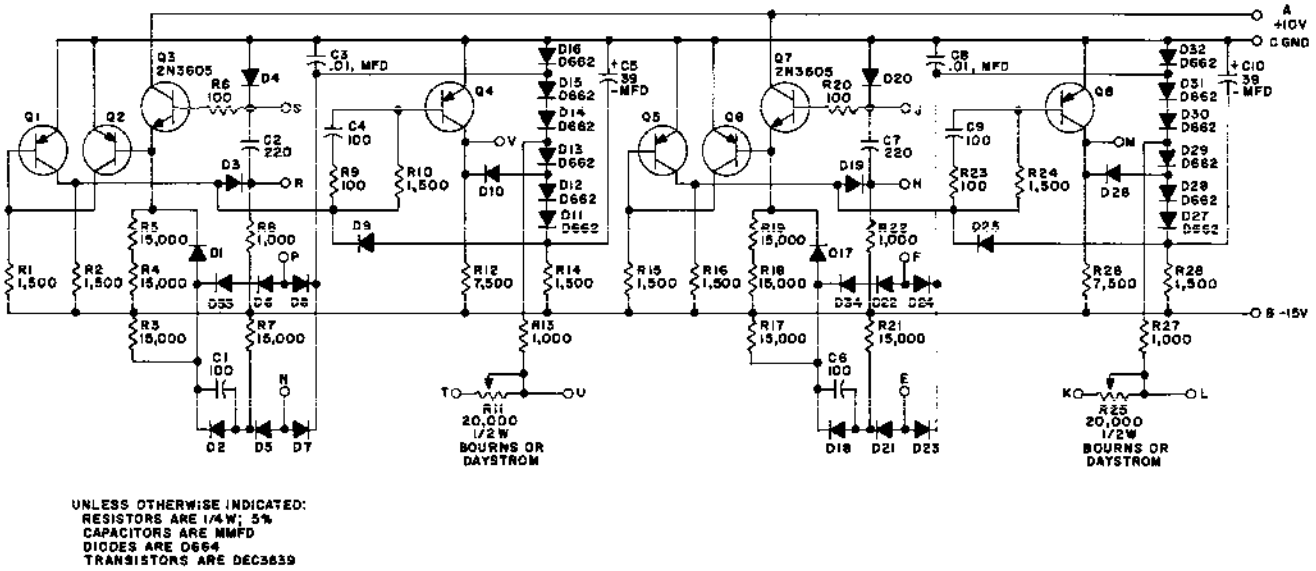
Schmitt Trigger W501-5



Dual Flip-flop R202-4

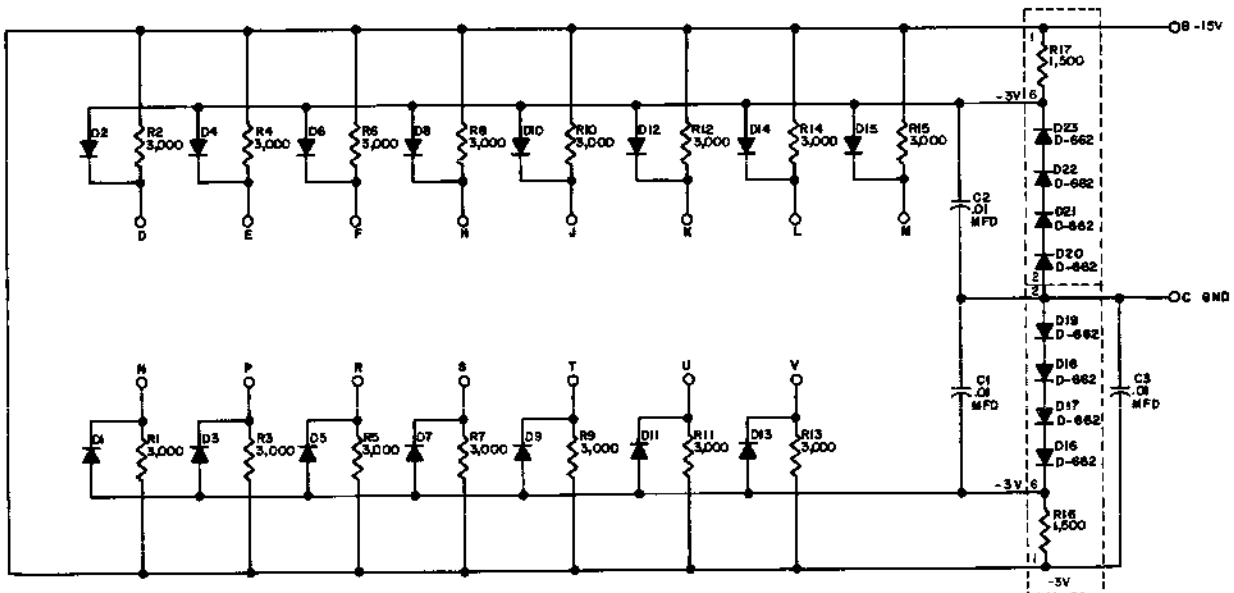


Binary to Octal Decoder R151-3



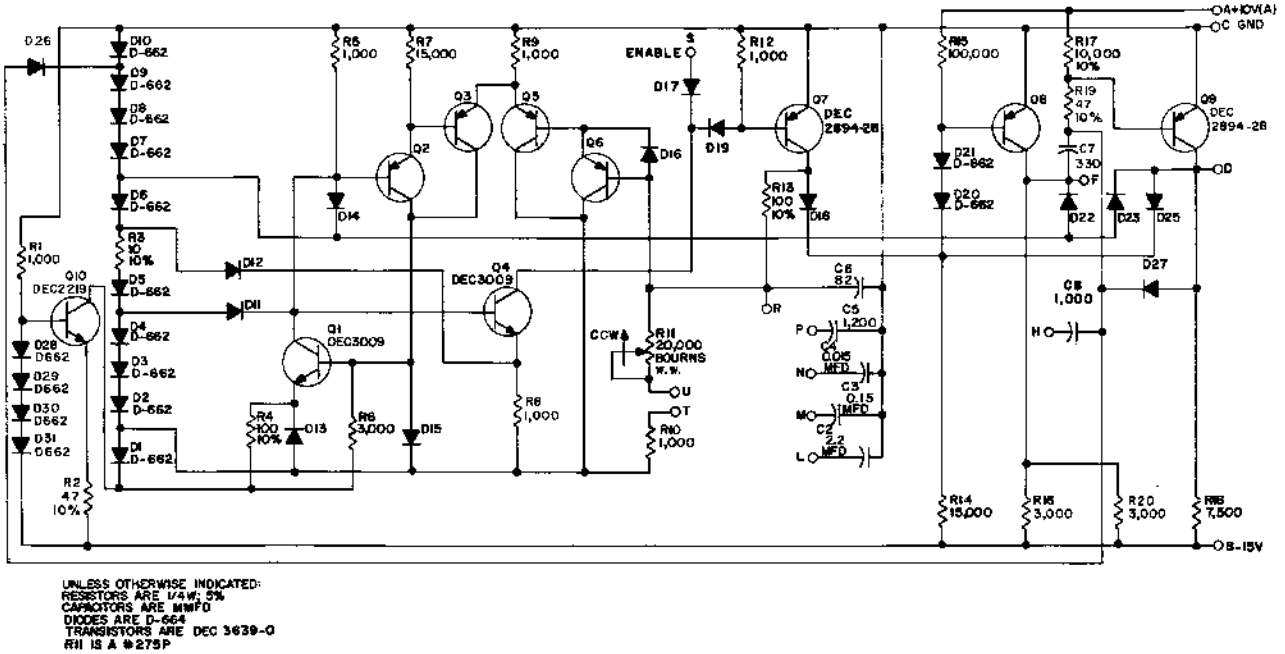
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D664
TRANSISTORS ARE DEC3839

Delay (one shot) R302-9

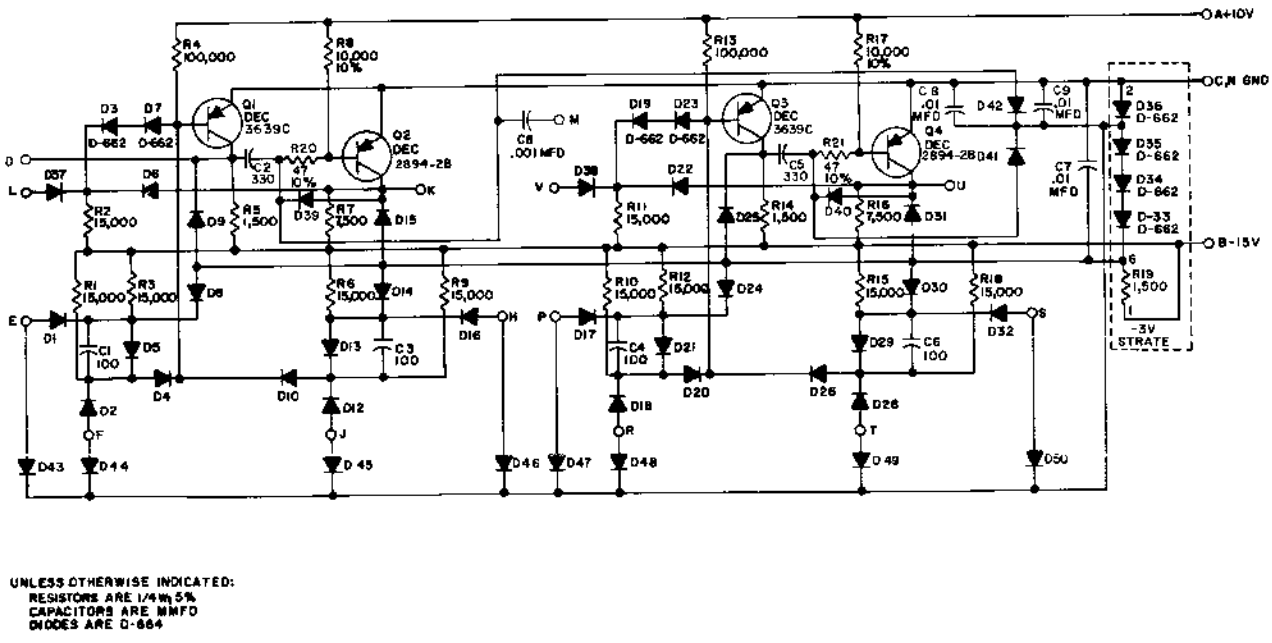


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
DIODES ARE D-664

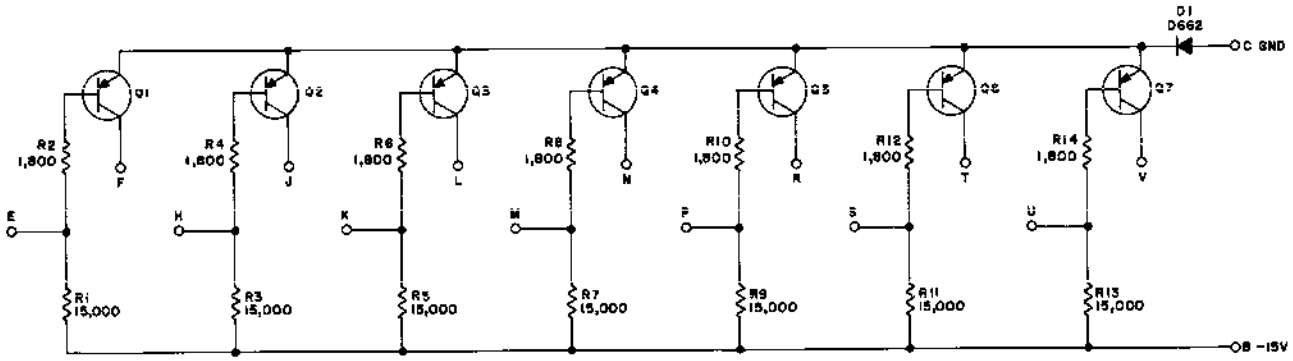
Clamped Loads W005-0-1-B



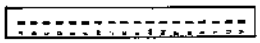
Clock R401-8



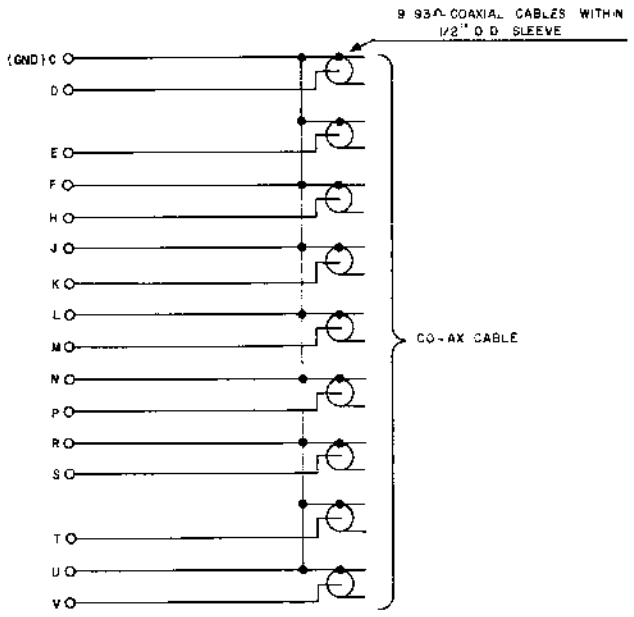
Pulse Amplifier R602-0-1-L

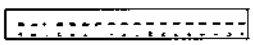


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
TRANSISTORS ARE DEC6534D (DEC86348 MAY BE SUBSTITUTED)

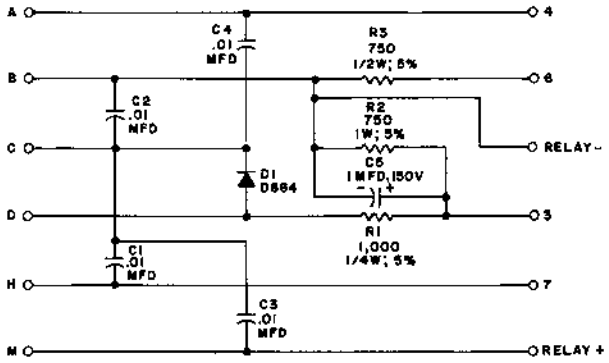


Indicator Driver W050-3

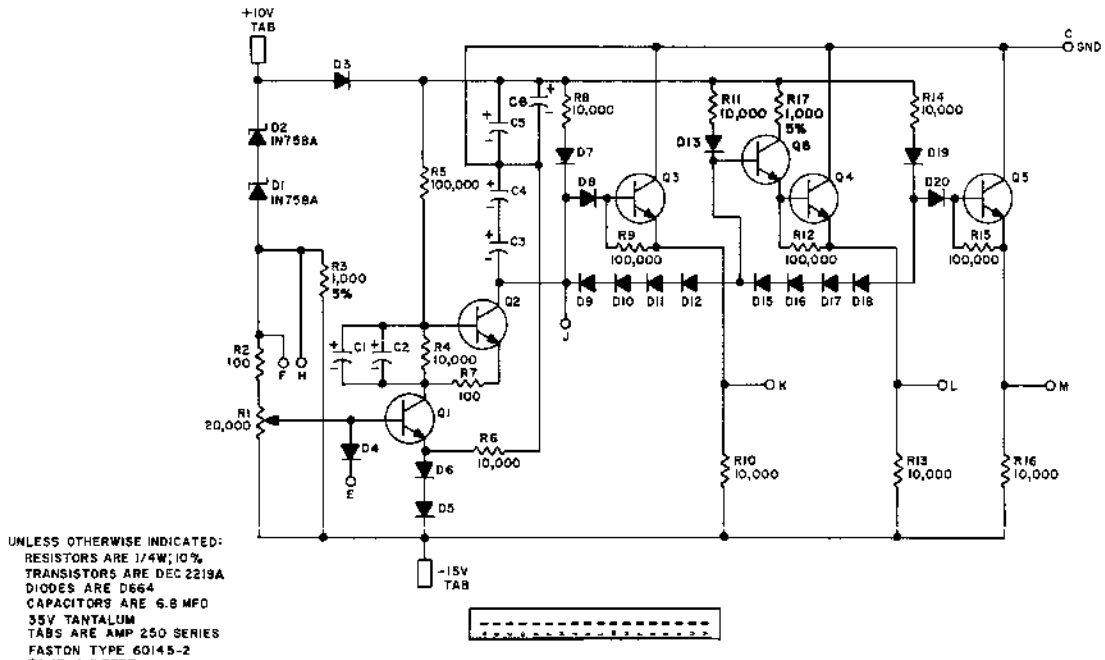




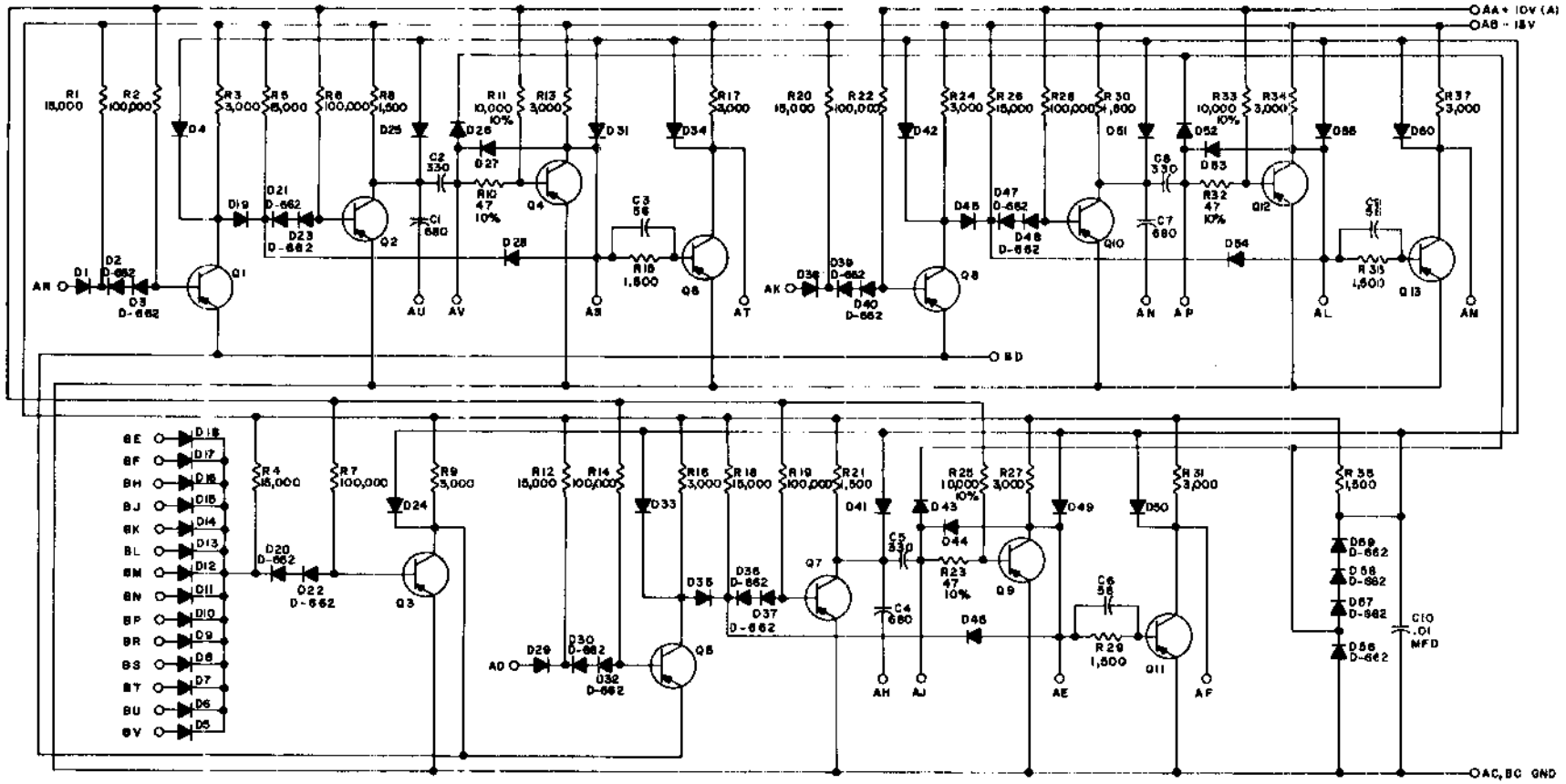
Signal Cable Terminator W011



Teletype Connector W070-2

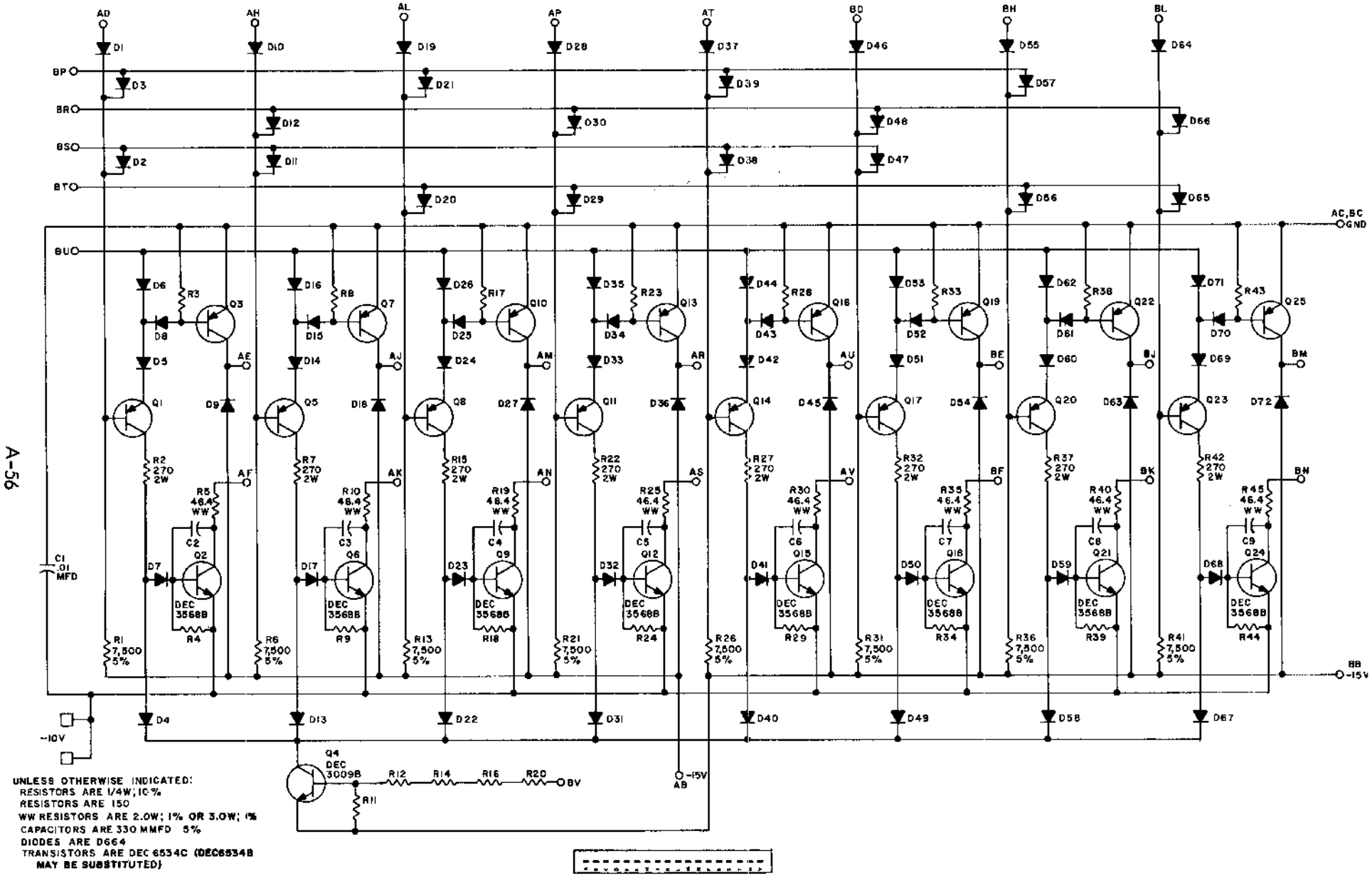


Power Monitor W506-0-1-A



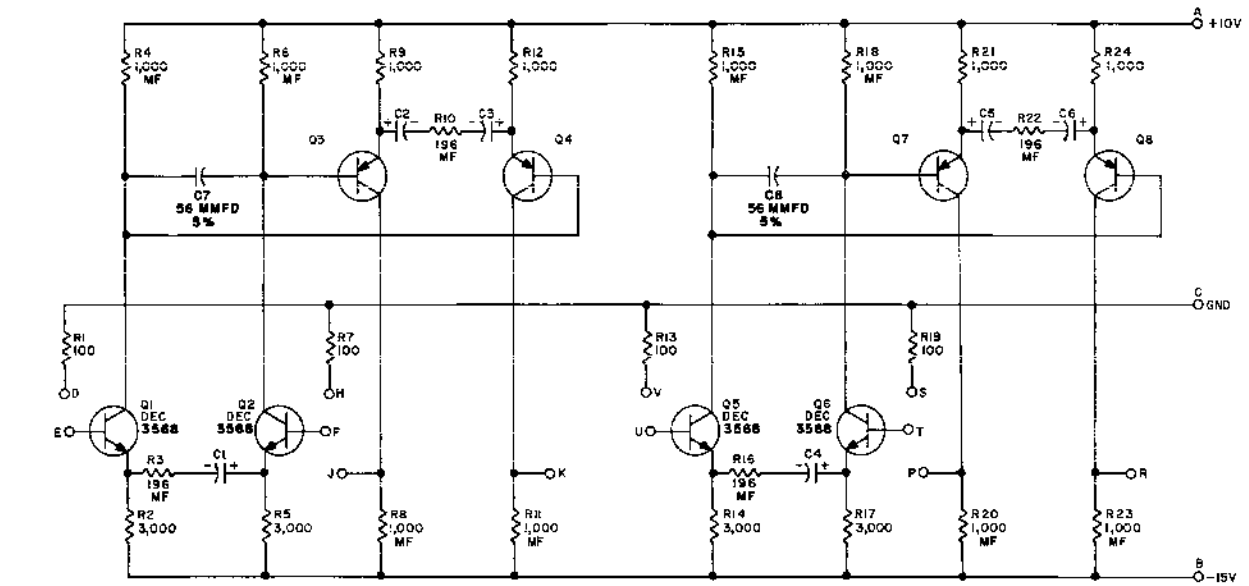
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

Device Selector W103-3



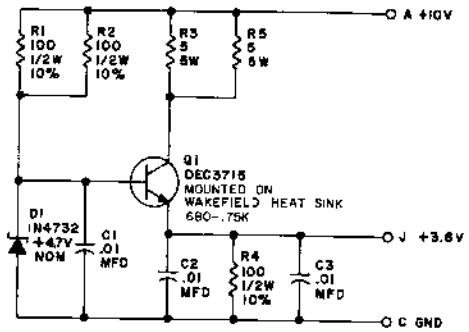
A-56

Decoding Driver W108-0-1-A



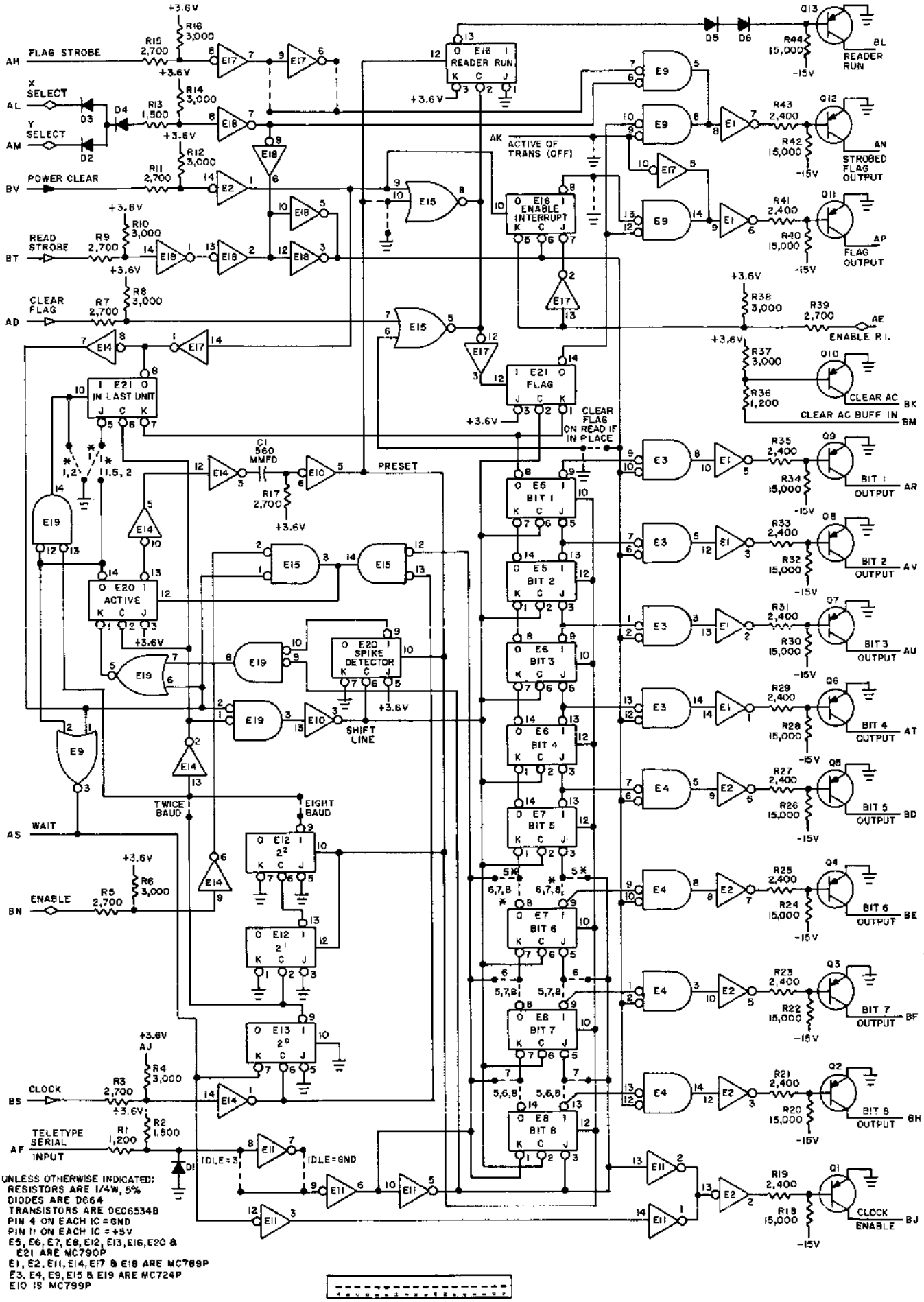
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
MF RESISTORS ARE 1/8W; 1% METAL FILM TO
CAPACITORS ARE 3.9 MFD 10% 10V
TRANSISTORS ARE DEC6534C (DEC6534B MAY BE SUBSTITUTED)

Difference Amplifier W532-0-1-A

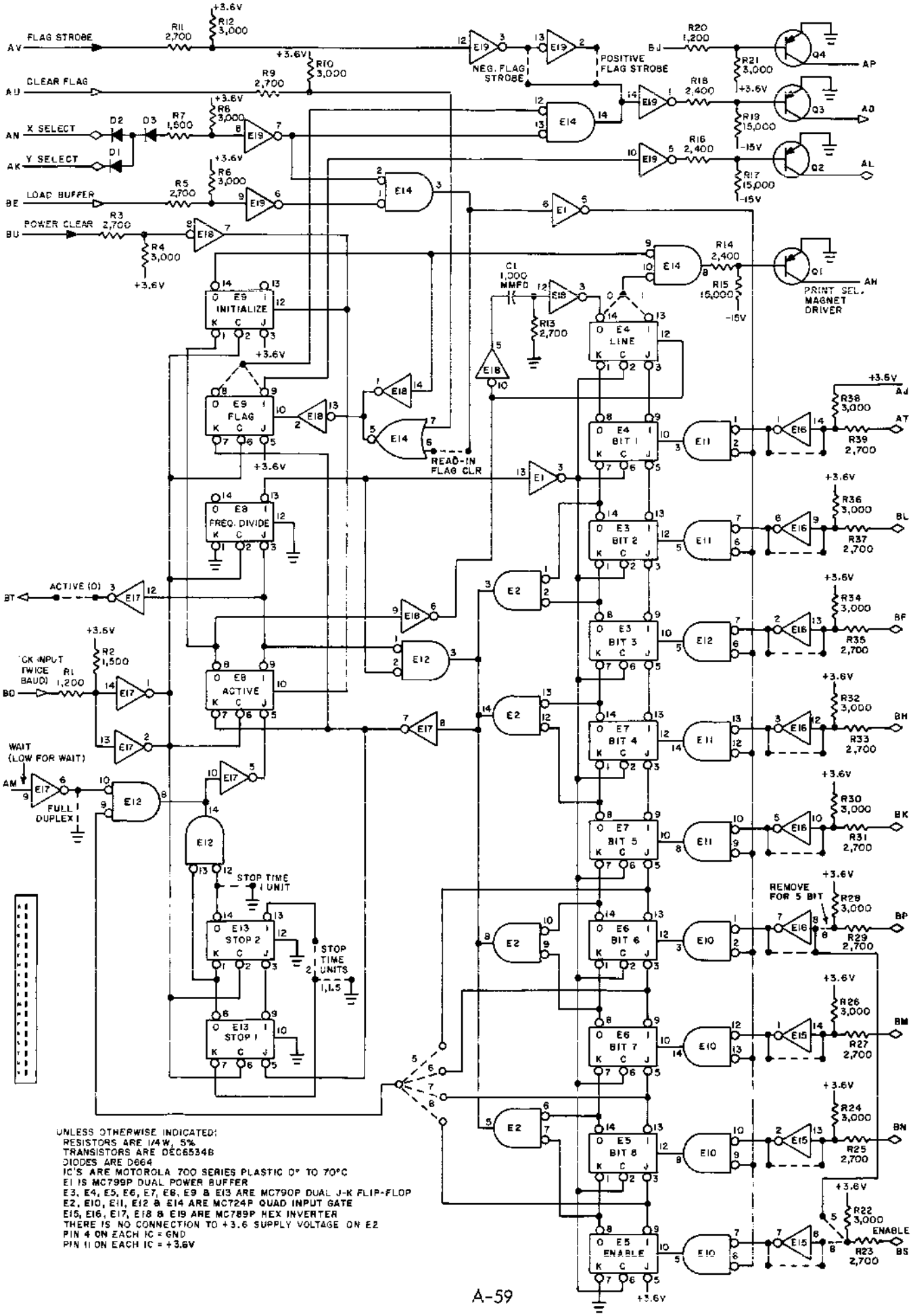


UNLESS OTHERWISE INDICATED:
R3 & R5 ARE WARD LEONARD 5XM5

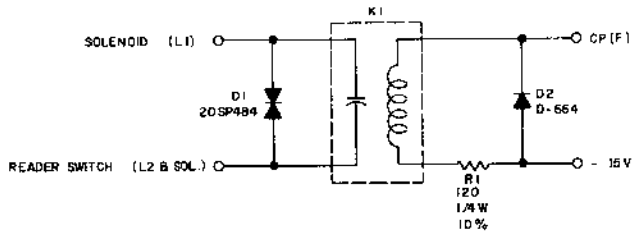
+3.6V Power Supply W705-0-1



Teletype Receiver W705-0-1-C



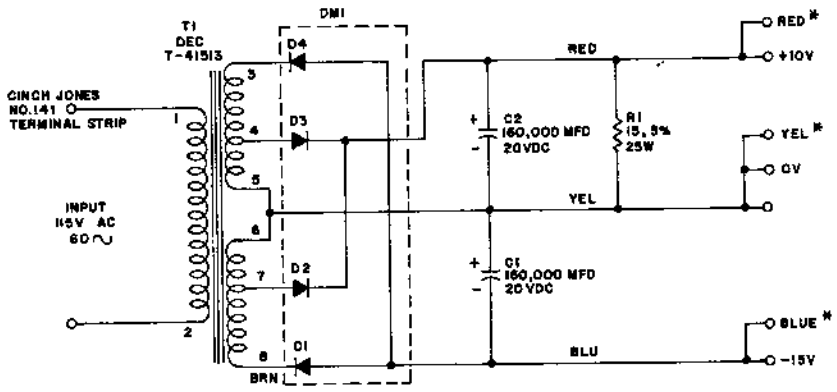
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 5%
TRANSISTORS ARE DEC6534B
DIODES ARE D664
IC'S ARE MOTOROLA 700 SERIES PLASTIC 0° TO 70°C
E1 IS MC799P DUAL POWER BUFFER
E3, E4, E5, E6, E7, E8, E9 & E13 ARE MC790P DUAL J-K FLIP-FLOP
E2, E10, E11, E12 & E14 ARE MC724P QUAD INPUT GATE
E15, E16, E17, E18 & E19 ARE MC789P HEX INVERTER
THERE IS NO CONNECTION TO +3.6 SUPPLY VOLTAGE ON E2
PIN 4 ON EACH IC = GND
PIN 11 ON EACH IC = +3.6V



NOTE

K1 - WHEELOCK RELAY 3002-1D1-12VDC
WITH NO OUTER SHIELD

Teletype Reader Control 4915



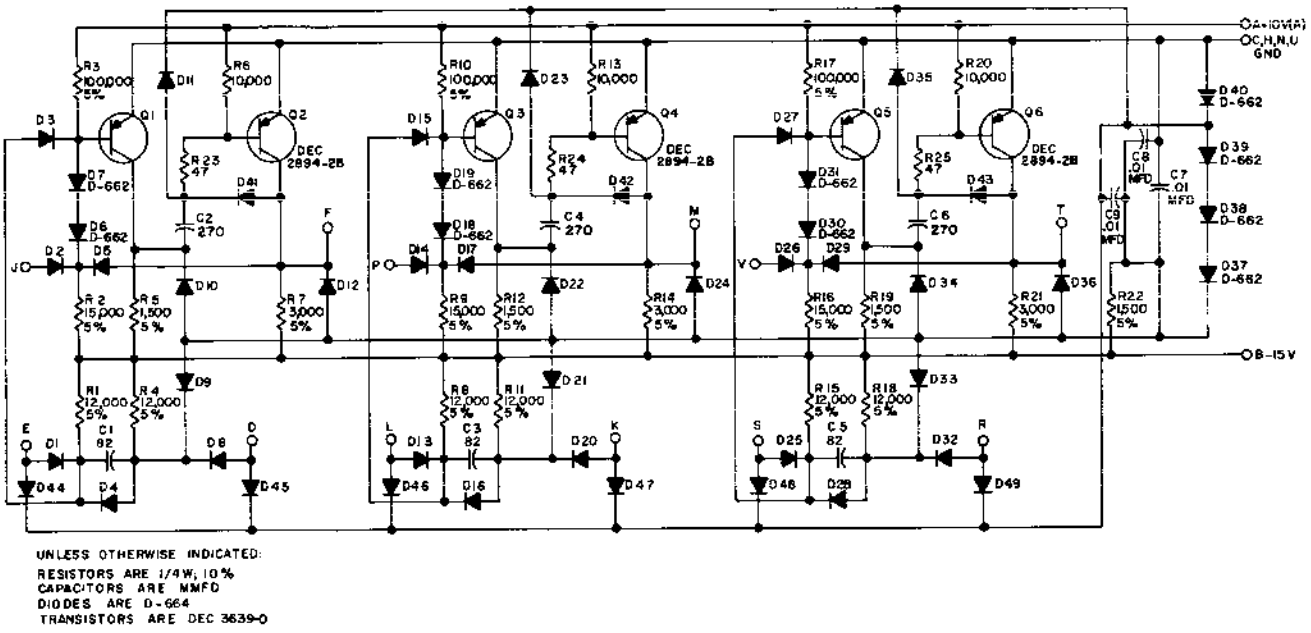
NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN
THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES LOADED	+10V 0 TO 7.0 AMPS -15V 1.0 TO 5.0 AMPS
ONE SIDE LOADED	+10V 0 TO 7.5 AMPS -15V 1.0 TO 6.5 AMPS

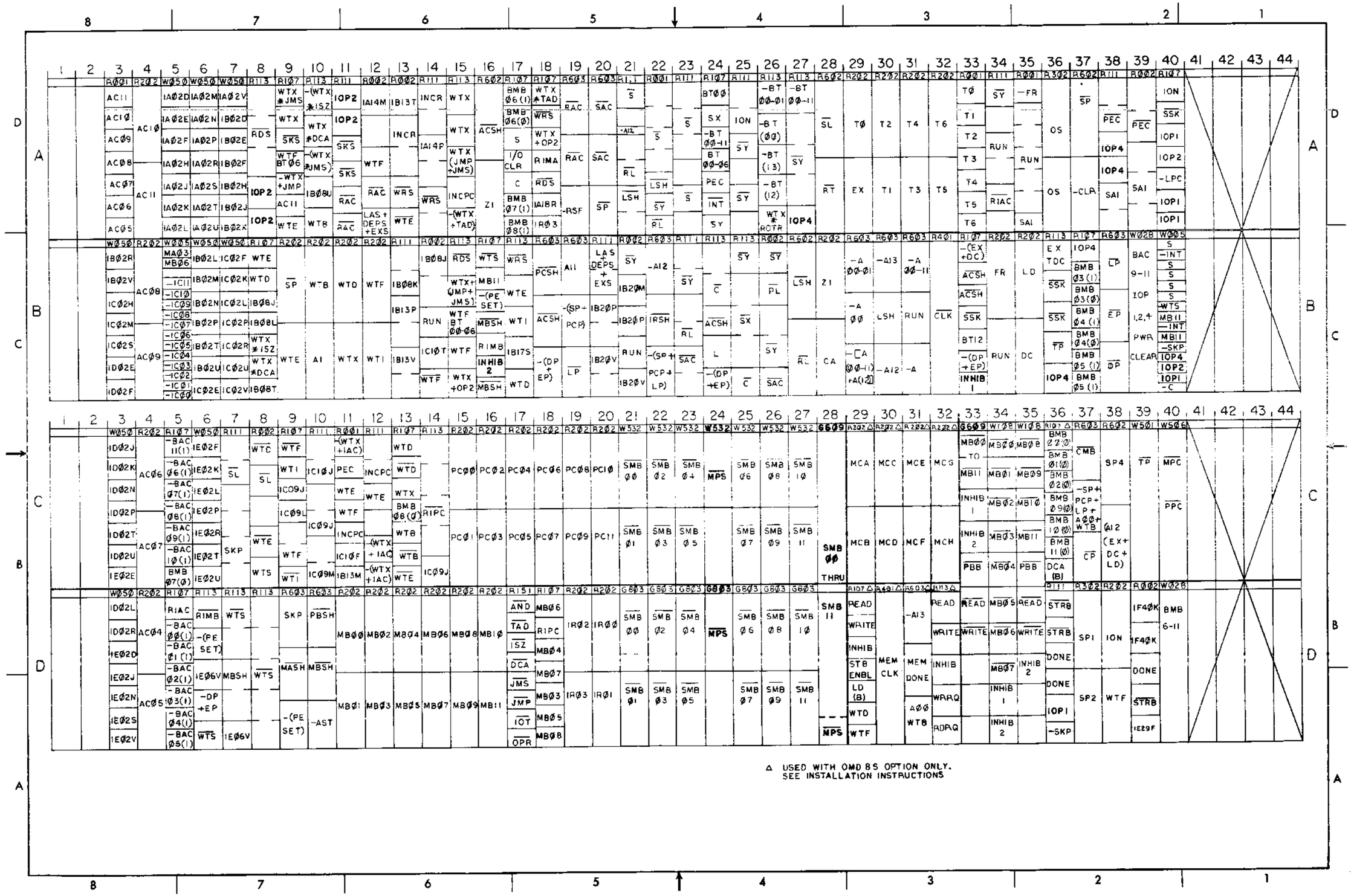
SUM OF THE OUTPUT CURRENTS ARE LIMITED BY
THE EQUATION: $51_{10} + 81_{15} \leq 53$

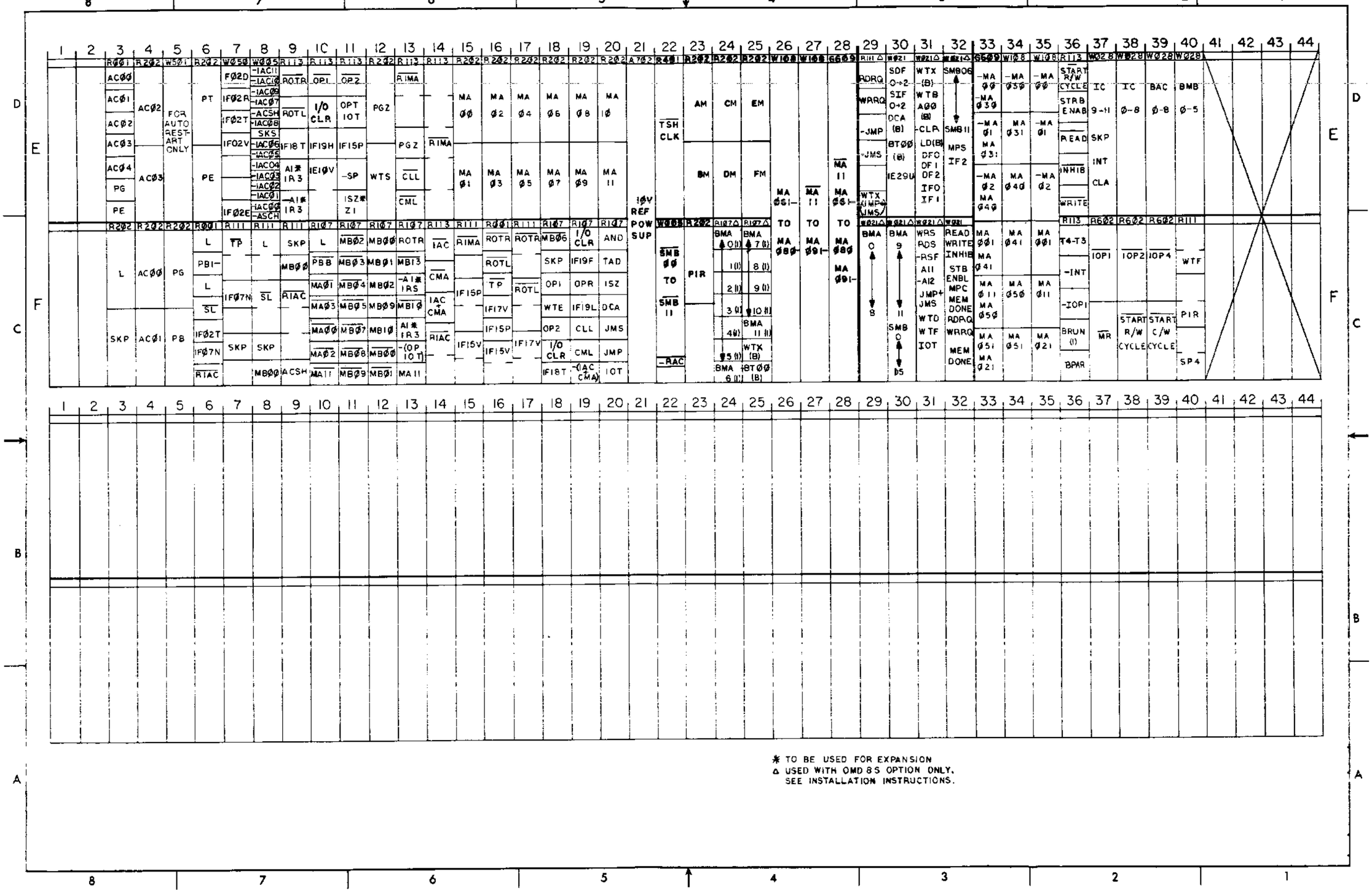
* HEYMAN MFG. CO. TAB TERMINALS

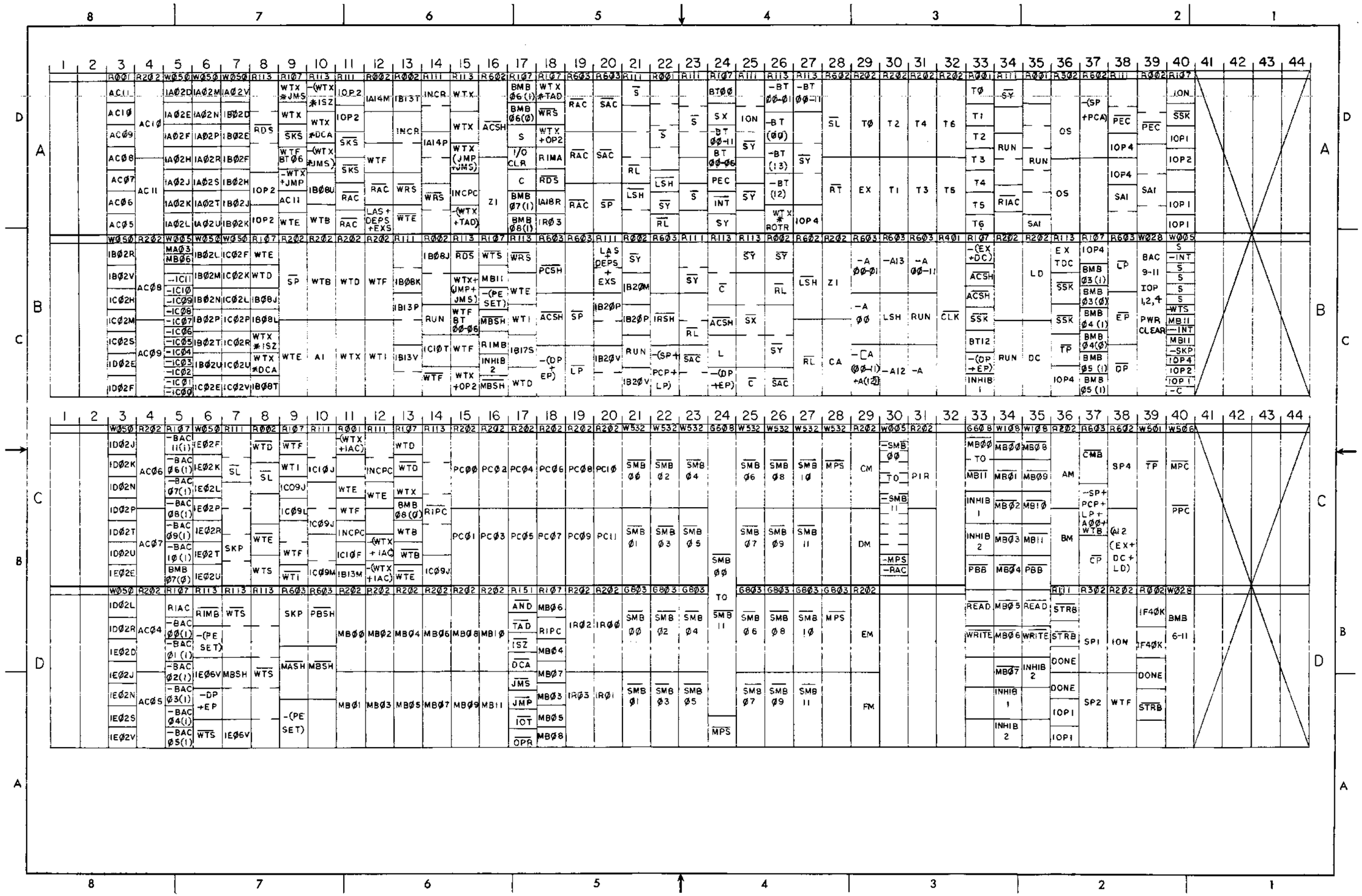
Power Supply 728



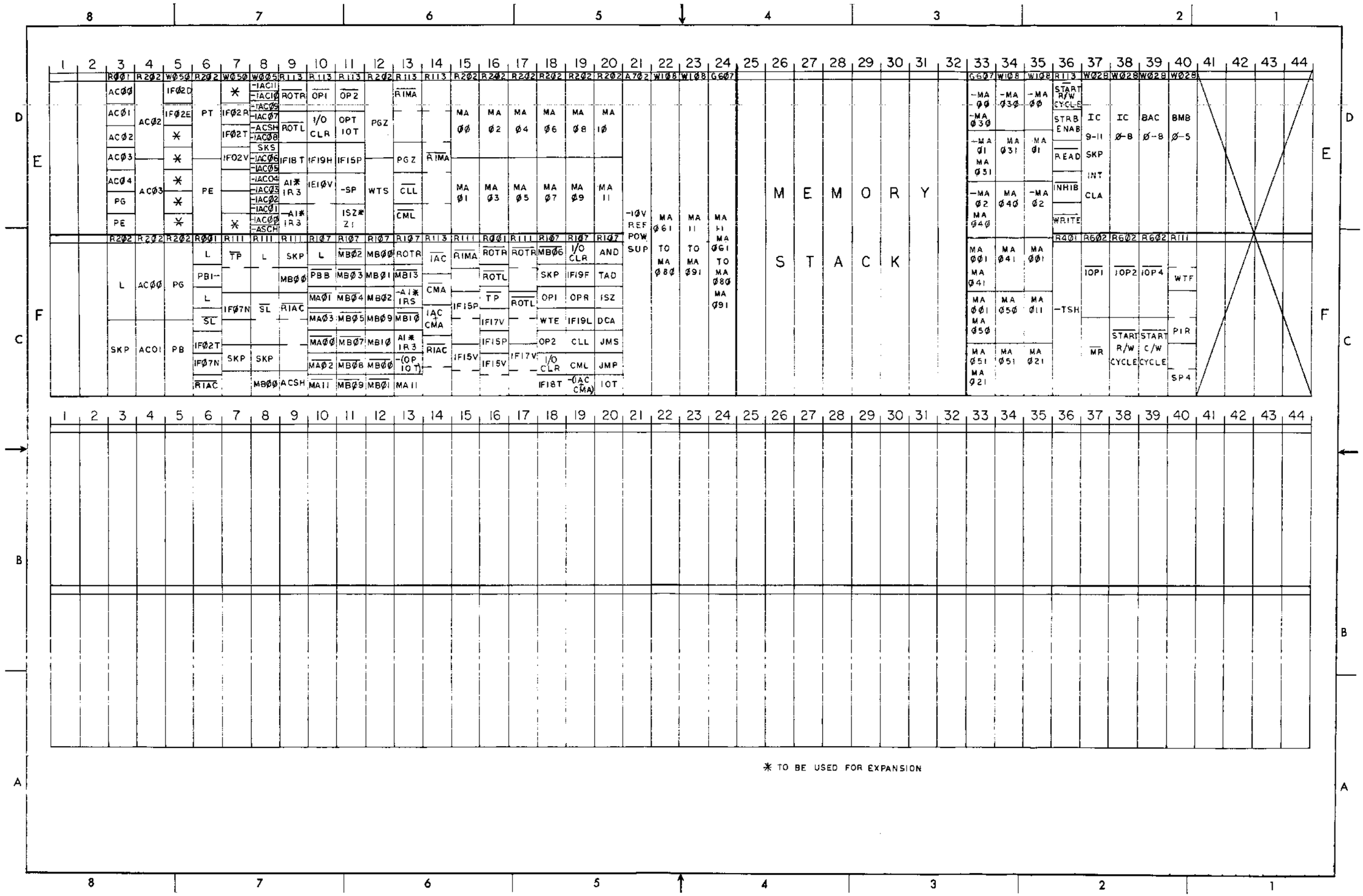
Pulse Amplifier S603


Δ USED WITH OMD 8S OPTION ONLY.
SEE INSTALLATION INSTRUCTIONS


* TO BE USED FOR EXPANSION
Δ USED WITH OMD 8S OPTION ONLY. SEE INSTALLATION INSTRUCTIONS.



Module Utilization (A-D) (4K) D-MU-8S-0-26



Module Utilization (E+F) (4K) D-MU-8S-0-26

APPENDIX B
GLOSSARY

It is not intended that use of this glossary be substituted for reading Chapter 3 or for using the flow charts when following any sequence of events in the logic drawings. The list includes all individual signal names, and for each gives its meaning and the number of the drawing on which it originates. Where no drawing is listed, the item is either a teletype signal (all of which originate on D-BS-PT08-A-1) or is a general abbreviation. No composite signal names are included because these are always made up of standard terms; and no generating conditions are given for logical functions as these are listed in the flow charts. An asterisk indicates that the signal is a pulse.

*A	11	Bit time pulses A00-A13
AC	20	Accumulator
*ACSH	20	AC shift
AI	13	Autoindex flip-flop
AND	16	Logical AND
*AST	15	Auto restart
B		Buffered
BAC	20	Buffered AC
BMB	9	Buffered MB
BT	11	Bit time
C	14	Carry output of adder
CA	14	Carry flip-flop
*CAC	20,17	Clear AC
CFF	15	Clock flip-flop
*CL	10	Clear link
*CLR AC	5,17	Clear AC from I/O channel
*CLK	11	Clock (processor)
CLL	16	Clear link
CLR		Clear
CMA	16	Complement AC
*CMB	9	Clear MB
CML	16	Complement link
CONS	15	Continue key
*CP	15	Continue pulse
DC	15	Deposit (word time)

DCA	16	Deposit and clear
DEPS	15	Deposit key
*DP	15	Deposit pulse
*DPA	15	Deposit pulse delayed
*EP	15	Examine pulse
*EPA	15	Examine pulse delayed
EX	15	Examine (word time)
EXS	15	Examine key
FR	17	Inhibit interrupt during memory field change**
IAC	16	Increment AC
IC	5	Input collector (from bus)
INCPC	13	Increment PC
INCR	13	Increment
INH	18,22	Inhibit level, memory control to core logic
INS	17	Interrupt synchronizer
INT	5,17	Interrupt from I/O channel
IO	17	In-out
I/O	17	In-out
*I/O CLEAR	17	Clear in-out equipment (to bus)
IOF	17	Interrupt off
ION	17	Interrupt on
*IOP	17	In-out pulse (to bus)
*IOSKP	17	In-out skip (from bus)
*IOSKS	17	In-out SKP set
IOT	16	In-out transfer
IR	16	Instruction register
*IR CLR	16	IR clear
ISZ	16	Increment and skip on zero
JMP	16	Jump
JMS	16	Jump to subroutine
L	20	Link
LAS	15	Load address key
LD	15	Load (word time)

**Used only with OMD8S

*LP	15	Load pulse
*LPA	15	Load pulse delayed
LPC	17	Low power condition
*LSH	10	Link shift
MA	12	Memory address
MAB	12	MA buffered
*MASH	12	MA shift
MB	9	Memory
*MBSH	9	MB shift
*MEM	4,23	Memory output pulses to MB and PB
MEMGO	18,22	Level that turns on memory clock
*MPC	17	Memory power clear
*MR	13	Memory request
OP	16	Operate
OP1	16	Operate group 1
OP2	16	Operate group 2
PIR	16	Operate
PB	9	Parity bit
PC	19	Program counter
*PCP	15	Power clear pulse
*PCSH	19	PC shift
PE	9	Parity error
PESEL	17	PE select (IOT)
*PE SET	9	Pulse that sets PE if PT and PB differ
PG	9	Parity generator
PGZ	12	Page zero
PIR	17	Program interrupt request flip-flop
PISEL	17	Program interrupt select (IOT)
*PPC	17	Processor power clear
PSM		Teletype print selector magnet
PT	9	Parity test
RCLE		Teletype receiver clock enable
*RCLO		Teletype receiver clock
RD		Read
READ	18,22	Read level, memory control to core logic

RIAC	20	Readin AC
RIMA	12	Readin MA
RIMB	9	Readin MB
RIPC	19	Readin PC
ROTL	16	Rotate left
ROTR	16	Rotate right
RRE		Teletype reader run
*RT	11	Reset timer
RUN	15	RUN flip-flop
*SAC	10,15	Set AC (from SR)
SAI	13	Sense autoindex
SIK	15	Single instruction switch
SKP	10	Skip flip-flop; skip from I/O channel
*SL	10	Set link
*SP	15	Start pulse
*SP	17	Special pulse (for IOP)
SSK	15	Single step switch
STOS	15	Stop key
*STROBE	18,22	Strobe, memory control to core logic
STS	15	Start key
S	14	Sum output of adder
SR	15	Switch register
SX	14	X-input to adder
SY	14	Y-input to adder
T	11	Timer (time ring counter)
TAD	16	(Two's) add
*TCLO		Teletype transmitter clock
*TP	15	Trigger pulse
*TSH	18,22	Time shift (memory clock output)
TSO		Teletype serial output
WR		Write
WRITE	18,22	Write level, memory control to core logic
WT	13	Word time
WTB	13	Word time break
WTD	13	Word time defer

WTE	13	Word time end
WTF	13	Word time fetch
WTI	13	Word time index
WTINCPC	13	Increment PC
WTINCR	13	Increment
*WT MEM C/W	13	Start clear-write cycle (to memory)
*WT MEM R/W	13	Start read-write cycle (to memory)
WTRD	13	Word time needs to read (from memory)
WTS	13	Word time stop (for memory cycle)
WTWR	13	Word time needs to write (in memory)
WTX	13	Word time execute
ZI	14	Zero indicator

APPENDIX C
ENGINEERING DRAWINGS AND GLOSSARY FOR OMD8S, MC8S, DB8S, ME8S, AND MM8S OPTIONS

C.1 DRAWINGS

This appendix contains reduced copies of logic diagrams, flow charts, and module utilization charts for this group of options. The drawings that are reproduced here for instruction purposes apply to the standard production PDP-8/S. During actual maintenance, use the current prints supplied with the equipment.

Other engineering drawings (assembly drawings, parts lists, etc.) used primarily for reference in maintenance are listed on the master drawing list for each option.

Option	Master Drawing List
OMD8S	A-ML-OMD8S-0
MC8S	A-ML-MC8S-0
DB8S	A-ML-DB8S-0
ME8S	A-ML-ME8S-0

Schematics and Flow Diagrams

DB8S Option

ME8S Option

MM8S Option

Circuit Schematics

Drawings for this group of options use the same format and graphic conventions as the PDP-8/S drawings. (See Chapter 3 and the introduction to Appendix A.)

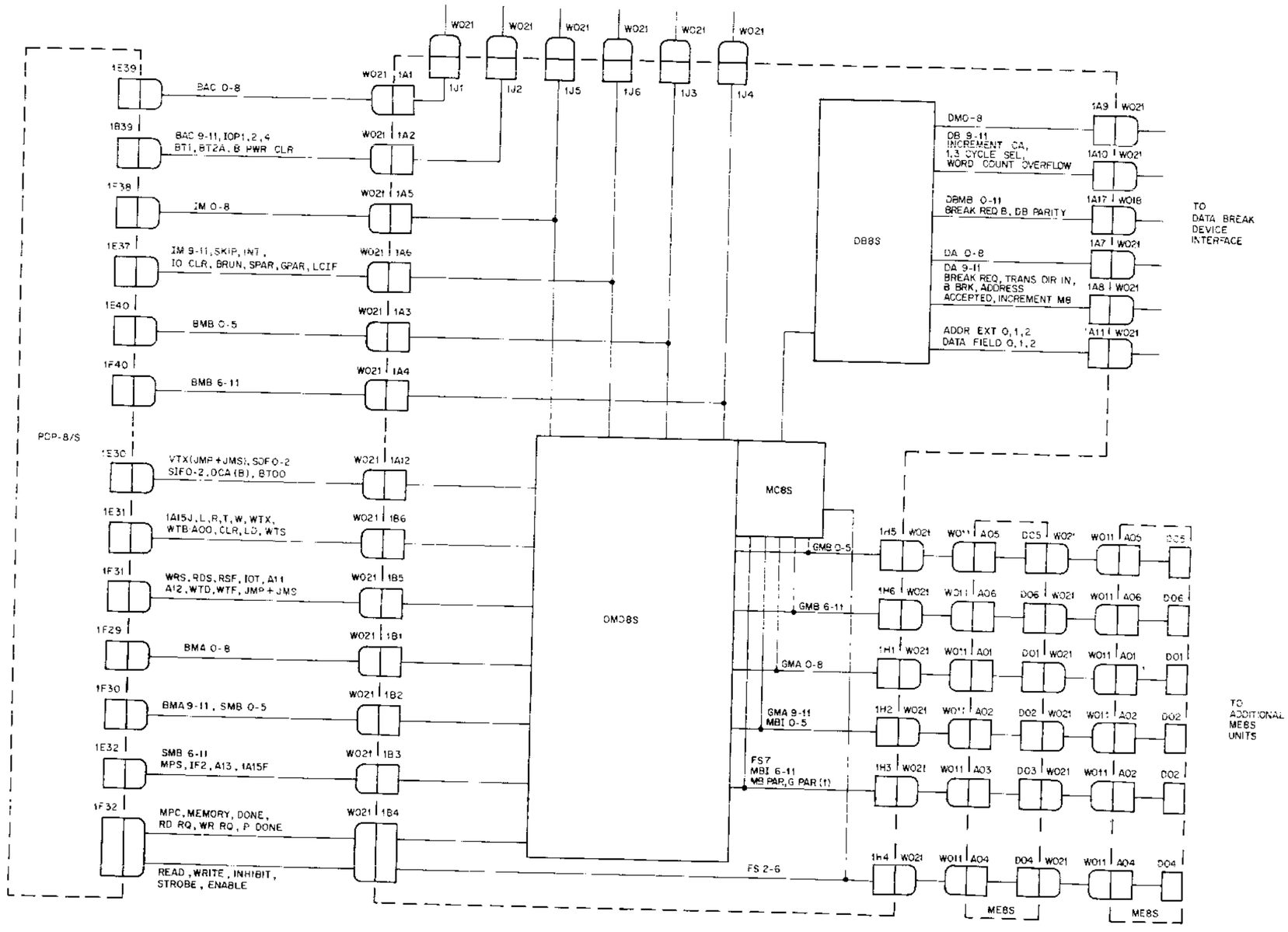
C.2 MODULE UTILIZATION

When an OMD8S Assembly is interconnected with the PDP-8/S, certain modules are removed from the PDP-8/S and either relocated within the PDP-8/S or installed in the OMD8S assembly. This module rearrangement is shown in Drawing No. C-SP-OMD-0-8. In addition, the standard 4K

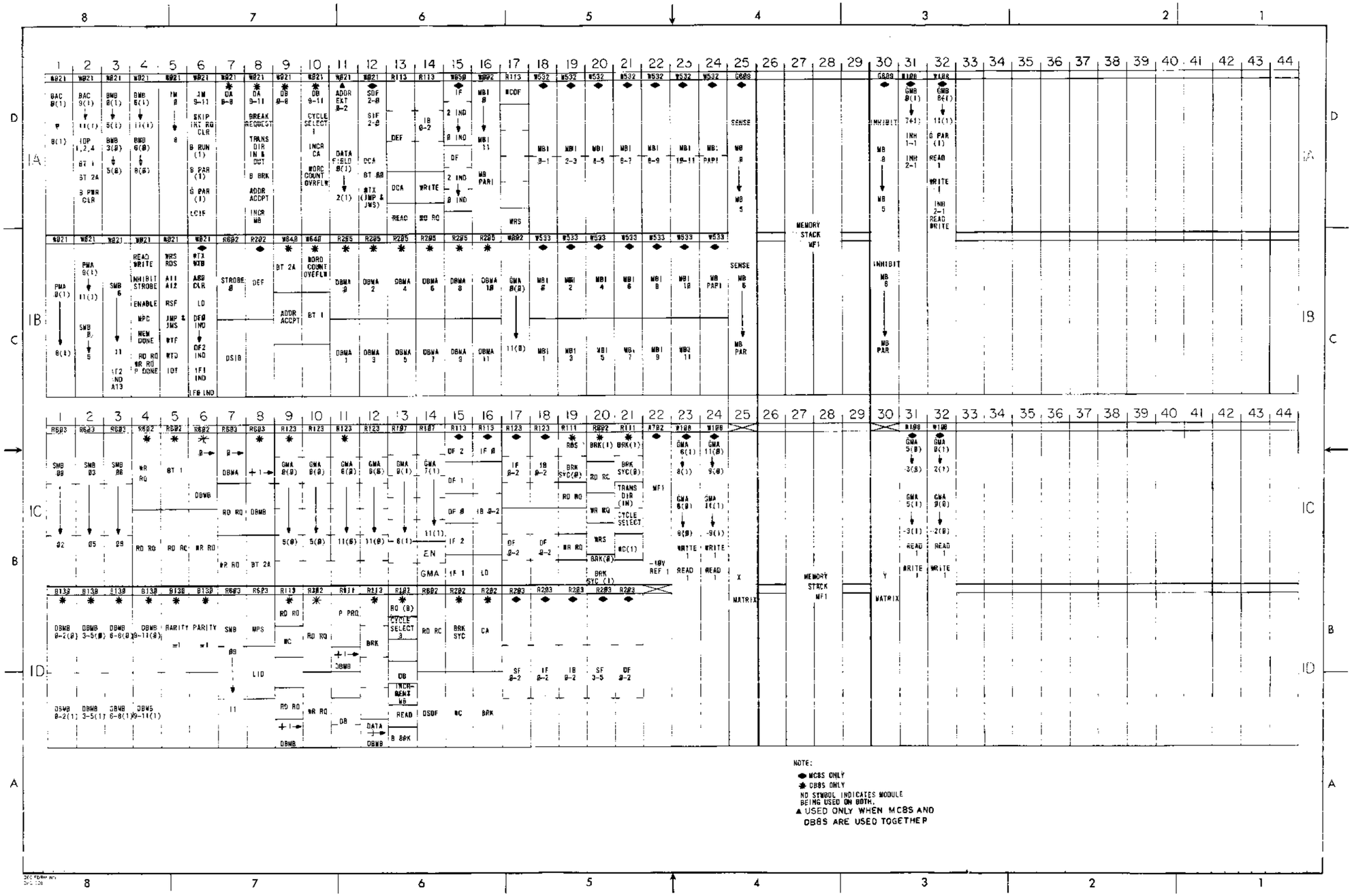
memory module (memory field 0) is removed from the PDP-8/S and installed in the OMD8S assembly. Relocation of the memory module is required whenever an OMD8S assembly is used, whether or not the memory is to be expanded. The resulting module utilization within the OMD8S assembly for any combination of options is shown in Drawing No. D-MU-OMD8S-0-1. Circuit schematics of module types used in these options (but not the standard PDP-8/S) appear after the logic diagrams.

C.3 GLOSSARY

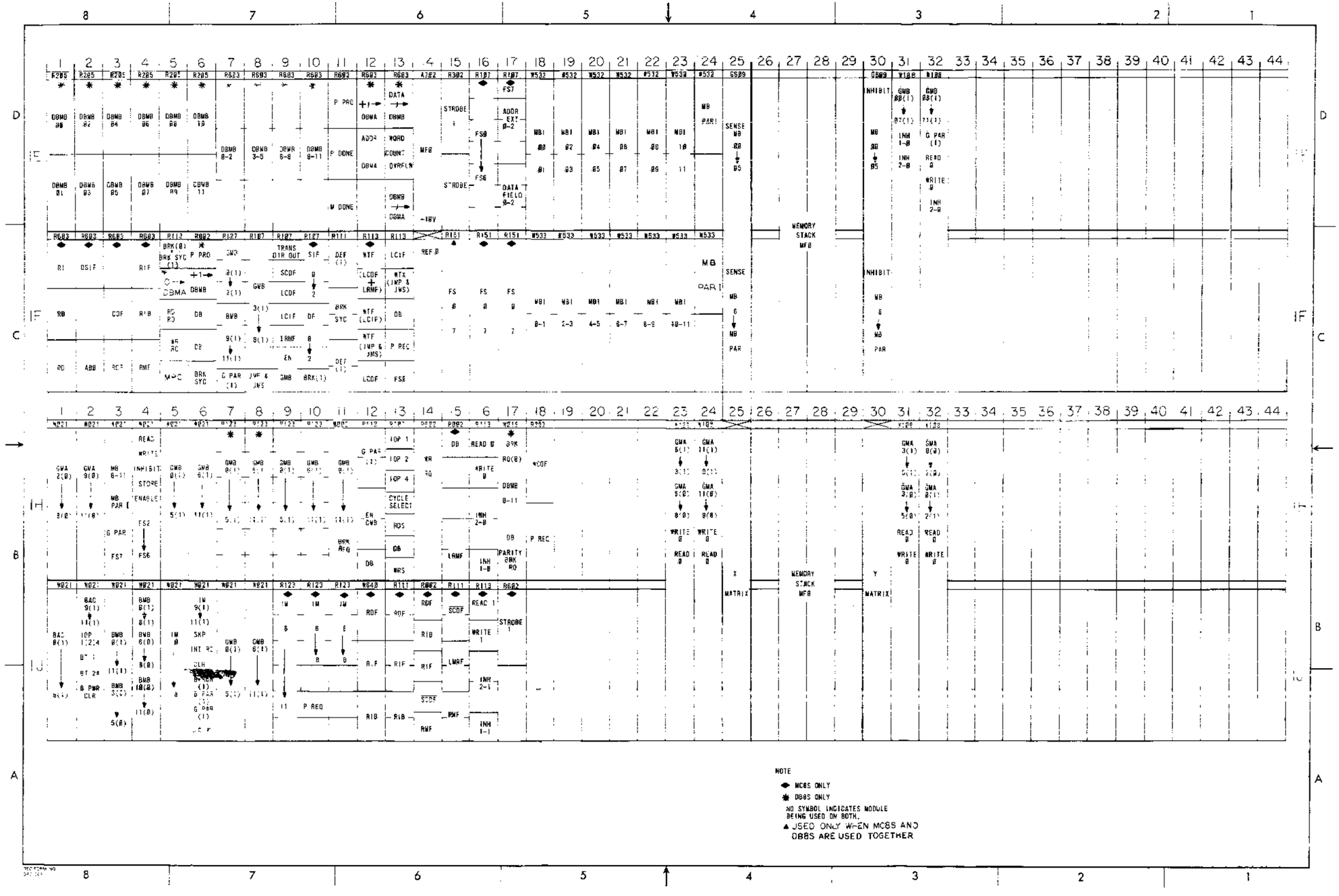
A glossary of signal names for this group of options appears at the end of this appendix.



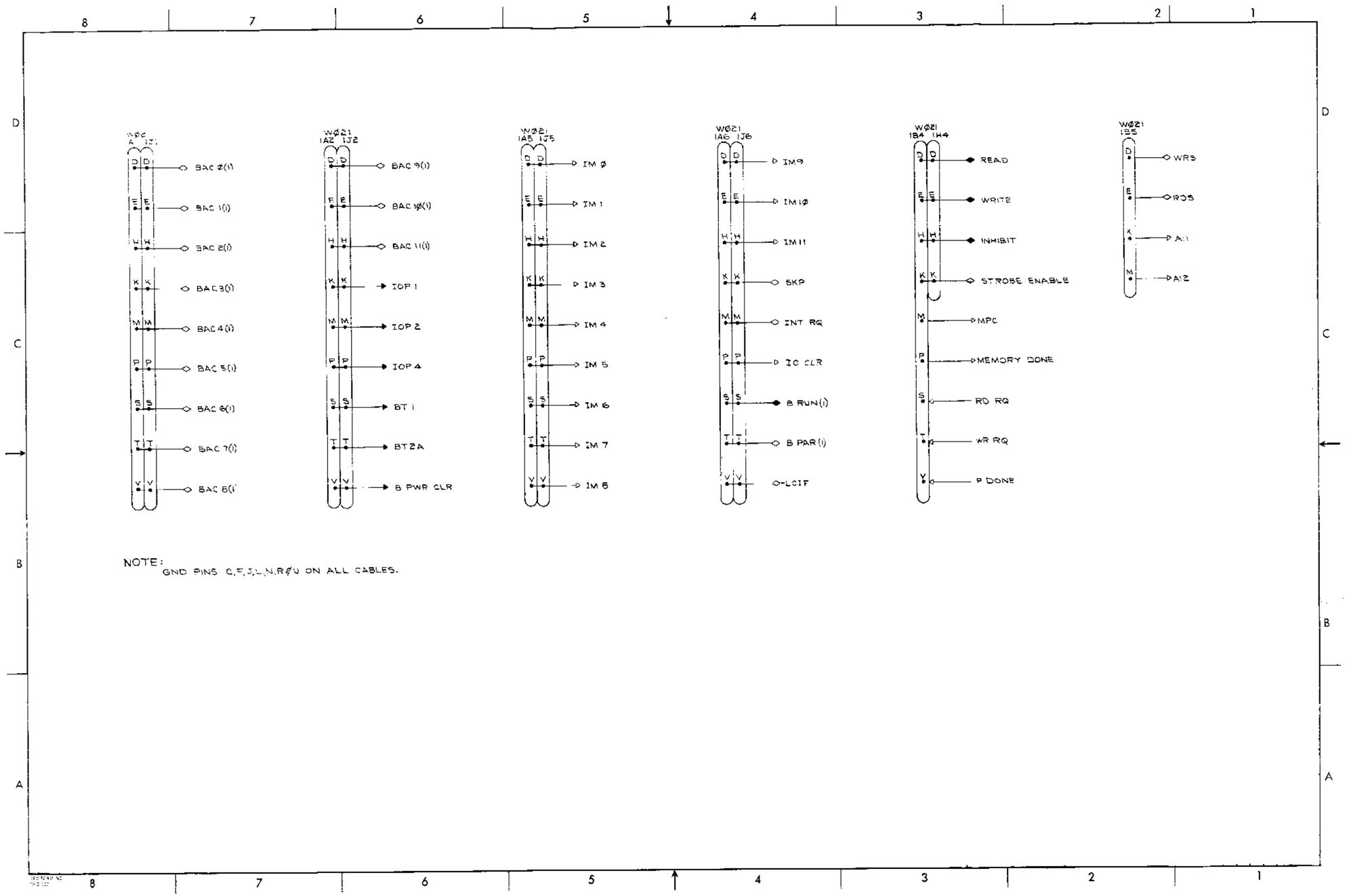
Memory Expansion and Data Break
Interconnecting Cables



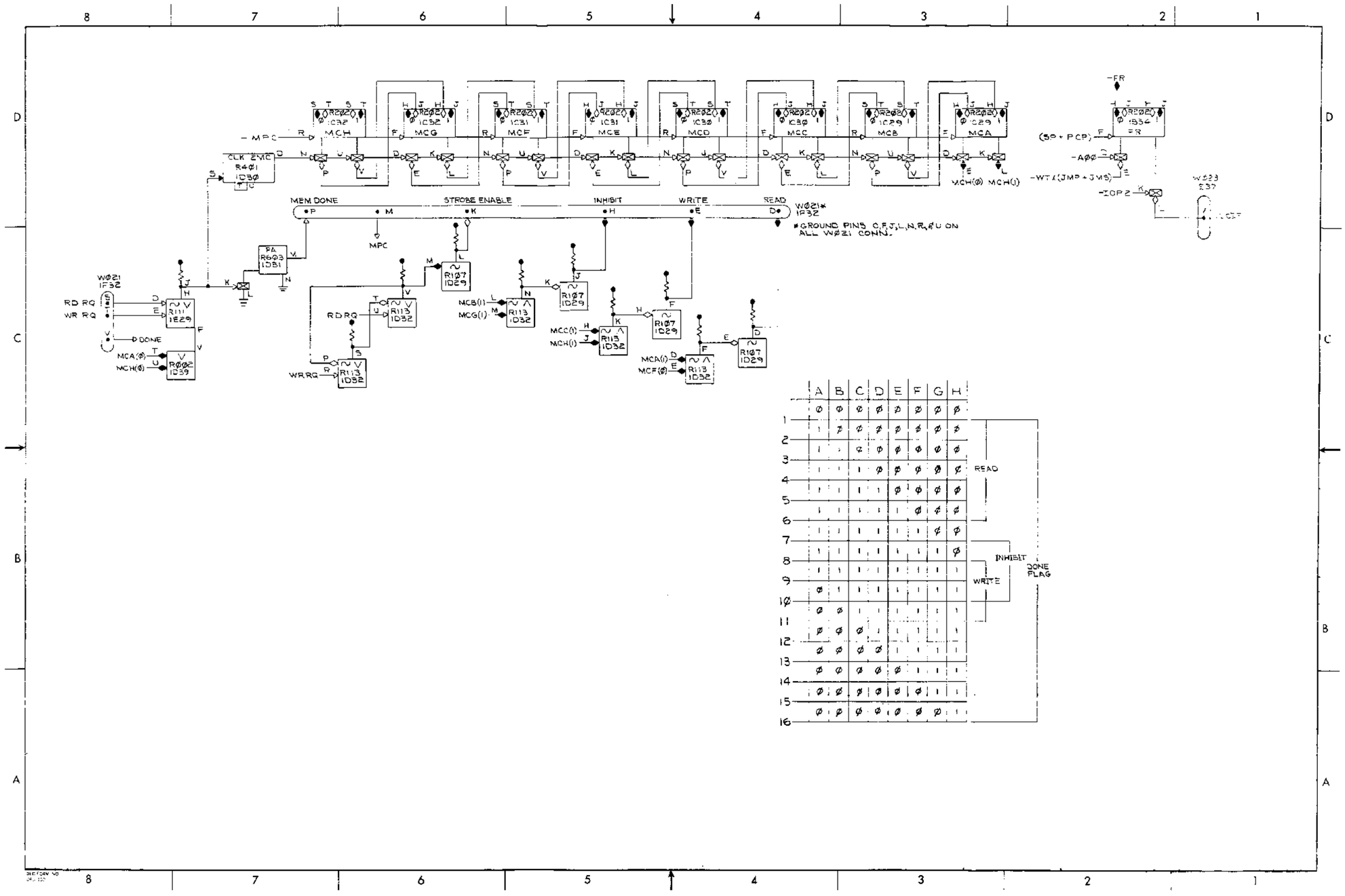
D-MU-OMD8S-0-1 Module Utilization
(OMD8S) (Sheet 1)



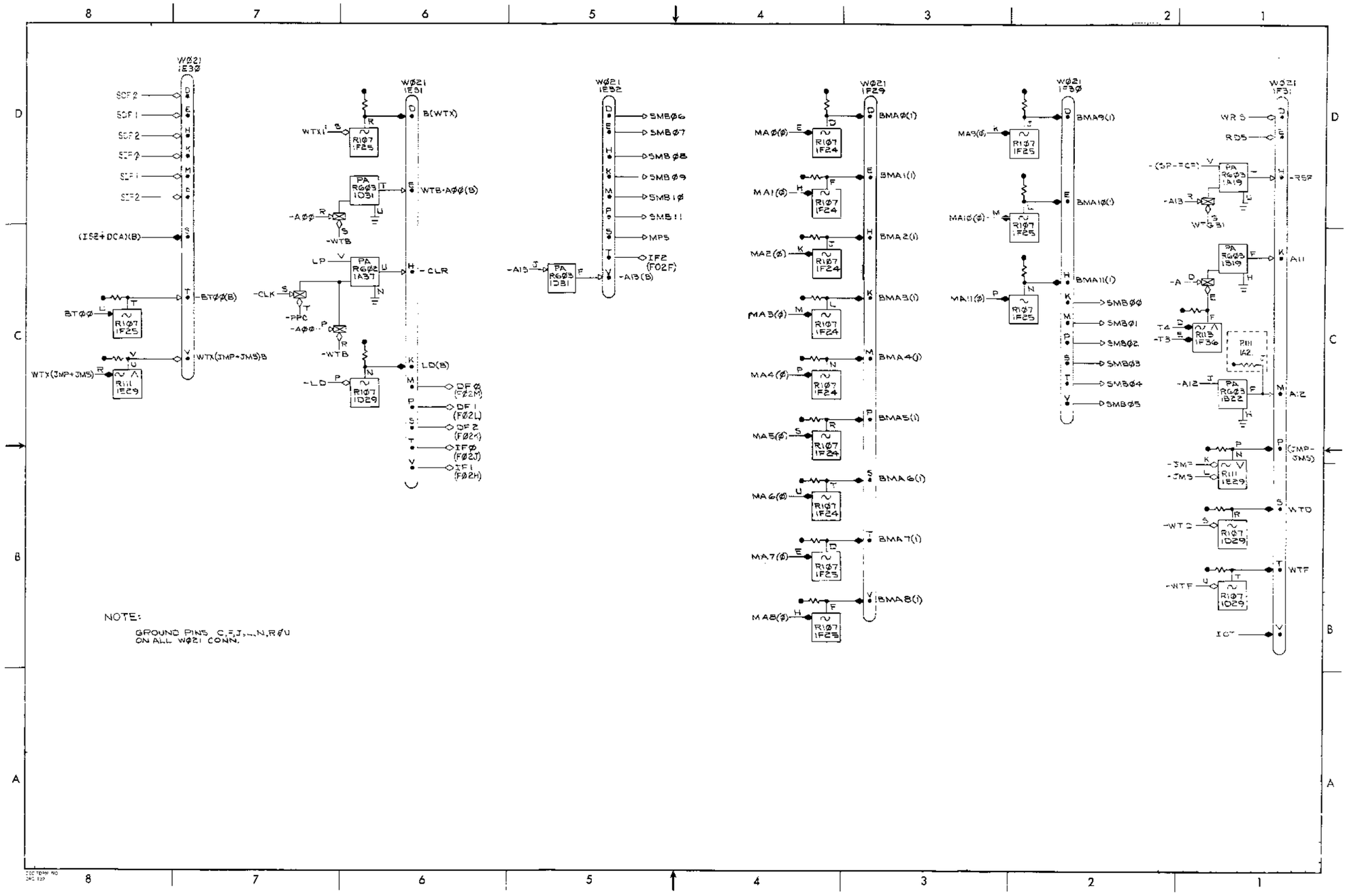
D-MU-OMD8S-0-1 Module Utilization
(OMD8S) (Sheet 2)



D-IC-OMD8S-0-3 DB8S, MC8S I/O Connectors



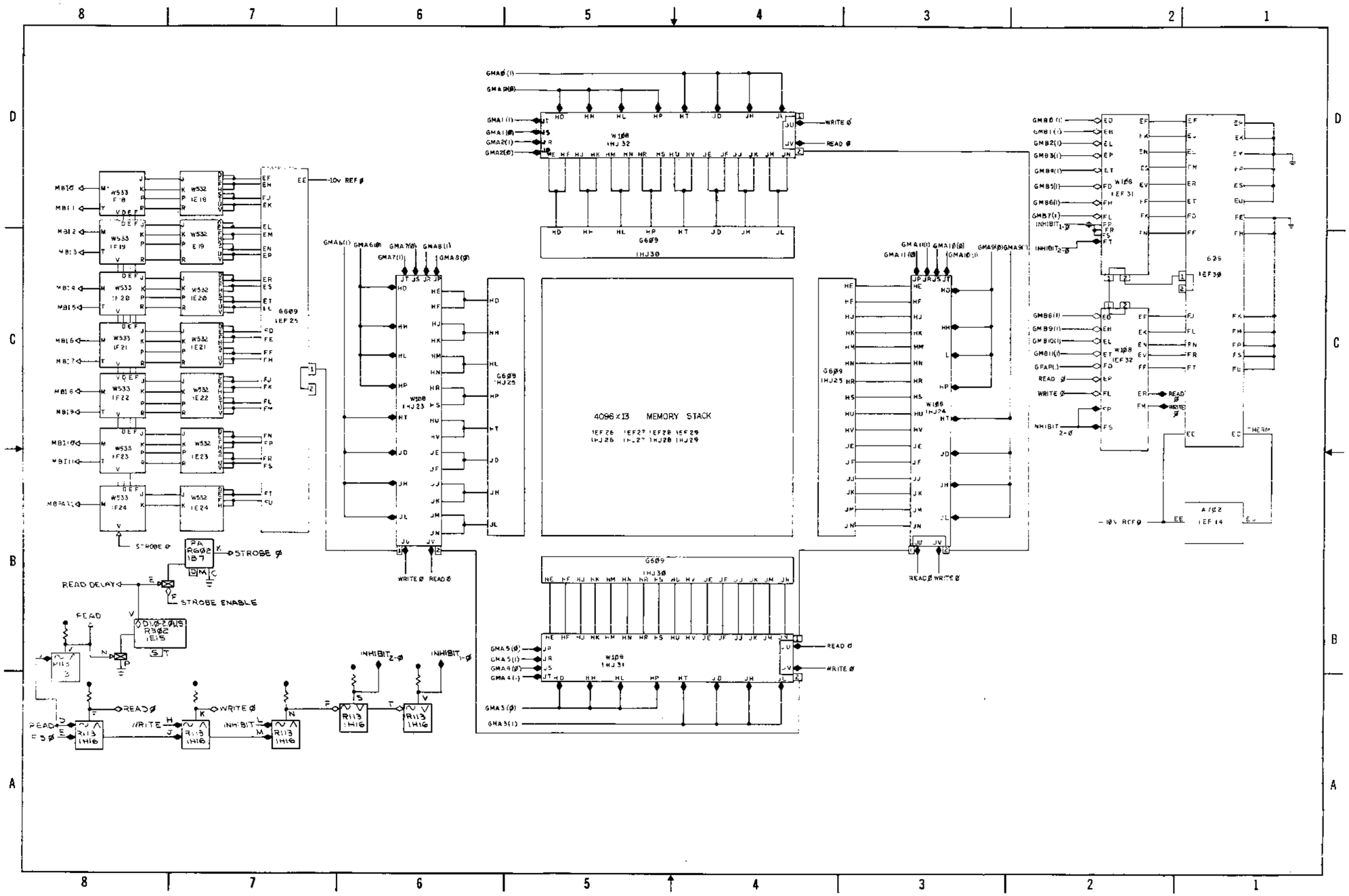
D-BS-OMD8S-0-4 OMD8S Conn and Logic in 8S
(Sheet 1)

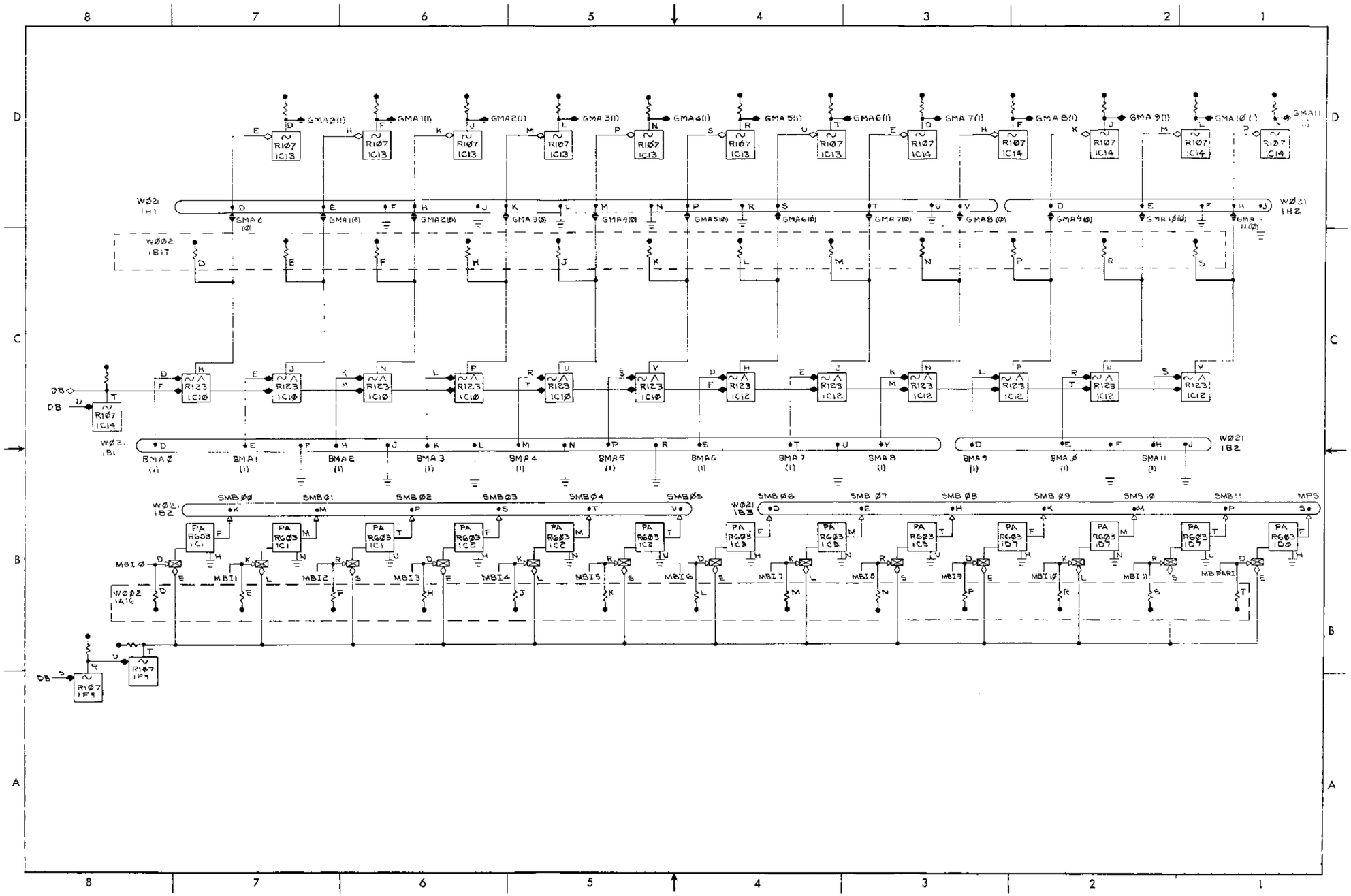


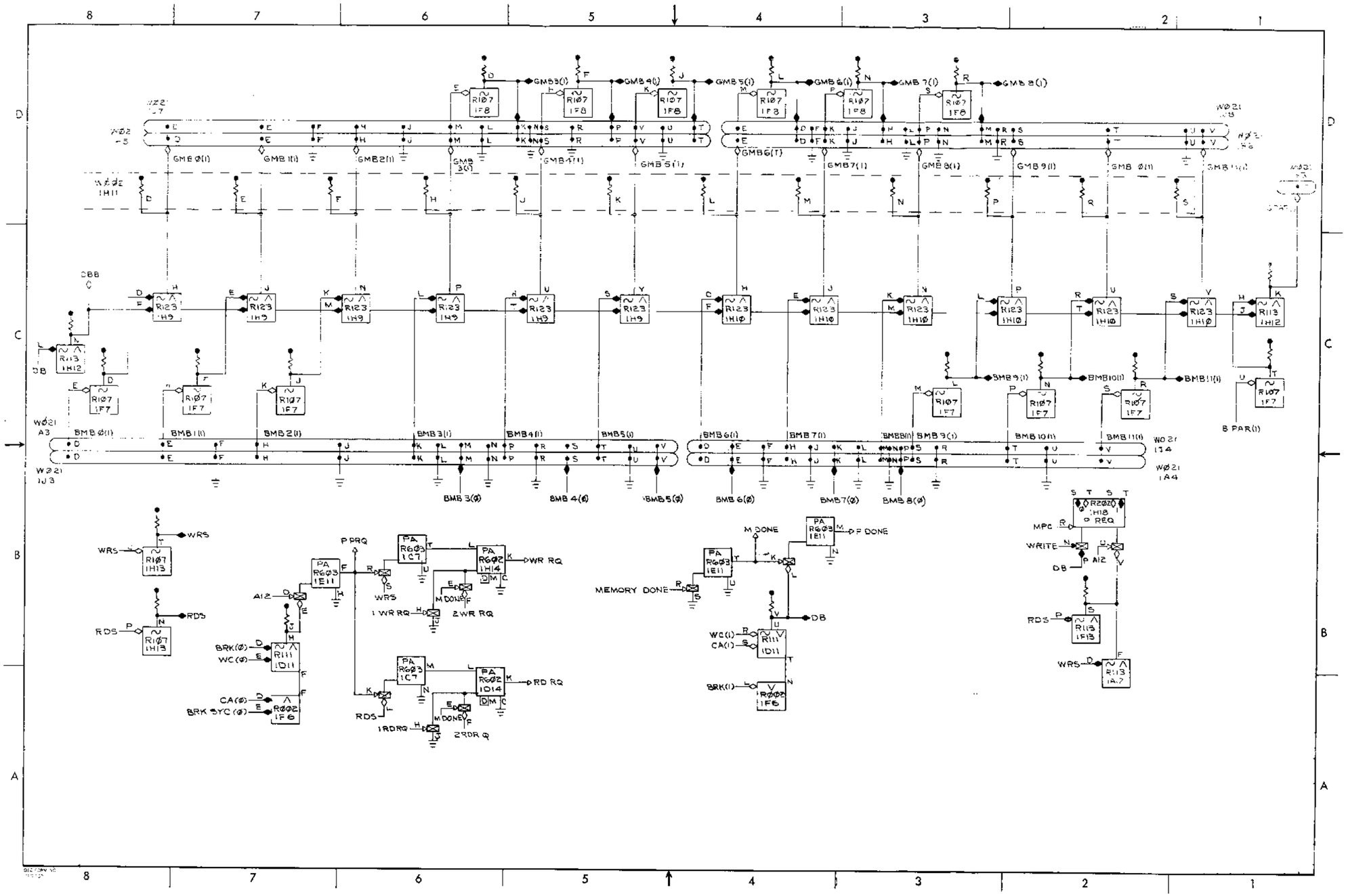
NOTE:

GROUND PINS C,F,J,L,N,R&U ON ALL W021 CONN.

D-8S-OMD8S-0-4 OMD8S Conn and Logic in 8S
(Sheet 2)


4096 x 13 MEMORY STACK
1EF26 1EF27 1EF28 1EF29
1HJ26 1HJ27 1HJ28 1HJ29
-10v REF Ø
STROBE Ø
STROBE Ø
STROBE ENABLE
READ DELAY
READ
WRITE
INHIBIT
READ Ø
WRITE Ø
THERM


8
7
6
5
4
3
2
1
D
C
B
A
WØ2 1H1
WØ2 1H2
WØ2 1B1
WØ2 1B2
WØ2 1B3
WØ2 1A7
WØ2 1A6
GMAØ(1)
GMA1(1)
GMA2(1)
GMA3(1)
GMA4(1)
GMA5(1)
GMA6(1)
GMA7(1)
GMA8(1)
GMA9(1)
GMA10(1)
GMA11(1)
GMA6(Ø)
GMA7(Ø)
GMA8(Ø)
GMA9(Ø)
GMA10(Ø)
GMA11(Ø)
R1Ø7 1C13
R1Ø7 1C14
R123 1CIØ
R123 1C12
R1Ø7 1C19
R1Ø7 1F9
DB
SMBØØ
SMBØ1
SMBØ2
SMBØ3
SMBØ4
SMBØ5
SMBØ6
SMBØ7
SMBØ8
SMBØ9
SMBIØ
SMBII
MPS
PA RGØ3 1C1
PA RGØ3 1C2
PA RGØ3 1C3
PA RGØ3 1D7
PA RGØ3 1D8
MBIØ
MBI1
MBI2
MBI3
MBI4
MBI5
MBI6
MBI7
MBI8
MBI9
MBIØ
MBII
MB PARI



D-BS-OMD8S-0-7 OMD8S MB Gating

OMD8S INSTALLATION PROCEDURE

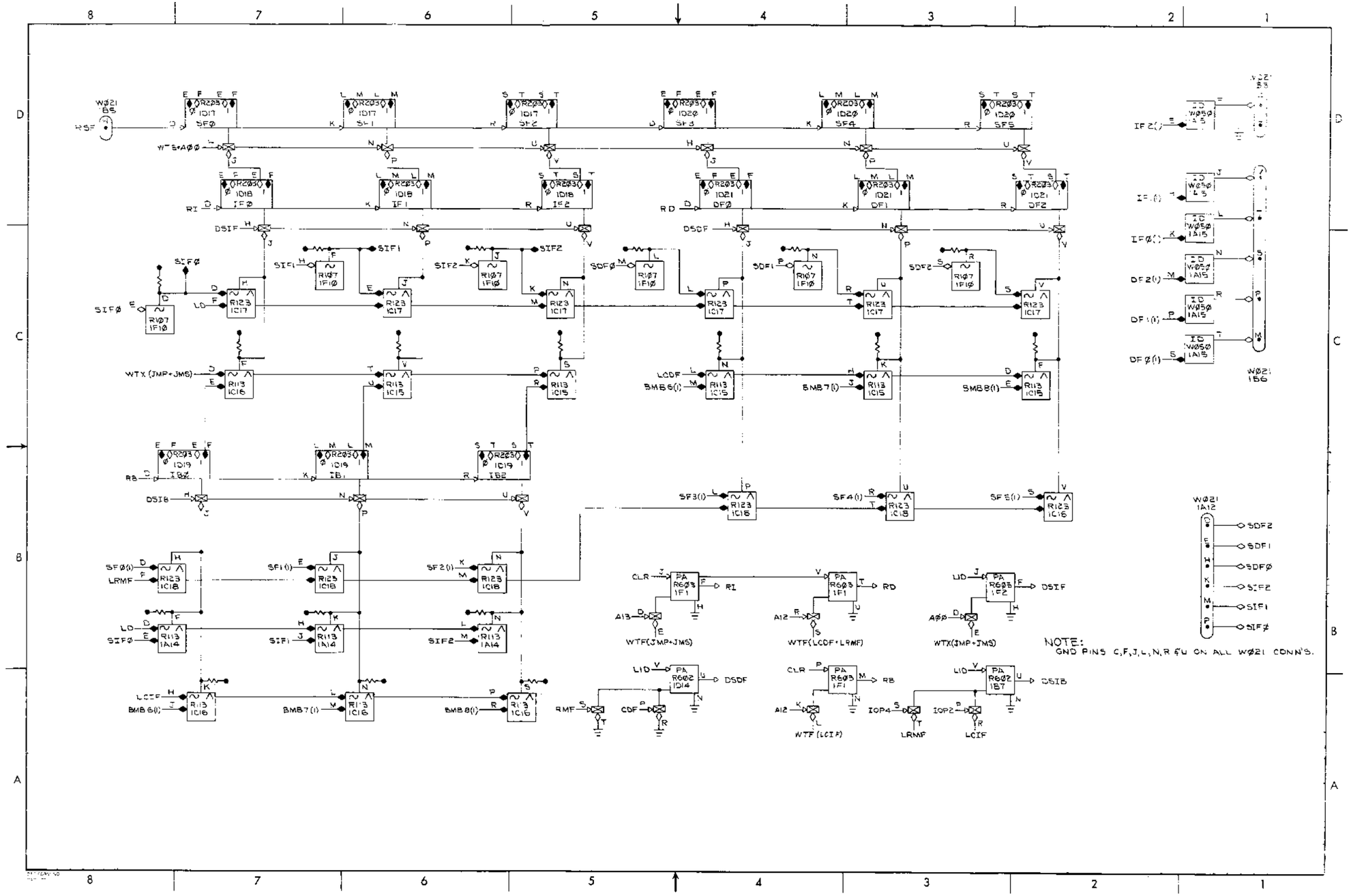
MODULE TYPE	REMOVE FROM 8S PROCESSOR	RELOCATE IN OMD8S LOGIC
A7Ø2	1EF21	1EF14
G6Ø9	1CDEF28	1EFHJ25
G6Ø9	1CDEF33	1EFHJ3Ø
W532	1C21	1E18
W532	1C22	1E19
W532	1C23	1E2Ø
W532	1C24	1E21
W532	1C25	1E22
W532	1C26	1E23
W532	1C27	1E24
W533(OR GBØ3)	1D21	1F18
W533(OR GBØ3)	1D22	1F19
W533(OR GBØ3)	1D23	1F2Ø
W533(OR GBØ3)	1D24	1F21
W533(OR GBØ3)	1D25	1F22
W533(OR GBØ3)	1D26	1F23
W533(OR GBØ3)	1D27	1F24
WIØ8	1EF26	1HJ28
WIØ8	1EF27	1HJ24
WIØ8	1EF34	1HJ31
WIØ8	1EF35	1HJ32
WIØ8	1CD34	1EF31
WIØ8	1CD35	1EF32
RIØ7	1A17	1F07
RIØ7	1B37	1F08
RIØ7	1CØ5	1C13

MODULE TYPE	REMOVE FROM 8S PROCESSOR	RELOCATE IN 8S PROCESSOR
RIIB	1E36	1D32
R2Ø2	1E25	1C29
R2Ø2	1E24	1C3Ø
R2Ø2	1E26	1C31
R4Ø1	1E22	1D3Ø
RIØ7	1C13	1D29
RIØ7	1C36	1F24

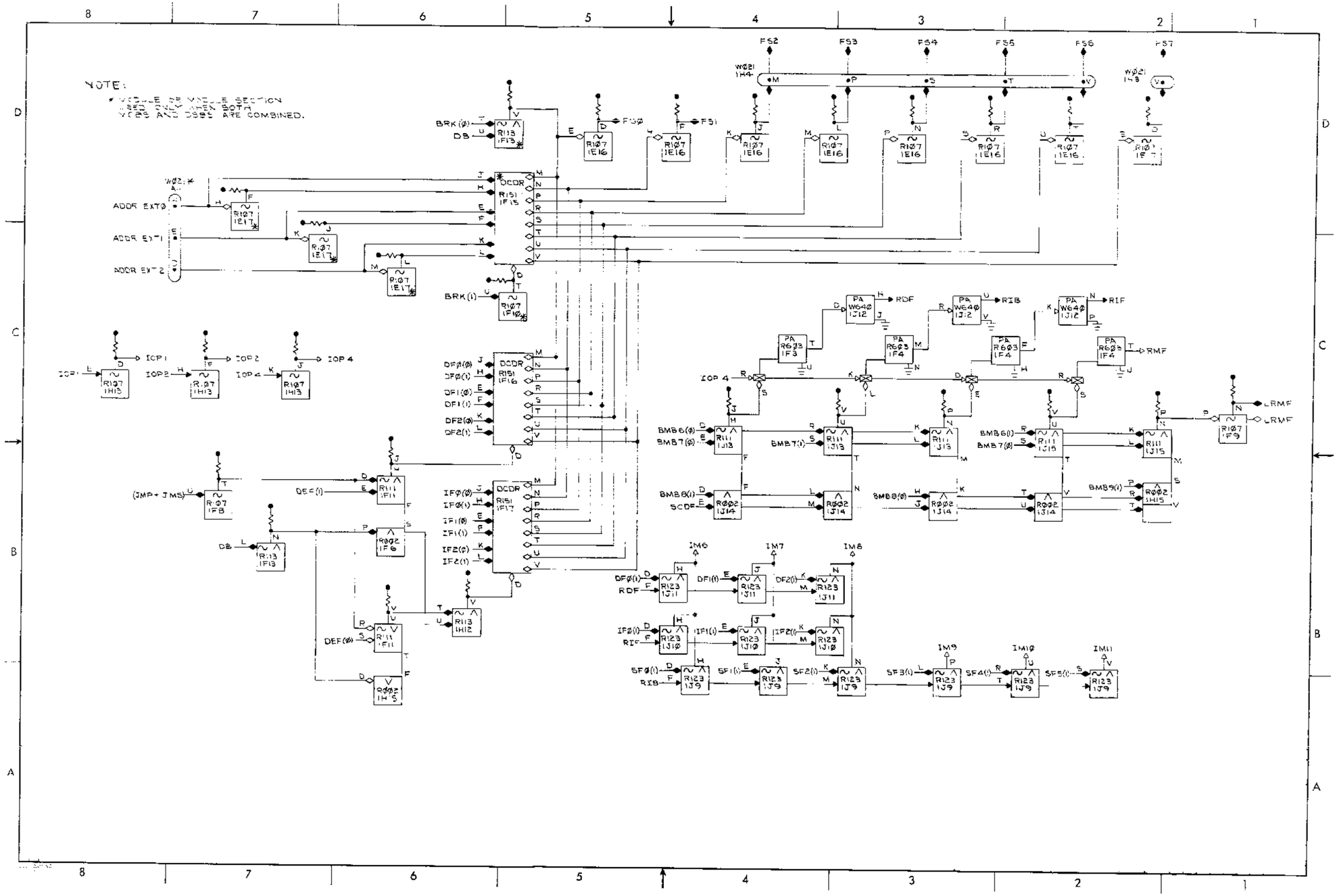
MODULE TYPE	ADD TO 8S PROCESSOR
RIØ7	1F25
RIII	1E29
R2Ø2	1C32
R6Ø3	1D31
WØ21	1F29
WØ21	1F3Ø
WØ21	1E31
WØ21	1F31
WØ21	1F32
WØ21	1E32
WØ21	1E3Ø
RIIB	1F36
JUMPER	1D36L TO 1D36C
SIØ7	1A17
SIØ7	1B37
SIØ7	1CØ5
SIØ7	1C13
SIØ7	1C36

TO CABLE SLOT IN OMD8S LOGIC
1BØ1
1BØ2
1BØ6
1BØ5
1BØ4
1BØ3
JA12

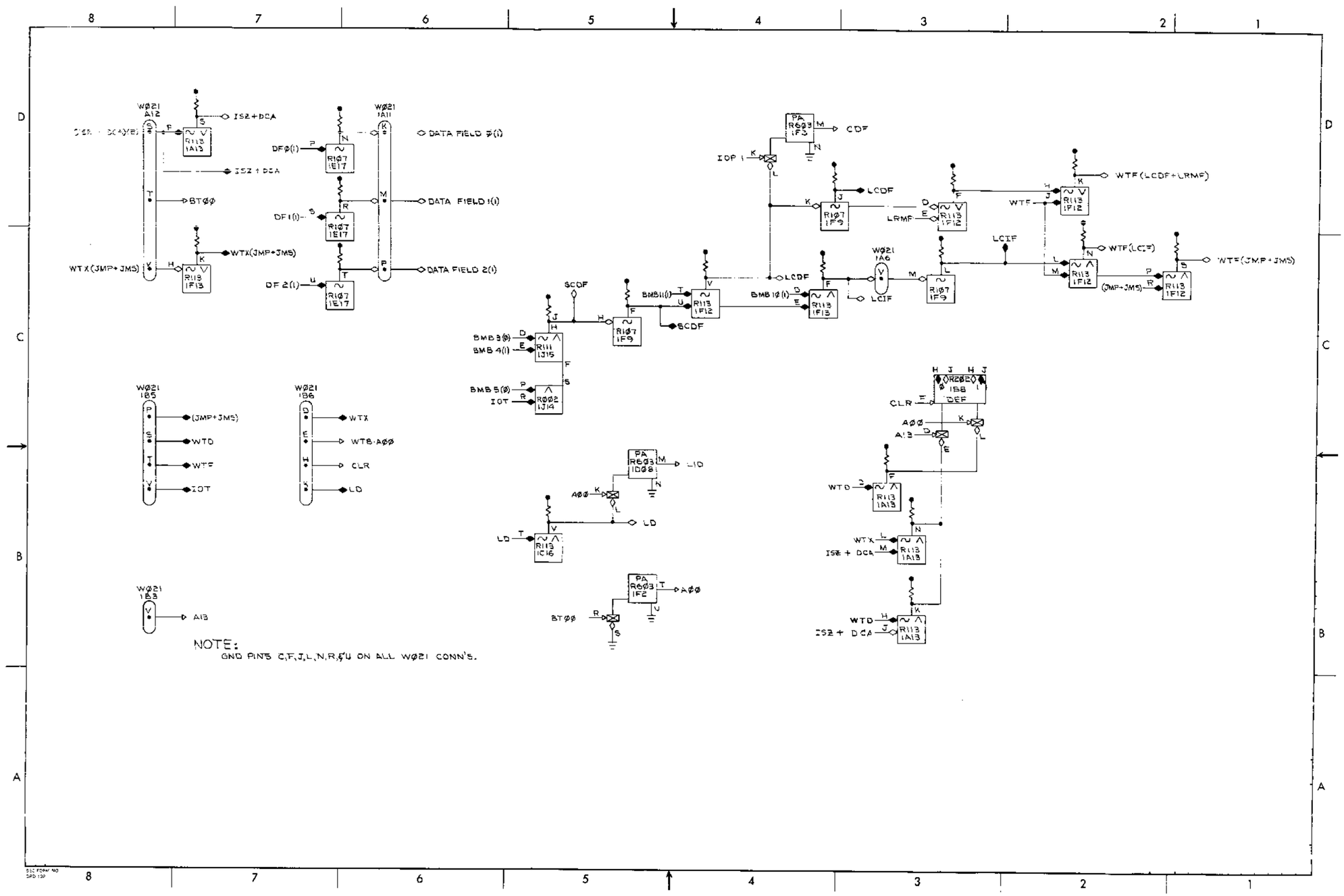
112 Ø1



D-BS-MC8S-0-1 Extended Memory Control
(MC8S) (Sheet 1)

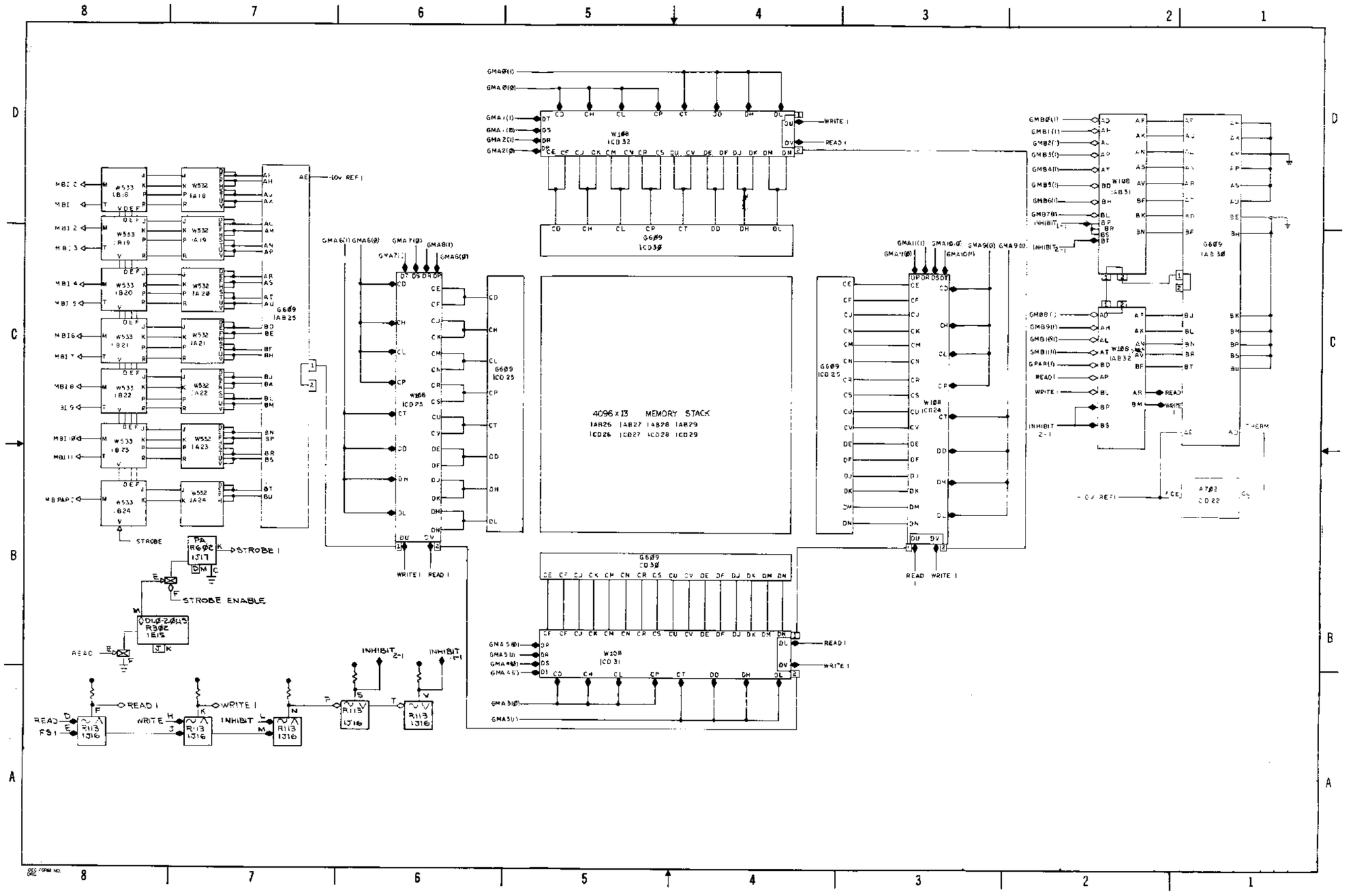


D-BS-MC8S-0-1 Extended Memory Control (MC8S) (Sheet 2)

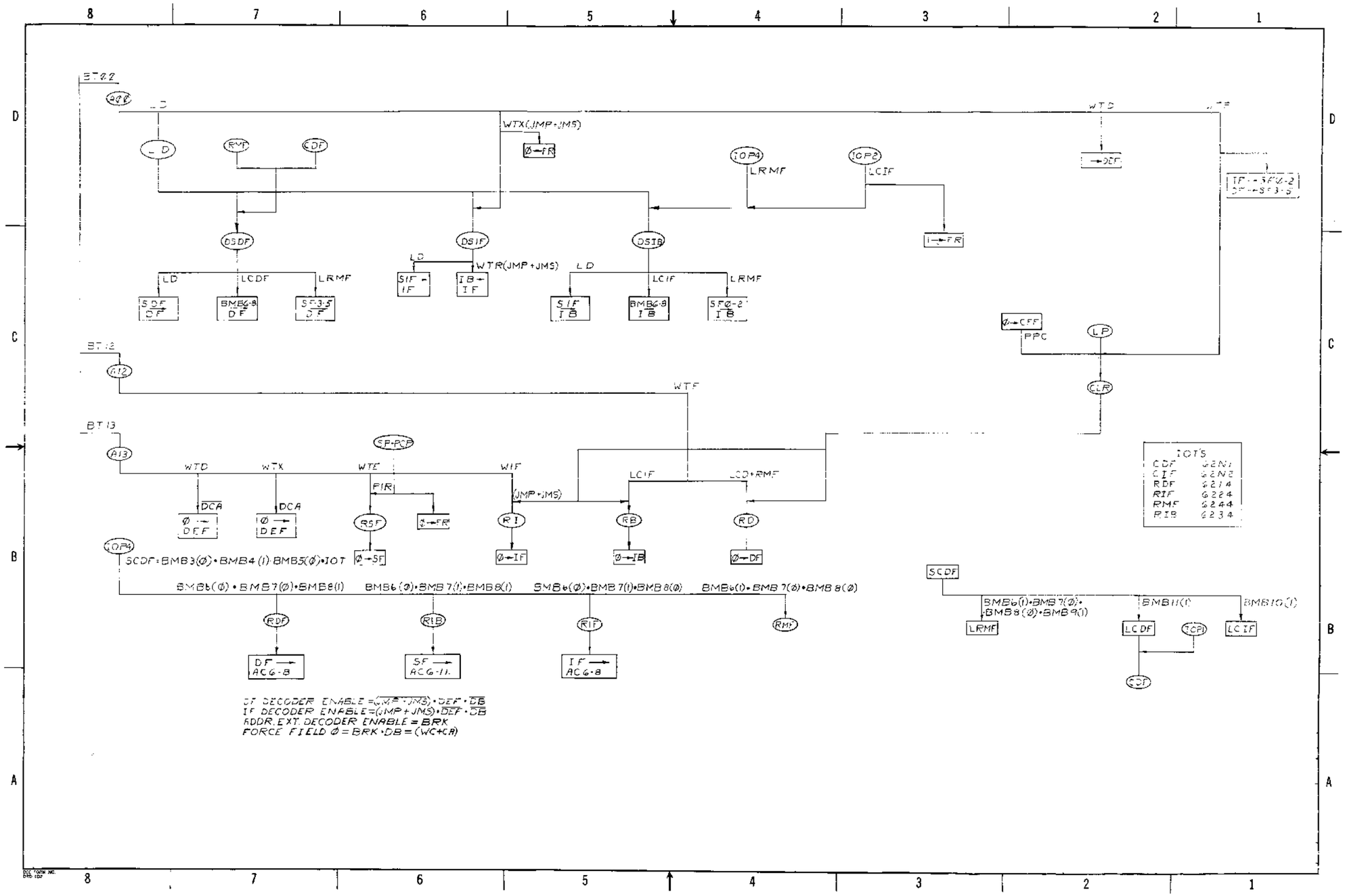


NOTE:
GND PINS C,F,J,L,N,R,&U ON ALL W@21 CONN'S.

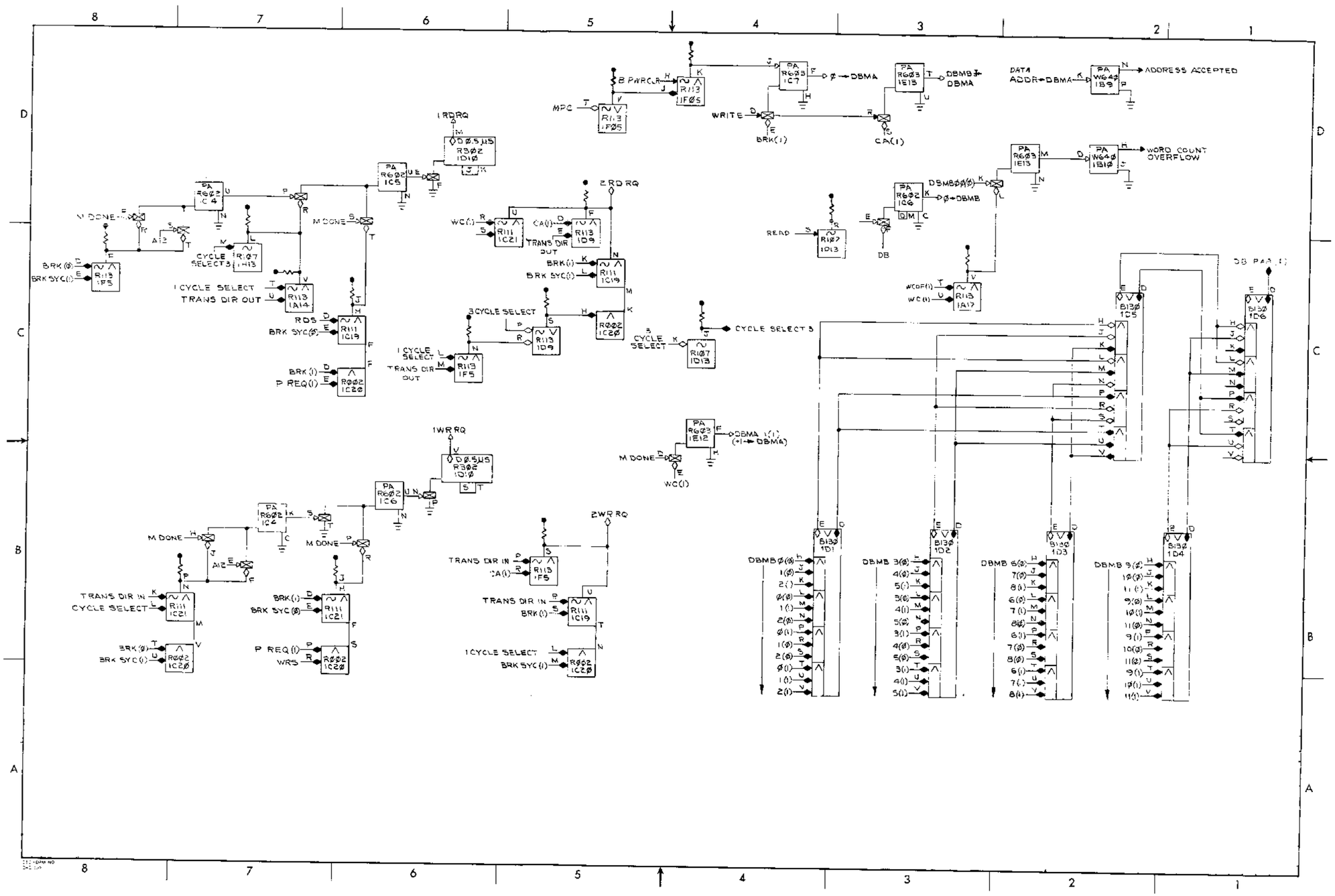
D-BS-MC8S-0-1 Extended Memory Control
(MC8S) (Sheet 3)



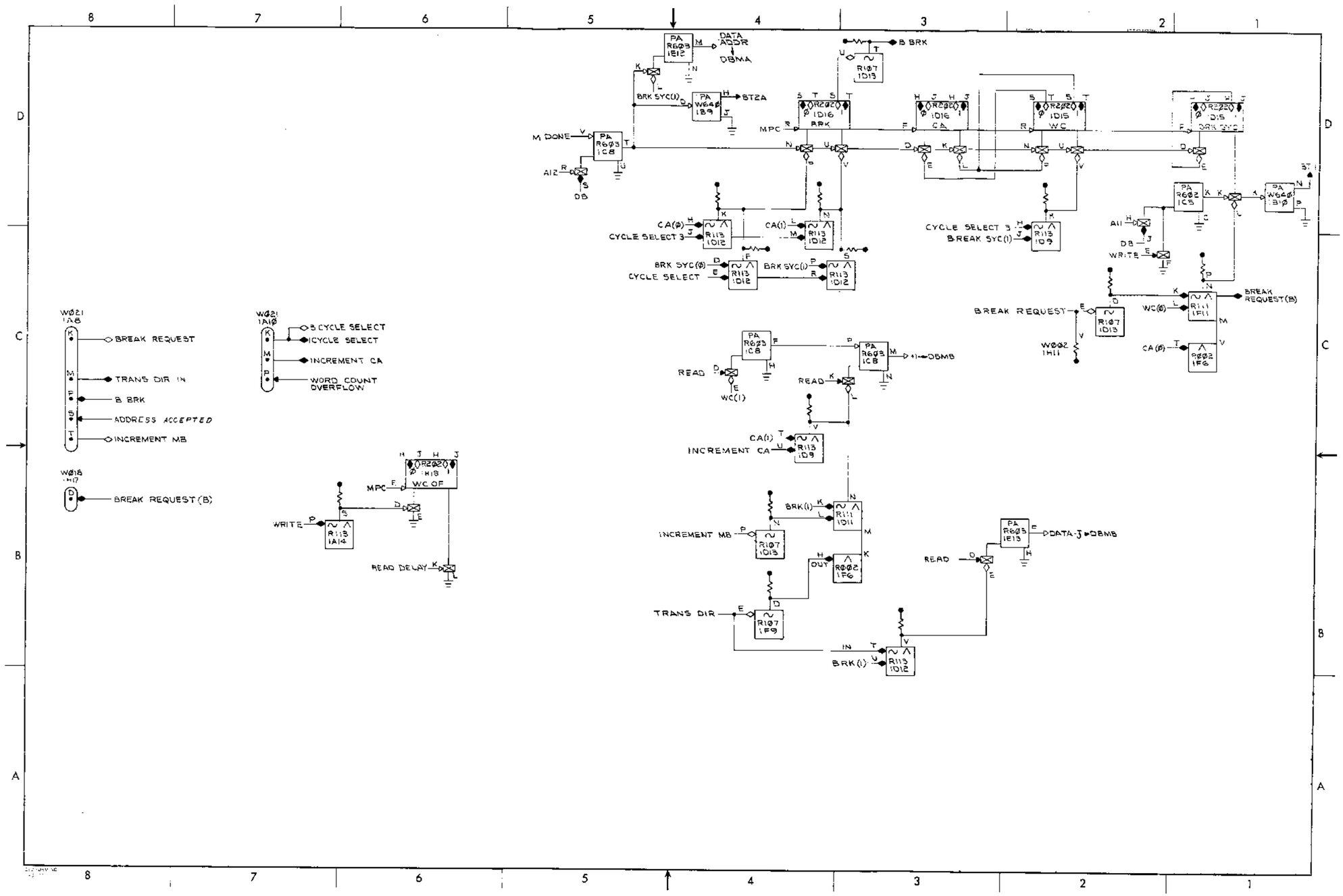
D-BS-MC8S-0-2 Memory Field 1 (MC8S)



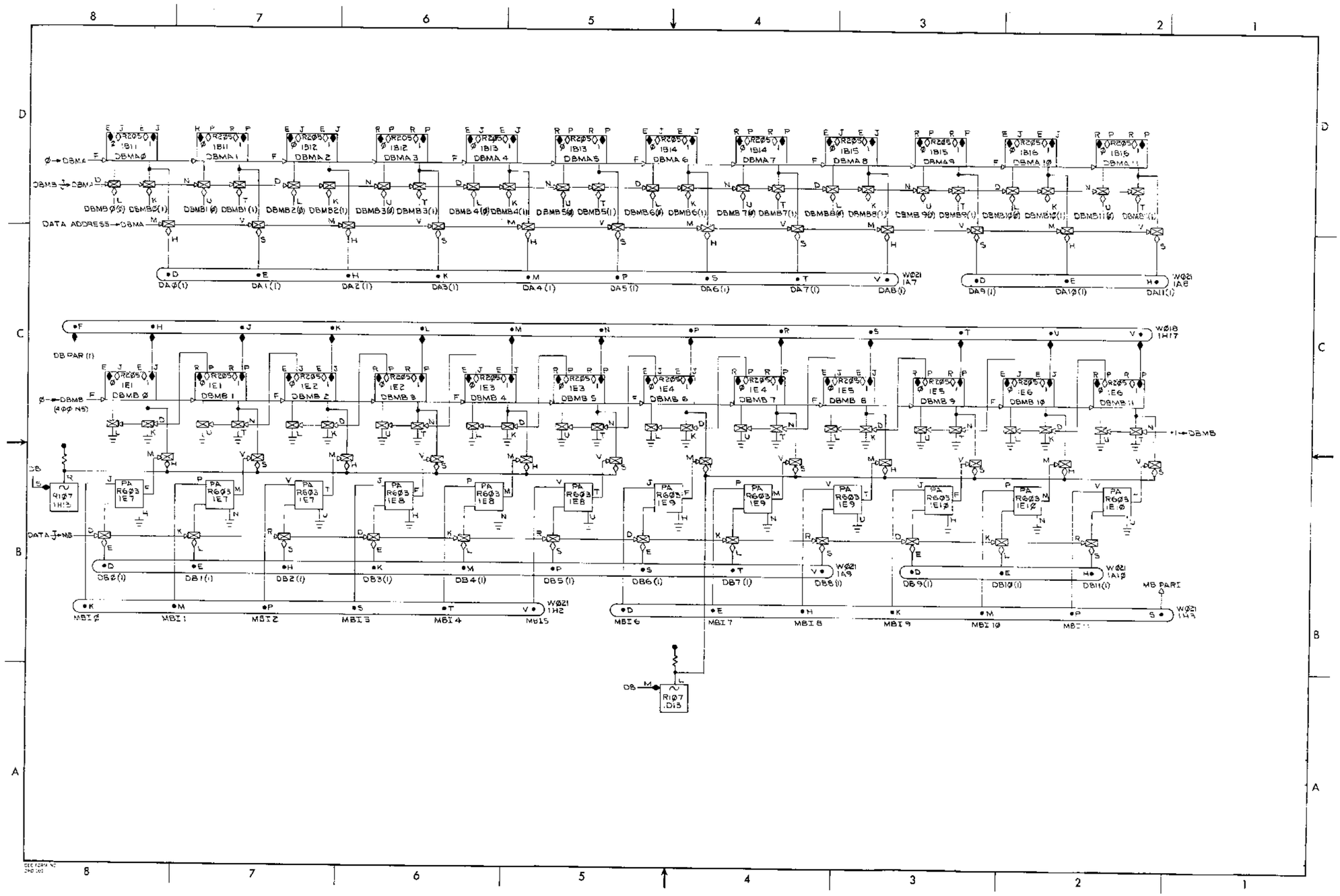
D-BS-MC8S-0-4 Flow Diagram (MC8S)



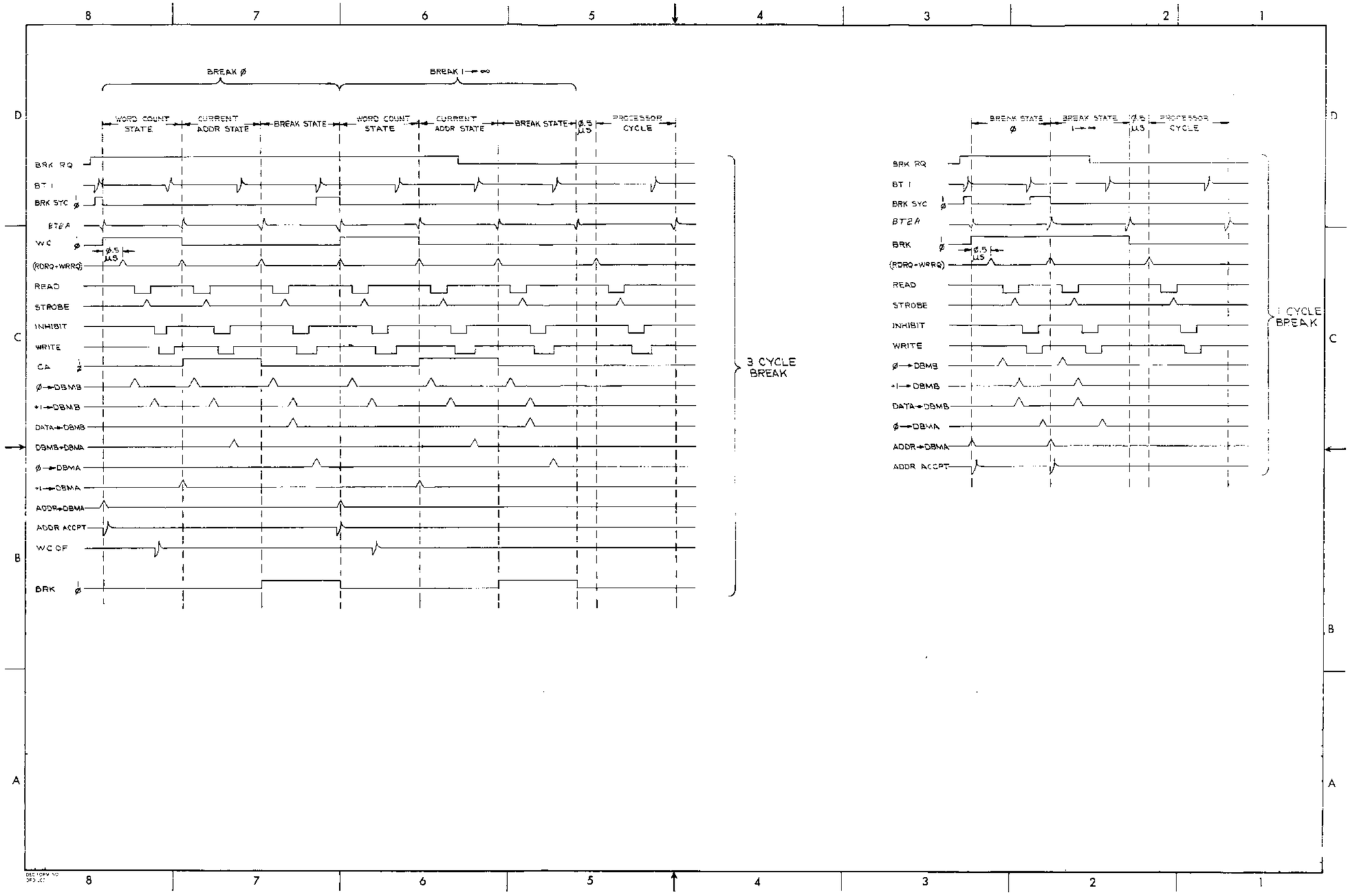
D-BS-DB8S-0-1 Control (DB8S)
(Sheet 1)



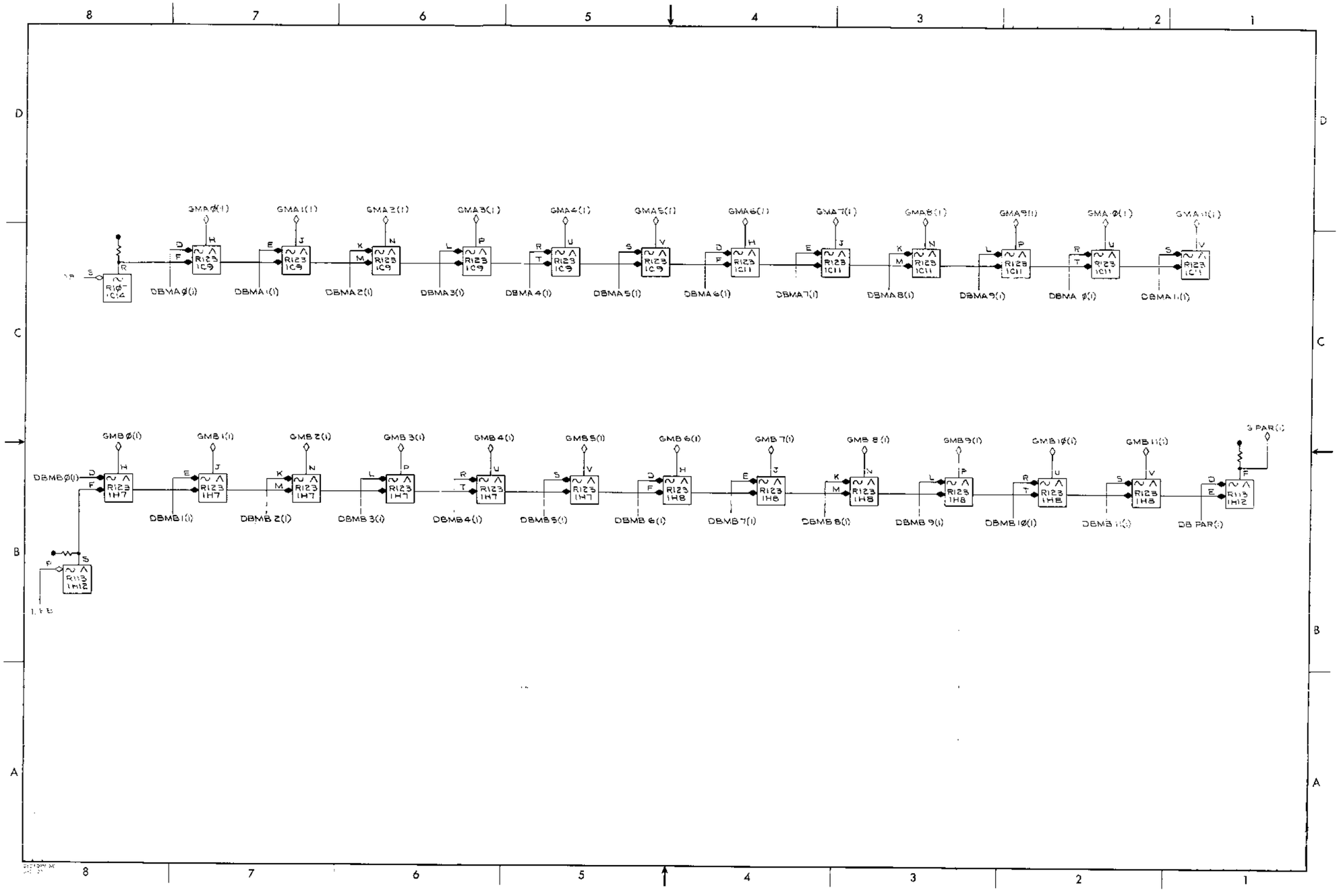
D-BS-DB8S-0-1 Control (DB8S)
(Sheet 2)



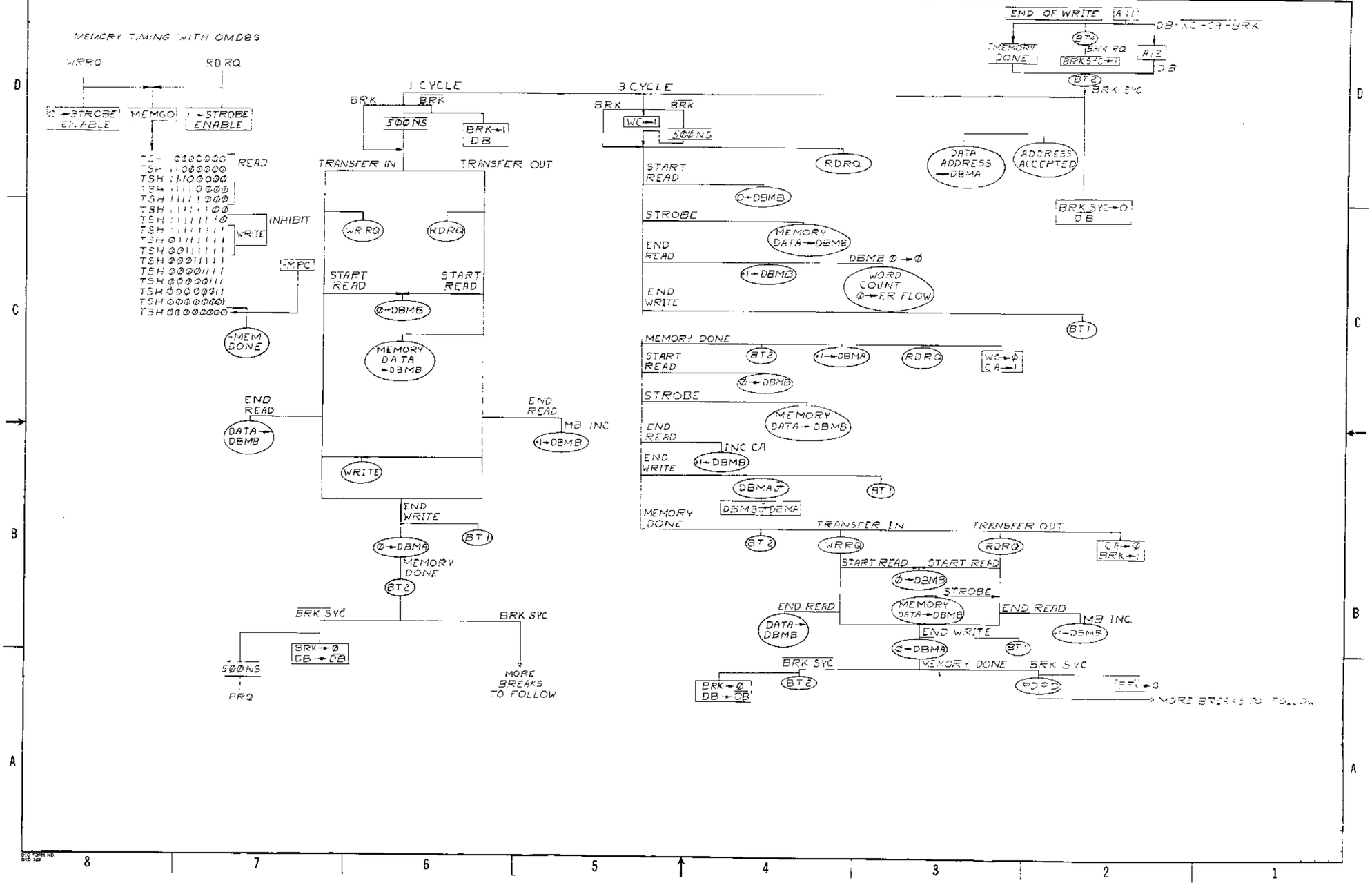
D-BS-D88S-0-2 MA and MB
Register (D88S)



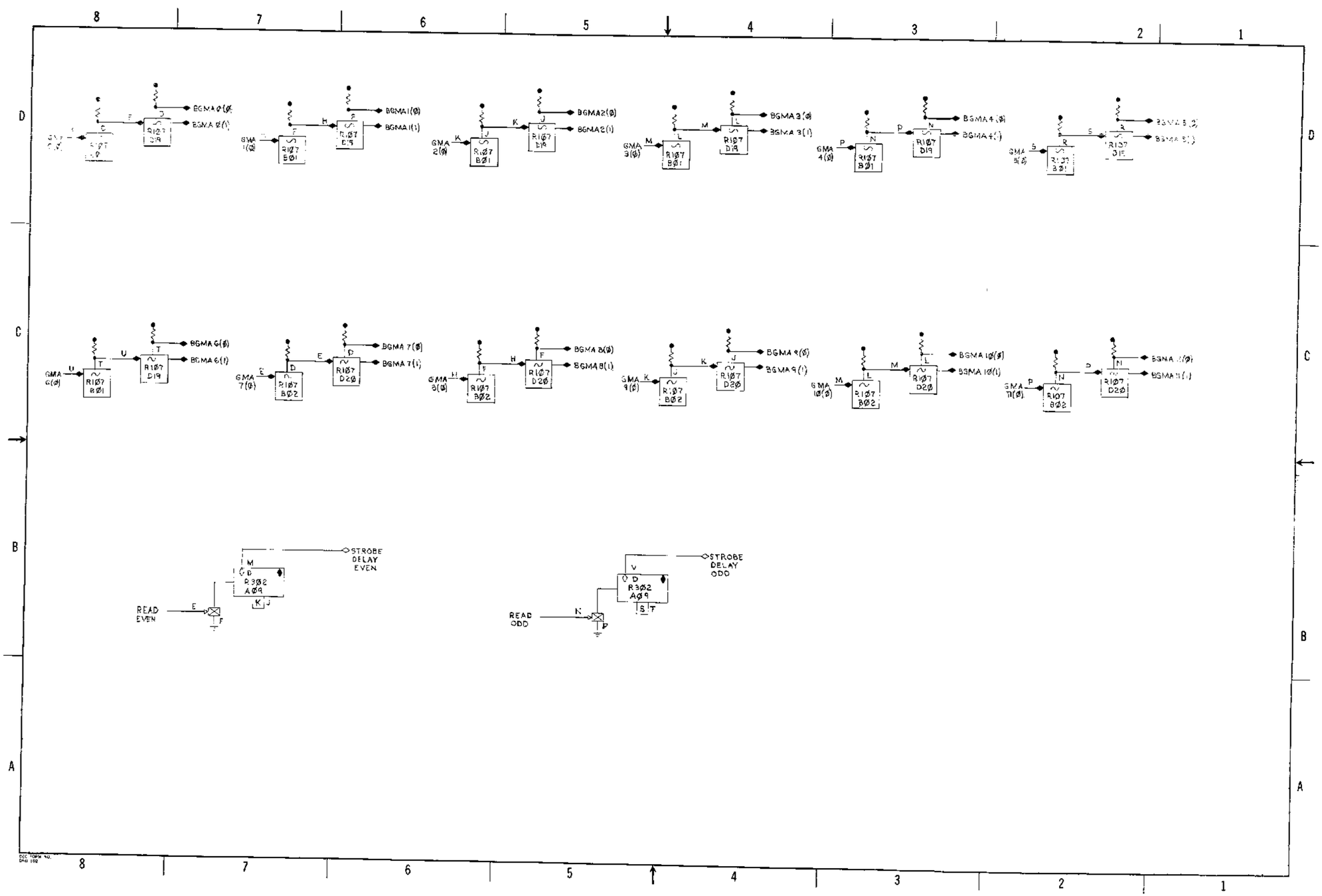
D-TD-DB8S-0-3 DB8S Timing Diagram

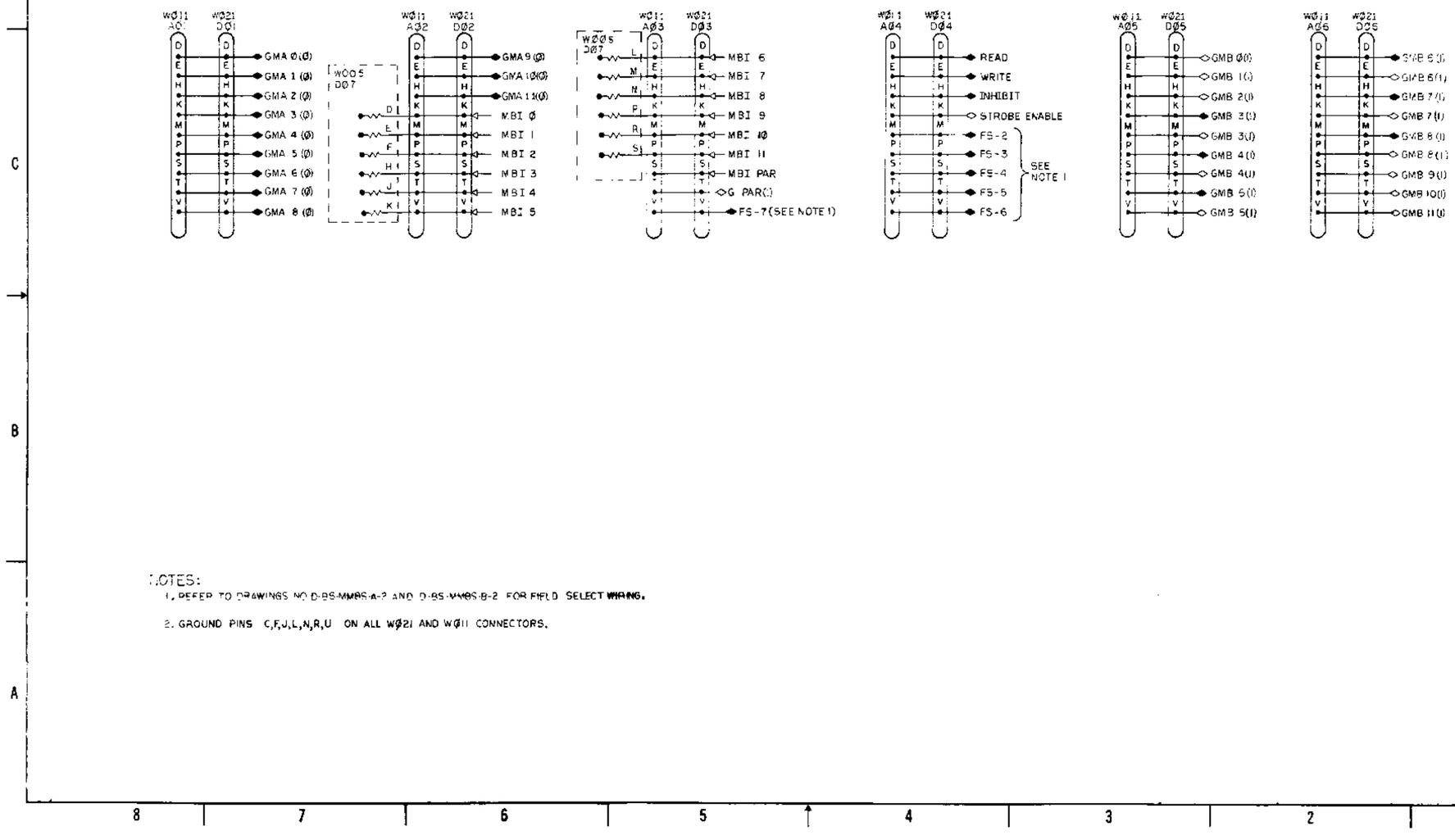


D-BS-DB8S-0-5 GMA and GMB Gating



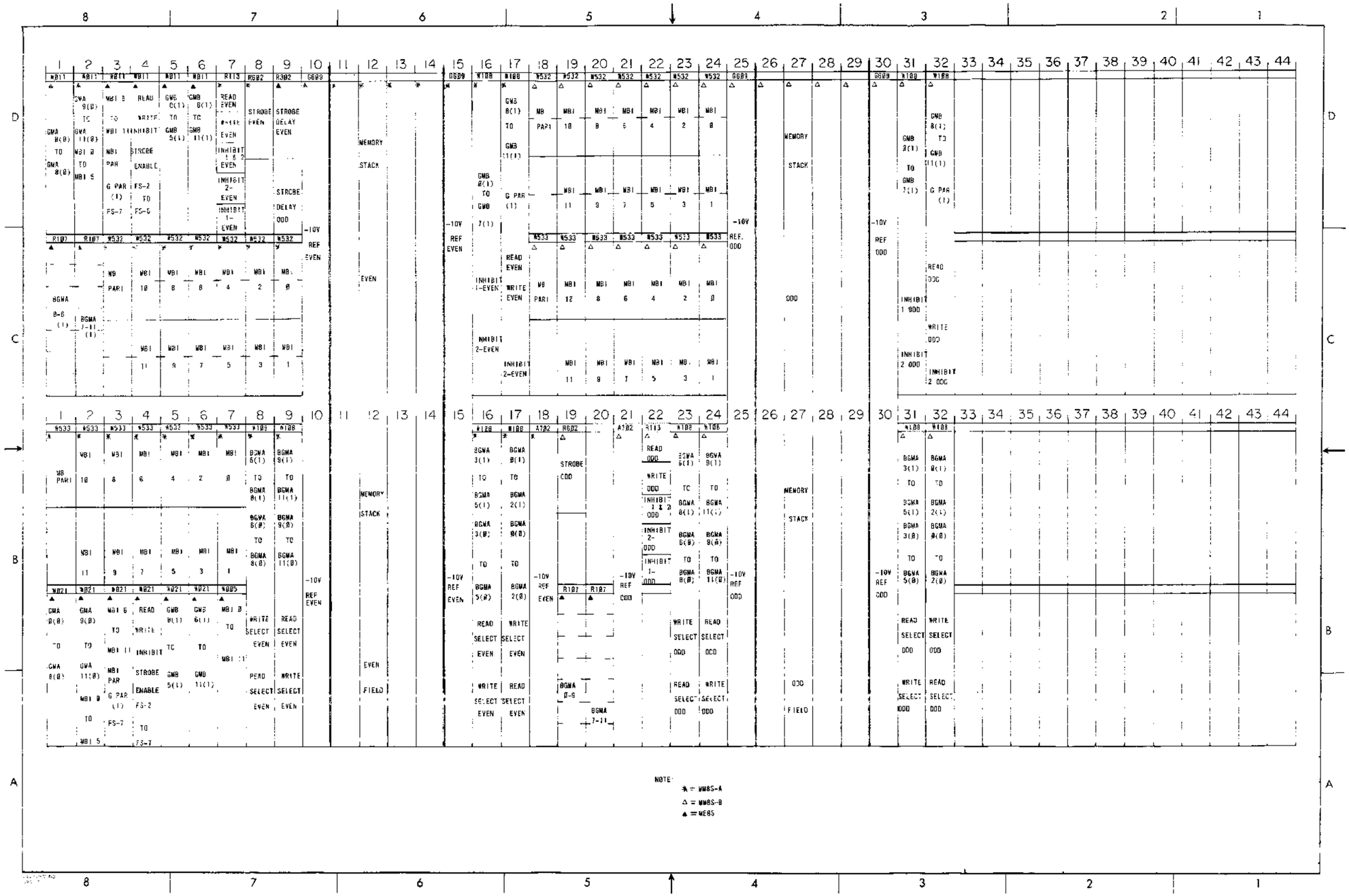
D-FD-DB8S-0-6 Flow Diagram DB8S

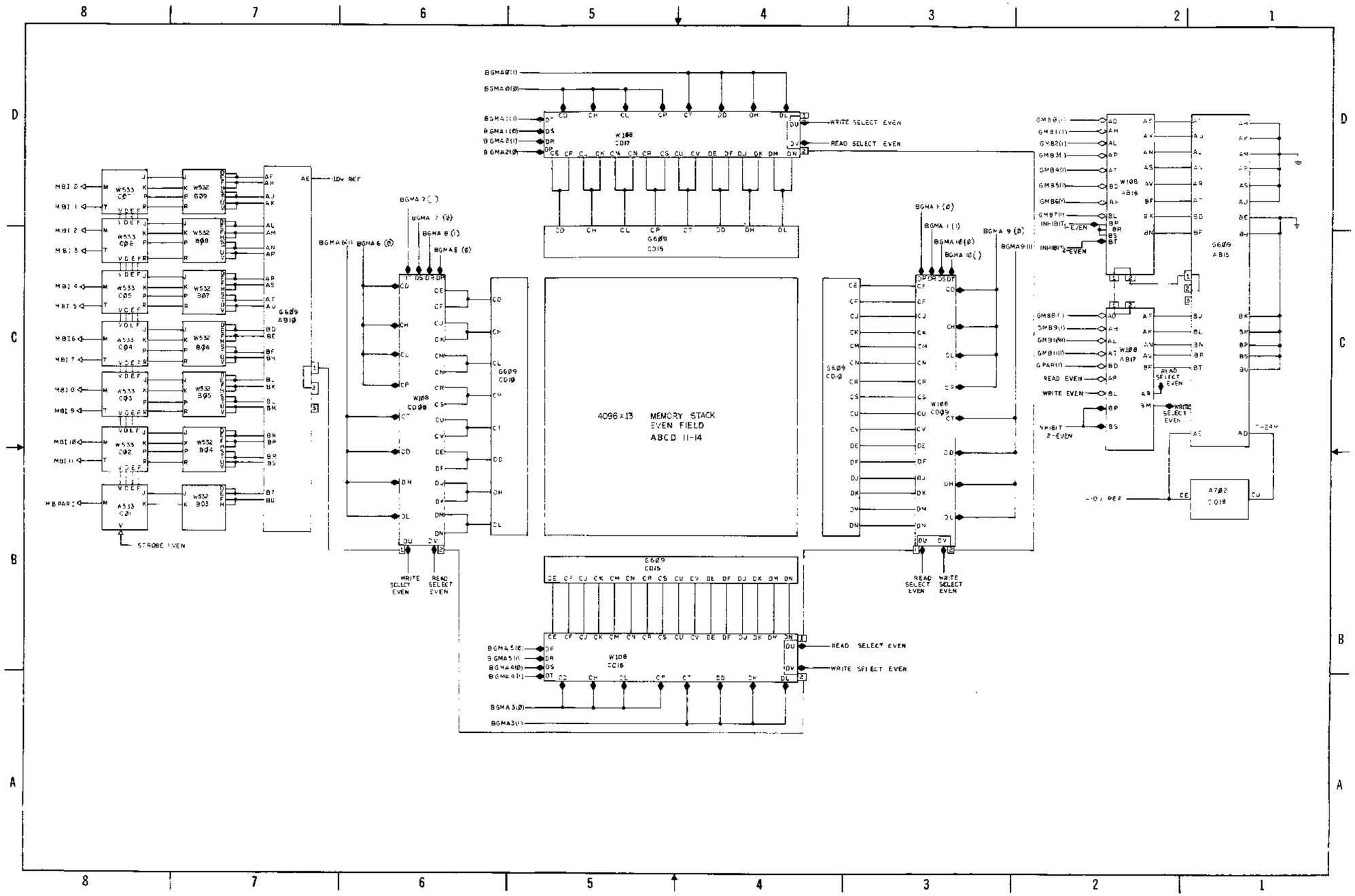

8
7
6
5
4
3
2
1
D
C
B
A
BGMA 0(Ø)
BGMA 0(1)
BGMA1(Ø)
BGMA1(1)
BGMA2(Ø)
BGMA2(1)
BGMA 3(Ø)
BGMA 3(1)
BGMA 4(Ø)
BGMA 4(1)
BGMA 5(Ø)
BGMA 5(1)
BGMA 6(Ø)
BGMA 6(1)
BGMA 7(Ø)
BGMA 7(1)
BGMA 8(Ø)
BGMA 8(1)
BGMA 9(Ø)
BGMA 9(1)
BGMA 10(Ø)
BGMA 10(1)
BGMA 11(Ø)
BGMA 11(1)
STROBE DELAY EVEN
STROBE DELAY ODD
READ EVEN
READ ODD



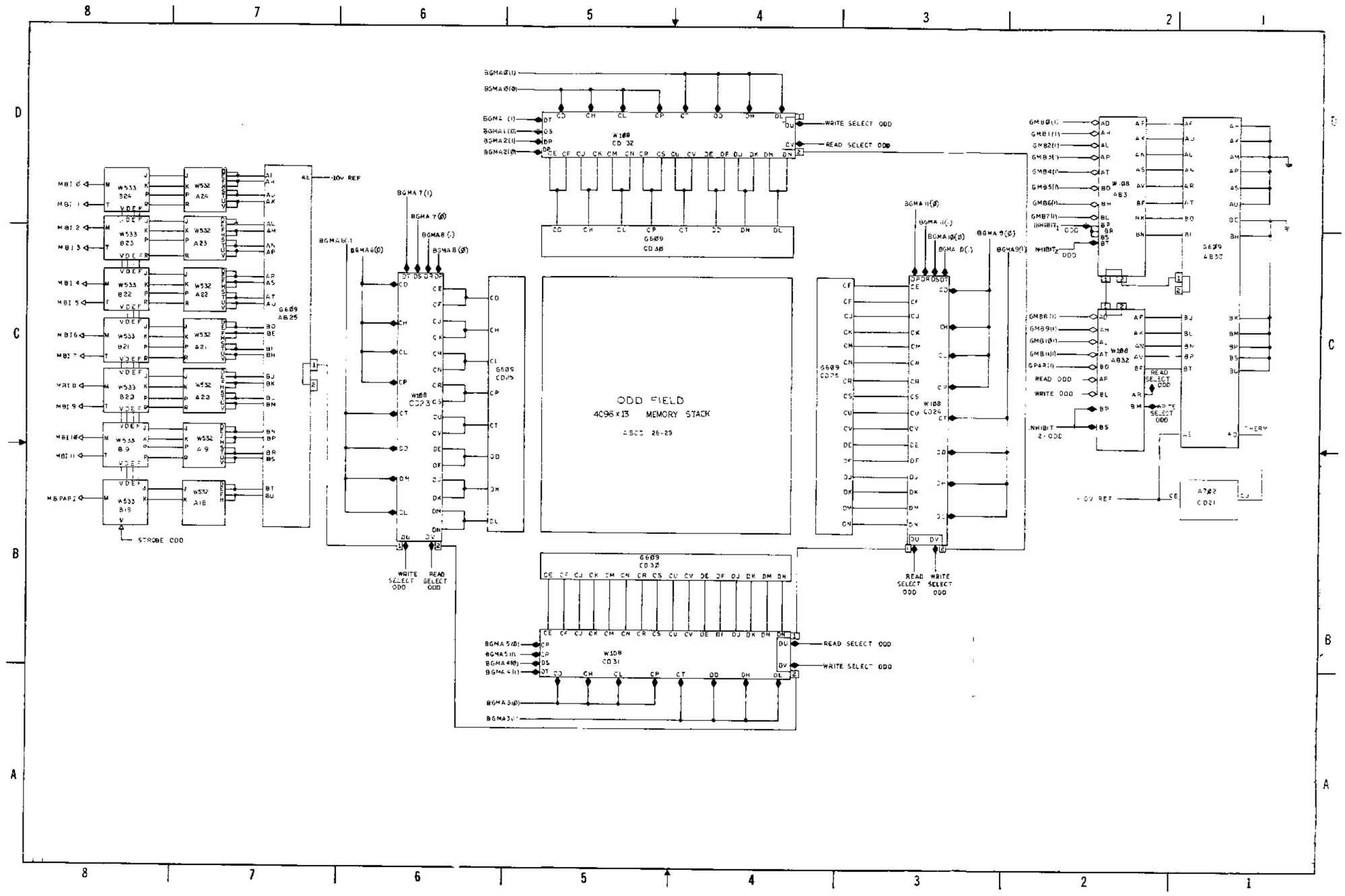
NOTES:

1. REFER TO DRAWINGS NO D-BS-MMBS-A-2 AND D-BS-MMBS-B-2 FOR FIELD SELECT WIRING.
2. GROUND PINS C,F,J,L,N,R,U ON ALL W@21 AND W@11 CONNECTORS.


NOTE:
* = MM8S-A
Δ = MM8S-B
▲ = ME8S

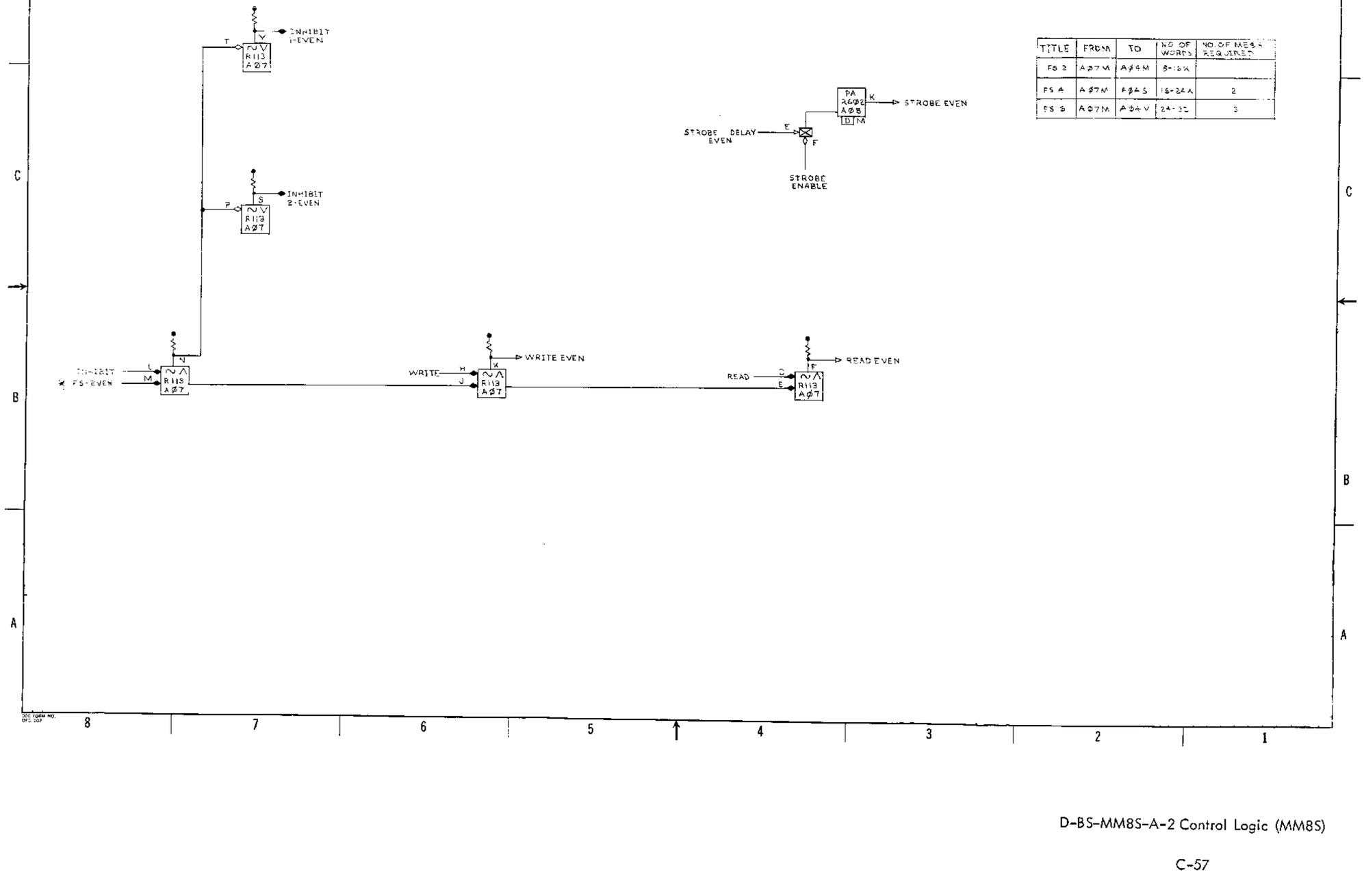


D-BS-MM8S-A-1 Memory Field Even (MM8S)


ODD FIELD
4096 x 13 MEMORY STACK
A8C0 26-29
-10V REF
STROBE CDD
WRITE SELECT ODD
READ SELECT ODD
WRITE SELECT ODD
READ SELECT ODD
READ SELECT ODD
WRITE SELECT ODD
WRITE SELECT ODD
READ SELECT ODD
WRITE SELECT ODD
INHIBIT 1 ODD
INHIBIT 2 ODD
INHIBIT 2 - ODD
READ ODD
WRITE ODD
- 6V REF

NOTE:
THE FOLLOWING CONNECTIONS FOR FIELD SELECTION SHOULD BE MADE PRIOR TO CHECKOUT

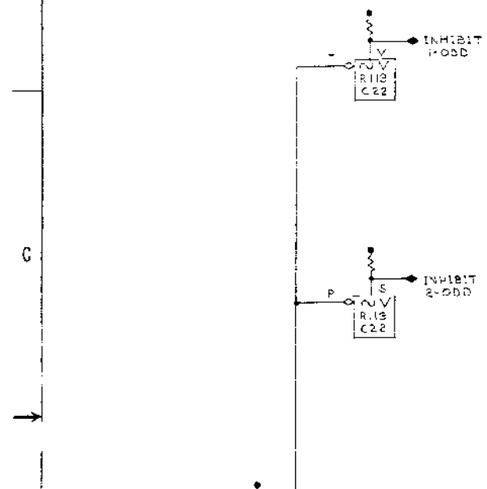
TITLE	FROM	TO	NO OF WORDS	NO. OF MEGS REQUIRED
FS 2	AØ7M	AØ4M	8-12K	
FS 4	AØ7M	AØ4S	16-24K	2
FS 6	AØ7M	AØ4V	24-32K	3

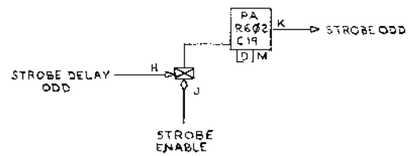


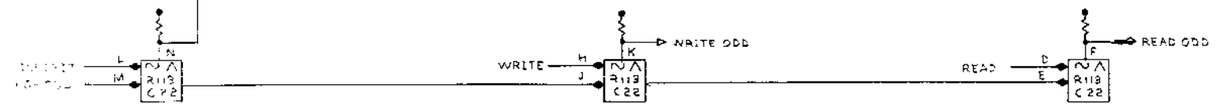
NOTE:

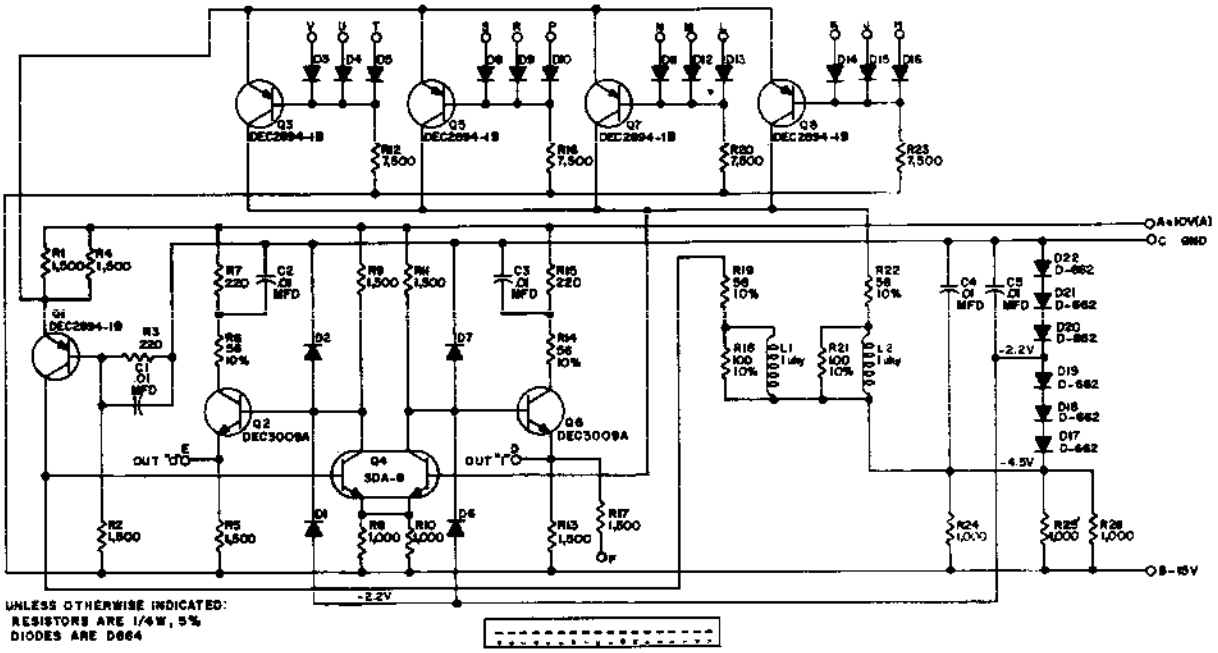
THE FOLLOWING CONNECTIONS FOR FIELD SELECTION SHOULD BE MADE TO CHECKOUT

TITLE	FROM	TO	NO OF WORDS	NO OF WDS REQUIRED
FS 3	C22 M	AØ4P	8-16K	1
FS 5	C22 M	AØ4T	16-24K	2
FS 7	C22 M	AØ3V	24-32	3

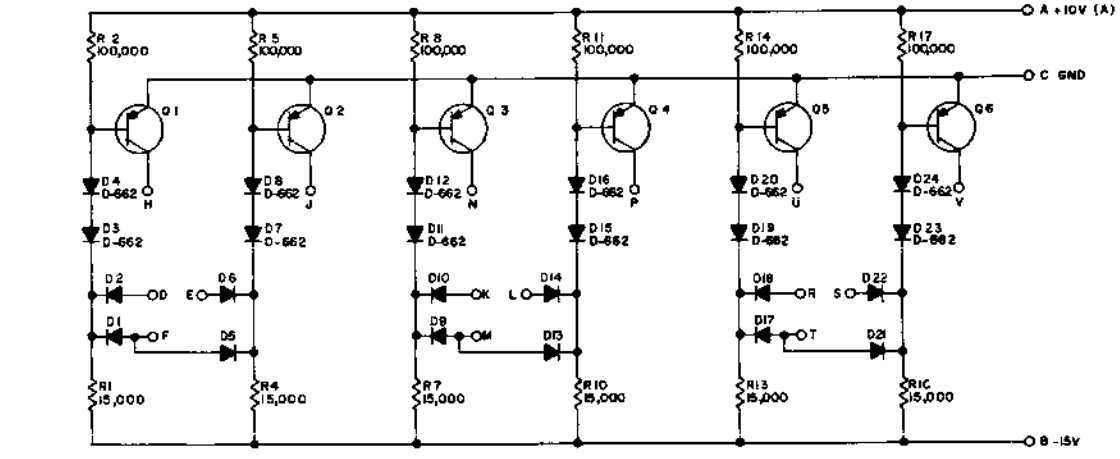






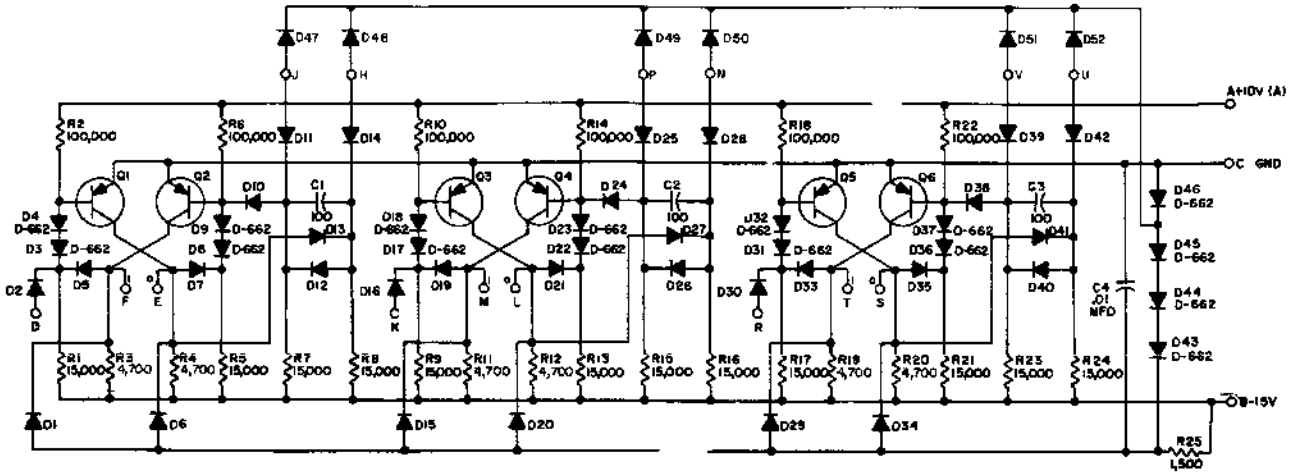


B-CS-B130

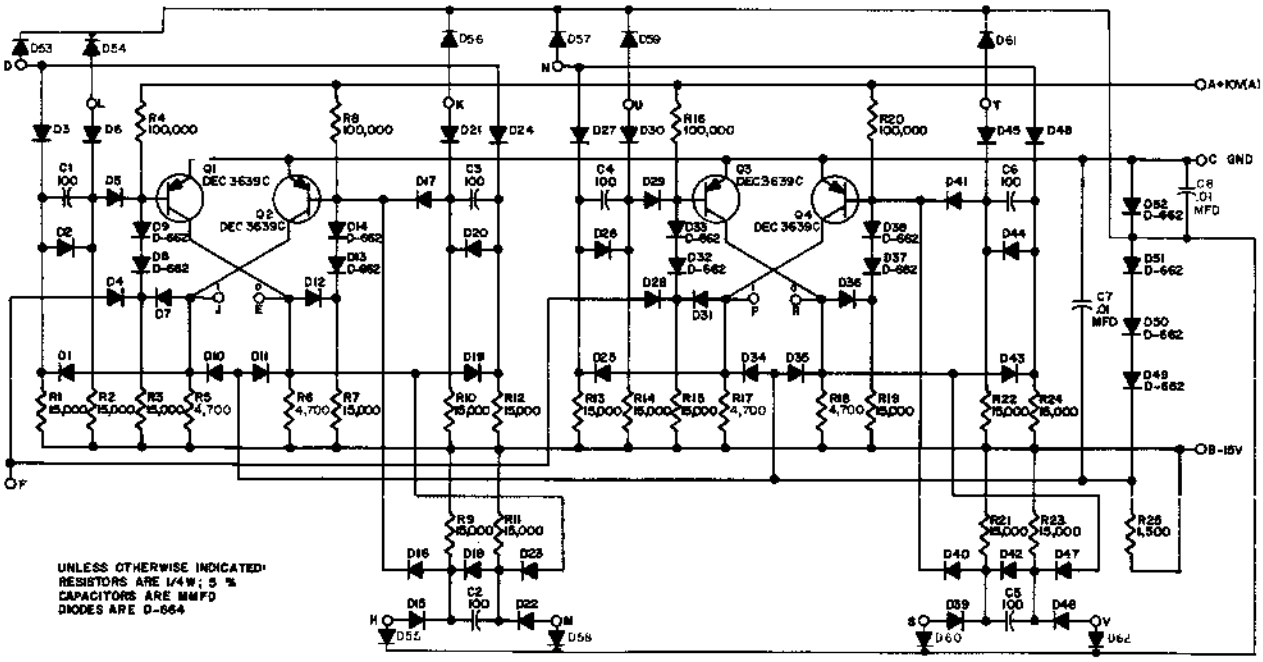


UNLESS OTHERWISE INDICATED.
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4 W, 5%
DIODES ARE D-664

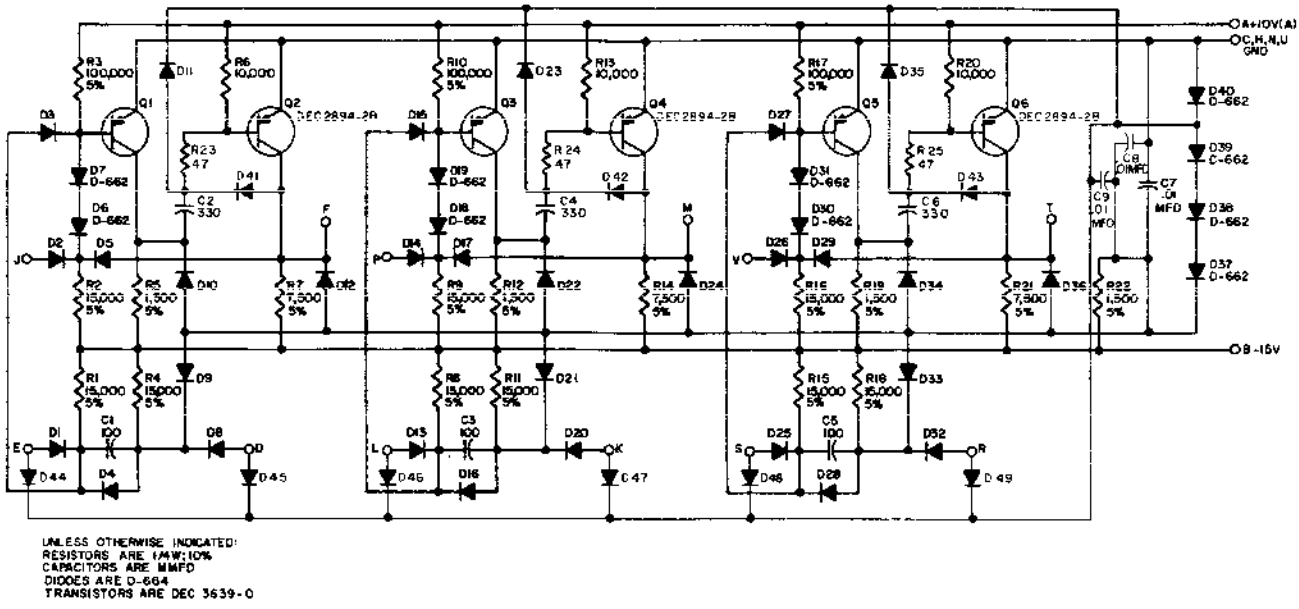
B-CS-R123-0-1 Diode Gate R123



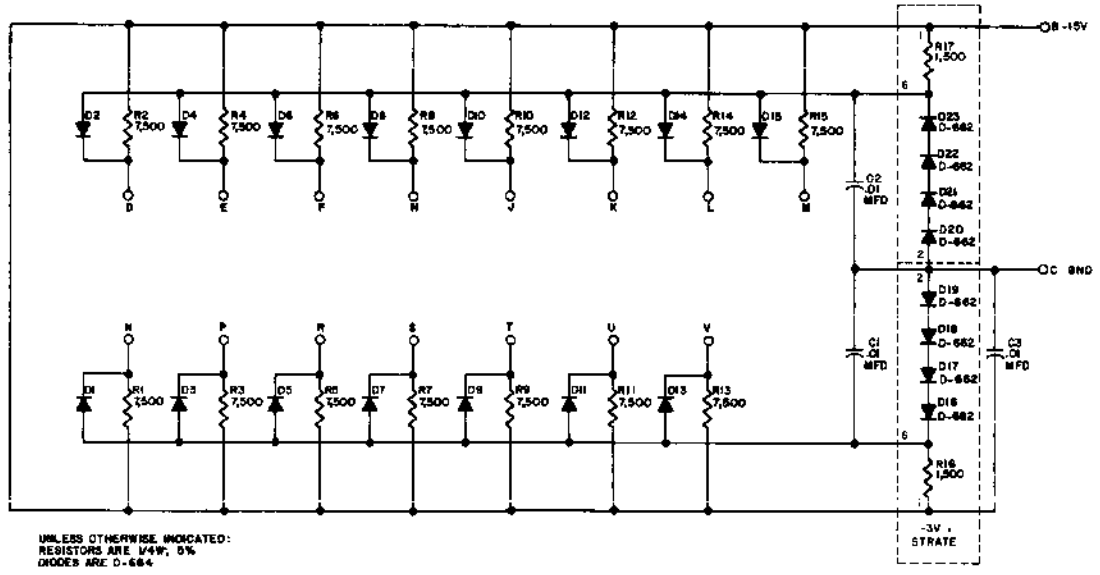
B-CS-R203 Triple Flip-Flop R203



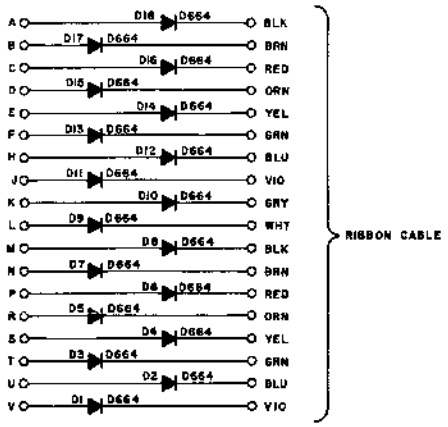
B-CS-R205 Dual Flip-Flop R205



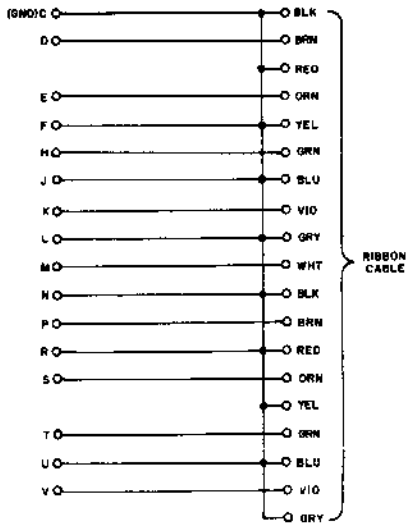
B-CS-R603



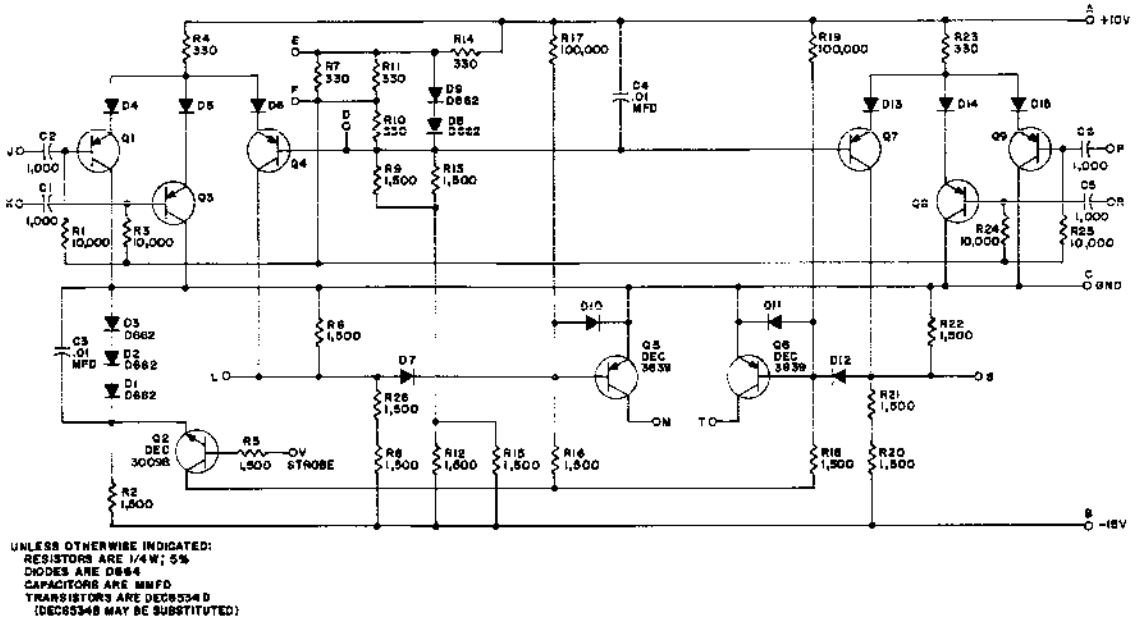
B-CS-W002-0-1 Clamp Loads W002



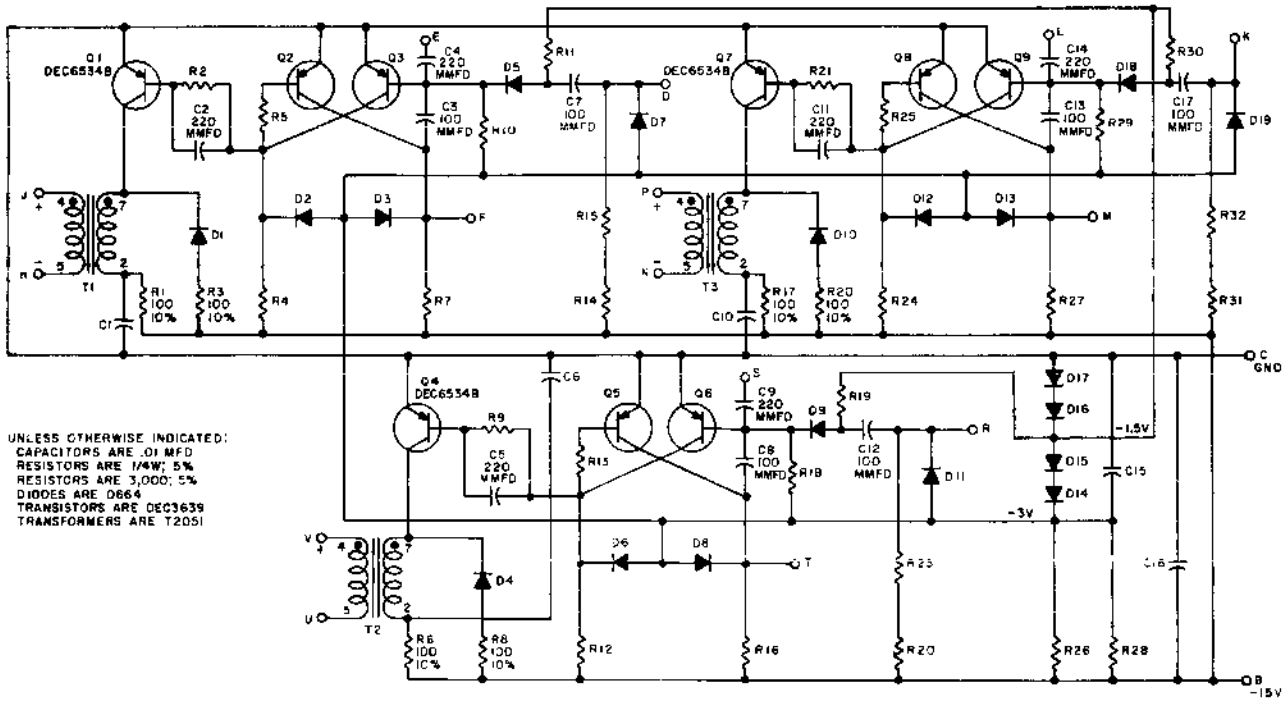
B-CS-W018-0-1 Indicator Connector



B-CS-W021 Signal Cable Connector



B-CS-W533-0-1 Rectifying Slicer



B-CS-W640

GLOSSARY
MEMORY EXPANSION AND DATA BREAK OPTIONS

Terms	Option-Page-Sheet	Definition
ADDRESS ACCEPTED	DB8S-1-1	Notifies data break device that the supplied address has been stored in DBMA
A00	MC8S-1-3	Processor bit time 0 pulse
A11,A12	OMD8S-4-2	Processor bit time 11, 12 pulses
-A13 (B)	OMD8S-4-2	Processor bit time 13 pulse
B BRK	DB8S-1-2	Break state data transfer cycle in process
BMA0(1) through BMA11(1)	OMD8S-4-2	Processor MA output bus (isolated)
BREAK REQUEST (B)	DB8S-1-2	External break request, inverted
-BT00(B)	OMD8S-4-2	Bit time 0 level
BT1	DB8S-1-2	Data break timing pulse
BT2A	DB8S-1-2	Data break timing pulse
B(WTX)	OMD8S-4-2	Processor WTX level
CDF	MC8S-1-3	IOP1 pulse during CDF instruction
-CLR	OMD8S-4-2	Reset IF, IB, DF during WTB, power failure, or load address
CYCLE SELECT 3	DB8S-1-1	3-cycle select, inverted
DA0 through DA11	DB8S-2	Externally applied address lines
DATA ADDR ⟶ DBMA	DB8S-1-2	Sets DA lines into DBMA register
DATA ⟶| DBMB	DB8S-1-2	Jam transfers DB lines into DBMB register
DATA FIELD 0-2	MC8S-1-3	DF register output to external equipment
DB	OMD8S-6	Data break in process
DB	OMD8S-7	
DBB	OMD8S-7	
DBMA1 through DBMA11	DB8S-2	Data break address register
DBMA11 (1)	DB8S-1-1	Increment DBM?
DBMB ⟶ DBMA	DB8S-1-1	
DBMB0 through DBMB11	DB8S-2	Data break data register
DB PAR (1)	DB8S-1-1	
DB PARITY		See 1H17 F (DB8S-2)
DCA (B)	OMD8S-4-2	Processor DCA instruction
DCA	MC8S-1-3	

Terms	Option-Page-Sheet	Definition
DEF	MC8S-1-3	Referred operand fetch in process; use DF register to select memory field
DF0 through DF2	MC8S-1-1	Data field register
DSDF	MC8S-1-1	Enable inputs to DF register
DSIB	MC8S-1-1	Enable inputs to IB register
DSIF	MC8S-1-1	Enable inputs to IF register
-FR	OMD8S-4-1	Interrupt inhibit after CIF instruction
FS0 through FS7	MC8A-1-2	Memory field select levels
GMA0 through GMA11	OMD8S-6	OMD8S memory address bus; gated from processor MA or data break DBMA
GMB0 through GMB11	OMD8S-7	OMD8S memory input (write) data bus; gated from processor MB or data break DBMB
IB0 through IB2	MC8S-1-1	Instruction buffer register
IF0 through IF2	MC8S-1-1	Instruction field register
IM6 through IM11	MC8S-1-2	Input to AC from DF, SF, IF registers
INHIBIT	OMD8S-4-1	OMD8S memory inhibit level
INHIBIT 1 ODD	MM8S-B-2	Odd memory field inhibit level
INHIBIT 2 ODD	MM8S-B-2	Odd memory field inhibit level
INHIBIT 1 EVEN	MM8S-A-2	Even memory field inhibit level
INHIBIT 2 EVEN	MM8S-A-2	Even memory field inhibit level
INHIBIT 2-0, 1-0	OMD8S-5	Field 0 memory inhibit levels
INHIBIT 2-1, 1-1	MC8S-2	Field 1 memory inhibit levels
IOP1, 2, 4	MC8S-1-2	Processor IOP pulses
(JMP + JMS)	OMD8S-4-2	JMP or JMS instruction in effect
LCDF	MC8S-1-3	CDF instruction (level)
LCIF	MC8S-1-3	CIF instruction (level)
LD (B)	OMD8S-4-2	Load address word time
LD	MC8S-1-3	
LID	MC8S-1-3	A00.LD
LRMF	MC8S-1-2	RMF instruction (level)
MBI0 through MBI11	OMD8S-5 MC8S-2 MM8SA-1 MM8SB-1	ORed output data bus from all memory modules
MB PAR I	OMD8S-5 MC8S-2 MM8SA-1 MM8SB-1	ORed parity output bit from all memory modules

Terms	Option-Page-Sheet	Definition
MCA through MCH	OMD8S-4-1	OMD8S memory timing ring counter
M DONE	OMD8S-7	Auxiliary MBM DONE
MEM DONE	OMD8S-4-1	Memory cycle complete
MPS	OMD8S-6	OMD8S parity bit to processor MB
P DONE	OMD8S-7	End of processor memory cycle (resets WTS)
P PRQ	OMD8S-7	Initiate processor memory cycle
P REQ	OMD8S-7	Processor waiting for memory cycle
RB	MC8A-1-1	Reset IB register (pulse)
RD	MC8S-1-1	Reset DF register (pulse)
RDF	MC8S-1-2	IOP4 pulse during RDF instruction
RD RQ	OMD8S-7	Start memory read cycle
RDS	OMD8S-7	Processor read cycle request
READ	OMD8S-4-1	Memory read time
READ	OMD8S-5	End-of-read pulse
READ DELAY	OMD8A-5	Memory field 0 strobe trigger (sets WCOF)
READ EVEN	MM8SA-2	Read pulse for even memory fields
READ ODD	MM8SB-2	Read pulse for odd memory fields
READ 1	MC8S-2	Field 1 read level
RI	MC8S-1-1	Reset IF register (pulse)
RIB	MC8S-1-2	IOP4 pulse during RIB instruction
RIF	MC8S-1-2	IOP4 pulse during RIF instruction
RMF	MC8S-1-2	IOP4 pulse during RMF instruction
-RSF	MD8S-4-2	Reset SF register (pulse)
SCDF	MC8S-1-3	IOT 62XX instruction in effect
SDF0 through SDF2	8S-15	DATA FIELD switch outputs
SF0 through SF5	MC8S-1-1	SF (save field) register
SIF0 through SIF2	8S-15	
SIF0 through SIF2	MC8S-1-1	INSTR FIELD switch outputs
SMB00 through SMB11	MD8S-6	MBI bus gated to processor MB register (non-break cycles)
STROBE ENABLE	OMD8S-4-1	Memory strobe enable
STROBE EVEN	MM8SA-2	Strobe pulse trigger for even memory field
STROBE ODD	MM8SB-2	Strobe pulse trigger for odd memory field
STROBE 0	OMD8S-5	Strobe pulse to memory field 0
STROBE 1	MC8S-2	Strobe pulse to memory field 1

Terms	Option-Page-Sheet	Definition
WCOF	DB8S-1-2	Time bracket for word count overflow detection
WORD COUNT OVERFLOW	DB8S-1-1	End of block transfer signal to device during 3-cycle breaks
WRITE	OMD8S-4-1	Write command to all memory modules
WRITE EVEN	MM8SA-2	Write pulse for even memory fields
WRITE ODD	MM8SB-2	Write pulse for odd memory fields
WRITE 0	OMD8S-5	Field 0 write level
WRITE 1	MC8S-2	Field 1 write level
WR RQ	OMD8S-7	Start memory write cycle
WRS	OMD8S-7	Processor write cycle request
WTB·A00 (B)	OMD8S-4-2	Word time B, bit time 0 (pulse)
WTD	OMD8S-4-2	Word time D
WTF	OMD8S-4-2	Word time F
WTF (LCIF)	MC8S-1-3	See WTR, LCIF
WTF (JMP + JMS)	MC8S-1-3	See WTF (JMP + JMS)
WTF (LCDF + LRMF)	MC8S-1-3	See WTF, LCDF, LRMF
WTX (JMP + JMS) (B)	OMD8S-4-2	Word time X; see (JMP + JMS)
0 ⟶ DBMA	DB8S-1-1	Reset DBMA register (pulse)
0 ⟶ DBMB	DB8S-1-1	Reset DBMB register (pulse)
1RDRQ	DB8S-1-1	Data break memory read request
1WRRQ	DB8S-1-1	Data break memory write request
2RDRQ	DB8S-1-1	Data break memory read request
2WRRQ	DB8S-1-1	Data break memory write request
+1 ⟶ DBMA	DB8S-1-1	Set DBMA11 (adds 1 to word count location to form current address location)
+1 ⟶ DBMB	DB8S-1-2	Increment DBMB (carries are propagated)

PDP LOG DATE ______

USER	METER ON&OFF	TIME ON&OFF	EQUIPMENT USED AND PERFORMANCE

MAINTENANCE PERFORMED DATE_____