DESCRIPTION

These devices are 2-input, 4-bit Digital Multiplexers designed for general purpose data-selection applications.

The 8233 features *non-inverting* data paths; and, the 8234 features *inverting* data paths.

The 8235 is designed for input to adders, registers and general paralleled data handling due to its capability to perform CONDITIONAL COMPLEMENTING (TRUE/COMPLEMENT). When the two inputs for each bit position (Ai, Bi) are connected together, the f output will provide either the *True* or *Complement* of the input data. This capability is especially useful for transferring data into parallel adders where both true data for adding or multiplying and also complemented data for subtracting or dividing are needed.

The 8234 and 8235 designs have open collector outputs which permit direct wiring to other open collector outputs (collector logic) to yield "free" four-bit words. As many as one hundred four-bit words can be multiplexed by using fifty 8234/8235s in the WIRED-AND mode.

The inhibit state $S_0 = S_1 = 1$ can be used to facilitate transfer operations in an arithmetic section.

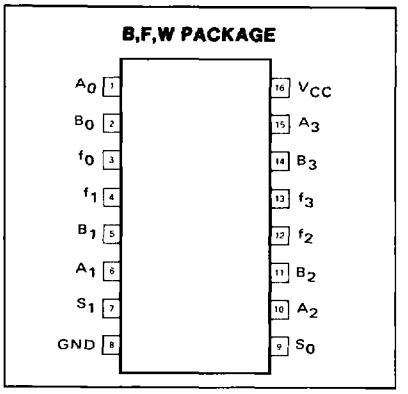
TRUTH TABLE

	S_0	S_1	f_n
8233/82S33	0	0	B
	1	0	A
	0	1	B
	1	1	0
8234/82S34	0	0	$\overline{B}$
	1	0	$\overline{A}$
	0	1	$\overline{B}$
	1	1	1
8235	0	0	$\overline{A}_n B_n$
	0	1	B_n
	1	0	$\overline{A}_n$
	1	1	1

V_{CC} = (16)
GND = (8)
( ) = denotes pin numbers

PIN CONFIGURATION

B,F,W PACKAGE

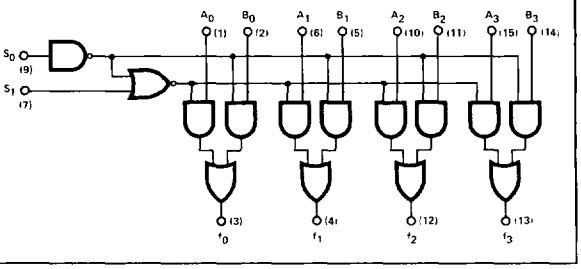


SPEED/PACKAGE AVAILABILITY

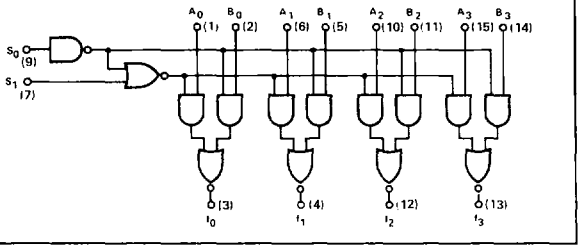
8233, 34, 35—B, F, W
82S33, S34—B, F

LOGIC DIAGRAMS

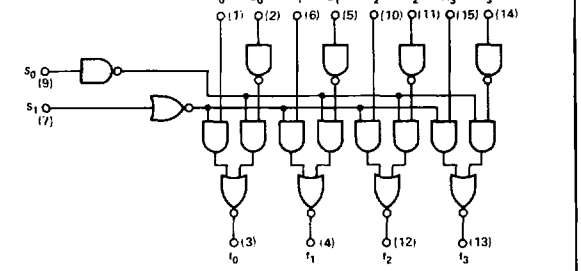
8233/82S33 (ACTIVE PULL-UP)



8234/82S34 (OPEN COLLECTOR)

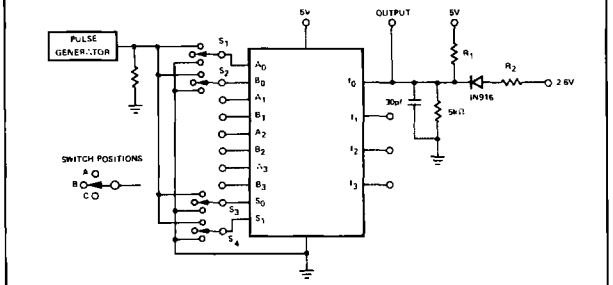


8235 (OPEN COLLECTOR)



AC TEST FIGURE

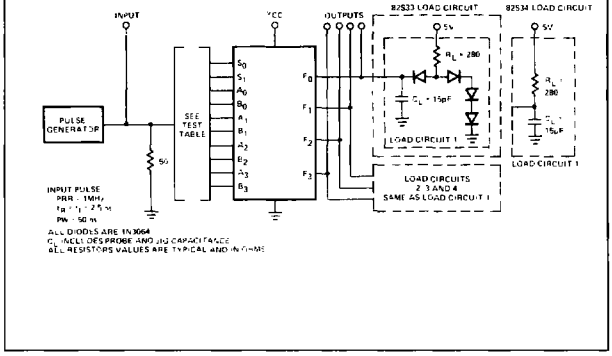
8233/34/35



	R_1	R_2
8233	∞	84.5Ω
8234 8235	360Ω	440Ω

Input pulse:
Amplitude = 2.6v
PW = 200ns
PRR = 1 MHz
$t_r = t_f$ = 5ns

82S33, 82S34

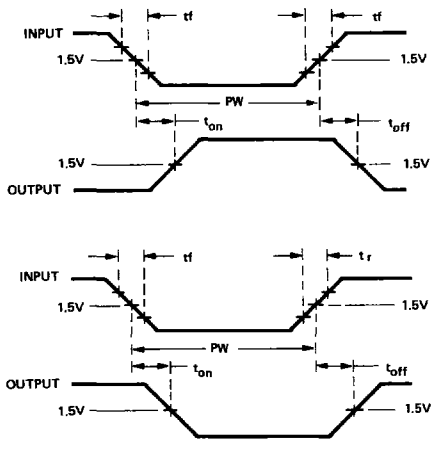


SWITCHING CHARACTERISTICS T_A=25°C, V_{CC}=5V

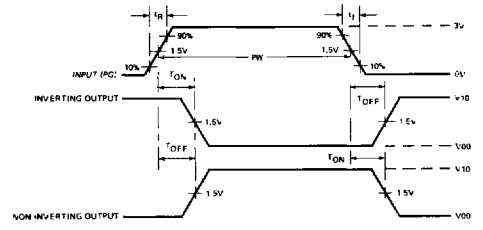
	LIMITS										
	8233		8234		8235		82S33		82S34		UNIT
PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
t_{on} Turn-on Time											
A_n,B_n to f_n	16	25	16	25	-	-	7	12	7	12	ns
S_o to f_n	27	38	27	38	27	38	13	18	13	18	ns
S_I to f_n	27	38	27	38	27	38	11	16	11	16	ns
A_n to f_n	-	-	-	-	16	25	-	-	-	-	ns
B_n to f_n	-	-	-	-	24	35	-	-	-	-	ns
t_{off} Turn-off Time											
A_n, B_n to f_n	16	25	16	25	-	-	7	12	7	12	ns
S_o to f_n	27	38	27	38	27	38	13	18	13	18	ns
S_I to f_n	27	38	27	38	27	38	11	16	11	16	ns
A_n to f_n	-	-	-	-	16	25	-	-	-	-	ns
B_n to f_n	-	-	-	-	24	35	-	-	-	-	ns

PULSE REQUIREMENTS

82S33/82S34



82S33/82S34



AC TEST CONDITIONS— 8233, 8234, 8235

PRODUCT	PATH	PARAMETER	S_1	S_2	S_3	S_4
ALL	A_0 to f_0	$\frac{t_{on}}{t_{off}}$	a	b	b	c
8233 8234	B_0 to f_0	$\frac{t_{on}}{t_{off}}$	c	a	c	b
8233 8234	S_0 to f_0	$\frac{t_{on}}{t_{off}}$	b	b	a	b
8233 8234	S_0 to f_0	$\frac{t_{on}}{t_{off}}$	b	c	a	c
8235	B_0 to f_0	$\frac{t_{on}}{t_{off}}$	c	a	c	b
8235	B_0 to f_0	$\frac{t_{on}}{t_{off}}$	b	c	a	b
8235	S_1 to f_0	$\frac{t_{on}}{t_{off}}$	b	b	c	a
8233 8234	S_1 to f_0	$\frac{t_{on}}{t_{off}}$	b	c	b	a

AC TEST CONDITIONS—82S33, 82S34

TEST	INPUTS										OUTPUTS			
NO.	S_0	S_1	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3
1	PG	0	1	0	1	0	1	0	1	0	T			
2	PG	0	1	0	1	0	1	0	1	0	T	T	T	T
3	PG	0	0	1	0	1	0	1	0	1		T		
4	1	PG	1	0	1	0	1	0	1	0			T	
5	0	0	0	PG	0	0	0	0	0	0	T			
6	0	1	0	0	0	PG	0	0	0	0		T		
7	1	0	0	0	0	0	PG	0	0	0			T	
8	1	0	0	0	0	0	0	0	PG	0				T

"1"=2.7V "0"=GROUND

NOTE
1. AC test jigs must not have any switches.
2. AC test jigs must have less than 1/8 inch lead length from package pins.

LOGIC