CHAPTER 8
TD8-E DECTAPE CONTROL

SECTION 1 INTRODUCTION

The TD8-E Simple DECtape Control is used to control a TU56M or TU56MH Tape Drive Unit (Figure 8-1). The TD8-E controls the assembly and disassembly of data to be read from or written onto the DECtape and provides control signals to the drive unit. The TD8-E logic is on one quad board, Module M868, that is inserted into the PDP-8/E OMNIBUS and connected to a single or dual TU56M Tape Drive by a 7008447 cable.

The TD8-E controls the direction and motion of the tape drive unit with signals generated by flip-flops in the Command Register. The Command Register allows the TD8-E to select even or odd tape drive, start and stop, move forward or reverse, and read or write by changing the state of four flip-flops. These flip-flops are controlled by an instruction (SDLC) that loads the Command Register with four bits of data from the AC.

The assembly and disassembly of the 12 data bits takes place in the Data Register. The Data Register contains the gating and register necessary to receive data from and place data on the OMNIBUS. The Data Register takes serial data from the tape during a read operation and puts serial data on the tape during a write operation.*

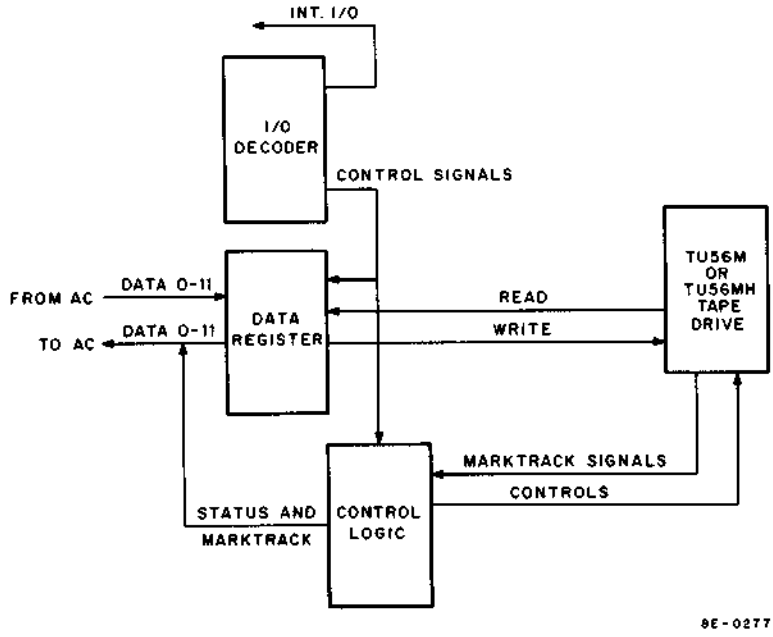


Figure 8-1 TD8-E Block Diagram

*See the *PDP-8/E & PDP-8/M Small Computer Handbook*, page 7-161, for more detailed information on DECtape formatting.

SECTION 2 INSTALLATION

The TD8-E is installed on site by DEC Field Service personnel. The customer should not attempt to unpack, inspect, install, checkout, or service the equipment until a Field Service representative is present.

8.1 INSTALLATION

Perform the following to install the TD8-E System.

Step	Procedure
1	Ensure power is off.
2	Ensure jumpers are installed on the M868 to select the correct I/O code for this TD8-E System (see Table 8-3 for a list of device code jumpers to be installed and unit numbers).
3	Insert the M868 Module into the OMNIBUS (see Volume 1 for module priority).
4	Ensure that the jumpers are installed on the M960 Module (Table 8-2).
5	Connect the 7008447 cable. P3 goes to J1 on the M868 Module and P1 to location A6 or A7 and P2 to location AB10 or AB11 in the TU56M (Table 8-1).
6	Ensure that the G742 Module has been installed in place of the M531 and the G888s are installed in the TU56M Drive Unit.
7	Ensure that the power is wired according to power wiring print TD8-E-3 for the configuration used.

8.2 ACCEPTANCE TEST

Perform the following to check the TD8-E System.

Step	Procedure
1	Run the Formatter Program (DEC-8E-EUZC-D) on each drive. Follow instructions in the formatter document. If testing a TU56M (Dual Drive) swap the formatted tapes from one drive to the other to run the diagnostic test.

NOTE

The Formatter will run only on TD8-Es with device code 677X (only on units 0 and 1).

2	Run the Diagnostic Programs (MAINDEC-08-DHTDA). Refer to the diagnostic document for instructions necessary to run the diagnostic.

8.3 TD8-E INTERFACE

A 7008447 cable is used to interface with the TU56M Tape Transport (Table 8-1). M960 and M961 Connector Modules are used to connect to the TU56M. The M960 Module is used as connector P1 and the M961 Module as connector P2. The M960 Module has unit selection jumpers that must be installed to select the correct unit. Jumpers are installed between split lugs as indicated in Table 8-2 to select the proper unit code for the unit.

Table 8-1

TD8-E Signal Interface

J1 (P3) on TD8-E	Wire Color	Logic on M960 or M961	M960 Module Pin No.	M961 Module Pin No.	Description
NN	Black		M1		Time Mark Enable
MM	Brown		C2		Ground
TT	Red		E1		Reverse
			H1		Forward
SS	Orange		C2		Ground
JJ	Yellow		B1		Stop
			D1		Go
HH	Green		C2		Ground
RR	Blue		J1		Con All Halt
PP	Violet		C2		Ground
LL	Gray	0	V2		Unit 0
		1	E2		Unit 1
		2	H2		Unit 2
		3	K2		Unit 3
		4	M2		Unit 4
		5	P2		Unit 5
		6	S2		Unit 6
		7	T2		Unit 7
KK	White		C2		Ground
N	Black		P1		Select Echo
M	Brown		C2		Ground
T	Red		S1		Write Echo
S	Orange		C2		Ground
AA	Black		C2		Ground
BB	Brown			AA1	Write Time Track Pulses
				AB1	Write Time Track Pulses
EE	Red			AC2	Ground
FF	Orange			AC1	Word 0
				AD1	
H	Yellow			AC2	Ground
J	Green			AK1	Read Time Track
E	Blue			AC2	Ground
F	Violet			AM1	Read Mark Track
W	Gray			AC2	Ground
X	White			AR1	Word 2
				AS1	Word 2
CC	Black			AC2	Ground
DD	Brown			AT1	Word 1
				AV1	Word 1
Y	Red			AC2	Ground
Z	Orange			BA1	Word Enable
K	Yellow			AC2	Ground
L	Green			BB1	Read 1
C	Blue			AC2	Ground
D	Violet			BE1	Read 0
U	Gray			AC2	Ground
V	White			BK1	Read 2

Table 8-2
M960 Module Jumpers

Octal Code	Unit Numbers	Install Select Jumpers
677X	0 and 1	0 and 1
676X	2 and 3	2 and 3
675X	4 and 5	4 and 5
674X	6 and 7	6 and 7

SECTION 3 FUNCTIONAL DESCRIPTION

The TD8-E M868 Quad Module is inserted into the OMNIBUS and used to control either the TU56M or TU56MH Tape Drives. The PDP-8/E System can have as many as four TD8-E Modules on the OMNIBUS to control a maximum of 8 tape units (4 dual drive). For each TD8-E System purchased, the user also receives one H716 Power Supply to supply +5 Vdc and −15 Vdc to the TU56M DECtape. The TU56MH (tabletop model) does not receive the H716 Power Supply.

8.4 INSTRUCTION AND STATUS BITS

The TD8-E uses the following instructions:

Simple DECtape Skip on Single Line Flag (SDSS)
Octal Code: 67X1
Operation: Skip if Single Line flag is set.

Simple DECtape Skip on Time Error (SDST)
Octal Code: 67X2
Operation: Skip if Time Error flag is set.

Simple DECtape Skip on Quad Line Flag (SDSQ)
Octal Code: 67X3
Operation: Skip if Quad Line flag is set.

Simple DECtape Load Command Register (SDLC)
Octal Code: 67X4
Operation: Load Command Register from the AC, clear Time Error, and start UTS Delay if UNIT, DIRECTION or STOP/GO flip-flops are changed.

Simple DECtape Load Data Register (SDLD)
Octal Code: 67X5
Operation: Load Data Register from the AC, do not clear the AC, and clear Single Line and Quad Line flags.

Simple DECtape Read Command Register (SDRC)
Octal Code: 67X6
Operation: Load contents of Command Register, Mark Track Register, and Status bits into the AC. Clear Single Line and Quad Line flags.

Simple DECtape Read Data Register (SDRD)
Octal Code: 67X7
Operation: Load contents of Data Register into the AC, and clear Single Line and Quad Line Flags.

The X in the octal code of the instruction indicates one of four different I/O codes used so that four TD8-E modules can be used on the PDP-8/E OMNIBUS. The I/O codes used are 677X, 676X, 675X, and 674X. The first two TD8-Es ordered will have I/O codes 677X and 676X, respectively. If three or four TD8-Es are ordered, they will have codes 675X and 674X, respectively. The jumpers to be installed to select the correct device code and the unit number to select the correct unit on the TU56M are shown in Table 8-3.

Table 8-3
Device Code Jumpers

Octal Code	Install Select Jumpers	Unit Numbers
677X	W2 and W4	0 or 1
676X	W2 and W3	2 or 3
675X	W1 and W4	4 or 5
674X	W1 and W3	6 or 7

8.5 FUNCTIONAL OPERATION

Figure 8-2 is a functional block diagram of the TD8-E Simple DECtape Control. For discussion purposes the TD8-E is broken into functional groups of logic. Section 4 contains a detailed discussion of each logic group.

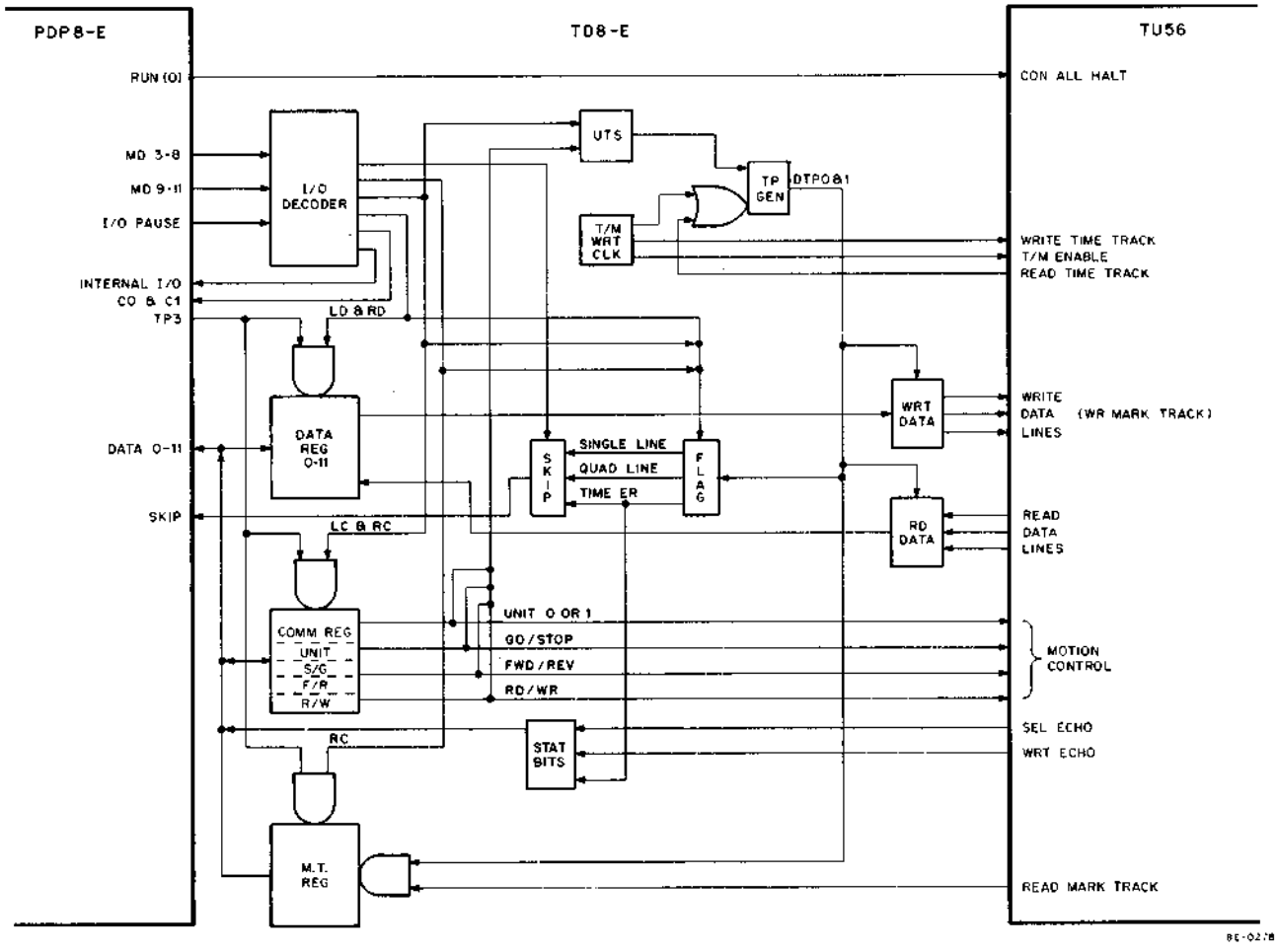


Figure 8-2 TD8-E Functional Block Diagram

8.5.1 I/O Decoder

As stated before, there are four sets of I/O codes that determine which of four possible TD8-Es is being addressed. The decoding is done by two jumpers connected to MD7 and MD8. When the correct code for the TD8-E goes to the I/O decoder and an I/O PAUSE is present an INTERNAL I/O is generated to allow decoding of bits MD 9–11 and generate an INTERNAL I/O L. The INTERNAL I/O L will prevent the positive I/O bus interface from generating IOTs while this operation is under way and will generate an enable signal (CC67X) to allow bits MD 9–11 to be decoded. MD 9–11 are decoded and control the transfer of data and commands to the Data Register, Command Register, and Mark Track Register. TP3 is used as a timing signal throughout the control logic. C0 and C1 determine the direction of data flow to and from the AC, and determine if the AC is cleared or not.

8.5.2 Command Register

The Command Register is made up of four flip-flops which are loaded from the DATA BUS by the SDLC instruction. 1s set the flip-flop and 0s clear it.

UNIT — Selects which drive on the TU56M is to be used. If UNIT is cleared, Unit 0 is selected.

F/R — Determines which direction the tape is to move. If F/R is cleared, direction is Forward (CW).

CAUTION

Because of circuit delays in the TU56M, the SDLC instruction to simultaneously change the F/R flip-flop and the S/G flip-flop should not be executed. If this instruction is executed, the brake signal in the TU56M will be applied to the wrong motor, causing the tape drive to drift much further down the tape (in the direction it was going) than it normally would if the brake were applied to stop tape movement.

S/G — Tells the selected unit to move tape or stop. If S/G is cleared, the selected tape will stop. The GO signal is delayed 200 ns after an SDLC instruction to ensure that the unit select line has had time to switch in the Tape Drive Unit before the tape starts to move.

R/W — Instructs the selected unit to read or write data. If R/W is cleared, a read operation will take place; if it is set, a write operation is executed.

The SDLC instruction also starts the UP TO SPEED (UTS) delay time and clears the TIME ERROR flip-flop. Figure 8-3 shows the format of data loaded into the Command Register when the SDLC instruction is executed.

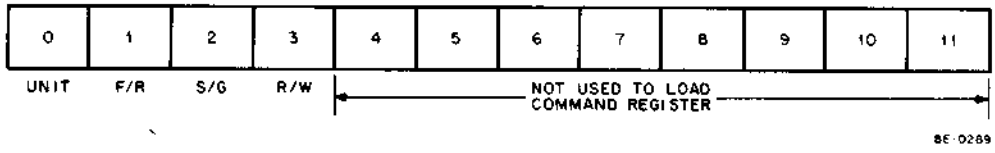


Figure 8-3 Format of Data Loaded into the Command Register

Any time an instruction is executed to change the Command Register, except when the R/W flip-flop is changed, it starts a new delay timeout of 120 ms; at the end of this time, the UTS will set again. UTS will not set when the S/G flip-flop is cleared.

The R/W flip-flop is cleared (set to a read condition) by any of the following:

a. SEL ERR
b. TIME ERROR
c. WRITE LOCKOUT
d. POWER NOT OK
e. INITIALIZE (Clears all logic)

8.5.3 Data Register

The Data Register contains the gating and register necessary to take data from the OMNIBUS and put data in the OMNIBUS. It also receives data from the tape during a read operation and places data on the tape during a write operation.

8.5.4 Mark Track Register

After UTS is set, the Mark Track (MT) Register constantly reads data from the mark track. The mark track data is read bit by bit, and tested by a Single Line Flag (SLF). Each time SLF is set, a new bit has been shifted into the MT Register. All decoding of mark track data must be done by the program.

The MT Register is cleared by the start of a UTS delay to ensure that no erroneous codes are left in from a previous operation. The program must be delayed at least six Single Line flags after UTS has timed out to ensure at least one complete mark track code has been shifted into the Mark Track Register. This delay ensures a valid code has been shifted into the register.

The contents of the MT Register are transferred to the AC using an SDRC instruction which also transfers the STATUS bits and the contents of Command Register at the same time. Figure 8-4 shows the format of the word used for this transfer.

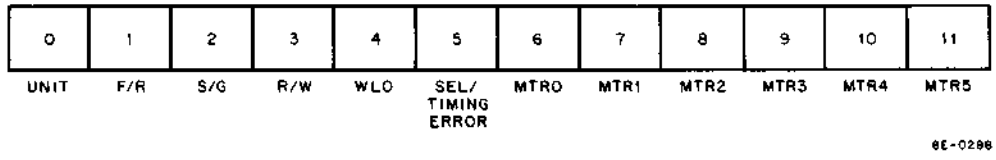


Figure 8-4 Format of Word Transferred to AC

8.5.5 Flags and Status Bits

The Single Line flag is set each time the DECtape reads one line of tape and is used to detect codes on the Mark Track as discussed in Paragraph 8.5.4. The Single Line flag is cleared by a not-up-to-speed condition and when an SDLD, SDRC, or SDRD instruction is executed.

A Quad Line flag is set once for each four lines of data read from the tape. Testing the Quad Line flag allows the program to read or write a full 12-bit word. The Quad Line flag is cleared by NOT UTS or by SDLD, SDRC, or SDRD instructions.

TIME ERROR is an indication that the program did not go back to the control in time to work on the Data Register before the next transfer of the DECtape took place or that the program was executing an SDLD, SDRD, or SDRC instruction when the DECtape requested another transfer. If the control has been writing data, TIME ERROR clears the R/W flip-flop to ensure that erroneous data is not written on the tape. TIME ERROR is ORed with SEL ERR and put onto the OMNIBUS during an SDRC instruction (Figure 8-4).

SEL ERR is sent to the TD8-E by the TU56M to indicate that no unit has been selected or more than one unit has been selected. SEL ERR has no effect on the TD8-E logic, but is transferred from the Command Register to allow the program to make decisions on what to do about the error.

WRITE LOCKOUT is sent to the TD8-E by the TU56M to indicate that the unit selected for writing was not write enabled. WRITE LOCKOUT clears the R/W flip-flop and has a status bit for transfer to the AC during an SDRC instruction (Figure 8-4).

8.5.6 Time Pulse Generator

The Time Pulse Generator and its logic reads a signal from the time track and produces full- and half-cycle pulses on the rising and falling edges of the time track signal. These pulses are required to read data from and write on the tape.

The time pulses are gated with and synchronized by the UTS flip-flop so that pulses will be produced when the tape is up to speed. There is a discriminating delay in the Time Pulse Generator to ensure that noise crosstalk picked up by the time track head during write operation is not converted into extra time pulses.

The Time Generator has a clock to produce the time pulses required to write the time and mark tracks. The time track is written directly from a complementing flip-flop in the Time Generator, and the mark track is written from DATA bit 0. The read time track line is gated off while writing the time and mark tracks to ensure that noise coming off the time track does not generate unwanted pulses.

8.6 TD8-E TIMING

The TD8-E timing discussed in this section does not indicate the correct way or the only way to program the TD8-E. The information presented here is meant only to show the interaction between groups of logic when various instructions are executed.

8.6.1 Timing for Writing Time and Mark Tracks

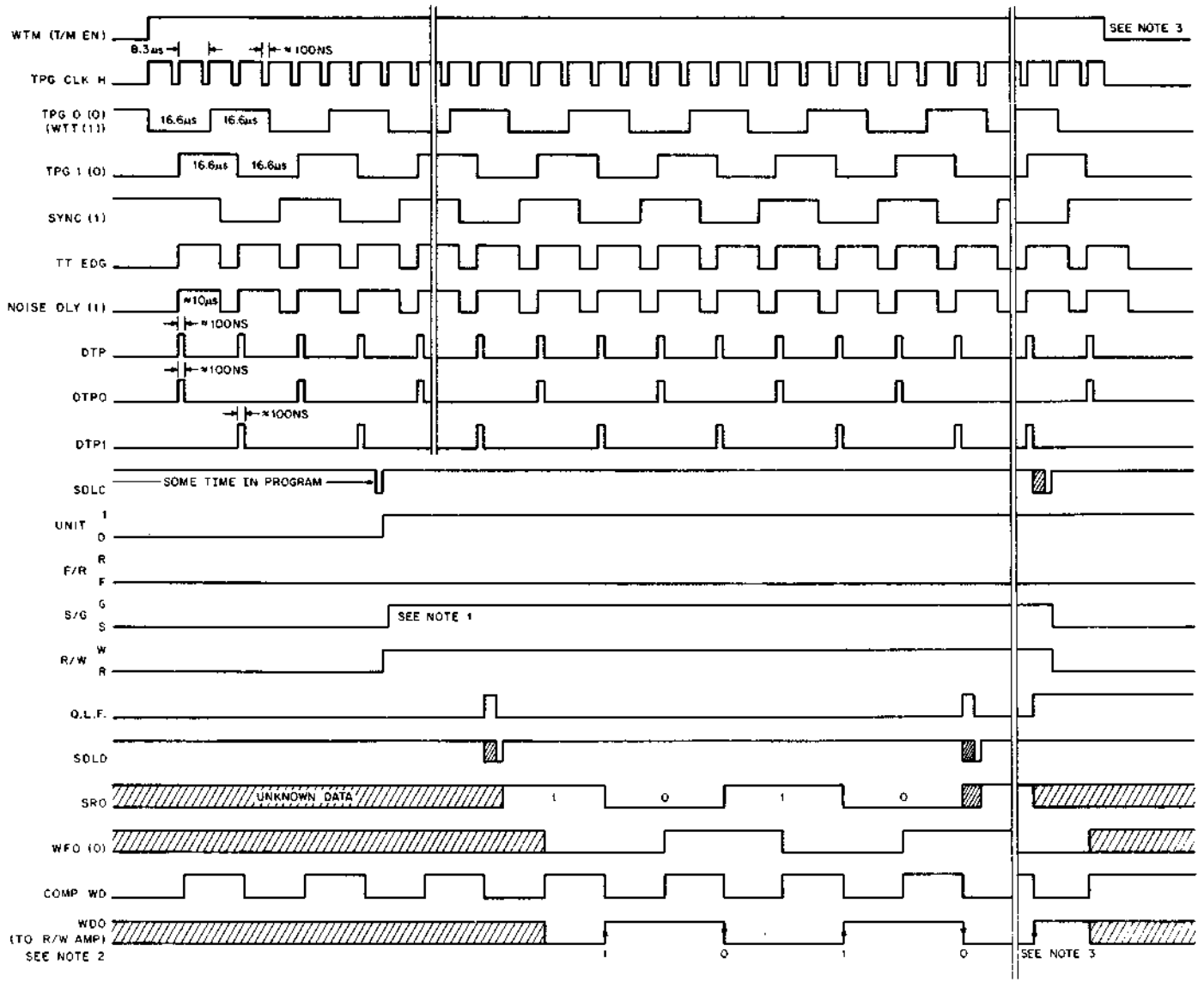
The time and mark tracks are written to format the DECtape for writing and reading data. Data to be written on the mark track is transferred from the AC to the DATA BUS in bit positions 00, 03, 06, and 09 (see the *PDP-8/E & PDP-8/M Small Computer Handbook* for the format of data on the tape). Figure 8-5 is a timing diagram for writing the mark and time tracks (formatting). Note that the T/M Enable switch, S1, must be set to WTM to enable writing the time and mark tracks (Table 8-4 for signal functions). DEC-8E-EUZC-D gives instructions for formatting DECtapes and the DEC-8E-EUZC-PD Tape Formatter should be used to format all tapes.

8.6.2 Write Data Timing

The timing diagram in Figure 8-6 shows the timing necessary to write data on the DECtape using the TD8-E. The data to be written is transferred to the TD8-E from the AC and written on the tape in four 3-bit bytes in the tape block determined by the programmed instructions. Note that the RTT time pulses must be written on tape using the Formatter prior to writing data.

8.6.3 Read Data Timing

Figure 8-7 shows the timing required to read data and the mark track from the TU56M DECtape (see Table 8-4 for signal functions).



NOTES

1. The GO signal is switched on by computer FP4 to allow setting of the Unit Select gates.
2. During formatting the Mark Track is written from the Bit 0 Logic.
3. At this time the last of the End Zone Gates has been written. The program stops the tape and the WTM switch is set to OFF.

Figure 8-5 Timing for Writing Mark and Time Tracks

Table 8-4
TD8-E Signals and Signal Functions

Signal	Function
CON ALL HALT	Signal sent to the TU56M to stop the tape drive if the computer program stops. The loss of the RUN signal from the processor will cause the TU56 to stop. CON ALL HLT stops an unselected drive that might be moving tape, clears the S/G command flip-flop to stop the selected drive, and clears the R/W command flip-flop to keep from writing while the drive comes to a stop.
F/R	F/R (Forward/Reverse) will control the direction of tape rotation. If F/R and S/G in the Command Register are set, the tape moves in reverse (CCW); if F/R is cleared and S/G is set, the tape will move forward (CW).
INITIALIZE	Signal generated by Clear key, Power Up, and CAF instruction used to clear all flags and control registers.
RD0 RD1 RD2	Four bits of serial data are taken from the three parallel tracks and assembled in the Data Register as a 12-bit word. The word is then transferred as 12 parallel bits to the DATA BUS as indicated below: RD0 Data, 00, 03, 06, 09 RD1 Data, 01, 04, 07, 10 RD2 Data, 02, 05, 08, 11
RMT	Read Mark Track is 6-bits of serial data from the mark track of the tape. The mark track codes and their functions are as follows (Figure 8-8): **Code** — **Name** — **Function** 55 REVERSE END ZONE MARK — This code identifies the code for end zone located at the beginning of the tape. When moving in the reverse direction, this code will be read as 22 meaning the end of tape is near and the program should HALT or change the direction of tape movement. 25 INTER BLOCK SYNC — Code 25 is another NO-OP code which lies between blocks and for several feet in the inside of the end zone. This code allows for turnaround time when reading the first and last block; it is used by the program to synchronize its timing logic between blocks. 26 FORWARD BLOCK MARK — The number assigned the block by the Formatter is stored on this cell. When the computer is searching for a block, it transfers this number into the AC and examines it. When code 26 is decoded by the program, it knows that the block number is in the Data Register and ready to be read into the AC and compared with the block wanted.

Table 8-4 (Cont)
TD8-E Signals and Signal Functions

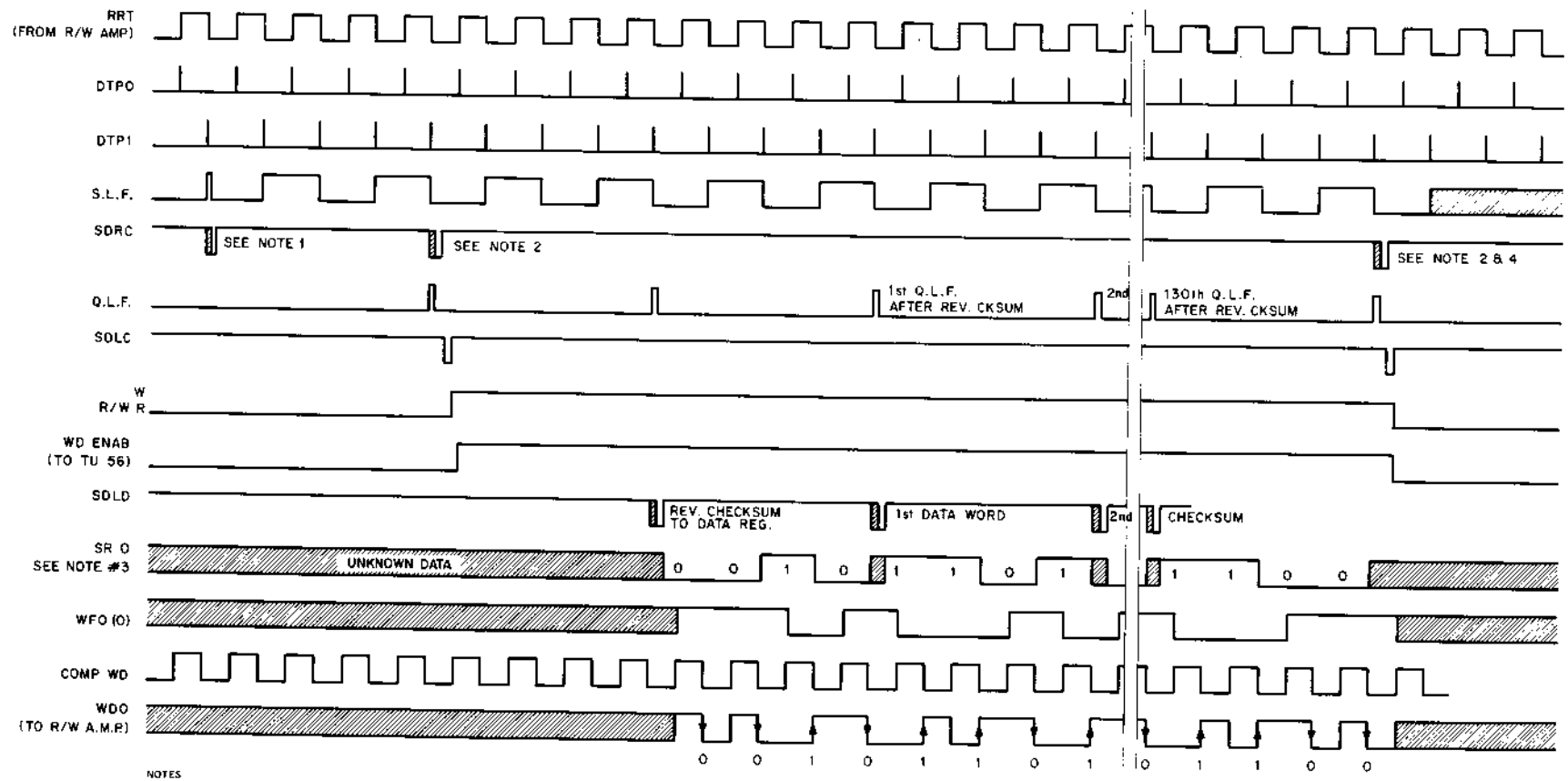
Signal	Function		
RMT (Cont)			
	Code	**Name**	**Function**
	32 10	REVERSE GUARD MARK LOCK MARK	These two cells are NO-OP conditions which give the program time to decide what to do with the block it has identified.
	10	REVERSE PCC MARK	This is the last cell before a data cell. It is used to initiate the parity checksum routine. If the computer is writing, the first 12-bit word to be written is transferred to the controller during this cell and every four lines thereafter.
	10 10	REVERSE FINAL MARK REVERSE PREFINAL MARK	These two codes indicate the first and second data words, respectively; otherwise, they have no special significance.
	70	DATA MARK	This code simply indicates that a data word is written on the data tracks. The program continuously checks to see that the mark track is coded.
	73 73	PREFINAL MARK FINAL MARK	These codes indicate that the last two words of data are being transferred.
	73	PCC MARK	The parity checksum which was being calculated by the program during the transfer is either written here during a write operation or compared by the program during a read operation.
	73 51	REVERSE LOCK MARK GUARD MARK	These are NO-OP spaces which become useful when the tape is traveling in the reverse direction.
	45	REVERSE BLOCK NUMBER	The block number is stored here to be picked up by the program when the tape is traveling in the reverse direction.
	25	INTER BLOCK SYNC	Has the same function as INTER BLOCK SYNC at the beginning of the tape.
	22	END ZONE MARK	When this code comes up, the program knows that it has just run out of tape (refer to REVERSE END ZONE) and that it had better do something about it. Note that this code is the complement of 55, the REVERSE END ZONE MARK.

Table 8-4 (Cont)
TD8-E Signals and Signal Functions

Signal	Function
RTT	Read Time Track is a 16.6-μs square wave signal coming from the time track. Pulses produced on the rising and falling edges of the time track signal are used to sync the TD8-E to read and write data.
SEL ERR	Select Error indicates no unit has been selected or that both units have been selected simultaneously. The software must decide what to do about the error.
SEL ECHO	Select Echo is sent to the TD8-E by the TU56M in response to command signals to indicate TU56M is on line.
S/G	Stop/Go is sent to the TU56 by the TD8-E to command the tape drive to move in the direction determined by F/R. This signal is generated by the S/G flip-flop in the Command Register.
TIME ERROR	Time Error is an indication that the program did not come back to the control in time to work on the Data Register before the next transfer occurred.
T/M ENABLE	Time Mark Enable allows tape to be formatted by writing on the time and mark tracks when S1 on the M868 Module is set to WTM.
WD0 WD1 WD2	Twelve bits of parallel data transferred from the DATA BUS to the Data Register and disassembled by the Data Register to form four 3-bit bytes of serial data. The four bytes of serial data are written by these three signals on parallel tracks on the DECtape as indicated below. WD0 Data, 00, 03, 06, 09 WD1 Data, 01, 04, 07, 10 WD2 Data, 02, 05, 08, 11
WTT	Write Time Track is a 16.6-μs square wave signal written on the time track when the tape is formatted.
WRITE LOCKOUT	Write Lockout is sent to the TD8-E by the TU56M to indicate that the unit to be written on is not write enabled. This signal will clear R/W in the Command Register and select the Read mode.
WD ENABLE	Word Enable is generated when R/W on the Command Register is set and UTS is set to allow writing data on tape.
UTS	Up To Speed is negated by any change in the Command Register except R/W. After a delay of 120 ms to allow tape to come up to speed, UTS is again asserted to allow reading or writing data. UTS is used to enable RTT or WTT time pulses.
TPG0 TPG1	Time pulses from the Time Pulses Generator which are produced by the rising and falling edges of the RTT signal (WTT signal while formatting).
QLF	The Quad Line flag is set each time four lines of data are transferred to or from the tape, so that by testing this line the program will know when a full 12-bit word has been read or written. QLF is cleared by NOT UTS, instructions SDLD, SDRC, SDRD or INITIALIZE.

Table 8-4 (Cont)
TD8-E Signals and Signal Functions

Signal	Function
SLF	The Single Line flag is set each time the DECtape transfers one line of data and is used to detect mark track codes. SLF is cleared by NOT UTS, instructions SDLD, SDRC, SDRD or INITIALIZE. SLF is ignored while reading or writing data.
NOISE DLY	Noise Delay is a 10-μs delay generated by the Time Pulse Generator to prevent the noise picked up by the time track head during a write operation from generating extra time pulses.
SYNC	The SYNC is used to generate and separate the TP0 and TP1 pulses required to read or write.



NOTES

1. At this point the COMMAND REGISTER is set for the correct UNIT, FWD, REV, GO, and READ. The correct block number has been found and at this SLF the REVERSE GUARD is in the MT register.
2. This SDRC loads the status of the COM REG into the AC so that the write bit can be set, in, or removed without changing any other COM REG condition. This also clears the QLF which the SDLC does not.
3. The other two parallel write bits work identically to SRD, WFO, and WDO.
4. At this point if any COM REG function other than R/W is changed, UTS disappears and the TIME pulses stop until UTS DELAY times out and UTS is set.

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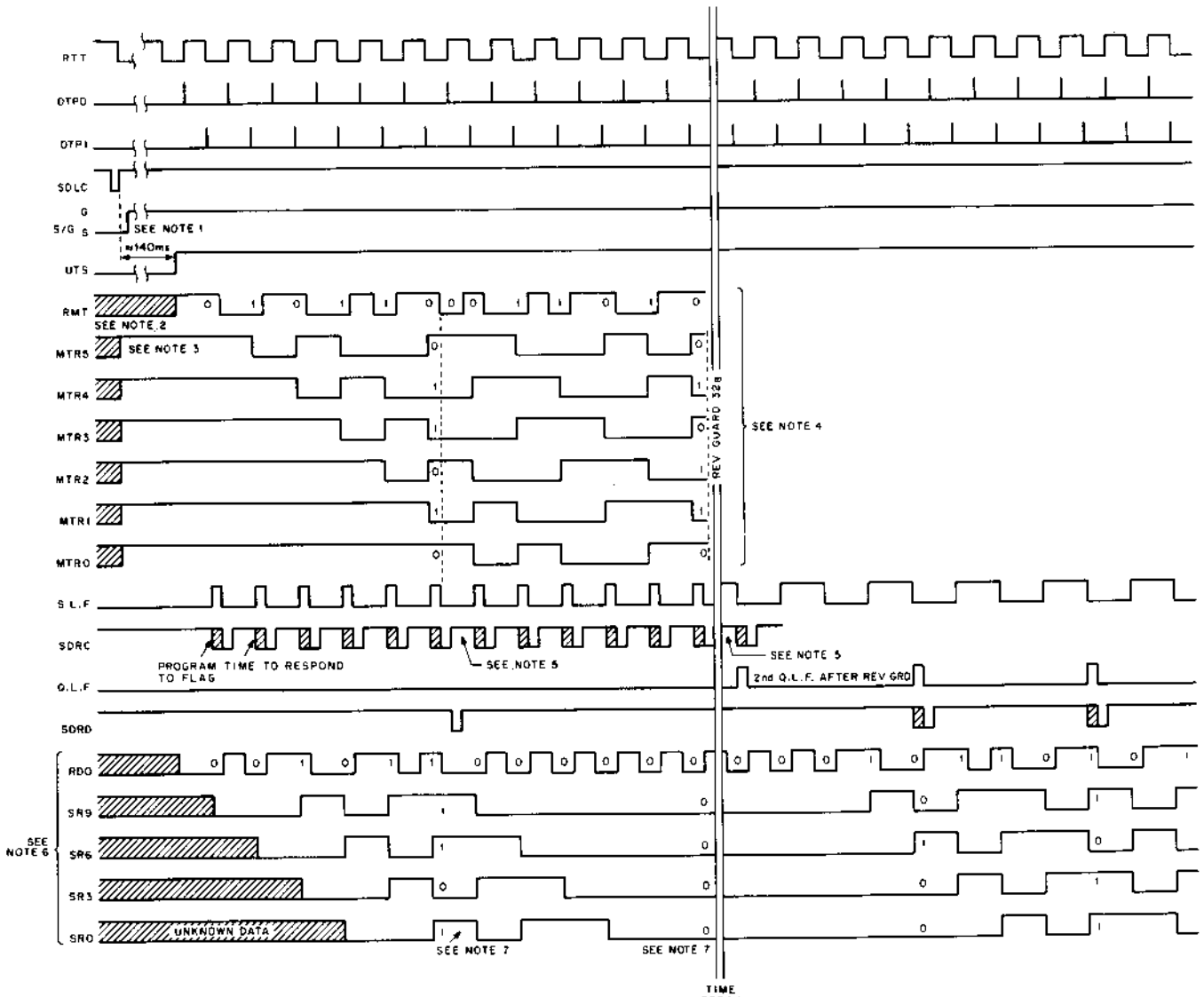
Figure 8-6 Write Data Timing



NOTES

1. The GO signal is switched on by computer TPI to allow settling time for the UNIT select lines. The UNIT DIRECTION and READ commands are set by the SDLC.
2. The inputs to and outputs from the Mark Track Regs are undefined. A 1 is a low level.
3. Any time the UTS mode is started, the MTR is set to all 0's (high output).
4. Once the system unlock and all REVERSE GUARD limits have been found, the Single Lane Flags are sensed. The MTR is not looked at again until another start is received.
5. At this point the complete Mark Track code is in the RC. It is a Block Mark so SDRD is raised to read the Block Number so that the proper location for the correct Block Number.
6. The other two parallel Read lines work identically to RD0, SR9, SR6, SR3, and SR0.
7. The last two bits of the Block Mark are not become the Block Number so in the last four bits of the Block Mark. The Reverse Guard bit detects the forward direction.

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Figure 8-7 Read Data and Mark Track Timing

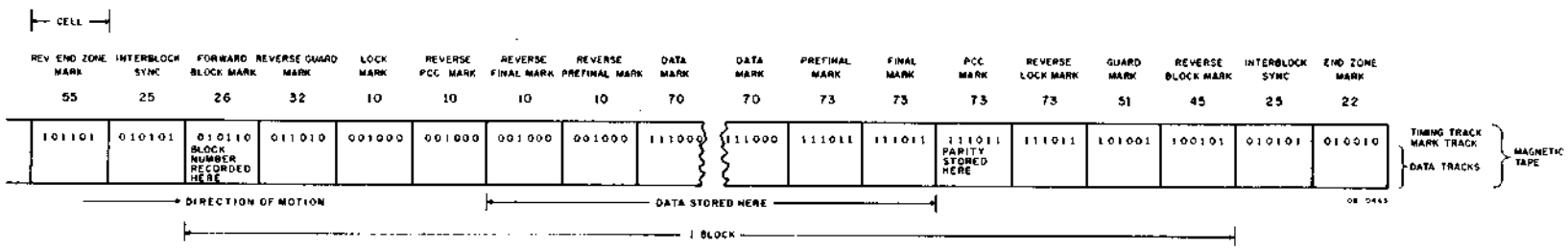

Figure 8-8 DECtape Data Format

The logic in the TD8-E will be broken into functional groups for discussion purposes. The block diagram, Figure 8-2, should be used to understand the interaction of the logic, the signal flow within the module, and the input or output signals.

8.7 INPUT/OUTPUT DECODER LOGIC

The I/O decoder decodes instructions from the Memory Data Bus and generates signals to control the operation of the TD8-E (Figure 8-9). Bits MD 3–11 are gated by the I/O PAUSE when an I/O instruction is generated. Bits MD 3 to MD 8 generate a signal CC67XH applying bits MD 9, MD 10, and MD 11 to the 8251 IC. The 8251 IC is a BCD-to-Decimal decoder (see Volume 1, Appendix A, for truth table logic and pin locations) which decodes MD 9–11 and produces a low on one output line. The low out of the 8251 IC indicates which instruction is to be executed. As an example MD 9 Low, MD 10 and MD11 High (100) produces a low on pin 4 which indicates an SDLC instruction was programmed. The jumpers for MD 7 and MD 8 will select the device code (see Table 8-3 for device codes) for multiple TD8-E Systems.

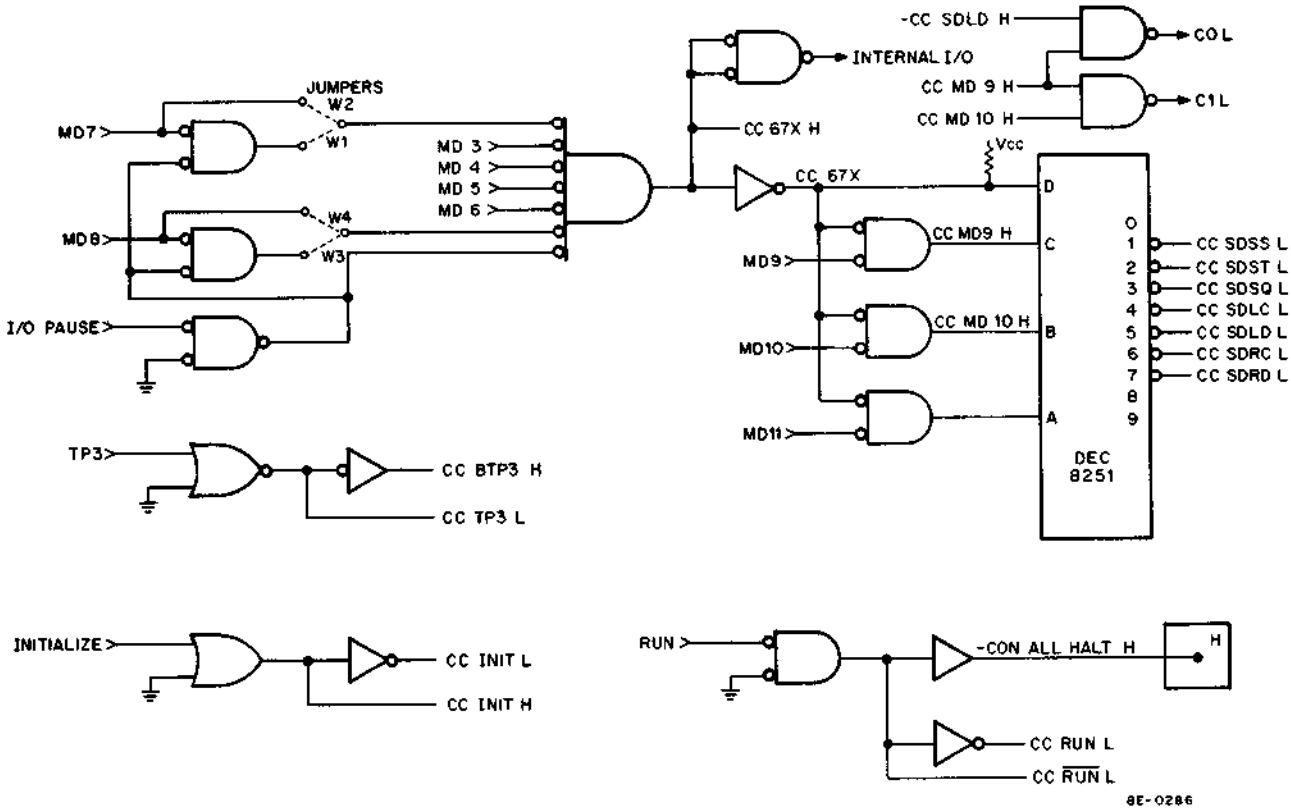

Figure 8-9 I/O Decoder Detailed Logic

8.7.1 Control Logic

8.7.1.1 C Line Select Logic – The C line logic (Figure 8-9) controls the direction of data flow between the DATA BUS and the AC and determines if the AC is clear or not. Table 8-5 shows the status of C0 and C1 to transfer data between the AC and the DATA BUS using the SDLC, SDLD, SDRC, and SDRD instructions.

Table 8-5
C-Line Select Levels and Transfer Operations

Instruction	C0	C1	Transfer Operation
SDLC	Low	High	AC → Data Bus then 0 → AC
SDLD	High	High	AC → Data Bus
SDRC	Low	Low	Data Bus → AC
SDRD	Low	Low	Data Bus → AC

8.7.1.2 Time Pulse 3 Logic – TP3 shown in Figure 8-9 is used throughout the module to enable gates for execution of instructions.

8.7.1.3 Initialize Logic – INITIALIZE clears all logic when the computer power is first turned on, when the CLEAR key on the console is operated, or when the CAF instruction is executed.

8.7.1.4 Run Signal and CON ALL HLT Logic – The loss of the RUN signal from the computer will generate CON ALL HLT, stopping the tape drive unit regardless of the status of the Command Register. RUN is negated any time the program stops.

8.8 COMMAND REGISTER

The Command Register (Figure 8-10) consists of the UNIT, Forward/Reverse (F/R), Stop/Go (S/G) and Read/Write (R/W) flip-flops. The flip-flops in the Command Register are set or cleared by AC 0–3 when the Command Register is loaded by the SDLC instruction (Paragraph 8.5.2).

8.8.1 Unit Select Logic

The UNIT SEL flip-flop determines which TU56M unit is selected. The UNIT flip-flop sets when bit 0 from the AC is a 1, and it is clocked into the flip-flop by TP3 during the execution of an SDLC instruction. If UNIT flip-flop is cleared, Unit 0 is selected. SDLC and TP3 clear the UNIT flip-flop if the data input is low (AC bit 0 is 0).

8.8.2 Forward/Reverse (F/R) Logic

The F/R flip-flop (Figure 8-10) determines the direction of tape movement. When an SDLC instruction is performed and bit 1 from the AC is a 1, the F/R flip-flop sets and directs the tape drive to move backward. If the data input is 0 (bit 1 from the AC is 0) F/R clears when the SDLC instruction and TP3 are applied to the clock (C) input, and the drive is directed to move forward.

8.8.3 Stop/Go Logic

The stop/go logic (S/G) flip-flop (Figure 8-9) enables the tape to move in a direction determined by the F/R flip-flop. If AC bit 2 is a 1 when the SDLC instruction is performed, the S/G flip-flop sets. The output of the flip-flop is applied to a latch which also has TP4 as an input. TP4 clocks the latch 300 ns after S/G is set and pulls latch output low. The 300-ns delay allows the unit select lines to settle before the S/G signal is applied to the TU56M. S/G is ANDed with POWER OK to remove the GO signal from the TU56M during a power down. Power in the TU56M does not drop as quickly as power on the PDP-8/E and the tape may continue to run and write erroneous data.

Loss of the RUN signal from the processor generates CON ALL HLT to the TU56M and clears the S/G flip-flop.

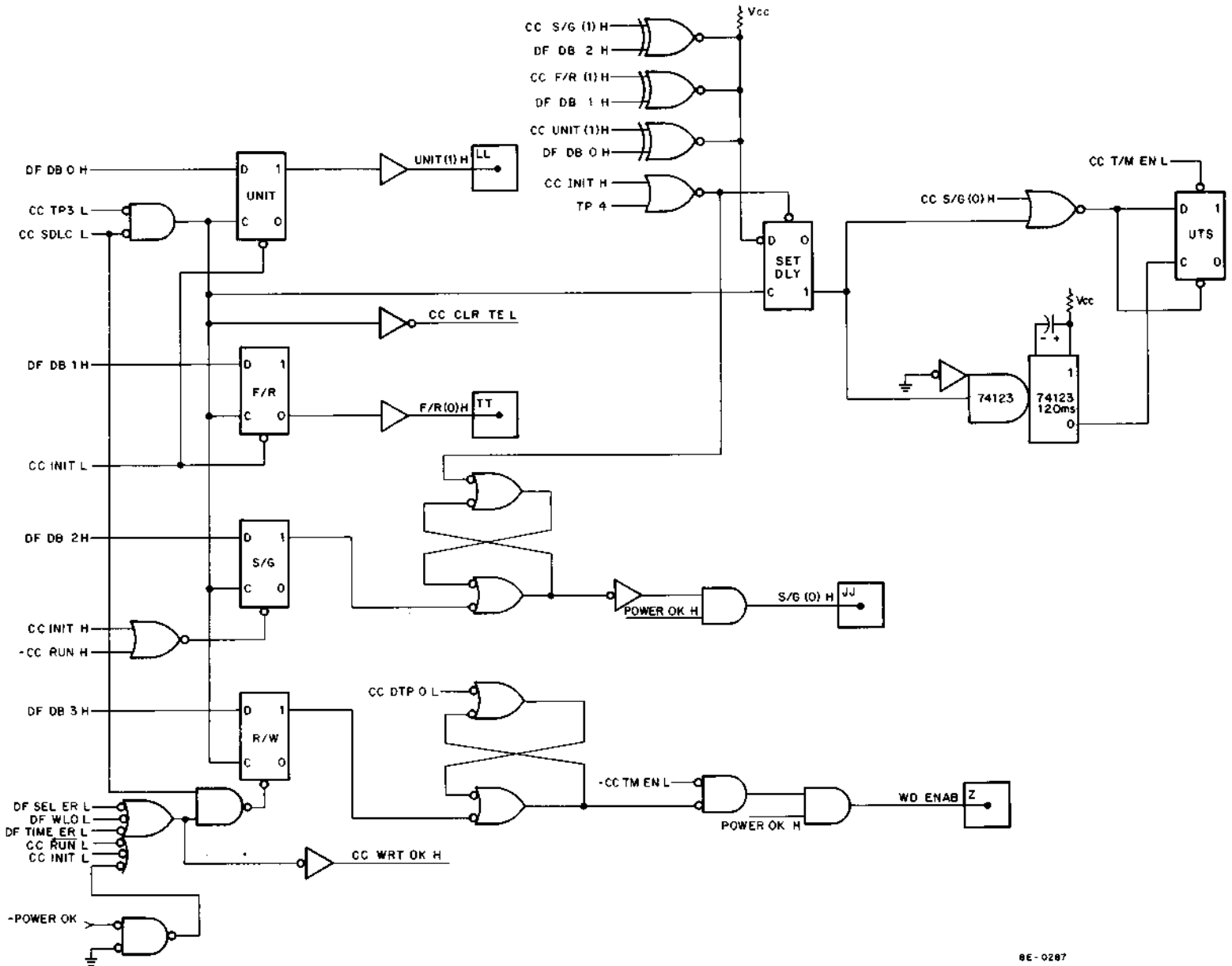

Figure 8-10 Command Register and UTS Logic

8.8.4 Read/Write Logic

The Read/Write flip-flop (R/W) (Figure 8-10) selects the read or write mode in the TU56M. If bit 3 from the AC is a 0 when the SDLC instruction is executed, R/W will clear and the TU56M will not write on the tape. If bit 3 is 1 when the SDLC instruction is executed, R/W sets, and its output is applied to the reset input of a latch. D TP0 is applied to the set input of the latch. When D TP0 is received from the Time Pulse Generator, the outputs of the latch will be low if R/W is set. The latch output is ANDed with NOT CC T/M EN, which enables the gate when S1 is set to OFF (Figure 8-11). The output of the first gate is ANDed with POWER OK H to generate WD ENAB, causing the TU56M to write on the DECtape. WD ENAB is ANDed with POWER OK to remove WD ENAB from the TU56M during a power down of the system. R/W is also cleared by any of the following conditions to select read mode and remove WD ENAB from the TU56M.

a. SEL ERR
b. TIME ERROR
c. WRITE LOCKOUT
d. POWER NOT OK
e. INITIALIZE
f. NOT RUN

The DECtape can read or write in both directions, but the program must take care of the obverse complement data.

8.9 UTS DELAY LOGIC

The UTS delay logic starts a 120-ms delay after S/G is set, to ensure the tape is up to speed before data is read from or written on the DECtape (Figure 8-10). Any change in the Command Register, except R/W, clears the UTS flip-flop and starts a new 120-ms timeout. The D input of SET DLY is enabled by the Exclusive-OR gates which cause SET DLY to set if the UNIT, S/G, or F/R flip-flops are changed, thus clearing UTS and starting another 120-ms delay. The following conditions set the SET DLY flip-flop clearing UTS:

a. S/G ≠ DF DB 2 (AC Bit 2)
b. F/R ≠ DF DB 1 (AC Bit 1)
c. UNIT ≠ DF DB 0 (AC Bit 0)

If SET DLY is set, the 74123 IC is triggered and starts a new 120-ms timeout. After 120 ms, if no new changes are made in the Command Register, the clock input of the UTS flip-flop goes high. This transition causes UTS to set if S/G is set supplying a true (high) to the D-input. UTS will not set if the S/G flip-flop is cleared. Any time UTS is cleared the TT ENABLE flip-flop (Figure 8-11) will clear and disable the Time Pulse Generator logic. The SET DLY flip-flop is cleared by TP4 of each CC SDLC instruction that changes the Command Register. This is to ensure that the 120 ms (74123) can trigger on each CC SDLC and the only timeout is 120 ms after the last SDLC.

When SET DLY clears it also clears the Mark Track Register (Figure 8-14, Paragraph 8.11).

8.10 TIME PULSE GENERATOR

The Time Pulse Generator (Figure 8-11) has two functions, one is to produce pulses to write the time and mark tracks (formatting) and the other is to produce timing pulses from the time track signal (RTT) to allow reading and writing of data. The WTT signal, a 33.2-μs square wave, is written on the time track of the DECtape when the tape is formatted. The Time Pulse Generator reads the RTT signal from the timing track of the tape when data is read from the tape or written on the tape. Full- and half-cycle pulses (Figure 8-5, signals DTP, DTP0, and DTP1) are produced on the rising and falling edges of the time track signal. The time pulses are synchronized with the UTS flip-flops so pulses will be produced only when the tape is up to speed.

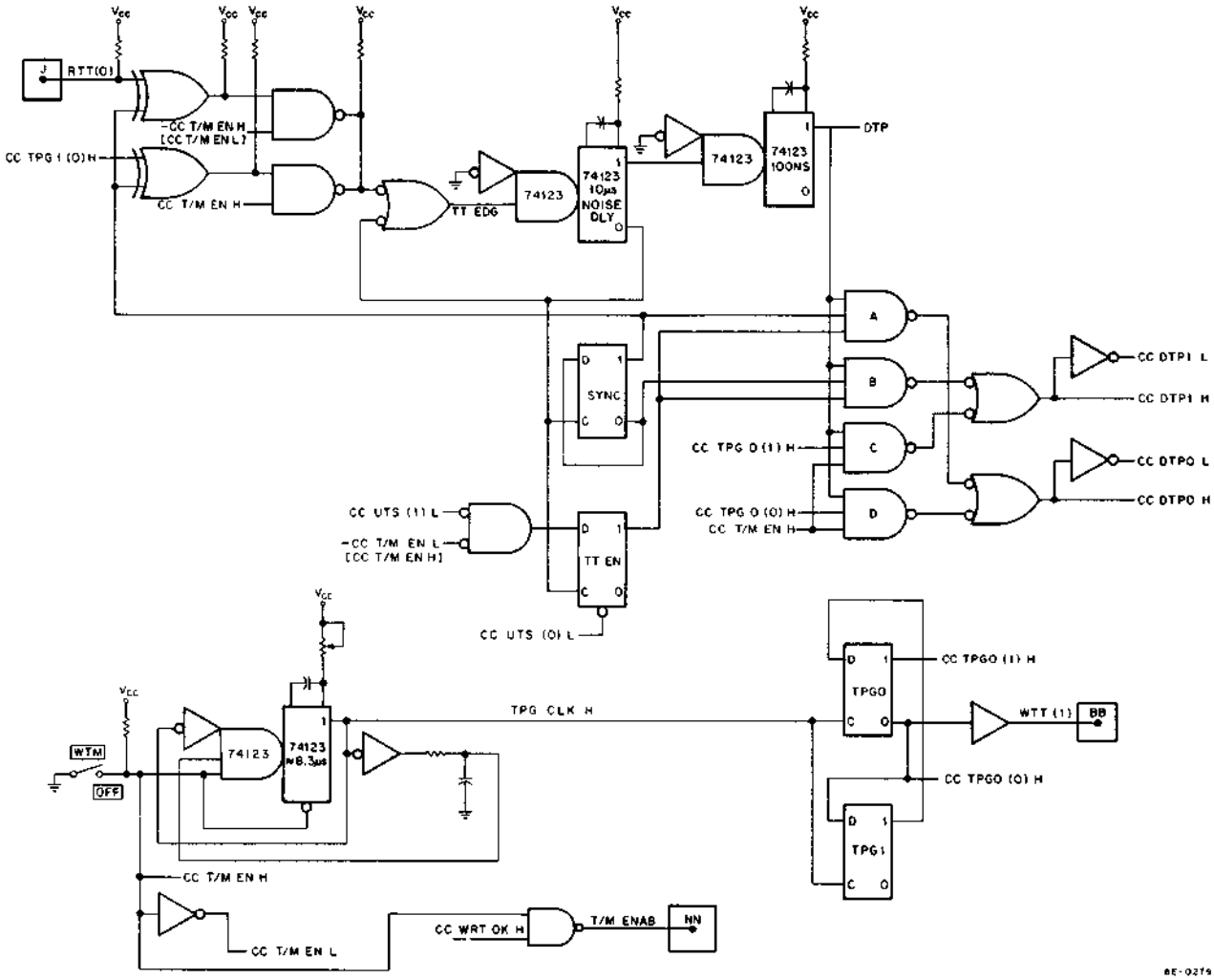

Figure 8-11 Time Pulse Generator Logic

8.10.1 Write Time Track Pulses

The Write Time Track (WTT) pulses are produced by a 74123 IC (Figures 8-5 and 8-11) and two flip-flops (TPG 0 and TPG 1) arranged in a conventional switch-tail ring counter. The 74123 IC outputs a pulse every 8.3 μs when S1 is set to WTM. S1 removes the low level from the clear input in the 74123 IC and enables the input gate, which allows the 74123 IC to be triggered. The T/M ENAB signal is also sent to the TU56M to allow writing on the time and mark tracks. CC T/M EN is ANDed with WRT OK to remove T/M ENAB from the TU56M during a power down of the PDP-8/E, and any other condition that clears the R/W flip-flop.

The 74123 used to generate TPG CLK H is a retriggerable monostable multivibrator (one shot) that is set for 8.3 μs. External circuitry causes this one shot to retrigger itself on its own trailing edge. An inverter and integrator on the output of the 74123 IC delays the triggering process for 100 ns, establishing a minimum width for TPG CLK H. TPG 0 and TPG 1 produce overlapping 33.2-μs square wave pulses (Figure 8-5). The leading edge of TPG 0 occurs 8.3 μs before the leading edge of TPG 1. The 0 output of TPG 0 is applied to the time track (WTT) signal. The outputs of TPG 0 and TPG 1 are also used to produce DTP0 and DTP1 when writing the time and mark tracks. Gates C and D (Figure 8-11) must be enabled to apply these signals to the control logic to allow writing on the time and mark track. CC T/M EN H is applied to C and D when S1 is set to WTM during a write operation and CC TPG 0 (1) H or CC TPG 0 (0) H are applied to the gates during a write. The source of the DTP signal is explained below.

CC TPG is combined in an Exclusive-OR gate with the output of SYNC. The output of the Exclusive-OR gate goes high when SYNC (1) H and CC TPG 1 (0) H are equal. The 74123 IC is triggered only on the rising edge of its input signal, and the SYNC flip-flop is complemented each time the 10-μs 74123 times out. Thus, the SYNC flip-flop changes state about 7 μs before CC TPG 1 changes state, this allows TT EDG to go low for about 7 μs. When CC TPG 1 switches to the same level as SYNC, then TT EDG again goes high retriggering the 10-μs 74123 (NOISE DLY). Once the NOISE DLY is triggered its output holds TT EDG high (through an OR gate) thus preventing any cross-talk noise coming from RTT (0) from retriggering the delay.

Note (Figure 8-5) the rising edge of NOISE DLY occurs in the center of CC TPG 0 (WTT). This produces a 90 degree phase shift between the writing of the time track and mark track. The phase shift is required so that when the time track (RTT) is read back during a normal data transfer, the time pulses used to strobe in the mark track occur in the center of the mark track signal.

The rising edge of the 10-μs 74123 IC (NOISE DLY) triggers the 100-ns 74123 and produces a 100-ns pulse (DTP). DTP is produced on every edge of CC TPG 1 and is applied to AND gates C and D. When CC TPG 0 (0) is high, D is enabled and CC DTP 0 H is produced; when CC TPG 0 (1) is high, C is enabled and CC DTP 1 L is produced. This separates the DTP pulses into two pulse trains, one has pulses on the rising edge of CC TPG 1 and the other has pulses on the falling edge of DTP 1.

Most signals in the Time Pulse Generator (Figure 8-11) are gated against CC TM EN. This is done to ensure the logic required for writing the time and mark tracks is enabled only for that operation and the logic to read and write data is gated off. The reverse is true when reading the time track and transferring data.

8.10.2 Read Time Track Pulses

The RTT signal read from the time track is used to produce time pulses (Figures 8-11 and 8-12) which allow data to be transferred to or from the DECtape. To supply time pulses (CC DTP0 and CC DTP1) AND gates A and B must be enabled by DTP, SYNC, and TT EN. TT EN is set by the first falling edge of NOISE DLY after UTS is set. This ensures that time pulses are not produced while the tape is getting up to speed. TT EN is cleared by the loss of the UTS signal.

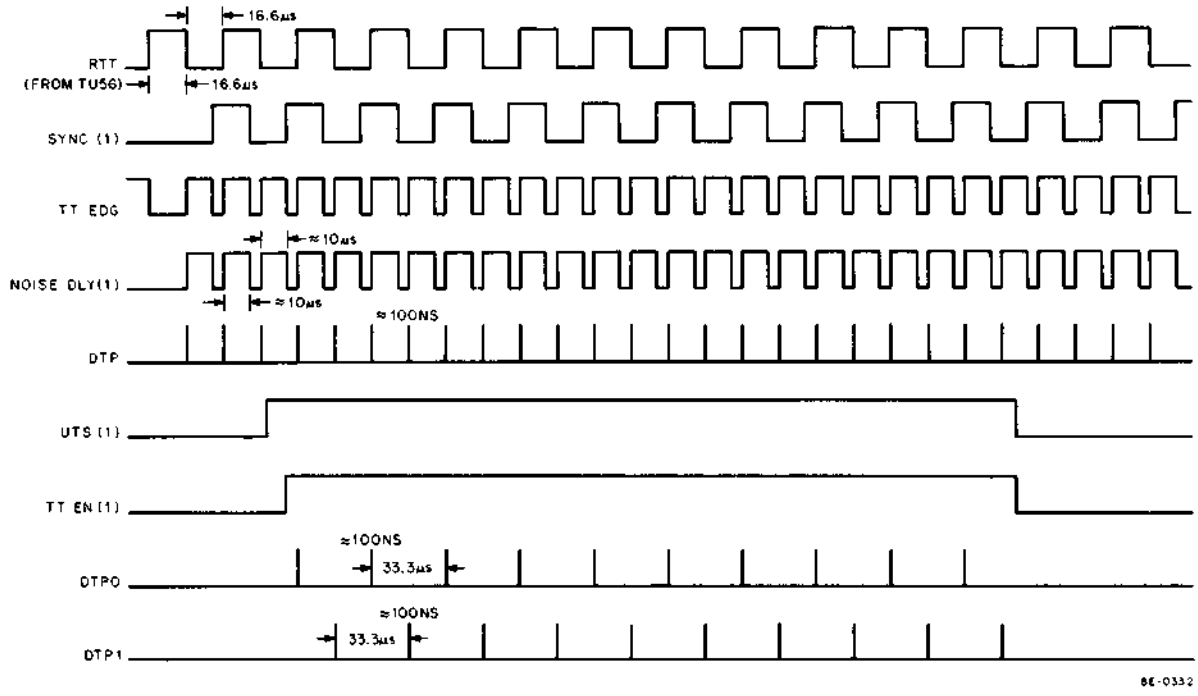

Figure 8-12 Read Time Track Pulse Timing

Note the WTM switch must be OFF when tapes are not being formatted. If it is in the WTM position and the tape moves (but it is not being formatted) the time and mark tracks will be destroyed and the tape must be formatted.

The third leg of gates A and B is enabled by DTP out of the 100-ns monostable multivibrator which is triggered by the rising edge of the 10-μs NOISE DLY.

The logic to produce CC DTP1 and CC DTP0 is the same as that for writing the time track. The only difference is that now the signal that generates these pulses is the time track (RTT) coming from the TU56M, rather than being generated on the M868. The SYNC flip-flop separates the DTP pulses through gates A and B, rather than CC TPG 0 and gates C and D.

As before SYNC is one input to the Exclusive-OR gate which triggers the NOISE DLY every time RTT and SYNC are at equal levels. The result is that DTP is produced on each edge of the RTT signal (Figure 8-12). When SYNC is set gate A is enabled and the DTP produced on the rising edge of RTT goes through gate A and comes out as CC DTP0. When SYNC is cleared, gate B is enabled and DTP produced on the falling edge of RTT goes through gate B and comes out as CC DTP1.

Thus, the time pulses are produced to shift in the data, set the flags, set WD ENAB (Figure 8-10) and shift the data out for writing, etc.

8.11 FLAGS AND SKIP LOGIC

The Single Line flag and Quad Line flag are used to count lines of data read from or written onto the tape and to enable skip logic when the CC SDSS or CC SDSQ instructions are performed (Figure 8-13). Time Error flag indicates the timing of a transfer was not correct and enables the skip logic when the SDST instruction is executed.

8.11.1 Single Line Flag

The Single Line flag (SLF) is used to detect codes on the mark track. SLF is set by CC DTP1 each time a line of data is read from the DECtape. If SLF is set and the SDSS instruction is executed, the SKIP line on the OMNIBUS is grounded, causing the program to skip to the next instruction. The SKIP could cause a subroutine to be performed to determine what code is in the Mark Track Register and take action accordingly; i.e., is the code a Block Mark? If so, read the Data Register, and check to see if it is the block number required. Is it an End Zone Mark? If it is, then you have run out of tape; stop, then reverse direction to continue. SLF is ignored by the program after the correct block of data has been found, as the program must keep track of the number of words being transferred and put the parity word at the end of the data.

8.11.2 Quad Line Flag and Counter Logic

The Quad Line Flag (QLF) (Figure 8-13) sets each time the counter made up of flip-flops B and C counts up to four, indicating four lines of data have been read from or written onto the DECtape. DTP1 is applied to the clock (C) input to cause the counter to increment each time a line of data is transferred. When QLF is set and the SDSQ instruction is performed, the SKIP line on the OMNIBUS is grounded causing the program to skip to the next instruction and call a routine to either load or read the Data Register. The 1 output of QLF is also applied to the logic to detect a TIME ERROR (Figure 8-13), as stated before SLF and QLF are cleared by instructions CC SDRC, CC SDRD, or CC SDLD, and the loss of UTS.

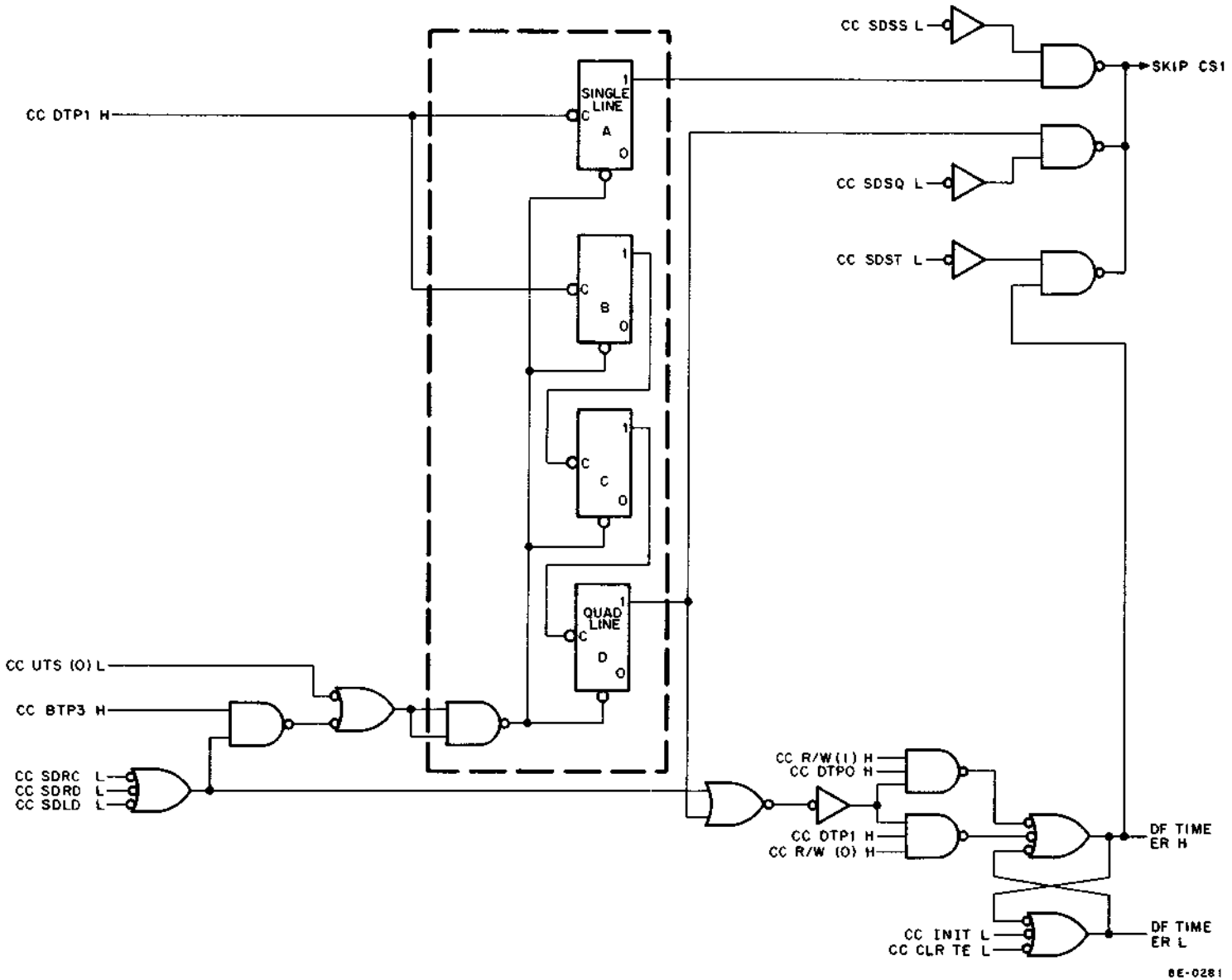

Figure 8-13 Single Line Flag, Quad-Line Flag, and Skip Logic

8.11.3 Time Error Flag

The Time Error flag (Figure 8-13) is a latch made from two 7410 gates which sets and generates a TIME ERROR to indicate the program did not transfer data to or from the Data Register before the next byte has transferred to or from the tape. Any of the following conditions will generate a TIME ERROR:

a. QLF (1), DTP0 H, and R/W Set (1) (Write Operation)

b. QLF (1), DTP1 H, and R/W Cleared (0) (Read Operation)

c. If SDRC, SDRD, or SDLD is executed just as the tape is ready to transfer another byte.

TIME ERROR is cleared by INITIALIZE or an SDLC instruction. When TIME ERROR is set and the SDST instruction is executed, the SKIP line is grounded, causing the program to skip the next instruction.

8.12 MARK TRACK REGISTER

The Mark Track (MT) Register (Figure 8-14) receives serial data from the mark track (RMT) containing the mark track codes and outputs 6 bits of parallel data for transfer to the AC. The MT Register is made up of two 8271 ICs. (See Appendix A.8, Volume 1, for timing diagram pin locator and truth table). The 8271 IC is a 4-bit shift register that receives a parallel serial input and provides a parallel output. The parallel output is applied to the Data Register (Figure 8-16) for the transfer to the AC during an SDRC instruction.

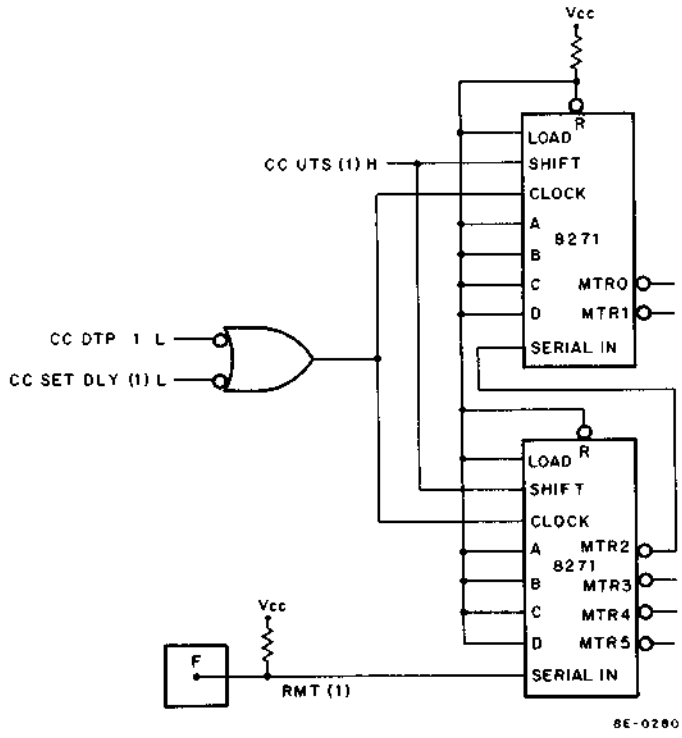

Figure 8-14 Mark Track Register

The output of the MT Register has been redefined; i.e., 1 is a low level and a 0 is a high level output.

The MT Register is cleared when SET DLY is cleared. When SET DLY is set UTS is cleared, so the CC UTS (1) signal on the shift input is low. When SET DLY is cleared it enables the clock input of the 8271, and as the parallel data output are held high the outputs all go high (redefined as 0 output). As stated before, the program must wait at least six SLFs before the MT Register holds a real mark track code.

8.13 DATA REGISTER AND GATING LOGIC

The Data Register (Figure 8-15) receives data from the DATA BUS and converts it to serial data to be written on the DECtape or takes serial data from the DECtape and converts it to parallel data to be gated to the DATA BUS for transfer to the AC. The Data Register consists of three 8271 ICs (see Volume 1, Paragraph A.8, for timing diagram, pin location, and logic diagram) and logic to select the input from the DATA BUS (parallel) or the input from the tape (serial). The output (the data being written on tape) is taken from SR0, SR1, and SR2.

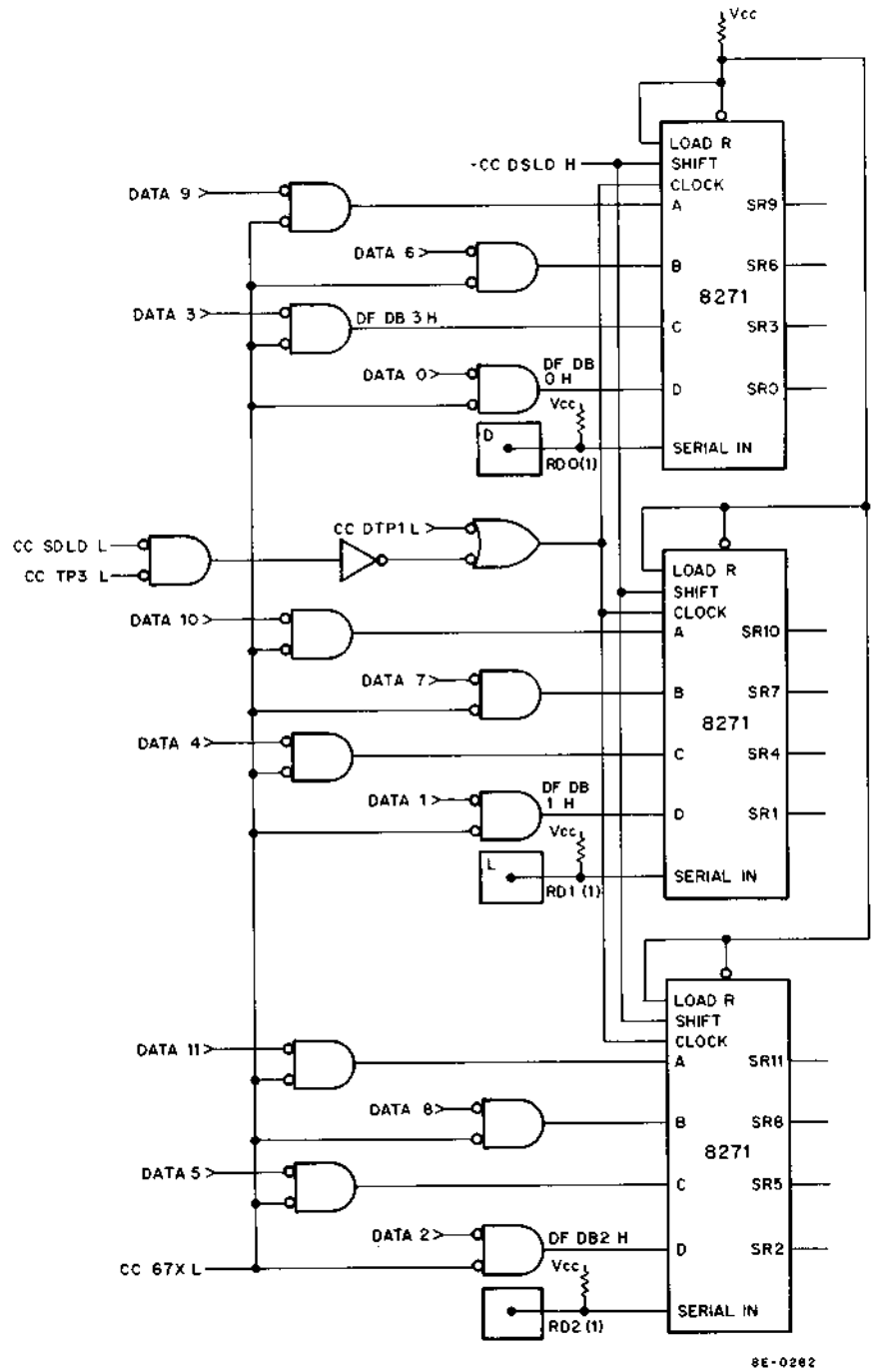

Figure 8-15 Data Register

Three outputs are shifted into the Write Register (Figure 8-17) to be written on tape. The serial input from the DECtape, RD0, RD1, or RD2 are shifted in by the CC DTP1 pulse and taken from the register as parallel data for transfer to the DATA BUS (Figure 8-16). The SDLD instruction is applied to the shift input to enable parallel transfer of data from the DATA BUS at TP3 time during a loading operation. At other times, the shift input is held high to enable serial shifting of data through the SR.

8.14 DATA GATING LOGIC

The data gating logic (Figure 8-16) will select the data to be applied to the DATA BUS for transfer to the AC by an SDRC or SDRD instruction. The SDRD instruction enables AND gates to transfer SR0–SR11 to the DATA BUS. SR0–SR11 are the 12 data bits read from the tape, applied to the Data Shift Register as serial data, and output to the data gating logic as 12 bits of parallel data. The SDRC instruction enables AND gates to transfer the contents of the Command Register, Status Bits, and MT Register to the DATA BUS.

8.15 WRITE FUNCTION REGISTER

The Write Function Register (WF0, WF1, WF2) receives data from SR0, SR1, and SR2 (Figures 8-17 and 8-6) and outputs the data to the TU56M at the correct timing pulse times.

At CC DTP0 (rising edge of RTT) the data from the Shift Register is loaded into the WF Register. At the same time, the Complement Word (COMP WD) output of the latch goes high. COMP WD is then compared to the complement of the data loaded into WF through the Exclusive-OR gates and if they are the same level, the Word (WD) lines go high. If a 1 had been loaded into WF0 at the CC DTP0, then its output would have been low. At CC DTP1 (falling edge of RTT) COMP WD goes low and WF0 will go high. The positive transition at CC DTP1 causes a 1 to be written on tape. If a 0 had been written into WF0, then between CC DTP0 and CC DTP1 the WD0 signal would be high. When COMP WD switches low at CC DTP1, there is a negative transition at WD0 and a 0 is written on tape. By examining the write timing diagram (Figure 8-6) you can see how alternating 1s and 0s always produce a negative transition for a 0 and a positive transition for a 1.

8.16 WRITE ECHO AND SELECT ECHO CIRCUITS

WRITE ECHO and SELECT ECHO (Figure 8-18) are supplied to the TD8-E by the TU56M. A SEL ERR condition exists if no unit has been selected or both units have been selected. Write Lockout exists if the selected drive unit is not Write Enabled. The voltage level for these signals and the resulting error condition are shown in Table 8-6.

The SEL ERR and WRITE LOCKOUT ERROR signals are applied to the data gates (Figure 8-16) as status bits to be transferred to the AC by an SDRC instruction. The software must decide what to do when these errors are detected. Both errors clear the R/W flip-flop to keep from writing under an error condition.

SECTION 5 MAINTENANCE

Recommended preventive maintenance should be scheduled on a regular basis to maintain the reliability and performance of the DECtape. Preventive maintenance schedules are found in the *TU56 DECtape Transport Maintenance Manual,* Chapter 6, Paragraph 6.2.

TD8-E DECtape Diagnostic (MAINDEC-08-DHTDA) and TD8-E Formatter (DEC-8E-EUZC-PB) were written to checkout and test the TD8-E DECtape Control with TU56M DECtape Transports. The diagnostic program and formatter check all logic, as well as the ability to read and write. The diagnostic also provides subroutines for monitoring TD8-E signals with an oscilloscope and display data in the AC. When a malfunction is suspected the TD8-E Diagnostic should be used to checkout and troubleshoot the TD8-E. Refer to the *TU56 Maintenance Manual* for test equipment, troubleshooting aids, and adjustments.

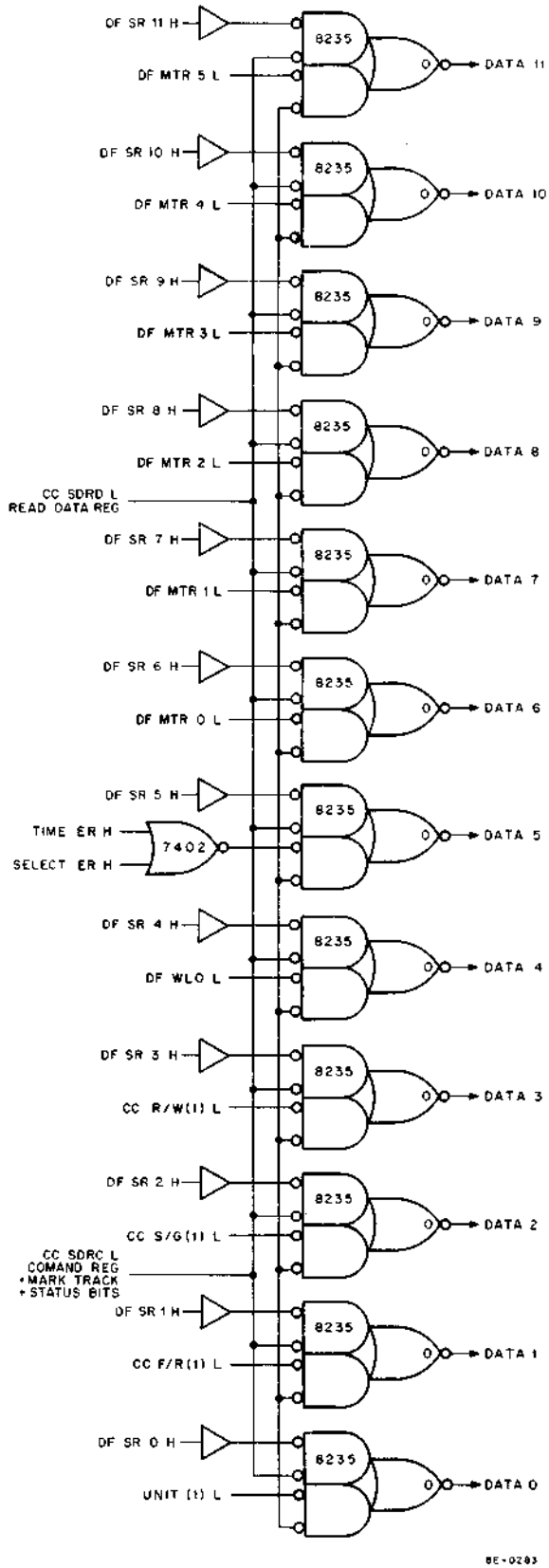

Figure 8-16 Data Gating Logic

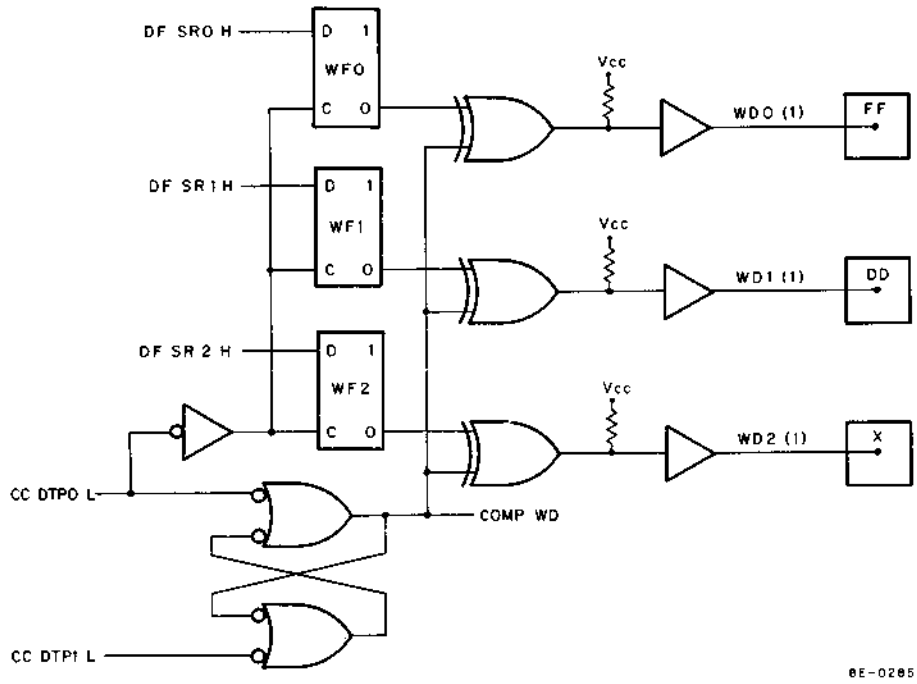

Figure 8-17 Write Function Register

Table 8-6

Write Echo and Select Echo Signal and Voltage Levels

Signal Voltage Level	Resulting Condition
WRITE ECHO 0V (Write Enable)	Write Lockout False
WRITE ECHO -3V (Write Lockout)	Write Lockout True
SELECT ECHO -3V (2 units selected)	Select Error (True)
SELECT ECHO -5V (1 unit selected)	Select Error (False)
SELECT ECHO -15V (No unit selected)	Select Error (True)

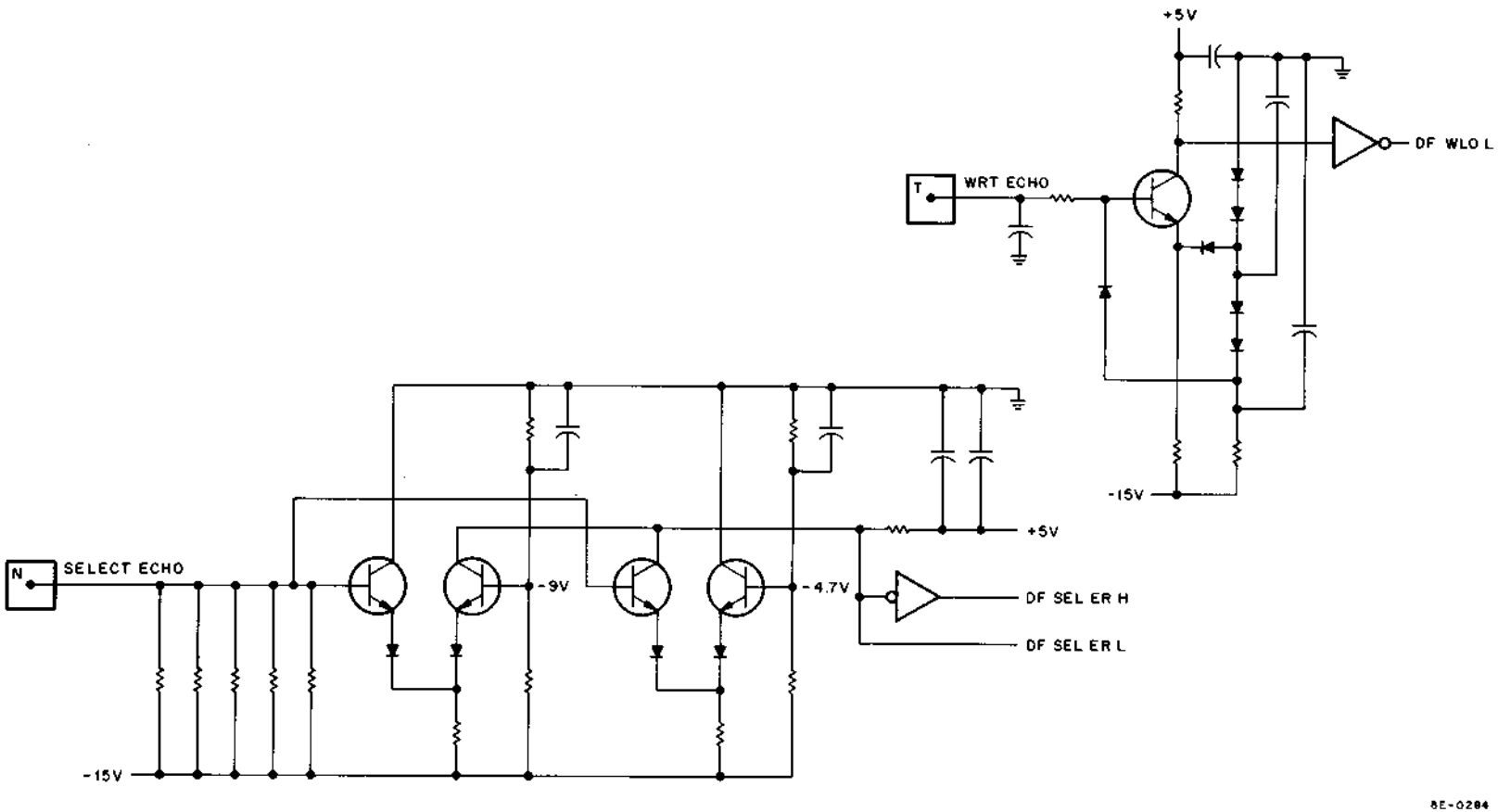

Figure 8-18 Write Echo and Select Error Circuits

SECTION 6 SPARE PARTS

Table 8-7 lists recommended spare parts for the TD8-E. These spare parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 8-7
TD8-E Recommended Spare Parts

DEC Part Number	Description	Quantity
19-10436	IC 74123	1
19-09935	IC 8235	1
19-09931	IC DEC 74H04	1
19-09929	IC DEC 7417	1
19-09712	IC DEC 8242	1
19-09705	IC DEC 8881	1
19-10391	IC DEC 5314	1
19-09686	IC DEC 7404	1
19-09615	IC DEC 8271	2
19-09594	IC DEC 8251	1
19-10394	IC DEC 5384	1
19-10392	IC DEC 5380	2
19-09054	IC DEC 7493	1
19-09050	IC DEC 7475	1
19-09004	IC DEC 7402	1
19-05590	IC DEC 7401	1
19-05578	IC DEC 7430	1
19-05576	IC DEC 7410	2
19-05575	IC DEC 7400	2
19-05547	IC DEC 7474	2
15-09338	Transistor DEC 6351	2
11-00114	Diode, D664	2
11-00113	Diode, D662	2