CHAPTER 3
MR8-E READ-ONLY MEMORY

SECTION 1 INTRODUCTION

3.1 READ-ONLY MEMORY DESCRIPTION

The MR8-E is a 256-word Read-Only Memory (ROM) option used in the PDP-8/E. The MR8-E consists of an M880 Quad Module that is inserted into the OMNIBUS and an H241 Braid Board mounted on the M880 Module. The thickness of the module and braid board requires that two spaces be allotted for this option on the OMNIBUS, although the MR8-E plugs into only one of these spaces. Each ROM option occupies two pages (400_8 locations) of the 32_{10} pages (7777_8 locations) in each field. The MR8-E can be located starting at the beginning of any even-numbered page in any field, such as 0000_8, 00400_8, or 64400_8. Note that the corresponding core memory locations cannot be used by the software while the MR8-E is installed in the OMNIBUS. When a memory location assigned to the MR8-E is addressed, ROM ADD L will be asserted which, in turn, disables core memory.

From a programming point of view, and as viewed from the OMNIBUS, the MR8-E is addressed the same way as core memory (Paragraph 3.24, Volume 1). Within the MR8-E these 400_8 words are organized as 200_8 lines, each running through or around 24 ferrite cores (two 12-bit words). Each drive line is terminated by a diode on one end and by a switch tied to a decoder on the other end. The memory locations are selected by MA00 to MA11 and EMA00 to EMA02. The MR8-E is interfaced to the processor by the OMNIBUS.

SECTION 2 INSTALLATION

The MR8-E will be installed on site by DEC Field Service personnel. The customer should **not** attempt to unpack, inspect, install, checkout, or service the MR8-E Module.

3.2 INSTALLATION

Perform the following steps to install the MR8-E Read-Only Memory:

Step	Procedure
1	Remove power from the PDP-8/E by turning Power Switch to OFF.
2	Ensure proper diodes are installed in the M880 Module to select the starting address of ROM (drawing CS-M880-0-1).
3	Insert the MR8-E (M880 and H241) into the OMNIBUS (refer to Table 2-3, Volume 1) for module installation priority.

3.3 ACCEPTANCE TEST

Perform the following steps to check the MR8-E Modules:

Step	Procedure
1	Load ROM Test Tape Low (MAINDEC-8E-D1JA-PB1) or ROM Test Tape High (MAINDEC-8E-D1JA-PB2). Refer to diagnostic write up for correct loading procedures.
2	Allow the diagnostic to run for 20 minutes with no errors.

NOTE
Refer to Section 5 for the procedure to change ROM contents if errors are found.

SECTION 3 SYSTEM DESCRIPTION

3.4 MR8-E BLOCK DIAGRAM

The MR8-E consists of an M880 Drive and Sense Module and an H241 Braid Board Assembly. The M880 Module contains the logic for addressing 256 words of memory located on the H241 Braid Board Assembly. The MR8-E is addressed in the same way as PDP-8/E Core Memory (Paragraph 3.24, Volume 1). If the MR8-E is placed in the same field with a 4K core memory, the two pages of core memory with the same addresses as ROM cannot be accessed by the program. If the software tries to write in ROM, the new information will be lost and the contents of ROM will not be changed. When the MR8-E detects an address to which it must respond it asserts ROM ADD L (Figure 3-1) which disables core memory. The 400_8 words of the MR8-E memory are organized as 200_8 lines with each line containing two words. The 200_8 lines run through or around 24_{10} ferrite cores and sense windings (Figure 3-2). Each of the 200_8 lines is terminated by a diode at one end and in 8 groups of 16_{10} lines tied to the outputs of a BCD decoder at the other end.

3.5 ROM ADDRESSING

Addressing of the 400_8 locations is accomplished as follows.

a. The three EMA lines and the four most-significant MA lines (MA00—MA03) are decoded in Address Selection AND gate within the MR8-E to determine whether the currently addressed location is within the option. The Address Selection gate consists in part of 14_{10} diodes, seven of which must be removed to define the combination of EMA and most-significant MA bits for which the MR8-E is active. If the MR8-E is selected, a gate at the output of the Address Selection gate asserts (grounds) the ROM ADD L line on the OMNIBUS, thereby disabling the core memory that would normally respond to that address. In addition, a second output of the Address Selection gate (labeled FIELD L on the logic diagrams) enables decoding of the remaining MA lines.

b. MA04 through MA07 are decoded and select one of 20_8 (16_{10}) drivers, each of which is connected to 10_8 (8_{10}) diodes.

c. MA08 through MA10 select one output of the line select decoder which is a BCD-to-decimal decoder. One of 10_8 outputs from the BCD-to-decimal decoder is selected and forward biases the diode selected by MA04 through MA07 so that current will flow through the selected line and induce a signal in the sense winding if it passes through the core. Data is taken from the MR8-E using high-permability ferrite U- and I-cores mated to form a closed magnetic path. The 200_8 lines run through or around the 24_{10} U-cores, the 24 I-cores are wound with a 50-turn sense winding. When current is driven through a selected line, which passes through the mated core, a 2.5V to 3.0V signal is magnetically induced in the winding. The signal induced in the sense winding is fed to a DTL-type gate and clocked by a strobe pulse. If the selected line passes around (not through) the mated core, no signal is induced in the sense winding.

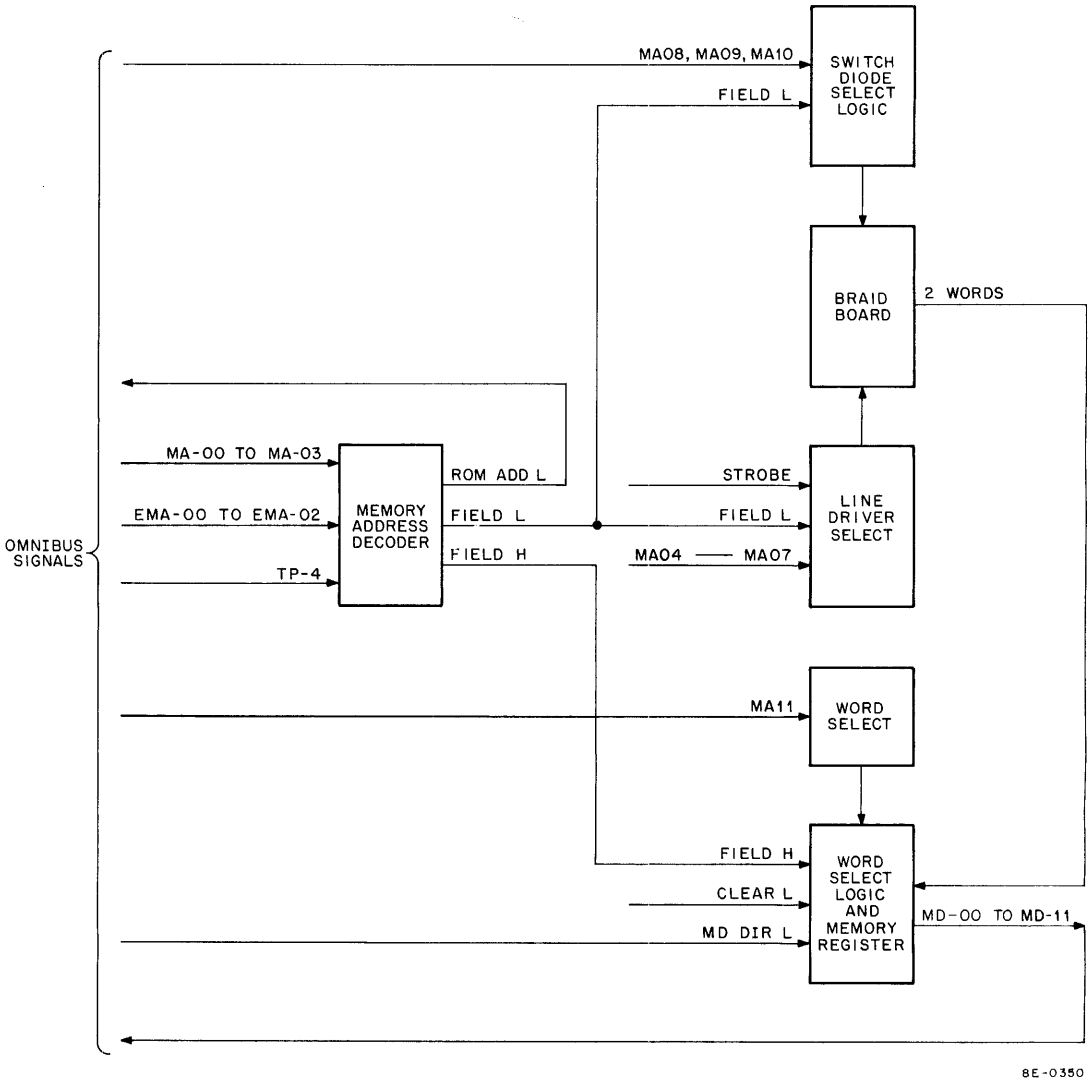


Figure 3-1 Read-Only Memory Block Diagram

d. The selected line causes a 24-bit word to be read. MA11 controls which half of the addressed word is applied to the Memory Register. The output of the DTL gates is clocked into a 12-bit Memory Buffer Register.

e. FIELD H, NOT CLEAR L and MD DIR L enable the output of the Memory Register to the MD lines.

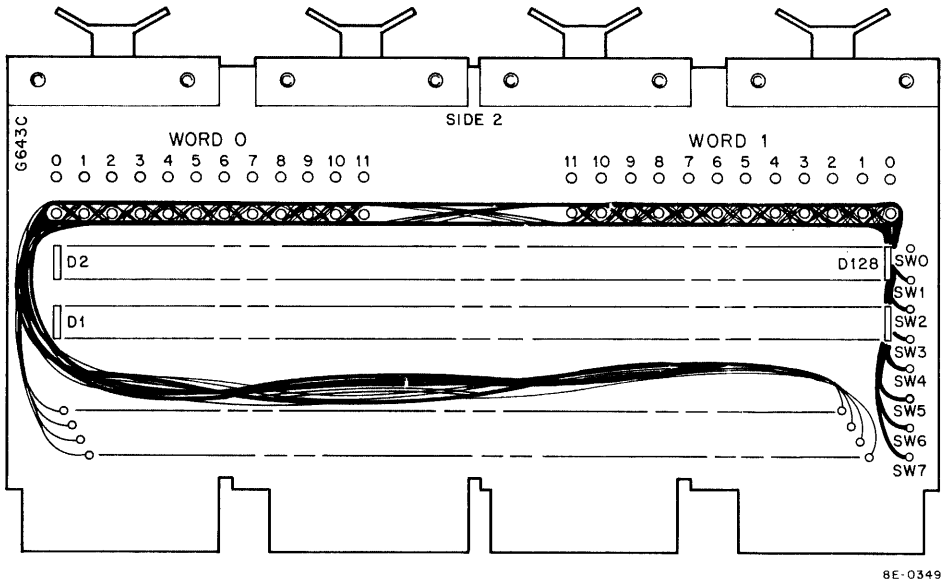


Figure 3-2 H241 Braid Board

SECTION 4 DETAILED LOGIC

The logic in the MR8-E is broken into functional groups for discussion purposes. The block diagram in Figure 3-1 should be used to understand the interaction of the groups of logic.

3.6 ADDRESS DECODER

The Address Decoder (Figure 3-3) receives bits MA00 through MA03 and EMA00 through EMA02 for decoding. The 14 diodes (7 of which are removed) select the high-order address of ROM. If the MA and EMA bits indicate the selected address is within ROM FIELD L, ROM ADD will be asserted, so that only ROM can be accessed by the program. FIELD L enables gates to allow MA04 through MA11 to be decoded and used to select a line driver, switch, and word 0 or 1.

3.7 SWITCH SELECT LOGIC

The switch select logic (Figure 3-4) decodes MA08 through MA10 and selects one of the groups of diodes on the H241 Braid Board Assembly using the proper switch line. FIELD L is used to enable E26 AND gates and the output of the AND gates is applied to the 74145 IC. The 74145 IC is a BCD-to-decimal decoder that pulls one of the output lines low when the 3-bit input is decoded. The output of E27 is applied to the 8 switches that enable the selection of the proper diode and one of the 16 line drivers (Figure 3-5).

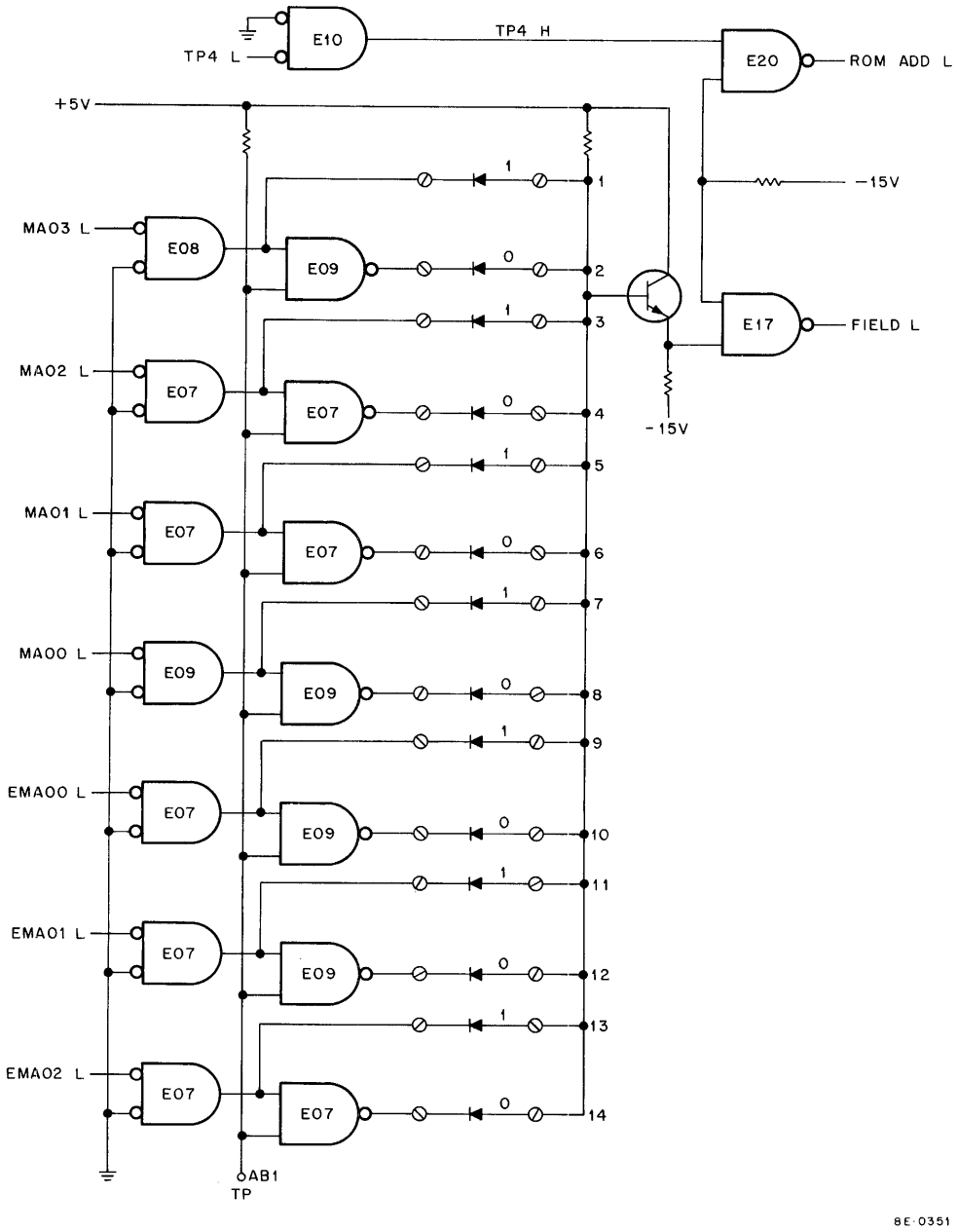


Figure 3-3 Address Decoder Logic

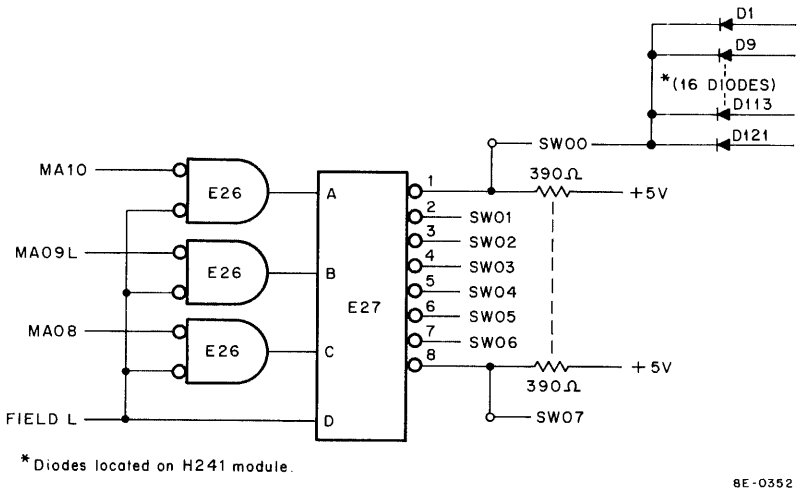


Figure 3-4 Switch Select Logic

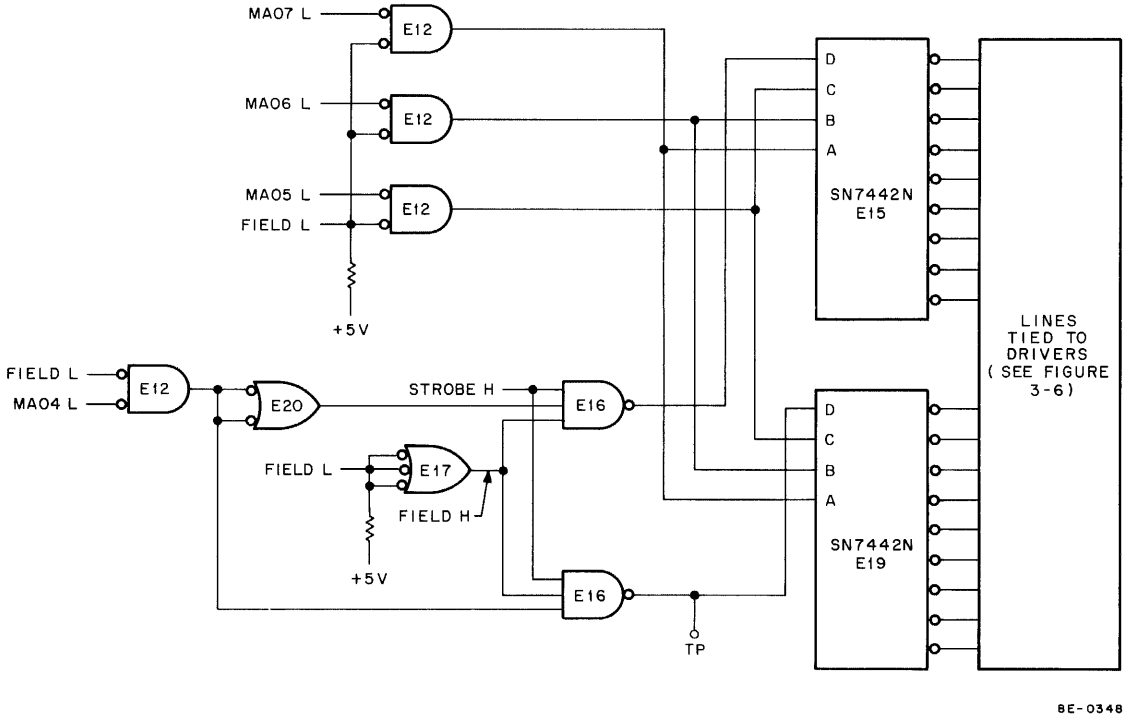


Figure 3-5 Line Driver Select Logic

3.8 LINE DRIVER SELECT LOGIC AND LINE DRIVERS

The line driver select logic (Figure 3-5) decodes MA04 through MA07 and selects one of the 16 line drivers. Each line driver has 8 diodes in its collector circuit, each of which is tied to one end of the 8 switch lines on the braid board (Figure 3-6). There are 16 line drivers, with 8 diodes each, to select 128 lines (256 words) on the braid board. The E12 AND gates are enabled by FIELD L; MA05 through MA07 are applied to E15 and E19. E15 and E19 are BCD-to-decimal decoders that assert one output line for each input and cause the line driver to forward bias 8 diodes. MA04 is used to select a control input at pin D on E15 or E19. When MA04 is 1 (low), E20 is disabled and input D of E19 has a low enabling input that allows E19 to pull one output low and select one of its line drivers. When MA04 is 0 (high), E20 and E16 are enabled and input D of E15 has a low (enabling) input. Note that each line driver has 8 diodes tied to 8 different switch lines in the diode matrix (Figure 3-6). When the diode is selected by a line driver and the switch on the other end of a line is selected, current flows through that line and induces a voltage in the sense windings of those cores that have a line passing through them. Table 3-1 lists the lines in the braid board and the two words associated with each line.

The diode tied to each line has the same numerical designation as the line, i.e., line 1 has D1 tied to one end.

3.9 SENSE LOGIC AND MEMORY REGISTER

The sense windings of the 24 ferrite cores are tied to DTL AND gates (Figure 3-7) on the M880 Module. As stated previously, when current flows through the selected line a voltage is induced in the sense windings shown as A1 through A11 for word 0, and B1 through B11 for word 1. MA11 applied to E26 allows one of the words to be applied to the Memory Register when FIELD L and STROBE L are applied to E24. If MA11 is 0, word 0 (sense winding A) is applied to the Memory Register; if MA11 is 1, word 1 (sense winding B) is applied to the Memory Register.

The Memory Register is made up of 12 set-reset type flip-flops that hold the 12 bits of data until MD DIR L, NOT CLEAR L and FIELD H are received. The result enables the AND gates and applies the contents of the Buffer Register to the MD lines.

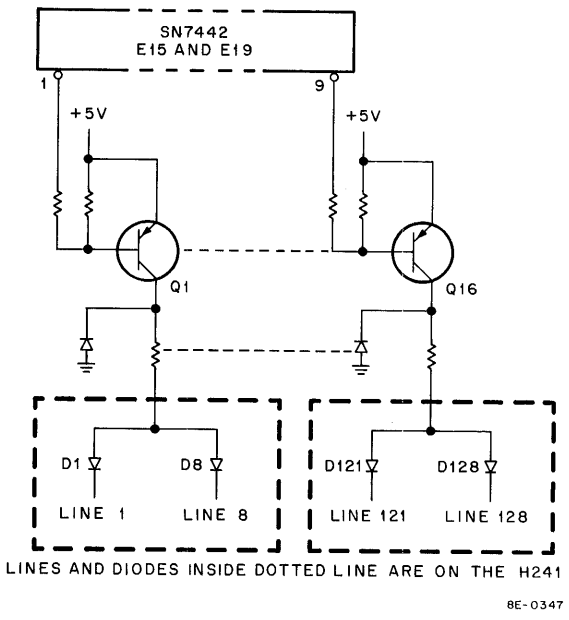


Figure 3-6 Line Drivers and Diodes

Table 3-1
Line and Switch Identification for ROM Addresses

Line Number	Addresses*	Sw. Term	Line Number	Addresses*	Sw. Term
1	000,001	0	41	120,121	0
2	002,003	1	42	122,123	1
3	004,005	2	43	124,125	2
4	006,007	3	44	126,127	3
5	010,011	4	45	130,131	4
6	012,013	5	46	132,133	5
7	014,015	6	47	134,135	6
8	016,017	7	48	136,137	7
9	020,021	0	49	140,141	0
10	022,023	1	50	142,143	1
11	024,025	2	51	144,145	2
12	026,027	3	52	146,147	3
13	030,031	4	53	150,151	4
14	032,033	5	54	152,153	5
15	034,035	6	55	154,155	6
16	036,037	7	56	156,157	7
17	040,041	0	57	160,161	0
18	042,043	1	58	162,163	1
19	044,045	2	59	164,165	2
20	046,047	3	60	166,167	3
21	050,051	4	61	170,171	4
22	052,053	5	62	172,173	5
23	054,055	6	63	174,175	6
24	056,057	7	64	176,177	7
25	060,061	0	65	200,201	0
26	062,063	1	66	202,203	1
27	064,065	2	67	204,205	2
28	066,067	3	68	206,207	3
29	070,071	4	69	210,211	4
30	072,073	5	70	212,213	5
31	074,075	6	71	214,215	6
32	076,077	7	72	216,217	7
33	100,101	0	73	220,221	0
34	102,103	1	74	222,223	1
35	104,105	2	75	224,225	2
36	106,107	3	76	226,227	3
37	110,111	4	77	230,231	4
38	112,113	5	78	232,233	5
39	114,115	6	79	234,235	6
40	116,117	7	80	236,237	7

*These addresses are within the MR8-E. To get the absolute address, add the starting address of the MR8-E to the MR8-E addresses, i.e., MR8-E starts at 4400, line 123 contains absolute addresses 4764 and 4765. 4764 is word 0 and 4765 is word 1. The word will be selected by Bit 11 applied to the MR8-E.

Table 3-1 (Cont)
Line and Switch Identification for ROM Addresses

Line Number	Addresses*	Sw. Term	Line Number	Addresses*	Sw. Term
81	240,241	0	105	320,321	0
82	242,243	1	106	322,323	1
83	244,245	2	107	324,325	2
84	246,247	3	108	326,327	3
85	250,251	4	109	330,331	4
86	252,253	5	110	332,333	5
87	254,255	6	111	334,335	6
88	256,257	7	112	336,337	7
89	260,261	0	113	340,341	0
90	262,263	1	114	342,343	1
91	264,265	2	115	344,345	2
92	266,267	3	116	346,347	3
93	270,271	4	117	350,351	4
94	272,273	5	118	352,353	5
95	274,275	6	119	354,355	6
96	276,277	7	120	356,357	7
97	300,301	0	121	360,361	0
98	302,303	1	122	362,363	1
99	304,305	2	123	364,365	2
100	306,307	3	124	366,367	3
101	310,311	4	125	370,371	4
102	312,313	5	126	372,373	5
103	314,315	6	127	374,375	6
104	316,317	7	128	376,377	7

*These addresses are within the MR8-E. To get the absolute address, add the starting address of the MR8-E to the MR8-E addresses, i.e., MR8-E starts at 4400, line 123 contains absolute addresses 4764 and 4765. 4764 is word 0 and 4765 is word 1. The word will be selected by Bit 11 applied to the MR8-E.

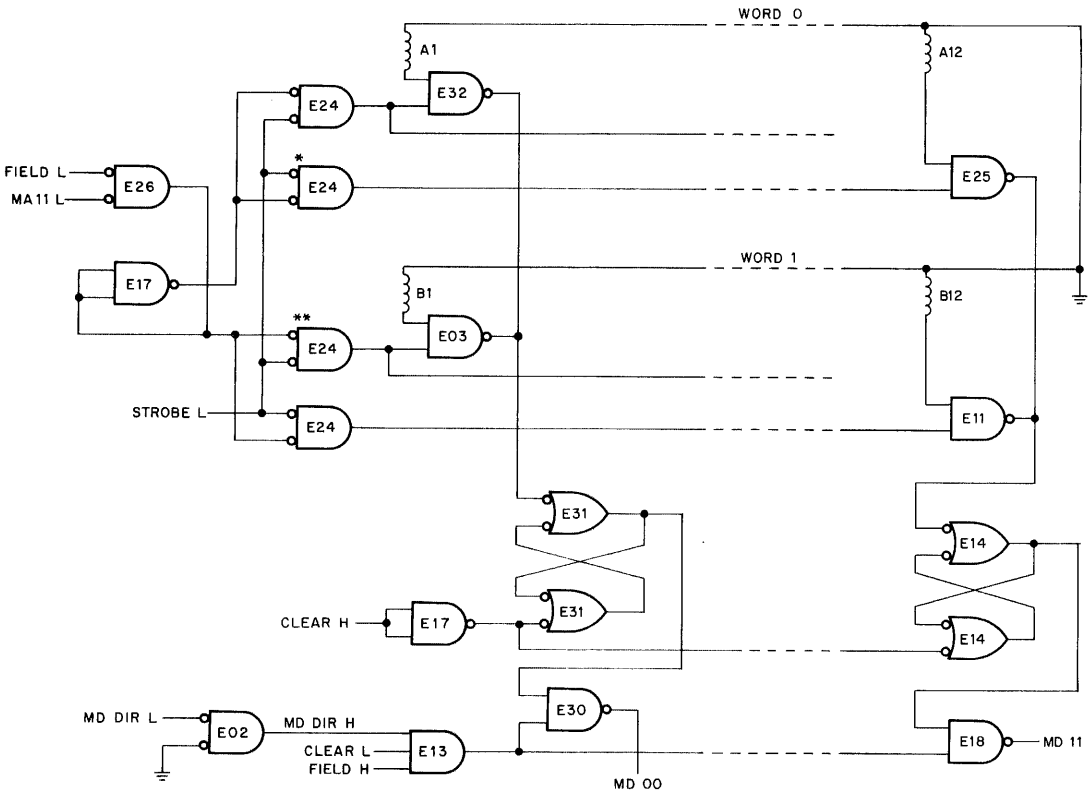
3.10 CLEAR LOGIC

The clear logic (Figures 3-8 and 3-9) clears the Memory Register and enables gates to place data from the Memory Register on the MD lines of the OMNIBUS. The Memory Register is cleared when RETURN H goes high (100 ns into the memory cycle) clearing the CLEAR flip-flop.

At STROBE TIME, the CLEAR flip-flop is set, enabling the Memory Register output gates (Figure 3-7) to transfer the contents of the Memory Register to the MD lines, when MD DIR is asserted (MD DIR on the OMNIBUS is low).

3.11 LINE SELECT DIODE MATRIX

The line select diode matrix (Figure 3-10) selects one of the lines which pass through or around the ROM core and allows current to flow through one line for each address. One end of each line is tied to a switch; the other end is tied to a diode. The diode is in the collector of a line driver (DR0 to DR15) and the selected diode is



* EACH GATE ENABLES HALF OF THE SENSE GATES
** DOTTED LINES INDICATE MISSING LOGIC IDENTICAL TO THAT SHOWN.

8E-0346

Figure 3-7 Sense Logic and Memory Register

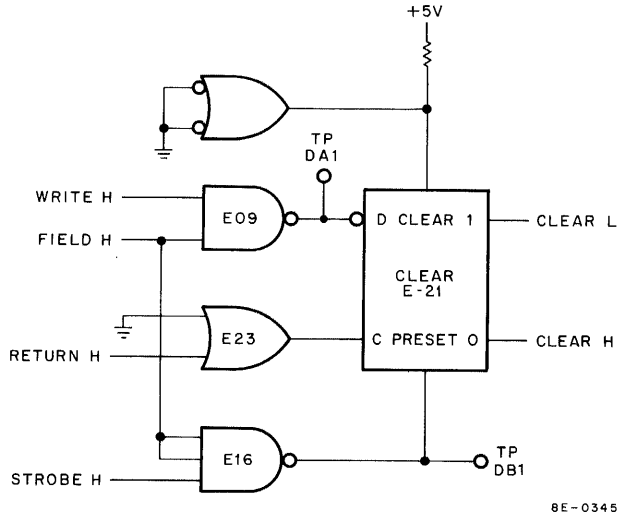


Figure 3-8 Clear Logic

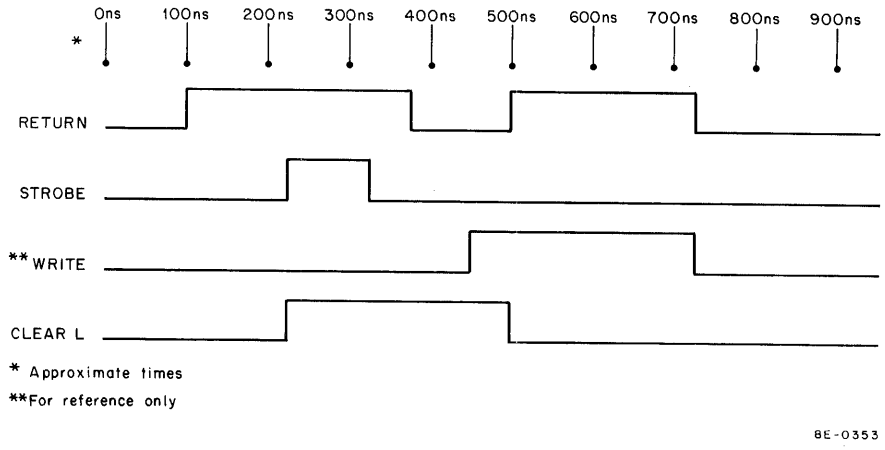


Figure 3-9 Read Timing Diagram

forward biased by the switch select logic to allow current flow through the line. Current flow through the line causes a voltage to be induced in the sense windings of the cores through which the line passes. This voltage is applied to the DTL logic (Figure 3-7) and gated to the Memory Register by MA11 and STROBE L.

SECTION 5 MAINTENANCE

The MR8-E diagnostic (MAINDEC-8E-D1JA-PB1 or MAINDEC-8E-D1JA-PB2) should be run when a ROM malfunction is suspected. Use the following procedure to change the contents of ROM or to correct errors.

Step	Procedure
1	Remove the H241 with cover and standoffs from M880.
2	With Side 2 of the H241 up, find the line that corresponds to the address of the word to be changed. Each line contains two words, so the 128 lines contain 256 addresses (Table 3-1). Cut the line to be changed.
3	Solder the new wire to the lug as follows: a. If you are placing new words in these addresses, string the wire through all 24 cores using all the tie down jumpers. The 24 cores correspond to the two 12-bit words of the line (Figure 3-2). For a logical 1, string the wire inside the "U" core; for a 0, string the wire outside the core. Terminate the wire on the proper switch (Table 3-1). b. If you are correcting an error in the MR8-E, the diagnostic program will provide all the information needed. A typical typeout would be as shown in Table 3-2. For this error, cut Line 5, replace it, and string wire through the cores as shown in the insert portion of the typeout. The 24 bits shown correspond one-to-one with the 24 cores on the board, from left to right. The line should be terminated on SW4. If an error occurs in the field, check the diode before replacing the line.
4	Check electrical continuity.

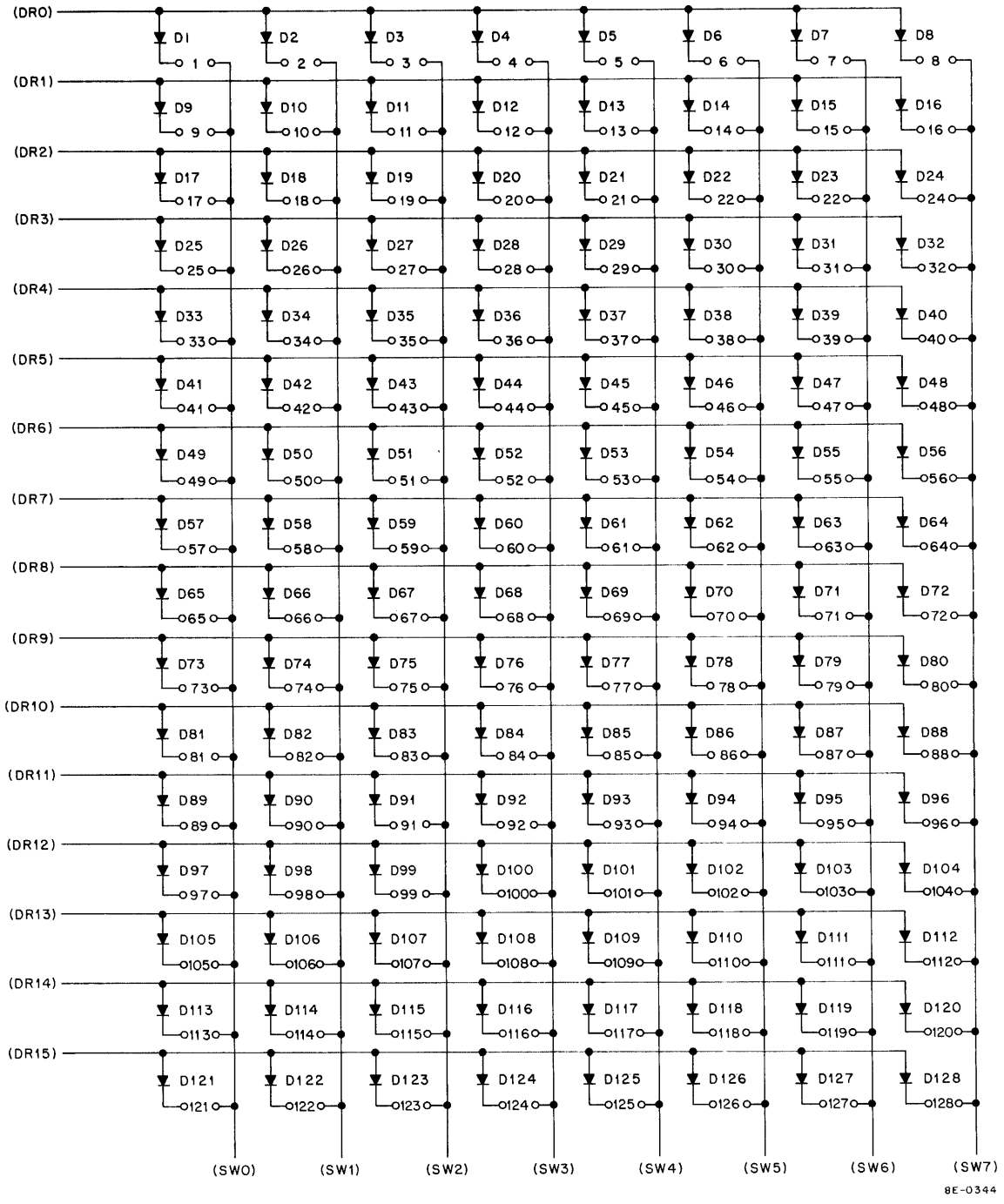


Figure 3-10 Line Select Diode Matrix

Table 3-2
Typical Error Typeout

ADDR	Good	Bad	Driver	Line	Diode	Insert	Term
7010	3635	3637	00	05	05	011110011101 010101010100	SW4

SECTION 6 SPARE PARTS

Table 3-3 lists recommended spare parts for the MR8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 3-3
Recommended MR8-E Spare Parts

DEC Part No.	Description	Quantity
15-05321	Transistor DEC 4258	2
15-03100	Transistor DEC 3009B	1
11-60114	Diode D664	10
19-10047	IC DEC 74145	1
19-10046	IC DEC 7442	1
19-09705	IC DEC 8881	1
19-09688	IC DEC 846	1
19-09667	IC DEC 74H74	1
19-09486	IC DEC 384	1
19-09971	IC DEC 6380	2
19-09267	IC DEC 74H11	1
19-09056	IC DEC 7402	1
19-05576	IC DEC 7410	1
19-05575	IC DEC 7400	2