CHAPTER 5
MP8-E MEMORY PARITY

SECTION 1 INTRODUCTION

5.1 MP8-E DESCRIPTION

The MP8-E Memory Parity option adds the circuits required to generate, store, and check the parity of memory words. The MP8-E consists of three quad boards, which are inserted into the OMNIBUS. An H220 Memory Stack is used to store parity for all words in memory. A G227 Memory X-Y Driver is used to provide word select currents. A special G105 Sense-Inhibit Module, which also contains IOT decoding, is used.

This option expands the memory system from 12 to 13 bits per word. When a word is written into memory, its parity is computed, and odd parity (odd number of binary ones in the 13-bit word) is generated and stored in the 13th, or parity, bit. When a word is retrieved from memory, the parity of the 13-bit word is checked. If even parity is detected, a memory error has occurred.

Much of the MP8-E is identical to the MM8-E 4K Core Memory described in Chapter 3, Section 4, Volume 1. The MP8-E is discussed in Chapter 7 of the *PDP-8/E & PDP-8/M Small Computer Handbook*. The reader should have a thorough understanding of this material before proceeding.

One major difference exists between the MP8-E and its description in the *PDP-8/E & PDP-8/M Small Computer Handbook*. The MP8-E is disabled whenever it encounters Read-Only memory. Thus, the initialization process described in the handbook is unnecessary. The CEP instruction (used for diagnostic purposes) will work, as described, as long as the next EXECUTE cycle deals with a location that does not ground the ROM ADDRESS L line on the OMNIBUS. (This EXECUTE cycle can even be the result of an indirect reference to a nonexistent memory field, if desired.)

SECTION 2 INSTALLATION

The MP8-E will be installed on site by DEC Field Service personnel. The customer should **not** attempt to unpack, inspect, install, test, or service the equipment.

5.2 INSTALLATION

Use the following procedure to install the MP8-E:

Step	Procedure
1	Ensure power is off.
2	Install the MP8-E on the position indicated in Table 2-3 of Volume 1.
3	Install the four H851 Edge Connectors between the three modules.

5.3 ACCEPTANCE TEST

To check the MP8-E, run the MP8-E diagnostic program, MAINDEC-8E-D1DA. The program should be run 15 minutes for each 4K MM8-E in the machine; e.g., if the machine has 16K of memory, run the diagnostic for 1 hour. Refer to the program writeup for instructions on how to run the program.

SECTION 3 PRINCIPLES OF OPERATION

Parity in the PDP-8/E is handled in a somewhat unconventional manner. The conventional method of handling parity is to use a special 13-bit memory stack and sense-inhibit system in each of the memory fields. In the PDP-8/E, however, the standard memory, Type MM8-E, is used for data and instruction storage, regardless of whether the system contains the parity option. When parity is desired, an additional memory is added. This special memory handles the parity bit for all possible memory fields. The advantage of this method of handling parity is that no special memory stack is required.

Figure 5-1 is a block diagram of the MP8-E. The lower half of this figure is identical to the lower half of Figure 3-33 in Volume 1; only the portion above the broken line is different. Eight of the twelve memory bits are used, corresponding to the eight possible fields. The FIELD signal into the G227 X-Y Driver is permanently enabled. Hence, during each memory cycle all eight parity bits are read and rewritten into the parity core memory.

Field select gating decodes the extended address bits (EMA 0, 1, and 2) and MD DIR L. The three EMA lines determine which of the eight parity bits are to be examined and possibly modified. All other bits are automatically rewritten from the local parity sense register. If MD DIR L is low, the selected bit is rewritten from the Sense Register. If MD DIR L is high, however, the parity of the twelve MD lines is written into the parity memory.

The selected bit read from the parity core memory is combined with the bits on the twelve MD lines. If parity is erroneous, the ERROR flip-flop is set. The ERROR flip-flop can be interrogated by a SKIP instruction, and can cause an interrupt. IOTs permit clearing of the Error flag, enabling the disabling of parity interrupt, and intentional reading of even parity for diagnostic purposes.

SECTION 4 DETAILED LOGIC

The G227 X-Y Driver and H220 Memory are discussed thoroughly in Volume 1. No attempt will be made in this chapter to duplicate that discussion. In addition, certain portions of the G105 are identical to corresponding parts of the G104 described in Volume 1. These portions are:

a.	Strobe Control Logic	(Vol. 1, Paragraph 3.27.8)
b.	Sense Amplifiers	(Vol. 1, Paragraph 3.27.9)
c.	Sense Flip-flops	(Vol. 1, Paragraph 3.27.10)
d.	Inhibit Drivers	(Vol. 1, Paragraph 3.27.12)
e.	Current Control Circuit	(Vol. 1, Paragraph 3.27.13)
f.	–6V Supply and Slice Control	(Vol. 1, Paragraph 3.27.14)

These parts will not be described here in detail.

5.4 FIELD SELECT GATING

The field select gating (Figure 5-2) connects the output of a SENSE flip-flop to the input of the corresponding Inhibit Driver. The output of gate A must be low in order to rewrite a 1 into the parity memory.

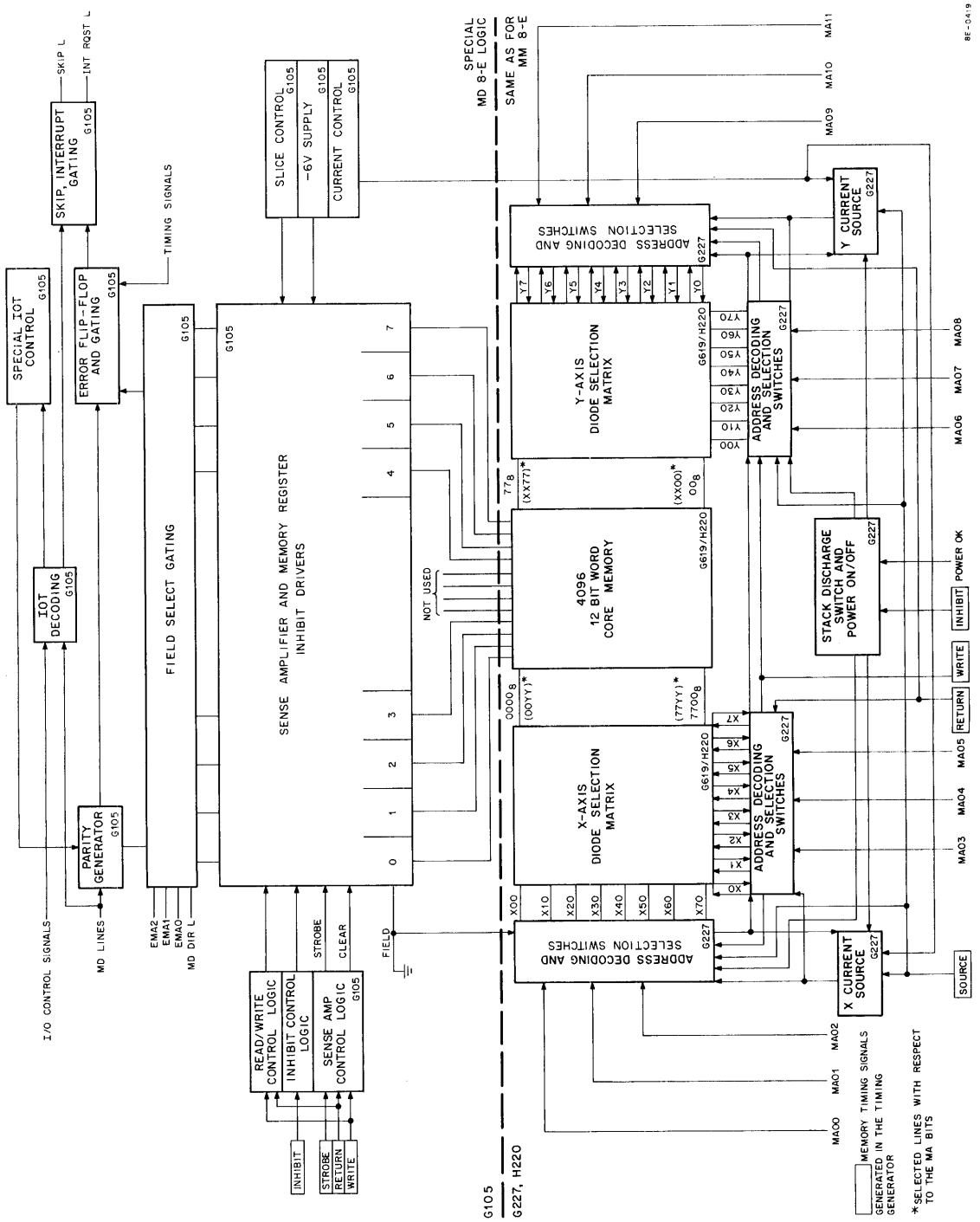

Figure 5-1 MP8-E Block Diagram

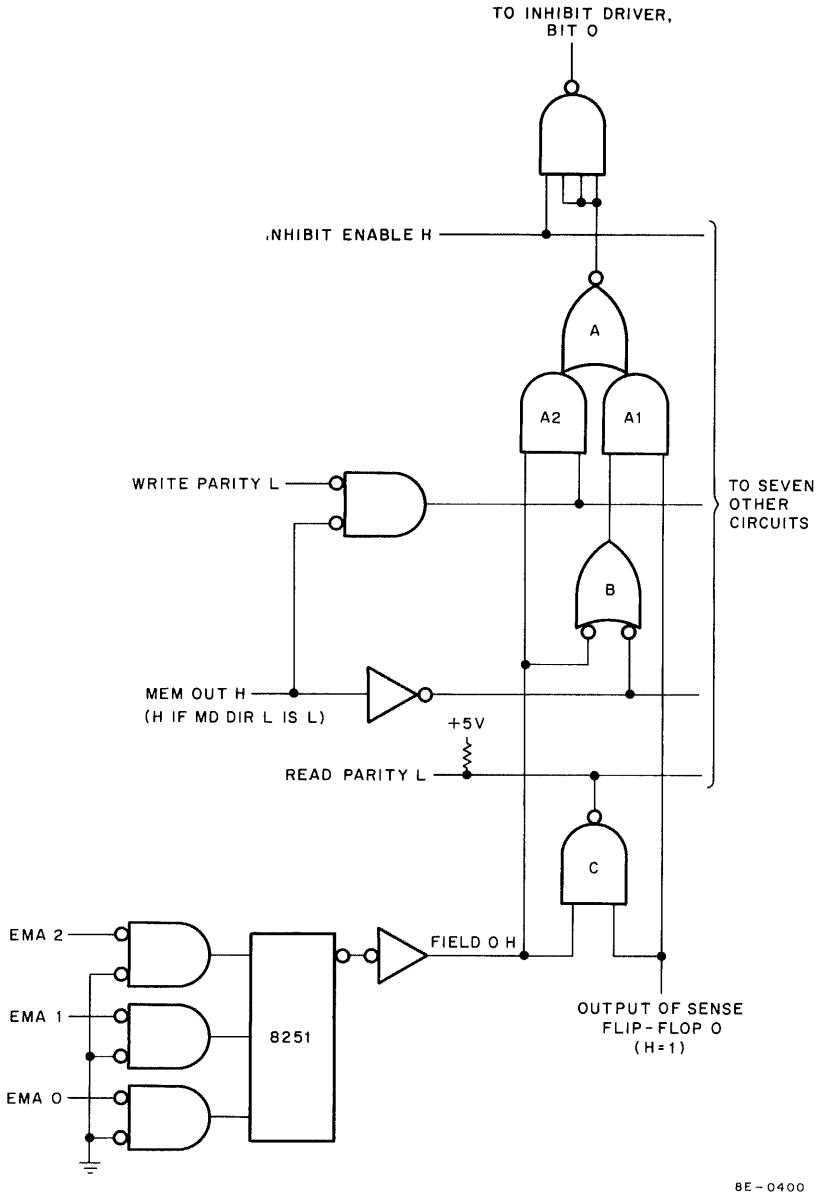

Figure 5-2 Field Select Gating

The EMA bits are buffered from the OMNIBUS and applied to the input of an 8251 Binary-to-Octal Decoder. One of the output lines of the 8251 is low for any combination of EMA bits. All outputs of the 8251 are inverted and applied to portions of the field select gating logic.

If the FIELD 0 H line in Figure 5-2 is low (field 0 is not selected), gates A2 and C are disabled. The output of gate B is high, enabling gate A1. Thus, the output of SENSE flip-flop 0 is applied, via gate A, to the input of the Inhibit Driver, writing the previously read bit back into memory.

If the FIELD 0 H line is high, Field 0 has been selected. The output of SENSE flip-flop 0 is gated onto the READ PARITY L bus via gate C. The source of information for the Inhibit Driver is now a function of MD DIR L. If MD DIR L is low during the latter half of the memory cycle (as it is for all fetches and non-autoindexed defers), gate B is enabled and the SENSE flip-flop provides the rewrite data. If MD DIR L is high, gate A1 is disabled, gate A2 is enabled, and WRITE PARITY L provides the data for the Inhibit Driver. A low on WRITE PARITY L writes a 1 in the parity bit.

5.5 PARITY GENERATOR

The heart of the Parity Generator is the 74180 8-bit parity generator IC which is shown in Figure 5-3. Two of these ICs are cascaded to form the 12-bit gated parity generator shown in Figure 5-4. Line A is high if a 1 has been read as the parity bit from memory. As will be discussed in Paragraph 5.6, the ODD PARITY H line is sampled part way through the memory cycle, before MD DIR L can go high. During the latter half of the memory cycle, if MD DIR L goes high, odd parity is sent to the selected Inhibit Driver via the WRITE PARITY L line. (The state of WRITE PARITY L is ignored by the field select gating if MD DIR L is low.) EVEN PARITY CONTROL H is normally low, as will be described in Paragraph 5.8.

5.6 ERROR FLIP-FLOP AND GATING

Before discussing this logic in detail, a review of MD DIR L and its ramifications in the machine cycle is necessary. MD DIR L is a signal that indicates the source of information on the MD lines. At the beginning of every memory cycle MD DIR L is low, causing the contents of the currently active memory's Sense Register to be placed on the MD lines. At TP2, MD DIR L may or may not change. It will not change during an F or non-autoindexed D cycle. It will change on all other cycles unless grounded by an option other than the CPU (for example, during a BREAK cycle with data direction from memory to peripheral). In any event, if MD DIR L remains low after TP2, no modification of memory is possible and the PDP-8/E may well be performing a "fast" 1.2-μs cycle. If MD DIR L goes high after TP2, the PDP-8/E is definitely performing a "slow" 1.4-μs cycle and is most likely modifying memory.

In a fast cycle, the MD lines have just about changed state by the leading edge of TP2, and there is insufficient time for the Parity Generator to settle. During such cycles, the parity decision must be deferred to the trailing edge of TP2 in order to gain 100 ns more time for the Parity Generator to settle. Since MD DIR L cannot change, there is no danger that the information on the MD lines will change.

In a slow cycle, the MD lines have set up 200 ns before TP2. The parity decision must be made at the leading edge of TP2, since MD DIR L may well change and place new information (the contents of CPU's MB Register) on the MD lines.

The ERROR flip-flop and its gating are shown in Figure 5-5. Assume that the ERROR flip-flop is cleared, and that the odd parity is received from the parity generator logic. At the leading edge of TP2, the SLOW flip-flop is clocked. At the trailing edge of TP2, the FAST flip-flop is clocked. Since no parity error has occurred, both flip-flops remain cleared.

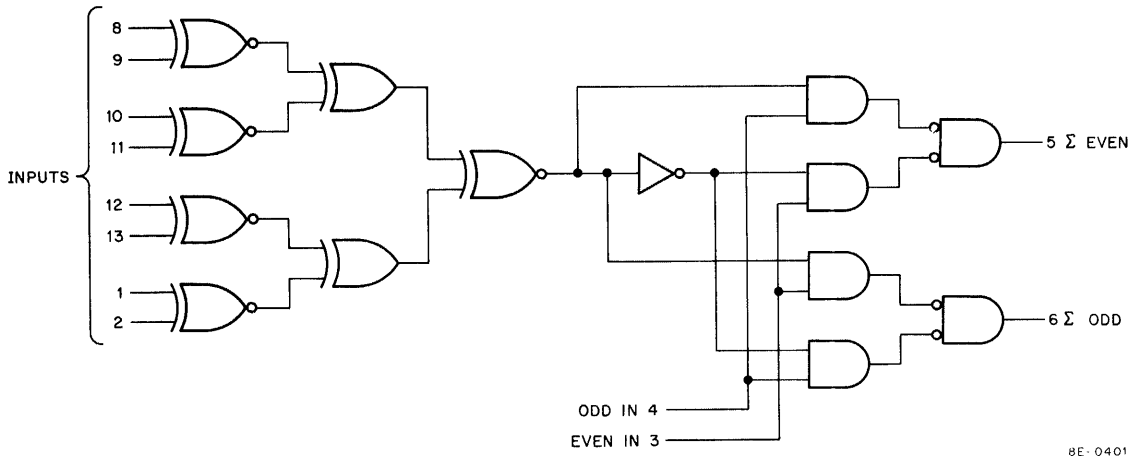

Figure 5-3 74180 8-Bit Parity IC

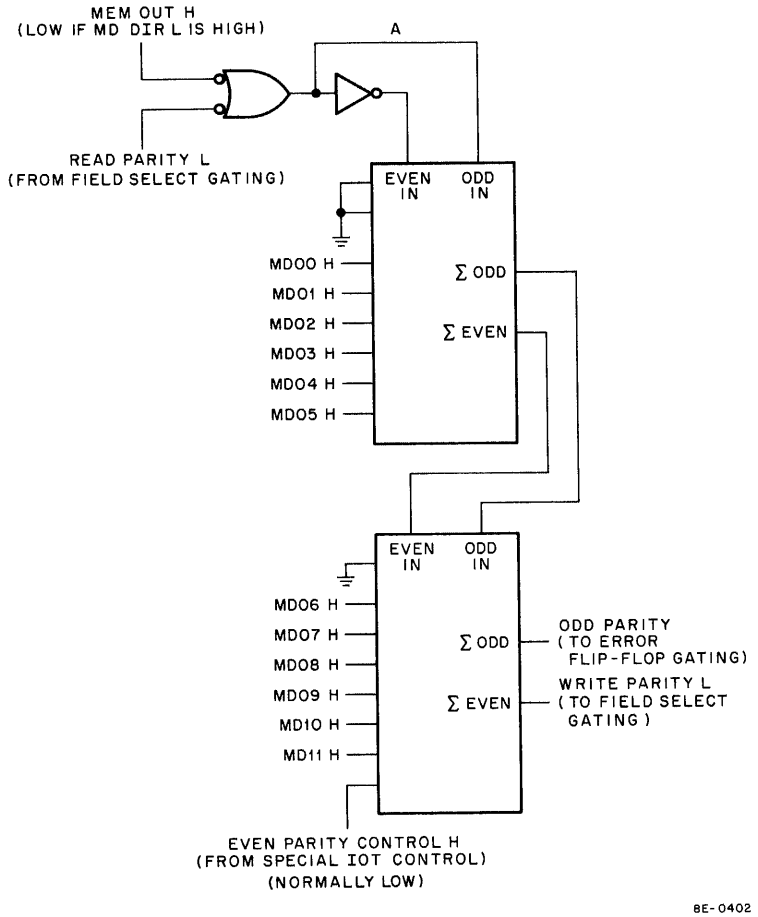

Figure 5-4 Parity Generator

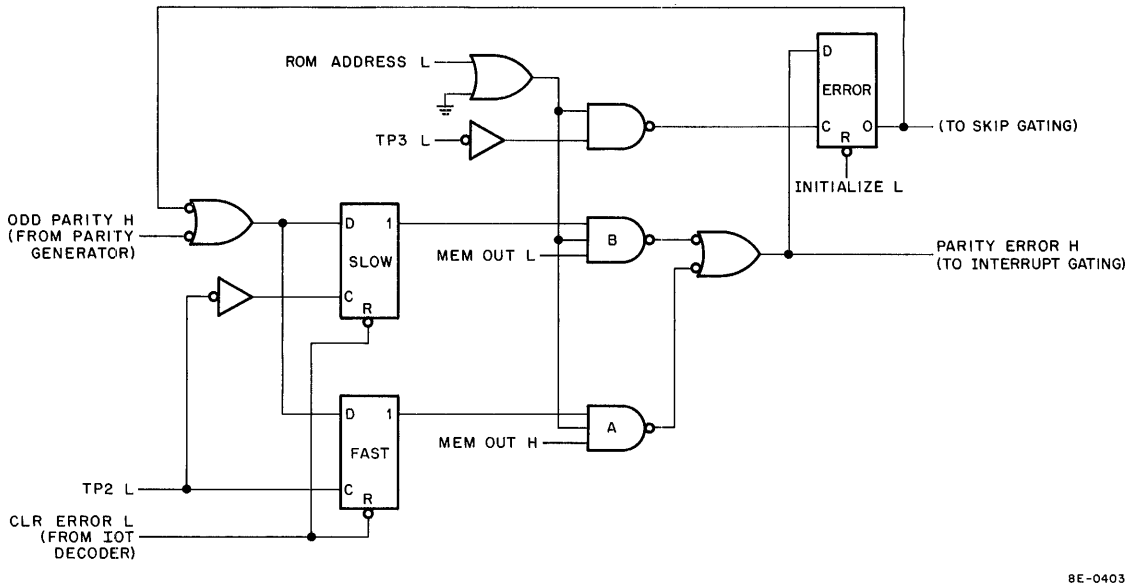

Figure 5-5 ERROR Flip-Flop and Gating

Now assume that the ODD PARITY H line becomes low during a fast cycle. MEM OUT L is low and MEM OUT H is high, since these lines are controlled by MD DIR L. The ODD PARITY H line, therefore, is low at the trailing edge of TP2, when the FAST flip-flop is clocked. Gate A is enabled, presenting a high signal to the D input of the ERROR flip-flop, and simultaneously requesting an interrupt. The SLOW flip-flop may have been set at the leading edge of TP2, but gate B is disabled because MEM OUT L is low.

Last, assume that the ODD PARITY H line becomes low during a slow cycle. At the leading edge of TP2, the SLOW flip-flop is clocked and set. MD DIR L goes high, the result of a flip-flop in the CPU's timing generator being clocked by TP2. Therefore, MEM OUT H goes low, disabling gate A; MEM OUT L goes high, enabling gate B. The MD lines change, the Parity Generator starts to respond, and the FAST flip-flop is clocked at the trailing edge of TP2. The state of the FAST flip-flop is ignored because gate A is now disabled.

Regardless of the type of cycle, the D input of the ERROR flip-flop is high well before TP3, allowing an interrupt request to be generated during the current memory cycle (if the interrupt system is enabled). At the trailing edge of TP3, the ERROR flip-flop is clocked, setting the ERROR flip-flop. During all succeeding memory cycles, the D inputs to both the FAST and SLOW flip-flops are high, maintaining the error condition. The three flip-flops remain set until CLR ERROR L is generated in the IOT decoder logic (discussed in Paragraph 5.7). CLR ERROR L clears FAST and SLOW at the leading edge of TP3. At the trailing edge of TP3, ERROR (its D input is now low) is clocked and thus cleared.

If ROM ADDRESS L is low, gates A and B are both disabled and PARITY ERROR H, therefore, is low. No interrupt request is made. Also, the clock input to the ERROR flip-flop is disabled so that any previously detected error will not be lost.

5.7 IOT DECODING AND SKIP, INTERRUPT GATING

A summary of the IOTs for the MP8-E is given in Table 5-1. The logic is shown in Figure 5-6. The device code is decoded by a 314 gate in a manner similar to any OMNIBUS decoding scheme. As in any internal device, the

device must ground INTERNAL I/O L when it sees its device code to inhibit operation of the KA8-E. Decoding of the IOT operation is done by an 8251 Binary-to-Octal Decoder.

The EPI L and DPI L signals are used to set and clear, respectively, the IRE (Interrupt Enable) flip-flop. The CMP L and the SMP, CMP L signals are ORed together, gated with TP3, and the result used to clear both the FAST and SLOW flip-flops in the ERROR flip-flop and gating logic. As was explained in Paragraph 5.6, the ERROR flip-flop is then cleared at the trailing edge of TP3. The SMP L and the SMP, CMP L signal is ORed together and the result ANDed with ERROR (1) to drive the SKIP L line of the OMNIBUS. The SKIP L line is also grounded any time the SPO L line is grounded.

The one remaining output of the 8251, the CEP L line, is used to enable the special IOT control described in the following paragraph.

NOTE

This IOT decoding scheme is somewhat special, and should not be used as an example of general I/O decoding design.

Table 5-1
MP8-E IOT Summary

Octal	Mnemonic	Description
6100	DPI	Disable MP8-E interrupts.
6101	SMP	Skip if no parity error.
6102	---	Not used.
6103	EPI	Enable MP-E interrupts.
6104	CMP	Clear parity error flag.
6105	SMP, CMP	Skip if no parity error, clear error flag.
6106	CEP	Check for even parity. Complement the read parity but write odd parity in the next EXECUTE cycle only. Used for diagnostic purposes. Execution to a ROM address results in no operation.
6107	SPO	Skip if MP8-E is in machine.

5.8 SPECIAL IOT CONTROL

The CEP instruction gating requires additional comment. As shown in Figure 5-7, CEP ANDed with TP3 sets the DAE flip-flop, causing one input of gate A to go low. The next time the computer's major state becomes EXECUTE, OMNIBUS signal EL goes low. Gate A is fully enabled, generating EVEN PARITY CONTROL H and causing the output of gate B to go low. At the leading edge of TP2, the output of gate B goes high again; DAE clears; and EVEN PARITY CONTROL H is negated.

EVEN PARITY CONTROL H drives one input of the Parity Generator, causing the MP8-E to intentionally read wrong parity to test the MP8-E logic. Since EVEN PARITY CONTROL H is negated at TP2 (before the memory starts to rewrite), odd parity is written into the parity memory.

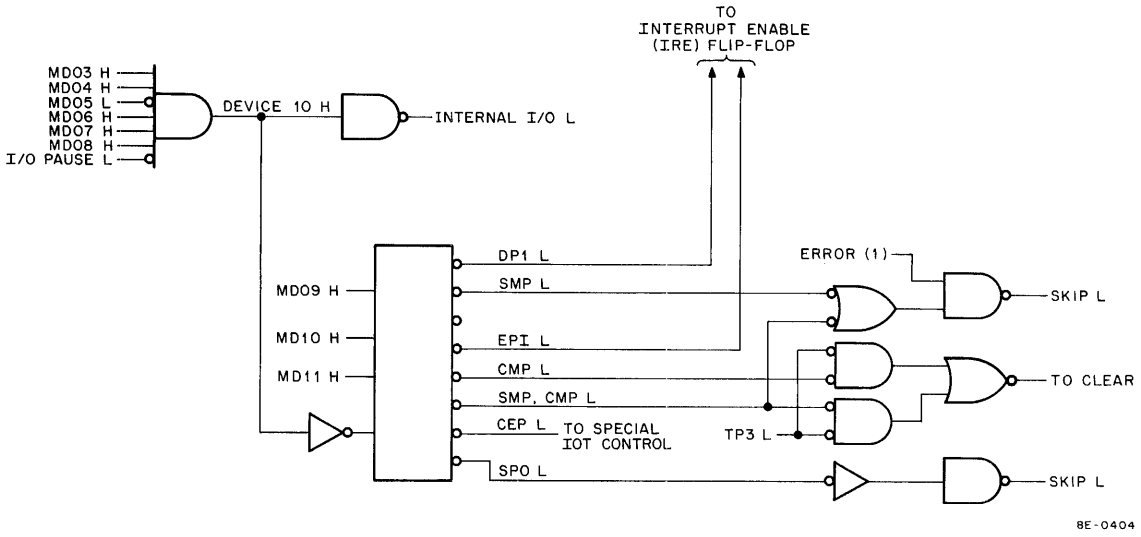

Figure 5-6 IOT Decoding and Skip, Interrupt Gating

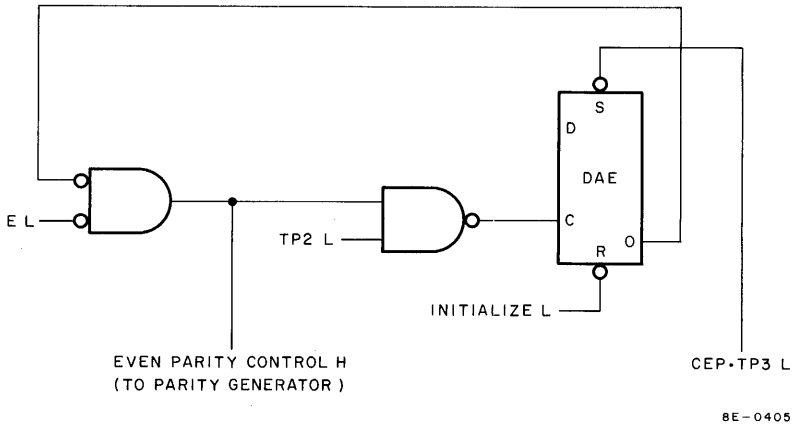

Figure 5-7 Special IOT Control

SECTION 5 MAINTENANCE

The MP8-E diagnostic program is a particularly good test of core memory stacks. If a stack operates properly in the MP8-E, it is virtually certain to operate properly in any MM8-E, unless there is a problem with one of the four bits that the MP8-E does not use. The MP8-E diagnostic should be run as a regular part of system maintenance. Diagnostic messages and the program listing should serve to pinpoint any commonly encountered malfunctions.

The same procedures as described under memory troubleshooting in Paragraph 4.7, Volume 1 are applicable. Note that the standard memory checkerboard programs are insufficient tests of the MP8-E, since a checkerboard pattern of all 1s and all 0s is used. The odd parity of all 0s is 1. Likewise, the odd parity of all 1s is 1. The strobe adjustment procedure for the MP8-E is the same as for the MM8-E, with the exception of the checkerboard program used.

SECTION 6 SPARE PARTS

Table 5-2 lists recommended spare parts for the MP8-E. These spare parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 5-2
Recommended MP8-E Spare Parts

DEC Part No.	Description	Quantity
12-10043	Rotary Switch	1
16-09651	Transformer 8010	2
16-09996	Transformer 6501	1
16-09478	Transformer 1775	2
16-10031-0	Delay Line, 100 ns	1
13-10032	Resistor, 16.9 ohm, 6W, 1%	1
13-02858	Resistor, 100 ohm, 1/8W, 1%	2
13-02956	Resistor, 196 ohm, 1/8W, 1%	1
13-04858	Resistor, 348 ohm, 1/8W, 1%	1
13-02953	Resistor, 750 ohm, 1/8W, 1%	1
13-03114	Resistor, 1K ohm, 1/8W, 1%	1
13-02871	Resistor, 1.21K ohm, 1/8W, 1%	1
13-04833	Resistor, 1.96K ohm, 1/8W, 1%	1
13-04856	Resistor, 4.64K ohm, 1/8W, 1%	1
13-04885	Resistor, 9.09K ohm, 1/8W, 1%	1
13-02941	Resistor, 14.7K ohm, 1/8W, 1%	1
13-03156	Resistor, 34.8K ohm, 1/8W, 1%	1
13-05128	Resistor, 56.2K ohm, 1/8W, 1%	1
13-05252	Resistor, 68.1K ohm, 1/8W, 1%	1
13-10071	Thermistor, 1K, 1%	1
11-05275	Diode D672	7
11-00114	Diode D664	10
11-09991	Zener Diode 1/4M6, 8AZ1	1
19-10010	Diode Pack DEC 2501	2

(continued on next page)

Table 5-2 (Cont)
Recommended MP8-E Spare Parts

DEC Part No.	Description	Quantity
15-02155	Transistor DEC 1008	1
15-01881	Transistor DEC 2219	1
15-03100	Transistor DEC 3009B	1
15-10062	Transistor DEC 3734	2
15-09649	Transistor DEC 3762	1
15-10015	Transistor DEC 4008	2
15-05312	Transistor DEC 4258	1
15-03409-01	Transistor DEC 6534B	2
19-05575	IC DEC 7400	1
19-05590	IC DEC 7401	1
19-09004	IC DEC 7402	1
19-09686	IC DEC 7404	1
19-05580	IC DEC 7450	1
19-05547	IC DEC 7474	1
19-10724	IC DEC 74180	1
19-09056	IC DEC 74H00	1
19-09057	IC DEC 74H10	1
19-09267	IC DEC 74H11	1
19-05586	IC DEC 74H40	1
19-09967	IC DEC 74H74	1
19-09704	IC DEC 314	1
19-09485	IC DEC 380	1
19-09486	IC DEC 384	1
19-09594	IC DEC 8251	1
19-09705	IC DEC 8881	1