CHAPTER 1
LC8-E DECWRITER CONTROL

SECTION 1 INTRODUCTION

The LC8-E DECwriter Control interfaces the parallel version of the LA30 DECwriter (LA30P) to the PDP-8/E. The Control consists of a single M8329 quad module that plugs into the OMNIBUS and connects to the DECwriter with a signal cable that is supplied with the module.

The LA30 DECwriter is discussed here only to the extent necessary to both fully describe LC8-E Control operation and present supplementary information concerning installation and checkout. Details concerning the installation, operation, troubleshooting, and maintenance of the LA30, itself, can be found in the *LA30 DECwriter Maintenance Manual,* DEC-00-LA30-DA. Other publications and documents relevant to the LC8-E are:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* — DEC, 1972
b. *PDP-8/E Maintenance Manual, Volume 1*
c. LA30 DECwriter Diagnostic, MAINDEC-8E-D2FA
d. DEC Engineering Drawing, DECwriter Control, E-CS-M8329-0-1.

SECTION 2 INSTALLATION

The LC8-E DECwriter Control is installed on site by DEC Field Service personnel. The customer should *not* attempt to unpack, inspect, install, checkout, or service the equipment.

Insert the LC8-E Control in the PDP-8/E OMNIBUS. See Table 2-3, Volume 1, for information concerning recommended module priorities (the LC8-E is a "non-memory" option).

Connect the LC8-E to the DECwriter with the signal cable provided. J1 of the LC8-E, a 40-pin Berg Connector, connects to module slot A02 of the LA30P logic rack.

See Chapter 2 of the *LA30 DECwriter Maintenance Manual* for additional information concerning system installation and for procedures to be followed to checkout both the Control and the DECwriter.

SECTION 3 DESCRIPTION

Figure 1-1 is a block diagram of the LC8-E Control. Pin assignments for OMNIBUS signals and connector J1 signals can be found on engineering drawing no. E-CS-M8329-0-1. Information concerning pin assignments of the interconnecting cable is given in Section 5.

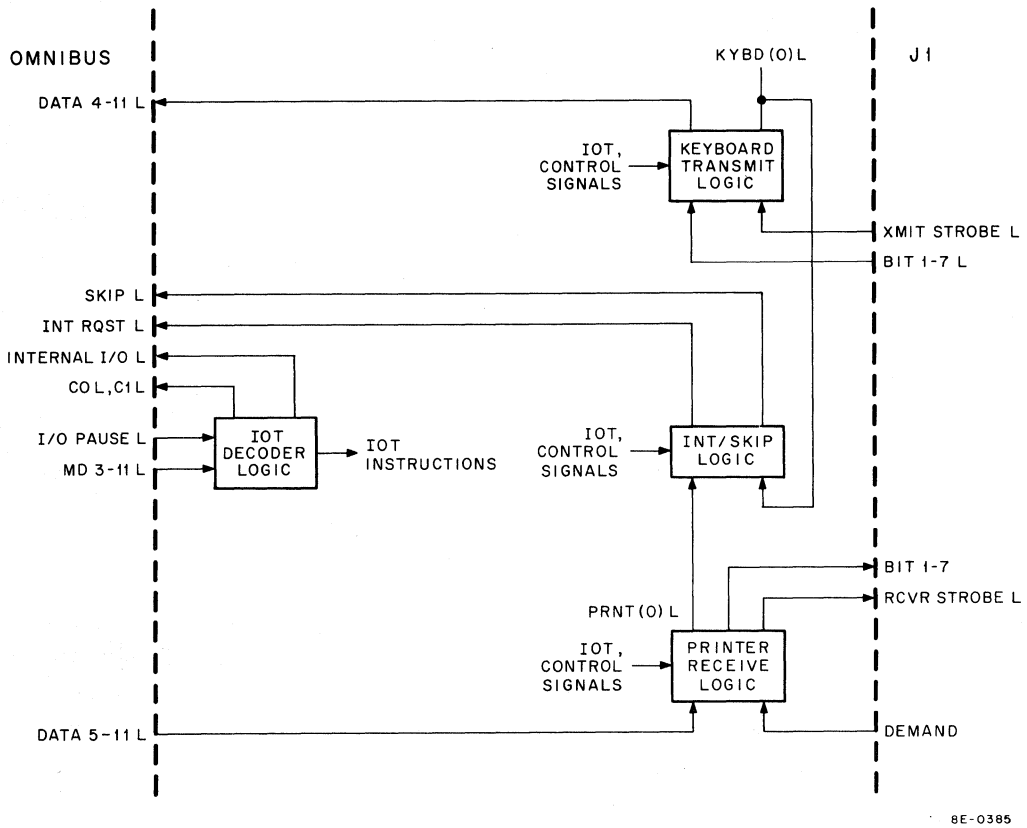

Figure 1-1 LC8-E Block Diagram

The LC8-E has two distinct functions: transfer of data from the CPU AC Register to the LA30 Printer Buffer Register and transfer of data from the LA30 Keyboard Buffer Register to the AC Register. The transfer of data to the LA30 Printer Buffer is carried out by the printer receive logic. When the LA30 is able to receive data, it asserts the DEMAND signal. This signal sets the printer flag in the printer receive logic. The resulting PRNT (0) L signal causes the INT/skip logic to assert OMNIBUS INT RQST L if the LC8-E has been logically connected to the interrupt system. Alternatively, PRNT (0) L can be tested by a program skip instruction in the INT/skip logic. In either case, the computer ultimately proceeds to a program subroutine that begins the data transfer. When this subroutine is executed, the information is transferred from the AC Register to the DATA 5–11 lines and clocked into a 7-bit register in the printer receive logic. The register outputs are available at J1 as the BIT 1–7 signals. The logic then generates a RCVR STROBE L signal that clocks the BIT 1–7 data into the Printer Buffer Register, clears the Printer flag, and causes the LA30 to negate the DEMAND signal.

The transfer of data from the LA30 Keyboard Buffer Register to the AC Register is carried out by the keyboard transmit logic. When an LA30 key is depressed, information is applied, via the BIT 1–7 lines, to a 7-bit register in the keyboard transmit logic. When the LA30 generates an XMIT STROBE L signal, the information is clocked into the 7-bit register and the KYBD (0) signal is asserted. The KYBD (0) L signal can be tested in the INT/skip logic with a skip instruction, or the interrupt system can be used to cause the program to enter an appropriate subroutine. When the subroutine is executed, the information is gated from the register in the keyboard transmit logic to lines DATA 5–11 (the logic asserts the DATA 4 L signal separately so that the input character is compatible with the modified-ASCII Teletype® code), then to the AC Register. The AC is loaded and, simultaneously, KYBD (0) L is negated.

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SECTION 4 DETAILED LOGIC

1.1 IOT DECODER LOGIC

The IOT decoder logic is shown in Figure 1-2. The LC8-E uses 12 IOT instructions, 6 for the keyboard functions and 6 for the printer functions (one of the listed printer IOTs — Skip on Printer or Keyboard Interrupt — applies to both functions). More than one LA30 DECwriter can be interfaced to the PDP-8/E at the same time. The LC8-E Control associated with each LA30 must have a unique device selection code. Therefore, the M8329 Control Module is fabricated with machine-inserted jumpers and solder terminals that allow the user to assign any two of 64 possible device selection codes to a particular LC8-E (care should be taken when assigning device selection codes to preclude multiple assignments of the same code). Figure 1-2 illustrates the octal codes and mnemonics that pertain when the LC8-E Control is manufactured. The octal codes and mnemonics are listed in Table 1-1 and the respective functions, which remain constant regardless of the code or mnemonic, are detailed.

Figure 1-2 identifies the 12 machine-inserted jumpers, W1 through W12, and 6 groups, lettered from A to F, of 4 numbered solder terminals (jumper and terminal designations are etched on the quad module for each identification). To change a control device selection code, first cut a selected "W" jumper (or jumpers); then, solder a new jumper between designated terminals associated with the "W" jumper(s). For example, the device selection code for the keyboard functions can be changed from 03 to 13 by removing W5 and connecting terminals C3 and C4; the printer functions device code can be changed from 04 to 10 by removing W6 and W8 and connecting terminals C2 and C4 and D2 and D3.

As Figure 1-2 shows, the device selection code signals, 603X and 604X, are applied to separate DEC 7442 Decoder ICs. The device operation codes represented by bits MD 9, 10, and 11 are then decoded by E9 and E6 to provide the listed IOT instruction signals. Note that the device selection code signals assert the OMNIBUS INTERNAL I/O L signal; thus, the positive I/O bus interface ignores the IOT instruction.

Three of the keyboard IOT instruction signals cause OMNIBUS "C" lines to be activated. When the KCC L signal is generated, both the C0 L and C1 L signals are asserted; the resulting transfer of 0s clears the AC Register. The KRB L signal also results in a transfer to the AC; however, this transfer involves data from the keyboard, rather than 0s. Finally, the KRS L signal causes only the C1 L signal to be asserted; the result is an inclusive-OR transfer of data to the AC.

1.2 PRINTER RECEIVE LOGIC

The printer receive logic is shown in Figure 1-3. The 7-bit register is shown only in part, the logic associated with bits DATA 10—6 being similar to that illustrated for bits 11 and 5. Significant signals are related by the timing diagram in Figure 1-4. Refer to both figures when reading the logic description.

The LA30 printer routine is initiated by the program instruction TFL, Set the Printer Flag. At TP3 time of this instruction, NAND gate E7 is enabled, causing the PRNT flip-flop to be set. This flip-flop is also set by the DEMAND signal, which is asserted by the printer each time it completes a print cycle (Figure 1-4 illustrates this signal rather than the TFL L signal). If the LC8-E is logically connected to the interrupt system, as Figure 1-4 and this discussion assume, PRNT (0) L causes the INT/skip logic to assert OMNIBUS INT RQST L. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The TSK instruction in the routine causes the program to jump to an LC8-E routine that determines if the printer or keyboard requested the interrupt (other options are open to the programmer, this is but one example). Ultimately, the LC8-E printer routine executes the TLS instruction.

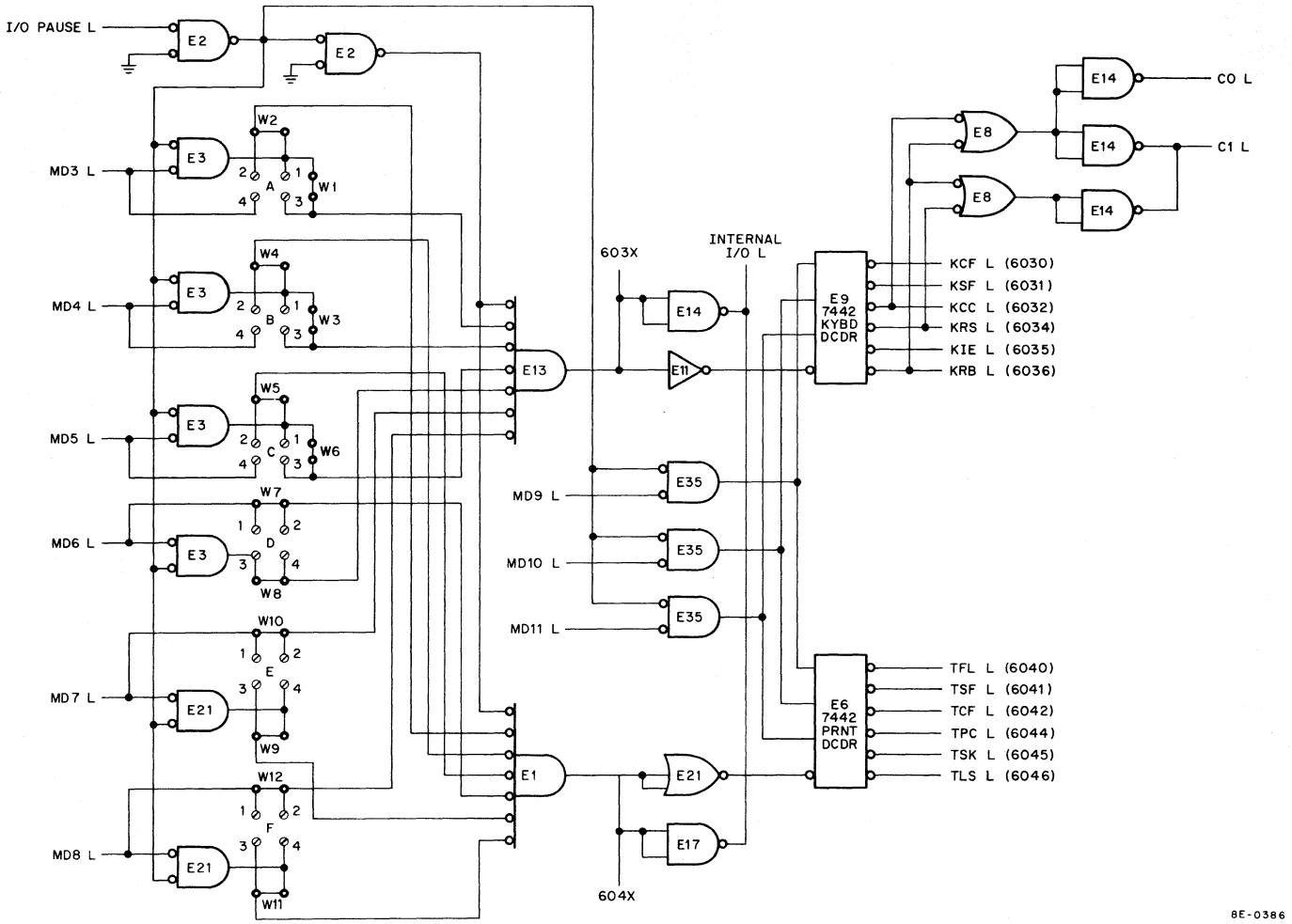

Figure 1-2 LC8-E IOT Decoder

Table 1-1
LC8-E IOT Instruction List

Octal Code	Mnemonic	Function
6030	KCF	Clear the Keyboard flag. Clears the KYBD flip-flop.
6031	KSF	Skip on the Keyboard flag. Senses the state of the KYBD flip-flop. If the flip-flop is set, increments the program counter so that the next sequential instruction is skipped.
6032	KCC	Clear the flag, clear the AC. Clears both the KYBD flip-flop and the AC Register.
6034	KRS	Read the keyboard buffer. Gates character information from the keyboard transmit logic and ORs it into AC Register bits 5 through 11. Sets AC4.
6035	KIE	Set/clear interrupt enable. Sets the INT ENA flip-flop if AC11 is logic 1; clears the flip-flop if AC11 is logic 0.
6036	KRB	Read the keyboard buffer, clear the flag, clear the AC. Gates character information from the keyboard transmit logic and jams it into AC Register bits 5 through 11. Sets AC4. Clears the KYBD flip-flop.
6040	TFL	Set the printer flag. Sets the PRNT flip-flop.
6041	TSF	Skip on the Printer flag. Senses the state of the PRNT flip-flop. If the flip-flop is set, increments the program counter so that the next sequential instruction is skipped.
6042	TCF	Clear the Printer flag. Clears the PRNT flip-flop.
6044	TPC	Load the printer buffer and print. Causes the character information to be gated to the BIT 1–7 lines. Sets the RCVR STROBE flip-flop. At TS2 of the next instruction, the information is loaded into the LA30 input buffer.
6045	TSK	Skip on a keyboard/printer interrupt request. Skips the next sequential instruction if the INT ENA flip-flop is set (the LC8-E is logically connected to the interrupt system) and if either the KYBD flip-flop or the PRNT flip-flop is set.
6046	TLS	Load the printer buffer and print. Clears the flag. The character information is gated to the BIT 1–7 lines. Sets the RCVR STROBE flip-flop. At TS2 of the next instruction, the information is loaded into the LA30 input buffer. Clears the PRNT flip-flop.

During TS2 of the TLS instruction, information is gated from the AC Register to the DATA lines and remains on the DATA lines through TS3. When TLS L is decoded in the IOT Decoder logic, it enables NOR gates E5B and E5D (Figure 1-3). The enabled output of E5D causes the information on lines DATA 5–11 to be gated to the D-inputs of the register flip-flops, while at the same time providing a high level on the D-input of E27B, the RCVR STROBE L flip-flop. At TP3 time of the instruction the register flip-flops are clocked, flip-flop E27B is set, and the PRNT flip-flop is cleared. The register data is applied, via the BIT 1–7 lines, to the printer buffer

register. During TS2 of the instruction following TLS, NAND gate E29 asserts the RCVR STROBE L signal (flip-flop E27B is cleared at TP3 time of this instruction). This signal loads the printer buffer register and negates the DEMAND signal. When the print cycle ends approximately 30 ms later, the DEMAND signal is again asserted and a new transfer is begun.

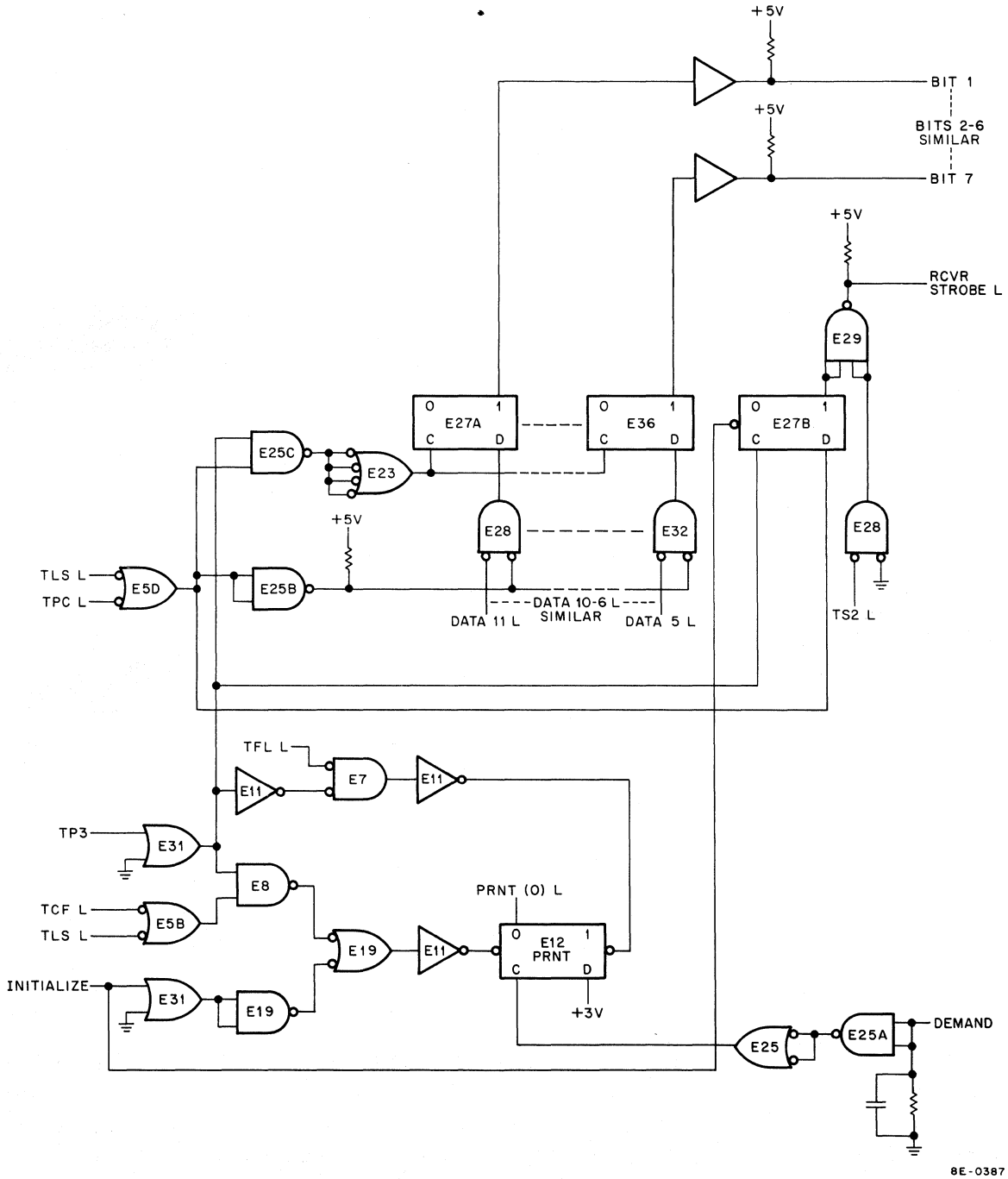

Figure 1-3 Printer Receive Logic

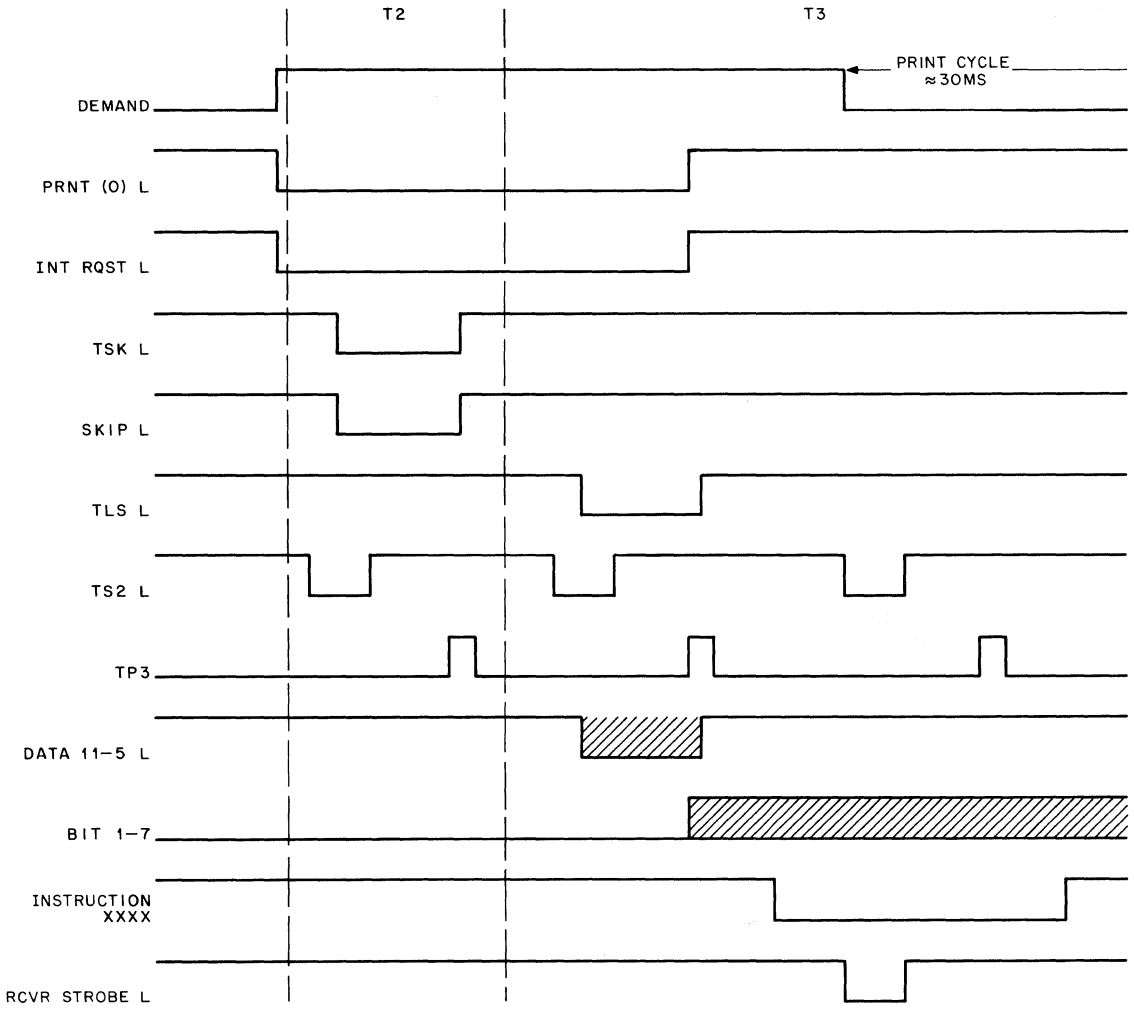

Figure 1-4 Timing, Printer Receive Logic

1.3 KEYBOARD TRANSMIT LOGIC

The keyboard transmit logic is shown in Figure 1-5. The 7-bit register is shown only in part. Significant signals are related by the timing diagram in Figure 1-6. Refer to both figures when reading the logic description.

The user initiates the keyboard sequence by depressing a key on the LA30. The character information is placed on the BIT 1–7 lines. After a period of time that allows the BIT lines to settle, the keyboard generates the XMIT STROBE L signal. This signal clocks the information into the 7-bit register and sets the KYBD flip-flop. If the LC8-E is logically connected to the interrupt system, as assumed, KYBD (0) L causes the INT/skip logic to assert the OMNIBUS INT RQST L signal. The program proceeds to an interrupt servicing routine to determine the identity of the requesting device. The TSK instruction in the routine causes the program to jump to an LC8-E routine that determines if the printer or keyboard requested the interrupt. Ultimately, the LC8-E keyboard routine executes the KRB instruction.

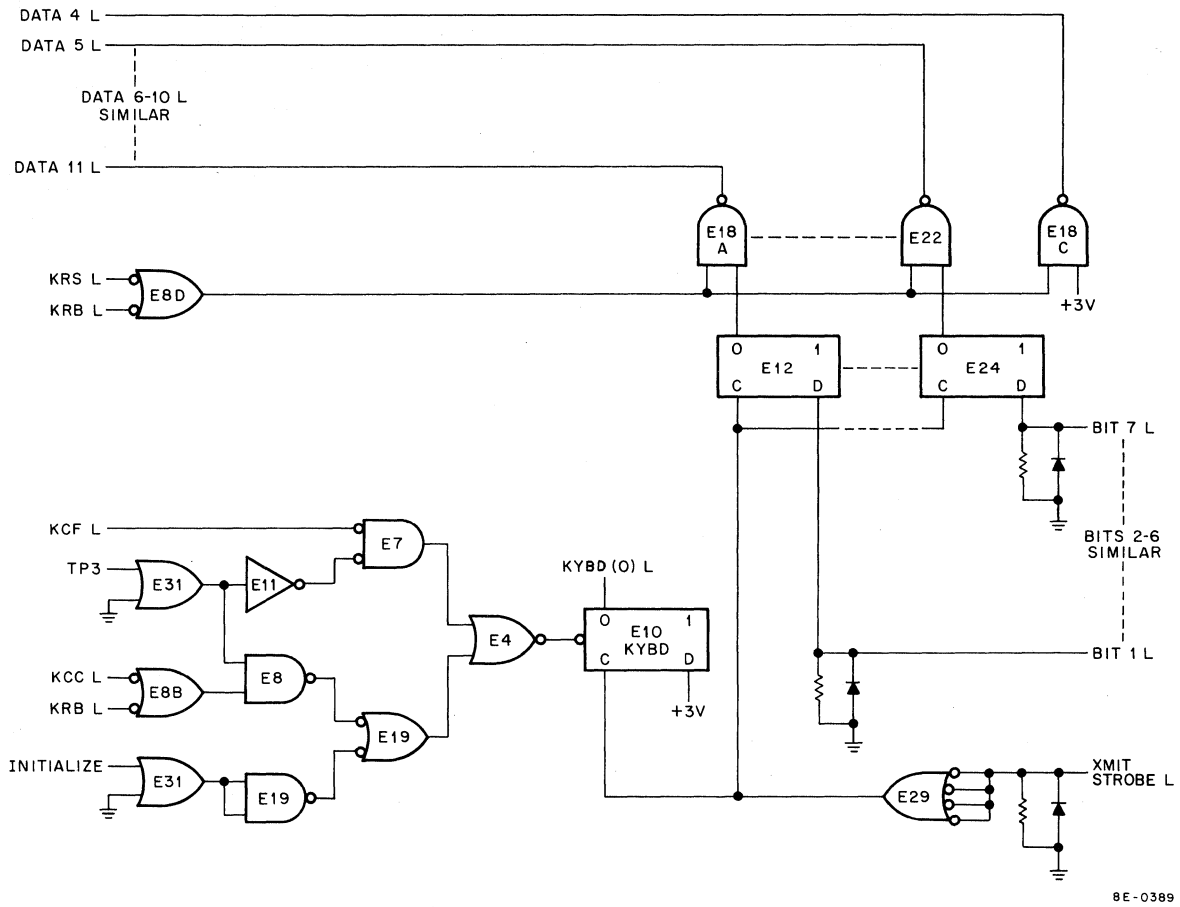

Figure 1-5 Keyboard Transmit Logic

When the KRB instruction is decoded, the IOT decoder logic generates the KRB L signal and activates the C0 and C1 lines. The KRB L signal enables NOR gate E8D; the output signal from E8D gates the information from the register outputs to DATA lines 5–11, and also causes NAND gate E18C to assert DATA 4 L. The DATA lines are gated to the AC Register and the information is clocked into the register at TP3 time. Also at TP3, the KYBD flip-flop is cleared, readying the logic for a new data transfer.

1.4 INT/SKIP LOGIC

The INT/skip logic is shown in Figure 1-7. The PRNT (0) L signal and the KYBD (0) L signal can cause program skips when tested by instructions TSF and KSF, respectively. The signals can also be tested by the TSK instruction, provided the INT ENA flip-flop, E10, has been set, logically connecting the LC8-E to the interrupt system. When E10 is set, the TSK L signal enables NAND gate E4D, which, in turn, enables AND-NOR gate E15 if either the PRNT (0) L signal or the KYBD (0) L signal is asserted. Simultaneously, NAND gate E17 asserts the INT RQST L signal.

The INT ENA flip-flop is set by the OMNIBUS INITIALIZE signal for the PDP-8 Family program compatibility. To clear the flip-flop, removing the LC8-E from the interrupt system, load AC11 with logic 0 and then program the KIE instruction. The logic 0 in AC11 keeps the DATA 11 L signal negated. Thus, the D-input of E10 remains high. At TP3 time, NAND gate E7 provides a clock pulse for E10, clearing the flip-flop. E10 can be set at any time with the same instruction merely by loading AC11 with logic 1.

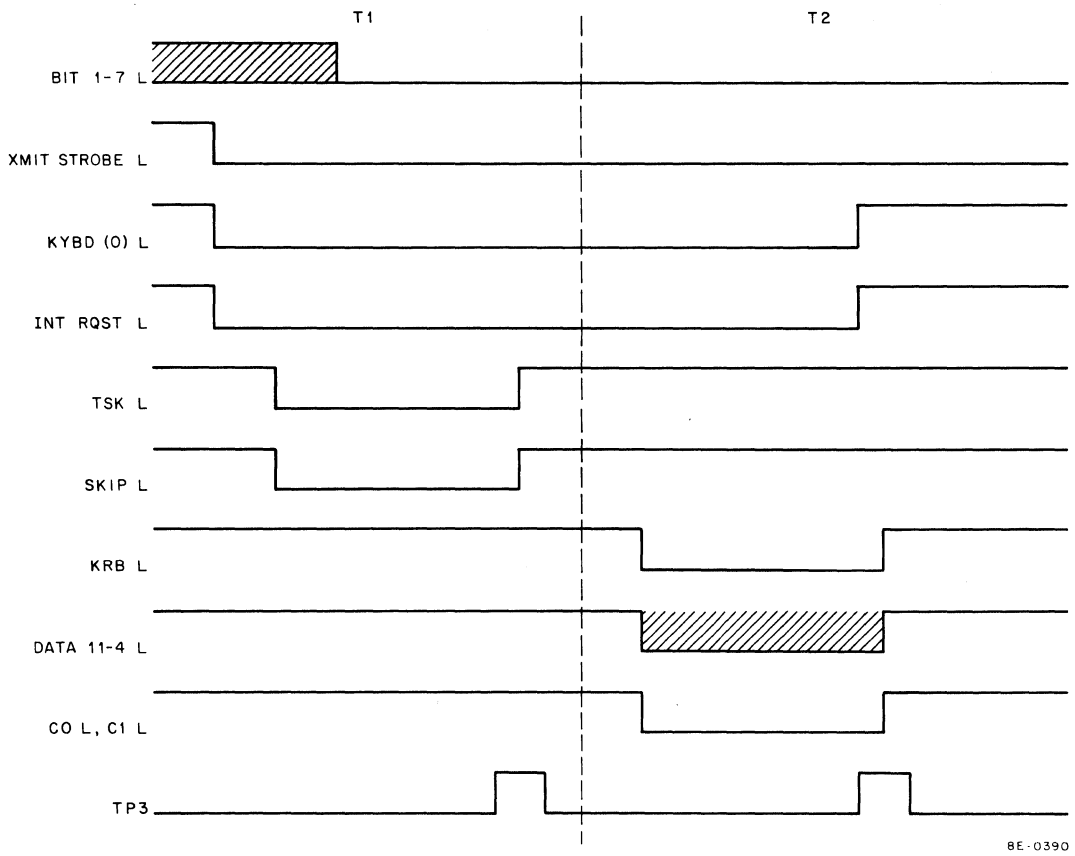

Figure 1-6 Timing, Keyboard Transmit Logic

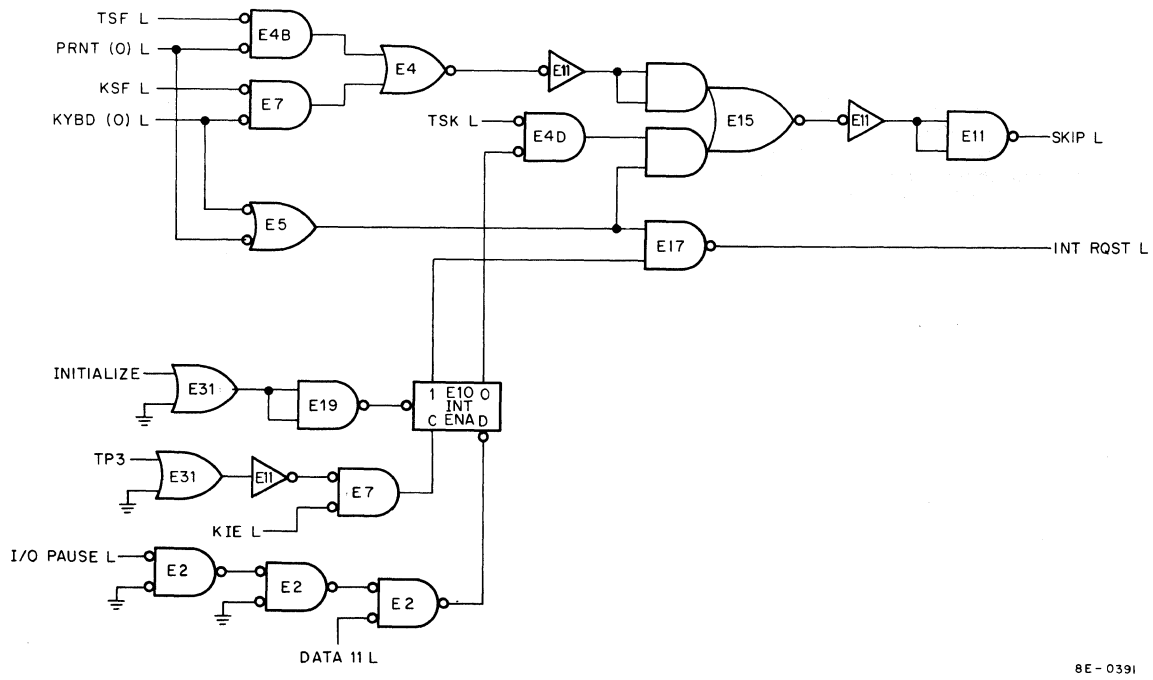

Figure 1-7 INT/Skip Logic

SECTION 5 MAINTENANCE

Refer to Volume 1 and to the *LA30 DECwriter Maintenance Manual* for maintenance information that pertains to both the LC8-E Control and the LA30 DECwriter. The LA30 DECwriter Diagnostic, MAINDEC-8E-D2FA, should be run when an error is suspected.

SECTION 6 SPARE PARTS

Table 1-2 lists recommended spare parts for the LC8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 1-2
LC8-E Recommended Spare Parts

DEC Part No.	Description	Quantity
19-10394	IC DEC 5384	1
19-10392	IC DEC 5380	1
19-10391	IC DEC 5314	1
19-10046	IC DEC 7442	1
19-9929	IC DEC 7417	1
19-9973	IC DEC 97401	1
19-9686	IC DEC 7404	1
19-9056	IC DEC 74H00	1
19-9004	IC DEC 7402	1
19-5580	IC DEC 7450	1
19-5579	IC DEC 7440	1
19-5575	IC DEC 7400	1
19-5547	IC DEC 7474	1
10-1610	Capacitor, 0.01 μF, 100V, 20% Disk	1
10-0067	Capacitor, 6.8 μF, 35V, 20% Tant	1
10-0024	Capacitor, 47 pF, 100V, 5% DM	1
70-8417	Signal Cable	1