CHAPTER 2
KM8-E MEMORY EXTENSION AND TIME-SHARE

SECTION 1 INTRODUCTION

The KM8-E Memory Extension and Time-Share option generates a 3-bit address for the extended memory address lines. This address allows the use of more than 4K of memory and, when required, is used as a prerequisite in a time-sharing system.

All logic is contained on one M837 quad-size module that plugs directly into the OMNIBUS.

All signals enter and leave the module via the OMNIBUS.

2.1 MEMORY EXTENSION DESCRIPTION

Memory extension hardware is required when more than 4K of memory is to be addressed. Except for data break devices, the KM8-E Memory Extension is the only means by which extended memory addresses can be applied to the three extended memory address lines called EMA 0-2. Memory is divided into 4K fields, starting with field 0, for the basic 4K memory, up to field 7, when 32K of memory is employed. Each 4K of memory receives and decodes the EMA signals. This provides the addressing capability of up to 32,768 memory locations.

There are two types of fields: the Instruction Field, which acts as an extension to the PC and direct argument addresses; and the Data Field, which augments the address of indirectly obtained arguments. When the programmer desires to use one field for instructions and a different field for data, he directs the corresponding field address to either the Instruction Field Register or the Data Field Register contained on the KM8-E. The field addresses are applied to the EMA lines by specific instructions and conditional logic. Safeguards are provided so that during unplanned events, such as interrupts and data breaks, no field addresses are lost. Program instructions allow any field address to be stored; this is particularly important to the programmer desiring to nest interrupts.

A simplified block diagram showing the basic transfer paths dealing with memory addressing and field addressing is shown in Figure 2-1. The KM8-E is the only route by which fields above field 0 may be selected. The only exception is the data break device that has the capability of selecting its own memory field. The programmer has two methods of selecting memory fields. One method is via the Console Switch Register; the second method is via an IOT instruction. In either event, field information is loaded into the appropriate register in the extension control. The extension control automatically responds to the appropriate instructions and major states by placing the contents of the correct field register onto the EMA lines.

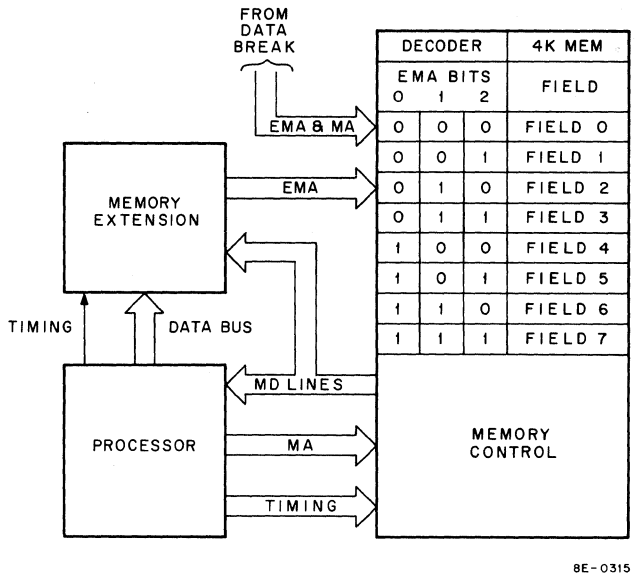

Figure 2-1 Memory Extension, Simplified Block Diagram

2.2 TIME-SHARE DESCRIPTION

The time-share portion of the KM8-E is used only when a time-sharing system is to be employed. The KM8-E Module contains a jumper in the inhibit logic that prevents the operation of the time-share function. Unless this jumper is to be removed from the module, the reader need not be concerned with the time-share description in this chapter.

The KM8-E Memory Extension and Time-Share option provides the necessary additional hardware for a general-purpose time-share system. This option, coupled with a time-sharing program, such as TSE, and 12K to 32K of core, allows a maximum of 16 users to independently run programs. This creates the appearance that each user has the computer to himself.

As a system, the user can be considered operating in one of three levels: a) not logged-in level, b) monitor level, and c) user level. A typical system is illustrated in Figure 2-2. The user interface to the system is the KL8-E Teleprinter Control. The monitor program performs a dominant role in controlling operation between the processor and the KM8-E option and between the users and the processor.

The monitor is a complex of subprograms to coordinate the operations of various programs and user consoles. The monitor allocates the computer's time and services to various users; it grants a slice of processing (computing) time to each job, and schedules jobs in sequential order to make the most use of the mass-storage device. The monitor also handles user requests for hardware operations (reader, punch, etc.), swaps (moves) programs between memory and mass storage, and manages the user's private files. Thus, the primary time-sharing capability is provided by the system monitor and the PDP-8/E Processor. However, certain additional hardware not provided by the PDP-8/E Processor is needed to accommodate the special requirements of time-sharing and extended addressing capability.

For more information on the monitor and user programming, refer to Chapter 10 of *Introduction to Programming.*

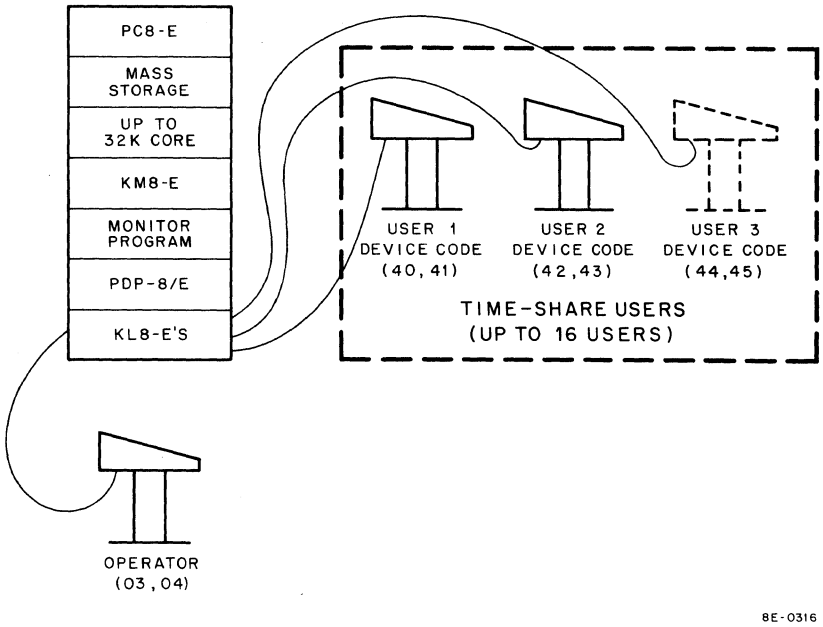

Figure 2-2 Typical Time-Share System

2.3 EXTENDED MEMORY AND TIME-SHARE SUMMARY

As a memory extension control, the KM8-E provides:

a. Hardware to allow the programmable selection of the extended memory field (fields 1 through 7), allowing the extended addressing capability of the processor from a basic system of 4096 addresses to an extended memory system of up to 32,768 addresses.

b. Hardware to prevent an interrupt or data break from interferring with the extended addressing scheme.

c. Hardware to save and restore a field return address.

As a time-share control, the KM8-E provides:

a. Hardware to distinguish between user and monitor modes.

b. Hardware to trap certain instructions, causing an interrupt and placing the time-share system in monitor mode.

c. Ability to establish user mode.

2.4 SOFTWARE

The following programs are used in time-sharing and memory extension operations:

a. System Programs

1. TSE Time-Sharing Monitor (DEC-T8-MRFB) – TSE (Time-Sharing System for the PDP-8/E Computer) is a general-purpose, stand-alone, time-sharing system. TSE offers each of a maximum of 16 users a comprehensive library of programs for compiling, assembling, editing, loading, saving, calling, debugging, and running user programs on-line.

b. Diagnostic Programs

1. Extended Memory Address Test (MAINDEC-8E-D1FA) – This program tests all of memory (up to 32K) not occupied by the program to verify that each location can be uniquely addressed.

2. Extended Memory Checkerboard (MAINDEC-8E-D1BA) – This program is designed to provide worst-case half-select noise conditions to determine the operational status of core memory. The patterns generate worst-case noise conditions in all used fields of a PDP-8/E equipped with at least 8K of core memory.

3. Extended Memory Control and Time-Share Test (MAINDEC-8E-D1HA) – This program tests the Extended Memory Control and Time-Share option logic for proper operation. The program exercises and tests the control IOT's, time-share instruction trapping, and the ability to address all fields, program interrupt, and auto-index.

2.5 COMPANION DOCUMENTS

The following documents and publications are necessary for the operation, installation, and maintenance of this option:

a. *PDP-8/E & PDP-8/M Small Computer Handbook* – DEC, 1972
b. *PDP-8/E Maintenance Manual – Volume 1*
c. *Introduction to Programming* – DEC, 1972
d. DEC engineering drawing, Memory Extension and Time-Share Option, number E-CS-M737-0-1
e. Extended Memory Address Test, MAINDEC-8E-D1FA-D
f. Extended Memory Control and Time-Share Test, MAINDEC-8E-D1HA-D

SECTION 2 INSTALLATION

The KM8-E Memory Extension and Time-Share option is installed on-site by DEC Field Service personnel. The customer should **not** attempt to unpack, inspect, install, checkout, or service the equipment.

2.6 INSTALLATION

Perform the following procedures to install the KM8-E option:

Step	Procedure
1	Remove the module from the shipping container.
2	Inspect the module for any apparent damage.
3	Connect the module to a convenient OMNIBUS slot.

2.7 CHECKOUT

Perform the following procedure to checkout the KM8-E option:

Step	Procedure
1	Verify that the extended memory modules have been installed.
2	Verify that the corresponding jumpers have been installed to reflect the appropriate memory fields.

(continued on next page)

Step	Procedure
3	Perform acceptance tests provided in Volume 1, Chapter 2, Paragraph 2.3.
4	Load MAINDEC-8E-D1FA, Extended Memory Address Test. This program tests all of memory (up to 32K) not occupied by the program to verify that each location can be addressed uniquely.
5	Load MAINDEC-8E-D1BA, Extended Memory Checkerboard. This diagnostic program provides worst-case half-select noise conditions and verifies the operational status of core memory.
6	Load MAINDEC-8E-D1HA, Extended Memory Control and Time-Share Test. This program tests the Extended Memory Control and Time-Share option logic for proper operation. The program exercises and tests the control IOT's time-share instruction trapping; and, if time sharing is implemented, the ability to address all fields, program interrupt, and auto-index.
7	Make entry on user's log that the acceptance test for the KM8-E option was performed satisfactorily.

SECTION 3 PRINCIPLES OF OPERATION

2.8 INTRODUCTION

The KM8-E system description is given in terms of its functional operation. From the functional point of view, instructions that make either the memory extension or time-share portion do something must be considered, as well as the philosophy of why the events happen as they do. The system description, therefore, is a composite treatment of the hardware, represented in block diagram form, and of the flow of events, represented in flow diagram form. The events that occur in the Memory Extension and Time-Share option are considered fully; the events within the processor are considered only partially. Such areas as major register gating and how the processor functions are completely described in Volume 1.

2.9 SYSTEM DESCRIPTION

A block diagram representing all of the functional elements of the KM8-E Memory Extension and Time-Share option is given in Figure 2-3. The logic can be considered divided into three groups: the Control (located on the left portion of the illustration), the Instruction Field Registers (located in the center of the illustration), and the Data Field Registers (located in the far right of the illustration). The only interface is the OMNIBUS. All signals entering and leaving the system, therefore, are directed from and to the OMNIBUS. Data paths between the KM8-E and the processor are via the DATA BUS. Data is directed to the console status indicators via the DATA BUS during TS1 to tell the operator which instruction and data fields have been addressed. When the data field and/or the instruction field are to be stored in memory, the data path is from the DATA BUS to the AC Register. A DCA instruction is then used to store information in memory. The data paths between the processor and the KM8-E are via the DATA BUS and MD lines.

Special inhibiting features are designed into this option. For example, during a data break operation, when some peripheral such as a disk is being operated, control lines such as CPMA DIS prevent the transmission of data to the EMA lines. For the case of programmed interrupts, the logic provides the means of holding an interrupt back until a CIF or RMF instruction has been completely processed.

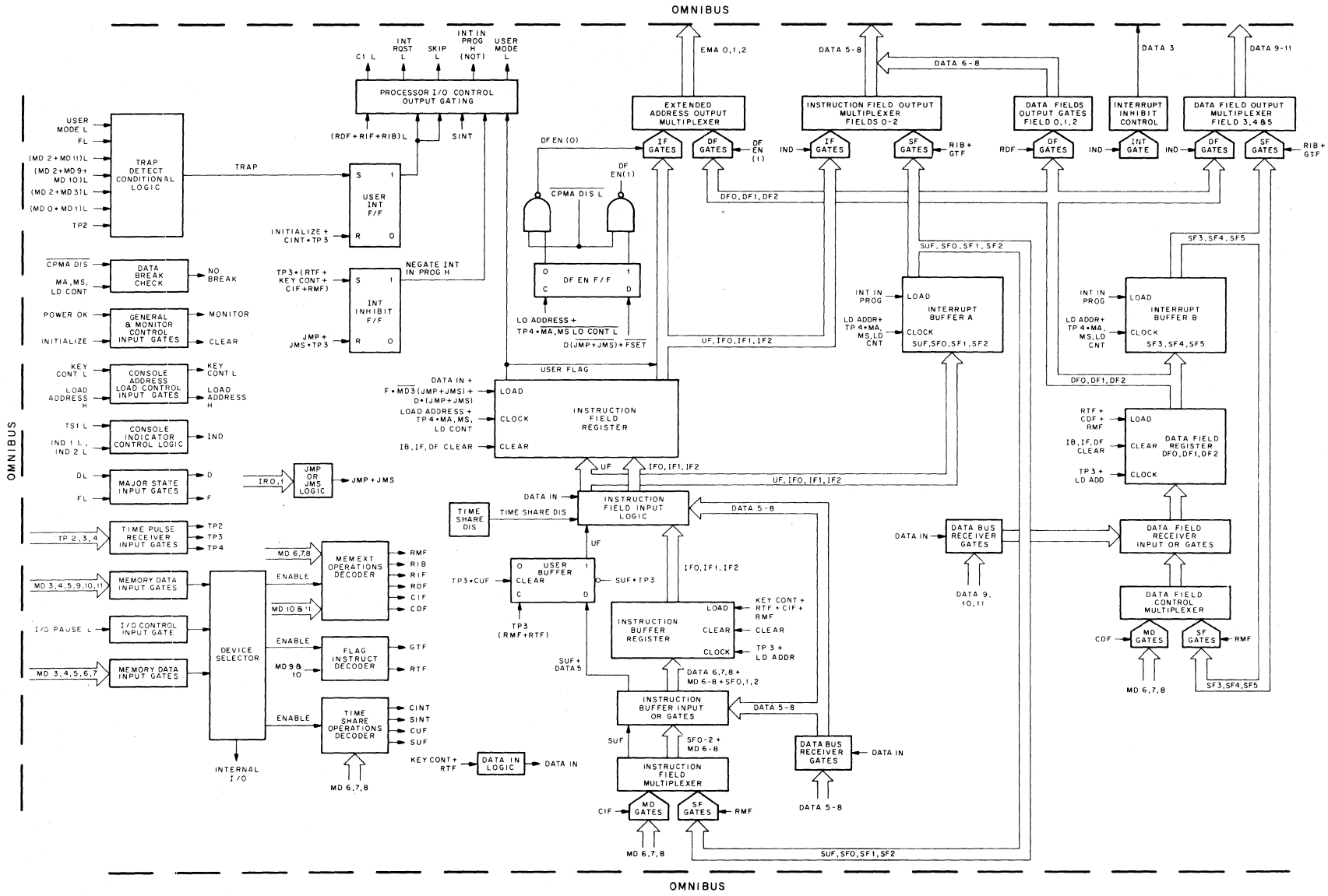

Figure 2-3 Memory Extension and Time-Share Control, System Block Diagram

Another design feature is the time-share trap logic that signals the monitor when certain instructions are used by the user.

2.9.1 Control Logic

The control logic (Figure 2-3) for the Memory Extension and Time-Share option contains elements similar to most I/O devices. These are the device selector logic, operations decoders, and the C1, INT RQST, and SKIP signal lines. Before operation begins, an IOT instruction addressed to this option is required. The INT RQST and SKIP lines are directly controlled by the USER INT flip-flop that functions to detect a TRAP signal. This flip-flop signals the monitor that a TRAP has been detected; the monitor then evaluates and takes appropriate action. The USER MODE L control signal is used in the processor to prevent the processor from responding to HLT, OSR, and IOT instructions. The INT INHIBIT flip-flop serves to ground the INT IN PROG line, thereby preventing an interrupt from occurring when instruction field changes are being processed.

For the user not desiring to use the time-share portion of the option, a simple jumper on the module prevents the User Flag (UF) flip-flop from being loaded. The instructions used with the Memory Extension and Time-Share option are listed in Table 2-1. For a detailed explanation of each instruction, refer to the KM8-E Memory option description in Chapter 7 of the *PDP-8/E & PDP-8/M Small Computer Handbook.*

Table 2-1
KM8-E Extended Memory and Time-Share Option Instructions

MEMORY EXTENSION OPERATIONS	
Data Field and Instruction Field Operations	
RMF	Restore Memory Field
RIB	Read Interrupt Buffer
Data Field Operations	
CDF	Change to Data Field
RDF	Read Data Field
Instruction Field Operations	
RIF	Read Instruction Field
CIF	Change to Instruction Field
FLAG OPERATIONS	
GTF	Get the Flags
RTF	Restore the Flags
TIME-SHARE OPERATIONS	
CINT	Clear User Interrupt
SINT	Skip on User Interrupt
CUF	Clear User Flag
SUF	Set User Flag

2.9.2 Instruction Field Register and Controls

The Instruction Field Register receives new instruction field information from any one of three sources: a) Memory Data Lines, b) DATA BUS, c) Interrupt Buffer. The main registers are the Instruction Buffer Register and the Instruction Field Register. The three output lines of the Instruction Field Register are connected, via the Extended Address Output Multiplexer, to the three EMA lines.

The control logic (Figure 2-3) associated with the Instruction Field Register governs data flow, providing the necessary gating and the primary control signals to enable gating, loading, clocking, etc. This logic selects either the Save Field, the DATA BUS, or the Memory Data lines as input and outputs this information to either the Extended Address Output Multiplexer or the DATA BUS. The flow of data is from the bottom to the top of the illustration. When the contents of the Interrupt Buffer are transferred to the Instruction Field Register, an RMF instruction gates the Save Field bits through the Instruction Field Multiplexer. When the contents of the Instruction Register were previously stored in some memory location, the CIF instruction gates bits MD 6–8 through the Instruction Field Multiplexer.

The DATA BUS Receiver Gates receive data from the AC Register or the Console Switch Register. During TS3 of the FETCH state, the contents of the AC are applied to the DATA BUS, while the KM8-E Operations Decoder is decoding the RTF instruction. The RTF instruction immediately gates bits 5–8 into the Instruction Buffer Input OR Gates. This information may have been fetched from memory during the previous memory cycle or input from the Console Switch Register.

The contents of either the MD lines or the Save Field are gated through the Instruction Field Multiplexer by instruction RMF or CIF. The Instruction Buffer Input OR Gates, in turn, apply either DATA 5–8, MD 6–8, or the Save Field to the Instruction Buffer Register and apply the UF flip-flop, obtained from the Save Field, to the User Buffer. The purpose of the Instruction Buffer is to prevent the logic from prematurely loading the Instruction Field Register.

If a CIF, RTF, or RMF instruction is issued, the actual change of field does not take place until the next JMP instruction has been completed or until the EXECUTE cycle of a JMS instruction has been entered. The new instruction field is first loaded into the Instruction Buffer and then transferred from the Instruction Buffer to the Instruction Register at TP4 so that memory is not disturbed.

Although data is available for input to the Instruction Buffer Register and the User Buffer, loading does not occur until the loading lines are asserted. To load the Instruction Buffer, signal line KEY CONTROL must be grounded or one of the three loading instructions (RTF, CIF, RMF) must be asserted (grounded) and clocked in by TP3. Manual loading of data at the Console Switch Register creates LOAD ADDRESS L for the Instruction Buffer Clock input and KEY CONTROL for the buffer loading. Bits IF 0–2, representing one of eight possible instruction fields, are on the buffer output lines when the buffer is loaded. The instruction field input logic receives IF 0–2 and the UF flip-flop. Bits IF 0–2 are then ORed with DATA 5–8 unless the operator is manually loading data into the Switch Register or an RTF instruction is executed. These conditions allow only DATA 5–8 to enter the Instruction Field Register. The UF flip-flop is inhibited if the TIME SHARE DIS signal is asserted.

Program loading of the Instruction Field Register is accomplished by a directly addressed JMP or JMS instruction at the end of FETCH, or by a JMP or JMS at the end of FETCH, or by an RTF instruction. Manual loading is accomplished by signal KEY CONTROL, which is developed when the operator loads data into the Console Switch Register. The clocking for programmed loading occurs at TP4; for manual input, clocking occurs any time LOAD ADDRESS L is asserted.

Once the Instruction Field Register is loaded, the contents are ready to be loaded into either the Extended Address Output Multiplexer or the Interrupt Buffer.

2.9.3 Interrupt Buffer A

Interrupt Buffer A functions to save the contents of the instruction field when an interrupt occurs. Signal INT IN PROG H loads the UF flip-flop and bits IF 0–2 at TP4. When the interrupt has been serviced and the memory extension is again activated, the contents of the Interrupt Buffer are input to the Instruction Field Multiplexer by an RMF instruction and the field change sequence of events will be repeated. Should the programmer wish to nest interrupts, he can store the contents of the Interrupt Buffer using the GTF instruction (or RIB instruction). The machine can be restored to its original condition using the RTF (or CIF and CDF) instruction.

2.9.4 Data Field Register And Controls

The Data Field Register and Controls function to receive a new data field from any one of three sources: a) Memory Data Lines; b) DATA BUS; c) Interrupt Buffer. The output lines of the Data Field Register are connected to the Extended Address Output Multiplexer and, when selected, address the data field by means of a combination of three bits on the EMA lines.

The simplified blocks (Figure 2-3) concerned with the Data Field Register and Data Field Register operation represent the flow of data, the necessary gating, and the primary control signals to enable gating, loading, clocking, etc. They function to select either the Save Field, DATA BUS, or memory data lines as an input and output this information to the EMA lines or the DATA BUS.

The flow of data is from the bottom to the top of the illustration. When the contents of the Interrupt Buffer are transferred to the Data Field Register, an RMF instruction gates the Save Field bits through the Data Field Control Multiplexer. When a CDF instruction is executed, bits MD 6–8 are gated through the Data Field Control Multiplexer.

The DATA BUS Receiver Gates receive data from the AC Register or the Console Switch Register. During TS3 of the FETCH state, the contents of the AC are applied to the DATA BUS while the KM8-E Flag Instruction Decoder decodes the RTF instruction. The RTF gates bits 9 through 11 into the Data Field Register.

The contents of either the MD lines or the Interrupt Buffer (RMF instruction) are gated through the Data Field Control Multiplexer. At TP3, the new data field is loaded into the Data Field Register. The manual loading operation is similar to manual loading of the Instruction Field Register.

2.9.5 Interrupt Buffer B

Interrupt Buffer B saves the contents of the data field whenever an interrupt occurs. Signal INT IN PROG H loads data field bits DF 0–2 at TP4. When the interrupt has been serviced and the memory extension is to be activated, the data field is restored to the Data Field Register by the RMF instruction.

2.9.6 Extended Memory Addressing Output Control

The three EMA 0–2 lines address any one of 8 memory fields. When any combination of these lines is grounded, the result is a selected memory field. The Extended Address Output Multiplexer with the DF EN flip-flop determines whether the EMA bits will be the data field or the instruction field (Figure 2-3). A simplified flow diagram illustrating the conditions which determine the selection is shown in Figure 2-4.

Beginning at the top of the flow diagram, the logic tests for a JMP or JMS instruction. If the JMP or JMS instruction is activated, the instruction field is addressed. Otherwise, the logic tests the DEFER state. The DF EN flip-flop is clocked by TP4 or LOAD ADDRESS if the field is applied at the console switches. If a data break is in operation, the extended address will not be applied to the EMA lines at that time. As soon as the data break ends,

the Extended Address Output Multiplexer will be enabled to gate either the instruction field or data field bits out to the EMA lines and thereby select a memory field.

The rule for data field usage is as follows: If the current instruction is an AND, TAD, ISZ, DCA or EAE instruction, and if the processor is currently in the DEFER state, the next EXECUTE cycle will use the data field. All other machine cycles that are not data break cycles use the instruction field.

Notice that the DEFER state is tested at the end of the current processor cycle. The decision whether the processor is to go to the EXECUTE state or the FETCH state is clearly indicated in Figure 3-17 of Volume 1. The same type of decisions that determine if the next state is to be EXECUTE or FETCH determine if the instruction field or data field is to be addressed.

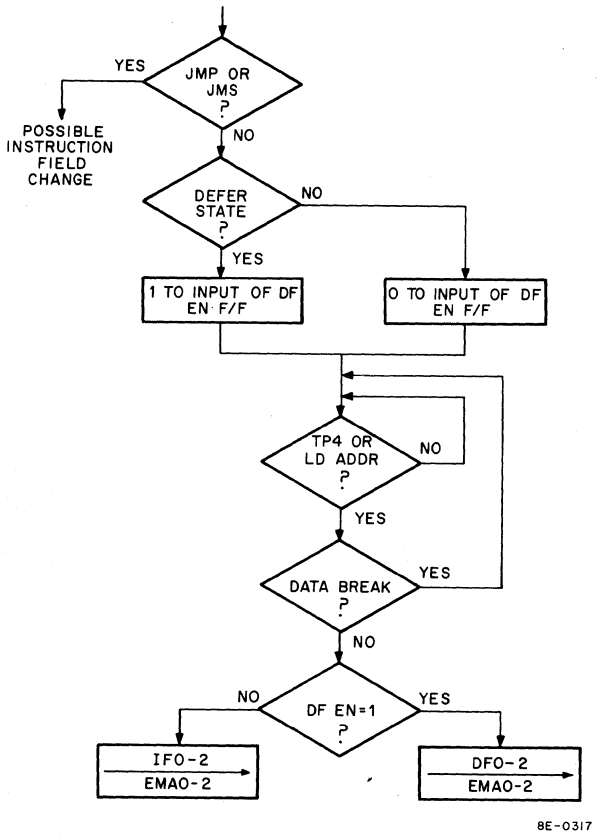

Figure 2-4 Extended Memory Addressing, Flow Diagram

2.10 OPERATING FUNCTIONS

The following paragraphs provide some examples of KM8-E operation. These descriptions reflect the flow of events for illustrative purposes and do not reflect the method by which this option is to be programmed.

2.10.1 Status Operation

Occasionally the user wants to select the STATUS position on the Console Selector Switch. When he does this, IND L will be generated at the start of TS1 and remain until TS2. Signal IND is used in the memory extension

and time-share logic to gate the contents of the IF and DF Registers through the output multiplexers and onto the DATA BUS. Refer to the system block diagram given in Figure 2-3 and to Figure 2-5 for the bit arrangement illustrating the status. Only bit 3 and bits 5 through 11 represent the status of the Memory Extension and Time-Share Control.

Bit 3 represents the interrupt status of the INT INHIBIT flip-flop. Signal INT INHIBIT is generated at TP3 whenever an RTF, KEY CONTROL, CIF, or RMF signal is asserted, and negated at TP3 whenever a JMP or JMS instruction occurs. This prevents any memory field from being lost during a program interrupt. Thus, whenever bit 3 of the status indicator is illuminated, indicating a program interrupt inhibiting condition, the processor has not started a JMP or JMS instruction since the last instruction field change instruction was performed. When the IF and DF Registers are loaded and INT IN PROG H is asserted, the contents of the registers are loaded into the Interrupt Buffers at TP4.

Bits 5 through 8 represent the contents of the instruction field and the flag in the IF Register; bits 9 through 11 represent the contents of the data field in the DF Register.

2.10.2 Interrupt Buffer Transfer to Memory and Restoration

A simplified explanation of how the Interrupt Buffers could be stored in memory and restored to the Instruction Field and Data Field Registers is illustrated in Figures 2-6 and 2-7. An RIB or GTF instruction creates the necessary gating signals to allow the instruction field and data field to pass through the corresponding output multiplexers and be applied to the DATA BUS. The same instruction grounds the C1 line, which causes the contents of the DATA BUS to be loaded into the AC Register. A DCA instruction transfers the contents of the AC Register to the corresponding addressed memory location. The next time the field is to be addressed, the TAD instruction returns the data to the AC Register and an RTF instruction allows the corresponding bits to be loaded into the Instruction Buffer and Data Field Registers at TP3. The addition of PC, AC, and MQ handling allows nesting of interrupts.

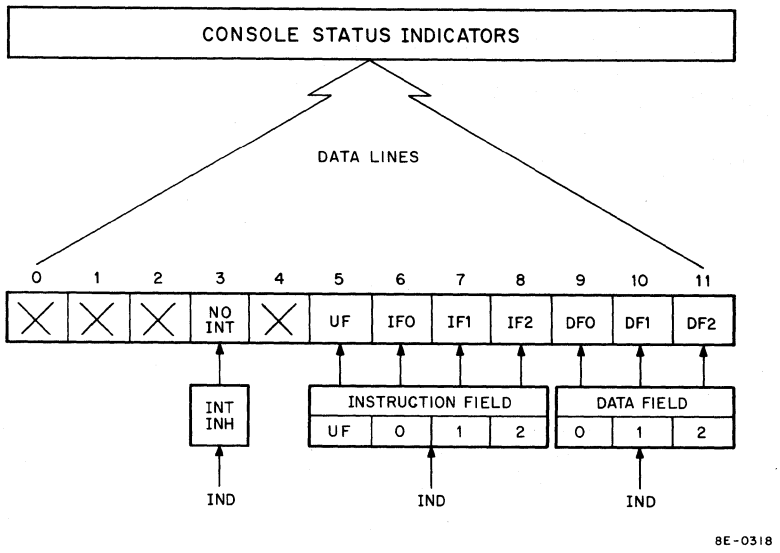

Figure 2-5 IF and DF Display Status During TS1

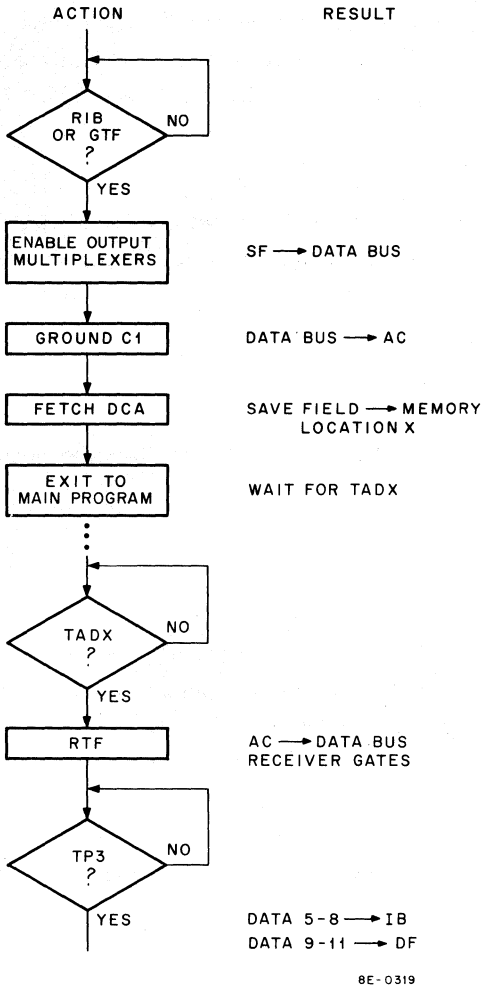

Figure 2-6 Interrupt Buffer Transfer to Memory and Restoration, Flow Diagram

2.10.3 Instruction Field Register Loading Operation

The Instruction Field Register loading operation is illustrated in the Instruction Field Register loading flow diagram (Figure 2-8). The first four decision blocks represent a go condition if any one of the blocks contain a status of yes. For example, KEY CONTROL is developed when the operator depresses the EXTD ADDR LOAD key. The corresponding clock input is LOAD ADDRESS. If the loading of the Instruction Field Register is under program control, the next three conditions are tested. An RTF instruction allows the Instruction Field Register to be loaded at TP4 of next JMP. Otherwise, the major states are tested. If the processor is in the FETCH state and not performing an RTF instruction, JMP or JMS is tested and finally MD3L is tested. When MD3H is present (indicating direct addressing), the Instruction Field Register will be loaded at TP4. Otherwise, a DEFER state with JMP or JMS is tested. Note that the Instruction Field Register is not loaded during a data break. The input is at TP4 to ensure that there is no address mixup during the current memory cycle.

2.10.4 Time-Share Operation of the System

Because much of the logic is shared between the time-share operation and the memory extension operation, it may not be obvious what logic is specifically dedicated to the time-share function.

The time-share portion operates in two modes as denoted by the UF flip-flop (refer to the system block diagram presented in Figure 2-3). When the UF flip-flop is in the logic 1 state, the system is operating in the user mode and a user program is running in the central processor. When the UF flip-flop is in the logic 0 state, the system is operating in the executive mode and the time-sharing monitor is in control of the central processor.

The four instructions developed by the Time-Share Operations Decoder are used by the monitor in the executive mode and are never executed by a user program. The trap logic is a monitoring device to assure the system that the user is programming valid instructions. When TRAP is developed, INT RQST is grounded and SKIP is enabled. The monitor then takes over and examines the invalid instruction and determines what action must be taken.

The UF flip-flop also plays an important role in monitoring for valid instructions. When the UF flip-flop is a 1, USER MODE L is developed and the grounded line, which goes to the processor, inhibits STOP and I/O PAUSE. The processor is operating in the executive mode during the time that memory extension or time-sharing instructions are being processed. The user mode begins when an SUF instruction has been completed. This sets the USER BUFFER flip-flop and inhibits the processor interrupt until the next JMP or JMS instruction. At the conclusion of either of these instructions, the UF flip-flop is transferred to the Instruction Field Register. At that time, the UF signal is applied to the processor I/O control output gating where USER MODE L is developed.

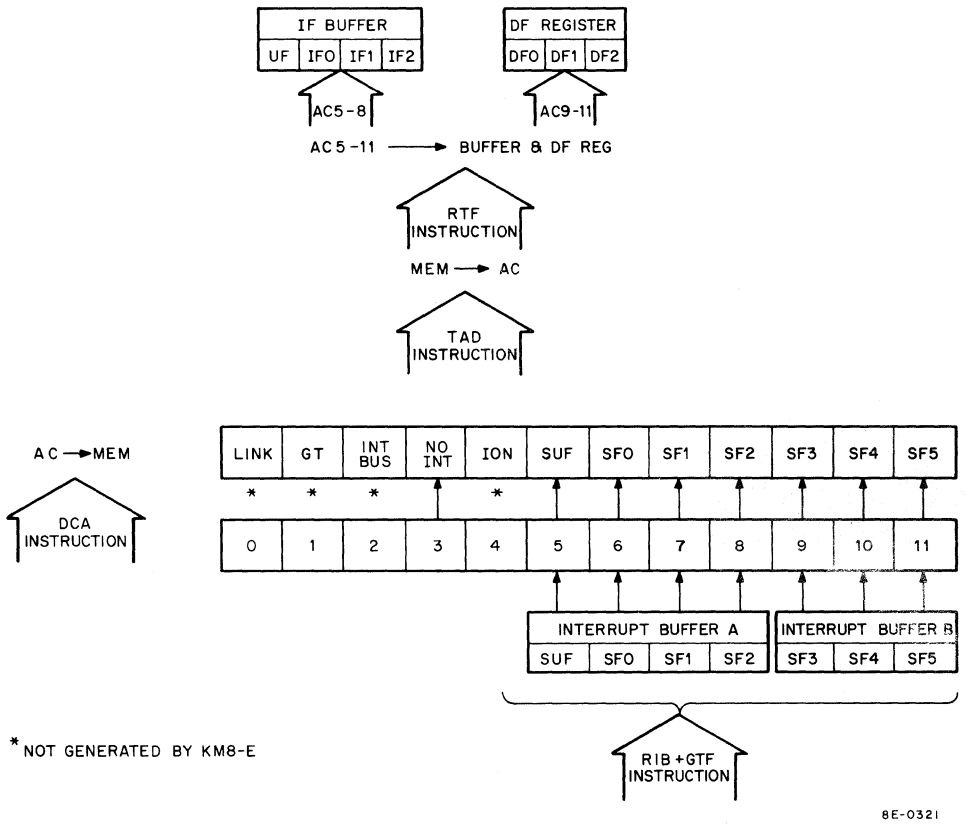

Figure 2-7 Interrupt Buffer Transfer to Memory and Restoration

The following is a summary concerning valid and trapped instructions:

FUNCTION NORMALLY:

AND
TAD
ISZ
DCA
JMP
JMS
most OPERATES

TRAPPED INSTRUCTIONS:

HLT	Monitor Return. Machine must not stop because all users would be shut down.
OSR, LAS	Requires special action. A user does not have his own Switch Register.
IOT	Requires interpretation (usually a device code change) by the monitor. For example, any user can use a KSF instruction (octal 6031). If executed by the computer, this instruction would test the flag of the console TTY (the operator). However, the monitor alters this instruction by changing the middle 6 bits to the device code of the user's TTY.

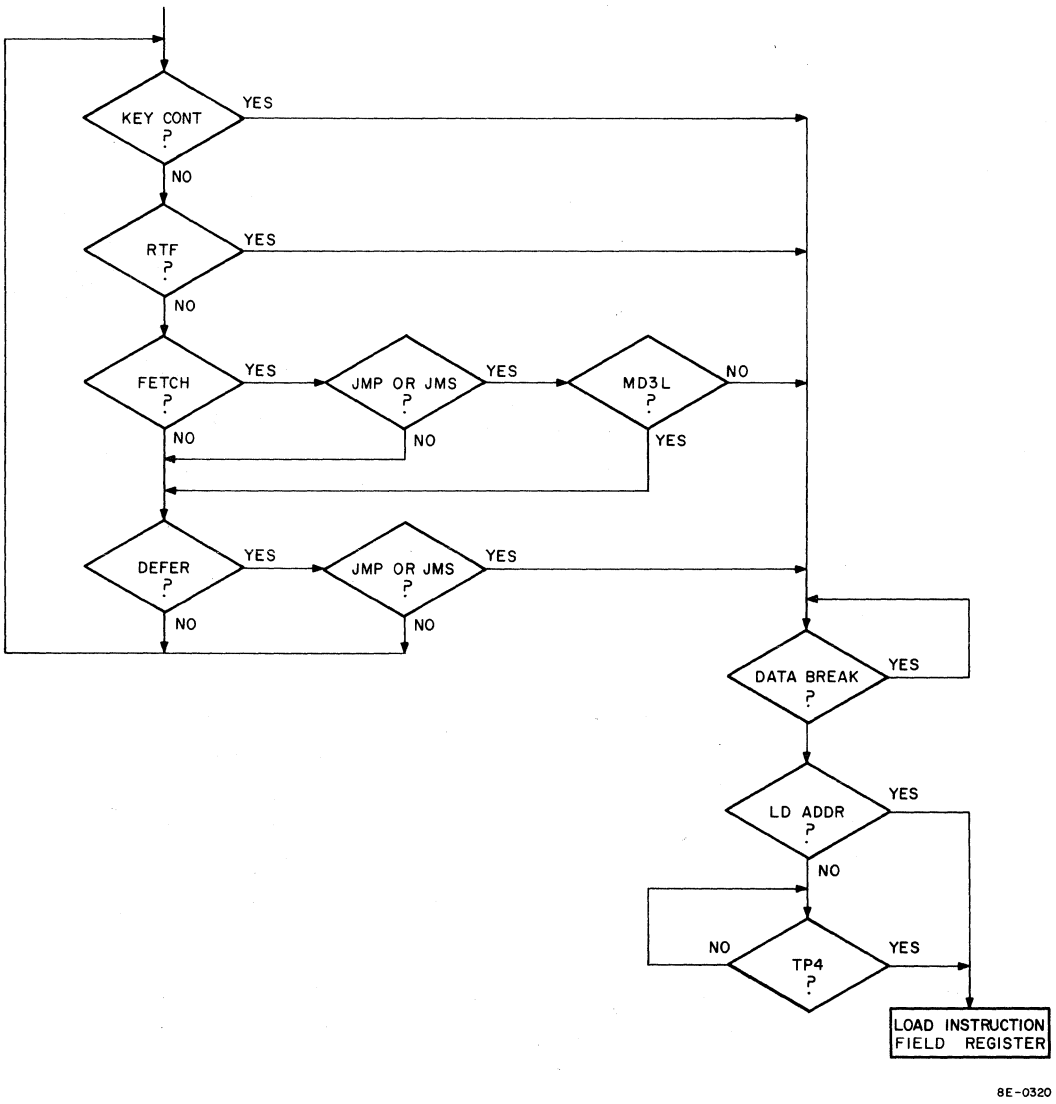

Figure 2-8 Instruction Register Loading, Flow Diagram

SECTION 4 DETAILED LOGIC

The following description represents an expansion of the Memory Extension and Time-Share Control system block diagram given in Figure 2-3.

2.11 INSTRUCTION FIELD REGISTERS

The Instruction Field Registers and gating logic are illustrated in Figure 2-9. The major parts are the Input Multiplexer, Instruction Buffer, and Instruction Field Register.

If the instruction field is to be changed, instruction CIF causes MD bits 6-8 to pass through the Input Multiplexer. If the instruction field is to be restored, instruction RMF causes the save field bits from Interrupt Buffer A to pass through the Input Multiplexer. If the data is to come from the DATA BUS, the signal DATA IN gates in bits DATA 5–8. Bit 5 holds the content of the UF flip-flop. The Instruction Buffer receives three bits. The same signals that were used to gate the bits through the Input Multiplexer are used to load the Instruction Buffer at TP3. The Instruction Field Register loads the inputs by DATA IN or during a JMP or JMS. The outputs are applied to the input gates of the Extended Address Output Multiplexer and Interrupt Buffer A.

2.12 INSTRUCTION FIELD OUTPUT MULTIPLEXER

The Instruction Field Output Multiplexer is illustrated in Figure 2-10. It consists of an 8235 IC and various control gates. Data selection lines select either the instruction field or the save field which, in turn, is applied to the DATA BUS. Signal IND L or instruction RIF selects the instruction field. Instruction GTF or RIB gates the contents of SUF and SF0 through SF2 to the DATA BUS. Bit DATA 5 is used to indicate the status of the UF flip-flop.

2.13 DATA FIELD LOGIC

The data field logic is illustrated in Figure 2-11. It consists of an 8266 IC Input Multiplexer and an 8271 IC Data Field Register. Instruction CDF is used to select bits MD 6–8; instruction RMF selects save field bits SF3 through SF5, which are to be restored from the Interrupt Buffer B. Signal DATA IN L gates in three DATA BUS bits, DATA 9–11.

The data field bits are loaded into the Data Field Register by DATA IN L or by CDF or RMF at LOAD ADDRESS time or TP3.

2.14 DATA FIELD OUTPUT MULTIPLEXER

The Data Field Output Multiplexer is illustrated in Figure 2-12. Data Field bits DF0–2 and INT INHIBIT (1) H are selected by IND L. This places these bits onto the DATA BUS during TS1 and into the Status Display on the front panel. The contents of the Interrupt Buffer can be selected by the GTF or RIB instruction.

2.15 DATA FIELD OUTPUT GATES

The Data Field Output Gates are illustrated in Figure 2-13. The contents of data field bits DF0–2 are applied to DATA 6–8 when the RDF instruction is used.

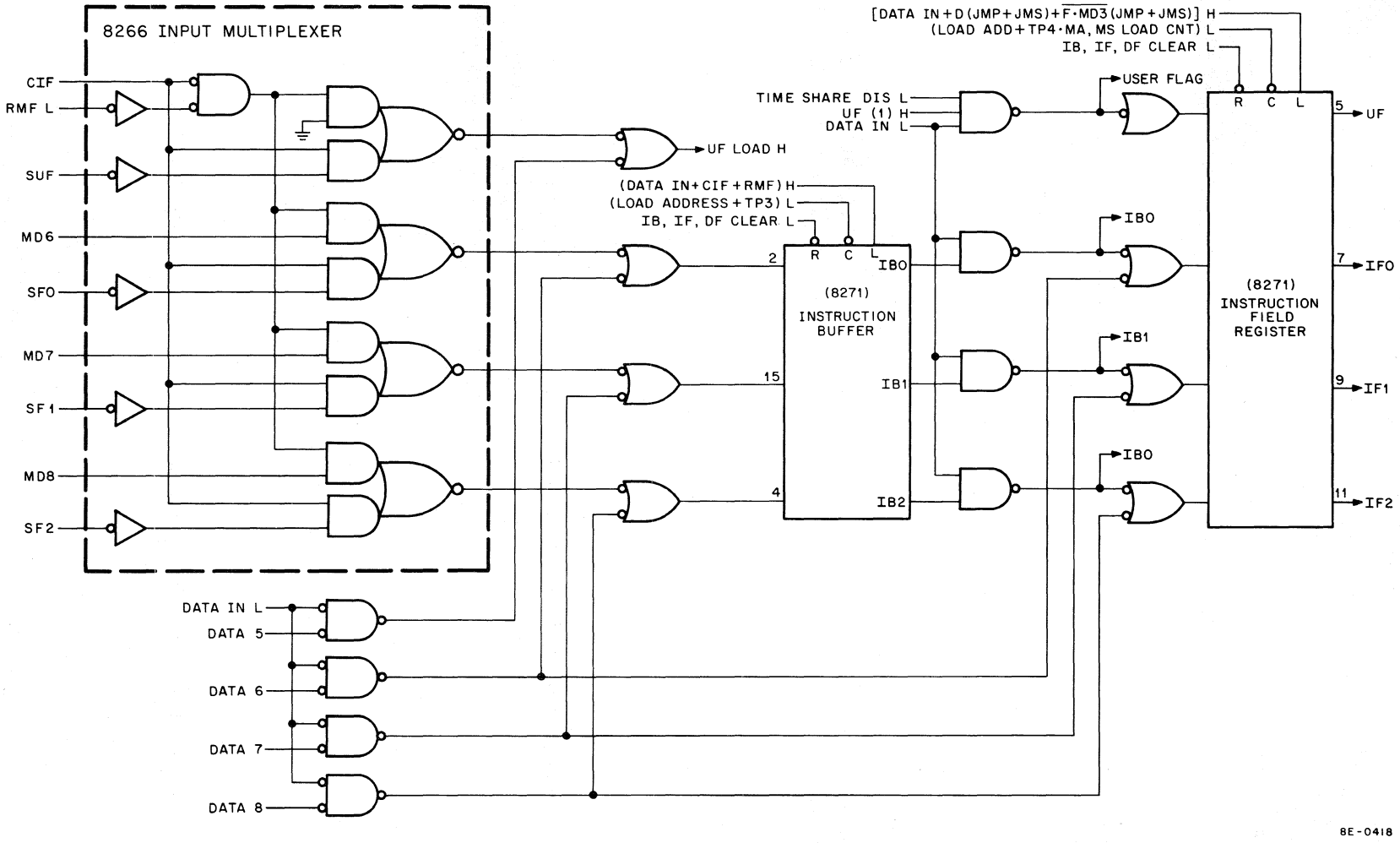

Figure 2-9 Instruction Field Registers and Gating Logic

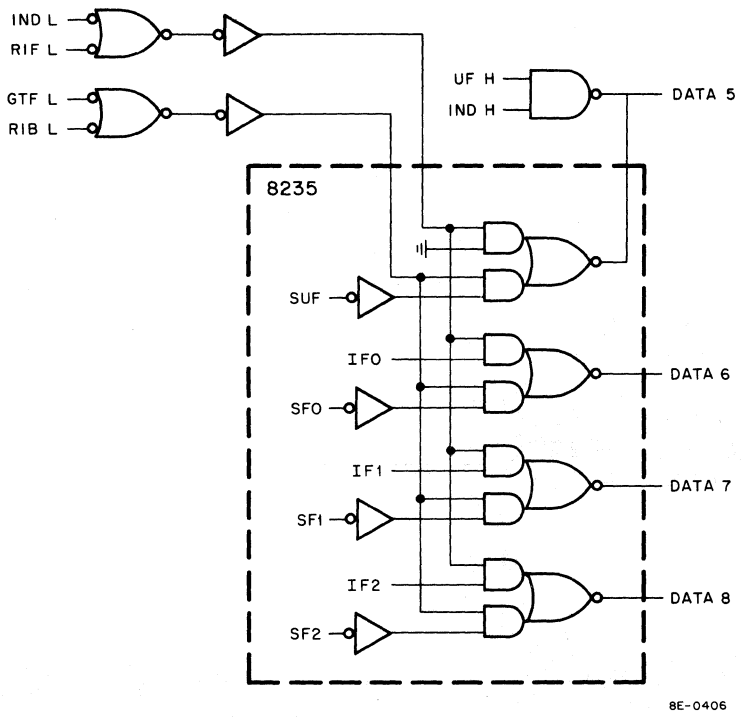

Figure 2-10 Instruction Field Output Multiplexer

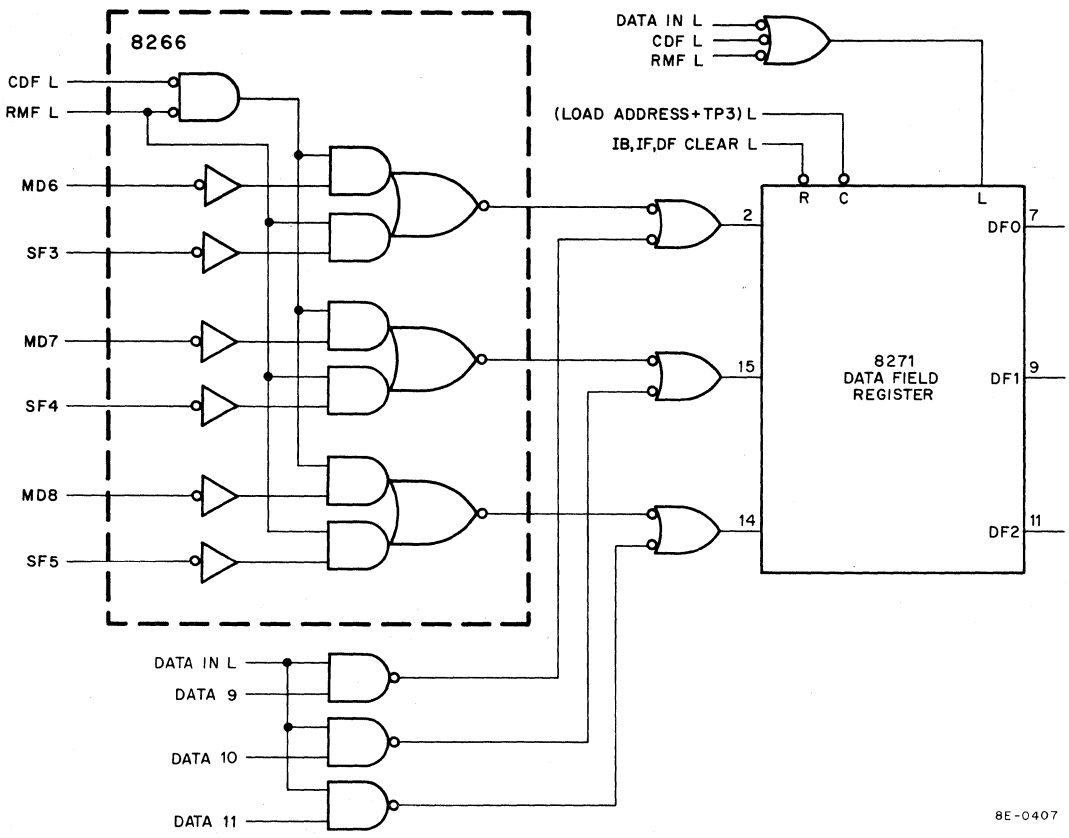

Figure 2-11 Data Field Logic

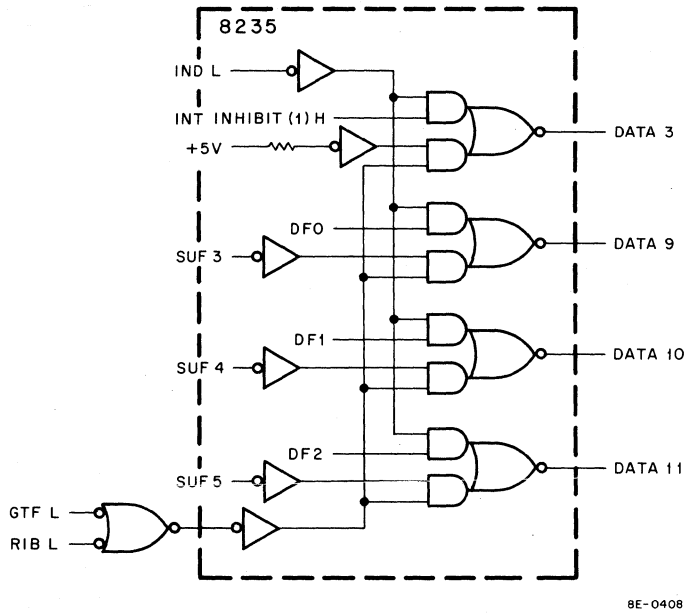

Figure 2-12 Data Field Output Multiplexer

2.16 INTERRUPT BUFFERS LOGIC

Interrupt Buffers A and B are illustrated in Figure 2-14. Buffer A is used to store the contents of the instruction field in the event of an interrupt; Buffer B is used to store the contents of the data field in the event of an interrupt. Each time an interrupt occurs, the buffers are loaded at TP4.

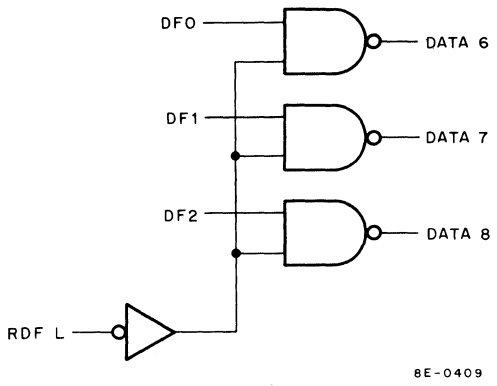

Figure 2-13 Data Field Output Gates

2.17 INTERRUPT INHIBIT LOGIC

When the processor is honoring an interrupt, INT IN PROG H is asserted. This signal is asserted at +5V, and is driven positive by a load resistor. Thus, anytime INT IN PROG H is to be negated, the signal line is simply grounded. Within the memory extension logic there is a period of time in which INT IN PROG H must not be asserted; for example, when the processor has issued a CIF instruction and has not yet encountered a JMP or JMS. These logical conditions are represented in the logic diagram illustrated in Figure 2-15. Signal INT INHIBIT (1) H is carried to DATA 3 of the DATA BUS to report to the Status Display that signal line INT IN PROG H has been negated, thereby inhibiting any interrupts if IND L is low.

2.18 INTERRUPT-BREAK DETECT LOGIC

The interrupt-break detect logic ensures that no critical operation, such as clearing of the IB, IF or DF registers or loading the Save Field Register, is accomplished while a data break is taking place. At the time an interrupt is being honored, both of these operations must take place. The two signal lines representing these activities (INT IN PROG H and MA, MS, LD CONT) are tested. Refer to Figure 2-16 for the detailed logic.

2.19 REGISTER CLEAR LOGIC

The Instruction Buffer, the Instruction Field Register, and the Data Field Register will be cleared at TP4 (Figure 2-17) if there is an interrupt and no data break is occurring, or if the machine is powered up.

2.20 DATA IN LOGIC

The data in logic develops DATA IN L to load the memory extension registers or to allow bits 5–8 of the DATA BUS to be gated into the instruction field logic and bits 9–11 of the DATA BUS to be gated into the data field logic. Signal DATA IN L is asserted by the program when an RTF instruction is decoded, or under manual control during TS1. Refer to Figure 2-18 for the logic diagram.

2.21 USER FLAG LOGIC

The User Flag (UF) is used only when the time-sharing portion of this option is implemented. The UF logic (Figure 2-19) is a D-type flip-flop that acts as a buffer in the same manner as the Instruction Buffer. Signal UF LOAD H is generated by the instruction field loading logic when DATA 5 is a 1 or SUF is asserted and clocked in by either an RMF or RTF instruction at TP3. The UF flip-flop can be set by instruction SUF and cleared by the instruction SUF and cleared by the logical conditions shown in Figure 2-19.

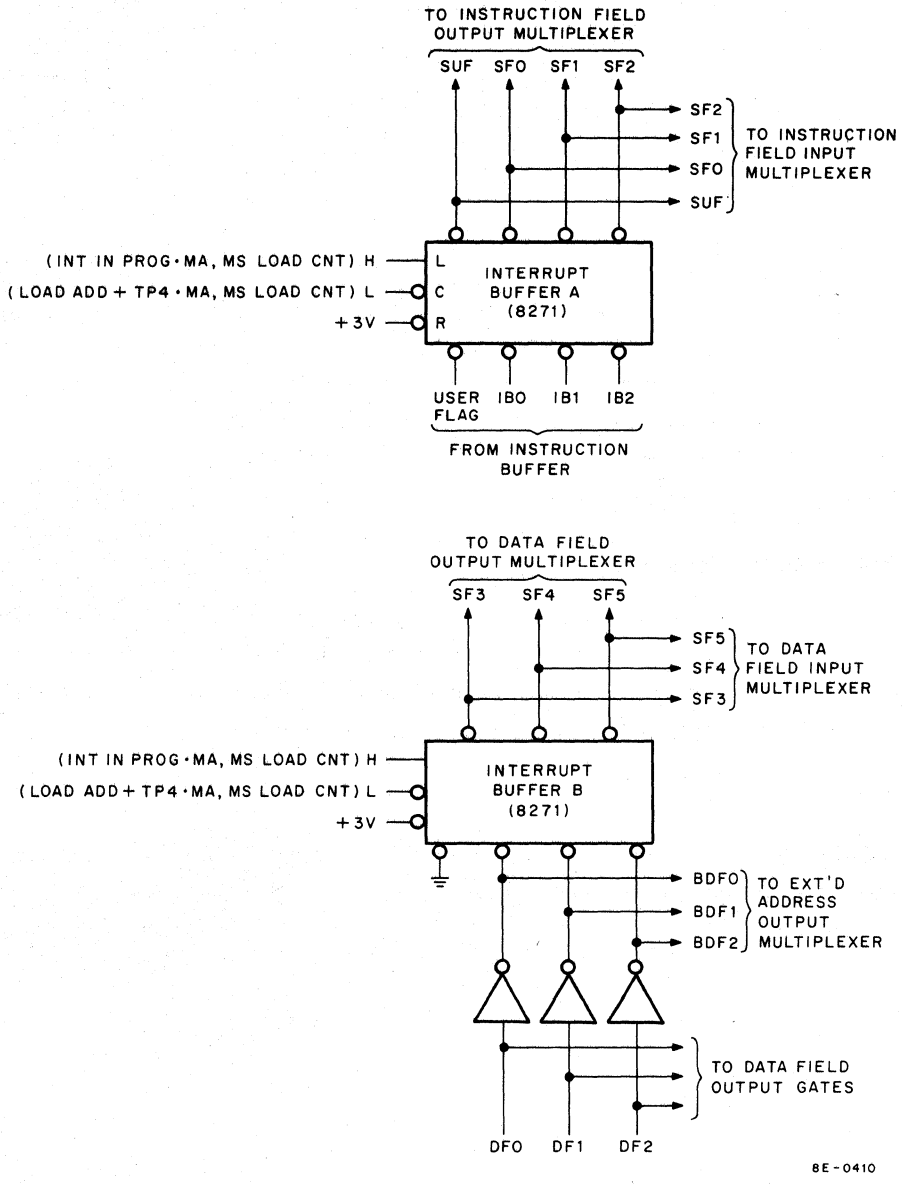

Figure 2-14 Interrupt Buffers Logic

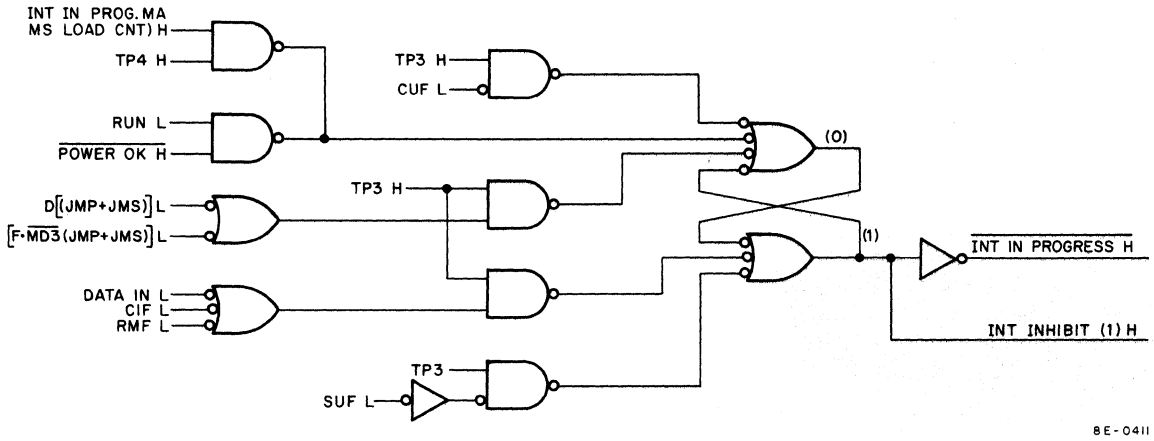

Figure 2-15 Interrupt Inhibit Logic

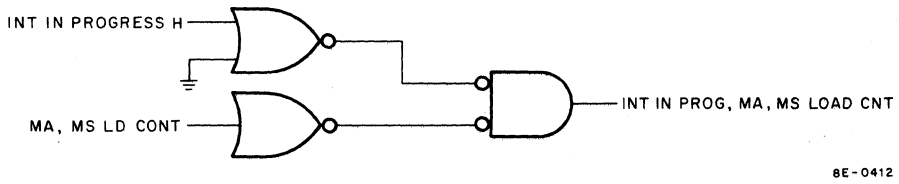

Figure 2-16 Interrupt Break Detect Logic

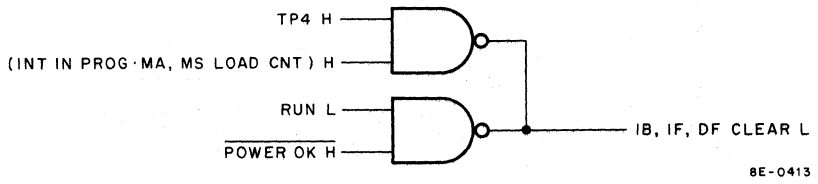

Figure 2-17 Register Clear Logic

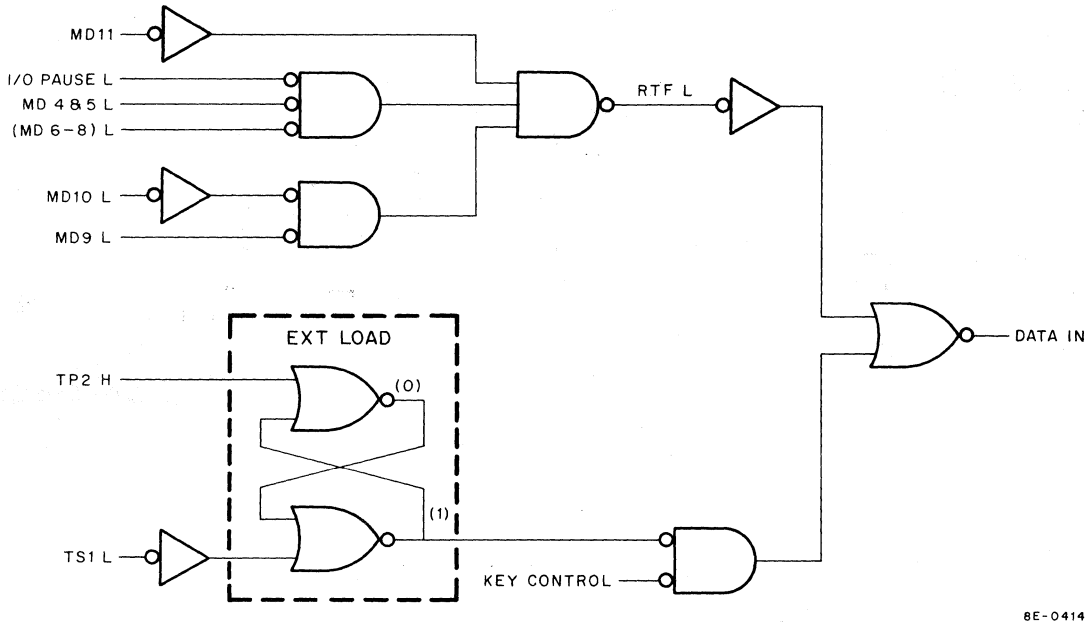

Figure 2-18 Data In Logic

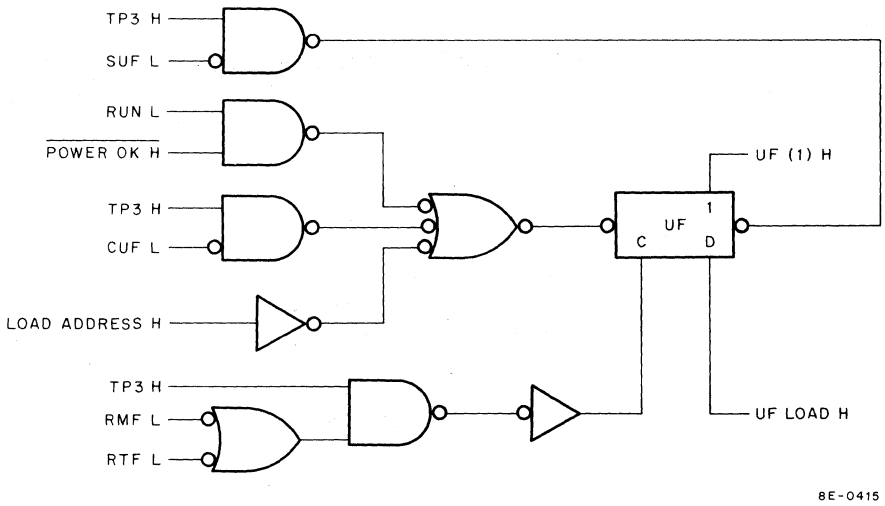

Figure 2-19 User Flag Logic

2.22 TRAP DETECT LOGIC

The trap detect logic (Figure 2-20) is used when the time-sharing portion of this option is implemented. When it is not implemented, the time-share disable circuit will contain jumpers that will hold the (0) side high and the (1) side low. Signal USER MODE L will be high because UF (1) will be low. Signal TRAP is high if the MD lines indicate an IOT (F.UM.6xxx) or special operate (F.UM.74x1, where bits 9 or 10 are 1s).

2.23 EXTENDED MEMORY ADDRESS LOGIC

The extended memory address logic (Figure 2-21) includes the output gates within the 8235 IC and the DF EN and EMA DISABLE flip-flops with corresponding control logic. The output gates, IC 8235, are a multiplexer of which the data selected for output is determined by the EMA DISABLE and DF EN flip-flops. The EMA DISABLE flip-flop serves the same function as the MAC flip-flop in the M8310 CPU Control Module, and is used to disable the output multiplexer at TP4 in the event of a data break.

The interrupt break logic signal clears the EMA DISABLE flip-flop at TP4 or when the machine is in the manual mode. The DF EN flip-flop determines if the output data is the data field or the instruction field. If the processor is not doing a JMP or JMS instruction, but is in the DEFER state, the data field will be addressed during the next machine cycle. If the processor is doing a JMP or JMS or is not in the DEFER state, the instruction field will be addressed.

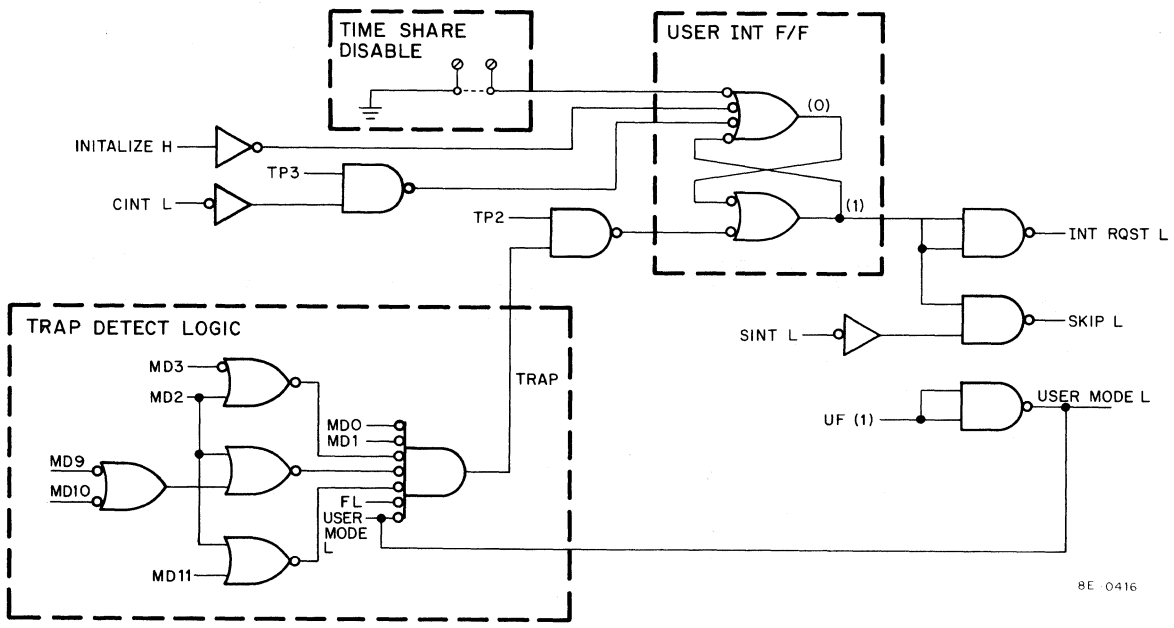

Figure 2-20 Time-Share Trap Logic

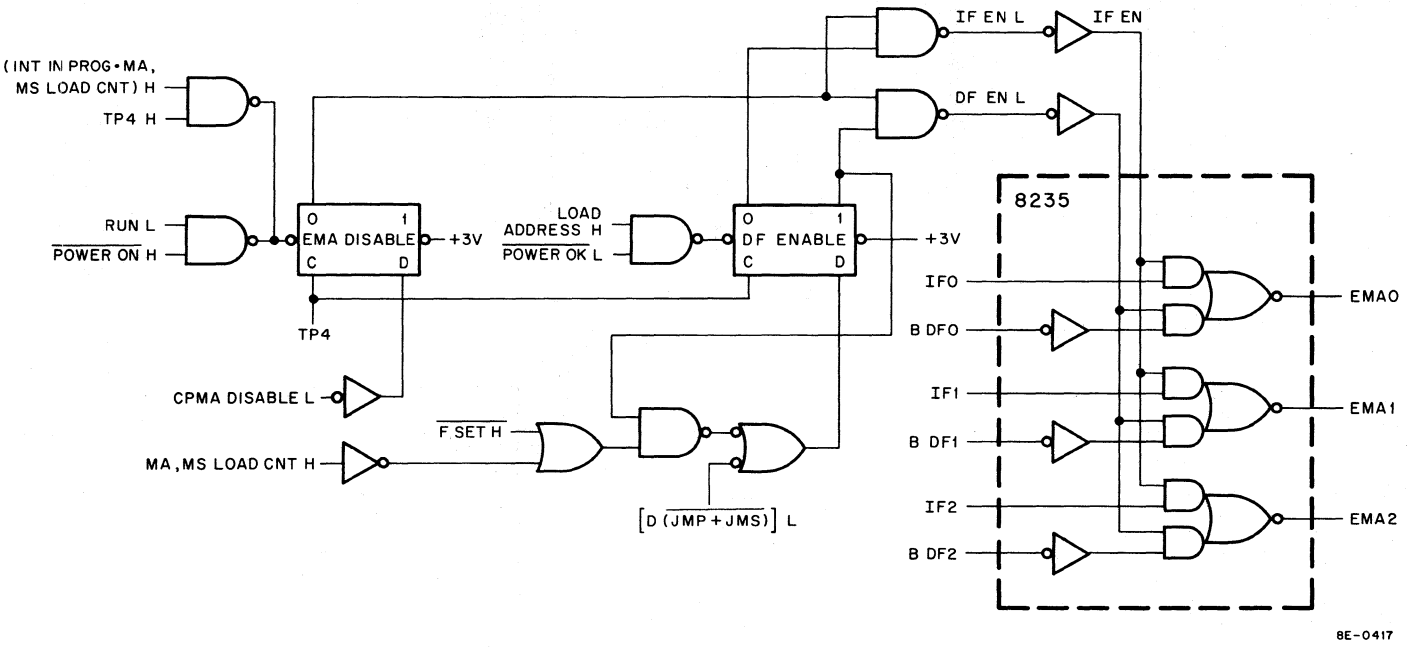

Figure 2-21 Extended Memory Address Logic

SECTION 5 MAINTENANCE

The general procedures concerning preventive and corrective maintenance are given in Volume 1, Chapter 4. When corrective maintenance is required, the technician should use the maintenance programs given in Section 2 of this chapter to determine the nature of the problem. Refer to the option schematic, drawing number E-CS-M737-0-1, for IC locations and pin numbers. Test points have been provided on the module to facilitate troubleshooting.

SECTION 6 SPARE PARTS

Table 2-2 lists recommended spare parts for the KM8-E. These parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 2-2
Recommended KM8-E Spare Parts

DEC Part No.	Description	Quantity
19-05575	IC DEC 7400	1
19-09705	IC DEC 8881	1
19-09615	IC DEC 8271	1
19-09935	IC DEC 8235	1
19-09934	IC DEC 8266	1
19-09594	IC DEC 8251	1
19-09667	IC DEC 74H74	1
19-05547	IC DEC 7474	1
19-05577	IC DEC 7420	1
19-05576	IC DEC 7410	1
19-09686	IC DEC 7404	1
19-09056	IC DEC 74H00	1
19-09486	IC DEC 384A	1
19-09972	IC DEC 6314A	1
13-00365	Resistor 1K, 1/4W, 5%	1
10-01610	Capacitor 0.01 MF DISK, 20%	6
10-05306	Capacitor 6.8 μF, 35V, 10%	1