SECTION 3 – TIMING GENERATOR

3.12 TIMING GENERATOR, GENERAL DESCRIPTION

The M8330 Timing Generator provides synchronizing signals for memory and processor operations. Eight basic processor timing signals and five basic memory timing signals are generated.

3.13 TIMING GENERATOR, FUNCTIONAL DESCRIPTION

Figure 3-19 shows the functional sections of the PDP-8/E Timing Generator. At the heart of the timing operation is a chain of 4-bit shift registers, designated the Timing Shift Register. A preset combination of logic 1s and 0s is repetitively cycled through the chain. Selected outputs of the Timing Shift Register are used to control flip-flops that produce the basic timing signals. Think of the chain of shift registers as a tapped delay line; in this way the concept of shift register timing might be more easily understood. A control signal is placed on the input of this delay line at time 0. This signal flows along the delay line and is sampled at selected taps, where it is used to set or reset flip-flops. Thus, consecutive timing signals can be produced. When the signal reaches the end of the delay line it can be returned to the beginning to start another timing cycle.

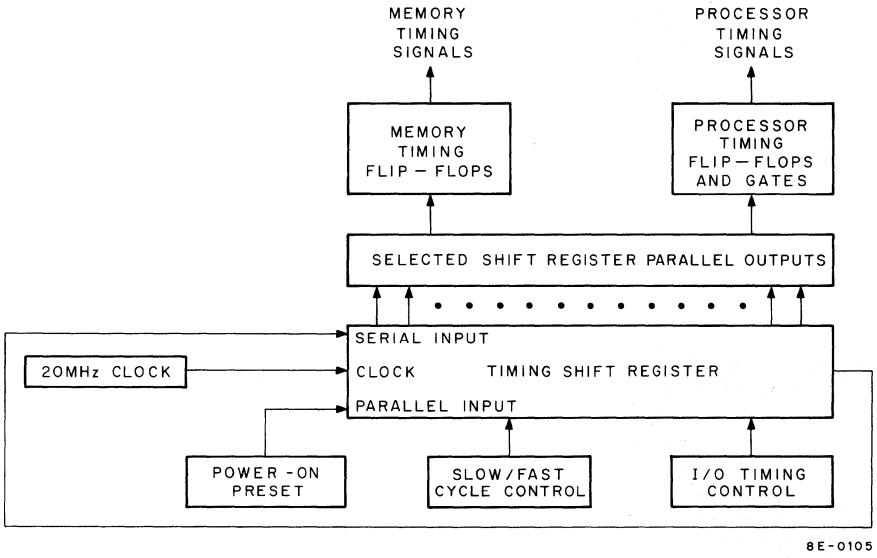

Figure 3-19 Timing Generator, Block Diagram

The delay line concept is easily understood; however, the PDP-8/E features a variable timing cycle. A delay line does not provide the necessary balance between flexibility and simplicity of design, nor does it provide a stable cycle time. Balance and stability are achieved by using a chain of shift registers to produce the timing signals. In its simplest form, the Timing Shift Register is a 28-bit shift register that is right-shifted by clock pulses derived from a 20 MHz, crystal-controlled transistor oscillator.

3.14 BASIC TIMING OPERATION

Figure 3-20 is a simplified representation of the Timing Shift Register; it illustrates the basic timing operation. Assume a method exists for presetting a 0 voltage level in the first stage of this register and also presetting positive voltage levels in every other stage. After this initial condition has been established, the clock is turned on. The first clock pulse shifts the 0 level to stage 2; simultaneously, the positive level from stage 28 is shifted into stage 1. Clock pulse 2 shifts the 0 level into stage 3 and simultaneously shifts a positive level into both stages 1 and 2. Each pulse moves the 0 level to the right by 1 bit, replacing it with a positive level. When the clock shifts the level into stage 5, the flip-flop is cleared by the negative-going edge of the pulse. The flip-flop remains in this reset state until clock pulse 8 shifts the level into stage 9, thereby setting the flip-flop. The signal produced at the 0 side of the flip-flop is a 200 ns gate. Pulses can also be generated, as shown by the AND gate connected to stage 12. When the level is shifted into the stage by clock pulse 11, the gate is enabled and the desired output is produced.

The actual operation is more detailed than the example given, although the basic shifting process remains the same. As the block diagram indicates, the shift register is preset by a circuit that operates the moment power is turned on. Each clock pulse shifts the preset control signal to the right; the register is recycled by connecting the last stage back to the first. In the simplest arrangement, a complete cycle requires 28 clock pulses, or 1.4 μs; this is the "slow" cycle. If a "fast" cycle is called for, the slow/fast cycle control decreases the cycle time by 200 ns. Another control network that modifies the basic shifting operation is shown as I/O timing control on Figure 3-19. This control is used to interrupt the timing cycle while certain I/O transfers are carried out. All of these control circuits are discussed in detail in the following sections.

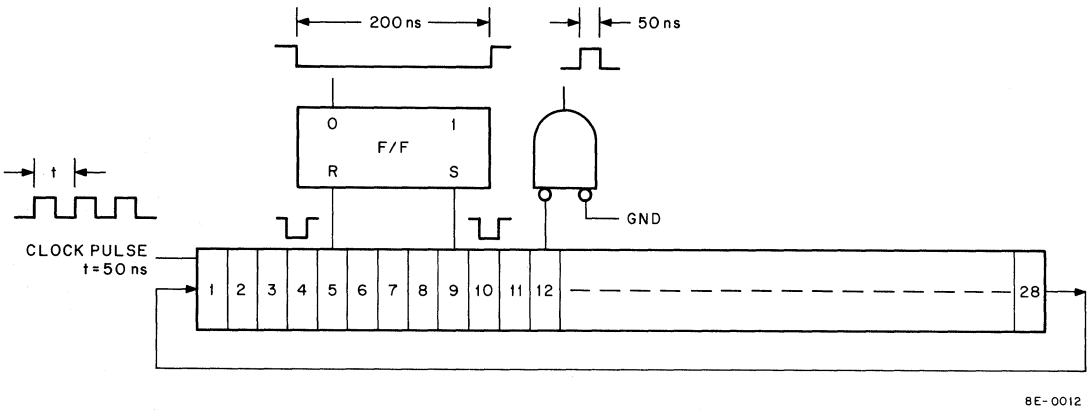

Figure 3-20 Simplified Timing Shift Register Operation

3.15 TIMING SHIFT REGISTER

As previously noted, the shift register is the key to the timing operation. The shift register comprises ten DEC 74194, 4-bit shift registers. A logic representation of the DEC 74194 integrated circuit (IC) is shown in Figure 3-21. The circles at the outputs of each bit (pins 15, 14, 13, and 12), at the corresponding parallel-entry inputs (pins 3, 4, 5, and 6, respectively), and at the serial-in (S) line, indicate that ground level signals represent logic 1s. If the mode (M) input is taken to a positive voltage, the DEC 74194 IC is programmed for parallel loading. Those signals present at the parallel-entry inputs are transferred to the corresponding outputs by a clock pulse at C. Thus, the logic 1 at pin 3 is transferred to output pin 15. The same clock pulse transfers a logic 1 from pin 4 to pin 14 and logic 0s from pins 5 and 6 to pins 13 and 12, respectively.

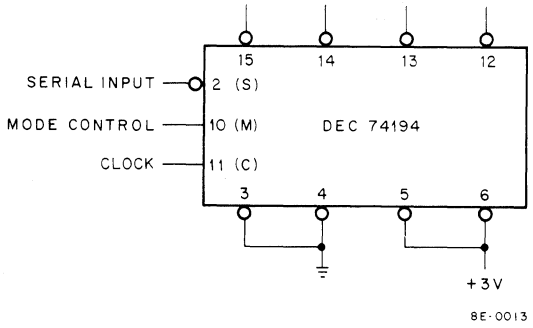

Figure 3-21 DEC 74194 Shift Register Logic

If the M input is taken to ground, rather than to a positive voltage, the DEC 74194 IC is programmed for shifting operation and the parallel-entry inputs are disabled. Information at the S input is shifted to the right one bit each time a clock pulse is applied at C. Thus, a logic 1 at S is shifted to pin 15 by the first clock pulse, to pin 14 by the second, etc. Refer to Appendix A for a detailed discussion of DEC 74194.

Ten shift register ICs are connected to form the Timing Shift Register referred to in Figure 3-19. This arrangement is presented in detail in Figure 3-22. For the moment, all ICs, with the exception of the first, E43, are shown programmed for serial-shift operation; i.e., the M inputs are grounded. Outputs that are used to produce the timing signals are identified according to function. Parallel-entry inputs are shown only on E43.

The discussion of the 28-stage shift register (Figure 3-20) assumed that the register could be preset so that stage 1 contained a 0-voltage level, while all other stages contained positive voltage levels. Essentially, this is accomplished by the power-on preset control. This control operates when the power is first turned on and ensures that, before a timing cycle is initiated, bits 1 and 2 of E43 (represented by output pins 15 and 14, respectively) contain logic 1s, while all other bits of the Timing Shift Register contain logic 0s. The control takes the M input of E43 to a positive voltage and maintains this voltage for a predetermined delay period. Thus, during this time period E43 is programmed for parallel-entry, while the remaining ICs of the register are programmed for serial shifting (the delay period is required to offset the indeterminate state of individual bits at power turn-on; because a bit can assume either a 0 or a 1 level at power-on, the delay period is used to shift out of the register any logic 1s that may be present). The first clock pulse that occurs transfers the logic levels at the parallel-entry inputs of E43 to the outputs. Pins 15 and 14 go to ground (logic 1), and pins 13 and 12 go to +3V (logic 0). The logic 0 at pin 12 is applied to the S input of E38. Thus, the next clock pulse shifts the logic 0 into E38. Each succeeding clock pulse does the same, while also right-shifting the register. During the shifting operation, a signal from the control holds the timing flip-flops in the reset state. This action ensures that the logic 1s being shifted through the register have no affect on the flip-flops. All logic 1s are shifted out of the register in approximately 1.2 μs (25 clock pulses). The register is then in the preset condition.

When the predetermined delay period has ended, E43 must be placed in the right-shift mode by activating a key on the operator's console, thereby asserting the OMNIBUS MEM START L signal. This signal causes the power-on preset control to bring the M input of E43 to ground, programming E43 for shifting operation. Clock pulses at C begin shifting the logic 1s of bits 1 and 2 to the right. A negative pulse moves through the shift register (see Figure 3-23 for a graphic representation of this pulse). The negative-going edge is used to set and reset flip-flops, thereby producing timing gates, while the entire pulse is used to produce timing pulses. Note that 28 clock pulses return the register to the initial condition; thus, a timing cycle of 1.4 μs results (28 clock pulses $\times$ 50 ns per clock pulse).

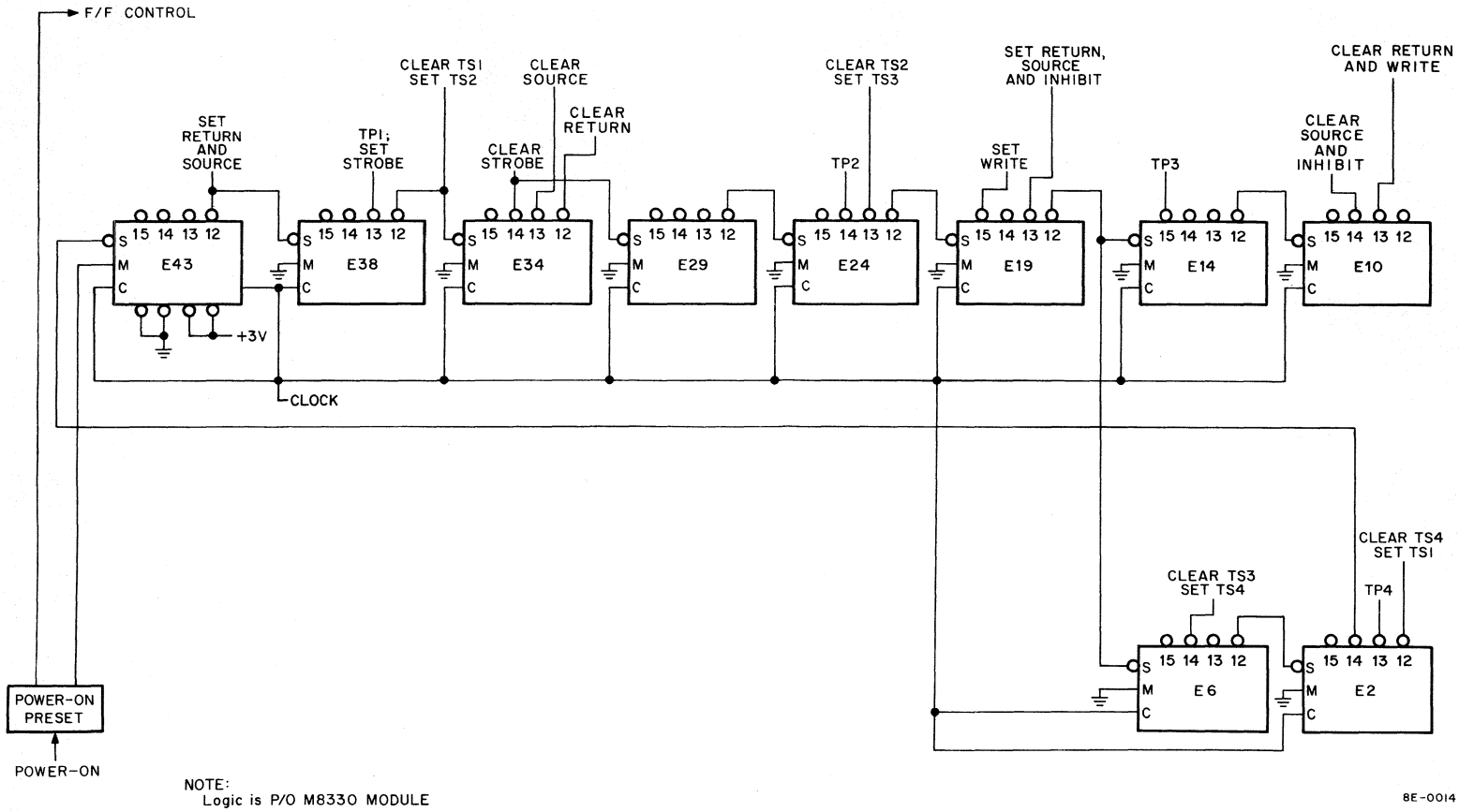

Figure 3-22 Timing Shift Register, Simplified Version

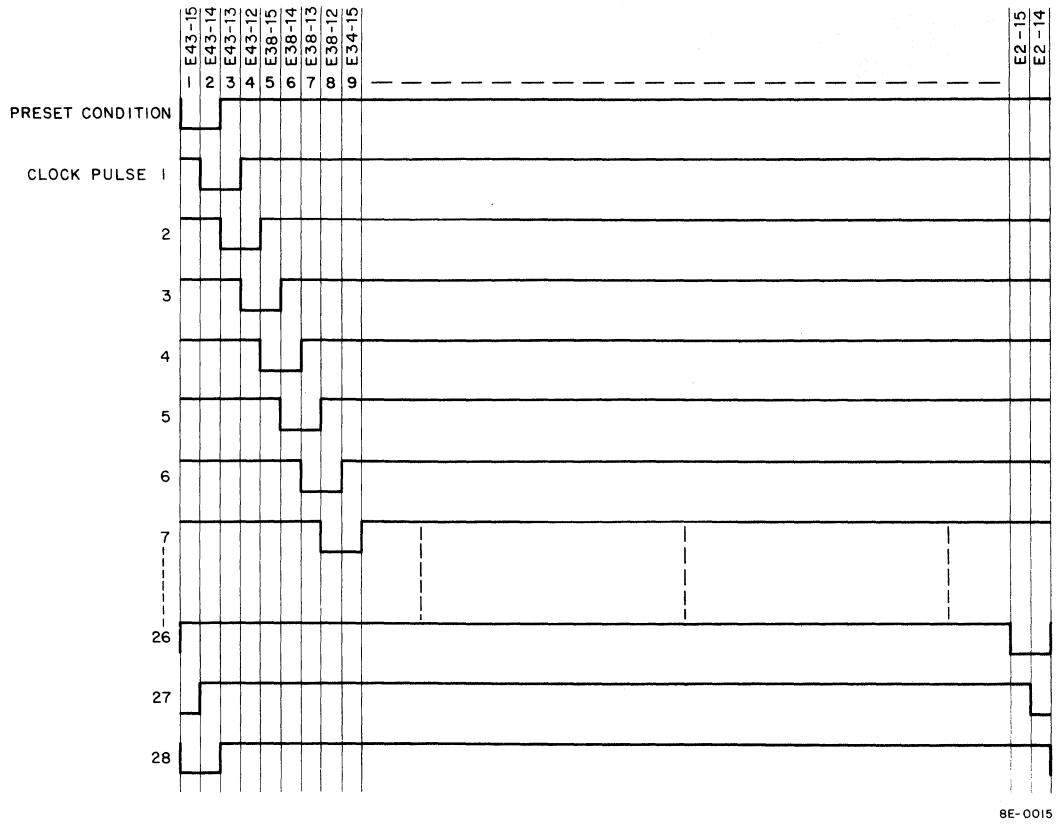

Figure 3-23 Register Composite Logic Signal Timing Diagram

3.16 POWER-ON PRESET CONTROL

The power-on preset control logic is shown in Figure 3-24. Remember that this logic determines the operating mode of IC E43 in the Timing Shift Register. At power-on, the control holds E43 in the parallel-entry mode while all logic 1s are shifted out of the remainder of the register. To carry out this function, the control logic monitors the OMNIBUS POWER OK signal that originates in the power supply (Paragraph 3.47.6).

When power is turned on, POWER OK is negated (grounded). This signal is negated when power supply voltages are below a predetermined level, which is the case at power-on. Power supply voltages do not reach this predetermined level instantaneously at power-on; rather, there is a delay of perhaps hundreds of microseconds before POWER OK is asserted. However, at some time during this delay, the voltages reach a level that is sufficient to start the clock and begin loading and/or shifting the Timing Shift Register. Note that when POWER OK is low, both flip-flop E39B and flip-flop E39A (RUN) are held in the clear state by the asserted POWER PRESET L signal. The 0 output of E39B is high; this signal keeps E43 in the parallel-entry mode. Thus, the conditions for presetting the register are met, viz., E43 is held in the parallel-entry mode, clock pulses shift out the remaining register bits, and the POWER PRESET L signal holds the timing flip-flops in the reset state.

Long after the register has been preset, POWER OK is asserted. After a delay introduced by the delay circuit shown in Figure 3-24, POWER PRESET L is negated (the delay circuit has major significance only at power-off; this is explained shortly). The operator can activate either the DEP, CONT, or EXAM key (Paragraph 3.32.2.1), causing MEM START L to be asserted. This signal sets the RUN flip-flop; the 1 output of the flip-flop causes RUN L to be asserted and provides a high level at the D-input of flip-flop E39B. The next clock pulse sets E39B; the 0-output of the flip-flop places IC E43 in the right-shift mode, and the timing cycle begins.

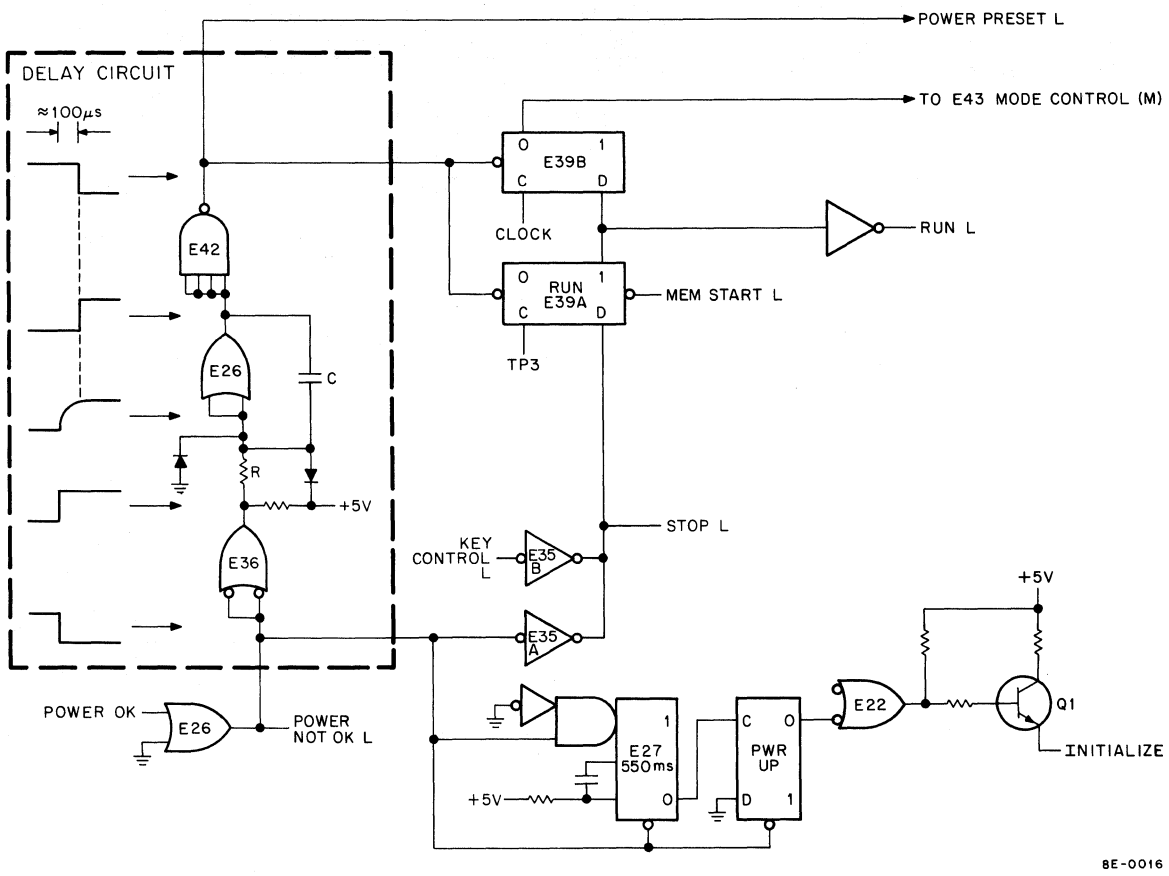

Figure 3-24 Power-On Preset Control Logic

The power-on preset control has an important function at power-off as well. If the operator turns off the power, or a low power supply voltage is detected, POWER OK is negated. To ensure that both processor and memory complete the current timing cycle, the assertion of POWER PRESET L is delayed by approximately 100 μs. This delay is accomplished by the circuit shown within the dashed line; the method is illustrated by the waveforms shown.

When POWER OK is negated, POWER NOT OK L is asserted. The next occurring TP3 pulse resets the RUN flip-flop, thereby negating the RUN L signal and enabling the clock to reset flip-flop E39B. The current timing cycle proceeds to its conclusion and, because IC E43 of the Timing Shift Register is in the parallel-entry mode, the register halts in the preset state. When the POWER PRESET L signal goes low after the delay, it holds E39A, E39B, and the timing flip-flops in the clear state. Timing can be restarted only if the operator activates one of the keys mentioned earlier.

Note that when POWER OK is negated, the STOP L signal is asserted by gate E35A. The STOP L signal can be asserted in a number of other ways as well:

a. A HLT instruction in the program can assert STOP L.

b. The HALT switch or the SING STEP switch on the operator's console can be closed, asserting STOP L.

c. The DEP key, the EXAM key, or the EXTD ADDR LOAD key can be activated, asserting KEY CONTROL L that causes STOP L to be asserted, if the processor is not in a running condition.

That part of the logic in the lower right portion of Figure 3-24 is used to generate the INITIALIZE signal at power-on. At some time before POWER OK goes high, the power supply voltages become sufficiently high for transistor Q1 to conduct, asserting the INITIALIZE signal (note that 1-shot E27 is held in the clear state and the PWR UP flip-flop is held in the set state, both by POWER NOT OK L). When POWER OK goes high, the 1-shot is triggered. 550 ms later, E27 times out; its 0-output clears the PWR UP flip-flop; this causes the INITIALIZE signal to be negated. The long-duration INITIALIZE signal allows all system equipment to complete the operations initiated by the leading edge of the signal.

3.17 SLOW/FAST CONTROL

Figure 3-22 shows only the intermodule connections required for a slow cycle of operation. Other connections, necessary for normal timing operation, are omitted for clarity. The PDP-8/E uses a fast timing cycle (1.2 μs) in normal operation; to produce this fast cycle, five additional connections are necessary (Figure 3-25). The connections are:

a. a connection between E34, pin 14 and E24, pin 3

b. three connections on E24 itself

c. a connection from the slow/fast control to the mode input of E24.

The key to the difference between a fast and slow cycle can be found in IC E24. The mode control signal of E24 is controlled by the 0 side of flip-flop E30. This flip-flop is reset each time either a FETCH state or a non-autoindex DEFER state, both requiring a fast cycle, is entered. Thus, a fast cycle puts E24 in the parallel-entry mode. The outputs of E24 are connected to the parallel-entry inputs; consequently, parallel loading of E24 accomplishes the same result as serial shifting, e.g., four clock pulses shift the signal in E24, pin 15 into E19, pin 15. The difference between fast and slow cycles occurs because of the number of clock pulses needed to shift a signal from E34, pin 14 into E24, pin 15. During a slow cycle, when the parallel-entry inputs of E24 are disabled, five clock pulses shift a signal from E34, pin 14, through E29 and into E24, pin 15. During the fast cycle, however, with the parallel-entry at E24, pin 3 enabled, E29 is bypassed and only one clock pulse is needed to shift the signal from E34, pin 14 into E24, pin 15. TP2 and all subsequent timing signals are generated four clock pulses earlier than during the slow cycle. Therefore, the fast cycle shortens both the memory and processor timing cycles by 200 ns.

NOTE

E30 can be held in the set state by connecting jumper W1 from the "dc set" input to ground. The SLOW CYCLE ONLY feature facilitates troubleshooting by keeping the timing cycle at a constant 1.4 μs.

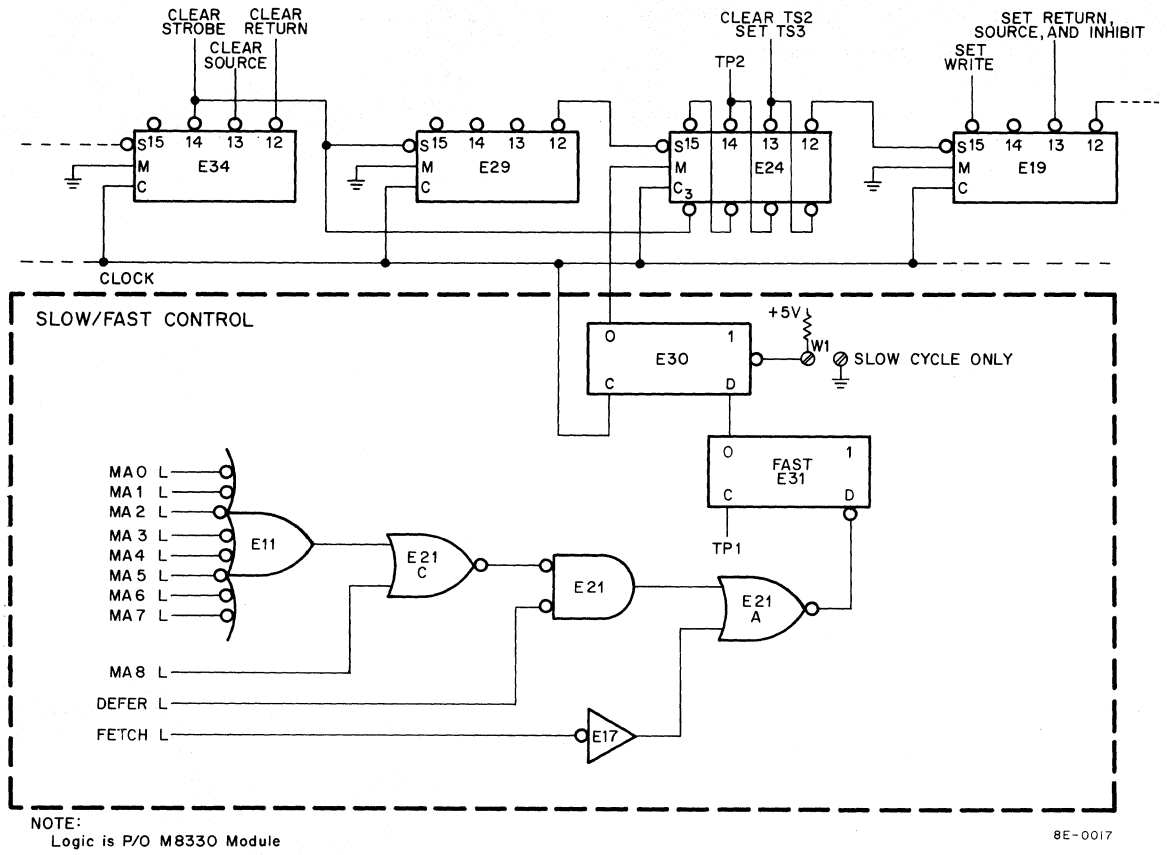

Figure 3-25 Slow/Fast Control Logic

3.18 TIMING DIAGRAM

Timing diagrams of the two cycles of operation are shown in Figure 3-26. The slow cycle is taken as the base and is shown for one timing cycle with TS1 as the initial signal. Processor time states (TS1, etc.) are entered successively, and the timing pulses (TP1, etc.) bracket the trailing edges of their corresponding time state signals.

Note that the time duration of each timing signal, except TS2, remains constant whether the cycle is slow or fast. The 200 ns difference between the slow and fast cycle is accomplished by varying the time duration of TS2 alone and, thus, the amount of time between the read and write portions of a memory cycle is variable. The slow cycle is used when data is read from memory, taken to the processor for modification, and returned to memory. If the data is to be read and then rewritten, as in a FETCH cycle, less cycle time is required; thus, the fast cycle is provided.

3.19 PROCESSOR TIMING

Figure 3-27 shows the logic that provides processor timing signals. Time state signals are provided by four R/S flip-flops; each flip-flop consists of two cross-coupled NOR gates and is controlled by selected pins of the Timing Shift Register. Timing pulse signals are provided by four NOR gates connected to the register. The POWER PRESET L signal from the power-on preset controls the flip-flops at both power-on and power-off (or at some condition of low power supply voltage). The signal clears the TS2, TS3, and TS4 flip-flops and sets the TS1 flip-flop. Thus, the processor is clamped in TS1 if a timing cycle is not in progress.

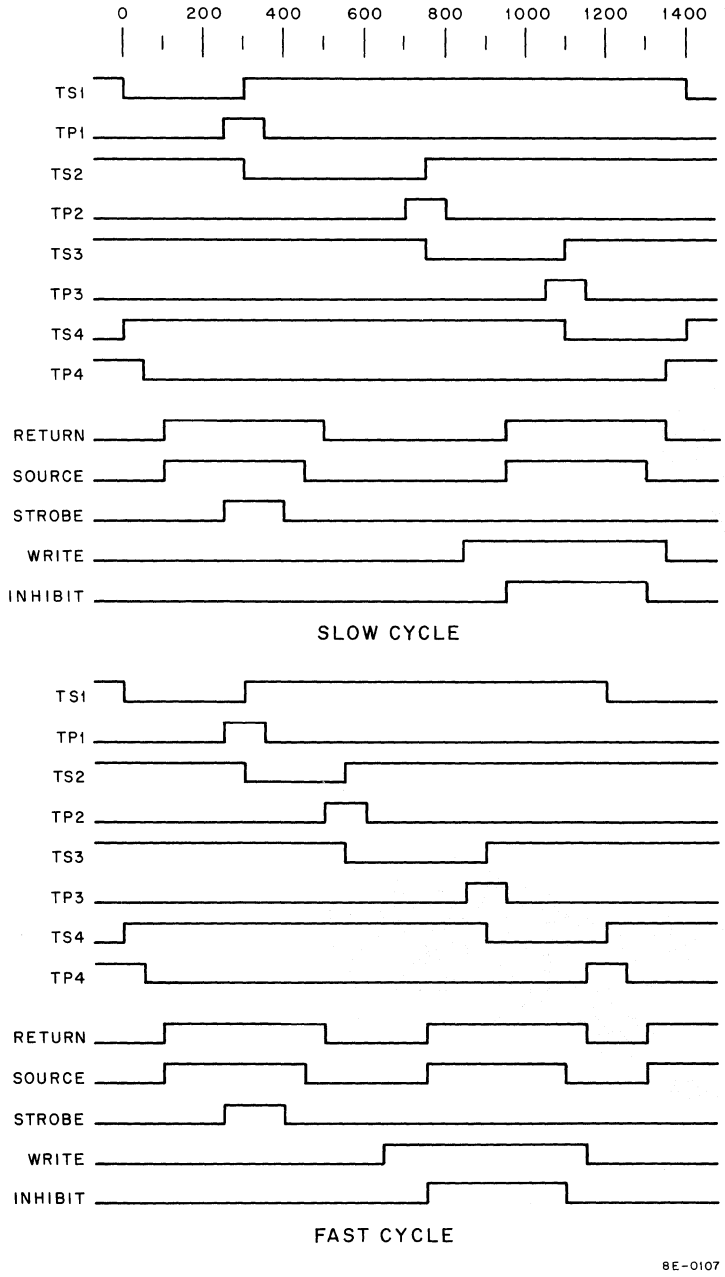

Figure 3-26 Memory and Processor Signals, Timing Diagram

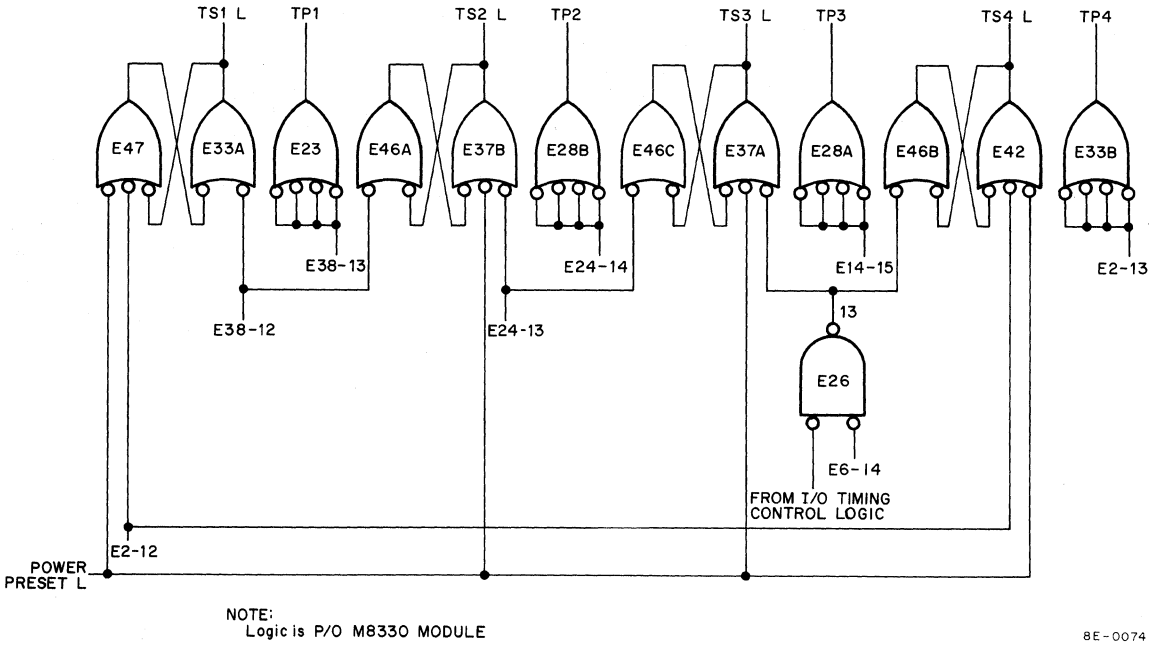

Figure 3-27 Processor Timing Signal Logic

The processor timing signals are used primarily in the CPU, where they generate signals for major register gating and control. Timing pulses have two major functions within the CPU: to sample processor control lines, and to generate "load" signals for the major registers. The time state signals generally provide enabling levels, during which major register outputs are processed.

3.20 MEMORY TIMING

Figure 3-28 shows the logic that provides the memory timing signals. Each signal is generated by an R/S flip-flop of two cross-coupled NOR gates and is controlled by the indicated shift register output pins. The POWER PRESET L signal resets all flip-flops at power-on and power-off.

These timing signals are used in the memory to control the read and write portions of the timing cycle. RETURN and SOURCE are generated during both halves of the cycle, thereby turning on memory current. The conjunction of these two signals determines the width of the current pulse. Note on the timing diagram that return and source are asserted at the same time, but that return is negated 50 ns later than source; this ensures that the memory stack does not remain capacitively charged. STROBE is generated only during the read half of the memory cycle and is used to provide a time reference from which the outputs of the sense amplifiers are sampled. WRITE and INHIBIT are generated only during the write half of the memory cycle. WRITE enables the proper Read/Write switches, thereby providing write currents to the memory stack. INHIBIT is asserted 100 ns later than WRITE and gates the Inhibit Drivers associated with memory control. Details regarding the function of these signals are presented in Section 4, Memory System.

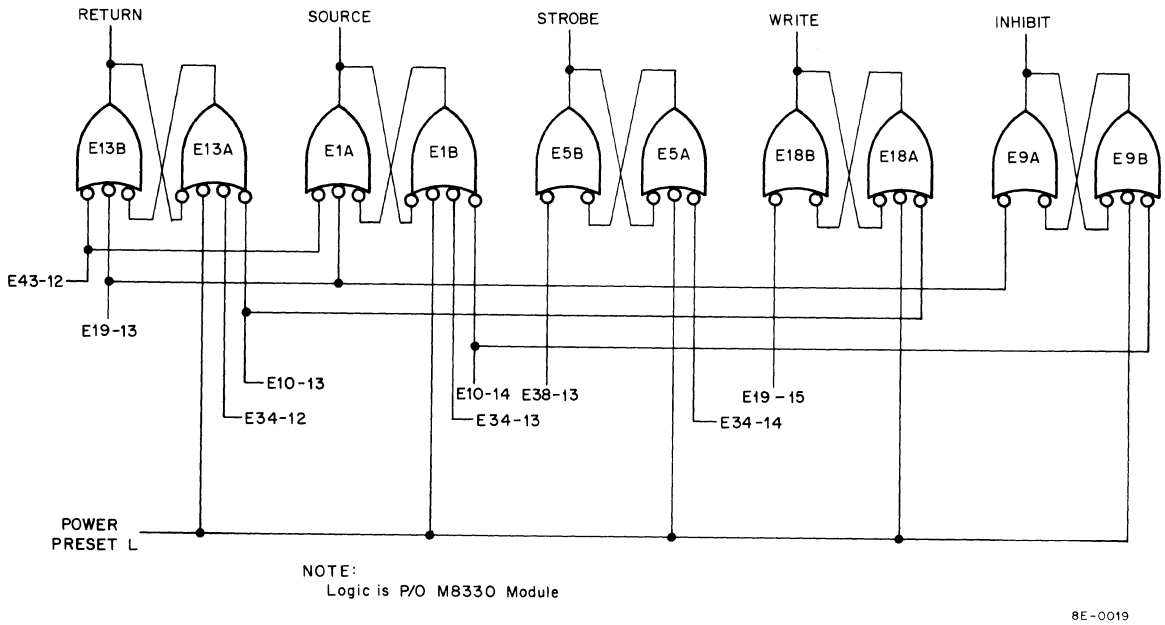

Figure 3-28 Memory Timing Signal Logic

3.21 I/O TIMING CONTROL

The connection between the I/O Timing Control and the mode input of IC E6, omitted from Figure 3-22, is illustrated in Figure 3-29. This control network is used when a peripheral is making more than one I/O transfer during a single IOT instruction and when, because of gating delays, the peripheral needs more time for a transfer than is allowed with normal timing. In either case, the peripheral takes the NOT LAST TRANSFER line to ground, and at the next TP3 time the timing cycle is interrupted and stalled in TS3. The peripheral transfers the information, issuing a BUS STROBE L signal with each transfer. Transfers continue until the peripheral negates the NOT LAST TRANSFER L signal, signifying that the next BUS STROBE L issued by the peripheral is the last of the I/O transfer. This last BUS STROBE L signal restarts the timing cycle, allowing TS3 to end and TS4 to begin.

The last five shift register ICs of the chain are shown in Figure 3-29. Note that all but E6 are programmed for serial shifting. The mode input of E6 is controlled by flip-flop E20B, which is, in turn, controlled by flip-flop E20A. This mode input is normally at a ground level, and the timing signals are generated in the normal way, i.e., the 100 ns negative pulse is shifted from E19 through E14 and E6 to E10 and E2, respectively (Figure 3-23). Note that when E6, pin 14 goes low NAND gate E26 is enabled, provided flip-flop E20A is set; the TS3 L signal is negated, and TS4 is entered.

However, if the peripheral has caused the NOT LAST TRANSFER L signal to be asserted, E20A is cleared at TP3 time, and NAND gate E26 cannot be enabled (the timing diagram in Figure 3-30 visualizes the process). This action prevents both the TS3 L signal from being negated and the TS4 L signal from being asserted. In order to complete the interruption of the timing cycle, the shifting process must be halted. This is done at the next clock pulse time, when flip-flop E20B is cleared. The 0 output of the flip-flop places E6 in the parallel-entry mode. The 100 ns negative pulse is stalled in E6, pins 15 and 14 staying low until the I/O transfer has ended (the state of the parallel-entry inputs of E6 ensures that the state of the outputs remains constant). Note that IC E14 is allowed to continue shifting the negative pulse down the line. This path of the shift register deals with the write half of the memory timing signals. Because I/O transfer data is not transferred directly to memory, the memory timing signals need not be altered in any way.

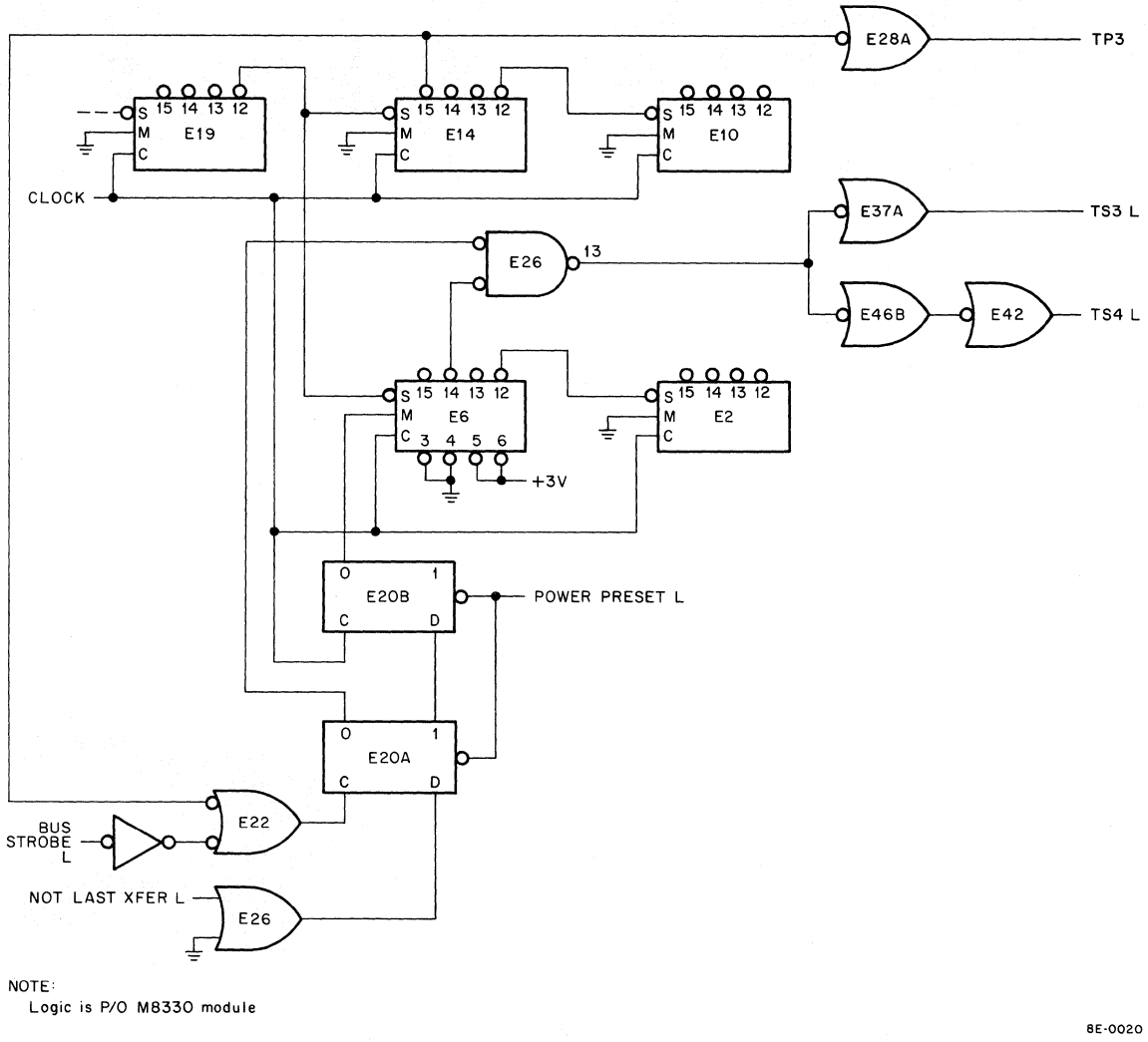

Figure 3-29 I/O Timing Control Logic

When the I/O transfer is complete, the NOT LAST TRANSFER L signal is negated and the peripheral generates a BUS STROBE L signal that sets E20A. NAND gate E26 is enabled, causing the TS3 L signal to be negated and the TS4 L signal to be asserted. The first clock pulse to occur after E20A is set, sets E20B, and E6 is returned to the right-shift mode. The next clock pulse begins shifting the negative pulse through E6 and the timing returns to normal.

Figure 3-30 illustrates an I/O timing interrupt. The cycle time is arbitrarily shown as 1550 ns. Note that the timing, before interruption, is that of a fast cycle. This is always true, because I/O transfers are accomplished while the processor is in the FETCH state, which uses a fast timing cycle.

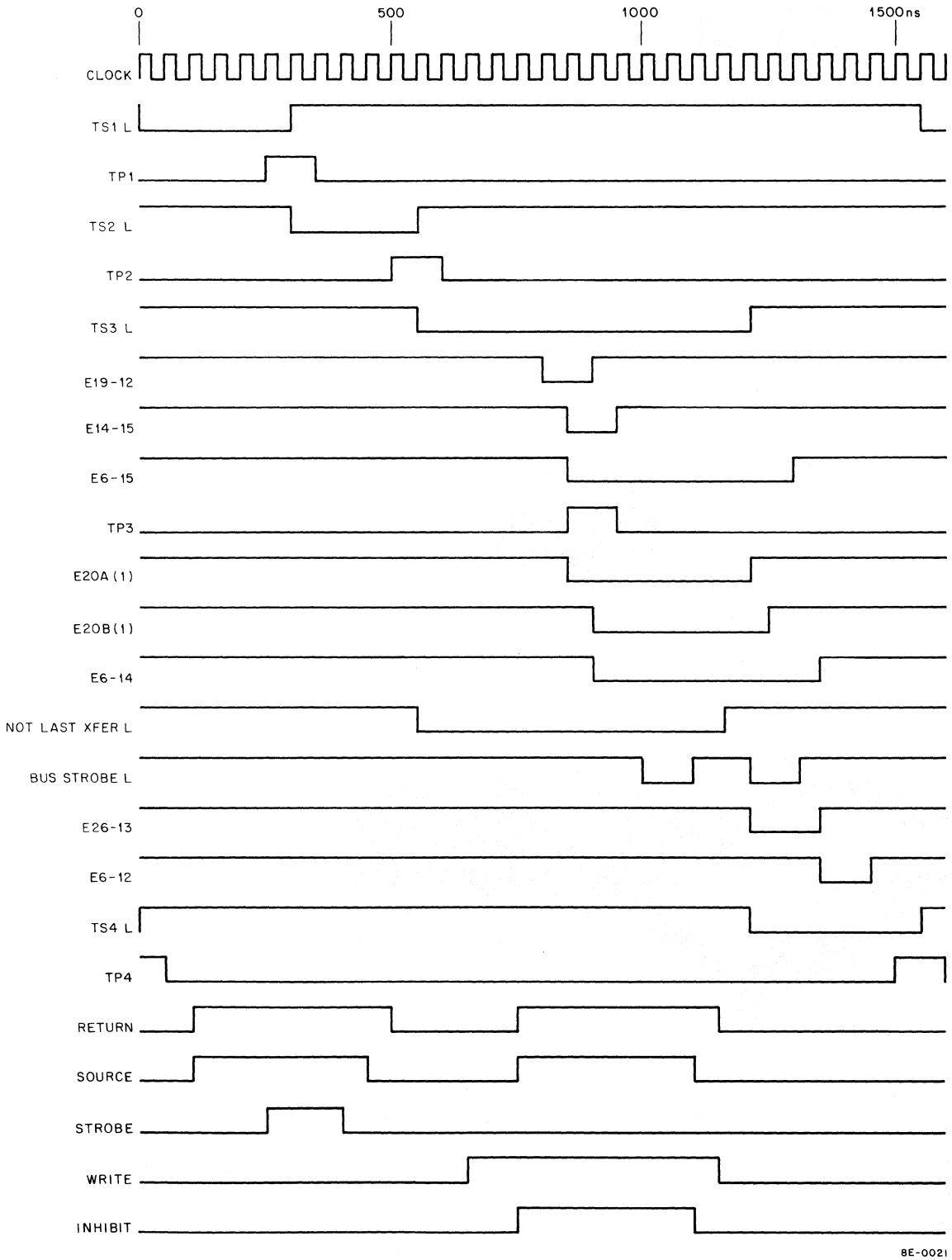

Figure 3-30 Memory and Processor Timing I/O Interrupt