

KG8-E
generator/detector
engineering drawings

MASTER DRAWING LIST

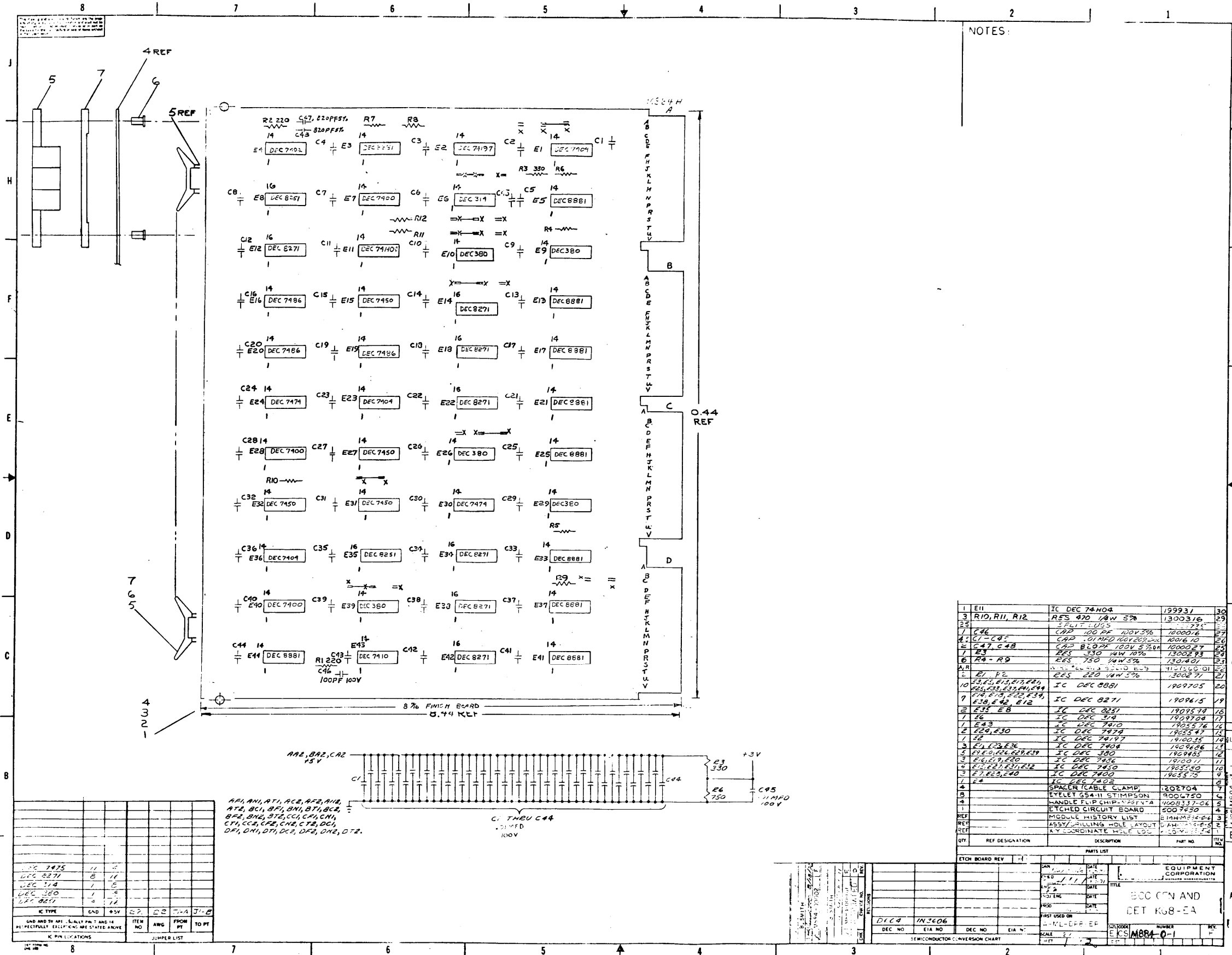
NO.	TITLE	UNIT VARIATIONS															
		KG8-EA															
KG8-E	BCC GENERATION AND DETECTIONS	X															

USED ON OPTIONS	
PDP8-E	
PDP8-M	
PDP8-F	

REVISIONS	DRN.	R. SMITH	DATE	6/71	digital EQUIPMENT CORPORATION <small>MAYNARD, MASSACHUSETTS</small>
	CHK'D.	K. GULICK	DATE	6/71	
	ENG.		DATE		
	PROJ. ENG.		DATE	1-1972	
	PROD.	R. ALLEN	DATE	7/71	
DATE	1-72	CHG. NO.	00001	APP'D.	
REV.	A		KG8-E	GULICK	
	B		KG8-E-2		

FIRST USED ON			SIZE	CODE	NUMBER	REV.
PDP8-E			A	ML	KG8-E	B
SCALE	NONE					
SHEET	1	OF	2	DIST.		

PRINT SET				DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE	OPTION NO.
REV.	DATE	CHG. NO.	APP'D.					
				E-CS-M884-0-1	A	2	REDUNDANCY CHECK	
				A-SP-KG8-EA-1	A	12	SPECIFICATIONS FOR KG8-EA	
				A-SP-KG8-EA-2	A	7	TEST PROCEDURE KG8-EA	
				A-SP-KG8-EA-3		10	ACCEPTANCE PROCEDURE KG8-EA	
				A-PL-KG8-E-0		1	PARTS LIST	
				A-AL-KG8-E-1		1	KG8-E ACCESSORY LIST	
TITLE				REDUNDANCY CHECK		SHEET 2 OF 2		REV 6
						SIZE CODE		NUMBER
						A ML		KG8-E



NOTES:

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	REV
1	E11	IC DEC 7404	199931	30
3	R10, R11, R12	RES 470 1/4W 5%	1300316	29
25	R3, R7, R8	SPLIT LOSS	199705	27
1	C46	CAP 100 PF 100V 5%	1000016	27
4	C1-C5	CAP .01MFD 100V 20% 100K10	1001610	26
2	C47, C48	CAP B50PF 100V 5% 1000027	1000027	25
1	E3	RES 330 1/4W 10%	1300293	24
6	R4-R9	RES 750 1/4W 5%	1304401	23
4	R, R	RES 220 1/4W 5% 110150001	110150001	22
2	E1, E2	RES 220 1/4W 5%	1300271	21
10	E3, E13, E14, E24, E25, E26, E27, E28, E29, E30, E31, E32, E33, E34, E35, E36, E37, E38, E39	IC DEC 8881	1909705	20
7	E9, E10, E22, E23, E38, E40, E12	IC DEC 8271	1909615	19
2	E35, E8	IC DEC 8251	1909579	18
1	E6	IC DEC 84	1909708	17
1	E43	IC DEC 7410	1905576	16
2	E20, E30	IC DEC 7474	1905547	15
1	E8	IC DEC 74197	1900355	14
3	E1, E2, E36	IC DEC 7408	1909686	13
1	E16	IC DEC 380	1909485	12
3	E14, E19, E20	IC DEC 7456	1909011	11
4	E12, E13, E31, E32	IC DEC 7450	1905540	10
3	E1, E20, E40	IC DEC 7400	1905575	9
1	E4	IC DEC 7408	1905575	8
4	SPACER (CABLE CLAMP)	202704		7
8	EYELET GS4-11 SIMPSON	200750		6
4	HANDLE FLIP CHIP (SMT)	1108337-06		5
1	ETCHED CIRCUIT BOARD	6007930		4
1	INCLUDE HISTORY LIST	21449543		3
REF	ASSY DRILLING HOLE LAYOUT	21449543		2
REF	XY COORDINATE HOLE LOC	21449543		1

IC TYPE	GND	+5V	Q1	Q2	Q3	Q4	Q5
DEC 7475							
DEC 8271							
DEC 314							
DEC 380							
DEC 8251							

A01, A02, A03, A04, A05, A06, A07, A08, A09, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, A32, A33, A34, A35, A36, A37, A38, A39, A40, A41, A42, A43, A44, A45, A46, A47, A48, A49, A50, A51, A52, A53, A54, A55, A56, A57, A58, A59, A60, A61, A62, A63, A64, A65, A66, A67, A68, A69, A70, A71, A72, A73, A74, A75, A76, A77, A78, A79, A80, A81, A82, A83, A84, A85, A86, A87, A88, A89, A90, A91, A92, A93, A94, A95, A96, A97, A98, A99, A100.

SEMICONDUCTOR CONVERSION CHART

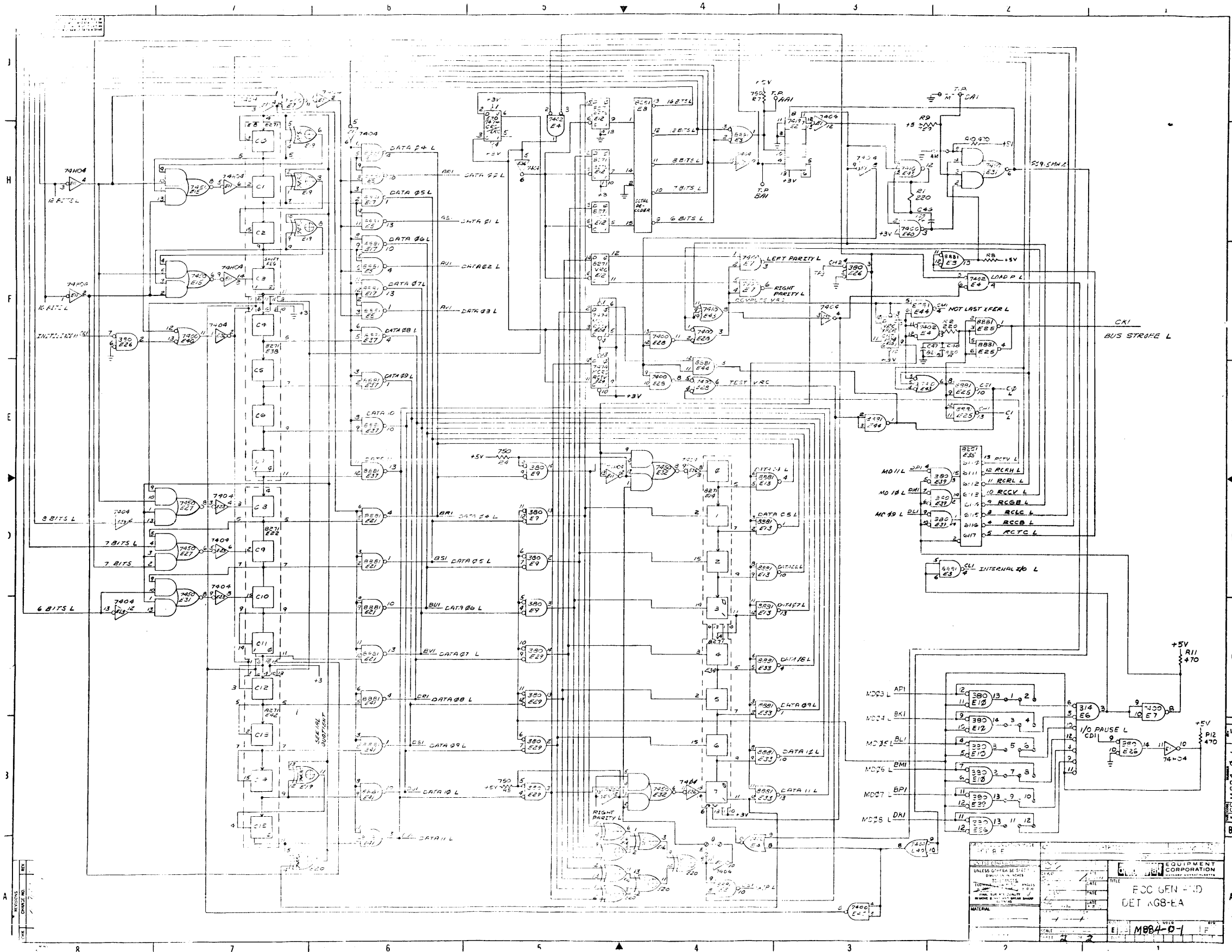
DEC NO	EIA NO	DEC NO	EIA NO
DEC 7404	7404	DEC 7404	7404
DEC 8271	8271	DEC 8271	8271
DEC 8881	8881	DEC 8881	8881

SCALE: 2X

EQUIPMENT CORPORATION

800 CON AND DET K8B-EA

SCALE: 2X



UNLESS OTHERWISE SPECIFIED		EQUIPMENT CORPORATION	
DATE	REV	DATE	REV
ECC GEN AND DET W88-EA		M884-0-1	

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DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 7/1/71

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A		KG8E-00002	B.SMITH	7-72		7/1/72

Formerly DP8-EP Redundancy Check.

ENG	APPD	SIZE	CODE	NUMBER	REV
Robert Smith		A	SP	KG8-EA-1	A

ENGINEERING SPECIFICATION

digital

CONTINUATION SHEET

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

0.0 Overall Description

The KG8-EA Block Check Character Generation and Detection Option provides error detection capabilities for data communications applications. This option performs directly with the PDP8/E bi-directional data bus, coupled with input/output instruction. Thus, it can perform, non-currently, with a number of communication devices.

Additionally, the KG8-EA adds an exclusive "OR" Instruction to the PDP8/E repertoire.

1.0 General Specification

1.1 Definition of Basic System

The Block Check Character Generation and Detection Option provides three types of error detection facilities: Vertical Redundancy Check (VRC), Longitudinal Redundancy Check (LRC) and Cyclic Redundancy Check (CRC).

Refer to appendix for detailed definition and example of VRC, LRC and CRC.

The System Block Diagrams (Fig. 1) shows the error detection capabilities simplified. The basic parts are: The cyclic 16-bit shift register for LRC and CRC, the Shift/Hold Register, the VRC logic, and the control.

Cyclic Shift Register: accumulates the Block, check character (BCC) for LRC and CRC. The contents of the cyclic shift register is available to the program for testing and/or transferring to some data communications facilities.

Shift/Hold Register: Provides a) shift register for a serial data transfer to the cyclic shift register, b) hold or latch register for generation of Vertical Redundancy.

VRC Logic: Generates or tests character parity.

Control: Provides a) buffering to (from) the PDP8/E OMNIBUS, b) device selection c) function selection and d) timing.

1.2 Option: Either ODD parity or EVEN parity (VRC) can be jumper selected.

SIZE	CODE	NUMBER	REV
A	SP	KG8-EA-1	A

ENGINEERING SPECIFICATION



CONTINUATION SHEET

TITLE KGS-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

- 1.3 Mechanical Packaging:
The Redundancy logic is contained in one 8½ inch Quad Logic module. Pin assignments conform to the PDP8/E OMNIBUS specifications.
- 1.4 Environmental Specification:
 - 1.4.1 Power Required
 - +5 @ 931 ma (max)
 - +15 @ NONE
 - 15 @ NONE
 - 1.4.2 Temperature Range
 - 0° - 60°C C 95% Humidity (non-condensing)
- 1.5 Performance Specifications:
 - 1.5.1 Vertical Redundancy Check (VRC): Test or generate odd or even parity for up to eight bit characters. The parity bit is either right justified to AC11 or left justified to AC04.
 - 1.5.2 Longitudinal Redundancy Check (LRC): Computes or compares check sum for 6, 7, 8, 12 and 16 bit characters. Two bytes are required for LRC 12 & 16.
 - 1.5.3 Cyclic Redundancy Check (CRC): IBM compatible for CRC-16 and CRC-12. Constants utilized are $X^{16} + X^{15} + X^2 + 1$ and $X^{12} + X^{11} + X^3 + X^2 + X + 1$ for CRC-16 and CRC-12 respectively. "X" is module two.
 - 1.5.4 Cycle Time:

VRC compute	1.5 usec.
VRC Test	1.2 usec.
CRC/LRC	1.2 usec.

2.0 Vendor
None

3.0 Programming:

3.1 Instructions

CODE	INSTRUCTIONS	DESCRIPTION
6XX0	Test VRC (RCRV)	Test character parity for the contents of AC04 to AC11. The next instruction is skipped if the contents of the AC has an ODD number of ONE's. This function may be

SIZE A	CODE SP	NUMBER KGS-EA-1	REV A
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TITLE KGS-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

- 6XX1 Read BCC High (RCRH)
JAM transfers the Least Significant (LSB) 8 bits of the BCC accumulation to the AC (right justified). This instruction is utilized only for 16-bit check sums. If the characters included in the BCC had their MSB in AC11 then RCRL will deliver the LSB of the BCC in AC04.
- 6XX2 Read BCC Low (RCRL)
JAM transfers the Most Significant (MSB) 8 or 12 bits of the BCC Accumulation to the AC (right justified). If the characters included in the BCC had their MSB in AC11, then RCRH will deliver the MSB of the BCC to AC11.
- 6XX3 Compute VRC (RCCV)
Generates character parity for the contents of AC04 to AC11 (unused bits must be negated). Parity bit can be in position AC04 or AC11 and this function may be issued with the RCGB instruction if the appropriate control bit is selected. See RCGB and RCLC instructions for details.

Hardware Procedure: The character in the AC is latched into the KGS-EA, with corrected parity, and via an extended cycle the character is then JAM transferred back to AC04 - AC11.
- 6XX4 Generate BCC (RCGB)
Generates a LRC or CRC Block check character (BCC). The LRC can be generated from 6, 7, 8, 12 and 16 bit characters. Note the LRC 12 is accumulated with two 6-bit bytes and LRC 16 with two 8-bit bytes. The CRC is generated from 6 or 8 bit characters for a 12 and 16 bit BCC, respectively. The Receive and Transmit BCC's are compared by treating the transmitted BCC as data and including it in the Receive accumulation. In doing so, the Receive BCC generator will go to Zero if there were no errors in transmission.

SIZE A	CODE SP	NUMBER KGS-EA-1	REV A
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TITLE KGS-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

Additionally, the hardware clears the AC if RCCV is not micro programmed with RCGB. Also this instruction provides the functions defined for RCCV and RCTV instructions - if the appropriate control bit is selected. (See RCLC instruction)

6XX5 Load Control (RCLC)

"JAM" transfers the contents of the AC to the control register. The control functions are as follows:

AC05 One: cyclic redundancy check
Zero: Longitudinal redundancy check

AC Bit 678:
000: 16 Bit BCC
001: 12 Bit BCC
010: 8 Bit BCC
011: 7 Bit BCC
100: 6 Bit BCC

AC09 One: Generated VRC bit → AC11
Zero: Generated VRC bit → AC04

AC10 One: A RCGB instruction also causes an RCCV sequence to occur. The BCC will be generated utilizing the character with corrected parity.

AC11 One: A RCGB instruction also causes an RCTV sequence to occur.

6XX6 Clear BCC Accumulation (RCCB)

Clears the 16-bit Cyclic Register. This register is also cleared by INITIALIZE.

6XX7 Maintenance Clock RCTC

When the "M" jumper is installed this instruction causes one clock pulse for BCC computation.

4.0 Interface Specification
The interface conforms to the FDP8/E OMNIBUS specifications.

5.0 Test Procedures
The diagnostic program for the KGS-EA is MAINDEC-8E-D8CA. Refer to the document for operating instructions.

SIZE A	CODE SP	NUMBER KGS-EA-1	REV A
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TITLE KGS-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

APPENDIX

- A. Vertical Redundancy is parity on a character basis, where one bit of each character is reserved as the parity bit. The parity bit forces the character to have either an even or odd number of ONE's. This option will generate *EVEN/ODD parity. However, odd or even parity may be checked.
- B. Longitudinal Redundancy is a checksum accumulation over a Block of Characters and is more reliable than VRC in detecting errors. A common configuration utilizes LRC and VRC to increase the probability of detecting multiple errors.

The LRC accumulation is an exclusive "OR" of all characters in a message, by column (Figure A1).

	Column
	P 7 6 5 4 3 2 1
Character 1	0 1 1 1 1 0 0 1
Character 2	1 0 0 1 1 0 0 0
Character 3	0 0 0 0 0 1 1 1
Character 4	1 1 1 1 0 0 0 0
LRC Check Sum	0 0 0 1 0 1 1 0

FIGURE A1

The hardware implementation is cyclic. Figure A2 illustrates the hardware configuration for an eight bit code whereas the polynomial is $(X^8 + 1)$.

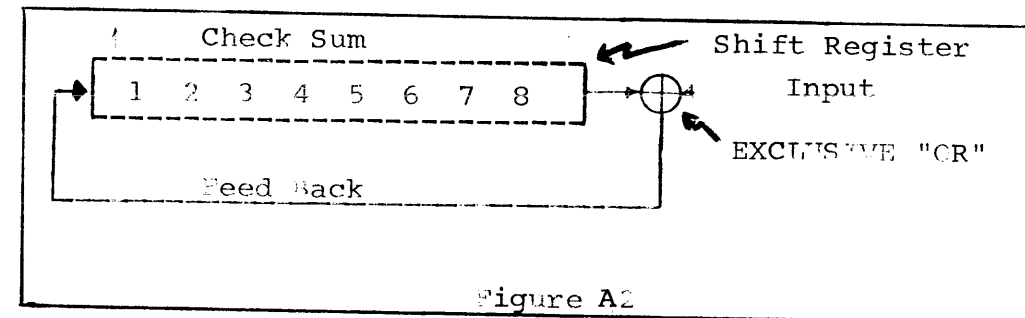


Figure A2

Both the Transmitting and Receiving Stations are expected to compute the check sum. At the end of each message block, the transmitting stations sends its check sum. The receiving station than compares the check sums--if equal--the message is assumed to be without error.

*For EVEN parity: Install jumper "E"; remove jumper "O".
For ODD parity: Install jumper "O"; remove jumper "E".

SIZE A	CODE SP	NUMBER KGS-EA-1	REV A
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TITLE KGB-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

C. Cyclic Redundancy (CRC) as implemented in this option is IBM compatible for CRC-12 and CRC-16.

The CRC Check sum is a division using the numeric binary value of a message as the dividend which is divided by a constant. The division is performed serially with the quotient discarded. When the process is completed, the remainder becomes the check sum.

Both the Transmitting and Receiving Stations are expected to compute the check sum. At the end of each message block, the transmitting stations sends its check sum. The receiving station then compares the check sums--if equal--the message is assumed to be without error.

The probability of error detection is somewhat increased when CRC and VRC are combined.

C.1 CRC-12

When operating with six bits per character, the BCC accumulation is 12 bits and utilizes the generator polynomial $x^{12} + x^{11} + x^3 + x^2 + x + 1$. This polynomial has the prime factors $(X + 1)$ and $(X^{11} + X^2 + 1)$, and provides error detection of butst up to 12 bits in lenth. Additionally, 99.955% of error burst greater than 12 bits will be detected.

Figure A3 illustrates the operation of the cyclic generators for CRC-12 block check. NOTE: the crosses are exclusive OR's and the squares are stages of the shift register.

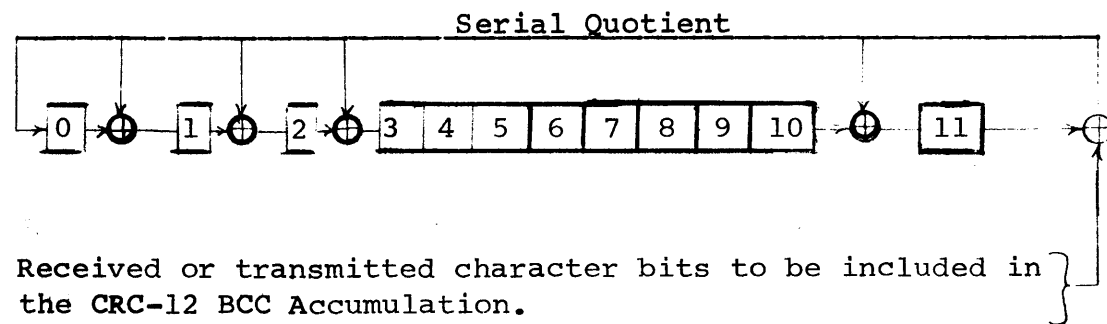


Figure A3

SIZE A	CODE SP	NUMBER KGB-EA-1	REV A
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TITLE KGB-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

C.2 CRC-16

When operating with 8 bits per character, the BCC accumulation is 16 bits and utilizes the generator polynomial $x^{16} + x^{15} + x^2 + 1$. This polynomial has the prime factors $(X + 1)$ and $(X^{15} + X + 1)$ and provides error detection of burst up to 16 bits in length. Additionally, 99.9997% of error burst greater than 16 bits will be detected.

Figure A4 illustrates the operation of the cyclic generator for CRC-16 block check. NOTE: the crosses are exclusive OR's and the squares are stages of the shift register.

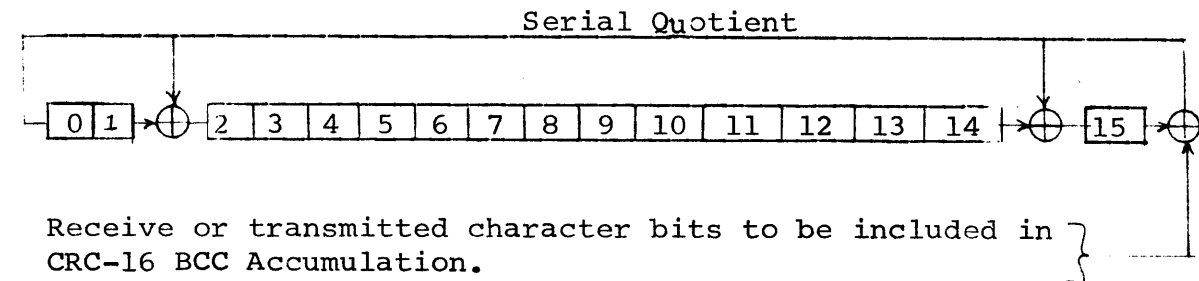


Figure A4

C.3 CRC-16 example

The data used to accumulate a CRC-16 BCC is the ACSII coded letters A, B, C with odd character parity.

The transmit sequence is illustrated in Figure A5. Illustrated is the step-by-step shift pattern of the cyclic generator as the data is serially applied to the input.

Line 1: the first row of numbers, lines, and asterisks is symbolic of the hardware configuration for CRC-16. The asterisks represent exclusive OR operations and the lines represent the feedback path (quotient) and direction. Note that the encoded data is shifted from left to right.

Line 2: is the initial conditons, an all Zero register.

Line 3: a ONE is presented to the input line, from data for transmit, and is exclusive OR'ed with a ZERO from bit 15. The resultant on the serial quotient line is a ONE. Further, the serial quotient is presented to: a) bit 0 b) the exclusive OR between bits 1 and 2, c) the exclusive OR between bits 14 and 15. When the feed back settles down

SIZE A	CODE SP	NUMBER KGB-EA-1	REV A
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TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

Figure A5 Transmit CRC 16

* Indicates an exclusive OR function.

Line #	SERIAL QUOTIENT															SERIAL QUOTIENT	DATA FOR TRANSMIT				
	0	1	*	2	3	4	5	6	7	8	9	10	11	12	13			14	*	15	*
1	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Input	Initial
2	1	0		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
3	1	1		1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
4	1	1		0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0 A
5	1	1		0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0
6	1	1		0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	1	1		0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0
8	1	1		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0
	0	1		1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1
	1	0		0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1
	1	1		1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0
	0	1		1	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1
	0	0		1	1	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0 B
	0	0		0	1	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0
	0	0		0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	1	0	0
	0	0		0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	1	1
	1	0		1	0	0	0	0	1	1	1	0	1	0	0	0	0	0	1	1	1
	0	1		0	1	0	0	0	0	0	1	1	1	0	1	0	0	0	0	1	0
	0	0		1	0	1	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0
	0	0		0	1	0	1	0	0	0	0	0	1	1	1	0	1	0	1	0	0 C
	1	0		1	0	1	0	1	0	0	0	0	0	1	1	1	1	1	1	1	0
	1	1		1	1	0	1	0	1	0	0	0	0	0	1	1	0	0	1	1	0
	1	1		0	1	1	0	1	0	1	0	0	0	0	0	0	1	0	0	1	0
	0	1		1	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0

BCC

TRANSMIT BIT PATTERN (LEFT TO RIGHT)

10000011 01000011 110000010 1000001010110110
 a b c BCC

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

the first shift takes place netting line 3.

This shift also presents a new bit, for encoding, at the input line causing another serial quotient.

The next shift leads to line 4 etc., etc. This is continued until all data bits have been processed. The BCC is the contents of the shift register after the last shift.

The BCC is expected to be transmitted most significant bit first (ie. bit 15).

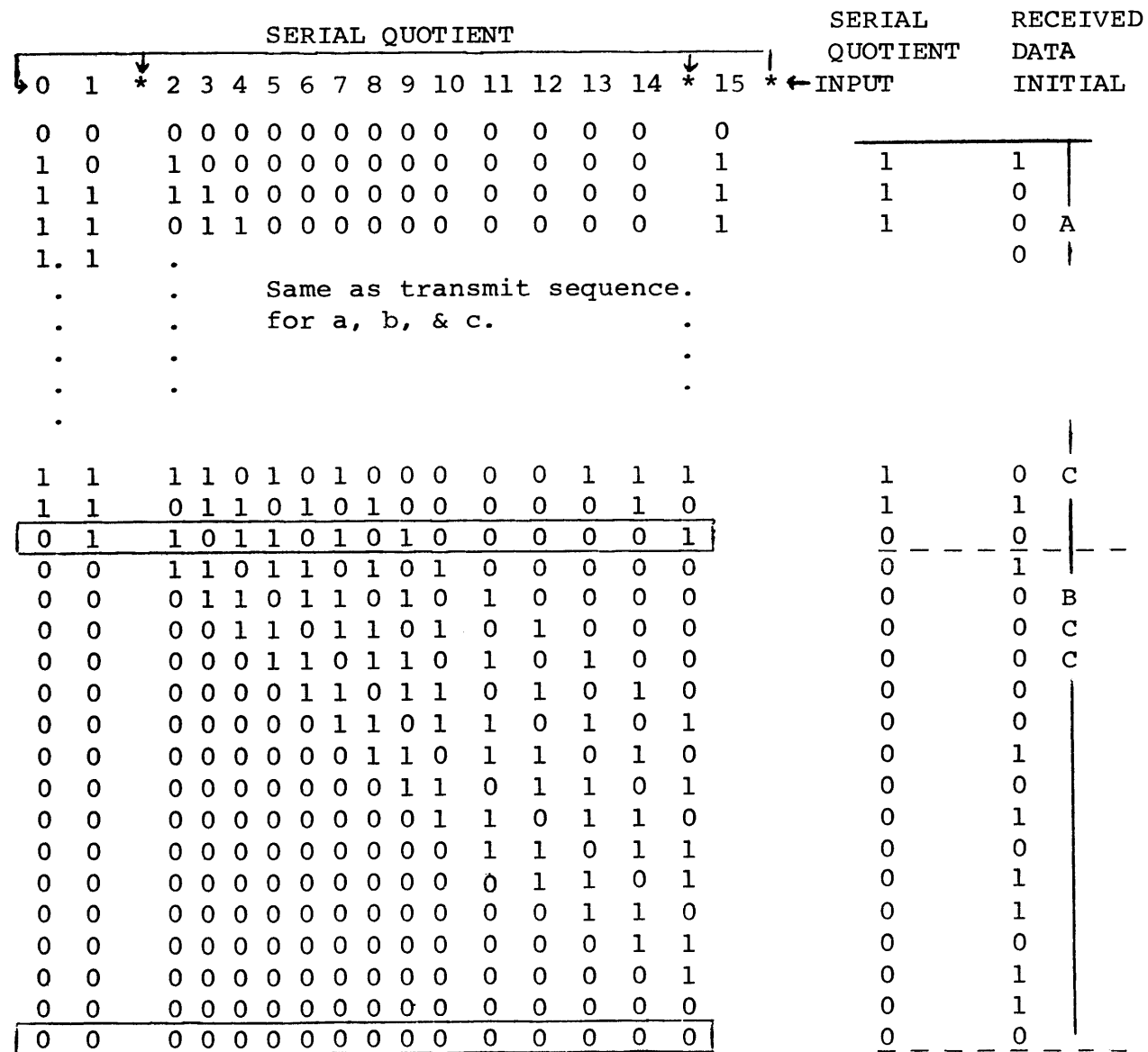
See the bottom of figure A5 for the transmit bit pattern.

The receive step-by-step sequence is illustrated in figure A6 and is identical in procedure used for the transmit sequence. Additionally, the Receive shift register operates (encodes) on the transmitted BCC. This last step is really a comparison of the Transmitted BCC to the Receive BCC and MUST result in an all ZERO receive shift register.

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

Figure A6 Receive CRC 16

*Indicates an exclusive OR function



Message is assumed to be without error if the CRC register is returned to all zeroes.

TITLE KG8-EA BLOCK CHECK CHARACTER GENERATION AND DETECTION

5.0

1. LRC/CRC Generator:
 - a) Generates check sum with right shift.
 - b) Indicates an exclusive OR function.
 - c) Boxes are storage elements.
 - d) CRC or LRC check sum is compared by an LRC if the check sum character compares OK, the register contents go to 0.
 - e) Performs the following via 6, 7, or 8 bit bytes:
 - E1...CRC16 ($X^{16}+X^{15}+X^2+1$)
 - E2...CRC12 ($X^{12}+X^{11}+X^3+X^2+X+1$)
 - E3...LRC16
 - E4...LRC12
 - E5...LRC 8
 - E6...LRC 7
 - E7...LRC 6

