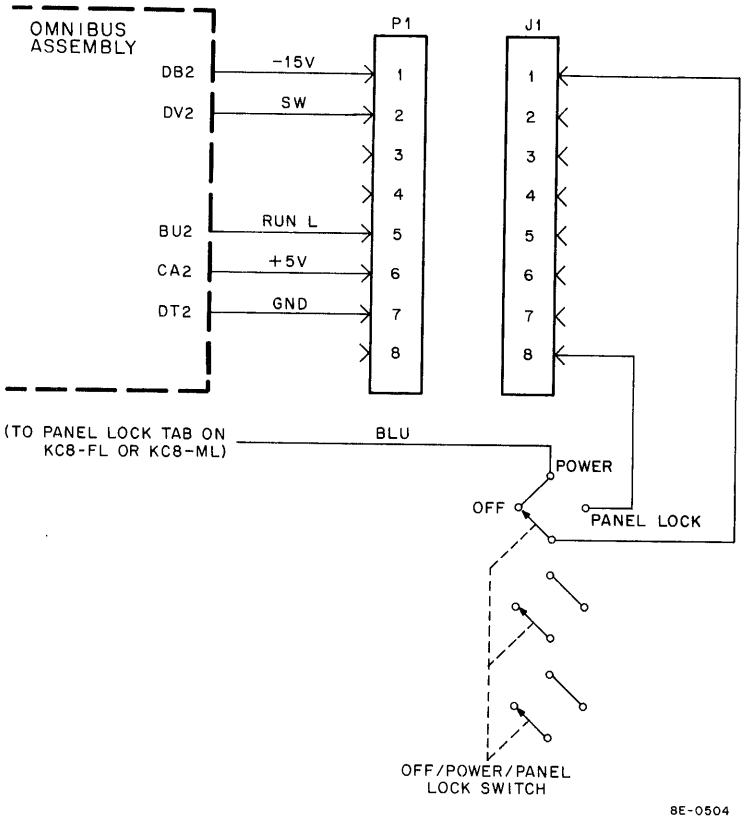


Figure 3-66 PDP-8/M Panel Lock Wiring

3.33 PROGRAMMER'S CONSOLE, GENERAL DESCRIPTION

Figure 3-67 is a block diagram of the two major functions of the KC8 Programmer's Console: manual operation and display. The display enables the operator to monitor the content of certain processor major registers, as well as the state of many of the OMNIBUS signal lines. Manual operation enables the operator to load programs into memory, initiate and halt automatic operation of the computer, and perform specialized tasks, which are discussed in subsequent sections.

As shown in Figure 3-67, the manual operations can be divided into a number of subordinate functions for convenience. Thus, several keys are grouped under the heading "manual start" to indicate that these keys initiate a timing cycle. Two switches, SING STEP and HALT, can be used to stop operation and are grouped under the heading "manual stop". The flow diagram, Figure 3-68, relates the manual functions to the processor time states.

The logic that makes manual operation and display possible is contained on the Programmer's Console module. The logic of the PDP-8/F Programmer's Console, KC8-FL, is simpler than that of the PDP-8/E Programmer's Console, KC8-EA (an earlier version of the KC8-FL uses logic that is similar to that of the KC8-EA; this version, which is not detailed in this manual, has been improved on the current model). The KC8-EA is described in Paragraph 3.33.1; the KC8-FL is described in Paragraph 3.33.2.

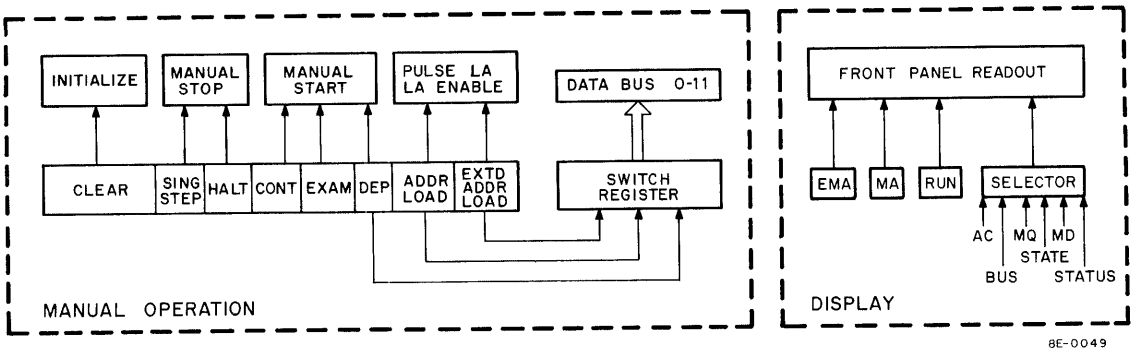


Figure 3-67 Programmer's Console, Block Diagram

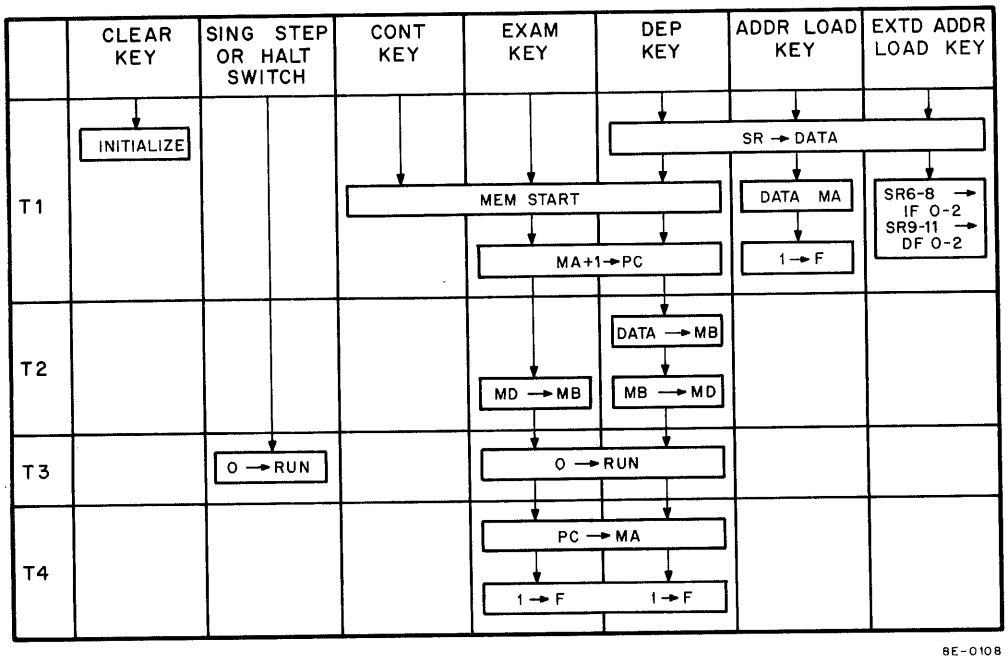


Figure 3-68 Manual Operation Function, Flow Diagram

3.33.1 KC8-EA Programmer's Console

3.33.1.1 Manual Operation

Switch Register — The switch register consists of 12 switches that enable the operator to load the processor CPMA Register with a 12-bit memory address, to deposit a 12-bit data word in a selected memory location, and to load the extended address bits, if more than 4K of memory is used. To carry out these functions, the switch register is operated in conjunction with the DEP, ADDR LOAD, and EXTD ADDR LOAD keys, as indicated on the block diagram.

Figure 3-69 illustrates the logic and circuits used to set data into the switch register and to place it on the DATA 0–11 lines; the circuit used with switch register bit 0 is shown in detail. If switch S11 is open (in the up position on the front panel), a positive voltage is applied to one input of NAND gate E25. If a positive enabling voltage is

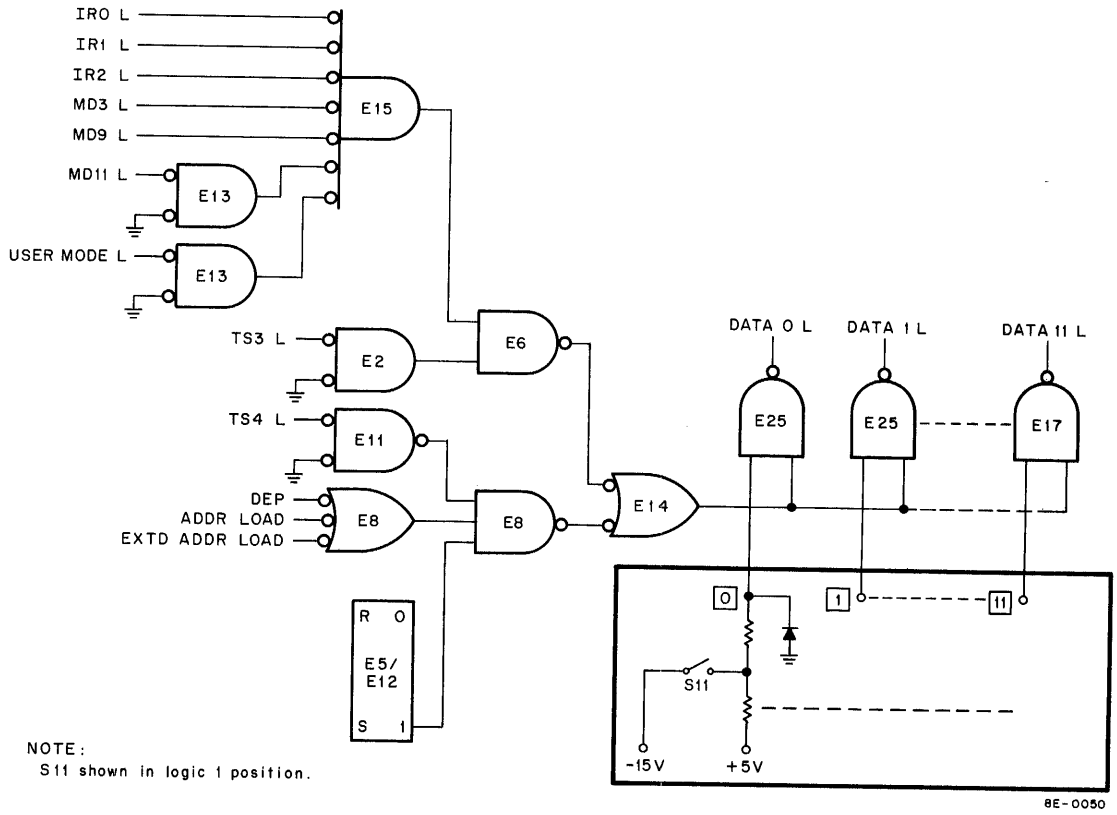


Figure 3-69 Switch Register Control Logic

applied at the other input, the DATA 0 line will go to ground, thereby indicating a logic 1. When the switch is closed, the diode in the circuit begins conducting. The resulting voltage drop across the diode takes the diode cathode below ground potential, inhibiting the NAND operation. The DATA 0 line remains at a positive voltage level, indicating a logic 0.

The NAND operation of E25 can be enabled by NOR gate E14 in either of two ways: (a) If the machine is stopped, the DEP, LOAD, or EXTD ADDR LOAD key can be activated. This action enables gate E25 and all of the other enable gates. (The DATA lines are reserved during TS4 for priority checking by peripherals; NANDing TS4 L ensures that no switch register information appears on the DATA lines during this time state.) (b) The OSR (inclusive OR, switch register with AC) instruction or the LAS (load AC with switch register) instruction can be issued, thereby enabling the gates at TS3, provided the USER MODE line has not been asserted by the KM8-E Memory Extension and Time Share option.

ADDR LOAD Key and EXTD ADDR LOAD Key – The ADDR LOAD key is used to load the CPMA Register with the memory address specified by the switch register. When the operator depresses this key, switch register information is placed on the DATA 0–11 lines. At the same time, LA ENABLE L and MS, IR DISABLE L are asserted. These two control signals enable a path for the DATA lines through the adder network to the MAJOR REGISTERS BUS. The PULSE LA signal is then asserted. This signal produces the CPMA LOAD L pulse, which loads the CPMA Register with the information on the DATA 0–11 lines. The memory location specified by the CPMA Register can then be operated on by the DEP key or the EXAM key.

Note, in Figure 3-68, that the ADDR LOAD key does not initiate a timing cycle. The purpose of this key is to establish a memory location at which some operation will take place. If a timing cycle is initiated, the CPMA address is incremented, and the operation takes place at the desired address plus 1. Thus, to avoid confusion, ADDR LOAD does not initiate a timing cycle.

The EXTD ADDR LOAD key, likewise, does not initiate a timing cycle. This key is used to load switch registers bits 6–11 into the Instruction Field (IF) and Data Field (DF) Registers of the KM8-E Memory Extension and Time Share option (bits 0–5 of the switch register are used for IOT designation and device selection code). When the operator depresses the EXTD ADDR LOAD key, the switch register information is placed on the DATA 0–11 lines. The LA ENABLE L and KEY CONTROL L signals are asserted, providing a path to the KM8-E option for the DATA 6–11 lines. The PULSE LA signal is then asserted, and the DF and IF Registers are loaded with the extended address information. The address specified by the CPMA Register and the DF and IF Registers can then be operated on by other keys.

Figure 3-70 shows the logic used by the ADDR LOAD and EXTD ADDR LOAD keys. When either key is depressed, NOR gate E14A is enabled. If the RUN L signal is negated, NAND E12A is also enabled (if RUN L is asserted, the computer is in automatic operation; E12A ensures that this operation is not inadvertently interrupted by key action). R/S flip-flop E5/E12, which is reset by INITIALIZE or by a previous TP4 pulse, is set when NAND E12B is enabled. The 1-side of the flip-flop is NANDed with positive voltage levels produced by key closure. Thus, LA ENABLE L, MS, IR DISABLE L, KEY CONTROL L, and SR → DATA are produced (note that LA ENABLE L asserts IND1 L and negates IND2 L, removing AC, MQ, or STATUS words from the DATA lines).

When NAND E12A is enabled, the block designated "pulse processor and delay network" also receives an initiating signal. This block, representing a noise filter, a differentiator, and a delay circuit, is discussed in detail in Paragraph 3.33.1.2. Essentially, the network generates a noise-free logic gate of 400 ns duration when activated. The start of the gate is delayed approximately 20 ms from the time the key is depressed, thus filtering out contact noise and allowing preliminary operations to be completed before PULSE LA is generated. The gate is NANDed with the positive voltage level that results from key closure. The amount of time that the key remains closed is indeterminate, being a result of operator action; however, it is much longer than the gate duration. Thus, PULSE LA is asserted for 400 ns.

DEP Key – If the operator wants to deposit data in a particular location of the basic 4K memory, he first loads the address into the CPMA, as described above. Then he sets the switch register switches to correspond to the data to be deposited, and lifts the DEP key. As the flow diagram in Figure 3-68 shows, the switch register data is placed on the DATA 0–11 lines. At the same time two control signals, MS, IR DISABLE L and KEY CONTROL L, are asserted. KEY CONTROL L selects the MA lines for gating into one leg of the adder network, while MS, IR DISABLE L provides an arithmetic 0 at the other adder input. KEY CONTROL L also asserts the CAR IN L signal, thus incrementing the CPMA Register. Some milliseconds later, MEM START L is asserted, the RUN flip-flop is set, and a timing cycle begins. At TP1 time the PC Register is loaded with the next consecutive memory address (note that the nonincremented address remains in the CPMA Register until TP4 of the cycle).

During TS2 of the timing cycle, the adder control signals enable a path through the adder network for the DATA 0–11 lines, adding an arithmetic 0 to each DATA bit. The switch register information is placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time. This same TP2 pulse causes the MD DIR L signal to be negated, placing the MB Register data on the MD 0–11 lines. The data is then read into the memory location specified by the content of the CPMA.

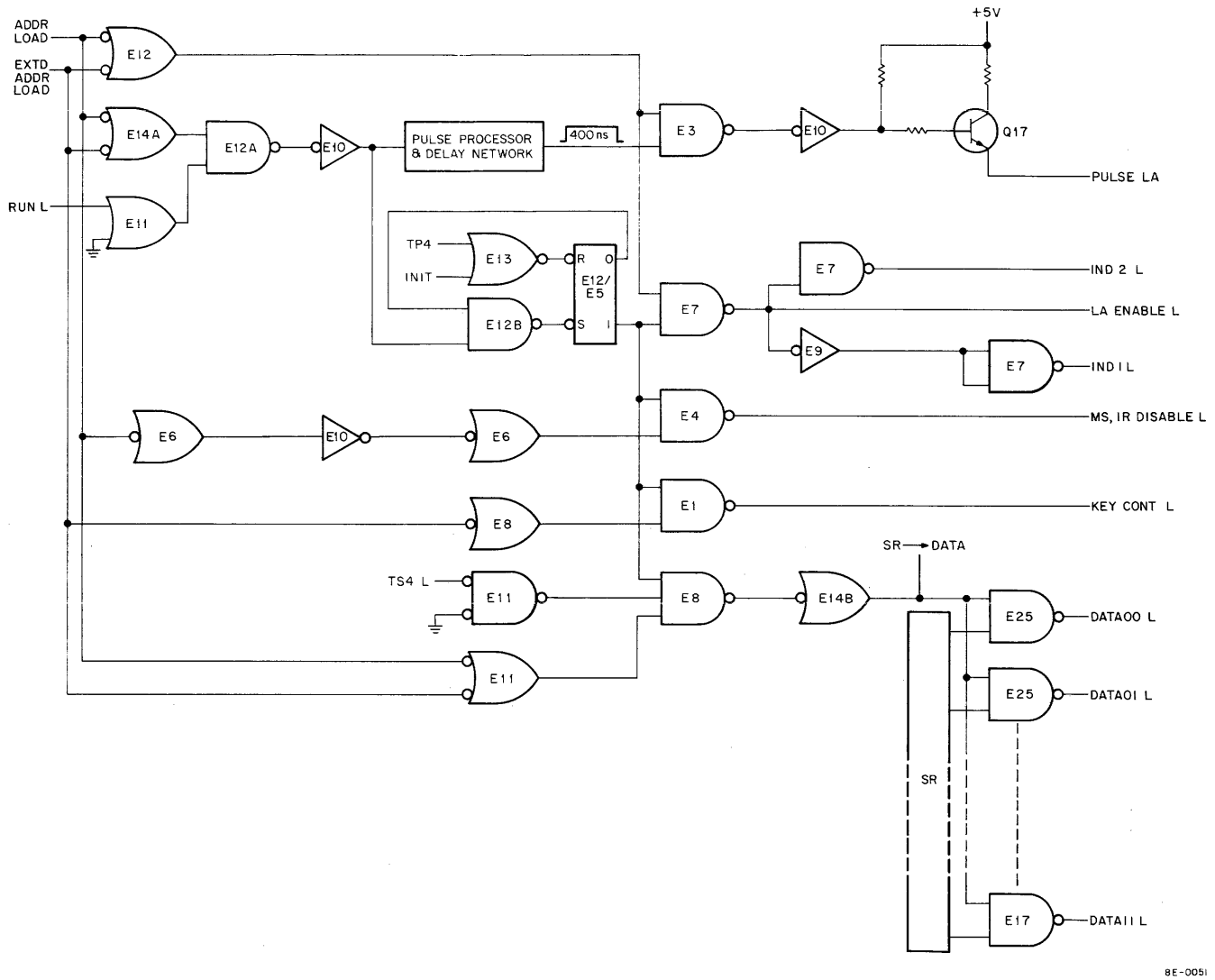


Figure 3-70 LOAD and EXTD LOAD Keys

At TP3 time, the KEY CONTROL L signal generates a STOP L signal, which resets the RUN flip-flop. The timing continues through TS4 and TP4 to halt in TS1 of some as yet unspecified cycle. Before completion of the cycle, one other operation is performed. The consecutive address must be transferred from the PC Register to the CPMA Register. Thus, the PC is gated to one leg of the adder, a 0 is added to each bit, and the new address is placed on the MAJOR REGISTERS BUS and loaded into the CPMA Register at TP4. The cycle then ends.

Figure 3-71 shows the logic used when a timing cycle is initiated by the DEP key. Again, flip-flop E5/E12 is set, provided that the RUN L signal is negated. The 1 side of E5/E12 is NANDed with positive voltage levels produced by the key closure, thereby asserting KEY CONTROL L, MS, IR DISABLE L, and SR → DATA. After the 20 ms delay, a 400 ns MEM START L signal is produced, which sets the RUN flip-flop. KEY CONTROL L enables TP3 to reset the RUN flip-flop; thus, only one cycle is produced.

EXAM Key – The EXAM key also initiates a timing cycle. By depressing this key, the operator can cause the contents of a selected memory location to be brought from memory and loaded into the MB Register. Except for the absence of SR → DATA, TS1 operations are identical to those of the DEP key. KEY CONTROL L and MS, IR DISABLE L are asserted. However, the EXAM key asserts two signals that are not needed by the DEP key and, therefore, TS2 operation is different. MD DIR L and BRK DATA CONT L are the additional signals. BRK DATA CONT L gates the MD lines to the adder network, where a 0 is added to the data being brought from the memory location. The MD bits are placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time. The operator can monitor the contents of the MD lines by selecting the MD position with the front panel function selector switch. The data in the examined location can be modified by using the switch register and the DEP key. However, the EXAM cycle increments the PC Register to set up the next sequential memory address; therefore, to modify the data in an examined location, the switch register and ADDR LOAD key must be used to return to the correct address.

Figure 3-72 shows the EXAM key logic. This logic differs from the DEP logic only in the deletion of the SR → DATA enabling gate and the addition of enabling gates for MD DIR L and BRK DATA CONT L.

CONT Key – The CONT key also initiates a timing cycle by generating MEM START L. This is an important function because this is the only key that initiates repetitive timing cycles. Thus, the operator can begin automatic operation only by depressing the CONT key. Figure 3-73 shows the logic used to implement this function.

CLEAR Key – The last key on the Programmer's Console is the CLEAR key. As the flow diagram indicates, a timing cycle is not initiated. The logic diagram, Figure 3-74, shows that this key generates a 400 ns INITIALIZE signal. This signal clears the AC, LINK, and all peripheral flags.

SING STEP Switch and HALT Switch – The PDP-8/E can be stopped manually by either the SING STEP switch or the HALT switch. The logic is shown in Figure 3-75. Either switch enables TP3 to reset the RUN flip-flop, ending the generation of timing cycles. Both switches produce the STOP L signal, which is NANDed with TP3 in the timing logic. The resulting pulse resets the RUN flip-flop. If the SING STEP switch is used, the timing cycle halts at the beginning of the next TS1. However, the HALT switch produces the STOP L signal only when F SET L is asserted. Because F SET L is asserted only when the next machine cycle is to be a FETCH cycle, the processor completes an entire instruction before halting in TS1. The operator can use these switches, with the CONT key, to step a program one cycle or one instruction at a time.

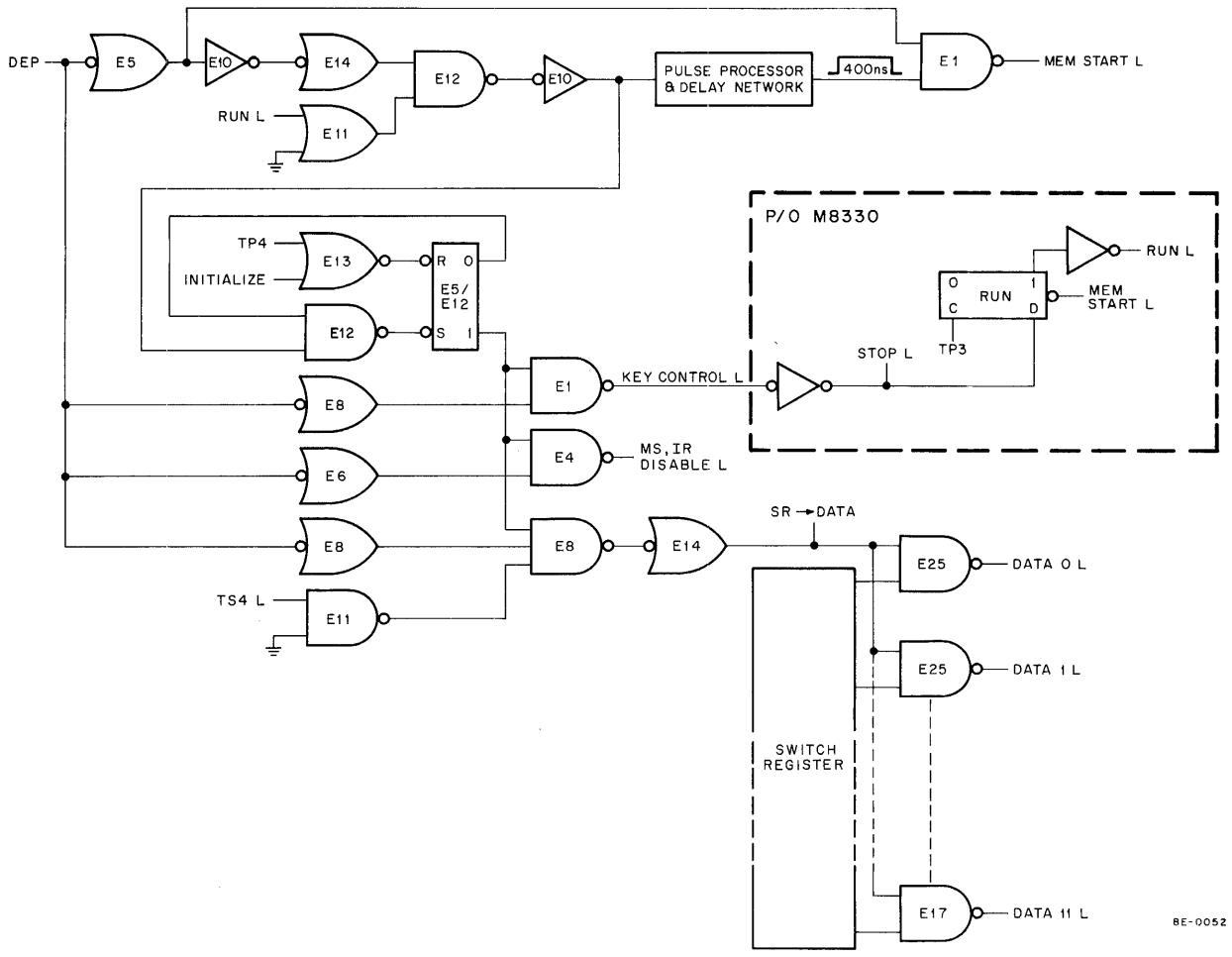


Figure 3-71 DEP Key Logic

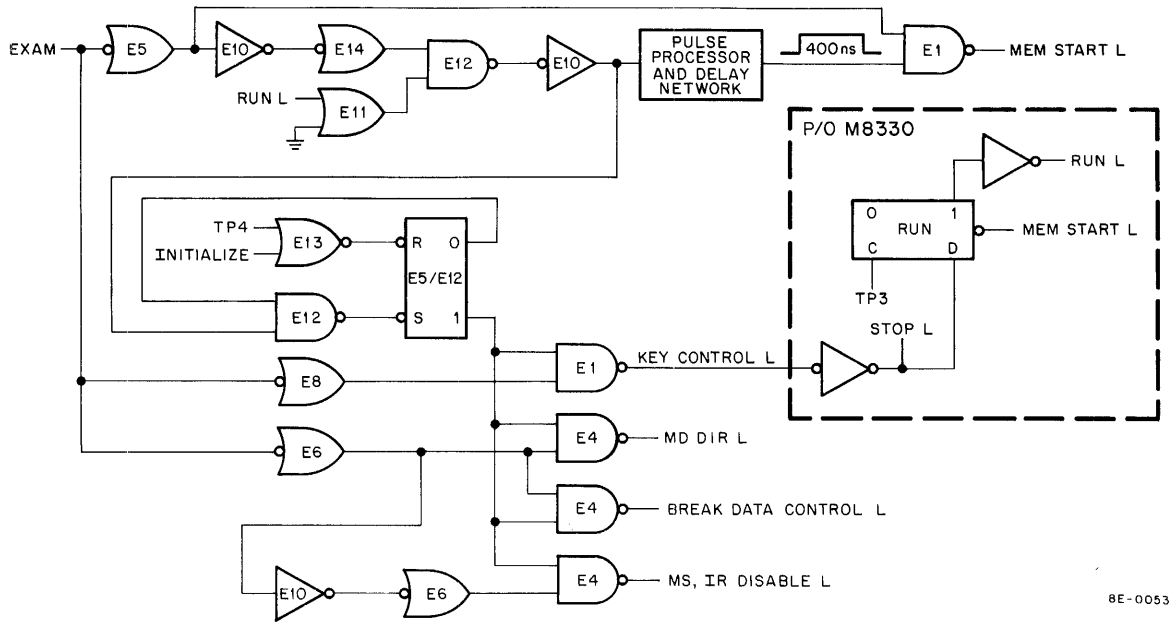


Figure 3-72 EXAM Key Logic

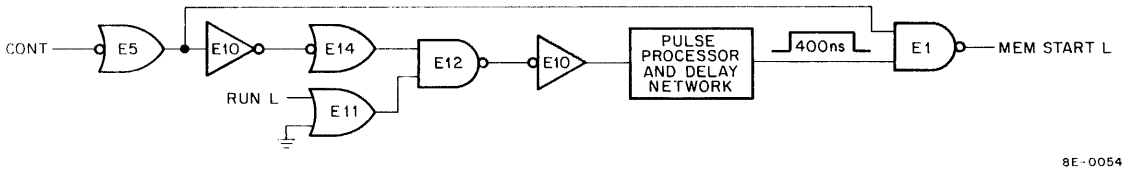


Figure 3-73 CONT Key Logic

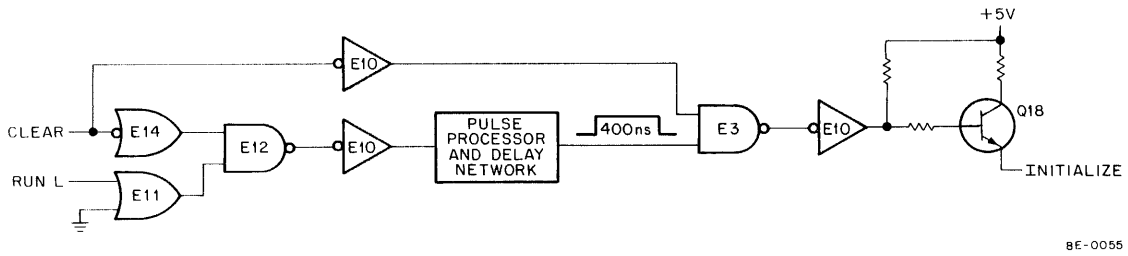


Figure 3-74 CLEAR Key Logic

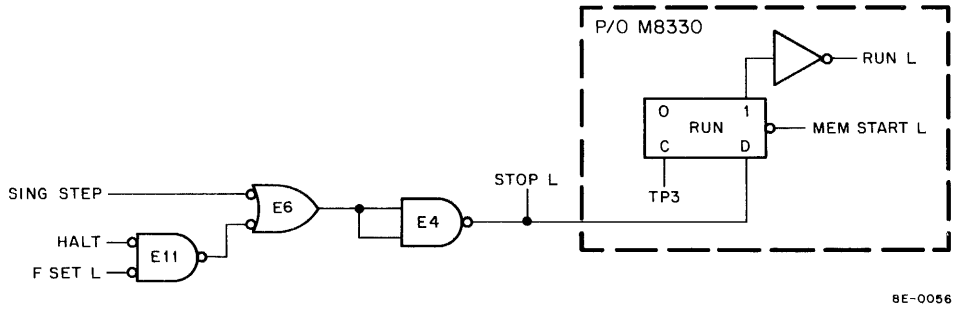
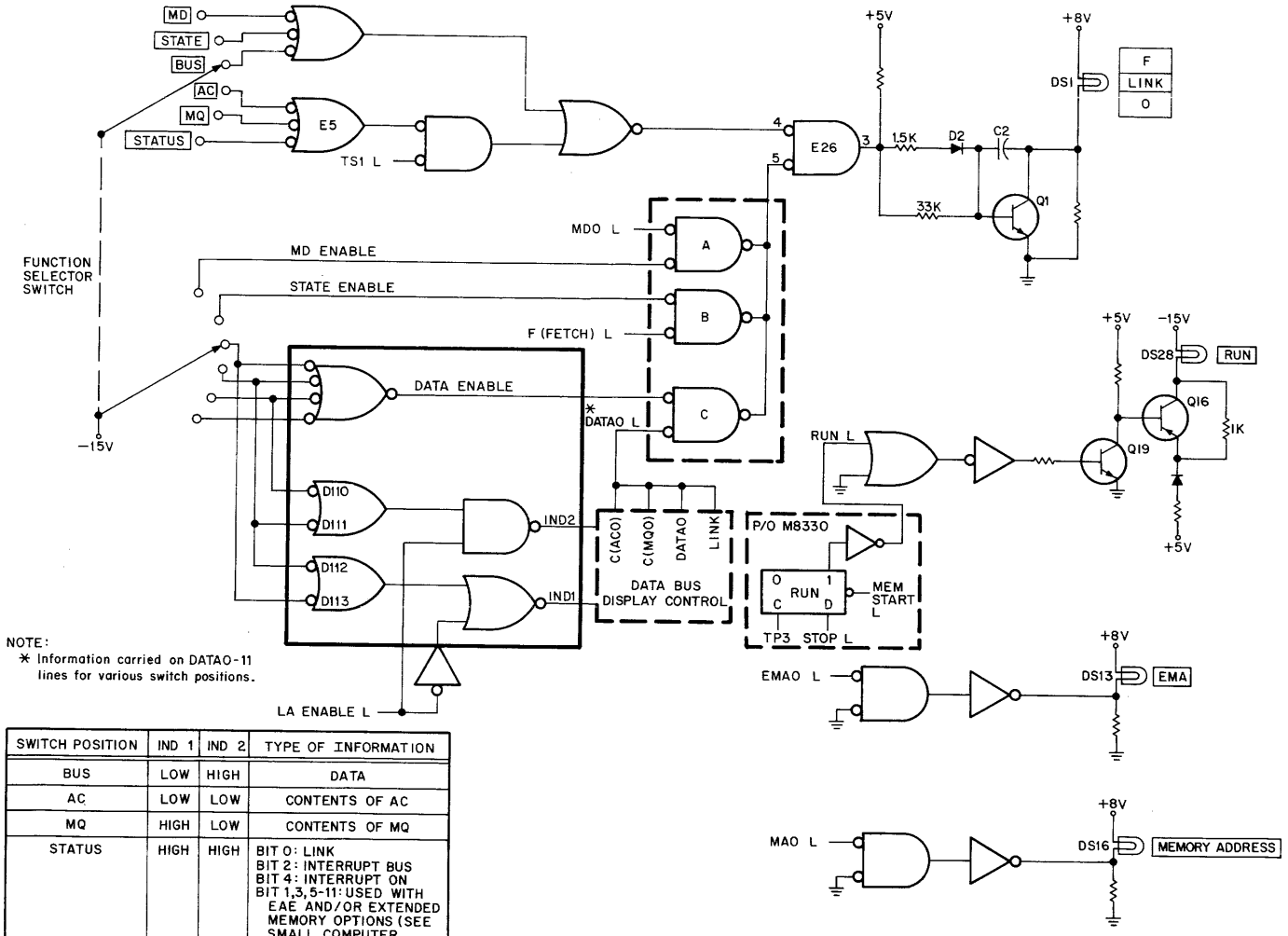


Figure 3-75 SING STEP and HALT Switch Logic

3.33.1.2 Display – The display logic and circuits are shown in Figure 3-76. There are three groups of indicator lamps and a single lamp (RUN) which, when lit, indicates that timing cycles are being generated. Each of the three groups is represented by its 0 bit, e.g., EMA0 L, MA0 L, LINK. The circuits used to display EMA and MEMORY ADDRESS are relatively simple; for example, if MA0 L is a logic 1, the NAND gate is enabled. The output of the inverter drops to a ground level. The full 8V supply voltage appears across the lamp and causes it to light. The lamp has a small voltage across it when MA0 L is a logic 0 (this condition extends the life of the lamp by eliminating the full-on/full-off cycle that often burns out lamp filaments). Consequently, it is lit at this time; however, the lamp is so dim that it is not visible from the front panel.

The circuit used to display RUN is shown above the EMA display circuit. When timing cycles are not being generated, the RUN flip-flop in the Timing Generator is cleared. Q19 and Q16 are in the nonconducting state. The conducting path for the lamp voltage includes the 1000Ω resistor; thus, a small voltage appears across DS28, causing it to be dimly lit. When RUN L is asserted by MEM START L, Q19 and Q16, in turn, are turned on. The conducting path from +5V to -15V takes the low impedance route through Q16 (from emitter to collector), rather than through the 1000Ω resistor. Thus, the RUN lamp is brightly lit, indicating that timing cycles are being generated.



SWITCH POSITION	IND 1	IND 2	TYPE OF INFORMATION
BUS	LOW	HIGH	DATA
AC	LOW	LOW	CONTENTS OF AC
MQ	HIGH	LOW	CONTENTS OF MQ
STATUS	HIGH	HIGH	BIT 0: LINK BIT 2: INTERRUPT BUS BIT 4: INTERRUPT ON BIT 1,3,5-11: USED WITH EAE AND/OR EXTENDED MEMORY OPTIONS (SEE SMALL COMPUTER HANDBOOK-1972)

Figure 3-76 Display Logic

The RUN indicator uses - 15V and +5V, rather than +8V, to operate the lamp. The +8V supply is removed from the display panel, thus extending the lamp life, when the panel is locked. The - 15V supply is not removed; thus, there is an indication of whether or not the computer is running.

The last group of indicators uses the greatest amount of the display logic and circuitry. This group reflects the data appearing on the MD 00–11 lines, the data appearing on the DATA 00–11 lines, and the state of selected registers and OMNIBUS control lines.

The type of information displayed by this group of indicators is selected at the front panel by a six-position rotary switch, labeled "Function Selector Switch" on Figure 3-76. Note that this switch produces one of three enable signals, depending on its position. If MD ENABLE is asserted, data on the MD 00–11 lines is displayed on the front panel; if STATE ENABLE is asserted, data on selected OMNIBUS signal lines is displayed; if DATA ENABLE is asserted, data on the DATA 00–11 lines is displayed.

If the operator wants to monitor the information on the MD lines, he selects the MD position of the rotary switch. This action asserts MD ENABLE, which is ANDed with MD0 L (the actual circuits within this dashed line are presented in a following paragraph of this section). If MD0 L is a logic 1, the AND gate brings pin 5 of NAND gate E26 to a virtual ground. Because pin 4 is also at ground, E26 is enabled, and pin 3 goes to +5V. Transistor Q1 turns on rapidly because its base drive is supplied through the low-impedance diode path. The switching action of Q1 places a ground on its collector; thus, approximately 8V appear across DS1, causing it to be brightly lit. When E26 is again disabled, pin 3 goes to ground, and diode D2 is reversed-biased. Capacitor C2 begins to discharge through the 33 kΩ resistor. This long RC time constant ensures that Q1 turns off slowly, increasing the visibility of DS1.

If the operator wants to monitor the content of the AC Register, he selects the AC position; the DATA ENABLE signal is then asserted. In addition, NOR gates D110/D111 and D112/D113 are enabled (the actual circuit within this solid line is presented in a following paragraph). When these gates are enabled, both IND1 and IND2 are asserted, provided that LA ENABLE L is not asserted. These control lines cause the content of the AC Register to be placed on the DATA 00–11 lines. If DATA 0 is a logic 1, E26, pin 5 is grounded; pin 4 is also grounded, but only during TS1, and the content of DATA 0 is displayed on DS1.

Similarly, the content of the MQ Register, STATUS information, and BUS data can be displayed. The relationship between IND1/IND2 and the type of information displayed is indicated on Figure 3-76. Figure 3-77 shows the logic used to generate control signals in response to IND1 and IND2. This logic is contained within the block designated DATA BUS DISPLAY CONTROL in Figure 3-76.

Figure 3-78 shows the circuit represented by AND gate C, enclosed within the dashed line in Figure 3-76 (gate C was arbitrarily selected for discussion; the following can apply to gates A and B, if the signal names and component designations are changed accordingly). Both the DATA ENABLE line and the DATA 0 line must be asserted if pin 5 of E26 is to be true (logic 1, or 0V). If the DATA ENABLE line is not asserted, it is at +5V. The junction of diodes D61 and D36 is +5V; neither diode conducts current; thus, pin 5 is +5V. When the DATA ENABLE line is asserted, both diodes can conduct current. If the DATA 0 line is negated (at 3V), the diode junction goes to approximately 2.3V. Pin 5 then goes to 3V, and E26 remains disabled. When DATA 0 becomes true (0V), the junction goes to -0.7V, pin 5 goes to ground, and E26 is enabled.

Figure 3-79 shows the circuit represented by the logic gates and enclosed within the solid line in Figure 3-76. Each of the four switch positions asserts DATA ENABLE by switching the DATA ENABLE line to - 15V through a diode. Thus, the line, when asserted, is at approximately - 14V.

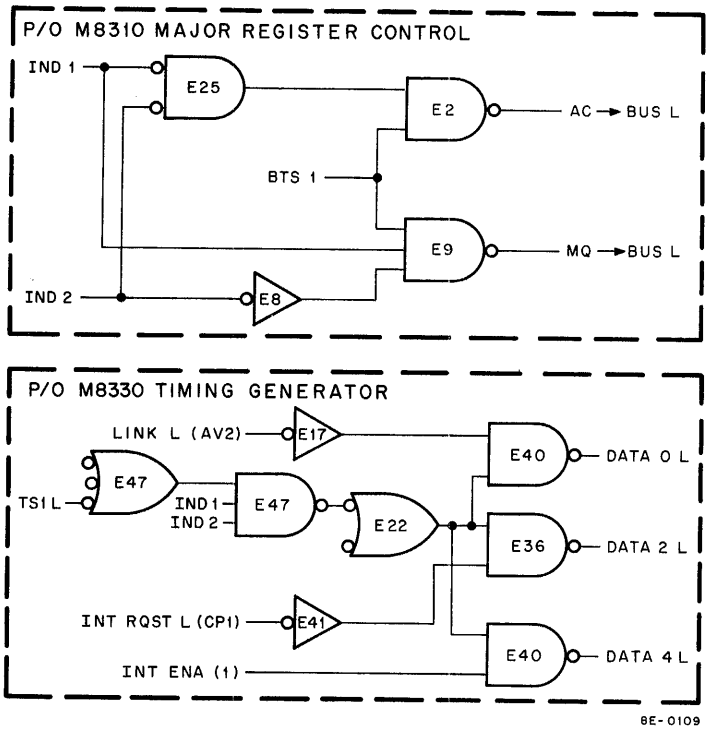


Figure 3-77 Data Bus Display Control Signals

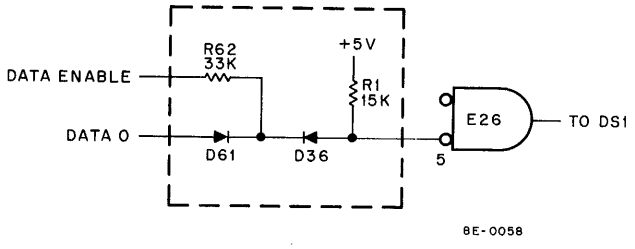


Figure 3-78 Enable Circuit

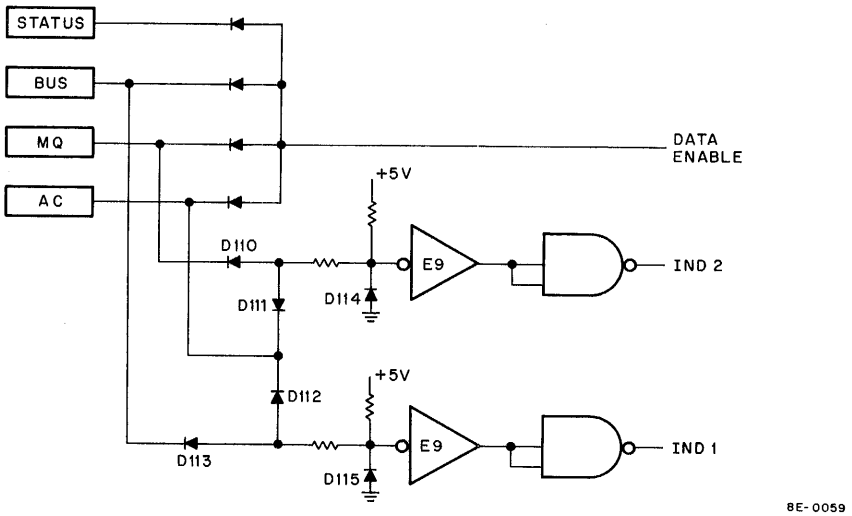


Figure 3-79 DATA ENABLE/IND SELECT

Only STATUS asserts DATA ENABLE without affecting either the IND1 or IND2 control lines. Each of the remaining three positions causes one or both of these control lines to be asserted. For example, if BUS is selected, the junction of diodes D113 and D112 goes to approximately -14V. D115 has a conduction path and, thus, clamps the input of E9 at -0.7V. The resulting positive voltage at the output of E9 enables the following NAND gate to assert IND1. If neither D112 nor D113 conducts, D115 remains in the nonconducting state. The input to E9 remains at +5V, and IND1 is negated.

The pulse processor and delay network is shown in Figure 3-80. The input to the network, from inverter E10, is a positive-going level that results from closure of a front panel key. The output from the network is a noise-free, 400 ns gate that is used to assert either MEM START L, PULSE LA, or INITIALIZE.

When a front panel key, EXAM, is depressed, the resulting negative-going edge at the input to inverter E10 may appear as shown in Figure 3-80; i.e., noise spikes appear because of contact bounce. The integrator at the output of E10 is designed to remove the noise spikes. The large capacitance is unresponsive to noise, and, therefore, smooths the edge, while also greatly increasing its rise time. The integrating action, along with the shaping and filtering accomplished by the three transistors, which comprise a Schmitt trigger, produces a positive transition at the collector of Q15. This transition is delayed approximately 20 ms from the negative transition at the input of E10.

The differentiator converts the transition to a positive spike, which triggers a one-shot. This spike is inverted by NOR gate E2; the leading edge of the negative spike is coupled through the 330 pF capacitor and enables NAND gate E2. Simultaneously, the leading edge enables a charging path for the capacitor. This path is sustained by bringing the NAND gate output back to keep the NOR gate enabled. The capacitor charges toward +5V on a long time constant, keeping the NAND gate enabled for approximately 400 ns. When the capacitor has charged to a voltage sufficiently high to disable NAND gate E2, the charging path is removed. Thus, the output of E2 is a 400 ns positive gate and, in this instance, asserts MEM START L for that length of time.

3.33.2 KC8-FL Programmer's Console

3.33.2.1 Manual Operation

Switch Register – The switch register comprises 12 switches that allow the operator to load the CPMA Register with a 12-bit memory address; to load the extended address bits, if more than 4K of memory is used; to deposit a 12-bit data word in a selected memory location; and to change the content of the AC Register. To carry out these functions, the switch register is operated in conjunction with the DEP, ADDR LOAD, and EXTD ADDR LOAD keys (Figure 3-67).

Figure 3-81 illustrates the logic used to set data into the switch register and to place it on the DATA 0–11 lines. The operator selectively closes switches S11 through S22 (designated "0" through "11", respectively, on the front panel). He then causes NOR gate E20 to assert SR → DATA; this signal gates the information represented by the switch register keys onto the DATA lines.

There are three ways for the operator to assert SR → DATA. If he wants to load the CPMA Register, he depresses ADDR LOAD, causing NAND gate E13A to be enabled. (The signals designated A0 L, A1 L, A2 L, and E4 (1) are enable signals that are selectively generated when the operating keys are activated; these signals are described in the *Operating Keys* section.) If he wants to load the extended address bits, he depresses EXTD ADDR LOAD, again causing E13A to be enabled. If he wants to deposit data in a memory location, he raises the DEP key, causing NAND gate E9C to be enabled during TS2 (a variety of information must be carried by the DATA lines;

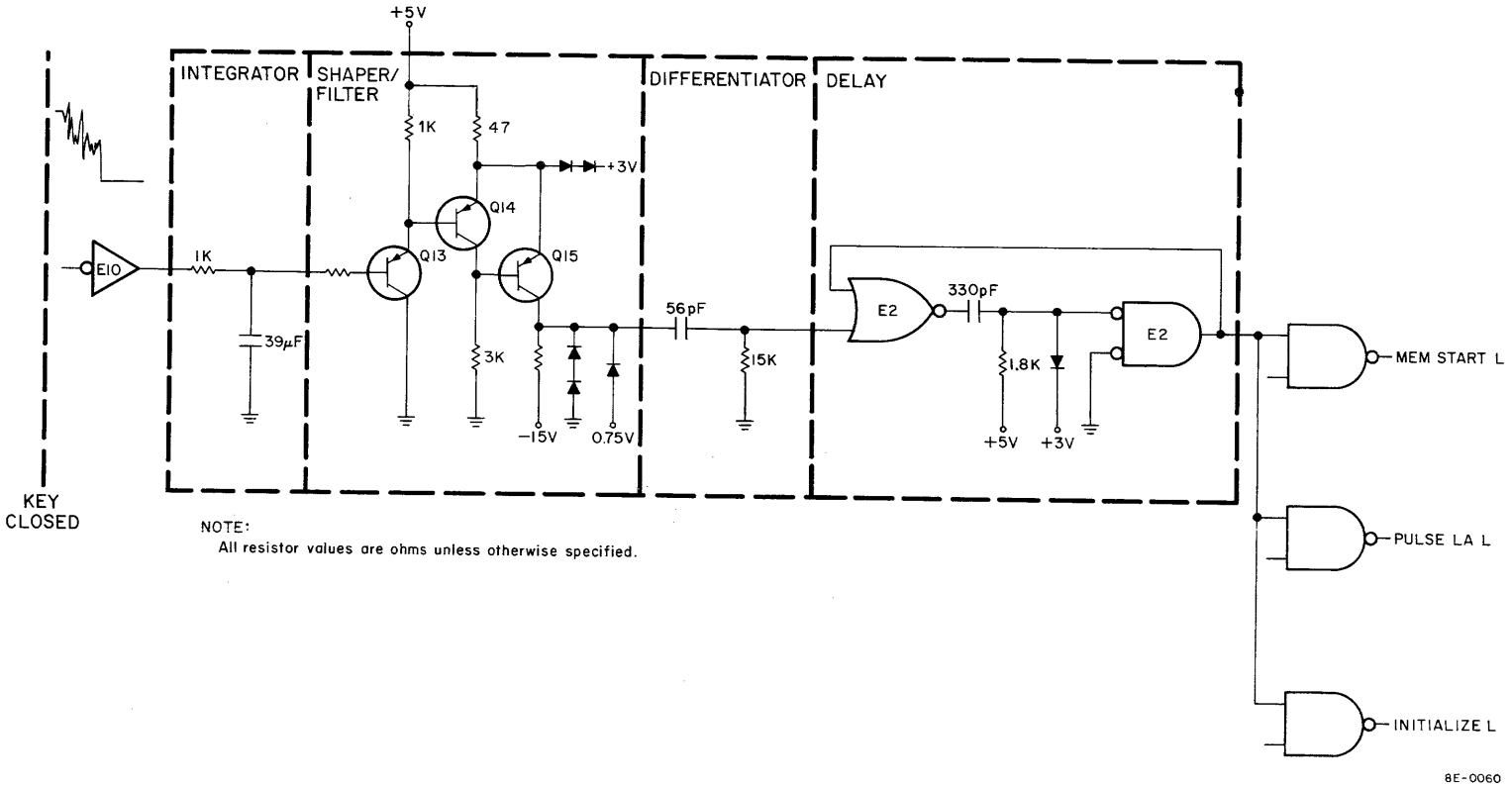


Figure 3-80 Pulse Processor and Delay Network, Schematic

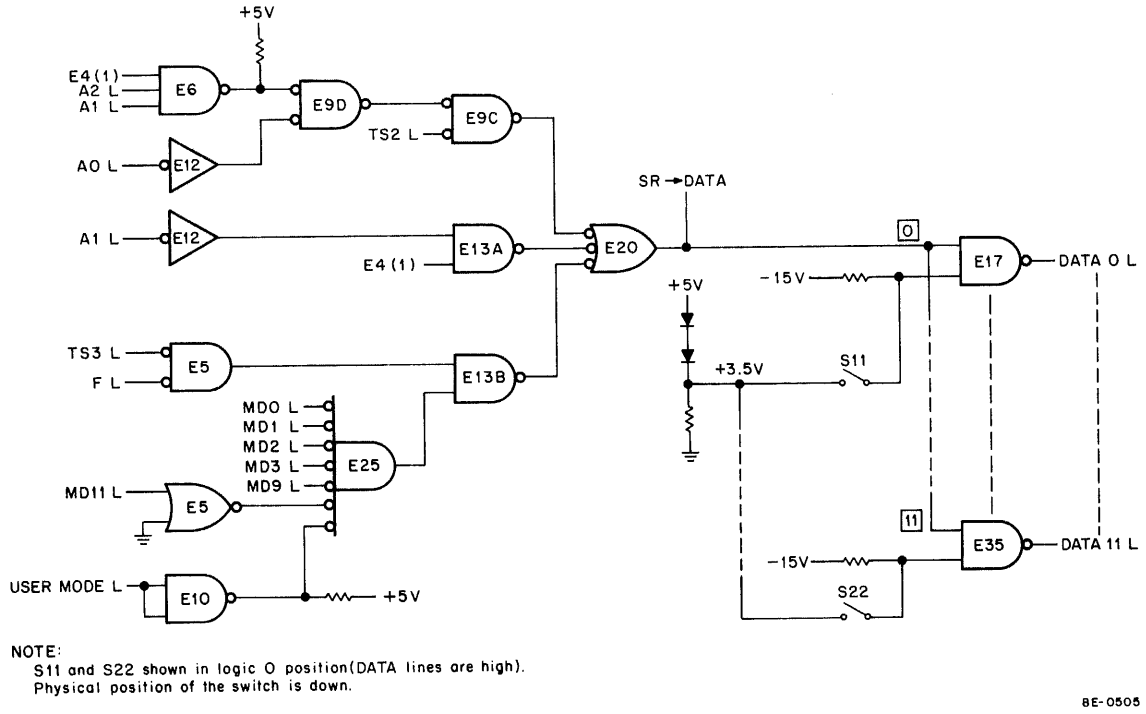
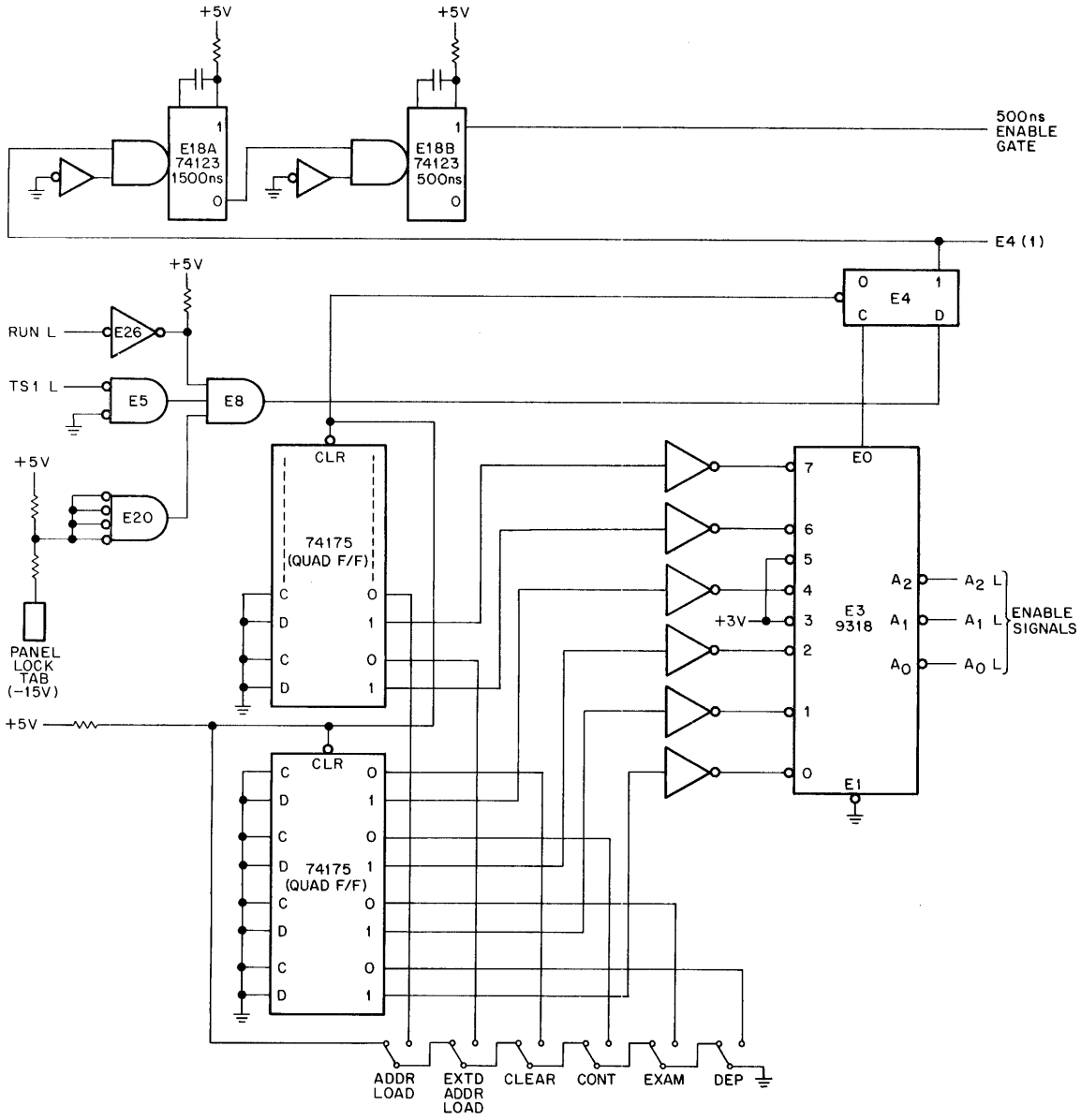


Figure 3-81 Switch Register Control Logic

time sharing of the lines must be employed to maintain the identity of each type of information). Finally, if the operator wants to change the content of the AC Register under program control, he can program either the OSR instruction (inclusive OR, switch register with AC) or the LAS instruction (load AC with switch register). Either instruction causes gate E25 to be enabled, provided USER MODE L is not asserted by the KM8-E option. When NAND gate E5 is enabled during TS3, E13B is enabled, in turn, and the SR → DATA signal is asserted. NANDing the F L signal in gate E5 ensures that E13B is not enabled during the DEFER or EXECUTE cycle of a multicycle instruction.

Operating Keys – The operating keys selectively generate enable signals when they are activated. The enable signals, in turn, selectively assert control signals that cause the processor to carry out the intended key function (all but one of the control signals, SR → DATA, are on the OMNIBUS). The logic used to generate the enable signals is shown in Figure 3-82.

Each key controls one of the D-type flip-flops of a DEC 74175 quad flip-flop IC. The normally open contact of each key is connected to the 0 output of a flip-flop. When a key is activated, the ground placed on the 0 output of the associated flip-flop forces the flip-flop to the set state. The 1 output is applied through an inverter to a DEC 9318 8-input priority encoder. Each input of the encoder is assigned a value from 0 to 7. When an input line is activated, the 9318 encoder provides a binary representation on the active low outputs A0, A1, and A2 (A0 is the LSB). At the same time, the 9318 active high output, EO, goes high, clocking flip-flop E4. If the computer is stopped (power is on but timing has not been initiated), the RUN L signal is high and the D input of E4 is high. Thus, E4 is set and the E4 (1) signal is asserted (if the front panel OFF/POWER/PANEL LOCK switch is in the PANEL LOCK position, the -15V supply voltage is removed from the panel lock tab, and NAND gate E8 cannot be enabled; this effectively disables the operating keys and switches and prevents manual operation of the switch register). The E4 (1) signal triggers 1-shot E18A; 1500 ns later the 500 ns enable gate is generated when E18B is triggered.



7	6	5	4	3	2	1	0	E0	A_2	A_1	A_0	KEY
H	H	H	H	H	H	H	H	L	H	H	H	—
L	X	X	X	X	X	X	X	H	L	L	L	ADDR LOAD
H	L	X	X	X	X	X	X	H	L	L	H	EXTD ADDR LOAD
H	H	H	L	X	X	X	X	H	L	H	H	CLEAR
H	H	H	H	H	L	X	X	H	H	L	H	CONT
H	H	H	H	H	H	L	X	H	H	H	L	EXAM
H	H	H	H	H	H	H	L	H	H	H	H	DEP

H = High voltage level
L = Low voltage level
X = Dont care

8E-0506

Figure 3-82 Operating Keys, Enable Signal Logic

The table in Figure 3-82 relates the keys and the 9318 inputs and outputs. The table reflects the dominant feature of the 9318 priority encoder, viz., if two or more inputs are simultaneously active, the input with the highest priority is represented by the binary output. Input 7 is assigned highest priority; thus, the ADDR LOAD key takes precedence over all other keys. If the operator depresses the ADDR LOAD key, for example, the 9318 IC asserts the A0 L, A1 L, A2 L, and EO signals. Until this key is released, no other key can affect the enable signals. When the key is released, the 74175 CLR input is returned to ground, clearing the flip-flop that was set by the ADDR LOAD key. Now, the flip-flop associated with a key of lower priority causes the 9318 output to change. Note that flip-flop E4 is also cleared when a key is released. Thus, the enable signals and, as a result, the control signals are asserted only as long as the operator depresses a key. Manual operation with the KC8-FL is, therefore, as fast as the operator can make it.

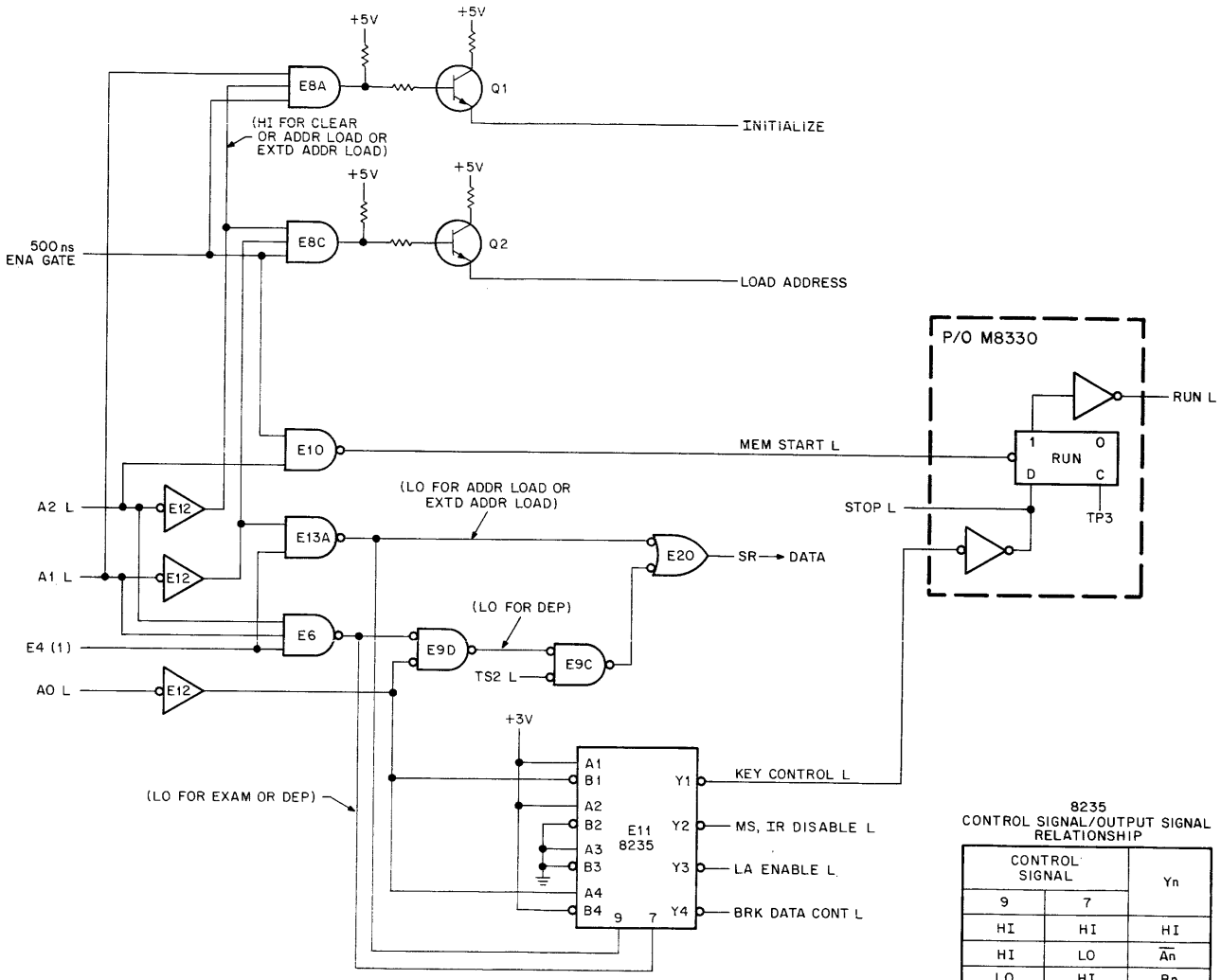
The logic used to generate the control signals is shown in Figure 3-83. The gating of the logic in response to the enable signals is not discussed; this task is left to the reader. Table 3-4, which will facilitate this task, relates the control signals, the enable signals, and the keys. The state of each of the control inputs of the 8235 IC is also tabulated. A functional description of each of the keys follows. Refer to the flow diagram, the logic diagrams, and the tables while reading the functional descriptions.

ADDR LOAD Key and EXTD ADDR LOAD Key – The ADDR LOAD key is used to load the CPMA Register with the memory address specified by the switch register. When the operator depresses this key, switch register information is placed on the DATA 0–11 lines. At the same time, LA ENABLE L and MS, IR DISABLE L are asserted. These two control signals enable a path for the DATA lines through the adder network to the MAJOR REGISTERS BUS. The LOAD ADDRESS signal is then asserted. This signal produces the CPMA LOAD L pulse, which loads the CPMA Register with the information on the DATA 0–11 lines. The memory location specified by the CPMA Register can now be operated on by the DEP key or the EXAM key.

Note that the ADDR LOAD key does not initiate a timing cycle. The purpose of this key is to establish a memory location at which some operation will take place. If a timing cycle were to be initiated, the CPMA address would be incremented, and the operation would take place at the desired address, plus 1. Therefore, to avoid confusion, ADDR LOAD does not initiate a timing cycle.

The EXTD ADDR LOAD key, likewise, does not initiate a timing cycle. This key is used to load switch register bits 6–11 into the Instruction Field (IF) and Data Field (DF) Registers of the KM8-E Memory Extension and Time Share option (bits 0–5 of the switch register are used for IOT designation and device selection code). When the operator depresses the EXTD ADDR LOAD key, the switch register information is placed on the DATA 0–11 lines. The LA ENABLE L and KEY CONTROL L signals are asserted, providing a path to the KM8-E option for the DATA 6–11 lines. The LOAD ADDRESS signal is then asserted and the DF and IF Registers are loaded with the extended address information. The address specified by the CPMA Register and the DF and IF Registers can now be operated on by other keys.

DEP Key – The DEP key is used to deposit the data represented by the switch register in a specified memory location. When the DEP key is lifted, two control signals, MS, IR DISABLE L and KEY CONTROL L, are asserted. KEY CONTROL L selects the MA lines for gating into one leg of the adder network, while MS, IR DISABLE L provides an arithmetic 0 at the other adder input. KEY CONTROL L also asserts a processor signal that increments the CPMA Register. 1500 ns later, the MEM START L signal is asserted, the RUN flip-flop is set, and a timing cycle begins. At TP1 time the PC Register is loaded with the next consecutive memory address (note that the nonincremented address remains in the CPMA Register until TP4 time of the cycle).



8235
CONTROL SIGNAL/OUTPUT SIGNAL RELATIONSHIP

CONTROL SIGNAL		Yn
9	7	
HI	HI	HI
HI	LO	$\overline{An}$
LO	HI	Bn

8E-0507

Figure 3-83 Operating Keys, Control Signal Logic

Table 3-4
KC8-FL CONTROL/ENABLE Signals

Key	ENABLE Signals					E11		CONTROL Signals
	A0 L	A1 L	A2 L	E4 (1)	500 ns ENA Gate	9	7	
ADDR LOAD	LO	LO	LO	HI	HI	LO	HI	LOAD ADDRESS, SR → DATA, MS, IR DISABLE L, LA ENABLE L
EXTD ADDR LOAD	HI	LO	LO	HI	HI	LO	HI	LOAD ADDRESS, SR → DATA, MS, IR DISABLE L, LA ENABLE L, KEY CONTROL L
CLEAR	HI	HI	LO	HI	HI	HI	HI	INITIALIZE
CONT	HI	LO	HI	HI	HI	HI	HI	MEM START L
EXAM	LO	HI	HI	HI	HI	HI	LO	MEM START L, KEY CONTROL L, MS, IR DISABLE L, BRK DATA CONT L
DEP	HI	HI	HI	HI	HI	HI	LO	MEM START L, KEY CONTROL L, MS, IR DISABLE L, SR → DATA

During TS2 of the timing cycle, the switch register data is gated onto the DATA 0–11 lines and the adder control signals enable a path through the adder network, adding an arithmetic 0 to each DATA bit. The switch register information is placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time. At the same time, the MD DIR L signal is negated causing the content of the MB Register to be placed on the MD 0–11 lines. The data is then read into the memory location specified by the content of the CPMA Register.

At TP3 time the RUN flip-flop is reset (the STOP L signal is asserted when KEY CONTROL L is generated). The timing continues through TS4 and TP4 to halt in TS1 of some as yet unspecified cycle. Before the cycle is completed, one other operation is performed. The next consecutive address must be transferred from the PC Register to the CPMA Register. Therefore, the information in the PC Register is gated to one leg of the adder, and a 0 is added to each bit; the new address is placed on the MAJOR REGISTERS BUS and loaded into the CPMA Register at TP4 time. The cycle then ends.

EXAM Key – The EXAM key also initiates a timing cycle. By depressing this key the operator causes the content of a selected memory location to be brought from memory and loaded into the MB Register. Except for the absence of the SR → DATA signal, the TS1 operations are the same for the EXAM key as for the DEP key. The MS, IR DISABLE L, KEY CONTROL L, and MEM START L signals are asserted and function as described. However, the EXAM key also causes the BRK DATA CONT L signal to be asserted; this signal causes the TS2 operations to differ from those of the DEP key.

The BRK DATA CONT L signal gates the MD lines to the adder network, where a 0 is added to the data being brought from the memory location. The MD bits are placed on the MAJOR REGISTERS BUS and loaded into the MB Register at TP2 time (at the same time, the MD DIR L signal is negated, causing the register content to be again placed on the MD lines; thus, the content of the memory location can be re-written during the write half of the timing cycle). The operator can view the content of the MB Register by selecting the MD position on the front panel function selector switch. The operator can modify the data in the examined location by using the switch register and the DEP key. However, the EXAM cycle increments the PC Register to set up the next sequential memory address; therefore, to modify the data in the examined location, the switch register and ADDR LOAD key must be used to get back to the correct address.

CONT Key – The CONT key initiates a timing cycle by causing the MEM START L signal to be asserted. This is an important function because this is the *only* key that initiates repetitive timing cycles. Thus, the operator can begin automatic operation only by depressing the CONT key.

CLEAR Key – The CLEAR key generates the INITIALIZE signal. This signal clears the AC Register, the LINK, the Interrupt system, all peripheral flags, and various flip-flops within the basic system.

SING STEP Switch and HALT Switch – The operator can stop the PDP-8/E by closing either the SING STEP or the HALT switch. The logic is shown in Figure 3-84. If the SING STEP switch is used, the STOP L signal is generated and the first TP3 pulse clears the RUN flip-flop. The RUN L signal is negated, and the machine stops at the beginning of the next TS1 period. If the HALT switch is used, the STOP L signal is generated only when the F SET L signal is asserted. Because F SET L is asserted only when the next timing cycle is to be a FETCH cycle, the processor completes an entire instruction before halting in TS1. The operator can use these two switches and the CONT key to step a program one cycle or one instruction at a time.

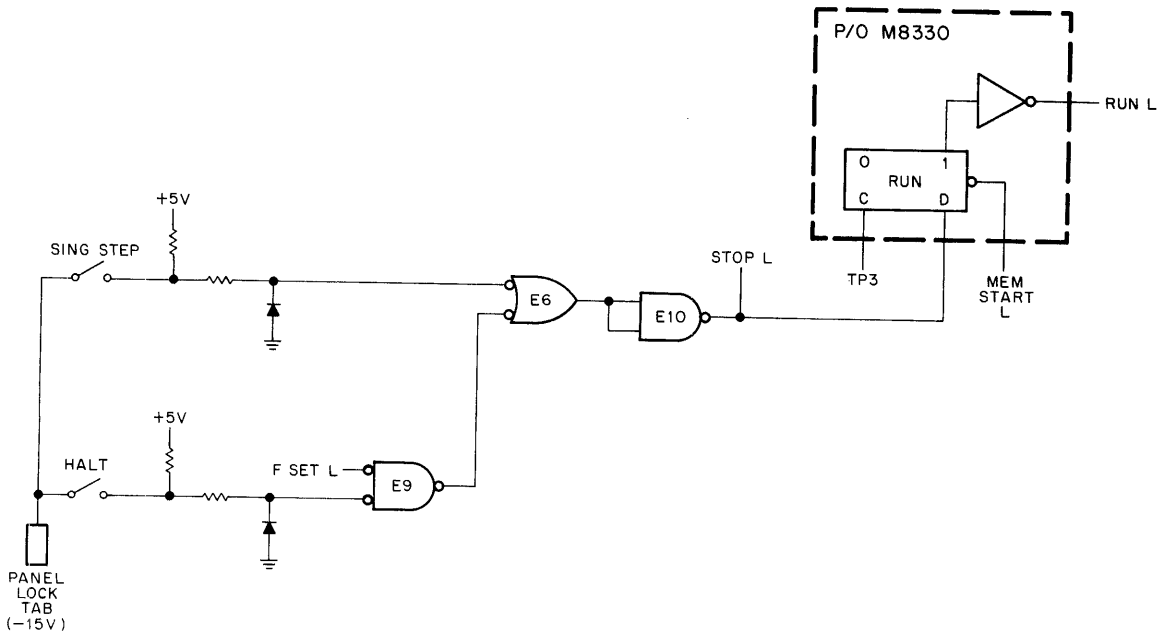


Figure 3-84 SING STEP and HALT Switches

3.33.2.2 Display – The KC8-FL Programmer's Console uses solid-state devices rather than filament-type lamps to indicate the state of various PDP-8/F (PDP-8/M) major registers and OMNIBUS signals. These indicators, light-emitting diodes (LEDs), are more durable than lamps and help to promote maintenance-free operation. LEDs differ from incandescent lamps in another important way. As the name implies, LEDs are diodes. Consequently, they exhibit the usual nearly constant forward voltage when conducting. A series resistor to define the forward current through the diode is necessary. In the KC8-FL, the resistor value of 330Ω establishes the LED on-current at about 10 mA. At currents of less than 500 μA, the diode does not emit detectable amounts of light.

A single indicator, designated RUN, emits light when timing cycles are being generated. The light from this and all other indicators, is visible on the front panel (Figure 1-1). The other indicators are divided into two groups. One group, comprising 15 LEDs, displays the current memory address. This group is represented by the designations MEMORY ADDRESS and EMA. The other group, comprising 12 LEDs, displays the contents of selected registers and important OMNIBUS signals. A front panel switch enables the operator to select the register or type of OMNIBUS signal that he wishes displayed.

The display logic is represented in Figure 3-85. The RUN indicator is shown in the lower right of the figure. When the timing generator logic (M8330) asserts the RUN L signal, LED D35 emits light, indicating that the computer is running (power is on and timing cycles are being generated).

The two groups of indicators are represented by the 0 bit logic. For example, a complete 15-bit memory address has two 0 bits, EMA0 and MA0. Both bits are shown in the logic. When either the EMA0 L signal or the MA0 L signal is asserted, the +V voltage appears across the corresponding LED and its current determining resistor, causing it to light. The +V voltage, approximately +4.5V, is taken from the circuit that includes Q3 and Q4. When the front panel OFF/POWER/PANEL LOCK switch is in the PANEL LOCK position, the -15V supply is removed from the panel lock tab, thereby removing the +V voltage. Consequently, only the RUN indicator is lit with the switch in this position.

The majority of the logic in Figure 3-85 is used with the group of indicators that displays OMNIBUS signals and major register contents. Again, only the 0 bit logic is represented. The type of information displayed is selected on the front panel by a 6-position rotary switch, labeled S1 in Figure 3-85. This switch causes one of three signals to be asserted, depending on its position: in the MD position, MD IND is asserted; in the STATE position, STATE IND is asserted; in all other positions, DATA IND is asserted.

If the operator wants to monitor the MD lines, he switches to the MD position, causing the MD IND signal to be asserted. This signal is ANDed with the MD0 L signal in AND/NOR gate E15. The three other AND gates of E15 are disabled when S1 is in the MD position. If the MD0 L signal is asserted, E15 is disabled. Therefore, the output of inverter E22 is low. The +V voltage appears across LED D23, causing it to emit light that is visible on the front panel. The same analysis can be repeated for the F L signal when S1 is in the STATE position. However, the logic gating is more complicated when any of the other four switch positions is selected. The reason for this is that the four different types of signals must be carried on only the DATA lines; furthermore, remember that the DATA lines are time-shared and display information has access to these lines only during TS1.

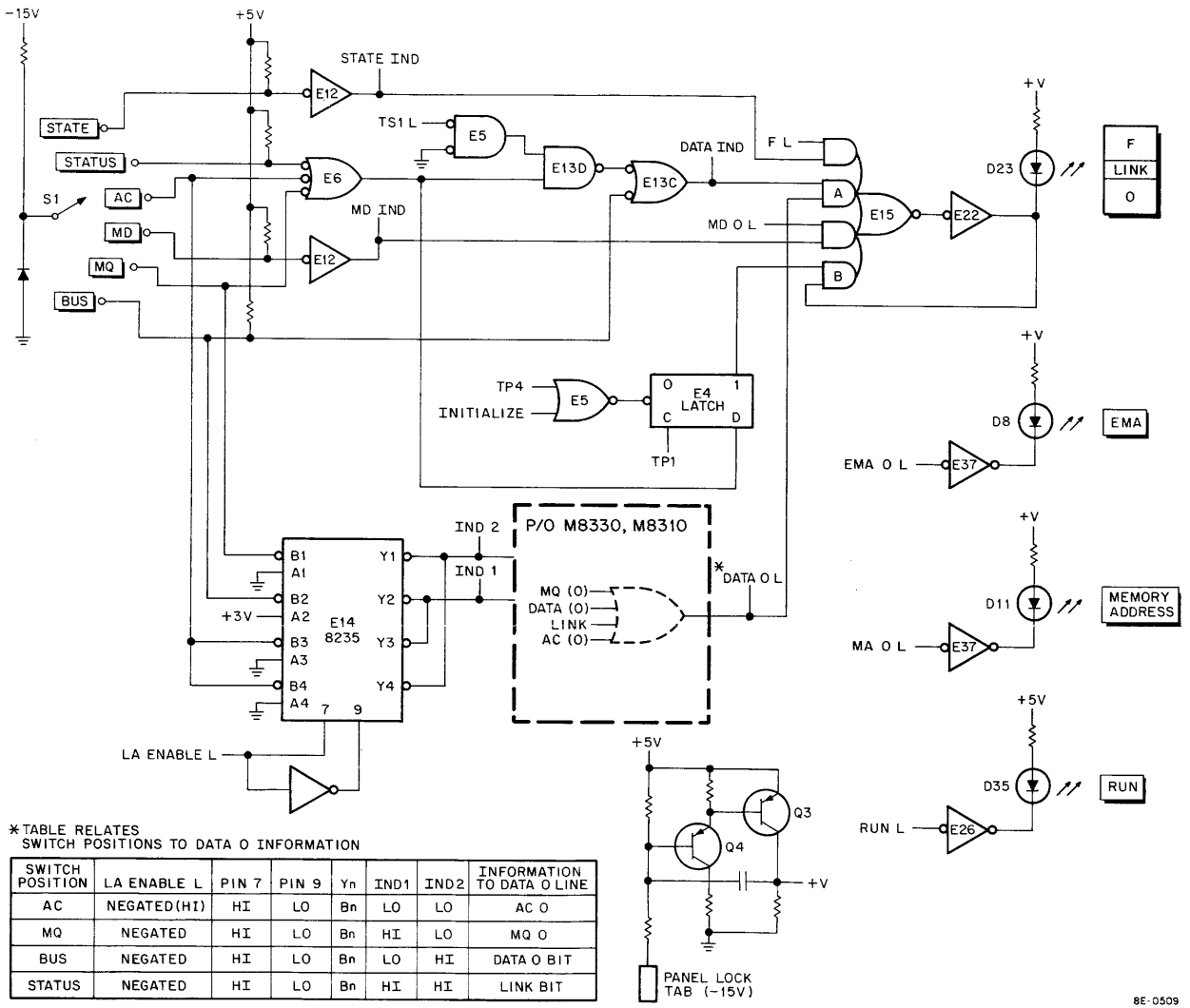


*TABLE RELATES SWITCH POSITIONS TO DATA O INFORMATION

SWITCH POSITION	LA ENABLE L	PIN 7	PIN 9	Yn	IND1	IND2	INFORMATION TO DATA O LINE
AC	NEGATED(HI)	HI	LO	Bn	LO	LO	AC O
MQ	NEGATED	HI	LO	Bn	HI	LO	MQ O
BUS	NEGATED	HI	LO	Bn	LO	HI	DATA O BIT
STATUS	NEGATED	HI	LO	Bn	HI	HI	LINK BIT

Figure 3-85 Display Logic

Assume that the operator positions S1 at AC. The DATA IND signal is asserted during TS1. The AC0 bit must be gated to the DATA 0 line so that its state can be displayed. The table in Figure 3-85 shows that when the AC position is selected, the 8235 IC takes both IND1 and IND2 low. This combination of IND1 and IND2 causes the logic within the broken line (the actual logic is shown in Figure 3-86) to assert the AC → BUS L signal. Thus, the AC0 bit is gated to the DATA 0 line. If the AC0 bit is logic 1, AND gate A of E15 is disabled, the output of E15 stays high, and D23 emits light.

If the AC0 bit is logic 0, the LATCH flip-flop performs an important function. To illustrate, assume that the operator, while stepping the computer through a series of timing cycles (with the SINGLE STEP switch closed), causes a TAD instruction to be executed. The computer stops in TS1 of the cycle following the TAD instruction. The operator wants to check the result and switches to the AC position. D23 indicates logic 0. When the CONT key is depressed, AND gate A of E15 is disabled as soon as TS2 of the new timing cycle is entered. Therefore, if AND gate B and the LATCH flip-flop were not present, D23 would emit light for most of the timing cycle following the TAD execute cycle. Instead, the LATCH flip-flop is set at TP1 time (the D-input is high when the AC position is selected). The 1 output of the flip-flop and the high at the output of E22 keep E15 enabled; D23 remains dark throughout the timing cycle. At TP1 time the LATCH flip-flop is cleared.

Similarly, the content of the MQ Register, STATUS information, and BUS data can be displayed. The relationship between IND1/IND2 and the type of information displayed is indicated on Figure 3-85. Figure 3-86 shows the logic used to generate control signals in response to IND1 and IND2.

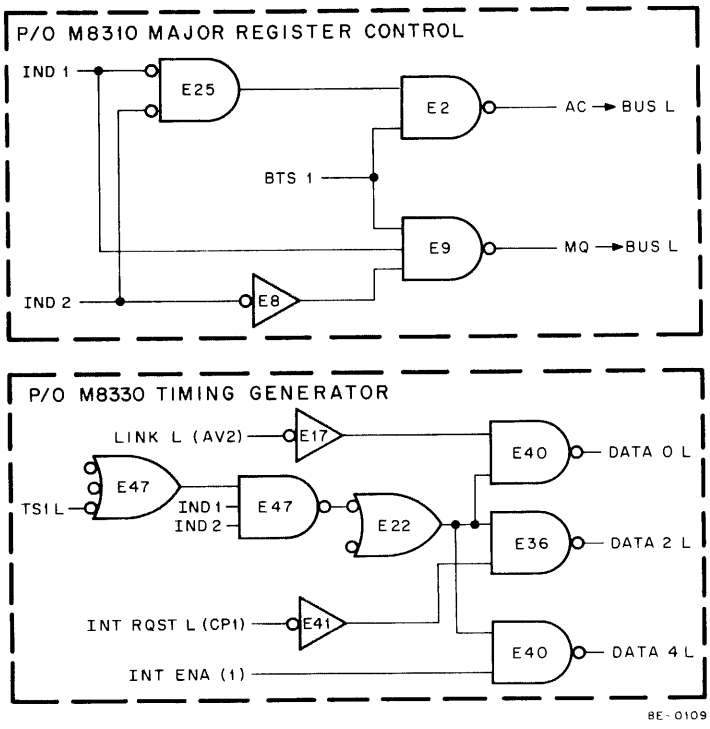


Figure 3-86 Data Bus Display Control Signals