CHAPTER 8
DB8-E INTERPROCESSOR BUFFER

SECTION 1 INTRODUCTION

The DB8-E Interprocessor Buffer is designed to plug directly into the PDP-8/E OMNIBUS. This option allows two PDP-8/E Computers to transfer data between themselves, one 12-bit word at a time, at a software-limited rate of 50 kHz. The DB8-E can also be used to transfer data to user-designed logic on single-ended data lines.

The basic DB8-E option has one M8326 Module and one BC08-R cable (up to 100-ft long). The DB8-EB has one M8326 Module, two BC08-R cables, and two 5409209 Module Adapters for connection to user-designed logic.

Device codes on the module are jumper-selected between 50 and 57, allowing a maximum of eight Interprocessor Buffers to be used in one PDP-8/E.

SECTION 2 INSTALLATION

The DB8-E Interprocessor Buffer is installed on site by DEC Field Service personnel. The customer should **not** attempt to unpack, inspect, install, checkout, or service the equipment.

8.1 INSTALLATION

To install the Interprocessor Buffer, remove power from PDP-8/E No. 1 and insert the M8326 Module into the OMNIBUS. Refer to Table 2-3, Volume 1, for information about recommended module priorities (the DB8-E is a non-memory option). Remove power from PDP-8/E No. 2 and insert the second M8326 Module into its OMNIBUS. Connect one of the BC08-R cables between J1 of the first and J2 of the second DB8-E Module. Connect the second BC08-R cable between J2 of the first DB8-E and J1 of the second DB8-E. This will connect the output of PDP-8/E No. 1 buffer to the input of PDP-8/E No. 2 module and the output of PDP-8/E No. 2 to the input of PDP-8/E No. 1. Table 8-1 shows the pin-to-pin connections of J1 and J2.

Table 8-1
Connection from J1 to J2

J1 Pin No.	Adapter Module Pins	J2 Pin No.	Adapter Module Pins
J1TT	A1	J2C	V2
J1RR	B1	J2E	U2
J1D	V1	J2SS	A2
J1F	U1	J2PP	B2
J1J	T1	J2MM	C2

Table 8-1 (Cont)
Connection from J1 to J2

J1 Pin No.	Adapter Module Pins	J2 Pin No.	Adapter Module Pins
J1L	S1	J2KK	D2
J1N	R1	J2HH	E2
J1R	T1	J2EE	F2
J1T	N1	J2CC	H2
J1V	M1	J2AA	J2
J1X	L1	J2Y	K2
J1Z	K1	J2W	L2
J1BB	J1	J2U	M2
J1DD	H1	J2S	N2

NOTE: All pins not listed are tied to ground.

8.2 ACCEPTANCE TEST

The acceptance test should be performed when the DB8-E Modules are installed and periodically after installation to check the operation of the DB8-E logic. A working M8326 Test Module is needed to perform this test. The programs in Section 5 can be used for preliminary operational checks.

Perform the following steps to check the DB8-E Modules installed in the PDP-8/E OMNIBUS.

NOTE
The PDP-8/E under test will be referred to as PDP-8/E
No. 1; the PDP-8/E with test module used to check the
DB8-E Module in PDP-8/E No. 1 will be referred to as
PDP-8/E No. 2.

Step	Procedure
1	Remove the DB8-E Module from PDP-8/E No. 2 and install the test module in its place; connect the cables from the DB8-E Module to the test module.
2	Load binary loader in PDP-8/E No. 1 and No. 2.
3	Load diagnostic MAINDEC-8E-DOPA-PB in PDP-8/E No. 1 and No. 2.
4	Run Part 1 and Part 2 of the test for 5 minutes each. There should be no errors.
5	If there are no errors, remove the test module from PDP-8/E No. 2 and reinstall the DB8-E Module.
6	To check the DB8-E Module in PDP-8/E No. 2, repeat Steps 1 through 5 with test module in PDP-8/E No. 1.

SECTION 3 SYSTEM DESCRIPTION

The Interprocessor Buffer (Figure 8-1) receives or transmits data under control of programmed instructions from the CPU. Data can be put on the DATA BUS of the OMNIBUS to be transferred to the accumulator, or data can be taken from the DATA BUS and transferred to another PDP-8/E or user's equipment.

The following instructions are used to program interprocessor data transfers.

Skip on Receive Flag (DBRF)

Octal Code: 65X1
Operation: Skip if the RECEIVE FLAG equals one.

Read Incoming Data (DBRD)

Octal Code: 65X2
Operation: Read the incoming data into the AC, clear the RECEIVE FLAG, and set DONE flip-flop.

Skip on Transmit Flag (DBTF)

Octal Code: 65X3
Operation: Skip if the DONE FLAG equals one.

Transmit Data (DBTD)

Octal Code: 65X4
Operation: Transfer the contents of the AC Register to the transmit buffer. Transmit data and set the FLAG.

Enable Interrupt (DBEI)

Octal Code: 65X5
Operation: Enable the interrupt request line.

Disable Interrupt (DBDI)

Octal Code: 65X6
Operation: Disable the interrupt line.

Clear Done Flag (DBCD)

Octal Code: 65X7
Operation: Clear the DONE FLAG.

To transfer data from PDP-8/E No. 1 to PDP-8/E No. 2, data is loaded into the AC of PDP-8/E No. 1 and transferred to the output buffer of its DB8-E using the 65X4 IOT. In addition to loading the output buffer, IOT 65X4 also sets the FLAG flip-flop in PDP-8/E No. 2. When the program in PDP-8/E No. 2 has sensed its FLAG flip-flop, data is gated into the AC of PDP-8/E No. 2 using IOT 65X2. IOT 65X2 then sets the DONE flip-flop of PDP-8/E No. 1, indicating the transfer was completed, and clears the FLAG flip-flop of PDP-8/E No. 2. PDP-8/E No. 1 then clears its DONE flip-flop using IOT 6507.

SECTION 4 DETAILED LOGIC

The logic in the Interprocessor Buffer will be broken into functional groups for discussion purposes. Figure 8-1 should be used to understand the relationship between each group of logic.

8.3 DEVICE SELECT LOGIC

The device select logic is shown in Figure 8-2. Bits MD03 through MD11 are gated by I/O PAUSE when a 65XX instruction is decoded. An INT I/O L and SELECT L will be asserted to allow the operation decoder to receive its input and to cause the positive I/O bus interface to ignore the IOT instruction.
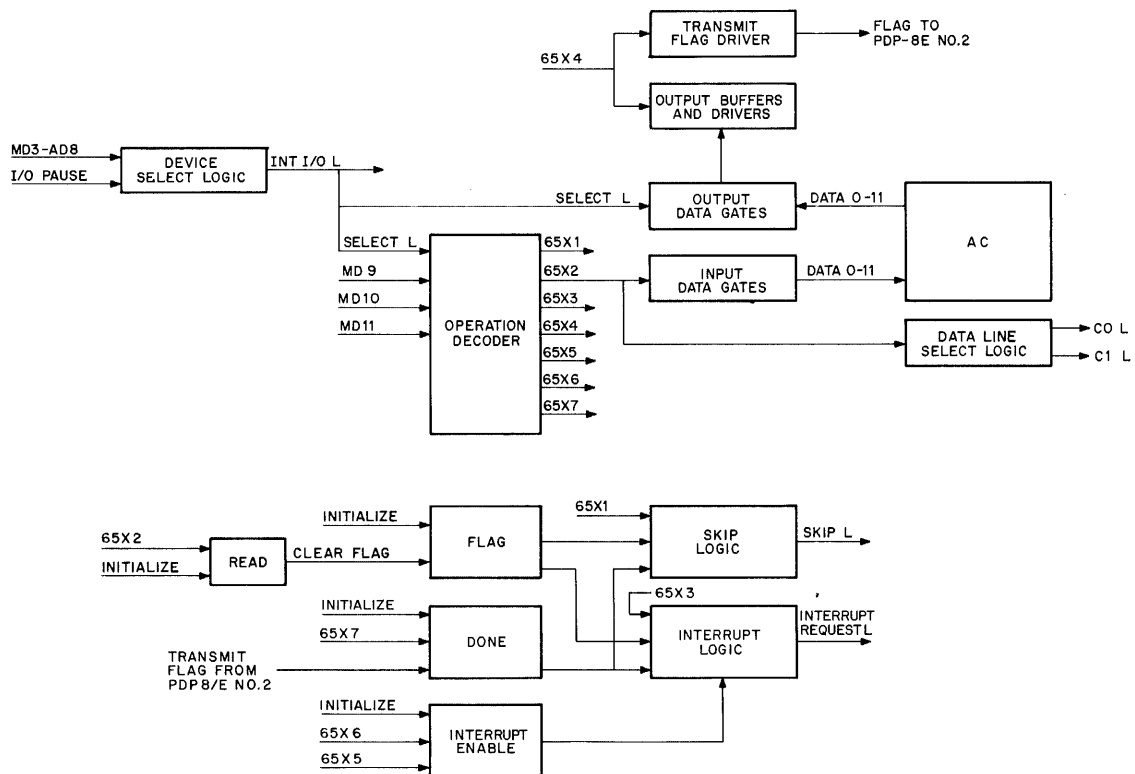
8.4 OPERATION SELECT LOGIC

SELECT L in Figure 8-3 will enable the gates for bits MD09 through MD11 and allow inputs to the operation decoder which is a BCD-to-decimal decoder. (Refer to Appendix A, Volume 1, for details about the 8251 IC.) The decoder will supply signals that represent instructions 65X1 through 65X7. When a 65X2 instruction is decoded, the C line select logic will pull C0 and C1 low to allow data to be transferred from the DATA BUS to the AC.
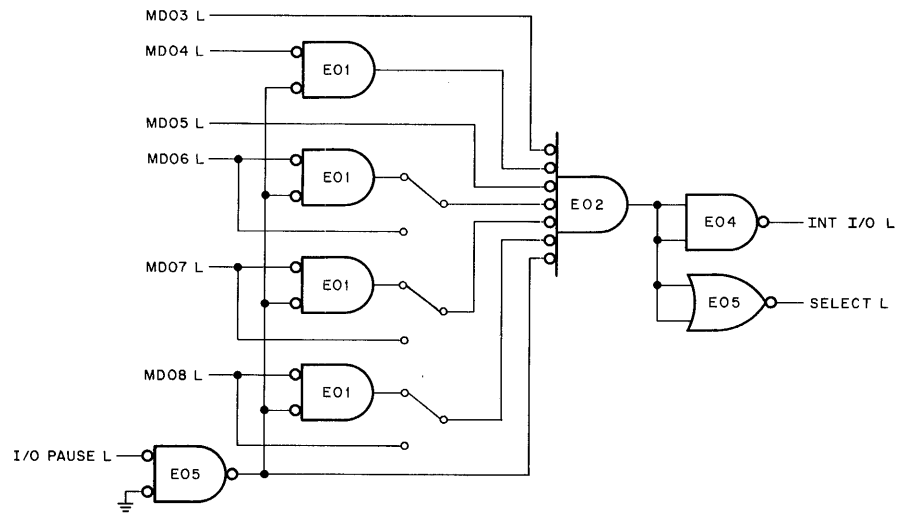
8.5 INTERRUPT AND SKIP LOGIC

The interrupt and skip logic is used to interrupt the program when a data transfer is required. To allow an interrupt to occur, the INT ENA flip-flop must be set (Figure 8-4) by a 65X6 instruction. The 1-output of the INT ENA flip-flop will go to E17 and assert one side of the AND gates allowing them to generate INT RQST L. A more detailed explanation of interrupt and skip logic can be found in Volume 1.

Table 8-2 shows the signal and data flow required to transfer information between two PDP-8/E Computers.
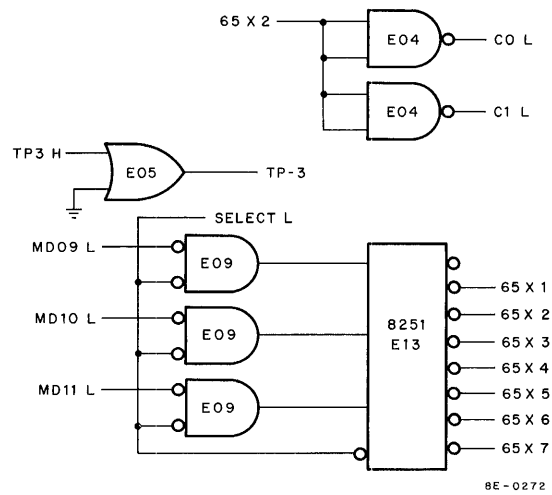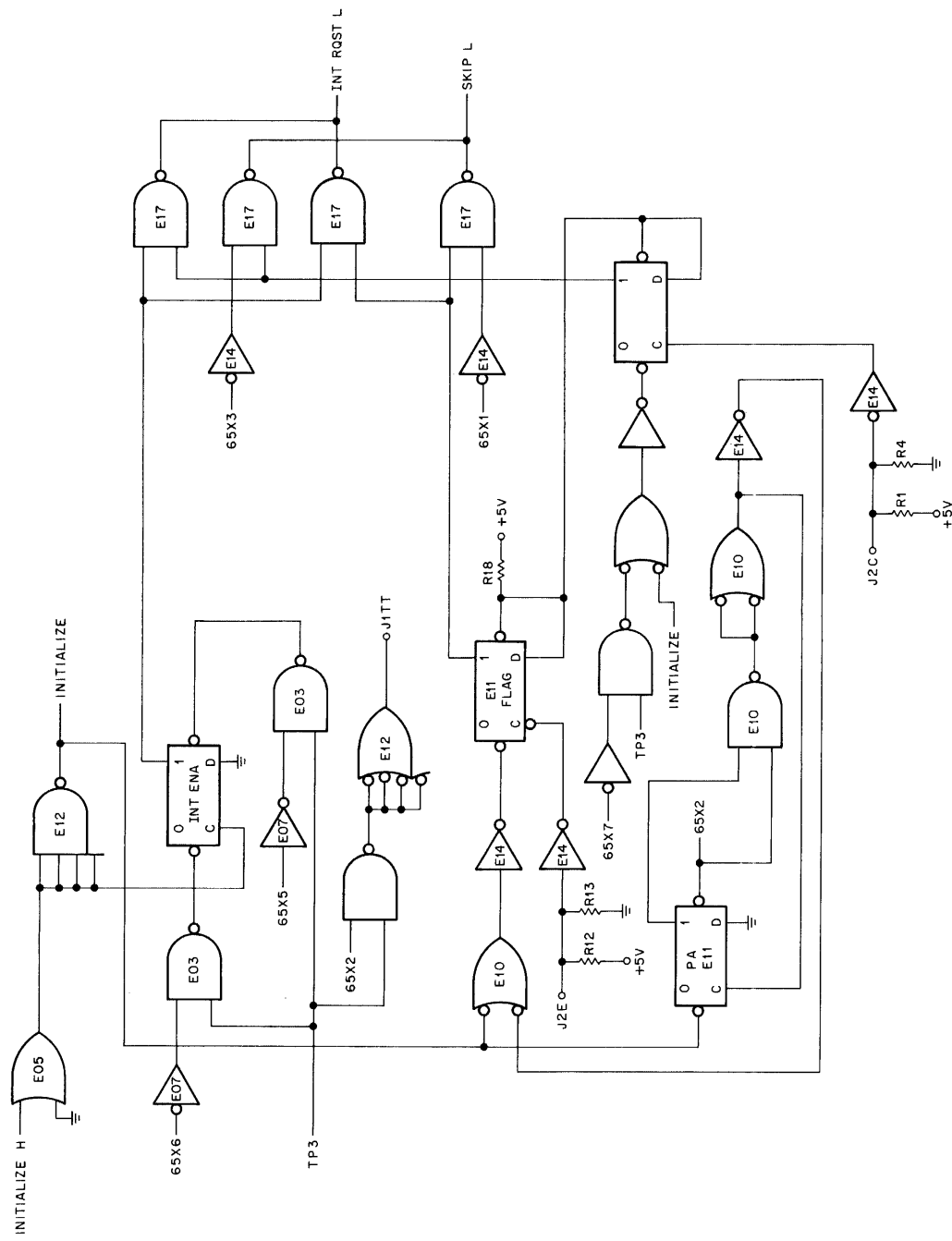

Figure 8-1 Interprocessor Buffer, Block Diagram

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Figure 8-2   Device Select Logic

Figure 8-3   Operation Select Logic

Figure 8-4 Interrupt and Skip Logic

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8.6 INPUT DATA GATES AND OUTPUT BUFFERS

The input data gates (Figure 8-5) will be enabled by a 65X2 instruction and transfer data to the AC via the DATA BUS.

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Table 8-2

Simultaneous Receive and Transmit Operation by

Two PDP-8/E Computers Using Interprocessor Buffer

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PDP-8/E No. 1 Data Transmitter	PDP-8/E No. 2 Data Receiver
Data is transferred from AC to the DATA BUS and applied to the data inputs of buffer flip-flops by programmed instructions.	
A 6504 instruction clocks the buffer flip-flops and transmits information to PDP-8/E No. 2 and simultaneously sends a signal from J1RR of PDP-8/E No. 1 to J2E of PDP-8/E No. 2.	Data is received and FLAG is set by signal at J2E. INT RQST if ENA is set, and SKIP generated and subroutine to read data is started.
The trailing edge of the signal at J2C sets the DONE flip-flop to indicate PDP-8/E No. 2 has read data.	6502 instruction gates data to DATA BUS. TP3 and 6502 instruction enable signal to J1TT to be transmitted to J2C of PDP-8/E No. 1.
Signal is removed from J2C when 6502 signal is removed from gate in PDP-8/E No. 2.	The Flag is cleared by trailing edge of 6502 instruction.
DONE is cleared by 6507 instruction.	
PDP-8/E No. 1 is ready to transmit or receive data.	PDP-8/E No. 2 is ready to receive or transmit data.

The SELECT L signal applied to the output data gates will allow 1s to be transferred from the DATA BUS to the data input side of flip-flops in the output buffer. When a 65X4 instruction is generated, the clock input of the flip-flop will be pulsed and the data will be transferred to the input gates of PDP-8/E No. 2. This instruction will also cause J1RR to go high and set the FLAG in PDP-8/E No. 2. The data transferred from the Interprocessor Buffer is +3V for true (1) signals and 0.0V for false (0) signals.

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SECTION 5 MAINTENANCE

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Refer to Volume 1 for maintenance information about PDP-8/E Computers. The acceptance test given in Section 2 should be performed when an error is suspected in the DB8-E.

8.7 DATA TRANSFER TEST

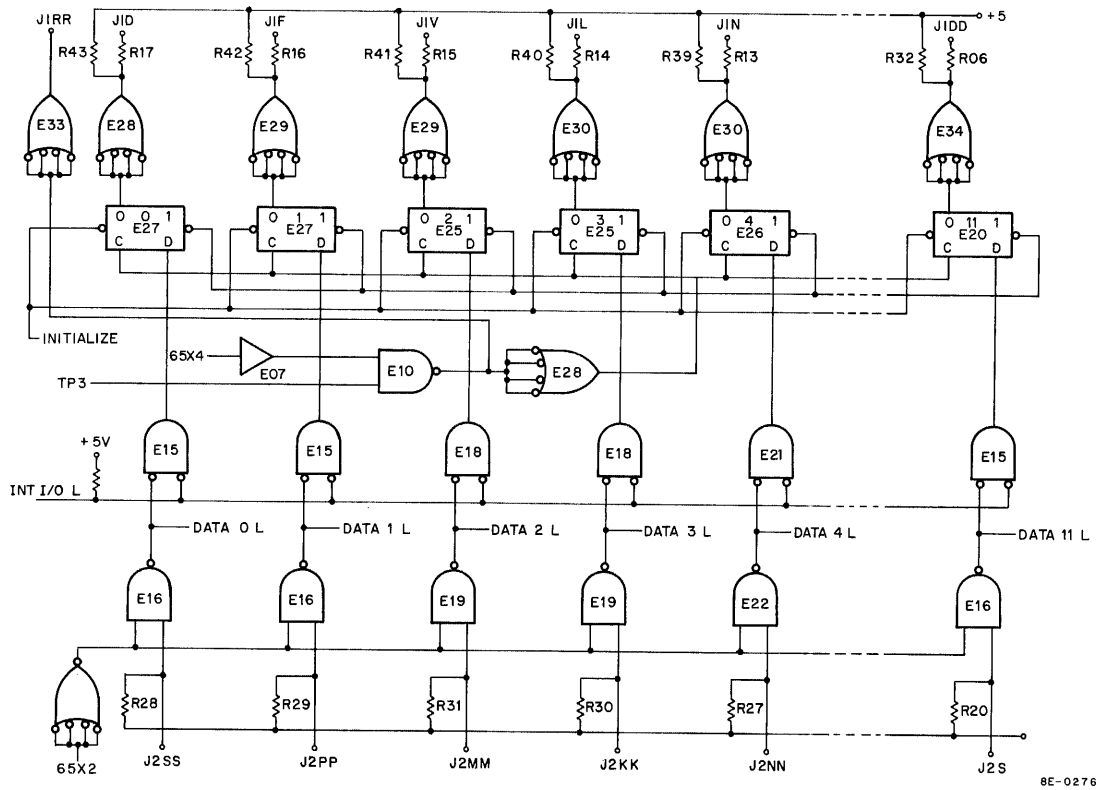Perform the following programs to transfer data from the switch register of PDP-8/E No. 1 to the AC of PDP-8/E No. 2.

Figure 8-5 Input Data Gates and Output Data Gates and Drivers

PDP-8/E No. 1			PDP-8/E No. 2	
Address	Contents		Address	Contents
200	7604		200	6501
201	6504		201	5200
202	6503		202	6502
203	5202		203	5200
204	6507			
205	5200			

After the programs are loaded, load address 200 and start both PDP-8/Es. The AC lights of PDP-8/E No. 2 will display contents of SR on PDP-8/E No. 1. It is recommended that the following be tried.

a. All 1s
b. All 0s
c. A single 1 in each bit position
d. A single 0 in each bit position.

SECTION 6 SPARE PARTS

Table 8-3 lists recommended spare parts for the DB8-E. These spare parts can be obtained from any local DEC office or from DEC, Maynard, Massachusetts.

Table 8-3
DB8-E Recommended Spare Parts

DEC Part No.	Description	Quantity
19-05547	IC DEC 7474	1
19-05575	IC DEC 7400	1
19-05579	IC DEC 7440	1
19-09486	IC DEC 384	1
19-09594	IC DEC 8251	1
19-09686	IC DEC 7404	1
19-09973	IC DEC 97401	1
19-09971	IC DEC 6380	1
19-09972	IC DEC 6314	1