EK-KL80A-OP-001

KL8-A USER'S MANUAL

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EK-KL80A-OP-001

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CHAPTER 1
INTRODUCTION

The KL8-A Multiple Serial Line Unit Interface (Figure 1-1) contains the receive, transmit, and control circuitry needed to interface the PDP-8/A to four asynchronous (serial) devices. The KL8-A is made up of the M8319 hex module, which inserts into the PDP-8/A Omnibus and is connected to four EIA serial, or 20 mA serial devices. Line 3 provides full modem control and lines 0, 1, and 2 provide partial modem control. On lines 0, 1, and 2 DATA TERMINAL READY and REQUEST TO SEND are permanently enabled.

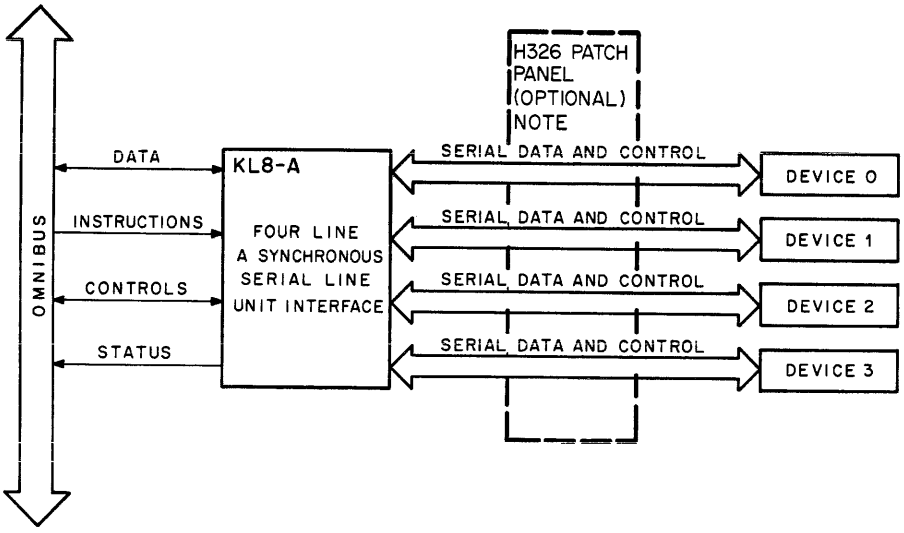

Figure 1-1 KL8-A Simplified Block Diagram

Operation is controlled by PDP-8/A instructions. A UART for each line performs parallel to serial conversions during transmit operations and serial to parallel conversions during receive operations. Baud rates for each line are switch selectable on the M8319 module. Jumpers may be installed on the UART for each line to enable parity, select even or odd parity, select 1 or 2 stop bits, and to select character length (5 through 8 bits).

An optional H326 patch and connector panel is provided for the KL8-A. The H326 panel contains eight 25-pin Cinch type connectors for EIA signals, eight 8-pin MATE-N-LOK connectors for 20 mA signals, switches for each line to connect input to output, and switches to connect a filter across the 20 mA receive leads (used only for 110 baud or less). Each panel services two KL8-A modules (8 lines). The H326 panel is required for those systems that interface to ASR and KSR Teletypes®, Bell 811B type modems or their equivalent, and is also required if the KL8-A interfaces to a mixture of EIA and 20 mA devices.

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1.1 SPECIFICATIONS AND OPERATING CONDITIONS

The specifications and operating conditions for the KL8-A are as follows:

Patch Panel

An H326 patch panel is provided for cable connections and maintenance.

Drive Capability (20 mA Serial)

Drivers/Receivers on all four lines function properly at 110 baud with up to 5000 feet of 18 gauge or larger twisted pair cable.

EIA

Drivers/Receivers function properly with up to 50 feet of cable.

Baud Rates

The following baud rates are switch selectable on the M8319 module:

50	150	1800	4800
75	300	2000	7200
110	600	2400	9600
134.5	1200	3600	

Transmit and recieve baud rates on a given line must be the same.

Stop Bits

One or two jumper selectable. One and one-half stop bits are produced when 5 bits per character is selected and the 2 SB jumper is installed.

Parity

Parity is enabled by installing a jumper. Even or odd parity is selected using a second jumper.

Device Codes

VDT's/BOARD 40541
LINE PRINTER BOARD 42543

00 through 76. Two device codes, one odd one even, are required. The even device code is jumper selectable and the other device code automatically becomes the next odd number.

Number of Bits

The number of bits per character for each line is jumper selectable between 5 and 8. Jumpers NB1 and NB2 are used to select the number of bits per character as follows:

Number of Bits	NB1	NB2
5	In	In
6	Out	In
7	In	Out
8	Out	Out

The normal configuration is 8 bits per character.

Modems

The KL8-A accommodates Bell 103/E/F/G/H, 202D, 811B, and 113B or equivalent type modems. Line 3 provides for full modem control and lines 0, 1, and 2 provide for partial modem control. On these lines, DATA TERMINAL READY and REQUEST TO SEND are permanently enabled. Line 3 provides for change of phase detection, interrupts, and Skip on CARRIER, CLEAR TO SEND, SECONDARY RECEIVE, SECONDARY TRANSMIT, REQUEST TO SEND, DATA TERMINAL READY and SPEED SELECT are programmable. For line 3 there are

	jumpers on the H326 patch panel to assert the BUSY signal, assert the DATA RATE signal, and to connect SECONDARY RECEIVE to normal or to Bell 202 SECONDARY RECEIVE. There is also a jumper to connect SECONDARY TRANSMIT to normal or to Bell 202 transmit.
Operating Conditions	Temperature: +5° C to +50° C
	Humidity: 10 to 90% non-condensing
Power Required	+5.0 V @ 2.5 A
	−15 V @ 425 mA maximum (with four 20 mA devices connected)
	+15 V @ 90 mA maximum

1.2 COMPANION DOCUMENTS

The following documents are necessary in the operation, installation and maintenance of this option:

PDP-8/A Miniprocessor Handbook 1975–1976

Introduction to Programming

PDP-8/A User's Manual

PDP-8/A Operator's Handbook

M8319 Engineering Drawings

H326 Engineering Drawings

CHAPTER 2
INSTALLATION AND ACCEPTANCE TEST

This chapter provides the procedures to be used to unpack, inspect, install, and test the KL8-A when it is installed in the PDP-8/A system.

2.1 EQUIPMENT REQUIRED

The following equipment is required to run the KL8-A Diagnostic Test:

1. PDP-8/A computer
2. At least 4K read/write memory
3. Programmer's Console. PDP-8/A console (KC8-AA) or modified PDP-8/M (KC8-M) console. To modify the PDP-8/M Programmer's Console for PDP-8/A or KL8-A maintenance, solder a wire from the lower tab (marked blue) on the left side of the front panel to Omnibus pin A2B.
4. MAINDEC-08-DJKLA Diagnostic Program
5. 50-pin Berg test connector (70-11451) or H326 patch panel with BC08Y-10 cable
6. Paper-tape reader

NOTE

It is the customer's responsibility to provide the Programmer's Console and paper-tape reader.

2.2 INSTALLATION

Install the KL8-A as follows:

1. Set switches to select baud rate for each line (Table 2-1) and to select the type of lines used, EIA or 20 mA (Table 2-2).
2. Install jumpers to select the numbers of bits per character, parity (even, odd, or none), number of stop bits, device codes, and the type of branch addressing used (Figure 2-1 and Table 2-3).

   The KL8-A is shipped in the following configuration:

   Device codes 40 and 41

   Eight branch addresses

   Parity disabled

Two stop bits per character

Eight data bits per character

Switches, any position

3. Ensure that the user does not have an option plugged into the Omnibus that uses the 40 and 41 device codes.

4. Turn PDP-8/A power OFF. Insert the M8319 into a slot other than 1, 2, or 3. Do not plug the cable into the M8319. Slot 1 is at the top of the PDP-8/A enclosure.

5. If the H326 patch panel is used, install it on the rear of the cabinet. The H326 switch settings are shown in Table 2-4.

Table 2-1
Baud Rate Select Switch Settings

Line No.	Switch No.				
L0	S2-8	S2-7	S2-6	S2-5	
L1	S2-4	S2-3	S2-2	S2-1	
L2	S3-8	S3-7	S3-6	S3-5	
L3	S3-4	S3-3	S3-2	S3-1	Baud Rate
	ON	ON	ON	ON	50 Baud
	ON	ON	ON	OFF	75 Baud
	ON	ON	OFF	ON	110 Baud
	ON	ON	OFF	OFF	134.5 Baud
	ON	OFF	ON	ON	150 Baud
	ON	OFF	ON	OFF	300 Baud
	ON	OFF	OFF	ON	600 Baud
	ON	OFF	OFF	OFF	1200 Baud
	OFF	ON	ON	ON	1800 Baud
	OFF	ON	ON	OFF	2000 Baud
	OFF	ON	OFF	ON	2400 Baud
	OFF	ON	OFF	OFF	3600 Baud
	OFF	OFF	ON	ON	4800 Baud
	OFF	OFF	ON	OFF	7200 Baud
	OFF	OFF	OFF	ON	9600 Baud
	OFF	OFF	OFF	OFF	19,200* Baud

*Illegal. The module will not operate with these switch settings.

2.3 ACCEPTANCE TEST

The MAINDEC 08-DJKLA diagnostic has four types of tests. Refer to the MAINDEC write up for loading and starting instructions.

Internal Logic/Data Test –No cable is connected; the programmable loopback mode is used. Run test for five minutes with no errors.

Operator Intervention Test – This test checks the baud rates on all lines. The program runs and the operator must time the test at 30 seconds.

Modem Control and 20 mA Data Test – This test requires the 70-11451 test plug. If the test plug is not available, the H326 patch panel may be used. If the H326 patch panel is used, the modem control signals are not checked for correct operation. Run this test for five minutes with no errors.

Terminal/Keyboard Test – This test is optional and can only be run if a terminal is available. Run this test for five minutes.

After all tests have been performed as explained in the diagnostic document running the diagnostic without errors, the M8319 must be set up to customer specifications, and re-inserted into the bus. Refer to Tables 2-1 through 2-4 for switch settings and jumper installation requirements. Paragraph 2.7 shows some typical KL8-A configurations. If it is necessary to change device codes from 40 and 41, install jumpers as shown in Table 2-5. Do not assign device codes used by another device in the system.

NOTE

IOT device codes below 30 should not be used unless it is known positively that no IOT device code conflicts exist.

Table 2-2
EIA on 20 mA Line Selection Switch Settings

Line No.	Switch No.	EIA	20 mA
L0	S1-1	ON	OFF
L1	S1-2	ON	OFF
L2	S1-3	ON	OFF
L3	S1-4	ON	OFF

NOTE

Lines that do not have a device connected to them must have their switch in the ON position.

2.4 INTERFACE PANEL AND CABLES

An optional H326 patch panel and three types of cables are available to connect the KL8-A to the user's devices.

2.4.1 H326 Patch Panel

The H326 patch panel (Figure 2-2) is supplied with the KL8-A as an option. The patch panel is required for systems that have both 20 mA and EIA inputs if the KL8-A is the interface to the ASR and KSR Teletypes, or if the KL8-A is interfaced to Bell 811B modems.

The patch panel is rack mountable and occupies a space 5.25 inches high (13.34 cm), 19 inches wide (48.26 cm), and 4.5 inches deep (11.43 cm).

The panel contains the following items:

1. Eight 25-pin Cinch type connectors for EIA signals
2. Eight 8-pin MATE-N-LOK type connectors for 20 mA signals
3. Switches for each line: To connect input to output on the data signal leads for both EIA and 20 mA circuits, and to connect a filter (2.2 mF capacitor) across the 20 mA receive leads. The filter is used only for 110 baud operation or less.

Each patch panel services two KL8-A modules or eight serial devices.

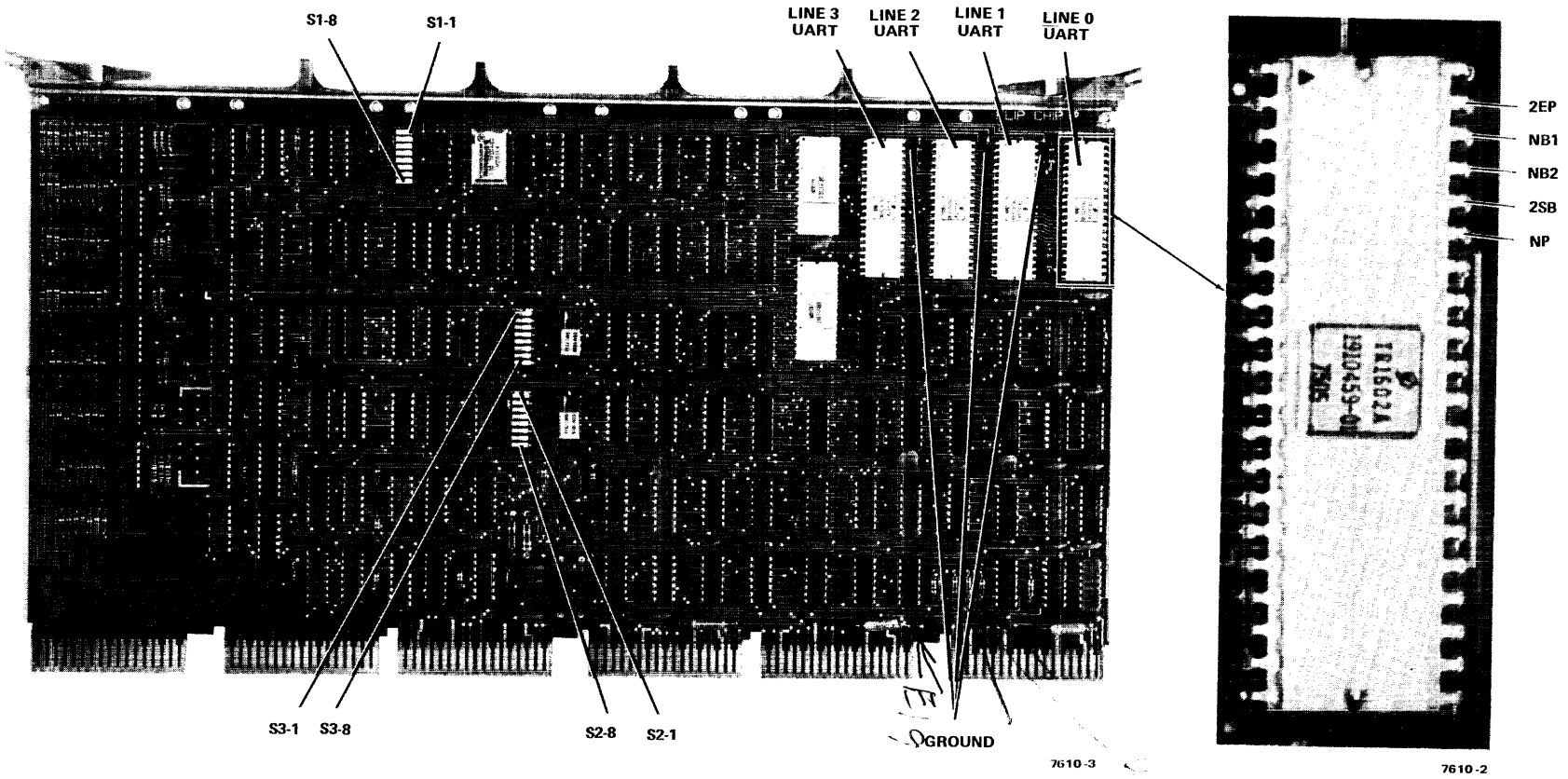


Figure 2-1 KL8-A (M8319) Module (Photo)

Table 2-3
UART Jumper Installation

Jumper Name	Option Selected With Jumper Out	Jumper Selected With Jumper In
EP	Even Parity	Odd Parity
2 SB	Two Stop Bits*	One Stop Bit
NP	Parity Disabled	Parity Enable

*1.5 stop bits are produced if 5 bits per character are selected.

NB1 and NB2	Bits per Character			
	8	7	6	5
NB1	Out	Out	In	In
NB2	Out	In	Out	In

TO JUMPER W1, SOLDER ON UART PIN TO GND.

Table 2-4
H326 Switch Settings for Teletype Filter

Line No.	Section A	Section B
L0	S2-7 ON	S4-7 ON
L1	S2-6 ON	S4-6 ON
L2	S2-5 ON	S4-5 ON
L3	S2-8 ON	S4-8 ON

Note: The ON position activates the Teletype filter.

Table 2-5
Device Code Jumper Installation

First Number of Device Code				Second Number of Device Code		
	MD3	4	5		MD6	7
	W1	W2	W3		W4	W5
0	Out	Out	Out	0	Out	Out
1	Out	Out	In			
2	Out	In	Out	2	Out	In
3	Out	In	In			
4	In	Out	Out	4	In	Out
5	In	Out	In			
6	In	In	Out	6	In	In
7	In	In	In			

TO 40, W1 ONLY

TO 42, W1 & W5

FOR W5, JUMP GND (FRONT SIDE OF W1) TO E19-12

Example: To Select Device Code 34, Jumpers W2, W3, and W4 would be In. Jumpers W1 and W5 would be Out.

NOTE

IOT Device Codes below 30 should not be used unless it is known positively that no IOT Device Code conflicts exist.

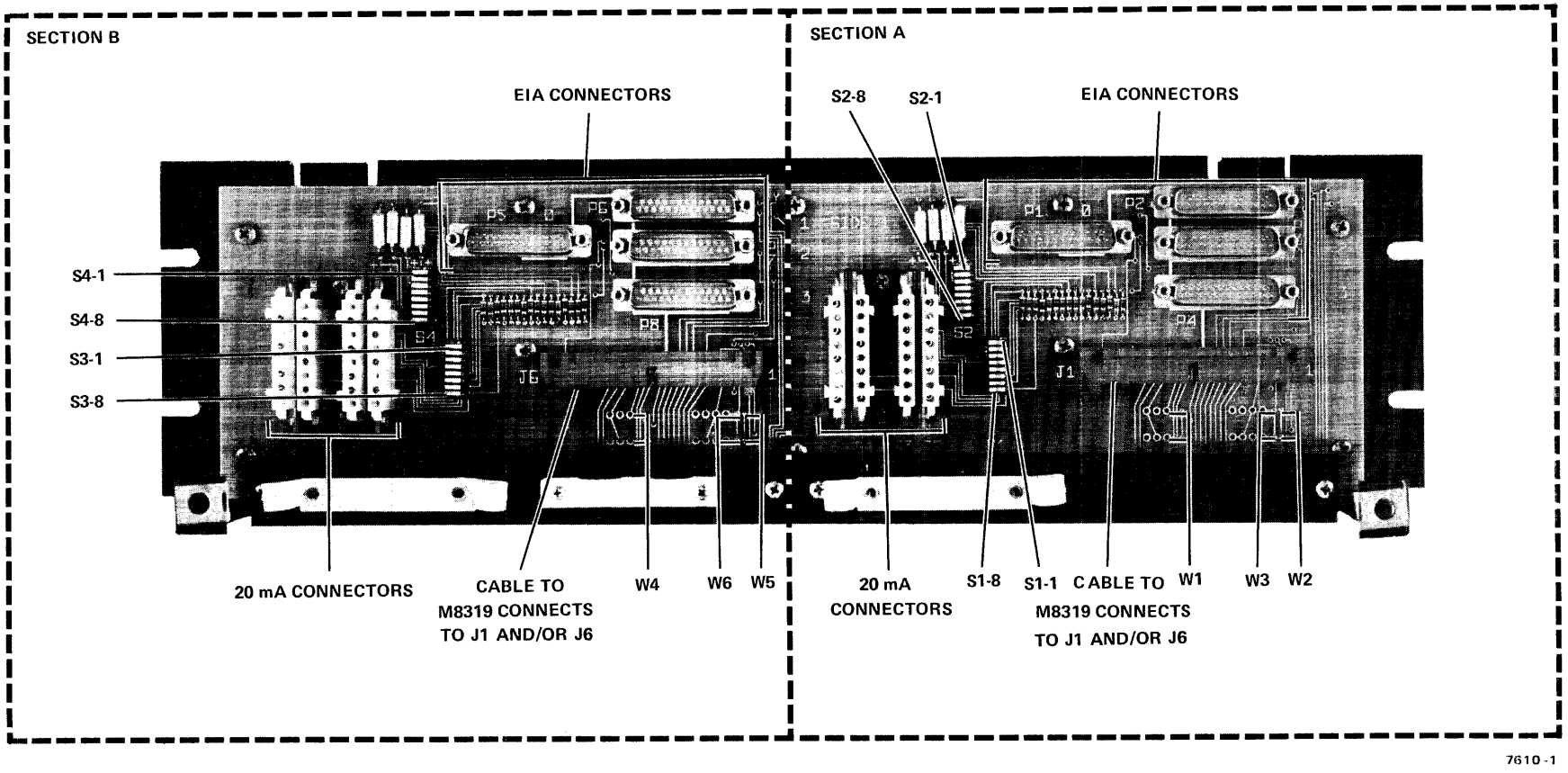


Figure 2-2 H326 Patch Panel (Photo)

Table 2-6
50 Pin Berg Connector Signals

M8319 Pin	H326	Line No.	Signal
1	2	L3	CLEAR TO SEND
2	1	L3	DATA TERMINAL READY
3	4	L3	SECONDARY RECEIVE
4	3	L2	CARRIER
5	6	L2	DATA TERMINAL READY
6	5	L3	SPEED SELECT
7	8	L1	DATA TERMINAL READY
8	7	L0	CARRIER
9	10	L3	CARRIER
10	9	L3	DATA SET READY
11	12	L0	DATA TERMINAL READY
12	11	L1	CARRIER
13	14	L2	REQUEST TO SEND
14	13	L1	RECEIVED DATA
15	16	L1	REQUEST TO SEND
16	15	L2	RECEIVED DATA
17	18	L0	REQUEST TO SEND
18	17	L3	RECEIVED DATA
19	20	L2	RING
20	19	L0	RECEIVED DATA
21	22	L3	RING
22	21		GROUND
23	24	L1	RING
24	23		GROUND
25	26	L0	RING
26	25		GROUND
27	28	L3	REQUEST TO SEND
28	27		GROUND
29	30	L3	SECONDARY TRANSMIT
30	29		GROUND
31	32	L2	TRANSMIT DATA
32	31	L3	20 mA RECEIVE (–)
33	34	L3	TRANSMIT DATA
34	33	L3	20 mA RECEIVE (+)
35	36	L1	TRANSMIT DATA
36	35	L2	20 mA RECEIVE (-)
37	38	L0	TRANSMIT DATA
38	37	L2	20 mA RECEIVE (+)
39	40	L2	20 mA TRANSMIT (+)
40	39	L1	20 mA RECEIVE (-)
41	42	L2	20 mA TRANSMIT (-)
42	41	L1	20 mA RECEIVE (+)
43	44	L1	20 mA TRANSMIT (+)
44	43	L0	20 mA RECEIVE (-)
45	46	L1	20 mA TRANSMIT (-)
46	45	L0	20 mA RECEIVE (+)
47	48	L0	20 mA TRANSMIT (+)
48	47	L3	20 mA TRANSMIT (-)
49	50	L0	20 mA TRANSMIT (-)
50	49	L3	20 mA TRANSMIT (+)

Table 2-7
Cinch Connector Signals

Pin	Signal
1	FRAME GROUND
2	TRANSMITTED DATA
3	RECEIVED DATA
**4	REQUEST TO SEND
*5	CLEAR TO SEND
*6	DATA SET READY
7	SIGNAL GROUND (logic ground)
8	RECEIVED LINE SIGNAL DETECTOR (carrier)
9	NOT USED
10	NOT USED
*11	SECONDARY TRANSMIT (for 202 modems or equivalent)
*12	SECONDARY RECEIVE (for 202 modems or equivalent)
13	NOT USED
*14	SECONDARY TRANSMITTED DATA
15	NOT USED
*16	SECONDARY RECEIVED DATA
*17	RESTRAINT (for Bell 811B modems or equivalent)
18	SPARE
19	NOT USED
**20	DATA TERMINAL READY
21	NOT USED
22	RING INDICATOR
*23	DATA SIGNAL RATE SELECTOR (speed select)
24	NOT USED
*25	BUSY

*The signals on these pins are available on line 3 connector only.
**These signals are always asserted on lines 0, 1, 2.

2.4.2 Cables

Several cables are available to connect the KL8-A to system devices. The following paragraphs describe each cable and Tables 4-1 through 4-3 list the signals carried on the cables.

2.4.2.1 BC08W Cable – The BC08W cable is a 25-foot cable with one 50-pin Berg connector on the KL8-A end and four 25-pin Cinch type EIA connectors on the device end (Tables 2-6 and 2-7).

2.4.2.2 BC08X Cable – The BC08X cable is a 6-foot cable with one 50-pin Berg connector on the KL8-A end and four 8-pin Mate-N-Lok connectors on the device end (see Tables 2-6 and 2-8).

2.4.2.3 BC08Y Cable – The BC08Y is a 10-foot cable with one 50-pin Berg connector at each end (Table 2-6). The BC08Y is used to connect the KL8-A to the H326 patch panel.

2.4.2.4 BC08Z Cable – The BC08Z is a 25-foot cable with one 50-pin Berg connector on the KL8-A end. This cable allows a mix of one EIA device and up to three 20 mA devices. The EIA cable is 25 feet long and terminates with a 25-pin EIA type connector which has connections for full MODEM control signals and is connected to line 3 data leads at the KL8-A. The three remaining cables, for lines 0, 1, and 2, are six feet long and terminate in an 8-pin MATE-N-LOK connector for each line. This cable is not intended for connecting Teletypes to the KL8-A.

Table 2-8
MATE-N-LOK Connector Signals

Pin	Signal
1	NOT USED
2	TRANSMIT (-)
3	RECEIVE (-)
4	NOT USED
5	TRANSMIT (+)
6	NOT USED
7	RECEIVE (+)
8	NOT USED

2.5 EIA DRIVERS/RECEIVERS

The EIA level convertors meet the electrical specifications of EIA specification RS-232-D. Maximum cable length of 50 feet, not including the cable between the KL8-A and the H326 patch panel, must be maintained in order to meet these specifications. Maximum capacitive load, including all cables, connectors, and electronic circuits connected to each driver must not exceed 2500 pF.

2.6 TWENTY mA DRIVERS/RECEIVERS

The maximum cable length that may be connected to a 20 mA driver/receiver is limited by a total loop dc resistance and the maximum tolerable load capcitance, which is cable and baud rate dependent. The maximum resistances are as follows:

Between Transmit (+) and Transmit (–) = 700 ohms

Between Receive (+) and Receive (–) = 600 ohms

The maximum resistance is the sum of the cable resistance to the load and back on a given pair of wires.

The maximum tolerable capacitance may be calculated using the following formula:

D (MAX)= 0.0003/C(C)XB(R)-[C(T)+C(R)/C(C)]

D (MAX)= MAXIMUM CABLE LENGTH, IN FEET

C(C)= CABLE CAPACITANCE, FARADS/FOOT

B(R)= BAUD RATE

C(T)= CAPACITANCE ACROSS TRANSMITTER IN FARADS

C(R)= CAPACITANCE ACROSS RECEIVER IN FARADS

C(T) FOR THE KL8-A IS 0

C(R) FOR THE KL8-A IS EITHER 0 OR 2.2 μF

2.7 TYPICAL CONFIGURATIONS

Some typical KL8-A configurations are shown in Figures 2-3 through 2-6. Tables 2-6 through 2-8 list the signals on each pin of the three connectors used with these cables.

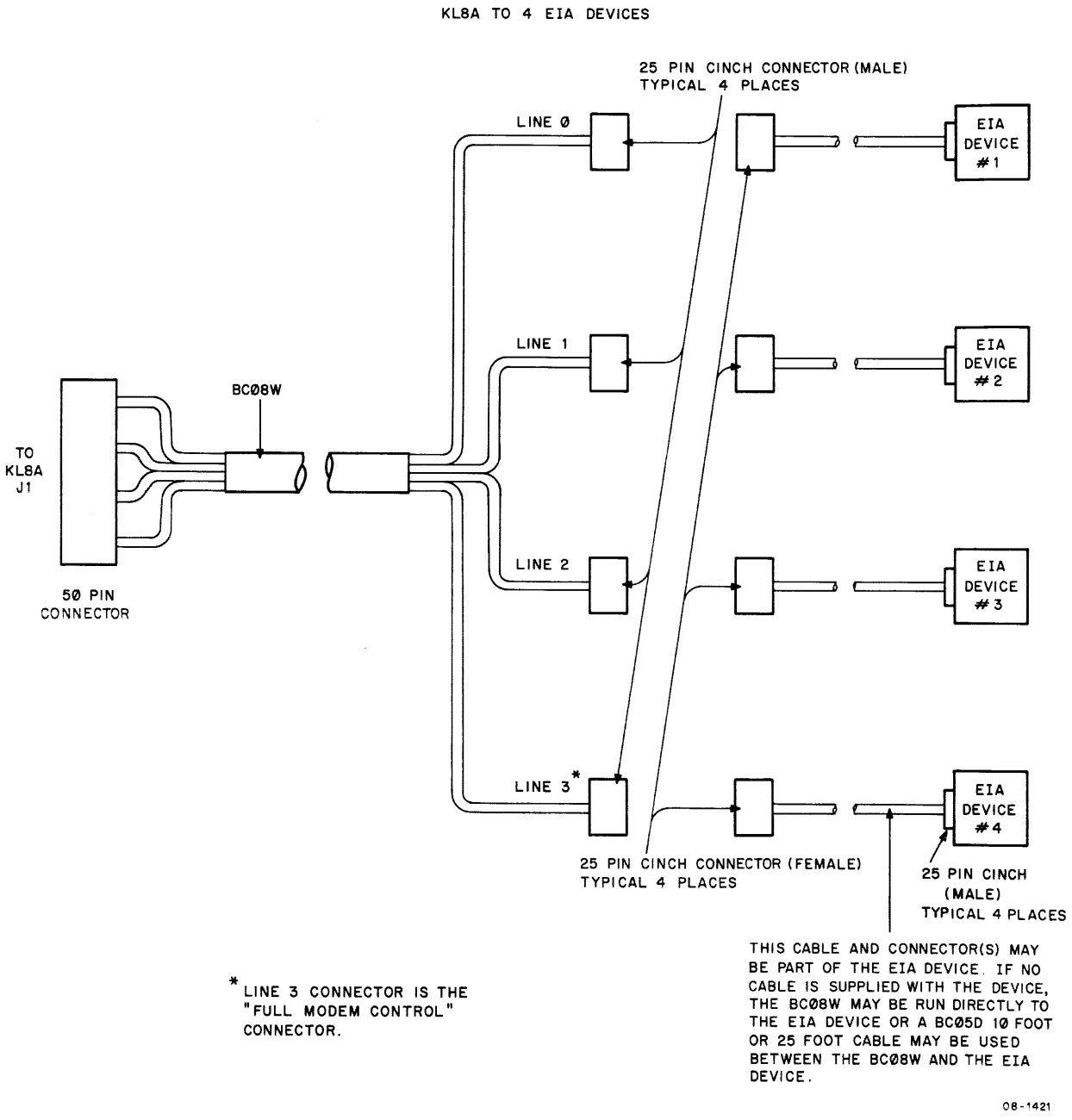


Figure 2-3 KL8-A Connected to 4 EIA Devices

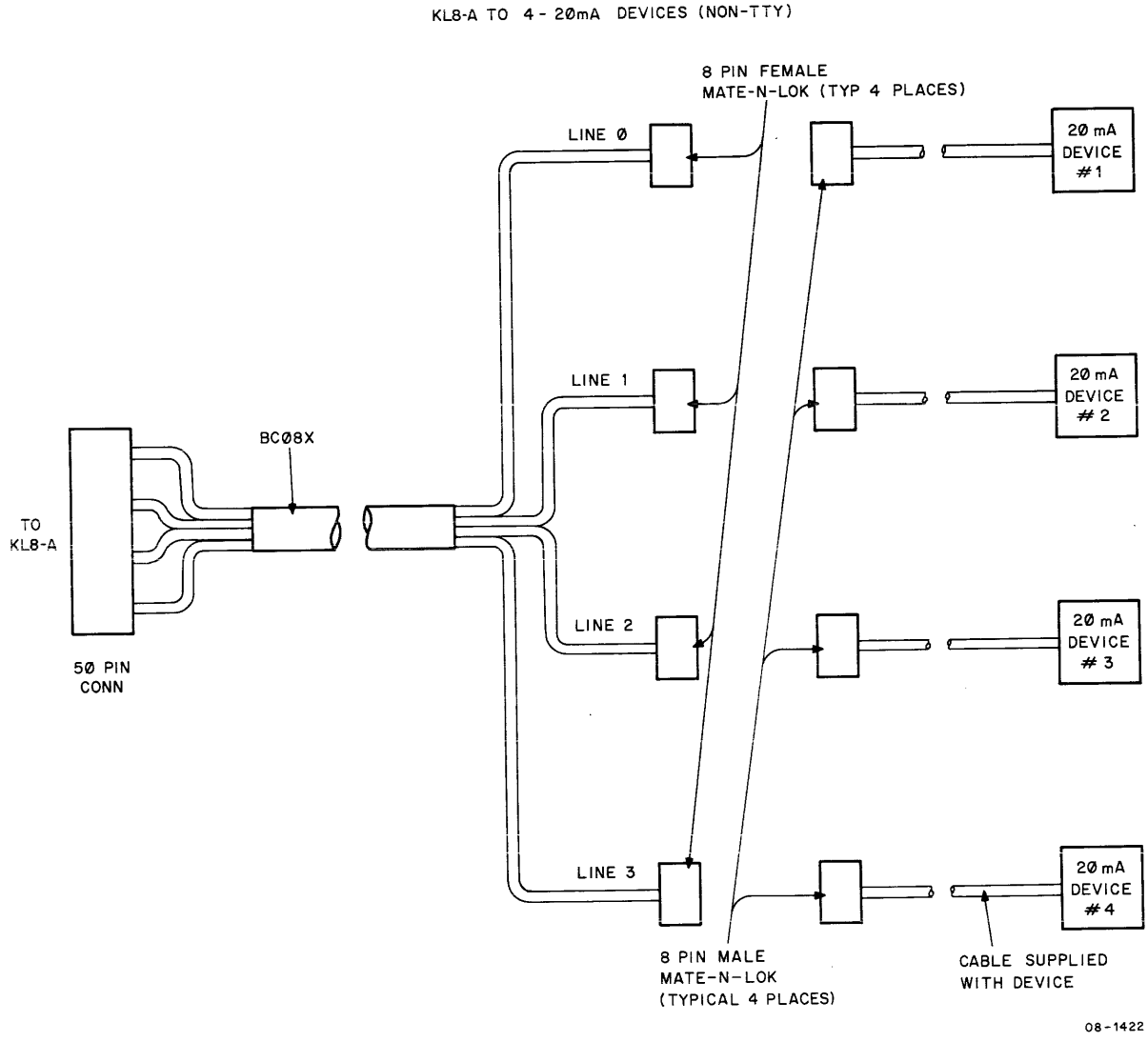


Figure 2-4 KL8-A Connected to 4 20mA Devices (Non TTY)

KL8-A TO 2-20mA DEVICES AND TO 2 EIA DEVICES

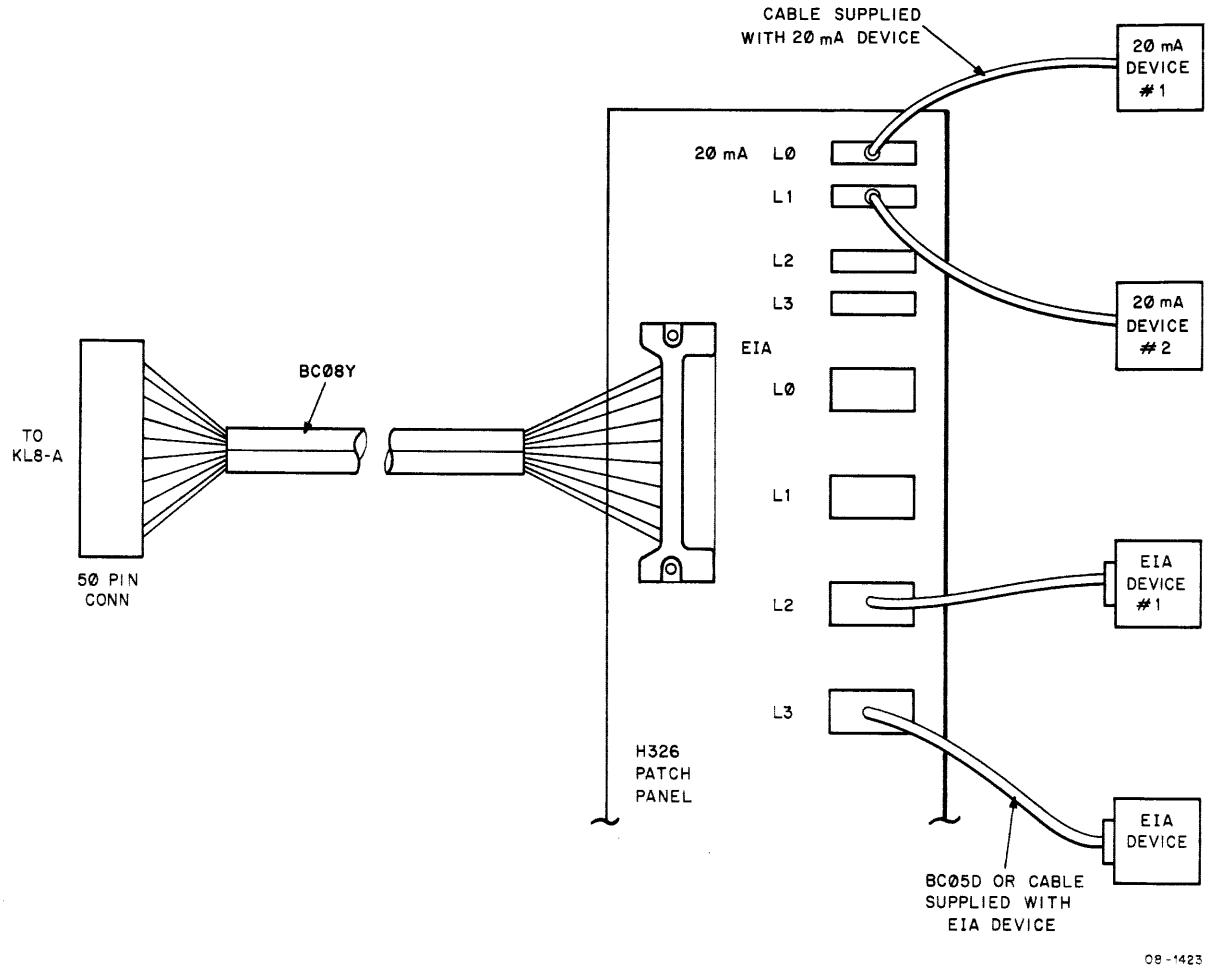


Figure 2-5 KL8-A Connected to 2 EIA Devices and 2 20mA Devices

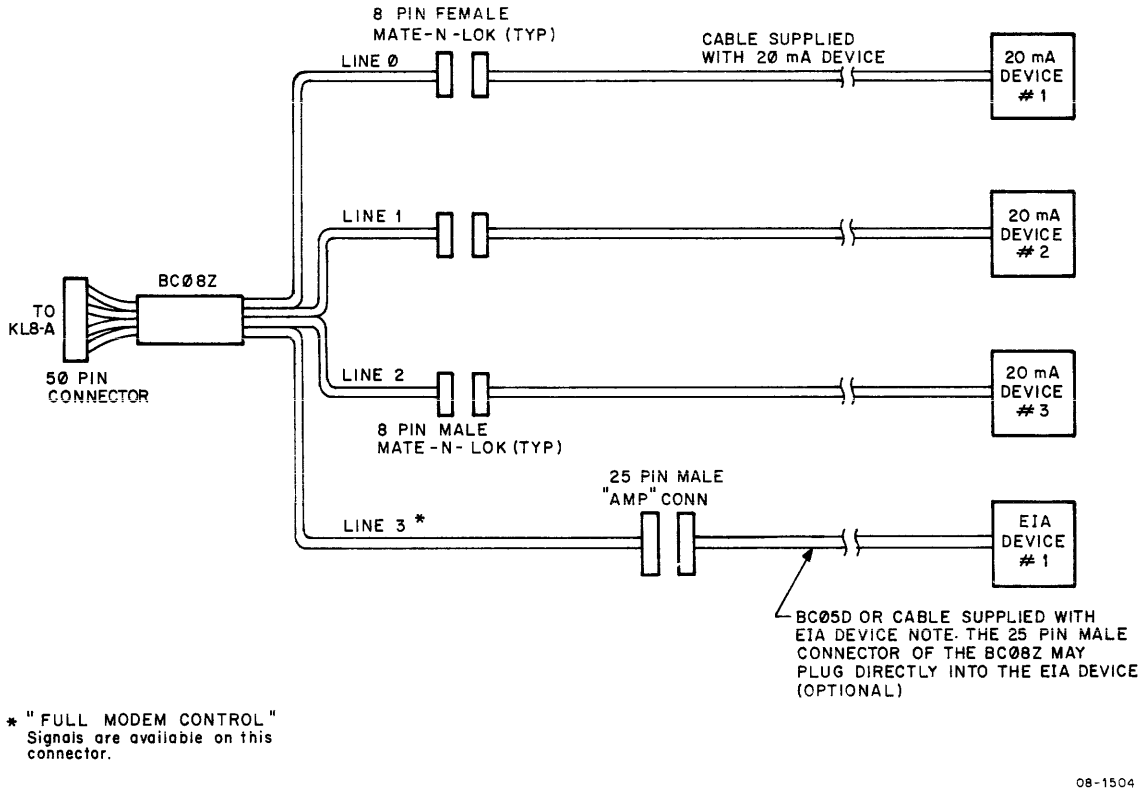


Figure 2-6 KL8-A Connected to 3 20mA Devices and 1 EIA Device

2.8 MODEM RESTRICTIONS

Since DATA TERMINAL READY and REQUEST TO SEND are permanently enabled on lines 0, 1, and 2, these lines should not be used on switch network type lines. However, lines 0, 1, and 2 can be connected to leased or private wire type lines. If lines 0, 1, and 2 are connected to switched lines, there is a possibility that when the device at the other end of the line hangs up, the line at the computer end may not hang up. This results in the line always being BUSY from that time on. On these lines, the only way to hang up at the computer is to physically disconnect the cable from the Data Set so that REQUEST TO SEND goes false.

On lines 0, 1, and 2 it is impossible to run Bell type 202 modems in half duplex or switched networks. However, Bell type 202 modems or their equivalent may be run full duplex on leased lines.

CHAPTER 3
PROGRAMMING AND OPERATION

3.1 DATA TRANSFERS

All data transfers between the KL8-A and the AC are via the Data Bus using programmed instructions. All data transfers into the AC use clear, then load type instructions.

3.2 KL8-A INSTRUCTIONS

There are two types of KL8-A instructions:

1. IOTs 6XX0 through 6XX7 for handling UART data and flags

2. IOTS 6XY0 through 6XY7 for handling the full MODEM control line, line 3

The first device code, XX, which must be even is selected by jumpers, and the second device code, XY, automatically becomes the next sequential device code. Jumpers are installed at the factory to select 640X and 641X. Device codes 00 through 76 may be assigned to the KL8-A. However, device codes below 30 should not be assigned before checking to ensure that these device codes are not assigned to some other device on the system.

The following instructions are used to program the KL8-A:

Mnemonic	Octal Code	Operation
MSIE	6XX0	Load AC11 into the interrupt enable flip-flop for both transmit and receive. AC11 = 1 Enable Interrupt AC11 = 0 Disable Interrupt
MSAB	6XX1	If the transmit or receive device flag is set (true), branch to service routine, and load AC11 and AC10 with line number. Clear the transmit flag if it is set. The branch address is loaded by the MSLB instruction (see MSAB programming example in Paragraph 3.3).
MSRA	6XX2	Transfer the content of Status A register to the AC (see Figure 3-1 and Table 3-1).

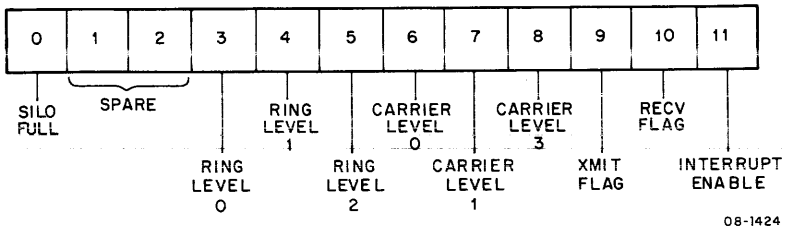


Figure 3-1 Status A Register Bits

Table 3-1
Status A Register Bits

AC Bit	Description	Functions
0	SILO FULL	SILO FULL is a one when there are 32 words in the FIFO register.
1 and 2		Not used.
3	RING LEVEL 0	RING LEVEL 0 is a one when a ring is received on line 0.
4	RING LEVEL 1	RING LEVEL 1 is a one when a ring is received on line 1.
5	RING LEVEL 2	RING LEVEL 2 is a one when a ring is received on line 2.
6	CARRIER LEVEL 0	CARRIER LEVEL 0 is a one when an incoming carrier is present on line 0.
7	CARRIER LEVEL 1	CARRIER LEVEL 1 is a one when an incoming carrier is present on line 1.
8	CARRIER LEVEL 3	CARRIER LEVEL 3 is a one when an incoming carrier is present on line 3.
9	XMIT FLAG	The XMIT FLAG is set (1) when one or more of the UARTs are ready for a new transmit word.
10	RECV FLAG	The RECV FLAG is set (1) when the CHARACTER flag is set. The CHARACTER flag sets when there is one or more words in the FIFO register.
11	INTERRUPT ENABLED	INTERRUPT ENABLED is a one when the interrupt flip-flop has been set by the MSIE instruction.

Mnemonic	Octal Code	Operation
MSSR	6XX3	Skip an instruction if a ring occurs and clear RING LEVEL if the ring occurred on lines 0, 1, or 2.
MSXD	6XX4	Transfer a character and line number (Figure 3-2) from the AC to the XMIT buffer. The AC is not cleared.
MSRD	6XX5	Clear the AC and transfer a character, line number, and error status from the FIFO register to the AC (Figure 3-3 and Table 3-2). Clear RECEIVE flag if FIFO register is empty.
MSCT	6XX6	Unconditionally clear TRANSMIT flag and highest priority Transmit Buffer Empty (TBMT) Latch.

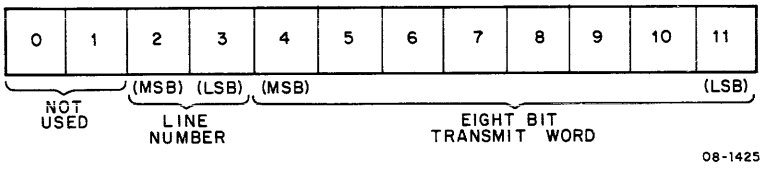


Figure 3-2 Transmit Word

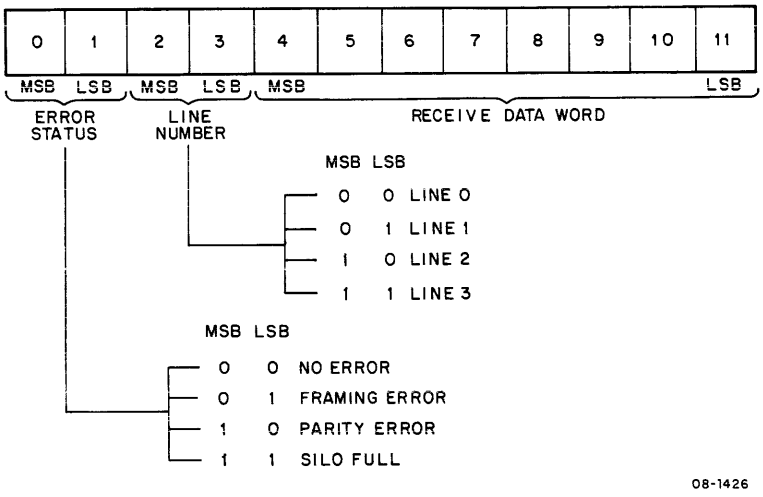


Figure 3-3 Receive Status and Data Word

3.3 PROGRAMMING EXAMPLE

The following program is an example of a routine used to service a device which has generated an interrupt request to the KL8-A:

Interrupt Service Routine

/SPF	Test Power Fail
/SKP	No, Continue
/JMS	Exit to Power Fail Routine
/MSAB	Assert Branch Address (Figure 3-6)
/IOT N	Test next device
/SKP	No, continue
/JMS	Exit to device routine

Table 3-2
Receive Status and Data Word Bits

AC Bit	Description	Function
0 and 1	Error Status	The errors indicated by bits 0 and 1 are as follows:
	AC0 AC1 Error	
	0 0 None	No error.
	0 1 FRM Error	Framing error is asserted when the received character did not contain a valid STOP bit(s).
	1 0 PAR Error	Parity error is asserted when a bit has been added or dropped from the received character during transmission. If both FRM Error and PAR Error are true, FRM Error is reported.
	1 1 Silo Full	Silo Full is set when the silo contains 32 words. This error is reported as soon as the next MSRD IOT is executed. This error overrides any error condition that may be present at the bottom of the silo.
2 and 3	Line Number	AC bits 2 and 3 contain the line number (Figure 3-3).
4 through 11		AC4 through AC11 contain the received character.

Mnemonic	Octal Code	Operation
None	6XX7	Not used.
MCCD	6XY0	Clear device, all flags, silo and control and status words.
MSLC	6XY1	Transfer AC0–AC4 to the line 3 control register (Figure 3-4 and Table 3-3).

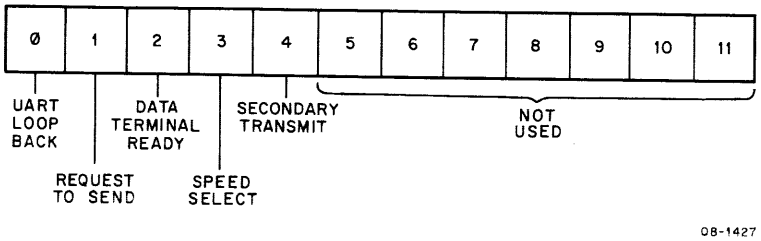


Figure 3-4 Control Word For Line 3

Table 3-3
Control Word For Line 3 Bits

AC Bit	Description	Function
0	UART LOOP BACK	UART LOOP BACK is used during maintenance operations to enable serial data out of the UART to be fed back as serial data into the UART for all four lines. This allows the transmit and receive logic to be checked while the KL8-A is not connected to a device.
1	REQUEST TO SEND	REQUEST TO SEND is set to one to assert the RQST TO SEND signal to the modem or data set on line 3. This signal is permanently enabled on all lines except line 3.
2	DATA TERMINAL READY	DATA TERMINAL READY on line 3 is asserted low to indicate that the line data communication equipment is connected to a channel, not in a talk mode, or test mode, the equipment has completed where applicable any timing functions required to complete the call, and the transmission of any answer tone is complete.
3	SPEED SELECT	SPEED SELECT on line 3 is set to one to activate the signal rate selection circuitry in the modem and select the highest signaling rate if the modem is equipped with this circuitry.
4	SECONDARY TRANSMIT	SECONDARY TRANSMIT on line 3 is set to a one to activate a secondary channel in the modem for transmission of data.

Mnemonic	Octal Code	Operation
MSLB	6XY2	Transfer the branch address in AC0—AC8 to the Branch Address register. AC0—AC8 contain the most significant 8 bits of the address of the KL8-A service routine. The 3 least significant bits are determined by whether it is a receive or transmit flag and the line number (see programming examples for MSAB IOT in Paragraph 3.3).
MSSB	6XY3	Skip an instruction if RING is set and clear the RING flag. This instruction is used for line 3 only.
MSSS	6XY4	Skip an instruction if CLEAR TO SEND is set and clear the CLEAR TO SEND flag. This instruction is used for line 3 only.
MSSC	6XY5	Skip an instruction if CARRIER is set and clear the CARRIER flag. This instruction is used for line 3 only.
MSSV	6XY6	Skip an instruction if SECONDARY RECEIVE is set and clear SECONDARY RECEIVE. This instruction is used for line 3 only.
MSRB	6XY7	Transfer the content of the status B register into AC0—AC11 (Figure 3-5 and Table 3-4). This register shows status of line 3 only.

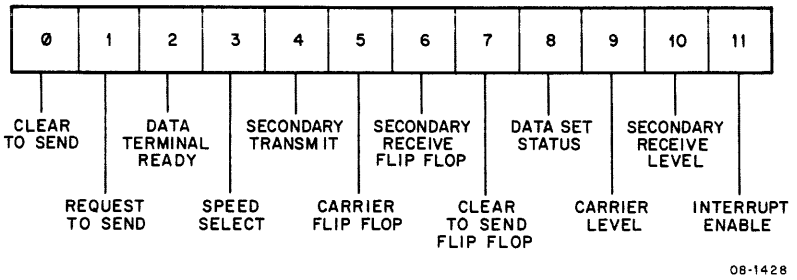


Figure 3-5 Status B Bit Assignments For Line 3

Table 3-4
Content of Status B Register

AC Bit	Description	Function
0	CLEAR TO SEND	CLEAR TO SEND is asserted to a one when the data set is ready to transmit data.
1	REQUEST TO SEND	REQUEST TO SEND is asserted to a one to condition the data communications device for a transmit operation.
2	DATA TERMINAL READY	DATA TERMINAL READY is asserted to a one to indicate that the local data communication equipment is connected to a communication channel, not in test or talk modes, the equipment has completed where applicable any timing functions required to complete the call, and the transmission of any answer tone is complete.
3	SPEED SELECT	SPEED SELECT is asserted to a one when the highest signaling rate has been selected in the data communication equipment. The equipment must contain the circuitry to select between two signaling rates if this feature is used.
4	SECONDARY TRANSMIT	SECONDARY TRANSMIT is asserted to a one if the secondary transmit channel (if there is one) has been selected fro transmit operations.
5	CARRIER	The CARRIER flip-flop is set (1) when the data communications equipment is receiving a suitable signal from the communications line.
6	SECONDARY RECEIVE	The SECONDARY RECEIVE flip-flop is set (1) if the secondary receive channel has been selected for receiving data.
7	CLEAR TO SEND	The CLEAR TO SEND flip-flop is set (1) if the communication equipment is ready to transmit data.

Table 3-4 (Cont)
Content of Status B Register

AC Bit	Description	Function
8	DATA SET STATUS	The DATA SET STATUS flip-flop is set (1) if the following are true: 1. The data communications equipment is connected to a communication channel. 2. The data communications equipment is not in test or talk mode. 3. The data communications equipment has completed where applicable a. Any timing functions required to complete a call b. The transmission of any answer tone of which the duration is determined by the equipment.
9	CARRIER LEVEL	CARRIER LEVEL is asserted (1) when the data communication equipment is receiving a signal which meets its stability criteria.
10	SECONDARY RECEIVE LEVEL	The SECONDARY RECEIVE LEVEL line is asserted (1) for circuit assurance or to interrupt the flow of data in the primary channel.
11	INTERRUPT ENABLE	INTERRUPT ENABLE is set (1) when the program executes the MSIE instructions and loads a one from AC11 to enable an interrupt request.

3.4 TRANSMIT OPERATION

The sequence of operations required to transmit a character are as follows:

1. Load the transmit buffer register (Figure 3-2) with data and line number from the AC using the MSXD instruction. AC bits 2 and 3 contain the line number on which the data is to be transmitted and AC bits 4 through 11 contain the data to be transmitted.

2. The next positive transition of TBMT from the UART latches the TBMT flip-flop for that line. The four TBMT flip-flops are then sampled at TP4 time and the results of this sample are directed to a priority encoding network which generates a level indicating that one or more UARTs are waiting for another transmit word. Also produced by the priority encoding network is the two-bit line number of the highest priority line requesting service at this time. The level generated by the priority is sampled at TP1 time. The two-bit line number then is used for part of the Branch Address when the MSAB IOT is executed (Figure 3-6). When the MSAB IOT is executed, the program branches to a location corresponding to a particular line number for a transmit flag, then the line that caused the interrupt has its TBMT flip-flop cleared by the MSAB IOT. This allows the next higher priority line to cause an interrupt; or, if the interrupt system is off, the next MSAB instruction causes the program to branch to the appropriate location.

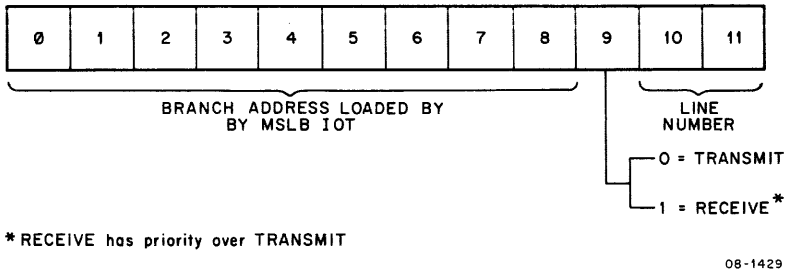


Figure 3-6 Branch Address Register

3.5 RECEIVE OPERATION

The sequence of operations for a receive operation is as follows:

1. Serial data from a device is assembled in the UART to form a parallel data word. When DATA AVAIL is asserted by any UART, an internal scanner/timing generator moves the data from the UART whose number equals the scan count number into the FIFO register (silo). Assuming the FIFO register is not full, the FIFO register contains the scan count (line number), two error status bits, and the data character (Figure 3-3).

2. The FIFO register, which holds 32 words, automatically forces the word in the top down toward the bottom of the register. The word moves down to the last empty location and continues to move down one location each time as a word is read from the FIFO register. The character flag sets when the FIFO register produces a level which indicates that there is one or more words in the FIFO register. This level from the FIFO register is sampled at TP4 time.

3. When the MSAB IOT is executed, the program will branch to a location determined by the bottom word in the FIFO register (Figure 3-3).

4. The MSRD IOT transfers the content of the FIFO register into the AC and attempts to clear the receive flag after each transfer. The receive flag clears when the FIFO register is empty. The program can simply empty the FIFO register using the MSRD and later check the data to determine line numbers or the MSAB IOT can be issued after an MSRD causing the program to branch to a location for the same or next line number in the FIFO register.

3.6 BRANCH ADDRESSING

If the transmit and/or the receive flag is set, and the MSAB IOT is executed, the following occur:

1. AC bits 10 and 11 contain the octal value of the line causing the interrupt (Figure 3-6).

2. The program counter in the CPU is forced to the address determined by:

   a. Bits 0 through 8 of the Branch Address register which must have been set by the MSLB instruction.

   b. Bit 9, 0 if transmit flag is set, and 1 if the receive flag is set. If both flags are set, receive has priority.

   c. Bits 10 and 11 equal the octal value of the line number causing the INTERRUPT flag to set. Transmit flags come up in order of priority. Line 3 has the highest priority while line 0 has the lowest priority. There are jumpers which can be inserted that will cause the KL8-A to disregard bits 10 and 11. With the jumpers installed, the KL8-A has only two Branch Addresses; one address for transmit, and one address four addresses greater than the transmit address for the receive address.

If the receive and transmit flags are both set, the MSAB branch IOT branches on the receive flag and the line number (Figure 3-3) at the bottom of the First In First Out (FIFO) register. As the FIFO register is unloaded and read into the AC by the MSRD instruction, the MSRD IOT attempts to clear the receive flag. The receive flag does not clear until the last word is read out of the FIFO register. If new characters are read into the FIFO register, they must also be transferred to the AC before the receive flag can be cleared. When the receive flag clears, the transmit flag causes an interrupt request and when the MSAB IOT is executed by the program, a branch to the transmit address is done. The transmit flag is cleared by the MSAB IOT.

When the KL8-A generates an interrupt request (interrupts must be enabled), the normal interrupt sequence takes place. That is, the PC is forced to location 0000 of field 00, the old PC value is stored in location 0000, and a JMS is forced. It is only when the MSAB IOT is issued that the Branch Address is forced into the PC. Normally, the MSAB IOT would be executed in the interrupt service routine or in multi-field systems the current field would be restored, and then the MSAB IOT would be executed. The MSAB IOT does not cause the computer to cross field boundaries.

CHAPTER 4
PRINCIPLES OF OPERATION

4.1 BLOCK DIAGRAM DESCRIPTION

Figure 4-1 is a block diagram of the KL8-A Multiple Serial Line Unit Interface. The block diagram should be used to understand the flow of control signals and data between the functional groups of logic which are described in the following paragraphs.

4.1.2 Device Select Logic

The device select logic decodes bits MD3 L–MD8 L when I/O PAUSE is asserted (low) and enables the Instruction Decoders to decode bits MD9–MD11 when the program executes one of the KL8-A instructions. Each KL8-A must be assigned two device codes (one even and one odd octal number). The even device code is selected by jumpers on the M8319 module and the odd device code automatically becomes the next highest number. Device codes 00–76 may be assigned to the KL8-A. The device select logic also asserts INTERNAL I/O L to inform the Positive I/O Bus Interface (if it is installed) that this is a KL8-A instruction which does not affect it.

4.1.3 Instruction Decoders

The Instruction Decoders are enabled by the device select logic and MD8 L when a KL8-A instruction is executed by the program. MD8 L being low selects the Odd Instruction Decoder and MD8 L being high selects the Even Instruction Decoder. The Instruction Decoders decode bits MD9 L–MD11 L and provide the necessary control signals to operate the KL8-A. A list of instructions and their function is provided in Chapter 3 along with a programming example.

The C line control logic associated with the Instruction Decoder controls the direction of data transfer on the Data Bus. The details and logic levels of these lines for the KL8-A instructions are explained in the detailed logic description.

4.1.4 Interrupt and Skip Logic

The Interrupt and Skip logic are used to interrupt the program when a data transfer is required.

SKIP L is asserted to cause the program to skip an instruction when one of the following occurs:

1. The program executes an MSSR instruction and the RING flag on any of lines 0, 1, or 2 is set (1).
2. The program executes an MSSB instruction and the line 3 RING flag is set (1).
3. The program executes an MSSS instruction and the line 3 CLEAR TO SEND flag is set (1).
4. The program executes an MSSC instruction and the line 3 CARRIER flag is set (1).
5. The program executes an MSSV instruction and the line 3 SECONDARY RECEIVE flag is set (1).

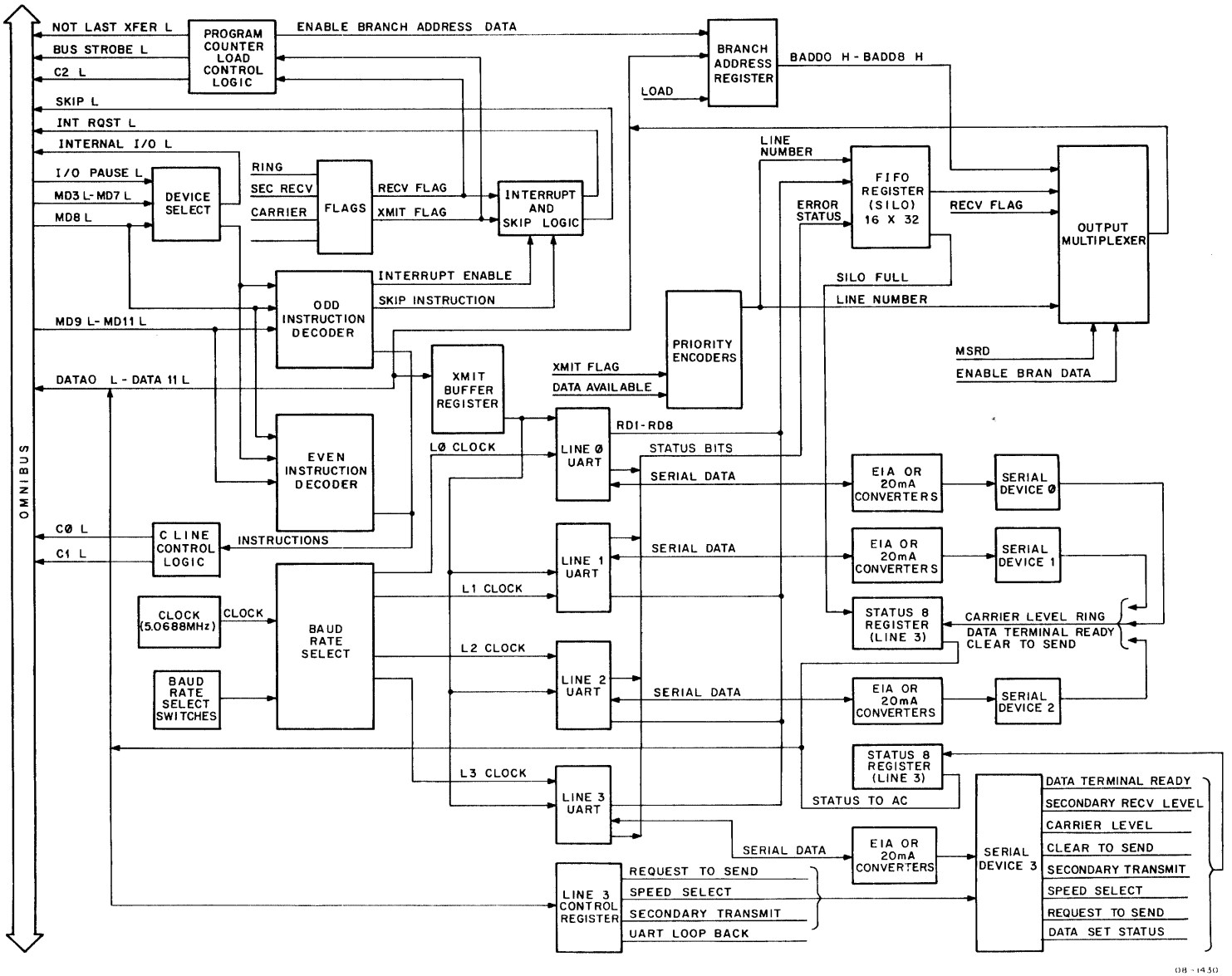


Figure 4-1 KL8-A Block Diagram

The program is interrupted by an interrupt request (INT RQST L is asserted low) if interrupt enable is set and one of the following occurs:

1. The XMIT flag is set (1)
2. The RECV flag is set (1).
3. The CHARACTER flag is set (1).
4. The 1/2 FULL flag is set (1).
5. A RING occurs on any line.
6. The CARRIER flag for line 3 is set (1).
7. The SECONDARY RECEIVE flag for line 3 is set (1).
8. The CLEAR TO SEND flag for line 3 is set (1).

4.1.5 Universal Asynchronous Receiver/Transmitter

The KL8-A contains four Universal Asynchronous Receiver/Transmitters (UART) to transmit and receive serial data. The UART performs serial to parallel (receive) and parallel to serial (transmit) conversion of data received from or sent to a serial device.

The UART operation can best be understood by dividing the operation into two functions. A block diagram description of these functions is given in the following paragraphs.

4.1.6 Transmit Operation Block Diagram Description

Figure 4-2 is a block diagram of the UART transmit operation. The transmit portion of the UART receives an 8-bit parallel character and changes it to 8 bits of serial data for transmission to a serial device. The number of bits/characters is selected by installing jumpers on the UART.

A transmit operation is started when parallel data is transferred from the AC to the XMIT BUFFER register. A TRANSMIT DATA strobe is given, loading the holding register. At this point TBMT is brought low by the UART. On the next transition of the transmit clock, the Holding register is transferred to the XMIT shift register. TBMT is then allowed to go high setting the XMIT flag. The transmit flag signals that the Holding register is empty and ready for another word. The UART then shifts out the word appending start and stop bits and parity as required to the serial device (Figure 4-3).

4.1.7 Receive Operation Block Diagram Description

A block diagram of the receive operation is shown in Figure 4-4. The receive portion of the UART will receive serial data from a serial device and change it to parallel data for transfer to the AC. Data from the device is assembled in the Receiver SHIFT register, start and stop elements are stripped off, parity, if selected, is checked and transferred to the FIFO register as parallel data. At the same time, the line number and error status information are loaded into the FIFO register (Figure 3-3). The FIFO register holds 32 received characters. If the FIFO register is empty when a character is transferred into it, the character goes to the bottom of the register and it is the next word transferred to the AC by the program. If the FIFO register is not empty, it will be transferred to the first empty location and drop down one location each time a word is transferred to the AC.

4.1.8 First In First Out Register

The First In First Out (FIFO) register consists of two 8 bit X 32 bit first in first out memories. Data is parallel transferred from the UART and then parallel transferred to the Data Bus via an output multiplexer by the MSRD instruction.

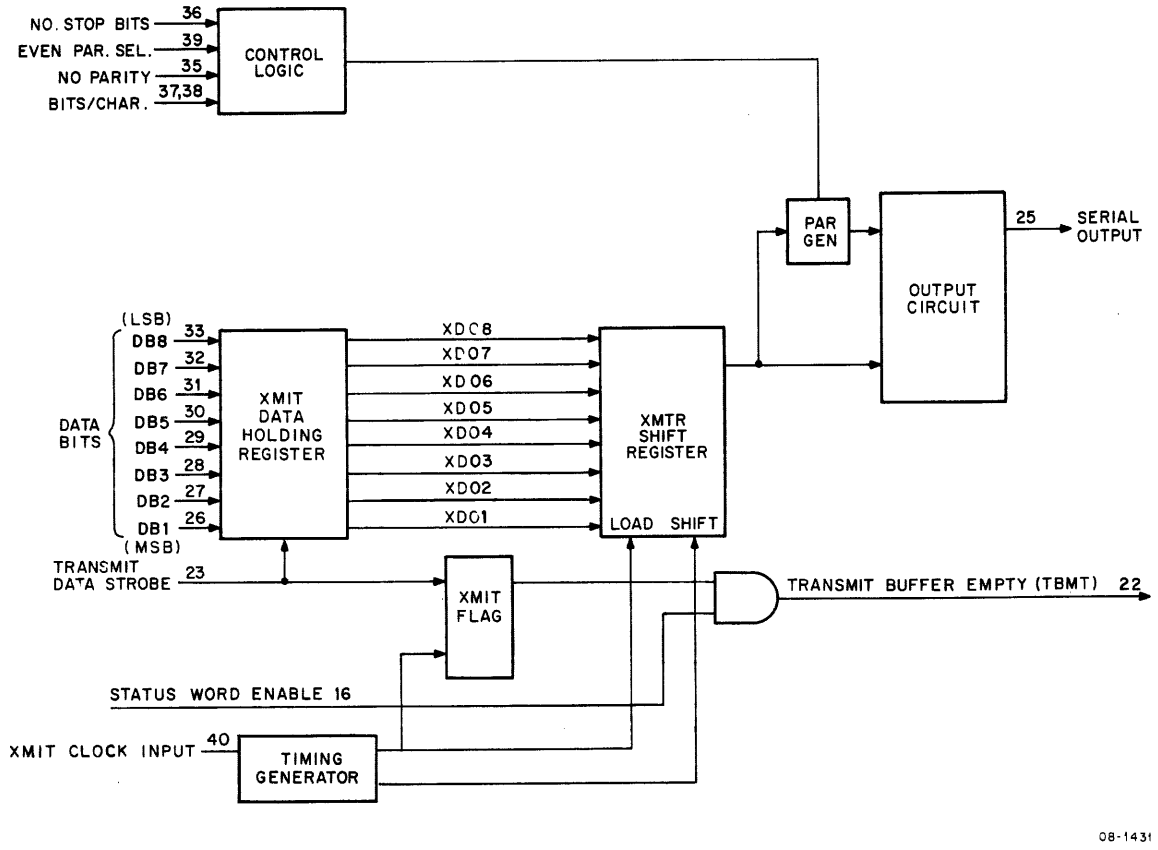


Figure 4-2 Transmit Operation Block Diagram

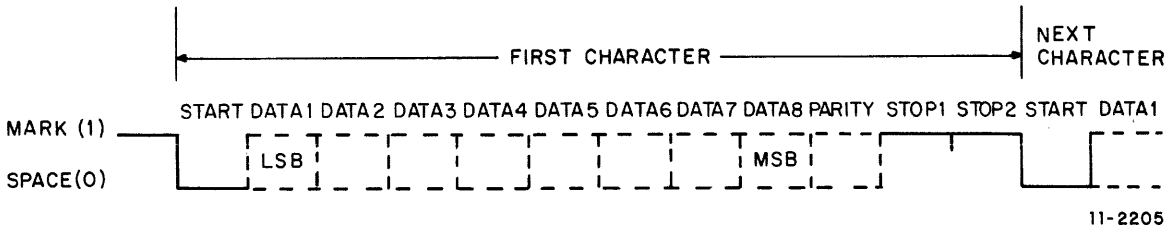


Figure 4-3 Format of I/O Character

4.1.9 Output Multiplexer

The Output Multiplexer allows the program to transfer the received data using the MSRD instruction to the AC, or to load the PC via the Data Bus using the MSAB instruction.

4.1.10 Branch Address Register

The Branch Address register is loaded from the AC by the MSLB instruction with the 9 most significant bits of the address of a memory location. The 3 least significant bits are determined by whether or not the operation is transmit or receive and by the line number (Figure 3-6). This allows the selection of a different memory location for each line for transmit and receive operations.

The PC is forced to the value of the Branch Address when the MSAB instruction is executed by the program after a transmit or receive flag sets.

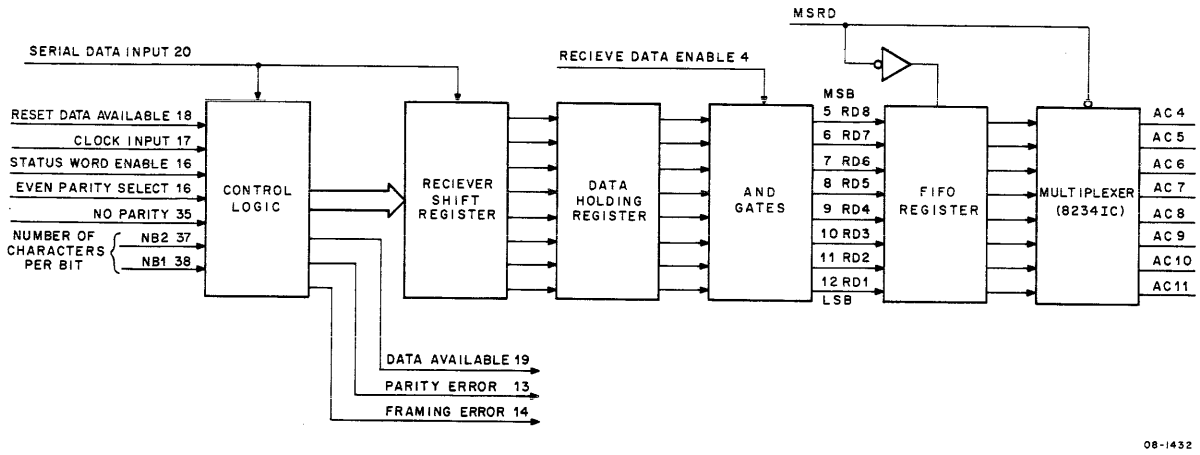


Figure 4-4 Receive Operation Block Diagram

4.1.11 Priority Encoder

There are two priority circuits, one gates the transmit and receive flags in such a way that if both transmit and receive flags are true, the receive flag takes priority. Only after the receive flag is cleared, after the silo is emptied, will the transmit flag raise an INT RQST. The second priority circuit decides which TBMT latch, if more than one is set, raises the transmit flag. Line 3 TBMT latch has the highest priority, while line 0 has the lowest.

4.1.12 Program Counter Loading Control Logic

The Program Counter (PC) loading control logic is used when the MSAB instruction is executed by the program to transfer the Branch Address via the Data Bus to the PC (Paragraph 3.5 of the *PDP-8/A User's Manual* for the timing). Assertion of BUS STROBE L and C2 L allows the PC to be loaded with the Branch Address from the Data Bus.

4.1.13 Clock Signal Generator and Baud Rate Select Logic

The KL8-A clock is a 5.0688 MHz crystal controlled oscillator whose output is applied to the baud rate select logic. The switches associated with the baud rate select logic allow the selection of a divided clock signal and thus a different baud rate for each of the four SLU lines. The clock signal (i.e., LO) is 16 times the selected baud rate. For example, a line with a baud rate of 110 baud has a clock whose frequency is 1760 Hz.

4.1.14 Status A Register

The contents of Status A register (Figure 3-1) is transferred to the AC when an MSRA instruction is executed by the program. As shown in Figure 3-1, the content indicates the status of lines 0, 1, and 2, the FIFO register, and the interrupt enable flip-flop.

4.1.15 Status B Register

The contents of Status B register is transferred to the AC when the MSRB instruction is executed by the program (Figure 3-5). As shown in Figure 3-5, the contents of this register indicate the status of line 3 and the Interrupt Enable flip-flop.

4.1.16 Control Register

The Control register is loaded from the AC by the MSLC instruction to control line 3 transmit and receive operations (Figure 3-4). Line 3 is the only line that allows the program full control of the modem. The level of the control signals out of the Control register may be checked by reading the content of Status B register (Figure 3-5).

4.1.17 Level Converters

Level converters are provided to convert TTL levels to EIA or 20 mA levels during transmit operations and to convert EIA or 20 mA levels to TTL levels during receive operations.

4.1.18 Maintenance Logic

Logic is provided on the M8319 which allows the serial output of the UARTs to be fed back to the serial input for maintenance checks. If bit 0 is set when the control register is loaded by the MSLC instruction, the loop back of serial data is enabled.

4.2 DETAILED LOGIC DESCRIPTION

The logic in the KL8-A will be divided into functional groups for discussion purposes. Figure 4-1 should be used to understand the relationship between each group of logic.

4.2.1 Device Select Logic

The device select logic shown in Figure 4-5 enables the odd or even instruction decoder if I/O PAUSE L is asserted low and one of the KL8-A instructions is executed by the program. The KL8-A can be assigned any even device code (00 through 76) by installing or removing jumpers on the M8319 module (see Table in Figure 4-5). The next odd numbered device code after the jumper selected device code automatically becomes the second device code for the KL8-A.

The Table in Figure 4-5 shows separate jumper configurations for each of the numbers in the device code which can be jumper selected.

INTERNAL I/O L is asserted by the device select logic to alert the KA8-E positive I/O BUS Interface that an I/O device on the Omnibus has recognized this instruction. If INTERNAL I/O L is not grounded, the KA8-E decodes the IOT instruction.

4.2.2 Instruction Decoder

The odd and even Instruction Decoders for the KL8-A are shown in Figure 4-6. One of the Instruction Decoders is enabled by the device select logic when a KL8-A instruction is executed by the program. MD8 L being low (1) enables the odd Instruction Decoder and MD8 L being high enables the even Instruction Decoder.

The Instruction Decoders are 7442 ICs which decode MD9 L–MD11 L and provide the control signals for KL8-A operation. The 7442 ICs are BCD to decimal decoder which grounds one output line for each combination of inputs. For example, if MD9 L is low (1), MD10 L is high (0), MD11 L is high (0), (100), and MD8 L is high (0). Pin 4 of the even Instruction Decoder is grounded. The MSXD instruction was executed by the program.

4.2.3 C Line Control Logic

CO L and C1 L are asserted (low) by the KL8-A to transfer data into the AC via the Data Bus (Figure 4-7).

4.2.4 Interrupt and Skip Logic

The interrupt logic is used to interrupt the program for a data transfer during receive and transmit operations. The SKIP logic allows the program to skip an instruction when certain events occur (i.e., a flag sets).

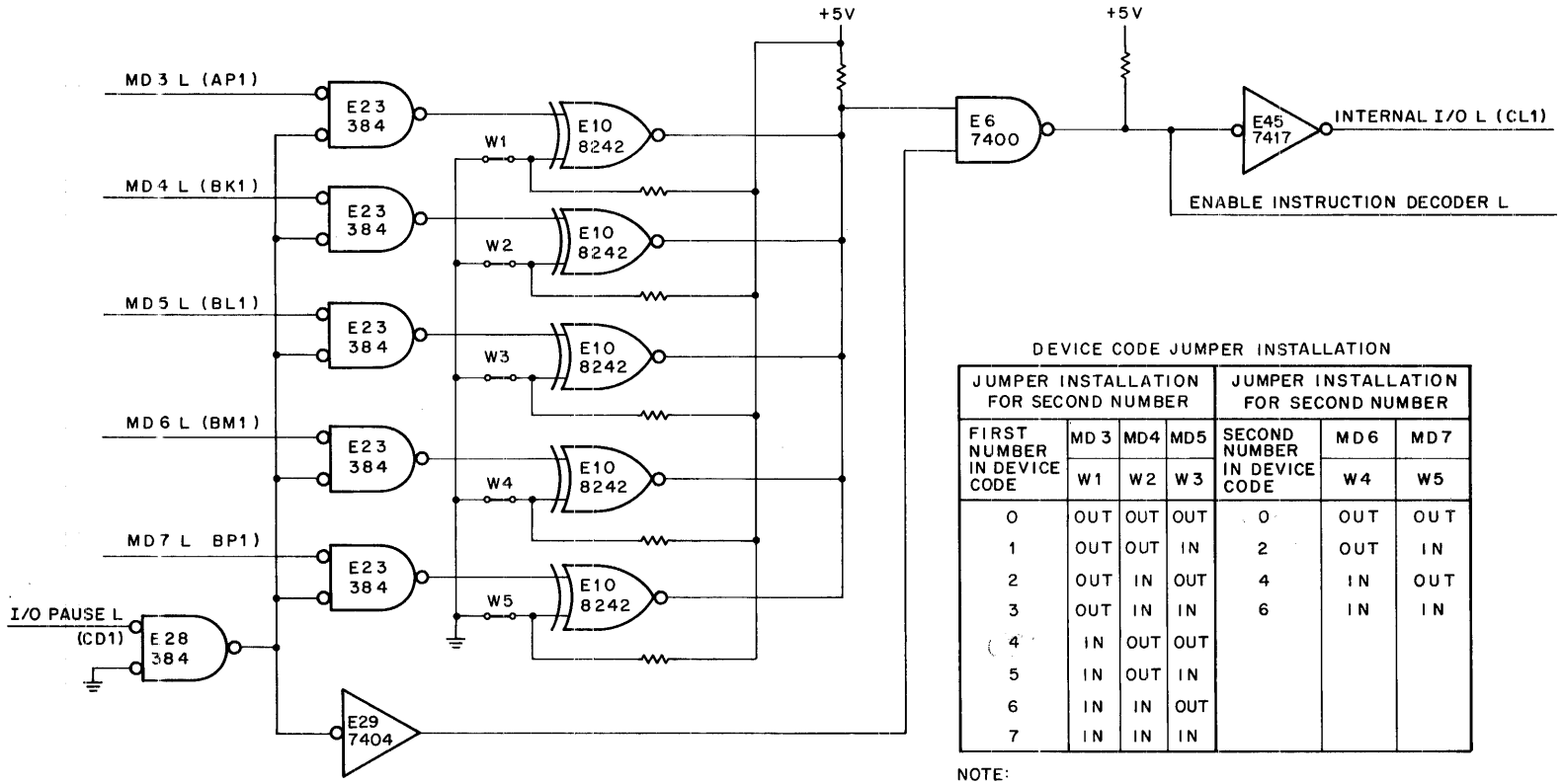
4.2.5 Interrupt Logic

Interrupts are enabled by a one being transferred from AC11 via the Data Bus (DATA11 L) when the program executes the MSIE instruction. This allows INT RQST L to be asserted low when one of the following occurs:

1. The RECV CHARACTER flag sets (Figure 4-8). RECV CHARACTER is set (1) when there is a character in the FIFO register. A OR H and B OR H (output ready) are asserted high when there is a character in the FIFO register. (Figure 4-8).

2. The XMIT flag (Figure 4-8) sets to indicate one or more of the UARTs are ready for a new character. The line to be serviced when there is more than one UART ready for another character is determined by the transmit priority encoder (see paragraph 4.2.14).

3. If any of the RING flags (R0-R3) for lines 0, 1, 2, or 3 sets (Figure 4-9).



DEVICE CODE JUMPER INSTALLATION

JUMPER INSTALLATION FOR SECOND NUMBER				JUMPER INSTALLATION FOR SECOND NUMBER		
FIRST NUMBER IN DEVICE CODE	MD 3	MD4	MD5	SECOND NUMBER IN DEVICE CODE	MD6	MD7
	W1	W2	W3		W4	W5
0	OUT	OUT	OUT	0	OUT	OUT
1	OUT	OUT	IN	2	OUT	IN
2	OUT	IN	OUT	4	IN	OUT
3	OUT	IN	IN	6	IN	IN
4	IN	OUT	OUT			
5	IN	OUT	IN			
6	IN	IN	OUT			
7	IN	IN	IN			

NOTE:
MD8 selects odd or even instruction decoder.

08-1433

Figure 4-5 Device Select Decoder

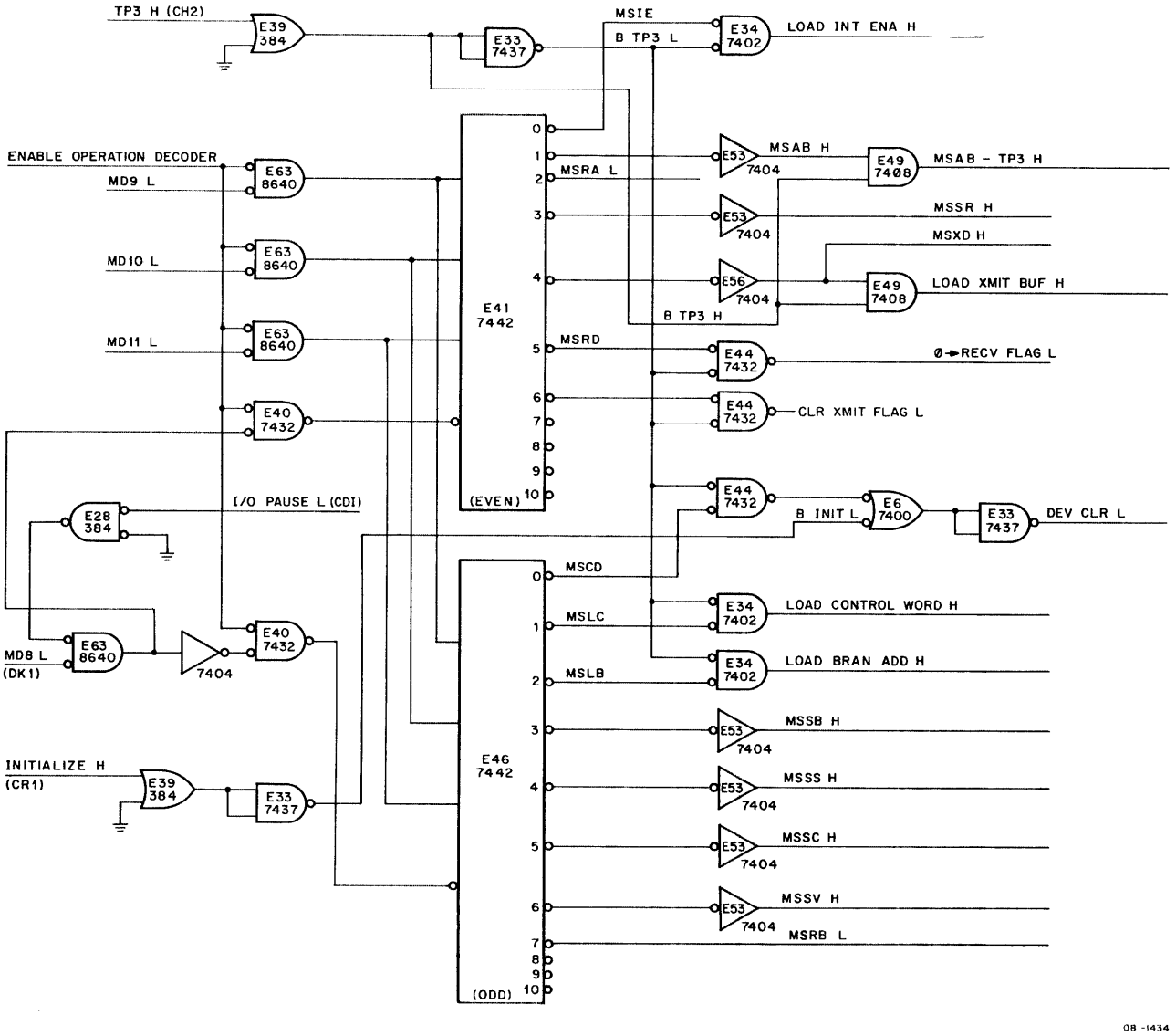


Figure 4-6 Instruction Decoders

4. If any of the following line 3 flags set.

   a. CARRIER B

   b. CTS (clear to send)

   c. SECONDARY RECV

Note that these last three flags set anytime there is a change in the status of the CLR TO SEND, CARR L3 or SECONDARY RECV L3 flags. This is accomplished by clocking each flag with the output of two one-shots. One of the one shots receives an input directly and the input to the other one shot is inverted. The one-shots are triggered when the input signals make a positive to negative transition or negative to positive. Thus, any change in the level of the input signal sets the flag.

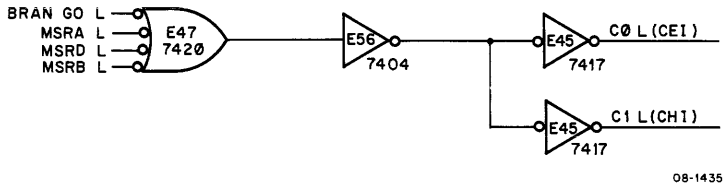


Figure 4-7 C Line Control Logic

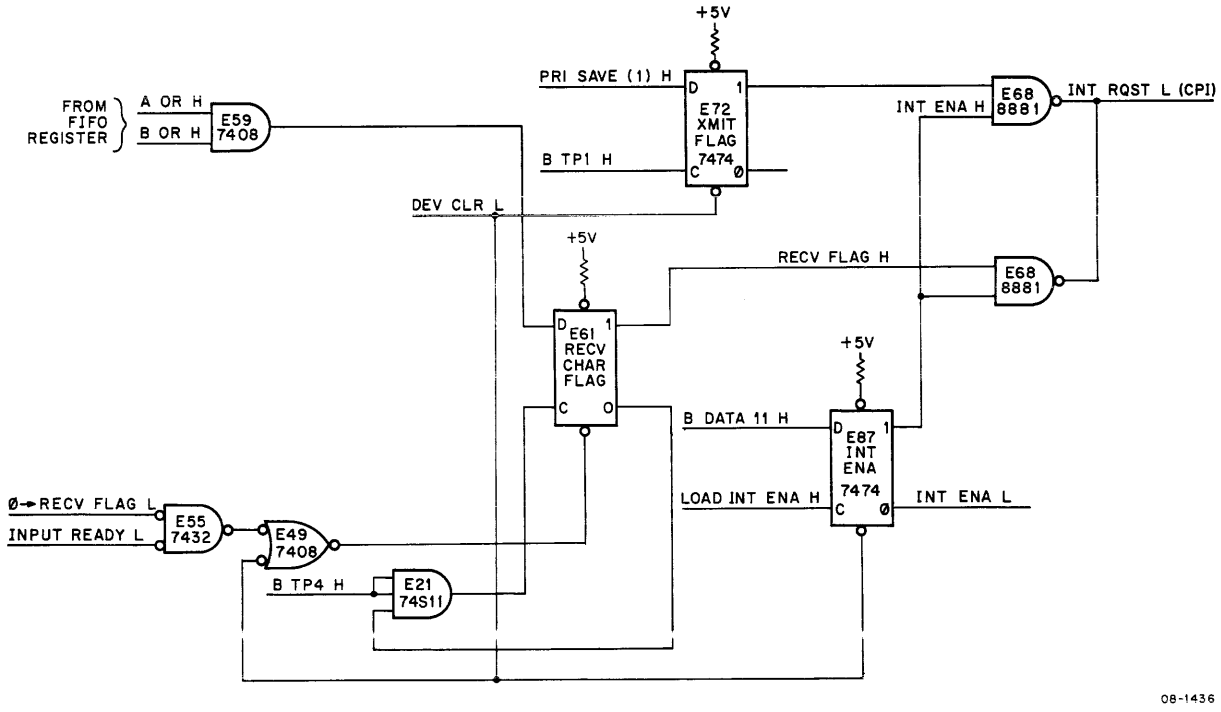


Figure 4-8 Transmit and Receive Interrupt and Skip Logic

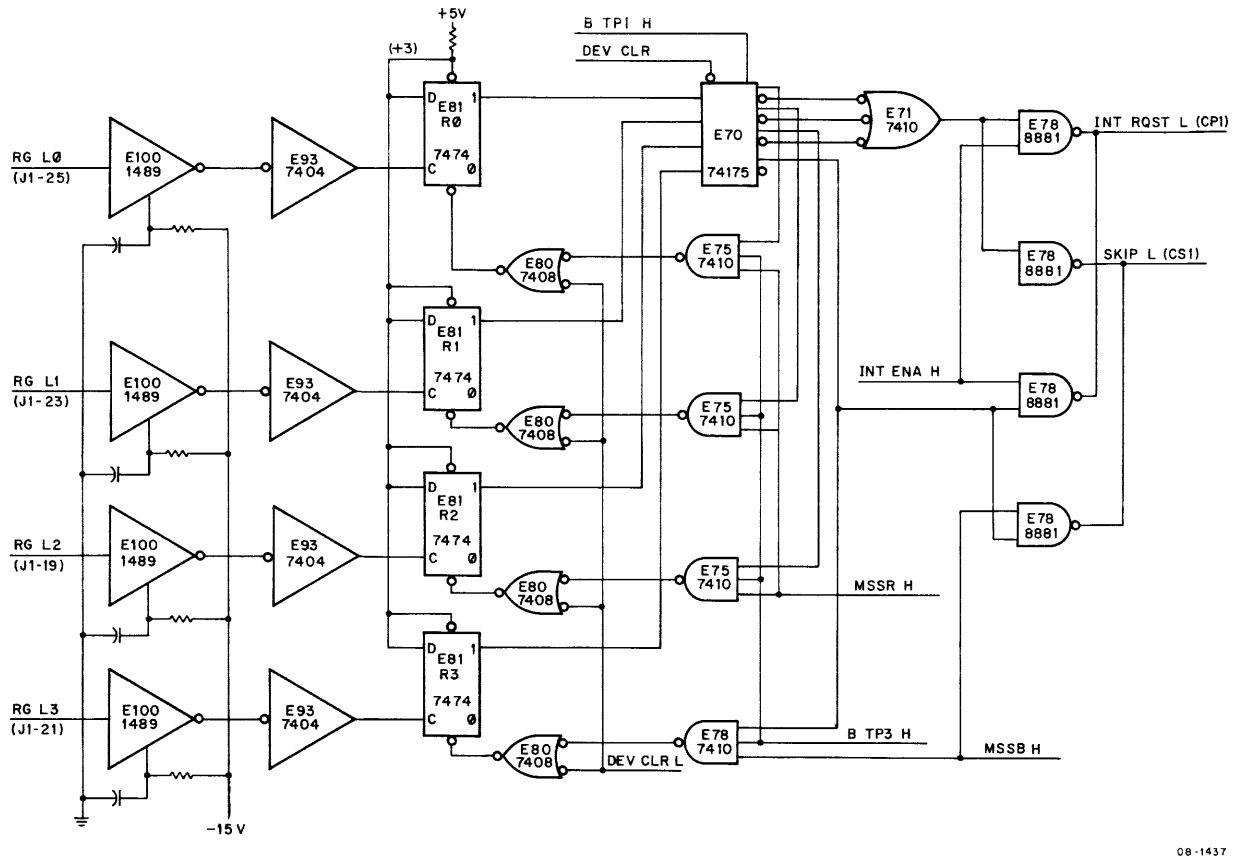


Figure 4-9 Ring Interrupt and Skip Logic

4.2.6 Skip Logic

If SKIP L is asserted (low), the program skips the next instruction (Figures 4-9 and 4-10). In the KL8-A, SKIP L may be asserted when one of the following occurs:

1. If the program executes the MSSR instruction and the RING flag for line 0, 1, or 2 (Figure 4-9) is set (1).
2. If the program executes the MSSB instruction and the RING flag (R3) for line 3 is set (1).
3. If the MSSC instruction is executed, the program and the L3 CARRIER flag (Figure 4-10) is set (1).
4. If the MSSG instruction is executed by the program and the CTS flag (Figure 4-10) for line 3 is set (1).
5. If the MSSV instruction is executed by the program and the SECONDARY RECV flag (Figure 4-10) is set (1).

4.2.7 Universal Asynchronous Receiver Transmitter (UART)

The UART (Figure 4-11) is a full duplex device with a receive and transmit section. There are four of these UARTs on the KL8-A, one for each KL8-A line. The receiver section accepts serial binary characters from a serial device and converts them to parallel format for transfer to the AC via the FIFO register and the Data Bus. The transmitter section receives data in parallel format from the AC via the Data Bus and converts it to serial form for output to a serial device. Table 4-1 lists the signals required to operate each of the UARTs in the KL8-A. The receiver block diagram (Figure 4-4) and transmit block diagram (Figure 4-2) should be used to understand functional logic inside the UART.

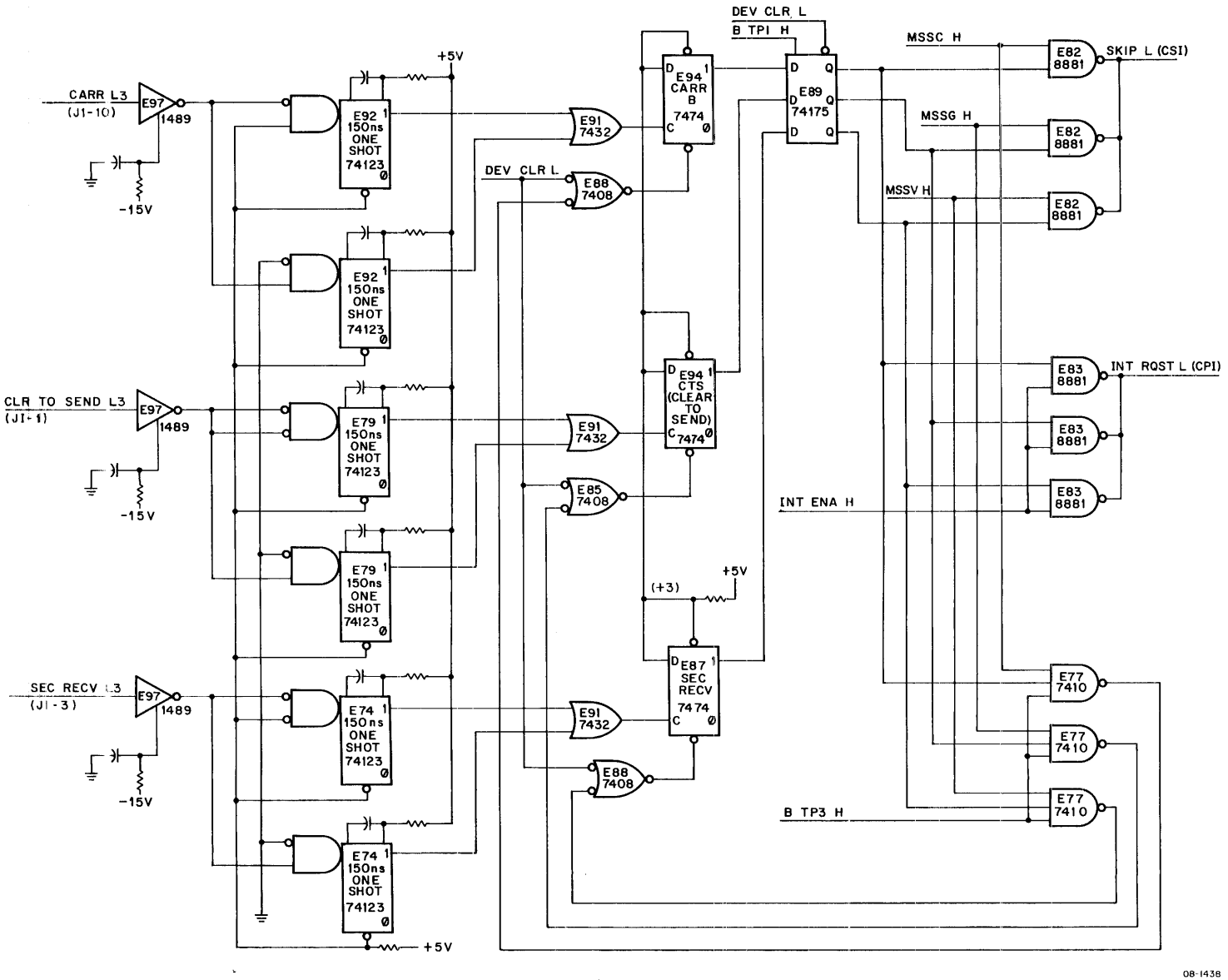


Figure 4-10 Line 3 Interrupt and Skip Logic

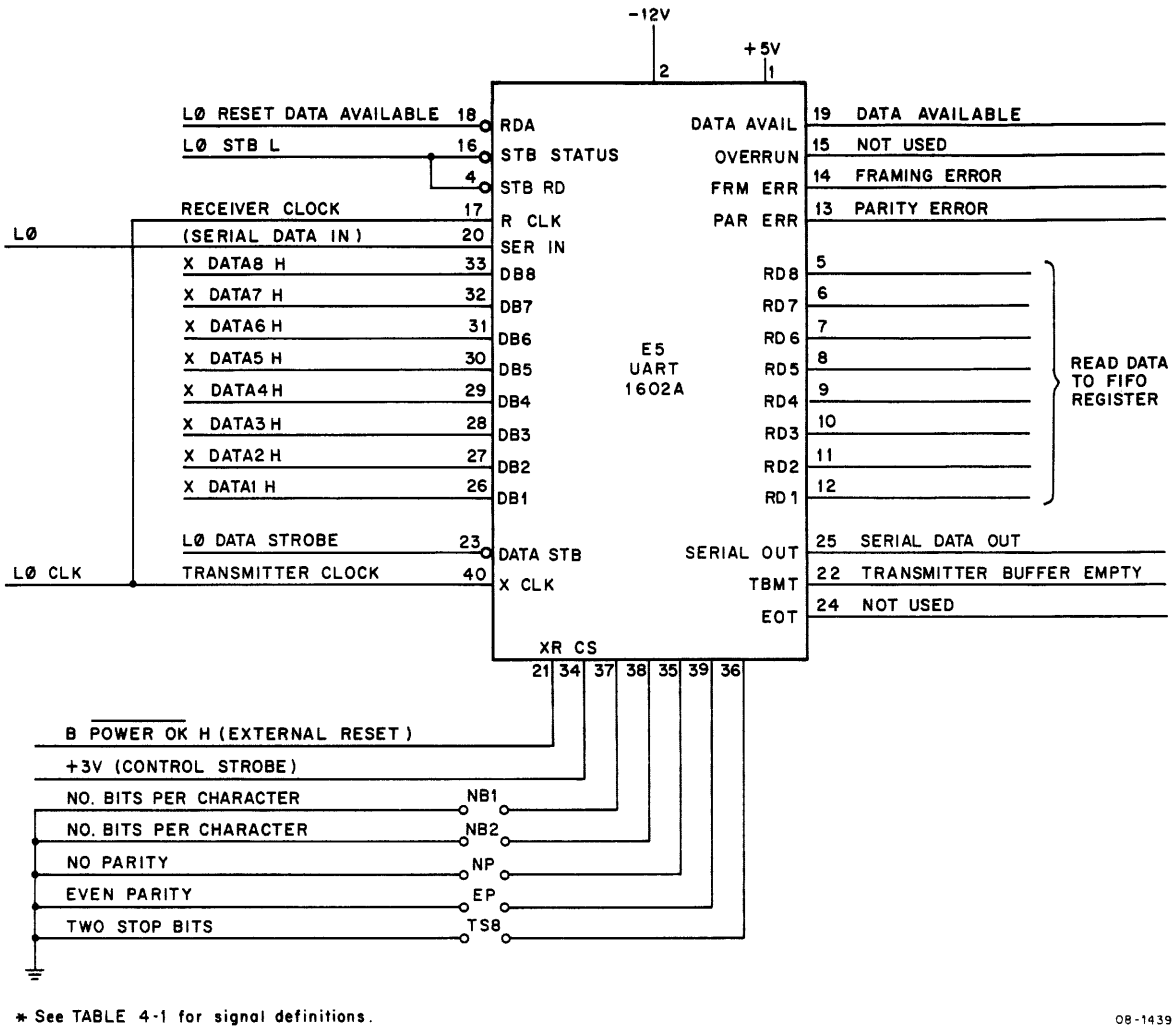


Figure 4-11 Universal Asynchronous Receiver Transmitter (UART)

4.2.8 UART Receive Operation

EIA or 20 mA serial data is received from a serial device (Figures 4-10 and 4-11) and converted to TTL levels. Each data character contains a start bit, 5, 6, 7, or 8 data bits and one or two stop bits (Figure 4-10). The number of data bits and stop bits is jumper selectable (Table 4-1). The stop bits are opposite in polarity to the start bits.

The converted EIA or 20 mA serial input is used to supply an input to SERIAL IN on the UART.

When the receiver is in the idle state it samples the serial input at the selected clock edges after the first low to high transition of the serial input. If the first sample is high, the receiver remains in the idle state and is ready to detect another low to high transition. If the sample is low, the receiver enters the data entry state.

Received data may be checked for even or odd parity (Table 4-1).

The serial data is shifted into the UART a bit at a time and the occurrence of a stop bit indicates that the entire character has been received and shifted into the Shift register. After the stop bit(s) is sampled, the receiver control logic parallel transfers the content of the shift register to the Data Holding register and asserts Master Reset (MSTR) and DATA AVAIL H. DATA AVAIL H is allowed to go high only when the scanner selects the UART by asserting RDE and STB STATUS while the STB L signal is low.

Table 4-1
UART Signal Functions

Pin No.	Mnemonic	Name	Function
4	RDE	Received Data Enable	A low on this line enables the received to the Output lines (RD1–RD8).
5–12	RD1–RD8	Received Data	Eight data out lines: RD8 (pin 5) is the MSB, and RD1 (pin 12) is the LSB. When 5, 6, or 7 bit character is selected, the most significant unused bits are low. Character is right justified into the least significant bits.
13	PAR ERR	Receive Parity Error	High if the received character parity does not agree with the selected parity.
14	FRM ERR	Framing Error	High if the received character has no valid stop bit.
15	OR ERR	Overrun	Not used.
16	STB STATUS	Strobe Status	Asserted low to enable status information out to TBMT, DATA AVAIL, PARITY ERR, and FRM ERR.
17	R CLK	Receiver Clock	Input for an external clock whose frequency must be 16 times the desired receiver baud rate.
18	RDA	Reset Data Available	When low, resets the received DA (Data Available) line.
19	DATA AVAIL	Received Data Available	Goes high when an entire character has been received, transferred to the UART receiver Holding register and is waiting to be transferred to the FIFO register. Enabled out of the UART by STB STATUS.
20	SER IN	Serial Input	Input for serial asynchronous data. (Figure 4-3)
21	XR	Clear (reset)	When power is turned on, this line is pulsed high by POWER NOT OK H which resets all registers, sets serial output line high, and sets transmitter buffer empty line high.
22	TBMT	Transmitter Buffer Empty	Goes high when the transmitter Data Holding register in the UART may be loaded with another character. Enabled out of the UART by STB STATUS.
23	DATA STB	Data Strobe	Pulsed low to load the data bits into the transmitter Data Holding register in the UART during the positive-going trailing edge of the pulse.
24	EOC	End of Character	Not used.

Table 4-1 (Cont)
UART Signal Functions

Pin No.	Mnemonic	Name	Function
25	SERIAL OUT	Serial Output	Output for transmitted character in serial asynchonous format. A mark is high and a space is low. Remains high when no data is being transmitted.
26–33	DB1–DB8	Data Input	Eight parallel data in lines. DB8 (pin 33) is the MSB and DB1 (pin 26) is the LSB. If 5, 6, or 7 bit characters are selected, the least significant bits are used.
34	CS	Control Strobe	Not used.
35	NP	No Parity	When high, eliminates the parity bit from the transmitted and received character and drives the received parity error line low. As a result, the receiver does not check parity on reception and during transmission the stop bits immediately follow the last data bit.
36	2 SB	Two Stop Bits	Selects the number of stop bits that immediately follow the data bits. A low inserts 1 stop bit and a high inserts 2 stop bits.
37, 38	NB2, NB1	Number of Bits per Character	Select 5, 6, 7, or 8 data bits per character as follows. **Bits/Char** — **NB2 (37)** — **NB1 (38)** 5* — L — L 6 — L — H 7 — H — L 8 — H — H *Gives 1.5 stop bits if 5 characters selected.
39	EP	Even Parity Select	Selects the type of parity to be added during transmission and checked during reception. A low selects odd parity and a high selects even parity.
40	X CLK	Transmitter Clock	Input for an external clock whose frequency must be 16 times the desired transmitter baud rate.

The timing for this operation is shown in Figure 4-12. At this time the character is transferred to the FIFO register along with the line number and the ERROR status (Paragraph 4.2.10).

4.2.9 UART Transmit Operation

A transmit operation (Figure 4-13 and 4-16) is started when a parallel data character is transferred to the UART Data Holding register from the AC. The XMIT Buffer register is loaded by an MSXD instruction at TP3 H time. The data is then loaded into the Data Holding register during TS4.

If the UART transmitter is idle, the data is immediately transferred from the Data Holding register into the Shift register by the UART control logic. During this transfer the internal UART control logic will add parity or no parity, the stop bits, and provide for the correct number of data bits. The format is determined by the jumpers installed on the UART (Table 4-1). After the transfer is complete, TBMT is gated out by the STB STATUS signal on the UART which is asserted by STB L. TBMT sets its respective latch which then raises the XMIT flag. At this time the program is interrupted for another data transfer. Note that the line with the highest priority is serviced first (Paragraph 4.2.14).

The transmit flag is always cleared during a power up or initialize operation.

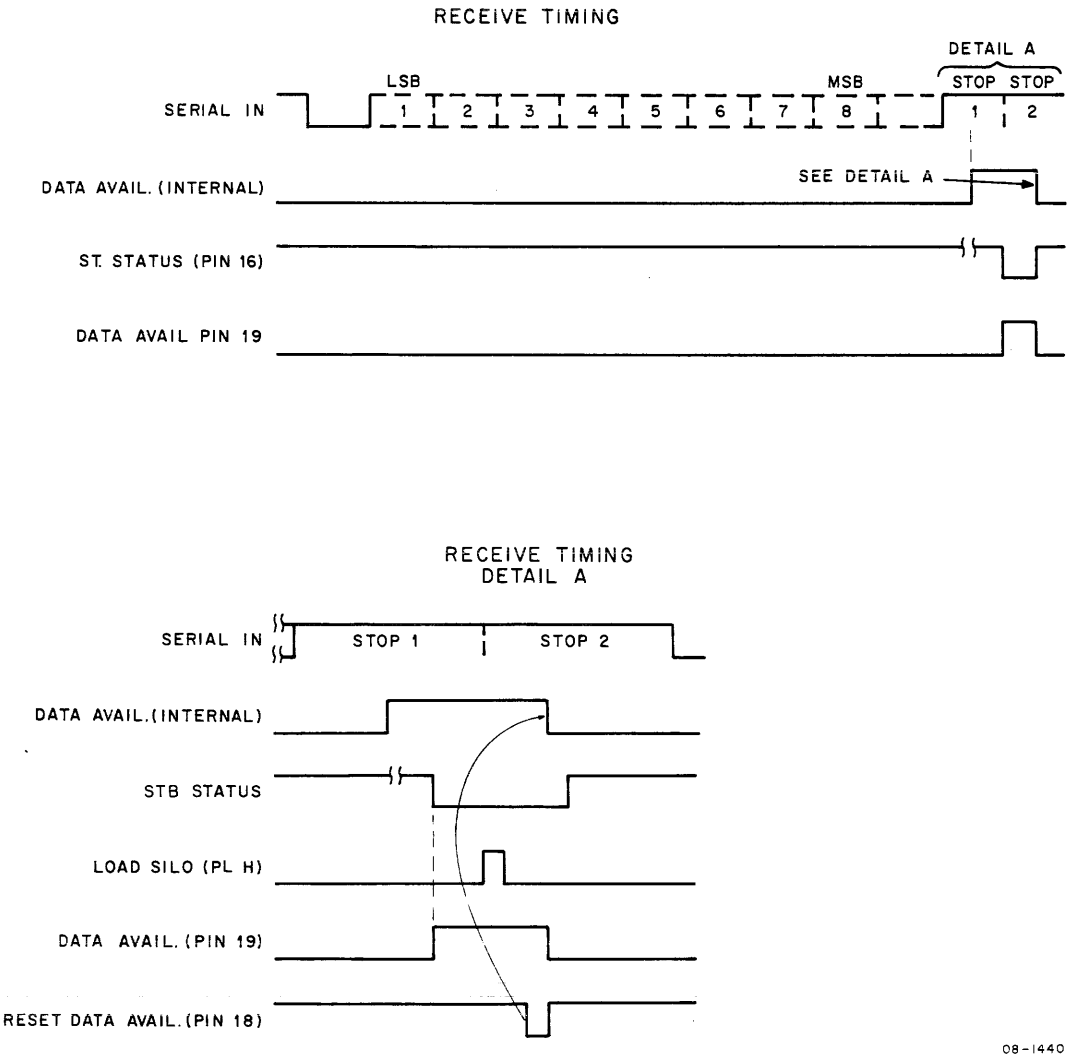


Figure 4-12 UART Receiver Timing

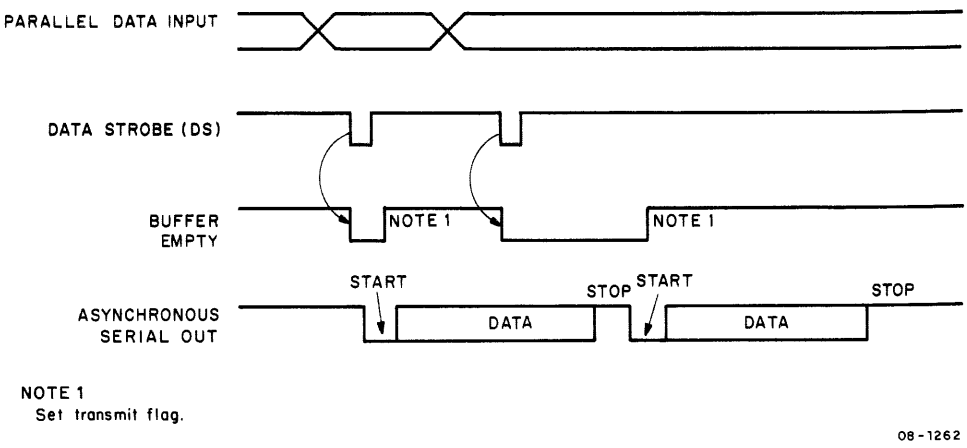


Figure 4-13 UART Transmitter Timing

4.2.10 First In First Out (FIFO) Register

The FIFO register (Figure 4-14) is a 12 X 32 bit Holding register for received data, line number, and error status bits associated with the received character (Figure 3-3).

The FIFO register consists of two 2812A First In First Out memory devices (Figure 4-15). An explanation of the register control signals, inputs, and outputs are explained in Table 4-2. When the FIFO register is loaded with a data word, it automatically ripples through the register until it reaches the output or another data word. An Output Ready (OR) signal indicates that data is available for transfer to the AC. When the FIFO register is not full, the Input Ready signal being low indicates that the FIFO register is ready to accept data. The IR signal is high when the FIFO register is full.

PL H is asserted on the FIFO register (Figure 3-14) and it is loaded when DATA AVAIL H is asserted by one of the four UARTs (Table 4-1) at 03 time of the clock signal.

The FIFO register is cleared by DEV CLR L during power up or when INITILIZE is asserted by the CAF instruction or by the INIT key on the programmer's console or by the MSCD instruction.

4.2.11 Output Multiplexer

The Output Multiplexer (Figure 4-14) allows either the content of the Branch Address register when the MSAB instruction is executed by the program or the output of the FIFO register when the MSRD instruction is executed by the program to be applied to the Data Bus.

The jumpers on (E50) limit the Branch Address to only two addresses if they are installed (Figure 3-6). In this configuration the line number is always 00, thus there will be only two Branch Addresses, one for transmit and one for receive.

4.2.12 XMIT Buffer Register

The XMIT Buffer register (Figure 4-16) is loaded with a data character and line number from the AC when the MSXD instruction is executed by the program. DATA 2 L and DATA 3 L are decoded by E4 a 74S139 IC to generate a strobe signal to load the content of the XMIT Buffer register into the UART of that line number. For example DATA2 L and DATA3 L both being low (1) asserts L3 DS L (low) and the content of the XMIT Buffer register is loaded into the UART for line 3 (Table 4-1).

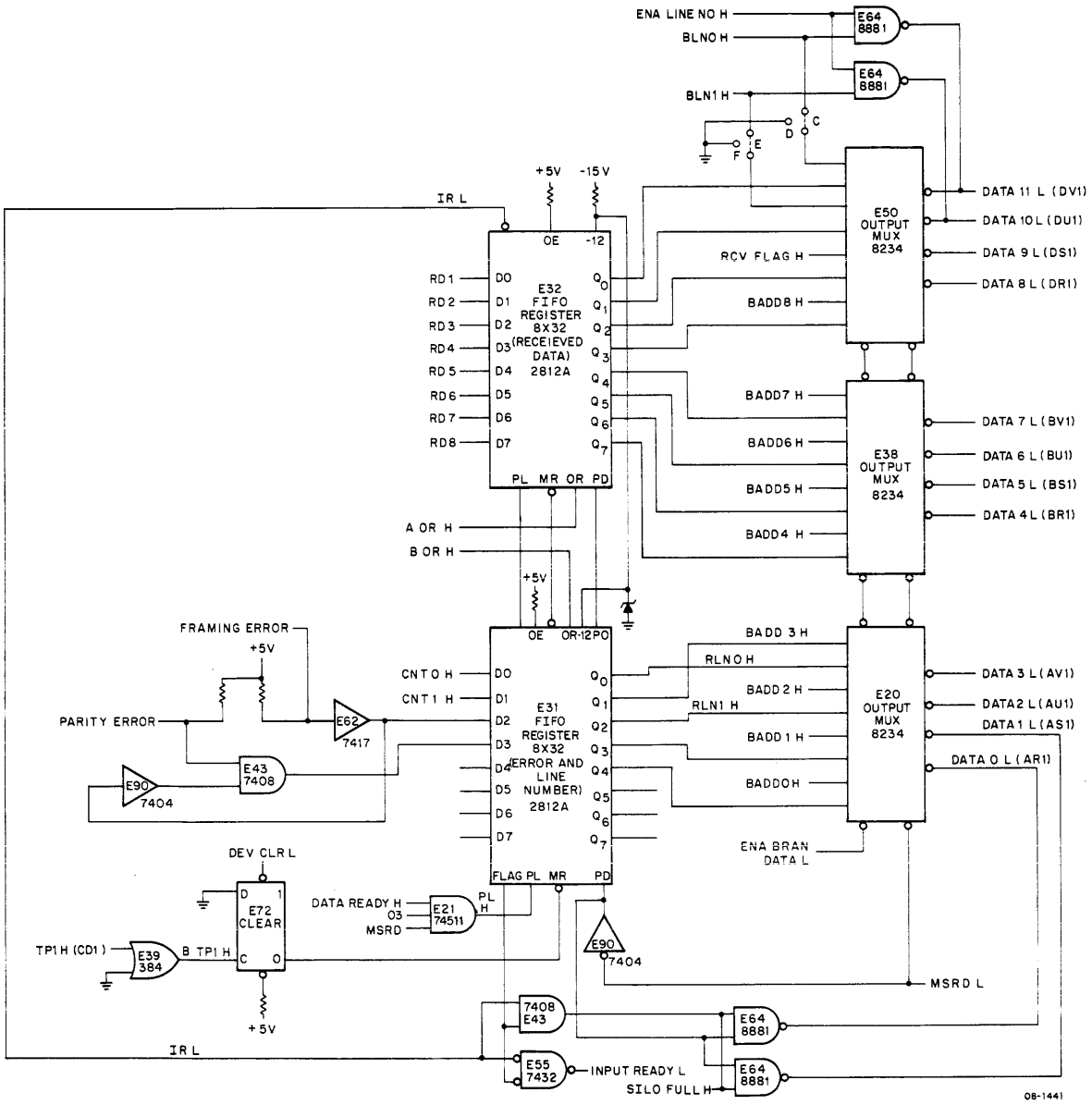


Figure 4-14 First-In First-Out Register

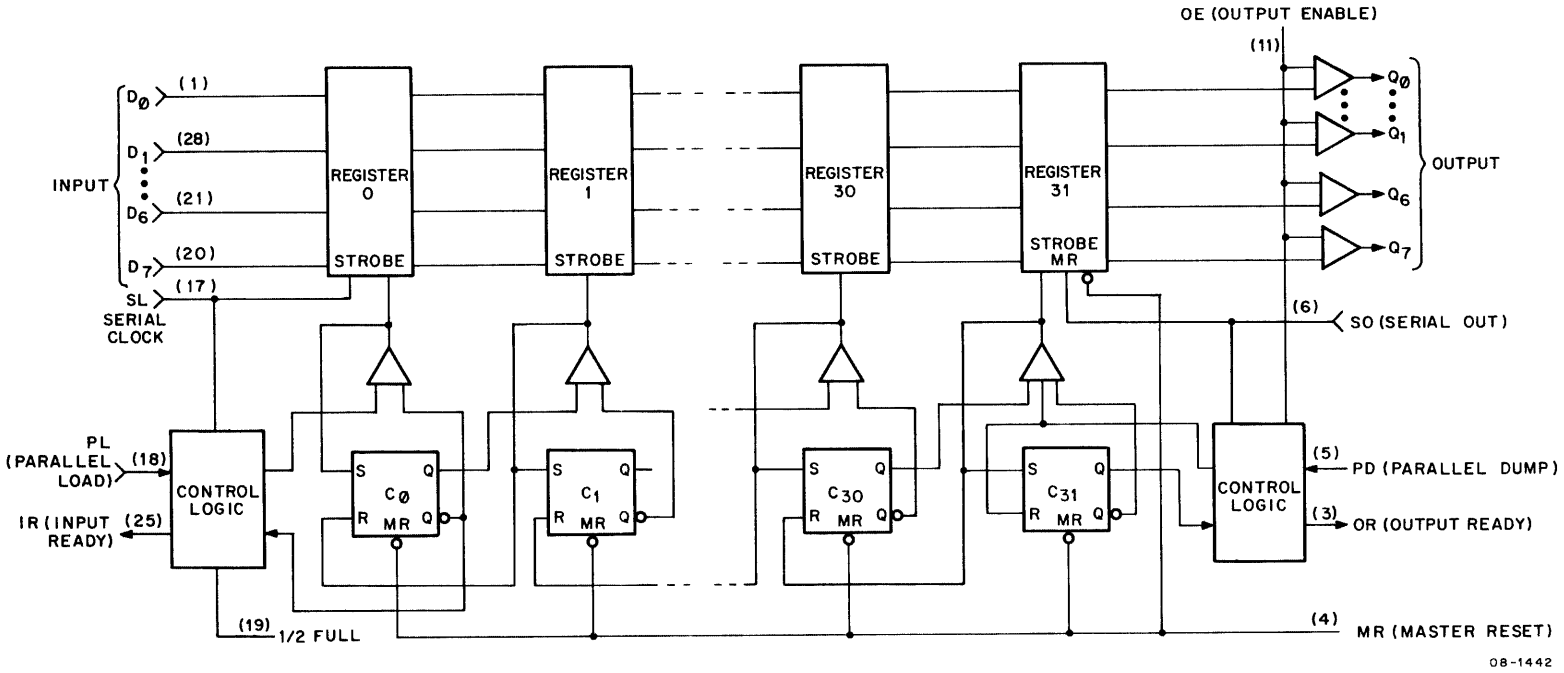


Figure 4-15 First-In First-Out Register Block Diagram

Table 4-2
FIFO Register Signals

Mnemonic	Name	Function
IR L	Input Ready	The IR L signal is asserted (low) when the FIFO register is ready to receive data. IR L being high is an indication that the FIFO register is full.
PL H	Pulse Load	PL H is asserted high to transfer the output of the UART into the FIFO register.
SL	Serial Clock	Not used.
1/2 FULL	1/2 FULL	Not used.
D0–D7	DATA0–DATA7	8 bits of received data from the UART.
CNT0–CNT1	Count0 and Count1	CNT0 and CNT1 is a binary number that is read into the FIFO register the same time as the data bits to indicate the line number on which the data was received (Figure 3-3).
OR H	Output Ready	OR H is asserted high when there are one or more words available for transfer to the AC.
OE	Output Enable	OE is tied to +5 V which enables the output of the FIFO register to be enabled at all times.
PL	Pulse Load	Pulse Load is asserted (high) to transfer a word in the FIFO register to the data output multiplexer.
MR	Master Reset	Clears (empties) the FIFO register.

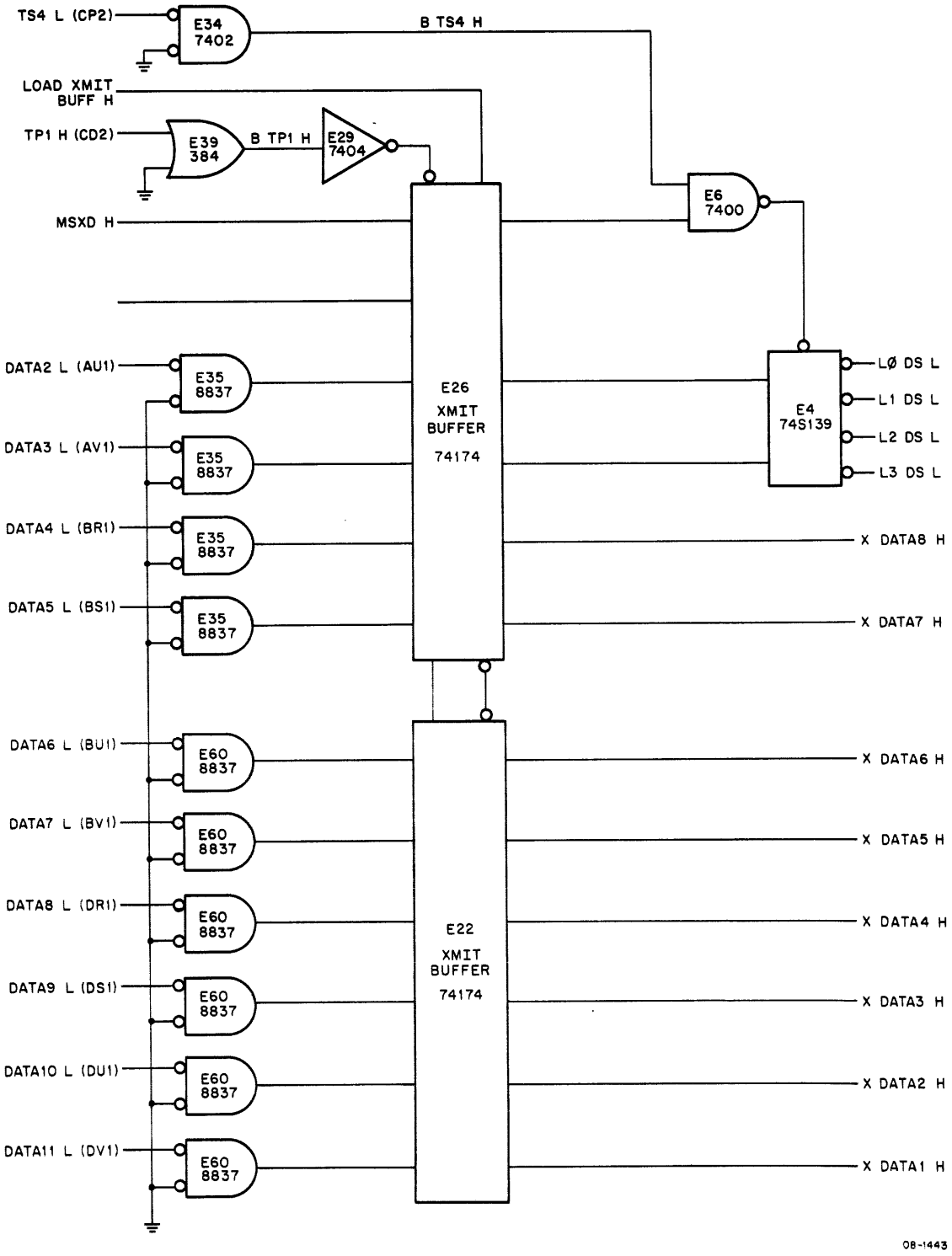


Figure 4-16 XMIT Buffer Register

4.2.13 Receive Line Multiplexer and Scanner Logic

The Receive Line Multiplexer and Scanner logic shown in Figure 4-17 generate the control signals to transfer a received character to the FIFO register and supply the line number of the line that received the data. This logic generates a strobe signal to transfer a character from the UART and provides the PL H signal to load the FIFO register. Figure 4-18 shows the timing required for this operation.

The RDA flip flop (E8) is cleared during 01 time to ensure that only the line being strobed by the strobe signal (i.e., L0 STB L) is the line that supplied DATA AVAIL to set RDA. The RDA input is asserted to clear the UART DATA AVAIL during 04 time (Table 4-1) so that the UART can accept another input character.

The Scanner supplies a two-bit line number, CNT0 H and CNT1 H, which corresponds to the line number of the line that has its strobe signal applied to the UART for that line. As an example, if L1 STB L is asserted, the Priority Encoder outputs a binary 01 (see truth table in Figure 4-17).

The strobe signal (i.e., L0 STB L) is also applied to the Transmit Line Multiplexer and Priority logic (Paragraph 4.2.14) to enable the TBMT signal from the UART at the same time the MSTR DATA AVAIL is checked in the receive logic.

4.2.14 Transmit Line Multiplexer and Priority Encoder Logic

The Transmit Line Multiplexer and Priority Encoder logic (Figure 4-19) monitor the TBMT lines from the four UARTs, and supply the line number of the line with the highest priority to the Branch Address register when the program executes the MSAB instruction. The timing for this operation is shown in Figure 4-20.

The CATCH flag for a line sets during the time the strobe signal (i.e., L0 STB L) is asserted (low) if the TBMT signal from the UART is asserted (high). When the CATCH flag sets, the TBMT flag for that line sets and an input is supplied to the Priority Encoder. Anytime there is an input to the Priority Encoder, the EO signal is asserted high to set PRIORITY SAVE and at the next TP1 time the XMIT flag sets. The Priority Encoder may have more than one input as other UARTs assert their TBMT lines; thus the Priority Encoder outputs a two bit binary number which is the line numer of the line with the highest priority supplying an input to the encoder.

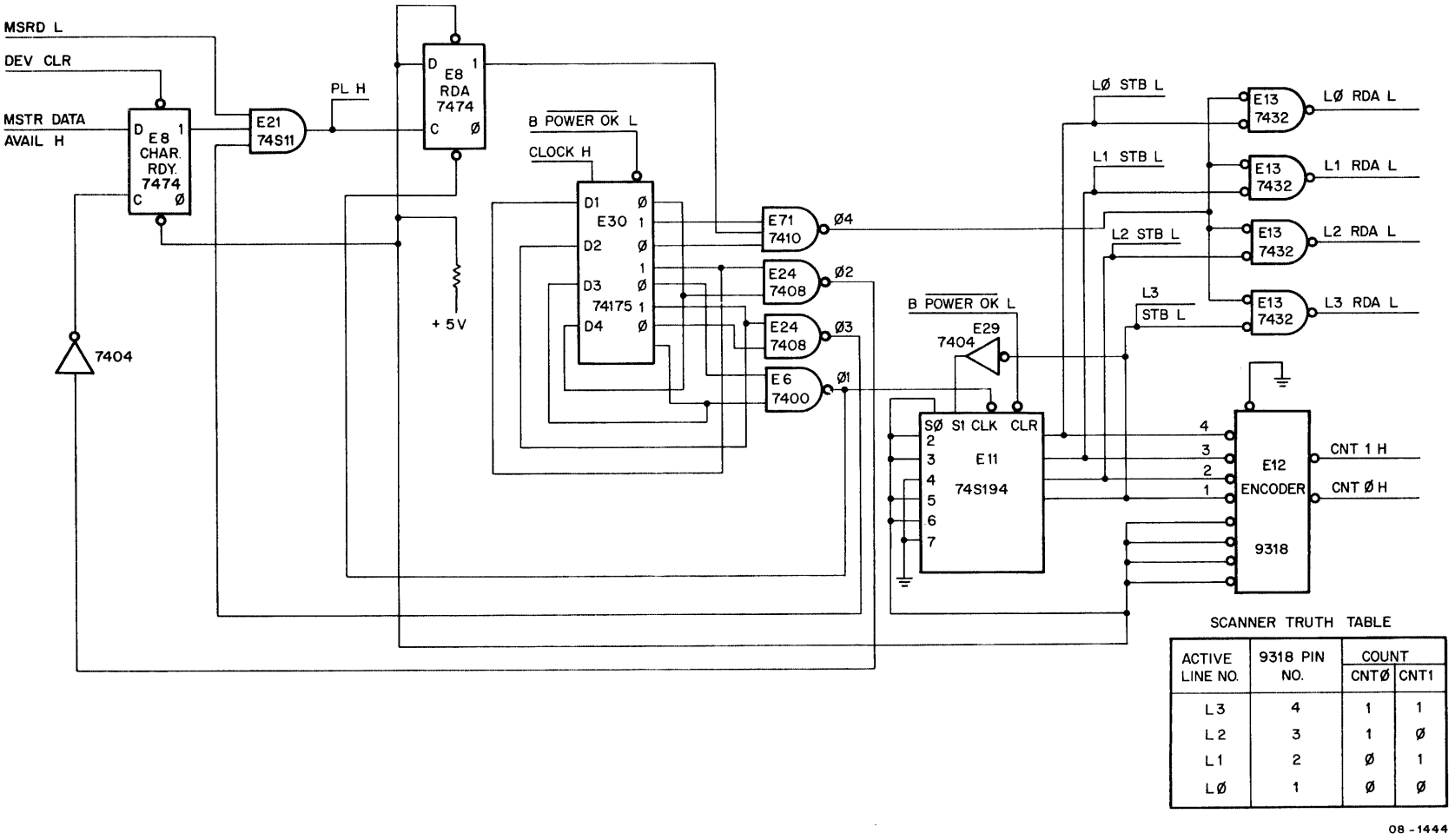
When the transmit flag sets, and the program executes the MSAB instruction, the line number is output to the AC 10 and 11. Note that if the RECV flag is set (1), a receive line number is transferred out of E37. Receive operations have higher priority.

The output of E4 clears the TBMT flag for the line with the highest priority of the same time the line number is supplied to the Branch Address register. The CATCH flag clears the next time that line is strobed if that line has been serviced by the program.

4.2.15 Branch Address Register and Control Logic

The Branch Address register (Figures 3-6 and 4-21) contains the nine most significant bits of the address of a location in memory. The other three bits of the address are determined by the line number which caused the interrupt and whether this is a transmit or receive operation. LOAD BRAN ADD H is asserted (high) to load the Branch Address register when the program executes the MSLB instruction to transfer the nine most significant bits of the Branch Address from the AC. The output of the Branch Address register is applied to the output Multiplexer (Figure 4-14) and is transferred to the Data Bus when the program executes the MSAB instruction.

The MSAB instruction enables the PC control logic (Figure 4-22) which generates the necessary control signals to transfer the address to the PC via the Data Bus. The timing required to load the PC is shown in Figure 4-23. Chapter 3 of the *PDP-8/A User's Manual* contains a detailed description of the timing required to load the PC and the Omnibus signals used in this operation.

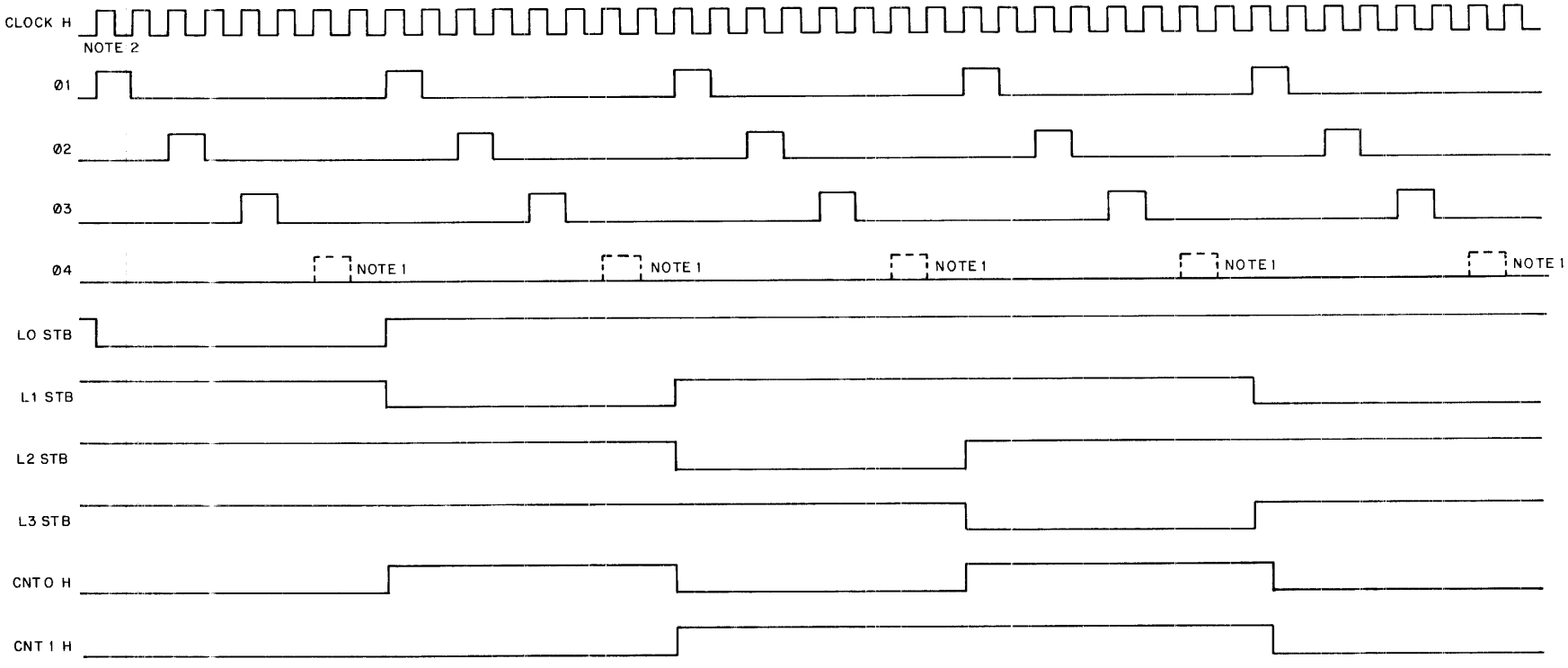


SCANNER TRUTH TABLE

ACTIVE LINE NO.	9318 PIN NO.	COUNT	
		CNTØ	CNT1
L3	4	1	1
L2	3	1	Ø
L1	2	Ø	1
LØ	1	Ø	Ø

08-1444

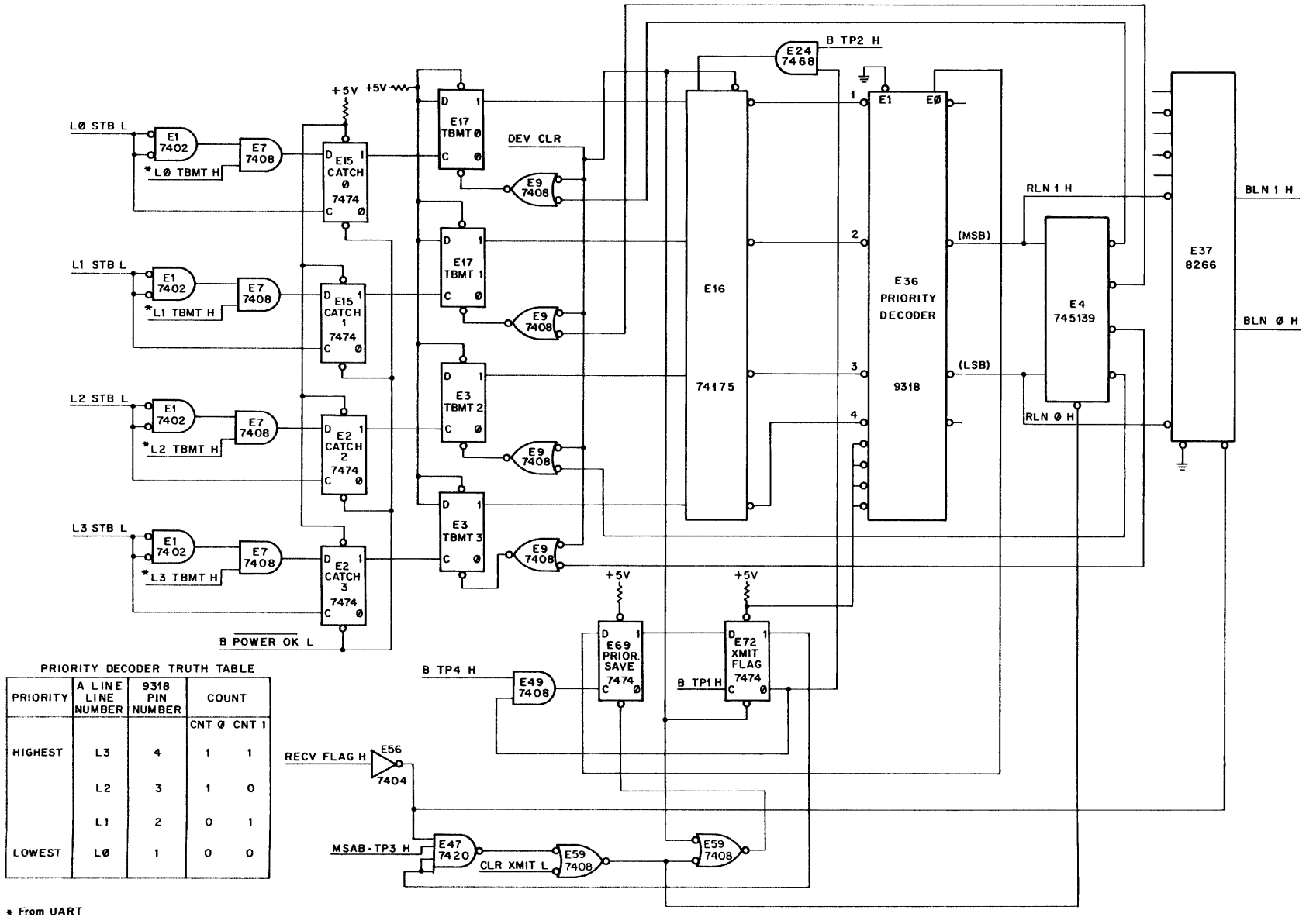
Figure 4-17 Receive Line Scanner Logic



NOTES:
1. Ø4 is true only if the RDA flip flop is set to a logical 1.
2. Clock frequency is 5.0688MHz.

08-1445

Figure 4-18 Receive Line Scanner Logic Timing



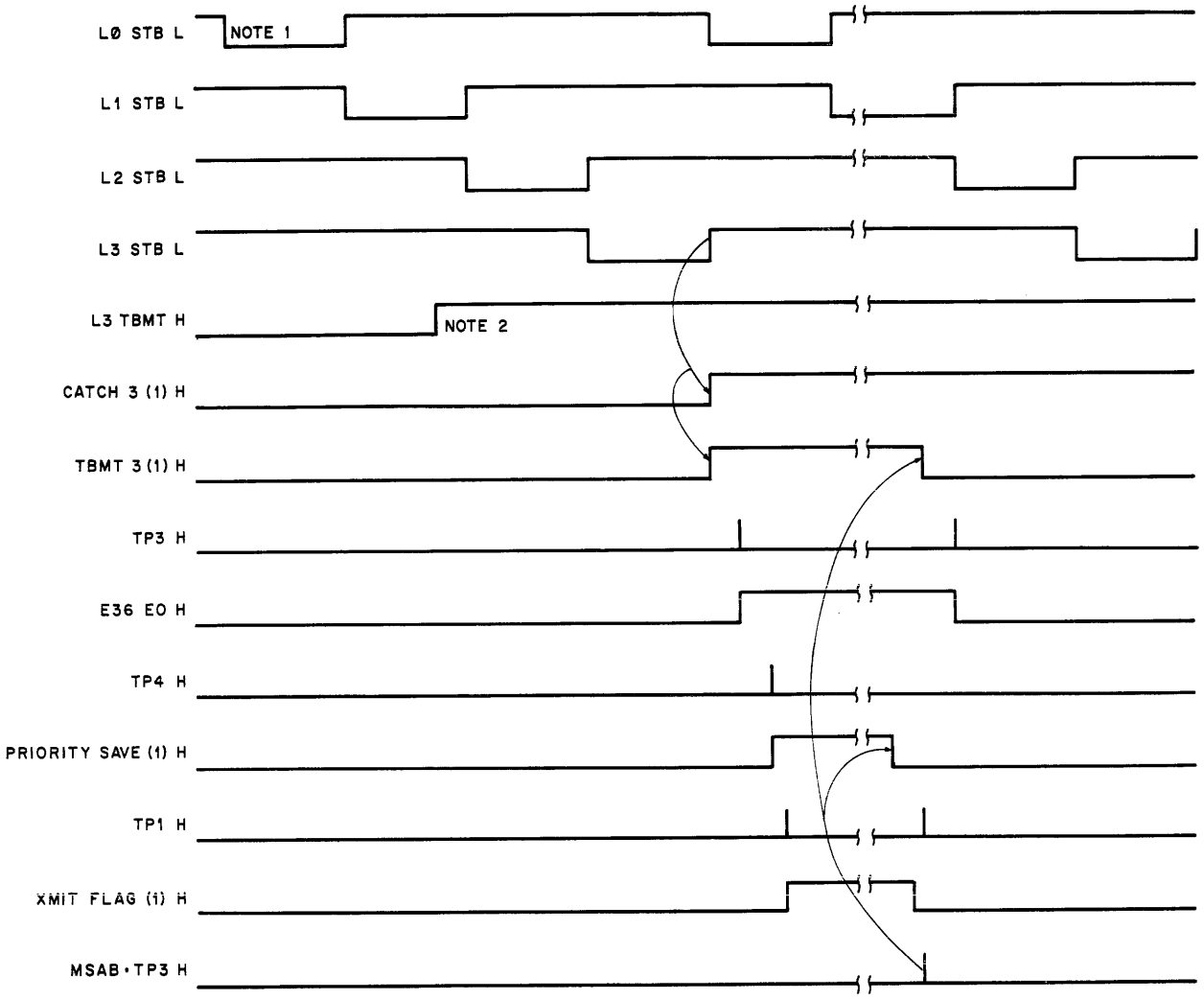
PRIORITY DECODER TRUTH TABLE

PRIORITY	A LINE LINE NUMBER	9318 PIN NUMBER	COUNT	
			CNT 0	CNT 1
HIGHEST	L3	4	1	1
	L2	3	1	0
	L1	2	0	1
LOWEST	L0	1	0	0

* From UART

08-1446

Figure 4-19 Transmit Line Multiplexer and Priority Logic



NOTE 1:
Timing for generation of strobe signals is shown in Figure 4-16

NOTE 2:
L3 TBMT can be asserted any time prior to L3 STB L time

08-1447

Figure 4-20 Transmit Line Multiplexer and Priority Logic Timing

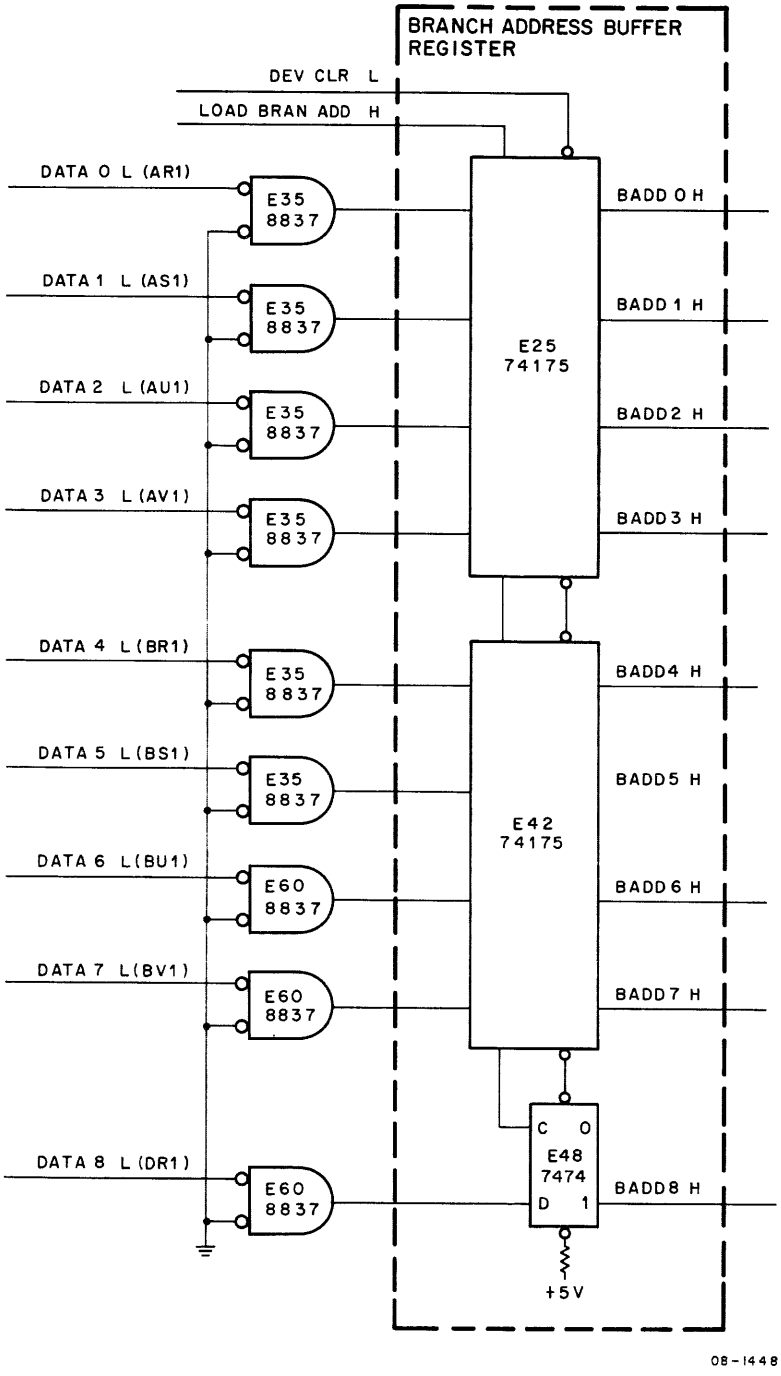


Figure 4-21 Branch Address Register

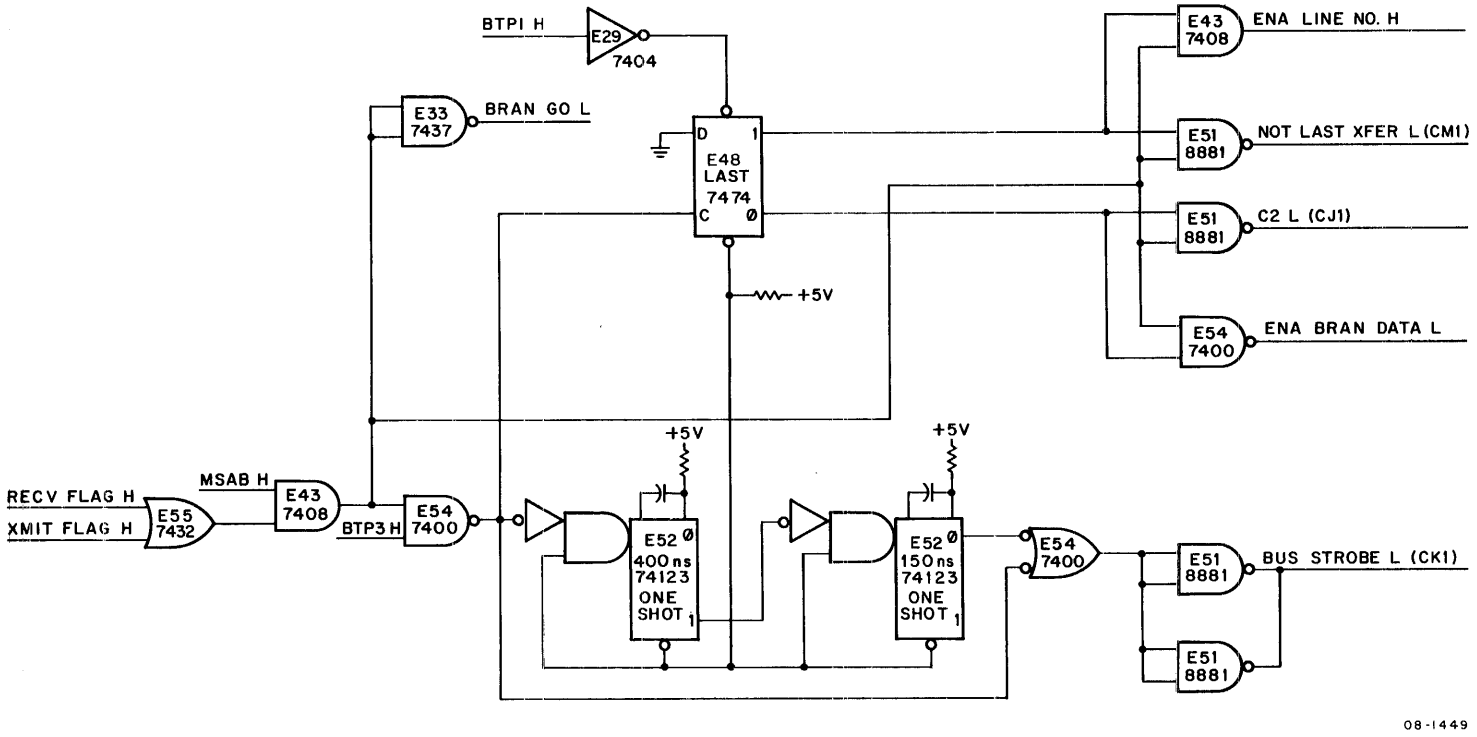


Figure 4-22 PC Loading Control Logic

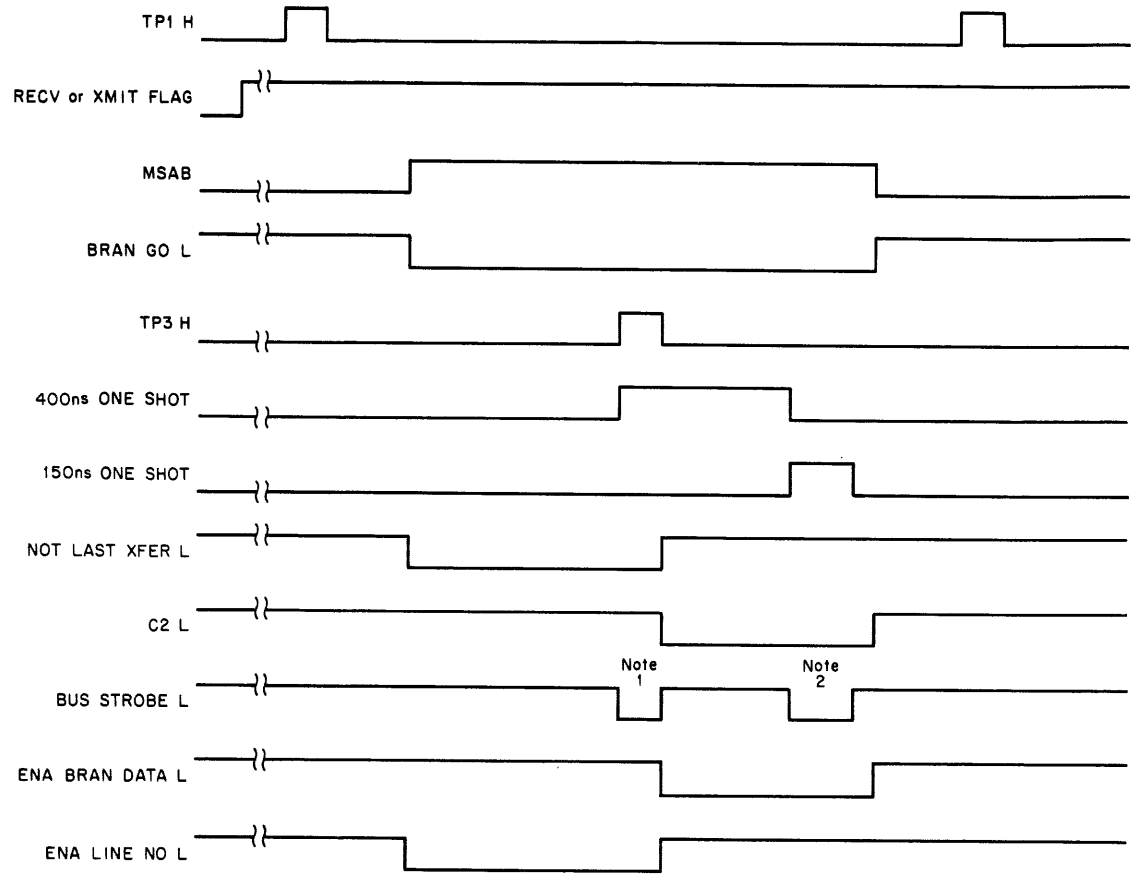


Figure 4-23 PC Loading Control Timing

4.2.16 Line 3 Control Register

The Line 3 Control register (Figures 3-4 and 4-24) is loaded from the AC by the MSLC instruction. Logical ones in the AC set control bits in the Control register. The outputs of the Control register assert control signals to the line 3 device allowing full modem control on this line. The output of the Control register is also applied to Status B register so that the status of these signals may be checked by the program (Figure 3-5).

4.2.17 Status A Register

The content of Status A register (Figures 3-1 and 4-24) is transferred to the AC using the MSRA instruction. This IOT transfers the condition of bits in the Status A register which indicate the status of lines 0, 1, and 2 and whether the FIFO register (silo) is full or not.

4.2.18 Status B Register

The content of Status B register (Figures 3-5 and 4-24) may be transferred to the AC using the MSRB instruction. This IOT transfers the condition of bits in the Status B register which indicate the status of line 3 and the condition of the bits in the control register.

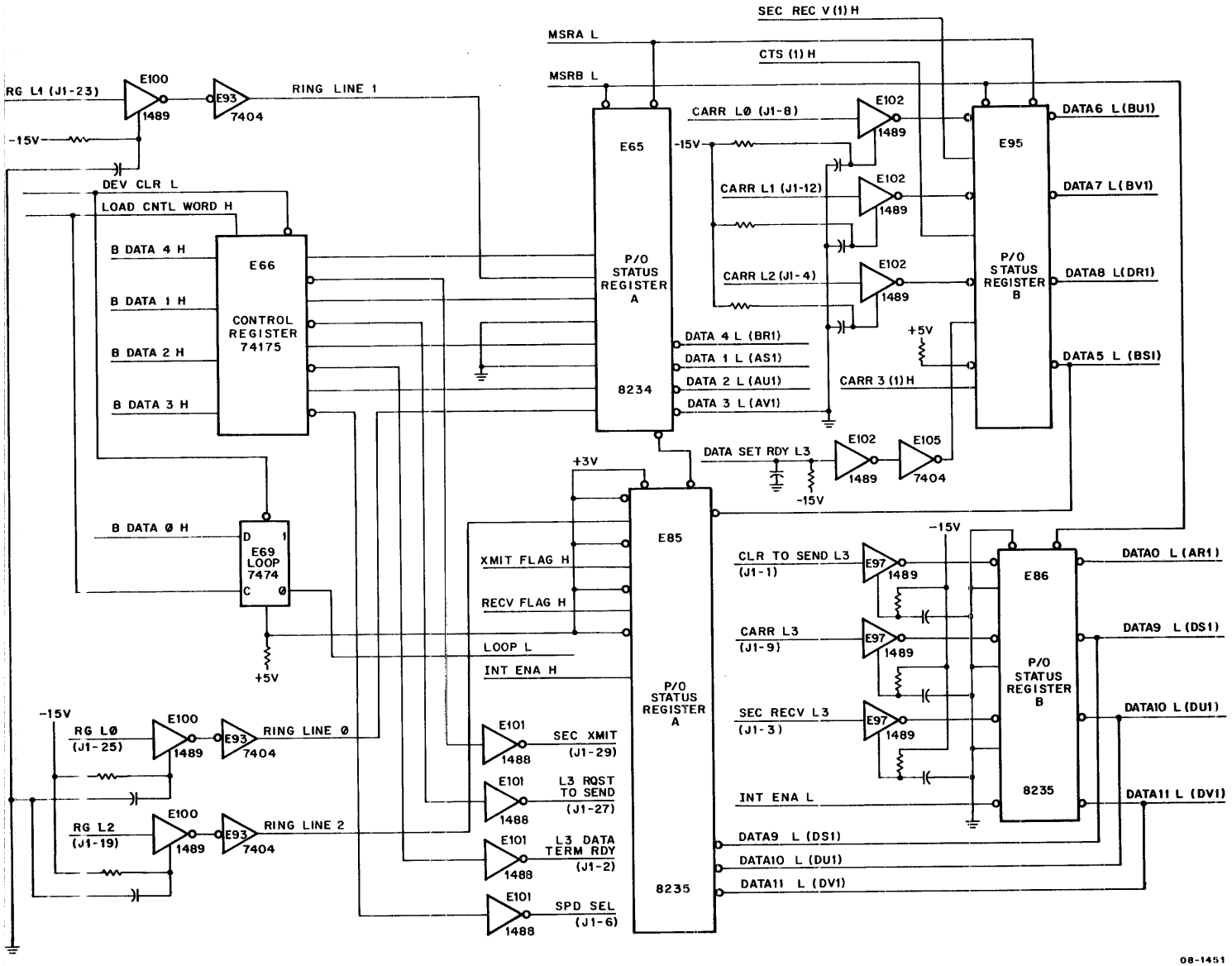


Figure 4-24 Control and Status Registers

4.2.19 Request to Send and Data Terminal Ready

The REQUEST TO SEND and DATA TERMINAL READY signals to lines 0, 1, and 2 are always asserted (Figure 4-25). The input to the 1488 ICS are grounded so that the output is asserted (high).

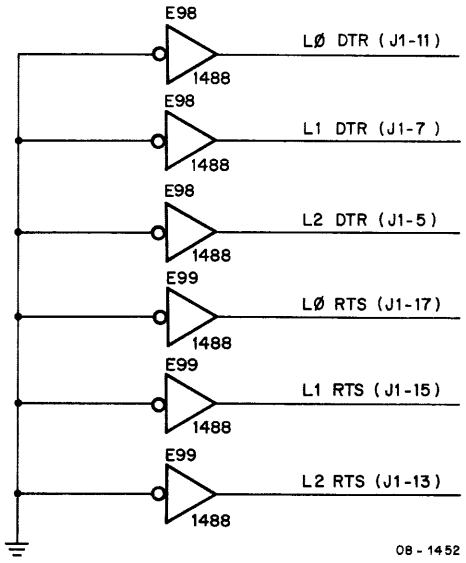


Figure 4-25 Lines 0, 1, and 2 REQUEST TO SEND and DATA TERMINAL READY Logic

4.2.20 Level Converters

Level conversions are provided on both the receive and transmit lines between TTL levels of ground and +3 V to either EIA levels of ±6 V or 20 mA current loop operation.

4.2.20.1 EIA to TTL Converter – The L1 receive EIA to TTL converter is shown in Figure 4-26. The 1489 IC converts ±6 V EIA levels to ground and +3 V levels. The EIA to TTL converters for lines 0, 2, and 3 are identical to line 1.

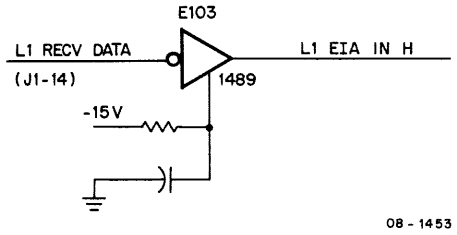


Figure 4-26 Receive EIA To TTL Converter

4.2.20.2 TTL to EIA Converter – The L1 TTL to EIA converter is shown in Figure 4-27. The 1488 IC converts ground and +3 V levels to +12 V and -12 V levels. The TTL to EIA converters for lines 0, 2, and 3 are identical to line 1.

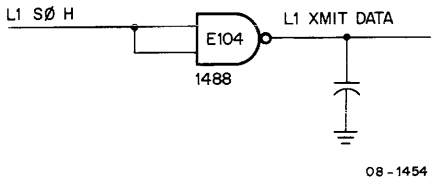


Figure 4-27 TTL To EIA Converter

4.2.20.3 Twenty mA to TTL Converter – The L1 20 mA to TTL converter is shown in Figure 4-28. Q15 and Q3 are turned off when no signal is present at the input. A current in the loop greater than 10 mA turns Q15 and Q3 on. The differential between RECV+ and RECV– are sensed by Q15 and Q3 amplified by Q16 and Q4 and applied to the latch flip-flop E107. The latch flip-flop is an 8640 IC used to eliminate noise spikes on the receive line from the received signal. The 20 mA to TTL converters for lines 0, 2, and 3 are identical to line 1.

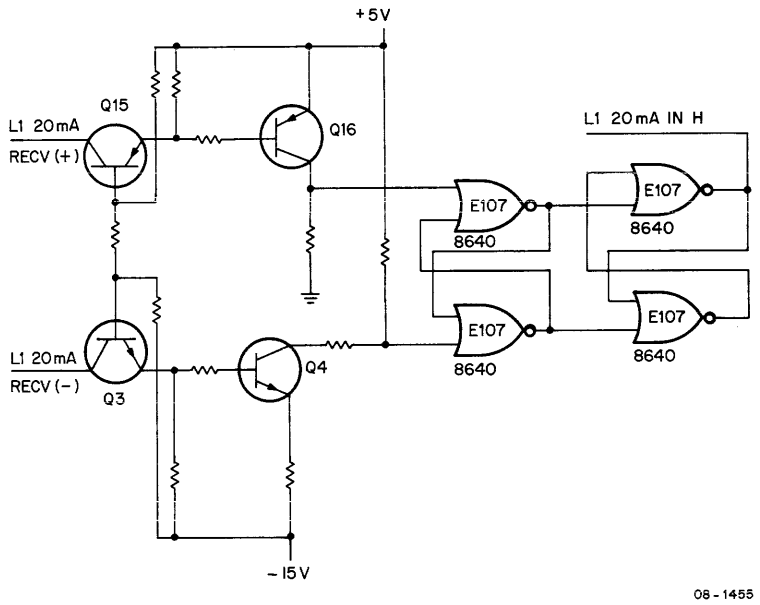


Figure 4-28 20mA To TTL Converter

4.2.20.4 TTL to 20 mA Converter – The L2 TTL to 20 mA Converter is shown in Figure 4-29. A low out of the converter E105 generates a low at the base of Q27 (a series transistor) establishing a voltage divider from +5 V to –15 V. This provides a bias to enable Q28 and Q12 to conduct. The conduction of Q28 and Q12 establishes a differential current source for the 20 mA current loop through the external device. The TTL converters for lines 0, 1, and 3 are identical to line 2.

4.2.21 Level Converter Selection Logic

Figure 4-30 shows the logic used to select the EIA or 20 mA inputs for all four lines. When the SELECT switch is in the ON position the EIA input is selected, and in the OFF position the 20 mA input is selected.

The level of the output signals is determined by the type of output cable used. For four EIA devices, the BC08W cable may be used and for four 20 mA devices the BC08X cable must be used. If two 20 mA and two EIA devices are used the BC08Y cable and the H326 patch panel must be used (Chapter 2). If three 20 mA and one EIA devices are used, the BC08-Y cable may be used (Chapter 2).

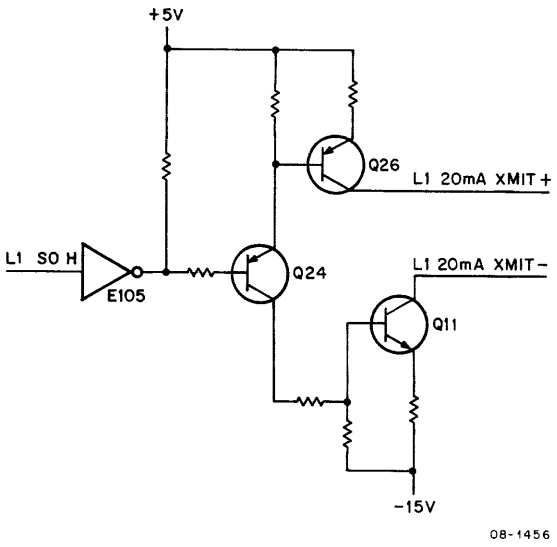


Figure 4-29 TTL To 20mA Converter

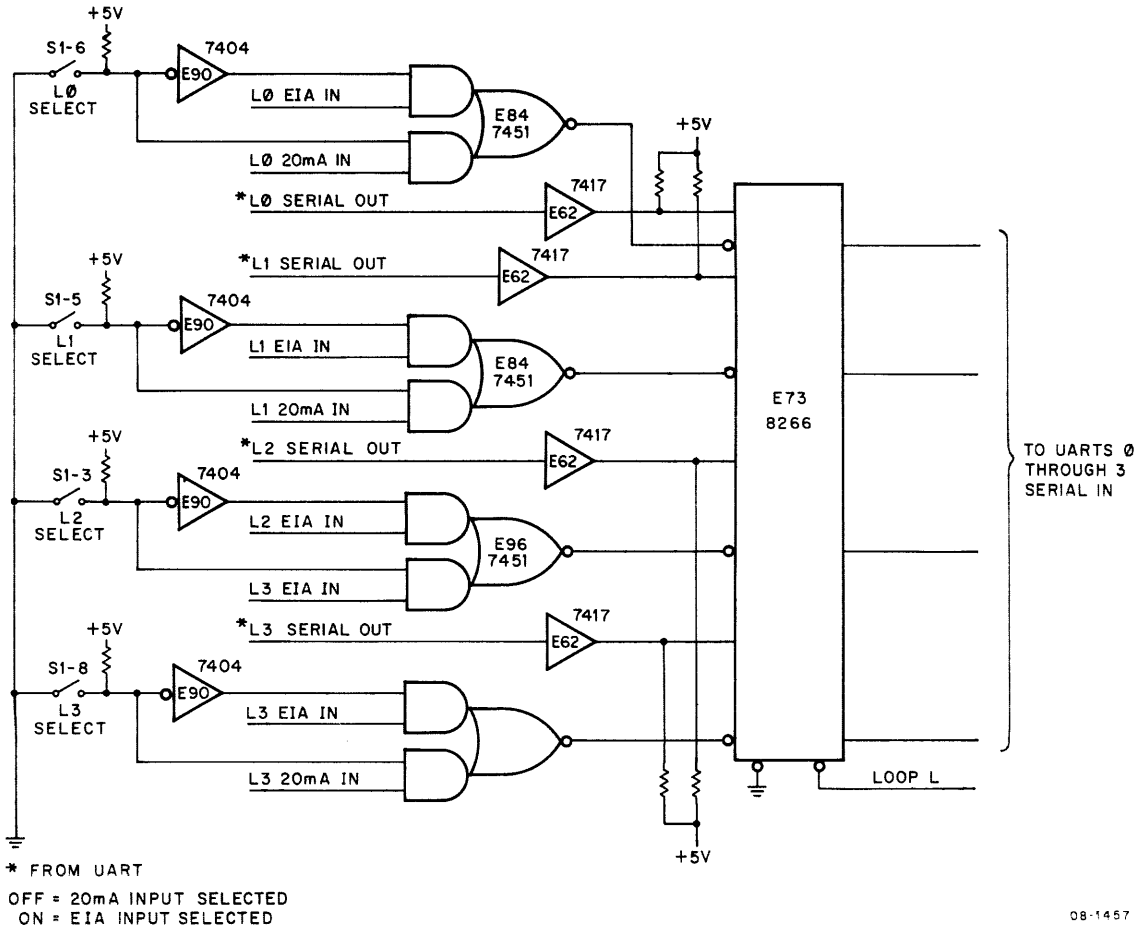


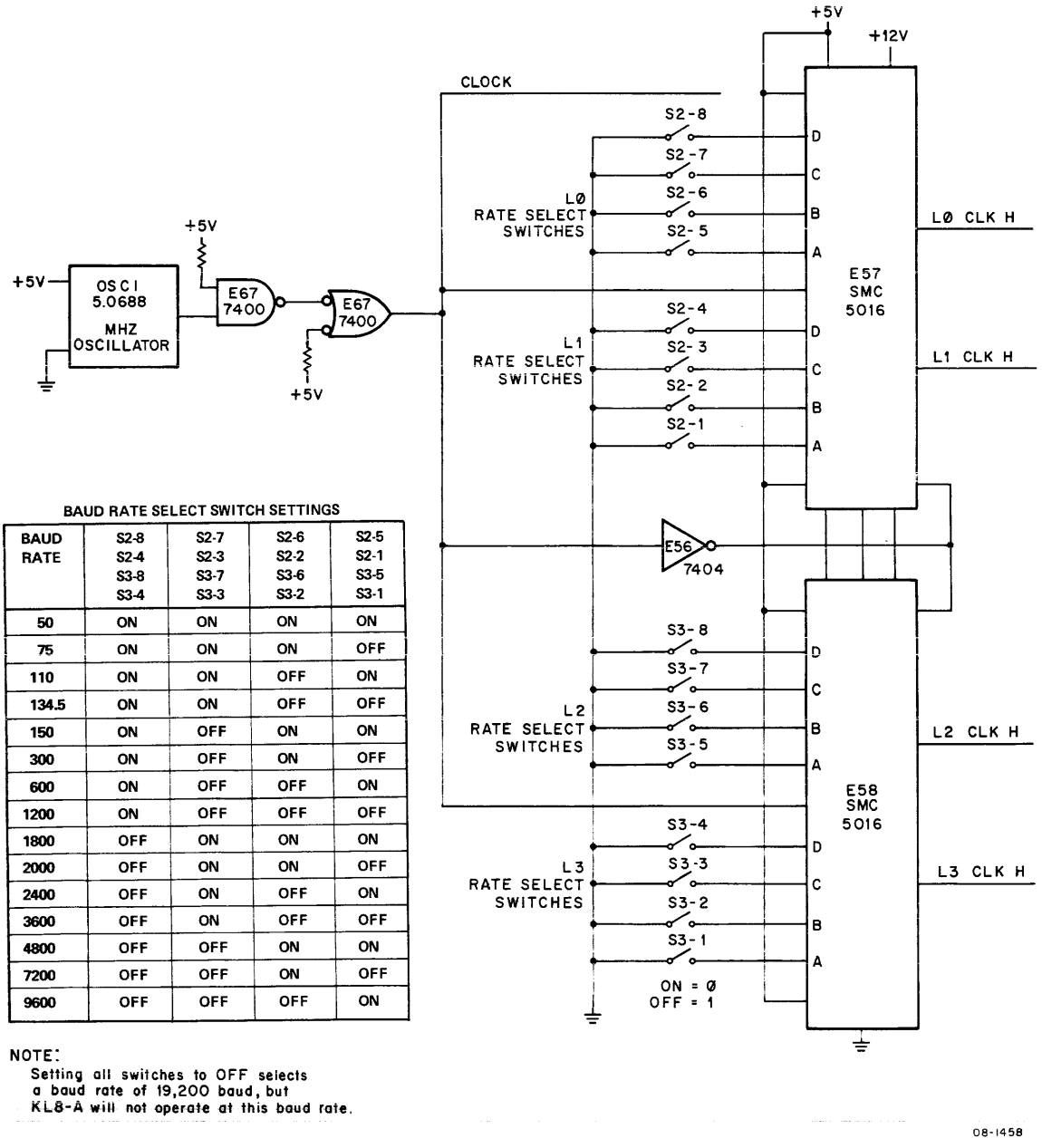
Figure 4-30 Input Level Converter Selection and Maintenance Logic

4.2.22 Maintenance Logic

For maintenance operations the serial output of the UARTs can be fed back to the same UART as a serial input if the Control register is loaded by the MSLC instruction and AC 0 is a one. AC 0 being a one asserts LOOP L (Figure 4-26) and enables the SERIAL OUT from the UART to be supplied as SERIAL IN. This allows checks to be made on the UART without connecting it to a device. The select switches must be on for each line to use the loop back feature.

4.2.23 Clock and Baud Rate Select Logic

The KL8-A clock signal is generated by a 5.0688 MHz crystal controlled oscillator package (Figure 4-31).



BAUD RATE SELECT SWITCH SETTINGS

BAUD RATE	S2-8 S2-4 S3-8 S3-4	S2-7 S2-3 S3-7 S3-3	S2-6 S2-2 S3-6 S3-2	S2-5 S2-1 S3-5 S3-1
50	ON	ON	ON	ON
75	ON	ON	ON	OFF
110	ON	ON	OFF	ON
134.5	ON	ON	OFF	OFF
150	ON	OFF	ON	ON
300	ON	OFF	ON	OFF
600	ON	OFF	OFF	ON
1200	ON	OFF	OFF	OFF
1800	OFF	ON	ON	ON
2000	OFF	ON	ON	OFF
2400	OFF	ON	OFF	ON
3600	OFF	ON	OFF	OFF
4800	OFF	OFF	ON	ON
7200	OFF	OFF	ON	OFF
9600	OFF	OFF	OFF	ON

NOTE:
Setting all switches to OFF selects a baud rate of 19,200 baud, but KL8-A will not operate at this baud rate.

Figure 4-31 SLU Clock and Baud Rate Select Logic

The Baud Rate Select logic consists of two 5016 ICs (Figures 4-31 and 4-32) and 4 switches which allow the selection of a different clock signal (i.e., LO CLK H) and thus a different baud rate for each of the KL8-A lines. The frequency of the clock signal is 16 times the baud rate selected. Receive and transmit baud rates are the same.

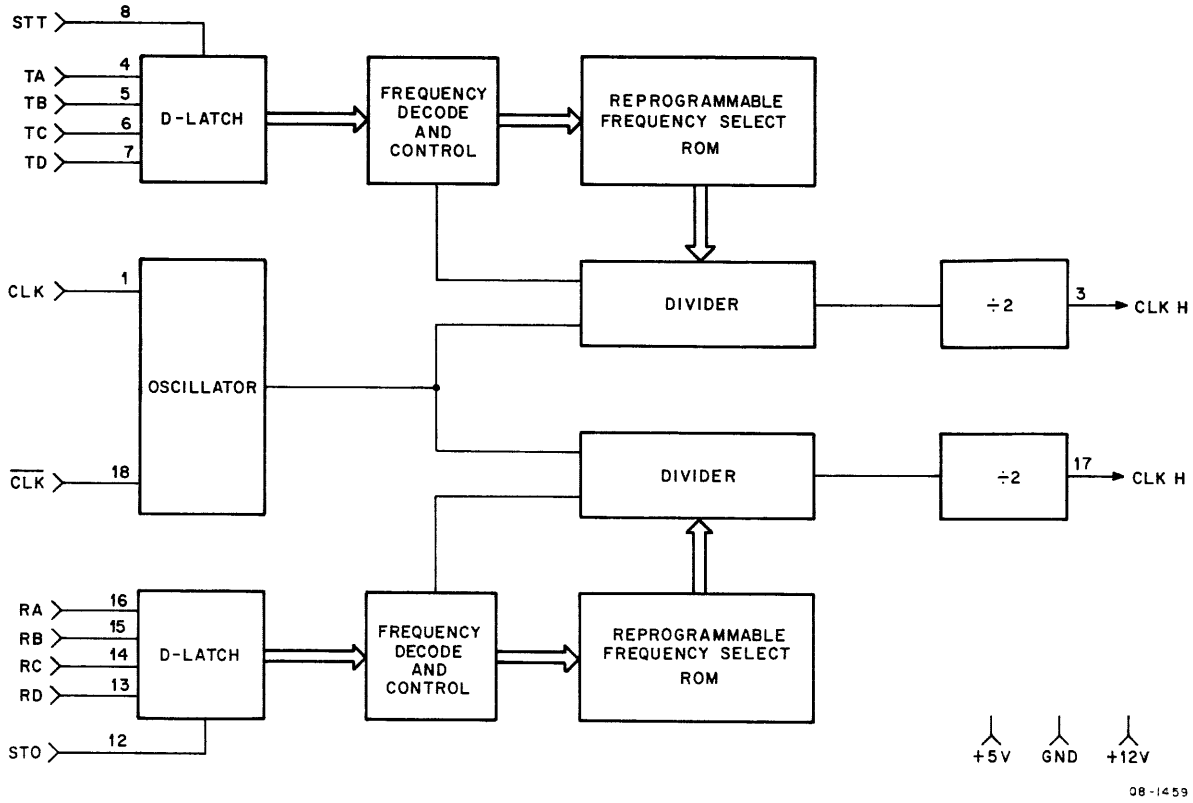


Figure 4-32 5016 IC Block Diagram

4.3 H326 PATCH PANEL DESCRIPTION

The H326 patch panel is divided into two sections: the A section for one KL8-A module and the B section for the second KL8-A module. The circuits in both sections are the same for L3 (Figure 4-33) and lines 0, 1, and 2 in both sections are identical to LO (Figure 4-34).

4.3.1 Loop Back Operation

Switches have been provided on the patch panel to connect EIA DATA OUT to EIA DATA IN and 20 mA XMIT to 20 mA RECV. In this mode the serial data out is tied to the serial data input for troubleshooting and testing the KL8-A. The switches must be on to make these connections. Table 4-3 lists the EIA loop back switches and Table 4-4 lists the 20 mA loop back switches.

4.3.2 ASR/KSR 33 or 35 TTY Operations

Switches on the patch panel (Table 4-5) connect a filter across the 20 mA receive leads for lines connected to Teletypes with a baud rate of 110 baud or less.

4.3.3 Modem Operation

Jumpers on the KL8-A are provided to allow the H326 to be connected to various modems. Table 4-6 lists the jumper configurations for several Bell (or equivalent) modems. An asterisk (*) in the table indicates that it does not matter if the jumper is in or out.

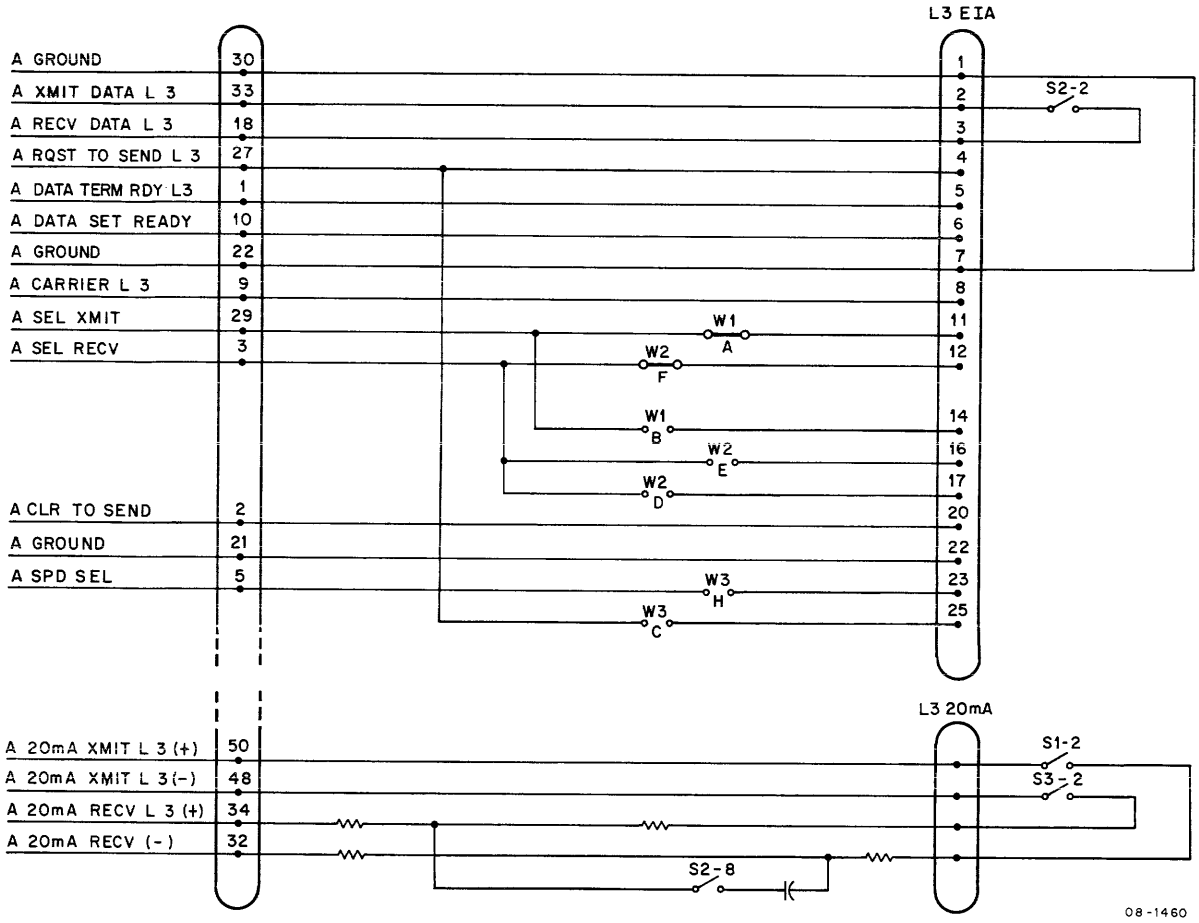


Figure 4-33 L3 EIA and 20mA Patch Panel Circuits

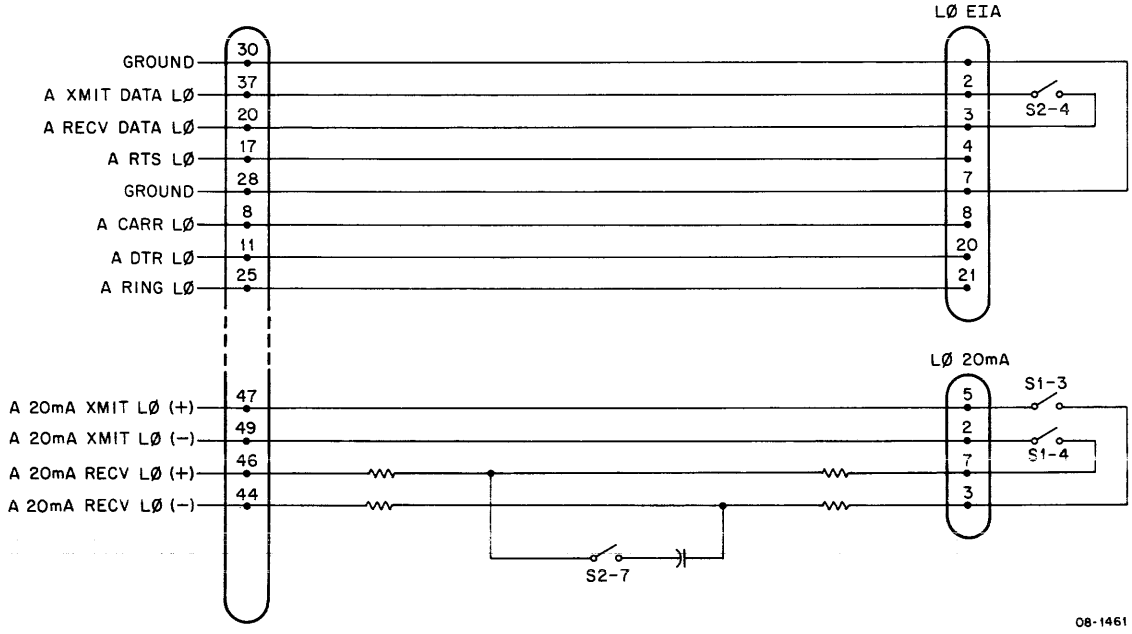


Figure 4-34 LO EIA and 20mA Patch Panel Circuits

Table 4-3
EIA Loopback Switches

Line No.	Section A	Section B
L0	S2-4	S4-4
L1	S2-3	S4-3
L2	S2-1	S4-1
L3	S2-2	S4-2

Table 4-4
Twenty mA Loop Back Switches

Line No.	Section A	Section B
L0	S1-3 and S1-4	S3-3 and S3-4
L1	S1-5 and S1-6	S3-5 and S3-6
L2	S1-7 and S1-8	S3-7 and S3-8
L3	S1-1 and S1-2	S3-1 and S3-2

Table 4-5
Teletype Filter Switches

Line No.	Section A	Section B
L0	S2-7	S4-7
L1	S2-6	S4-6
L2	S2-5	S4-5
L3	S2-8	S4-8

Table 4-6
Jumpers For Modem Operation

Bell Modem Type	Description	Jumpers			
		B	C	D	E
103A	300 baud/full duplex	*	*	*	*
103E, G, H	300 baud/full duplex	*	In	*	*
103F	300 baud/full duplex	*	*	*	*
113A	300 baud/originate only	*	*	*	*
202C, D	1800 baud/half duplex	*	*	*	*
811B	Low speed TWX	*	*	In	*
EIA	RS232-C	In	Out	Out	In

4.3.4 Signal Disconnection

The following L3 signals may be disconnected by removing the indicated jumper (Figure 4-33).

Signal Name	Remove Jumper
SEC XMIT	W1-A
SEC RECV	W2-F
SPEED SEL	W3-H

CHAPTER 5
MAINTENANCE

NOTE

Module repair should not be attempted at the user's site. Removal and replacement of components on the M8319 module requires special tools and equipment which are only available at DIGITAL repair depots. All defective modules should be returned to a DIGITAL repair depot for repair.

There are no specific maintenance procedures for the KL8-A module (M8319) itself. The KL8-A diagnostics should be run according to the procedure in Chapter 2. Once it has been determined that the KL8-A module is defective, it should be returned to a DIGITAL repair depot for repair. If possible, cables connecting the KL8-A and the communications devices should be disconnected to ensure that a defective cable is not causing the problems encountered during operation.

All defective modules should be sent to a DIGITAL repair depot as soon as possible for repair.

CHAPTER 6
SPARE PARTS

DIGITAL recommends that the user keep a spare M8319 module and spare cables of the type required to connect the user's communication device as spare parts. Paragraph 2.6 lists the cables available from DIGITAL to connect the KL8-A to various types of communications devices.

ERRATA SHEET

TO

KL8-A USER's MANUAL
(EK-KL80A-OP-001)

Replace pages 2-3 through 2-6 with the attached sheets.

Modem Control and 20 mA Data Test - This test requires the 70-11451 test plug. If the test plug is not available, the H326 patch panel may be used. If the H326 patch panel is used, the modem control signals are not checked for correct operation. Run this test for five minutes with no errors.

Terminal/Keyboard Test - This test is optional and can only be run if a terminal is available. Run this test for five minutes.

After all tests have been performed as explained in the diagnostic document running the diagnostic without errors, the M8319 must be set up to customer specifications, and re-inserted into the bus. Refer to Tables 2-1 through 2-4 for switch settings and jumper installation requirements. Paragraph 2.7 shows some typical KL8-A configurations. If it is necessary to change device codes from 40 and 41, install jumpers as shown in Table 2-5. Do not assign device codes used by another device in the system.

NOTE

IOT device codes below 30 should not be used unless it is known positively that no IOT device code conflicts exist.

Table 2-2
EIA on 20 mA Line Selection Switch Settings

Line No.	Switch No.	EIA	20 mA
L0	S1-1	ON	OFF
L1	S1-2	ON	OFF
L2	S1-3	ON	OFF
L3	S1-4	ON	OFF

NOTE

Lines that do not have a device connected to them must have their switch in the ON position.

If the user desires to use only two branch addresses, one for transmit and one for receive, the two jumpers at the S2-8 end of S2 (see Figure 2-1) should be removed and pins 1 and 6 of E50 should be tied to ground. Pin 8 of E50 is tied to ground. Install a jumper from pin 8 to pins 1 and 6 to ground them.

2.4 INTERFACE PANEL AND CABLES

An optional H326 patch panel and three types of cables are available to connect the KL8-A to the user's devices.

2.4.1 H326 Patch Panel

The HI26 patch panel (Figure 2-2) is supplied with the KL8-A as an option. The patch panel is required for systems that have both 20 mA and EIA inputs if the KL8-A is the interface to the ASR and KSR Teletypes, or if the KL8-A is interfaced to Bell 811B modems.

The patch panel is rack mountable and occupies a space 5.25 inches high (13.34 cm), 19 inches wide (48.26 cm), and 4.5 inches deep (11.43 cm).

The panel contains the following items:

1. Eight 25-pin Cinch type connectors for EIA signals
2. Eight 8-pin MATE-N-LOK type connectors for 20 mA signals
3. Switches for each line: To connect input to output on the data signal leads for both EIA and 20 mA circuits, and to connect a filter (2.2 mF capacitor) across the 20 mA receive leads. The filter is used only for 110 buad operation or less.

Each patch panel services two KL8-A modules or eight serial devices.

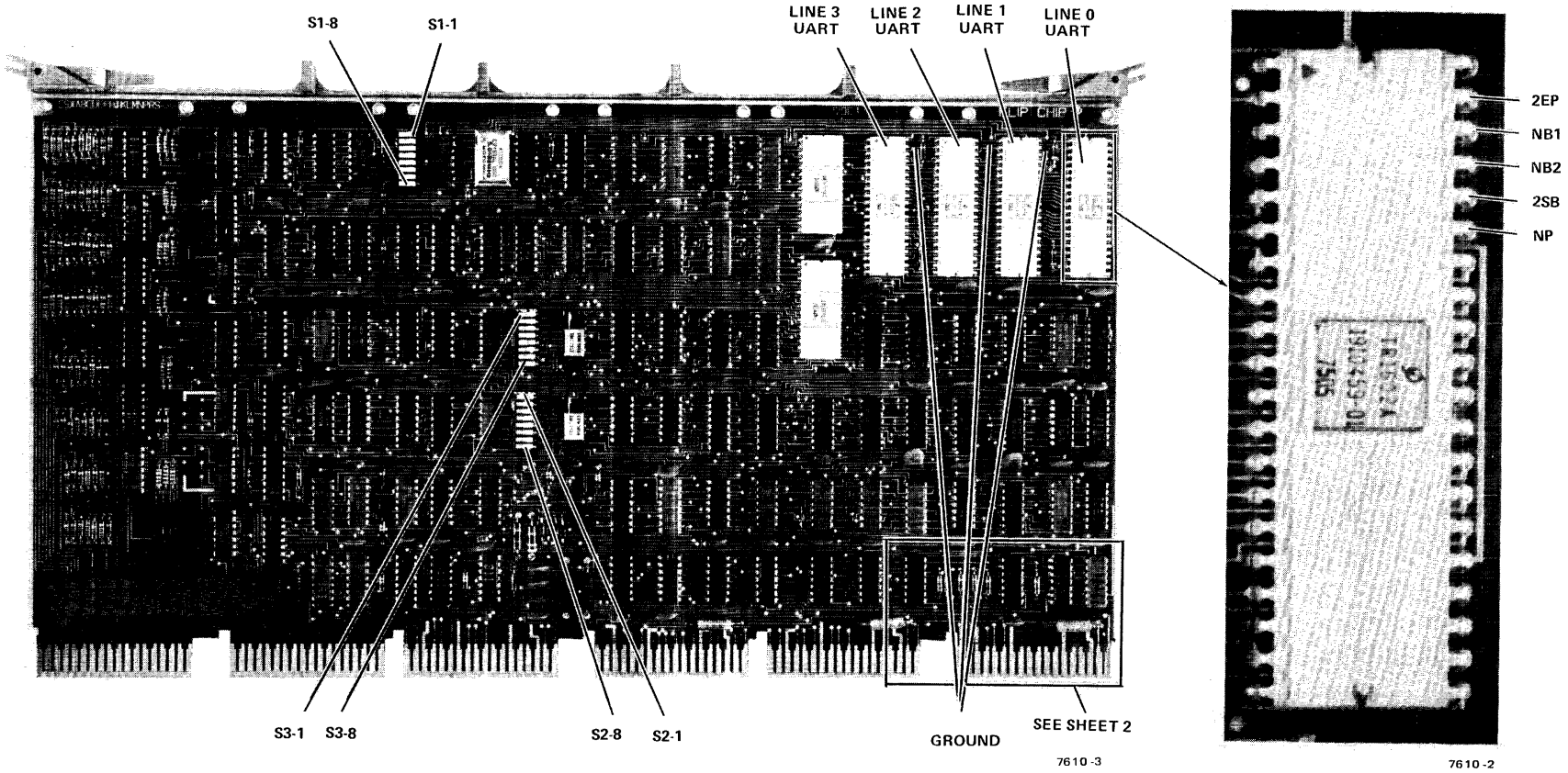


Figure 2-1 KL8-A (M8319) Module (Photo) (Sheet 1 of 2)

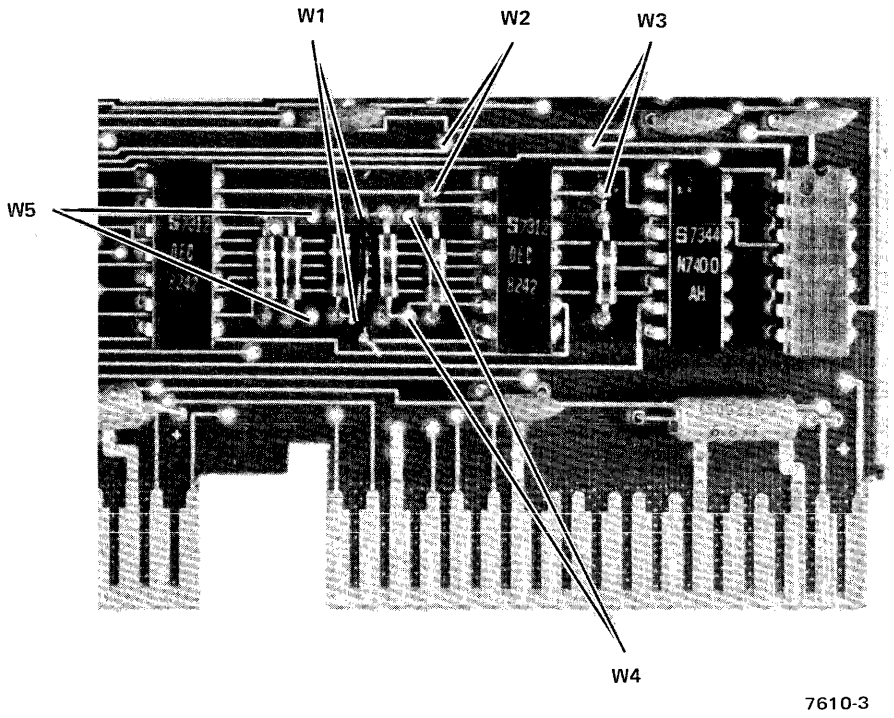


Figure 2-1 KL8-A (M8319) Module (Photo) (Sheet 2 of 2)

Table 2-3
UART Jumper Installation

Jumper Name	Option Selected With Jumper Out	Jumper Selected With Jumper In
EP	Even Parity	Odd Parity
2 SB	Two Stop Bits*	One Stop Bit
NP	Parity Disabled	Parity Enable

*1.5 stop bits are produced if 5 bits per character are selected.

NB1 and NB2	Bits per Character			
	8	7	6	5
NB1	Out	In	Out	In
NB2	Out	Out	In	In

Jumpers are installed by running a wire from the appropriate pin to ground-feed through.

Table 2-4
H326 Switch Settings for Teletype Filter

Line No.	Section A	Section B
L0	S2-7 ON	S4-7 ON
L1	S2-6 ON	S4-6 ON
L2	S2-5 ON	S4-5 ON
L3	S2-8 ON	S4-8 ON

Note: The ON position activates the Teletype filter.

Table 2-5
Device Code Jumper installation

First Number of Device Code				Second Number of Device Code		
	MD3	4	5		MD6	7
	W1	W2	W3		W4	W5
0	Out	Out	Out	0	Out	Out
1	Out	Out	In			
2	Out	In	Out	2	Out	In
3	Out	In	In			
4	In	Out	Out	4	In	Out
5	In	Out	In			
6	In	In	Out	6	In	In
7	In	In	In			

Example: To Select Device Code 34, Jumpers W2, W3, and W4 would be In. Jumpers W1 and W5 would be Out.

To install the jumper, use a small wire and tuck it in.

NOTE

IOT Device Codes below 30 should not be used unless it is known positively that no IOT Device Code conflicts exist.

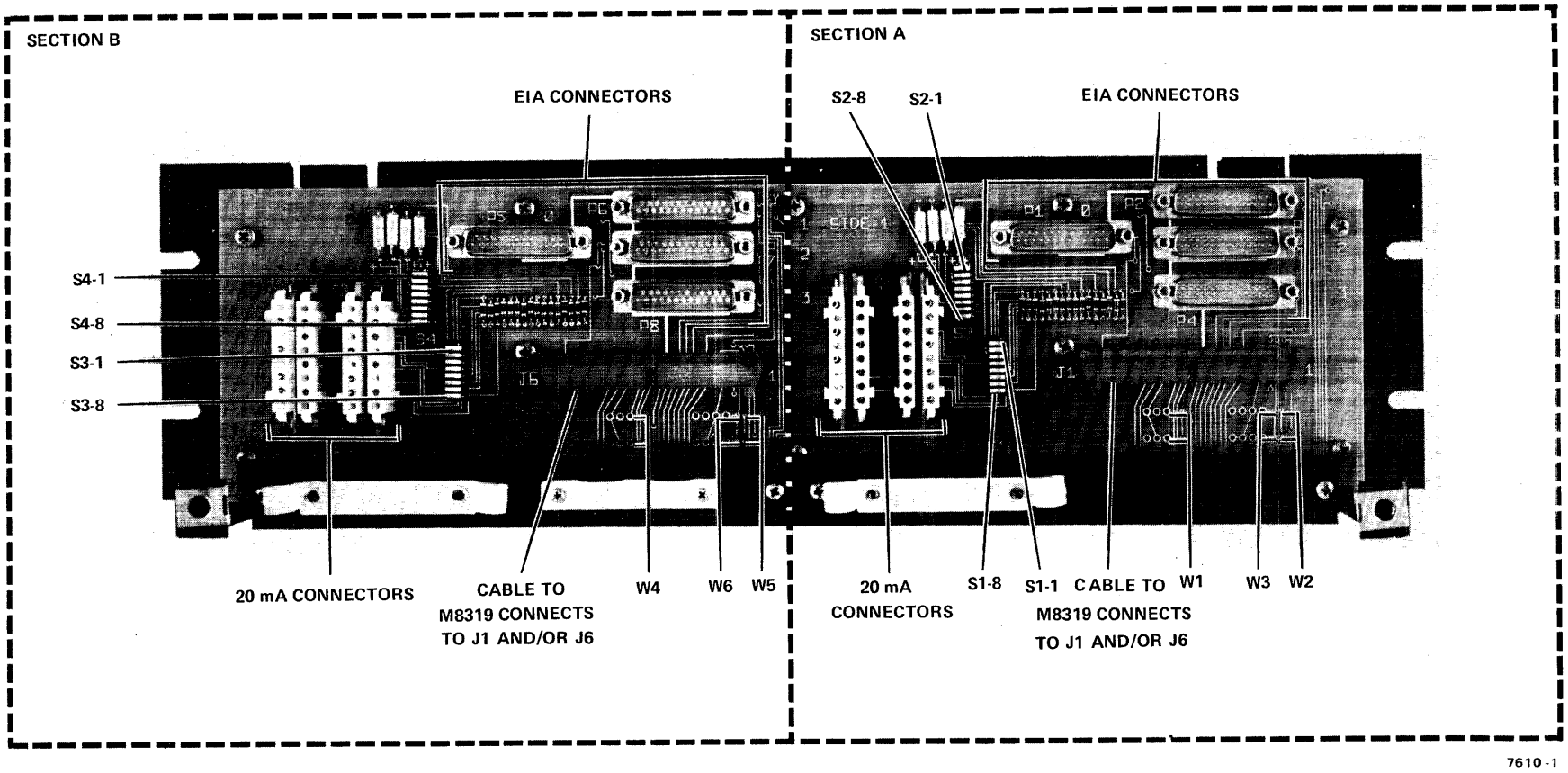


Figure 2-2 H326 Patch Panel (Photo)