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KW12A

IDENTIFICATION

PRODUCT CODE: MAINDEC 12-06CD-D
PRODUCT NAME: KW12A CLOCK TEST
DATE CREATED: DECEMBER 1, 1971
MAINTAINER: DIAGNOSTIC GROUP
AUTHOR: RAYMOND SHOOP

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1.0 ABSTRACT

1.1 THE KW12 REAL TIME CLOCK TEST IS DESIGNED TO VERIFY THE CORRECT OPERATION OF THE BUFFER PRESET REGISTER, CLOCK COUNTER REGISTER, CLOCK CONTROL REGISTER, CLOCK ENABLE REGISTER, CLOCK I/O INTERFACE, EXTERNAL INPUT CHANNELS, AND FAST SAMPLE MODE (IF THE AD12 OPTION IS CONCURRENTLY INSTALLED.)

1.2 PROGRAM CONTROL IS MAINTAINED BY A MONITOR RESIDENT IN BANK 0. SEVERAL OPTIONS ARE AVAILABLE TO THE OPERATOR FOR ERROR HANDLING.

2.0 REQUIREMENTS:

2.1 EQUIPMENT:

- A. A PDP-12 WITH KW12 INSTALLED.
- B. AN AD12 ANALOG-TO-DIGITAL CONVERTER IF FAST SAMPLE TESTING IS REQUIRED.
- C. AN ASR-33 OR EQUIVALENT.

2.2 PRELIMINARY PROGRAMS

- A. ALL CENTRAL PROCESSOR AND MEMORY DIAGNOSTIC PROGRAMS FOR A BASIC PDP-12 MUST BE ABLE TO RUN SUCCESSFULLY PRIOR TO TESTING THE KW12.

2.3 STORAGE:

- A. 4K MINIMUM CORE.
- B. PROGRAM OCCUPIES LOCATIONS 0000 TO 7600.

3.0 LOADING PROCEDURES

3.1 METHOD

LOAD THIS PROGRAM USING THE STANDARD METHOD OF LOADING A BINARY PROGRAM.

4.0 STARTING PROCEDURES

4.1 METHOD

- A. SET THE MODE SWITCH TO 8 MODE.
- B. SET THE LEFT SWITCHES TO 0000.
- C. SET THE RIGHT SWITCHES TO THE DESIRED OPTIONS.
- D. DEPRESS I/O PRESET.
- E. DEPRESS START 20.
- F. THE PROGRAM IS NOW RUNNING. THE TELETYPE BELL WILL RING AT THE END OF EACH PASS. IN ADDITION, THE CONTENTS OF THE PASS COUNTER WILL BE TYPED OUT.

4.2 SWITCH SETTINGS

- A. IF FAST SAMPLE TESTING IS TO BE ATTEMPTED, SET KNOB 0 FULLY COUNTERCLOCKWISE AND KNOB 1 FULLY CLOCKWISE.
- B. SET THE SELECTOR SWITCHES ON THE FRONT PANEL TO LINE FREQUENCY.
- C. SET THE INPUT LEVEL KNOBS TO MID-RANGE.
- D. SELECT ANY DESIRED ERROR HANDLER OPTIONS. WITH RSW = 0000, THE FOLLOWING SEQUENCE WILL OCCUR FOR AN ERROR: (MESSAGE TYPEOUT, ERROR HALT) THE OPERATOR SELECTS ANY FURTHER ERROR OPTIONS AND DEPRESSES CONTINUE.... (MONITOR EXECUTES NEXT SEQUENTIAL TEST)

RSW 00 = 1; INHIBIT ERROR HALT
RSW 01 = 1; INHIBIT ERROR PRINTOUT
RSW 02 = 1; SCOPE LOOP ON ERROR
RSW 03 = 1; SCOPE LOOP ON NON-FAILING TEST
RSW 04 = 1; INHIBIT PASST SAMPLE TESTING
RSW 05 = 1; INHIBIT BELL RINGING
RSW 06 = 1; INHIBIT PASS COUNTER PRINTOUT

5.0 ERROR ROUTINE

5.1 ERROR PRINTOUT

- A. THE ERROR MESSAGES HAVE THE FOLLOWING GENERAL FORM:
TEST NC. TEST MESSAGE
REG1 REG2 REG3 ...
- B. TEST NC. REFERS TO THE TEST NUMBER AS ORGANIZED IN THE LISTING. THIS IS INCLUDED TO AID THE OPERATOR IN FINDING THE TEST IN THE LISTING.
- C. TEST MESSAGE IS THE BODY OF THE TEXT, DESCRIBING WHAT WAS TESTED, AND INDICATING ANY AREAS OF PROBABLE FAILURE.
- D. REG1, REG2, REG3, ARE SPECIFIC DATA WORDS PERTAINING TO THE FAILURE.

ERROR MESSAGES

TST10 CLAB CHANGED AC
7741 7020
TST11 CLBA FAILED
0402 7020
TST12 CLAB FAILED
0402 7020
TST13 CLAB FAILED
7741 7020
TST14 CLAB FAILED
0402 7020
TST15 CLBA CHANGED BUFFER
0402 7020
TST16 CLAB <> CLBA FAILED
7741 7020
TST17 CLAB <> CLBA FAILED
0402 7020
TST18 CLAB <> CLBA FAILED
0402 7020
TST19 CLEN CHANGED AC
7741 7020
TST20 CLEN CHANGED BUFFER
7741 7020
TST21 CLCA FAILED
0402 7020
TST22 "CLR CNT" FAILED
0402 7020
TST23 CLEN FAILED
7741 7020
TST24 CLEN FAILED
0402 7020
TST25 CLCA CHANGES COUNT
0402 7020
TST26 BUFFER <> COUNTER FAILED
0402 7020
TST27 "LOAD CNT" FAILS TO "OR"
0402 7020
TST28 "LOAD CNT" LOADED IN ERROR
0402 7020
TST29 "LOAD CNT" LOADED IN ERROR
0402 7020
TST30 MODE REG CAUSES "LOAD CNT"
0402 7020
TST31 MODE REG CAUSES "LOAD CNT" OR "CLR BUF"
0402 7020 0000
TST32 MODE 21 1>0 CLOCKED CNTR
0402 7020
TST33 MODE 21 0>1 CLOCKED CNTR
0000 7020
TST34 01FLO FAILED TO SET 01FLO FLOP
TST35 CLSA FAILED TO CLEAR 01FLO FLOP

TST36 CLSK SKIPPED IV ERROR
TST37 ILLEGAL CLOCK INTERRUPT!
TST38 CLSK FAILED TO SKIP
TST39 CLOCK INTERRUPT FAILED
TST40 O'FLC ENABLE WON'T ZERO
TST41 O'FLC FLAG WON'T CLEAR
TST42 CLOCK INTR WON'T CLEAR
TST43 BIT 11 FAILED.
0402 7020
TST44 BIT 10 FAILED.
0402 7020
TST45 BIT 09 FAILED.
0402 7020
TST46 BIT 08 FAILED.
0402 7020
TST47 BIT 07 FAILED.
0402 7020
TST48 BIT 06 FAILED.
0402 7020
TST49 BIT 05 FAILED.
0402 7020
TST50 BIT 04 FAILED.
0402 7020
TST51 BIT 03 FAILED.
0402 7020
TST52 BIT 02 FAILED.
0402 7020
TST53 BIT 01 FAILED.
0402 7020
TST54 BIT 00 FAILED.
0402 7020
TST55 RATE 400KC FAILS
TST56 RATE 100KC FAILS
TST57 RATE 10KC FAILS
TST58 RATE 1KC FAILS
TST59 RATE 100CPS FAILS
TST60
CHAN 1 INPUT LOCKED OUT
TST61 CHAN 3 MON'Y TOGGLE
0402 7020
TST62 CHAN 2 MON'Y TOGGLE
0402 7020
TST63 CHAN 1 MON'Y TOGGLE
0402 7020
TST64 CHAN 1 MON'Y TOGGLE

TST65 CHAN 1 INTR IN ERROR
TST66 CHAN 2 MON'IT INTR.
0402 7020
TST67 CHAN 2 INTR IN ERROR
TST68 CHAN 3 MON'IT INTR.
0402 7020
TST69 CHAN 3 INTR IN ERROR
TST70 CHAN 3 INPUT LINE FREQ FAILED
7020
TST71 CHAN 2 INPUT LINE FREQ FAILED
7020
TST72 CHAN 1 INPUT LINE FREQ FAILED
7020
TST73 FAST SAM FAILS
0402 7020
TST74 O'FLOC MON'IT FAST SAD
0402 7020
TST75 FAST SAM MON'IT SET
0402 7020
TST76 MODES 2-1 INHIBIT FAST SAM
0402 7020
TST77 RATE 10KC FAILS
0402
TST78 I/O PRESET MON'IT STOP CLOCK
(RATE BITS 1 & 2)
TST79 1KC FAILS
0402
TST80 I/O PRSET MON'IT STOP CLOCK
(RATE BIT 2)
TST81 I/O PRESET MON'IT CLEAR O'FLO
TST82 I/O PRESET MON'IT CLEAR INTERRUPT ENABLE
TST83 I/O PRESET MON'IT CLEAR INPUTS
TST83 I/O PRESET MON'IT CLEAR MODE 2
TST85 I/O PRESET MON'IT CLEAR MODE 0
TST 86 FAST SAM NOT CLEARED
TST 87 CHAN 1 MON'IT TRANS CNT TO BUF
0200
TST88 CHAN 2 MON'IT TRANS CNT TO BUF
0200
TST89 CHAN 3 MON'IT TRANS CNT TO BUF
0200
TST90 CHAN 1 MON'IT TRANS CNT TO BUF
0300
TST91 CHAN 2 MON'IT TRANS CNT TO BUF
0300
TST92 CHAN 3 MON'IT TRANS CNT TO BUF

0300
TST93 CHAS INPUT FAILED TO CLR CNT
7020

TST94 ECO EM12-00034 IS EITHER NOT WORKING OR NOT
INSTALLED

TST95 ECO EM12-00055 IS EITHER NOT WORKING OR NOT
INSTALLED PROPERLY

KW12 PASS=0000


```

/PDP-12 KW12A CLOCK TEST, MAINDEC 12-08CD=L
/COPYRIGHT 1970, DIGITAL EQUIPMENT CORP., MAYNARD, MASS.
/THIS TEST IS DESIGNED TO VERIFY PROPER OPERATION
/OF THE KW-12A REAL TIME CLOCK AND TO DIAGNOSE
/MALFUNCTIONS IN REGISTERS, REGISTER TRANSFERS, IO
/BUS INTERFACE, AND EXTERNAL INPUT CHANNELS.
/
/AUTHORS: JAMES KELLY, STEVE TEICHER, HAROLD LONG
/RAYMOND SHOOP
/MAJOR START
/I/O PRESET 8 MODE
/SET LEFT SWITCHES TO 0000
/SET RIGHT SWITCHES TO DESIRED OPTIONS
/DEPRESS START 20
/
/SWITCH SETTINGS: (NORMALLY 0000)
/RSW 00=1, INHIBIT ERROR HALT
/RSW 01=1, INHIBIT ERROR PRINTOUT
/RSW 02=1, SCOPE LOOP ON FAILING TEST
/RSW 03=1, SCOPE LOOP ON NON-FAILING TEST
/RSW 04=1, INHIBIT FAST SAMPLE TESTING.
/RSW 05=1, INHIBIT BELL RINGING
/RSW 06=1, INHIBIT TEST COMPLETION ALARM
/
/SOME IOT DEFINITIONS:
/
6131 CLSK#6131 /SKIP ON CLOCK INTERRUPT
6132 CLLR#6132 /AC TO CLOCK CONTROL REGISTER
6133 CLAB#6133 /AC TO BUFFER PRESET REGISTER
6134 CLEN#6134 /AC TO CLOCK ENABLE REGISTER
6135 CLSA#6135 /CLOCK STATUS TO AC, CLEAR STATUS FLIP-FLOPS
6136 CLBA#6136 /BUFFER PRESET REGISTER TO AC
6137 CLCA#6137 /COUNTER TO AC
0020 EXIT#0000 /MESSAGE TERMINATOR
7777 EXITA#7777 /MESSAGE SWITCH
4444 EXITB#4444 /RESTART SWITCH
/
/SOME LINC PROGRAMMING DEFINITIONS
/
6141 LINC#6141
0022 PDP#0002
0011 CLR#0011
0004 ESF#0004
0100 SAM0#0100
0101 SAM1#0101
1020 LDAI#1020

```

/PDP-12 KW124 CLOCK TEST, MAINDEC 12=D6CD=L

```

0001      0021      JMP I RETURN
0010      0451      *10
0020      0010      PRINT, 0
0020      0020      *20
0020      0020      JMP 177
0020      5177

```

/MAJOR START 8 MODE

/PAGE 0 REGISTERS AND CROSS-PAGE TAGS

0021	5200	BELL,	BELLS
0022	1561	DN43,	BK43
0023	2362	DN55,	BK55
0024	0000	CNTR,	0000
0025	5020	ERROR,	ERRORS
0026	0000	LSTERR,	0000
0027	5000	NEAROR,	NERROS
0030	5051	OUTPAS,	ASCII
0031	0000	PASS,	0000
0032	1425	PNTA,	LOCA
0033	1457	PNTB,	LOCB
0034	1527	PNTC,	LOCC
0035	2720	PNTD,	LOCD
0036	2742	PNTE,	LOCE
0037	2763	PNTF,	LOCF
0040	3025	PNTG,	LOCG
0041	3027	PNTH,	LOCH
0042	3051	PNTI,	LOCI
0043	4307	PNTJ,	LOCJ
0044	5210	RANDOM,	RANDY
0045	0000	REGA,	0000
0046	0000	REGB,	0000
0047	0000	REGC,	0000
0050	0000	REGT,	0000
0051	0000	RETURN,	0000
0052	0000	RXED,	0000
0053	0000	SEND,	0000
0054	5252	SET,	SETN
0055	0000	SPACE,	0000
0056	1342	TST35N,	TST35-2
0057	2753	TST66N,	TST66
0060	3313	TST75N,	TST75
0061	3375	TST77N,	TST77
0062	3436	TST79N,	TST79
0063	4040	TST90N,	TST90
0064	5243	TYPE,	TYPOUT
0065	1572	UP43,	FD43
0066	2201	UP51,	FD51
0067	2372	UP55,	FD55
0070	2617	UP61,	FD61

/PAGE 0 CONSTANTS

0071	0000	K0000,	0000
0072	0001	K0001,	0001
0073	0002	K0002,	0002
0074	0003	K0003,	0003
0075	0004	K0004,	0004
0076	0007	K0007,	0007
0077	0010	K0010,	0010
0100	0014	K0014,	0014
0101	0017	K0017,	0017
0102	0020	K0020,	0020
0103	0037	K0037,	0037
0104	0040	K0040,	0040
0105	0060	K0060,	0060
0106	0077	K0077,	0077
0107	0120	K0120,	0120
0110	0177	K0177,	0177
0111	0200	K0200,	0200
0112	0240	K240,	0240
0113	0300	K0300,	0300
0114	0377	K0377,	0377
0115	0400	K0400,	0400
0116	0500	K0500,	0500
0117	0600	K0600,	0600
0120	0700	K0700,	0700
0121	0777	K0777,	0777
0122	1000	K1000,	1000
0123	1026	K1026,	1026
0124	1777	K1777,	1777
0125	2000	K2000,	2000
0126	3000	K3000,	3000
0127	3777	K3777,	3777
0130	4000	K4000,	4000
0131	4100	K4100,	4100
0132	5100	K5100,	5100
0133	5252	K5252,	5252
0134	5555	K5555,	5555
0135	6000	K6000,	6000
0136	7774	K7774,	7774


```

0176
0176 7410
0177 4454
0200 0200

*176
SKP
JMS I SET
/RESTART ADDRESS; DON'T CLEAR COUNTERS
/RESET BUFFERS

*200
/MAJOR START 8 MODE, AC=0
/TEST BUFFER AND PRESET REGISTER DATA INTERCHANGE
/CLAB=6133 AC TO CLOCK PRESET REGISTER
/CLBA=6136 CLOCK PRESET REGISTER TO AC
/DOES AC CHANGE AFTER A TRANSFER TO BUFFER REG?

0200 4421
0201 7300
0202 1045
0203 6133
0204 3052
0205 1052
0206 7041
0207 1045
0210 7650
0211 4427
0212 4425
0213 5261
0214 7402
0215 7610
0216 0201

TST10,
JMS I BELL
CLA CLL
TAD REGA
CLAB
DCA
TAD
CIA
TAD REGA
SNA CLA
JMS I NERROR
JMS I ERROR
TST10M
HLT
SKP CLA
TST10

/DOES BUFFER DATA JAM INTO THE AC?

TST11,
CLA CLL SEND
DCA
CLAB
CLA CMA
CLBA
DCA
TAD
SNA CLA
JMS I NERROR
JMS I ERROR
TST11M
HLT
SKP CLA
TST11

0217 7300
0220 3053
0221 6133
0222 7240
0223 6136
0224 3052
0225 1052
0226 7650
0227 4427
0230 4425
0231 5301
0232 7402
0233 7610
0234 0217

/BRING BELL
/CLEAR AC
/GET A NUMBER= BINARY UP-COUNT SEQUENCE 0 THRU 7777
/LOAD BUFFER
/STORE WHAT WAS LEFT IN AC
/FETCH IT
/INVERT CONTENTS OF AC
/SUBTRACT SEND
/EQUAL?
/CHECK MONITOR
/CLAB CHANGED AC.
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP; SCOPE LOOP

/CLEAR AC
/SEND REG
/SET BUFFER AND PRESET REGISTER TO 0000
/SET AC TO 7777
/JAM BUFFER PRESET (0000) OVER AC (7777)
/SAVE AC
/RESTORE AC
/DID AC BECOME (0000)?
/CHECK MONITOR
/CLBA FAILED TO JAM THE AC
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP; SCOPE LOOP

```

/PDP-12 KW12A CLOCK TEST, MAINDEC 12-0800-L

```

0235 7240 /SET AC=7777
0236 6133 /SET BUFF#7777
0237 7300 /CLEAR AC
0240 6133 /LOAD BUFFER TO ALL ZEROS
0241 3053 /SAVE AC
0242 6136 /READ BUFFER AND PRESET REGISTER
0243 3052 /SAVE TEST VALUE
0244 1052 /RESTORE IT
0245 7650 /DID BUFFER AND PRESET REGISTER GET CLEARED
0246 4427 /CHECK MONITOR
0247 4425 /AC JAM INTO BUFFER FAILED
0250 5317 /MESSAGE POINTER
0251 7402 /ERROR HALT
0252 7610 /TO NEXT TEST
0253 0235 /IS2 LOOP SCOPE LOOP

```

/DO ALL NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY?

```

0254 7300 /CLEAR AC
0255 1045 /GET TEST NUMBER
0256 6133 /SEND IT
0257 7200 /CLEAR AC
0260 6136 /RETRIEVE IT
0261 3052 /SAVE IT
0262 1052 /RESTORE IT
0263 7041 /COMPLEMENT
0264 1045 /ADD TEST NUMBER
0265 7650 /WERE THEY EQUAL?
0266 4427 /CHECK MONITOR
0267 4425 /AC - BUFFER TO AC DATA TRANSFER FAILED
0270 5335 /MESSAGE POINTER
0271 7402 /ERROR HALT
0272 7610 /TO NEXT TEST
0273 0254 /IS2 LOOP SCOPE LOOP

```

```

/DO RANDOM NUMBERS TRANSFER BETWEEN AC AND BUFFER PROPERLY?
/
TST14, JMS I RANDOM
DCA SEND
TAD SEND
CLAB
JMS I RANDOM
CLBA
DCA RXED
TAD RXED
CIA SEND
TAD SNA CLA
JMS I NERROR
JMS I ERROR
TST14M
HLT
SKP CLA
TST14

```

```

0274 4444
0275 3053
0276 1053
0277 6133
0300 4444
0301 6136
0302 3052
0303 1052
0304 7041
0305 1053
0306 7650
0307 4427
0310 4425
0311 5353
0312 7402
0313 7610
0314 0274

```

```

/DOES READING THE BUFFER CHANGE ITS CONTENTS?
/

```

```

TST15, JMS I RANDOM
DCA SEND
TAD SEND
CLAB
JMS I RANDOM
CLBA
JMS I RANDOM
CLBA
DCA RXED
TAD RXED
CIA SEND
TAD SNA CLA
JMS I NERROR
JMS I ERROR
TST15M
HLT
SKP CLA
TST15

```

```

0315 4444
0316 3053
0317 1053
0320 6133
0321 4444
0322 6136
0323 4444
0324 6136
0325 3052
0326 1052
0327 7041
0330 1053
0331 7650
0332 4427
0333 4425
0334 5371
0335 7402
0336 7610
0337 0315

```

```

/LOAD BUFFER AND PRESET REGISTER WITH A RANDOM NUMBER
/SAVE IT
/RESTORE IT
/SEND IT
/LOAD THE AC WITH A RANDOM NUMBER
/READ BACK RANDOM NUMBER FROM BUFFER PRESET REGISTER
/SAVE TEST RETURN
/RESTORE IT
/COMPLEMENT
/SUBTRACT TEST NUMBER
/EQUAL
/CHECK MONITOR
/AC - BUFFER = AC DATA INTERCHANGE FAILED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP/ SCOPE LOOP

/GET RANDOM NUMBER
/SAVE IT
/RESTORE IT
/SEND IT
/LOAD AC WITH A RANDOM NUMBER
/BRING BACK TEST NUMBER
/LOAD AC WITH A RANDOM NUMBER
/READ BUFFER AGAIN
/SAVE TEST VALUE
/RESTORE IT
/COMPLEMENT
/SUBTRACT TEST NUMBER
/EQUAL
/CHECK MONITOR
/CLBA CHANGED THE CONTENTS OF THE BUFFER
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP/ SCOPE LOOP

```

3-DEC-71

V141

PAL10

12-08CD=L

MAINDEC

KW12A

CLOCK TEST.

/PDP-12

/CAN THE GATES FUNCTION AT HIGH SPEED?

/CLEAR AC
/GET TEST NUMBER
/SEND IT
/GET IT

CLA CLL REGA

TST16,

0340 7300
0341 1045
0342 6133
0343 6136
0344 6133
0345 6136
0346 6133
0347 6136
0350 6133
0351 6136
0352 6133
0353 6136
0354 6133
0355 6136
0356 6133
0357 6136
0360 6133
0361 6136
0362 6133
0363 6136
0364 6133
0365 6136
0366 6133
0367 6136
0370 3052
0371 1052
0372 7041
0373 1045
0374 7650
0375 4427
0376 4425
0377 5413
0400 7422
0401 7610
0402 0340

/SEND IT
/GET IT
/SAVE IT
/FETCH IT
/215 COMPLEMENT
/COMPARE
/EQUAL?
/CHECK MONITOR
/BUF FAILED TO TOGGLE AT HIGH SPEED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP! SCOPE LOOP

RXED
RXED

REGA

NERROR
ERROR

SNA CLA
JMS I
JMS I
TST16M
HLT
SKP CLA
TST16


```

0550 7300
0551 1045
0552 6134
0553 3052
0554 1052
0555 7041
0556 1045
0557 7650
0560 4427
0561 4425
0562 5476
0563 7402
0564 7610
0565 0550

/CLEN=6134 AC TO CLOCK ENABLE REGISTER
/DOES CLEN AFFECT THE AC?
TST19. CLL CLA REGA
TAD
CLEN
DCA
TAD
CIA
TAD
SNA CLA
JMS I
TST19M
HLT
SKP CLA
TST19
/CLEAR AC
/RESTORE TEST NUMBER
/DOES CLEN AFFECT AC
/SAVE AC
/RESTORE IT
/COMPLEMENT
/SUBTRACT TEST NUMBER
/EQUAL?
/CHECK MONITOR
/AC TO CLOCK ENABLE REG CHANGED AC
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP; SCOPE LOOP

```

```

/PRESET REGISTER AND COUNTER DATA INTERCHANGE
/CLSA=6135 STATUS REGISTER TO AC
/CLLR=6132 AC TO CLOCK CONTROL REGISTER
/DOES BUFFER CHANGE AFTER A TRANSFER TO THE COUNTER?
TST20. CLL CLA
CLSA
CLA CLL
TAD
CLAB
CLA CLL
CLLR
TAD
K0100
CLL
CLA
TAD
K0200
CLRA
DCA
TAD
CIA
TAD
SNA CLA
JMS I
TST20M
HLT
SKP CLA
TST20+2

```

```

0566 7300
0567 6135
0570 7300
0571 1045
0572 6133
0573 7300
0574 6132
0575 1107
0576 6132
0577 7200
0600 1111
0601 6134
0602 6136
0623 3052
0604 1052
0605 7041
0606 1045
0607 7650
0610 4427
0611 4425
0612 5516
0613 7402
0614 7610
0615 0570

/CLEAR AC
/CLEAR STATUS
/CLEAR AC
/RESTORE TEST NUMBER
/LOAD BUFFER PRESET REGISTER WITH A BINARY UPCOUNT NUMBER
/CLEAR AC
/STOP CLOCK, SET ALL MODES=0
/MODE CONTROL, REG BIT 2=1
/SET MODE 2, ENABLING CLR LOAD CNT
/CLEAR AC
/AC BIT 4#1, SIMULATE CLR OFLOW ON 6134
/TRANSFER PRESET COUNT TO CLOCK COUNTER
/READ THE BUFFER
/SAVE IT
/RESTORE IT
/COMPLEMENT
/SUBTRACT TEST NUMBER
/EQUAL?
/CHECK MONITOR
/TRANSFER FROM BUFFER TO COUNTER CHANGES BUFFER
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP; SCOPE LOOP

```

```

0616 6135
0617 7300
0620 6133
0621 6132
0622 1107
0623 6132
0624 6134
0625 7240
0626 3053
0627 1053
0630 6133
0631 6137
0632 3052
0633 1052
0634 7650
0635 4427
0636 4425
0637 5540
0640 7402
0641 7610
0642 0616

/DOES COUNTER DATA JAM THE BUFFER AND AC?
/CLCA=6137 CLOCK COUNTER TO PRESET REGISTER, THEN PRESET REG TO AC
/
TST21, CLSA
CLA CLL
CLAB
CLLR
TAD K0100
CLLR
CLEN
CLA CMA
DCA SEND
TAD SEND
CLAB
CLCA
DCA RXED
TAD RXED
SNA CLA
JMS I NERROR
JMS I ERROR
TST21M
HLT
SKP CLA
TST21

/CLEAR STATUS
/CLEAR AC
/LOAD BUFFER TO 0000
/STOP CLOCK, SET ALL MODES=0
/SET AC 05#1
/SET MODE 2=1, THEREBY CLEARING CLOCK COUNTER
/ENABLE INTERRUPT ON OVERFLOW
/SET AC 7777
/SAVE IT
/FETCH IT
/SET BUFFER 7777
/READ COUNTER
/SAVE COUNT
/RESTORE IT
/ZERO?
/CHECK MONITOR
/COUNTER FAILED TO JAM 0000 INTO 7777
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP; SCOPE LOOP

```

/DOES SIGNAL CLR CNT WORK

```

0643 6135
0644 7350
0645 3053
0646 1053
0647 6133
0650 7300
0651 1111
0652 6134
0653 7300
0654 6132
0655 1107
0656 6132
0657 7300
0660 6137
0661 3052
0662 1052
0663 7650
0664 4427
0665 4425
0666 5556
0667 7402
0670 7610
0671 0643

/DOES SIGNAL CLR CNT WORK
/
TST22, CLSA
CLA CMA
DCA SEND
TAD SEND
CLAB
CLA CLL
TAD K0200
CLEN
CLA CLL
CLLR
TAD K0100
CLLR
CLCA
DCA RXED
TAD RXED
SNA CLA
JMS I NERROR
JMS I ERROR
TST22M
HLT
SKP CLA
TST22

/CLEAR STATUS
/SET AC=3777
/SAVE AC
/FETCH IT
/SET BUFFER TO 3777 (USE 3777 SO WE DONT SET OVERFLOW FLOP)
/CLEAR AC
/ENABLE LOAD COUNT GATES
/LOAD COUNTER TO 3777 (GENERATE LOAD CNT)
/CLEAR AC
/ZERO MODE 2
/SET AC 05#1
/SET MODE 2, THEREBY GENERATING "CLC CLR CNT"
/CLEAR AC
/READ THE COUNTER
/SAVE IT
/RESTORE IT
/ZERO?
/CHECK MONITOR
/CLR CNT FAILED TO CLEAR THE COUNTER FROM 3777 TO 0000
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP; SCOPE LOOP

```

```

/DO ALL NUMBERS TRANSFER BETWEEN THE BUFFER AND COUNTER?
/
TST23:  CLSA      6135
        CLA CLL   7300
        TAD      1045
        CLAB     6133
        CLA CLL   7300
        CLLR     6132
        TAD      1107
        CLLR     6132
        CLA      7200
        TAD      1111
        CLCA     6134
        DCA      6137
        TAD      3052
        CLA      1052
        TAD      7041
        CIA      1045
        TAD      7650
        SNA CLA  4427
        JMS I    4425
        JMS I    5576
        TST23M  7402
        HLT     7610
        SKP CLA  0672
        TST23  0672

        REGA
        K0100
        K0200
        RXED
        RXED
        REGA
        NERROR
        ERROR

```

```

/CLEAR STATUS
/CLEAR AC
/LOAD AC WITH TEST NUMBER
/SET BUFFER TO TEST NUMBER
/CLEAR AC
/STOP CLOCK; SET ALL MODES=0
/SET AC 05=1
/GENERATE "CLR CNT"
/CLEAR AC
/SET AC 04=1
/GENERATE "LOAD CNT"
/COUNTER TO AC
/SAVE IT
/RESTORE IT
/COMPLEMENT
/SUBTRACT TEST NUMBER
/EQUAL?
/CHECK WITH MONITOR
/BUFFER TO COUNTER DATA INTERCHANGE FAILED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP; SCOPE LOOP

```

/DO RANDOM NUMBERS TRANSFER BETWEEN BUFFER AND COUNTER?

```

0721 4444 /GET RANDOM NUMBER
0722 6133 /LOAD BUFFER RANDOM
0723 3053 /SAVE TEST NUMBER
0724 6135 /CLEAR CLOCK STATUS
0725 7200 /CLEAR AC
0726 6132 /STOP CLOCK, SET ALL MODES=0
0727 1107 /SET AC 05#1
0730 6132 /GENERATE "CLR CNT"
0731 7200 /CLEAR AC
0732 1111 /SET AC 04#1
0733 6134 /GENERATE "LOAD CNT"
0734 4444 /GET RANDOM NUMBER
0735 6133 /LOAD BUFFER RANDOM
0736 4444 /LOAD AC RANDOM
0737 6137 /READ COUNTER
0740 3052 /SAVE TEST VALUE
0741 1052 /RESTORE IT
0742 7041 /COMPLEMENT
0743 1053 /SUBTRACT TEST NUMBER
0744 7650 /EQUAL?
0745 4427 /CHECK MONITOR
0746 4425 /BUFFER TO COUNTER RANDOM DATA INTERCHANGE FAILED
0747 5614 /MESSAGE POINTER
0750 7422 /ERROR HALT
0751 7610 /TO NEXT TEST
0752 0721 /ISE LOOP! SCOPE LOOP

```

```

/DOES READING THE COUNTER CHANGE ITS STATE?
/
TST25, JMS I RANDOM
CLAB SEND
DCA K0100
CLLR
TAD K0200
CLLR
CLSA
CLA
TAD
CLEN
JMS I RANDOM
CLAB RANDOM
JMS I RANDOM
CLCA
JMS I RANDOM
CLAB RANDOM
JMS I RANDOM
CLCA RXED
DCA RXED
TAD
CIA SEND
TAD SNA CLA
JMS I NERROR
JMS I ERROR
TST25M
HLT
SKP CLA
TST25
CLA CLL CMA
DCA REGA

/GET RANDOM TEST NUMBER
/SEND IT TO BUFFER
/SAVE IT
/STOP CLOCK, SET ALL MODES=0
/SET AC 05=1
/GENERATE "CLR CNT"
/CLEAR CLOCK STATUS
/CLEAR AC
/SET AC 04=1
/GENERATE "LOAD CNT"
/GET RANDOM NUMBER
/SEND IT TO BUFFER
/GET RANDOM NUMBER
/READ CLOCK COUNTER
/GET RANDOM NUMBER
/SEND IT TO BUFFER
/GET RANDOM NUMBER
/READ CLOCK COUNTER
/SAVE IT
/RESTORE IT
/COMPLEMENT
/SUBTRACT TEST NUMBER
/EQUAL?
/CHECK MONITOR
/(CLCA) READ THE COUNTER CHANGES THE COUNTERS STATE
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP/ SCOPE LOOP
/SET AC=777
/PRESET COUNTER FOR NEXT TEST

```

```

1012 4444 /CAN THE BUF TO COUNTER AND COUNTER TO BUF FUNCTION AT HIGH SPEED?
1013 6133 /
1014 3053 /TST26; JMS I RANDOM
1015 7200 DCA SEND
1016 6132 CLA
1017 1107 TAD K0100
1020 6132 CLLR
1021 6135 CLSA
1022 7200 CLA K0200
1023 1111 TAD
1024 6134 CLEN
1025 6137 CLCA
1026 2046 ISZ REGB
1027 5215 JMP TST26+3
1030 3052 DCA RXED
1031 1052 TAD RXED
1032 7041 CIA
1033 1053 TAD SEND
1034 7650 SNA CLA
1035 4427 JMS I NERROR
1036 4425 JMS I ERROR
1037 5653 TST26M
1040 7402 HLT
1041 7610 SKP CLA
1042 1012 TST26
/GET RANDOM NUMBER
/SEND IT TO BUFFER
/SAVE IT
/CLEAR AC
/STOP CLOCK
/SET AC 05#1
/GENERATE "CLR CNT"
/CLEAR CLOCK STATUS
/CLEAR AC
/SET AC 04#1
/GENERATE "LOAD CNT"
/READ COUNTER
/DONE?
/BACK TO START 4096 TIMES
/SAVE FINAL NUMBER
/RESTORE IT
/COMPLEMENT
/SUBTRACT TEST NUMBER
/EQUAL?
/CHECK MONITOR
/THE BUFFER COUNTER BUFFER DATA INTERCHANGE FAILED AT HIGH SPEED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP; SCOPE LOOP

```


/DOES (LOAD CNT) PERFORM LOGIC OR?
/

1043	7300	CLA CLL	/CLEAR AC
1044	6132	CLLR	/STOP CLOCK
1045	1107	TAD K0100	/SET AC 05=1
1046	6132	CLLR	/GENERATE "CLR CNT"
1047	6135	CLSA	/CLEAR CLOCK STATUS
1050	4444	JMS I RANDOM	/GET RANDOM TEST NUMBER
1051	6133	CLAB	/LOAD BUFFER WITH A RANDOM NUMBER
1052	3053	DCA	/SAVE IT
1053	1111	TAD	/SET AC 04=1
1054	6134	CLEN	/LOAD COUNTER FROM THE BUFFER REGISTERI GENERATE "LOAD CNT"
1055	7300	CLA CLL	/CLEAR AC
1056	1053	TAD SEND	/GET TEST NUMBER
1057	7040	CMA	/COMPLEMENT
1060	6133	CLAB	/LOAD BUFFER WITH THE COMPLEMENT OF THE PREVIOUS NUMBER
1061	7300	CLA CLL	/CLEAR AC
1062	1111	TAD K0200	/SET AC 04=1
1063	6134	CLEN	/LOAD COUNTER (OR) IN COMPLEMENT OF THE FIRST NUMBER
1064	6137	CLCA	/READ COUNTER.
1065	3052	DCA	/SAVE IT
1066	1052	TAD	/RESTORE IT
1067	7040	CMA	/CONVERT TO ALL ZEROS FOR TESTING
1070	7650	SNA CLA	/ZERO?
1071	4427	JMS I NERROR	/CHECK MONITOR
1072	4425	JMS I ERROR	/THE (LOAD CNT) SIGNAL FAILED TO "OR" DATA INTO COUNTER
1073	5676	TST27M	/MESSAGE POINTER
1074	7402	HLT	/ERROR HALT
1075	7610	SKP CLA	/TO NEXT TEST
1076	1043	TST27	/ISE LOOPI SCOPE LOOP

/POP-12 KW12A CLOCK TEST, MAINDEC 12-0800=L

/TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 2 (0)

```

1077 7300 /TST28, CLA CLL
1100 6133 CLAB
1101 6132 CLLR
1102 1107 TAD
1103 6132 CLLR
1104 6135 CLSA
1105 4444 JMS I
1106 6133 CLAB
1107 3053 DCA
1110 6132 CLLR
1111 1107 TAD
1112 6132 CLLR
1113 7200 CLA
1114 6132 CLLR
1115 1111 TAD
1116 6134 CLEN
1117 6137 CLCA
1120 3052 DCA
1121 1052 TAD
1122 7650 SNA CLA
1123 4427 JMS I
1124 4425 JMS I
1125 5722 TST28M
1126 7402 HLT
1127 7610 SKP CLA
1130 1077 TST28

/CLEAR AC
/CLEAR BUFFER
/CLEAR ALL MODES
/SET AC 05=1
/GEN. "CLR CNT"
/CLEAR STATUS
/GET RANDOM NUMBER
/SEND IT TO BUFFER
/SAVE IT
/STOP CLOCK, SET ALL MODES=0
/SET AC 05=1
/GENERATE "CLR CNT"
/CLEAR AC
/SET ALL MODES=0
/SET AC 04=1
/TRY TO GENERATE "LOAD CNT"
/GET COUNTER
/SAVE IT
/RESTORE IT
/WAS IT ZERO?
/CHECK MONITOR
/LOAD CNT GATES FUNCTIONED WITH MODE 2=0 IN ERROR
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP! SCOPE LOOP

```

```

1131 444
1132 6133
1133 3053
1134 1117
1135 6132
1136 6135
1137 7200
1140 1111
1141 6134
1142 6137
1143 3052
1144 1052
1145 7650
1146 4427
1147 4425
1150 5747
1151 7402
1152 7610
1153 1131
1154 7340
1155 3045

/TEST LOAD CNT GENERATION GATES (CLR CLOCK RATE) MODE 1(1)
/
TST29, JMS I RANDOM
      CLAB
      DCA SEND
      TAD K0600
      CLLR
      CLSA
      CLA
      TAD K0200
      CLEN
      CLCA
      DCA
      TAD
      SNA CLA
      JMS I NERROR
      JMS I ERROR
      TST29M
      HLT
      SKP CLA
      TST29
      CLA CLL CMA
      DCA REGA

/GET RANDOM NUMBER
/SEND IT TO BUFFER
/SAVE IT
/SET AC 04,05#1
/GENERATE "CLR CNT", SET MODE 1 AND 2 #1
/CLEAR CLOCK STATUS
/CLEAR AC
/SET AC 04#1
/TRY TO GENERATE "LOAD CNT"
/READ COUNTER
/SAVE TEST VALUE
/RESTORE IT
/ZERO?
/CHECK MONITOR
/LOAD CNT GATES FUNCTIONED WITH MODE 1#1 IN ERROR
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP/ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

```

1156 4444 /CLITCH TEST OF LOAD CNT GATES
1157 6133 /TST30. JMS I RANDOM
1160 3053 CLAB SEND
1161 1111 DCA K0200
1162 6132 TAD CLLR
1163 7200 CLA K0300
1164 1113 TAD CLLR
1165 6132 CLA
1166 7200 ISZ REG8
1167 2046 JMP :07
1170 5361 CLCA RXED
1171 6137 DCA RXED
1172 3052 TAD SNA CLA
1173 1052 JMS I NERROR
1174 7650 JMS I ERROR
1175 4427 TST30M
1176 4425 HLT
1177 5774 CLA
1200 7402 TST30
1201 7200 CLA CLL CMA
1202 1156 DCA REGA
1203 7340
1204 3045

/GET RANDOM NUMBER
/SEND IT TO BUFFER
/SAVE IT
/SET AC 04R1
/SET MODE 1R1
/CLEAR AC
/SET AC 04:00R1
/SET MODE 2R1
/CLEAR AC
/DONE?
/BACK 4096 TIMES
/READ COUNTER
/SAVE IT
/RESTORE IT
/ZERO?
/CHECK MONITOR
/THE MODE REGISTER CAUSES ILLEGAL LOAD COUNTER
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC=777
/PRESEY REGA FOR NEXT TEST

```

```

1205 4444
1206 6133
1207 3053
1210 1046
1211 7006
1212 7006
1213 7006
1214 0120
1215 6132
1216 7040
1217 0120
1220 6132
1221 2046
1222 5210
1223 6136
1224 3052
1225 1052
1226 7041
1227 1053
1230 7640
1231 5237
1232 6137
1233 3046
1234 1046
1235 7650
1236 4427
1237 4425
1240 6021
1241 7402
1242 7200
1243 1205
1244 3046

/GENERAL GATE SHAKING TEST OF THE MODE FLIP FLOPS
/
TST31, JMS I RANDOM
      CLAB
      DCA SEND
      TAD REGB
      RTL
      RTL
      RTL
      AND K0700
      CLLR
      CMA
      AND K0700
      CLLR
      ISZ
      JMP REGB
      CLBA TST31+3
      DCA RXED
      TAD RXED
      CIA SEND
      TAD
      SEA CLA
      JMP
      CLCA
      DCA
      TAD
      SNA CLA
      JMS I
      JMS I
      TST31M
      HLT
      CLA
      TST31
      DCA REGB

      /GET RANDOM NUMBER
      /SEND IT TO BUFFER
      /SAVE IT
      /GET TEST COUNTER
      /ROTATE TWO LEFT
      /ROTATE TWO LEFT
      /ROTATE TWO LEFT
      /INSURE THAT MODE 0,1,2=1
      /SEND RANDOM NUMBER TO CONTROL REGISTER
      /COMPLEMENT
      /INSURE THAT MODE 0,1,2=1
      /SET TO COMPLEMENT OF THE NUMBER
      /DONE?
      /BACK 4096 TIMES
      /GET TEST VALUE FROM BUFFER
      /SAVE IT
      /RESTORE IT
      /COMPLEMENT
      /SUBTRACT TEST NUMBER
      /EQUAL?
      /BUFF CHANGED IN ERROR
      /READ COUNTER
      /SAVE IT
      /RESTORE IT
      /STILL ZERO?
      /CHECK MONITOR
      /COUNTER CHANGED IN ERROR
      /MESSAGE POINTER
      /ERROR HALT
      /TO NEXT TEST
      /IS2 LOOP; SCOPE LOOP
      /CLEAR FOR NEXT IS2 LOOP

```

/DOES MODE 2 1-0 CLK CNT?
/TST32,

1245	4444	JMS I	RANDOM
1246	6133	CLAB	SEND
1247	3053	DCA	K0100
1250	6132	CLLR	K0200
1251	1127	TAD	
1252	6132	CLLR	
1253	6135	CLSA	
1254	7200	CLA	
1255	1111	TAD	
1256	6134	CLEN	
1257	7200	CLA	
1260	6132	CLLR	
1261	6137	CLCA	
1262	3052	DCA	RXED
1263	6133	CLAB	RXED
1264	1052	TAD	
1265	7041	CIA	SEND
1266	1053	TAD	
1267	7650	SNA CLA	
1270	4427	JMS I	NERROR
1271	4425	JMS I	ERROR
1272	6056	TST32M	
1273	7402	HLT	
1274	7410	SKP	
1275	1245	TST32	

/DOES MODE 2 0-1 CLOCK CNT?
/TST33,

1276	1127	TAD	K0100
1277	6132	CLLR	
1300	6137	CLCA	
1301	3052	DCA	RXED
1302	1052	TAD	RXED
1303	7650	SNA CLA	
1304	4427	JMS I	NERROR
1305	4425	JMS I	ERROR
1306	6102	TST33M	
1307	7402	HLT	
1310	7410	SKP	
1311	1276	TST33	
1312	7340	CLA CLL	CMA
1313	3045	DCA	REGA
1314	5715	JMP I	.*1
1315	1542	TST43	

```

/GET RANDOM NUMBER
/SEND IT TO BUFFER
/SAVE IT
/ZERO MODE 2
/AC 05*1
/GENERATE "CLR CNT"
/CLEAR STATUS
/CLEAR AC
/SET AC 04*1
/GENERATE "LOAD CNT"
/CLEAR AC
/0 MODE 2
/READ COUNTER
/SAVE IT
/CLEAR BUF OR OVERFLOW WILL RELOAD CNT
/RESTORE IT
/COMPLEMENT
/SUBTRACT TEST NUMBER
/EQUAL?
/CHECK MONITOR
/MODE 2 1-0 DID IT
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP; SCOPE LOOP

```

```

/SET AC 05*1
/GENERATE "CLR CNT"
/READ COUNTER
/SAVE IT
/RESTORE IT
/ZERO?
/CHECK MONITOR
/MODE 2 0-1 FAILED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP; SCOPE LOOP
/SET AC=7777
/PRESET ISZ COUNT
/NEXT TEST

```

/DOES COUNTER OVERFLOW SET OVERFLOW FLOP?

```

1316 7300 TST34, CLA CLL /CLEAR AC
1317 6132 CLLR /CLEAR STATUS
1320 1107 TAD K0100 /SET AC 05#1
1321 6132 CLLR /O TO COUNTER
1322 6135 CLSA /CLEAR CLOCK STATUS
1323 7340 CLA CLL CMA /SET AC#7777
1324 6133 CLAB /SET BUFFER TO 7777
1325 7300 CLA CLL /CLEAR AC
1326 1111 TAD /SET AC 04#1
1327 6134 CLEN /LOAD CNT (00)#1
1330 4157 CLEAR /GENERATE I=0 PRESET
1331 6135 CLSA /GET STATUS OF CLOCK
1332 7710 SPA CLA /OVERFLOW SET?
1333 4427 JMS I NERROR /CHECK MONITOR
1334 4425 JMS I ERROR /OVERFLOW NOT SET
1335 6126 TST34M /MESSAGE POINTER
1336 7402 HLT /ERROR HALT
1337 7410 SKP / OR EGO EM12#25 IS NOT WORKING PROPERLY
1340 1316 TST34 /TO NEXT TEST
1341 7340 CLA CLL CMA /ISZ LOOPJ SCOPE LOOP
1342 3046 DCA REG8 /SET AC#7777
1343 3045 DCA REGA /PRESET ISZ COUNTER FOR NEXT TEST
/RESET REGA

```

```

1344 7300 /DOES CLSA (6135) CLEAR OVERFLOW FLOP?
1345 6132 /
1346 1107 /TST35, CLA CLL
1347 6132 CLLR K0100
1348 6135 TAD
1349 7340 CLLR
1350 6135 CLSA
1351 7340 CLA CLL CMA
1352 6133 CLAB
1353 7300 CLA CLL K0200
1354 1111 TAD
1355 6134 CLEN
1356 4197 CLEAR
1357 6135 CLSA
1360 7300 CLA CLL
1361 6135 CLSA
1362 7700 SMA CLA
1363 4427 JMS I NERROR
1364 4425 JMS I ERROR
1365 6152 TST35M
1366 7402 HLT
1367 7410 SKP
1370 1344 TST35
1371 7340 CLA CLL CMA
1372 3045 DCA REGA

1344 7300 /CLEAR AC
1345 6132 /CLEAR ALL MODES
1346 1107 /SET AC 05=1
1347 6132 /GEN "CLR CNT"
1348 6135 /CLEAR CLOCK STATUS
1349 7340 /SET AC=7777
1350 6133 /SET BUF=7777 OCTAL
1351 7300 /CLEAR AC
1352 1111 /SET AC 04=1
1353 6134 /GEN LOAD CNT
1354 4197 /GENERATE I=0 PRESET
1355 6135 /SET STATUS BIT 0=1
1356 7300 /GET STATUS BIT 0=0
1357 6135 /OVERFLOW SET?
1360 7700 /CHECK MONITOR
1361 4427 /CLSA FAILED TO CLEAR OVERFLOW FLOP
1362 4425 /MESSAGE POINTER
1363 6152 /ERROR HALT
1364 7402 /TO NEXT TEST
1365 7410 /ISE LOOP; SCOPE LOOP
1366 7402 /SET AC=7777
1367 7410 /PRESET REGA FOR NEXT TEST

```



```

1373 7300
1374 6132
1375 1107
1376 6132
1377 6135
1400 7340
1401 6133
1402 7300
1403 1111
1404 6134
1405 4157
1406 6131
1407 4427
1410 4425
1411 6177
1412 7402
1413 7410
1414 1373
1415 7340
1416 3045

/TEST OVERFLOW SKIP
/
TST36, CLA CLL
      CLLR
      TAD K0100
      CLLR
      CLSA CLA CLL CMA
      CLAB
      CLA CLL K0200
      TAD
      CLEN
      CLEAR
      CLSK
      JMS I NERROR
      JMS I ERROR
      TST36M
      HLT
      SKP
      TST36
      CLA CLL CMA
      DCA

/TEST FOR NO INTERRUPT
/
TST37, TAD PNTA
      DCA RETURN
      ION
      NOP
      IOP
      JMS I NERROR
      JMS I ERROR
      TST37M
      HLT
      SKP
      TST37
      CLA CLL CMA
      DCA

1417 1032
1420 3051
1421 6001
1422 7000
1423 6002
1424 4427
1425 4425
1426 6217
1427 7402
1430 7410
1431 1417
1432 7340
1433 3045

/GET RETURN POINTER TO LOCA
/PUT IT IN INTERRUPT HANDLER
/ENABLE INTERRUPTS
/WAIT
/DISABLE INTERRUPTS
/CHECK MONITOR
/ILLEGAL INTERRUPT OVERFLOW#1 OVERFLOW ENABLE#0
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOPJ SCOPE LOOP
/SET AC#7777
/RESET REGA FOR NEXT TEST

/SET AC
/CLEAR ALL MODES
/SET AC 05#1
/GEN #CLR CNT#
/CLEAR CLOCK STATUS
/SET AC#7777
/SET BUF#7777 OCTAL
/CLEAR AC
/SET AC 04#1
/GEN LOAD CNT
/GENERATE I=0 PRESET
/OVERFLOW SET?
/CHECK MONITOR
/CLOCK PRESET DIDN'T 0 OVERFLOW ENABLE
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOPJ SCOPE LOOP
/SET AC#7777
/RESET REGA FOR NEXT TEST

```

```

1434 1107 /SET INT ENABLE
1435 8134 /TST39, TAD K0100
1436 7320 CLEN
1437 6131 CLA CLL
1440 7410 CLSK
1441 4427 SKP
1442 4425 JMS I NERROR
1443 6240 JMS I ERROR
1444 7402 TST38H
1445 7410 HLT
1446 1434 SKP
1447 7340 TST38
1450 3045 CLA CLL CMA
DCA REGA

/TEST FOR CLOCK INTERRUPT
/
1451 1033 /TST39, TAD PNT8
1452 3051 DCA RETURN
1453 6001 ION
1454 7000 NOP
1455 6002 IOF
1456 7410 SKP I NERROR
1457 4427 JMS I ERROR
1460 4425 TST39H
1461 6257 HLT
1462 7402 SKP
1463 7410 TST39
1464 1451 CLA CLL CMA
1465 7340 DCA REGA
1466 3045

/SET AC 05=1
/TURN ON CLOCK OVERFLOW INT
/CLEAR AC
/INTERRUPT SET?
/TO HERE IF INTERRUPT NOT SET
/CHECK MONITOR
/CLKS FAILED TO SKIP OVERFLOW=1 EN OVFL INT=1
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOPJ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

/GET RETURN POINTER TO LOCB
/PUT IT IN INTERRUPT HANDLER
/ENABLE INTERRUPTS
/WAIT
/DISABLE INTERRUPTS
/TO HERE IF NO INTERRUPT
/CHECK WITH MONITOR
/CLOCK INT FAILED TO INTERRUPT
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOPJ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

```

1467 7300 /TEST WITH FLAG UP ZERO OVERFLOW INT ENABLE
1470 6134 /CLEAR AC
1471 6131 /CLOCK ENABLE
1472 4427 /INTERRUPT AVAILABLE?
1473 4425 /CHECK MONITOR
1474 6277 /OVERFLOW ENABLE WON'T ZERO
1475 7402 /MESSAGE POINTER
1476 7410 /ERROR HALT
1477 1467 /TO NEXT TEST
1500 7340 /ISZ LOOPJ SCOPE LOOP
1501 3045 /SET AC=7777
        /PRESET REGA FOR NEXT TEST

```

```

/TEST WITH FLAG ZERO OVERFLOW SET
/
TST41, TAD K0100
        CLEN
        CLA CLL
        CLLR
        CLSA
        CLA CLL
        CLSK
        JMS I NERROR
        JMS I ERROR
        TST41M
        HLT
        SKP
        TST41
        CLA CLL CMA
        DCA REGA

```

```

/TEST INT OVERFLOW=0
/
TST42, TAD PNTC
        DCA RETURN
        ION
        NOP
        IOF
        JMS I NERROR
        JMS I ERROR
        TST42M
        HLT
        SKP
        TST42
        ISZ REGB
        JMP I TST35N
        CLA CLL CMA
        DCA REGA
        JMP I .+1
        TST55

```

1502 1107 /SET AC 05=1
1503 6134 /ENABLE INTERRUPTS
1504 7300 /CLEAR AC
1505 6132 /STOP THE CLOCK
1506 6135 /READ AND ZERO FLAG
1507 7300 /CLEAR AC
1510 6131 /INTERRUPT SET?
1511 4427 /CHECK MONITOR
1512 4425 /BAD INTERRUPT CONDITION STILL EXISTS
1513 6320 /MESSAGE POINTER
1514 7402 /ERROR HALT
1515 7410 /TO NEXT TEST
1516 1502 /ISZ LOOPJ SCOPE LOOP
1517 7340 /SET AC=7777
1520 3045 /PRESET REGA FOR NEXT TEST

1521 1034 /GET RETURN POINTER TO LOCC
1522 3051 /PUT IT IN INTERRUPT HANDLER
1523 6001 /ENABLE INTERRUPTS
1524 7000 /WAIT
1525 6002 /DISABLE INTERRUPTS
1526 4427 /CHECK MONITOR
1527 4425 /ILLEGAL CLOCK INTERRUPT
1530 6340 /MESSAGE POINTER
1531 7402 /ERROR HALT
1532 7410 /TO NEXT TEST
1533 1521 /ISZ LOOPJ SCOPE LOOP
1534 2046 /INCREMENT PASS COUNTER
1535 5456 /CROSS-PAGE TO TEST 35 4096 TIMES
1536 7340 /SET AC=7777
1537 3045 /PRESET REGA FOR NEXT TEST
1540 5741 /NEXT TEST
1541 2354

```

1542 /COUNTER CARRY TESTING
1543 /COUNTER PRESET SUCH THAT CLOCK CNT RAISES BIT IN QUESTION
1544 /
1545 /DOES BIT 11 SET UP?
1546 /
1547 /TST43.
1548   CLA
1549   CLLR
1550   CLAB
1551   TAD
1552   CLLR
1553   CLSA
1554   CLA
1555   DCA
1556   DCA
1557   CLAB
1558   TAD
1559   CLEN
1560   CLA CLL
1561   TAD
1562   CLLR
1563   CLCA
1564   DCA
1565   TAD
1566   SNA CLA
1567   JMP I
1568   IS2
1569   JMP I
1570   SKP I
1571   JMS I
1572   JMS I
1573   TST43M
1574   HLT
1575   SKP
1576   TST43
1577   CLA CLL
1578   DCA
1579   CMA
1580   REGA
1581   3045

2000 /CLEAR AC
2001 /CLEAR ALL MODES
2002 /CLEAR BUF
2003 /SET AC 05=1
2004 /GEN "CLR CNT"
2005 /CLEAR STATUS
2006 /CLEAR AC
2007 /CLEAR COUNTER
2008 /CLEAR SEND
2009 /CLEAR BUFFER
2010 /MODE 1
2011 /ENABLE MODE
2012 /CLEAR AC
2013 /SELECT 100 Hz RATE TO BE USED IN TST 43 TO TST 54
2014 /ENABLE RATE
2015 /READ COUNTER
2016 /SAVE IT
2017 /FETCH IT
2018 /BIT 11 AND ONLY BIT 11 SET?
2019 /IF NOT, WAIT A WHILE
2020 /SET; GO CHECK MONITOR (,=4)
2021 /TIMER DONE?
2022 /NO, GO BACK (,=7)
2023 /TO HERE IF BAD BIT
2024 /CHECK MONITOR
2025 /BIT 11 FAILED TO GET SET BY A CLOCK PULSE
2026 /MESSAGE POINTER
2027 /ERROR HALT
2028 /TO NEXT TEST
2029 /IS2 LOOP; SCOPE LOOP
2030 /SET AC=7777
2031 /PRESET REGA FOR NEXT TEST

8K43.
FD43.

```

/DOES BIT 10 SET UP?
/TST44,

1602 7200
1603 6132
1604 6133
1605 6132
1606 6135
1607 7200
1610 3024
1611 1072
1612 6133
1613 3053
1614 1111
1615 6134
1616 7300
1617 1132
1620 6132
1621 6137
1622 3052
1623 1052
1624 1140
1625 7650
1626 5232
1627 2024
1630 5221
1631 7410
1632 4427
1633 4425
1634 6377
1635 7402
1636 7410
1637 1602
1640 7340
1641 3045

CLA
CLLR
CLAB
CLSA
CLA
DCA
TAD
CLAB
DCA
TAD
CLEN
CLA CLL
TAD
CLLR
CLCA
DCA
TAD
TAD
SNA CLA
JMP
ISZ
JMP
SKP
JMS I
JMS I
TST44M
HLT
SKP
TST44
CLA CLL
DCA

/PRESET FOR BIT 10

/BIT 10, AND ONLY BIT 10, SET?

/CHECK MONITOR
/BIT 10 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOPJ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

/DOES BIT 9 SET UP?

1642	7200	CLA	
1643	6132	CLLR	
1644	6133	CLAB	
1645	1107	TAD	K0100
1646	6132	CLLR	
1647	6135	CLSA	
1650	7200	CLA	
1651	3024	DCA	CNTR
1652	1074	TAD	K0003
1653	6133	CLAB	
1654	3053	DCA	SEND
1655	1111	TAD	K0200
1656	6134	CLEN	
1657	7300	CLA CLL	
1660	1132	TAD	K5100
1661	6132	CLLR	
1662	6137	CLCA	
1663	3052	DCA	RXED
1664	1052	TAD	RXED
1665	1141	TAD	M0004
1666	7650	SNA CLA	
1667	5273	JMP	:+4
1670	2024	ISE	CNTR
1671	5262	JMP	:+7
1672	7410	SKP	
1673	4427	JMS I	NERROR
1674	4425	JMS I	ERROR
1675	6416	TST45M	
1676	7402	HLT	
1677	7410	SKP	
1700	1642	TST45	
1701	7340	CLA CLL CMA	
1702	3045	DCA REGA	

/PRESET FOR BIT 09

/BIT 09, AND ONLY BIT 09, SET?

/CHECK MONITOR
 /BIT 9 FAILED TO GET SET BY COUNTING
 /MESSAGE POINTER
 /ERROR HALT
 /TO NEXT TEST
 /ISE LOOPJ SCOPE LOOP
 /SET AC#7777
 /PRESET REGA FOR NEXT TEST

```

1703 7200
1704 6132
1705 6133
1706 1107
1707 6132
1710 6135
1711 7200
1712 3024
1713 1076
1714 6133
1715 3053
1716 1111
1717 6134
1720 7300
1721 1132
1722 6132
1723 6137
1724 3052
1725 1052
1726 1142
1727 7650
1730 5334
1731 2024
1732 5323
1733 7410
1734 4427
1735 4425
1736 6435
1737 7422
1740 7410
1741 1703
1742 7340
1743 3045

/DOES BIT 8 SET UP?
TST46,
CLA
CLLR
CLAB
YAD
CLLR
CLSA
CLA
DCA
YAD
CLAB
DCA
YAD
CLEN
CLA CLL
TAD
CLLR
CLCA
DCA
YAD
SNA CLA
JMP
ISE
JMP
SKP
JMS I
JMS I
TST46M
HLT
SKP
TST46
CLA CLL
DCA
CMA
REGA

/PRESET FOR BIT 08
CNTR
K0007
SEND
K0200
K5100
RXED
RXED
M0010
.44
CNTR
.07
NERROR
ERROR

/BIT 08, AND ONLY BIT 08, SET?
/CHECK MONITOR
/BIT 8 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP/ SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

```

1744 7200
1745 6132
1746 6133
1747 1107
1750 6132
1751 6135
1752 7200
1753 3024
1754 1101
1755 6133
1756 3053
1757 1111
1760 6134
1761 7300
1762 1132
1763 6132
1764 6137
1765 3052
1766 1052
1767 1143
1770 7650
1771 5375
1772 2024
1773 5364
1774 7410
1775 4427
1776 4425
1777 6454
2000 7402
2001 7410
2002 1744
2003 7340
2004 3045

/DOES BIT 7 SET UP?
/
TST47,
CLA
CLLR
CLAB
TAD
K0100
CLLR
CLSA
CLA
CNTR
K0017
DCA
SEND
K0200
TAD
CLEN
CLA CLL
TAD
K5100
CLLR
CLCA
DCA
RXED
RXED
M0020
TAD
SNA CLA
JMP
JSE
CNTR
JMP
SKP
JMS I
JMS I
TST47M
HLT
SKP
TST47
CLA CLL
CMA
DCA
REGA

/PRESET FOR BIT 07

8K47,

/BIT 07, AND ONLY BIT 07, SET?

/CHECK MONITOR
/BIT 7 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```



```

2005 7200 /DOES BIT 6 SET UP?
2006 6132 /TST48;
2007 6133 TST48;
2010 1107 K0100
2011 6132 CLR
2012 6135 CLSA
2013 7200 CLA
2014 3024 DCA
2015 1103 TAD
2016 6133 CLAB
2017 3053 DCA
2020 1111 SEND
2021 6134 TAD K0200
2022 7300 CLEN
2023 1132 CLA CLL
2024 6132 TAD K5100
2025 6137 CLR
2026 3052 DCA
2027 1052 RXED
2030 1144 TAD M0040
2031 7650 SNA CLA
2032 5236 JMP
2033 2024 ISZ
2034 5225 JMP
2035 7410 SKP
2036 4427 JMS I
2037 4425 JMS I
2040 6473 TST48M
2041 7402 HLT
2042 7410 SKP
2043 2005 TST48
2044 7340 CLA CLL CMA
2045 3045 DCA REGA

/PRESET FOR BIT 06

/BIT 06, AND ONLY BIT 06, SET?

/CHECK MONITOR
/BIT 6 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP; SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

```

2046 7200          /DOES BIT 5 SET UP?
2047 6132          /TST49,
2050 6133          CLA
2051 1107          CLLR
2052 6132          CLAB
2053 6135          TAD
2054 7200          K0100
2055 3024          CNTR
2056 1106          K0077
2057 6133          SEND
2060 3053          K0200
2061 1111          DCA
2062 6134          TAD
2063 7300          CLEN
2064 1132          CLA CLL
2065 6132          TAD
2066 6137          CLLR
2067 3052          DCA
2070 1052          RXED
2071 1146          RXED
2072 7650          M0100
2073 5277          SNA CLA
2074 2024          JMP
2075 5266          ISE
2076 7410          JMP
2077 4427          SKP
2100 4425          JMS I
2101 6512          JMS I
2102 7402          TST49M
2103 7410          HLT
2104 2046          SKP
2105 7340          TST49
2106 3045          CLA CLL
                CMA
                REGA
                DCA

                /PRESET FOR BIT 05

                /BIT 05, AND ONLY BIT 05, SET?

                /CHECK MONITOR
                /BIT 5 FAILED TO GET SET BY COUNTING
                /MESSAGE POINTER
                /ERROR HALT
                /TO NEXT TEST
                /ISE LOOP/ SCOPE LOOP
                /SET AC=777
                /PRESET REGA FOR NEXT TEST

```

/DOES BIT 4 SET UP?

```

2107 7200 CLA
2110 6132 CLLR
2111 6133 CLAB
2112 1107 TAD K0100
2113 6132 CLLR
2114 6135 CLSA
2115 7200 CLA
2116 3024 DCA CNTR
2117 1110 TAD K0177
2120 6133 CLAB
2121 3053 DCA SEND
2122 1111 TAD K0200
2123 6134 CLEN
2124 7300 CLA CLL
2125 1132 TAD K5100
2126 6132 CLLR
2127 6137 CLCA
2130 3052 DCA
2131 1052 TAD
2132 1147 TAD M0200
2133 7650 SNA CLA
2134 5340 JMP
2135 2024 ISZ CNTR
2136 5327 JMP
2137 7410 SKP
2140 4427 JMS I NERROR
2141 4425 JMS I ERROR
2142 6531 TST50H
2143 7402 HLT
2144 7410 SKP
2145 2107 TST50
2146 7340 CLA CLL CMA
2147 3045 DCA REGA

```

/PRESET FOR BIT 04

/BIT 04, AND ONLY BIT 04, SET?

```

/CHECK MONITOR
/BIT 4 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

```

/DOES BIT 3 SET UP↑
/
TST51, CLA
2150 7200
2151 6132 CLLR
2152 6133 CLAB
2153 1127 TAD K0100
2154 6132 CLLR
2155 6135 CLSA
2156 7200 CLA
2157 3024 DCA CNTR K0377
2160 1114 TAD
2161 6133 CLAB
2162 3053 DCA SEND
2163 1111 TAD K0200
2164 6134 CLEN
2165 7300 CLA CLL K5100
2166 1132 TAD
2167 6132 CLLR
2170 6137 CLCA
2171 3052 DCA RXED
2172 1052 TAD RXED
2173 1150 TAD M0400
2174 7650 SNA CLA
2175 5466 JMP I UP51
2176 2024 ISZ CNTR
2177 5370 JMP :07
2200 7410 SKP
2201 4427 JMS I NERROR
2202 4425 JMS I ERROR
2203 6550 TST51M
2204 7402 HLT
2205 7410 SKP
2206 2150 TST51
2207 7340 CLA CLL CMA
2210 3045 DCA REGA

/PRESET FOR BIT 03

/BIT 03, AND ONLY BIT 03, SET?
/ (.04)

/CHECK MONITOR
/BIT 3 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP, SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

```

2211 7200 /DOES BIT 2 SET UPT
2212 6132 /TST52.
2213 6133 CLLA
2214 1107 TAD K0100
2215 6132 CLLR
2216 6135 CLSA
2217 7200 CLA
2220 3024 DCA CNTR
2221 1121 TAD K0777
2222 6133 CLAB
2223 3053 DCA SEND
2224 1111 TAD K0200
2225 6134 CLEN
2226 7300 CLA CLL
2227 1132 TAD K5100
2230 6132 CLLR
2231 6137 CLCA
2232 3052 DCA RXED
2233 1052 TAD RXED
2234 1151 TAD H1000
2235 7650 SNA CLA
2236 5242 JMP
2237 2024 ISZ CNTR
2240 5231 JMP
2241 7410 SKP
2242 4427 JMS I NERROR
2243 4425 JMS I ERROR
2244 6567 TST52M
2245 7402 HLT
2246 7410 SKP
2247 2211 TST52
2250 7340 CLA CLL CMA
2251 3045 DCA REGA

/PRESET FOR BIT 02

/BIT 02. AND ONLY BIT 02. SET?

/CHECK MONITOR
/BIT 2 FAILED TO GET SET BY COUNTING
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

```

2252 7200 /DOES BIT 1 SET UP?
2253 6132 /
2254 6133 TST53.
2255 1107 CLA
2256 6132 CLLR
2257 6135 CLAB
2260 7200 TAD K0100
2261 3024 CLA
2262 1124 DCA CNTR
2263 6133 TAD K1777
2264 3053 CLAB
2265 1111 DCA SEND
2266 6134 TAD K0200
2267 7300 CLEN
2270 1132 CLA CLL
2271 6132 TAD K5100
2272 6137 CLLR
2273 3052 CLCA
2274 1052 DCA
2275 1153 TAD RXED
2276 7650 TAD RXED
2277 5303 SNA CLA M2000
2300 2024 JMP *4
2301 5272 ISZ CNTR
2302 7410 JMP .07
2303 4427 SKP
2304 4425 JMS I NERROR
2305 6606 JMS I ERROR
2306 7402 TST53M
2307 7410 HLT
2310 2252 SKP
2311 7340 TST53
2312 3045 CLA CLL CMA
DCA REGA

```

/PRESET FOR BIT 01

/BIT 01. AND ONLY BIT 01. SET?

/CHECK MONITOR
 /BIT 1 FAILED TO GET SET BY COUNTING
 /MESSAGE POINTER
 /ERROR HALT
 /TO NEXT TEST
 /ISZ LOOP; SCOPE LOOP
 /SET AC=7777
 /PRESET REGA FOR NEXT TEST

```

2313 7200          /DOES BIT 0 SET UP?
2314 6132          /TST54,
2315 6133          CLLA
2316 1107          CLLR
2317 6132          CLAB
2320 6135          TAD
2321 7200          K0100
2322 3024          CNTR
2323 1127          K3777
2324 6133          DCA
2325 3053          TAD
2326 1111          DCA
2327 6134          SEND
2330 7300          K0200
2331 1132          CLEN
2332 6132          CLA
2333 6137          GLL
2334 3052          TAD
2335 1052          K5100
2336 1154          CLLR
2337 7650          CLCA
2340 5344          DCA
2341 2024          RXED
2342 5333          RXED
2343 7410          M4000
2344 4427          SNA
2345 4425          CLA
2346 6625          JMP
2347 7402          ISE
2350 2313          CNTR
2351 5753          JMP
2353 1316          SKP
                JMS I
                JMS I
                TST54M
                HLT
                SKP
                TST54
                JMP I
                TST34
                NERROR
                ERROR
                /CHECK MONITOR
                /BIT 0 FAILED TO GET SET BY COUNTING
                /MESSAGE POINTER
                /ERROR HALT
                /TO NEXT TEST
                /ISE LOOP/ SCOPE LOOP
                /PRESET FOR BIT 00
                /BIT 00, AND ONLY BIT 00, SET?
                /+4
                /+7
    
```

```

2354 7300
2355 1152
2356 3046
2357 1122
2360 6132
2361 7300
2362 2046
2363 7410
2364 5467
2365 6135
2366 7000
2367 7700
2370 5423
2371 4427
2372 4425
2373 6644
2374 7402
2375 7410
2376 2354
2377 7340
2400 3045

/DOES COUNTER COUNT NORMALLY AND AT ALL RATES?
/CHECK 400 KHZ RATE
/
TST55,  CLA CLL
      TAD M1400
      DCA REGB
      TAD      K1000
      CLLR
      CLA CLL
      ISZ REGB
      SKP I UP55
      JMP I UP55
      CLSA
      NOP
      SMA CLA
      JMP I ON55
      JMS I NERRR
      JMS I NERRR
      TST55M
      HLT
      SKP
      TST55
      CLA CLL CMA
      DCA REGA

BK55,

FD55,

/CHECK 100 KHZ RATE
/
TST56,  CLA CLL
      TAD M5400
      DCA REGB
      TAD      K2000
      CLLR
      CLA CLL
      ISZ REGB
      SKP
      JMP
      CLSA
      NOP
      SMA CLA
      JMP
      JMS I NERRR
      JMS I NERRR
      TST56M
      HLT
      SKP
      TST56
      CLA CLL CMA
      DCA REGA

/CLEAR AC
/GET PRESET
/SET UP FOR TIMER
/GET AC 02
/SET 400KC RATE

/INCREMENT COUNT
/TIME OK
/TIMER NOT OK (, +6)
/GET STATUS
/WAIT
/OVERFLOW?
/TRY AGAIN (, +6)
/CHECK MONITOR
/400 KC FAILED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC = 7777
/PRESET REGA

/CLEAR AC
/GET PRESET
/SET UP TIMER
/GET AC 01
/SET 100 KHZ RATE

/INCREMENT COUNT
/TIMER OK
/TIMER NOT OK
/GET STATUS
/WAIT
/OVERFLOW?
/TRY AGAIN
/CHECK MONITOR
/100KC FAILED
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP/ SCOPE LOOP
/SET AC = 7777
/PRESET REGA

```



```

2426 7300
2427 1142
2430 3047
2431 1151
2432 3046
2433 1126
2434 6132
2435 7300
2436 2046
2437 7410
2440 2047
2441 7410
2442 5250
2443 6135
2444 7000
2445 7700
2446 5236
2447 4427
2450 4425
2451 6676
2452 7402
2453 7410
2454 2426
2455 7340
2456 3045
2457 3046

/ CHECK 10 KHZ RATE
/
TST57, CLA CLL M0010
      TAD REGC
      DCA M1000
      DCA REGB
      TAD K3000
      CLLR
      CLA CLL REGB
      ISZ REGC
      SKP REGC
      ISZ REGC
      SKP .+6
      JMP CLSA
      NOP SMA CLA
      JMP .-10
      JMS I NERROR
      JMS I ERROR
      TST57M
      HLT
      SKP
      TST57
      CLA CLL CMA
      DCA REGA
      DCA REGB

/ CLEAR AC
/ GET PRESET
/ SET UP FOR X10

/ SET 10KC RATE

/ INCREMENT COUNT
/ TIMER OK
/ INCREMENT MULTIPLIER
/ MULTIPLIER OK
/ TIMER NOT OK
/ GET STATUS
/ WAIT
/ OVERFLOW?
/ TRY AGAIN
/ CHECK MONITOR
/ 10KC FAILED
/ MESSAGE POINTER
/ ERROR HALT
/ TO NEXT TEST
/ IS2 LOOP/ SCOPE LOOP
/ SET AC = 7777
/ PRESET REGA
/ CLEAR REGB

```

```

2460 7300
2461 1146
2462 3047
2463 1131
2464 6132
2465 7300
2466 2046
2467 7410
2470 2047
2471 7410
2472 5300
2473 6135
2474 7000
2475 7700
2476 5256
2477 4427
2500 4425
2501 6713
2502 7422
2503 7410
2504 2460
2505 7340
2506 3045

/ TEST 1KHZ RATE
/
TST58, CLA CLL M0100
      TAD REGC
      DCA K4100
      CLLR
      CLA CLL REGB
      ISZ REGC
      SKP REGC
      ISZ REGC
      SKP .+6
      JMP CLSA
      NOP SMA CLA
      JMP .-10
      JMS I NERROR
      JMS I ERROR
      TST58M
      HLT
      SKP
      TST58
      CLA CLL CMA
      DCA REGA

/ CLEAR AC
/ GET PRESET
/ SET UP FOR X100
/ SET 1KC RATE

/ INCREMENT COUNT
/ TIMER OK
/ INCREMENT MULTIPLIER
/ MULTIPLIER OK
/ TIMER NOT OK
/ GET STATUS
/ WAIT
/ OVERFLOW?
/ TRY AGAIN
/ CHECK MONITOR
/ 1KC FAILED
/ MESSAGE POINTER
/ ERROR HALT
/ TO NEXT TEST
/ IS2 LOOP/ SCOPE LOOP
/ SET AC = 7777
/ PRESET REGA
/ CLEAR REGB

```

```

2507 7300 /CHECK 100 CPS RATE
2510 3046 /TST59, CLA CLL REGC
2511 1146 DCA M0100
2512 3047 TAD M0100
2513 1150 DCA REGC
2514 6133 TAD M0400
2515 7300 CLA CLL K0200
2516 1111 TAD K0200
2517 6134 CLEN
2520 7300 CLA CLL K5100
2521 1132 TAD K5100
2522 6132 CLLR
2523 7300 CLA CLL REGC
2524 2046 ISZ
2525 7410 SKP
2526 2047 ISZ
2527 7410 SKP
2530 5336 JMP
2531 6135 CLSA
2532 7000 NOP
2533 7700 SMA CLA
2534 5324 JMP
2535 4427 JMS I
2536 4425 JMS I
2537 6727 TST59M
2540 7402 HLT
2541 7610 SKP CLA
2542 2507 TST59
2543 1146 TAD
2544 3045 DCA
2545 3046 DCA

```

```

/CLEAR AC
/CLEAR REGC
/GET PRESET
/SET FOR X100
/GET PRESET
/PRESET BUFFER
/CLEAR AC
/SET AC 05=1
/ENABLE PRESET
/SET 100 CPS RATES
/ENABLE RATE
/CLEAR AC
/INCREMENT TIME
/INCREMENT MULTIPLIER
/TIME OK
/TIME NOT OK1 RATE FAILED
/GET STATUS
/WAIT
/OVERFLOW?
/TRY AGAIN
/CHECK MONITOR
/RATE 100 HZ FAILED
/CLEAR REGC

```



```

2573 1072
2574 6134
2575 6132
2576 6132
2577 7300
2600 6134
2601 6135
2602 0127
2603 3053
2604 6135
2605 0074
2606 3052
2607 1052
2610 7640
2611 5470
2612 1053
2613 7041
2614 1074
2615 7650
2616 4427
2617 4425
2620 6766
2621 7402
2622 7410
2623 2573

/SIMULATED INPUT TESTS CHANNEL 3
/TST61, TAD K0001
CLEN
CLLR
CLLR
CLA CLL
CLEN
CLSA
AND K3777
DCA SEND
CLSA
AND K0003
DCA RXED
TAD RXED
SEA CLA
JMP I UP61
TAD SEND
CIA
TAD K0003
SNA CLA
JMS I NERROR
JMS I ERROR
TST61M
HLT
SKP
TST61

/SET AC 11=1
/ENABLE CHANNEL 3
/SET EVENT FLOP
/SET SET PRE-EVENT FLOP
/CLEAR AC
/CLEAR ENABLES
/GET STATUS
/IGNORE OIFLO
/SAVE IY
/GET STATUS AGAIN
/SAVE CHANNEL 3
/SAVE IY
/FETCH IT
/CHANNEL 3 07 INPUT CHANNEL 3 (.+6)
/CLSA DOESN'T 0
/GET STATUS
/2'S COMPLEMENT
/SUBTRACT SET
/EQUAL?
/CHECK MONITOR
/BOTH PRE-EVENT AND EVENT NOT SET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP; SCOPE LOOP

```

```

2624 1075 /SIM INPUT TESTS CHAN 2
2625 6134 /TST62, TAD K0004
2626 6132 CLEN
2627 6132 CLLR
2630 7300 CLA CLL
2631 6134 CLEN
2632 6135 CLSA
2633 0127 AND K3777
2634 3053 DCA SEND
2635 6135 CLSA K0014
2636 0100 AND RXED
2637 3052 DCA RXED
2640 1052 TAD CLA
2641 7640 SEA CLA
2642 5250 JMP .+6
2643 1053 TAD SEND
2644 7041 CIA
2645 1100 TAD K0014
2646 7650 SNA CLA
2647 4427 JMS I NERROR
2650 4425 JMS I ERROR
2651 7010 TST62M
2652 7402 HLT
2653 7410 SKP
2654 2624 TST62

/SET AC 09#1
/ENABLE CHAN 2
/SET EVENT FLOP
/SET PREVENT FLOP
/CLEAR AC
/CLEAR ENABLES
/GET STATUS
/IGNORE OIFLO
/SAVE IT
/GET STATUS
/SAVE CHANNEL 2
/SAVE IT
/FETCH IT
/0?
/CLSA DOESN'T 0 INPUT CHANNEL 2
/GET FIRST STATUS
/2'S COMPLEMENT
/SUBTRACT SET
/EQUAL?
/CHECK MONITOR
/BOTH PRE-EVENT AND EVENT NOT SET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP; SCOPE LOOP

```

/SIM INPUT TESTS CHAN 1

2655 1102
 2656 6134
 2657 6132
 2660 6132
 2661 7300
 2662 6134
 2663 6135
 2664 0127
 2665 3053
 2666 6135
 2667 0105
 2670 3052
 2671 1052
 2672 7640
 2673 5301
 2674 1053
 2675 7041
 2676 1105
 2677 7650
 2700 4427
 2701 4425
 2702 7032
 2703 7402
 2704 7410
 2705 2655
 2706 7340
 2707 3045

TST63, TAD K0020
 CLEN
 CLLR
 CLLR
 CLA CLL
 CLEN
 CLSA
 AND K3777
 DCA SEND
 DCA
 CLSA K0060
 AND RXED
 DCA RXED
 TAD CLA
 SEA CLA
 JMP
 TAD SEND
 CIA
 TAD K0060
 SNA CLA
 JMS I NERROR
 JMS I ERROR
 TST63M
 HLT
 SKP
 TST63
 CLA CLL CMA
 DCA REGA

/SET AC 07*1
 /SET ENABLE
 /SET EVENT FLOP
 /SET PREVENT FLOP
 /CLEAR AC
 /CLEAR ENABLES
 /GET STATUS
 /IGNORE 0IFLO
 /SAVE IT
 /GET STATUS
 /SAVE CHANNEL 1
 /SAVE IT
 /FETCH IT
 /ZERO?
 /CLSA DOESNIT 0 INPUT CHANNEL 1
 /GET FIRST STATUS
 /2'S COMPLEMENT
 /SUBTRACT SET
 /EQUAL?
 /CHECK MONITOR
 /BOTH PRE-EVENT AND EVENT NOT SET
 /MESSAGE POINTER
 /ERROR HALT
 /TO NEXT TEST
 /IS2 LOOP1 SCOPE LOOP
 /SET AC=7777
 /PRESET REGA

```

/TEST INPUT CHANNEL INTERRUPT CHAN 1
/
TST64, 1035 /GET RETURN POINTER TO LOCD
2710 3051 /SET UP INTERRUPT RETURN
2711 1105 /ENABLE INPUT AND INTERRUPT
2712 6134 /ENABLE
2713 6132 /SIMULATE INPUT CHANNEL ONE
2714 6001 /ENABLE INTERRUPTS
2715 7000 /WAIT
2716 7410 /NO INTERRUPT
2717 4427 /CHECK MONITOR
2720 4425 /NO INTERRUPT ERROR
2721 7054 /MESSAGE POINTER
2722 7482 /ERROR HALT
2723 7610 /TO NEXT TEST
2724 2710 /ISE LOOP
2725 7340 /SET AC=7777
2726 3045 /PRESET REGA
2727

LOC0,
JMS I NERROR
JMS I ERROR
TST64M
HLT
SKP CLA
TST64
CLA CLL CMA
DCA REGA

/TEST WITH INTERRUPTS DISABLED
/
TST65, 1102 /CLEAR INTERRUPT ENABLE SET SIMULATE INPUT
2730 6134 /ENABLE
2731 7300 /CLEAR AC
2732 1036 /GET RETURN POINTER TO LOCE
2733 3051 /PUT IT IN INTERRUPT HANDLER
2734 6001 /ENABLE INTERRUPTS
2735 7000 /WAIT
2736 6002 /DISABLE INTERRUPTS
2737 4135 /CLEAR CLOCK STATUS
2740 4427 /CHECK MONITOR
2741 4425 /INTERRUPT IN ERROR
2742 7072 /MESSAGE POINTER
2743 7402 /ERROR HALT
2744 7610 /TO NEXT TEST
2745 2730 /ISE LOOPJ SCOPE LOOP
2746 7340 /SET AC=7777
2747 3045 /PRESET REGA
2750 2046 /DO THE PAIR OF TESTS 4096 TIMES
2751 5310 /BACK
2752 JMP TST64

```

```

/TEST INPUT CHANNEL INTERRUPT CHAN 2
/
TST66,      TAD      PNTF      /GET RETURN POINTER TO LOCF
            DCA      RETURN     /SET UP INTERRUPT RETURN
            TAD      K0014      /SET AC 08, 09=1
            CLEN     /ENABLE CHANNEL 2
            CLLR     /ENABLE RATES
            ION      /ENABLE INTERRUPTS
            NOP      /WAIT
            SKP      /TO HERE IF NO INTERRUPT
            JMS I    NERROR     /CHECK MONITOR
            JMS I    ERROR     /NO INTERRUPT
            TST66M   /MESSAGE POINTER
            HLT      /ERROR HALT
            SKP      /TO NEXT TEST
            TST66    /ISZ LOOPJ SCOPE LOOP
            CLA CLL  CMA       /SET AC=7777
            DCA      REGA      /PRESET REGA

```

```

/TEST WITH INTERRUPTS DISABLED
/
TST67,      TAD      K0004      /SET AC 09=1
            CLEN     /ENABLE CHANNEL 2
            CLA CLL  PNTG      /CLEAR AC
            TAD      RETURN     /GET RETURN POINTER TO LOCG
            DCA      /PUT IT IN INTERRUPT HANDLER
            ION      /ENABLE INTERRUPTS
            NOP      /WAIT
            JOF      /DISABLE INTERRUPTS
            CLSA     /CLEAR CLOCK STATUS
            JMS I    NERROR     /CHECK MONITOR
            JMS I    ERROR     /INTERRUPT IN ERROR--CLEA EN EVENT 2 INT BAD
            TST67M   /MESSAGE POINTER
            HLT      /ERROR HALT
            SKP      /TO NEXT TEST
            TST67    /ISZ LOOPJ SCOPE LOOP
            CLA CLL  CMA       /SET AC=7777
            DCA      REGA      /PRESET REGA
            ISZ     /DO THIS PAIR OF TESTS 4096 TIMES
            JMP I    TST66N     /BACK

```

2753 1037
2754 3051
2755 1100
2756 6134
2757 6132
2760 6001
2761 7000
2762 7410
2763 4427
2764 4425
2765 7112
2766 7402
2767 7410
2770 2753
2771 7340
2772 3045

2773 1075
2774 6134
2775 7300
2776 1040
2777 3051
3000 6001
3001 7000
3002 6002
3003 6135
3004 4427
3005 4425
3006 7133
3007 7402
3010 7410
3011 2773
3012 7340
3013 3045
3014 2046
3015 5457


```

3016 1041
3017 3051
3020 1074
3021 6134
3022 6132
3023 6001
3024 7000
3025 6002
3026 7410
3027 4427
3030 4425
3031 7152
3032 7402
3033 7410
3034 3016
3035 7340
3036 3045

/TEST INPUT CHANNEL INTERRUPT CHAN 3
/
TST69; TAD PNTI
DCA RETURN
TAD K0003
CLEN
CLLR
ION
NOP
IOF
SKP
JMS I NERROR
JMS I ERROR
TST68M
HLT
SKP
TST68
CLA CLL CMA
DCA REGA

/TEST WITH INTERRUPTS DISABLED
/
TST69; AND K0001
CLEN
CLA CLL
TAD PNTI
DCA RETURN
ION
NOP
IOF
CLSA
JMS I NERROR
JMS I ERROR
TST69M
HLT
SKP
TST69
CLA CLL CMA
DCA REGA
ISZ
JMP TST68
TAD M0040
DCA REGA

/GET RETURN POINTER TO LOCH
/SET UP INTERRUPT RETURN
/SET AC10,11#1
/ENABLE CHANNEL 3
/ENABLE RATES
/ENABLE INTERRUPTS
/WAIT
/DISABLE INTERRUPTS
/NO INTERRUPT
/CHECK MONITOR
/NO INTERRUPT
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA

/SET AC 11#1
/ENABLE CHANNEL 3
/CLEAR AC
/GET RETURN POINTER TO LOCI
/PUT IT IN INTERRUPT HANDLER
/ENABLE INTERRUPTS
/WAIT
/DISABLE INTERRUPTS
/CLEAR CLOCK STATUS
/CHECK MONITOR
/INTERRUPT IN ERROR
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA
/DO THIS PAIR OF TESTS 4096 TIMES
/BACK
/PRESET REGA IF NEXT TEST IS TO BE EXECUTED

```

```

/TEST OF INPUT CHNNEL 3
/KNOBS OF CHAN1,CHAN2,CHAN3 SET TO LINEFREQ, LEVEL IS DISABLED:
/TS770,
3064 6135      CLSA
3065 7300      CLA CLL
3066 6132      CLLR
3067 1074      TAD      K0003
3070 6134      CLEN
3071 7200      CLA
3072 2046      ISZ
3073 7410      SKP
3074 5277      JMP
3075 6131      CLSK
3076          JMP
3077 6135      CLSA
3100 3052      DCA
3101 3046      DCA
3102 1052      TAD
3103 7041      CIA
3104 1073      TAD
3105 7650      SNA CLA
3106 4427      JMS I
3107 4425      JMS I
3110 7212      TST70M
3111 7402      HLT
3112 7410      SKP
3113 3064      TST70
3114 1144      TAD
3115 3045      DCA

/CLEAR STATUS
/CLEAR AC
/CLEAR ALL MODES
/SET AC 10, 11*1
/ENABLE CHAN3 INPUT AND INTER,
/CLEAR AC
/INCREMENT TIMER
/NOT DONE YET
/TIMER OUT/ ERROR CONDITION
/SKIP ON CLOCK INTER.
/WAIT
/GET CLOCK STATUS
/SAVE IT
/CLEAR COUNT
/RESTORE IT
/2'S COMPLEMENT
/ADD EVENT 3
/EQUAL?
/CHECK WITH MONITOR
/CHAN 3 EVENT NOT SET, OR PRE-EVENT WAS SET, OR OTHER CHAN UP
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP/ SCOPE LOOP
/PRESET REGA
M0040
REGA

```

/TEST OF INPUT CHANNEL 2

```

3116 6135
3117 7320
3120 6132
3121 1100
3122 6134
3123 7200
3124 2046
3125 7410
3126 5331
3127 6131
3130 5324
3131 6135
3132 3052
3133 3046
3134 1052
3135 7041
3136 1077
3137 7650
3140 4427
3141 4425
3142 7240
3143 7422
3144 7410
3145 3116
3146 1144
3147 3045

/TEST OF INPUT CHANNEL 2
TST71.
  CLSA
  CLA CLL
  CLLR
  TAD K0014
  CLEN
  CLA
  ISZ REG8
  SKP 1=3
  JMP CLSK
  JMP 1=4
  CLSA
  DCA
  DCA
  TAD
  CIA
  TAD K0010
  SNA CLA
  JMS I NERROR
  JMS I ERROR
  TST71M
  HLT
  SKP
  TST71
  TAD M0040
  DCA REGA

/CLEAR STATUS
/CLEAR AC
/ZERO ALL MODES
/ENAB, CHAN. 2 INPUT AND INTERRUPT FLOPS
/ENABLE
/CLEAR AC
/INCREMENT TIMER
/NOT DONE YET
/TIMER OUT/ ERROR CONDITION
/CHECK FOR CLOCK INTER.
/WAIT
/GET STATUS
/SAVE IT
/CLEAR COUNT
/RESTORE IT
/2'S COMPLEMENT
/ADD EVENT 2
/EQUAL?
/CHECK MONITOR
/CHAN 2 EVENT NOT SET, OR PRE-EVENT WAS SET, OR OTHER CHAN UP
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP; SCOPE LOOP
/PRESET REGA

```

/TEST OF INPUT CHAN 1

```

3150 6135
3151 7300
3152 6132
3153 1105
3154 6134
3155 7200
3156 2046
3157 7410
3160 5363
3161 6131
3162 5356
3163 6135
3164 3052
3165 3046
3166 1052
3167 7041
3170 1104
3171 7650
3172 4427
3173 4425
3174 7266
3175 7402
3176 7410
3177 3150
3200 7340
3201 3045

/TEST OF INPUT CHAN 1
TST72, CLSA
CLA CLL
CLR
TAD K0060
CLEN
CLA
ISZ
SKP
JMP
CLSK
JMP
CLSA
DCA
DCA
TAD
CIA
TAD
SNA CLA
JMS I
JMS I
TST72M
HLT
SKP
TST72
CLA CLL CMA
DCA REGA

/CLEAR STATUS
/CLEAR AC
/CLEAR ALL MODES
/SET AC=7777
/ENABLE CHAN 1 INPUT AND INTERRUPT
/CLEAR AC
/INCREMENT TIMER
/NOT DONE YET
/TIMER OUT/ ERROR CONDITION
/CHECK FOR CLOCK INTER.
/WAIT
/GET CLOCK STATUS
/SAVE IT
/CLEAR COUNT
/RESTORE IT
/COMPLEMENT
/ADD INPUT 1
/EQUAL?
/CHECK MONITOR
/CHAN 1 EVENT NOT SET; OR PREVENT WAS SET; OR OTHER CHAN UP
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCORE LOOP
/SET AC=7777
/PRESET REGA

```

```

3202 7404 OSR
3203 7006 RTL
3204 7006 RTL
3205 7024 RAL
3206 7710 SPA CLA
3207 5461 JMP I TST77N
3210 6141 LINC
3211 0011 CLR
3212 0004 ESF
3213 0100 SAM0
3214 0002 POP
3215 3053 DCA
3216 6141 LINC
3217 0101 SAM1
3220 0011 CLR
3221 1020 LDAI
3222 0100 0100
3223 0024 ESF
3224 0002 POP
3225 6135 CLSA
3226 7300 CLA CLL K0400
3227 1115 TAD
3230 6132 CLLR
3231 6141 LINC
3232 0100 SAM0
3233 0100 SAM0
3234 0002 PDP
3235 3052 DCA
3236 1052 TAD
3237 7041 CIA
3240 1053 TAD
3241 7640 SEA CLA
3242 4427 JMS I
3243 4425 JMS I ERROR
3244 7314 TST73M
3245 7422 HLT
3246 7410 SKP
3247 3202 TST73
3250 7340 CLA CLL CMA
3251 3045 DCA REGA

/TEST FAST SAMPLE MODE IF BIT 04=0
/
TST73,
/IF RIGHT SW BIT 2(1)
/SKIP FAST SAM TEST?
/RSW 04=1?
/INDIRECT REF TO TST77
/ENTER LINC MODE
/CLR AC
/CLR SPEC. IN REG.
/READ KNOB ZERO
/BACK TO PMODE
/TO PAGE 0
/BACK TO LMODE
/READ KNOB 1
/CLR AC
/PICK UP AC BIT 03

/ENABLE FAST SAM
/ENTER POP-8 MODE
/CLR CLOCK STATUS
/CLR AC
/SET MODE BIT0=1
/ENABLE COUNT
/ENTER LINC MODE
/FAST SAM SET THEREFORE READ IN KNOB 1
/SHOULD STILL READ KNOB1
/ENTER POP-8 MODE
/SAVE VALUE
/RESTORE IT
/2'S COMPLEMENT
/COMPARE IT
/EQUAL?
/CHECK MONITOR
/READING FAST SAM CONVERTED IN ERROR
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP; SCOPE LOOP
/SET AC=7777
/PRESET REGA FOR NEXT TEST

```

/TEST FAST SAMPLE WITH MODE 2=1 (CHECK THAT KNOBS 0 & 1 ARE SET PROPERLY)

```

3252 1116 TAD K0500
3253 6132 CLLR
3254 7330 CLA CLL CML RAR
3255 6133 CLAB
3256 7200 CLA
3257 1111 TAD K0200
3260 6134 CLEN
3261 7200 CLA
3262 6133 CLAB
3263 7200 CLA
3264 6132 CLLR
3265 1116 TAD K0500
3266 6132 CLLR
3267 6141 LINC
3270 0100 SAM0
3271 0002 PDP
3272 3052 DCA
3273 1052 TAD
3274 7041 CIA
3275 1053 TAD
3276 7650 SNA CLA
3277 4427 JMS I
3300 4425 JMS I
3301 7333 TST74M
3302 7402 HLT
3303 7410 SKP
3304 3252 TST74
3305 7340 CLA CLL
3306 3045 DCA
3307 2046 ISE
3310 5202 JMP
3311 1144 TAD
3312 3046 DCA

/SET AC 03,05=1
/MODE 2(1),0(1)
/SET AC=4000
/SET BUFF=4000
/CLEAR AC
/SET AC 04=1
/LOAD CTN FROM BUF
/CLEAR AC
/CLR BUF
/CLEAR AC
/CLEAR ALL MODES
/SET AC 03,05=1
/SET OVERFLOW MODE 0(1)
/ENTER LINC MODE
/SAMPLE KNOB 0
/ENTER PDP=B MODE
/STORE
/RESTORE
/2'S COMPLEMENT
/ADD FIRST SAMPLE
/EQUAL?
/CHECK MONITOR
/CONVERSION NOT INITIATED BY OVFLOW
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP I SCOPE LOOP
/SET AC#7777
/REGA FOR NEXT TEST
/DONE?
/BACK

```

```

3313 7200 /CHECK THAT MODE 0(0),1(1),2(1) DO NOT AFFECT SAMPLE
3314 6132 /TST75,
3315 1113 /CLA
3316 6132 /CLLR
3317 6141 /TAD
3320 0011 /CLLR
3321 0024 /LINC
3322 0120 /CLR
3323 0002 /ESP
3324 3053 /SAM0
3325 6141 /PDP
3326 0101 /DCA
3327 1020 /LINC
3330 0100 /SAMI
3331 0004 /LDAI
3332 0100 /0100
3333 0002 /ESP
3334 3052 /SAM0
3335 1052 /POP
3336 7041 /DCA
3337 1053 /TAD
3340 7640 /SEA CLA
3341 4427 /JMS I
3342 4425 /JMS I
3343 7355 /TST75M
3344 7402 /HLT
3345 7410 /SKP
3346 3313 /TST75
3347 7340 /CLA CLL CMA
3350 3045 /DCA REGA

```

```

/CLEAR AC
/ZERO ALL MODES
/SET AC04,05=1
/MODE 1(1),2(1),0(0)
/ENTER LINC MODE
/CLEAR AC
/ZERO SPEC. IN. REG.
/SAMPLE KNOB 0
/TO PMODE
/SAVE KNOB 0
/TO LMODE
/SAMPLE KNOB 1
/PICK UP AC 05
/SET FAST SAM FLOP
/GET KNOB 1 SETTING
/ENTER POP MODE
/STORE
/RECEIVE
/RIS COMPLEMENT
/COMPARE
/EQUALY
/CHECK MONITOR
/FAST SAM NOT SET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC#777
/PRESET REGA FOR NEXT TEST

```

```

K0300
SEND
RXED
RXED
SEND
NERROR
ERROR

```

/NOW CHECK FOR INHIBITING OF FAST SAM

```

3351 6141
3352 0100
3353 0002
3354 3052
3355 1052
3356 7041
3357 1053
3360 7650
3361 4427
3362 4425
3363 7376
3364 7402
3365 7410
3366 3351
3367 7340
3370 3045
3371 2046
3372 5460
3373 1144
3374 3046

/ENTER LINC MODE
/READ KNOB 0
/ENTER POP MODE
/STORE
/RESTORE
/2'S COMPLEMENT
/COMPARE
/EQUAL?
/CHECK MONITOR
/MODE 2(1),1(1) INHIBIT FAST SAM
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/PRESET REGA FOR NEXT TEST
/DONE?
/BACK VIA PAGE 0
/PRESET REGB

LINC
SAM0
PDP
DCA
TAD
CIA
TAD
SNA CLA
JMS I
JMS I
TST76H
HLT
SKP
TST76
CLA CLL
DCA
ISZ
JMP I
TAD
DCA
RXED
RXED
SEND
NERROR
ERROR
CMA
REGA
REGB
TST75N
M0040
REGB

```


/DOES TO PRESET CLEAR OVFLO, ENABLES, RATES AND MODES
 /PROGRAMED IO PRESET USED

```

3375 7200          /TST77, CLA
3376 6132          /CLEAR ALL MODES
3377 6134          /CLEAR ALL ENABLES
3400 1126          TAD K3000
3401 6132          CLLR
3402 7200          CLA
3403 1135          TAD K6000
3404 7001          IAC
3405 7440          SZA
3406 5204          JMP :=2

          /SET AC 00:01#1
          /INCREMENT COUNTER
          /DONE?
          /WAIT LOOP 4.92 MSEC
  
```

/NOW DO IO PRESET CHECK IF RATE BITS 1,2 CLEAR

```

3407 4157          CLEAR
3410 6137          CLCA
3411 3053          DCA SEND
3412 1135          TAD K6000
3413 7001          IAC
3414 7440          SZA
3415 5213          JMP :=2
3416 6137          CLCA
3417 7041          CIA
3420 1053          TAD SEND
3421 7650          SNA CLA
3422 4427          JMS I NERROR
3423 4425          JMS I ERROR
3424 7423          TST77M
3425 7422          HLT
3426 7410          SKP
3427 3375          TST77
3430 7340          CLA CLL CMA
3431 3045          DCA REGA
3432 2046          ISZ REGB
3433 5461          JMP I TST77N
3434 1344          TAD M0040
3435 3046          DCA REGB

          /GENERATE I-O PRESET
          /GET COUNTER
          /STORE
          /SET UP DELAY
          /INCREMENT COUNTER
          /DONE?
          /WAIT LOOP 4.92 MSEC
          /READ COUNTER AGAIN
          /2'S COMPLEMENT
          /COMPARE
          /HAS COUNTER CHANGED?
          /CHECK MONITOR
          /IO PRESET FAILED TO CLEAR RATE BITS 1 & 2
          /MESSAGE POINTER
          /ERROR HALT
          /TO NEXT TEST
          /IS2 LOOP SCOPE LOOP
          /SET AC=7777
          /PRESET REGA FOR NEXT TEST
          /LOOP BACK

          /PRESET REGB
  
```

```

3436 7200 /NOW ENABLE RATE BIT 0
3437 6132 /TST79, CLA
3440 6134 CLLR
3441 1130 TAD K4000
3442 6132 CLLR
3443 7200 CLA
3444 7001 IAC
3445 7440 SEA
3446 5244 JMP I=2

```

```

/CLEAR AC
/CLEAR ALL MODES
/CLEAR ENABLES
/SET AC 00=1
/SET RATE=1KHZ
/INCREMENT COUNTER
/DONE?
/WAIT LOOP 16 MSEC

```

/NOW DO IO PRESET AND SEE IF BIT 0 CLEARED

```

3447 4157 CLEAR
3448 6137 CLCA
3451 3053 DCA SEND
3452 7001 IAC
3453 7440 SEA I=2
3454 5252 JMP SEND
3455 6137 CLCA
3456 7041 CIA
3457 1053 TAD CLA
3460 7650 SNA CLA NERROR
3461 4427 JMS I ERROR
3462 4425 JMS I ERROR
3463 7457 TST79M
3464 7402 HLT
3465 7410 SKP
3466 3036 TST79
3467 7340 CLA CLL CMA
3470 5045 DCA REGA
3471 2046 ISZ REGB
3472 5462 JMP I TST79N
3473 3045 DCA REGA

```

```

/GENERATE I=0 PRESET
/READ COUNTER
/STORE
/INCREMENT COUNTER
/DONE?
/WAIT 16 MSEC
/READ COUNTER AGAIN
/2'S COMPLEMENT
/COMPARE
/COUNTER STILL THE SAME
/CHECK MONITOR
/RATE BIT 0 SET AFTER IO PRESET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP1 SCOPE LOOP
/SET AC=7777
/PRESET REGA
/LOOP BACK
/BACK VIA PAGE 0
/CLEAR REGA IF EXECUTING NEXT TEST

```

/DOES OVERFLOW AND OVFL0 INT. FLOP
/CLEAR WITH IO PRESET

```

3474 7200          CLA
3475 6132          CLR
3476 1107          TAD          K0100
3477 6132          CLR
3500 6135          CLSA
3501 7240          CLA CMA
3502 6133          CLAB
3503 7200          CLA
3504 1111          TAD          K0200
3505 6134          CLEN
3506 4157          CLEAR
3507 4157          CLEAR
3510 6135          CLSA
3511 7700          SMA CLA
3512 4427          JMS I   NERR0R
3513 4425          JMS I   ERR0R
3514 7511          TST81M
3515 7402          HLT
3516 7410          SKP
3517 3474          TST81

/CLEAR AC
/CLEAR ALL MODES

/SET MODE 2(1)
/CLEAR STATUS

/SET BUF TO 7777

/LOAD COUNTER
/GENERATE 1=0 PRESET THIS ONE WILL SET OVERFLOW
/THIS ONE WILL CLEAR IT
/GET STATUS

/CHECK MONITOR
/OVFLO STILL SET AFTER IO PRESET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOPJ SCOPE LOOP

```

```

3520 7200
3521 1107
3522 6132
3523 6135
3524 7240
3525 6133
3526 7200
3527 1111
3530 6134
3531 4157
3532 6132
3533 1107
3534 6132
3535 6131
3536 4427
3537 4425
3540 7534
3541 7402
3542 7610
3543 3520

/TEST OVFL0 INT ENABLE
/TST02.
  CLA
  TAD K0100
  CLLR
  CLSA CMA
  CLAB
  CLA
  TAD K0200
  CLEN
  CLEAR
  CLLR
  TAD K0100
  CLLR
  CLSK
  JMS I NERR0R
  JMS I ERR0R
  TST02M
  HLT
  SKP CLA
  TST02

/CLEAR AC
/SET MODE 2(1)
/CLEAR STATUS
/SET BU0 PRESET REG.

/LOAD CNT WITH 4000
/GENERATE I=0 PRESET; WHIS WILL SET OVERFLOW
/CLEAR ALL MODES
/GEN.

/CHECK MONITOR
/OVFL0 INTER; SET AFTER I/O PRESET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP; SCOPE LOOP

```

/DOES IO PRESET CLEAR INPUT ENABLE FLOPS

```

3544 7200          CLA
3545 6132          CLLR
3546 1106          TAD
3547 6134          CLEN
3550 4157          CLEAR
3551 6135          CLSA
3552 7200          CLA
3553 1106          TAD
3554 6132          CLLR
3555 7200          CLA
3556 6135          CLSA
3557 0127          AND
3560 7650          SNA CLA
3561 4427          JMS I
3562 4425          JMS I
3563 4310          TSTB3M
3564 7402          HLT
3565 7610          SKP CLA
3566 3544          TSTB3

          /CLEAR ALL MODES
          /ENABLE INPUTS TO ALL CHAN
          /GENERATE I=0 PRESET
          /CLEAR STATUS

          /SIMULATE INPUTS ON ALL CHAN

          /GET STATUS
          /IGNORE 0IFLO

          /CHECK MONITOR
          /STATUS NOT ZERO I/O PRESET FAILED
          /MESSAGE POINTER
          /ERROR HALT
          /TO NEXT TEST
          /ISZ LOOP; SCOPE LOOP

```

```

/DOES 10 PRESET CLEAR MODE 2
/
TST84.
3567 6133      CLAB
3570 6132      CLLR
3571 1127      TAD      K0100
3572 6132      CLLR
3573 4157      CLEAR
3574 1134      TAD
3575 6133      CLAB      K5555
3576 7200      CLA
3577 1111      TAD      K0200
3600 6134      CLEN
3601 6137      CLCA
3602 7700      SMA CLA
3603 4427      JMS I   NERROR
3604 4425      JMS I   ERROR
3605 4334      TST84M
3606 7402      HLT
3607 7610      SKP CLA
3610 3567      TST84
3611 7340      CLA CLL CMA
3612 3045      DCA      REGA

/CLEAR MODES
/SET MODE 2(1) = CLR CNT
/GENERATE I-O PRESET
/LOAD BUF WITH 5555

/GEN LOAD CNT
/LOAD CNT TO AC

/CHECK MONITOR
/MODE 2 NOT CLEARED BY I/O PRESET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOPJ SCOPE LOOP
/SET AC = 7777
/PRESET REGA

```

```

3613 7604 /DOES IO PRESET CLEAR MODE 0
3614 7006 /TST85;
3615 7006 /
3616 7710 LAS
3617 5320 RTL
3620 7220 SPA CLA RESET
3621 6132 JMP
3622 6141 CLA
3623 0120 CLLR
3624 0002 LINC
3625 3053 SAM0
3626 6141 PDP
3627 0101 DCA
3630 0002 LINC
3631 7200 SAM1
3632 1115 PDP
3633 6132 CLA
3634 6141 TAD
3635 1020 K0400
3636 0020 CLLR
3637 0004 LINC
3640 1020 LDAI
3641 0100 ESP
3642 0004 LDAI
3643 0100 ESP
3644 0002 SAM0
3645 7041 PDP
3646 1053 CIA
3647 7640 TAD
3650 4427 SEA CLA SEND
3651 4425 JMS I NERROR
3652 4360 JMS I ERROR
3653 7402 TST85M
3654 7410 HLT
3655 3613 SKP
3656 7340 TST85
3657 3045 CLA CLL CMA REGA
DCA

```

/IF RIGHT SW BIT 4(1)
/SKIP FAST SAM TEST

/CLEAR ALL MODES
/ENTER LINC MODE
/READ KNOB 0

/READ KNOB 1
/ENTER PDP MODE

/SET MODE 0(1)
/ENTER LINC MODE

/DO IO PRESET

/ENABLE FAST SAM

/READ KNOB 1=FAST S. MODE
/ENTER PDP MODE

/CHECK MONITOR
/FAST SAM NOT SET
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TAPE
/IS2 LOOP/ SCOPE LOOP
/SET AC = 7777
/PRESET REGA

```

3660 6141
3661 0100
3662 0002
3663 7041
3664 1053
3665 7650
3666 4427
3667 4425
3670 4425
3671 7402
3672 7410
3673 3660
3674 7340
3675 3045
3676 2046
3677 5213

/ENTER LINC MODE
/READ KNOB 0
/ENTER POP MODE

/NOV CHECK FOR MODE 0 CLEARED
TST06, LINC
      SAM0
      PDP
      CIA
      TAD SEND
      SNA CLA
      JMS I NERROR
      JMS I ERROR
      TST86M
      HLT
      SKP
      TST86
      CLA CLL CMA
      DCA REGA
      ISE REGB
      JMP TST85

/RESET ANYTHING LEFT HANGING
/RESET, CLEAR
      TAD M0040
      DCA REGA

/GENERATE I=0 PRESET
/PRESET REGA PRIOR TO NEXT TEST

```



```

/DOES MODE 1(1) WORK CHAN 1
TST07, CLA
3703 7200 /CLEAR ALL MODES
3704 6132 CLLR /CLEAR BUF
3705 6133 CLAB /GET RANDOM NUM
3706 4444 JMS I RANDOM
3707 3053 DCA SEND
3710 1053 TAD SEND
3711 6133 CLAB
3712 7200 CLA
3713 1107 TAD K0100
3714 6132 CLLR
3715 6135 CLSA
3716 7200 CLA
3717 1111 TAD K0200
3720 6134 CLEN
3721 6132 CLLR
3722 7200 CLA
3723 6133 CLAB
3724 1105 TAD K0060
3725 6134 CLEN
3726 2046 ISZ REG8
3727 7410 SKP .+3
3730 5333 JMP .+4
3731 6131 CLSK
3732 5326 JMP
3733 6135 CLSA
3734 7200 CLA
3735 3046 DCA REG8
3736 6136 CLBA
3737 7041 CIA
3740 1053 TAD SNA CLA
3741 7650 JMS I NERROR
3742 4427 JMS I ERROR
3743 4425 TSTB7M
3744 4425 HLT
3745 7422 SKP
3746 7410 TSTB7
3747 3703 TAD M0040
3750 1144 DCA REGA
3751 3045

/CLEAR ALL MODES
/CLEAR BUF
/GET RANDOM NUM

/SEND RANDOM NUM TO BUF

/GEN "CLR CNT"
/CLEAR CLOCK STATUS

/GEN LOAD CNT
/SET MODE BIT 1(1)

/CLEAR BUFFER

/ENABLE INPT 1 AND INT CHAN1
/INCREMENT TIMER
/NOT DONE YET
/TIME OUT
/SKP ON CLOCK INT

/CLEAR STATUS
/CLEAR REG8
/GET BUFFER

/COMPARE

/CHECK MONITOR
/CHAN 1 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP

```

```

3752 6134
3753 6135
3754 7200
3755 6133
3756 1100
3757 6134
3760 2046
3761 7410
3762 5365
3763 6131
3764 5360
3765 6135
3766 7200
3767 3046
3770 6136
3771 7041
3772 1053
3773 7650
3774 4427
3775 4425
3776 4453
3777 7402
4000 7410
4001 3752
4002 1144
4003 3045

/DOES MODE 1 (1) WORK CHAN 2
/TST88,
CLEN
CLSA
CLA
CLAB
TAD
CLEN
ISE
SKP
JMP
CLSK
JMP
CLSA
CLA
DCA
CLBA
CIA
TAD
SNA CLA
JMS I
JMS I
TST88M
HLT
SKP
TST88
TAD
DCA

K0014
REGB
I=3
I=4
REGB
SEND
NERRR
ERROR
M0040
REGA

/CLEAR ENABLES
/CLEAR CLOCK STATUS
/CLEAR BUFFER
/ENABLE CHAN 2 INPUT AND INT
/INCREMENT TIMER
/NOT DONE YET
/TIME OUT
/SKP ON CLOCK INT
/CLEAR STATUS
/CLEAR REGB
/GET BUFFER
/COMPARE
/CHECK MONITOR
/CHAN2 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISE LOOP1 SCOPE LOOP

```

/DOES MODE 1 (1) WORK CHAN 3

```

4004 6134 /CLEAR ENABLE
4005 6135 /CLEAR STATUS
4006 7200 /CLEAR BUFFER
4007 6133 /ENABLES CHAN 3 INPUT AND INT
4010 1074 /INCREMENT TIMER
4011 6134 /NOT DONE YET
4012 2046 /TIME OUT
4013 7410 /SKIP ON CK INT
4014 5217 /CLEAR CLOCK STATUS
4015 6131 /CLEAR REGB
4016 5212 /GET BUF
4017 6135 /COMPARE
4020 7200 /CHECK MONITOR
4021 3046 /CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
4022 6136 /MESSAGE POINTER
4023 7041 /ERROR HALT
4024 1053 /TO NEXT TEST
4025 7650 /ISZ LOOP1 SCOPE LOOP
4026 4427 /SET AC=7777
4027 4425 /PRESET REGA
4030 4501 /PRESET REGB
4031 7402
4032 7410
4033 4024
4034 7340
4035 3045
4036 1144
4037 3046

```

```

/STB9,
CLEN
CLSA
CLA
CLAB
TAD
K0003
CLEN
ISZ
SKP
REGB
JMP
.03
JMP
.04
CLSA
REGB
CLA
DCA
REGB
CIA
SEND
TAD
SNA CLA
NERRR
JMS I
ERROR
TSTB9M
HLT
SKP
TSTB9
CLA CLL
CMA
DCA
REGA
TAD
M0040
REGB
DCA

```

```

4040 6134
4041 1113
4042 1122
4043 6132
4044 7200
4045 1113
4046 6132
4047 6137
4050 3053
4051 6135
4052 7200
4053 6133
4054 1125
4055 6134
4056 2050
4057 7410
4060 5263
4061 6131
4062 5256
4063 6135
4064 7200
4065 3050
4066 6136
4067 7041
4070 1053
4071 7650
4072 4427
4073 4425
4074 4527
4075 7402
4076 7410
4077 4040
4100 7340
4101 3045

/TEST MODE 1(1) AND MODE 2(1) CHAN 1
/
TST90, CLEN
TAD K0300
TAD K1000
CLLR
CLA
TAD
CLLR
CLCA
DCA
CLSA
CLA
CLAB
TAD
CLEN
ISE
SKP
JMP
CLSK
JMP
CLSA
CLA
DCA
CLBA
CIA
TAD
SNA CLA
JMS I
JMS I
TST90M
HLT
SKP
TST90
CLA CLL
DCA

/CLEAR ENABLES
/START CNT RATE=400KHZ * MODE 1(1) AND 2(1)
/STOP CNT - MODE 1(1) AND 2(1)
/GET CNT
/STORE
/CLEAR BUF
/ENABLE CHAN1 INPUT AND INT
/INCREMENT TIMER
/NOT DONE YET
/TIME OUT
/SKP ON CLOCK INT
/CLEAR CLOCK STATUS
/CLEAR TIMER
/GET BUF
/COMPRE
/CHECK MONITOR
/CHAN1 FAILED TO CAUSE CNT TO BUF TRANSFER
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/IS2 LOOP/ SCOPE LOOP

```

```

/TEST MODE 1 (1) AND MODE 2 (1) CHAN 2
/
TST91.
4102 6134 CLEN /CLEARS ENABLES
4103 6135 CLSA /CLEAR STATUS
4104 7200 CLA /CLEAR BUF
4105 6133 CLAB
4106 1100 TAD K0014
4107 6134 CLEN /ENABLE CHAN 2 INPUT AND INT
4110 2050 ISZ /INCREMENT TIMER
4111 7410 SKP /NOT DONE YET
4112 5315 JMP /TIME OUT
4113 6131 CLSK /SKP ON CLOCK INT
4114 5310 JMP
4115 6135 CLSA /CLEAR STATUS
4116 7200 CLA /CLEAR REGT
4117 3050 DCA
4120 7000 NOP
4121 6136 CLBA /GET BUF
4122 7041 CIA /COMPARE
4123 1053 TAD SEND
4124 7650 SNA CLA
4125 4427 JMS I NERROR
4126 4425 JMS I ERROR
4127 4555 TST91M
4130 7402 HLT
4131 7610 SKP CLA
4132 4102 TST91
4133 7340 CLA CLL CMA
4134 3045 DCA REGA /PRESET REGA

```

```

/TEST MODE 1 (1) AND MODE 2 (1) CHAN 3
/
TST92:
4135 6134 CLEN /CLEAR ENABLES
4136 6135 CLSA /CLEAR BUF
4137 7200 CLA /ENABLES CHAN3 INPUT AND INT
4140 6133 CLAB /INCREMENT TIMER
4141 1074 TAD /NOT DONE YET
4142 6134 CLEN /TIME OUT
4143 2050 ISZ /SKP ON CLOCK INT
4144 7410 SKP /CLEAR CLOCK STATUS
4145 3350 JMP .+3 REGT
4146 6131 CLSK .e4
4147 5343 JMP /CLEAR REGT
4150 6135 CLSA SEND
4151 7200 CLA NERRR
4152 3050 DCA ERRR
4153 7000 NOP
4154 6136 CLBA
4155 7041 CIA
4156 1053 TAD SNA CLA
4157 7050 JMS I
4160 4427 JMS I
4161 4425 TST92M
4162 4003 HLT
4163 7402 SKP
4164 7410 TST92
4165 4135 CLA CLL CMA
4166 7340 DCA REGA
4167 3045
/CHAN 3 INPUT FAILED TO CAUSE CNT TO BUF TRANSFER
/MESSAGE POINTER
/ERROR HALT
/TO NEXT TEST
/ISZ LOOP1 SCOPE LOOP
/SET AC = 7777
/PRESET REGA

```

```

4170 6137
4171 3052
4172 1052
4173 7650
4174 4427
4175 4425
4176 4631
4177 7402
4200 7410
4201 4170
4202 7340
4203 3045
4204 2046
4205 5463
4206 1144
4207 3045

/ CHECK THAT CHAN 3 CLEARED COUNTER FROM TEST 92
/
TST93, CLCA /GET CNT
DCA RXED
TAD RXED
SNA CLA
JMS I NERROR
JMS I ERROR
TST93M
HLT
SKP
TST93
CLA CLL CMA
DCA REGA
ISZ REGB
JMP I TST90N
TAD M0040
DCA REGA

```

```

4210 1135
4211 3050
4212 1214
4213 6135
4214 7300
4215 1107
4216 6132
4217 6134
4220 1125
4221 6132
4222 6131
4223 5222
4224 2050
4225 5224
4226 7200
4227 6132
4230 6134
4231 6135
4232 6137
4233 7440
4234 7710
4235 4427
4236 4425
4237 4657
4240 7402
4241 7410
4242 4210

/ CHECK THAT OIFLO ALWAYS TRANSFERS BUFFER TO COUNTER ON MODE 2(1)
/
TST94, TAD K6000
DCA REGT
TAD K7300
CLAB
CLA CLL K0100
TAD K2000
CLLR
CLEN
TAD
CLLR
CLSK
JMP
ISZ
JMP
CLA
CLLR
CLEN
CLSA
CLCA
SZA SPA CLA
JMS I NERROR
JMS I ERROR
TST94M
HLT
SKP
TST94

```

/GET THE COUNTER
/0 IS OK
/COUNTER SHOULD NEVER GO POSITIVE
/ECO EM12-00034 IS EITHER NOT INSTALLED OR NOT WORKING

```

/TEST THAT THE CLOCK COUNTER IS INCREMENTED
/ BY 1 WITH AN I=0 PRESET

```

```

4243 7300          CLA CLL          /CLEAR REGA
4244 3045          DCA              /PRESET SEND TO 0000
4245 3053          DCA              /CLEAR CLOCK
4246 6132          CLLR            /GET 0100
4247 1107          TAD              /
4250 6132          CLLR            /
4251 6135          CLSA            /LOAD PRESET BUFFER
4252 7300          CLA CLL          /GET 0200
4253 6133          CLAB            /ENABLE
4254 7300          CLA CLL          /GENERATE I=0 PRESET
4255 1111          TAD              /INCREMENT DATA
4256 6134          CLEN            /READ COUNTER
4257 4157          TAD              /SAVE VALUE
4260 2053          ISZ              /GET IT BACK
4261 7000          NOP              /NEGATE IT
4262 6137          CLCA            /ADD EXPECTED VALUE
4263 3052          DCA              /ARE THEY EQUAL ?
4264 1052          TAD              /YES, NO ERROR
4265 7041          CIA              /NO, ECO EM12-00055 IS NOT INSTALLED
4266 1053          TAD              /OR NOT WORKING CORRECTLY
4267 7650          SNA CLA          /
4270 4427          JMS I           /
4271 4425          JMS I           /
4272 4716          TST95M          /
4273 7402          HLT              /
4274 7410          SKP              /
4275 4257          TST95N          /

```

```

/ALERT OPERATOR OF PASS COMPLETION
/SUPPRESS PRINTOUT IF RSW 06 = 1

```

```

4276 2031          ISZ              /INCREMENT PASS
4277 7000          NOP              /DON'T SKIP
4300 7604          LAS              /READ SWITCHES
4301 0104          AND              /PICK OUT RSW 06
4302 7640          SZA CLA          /SET?
4303 5176          JMP              /YES, NO PRINTOUT
4304 1043          TAD              /GET POINTER
4305 3425          DCA I           /CHEAT MONITOR
4306 5430          JMP I           /GO TYPE ALARM
4307 4755          TST96M          /MESSAGE POINTER

```

```

/LOGJ,
/RETJRN TO LOC 176 FROM ASCII TYPEOUT (MONITOR WILL HANDLE LINK)

```



```

5000 *5000
5001 /NON ERROR MONITOR DETERMINES IF OPERATOR WANTS TO LOOP ON NONFAILING TEST
5002 /RETURN ADDRESS
5003 /SET AC = 4
5004 /GET RETURN ADDRESS
5005 /UPDATE RETURN ADDRESS
5006 /GET SCOPE LOOP ADDRESS
5007 /STORE IT
5008 /UPDATE DATA
5009 /EXIT
5010 /READ SWITCHES
5011 /SAVE SR3
5012 /TEST AND CLEAR
5013 /LOOPING
5014 /SET AC=-1
5015 /ADD NERROS
5016 /STORE IN NERROS
5017 /JUMP INDIRECT LOOP

5020 /ERROR PROCESSOR, SCOPE LOOP, HALT, PRINT
5021 /RETURN ADDRESS STORAGE
5022 /READ SWITCHES
5023 /MOVE SR1 INTO AC00
5024 /IS IT SET
5025 /NO TYPE A MESSAGE
5026 /RING THE BELL
5027 /GET CURRENT ERROR ADDRESS
5028 /INVERT IT
5029 /STORE IN LAST ERROR
5030 /YES INDEX ESCAPE
5031 /READ SWITCHES
5032 /IS SR0 SET
5033 /NO ERROR HALT
5034 /YES INDEX ESCAPE TO JUMP OUT
5035 /INDEX ERRORS TO SCOPE MODE
5036 /GET SCOPE ADDRESS
5037 /STORE IN TYPE
5038 /READ SWITCHES
5039 /MOVE SR02 TO AC0
5040 /IS SCOPE MODE SELECTED
5041 /YES CONTINUE IN SCOPE LOOP
5042 /NO SET AC#7777 (=1)
5043 /SUBTRACT ONE FROM ERRORS
5044 /STORE SELECTED ADDRESS
5045 /EXIT TO NEXT TEST
5046
5047
5050

```

5051	7240	ASCII,	CLA CMA	ERRORS	/SET CIAC)=-1
5052	1620	TAD I	DCA	PINT	/GET MESSAGE ADDRESS STORAGE
5053	3010	DCA	TAD	ERRORS	/STORE IT IN AUTO INDEX REGISTER
5054	1220	TAD	TAD	ERRORS	/GET RETURN ADDRESS
5055	1026	TAD	TAD	LSTERR	/SUBTRACT LAST ERROR ADDRESS
5056	7650	SNA CLA	SNA CLA		/TEST
5057	5363	JMP	DATYP	DATYP	/SAME GO TYPE DATA
5060	1410	TAD I	PINT	PINT	/GET FIRST CHARACTER
5061	3200	DCA	NERROS	NERROS	/SAVE IT
5062	1200	TAD	NERROS	NERROS	/GET IT
5063	7450	SNA	ASCRXT	ASCRXT	/TEST IT
5064	5226	JMP	CMA	CMA	/NUMBER=EXIT;
5065	7040	CMA	SNA	SNA	/INVERT IT
5066	7450	SNA	JMP	DATUM	/NUMBER=EXITA
5067	5315	JMP	CMA CLL	DATUM	/TYPE OUT DATA ROUTINE
5070	7040	CMA CLL	RTR	RTR	/CHANGE IT BACK
5071	7112	RTR	RTR	RTR	/SWAP AC TO THE RIGHT
5072	7012	RTR	JMS	TYPECH	/MOVE
5073	7012	RTR	TAD	NERROS	/MOVE
5074	4300	JMS	JMS	NERROS	/TYPE IT
5075	1200	TAD	JMS	TYPECH	/GET IT AGAIN
5076	4300	JMS	JMP	ASCII*7	/TYPE IT
5077	5260	JMP	TYPECH* 0	ASCII*7	/MUST BE MORE WORDS THAT NEED TYPING
5100	0000	AND	K0077	K0077	/SAVE SIGNIFICANT PART
5101	0106	DCA	SPACE	SPACE	/STORE WORD
5102	3055	TAD	SPACE	SPACE	/FETCH IT
5103	1055	TAD	SNA CLA	CRLF	/TEST FOR 00 CRLF CODE
5104	7650	JMS	TAD	SPACE	/YES IT WAS
5105	4354	TAD	SPA	M0040	/NO TYPE IT
5106	1055	TAD	TAD	K0100	/SUBTRACT 40
5107	1144	TAD	TAD	K240	/TEST POLARITY
5110	7510	SPA	TAD	TYPE	/ADD 340
5111	1107	TAD	JMS I	TYPE	/ADD 240
5112	1112	TAD	JMP I	TYPECH	/TYPE
5113	4464	JMS I	JMP I	TYPECH	/EXIT
5114	5700	JMP I			

5115	1410	DATUM,	TAD I	PINT	/GET ADDRESS OF REGISTER
5116	3200		DCA	NERROS	/STORE IN TEMP
5117	1200		TAD	NERROS	/GET TEMP
5120	7650		SNA	CLA	/TEST FOR EXIT
5121	5226		JMP	ASCRXT	/EQUALS 0000 EXIT
5122	1200		TAD	NERROS	/GET TEMP
5123	1153		TAD	M4444	/\$\$
5124	7650		SNA	CLA	/TEST
5125	5176		JMP	176	/SPECIAL RESTART
5126	1600		TAD I	NERROS	/GET DATA
5127	4333		JMS	OCTYP	/TYPE IT
5130	1112		TAD	K240	/SPACE
5131	4464		JMS I	TYPE	/TYPE IT
5132	5315		JMP	DATUM	/TYPE NUMERIC DATA
5133	0000	OCTYP,	Ø		/RETURN ADDRESS STORAGE
5134	3300		DCA	TYPECH	/STORE DATA TO BE PRINTED
5135	1136		TAD	K7774	/SET UP TALLY
5136	3055	HERE,	DCA	SPACE	/SET IT
5137	1123	REDO,	TAD	K1026	/GET FLAG NUMBER
5140	3394		DCA	CRLF	/STORE
5141	1300		TAD	TYPECH	
5142	7004		RAL		
5143	3300		DCA	TYPECH	
5144	1354		TAD	CRLF	
5145	7004		RAL		
5146	7420		SNL		
5147	5340		JMP	REDO	
5150	4464		JMS I	TYPE	
5151	2055		ISE	SPACE	
5152	5337		JMP I	HERE	
5153	5733		JMP I	OCTYP	
5154	0000		Ø		
5155	1374	CRLF,	TAD	K0215	/EXIT
5156	4464		JMS I	TYPE	/RETURN ADDRESS STORAGE
5157	1375		TAD	K0212	/GET CR
5160	4464		JMS I	TYPE	/TYPE IT
5161	1110		TAD	K0177	/TYPE IT
5162	5754		JMP I	CRLF	/SET TO RUBOUT
5163	1410	DATYP,	TAD I	PINT	/EXIT
5164	7450		SNA		/GET A TERM OFF OF TYPE LIST
5165	5226		JMP	ASCRXT	/END OF LIST?
5166	7040		CMA		/YES EXIT
5167	7640		SEA	CLA	/INVERT
5170	5363		JMP	DATYP	/BEGINNING OF DATA
5171	4354		JMS	CRLF	/NO
5172	7300		CLA	CLL	/YES OK RETURN THE TTY CARRIAGE AND LINE FEED
5173	5315		JMP	DATUM	/CLEAR AC AND LINK
5174	0215	K0215,	Ø215		/GO TYPE THE DATA
5175	0212	K0212,	Ø212		

```

5200 5200 #5200
0000 BELLS, 0
7604 LAS K0100
0107 AND SEA CLA
7640 SEA CLA
5203 JMP I BELLS
5204 JMP I K0007
5205 TAD TYPE
1076 TAD TYPE
4464 JMP I BELLS
5206 JMP I BELLS
5207 RANDY, 0
5210 TAD RNA
1240 TAD RNB
1241 TAD RNC
1242 TAD K5252
5213 TAD RNA
3240 DCA RNA
7004 RAL RNA
1240 TAD RNA
1241 TAD RNB
1242 TAD RNC
1133 TAD K5252
5221 TAD RNA
3241 DCA RNB
7004 RAL RNA
1240 TAD RNA
1241 TAD RNB
1242 TAD RNC
1133 TAD K5252
5231 TAD RNA
7004 RAL RNA
1240 TAD RNA
3240 DCA RNA
1241 TAD RNB
1242 TAD RNC
5237 JMP I RANDY
7601 RNA, 7601
3542 RNB, 3542
3755 RNC, 3755

```

/RING THE BELL

/RANDOM NUMBER GENERATOR

```

5243 0000 TYP0UT, 0
5244 6046 TLS
5245 6041 TSF
5246 5245 JMP .=1
5247 6042 TCF
5250 7300 CLA CLL TYP0UT
5251 5643 JMP I TYP0UT
5252 0000 SETN, 0
5253 7300 CLA CLL
5254 3031 DCA PASS
5255 3045 DCA REGA
5256 3046 DCA REGB
5257 3026 DCA LSTERR
5260 5652 JMP I SETN

```

/CLEAR FLAG

/RESET PASS COUNTER

/TEXT TEST ERROR MESSAGES

/TST10 CLAB CHANGED AC

5261	0024	TST12M:	0024
5262	2324		2324
5263	6160		6160
5264	4003		4003
5265	1401		1401
5266	0240		0240
5267	0310		0310
5270	0116		0116
5271	0705		0705
5272	0440		0440
5273	0103		0103
5274	4000		4000
5275	7777		EXITA
5276	0045		REGA
5277	0052		RXED
5300	0000		EXIT

/TST11 CLBA FAILED

5301	0024	TST11M:	0024
5302	2324		2324
5303	6161		6161
5304	4003		4003
5305	1402		1402
5306	0140		0140
5307	0601		0601
5310	1114		1114
5311	0504		0504
5312	4000		4000
5313	7777		EXITA
5314	0053		SEND
5315	0052		RXED
5316	0000		EXIT

/TST12 CLAB FAILED

5317	0024	TST12M:	0024
5320	2324		2324
5321	6162		6162
5322	4003		4003
5323	1401		1401
5324	0240		0240
5325	0601		0601
5326	1114		1114
5327	0504		0504
5330	4000		4000
5331	7777		EXITA
5332	0053		SEND
5333	0052		RXED
5334	0000		EXIT

/TST13 CLAB FAILED

5335	0024	TST13M:	0024
5336	2324		2324
5337	6163		6163
5340	4003		4003
5341	1401		1401

5342 0240
5343 0601
5344 1114
5345 0504
5346 4000
5347 7777
5350 0045
5351 0052
5352 0000

/TST14 CLAB FAILED

TST14M: 0024
5353 0024
5354 2324
5355 6164
5356 4003
5357 1401
5360 0240
5361 0601
5362 1114
5363 0504
5364 4000
5365 7777
5366 0053
5367 0052
5370 0000

/TST15 CLBA CHANGED BUFFER

TST15M: 0024
5371 0024
5372 2324
5373 6165
5374 4003
5375 1402
5376 0140
5377 0310
5400 0116
5401 0705
5402 0440
5403 0225
5404 0606
5405 0522
5406 4000
5407 7777
5410 0053
5411 0052
5412 0000

/TST16 CLAB <> CLBA FAILED

TST16M: 0024
5413 0024
5414 2324
5415 6166
5416 4003
5417 1401
5420 0274
5421 7603
5422 1402
5423 0140
5424 0601
5425 1114

5426 0524 0504
 5427 4000 4000
 5430 7777 EXITA
 5431 0045 REGA
 5432 0052 RXED
 5433 0000 EXIT

/TST17 CLAB <> CLBA FAILED

TST17M: 0024
 5434 0024 0024
 5435 2324 2324
 5436 6167 6167
 5437 4003 4003
 5440 1401 1401
 5441 0274 0274
 5442 7603 7603
 5443 1402 1402
 5444 0140 0140
 5445 0601 0601
 5446 1114 1114
 5447 0504 0504
 5450 4000 4000
 5451 7777 EXITA
 5452 0053 SEND
 5453 0052 RXED
 5454 0000 EXIT

/TST18 CLAB <> CLBA FAILED

TST18M: 0024
 5455 0024 0024
 5456 2324 2324
 5457 6170 6170
 5460 4003 4003
 5461 1401 1401
 5462 0274 0274
 5463 7603 7603
 5464 1402 1402
 5465 0140 0140
 5466 0601 0601
 5467 1114 1114
 5470 0504 0504
 5471 4000 4000
 5472 7777 EXITA
 5473 0053 SEND
 5474 0052 RXED
 5475 0000 EXIT

/TST19 CLEN CHANGED AC

TST19M: 0024
 5476 0024 0024
 5477 2324 2324
 5500 6171 6171
 5501 4003 4003
 5502 1405 1405
 5503 1640 1640
 5504 0310 0310
 5505 0116 0116
 5506 0705 0705
 5507 0440 0440
 5510 0103 0103
 5511 4000 4000

5512 7777
 5513 0045
 5514 0052
 5515 0000

/TST20 CLEN CHANGED BUFFER

5516 0024
 5517 2324
 5520 6260
 5521 4003
 5522 1405
 5523 1640
 5524 0310
 5525 0116
 5526 0705
 5527 0440
 5530 0225
 5531 0606
 5532 0522
 5533 4000
 5534 7777
 5535 0045
 5536 0052
 5537 0000

/TST21 CLCA FAILED

5540 0024
 5541 2324
 5542 6261
 5543 4003
 5544 1403
 5545 0140
 5546 0601
 5547 1114
 5550 0504
 5551 4000
 5552 7777
 5553 0053
 5554 0052
 5555 0000

/TST22 "CLR CNT" FAILED

5556 0024
 5557 2324
 5560 6262
 5561 4042
 5562 0314
 5563 2240
 5564 0316
 5565 2442
 5566 4006
 5567 0111
 5570 1405
 5571 0400
 5572 7777
 5573 0053
 5574 0052
 5575 0000

/TST23 CLEN FAILED

5576	0024	TST23M:	0024
5577	2324		2324
5600	6263		6263
5601	4003		4003
5602	1405		1405
5603	1640		1640
5604	0601		0601
5605	1114		1114
5606	0504		0504
5607	4000		4000
5610	7777		EXITA
5611	0045		REGA
5612	0052		RXED
5613	0000		EXIT

/TST24 CLEN FAILED

5614	0024	TST24M:	0024
5615	2324		2324
5616	6264		6264
5617	4003		4003
5620	1405		1405
5621	1640		1640
5622	0601		0601
5623	1114		1114
5624	0504		0504
5625	4000		4000
5626	7777		EXITA
5627	0053		SEND
5630	0052		RXED
5631	0020		EXIT

/TST25 CLCA CHANGES COUNT

5632	0024	TST25M:	0024
5633	2324		2324
5634	6265		6265
5635	4003		4003
5636	1403		1403
5637	0140		0140
5640	0310		0310
5641	0116		0116
5642	0705		0705
5643	2340		2340
5644	0317		0317
5645	2516		2516
5646	2400		2400
5647	7777		EXITA
5650	0053		SEND
5651	0052		RXED
5652	0000		EXIT

/TST26 BUFFER <> COUNTER FAILED

5653	0024	TST26M:	0024
5654	2324		2324
5655	6266		6266
5656	4002		4002
5657	2506		2506
5660	0605		0605

5661 2274 2274
 5662 7603 7603
 5663 1725 1725
 5664 1624 1624
 5665 0522 0522
 5666 4006 4006
 5667 0111 0111
 5670 1405 1405
 5671 0400 0400
 5672 7777 EXITA
 5673 0053 SEND
 5674 0052 RXED
 5675 0000 EXIT

/TST27 "LOAD CNT" FAILS TO "OR"

TST27M: 0024
 2324
 6267
 4042
 1417
 0104
 4003
 1624
 4240
 0601
 1114
 2340
 2417
 4042
 1722
 4200
 EXITA
 SEND
 RXED
 EXIT

/TST28 "LOAD CNT" LOADED IN ERROR

TST28M: 0024
 2324
 6270
 4042
 1417
 0104
 4003
 1624
 4240
 1417
 0104
 0504
 4011
 1640
 0522
 2217
 2200
 EXITA
 SEND
 RXED

5722 0024 0024
 5723 2324 2324
 5724 6270 6270
 5725 4042 4042
 5726 1417 1417
 5727 0104 0104
 5730 4003 4003
 5731 1624 1624
 5732 4240 4240
 5733 1417 1417
 5734 0104 0104
 5735 0504 0504
 5736 4011 4011
 5737 1640 1640
 5740 0522 0522
 5741 2217 2217
 5742 2200 2200
 5743 7777 EXITA
 5744 0053 SEND
 5745 0052 RXED

5746 0000
 5747 0024
 5750 2324
 5751 6271
 5752 4042
 5753 1417
 5754 0104
 5755 4003
 5756 1624
 5757 4240
 5760 1417
 5761 0104
 5762 0504
 5763 4011
 5764 1640
 5765 0522
 5766 2217
 5767 2200
 5770 7777
 5771 0053
 5772 0052
 5773 0000

EXIT
 TST29M, 0024
 2324
 6271
 4042
 1417
 0104
 4003
 1624
 4240
 1417
 0104
 0504
 4011
 1640
 0522
 2217
 2200
 EXITA
 SEND
 RXED
 EXIT

5774 0024
 5775 2324
 5776 6360
 5777 4015
 6000 1704
 6001 0540
 6002 2205
 6003 0740
 6004 0301
 6005 2523
 6006 0523
 6007 4042
 6010 1417
 6011 0104
 6012 4003
 6013 1624
 6014 4200
 6015 7777
 6016 0053
 6017 0052
 6020 0000

TST30M, 0024
 2324
 6360
 4015
 1704
 0540
 2205
 0740
 0301
 2523
 0523
 4042
 1417
 0104
 4003
 1624
 4200
 EXITA
 SEND
 RXED
 EXIT

6021 0024
 6022 2324
 6023 6361
 6024 4015
 6025 1704
 6026 0540
 6027 2205
 6030 0740
 6031 0301
 6032 2523

TST31M, 0024
 2324
 6361
 4015
 1704
 0540
 2205
 0740
 0301
 2523

/TST29 "LOAD CNT" LOADED IN ERROR

/TST30 MODE REG CAUSES "LOAD CNT"

/TST31 MODE REG CAUSES "LOAD CNT" OR "CLR BUF"

6033 0523
 6034 4042
 6035 1417
 6036 0104
 6037 4003
 6040 1624
 6041 4240
 6042 1722
 6043 4042
 6044 0314
 6045 2240
 6046 0225
 6047 0642
 6050 4000
 6051 7777
 6052 0053
 6053 0052
 6054 0046
 6055 0000

/TST32 MODE 21 1>0 CLOCKED CNTR

TST32M: 0024
 2324
 6362
 4015
 1704
 0540
 6272
 4061
 7660
 4003
 1417
 0313
 0504
 4003
 1624
 2200
 EXITA
 SEND
 RXED
 RECB
 EXIT

/TST33 MODE 21 0>1 CLOCKED CNTR

TST33M: 0024
 2324
 6363
 4015
 1704
 0540
 6272
 4060
 7661
 4003
 1417
 0313
 0504
 4003

6120 1624
6121 2200
6122 7777
6123 0071
6124 0052
6125 0000

6126 0024
6127 2324
6130 6364
6131 4017
6132 4706
6133 1417
6134 4006
6135 0111
6136 1405
6137 0440
6140 2417
6141 4023
6142 0524
6143 4017
6144 4706
6145 1417
6146 4006
6147 1417
6150 2000
6151 0000

/TST34 0'FLO FAILED TO SET 0'FLO FLOP

TST34M:

6152 0024
6153 2324
6154 6365
6155 4003
6156 1423
6157 0140
6160 0601
6161 1114
6162 0504
6163 4024
6164 1740
6165 0314
6166 0501
6167 2240
6170 4017
6171 4706
6172 1417
6173 4006
6174 1417
6175 2000
6176 0000

/TST35 CLSA FAILED TO CLEAR 0'FLO FLOP

TST35M:

6177 0024
6200 2324
6201 6366
6202 4003
6203 1423

/TST36 CLSK SKIPPED IN ERROR

TST36M:

6204 1340
6205 2313
6206 1120
6207 2005
6210 0440
6211 1116
6212 4005
6213 2222
6214 1722
6215 4000
6216 0000
EXIT

/TST37 ILLEGAL CLOCK INTERRUPT!

TST37M: 0024
6217 0024
6220 2324
6221 6367
6222 4011
6223 1414
6224 0507
6225 0114
6226 4003
6227 1417
6230 0313
6231 4011
6232 1624
6233 0522
6234 2225
6235 2024
6236 4100
6237 0000
EXIT

/TST38 CLSK FAILED TO SKIP

TST38M: 0024
6240 0024
6241 2324
6242 6370
6243 4003
6244 1423
6245 1340
6246 0601
6247 1114
6250 0504
6251 4024
6252 1740
6253 2313
6254 1120
6255 4000
6256 0000
EXIT

/TST39 CLOCK INTERRUPT FAILED

TST39M: 0024
6257 0024
6260 2324
6261 6371
6262 4003
6263 1417
6264 0313
6265 4011
6266 1624
6267 0522

6270 2225
 6271 2024
 6272 4006
 6273 0111
 6274 1405
 6275 0400
 6276 0000
 EXIT

TST40M: 0024
 6277 0024
 6300 2324
 6301 6460
 6302 4017
 6303 4706
 6304 1417
 6305 4005
 6306 1601
 6307 0214
 6310 0540
 6311 2717
 6312 1647
 6313 2440
 6314 3205
 6315 2217
 6316 4000
 6317 0000
 EXIT

/TST40 0'FLO ENABLE MONIT ZERO

TST41M: 0024
 6320 0024
 6321 2324
 6322 6461
 6323 4017
 6324 4706
 6325 1417
 6326 4006
 6327 1401
 6330 0740
 6331 2717
 6332 1647
 6333 2440
 6334 0314
 6335 0501
 6336 2200
 6337 0000
 EXIT

/TST41 0'FLO FLAG MONIT CLEAR

TST42M: 0024
 6340 0024
 6341 2324
 6342 6462
 6343 4003
 6344 1417
 6345 0313
 6346 4011
 6347 1624
 6350 2240
 6351 2717
 6352 1647
 6353 2440

/TST42 CLOCK INTR MONIT CLEAR

6354 0314
6355 0501
6356 2200
6357 0000
EXIT

/TST43 BIT 11 FAILED.

TST43M: 0024
6360 0024
6361 2324
6362 6463
6363 4002
6364 1124
6365 4061
6366 6140
6367 0601
6370 1114
6371 0504
6372 5600
6373 7777
6374 0053
6375 0052
6376 0000
EXITA
SEND
RXED
EXIT

/TST44 BIT 10 FAILED.

TST44M: 0024
6377 0024
6400 2324
6401 6464
6402 4002
6403 1124
6404 4061
6405 6040
6406 0601
6407 1114
6410 0504
6411 5600
6412 7777
6413 0053
6414 0052
6415 0000
EXITA
SEND
RXED
EXIT

/TST45 BIT 09 FAILED.

TST45M: 0024
6416 0024
6417 2324
6420 6465
6421 4002
6422 1124
6423 4060
6424 7140
6425 0601
6426 1114
6427 0504
6430 5600
6431 7777
6432 0053
6433 0052
6434 0000
EXITA
SEND
RXED
EXIT

/TST46 BIT 08 FAILED.

TST46M: 0024
6435 0024
6436 2324

6437 6466
6440 4002
6441 1124
6442 4060
6443 7040
6444 0601
6445 1114
6446 0504
6447 5600
6450 7777
6451 0053
6452 0052
6453 0000

6466
4002
1124
4060
7040
0601
1114
0504
5600
EXITA
SEND
RXED
EXIT

/TST47 BIT 07 FAILED.

TST47M: 0024
6454 0024
6455 2324
6456 6467
6457 4002
6460 1124
6461 4060
6462 6740
6463 0601
6464 1114
6465 0504
6466 5600
6467 7777
6470 0053
6471 0052
6472 0000

TST47M: 0024
2324
6467
4002
1124
4060
6740
0601
1114
0504
5600
EXITA
SEND
RXED
EXIT

/TST48 BIT 06 FAILED.

TST48M: 0024
6473 0024
6474 2324
6475 6470
6476 4002
6477 1124
6500 4060
6501 6640
6502 0601
6503 1114
6504 0504
6505 5600
6506 7777
6507 0053
6510 0052
6511 0000

TST48M: 0024
2324
6470
4002
1124
4060
6640
0601
1114
0504
5600
EXITA
SEND
RXED
EXIT

/TST49 BIT 05 FAILED.

TST49M: 0024
6512 0024
6513 2324
6514 6471
6515 4002
6516 1124
6517 4060
6520 6540
6521 0601
6522 1114

TST49M: 0024
2324
6471
4002
1124
4060
6540
0601
1114

6523 0504
6524 5600
6525 7777
6526 0053
6527 0052
6530 0000

6531 0024
6532 2324
6533 6560
6534 4002
6535 1124
6536 4060
6537 6440
6540 0601
6541 1114
6542 0504
6543 5600
6544 7777
6545 0053
6546 0052
6547 0000

/TST50 BIT 04 FAILED.

6550 0024
6551 2324
6552 6561
6553 4002
6554 1124
6555 4060
6556 6340
6557 0601
6560 1114
6561 0504
6562 5600
6563 7777
6564 0053
6565 0052
6566 0000

/TST51 BIT 03 FAILED.

6567 0024
6570 2324
6571 6562
6572 4002
6573 1124
6574 4060
6575 6240
6576 0601
6577 1114
6600 0504
6601 5600
6602 7777
6603 0053
6604 0052
6605 0000

/TST52 BIT 02 FAILED.

/TST53 BIT 01 FAILED.

6606	0024	TST53M:	0024
6607	2324		2324
6610	6563		6563
6611	4002		4002
6612	1124		1124
6613	4060		4060
6614	6140		6140
6615	0601		0601
6616	1114		1114
6617	0504		0504
6620	5600		5600
6621	7777		EXITA
6622	0053		SEND
6623	0052		RXED
6624	0000		EXIT

/TST54 BIT 00 FAILED

6625	0024	TST54M:	0024
6626	2324		2324
6627	6564		6564
6630	4002		4002
6631	1124		1124
6632	4060		4060
6633	6040		6040
6634	0601		0601
6635	1114		1114
6636	0504		0504
6637	5600		5600
6640	7777		EXITA
6641	0053		SEND
6642	0052		RXED
6643	0000		EXIT

/TST55 RATE 400KC FAILS

6644	0024	TST55M:	0024
6645	2324		2324
6646	6565		6565
6647	4022		4022
6650	0124		0124
6651	0540		0540
6652	6460		6460
6653	6013		6013
6654	0340		0340
6655	0601		0601
6656	1114		1114
6657	2300		2300
6660	0000		EXIT

/TST56 RATE 100KC FAILS

6661	0024	TST56M:	0024
6662	2324		2324
6663	6566		6566
6664	4022		4022
6665	0124		0124
6666	0540		0540
6667	6160		6160
6670	6013		6013
6671	0340		0340

6672 0024
6673 1114
6674 2324
6675 0000
EXIT

/TST57 RATE 10KC FAILS

TST57M: 0024
2324
6567
4022
0124
0540
6160
1303
4006
0111
1423
4000
EXIT

/TST58 RATE 1KC FAILS

TST58M: 0024
2324
6570
4022
0124
0540
6113
0340
0601
1114
2300
EXIT

/TST59 RATE 100CPS FAILS

TST59M: 0024
2324
6570
4022
0124
0540
6160
6003
2023
4006
0111
1423
4000
EXIT

/TST60 CHAN 1 INPUT LOCKED OUT

TST60M: 0024
2324
6660
0003
1001
1640
6140
1116

6676 0024
6677 2324
6700 6567
6701 4022
6702 0124
6703 0540
6704 6160
6705 1303
6706 4006
6707 0111
6710 1423
6711 4000
6712 0000

6713 0024
6714 2324
6715 6570
6716 4022
6717 0124
6720 0540
6721 6113
6722 0340
6723 0601
6724 1114
6725 2300
6726 0000

6727 0024
6730 2324
6731 6570
6732 4022
6733 0124
6734 0540
6735 6160
6736 6003
6737 2023
6740 4006
6741 0111
6742 1423
6743 4000
6744 0000

6745 0024
6746 2324
6747 6660
6750 0003
6751 1001
6752 1640
6753 6140
6754 1116

6755 2025
6756 2440
6757 1417
6760 0313
6761 0504
6762 4017
6763 2524
6764 4000
6765 0000
EXIT

TST61M: 0024 /TST61 CHAN 3 MON'Y TOGGLE

6766 0024
6767 2324
6770 6661
6771 4003
6772 1001
6773 1640
6774 6340
6775 2717
6776 1647
6777 2440
7000 2417
7001 0707
7002 1405
7003 4000
7004 7777
7005 0053
7006 0052
7007 0000
EXIT

TST62M: 0024 /TST62 CHAN 2 MON'Y TOGGLE

7010 0024
7011 2324
7012 6662
7013 4003
7014 1001
7015 1640
7016 6240
7017 2717
7020 1647
7021 2440
7022 2417
7023 0707
7024 1405
7025 4000
7026 7777
7027 0053
7030 0052
7031 0000
EXIT

TST63M: 0024 /TST63 CHAN 1 MON'Y TOGGLE

7032 0024
7033 2324
7034 6663
7035 4003
7036 1001
7037 1640
7040 6140

7041	2717	2717
7042	1647	1647
7043	2440	2440
7044	2417	2417
7045	0707	0707
7046	1405	1405
7047	4000	4000
7050	7777	EXITA
7051	0053	SEND
7052	0052	RXED
7053	0000	EXIT

/TST64 CHAN 1 MONIT INTR

TST64M:	0024	0024
7054	0024	2324
7055	2324	6664
7056	6664	4003
7057	4003	1001
7060	1001	1640
7061	1640	4061
7062	4061	4027
7063	4027	1716
7064	1716	4724
7065	4724	4011
7066	4011	1624
7067	1624	2200
7070	2200	EXIT
7071	0000	

/TST65 CHAN 3 INTR IN ERROR

TST65M:	0024	0024
7072	0024	2324
7073	2324	6665
7074	6665	4003
7075	4003	1001
7076	1001	1640
7077	1640	4061
7100	4061	4011
7101	4011	1624
7102	1624	2240
7103	2240	1116
7104	1116	4005
7105	4005	2222
7106	2222	1722
7107	1722	4000
7110	4000	EXIT
7111	0000	

/TST66 CHAN 2 MONIT INTR.

TST66M:	0024	0024
7112	0024	2324
7113	2324	6666
7114	6666	4003
7115	4003	1001
7116	1001	1640
7117	1640	6240
7120	6240	2717
7121	2717	1647
7122	1647	2440
7123	2440	1116
7124	1116	

7125 2422
7126 5600
7127 7777
7130 0053
7131 0052
7132 0000

7133 0024
7134 2324
7135 6667
7136 4003
7137 1001
7140 1640
7141 6240
7142 1116
7143 2422
7144 4011
7145 1640
7146 0522
7147 2217
7150 2200
7151 0000

/TST67 CHAN 2 INTR IN ERROR

7152 0024
7153 2324
7154 6670
7155 4003
7156 1001
7157 1640
7160 6340
7161 2717
7162 1647
7163 2440
7164 1116
7165 2422
7166 5600
7167 7777
7170 0053
7171 0052
7172 0000

/TST68 CHAN 3 MONIT INTR:

7173 0024
7174 2324
7175 6671
7176 4003
7177 1001
7200 1640
7201 6340
7202 1116
7203 2422
7204 4011
7205 1640
7206 0522
7207 2217
7210 2200

/TST69 CHAN 3 INTR IN ERROR

2422
5600
EXITA
SEND
RXED
EXIT

TST67M: 0024
2324
6667
4003
1001
1640
6240
1116
2422
4011
1640
0522
2217
2200
EXIT

TST68M: 0024
2324
6670
4003
1001
1640
6340
2717
1647
2440
1116
2422
5600
EXITA
SEND
RXED
EXIT

TST69M: 0024
2324
6671
4003
1001
1640
6340
1116
2422
4011
1640
0522
2217
2200

7211 0020
 7212 0024
 7213 2324
 7214 6760
 7215 4003
 7216 1001
 7217 1640
 7220 6340
 7221 1116
 7222 2025
 7223 2440
 7224 1411
 7225 1605
 7226 4006
 7227 2205
 7230 2140
 7231 0601
 7232 1114
 7233 0504
 7234 4000
 7235 7777
 7236 0052
 7237 0000

EXIT
 TST72M, 0024
 2324
 6760
 4003
 1001
 1640
 6340
 1116
 2025
 2440
 1411
 1605
 4006
 2205
 2140
 0601
 1114
 0504
 4000
 EXITA
 RXED
 EXIT

/TST70 CHAN 3 INPUT LINE FREQ FAILED

7240 0024
 7241 2324
 7242 6761
 7243 4003
 7244 1001
 7245 1640
 7246 6240
 7247 1116
 7250 2025
 7251 2440
 7252 1411
 7253 1605
 7254 4006
 7255 2205
 7256 2140
 7257 0601
 7260 1114
 7261 0504
 7262 4000
 7263 7777
 7264 0052
 7265 0000

EXIT
 TST71M, 0024
 2324
 6761
 4003
 1001
 1640
 6240
 1116
 2025
 2440
 1411
 1605
 4006
 2205
 2140
 0601
 1114
 0504
 4000
 EXITA
 RXED
 EXIT

/TST71 CHAN 2 INPUT LINE FREQ FAILED

7266 0024
 7267 2324
 7270 6762
 7271 4003
 7272 1001
 7273 1640
 7274 6140

EXIT
 TST72M, 0024
 2324
 6762
 4003
 1001
 1640
 6140

/TST72 CHAN 1 INPUT LINE FREQ FAILED

7275	1116	1116
7276	2025	2025
7277	2440	2440
7300	1411	1411
7301	1605	1605
7302	4006	4006
7303	2205	2205
7304	2140	2140
7305	0601	0601
7306	1114	1114
7307	0504	0504
7310	4000	4000
7311	7777	EXITA
7312	0052	RXED
7313	0000	EXIT

/TST73 FAST SAM FAILS

7314	0024	TST73M; 0024
7315	2324	2324
7316	6763	6763
7317	4006	4006
7320	0123	0123
7321	2440	2440
7322	2301	2301
7323	1540	1540
7324	0601	0601
7325	1114	1114
7326	2300	2300
7327	7777	EXITA
7330	0053	SEND
7331	0052	RXED
7332	0000	EXIT

/TST74 0'FLO MON'IT FAST SAM

7333	0024	TST74M; 0024
7334	2324	2324
7335	6764	6764
7336	4017	4017
7337	4706	4706
7340	1417	1417
7341	4027	4027
7342	1716	1716
7343	4724	4724
7344	4006	4006
7345	0123	0123
7346	2440	2440
7347	2301	2301
7350	1500	1500
7351	7777	EXITA
7352	0053	SEND
7353	0052	RXED
7354	0000	EXIT

/TST75 FAST SAM MON'IT SET

7355	0024	TST75M; 0024
7356	2324	2324
7357	6765	6765
7360	4006	4006

7361	0123
7362	2440
7363	2301
7364	1540
7365	2717
7366	1647
7367	2440
7370	2305
7371	2400
7372	EXITA
7373	SEND
7374	RXED
7375	EXIT

/TST76 MODES 2+1 INHIBIT FAST SAM

7376	0024	TST76M:	0024
7377	2324		2324
7400	6766		6766
7401	4015		4015
7402	1704		1704
7403	0523		0523
7404	4062		4062
7405	5561		5561
7406	4011		4011
7407	1610		1610
7410	1102		1102
7411	1124		1124
7412	4006		4006
7413	0123		0123
7414	2440		2440
7415	2301		2301
7416	1500		1500
7417	7777		EXITA
7420	0053		SEND
7421	0052		RXED
7422	0000		EXIT

/TST78 I/O PRESET MONIT STOP CLOCK / (RATE BITS 1 & 2)

7423	0024	TST77M:	0024
7424	2324		2324
7425	6770		6770
7426	4011		4011
7427	3417		3417
7430	4020		4020
7431	2205		2205
7432	2305		2305
7433	2440		2440
7434	2717		2717
7435	1647		1647
7436	2440		2440
7437	2324		2324
7440	1720		1720
7441	4003		4003
7442	1417		1417
7443	0313		0313
7444	4000		4000
7445	5022		5022

7446 0124
 7447 0540
 7450 0211
 7451 2423
 7452 4061
 7453 4046
 7454 4062
 7455 5100
 7456 0000

TST79M: 0024
 7457 0024
 7460 2324
 7461 7060
 7462 4011
 7463 3417
 7464 4020
 7465 2205
 7466 2305
 7467 2440
 7470 2717
 7471 1647
 7472 2440
 7473 2324
 7474 1720
 7475 4003
 7476 1417
 7477 0313
 7500 4000
 7501 5022
 7502 0124
 7503 0540
 7504 0211
 7505 2440
 7506 6051
 7507 4000
 7510 0000

/TST80 I/O PRESET MON'Y STOP CLOCK
 / (RATE BIT 00)

TST81M: 0024
 7511 0024
 7512 2324
 7513 7061
 7514 4011
 7515 3417
 7516 4020
 7517 2205
 7520 2305
 7521 2440
 7522 2717
 7523 1647
 7524 2440
 7525 0314
 7526 0501
 7527 2240
 7530 1747
 7531 0614
 7532 1700

/TST81 I/O PRESET MON'Y CLEAR O'FLO

```

7533 0000          EXIT
7534 0024          TST82M, 0024
7535 2324          2324
7536 7062          7062
7537 4011          4011
7540 3417          3417
7541 4020          4020
7542 2205          2205
7543 2305          2305
7544 2440          2440
7545 2717          2717
7546 1647          1647
7547 2440          2440
7550 0314          0314
7551 0501          0501
7552 2240          2240
7553 1116          1116
7554 2405          2405
7555 2222          2222
7556 2520          2520
7557 2440          2440
7560 0516          0516
7561 0102          0102
7562 1405          1405
7563 4000          4000
7564 0000          EXIT

```

/TST82 I/O PRESET MONIT CLEAR INTERRUPT ENABLE

/FOLD TEXT BACK INTO FREE CORE AREA

/TST83 I/O PRESET MONIT CLEAR INPUTS

```

4310          #LOCJ*1
4311 0024          TST83M, 0024
4312 2324          2324
4313 7063          7063
4314 4011          4011
4315 3417          3417
4316 4020          4020
4317 2205          2205
4320 2440          2440
4321 2717          2717
4322 1647          1647
4323 2440          2440
4324 0314          0314
4325 0501          0501
4326 2240          2240
4327 1116          1116
4330 2025          2025
4331 2423          2423
4332 4000          4000
4333 0000          EXIT

4334 0024          TST84M, 0024
4335 2324          2324
4336 7064          7064

```

/TST84 I/O PRESET MONIT CLEAR MODE 2

4337	4011	4011
4340	3417	3417
4341	4020	4020
4342	2205	2205
4343	2305	2305
4344	2440	2440
4345	2717	2717
4346	1647	1647
4347	2440	2440
4350	0314	0314
4351	0501	0501
4352	2240	2240
4353	1517	1517
4354	0405	0405
4355	4062	4062
4356	4000	4000
4357	0000	EXIT

/TST85 I/O PRESET WON'T CLEAR MODE 0

4360	0024	TST85M: 0024
4361	2324	2324
4362	7065	7065
4363	4011	4011
4364	3417	3417
4365	4020	4020
4366	2205	2205
4367	2305	2305
4370	2440	2440
4371	2717	2717
4372	1647	1647
4373	2440	2440
4374	0314	0314
4375	0501	0501
4376	2240	2240
4377	1517	1517
4400	0405	0405
4401	4060	4060
4402	4000	4000
4403	7777	EXITA
4404	0000	EXIT

/TST86 FAST SAM NOT CLEARED

4405	0024	TST86M: 0024
4406	2324	2324
4407	7066	7066
4410	4006	4006
4411	0123	0123
4412	2440	2440
4413	2301	2301
4414	1540	1540
4415	1617	1617
4416	2440	2440
4417	0314	0314
4420	0501	0501
4421	2205	2205
4422	0400	0400
4423	7777	EXITA

4424 0000 EXIT
 TST87M: 0024
 4425 0024
 4426 2324
 4427 7067
 4430 4003
 4431 1001
 4432 1640
 4433 6140
 4434 2717
 4435 1647
 4436 2440
 4437 2422
 4440 0116
 4441 2340
 4442 0316
 4443 2440
 4444 2417
 4445 4002
 4446 2506
 4447 4000
 4450 7777
 4451 0111
 4452 0000
 /TST87 CHAN 1 MONIT TRANS CNT TO BUF

TST88M: 0024
 4453 0024
 4454 2324
 4455 7070
 4456 4003
 4457 1001
 4460 1640
 4461 6240
 4462 2717
 4463 1647
 4464 2440
 4465 2422
 4466 0116
 4467 2340
 4470 0316
 4471 2440
 4472 2417
 4473 4002
 4474 2506
 4475 4000
 4476 7777
 4477 0111
 4500 0000
 /TST88 CHAN 2 MONIT TRANS CNT TO BUF

TST89M: 0024
 4501 0024
 4502 2324
 4503 7071
 4504 4003
 4505 1001
 4506 1640
 4507 6340
 /TST89 CHAN 3 MONIT TRANS CNT TO BUF

4510	2717	2717
4511	1647	1647
4512	2440	2440
4513	2422	2422
4514	0116	0116
4515	2340	2340
4516	0316	0316
4517	2440	2440
4520	2417	2417
4521	4002	4002
4522	2506	2506
4523	4000	4000
4524	7777	EXITA
4525	0111	K0200
4526	0000	EXIT

/TST90 CHAN 1 MONIT TRANS CNT TO BUF

4527	0024	TST90M: 0024
4530	2324	2324
4531	7160	7160
4532	4003	4003
4533	1001	1001
4534	1640	1640
4535	6140	6140
4536	2717	2717
4537	1647	1647
4540	2440	2440
4541	2422	2422
4542	0116	0116
4543	2340	2340
4544	0316	0316
4545	2440	2440
4546	2417	2417
4547	4002	4002
4550	2506	2506
4551	4000	4000
4552	7777	EXITA
4553	0113	K0300
4554	0000	EXIT

/TST91 CHAN 2 MONIT TRANS CNT TO BUF

4555	0024	TST91M: 0024
4556	2324	2324
4557	7161	7161
4560	4003	4003
4561	1001	1001
4562	1640	1640
4563	6240	6240
4564	2717	2717
4565	1647	1647
4566	2440	2440
4567	2422	2422
4570	0116	0116
4571	2340	2340
4572	0316	0316
4573	2440	2440
4574	2417	2417

4575 4002
 4576 2506
 4577 4000
 4600 7777
 4601 0113
 4602 0000

/TST92 CHAN 3 MONIT TRANS CNT TO BUF

TST92M: 0024
 4603 0024
 4604 2324
 4605 7162
 4606 4003
 4607 1001
 4610 1640
 4611 6340
 4612 2717
 4613 1647
 4614 2440
 4615 2422
 4616 0116
 4617 2340
 4620 0316
 4621 2440
 4622 2417
 4623 4002
 4624 2506
 4625 4000
 4626 7777
 4627 0113
 4630 0000

4802
 2506
 4000
 EXITA
 K0300
 EXIT

/TST93 CHAN 3 INPUT FAILED TO CLR CNT

TST93M: 0024
 4631 0024
 4632 2324
 4633 7163
 4634 4003
 4635 1001
 4636 1640
 4637 6340
 4640 1116
 4641 2025
 4642 2440
 4643 0601
 4644 1114
 4645 0504
 4646 4024
 4647 1740
 4650 0314
 4651 2240
 4652 0316
 4653 2400
 4654 7777
 4655 0052
 4656 0000

0024
 2324
 7163
 4003
 1001
 1640
 6340
 1116
 2025
 2440
 0601
 1114
 0504
 4024
 1740
 0314
 2240
 0316
 2400
 EXITA
 RXED
 EXIT

/TST94 ECO EM12=00034 IS EITHER NOT WORKING OR NOT INSTALLED

TST94M: 0024
 4657 0024
 4660 2324

4661	7164	7164
4662	4005	4005
4663	0317	0317
4664	4005	4005
4665	1561	1561
4666	6255	6255
4667	6060	6060
4670	6063	6063
4671	6440	6440
4672	1123	1123
4673	4005	4005
4674	1124	1124
4675	1005	1005
4676	2240	2240
4677	1617	1617
4700	2440	2440
4701	2717	2717
4702	2213	2213
4703	1116	1116
4704	0740	0740
4705	1722	1722
4706	4016	4016
4707	1724	1724
4710	4011	4011
4711	1623	1623
4712	2401	2401
4713	1414	1414
4714	0504	0504
4715	0000	EXIT

/TST95 ECO EM12-00055 IS EITHER NOT WORKING OR IS NOT INSTALLED

4716	0024	TST95M, 0024
4717	2324	2324
4720	7165	7165
4721	4005	4005
4722	0317	0317
4723	4005	4005
4724	1561	1561
4725	6255	6255
4726	6060	6060
4727	6065	6065
4730	6540	6540
4731	1123	1123
4732	4005	4005
4733	1124	1124
4734	1005	1005
4735	2240	2240
4736	1617	1617
4737	2440	2440
4740	2717	2717
4741	2213	2213
4742	1116	1116
4743	0740	0740
4744	1722	1722
4745	4016	4016
4746	1724	1724

4747 4011
 4750 1623
 4751 2401
 4752 1414
 4753 0504
 4754 0000
 4755 0013
 4756 2761
 4757 6240
 4760 2001
 4761 2323
 4762 9555
 4763 7777
 4764 0031
 4765 4444

TST96M; 0013
 2761
 6240
 2001
 2323
 5555
 EXITA
 PASS
 EXITB
 \$

/KW12 PASS--(PASS)

/EXIT B CAUSES A RETURN TO 0176

ASCII	5051	K0215	5174	NERROR	0027	TST18	0466
ASCRXT	5026	K0300	0113	NERROS	5000	TST19M	5455
BELL	0021	K0377	0114	OCTYP	5133	TST19	0550
BELLS	5200	K0400	0115	OUTPAS	0030	TST19M	5476
BK43	1561	K0500	0116	PASS	0031	TST20	0566
BK47	1764	K0600	0117	POP	0002	TST20M	5516
BK55	2362	K0700	0120	PINT	0010	TST21	0616
CLAB	6133	K0777	0121	PNTA	0032	TST21M	5540
CLAR	0157	K1000	0122	PNTB	0033	TST22	0643
CLBA	6136	K1026	0123	PNTC	0034	TST22M	5556
CLCA	6137	K1777	0124	PNTD	0035	TST23	0672
CLEAR	4157	K2000	0125	PNTE	0036	TST23M	5576
CLEN	6134	K240	0112	PNTF	0037	TST24	0721
CLLR	6132	K3000	0126	PNTG	0040	TST24M	5614
CLR	0011	K3777	0127	PNTH	0041	TST25	0753
CLSA	6135	K4000	0130	PNTI	0042	TST25M	5632
CLSK	6131	K4100	0131	PNTJ	0043	TST26	1012
CNTR	0024	K5100	0132	RANDOM	0044	TST26M	5653
CRLF	5154	K5252	0133	RANDY	5210	TST27	1043
DATUM	5115	K5555	0134	REGA	5140	TST27M	5676
DATYP	5163	K6000	0135	REGB	0045	TST28	1077
DN43	0022	K7300	4214	REGC	0046	TST28M	5722
DN55	0023	K7774	0136	REGD	0047	TST29	1131
ERROR	0028	LDAI	1020	REGT	0050	TST29M	5747
ERRORS	5020	LINC	6141	RESE	3700	TST30	1156
ESF	0004	LOCA	1425	RETURN	0051	TST30M	5774
EXIT	0000	LOCB	1457	RNA	5240	TST31	1205
EXITA	7777	LOCC	1527	RNB	5241	TST31M	6021
EXITB	4444	LOCD	2720	RNC	5242	TST32	1245
FD43	1572	LOCE	2742	RXD	0052	TST32M	6056
FD51	2201	LOCF	2763	SAM0	0100	TST33	1276
FD55	2372	LOGG	3005	SAM1	0101	TST33M	6102
FD61	2617	LOCH	3027	SEND	0053	TST34	1316
HERE	5137	LOCI	3051	SET	0054	TST34M	6126
K0000	0071	LOCJ	4307	SETN	5252	TST35	1344
K0001	0072	LSTERR	0026	SPACE	0055	TST35M	6152
K0002	0073	M0001	0137	TST10	0201	TST35N	0056
K0003	0074	M0002	0140	TST10M	5261	TST36	1373
K0004	0075	M0004	0141	TST11	0217	TST36M	6177
K0007	0076	M0010	0142	TST11M	5301	TST37	1417
K0010	0077	M0020	0143	TST12	0235	TST37M	6217
K0014	0100	M0040	0144	TST12M	5317	TST38	1434
K0017	0101	M0042	0145	TST13	0254	TST38M	6240
K0020	0102	M0100	0146	TST13M	5335	TST39	1451
K0037	0103	M0200	0147	TST14	0274	TST39M	6257
K0040	0104	M0400	0150	TST14M	5353	TST40	1467
K0060	0105	M1000	0151	TST15	0315	TST40M	6277
K0077	0106	M1400	0152	TST15M	5371	TST41	1502
K0100	0107	M2000	0153	TST16	0340	TST41M	6320
K0177	0110	M4000	0154	TST16M	5413	TST42	1521
K0200	0111	M4444	0155	TST17	0403	TST42M	6340
K0212	5175	M5400	0156	TST17M	5434	TST43	1542

TST43M	6360	TST68M	7152
TST44	1602	TST69	3837
TST44M	6377	TST69M	7173
TST45	1642	TST70	3864
TST45M	6416	TST70M	7212
TST46	1703	TST71	3116
TST46M	6435	TST71M	7240
TST47	1744	TST72	3190
TST47M	6454	TST72M	7266
TST48	2005	TST73	3202
TST48M	6473	TST73M	7314
TST49	2046	TST74	3252
TST49M	6512	TST74M	7333
TST50	2107	TST75	3313
TST50M	6531	TST75M	7355
TST51	2150	TST75M	0060
TST51M	6550	TST76	3351
TST52	2211	TST76M	7376
TST52M	6567	TST77	3375
TST53	2252	TST77M	7423
TST53M	6606	TST77N	0061
TST54	2313	TST79	3436
TST54M	6625	TST79M	7457
TST55	2354	TST79N	0062
TST55M	6644	TST81	3474
TST56	2401	TST81M	7511
TST56M	6661	TST82	3520
TST57	2426	TST82M	7534
TST57M	6676	TST83	3544
TST58	2460	TST83M	4310
TST58M	6713	TST84	3567
TST59	2507	TST84M	4334
TST59M	6727	TST85	3613
TST60	2546	TST85M	4360
TST60M	6745	TST86	3660
TST60N	2554	TST86M	4405
TST61	2573	TST87	3703
TST61M	6766	TST87M	4425
TST62	2624	TST88	3752
TST62M	7010	TST88M	4453
TST63	2655	TST89	4004
TST63M	7032	TST89M	4501
TST64	2710	TST90	4040
TST64M	7054	TST90M	4527
TST65	2730	TST90N	0063
TST65M	7072	TST91	4102
TST66	2753	TST91M	4555
TST66M	7112	TST92	4135
TST66N	0057	TST92M	4603
TST67	2773	TST93	4170
TST67M	7133	TST93M	4631
TST68	3016	TST94	4210

TST94M	4657
TST95	4243
TST95M	4716
TST95N	4257
TST96	4276
TST96M	4755
TYPE	0064
TYPECH	5100
TYPQUT	5243
UP43	0065
UP51	0066
UP55	0067
UP61	0070

7 2 7
/PDP-12 KW12A CLOCK TEST; MAINDEC 12-08CD=L PAL10 V141 3-DEC-71 16133 PAGE 77-34

ERRORS DETECTED 0

LINKS GENERATED 0

RUN-TIME 43 SECONDS

3K CORE USED


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0000 *20
0001 /
0002 / KW12A1
0003 / 18 JULY 1977
0004 / 18 JULY 1977
0005 /
0006 /
0007 /
0010 / SUPPLEMENT TO THE KW12A DIAGNOSTIC PROGRAM.
0011 / CHECKS WHETHER, IN MODE 011, EVENT 2 ZERO'S THE
0012 / CLOCK COUNTER AS WELL AS TRANSFERRING ITS CON-
0013 / TS TO THE CLOCK BUFFER.
0014 /
0015 / ASSUMES KW12A HAS RUN SUCCESSFULLY.
0016 /
0017 / DISCONNECT ALL INPUT LINES, AND DESELECT
0020 / "LINE FREQ" FROM ALL THREE SOURCES.
0021 / START 8MODE, 0020.
0022 /
0023 /
0024 / PMODE
0025 / *0020
0026 /
0027 / RATE AND MODE:
0030 / RATE 110 (COUNT INPUT 1 EVENTS)
0031 / MODE 011 (ANY EVENT TRANSFERS COUNTER TO BUFFER,
0032 / & EVENT 3 ZERO'S COUNTER)
0033 /
0033 0020 7200 CLA
0034 0021 1117 TAD K0025
0035 0022 6134 CLEN /ENABLE ALL 3 INPUTS
0036 0023 7200 CLA
0037 0024 1120 AGAIN, TAD K6300
0040 0025 6132 CLLR
0041 0026 7001 IAC
0042 0027 6132 CLLR /INPUT 3
0043 0030 6135 CLSA /REENABLE INPUTS
0044 0031 7200 CLA
0045 0032 1121 TAD K6301
0046 0033 6132 CLLR /AGAIN
0047 0034 6136 CLBA /BUFFER TO AC
0050 0035 7440 SZA /DID IT ZERO COUNTER?
0051 0036 7402 HLT /IT SHOULD HAVE.
0052 0037 1123 TAD K6320
0053 0040 6132 CLLR /INPUT 1
0054 0041 6132 CLLR /AGAIN
0055 0042 6137 CLCA /COUNTER TO AC
0056 0043 1124 TAD KM2
0057 0044 7440 SZA /WAS IT 2?
0060 0045 7402 HLT /IT SHOULD HAVE BEEN.
0061 0046 6133 CLAB /CLEAR BUFFER PRESET REG.
0062 0047 6135 CLSA /REENABLE INPUTS
0063 0050 7200 CLA
0064 0051 1121 TAD K6301
0065 0052 6132 CLLR /INPUT 3
0066 0053 6136 CLBA
0067 0054 1124 TAD KM2
0070 0055 7440 SZA /DID THE COUNTER GO TO THE
0071 / BUFFER BEFORE IT ZEROED?
0072 0056 7402 HLT /NO; IT SHOULD HAVE.
0073 0057 6137 CLCA
0074 0060 7440 SZA /DIT IT THEN ZERO?
0075 0061 7402 HLT /NO; IT SHOULD HAVE

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0076	0062	1123	TAD K6320	
0077	0063	6132	CLLR	/INPUT 1
0100	0064	6132	CLLR	/AGAIN
0101	0065	6132	CLLR	/AND AGAIN
0102	0066	6137	CLCA	
0103	0067	7450	SNA	/IS THERE SOMETHING THERE?
0104	0070	7402	HLT	/NO; THERE SHOULD BE.
0105	0071	3116	DCA BUF	/YES; KEEP IT
0106	0072	1122	TAD K6304	
0107	0073	6132	CLLR	/INPUT 2
0110	0074	6136	CLBA	
0111	0075	7041	CIA	
0112	0076	1116	TAD BUF	
0113	0077	7440	SZA	/IS THE SAME THING THERE?
0114	0100	7402	HLT	/NO
0115	0101	6135	CLSA	
0116	0102	7200	CLA	
0117	0103	6133	CLAB	/CLEAR THE BUFFER
0120	0104	1122	TAD K6304	/INPUT 2
0121	0105	6132	CLLR	
0122	0106	6136	CLBA	
0123	0107	7041	CIA	
0124	0110	1116	TAD BUF	
0125	0111	7440	SZA	/STILL THERE?
0126	0112	7402	HLT	/OH-OH! INPUT 2 MUST DO
0127				/SOMETHING TO THE COUNTER!
0130	0113	6135	CLSA	
0131	0114	7200	CLA	
0132	0115	5024	JMP AGAIN	
0133			/	
0134	0116	0000	BUF, 0	
0135	0117	0025	K0025, 0025	
0136	0120	6300	K6300, 6300	
0137	0121	6301	K6301, 6301	
0140	0122	6304	K6304, 6304	
0141	0123	6320	K6320, 6320	
0142	0124	7776	KM2, -2	

NO ERRORS

AGAIN	0024
BUF	0116
KM2	0124
K0025	0117
K6300	0120
K6301	0121
K6304	0122
K6320	0123