

1976

pdp11 peripherals handbook



digital

pdp-11

**peripherals
handbook**

digital equipment corporation

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CHAPTER 1

INTRODUCTION

1.1 SCOPE AND CONTENTS

This Handbook is a reference guide describing PDP-11 equipment other than central processors. It includes descriptions, specifications, programming and interfacing information on PDP-11 peripherals and options. The information in the Handbook supplements material found in the various PDP-11 Processor Handbooks. Familiarity with or access to a Processor Handbook will greatly facilitate an understanding of the material in this Handbook.

The intent of this Handbook is to provide extensive information on operation of PDP-11 peripheral equipment. It is not intended to be the sole reference for the peripherals. More comprehensive and detailed information is available in Peripherals Manuals, Maintenance Manuals, and Programming Manuals. Improvements and modifications in equipment made after March 1976 are not reflected in this Handbook.

1.2 PERIPHERAL EQUIPMENT

Digital Equipment Corporation designs and manufactures many of the peripheral devices described in this Handbook. The general design criteria was to provide maximum system throughput for peripherals when matched to a PDP-11 central processor—the processors and the peripherals were designed to work together. In addition to providing individual peripheral performance the overall goal is to provide a broad spectrum of compatible peripheral devices. This broad spectrum of peripherals and processors means the user can start with any system and be sure of easy compatible upgrades as needs increase. This ability when coupled with DIGITAL software and support allows going to one source for all data processing needs.

1.3 PDP-11 EQUIPMENT PHILOSOPHY

The PDP-11 family is a comprehensive set of hardware/software facilities that includes various central processors, a large number of peripheral devices and options, and extensive software. Products are compatible with each other. Thus, the user can choose the system which is most suitable to present applications and be sure that as needs change or grow, equipment can easily be changed or added. Some of the characteristics of PDP-11 equipment are:

- 16-bit word (two 8-bit bytes)
direct addressing of 32K 16-bit words or 64K 8-bit bytes ($K = 1024$)
- Word or byte processing
central processors are hardwired for word or byte instructions
- Asynchronous operation
systems run at their highest possible speed, replacement with faster devices means faster operation with no other hardware or software changes

- **Modular component design**
extreme ease and flexibility in configuring systems
- **Direct Memory Access (DMA)**
inherent in the architecture is direct memory access for multiple devices
- **Automatic Priority Interrupt**
four-line, multi-level system permits grouping of interrupt lines according to response requirements
- **Vectored interrupts**
fast interrupt response without device polling
- **Power Fail & Automatic Restart**
hardware detection and software protection for fluctuations in the AC power

1.4 CENTRAL PROCESSOR

The central processor, connected to the UNIBUS as a subsystem, controls the time allocation of the UNIBUS for peripherals and performs arithmetic and logic operations and instruction decoding. It contains multiple high-speed general-purpose registers which can be used as accumulators, address pointers, index registers, and other specialized functions. The processor can perform data transfers directly between input/output (I/O) devices and memory without disturbing the processor registers; does both single- and double-operand addressing and handles both 16-bit word and 8-bit byte data.

Instruction Set

The instruction complement uses the flexibility of the general-purpose registers to provide over 400 powerful hard-wired instructions. Unlike conventional 16-bit computers, which usually have three classes of instructions (memory reference instructions, operate or control instructions and I/O instructions) all operations in the PDP-11 are accomplished with one set of instructions. Since peripheral device registers can be manipulated as flexibly as core memory by the central processor, instructions that are used to manipulate data in core memory may be used equally well for data in peripheral device registers.

1.5 UNIBUS

Most computer system components and peripherals connect to and communicate with each other on a high-speed bus known as the UNIBUS, see Figure 1-1.

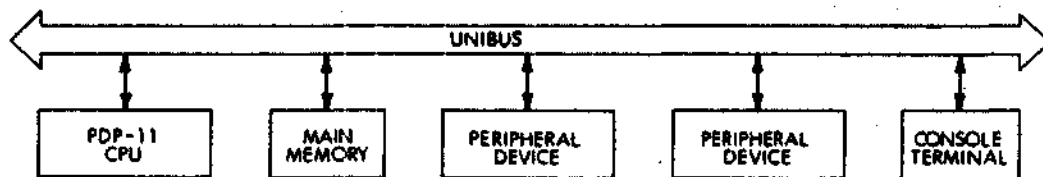


Figure 1-1 PDP-11 System Block Diagram

The form of communication is the same for every device on the UNIBUS. The central processing unit (CPU) uses the same set of signals to communicate with main memory as with peripheral devices. Peripheral devices also use this set of signals when communicating with the processor, memory or other peripheral devices. Each device, including memory locations, processor registers, and peripheral device registers, is assigned an address on the UNIBUS.

With bidirectional and asynchronous communications on the UNIBUS, devices can send, receive, and exchange data with minimum processor intervention. Because it is asynchronous, the UNIBUS is compatible with devices operating over a wide range of speeds. Interfaces to the UNIBUS are not time dependent; there are no pulse-width or rise-time restrictions.

Full 16-bit words or 8-bit bytes of information can be transferred on the bus. The information can be instructions, addresses, or data. Direct data transfers can occur between a peripheral device control and memory.

Refer to Chapter 5 for more detailed information about the UNIBUS and data transfers.

1.6 SOFTWARE

The PDP-11 family of central processors and peripherals is supported by a comprehensive family of licensed software products. This software family includes support for small stand-alone configurations, disk based real-time and program development systems, large multi-programming and time sharing systems, and many diverse dedicated applications. Some examples of general purpose operating systems and standard high level language processors are:

- **PAPER TAPE SYSTEM (PTS-11)**—A core only high-speed paper tape system with program development in assembly language. Editor, debugger, and linker are supplied along with a relocating assembler.
- **CASSETTE PROGRAMMING SYSTEM (CAPS-11)**—A small program development system with a core based monitor, utilizing dual magnetic tape cassettes as file structured media. Complete program development utilities such as a relocating assembler, linker, editor, debugger, and file interchange program are included.
- **SINGLE USER ON-LINE PROGRAM DEVELOPMENT SYSTEM (RT-11)**—A small, powerful, easy-to-use disk (or DECTape) based system for program development or fast on-line (real-time) applications. A Foreground/Background version can accommodate simultaneous program development in the background with on-line applications in the foreground. A MACRO assembler, linker, editor, debugger, and file utility programs are included.
- **REAL-TIME MEMORY-BASED SYSTEM (RXS-11S)**—A small, real-time operating system that provides a run-time environment for execution of tasks developed on an RSX-11M host system. RSX-11S is program compatible with both the RSX-11M and RSX-11D systems; any task that executes under RSX-11S will execute under the other two, more

powerful systems. RSX-11S is suitable for dedicated application environments.

- **MULTI-TASKING PROCESS CONTROL SYSTEM (RSX-11M)**—An efficient multi-tasking system suitable for controlling many processes simultaneously, in a protected environment with concurrent development of new programs. Utilities include a MACRO assembler, task builder (linker), editor, debugger, and file utility programs.
- **COMPREHENSIVE MULTI-PROGRAMMING SYSTEM (RSX-11D)**—The total job operating system. As a compatible extension of RSX-11M, the system allows concurrent fully hardware protected execution of multiple on-line jobs, with BATCH program development. Complete utilities include a MACRO assembler, task builder (linker), editor, debugger, and file utility programs.
- **EXTENDED RESOURCE TIME SHARING SYSTEM (RSTS/E)**—A disk-based time sharing system implementing BASIC-PLUS, an enriched version of the popular BASIC language. Up to 32 simultaneous users share system resource via interactive terminals. Additional features such as output spooling, and comprehensive file protection are included.
- **INTERACTIVE APPLICATION SYSTEM (IAS)**—A multi-function, multi-language operating system capable of supporting timesharing, real-time, and batch programming concurrently. It supports up to 16 interactive terminals and versions of BASIC, FORTRAN, COBOL, and MACRO assembler.
- **BASIC-11**—An extended version of Dartmouth Standard BASIC is available for PTS-11, CAPS-11 and RT-11. Many applications, such as signal processing and graphics are accessed by the user through extensions to this simple, yet powerful, language. A multiuser version is available under PTS-11 and RT-11.
- **PDP-11 FORTRAN IV**—An extended version of ANSI standard FORTRAN is supplied with RSX-11M and RSX-11D, and available under RT-11. As an optimizing compiler, FORTRAN IV is designed for fast compilation, yet requires very little main memory, and generates highly efficient code without sacrificing execution speed. Under RT-11, FORTRAN IV features the same signal-processing and graphics extensions as BASIC-11.
- **FORTRAN-IV PLUS**—A compatible extension to PDP-11 FORTRAN IV, this system uses sophisticated optimizations to achieve the fastest possible execution speed of the generated code. FORTRAN IV-PLUS requires a PDP-11/45 and Floating Point Processor hardware, in addition to the RSX-11D operating system.
- **PDP-11 COBOL**—To supplement the business data processing needs often associated with large scale PDP-11 system applications, an ANSI-74 COBOL language is available under RSX-11D. Running as a BATCH job, COBOL enhances the RSX-11D total job computing system, where some business data processing is required.

In addition to the above mentioned general purpose licensed software products, DIGITAL offers a great number of addition optional and ap-

plications oriented products. A wide range of educational, consulting, and maintenance services are also offered, to ensure full utility of any PDP-11 system. For a complete and detailed listing of DIGITAL software products and services, consult the latest CATALOG OF SOFTWARE PRODUCTS and SERVICES.

1.7 PDP-11 WORD

The 16-bit PDP-11 word can be represented conveniently as a 6-digit octal word. Bit 15, the Most Significant Bit (MSB), is used directly as the Most Significant Digit of the octal word. The other 5 octal digits are formed from the corresponding groups of 3 bits in the binary word. See Figure 1-2.

Octal Representation

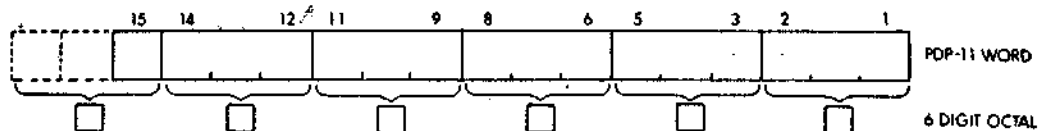


Figure 1-2

When an extended address of 18 bits is used (shown later in the Handbook), the Most Significant Digit of the octal word is formed from bits 17, 16, and 15. For unsigned numbers, the correspondence between decimal and octal is:

Decimal	Octal	
0	000 000	
$(2^{16} - 1) = 65,535$	177 777	(16-bit limit)
$(2^{18} - 1) = 262,143$	777 777	(18-bit limit)

CHAPTER 2

PROGRAMMING

2.1 GENERAL

Programming of peripherals is extremely simple in the PDP-11; a special class of instruction to deal with input/output operations is unnecessary. The UNIBUS permits a unified addressing structure in which control, status, and data registers for peripheral devices are directly addressed as memory locations. Therefore all operations on these registers, such as transferring information into or out of them or manipulating data within them, are performed by normal memory reference instructions.

The use of all memory reference instructions on peripheral device registers greatly increases the flexibility of input/output programming. For example, information in a device register can be compared directly with a value and a branch made on the result.

All peripheral device registers can be treated as accumulators. There is no need to funnel all data transfers, arithmetic operations, and comparisons through a single or small number of accumulator registers.

2.2 ADDRESSES

Words and Bytes

Since the PDP-11 can operate on individual 8-bit bytes, a 16-bit word allows addressing 65,536 bytes ($2^{16} = 65,536$). It is common to refer to this as 64K, where K is equal to 1,024. Thus 64K bytes, or 32K 16-bit words are directly addressable. Actually in the PDP-11, the top 4K addresses are reserved for internal CPU registers and external input/output (I/O) registers. If all of the memory space were used, there could be 28K words of physical memory plus 4K locations for the CPU and I/O registers.

A PDP-11 word is divided into a high byte and a low byte as shown in Figure 2-1.

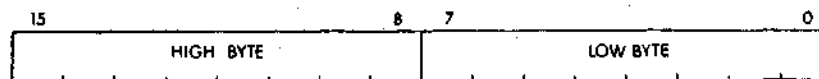


Figure 2-1 PDP-11 Word

Low bytes are stored at even numbered memory locations and high bytes are stored at odd numbered locations. Words always start at even numbered locations.

Expanded Addressing

With the large PDP-11 computers, expansion above 28K of memory can be achieved by using the Memory Management option. Memory Management provides an 18-bit effective memory address which permits addressing up to 124K words of actual memory, or with the PDP-11/70, 22 bits are used to address over 2 million words.

If Memory Management is not used, an octal address between 160 000 and 177 777 is interpreted as 760 000 to 777. That is, if bits 15, 14, and 13 are 1's, then bits 17 and 16 (the extended address bits) are considered to be 1's, which relocate the last 4K words (8K bytes) to become the highest locations accessed by the UNIBUS.

2.3 DEVICE REGISTERS

All peripheral devices are specified by a set of registers which are addressed as main memory. There are two types of registers associated with each device:

- a) Control and status
- b) Data buffer

Control and Status Registers

Each peripheral has one or more control and status registers that contain all the information necessary to communicate with that device. The general form, shown in Figure 2-2 does not necessarily apply to every device, but is presented as a guide.

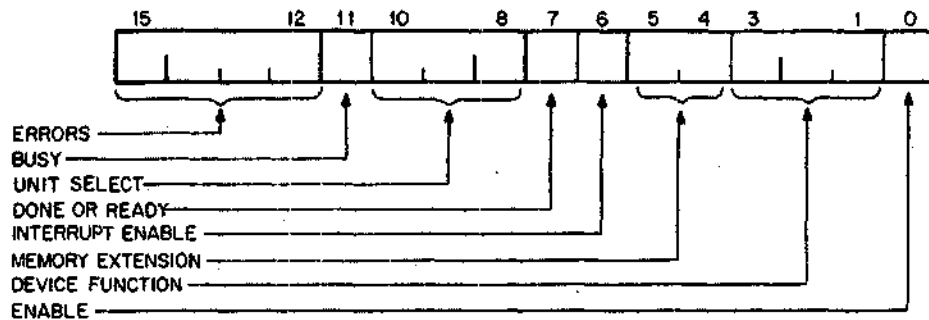


Figure 2-2 Control & Status Register

Many devices require less than 16 status bits. Other devices will require more than 16 bits and therefore will require additional status and control registers.

The bits in the control and status registers are generally assigned as follows:

BIT	NAME	FUNCTION
15-12	Errors	Generally there is an individual bit associated with a specific error. When more bits are required for errors, they can be obtained by expanding the error section in the word or by using another status word. Generally Bit 15 is the inclusive OR of all

		other error bits (if there is more than one). Most devices will have "hard" error conditions which will cause an interrupt if bit 6 is set. Some may also have "soft" errors (warning types) which do not cause immediate interrupts. All errors are generally indicated by individual status bits.
11	Busy	Set to indicate that a device operation is being performed.
10-8	Unit Select	Some peripheral systems have more than one device per control. For example, a disk system can have multiple surfaces per control and an analog-to-digital converter can have multiple channels. The unit bits select the proper surface or channel.
7	Done or Ready	The register can contain a Done bit, a Ready bit or a Done-Busy pair of bits, depending on the device. These bits are set and cleared by the peripheral device, but may be queried by the program to determine the availability of the device.
6	Interrupt Enable	Set by the program to allow an interrupt to occur as a result of a function done or error condition.
5-4	Memory Extension	Allows devices to use a full 18 bits to specify addresses on the bus.
3-1	Device Function Bits	Specifies the operation that a device is to perform.
0	Enable	Set to enable the device to perform an operation.

Data Buffer Registers

The data buffer register is used for temporarily storing data to be transferred into or out of the computer. The number and type of data registers is a function of the device.

2.4 PROCESSOR REGISTERS

2.4.1 General Registers

The central processor contains 8 general registers which can be used for a variety of purposes. The registers can be used as accumulators, index registers, auto-increment registers, auto-decrement registers, or as stack pointers for temporary storage of data. Arithmetic operations can be from one general register to another, from one memory or device register to another, or between memory or a device register and a general register. Refer to Figure 2-3.

R7 is used as the program counter (PC) and contains the address of the next instruction to be executed. It is a general register normally used only for addressing purposes and not as an accumulator for arithmetic operations.

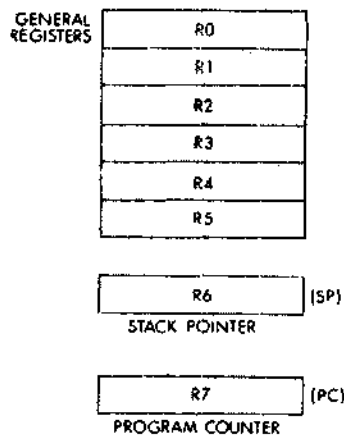


Figure 2-3 General Registers

The R6 register is normally used as the Stack Pointer indicating the last entry in the appropriate stack (a common temporary storage area with "Last-in First-Out" characteristics).

2.4.2 Processor Status Word (PS) 777 776

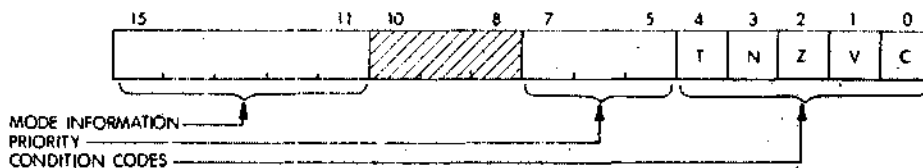


Figure 2-4 Processor Status Word

The Processor Status word, at location 777776, contains information on the current status of the computer. This information includes the condition codes describing the results of the last instruction; and an indicator for detecting the execution of an instruction to be trapped during program debugging, see Figure 2-4.

Bits 15 to 11 are used in the larger PDP-11 computers for operational mode information, and will not be covered in this Handbook. Refer to the Processor Handbooks for further information.

Processor Priority

The central processor operates at any one of eight levels of priority, 0-7. When the CPU is operating at level 7 an external device cannot interrupt it with a request for service. The central processor must be operating at a lower priority than the external device's request in order for the interruption to take effect. The current priority is maintained in the Processor Status word (bits 7-5), with bit 5 being the LSB. The 8 processor levels provide an effective interrupt mask.

Condition Codes

The condition codes contain information on the result of the last CPU operation.

The bits are set as follows:

Z = 1, if the result was zero

N = 1, if the result was negative

C = 1, if the operation resulted in a carry from the MSB

V = 1, if the operation resulted in an arithmetic overflow

Trap

The trap bit (T) can be set or cleared under program control. When set, a processor trap will occur through location 14 on completion of instruction execution and a new Processor Status word will be loaded. This bit is especially useful for debugging programs as it provides an efficient method of installing breakpoints.

2.5 INTERRUPT STRUCTURE

If the appropriate Interrupt Enable bit is set in the control and status register of a device, transition from 0 to 1 of the Ready or Error bit causes an interrupt request to be issued to the processor. Also if Ready or Error is a 1 when the Interrupt Enable is turned on, an interrupt request is made. If the device makes the request at a priority greater than that at which the processor is running and no other conflicts exist, the request is granted and the interrupt sequence takes place:

- a) the current program counter (PC) and processor status (PS) are pushed onto the processor stack;
- b) the new PC and PS are loaded from a pair of locations (the interrupt vector) in addressed memory, unique to the interrupting device.

Since each device has a unique interrupt vector which dispatches control to the appropriate interrupt handling routine immediately, no device polling is required. Furthermore, since the PS contains the processor priority, the priority at which an interrupt request is serviced can be set under program control and is independent of the priority of the interrupt request. The Return from Interrupt Instruction is used to reverse the action of the interrupt sequence. The top two words on the stack are popped into the PC and PS, returning control to the interrupted sequence.

2.6 PROGRAMMING WITH DEVICE REGISTERS

The diagram of Figure 2-5 shows 4 bits that would appear in many common Command and Status registers.

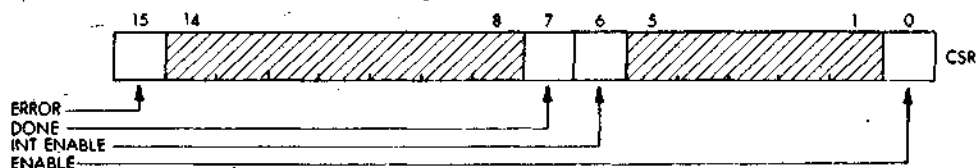


Figure 2-5 CSR Register

BIT	NAME	FUNCTION
15	Error	Set when an error occurs.
7	Done	Set when the device is either ready to accept new information, or has completed an operation and has data available.
6	Interrupt Enable (INT ENBL)	When set, an interrupt will be requested when Done or Error becomes a 1.
1	Device Enable (ENBL)	Set to allow the peripheral device to perform a function.

The diagram of Figure 2-6 shows a typical data buffer that can hold an 8-bit character.

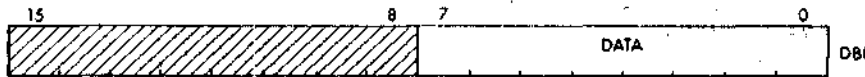


Figure 2-6 DBR Register

BIT	NAME	FUNCTION
7-0	Data	Holds the ASCII code for a character to be either written to or read from the peripheral device.

In the following examples, these two registers will be referred to by the symbolic designations, CSR and DBR.

Example: Transfer information from the peripheral data buffer to general register R3.

```
MOV DBR, R3
```

Since the information is only 8 bits, and it resides in the low part of the DBR, the byte instruction would accomplish the same purpose;

```
MOVB DBR, R3
```

The bit manipulating instructions,

BIT (bit test), set condition codes N & Z according to an AND operation on corresponding bits; neither source nor destination are modified.

BIC (bit clear), put 0's in all positions of the destination that correspond to a 1 in the source.

BIS (bit set), put 1's in all positions of the destination that correspond to a 1 in the source (OR operation).

can be used to conveniently modify or test the contents of the CSR register.

Example: Enable the peripheral device to perform an I/O function:

```
BIS #1, CSR ; OR CODE 000 001 WITH THE CSR
```

This instruction will set bit 0 of the CSR, but leave all other bits unchanged.

Example: Test for an error, and branch to an error handling routine if there is an error.

```
TST CSR      ;SET CONDITION CODE BITS ON CONTENTS OF CSR
BMI ERRTN    ;TEST BIT 15, BRANCH ON MINUS
```

ERRTN means the address of the error routine. When there is an error, bit 15 = 1, the CSR looks like a negative number (sign bit = 1).

Example: Test to see if the peripheral device has performed a read function, and data is available. Transfer to a read subroutine if data is available.

```
BIT #200, CSR ;TEST BIT 7 OF THE CSR
BNE SBR       ;BRANCH IF DONE IS SET
```

The CSR register is ANDed with a word of all 0's except for bit 7. If bit 7 (DONE) of the CSR is a 1, the result is not zero, and a branch on not equal to 0 can be made to a service subroutine (SBR).

Example: Prevent the peripheral device from causing an interrupt.

```
BIC #100, CSR ;CLEAR THE INT ENBL BIT
```

Using a source of 000 100 has the effect of clearing bit 6 (INT ENBL), but leaving all other bits of the CSR alone.

Example: Have the program continuously check the DONE bit, and read a word when it becomes a 1.

```
AGAIN: TSTB CSR ;TEST BIT 7, SIGN BIT
        BPL AGAIN ;BRANCH IF NOT SET
        MOV B, DBR, RO ;TRANSFER DATA TO CPU
```

Bit 7 of the CSR is conveniently the sign bit for the low order byte, and can be tested directly by a single instruction.

2.7 DEVICE PRIORITY

Each peripheral has a priority level assigned to it by hardware, allowing it to interrupt lower priority level devices. To ensure that the CPU which executes the peripheral's service routine is not incorrectly interrupted, the CPU itself must take on the priority level of the interrupting peripheral (Level 4, 5, 6, or 7) while running the service routine, see Figure 2-7.

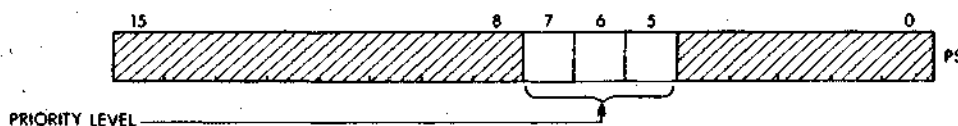


Figure 2-7 Processor Status Word

Example: Write a program to service the input keyboard data (register KBB) from the LA30 DECwriter. The interrupt vector is at location 60, and the priority level is 4.

```

    . = 60
    .WORD KBSBR ;PC = KEYBOARD SUBR ADDRESS
    . WORD 200 ;PS = 4 (BITS 7, 6, 5, = 100)
KBSBR; MOV KBB, R1
      RTI

```

Example: Set the priority level of the processor to level 3.

```

PS = 777776 ;ADDRESS OF PROC STATUS WORD
CLR PS      ;START WITH ALL 0's
BIS #140, PS ;SET BITS 6 & 5, PS = 3

```

Example: A paper tape reader interrupt service could appear as follows: First the user must initialize the service routine by specifying an address pointer and a word count

```

INIT: MOV #BUFADR,POINTR ;SET ADDRESS POINTER
      MOV #COUNT,COUNTR ;SET COUNTER
      MOV #101,PRS       ;ENABLE READER PROGRAM TO CON-
                          ;TINUE UNTIL INTERRUPT

```

When the interrupt occurs and is acknowledged, the processor stores the current PC and PS on the stack. Next it goes to the interrupt vector and picks up the new PC and PS beginning at location 70. When the program was loaded the address of PRSER, the PR service routine, would be put in location 70 and 200, in 72 (to set priority at 4). The next instruction executed is the first instruction of PRSER.

```

PRSER: TST PRS           ;TEST FOR ERROR
      BMI ERROR         ;BRANCH IF BIT 15 SET
      MOVB PRB,@POINTR ;MOVE CHARACTER TO BUFFER
      INC POINTR        ;INCREMENT POINTER
      DEC COUNTR        ;DECREMENT CHARACTER COUNT
      BEQ DONE         ;BRANCH WHEN INPUT DONE
      INC PRS           ;START READER FOR NEXT CHARAC-
                          ;TER
DONE:  RTI              ;RETURN TO INTERRUPTED PRO-
                          ;GRAM

```

CHAPTER 3

CATEGORIES OF PERIPHERALS

3.1 GENERAL

This chapter contains general information and comparisons of the PDP-11 peripherals. Sometimes a peripheral will fall into more than one category, and it will be listed wherever applicable.

This chapter shows the broad range of peripheral equipment offered and the wide span of equipment capabilities. Some of them are compared below.

Comparison of Input Equipment

MEDIUM	PRODUCT	INPUT SPEED (max)
Paper tape	High speed reader/punch, PC11	300 characters/sec
Cards	Card reader, CD11	1,600
Magnetic tape	Cassette, TA11	560
	DECtape, TC11	10,000
	Magtape, TS03	10,000
	, TM11	36,000
	, TU16	72,000

Comparison of Output Equipment

MEDIUM	PRODUCT	OUTPUT SPEED (max)
Paper tape	High speed reader/punch, PC11	50 characters/sec
Printer	DECwriter II, LA36	30
	DECprinter, LA180	180
	Line printer, LP11	2,600
CRT terminal	Alphanumeric terminal, VT05	240
	Graphic terminal, GT40	960
	DECscope, VT52	960
Magnetic tape	Cassette, TA11	560
	DECtape, TC11	10,000
	Magtape, TS03	10,000
	, TM11	36,000
	, TU16	72,000

3.2 MAIN MEMORY

Memories with different ranges of speeds and various physical and electrical characteristics can be freely mixed and interchanged within a PDP-11 system. Memory is treated as a physically modular, but electrically integral part of the computing system.

Types of Memory

Core, semiconductor, and read only memory (ROM) is offered for PDP-11 systems. Semiconductor memory (MOS and bipolar) is available for use with several of the PDP-11 Central Processing Units.

Parity is an available option for both core and semiconductor memory. No increase in mounting space is required.

Operating Speed

The CPU can begin processing data immediately after accessing it. (Access time is defined as the time interval between request and when the data is available.) Core memory then rewrites itself while the processor is working. (Semiconductor memory contents are not destroyed on read-out.) This makes the access time the important operating parameter for the PDP-11, thus providing increased speed and efficiency. The only effect cycle time has on the PDP-11 is the time needed between successive transfers to memory.

Packaging

Memory is offered as a complete system, including control and interfacing logic, interconnecting cables, and mounting assembly. Several of the PDP-11 processors have dedicated, pre-wired areas within the chassis for holding additional memory. In other cases, memory can be added within the CPU mounting assembly, and the necessary power taken from the cabinet power supplies.

3.3 TERMINALS

Characteristics and Applications

- a) convenient human interface to the computer
- b) typewriter-like keyboard for data entry
- c) printer or display for output from computer
- d) basic input/output device
- e) can be local (console terminal), or remote

Products

MODEL	DESCRIPTION	OUTPUT SPEED (max)
LA36	DECwriter II	30 characters/sec
VT05	Alphanumeric	240
VT50	Alphanumeric	960
GT40	Graphic display system (includes a computer)	960 char/sec as a simple serial interfaced terminal, operation can be faster as a syn- chronous device
VT52	Video display	960

3.4 PAPER TAPE

Characteristics and Applications

- a) simple medium to use
- b) separate tapes for individual programs
- c) variable program length
- d) data can be read by a person

Products

MODEL	DESCRIPTION	READ SPEED	PUNCH SPEED
PC11	Paper tape reader/punch	300 char/sec	50 char/sec
PR11	Paper tape reader	300	—

3.5 CARDS

Characteristics and Applications

- a) individual records
- b) easy to add, delete, or rearrange a card
- c) possible to print on the card
- d) can be read by a person

Products

MODEL	DESCRIPTION	TYPE	READ SPEED
CM11	Card reader	mark-sense or punch	285 cards/min
CR11	Card reader	punch	285
CD11	Card reader	punch	1200

3.6 PRINTERS

Characteristics and Applications

- a) hard copy for permanent records
- b) impact types can make multiple copies
- c) some plotting capability

Products

MODEL	DESCRIPTION	TYPE	PRINT SPEED	COLUMNS	CHAR.
LA36	DECwriter	impact	30 char/sec	80	64
LA180	DECprinter	impact	180 char/sec	132	96
LP11	Line Printer	impact	230 to 1200 lines/min	132	64 or 96
LV11	Printer/plotter	electro- static	500 lines/min	132	96

3.7 MAGNETIC TAPE

Characteristics and Applications

- a) unlimited off-line storage
- b) removable medium

Products

MODEL	DESCRIPTION	STORAGE/REEL	DATA RATE
TA11	Cassette	90,000 char	560 char/sec
TC11/TU56	DECTape	295,000	10,000
TS03	Magnetic tape	5,000,000	10,000
TM11/TU10	Magnetic tape	20,000,000	36,000
TU16	Magnetic tape	32,000,000	72,000

3.8 DISKS

Characteristics and Applications

- a) fast access to on-line storage
- b) swapping programs
- c) virtual memory
- d) efficient bulk storage

- a) Fixed Head—fast access time
- b) Moving head—high storage capacity, more economical storage
- c) Disk pack—removable medium, unlimited off-line storage

The average access time (avg latency) is equal to $\frac{1}{2}$ the time for a revolution plus the average head positioning time (for moving head disks only).

Products

MODEL	DESCRIPTION	CAPACITY/ DRIVE	AV ACCESS TIME	DATA RATE
RX11/RX01	Floppy disk	125K words	483 msec	36 μ sec/word
RK11/RK05	Disk cartridge	1.2 million words	70msec	11 μ sec/word
RP11/RP03	Disk pack	20 million	42	7.5
RS03	Fixed head disk	256 K	8.5	4 or 8
RS04	Fixed head disk	512 K	8.5	4
RP04	Disk pack	44 million	36	2.5

3.9 DISPLAYS

Characteristics and Applications

- a) pleasing human interface
- b) soft copy of information
- c) fast presentation of information
- d) alphanumeric and graphic capability

Products

MODEL	DESCRIPTION
VR01	Oscilloscope
VR14	Point plot display
VT01	Storage display
VT05	Alphanumeric terminal
VT50	Alphanumeric terminal
VT52	Alphanumeric terminal
GT40	Graphic display system (includes a computer)

3.10 COMMUNICATIONS OPTIONS

Characteristics and Applications

Asynchronous Interfaces—Character transmission time is variable, but bits within the character are timed; a character transmission normally includes a start bit, several data bits, one or more stop bits, and an optional parity bit.

Synchronous Interfaces—Continuous data stream once the receiver is synchronized; data is generally transmitted in message blocks containing both information and timing signals.

Other Communications Options—Provide error detection, autocalling unit interfacing, and signal conditioning.

Products

MODEL	DESCRIPTION	TYPICAL USE
DL11	Single Asynchronous Line Interface	Connects PDP-11 to local terminals (such as Teletype, LA36 and VT05) or to remote terminals via modems.
DJ11	16-Line Asynchronous Multiplexer	Connects PDP-11 to up to 16-local terminals or up to 16-remote terminals via modems. Transmission speeds and other parameters are switch or jumper selectable in 4-line groups.
DH11	16-Line Programmable Asynchronous Multiplexer	Connects PDP-11 to up to 16-local terminals or remote terminals. Transmission speeds and parameters are programmable.
DN11	Auto Calling Unit Interface	Interfaces PDP-11 to Bell 801 auto calling units.
DU11	Single Line Synchronous Interface	Connects PDP-11 to modems for medium speed (up to 9600 Baud) synchronous transmission.
DQ11	Single Line Synchronous Interface	Used for high throughput synchronous transmission.
KG11	Communication Arithmetic Element	Used to detect errors in serially transmitted data.
DC08 and H316	Telegraph Line Interfaces	Connects PDP-11 to telegraph equipment.

DF11	Signal Conditioning Options	Converts computer (TTL) signals to EIA or 20 ma signals. Can be used with DC11, DL11 and DH11 interfaces.
DF11-B	Integral Modems	Converts TTL signals to audio frequencies. Used to connect PDP-11 directly to Bell Data Access Arrangement options.
DF01	Acoustic Coupler	Connects terminal (VT05, LA36) to standard telephone for communication with computer via phone lines.
H313-A	Voltage Current Adapter	Converts Digital supplied TTY output for use with Bell 103 modems or equivalent.
H312-A	Null Modem	Allows direct connection of a terminal with an EIA cable to a DC11, DL11, or DM11-DB.

3.11 DATA ACQUISITION

Characteristics and Applications

- a) analog conversion equipment
- b) analog circuitry
- c) digital control and monitoring
- d) timing control
- e) laboratory experimentation
- f) industrial control

Products

MODEL	DESCRIPTION
AA11	Digital-to-analog conversion subsystem, 12 bits
AD01	Analog-to-digital conversion subsystem, 10 or 11 bits
LPS11	Lab Peripheral System, 12 bits (A/D, real time clock, D/A, digital I/O)
AFC11	Low level analog input subsystem, flying capacitor scanner
UDC11	Digital control subsystem
KW11-L	Line clock
KW11-P	Programmable clock

3.12 UNIBUS EQUIPMENT

MODEL	DESCRIPTION
DR11-K	General device interface
DR11-C	General device interface (program interrupts)
DR11-B	Direct Memory Access interface (NPR data transfers)
DT03	UNIBUS switch
DA11-B	UNIBUS link
DA11-F	UNIBUS window

3.13 MOUNTING EQUIPMENT

MODEL	DESCRIPTION	SYSTEM UNIT SPACE
BB11	Blank mounting panel	1
DD11	Peripheral mounting panel	1
BA11-K	Extension Mounting Box	5
H960-D	Cabinet with a drawer	9
H960-CA	Cabinet	

DESCRIPTIONS OF PERIPHERALS

4.1 INTRODUCTION

This chapter contains detailed descriptions, specifications, programming, and operating information for PDP-11 peripheral equipment. For ease of reference, the peripherals have been arranged alphanumerically by model number, with the model number appearing on the top right-hand side of each page.

Since some peripherals have similar descriptions and specifications, related peripherals will be described within the same section. Section 4.3 contains a complete list of all equipment described in this chapter. Appendix E contains an index to all equipment described in this Handbook.

4.2 EXPLANATION OF TERMS AND SPECIFICATIONS

4.2.1 Products

All the peripherals mentioned in this chapter must eventually interface to the UNIBUS. Some of the equipment, such as Line Printers, include a control unit as well as the printer itself. The control unit, sometimes referred to as a controller or interface unit, is the actual logic equipment between the UNIBUS and the peripheral device. With terminals, the control unit and the terminal itself are separate products. In this case, several different control units could be used, depending on the application. In other cases, such as disk drives, a single model number includes a control unit and the first disk drive of the system. Other disk drives, up to the limit of the system, are specified by another model number, see Figure 4-1.

4.2.2 Registers

The device registers are shown with their common name, their mnemonic in parentheses, then their UNIBUS address. Note that these addresses begin with 77 or 76 (instead of 17 or 16) to indicate that they are in the highest 4K words of address space. Within the functional description of each bit, if not otherwise indicated, the condition or operation when the bit is set (logic 1) is described.

Some bit positions of the registers are not used (not implemented with hardware). When diagrams are shown, unused positions are indicated by cross-hatching. Some of the bits are controlled only by the peripheral device and are indicated as read only (by the program). Some of the bits are write only (by the program), and are always read as zeros. Some bits are cleared (or set) by the UNIBUS master clear signal called Initialize, which has the mnemonic INIT. It is issued by turning Power ON, Console START, or the RESET instruction. Figure 4-2 summarizes the information about the device registers.

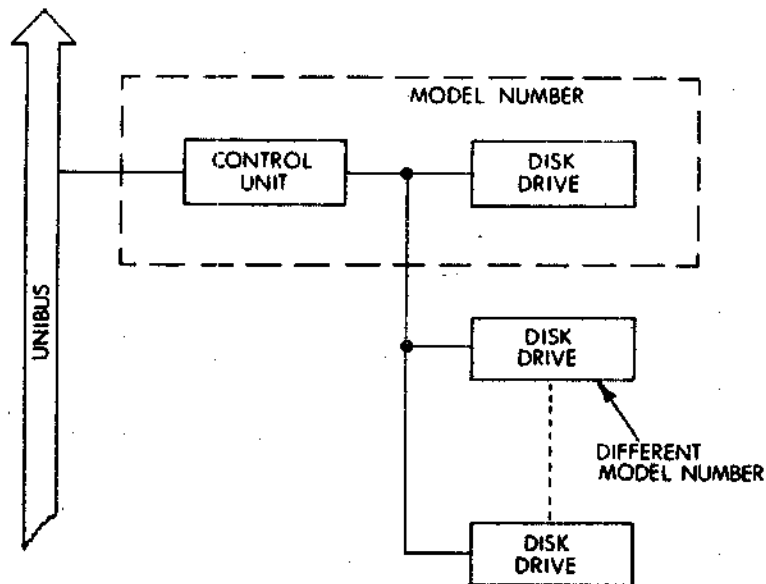
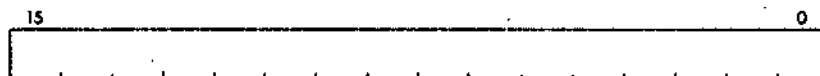


Figure 4-1. Disk Storage System

The unused or write only bits are always read as zeros by the program. Trying to load unused or read only bits has no effect on the addressed register.

Register (REG) 77x xxx



▨ = unused bit

Read only: (with respect to the CPU or bus master)—The program can monitor the bit, but cannot modify it.

Write only: (with respect to the CPU or bus master)—The program can set or clear the bit; but when reading, it will always appear to be a zero.

Figure 4-2. Device Register

4.2.3 Specifications
UNIBUS Interface

Interrupt and trap vectors are assigned to the lowest part of memory, generally in the range 000 000 to 000 377. Bus Request (BR) levels are indicated; also Non-Processor Request (NPR) operation if applicable. Most devices that interface to the UNIBUS represent only 1 bus load.

Mechanical

The mounting arrangement of the equipment is indicated as:

- a) module: plugs into a dedicated logic module slot
- b) SPC: fits in a small peripheral controller slot (quad module)
- c) SU: system unit mounting assembly is included
- d) panel: uses front panel space in a cabinet
- e) table top: suitable for placing on top of a table or a desk
- f) free standing: by itself, not in a cabinet
- g) cabinet: mounts in a standard PDP-11 cabinet

Some peripherals include 2 separate physical parts and are indicated by use of a plus (+) sign.

Relative Humidity

All humidity specifications mean without condensation.

Temperature

Correspondence between Centigrade and Fahrenheit is shown in the following table:

<u>°C</u>	<u>°F</u>
0	32
5	41
10	50
15	59
20	68
25	77
30	86
35	95
40	104
45	113
50	122
55	131

$$\left[(^\circ\text{C}) \times \frac{9}{5} \right] + 32 = (^\circ\text{F})$$

4.2.4 Conversion Factors

$$(\text{inches}) \times 2.54 = (\text{cm})$$

$$(\text{lbs}) \times 0.454 = (\text{kg})$$

$$(\text{Watts}) \times 3.41 = (\text{BTU/hr})$$

4.3 LIST OF PERIPHERALS

The peripherals described in this chapter are arranged in the following sequence:

Model Numbers	Description	Page
AA11 (also BA164)	D/A subsystem	4-5
AD01	A/D subsystem	4-9
AFC11	Low level analog subsystem	4-13
AR11	Analog subsystem	4-19
BA11-K	Expansion mounting box	4-22
BB11	Blank mounting panel	4-24
BM792 (also MR11-DB, M792)	Read only memory	4-25

BM873	Restart/Loader	4-27
CD11	Punched card reader	4-31
CR11 (also CM11)	Punched card reader	4-44
DA11-B	UNIBUS link	4-54
DA11-F	UNIBUS window	4-59
DB11	Bus repeater	4-67
DD11	Peripheral mounting panel	4-68
DF01	Acoustic telephone coupler	4-72
DF11	Serial line signal conditioning	4-74
DH11 (also DM11)	Asynch serial line multiplexer (prog)	4-82
DJ11	Asynch serial line multiplexer	4-111
DL11	Single asynch serial line interface	4-128
DL11-W	Serial line interface	4-145
DMC11	Network link	4-150
DN11	Automatic calling unit interface	4-169
DQ11	NPR synch line interface	4-177
DR11-B	Direct memory access interface	4-212
DR11-C	General device interface	4-217
DR11-K	General device interface	4-227
DT03	UNIBUS switch	4-231
DU11	Synchronous line interface	4-235
DUP11	Synchronous line interface	4-254
DV11	Synchronous preprocessor	4-278
GT40	Graphic display system	4-311
H312	Asynchronous null modem	4-317
H960	Standard PDP-11 cabinet	4-318
KE11	Extended arithmetic element	4-320
KG11	Communications arithmetic option	4-323
KW11-L	Line time clock	4-332
KW11-P	Programmable real time clock	4-333
LA35	DECwriter II printer	4-336
LA36	DECwriter II terminal	4-341
LA180	DECprinter	4-349
LP11	High speed line printer	4-353
LPS11	Lab peripheral system	4-360
LV11	Electrostatic printer/plotter	4-372
PC11 (also PR11)	High speed paper tape reader/punch	4-376
RJP04 (also RP04)	Disk pack	4-384
RJS04 (also RS04)	Fixed head disk	4-414
RK11 (also RK05)	DECpack disk cartridge	4-433
RP11 (also RP03)	Disk pack	4-445
RX11 (also RX01)	Floppy disk	4-455
TA11	Cassette	4-462
TC11 (also TU56)	DEctape	4-467
TJU16 (also TU16)	Magnetic tape	4-480
TM11 (also TU10)	Magnetic tape	4-501
TS03	Magnetic tape	4-515
UDC11	Universal digital control subsystem	4-519
VR01	Oscilloscope	4-526
VR14	Point plot display	4-527
VT01	Storage display	4-529
VT05	Alphanumeric display terminal	4-530
VT50	Alphanumeric display terminal	4-536
VT52	DECscope terminal	4-542

DIGITAL TO ANALOG SUBSYSTEM, AA11-D

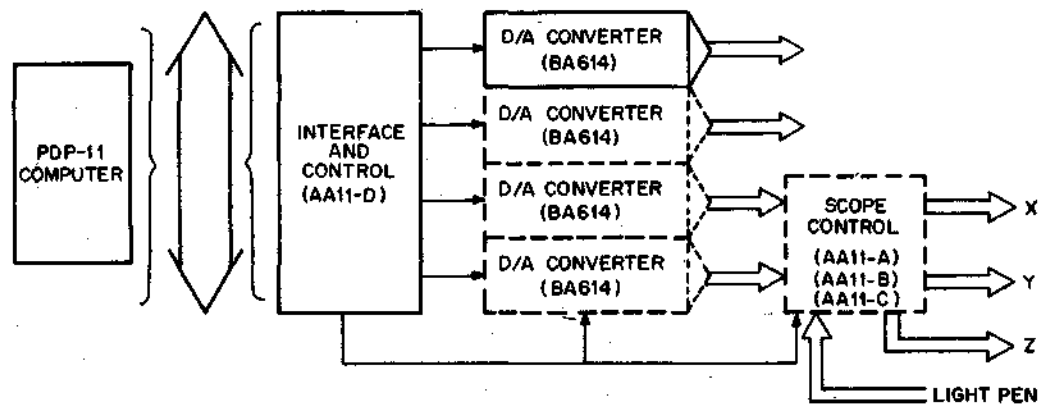
DESCRIPTION

The AA11-D is a low cost, high performance multichannel digital-to-analog conversion subsystem for PDP-11 computers.

Interfacing directly to the PDP-11 UNIBUS, the AA11-D controls up to four single buffered, 12-bit bipolar digital-to-analog converters. Each BA614 converter, which includes output amplifier and reference voltage source, is contained on a plug-in module and provides 10 ma current output at ± 10 volts. Full scale output voltage is trimpot adjustable from $\pm 1v$ to $\pm 10v$ in two ranges.

Storage scope, display scope, and light pen control options are available for the AA11-D. These options provide Z axis blanking for intensity control and require two D/A converters to control X and Y trace coordinates.

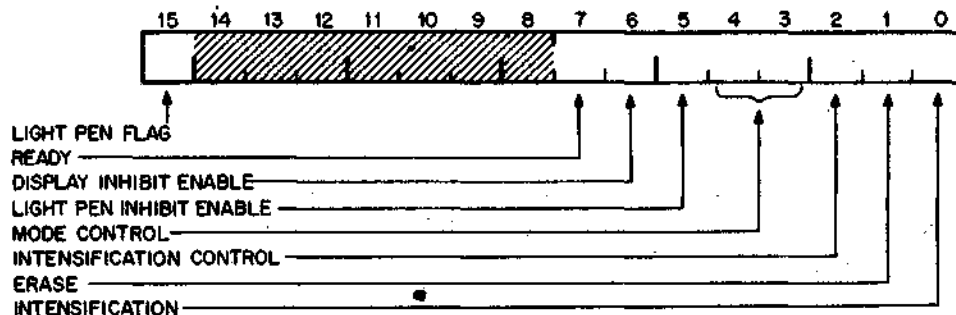
Available as a factory or field installed option, the AA11-D fully implemented with four digital to analog converters and a scope control option, is contained in a single System Unit. A rack mountable power supply is separate.



AA11-D Subsystem

REGISTERS

Command and Status Register (CSR) 776 756

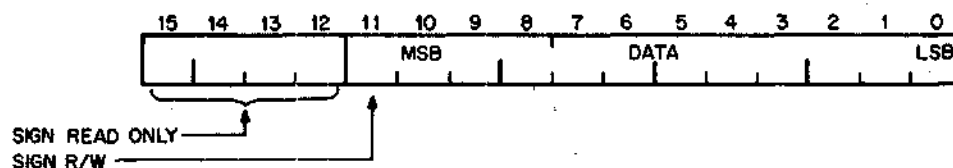


AA11

BIT	NAME	FUNCTION
15	Light Pen Flag	If bit 05 is "1," light pen flag causes interrupt. Cleared by INIT and reading the register. Read only.
7	Ready	Set when scope is ready for service, because of INTEN or ERASE commands or X or Y has been loaded. Interrupt occurs if bit 06 is "1." Bit 07 is set by INIT and cleared by displaying new point. Read only.
6	Display Inhibit Enable	Set to permit interrupts to occur when intensification or erasure is completed. This bit is set by program control and cleared by INIT. Read/Write.
5	Light Pen Inhibit Enable	Set to permit interrupts to occur when signal is received from light pen. This bit is set by program control and cleared by INIT. Read/Write.
4-3	Mode Control	Determines intensification on loading X or Y.
2	Intensification Control	Selects Stored Mode or High Intensity Mode depending on scope used. Read/Write
1	Erase	Set to erase storage scope display. Sets READY bit 7 at end of erase.
0	Intensification	Set to delay display until scope deflects to new X, Y values, then strobos intensification (Z axis) and sets READY bit 7.

Data Registers (DAC) 776 760 to 776 766

DAC1 and 2 may be used either in conjunction with the scope or for D/A channels. DAC3 and 4 may be used for additional D/A channels.



BIT	NAME	FUNCTION
15-12	Sign	Read only (2's complement)
11	Sign	Read/Write (2's complement)
10-0	Data	Read/Write.

AA11

SPECIFICATIONS FOR AA11-D

Register Addresses

Command and Status (CSR)	776 756
Data Register (DAC1)	776 760
Data Register (DAC2)	776 762
Data Register (DAC3)	776 764
Data Register (DAC4)	776 766

UNIBUS Interface

Interrupt vector address:	140, 144
Priority level:	BR4, or 5
Bus loading:	1 bus load

Mounting: 1 System Unit (SU)

Power

Input current:	0.5 A at 115 VAC 3 A at + 5 V
Heat dissipation:	60 W

Environment

Operating temperature:	10°C to 40°C
Relative humidity:	10% to 90%

Models

AA11-DA:	D/A converter subsystem, 115 VAC, 60 Hz
AA11-DB:	" " , 230 VAC, 50 Hz

SPECIFICATIONS FOR D/A CONVERTER (BA614)

Digital Input:	11 bits + sign, 2's complement code.
Digital Storage:	Single buffered.
Update Rate/Channel:	50 KHz
Analog Output Voltage:	2 continuously adjustable full scale ranges: 1v to 5v and 5v to 10v
Current:	10 ma
Gain Accuracy:	± 0.025% of full scale (25°C)
Linearity:	± 1/2 least significant bit (LSB)
Zero Offset:	Adjustable to zero
Settling Time:	20 μs max. to within 1/2 LSB for full scale step change (at output connector with zero capacitance loading).
Output Impedance:	Less than 1 ohm.
Temp Coefficient: (after 5 min. warmup)	± 50 μV/ °C - zero offset and ± .003%/ °C - gain accuracy

AA11

SCOPE CONTROL OPTIONS

The following scope controls each require two BA614 digital to analog converters:

AA11-A Scope Control for Tektronix 611 Storage Display Unit

Display Rate: 30 Hz (min) to 10 KHz (max)
Display Time: deflection time 80 μ s
intensification time 20 μ s
Non-storage mode:
deflection time 80 μ s
intensification time 2 μ s

Erase Time: 0.5 sec

AA11-B Scope Control for Tektronix RM503 Oscilloscope

Display Rate: 45 KHz (max)
Display Time: deflection time 20 μ s
intensification time 2 μ s

Intensification: (program selectable) two levels

AA11-C Scope Control for VR12 Point Plot Display

Display Rate/point: 40 Hz (min) to 40 KHz (max)
Display Time: deflection time 20 μ s
intensification time 2 μ s

Intensification: (program selectable) two levels

ANALOG TO DIGITAL SUBSYSTEM, AD01-D

DESCRIPTION

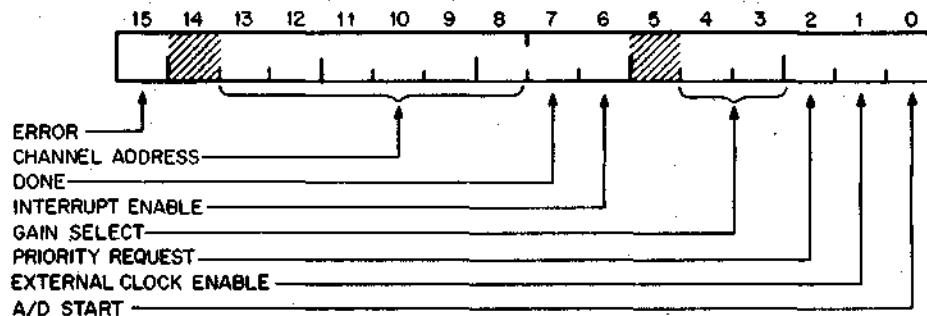
The AD01-D is a flexible, low-cost multichannel analog data acquisition option which interfaces directly to PDP-11 computers. When it is under computer or external clock control, the AD01-D provides 10-bit digitization of unipolar high-level analog signals having a nominal full-scale range of 0 to + 1.25, + 2.5, + 5.0 or + 10.0 volts. An optional sign-bit addition allows 11-bit bipolar operation. Programmable input range selection extends the AD01-D's dynamic range at moderate sampling rates to the equivalent of 13 bits for unipolar signals or 14 bits for bipolar signals.

An optional sample-and-hold amplifier reduces the conversion aperture to 100 nanoseconds.

The standard AD01-D consists of an expandable solid-state input multiplexer, programmable input range selector, A/D converter, control, and bus interface in a single 5 $\frac{1}{4}$ -inch rack-mountable assembly plus a separate logic power supply. The multiplexer can be expanded by adding 4-channel modules up to 32 channels. An expansion multiplexer may be added to provide a maximum configuration of 64 channels.

REGISTERS

Control and Status Register (ADCS) 776 770



BIT	NAME	FUNCTION
15	Error	Set when a new conversion is initiated while a conversion is being performed. Interrupt is produced when interrupt bit (bit 6) is enabled.
13-8	Channel Address	Selects 1 of 32 multiplexer channels.
7	Done	Set upon completion of conversion and reset upon reading data register.
6	Interrupt Enable	Program selectable interrupt mode. Interrupt produced on A/D done (bit 7) or error (bit 15) when selected.

AD01

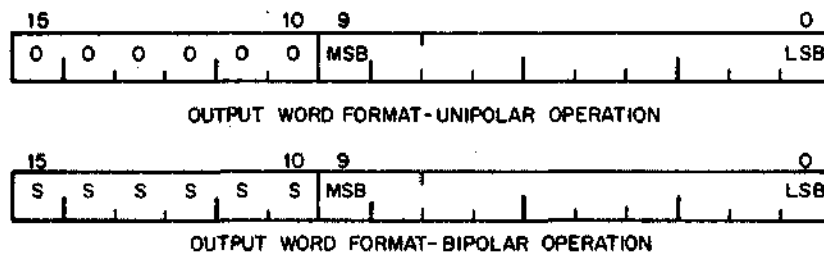
3-4	Gain Select	Selects input gain range of 1, 2, 4, or 8.
2	Priority Request	Program can select priority request BR7 or BR6, 5, 4.
1	External Clock Enable	Set to initiate conversion by external clock.
0	A/D Start	Set to initiate conversion by program. (Conversion is also started when a new multiplexer channel (and gain) is selected, except when external clock is enabled.)

One input channel is selected by the multiplexer and connected to a highly-linear programmable gain selector, which scales the input range to + 10 volts full-scale.

The scaled 10 volt output is directed to the summing junction of the A/D converter input through the sample-and-hold and sign-bit options, if installed. In 10 μ sec, the A/D converter digitizes the analog voltage at its input into a 10-bit binary code, using the successive-approximation technique. The sign-bit option permits conversion of bipolar inputs (0 to ± 1.25 , ± 2.5 , ± 5.0 , or ± 10.0 volts) to an 11-bit 2's complement code with an extended sign format.

Data Buffer Register (ADDB) 776 772

The A/D converter Data Register transfers data to the PDP-11 in the following format. To the processor, the data is read only.



Bits 15 to 10 are tied together, and are "0" in the standard unipolar configuration. With the sign bit option, bits 15 to 10 indicate the sign of the input voltage.

OUTPUT NOTATION TABLE *

Analog Input Voltage	Unipolar	Bipolar
-10.0		176 000
- 5.0		177 000
0.0	000 000	000 000
+ 5.0	001 000	001 000
+ 9.9902	001 777	001 777

* For 10 volt full scale input range. Divide by appropriate gain factor for other input ranges.

AD01

Each multiplexer channel switch consists of an enhancement mode MOSFET, which is normally open when unselected or when system power is removed. These switches provide overload protection up to ± 20 volts, and signal protection against electrical short-circuit.

SPECIFICATIONS

Main Specifications

Resolution:	Unipolar 10 bits, or 1 part in 1024 Bipolar (option) sign + 10 bits.
System Accuracy:	0.1% of full scale (FS) input
Quantizing Error:	$\pm 1/2$ least significant bit
System Conversion Time: (includes Channel and gain)	Unipolar: 22 μ sec Bipolar: 29 μ sec
Sample and Hold:	Acquisition: 5 μ sec to $\pm 0.01\%$ of FS step Aperture: 100 nanoseconds
Analog Input Channels:	4 minimum, expandable to 32 in groups of 4
Input voltage range: (program selectable)	Unipolar: 0 to + 1.25, + 2.5, + 5.0, + 10.0v FS Bipolar (option): 0 to ± 1.25 , ± 2.5 v, ± 5.0 , ± 10.0 v FS
Input Impedance:	1000 megohms in parallel with 20 pf
Input Isolation:	Enhancement mode MOSFET switches, "off" when unselected or power off.
Analog Input Connectors:	Plug-in cable-module
Channel Selection: (program selectable)	6 bit address
Cross channel attenuation:	78 db, DC-80Hz for 20 volts p-p signals, 100 ohm source impedance
Input Gain:	Program selectable
Modes of Operation:	Interrupting/non-interrupting (program se- lectable) Synchronous (Program control) Asynchronous (external clock enable + 2.0v minimum into Schmidt trigger, repetition rate, 60k Hz maximum.)

Expansion/Installation

Multiplexer expansion or option inclusion in the basic AD01-D is by module insertion into prewired slots.

AD01

Register Addresses

Control and Status (ADCS) 776 770
Data Buffer (ADDB) 776 772

UNIBUS Interface

Interrupt vector address: 130
Priority level: BR4 to 7
Bus loading: 1 bus load

Mechanical

Mounting: 1 panel mounted unit
Size: 5 $\frac{1}{4}$ " front panel height
Weight: 15 lbs.

Power

Input current: 0.5 A at 115 VAC
Heat dissipation: 60 W

Environment

Operating temperature: 5°C to 50°C
Relative humidity: 10% to 95%

Models

AD01-DA: A/D converter subsystem, 115 VAC, 60 Hz
AD01-DB: " , 230 VAC, 50 Hz

AFC11

LOW LEVEL ANALOG INPUT SUBSYSTEM, AFC11

DESCRIPTION

The AFC11 is a flexible, high performance, differential analog input subsystem for IDACS-11 industrial data acquisition control systems.

The AFC11 system multiplexes up to 1024 differential input analog signals, selects gain, and performs a 13-bit analog-to-digital conversion at a 200 channel per second rate under program control. Three signal conditioning modules and eight program-selectable gains allow the system to intermix and accept a wide range of signals: low level (10 mv full scale), high level (100.0v FS), and current inputs (1 to 50 ma FS).

Designed for accurate and reliable operation in demanding industrial environments, the AFC11 achieves high isolation and common mode noise rejection through relay switched capacitor multiplexing. The subsystem also simplifies input wiring, requiring only simple twisted pairs which connect to screw terminals.

Modularly constructed in eight-channel standard hardware units, the AFC11 is easy to configure to user applications, and simple to expand.

The analog input subsystem is particularly suited for data acquisition in the high noise environments encountered in process monitoring and control, production testing and laboratory applications. In such environments common and normal mode noise, cabling and grounding problems can greatly affect the operation of such transducers as thermocouples, strain gages, analytical bridges, and industrial milliamp current transmitters. These problems can also affect the accuracy and performance of the measuring system.

In typical applications, use of ungrounded sensors could cause common mode voltages of up to 150 volts peak-to-peak (at power line frequency) to appear on the input signal leads to the measuring system. For example, if thermocouples become ungrounded during operation, large common mode voltages can appear in coincidence with the signal. The design features of the AFC11 allow either floating or grounded signal sources thus insuring reliable, trouble-free operation. Due to the flying capacitor design, the system tolerates common mode voltages in excess of 200 volts. FET solid-state multiplexers, in contrast, can be seriously damaged with common mode voltages over 25 volts.

System Organization

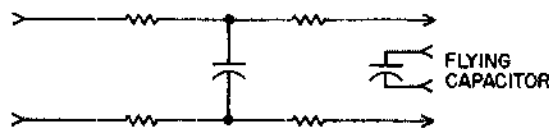
The AFC11 system is completely modular for ease of system configuration and expansion. For applications requiring 128 channels or less the system is available in a single cabinet configuration. Systems requiring greater than 128 but less than 512 channels are housed in a dual cabinet configuration—one cabinet to mount the electronics and one for the screw terminal connectors. Two dual cabinet configurations, each containing 512 channels, are required to implement a maximum system of 1024 channels.

AFC11

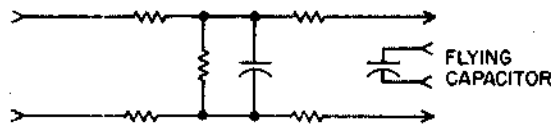
The system's electronic cabinets are organized in files. The first file in the system is a master file which contains the computer interface, system timing and control, an A/D converter, a programmable gain differential amplifier, and address decoding hardware for selection of up to 32 channels. The master file may also contain three additional file units, each providing address decoding and analog bus isolation for up to 32 channels. The hardware for each 32 channel group is implemented by adding up to four eight-channel pairs of multiplexer/signal-conditioning modules and the required screw terminal cable assemblies—one for each module pair. Fully implemented, the master file contains 128 channels.

Expansion beyond 128 channels is by addition of expander files. Each expander file contains a programmable gain amplifier and provision for a total of 192 channels in six file units.

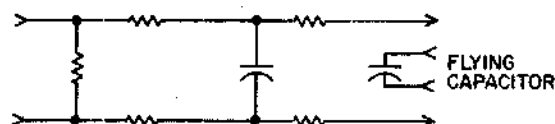
A file unit contains from one to four eight-channel Multiplexer Modules (Model BA150), each of which requires an eight-channel input signal conditioning module. The conditioning modules, which connect to screw terminal blocks via cable assemblies, are available in three types:



Direct Input Module (Model BA903) provides eight channels of normal mode input filtering with a break frequency of 2.5 Hz. Attenuation at 60 Hz is greater than 50 db.



Voltage/Voltage Input Module (Model BA904) provides 8 channels of 10:1 attenuated input with the same normal mode filtering as direct input. Maximum full scale input is + 100 volts.



Current/Voltage Input Module (Model BA905) scales eight channels of 50, 20, or 5 ma full scale current inputs to 0.5, 0.2, or 0.05 volts full

AFC11

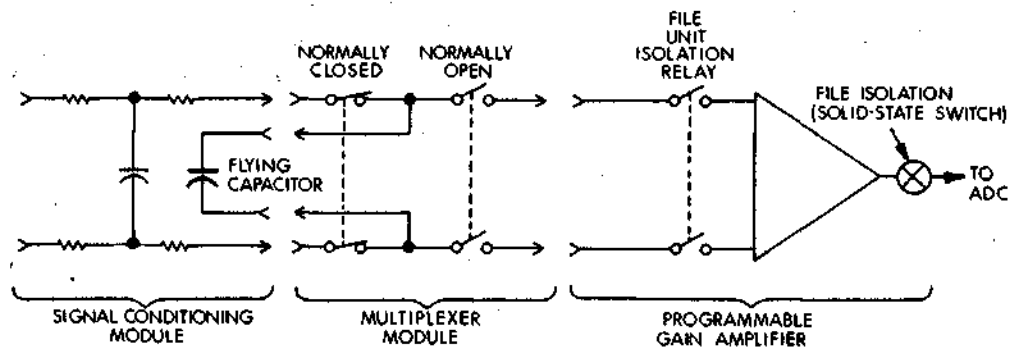
scale and provides the same normal mode filtering as the direct input module.

Flying Capacitor Multiplexing

The flying capacitor multiplexing technique permits micro-volt signals to be isolated, switched and digitized by an analog-to-digital converter with a high degree of noise immunity.

The Flying Capacitor is a two pole RC filter network in which a second or "flying" capacitor is charged, then isolated and switched to the measuring circuit. Since the source is never directly connected to the measuring circuit, extremely high isolation is achieved.

Lo-pass filtering per point (2.5 Hz cutoff) plus the high isolation of the flying capacitor technique provide high common mode noise rejection (120 db at 60 Hz) without requiring expensive individually-shielded input wiring.



Typical File Unit Channel

Programmable Gain Control Channel Selection

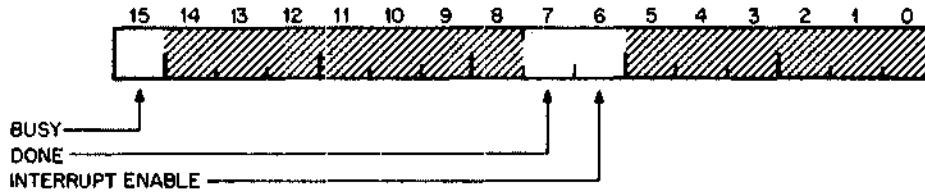
Both gain and channel are under program control. A 16-bit Channel Address Gain/Select Control word is transferred from the IDACS-11 processor to the AFC11 Channel/Gain Register (AFCG). The multiplexer channel address is contained in bits 0-10 and decoded to select 1 out of 64 File Units (6 bits) and 1 out of 32 channels (5 bits) within the File Unit. The programmable gain control on the input amplifier is buffered and FET switched for reliability. Amplifier gain is selected by bits 13-15.

When a channel is selected, the input signal is isolated and the File Unit isolation relay closes to connect the charged capacitor to the Programmable Gain Amplifier. The amplifier is connected to the analog bus and ADC by closing the file isolation switch. Timing is initiated which allows the switches to settle and conversion to begin.

AFC11

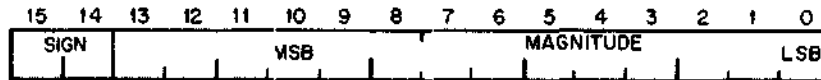
REGISTERS

Control and Status Register (AFCS) 772 570

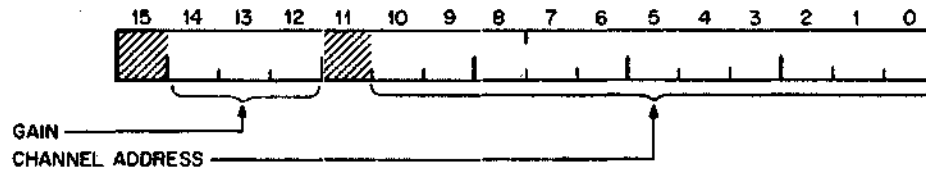


BIT	NAME	FUNCTION
15	Busy	Set by INIT or LOADING MX Channel Gain Register. Reset by A/D DONE.
7	Done	Set by A/D DONE. Reset by reading Data Buffer Register.
6	Interrupt Enable	Set under program control. Reset by INIT or under program control.

Data Buffer Register (AFBR) 772 572

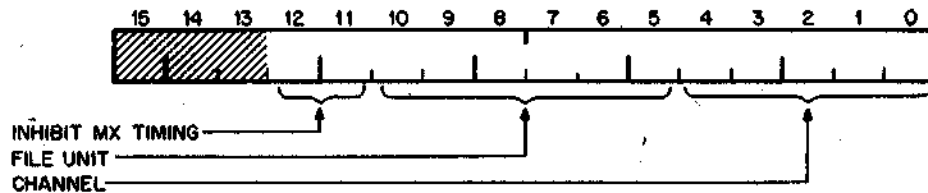


Multiplexer Channel/Gain Register (AFCG) 772 574



BIT	NAME	FUNCTION																				
14-12	Gain	Sets amplifier gain according to the following table. Cleared by INIT. (READ/WRITE).																				
		<table border="1"> <thead> <tr> <th>BIT</th> <th>GAIN</th> </tr> </thead> <tbody> <tr> <td>14 13 12</td> <td></td> </tr> <tr> <td>0 0 0</td> <td>1000</td> </tr> <tr> <td>0 0 1</td> <td>200</td> </tr> <tr> <td>0 0 0</td> <td>100</td> </tr> <tr> <td>0 1 1</td> <td>50</td> </tr> <tr> <td>1 0 1</td> <td>20</td> </tr> <tr> <td>1 0 0</td> <td>10</td> </tr> <tr> <td>1 1 0</td> <td>2</td> </tr> <tr> <td>1 1 1</td> <td>1</td> </tr> </tbody> </table>	BIT	GAIN	14 13 12		0 0 0	1000	0 0 1	200	0 0 0	100	0 1 1	50	1 0 1	20	1 0 0	10	1 1 0	2	1 1 1	1
BIT	GAIN																					
14 13 12																						
0 0 0	1000																					
0 0 1	200																					
0 0 0	100																					
0 1 1	50																					
1 0 1	20																					
1 0 0	10																					
1 1 0	2																					
1 1 1	1																					
10-0	Channel Address	Selects multiplexer channel. Bits 10-05 select 1 of 64 file units. Bits 04-00 select 1 of 32 channels in a file unit. Cleared by INIT. (READ/WRITE).																				

Maintenance Register (AFMR) 772 576



This Read/Write Register is for diagnostic purposes only. Permits checking of channel address by reading back decoded bits.

SPECIFICATIONS

Analog Input Specifications

Number of Inputs:	8 to 1024, in groups of 8
Type:	differential, 2 wire twisted pair
Connection:	solder lug, or screw terminal
System Performance	
Resolution:	Sign + 12 bits (2's complement)
Accuracy: (for direct input)	$\pm 0.025\%$ of full scale or $\pm 15 \mu\text{V}$ (whichever is larger) $\pm \frac{1}{2}$ least significant bit (LSB)
Scan Rate, Including A/D Conversion:	200 channels/second, maximum (20 samples/second, same channel)
Normal Mode Rejection:	> 50 db for frequencies 60 Hz or above
Common Mode Rejection:	> 120 db DC to 60 Hz
Common Mode Voltage Tolerance:	200 volts
Input Overload:	Amplifier fused against overload
Effects of Overload:	Recovers to within stated accuracy for next channel.
Channel-to-Channel Isolation:	10^{12} ohms at DC, Channel-to-channel. 10^{12} ohms at DC, channels on same multiplexer module.
Gain Accuracy:	$\pm 0.02\%$
Gain Linearity:	$\pm 0.01\%$
Temperature Coefficient:	$\pm .005\%/^{\circ}\text{C}$ or better

AFC11

Register Addresses

Control and Status (AFCS)	772 570
Data Buffer (AFBR)	772 572
MX Channel/Gain (AFCG)	772 574
Maintenance (AFMR)	772 576

UNIBUS Interface

Interrupt vector address:	134
Priority level:	BR4
Bus loading:	1 bus load

Mechanical

Size:	each cabinet is 72"H x 21"W x 30"D
Weight:	750 lbs. (dual cabinet, 512 channels)

Power (per cabinet)

Input current:	15 A at 115 VAC, 40 to 440 Hz, single phase
Heat dissipation:	1700 W

Environment

Operating temperature:	10°C to 40°C
Relative humidity:	10% to 90%

ANALOG REAL-TIME MODULE, AR11**FEATURES**

- Low Cost
- Compact
- Convenient interfacing and mounting
- Capabilities include:
 - A/D converter—auto zeroing technique (patent pending)
 - 16-channel multiplexer, with sample and hold
 - Programmable clock
 - Scope display control with 2 D/A converters
 - UNIBUS interface logic

DESCRIPTION

The AR11 is a compact analog real-time subsystem for use with the PDP-11 family of computers. Included in the subsystem are a 10-bit analog/digital converter, two 10-bit digital/analog converters, a crystal controlled clock, scope control, a 16-channel multiplexer, and a sample and hold circuit. Operation and selection of functions is under software control. Programming is subset-compatible with the LPS11, Laboratory Peripheral System, which is a more comprehensive analog processing system. The LPS11 is used for the larger and more demanding laboratory applications.

A/D Converter System

The 10-bit A/D Converter samples analog data at specified rates and allows the program to store the equivalent digital value for subsequent processing. Sample and hold circuitry ensures accurate conversions, even on rapidly changing signals, by holding the input voltage constant until the process is completed. The maximum throughput rate for a single channel is approximately 35 kHz. A 16-channel single-ended multiplexer is included. The input voltage range is program selectable for unipolar (0V to +5V), or bipolar (-2.5V to +2.5V) operation.

Display Control

The display control displays data in the form of a 1024 by 1024 dot array. Under program control, a bright dot may be produced at any point in this array. A series of these dots may be programmed to produce graphical output. The display control is primarily used with DIGITAL's VR14 display. However, it has the capabilities to operate with the Tektronix 602 and 604 display scopes and the 603, 611, and 613 storage scopes. It can also drive an X-Y analog recorder. The display control offers four program-controlled modes in which the scope can intensify a point. There are two 10-bit D/A converters with either a $\pm 5V$ or a $\pm 0.5V$ full scale output and all the necessary circuitry for scope control.

Programmable Clock

The programmable clock offers several methods for accurately measuring

AR11

and counting time intervals or events. It can be used to synchronize the central processor to external events, count external events, measure intervals of time between events, or provide interrupts at programmable intervals. It can be used to start the A/D converter at predetermined intervals or from an external logic input.

The clock operates in one of two program modes: single interval or repeated interval. There are seven programmable frequencies: 1 MHz to 100 Hz, an external input, and an auxiliary input (on the backplane wiring).

An 8-bit counter can be preset for a number of time pulses or events to occur before an interrupt (or A/D counter start) is initiated. This counter can be read from the processor at any time to determine timing status.

PACKAGING

The complete AR11 subsystem electronics are contained on one single hex module that can mount in either of the two center slots of a DD11-B system unit, or within the CPU mainframe assembly. All external connections are made via a Berg connector (supplied with mating plug) which is mounted on an outside corner of the module.

No external analog supply voltages are required. A unique DC to DC converter without transformer uses the +5V logic power to generate the high-quality positive and negative voltages needed by the AR11.

PROGRAMMING

There are 8 registers used for control and data. The address of the first register is selectable in increments of 20, between 770 000 and 777 760. With a starting address of 770 400, the arrangement is:

Register	Address
A/D Status	770 400
A/D Buffer	770 402
Clock Status	770 404
Clock Buffer	770 406
Display Status	770 410
X Buffer	770 412
Y Buffer	770 414
Clock Counter	770 416

There are three interrupt vectors, with the address of the first address vector selectable in increments of 20. If the first vector is at 300, the arrangement is:

Vector	Address	Priority Level
A/D	300	BR6
Clock	304	BR6
Scope Control	310	BR4

SPECIFICATIONS

A/D Converter System

Input voltage range: 0 to +5V, or
-2.5V to +2.5V,
program selectable

BA11-K

EXPANSION MOUNTING CHASSIS, BA11-K

DESCRIPTION

The BA11-KE/KF is a general purpose PDP-11 expansion mounting chassis (10½" x 17" x 25") and mounts in standard DIGITAL cabinets. It includes the H765 power system for either 115V or 230V operation and it supplies multiple voltages which deliver 660 watts of DC power. The expansion mounting chassis also includes mounting hardware, UNIBUS cable and a pop panel. The BA11-K has been approved by the Underwriter Laboratories (UL approved).

FEATURES

- Accommodates any mix DIGITAL modules, including both quad and hex modules.
- Provides space for up to five system units or 22 module slots.

Physical Characteristics

Chassis Size: 10.5 x 17 x 26.5 inches

Weight (unloaded/loaded):
90/115 lbs

Rack Slides (3-position):
horizontal, 45° & 90°

Configuration Expansion:
5 SU or 22 module slots (2 double SU and 1 single SU)

Environmental Characteristics

Air Inlet Temp: 41°F–122°F
(5°C–50°C)

Cooling Efficiency: temperature rise no greater than 18°F (10°C) from inlet air to exhausted air

Operating Humidity: 10-95% (no condensation)

Air Flow Direction: horizontally towards rear of box; air is drawn through filtered front pop panel and from within rack

Multiple Voltages:

(2) H744 regulators	+ 5V @ 25 amps (each)
(1) H745 regulator	–15V @ 10 amps
(1) H754 regulator	+20V @ 8 amps
	– 5V @ 1.1 amps*
(1) 54-11086 regulator	+15V @ 4 amps

BA11-K Input Power Specifications

Voltage: 90-132 (180-264) Vac, 47-63 Hz, single phase 115 (230) Vac nominal

sustained operation: 104-132 (208-264) Vac

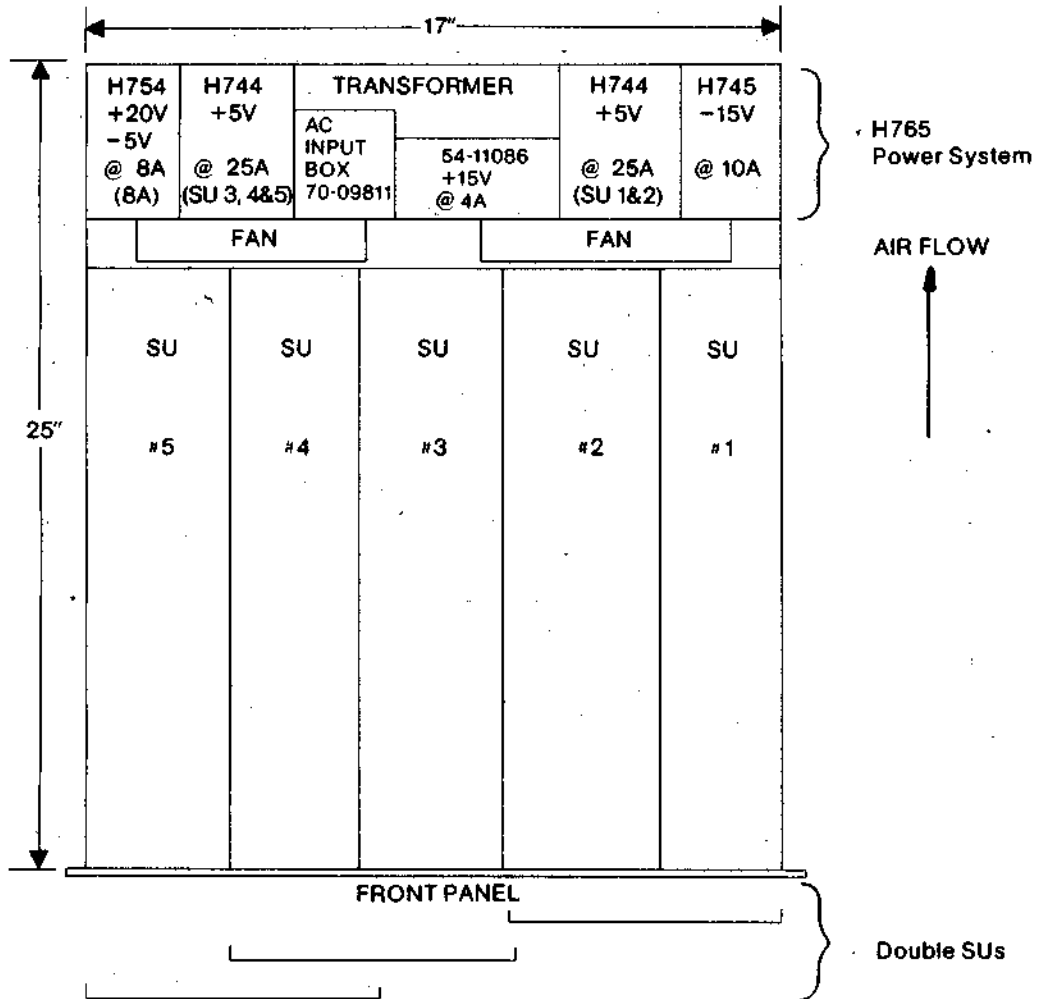
Power: 1200 maximum at 115/230 Vac nominal line (1380 VA)

Current: 12/6 amp AC maximum at 115/230 Vac nominal line

* Maximum –5V current is dependent upon +20V current. It is equal to 1 A plus the current of the +20V supply, up to a total of 8 A.

BA11-K

BA11-K—TOP VIEW



NOTES

1. Double-system units can be mounted in any two slots except two and three.
2. The two H744 regulators are individually dedicated and their outputs cannot be paralleled. Regulator #1 provides power to SU 1 & 2. Regulator #2 provides power to SU 3, 4 & 5.

BB11

BLANK MOUNTING PANEL, BB11

The BB11 Blank Mounting Panel is a prewired System Unit (SU) designed for general interfacing. It is prewired only for the UNIBUS and power. The unit contains three 288-pin blocks assembled end-to-end in a casting which can be mounted in the various PDP-11 assembly units. Bus and power connectors, described below, use only 6 of the module slots, thereby leaving 18 slots available for customer use.

The BB11 is wired to accept the UNIBUS in slots A1 and B1. This connection can be made with an M920 UNIBUS Connector or a BC11A UNIBUS Cable Assembly. All bus signals, including grant signals, are wired directly to corresponding pins in slots A4 and B4. From this point, the UNIBUS can be continued to the next unit by using an M920 or BC11A. If the BB11 is the last unit on the bus, slot A4-B4 accepts the M930 Bus Terminator Module. Standard bus pin names are listed in Appendix B.

The bus grant signals are wired through the BB11. These grant signal wires must be removed and replaced with wires to and from the user's control circuits for the grant levels used by the customer-supplied device.

Slot A3 accepts the G772 Power Connector (furnished as part of the BA11 Mounting Box). Power for + 5V is distributed to all A2 pins; - 15V is distributed to all B2 pins except in slots A1, B1, A4, and B4; and ground is maintained through the frame and power connector on pins C2 and T1 of all slots.

	A	B	C	D	E	F
4	UNIBUS CONN					
3	POWER					
2	RESERVED					
1	UNIBUS CONN					

BB11 Module Layout

**BM792
MR11
M792**

READ ONLY MEMORY (ROM)

Read only memory is available in 32 word increments, and a total of 256 words of ROM can be included in a PDP-11 system. ROM's can be programmed by the user; standard preprogrammed ROM's are offered as bootstrap loaders for various peripheral devices. Access time is 100 nsec per word.

Programmable ROM (M792)

The basic ROM module contains 32 16-bit words of diode read-only memory. The ROM is supplied with a 32 by 16 diode matrix. Diodes can be selectively cut out to yield the desired data pattern; diode in = 1, no diode = 0. The unprogrammed ROM contains all 1's; programming of the memory is accomplished by eliminating diodes for the bits that should be read as 0's. The location of the diodes with respect to word and bit number are indicated on the module.

Addresses

The 32 words are in consecutive memory addresses. The address range of the lowest address is jumper selectable between 773 000 and 773 700. The jumper wires affect bits 6 to 8 of the address, and are indicated on the module by the designations W1, W2, and W3.

Bit 8 (W3)	Bit 7 (W2)	Bit 6 (W1)	Address Range
0	0	0	773 000 to 773 076
0	0	1	773 100 to 773 176
0	1	0	773 200 to 773 276
0	1	1	773 300 to 773 376
1	0	0	773 400 to 773 476
1	0	1	773 500 to 773 576
1	1	0	773 600 to 773 676
1	1	1	773 700 to 773 776

To make the jumpers correspond to the desired bit addresses, jumper in = 0, no jumper = 1.

A maximum of 8 ROM modules can fit into the address space allotted, so that a small read-only memory of 256 words can be used. Such a memory could provide non-erasable recovery routines, or lowered program execution times for often-used loops or subroutines.

Bootstrap loaders (BM792-Y)

Several basic M792 modules are preprogrammed (diodes selectively eliminated) as bootstrap loaders for convenient loading of initial programs to handle various I/O and peripheral devices.

An M792 ROM module mounts in one Small Peripheral Controller (SPC) slot. The module is quad height.

BM792

READ ONLY MEMORY (M792) SPECIFICATIONS

Access time: 100 nsec
Memory size: 32 words, 16 bits each
UNIBUS loading: 1 bus load
Mounting space: 1 SPC slot (quad module)
Current requirements: 0.3 A at + 5V

Model No.	Address Range	Description
M792	773 000 to 773 776	Basic unit with all diodes included (contents are all 1's). Diodes are selectively removed to make 0's.
BM792-YA	773 000 to 773 076	Papertape bootstrap loader for Teletype or high-speed paper tape reader (PC11).
BM792-YB	773 100 to 773 176	Disk/DEctape bootstrap loader.
BM792-YC	773 200 to 773 276	Card Reader bootstrap loader (CR11)
BM792-YH	773 300 to 773 376	Cassette bootstrap loader (TA11)
MR11-DB	773 100 to 773 276	Bootstrap loader for mass storage devices.

Device	Starting Address
RF11	773 100
RK11	773 110
TC11	773 120
TM11	773 136
RP11	773 154
RC11	773 220

The MR11-DB consists of 2 preprogrammed M792 modules.

RESTART/LOADER, BM873**FEATURES**

- General-purpose program loader for all PDP-11 Systems.
- Can be connected to switches, pushbuttons or other external activating devices such as watchdog timers to initiate program load.
- Contains bootstrap loaders for the most frequently used PDP-11 devices.
- One version can be used in conjunction with an M792 diode ROM to load from user's special device.
- One version has a unit-select feature which permits the bootstrap to operate from any drive of some multi-drive controllers.
- One version supports down-line loading.

DESCRIPTION

The BM873 is a general-purpose loader which permits quick loading of bootstrap programs or restarting of PDP-11 programs for such devices as paper tape readers, disks, magnetic tape, DECTape, cassette tape, or communications lines. The general-purpose loader consists of one circuit board and will fit in a standard PDP-11 small peripheral controller (SPC) slot. There are three versions available. The BM873-YA version contains bootstraps for several devices. In addition, it can be used in conjunction with an M792 diode ROM to load from some user-specified device not in the ROM of the BM873-YA. The BM873-YA contains bootstrap loader programs within a 128-word read-only memory (ROM).

The BM873-YB version bootstraps for all the devices in the BM873-YA plus bootstraps for the RJP04, RJS03, RJS04, and TJU16. In addition, it has a unit-select feature that permits bootstrapping from any drive on the RK11-D, RJS03, RJS04, RJP04 RP11, and TA11 Cassette. The bootstrap programs are contained in a 256-word read-only memory (ROM).

The BM873-YC version contains bootstraps for all the devices in the BM873-YA plus a bootstrap for down-line loading a system over a synchronous communication link using the DU11 interface. Messages transmitted on the synchronous link must conform to DECnet protocols. Operation is point to point, private wire or switched. The bootstrap programs are contained in a 256 word read-only memory (ROM).

The H324 pushbutton panel is available as an option to the BM873. It contains four pushbuttons to select any one of four devices from which the user may bootstrap. Bootstrapping is initiated simply by pushing the button selected along with an interlock button which prevents accidental operation.

LOADING PROGRAM

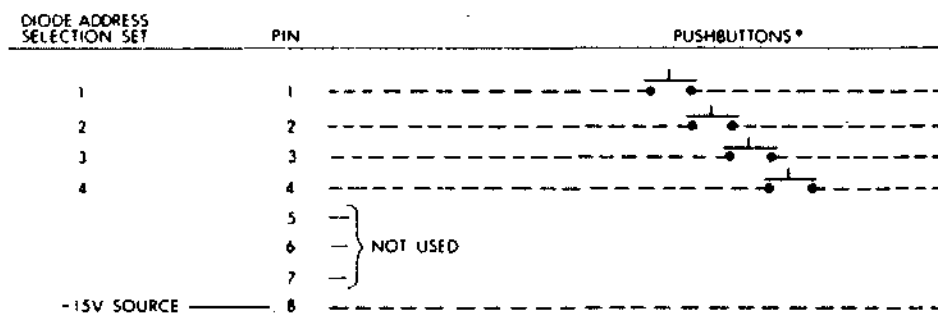
There are several methods available for loading programs with the BM873: via the PDP-11 program console, by a JMP instruction in the program, or by an external contact closure or voltage level. Four sets of

BM873

eight diodes are cut to select the address of the bootstrap programs. These diodes are used with the external sources.

An 8-pin Mate-N-Lok connector is provided for users who wish to install their own external mechanisms or the H324 pushbutton panel. The diagram shows how external devices are connected as well as the relationship of each external input to the set of diodes used to select the start address of the proper bootstrap program.

MATE-N-LOK CONNECTOR



* Pushbuttons are not included with the BM873 Module. They are installed at the discretion of the user.

SPECIFICATIONS

Mounting

1 SPC slot (quad module)

Programs Included

The BM873-YA, BM873-YB, and BM873-YC contain programs for RF11 Disk, RK11 Disk, TC11 DEctape, TM11 Magtape, RP11 Disk, RC11 Disk, ASR Paper-Tape Reader, TA11 Cassette, and PC11 High Speed Reader.

The BM873-YB also contains programs for the RJP04 Disk, RJS03 Disk, RJS04 Disk, and TJU16 Magtape.

The BM873-YC also contains a program for down-line load using the DU11 Synchronous Interface.

Power

1 A at +5V

2 mA at -15V

ROM Cycle Time

500 ns

Restart Address

User-selectable via diodes (four sets of eight diodes for each of the four inputs). Address range covers entire ROM area and can call special programs in other ROMs (BM792). The diodes select the XXX part of the address 773XXX.

BM873

External Interface Connection

8-pin Mate-N-Lok connector on the module.

UNIBUS Loading

1 bus load

Models

BM873-YA—Restart/Loader with ROM programs to load from paper tape, disks, magnetic tape, DECtape, and cassettes, or special user devices.

BM873-YB—Restart/Loader with ROM programs to load from paper tape, disks, Magnetic tape, DECtape, and cassettes with unit select feature for some disks and the cassette.

BM873-YC—Restart/Loader with ROM programs to load from synchronous communications link, paper tape, disks, magnetic tape, DECtape, and cassettes.

H324—Pushbutton Panel. Option for any BM873 version to provide single pushbutton operations for bootstrapping. Mounts in place of any 5¼ inch pop panel. Includes cable and Mate-N-Lok connector to connect to BM873 connector. No power required.

PROGRAMMING

No programming is required. If a special device is required, use the M792 in conjunction with the BM873-YA. If bootstrapping is to be done from the console of the PDP-11, the load addresses for the various devices are as follows:

FOR BM873-YA

ADDRESS	Device Type (Controller)
773000	RF11
773010	RK11
773020	Transfer to address contained in Switch Register
773030	TC11
773050	TM11
773100	RP11
773144	RC11
773210	Teletype Paper Tape Reader
773230	TA11
773312	PC11

If a BM792 is used for a special device not in the list above, its jumpers should be cut for address ranges 773400-773776.

FOR BM873-YB

ADDRESS	Device Type (Controller)
773000	RJS03/RJS04 Disk Unit 0
773002	RJS03/RJS04 Unit specified in console switch register
773030	RK11 Disk Unit 0

BM873

FOR BM873-YB ADDRESS

Device Type (Controller)

773032	RK11	Unit specified in console switch register
773070	TC11	
773110	TM11	
773136	RF11	
773150	TJU16	
773212	RC11	
773320	RJP04	Disk Unit 0
773322	RJP04	Unit specified in console switch register
773344	Transfer to address in console switch register	
773350	RP11	Disk Unit 0
773352	RP11	Unit specified in console switch register
773510	KL11/DL11	Console TTY Reader
773524	TA11	Cassette Unit 0
773526	TA11	Unit specified in console switch register
773620	PC11	

FOR BM873-YC

ADDRESS

Device Type (Controller)

773000	RF11	
773010	RK11	
773020	Transfer to address contained in Switch Register	
773030	TC11	
773050	TM11	
773100	RP11	
773144	RC11	
773210	ASR paper tape reader	
773230	TA11	
773312	PC11	
773400	DU11	

HIGH-SPEED PUNCHED CARD READER, CD11**DESCRIPTION**

The CD11 is a high-speed Card Reader that can process punched cards at up to 1200 cards/minute. There are two versions: a tabletop unit with an input hopper capacity of 1000 cards that operates at 1000 cards/minute; and a free-standing floor model with a large 2250-card hopper that has a speed of 1200 cards/minute. The Control Unit is a set of modules mounted in a System Unit (SU) assembly.

The CD11 Card Readers access the PDP-11 UNIBUS from the interrupt and non-processor request (NPR) modes of operation. Control and status information is relayed in the interrupt mode. Data is transferred through direct memory access (NPR):

Reader design helps prevent card jams and keeps card wear to a minimum. Readers also have a high tolerance to cards that have been nicked, warped, bent or subjected to high humidity.

To keep cards from sticking together, the readers use a special "riffle air" feature. The bottom half inch of cards in the input hopper is subjected to a stream of air which separates the cards and air cushions them from the deck and from each other.

Cards entering the reader are selected through a vacuum picker. The picker and its associated throat block prevent the unit from accepting cards that have been stapled or taped together (unless such taping is on the leading edge). Because the card track is very short, only one card is in motion at any time. This minimizes the chances of cards jamming. Stoppages are also reduced since the reader automatically makes six attempts to process a card before rejecting it.

The read station uses infrared light-emitting diodes (LEDs) as its light source and phototransistors as its sensors. No adjustments are required during the ten-year life expectancy of the diodes.

Because card reader operation is flexible, cards can be loaded and unloaded while the reader is operating. A switch may be set to provide system blower shutdown or continual running after the last card has been read. Automatic shutdown reduces computer room noise level, and indicates that the card hopper is empty.

A control unit is included with the card reader.

DATA FORMATS

The reader is designed to look, sequentially, for data in 80 columns, starting with column number 1. Each column has 12 zones, or rows. A hole (or a mark) is interpreted as a binary ONE, and the absence of a hole (or no mark) as a binary ZERO. Data is read from the card one column at a time. There are two data formats for input to the computer.

Non-Compressed Mode—A separate bit in the data register is used to

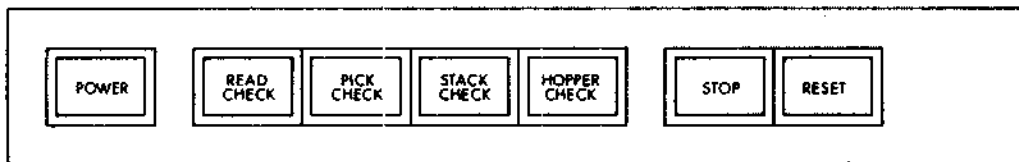
CD11

record the state of each card zone. The 12-zone bits correspond to 12 bits in the PDP-11 word (which has 16 bits).

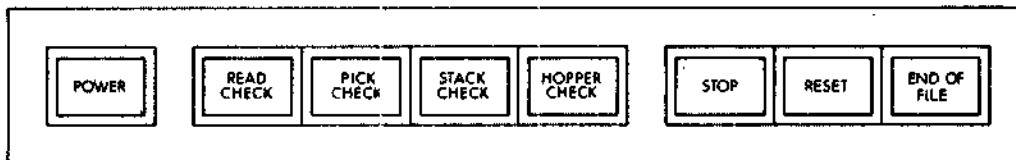
Compressed Mode—The 12-zone bits are encoded into 8 bits, to fit in a PDP-11 byte (8 bits). More efficient data storage is achieved in this mode. All present Hollerith Codes (the standard used for 12-zone card data), and the proposed expansion of the Code can be accommodated with the compressed format utilized.

The CD11 has 4 registers: Status, Column Count, Bus Address, and Data. A bit within the Status Register is set or cleared under program control to cause the Data Register to hold either the non-compressed or compressed format.

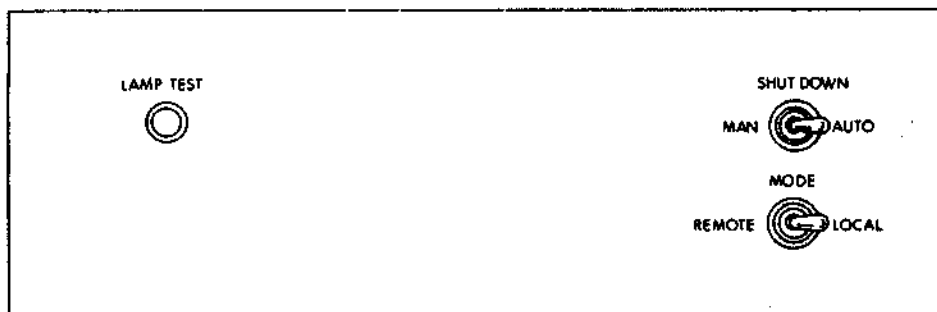
CONTROLS & INDICATORS



a. Front Control Panel—(CD11-A)



b. Front Control Panel—(CD11-E)



c. Rear Control Panel—Both Models

Front Panel Controls and Indicators

Control or Indicator	Type	Function
POWER switch	alternate-action pushbutton/indicator switch	<p>Controls application of all power to the card reader.</p> <p>When indicator is off, depressing switch applies power to reader and causes associated indicator to light.</p> <p>When indicator is lit, depressing switch removes all power from reader and causes indicator to go out.</p>
READ CHECK indicator	white light	<p>When lit, this light indicates that the card just read may be torn on the leading or trailing edges, or that the card may have punches in 0 or 81st column positions.</p> <p>Because READ CHECK indicates an error condition, whenever this indicator is lit, it causes the card reader to stop operation and extinguishes the RESET indicator.</p>
PICK CHECK indicator	white light	<p>When lit, this light indicates that the card reader failed to move a card into the read station after it received a READ command from the controller.</p> <p>Stops card reader operation and extinguishes RESET indicator.</p>
STACK CHECK indicator	white light	<p>When lit, this light indicates that the previous card was not properly seated in the output stacker and, therefore, may be badly mutilated.</p> <p>Stops card reader operation and extinguishes RESET indicator.</p>
HOPPER CHECK indicator	white light	<p>When lit, this light indicates that either the input hopper is empty or the output stacker is full.</p> <p>In either case, the operator must manually correct the condition before card reader operation can continue.</p>

Front Panel Controls and Indicators (cont.)

Control or Indicator	Type	Function
STOP switch	momentary pushbutton/indicator switch (red light)	<p>When depressed, immediately lights and drops the READY line, thereby extinguishing the RESET indicator. Card reader operation then stops as soon as the card currently in the read station has been read.</p> <p>This switch has no effect on system power; it only stops the current operation.</p>
RESET switch	momentary pushbutton/indicator switch (green light)	<p>When depressed and released, clears all error flip-flops and initializes card reader logic. Associated RESET indicator lights to indicate that the READY signal is applied to the controller.</p> <p>The RESET indicator goes out whenever the STOP switch is depressed or whenever an error indicator lights (READ CHECK, PICK CHECK, STACK CHECK, or HOPPER CHECK).</p>
END OF FILE switch	momentary pushbutton/indicator switch	<p>This switch is used as a programming aid to inform the user when an end-of-file has been reached.</p> <p>As an example, assume that a particular file greatly exceeds the input hopper capacity. The hopper is loaded to capacity, the card reader operated until a HOPPER CHECK indication occurs, and the hopper is loaded with more cards. When the last group of cards is loaded, the user can then depress END OF FILE. As soon as the last card in this group is read, an END OF FILE bit in the controller is set. This END OF FILE bit can then be read by the program at any time.</p> <p>Whenever the END OF FILE pushbutton is depressed, the card reader functions in a normal manner until</p>

Front Panel Controls and Indicators (cont.)

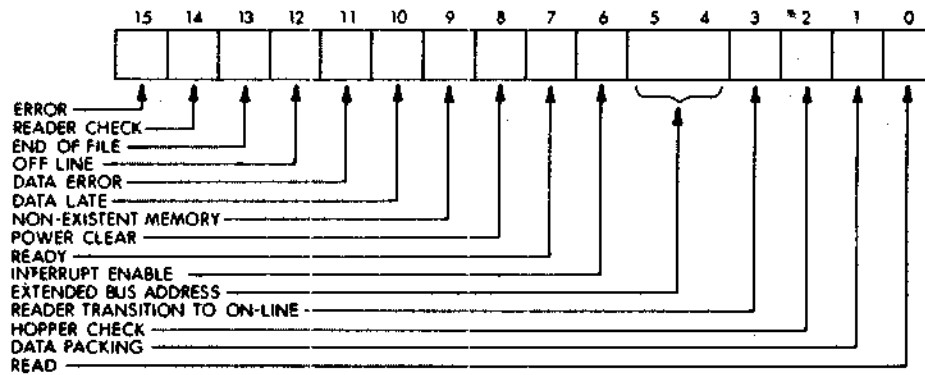
Control or Indicator	Type	Function
		<p>the input hopper is empty (the last card has been read). As soon as this occurs, the card reader HOPPER CHECK indicator comes on and the controller END OF FILE bit is set.</p> <p>Note that the END OF FILE can be depressed at any time but the END OF FILE signal is not sent to the controller until the last card has been completely read.</p>

Rear Panel Controls

Control	Type	Function
LAMP TEST switch	pushbutton	When depressed, illuminates all indicators on the front control panel to determine if any of the indicator lamps are faulty.
SHUTDOWN switch	2-position toggle	<p>Controls automatic operation of the input hopper blower.</p> <p>MAN position—blower operates continuously whether or not cards are in the input hopper.</p> <p>AUTO position—causes the blower to shut down automatically whenever the input hopper is emptied. Blower automatically restarts when cards are loaded into the hopper and the RESET switch is depressed.</p> <p>Blower activates approximately 3 sec after RESET is depressed.</p>
MODE switch	2-position toggle	<p>Permits selection of either on-line or off-line operation.</p> <p>LOCAL position—removes the READ command input from the controller to allow the operator to run the reader off-line by using the RESET and STOP switches on the front control panel.</p> <p>REMOTE position—enables the READ command input from the controller to allow normal on-line operation under program control once RESET is depressed.</p>

REGISTERS

Status and Control Register (CDST) 772 460



Effect of the Initialize (INIT) signal: clear bits 15 to 13, 11 to 9, 6 to 3, 1, and 0.

Read only: bits 15 through 9, 7, 3, and 2

Write only: bits 8 and 0

BIT	NAME	FUNCTION
15	Error (ERR)	<p>Set to indicate an error condition that is the inclusive OR of all error conditions (bits 14-09 in this register).</p> <p>If the error condition is due to bit 11, 10, or 9, the Error bit does not set until the Busy signal from the Card Reader is cleared. This permits the entire card to pass through the read station before an interrupt occurs.</p>
14	Reader Check	<p>Set when an abnormal condition exists in the card reader. Any one of the following four conditions sets this bit:</p> <ol style="list-style-type: none"> Hopper Check—input hopper is empty or the output stacker is full. This error indication occurs after column 80 of the last card has been read. Pick Check—feed mechanism failed to deliver a card to the read station when demanded. This error condition occurs if a card is not delivered within 400 ms after a Read command is initiated. Stack Check—previous card was not properly seated in the output stacker and, therefore, may be badly damaged.

CD11

BIT	NAME	FUNCTION
		<p>d. Read Check—read station electronics do not agree with the usual light and dark areas of the card. This could be caused by torn cards or cards with illegal punches (holes in 0 or 81st column positions).</p> <p>Error-causing condition should be corrected before clearing this bit.</p>
13	End of File (EOF)	<p>Used with CD11-E only. Associated with the END OF FILE pushbutton on that reader.</p> <p>The END OF FILE pushbutton is used as a programming aid to allow the user to insert an END OF FILE flag at the appropriate place in the program.</p> <p>When the last group of cards in a specific file has been loaded into the hopper, the user can then depress the END OF FILE switch. When the switch is depressed, the card reader functions in a normal manner until the input hopper is empty and the last card is read. At this time, the card reader HOPPER CHECK indicator light comes on and the controller END OF FILE bit (bit 13) is set. Because a hopper-empty condition is considered an error, the status register Reader Check, Hopper Check, and Error bits are also set.</p> <p>When a CD11-A is used, bit 13 is always clear.</p>
12	Off Line	<p>Set when the reader is off-line. When clear, the reader is on-line, under program control, and ready to accept a Read command.</p> <p>Depressing the card reader RESET switch brings the reader on-line, provided no error conditions exist and the reader MODE switch is in the REMOTE position.</p> <p>The card reader goes off-line (setting bit 12) whenever an error condition is sensed (STOP light on reader is lit), whenever the reader STOP pushbutton is depressed, or whenever the MODE switch is set to the LOCAL position.</p>
11	Data Error	<p>When the controller is in the packing mode of operation (bit 1 set), the normal 12-bit code is compressed into an 8-bit code that allows a column to be transferred as a single byte. When this compressed code is used, card zones 1-7</p>

CD11

BIT	NAME	FUNCTION
		are represented by an octal code; therefore, no more than one zone should be at 1 at any given time.
		Set in the packing mode whenever more than one of zones 1-7 are a 1.
		When bit 11 sets, it does not inhibit further transfer of data into memory.
10	Data Late	<p>Set when NPR request is not granted during the time that data is guaranteed valid from the Card Reader.</p> <p>This bit prevents further NPR requests from occurring, thereby preventing clocking of the column-count register (CDCC) and current address register (CDBA).</p>
9	Non-Existent Memory	<p>If the controller is engaged in an NPR data transfer and attempts to access a memory address that does not exist, bit 9 sets to provide an NXM error indication. This NXM error occurs if the controller does not receive Ssyn within a specified time after it has issued MSYN.</p> <p>When set, this bit inhibits further NPR requests.</p>
8	Power Clear (PWR CLR)	Set to clear the column-count register (CDCC), the current address register (CDBA), and all bits in the status register (CDST) with the exception of bits 12, 7, and 2.
7	Ready (RDY)	<p>Set when the CD11 is ready to receive a new command.</p> <p>This bit is set by one of the following conditions:</p> <ol style="list-style-type: none">Error bit set—an error condition exists and the program should branch to an error-handling routine.Power Clear bit set—all controller logic has been cleared and the controller can engage in a data transfer.INIT signal occurs—same as POWER CLEAR.Busy clear and CDCC overflow—the preset number of data transfers has been performed and the controller is now ready for a new Read command.

BIT	NAME	FUNCTION
6	Interrupt Enable (INT ENB)	Set to allow either Ready or Reader Transition to On Line = 1 to cause an interrupt.
5-4	Extended Bus Address (XBA17, XBA16)	Used to specify bus address lines 17 and 16 in direct memory transfers. Increment with the current address register (CDBA). Bit 5 corresponds to XBA17, bit 4 to XBA16.
3	Reader Transition to On Line (ON LINE TRANS)	Set when the card reader has gone on-line and is under program control. Depressing the card reader RESET switch brings the reader on-line, provided no error conditions exist and the reader MODE switch is in REMOTE. The card reader goes off-line whenever an error condition is sensed or when the STOP switch is depressed.
NOTE The READER TRANSITION TO ON-LINE bit does not clear when the reader goes off-line.		
2	Hopper Check	Set to indicate that either the input hopper is empty or the output stacker is full. The bit will set Reader Check (bit 14). The bit is cleared by correcting the condition that caused the error. Because the bit is controlled by the HOPPER CHECK signal from the card reader, it will not be cleared by Power Clear.
1	Data Packing	Determines whether the data is to be loaded as a 12-bit word or as a 8-bit byte; 0 = 12-bit word, 1 = 8-bit byte.
NOTE This bit has no effect on data read from the processor.		
0	Read	Set to cause the card reader feed mechanism to deliver one card to the read station for reading. When set, the bit clears the following bits in the status register: 15, 14, 11, 10, 9, 7, and 3. The bit also clears Error (bit 15), provided Hopper Check (bit 2) is clear. If the Read bit is set when the Card Reader is busy, it will reset bits 15 and 2. Error is set to indicate that a Read command was issued when the card reader was not available for use.

Column Count Register (CDCC) 772 462

BIT	NAME	FUNCTION
15-0	Column Count	Contains the 2's complement of the number of columns to be transferred to memory when cards are being read.

The column-count register is loaded prior to initiation of the read function. The register is incremented by 1 after each transfer. When the contents of the register equal all 0s, further transfers are inhibited until another READ command occurs.

If an entire 80-column card is read and the column-count register has still not advanced to 0, then the next card is automatically fed to the read station.

All bits may be loaded or read by the program. Cleared by POWER CLEAR (bit 8 in the status register set) or by INIT.

NOTE

The column-count register should not be modified by using byte instructions. Use only word instructions when loading this register. The register is wired in such a manner that the entire word is loaded even if a byte instruction is used. Therefore, if the programmer attempts to load only the low-order byte, for example, the data on the high-order data lines is also loaded. This latter data may be useless and/or unknown to the programmer.

Whenever the column-count register reaches 0, an interrupt is initiated if INT ENB is set to inform the processor that the desired number of columns has been transferred.

Current Address Register (CDBA) 772 464

BIT	NAME	FUNCTION
15-0	Address	These bits specify the bus or memory address into which the next column of data is to be stored.

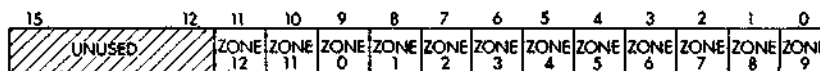
The current address register is initially set to the memory location of the first column to be read. It then increments by 1 for transfers in the packing mode (byte transfers) and increments by 2 for transfers in the non-packing mode

BIT	NAME	FUNCTION
		(word transfers). Incrementation occurs immediately after each data transfer.
		The bits in this register are used in conjunction with extended address bits A17 and A16 (bits 5 and 4, respectively, in the status register) so that 18-bit memory addresses may be used.
		Note that the extended address bits participate in the incrementation; they are a logical extension to this register.
		The current address register is loaded prior to issuing a READ command. The register may be loaded or read by the program.
		Cleared by POWER CLEAR (bit 08 in the status register set) or by INIT.

NOTE

The current address register should not be modified by using byte instructions. Use only word instructions when loading this register.

Data Buffer Register—Non-Packing Mode (CDDB) 772 466

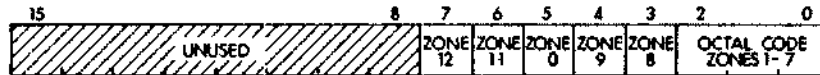


BIT	NAME	FUNCTION
11-0	Zone	These bits represent the output of a 12-bit data buffer register. When the register is in a non-packing mode (bit 01 in the status register is clear), data from a card is loaded into this buffer one column at a time on a word basis. After each column is loaded, the contents of the buffer is placed on the Unibus for transfer to the processor, memory, or other bus device.
		The contents of the buffer is coupled to the 12 least-significant bus data lines as shown below:

Bit	Corresponding Card Image
11	ZONE 12
10	ZONE 11
9-0	ZONES 0-9, respectively

Bits 11-0 are read as 1s whenever a card is not being read; bits 15-12 are always read as 0s.

Data Buffer Register—Packing Mode (CDDB) 772 466.



BIT	NAME	FUNCTION
7-0	Zone	<p>These bits also represent the output of the data buffer register. During a read operation, data from a card is loaded into this buffer one column at a time. After each column is loaded, the contents of the 12-bit buffer are compressed into an 8-bit character by an encoding network and are then gated onto the UNIBUS as a low-order byte. This data compression is made available so that the card reader controller is fully compatible with the proposed expansion of the Hollerith code.</p>

Bits 7 through 3 are encoded as follows:

Bit	Corresponding Card Image
7	ZONE 12
6	ZONE 11
5	ZONE 0
4	ZONE 9
3	ZONE 8

Bits 2 through 0 represent an octal code that defines the card zone as shown below. In the case of multiple zones, these bits are the inclusive OR of the octal codes of the zones.

Bit 02	Bit 01	Bit 00	Card Zone
0	0	0	zero, ZONES 1-7
0	0	1	ZONE 1
0	1	0	ZONE 2
0	1	1	ZONE 3
1	0	0	ZONE 4
1	0	1	ZONE 5
1	1	0	ZONE 6
1	1	1	ZONE 7

All bits are read-only bits with the same conditions as described previously.

CD11

SPECIFICATIONS	CD11-A	CD11-E (when different)
Main Specifications		
Input medium:	80-column punched cards, 12 zones (or rows)	
Speed:	1000 cards/minute	1200 cards/min
Hopper capacity:	1000 cards	2250 cards
Register Addresses		
Status and Control	(CDST)	777 160
Column Count	(CDCC)	777 162
Current Address	(CDBA)	777 164
Data	(CDDB)	777 166
UNIBUS Interface		
Interrupt vector address:	230	
Priority level:	BR4	
Data transfer:	NPR	
Bus loading:	1 bus load	
Mechanical		
Mounting:	1 table top unit + 1 system unit (SU)	1 free-standing unit +1 SU
Size:	14"H x 24"W x 18"D	38" x 24" x 38"
Weight:	85 lbs.	200 lbs.
Power		
Running current:	6A at 115 VAC	10A
Starting current:	15A at 115 VAC	22A
Current for control:	2.5A at +5V	
Heat dissipation:	600 W	1150 W
Environment		
Operating temperature:	15°C to 32°C	
Relative humidity:	20% to 80%	

Models

CD11-A: Card reader and control, 1000 cards/min, 115 VAC, 60 Hz

CD11-B: Card reader and control, 1000 cards/min, 230 VAC, 50 Hz

CD11-EA: Card reader and control, 1200 cards/min, 115 VAC, 60 Hz

CD11-EB: Card reader and control, 1200 cards/min, 230 VAC, 50 Hz

**PUNCHED CARD READER, CR11
AND MARK SENSE CARD READER, CM11-F**

DESCRIPTION

The CR11 Card Reader reads EIA standard 80-column punched data cards; the CM11-F reads 80-column mark-sense cards, which can have punched holes, at 285 cards per minute. The CR11 and CM11 are mechanically and electrically similar.

The CM11 can read cards marked with ordinary pencil or pen; it can also read punched holes. Intermixing of punched holes and mark sense can occur within the same batch of cards and even within the same card. Although the CM11 can read up to 80 columns of marked data, it is often better to use a maximum density of 40 columns, since it is difficult to confine the marking within a narrow area. The vertical spacing of the columns of data is flexible and is determined by the customer. The CM11 Reader does not look for data at predetermined distances along the card; it looks for timing tracks (dark marks) along the bottom edge of the card. These marks are used to indicate to the Reader that column data is to be read.

Cards that can be used with the CR11 and CD11 can also be used with the CM11, but only if they have the timing marks. The CR11 and CM11 Readers are suitable for placing on top of a table. The Control Unit is a quad module that mounts in a Small Peripheral Controller (SPC) slot.

Reader design helps prevent card jams and keeps card wear to a minimum. Readers also have a high tolerance to cards that have been nicked, warped, bent or subjected to high humidity.

To keep cards from sticking together, the readers use a special "riffle air" feature. The bottom half inch of cards in the input hopper is subjected to a stream of air which separates the cards and air cushions them from the deck and from each other.

Cards entering the reader are selected through a vacuum picker. The picker and its associated throat block prevent the unit from accepting cards that have been stapled or taped together (unless such taping is on the leading edge). Because the card track is very short, only one card is in motion at any time. This minimizes the chances of cards jamming. Stoppages are also reduced since the reader automatically makes six attempts to process a card before rejecting it.

The read station uses infrared light-emitting diodes (LEDs) as its light source and phototransistors as its sensors. No adjustments are required during the ten-year life expectancy of the diodes.

Because card reader operation is flexible, cards can be loaded and unloaded while the reader is operating. A switch may be set to provide system blower shutdown or continual running after the last card has been

CR11 CM11

read. Automatic shutdown reduces computer room noise level, and indicates that the card hopper is empty.

A control unit is included with the card reader.

DATA FORMATS

The readers are designed to look, sequentially, for data in 80 columns, starting with column number 1. Each column has 12 zones, or rows. A hole (or a mark) is interpreted as a binary ONE, and the absence of a hole (or no mark) as a binary ZERO. Data is read from the card one column at a time. There are two data formats for input to the computer.

Non-Compressed Mode—A separate bit in the data register is used to record the state of each card zone. The 12-zone bits correspond to 12 bits in the PDP-11 word (which has 16 bits).

Compressed Mode—The 12-zone bits are encoded into 8 bits, to fit in a PDP-11 byte (8 bits). More efficient data storage is achieved in this mode. All present Hollerith Codes (the standard used for 12-zone card data), and the proposed expansion of the Code can be accommodated with the compressed format utilized.

The CR11 and CM11 have 3 registers for communicating with the computer (and the UNIBUS). There is a Status Register and 2 Data Buffers. One of the Data Buffers contains the card data in the non-compressed (12-bit) format, the other has the data in compressed (8-bit) format. Selection of formats is made simply by addressing the appropriate register. The data is always available in both formats.

CONTROLS & INDICATORS

Front Panel

Control or Indicator	Type	Function
POWER switch	alternate-action pushbutton/indicator switch	<p>Controls application of all power to the card reader.</p> <p>When indicator is off, depressing switch applies power to reader and causes associated indicator to light.</p> <p>When indicator is lit, depressing switch removes all power from reader and causes indicator to go out.</p>
READ CHECK indicator	white light	<p>When lit, this light indicates that the card just read may be torn on the leading or trailing edges, or that the card may have punches in the 0 or 81st column positions.</p> <p>Because READ CHECK indicates an error condition, whenever this indicator is lit, it causes the card reader to stop operation and extinguishes the RESET indicator.</p>
PICK CHECK indicator	white light	<p>When lit, this light indicates that the card reader failed to move a card into the read station after it received a READ COMMAND from the controller.</p> <p>Stops card reader operation and extinguishes RESET indicator.</p>
STACK CHECK indicator	white light	<p>When lit, this light indicates that the previous card was not properly seated in the output stacker and therefore may be badly mutilated.</p> <p>Stops card reader operation and extinguishes RESET indicator.</p>
HOPPER CHECK indicator	white light	<p>When lit, this light indicates that either the input hopper is empty or that the output stacker is full.</p>

**CR11
CM11**

In either case, the operator must manually correct the condition before card reader operation can continue.

STOP switch	momentary pushbutton/indicator switch (red light)	<p>When depressed, immediately lights and drops the READY line, thereby extinguishing the RESET indicator. Card reader operation then stops as soon as the card currently in the read station has been read.</p> <p>This switch has no effect on the system power; it only stops the current operation.</p>
RESET switch	momentary pushbutton/indicator switch (green light)	<p>When depressed and released, clears all error flip-flops and initializes card reader logic. Associated RESET indicator lights to indicate that the READY signal is applied to the controller.</p> <p>The RESET indicator goes out whenever the STOP switch is depressed or whenever an error indicator lights (READ CHECK, PICK CHECK, STACK CHECK, or HOPPER CHECK).</p>

Rear Panel

Control	Type	Function
LAMP TEST switch	pushbutton	When depressed, illuminates all indicators on the front control panel to determine if any of the indicator lamps are faulty.
SHUTDOWN switch	2-position toggle	<p>Controls automatic operation of the input hopper blower.</p> <p>MAN position—blower operates continuously whether or not cards are in the input hopper.</p> <p>AUTO position—causes the blower to shut down automatically whenever the input hopper is emptied. Blower automatically restarts when</p>

CR11 CM11

cards are loaded into the hopper and the RESET switch is depressed.

Blower activates approximately three seconds after RESET is depressed.

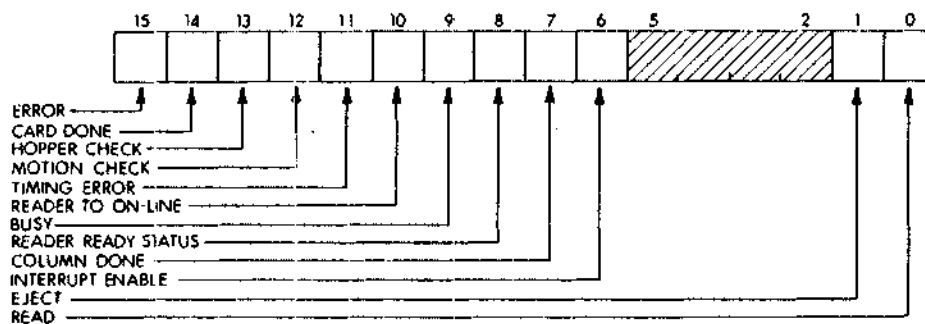
MODE switch 2-position toggle Permits selection of either on-line or off-line operation.

LOCAL position—removes the READ COMMAND input from the controller to allow the operator to run the reader off-line by using the RESET and STOP switches on the front control panel.

REMOTE position—enables the READ COMMAND input from the controller to allow normal on-line operation under program control once RESET is depressed.

REGISTERS

Card Reader Status Register (CRS) 777 160



Effect of the Initialize (INIT) signal: clear bits 15, 14, 11, 10, 7, 6, 1, and 0.

Read only: bits 15 through 7

Write only: bit 0

BIT	NAME	FUNCTION
15	Error	Set when an error occurs.
14	Card Done	Set when one card has passed through the read station and another one may be demanded from the input hopper.

CR11 CM11

13	Hopper Check	Set when the input hopper is empty or output stack is full. This signal is provided by mark sense card readers and later models of the punched card units.
12	Motion Check	Set to indicate abnormal condition in the card reader. Three conditions can cause this bit to be set: a) Feed error b) Motion error c) Stack Fail These signals are available from the mark sense readers and later models of the punched card units.
11	Timing Error	Set when a new column of data arrived into the CRB before the previously loaded column was attended to by a program.
10	Reader To on Line	Set when the reader is on-line. Sensing an error or operating the stop switch on the card reader panel causes the reader to go off-line. Operating the start switch brings the reader on-line providing no error causing condition exists.
9	Busy	Set when a card is being read.
8	Reader Ready Status	Set when the reader is off line; 0 indicates on-line and hence ready to accept read commands.
7	Column Done	Set when a column of data is ready in CRB.
6	Interrupt Enable	Set to allow Card Done, Column Done, or Error = 1 to cause an interrupt.
1	Eject	When set, column ready flag is inhibited from setting. However, data transfers between card reader and data buffer do take place.
0	Read	Set to allow the feed mechanism to deliver a card to the read station.

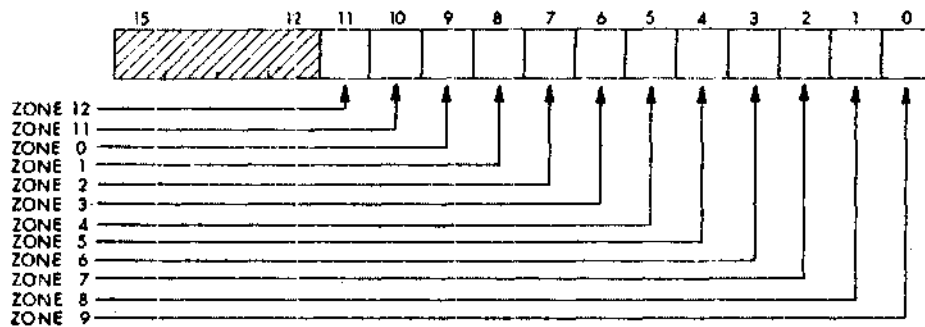
A program can load and read information from the Card Reader Status (CRS) register using appropriate instructions and considering the following limitations:

- a. Bits 15-7 can only be read on the bus.
- b. COLUMN DONE bit is automatically cleared by reading the Data Buffer.

CR11 CM11

- c. Bits 15-8 are automatically cleared when an attempt to load the status register is made. However, if this loading is to read a card, and an error condition requiring manual intervention has not been attended by the operator, appropriate error bit will be set again to cause an interrupt. Commands to READ CARD under these circumstances is not honored.
- d. BIT 0 is always read as zero on the bus.

Card Reader Data Buffer Register (CRB1, CRB2) 777 162, 777 164



Read only: all bits

Data from one column at a time of the card is loaded into this register.

BIT	FUNCTION
11	ZONE 12
10	ZONE 11
9	ZONE 0
8	ZONE 1
7	ZONE 2
6	ZONE 3
5	ZONE 4
4	ZONE 5
3	ZONE 6
2	ZONE 7
1	ZONE 8
0	ZONE 9

If the data buffer is addressed at CRB2, the 12-bit content is compressed into an 8-bit character by an encoding network before getting on to the bus as low order byte. The 8-bit code is:

CR11 CM11

BIT	FUNCTION
7	ZONE 12
6	ZONE 11
5	ZONE 0
4	ZONE 9
3	ZONE 8
2-0	DATA encoded as follows:
	000 = no punches, ZONE 1-7
	001 = ZONE 1
	010 = ZONE 2
	011 = ZONE 3
	100 = ZONE 4
	101 = ZONE 5
	110 = ZONE 6
	111 = ZONE 7

In case of multiple zones twice, bits will be the inclusive OR of the octal codes of the zones.

PROGRAMMING EXAMPLE

The following example shows a typical method of programming the CR11 Card Reader System. In this example, the card reader is used to read a bootstrap loader program from punched cards and load the program into core memory.

```
CRS=777160          ;CARD READER STATUS REGISTER
CRB1=777162         ;12-BIT DATA BUFFER
.=1000              ;STARTING ADDRESS FOR MEMORY

R1=%1
R2=%2
R3=%3
R4=%4

START:  MOV   #CRS, R1      ;SET UP ADDRESS OF CRS IN R1
        MOV   #CRB1, R3    ;ADD DATA BUFFER ADDRESS IN R3

RTST:   BIT   @R1, #1400   ;IS READER ON-LINE?
        BNE   RTST        ;NO, SO MAY AS WELL WAIT.

RD CD:   INC   @R1         ;O.K., READ A CARD

RCHK:   BIT   @R1, #140000 ;SPECIAL CONDITION OR CARD
        ;DONE SET?

        BGT   RD CD       ;SPECIAL CONDITION OFF BUT CARD
        ;DONE ON.

        BEQ   GOGO        ;BOTH OFF
```

CR11 CM11

```
END:   RESET                ;SPECIAL CONDITION ON, ASSUME
      JMP   @R2              ;HOPPER EMPTY AND BRANCH TO
                                   ;PROGRAM

GOGO:  TSTB   @R1            ;COLUMN READY?
      BPL   RCHK            ;NO, KEEP LOOKING.
      BIT   @R3, #400      ;ROW 1 IN THIS BYTE?
      BEQ   GO2            ;NO, MUST BE DATA
      MOVB  @R3, R2        ;YES, IS FIRST ADDRESS BYTE
      SWAB  R2             ;MOVE TO HIGH-ORDER BYTE
      MOV   R1, R4         ;AND SET SECOND-ADD.-BYTE FLAG
      BR    RCHK          ;AND GET NEXT COLUMN

GO2:   MOV   R4, R4        ;TEST SECOND-ADD.-BYTE FLAGS
      BNE   GO3            ;IF ON, USE THIS FOR ADD. BYTE
      MOVB  @R3, (R2)+    ;OTHERWISE, STORE IT IN MEMORY
      BR    RCHK          ;AND GET NEXT BYTE.

GO3:   ADD   @R3, R2      ;COMPLETE ADDRESS MAKEUP
      CLR   R4             ;RESET SECOND-ADD.-BYTE FLAG
      BR    RCHK          ;AND GO AROUND

      .END
```

SPECIFICATIONS

Main Specifications

Input medium:	80-column punched cards
Speed:	285 cards/minute
Hopper capacity:	550 cards

Register Addresses

Card Reader Status (CRS)	777 160
Card Reader Buffer (CRB1)	777 162, (12-bit characters)
Card Reader Buffer (CRB2)	777 164 (8-bit char, compressed)

UNIBUS Interface

Interrupt vector address:	230
Priority level:	BR6
Bus loading:	1 bus load

Mechanical

Mounting:	1 table-top unit + 1 SPC slot (quad module)
Size:	11"H x 19"W x 14"D
Weight:	60 lbs

CR11 CM11

Power

Starting current:	12 A at 115 VAC
Running current:	6 A at 115 VAC
Current for Control Unit:	1.5 A at +5 V
Heat dissipation:	600 W

Environmental

Operating temperature:	15°C to 32°C
Relative humidity:	20% to 80%

Models

CR11:	Punched card reader and control, 115 VAC, 60 Hz
CR11-A:	Punched card reader and control, 230 VAC, 50 Hz
CM11-FA:	Mark-sense card reader and control, 115 VAC, 60 Hz
CM11-FB:	Mark-sense card reader and control, 230 VAC, 50 Hz

UNIBUS LINK, DA11-B

DESCRIPTION

The DA11-B DMA UNIBUS Link is a high-speed, half-duplex data-transfer channel connecting two PDP-11 computer systems over a distance of up to 100 ft. (30 meters). Using the direct-memory-access (DMA) facilities of each computer, the link transfers either single words or blocks of data from the memory of one machine to the memory of the other. Data blocks up to 32K words in length can be transmitted via the Link in a single operation. The transfer rate can be as high as 500,000 words per second.

The Link consists of a general purpose DMA bus interface attached to each computer plus the interconnecting logic and cables that synchronize both interfaces. The bus link operates in two different modes: Word and Block. In Word Mode, information is passed between computers one word at a time by interrupt-driven program commands. In Block Mode, the link transmits blocks of consecutive locations from the memory of one computer to the memory of the other, using the DMA (NPR) facility in each machine. Each computer controls its own interface to the link. Each has its own Word Count and Bus Address registers that control the number of words in a block transfer and the memory addresses involved. The Link's Word Mode can be used to pass this control information prior to a block transfer.

After the interface registers have been initialized, a command is given to initiate the block transfer. The transmitting interface reads a word from its memory, using the NPR facility of the UNIBUS, and sends that word to the interface on the adjacent computer. The receiving interface gains control of its bus via an NPR request, and then transfers the word from the interface to memory. As each word is transferred, both interfaces automatically increment their Word Count and Bus Address registers. The alternating sequence of cycles continues until the block transfer is complete, whereupon both interfaces generate "transfer-done" interrupts. Each bus interface is constructed as a single system unit that can be installed in any PDP-11 mounting box. The interconnecting cables are shielded and terminated so that the two computers can communicate over distances up to 100 feet (30 meters).

PROGRAMMING

In order to coordinate the channel set-up procedures, the programmable control units in each interface are interconnected to pass interrupt requests and channel-usage parameters between the computers. Once the block transfer is initiated, no further programming operations on the link control units are required until the transfer is completed.

Each of the interfaces of the DA11-B contains the following four addressable registers:

DA11-B

REGISTER	MNEMONIC	PROGRAM OPERATION	BUS ADDRESS
Word Count	DRWC	Read/Write	XXXX00
Bus Address	DRBA	Read/Write	XXXX02
Control & Status	DRST	Read/Write	XXXX04
Data Buffer	DRDB	Read/Write	XXXX06

Data Buffer

The Data Buffer performs two separate functions in the interprocessor channel. In Word Mode, the Data Buffer is used as a 16-bit addressable register to transfer information between computers under program control. It is loaded by the processor transmitting the word, then read by the other processor. The Request-interrupt bit (bit 3) of the Control and Status Register can be used to signal that data has been loaded by the transmitting processor. In Block Mode, the Data Buffer serves as an internal storage register that holds the word being transferred under NPR control.

Word Count Register

The Word Count register is initially loaded with the two's complement of the number of words to be transferred. The register increments toward zero after each bus cycle. When the Word Count overflows (all 1's to all 0's), the Transfer Complete bit in the Control and Status register is set and the transfer halts.

Along with the Extended Address bits (bits 5 and 4) in the Control and Status Register, the Bus Address Register is used to specify the bus address of the location to be transferred during DMA cycles. Because the UNIBUS link is only used to transfer full 16-bit words, bit zero of the Bus Address Register is always zero. The Bus Address Register is incremented after each bus cycle, advancing the address to the next sequential word on the bus. If the Bus Address Register overflows, the ERROR bit in DRST is set. Since Bus Address overflow does not increment the Extended Address bits, the maximum block that can be transmitted in one operation is 32K words.

Control and Status Register

The Control and Status Registers in the two interfaces are interconnected to provide a means of transferring channel status and interrupt requests from one processor to the other. Either processor can set up bits 1, 2, and 3 in its own Control and Status Register to indicate that it wishes to initiate a transfer. Setting these bits causes bits 9, 10, and 11 to be set in the companion processor's Control and Status Register (and an interrupt generated, if enabled) thereby informing the companion processor of the request for transfer. The bits of the Control and Registers are defined as follows:

BIT	NAME	FUNCTION
15	Error	Set to indicate an error.
14	NEX	Set to indicate an attempt to transfer

DA11-B

		data to or from a non-existent address.
13		Unused
12		Maintenance only.
11	Interrupt Requested	Set to indicate that the companion computer has requested an interrupt (by setting bit 3 of its Control and Status Register).
10	Requested Transfer Direction	Set to indicate that the companion computer wishes to receive data. Cleared to indicate that the companion computer wishes to transmit data.
9	Requested Transfer Mode	Set to indicate that the companion computer wishes to initiate a single-word transfer. Cleared to indicate that it wishes to transfer a block of data.
8	Cycle	Set to initiate the first transmit cycle from the requesting computer. Used in conjunction with the Go bit.
7	Transfer Done	Set at the completion of a transfer to indicate that the Link is ready to accept a new command. Forces the interface to release control of the UNIBUS and inhibits further DMA cycles.
6	Interrupt Enabled	Set to force a program interrupt whenever an Error (bit 15), an Interrupt-Requested (bit 11), or a Transfer-Complete (bit 7) condition occurs.
5	XBA17	Extended-Bus Address bits. Set to 00 for a transfer in the area 0-32K, 01 for 32K-64K, 10 for 64K-96K, 11 for 96K-128K.
4	XBA16	
3	Request Interrupt	Set to request an interrupt in the companion processor. Sets Interrupt Requested (bit 11) and Transfer Complete (bit 7) in the companion computer and causes an interrupt in the other computer if its Interrupt Enable bit (bit 6) has been set.
2	Request Transfer Direction	Set to request a transfer of data from the companion processor. Clear to request a transfer to it.
1	Request Transfer Mode	Set to request a single-word transfer. Cleared to request a block transfer.
0	GO	Set to initiate a transfer.

SPECIFICATIONS

Option Designations

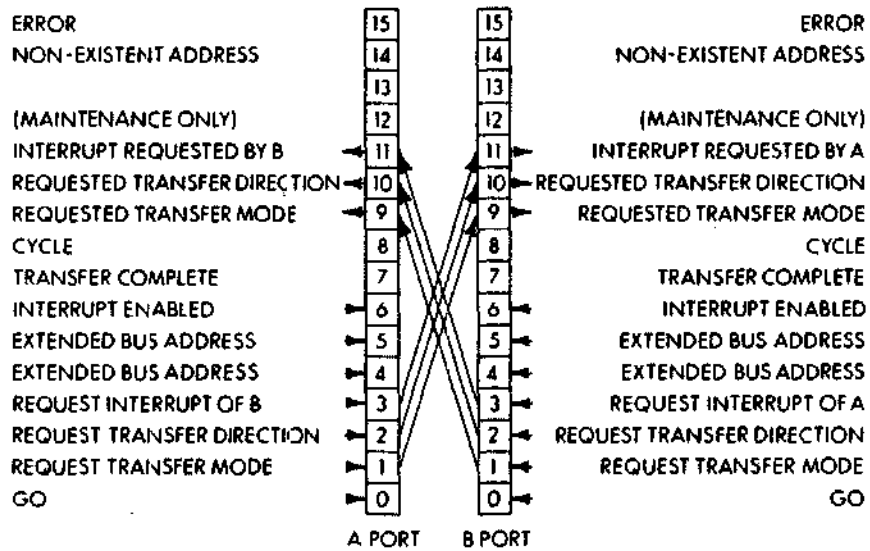
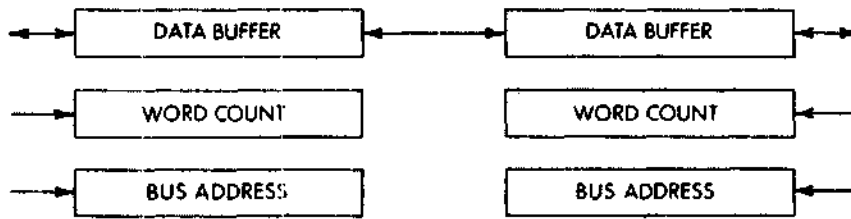
DA11-BP DMA Bus Link—25 ft. (7.5 meter) cables

DA11-BE DMA Bus Link—50 ft. (15 meter) cables

DA11-B

	DA11-BF DMA Bus Link—100 ft. (30 meter) cables
Addressable Registers	Four in each interface: Word Count Bus Address Control and Status Data Buffer
Interrupt Vector	Requires one vector at location 124 (or assigned to floating vector field, location 300 and above)
Priority Level	BR5
Modes	Word or Block Transfer
Direction	Send or Receive
Word Size	16-bits parallel data
Maximum Block Length	32K words
Bus Loading	Each interface places a one-unit bus load on its UNIBUS.
DC Power	Each interface draws 4A (max.) from + 5V dc supply.
Installation	Each interface occupies one system unit and can be installed in any PDP-11 mounting box.
UNIBUS Compatibility	Can be used with any PDP-11 Family processor.

DA11-B



Control and Data Transfer Between the A Port and B Port of A UNIBUS Link

DA11-F

UNIBUS WINDOW, DA11-F

DESCRIPTION

The DA11-F UNIBUS Window is a high-speed interbus channel that connects two PDP-11 systems. Since it is a bus-to-bus connection, the DA11-F permits communications between any two devices on the two busses. And, since it operates on a cycle-by-cycle basis, it permits interbus DMA transfers as well as single-word accesses.

The UNIBUS window allows a PDP-11 system to access addresses on a companion system's UNIBUS as though they (the addresses) were on its own. It does so by automatically translating requests to a designated part of the bus-address space into requests on the other bus. Since all synchronization is done internally by the window hardware, the operation is completely transparent to the operating software.

Any unused block of addresses on the UNIBUS, from 512 to 32K words in size, may be designated as the window. Normally, it is placed directly above the last memory module. Thus, on a system with 64K words of memory, an 8K window would be placed from 64K to 72K. Once this window is initialized, any access to a location between 64K and 72K will be translated automatically into an access to an 8K address area on the companion system's UNIBUS. (The 8K area to be accessed on the companion's UNIBUS is selected as part of the window initialization process.) Thus, a window operation involves both the UNIBUS on which the access was requested, referred to as the originator bus, and the bus on which the access is actually performed, referred to as the target bus. Any type of address access (instruction fetch, data fetch, data write, or DMA-type block transfer) may be performed through the UNIBUS window. Once the window is set up, the interbus transfer is completely transparent.

Any device capable of being bus master may originate an access through the window. A processor on one side, for example, can execute code that is contained in the other computer's memory. Or a mass-storage device can transfer data to memory on the opposite bus. An individual processor is not limited to a single UNIBUS window; multiple windows allow inter-communication between several processors.

The window channel appears as a field of UNIBUS addresses on the originator bus. When the DA11-F recognizes a bus cycle addressed to a location within that field, it gains control of the target bus via an NPR request. The DA11-F then executes the same bus cycle but addresses it to the desired physical location on the target bus. A "through-the-window" transaction, therefore, is composed of a data transfer cycle on each bus. UNIBUS cycles operate as master-slave handshaking sequences. As a result, the DA11-F appears as a slave on the originator bus and as a master on the target bus.

The window field on the originator bus is fixed in size and in its location in the total bus-address space. The target space that the DA11-F can ad-

DA11-F

dress on the target bus is the same size as the window field but may be relocated, under program control, throughout the full UNIBUS addressing range (128K). A device on the originator bus could address its data transfer to the window field between 64K and 72K, but would actually gain access to target-bus locations between 32K and 40K. The relocation factor may, of course, be changed to point the window to any set of locations (starting on an even 4K boundary) on the target bus.

The DA11-F is a completely symmetrical unit and contains two of the window channels described above. Transactions may, therefore, originate on either bus and data may flow in either direction. To distinguish the two sides of the bus window, the UNIBUS interfaces are designated as the A Port and the B Port.

Each processor is given complete control over accesses to locations on its own bus. A programmable control unit within each port governs the use of the channel that originates on the opposite bus. The processor on the target bus can disable transfers through the window, restrict them to read only, and decide which addresses on its bus the window may have access to.

PROGRAMMING

Since each processor controls window operations directed at its own bus, the two computers must cooperate in establishing the access parameters for the window channels. Both cross-interrupt and cross-parameter transfer facilities are provided in the port-control units for interprocessor communication. Information can be passed via the control units without disturbing any on-going window-channel operations. Typical messages would request that a channel be opened, indicate whether it is to be read/write or read only, and set up the relocation factor to be used in calculating the target address. Once a channel has been opened, programs on the originator side can make random accesses through the window at any time with no further programming operations on the DA11-F control unit itself.

Each port of the DA11-F contains the addressable registers explained below:

REGISTER	MNEMONIC		PROGRAM	
	A PORT	B PORT	OPERATION	ADDRESS
Control and Status Word	ACSR	BCSR	Read/Write	XXXX00
Output Data Buffer	ADB	BDB	Read/Write	XXXX02
Input Data Buffer	BDB	ADB	Read Only	XXXX04
Displacement Address (Internal)	ADA	BDA	Read Only	XXXX06
Relocation Address	ARA	BRA	Read/Write	XXXX10
Starting Address	ASA	BSA	Read Only	XXXX12
Vector Address	AVA	BVA	Read Only	XXXX14

Control and Status Register

The Control and Status Registers on each port are interconnected to provide a means of transferring information, channel status, and interrupt

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requests from one processor to the other. They also report error conditions due to illegal access by an originator bus or due to the inability of the window channel to complete a target bus cycle.

The bits of the Control and Status Registers are defined as follows:

BIT	NAME	FUNCTION
15	Error	Set if an access request from the originating bus fails. When the error bit is set, further window transactions originating on this bus are inhibited. If the Interrupt Enable bit (bit 6) is set, the error will cause an interrupt.
14	Timeout	Set on this port if a bus timeout occurs while the window is attempting to access a location on the opposite bus. Generally, the timeout is the result of attempting to access a non-existent target location in memory.
13	Power Failure	Set to indicate a power failure on the target bus.
12	New Data Loaded by Other Bus	When set, indicates that the opposite processor has loaded new information into its CSR (bits 11:9) or its Data Buffer. If Interrupt Enable (bit 6) is set, then loading new data causes an interrupt on this bus. The new-data bit can be set and cleared to signal successful passing of data. For example, if bit 0 (New Data for A) is set on the B port, a 1 appears at bit 12 of the A port. If Interrupt Enable (bit 6) on the A port is set, an interrupt request will be generated on the A bus. When the A processor has serviced the interrupt, it can clear the New-Data bit by writing a 0 into bit 12 of its own CSR. This action clears bit 0 of the B port CSR, thereby indicating that the message has been received.
11	Data 3 from Other Bus	Readout of contents of bits 5, 4, and 3 from the opposite port. Used to pass information bits and flags between computers.
10	Data 2 from Other Bus	
9	Data 1 from Other Bus	
8	Enable Transfer from Other Bus	Set to allow this port to be used as a target for transactions originating on the opposite bus. (Transfer Enable should only be set after Write Enable (bit 1) and

DA11-F

		the Relocation Address Register on this port are loaded correctly.)
7	Transfer to Other Bus Enabled	When set, indicates that an originator on this bus may perform a window transaction to the opposite bus, i.e., the target bus has set its Enable Transfer bit (bit 8). If this bit is clear, an attempt to originate a window transaction from this bus will cause an error.
6	Interrupt Enabled (IE)	Set to generate a program interrupt when an error occurs (bit 15) or when the companion processor loads new data (bit 12).
5	Data 3 for Other Bus	Loaded to pass information to the companion computer.
4	Data 2 for Other Bus	
3	Data 1 for Other Bus	
2	Writing to Other Bus Enabled	When set, indicates that the companion processor has allowed write access to its UNIBUS locations (i.e., the companion processor has set its bit 1).
1	Enable Writing from Other Bus	Set to allow the companion processor to change locations on the UNIBUS.
0	New Data	Set to indicate to the companion processor that either the Data bits (bits 11:9) or the Data Buffer on this port are loaded with new information.

Output Data Buffer

The 16-bit Output Data Buffer operates in two modes—either as an internal data-storage register during window transactions or as a cross-communication register during interprocessor program transfers. When the window is not enabled for transfers (bit 8 of the status register is cleared) the Output Data Buffer can be used to pass information to the opposite processor. Since data transfers can only be enabled by the target bus, the output data buffer provides a convenient way for the originator bus to request that a window be enabled.

Input Data Buffer

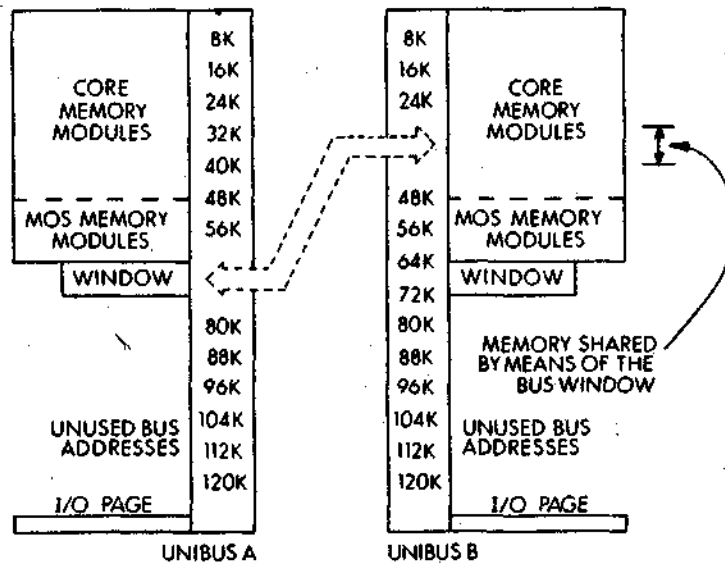
The 16-bit Input Data Buffer holds the contents of the Output Data Buffer from the opposite port. It permits the target bus to read data loaded by the originator bus.

Relocation Address Register

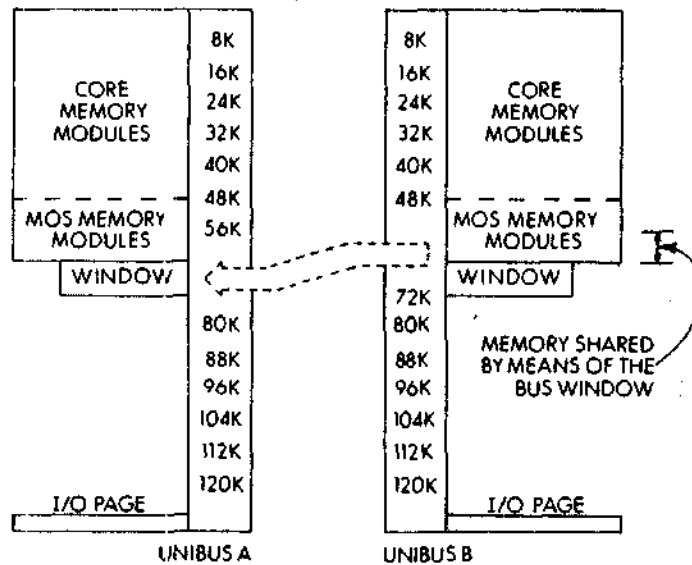
The Relocation Address Register specifies the high-order bits of a relocated target address, i.e., the area on the target bus to which the window points. It is loaded by the processor on the target bus. During a window transaction, the contents of the Relocation Address Register, shifted left by two bits, are added to the low order bits of the address

on the originator bus (that indicate the address within the window) to form an 18-bit target address.

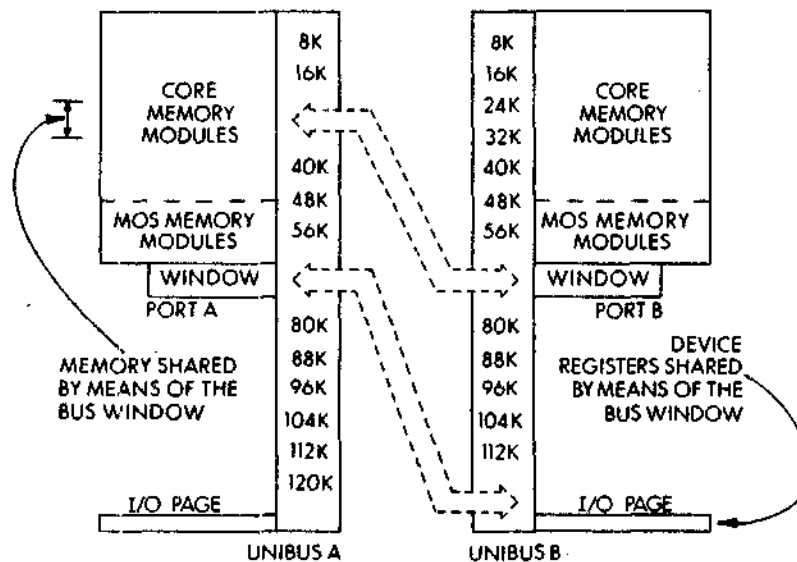
Operation of the UNIBUS Window
 (Simplified examples using identical processors and only one window port)



- a. Example: A is the originating bus; B is the target bus. An 8K Window on UNIBUS A is located at 64K. It has been initialized to connect to locations 32-40K of UNIBUS B. System A executes a MOV X, R0 instruction where X is defined to be a location between 64K and 72K.
 1. Processor A issues a request on UNIBUS A to fetch location X.
 2. The window recognizes this as an address within its address boundaries (64K-72K). It therefore translates it into the appropriate address on UNIBUS B (an address between 32K and 40K) and issues a request on UNIBUS B to fetch that location.
 3. The data is fetched from UNIBUS B and passed to the window.
 4. The data from UNIBUS B is transmitted to Processor A in response to the original fetch cycle on UNIBUS A.
 5. The data is loaded into Processor A's R0, thereby completing execution of the MOV X, R0. The fact that the data actually came from System B's memory is transparent to Processor A.



- b. In this second example, the window has been reinitialized to point to locations 56K-64K on UNIBUS B. If the same MOV X, R0 instruction were repeated, the value of X would be fetched from System B's MOS memory instead of from its core memory. Also, in this example, access to UNIBUS B has been initialized as read-only. An attempt to execute a MOV R0, X instruction would, therefore, result in a protection-violation trap.

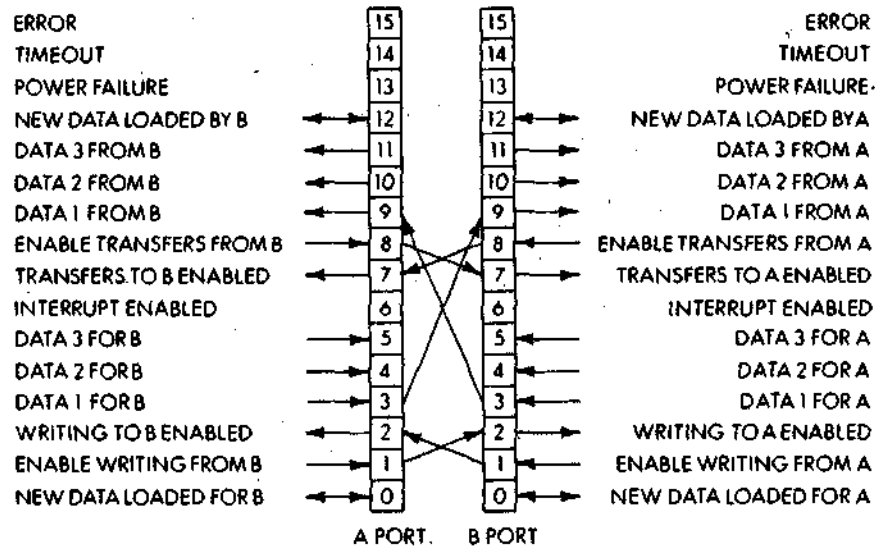
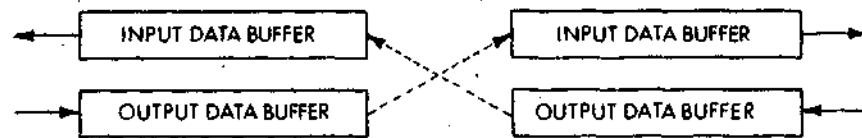


UNIBUS Window Operation Utilizing Both Window Ports

In previous examples, only one direction of window transfer was diagrammed. The window actually implements two independent paths between busses. Having both windows enabled for reading and writing

DA11-F

allows each system to have shared access to part of the other system's memory. In this special case example, System A's window allows it to access device registers and hence initiate transfers on one or more of System B's peripherals. By doing writes to the appropriate locations between 68K-72K on its own UNIBUS (automatically translated by the window to actually load disk controller registers in System B's I/O page), System A may initiate an 8K transfer to locations 64K-72K on System B's UNIBUS. But this data would, in turn, pass through System B's window to locations 24K-32K of System A's memory. Thus, the window permits System A to initiate a transfer from System B's disk directly into its own memory on a completely transparent, DMA, basis.



Control and Data Transfer Between the A Port and the B Port of a UNIBUS Window

SPECIFICATIONS

Option Designation
Addressable Registers

DA11-F UNIBUS Window

Seven in each port:
Control and Status
Output Data Buffer
Input Data Buffer
Displacement Address (internal use only)
Relocation Address

DA11-F

Interrupt Vector	Starting Address (maintenance) Vector Address (maintenance) Requires one vector assigned to floating vector field (location 300 and above)
Priority Level	BR7
Bus Loading	Each port places a one-unit bus load on its UNIBUS
Bus Latency	300-ns internal address-translation time plus time of the bus cycle on the target bus.
DC Power	Draws 5 amperes from + 5 V dc supply
Installation	Occupies one system unit and can be installed in any mounting box that accepts hex-height modules
UNIBUS Compatibility	Can be used with any PDP-11 Family Processor

BUS REPEATER, DB11-A

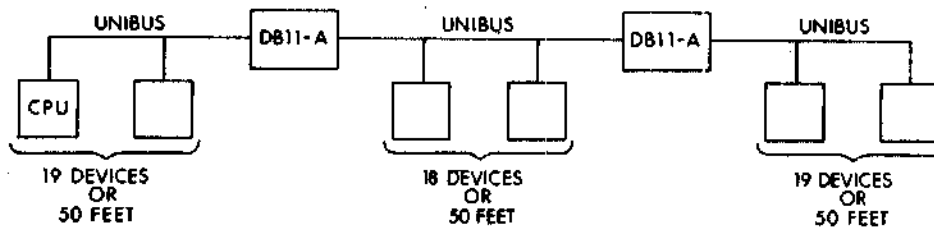
DESCRIPTION

The DB11-A Bus Repeater allows physical and electrical extension of the UNIBUS. Each DB11-A allows a 50-foot extension in bus length, and will drive 19 extra bus loads. Most PDP-11 options that interface to the UNIBUS are one bus load.

All UNIBUS signals are carried through from one side to the other by the DB11-A. Inclusion of a Bus Repeater in a PDP-11 system imposes no operational changes, and no timing restrictions. The operation is transparent to programming, and there are no addressable registers. The bus cycle time is unaffected for devices on the same side of the Repeater, and increase by only a maximum of 375 nsec for devices on the opposite sides.

Bus Loading

Each section of the UNIBUS is rated for 20 bus loads and a length of 50 feet. The DB11-A represents 2 bus loads, 1 on the input (CPU) side, and 1 on the output side. Therefore, the addition of one DB11-A allows a total of up to 38 devices (excluding the DB11-A), for a net gain of 18 bus loads.



DB11 Bus Repeater

SPECIFICATIONS

Increase in Bus Timing

Master and slave on same side: 0
Master and slave on opposite sides: 375 nsec, max

UNIBUS Interface

Bus loading: 2 bus loads (1 on each side)
Drive capability: 19 bus loads and 50 feet

Mounting: 1 System Unit (SU)
Input current: 3.2 A at + 5 V

Environment

Operating temperature: 5°C to 50°C
Relative humidity: 10% to 95%

PERIPHERAL MOUNTING PANEL, DD11

GENERAL

The DD11 Peripheral Mounting Panel is a pre-wired System Unit designed for mounting up to 4 Small Peripheral Controller (SPC) interfaces. It is pre-wired for logic and UNIBUS signals, and for power. The physical construction of the DD11 is similar to the BB11 Blank Mounting Panel.

Use of the DD11 requires specialized logic modules for the actual interface, since the pin assignments are fixed for the various control and data signals. Customers may design interfaces to go into a DD11 by using modules which have the same pin assignments for the signals.

There are two versions of the DD11, differing in only one functional aspect. The DD11-B is pre-wired for 2 DF11 interfaces, while the DD11-A is not.

DIFFERENCES

	DD11-A	DD11-B
1. Pre-wired area.	4 SPC slots.	4 SPC slots + 2 DF11 slots
2. Use with BA11-ES Mounting Box.	Must be used.	Cannot be used. (for power connection reasons)
3. Power Connections.	Module for power plugs into slot A3.	Tabs are used on the wire-wrap pin side.
4. Pin numbers CA1 to CV1.	Interconnected between slots 1 & 2, also 3 & 4.	Assigned to UNIBUS signals.

DD11-A

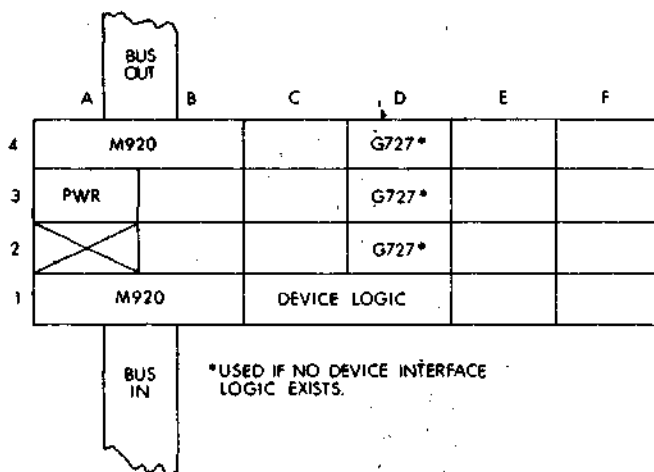
The following figure illustrates module allocation within a DD11-A unit. Slot A2 must be empty because of power cable overhang; slots B2 and B3 are unused. The DD11-A is wired to permit the installation of four M7821 modules in column F, four M105 modules in column E, and four double-height device interface modules in columns C and D or 4 quad module Small Peripheral Controllers (SPC's), which contain the equivalent of the M105 and M7821 plus the device interface logic. The uni-directional grant lines are wired to column D, and each device interface module must include jumper arrangements to allow selection of the device priority level at the time of installation. Only BR<7:4> levels are wired to this column; devices mounted in a DD11-A unit cannot be assigned to the NPR priority level without rewiring the panel. An additional constraint imposed on the interface is that each device may be on only one request level, since both interrupts available through one M7821 module are wired in series and must be at the same priority level.

DD11

If the device requires interface logic that occupies more than one full row of space in the DD11-A, columns C and D of the second row can be used by using wiring provided between rows 1 and 2 and rows 3 and 4. If this is done, it is no longer necessary to add another M105 and M7821 module to slots E and F of the second row.

UNIBUS—The UNIBUS enters through slots A1-B1 of the DD11-A. This connection can be made with either an M920 UNIBUS connector or a BC11A UNIBUS cable. All bus signals (except grants) are wired directly to corresponding pins in slots A4-B4. Connection can be made with either an M920 connector or BC11A cable to continue the UNIBUS to the next unit. If the DD11-A is the last unit on the bus, an M930 Bus Terminator must be placed in slots A4-B4.

Power—The G772 Power Connector plugs into slot A3. This connector distributes +5V power to all A2 pins and -15V power to all B2 pins except in slots A1, B1, A4, B4, A2, and A3. Ground is maintained through the frame and power connector on pins C2 and T1 of all slots.



DD11-A Module Layout

Note that a G727 Grant Continuity module must always be installed in column D if there is no interface logic in that row. The following figure shows the wiring assignments that must be adhered to when using the DD11-A.

Extended Usage—Additional wiring provides 10 signal lines between slots C1-D1 and C2-D2 as well as between slots C3-D3 and C4-D4. This permits use of multiple board device controls. Thus, if device logic can be divided into two sections with 10 or less interconnections between sections, then one section can be mounted in slots C1-D1 and the other section in slots C2-D2.

DD11

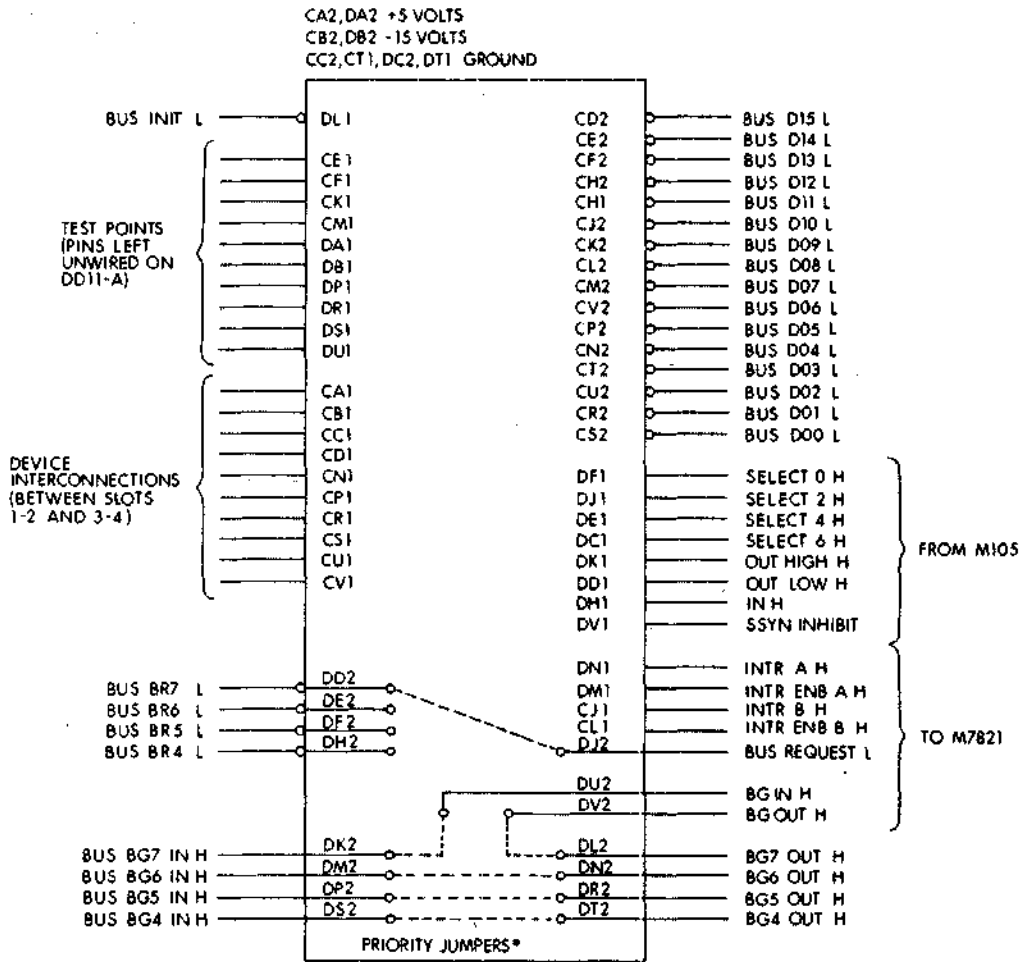
NOTE

Interconnections can be made only between rows 1 and 2 or between rows 3 and 4. No connections can be made between 1 and 3, for example.

Other sections of divided logic can also be placed into slots E and F with the interconnections provided by the normal M105 and M7821 module-to-device control signals.

CAUTION

When designing special logic, it is necessary to prevent interference with bus signals prewired to the pins of a particular slot.



Device Control as Wired in the DD11-A

Grant Continuity—The device control module mounted in slots C1-D1 receives the bus grant signal from the UNIBUS. As a function of its interrupt priority level, this device control must switch the grant signal into its interrupt control (BG IN). After passing through both stages of the interrupt control, if not the interrupting device, the signal (BG OUT) must be returned to the grant chain and passed on to the next device control (mounted in slots C2-D2). In addition, the device control must maintain the continuity of unused grant signals. The BG OUT signals of C1-D1 are wired to the BG IN lines of the next device control. This grant chain must be continued through each device until the BG OUT signals of the last device control are wired to the outgoing UNIBUS in slots A4-B4.

Whenever slot D is not used by a device control, a G727 Grant Continuity module must be inserted in this slot. This module provides jumpers between pins K2 and L2, M2 and N2, P2 and R2, and S2 and T2. Three G727 modules and one M920 module are provided with the DD11-A unit.

External Device Cables—An edge connector mounted on the device control module permits connection to external devices. An H807 36-pin module socket may be mounted on the device control module and an M927 cable connector or M925 ribbon connector may be used. The M927 is used for coaxial cables or twisted pairs and is electrically equivalent to the M904 connector; however, the cable is mounted at the edge of the module card rather than at the end. The M925 is similar to M903 and is used for ribbon cable connectors.

DD11-B

The DD11-B can hold:

4 SPC's plus 2 DF11's

	A	B	C	D	E	F
4	UNIBUS CONNECTION		SPC			
3	DF11		SPC			
2	DF11		SPC			
1	UNIBUS CONNECTION		SPC			

ACOUSTIC TELEPHONE COUPLER, DF01-A**FEATURES**

- Data rates up to 300 Baud
- Acoustic coupling
- TTY and EIA RS232C output
- Half- and full-duplex operation
- Integral acoustic shielding
- Impact-resistant case

The DF01-A acoustic coupler can be used to connect DIGITAL and other terminals to remote computing systems via ordinary telephone sets and the public switched telephone network.

Both 0-20 milliampere teletype current loop and EIA RS232C interfaces are standard in the DF01-A.

Through slide switches, the user may choose either full- or half-duplex operation.

“Sound-seal” cushions on the DF01-A hold the telephone handset firmly in position and provide excellent acoustic shielding. Good durability is provided by an injection-molded case made of special impact-resistant material. All electronic circuitry, switches and connectors are mounted on a single printed circuit board.

SPECIFICATIONS

Operating Modes: Originate-only, in half- or full-duplex.

Data Rate: Up to 300 Baud.

Receiver Sensitivity: -35dBm in acoustic mode.

Frequencies:

	Send	Receive
Mark	1270 Hz	2225 Hz
Space	1070 Hz	2025 Hz
Frequency Stability:	0.3%	0.4%

Modulation Technique: Audio Frequency—Shift Keyed (AFSK)

Transmit Power Level: -21dBm \pm 3dBm

Line Coupling: Acoustic coupling to telephone line.

Interface: 0 to 20 milliampere teletype levels or EIA RS232C (both available on the same unit; both outputs can be used simultaneously if desired).

Compatibility:

Used with remote terminals (teleprinter, typewriter, CRT display, plotter, card reader) to provide information transfer to/from a Bell 103A2 (or

DF01

equivalent) dataset. Cannot be used with 230V, 50 Hz, nor is it compatible with European modems.

Power Requirement: 115V, 60 Hz (less than 10W)

Operating Temperature: 32° to 140°F (0° to 60°C)

Size:
Width 7.5" (18 cm)
Height 3" (7.6 cm)
Length 12" (30.4 cm)

Weight: 6 lbs. (2.72 Kg)

Mounting: Tabletop case

Controls and Indicators:

Power ON/OFF

Full-Duplex/Half-Duplex (slide switch)

Carrier ON indicator light

Cables: Supplied with 8 ft. (2.27 m) cable for connection to Model 33 ASR or KSR teletypewriter.

Ordering Information:

OPTION	PREREQ.	DESCRIPTION
DF01-A	None	Acoustic Telephone Coupler

A cable may be ordered (DEC No. BC05D-25) to connect the DF01-A to EIA terminals already supplied with a cable.

Applications:

The DF01-A may be used to operate a standard DIGITAL LA30, LA36, VT05 or VT50 terminal over the switched network. In the case of the LT33D and E, connection to the DF01-A will disable the paper tape punch/reader. The reader may be enabled by DIGITAL field service personnel.

DF11

SERIAL LINE INTERFACE SIGNAL CONDITIONING, DF11

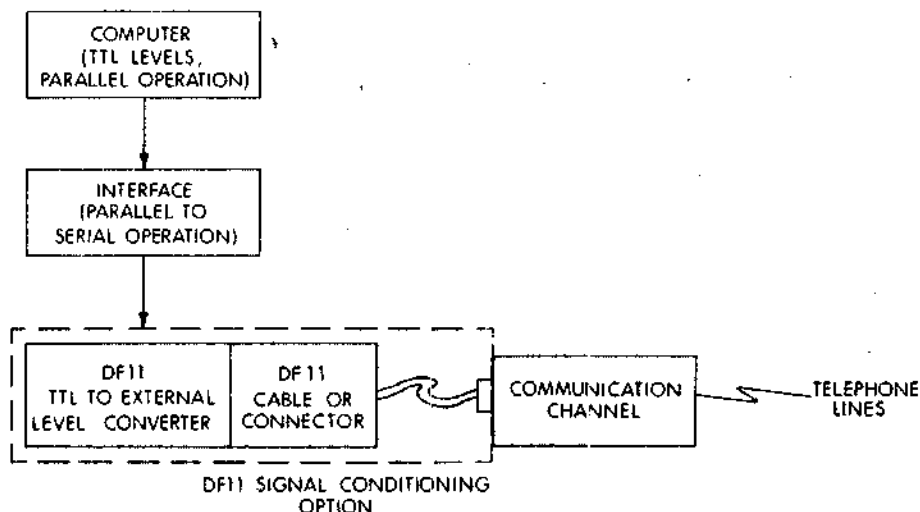
DESCRIPTION

The DF11 furnishes flexible, low-cost electrical and physical signal conditioning between most Digital-supplied serial line interface equipment and terminals, and commonly used serial communications channels. DF11 units are used with the following Digital serial line interface equipment: DC11, DP11, DL11, DH11, and LA30.

Most modern digital computers handle data signals as Transistor-Transistor Logic (TTL) levels. These levels must then be converted to other voltage levels or current values to prepare them for application to communications media so that they may be transmitted to a distant processor or terminal. In addition to the need for level conversion, there is a requirement to have cables of various lengths equipped with a variety of specialized fittings for each communications medium serviced.

CONSTRUCTION

A DF11 unit will normally consist of two single-height modules. One module performs the electrical signal conditioning function of converting from the TTL signal levels internal to the computer logic to the external signal discipline required (e.g., EIA RS-232C, 20 mA Teletypes, Bell System CBS or CDT Data Access Arrangements, etc.). The second module performs the physical interface conditioning required; i.e., furnishes a cable to connect the level-converted signals produced by the first module to the desired device or channel (e.g., a dataset). In the case of the DF11-F 20 mA Teletype Interface, this second module provides a Mate-n-Lok connector for a customer-furnished cable. In the case of the DF11-A EIA Interface, the second module provides the 25-conductor cable and plug to connect the level-converted signals on the back panel wires to the dataset.



DF11

TYPICAL CONFIGURATIONS:

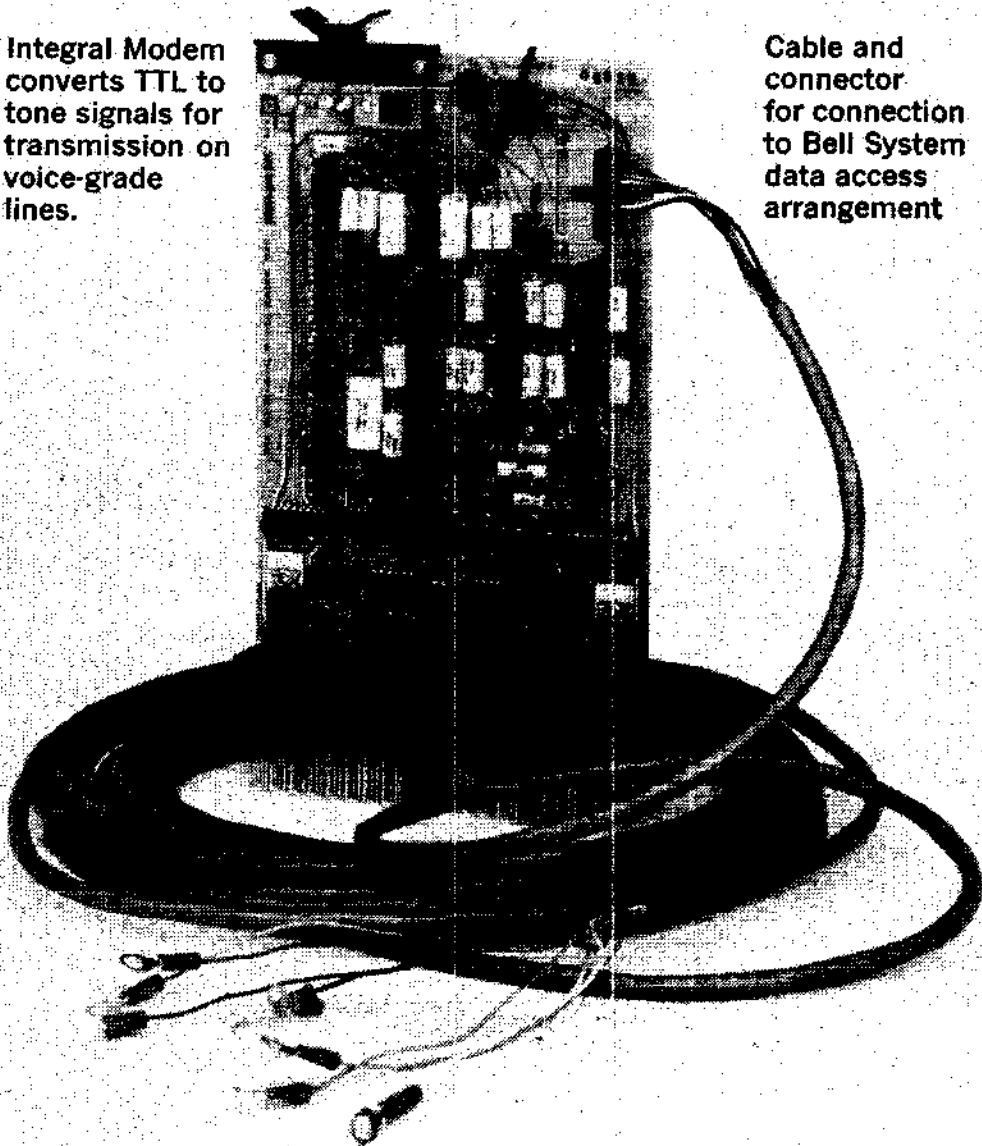


DF11-A

DF11

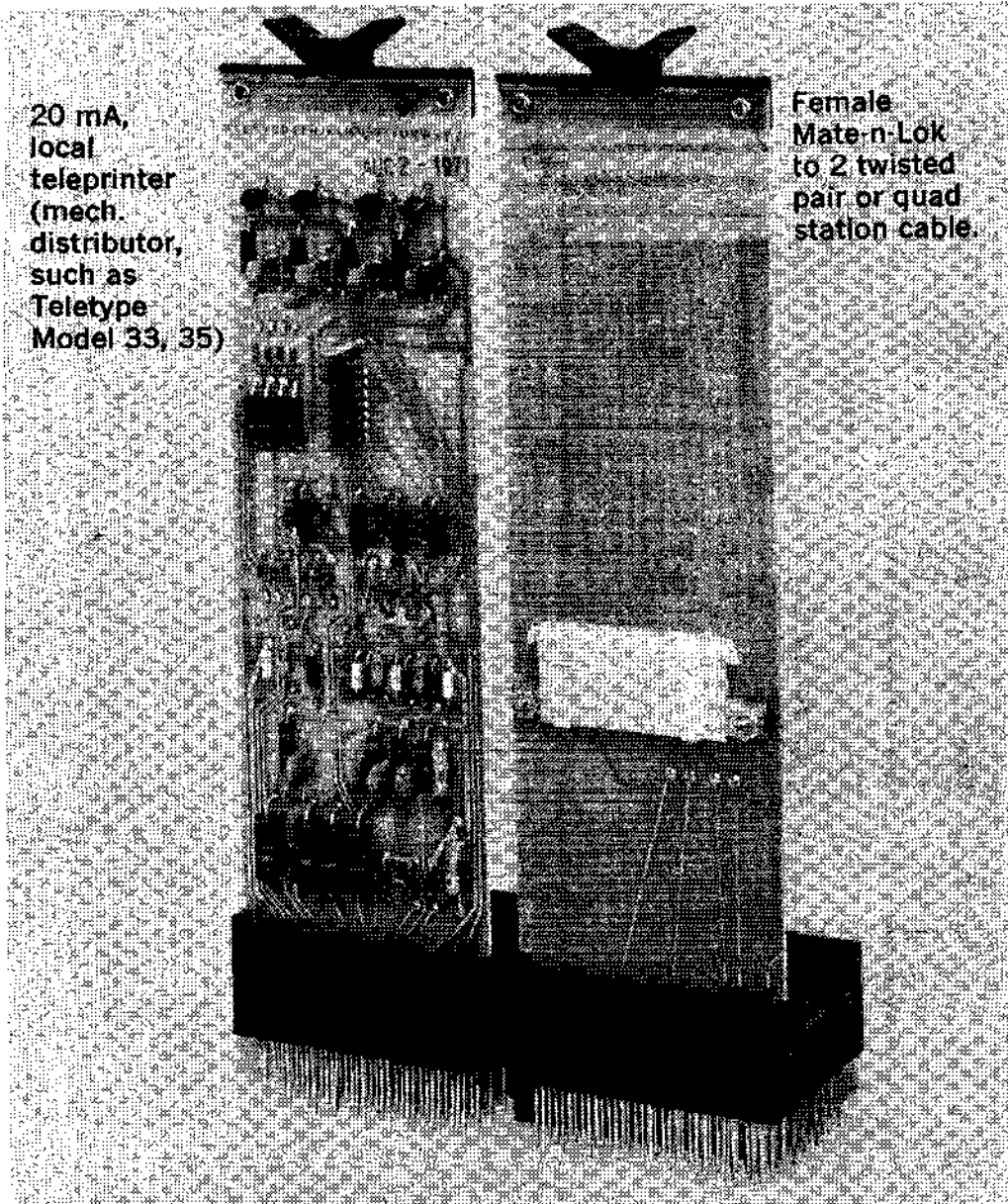
Integral Modem converts TTL to tone signals for transmission on voice-grade lines.

Cable and connector for connection to Bell System data access arrangement



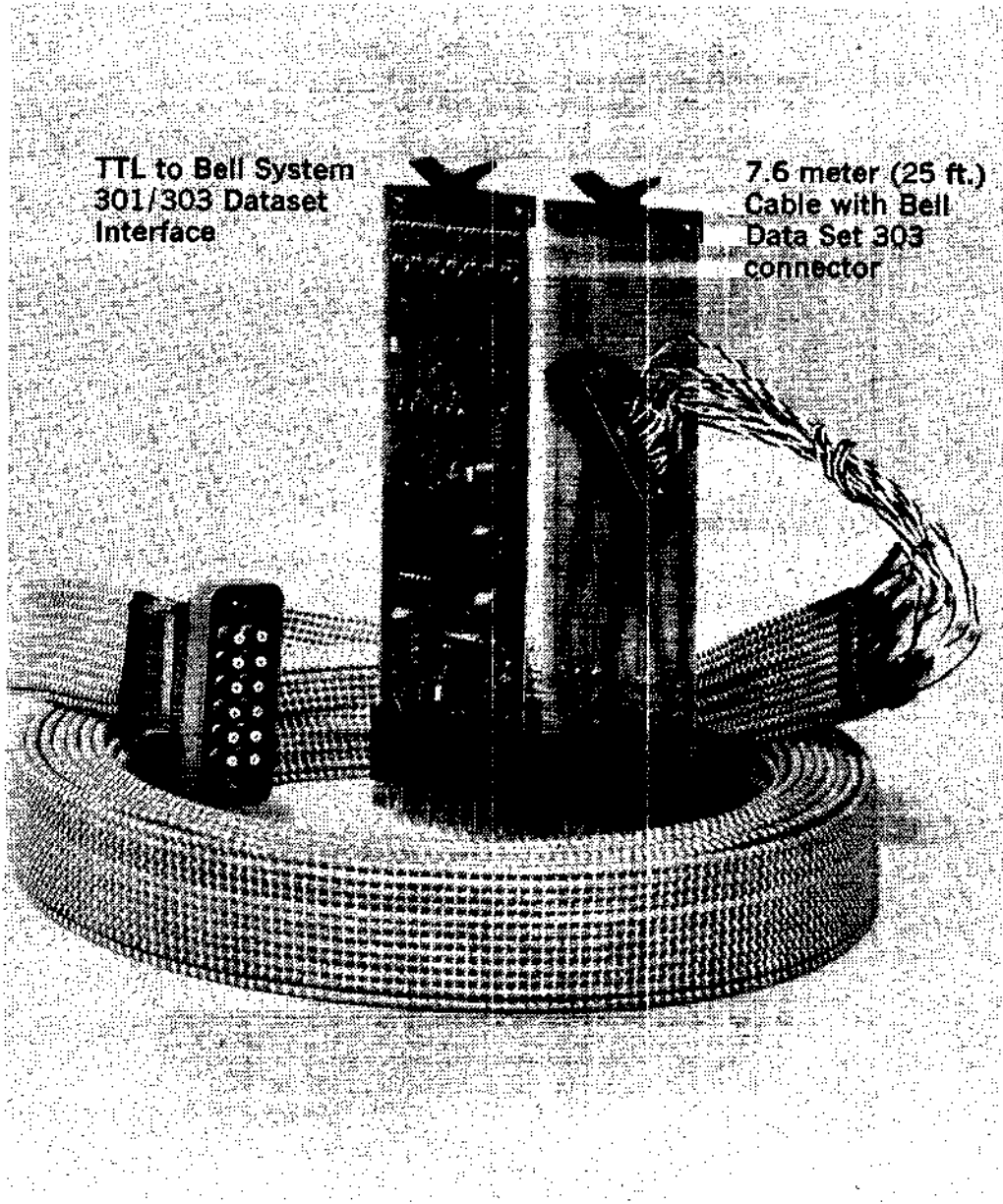
DF11-B

DF11



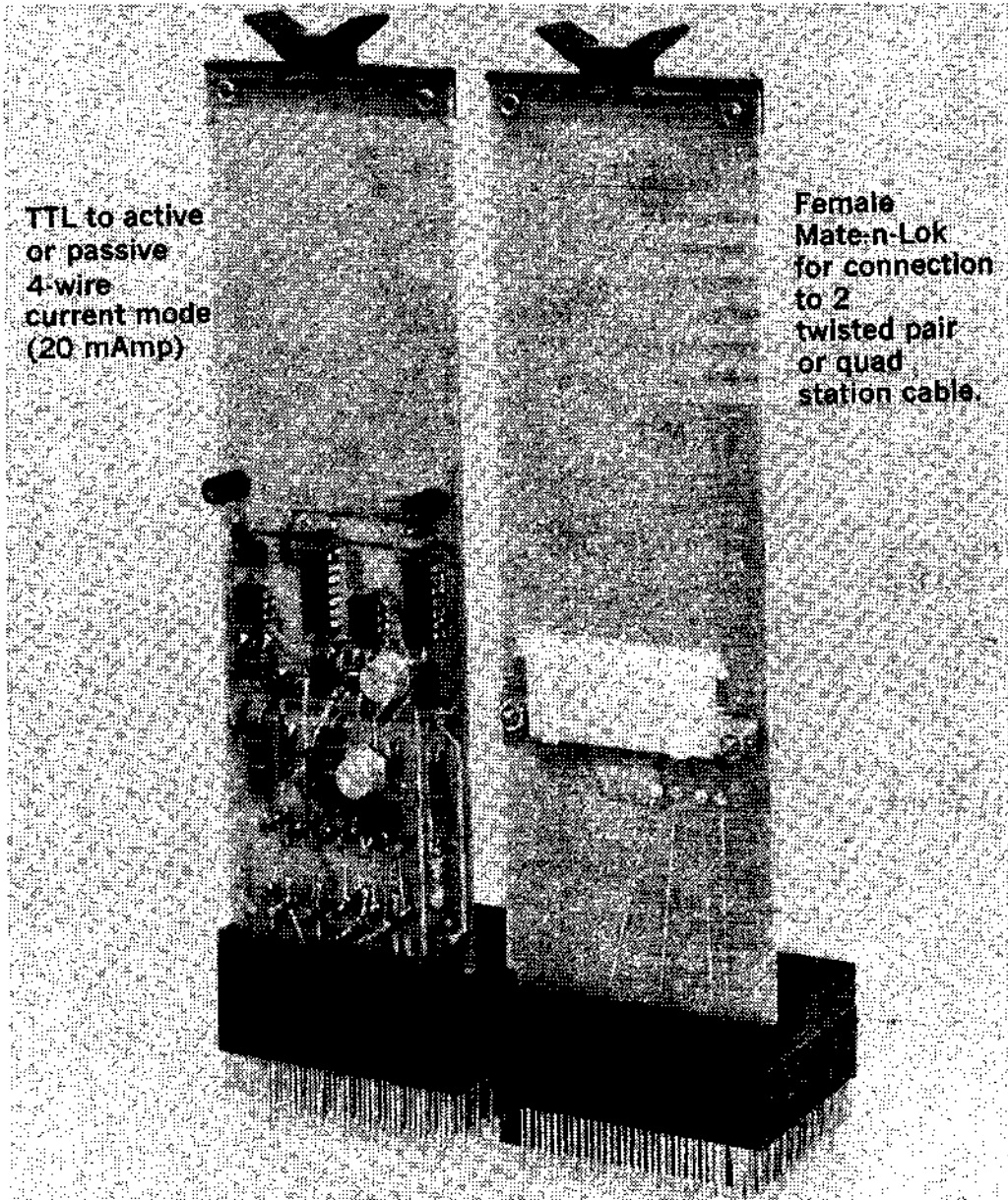
DF11-F

DF11



DF11-G

DF11



DF11-K

MODELS**DF11-A—EIA ADAPTER**

TTL to EIA/CCITT voltage levels. Connects to EIA circuits AA, AB, BA, BB, CA, CB, CE, CF, SBA, SBB, DA, CD, DB, DD, and C. Twenty-five foot cable with DB25P 25-pin male Dataset plug. Signaling rates up to 9600 Baud.

DF11-BA—INTEGRAL MODEM

Integral 103-type modem converts TTL to audio frequency shift keyed tone signals in the Originate-Only mode. Twenty-five foot cable and connector provided for connection with Bell System data access arrangement CDT or to private wireline channels. Signaling rate up to 300 Baud.

DF11-BB—INTERNAL MODEM

As above (DF11-BA) except unit operates in Answer-Only mode, and interfaces to Bell System data access arrangements CBS or CDT.

Note: The DF11-BA and BB may be used without data access arrangements on customer-owned lines, at distances up to 5000 ft.

DF11-F—TELETYPE ADAPTER

TTL to 20 mA active local Teletype loop. Connector is Amp Mate-n-Lok for connection with customer-supplied 22AWG, 2 twisted pair cable to local or remote (up to 1500 ft.) Model 33 or 35 Teletype. Signaling rates to 300 Baud.

DF11-G—303 DATASET ADAPTER

TTL to Bell System 301/303 Dataset Interface, Signal levels, cable connector, and signal pinning compatible with the Bell 301/303 Datasets. Supplied with 25-foot cable. Signaling rates to 250K Baud.

DF11-K—OPTICAL COUPLER

TTL to active or passive 4-wire current mode (20 mA) loop. Connector is Amp Mate-n-Lok for connection with customer-supplied cable. Signaling rates up to 2400 Baud, at distances up to 1500 ft.

Note: The data rates and distances cited above are recommended by DIGITAL. They are applicable in electrically quiet environments and do not necessarily represent limiting values.

APPLICATION

The DF11 series is applicable in most DECcomm-11 communications line interface equipment. The following is a partial list of line interfaces and mating DF11 signal conditioning options:

DL11*	DF11-BA, DF11-BB, DF11-K
DC11	DF11-A, DF11-F, DF11-K
DP11	DF11-A, DF11-G
DH11	DF11-A, DF11-BA, DF11-BB, DF11-F, DF11-K

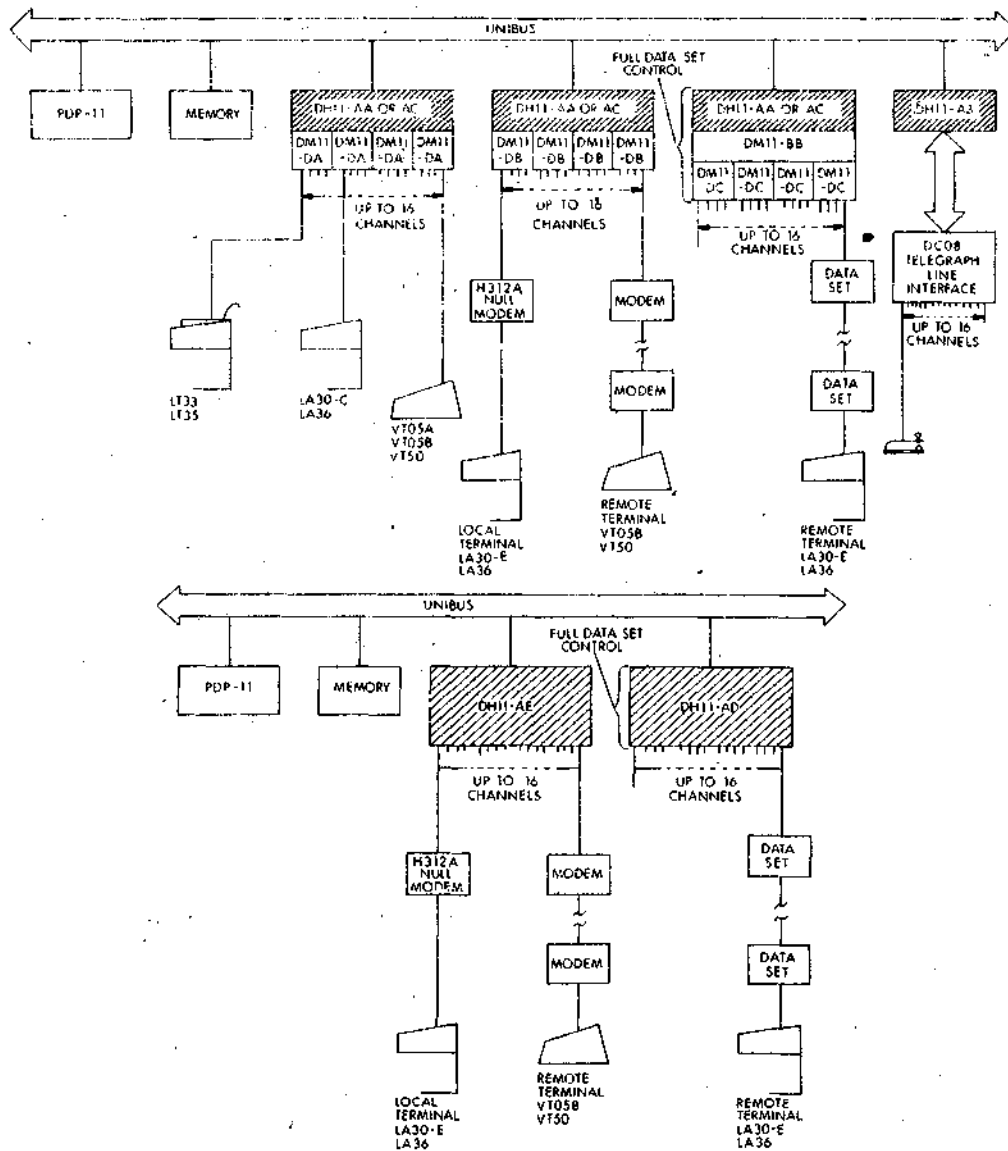
* Available only when the DL11 is used in a DD11-B system unit, or in the top small peripheral controller slot of a PDP-11/10.

DF11

Related Options

- H312-A Null Modem—for connection of DF11-A directly to local EIA-compatible terminals.
- 959-A Bag of 8 Male Mate-n-Lok connectors, with pins. For connection of customer-supplied cable with female Mate-n-Lok connectors supplied with DF11-F and DF11-K options.

16-LINE PROGRAMMABLE ASYNCHRONOUS SERIAL LINE MULTIPLEXER, DH11



Features

- Speed—Each line of the DH11 may run at program-selectable speeds up to 9600 Bauds.
- Flexibility—complete program control of each line for:
 - Data Rate—14 standard speeds, plus two external inputs
 - Character Size—5, 6, 7, or 8 bits
 - Stop Code Length—1, 1-1/2, (5-bit data only) or 2 bits
 - Transmission Mode—full-duplex, half-duplex or echo-plex
 - Parity generation and checking

DH11

- Program-controlled hardware echo of received characters
- 64-character hardware buffer for received characters
- DMA transmitter for each line, with byte count & address registers in hardware
- Split speed—transmitter and received of each line may run at different speeds
- Complete range of DF11 line conditioning interfaces available, including DF11-BA and DF11-BB Integral Modems*
- Hardware break detection and program-controlled break generation
- Capacity—up to 256 lines per PDP-11

APPLICATIONS

The excellent price/performance ratio of the DH11 allows it to serve in many communications applications. These include remote concentrators, front-end preprocessors, and store and forward message switches. The DH11 interfaces to a variety of local and remote terminal types.

Line Concentrators

A cluster of remote low-speed data terminals can often be interfaced more economically to a remote interactive computer via a data concentrator than by using a separate line per terminal. Communication line costs can be reduced by concentrating several low-speed terminals into a single medium-speed communication line using a data concentrator. Typically, a data concentrator performs the following functions:

- Character-to-message assembly/disassembly
- Communication line control
- Message buffering
- Error control
- Code conversion
- Automatic answering

Front-End Processors

Front ends handle routine tasks for large central computers, such as message input-output to remote terminals and local and remote peripherals. They perform most of the functions of line concentrators, but are connected directly to the host processor.

Store-and-Forward Message Switches

This type of system has a number of data terminals connected locally or via communications lines to a central computer. Any terminal can originate a message and transmit it to the central computer. Here the message is stored until it can be forwarded to the destination terminal. Typical functions performed by a store-and-forward message switch are:

- Assembly/disassembly of messages
- Polling and addressing of terminals
- Line control
- Error control
- Code and speed conversion
- Message header analysis

* Except for DH11-AD and DH11-AE

DH11

Sequence number of messages
Time and date stamping of messages
Message routing

DESCRIPTION

The DH11 multiplexer connects the PDP-11 with 16 asynchronous serial communications lines operating with individually programmable parameters. These parameters are:

Character length:	5, 6, 7, or 8 bits
Number of stop bits:	1 or 2 for 6-, 7-, 8-bit characters 1 or 1.5 for 5-bit characters
Parity generation and detection:	Odd, Even, or None
Operating mode:	Half Duplex or Full Duplex
Transmitter speed (Baud):	0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, Ext A, Ext B.
Receiver speed (Baud):	0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, Ext A, Ext B.

Breaks may be detected and generated on each line.

The DH11 Multiplexer uses 16 double-buffered MOS/LSI receivers to assemble the incoming characters. An automatic scanner takes each received character and the line number and deposits that information in a first-in, first-out buffer memory referred to as the "silo." The bottom of the silo is a register which is addressable from the UNIBUS.

The transmitter in the DH11 also uses double-buffered MOS/LSI units. They are loaded directly from message tables in the PDP-11 memory by means of single cycle direct memory transfers (NPR). The current addresses and data byte counts for each line's message table are stored in semi-conductor memories located in the DH11. This reduces the UNIBUS time required for NPR transfers to one NPR cycle per character transmitted.

As many as 16 DH11's may be placed on a single PDP-11 processor, creating a total capacity of 256 lines.

Models Available

The DH11 Multiplexer is available in five variations:

The DH11-AA consists of a double system unit, all modules necessary to implement a 16 line asynchronous multiplexer, an externally mounted 14 cm (5 $\frac{1}{4}$ inch) level conversion and distribution panel with its own power supply that can be mounted on the rear of the rack, and a data cable between the logic in the double system unit and the level conversion/distribution panel.

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The modules for level conversion are not included, so that the type and quantity of lines may be customized to the customer's requirements.

The DH11-AB is the same as the DH11-AA, but does not include the level conversion/distribution panel or its associated power supply. A data cable suitable for connecting the DH11-AB to the DC08CS telegraph converter panel is supplied instead of a cable to a distribution panel.

The DH11-AC is the same as the DH11-AA, except that the power supply for the level conversion/distribution panel is arranged for 240 V, 50 Hz operation. (There is no need for a 50 Hz version of the DH11-AB because it is a processor-powered option).

All of the above versions of the DH11 include pre-wired slots in the double system unit for the insertion of the DM11-BB modem control (not included in the basic DH11).

The DH11-AD consists of a double system unit, all modules necessary to implement a 16-line asynchronous multiplexer, including modem control (programming is same as DM11-BB programming), necessary level converters for EIA RS232-C interfacing and an externally mounted DJ11 distribution panel. This is a self-contained unit for applications where line interfacing flexibility is not needed.

The DH11-AE is the same as the DH11-AD except it does not include modem control. Includes EIA level conversion for data leads only.

Operation-Receiver

Reception on each line is effected by means of Universal Asynchronous Receiver/Transmitters (UARTs). These are 40-pin MOS/LSI circuits which perform all the necessary functions for double buffered asynchronous character assembly.

The receiver section of the UART samples the line at 16 times the bit rate of the signals to be received on that line. Upon detection of a Mark-to-Space transition, the UART counts 8 clock pulses and checks the line. This sampling will occur in the center of a normal start bit. If the sample is a Mark, the receiver returns to its idling state, ready to detect another Mark-to-Space transition. If the sample is a Space, the receiver samples the line at subsequent sample points spaced 16 clock ticks from the center of the start bit. The number of samples taken is determined by

the "character length" information entered into the UART via the Line Parameter Register. If parity checking has been enabled for this line, the receiver logic computes the parity of the character just received and compares it with the parity sense specified for reception on that line. If the parity sense differs, the parity error bit will be set.

The character length, parity sense, number of stop bits, etc. that will be used by the UART to perform the above operations are stored within

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each UART in a Control Bits Holding Register. The Control Bits Holding Registers are addressable on a write-only basis from the UNIBUS, by first setting the "line selection bits" of the System Control Register and then loading the desired line parameters into the Line Parameter Register. Then they will automatically be transferred to the Control Bits Holding Register of the designated UART. It is important that no interrupt handling routine intervene and change the contents of the System Control Register during the above operation.

The Silo

The silo is a MOS/LSI digital storage buffer that is 16 bits wide and 64 words deep. A 16-bit word is entered at the top, and automatically shifted down to the lowest location that does not already contain an entry. The bottom of the silo is the Next Received Character Register.

There are three registers associated with the silo. The Next Received Character Register is a read-once register and is the bottom of the silo. Reading it extracts a character from the silo and causes all other entries to shift down one more position.

The other two registers are byte-size registers and are contained within the Silo Status Register. The high byte is read only and contains the status of an up-down counter giving the actual fill level of the silo. The low byte (bits 7-0) is read/write, and contains the number of characters which must be loaded into the silo before an interrupt request will be generated. Details of these registers can be found in the Section on Programming under the heading "Silo."

Received Character Distortion

Received characters may contain up to 43.75% distortion on any bit, due to the sampling rate. However, the overall bit rate must be accurate. Specifically, errors in bit rate are cumulative such that when the receiver samples the first stop bit to see if it is a mark (if not, it's a "framing error") the error accumulated by that time must not exceed 43.75% of a bit time. The accumulated error (called "gross start-stop distortion") is calculated as clock error x number of data bits plus one, plus the bias distortion of the final character. Assuming the reception of eight data bits, or seven data bits plus parity, 4.8% speed distortion would be permissible. Speed distortion (clock error, bit rate error) of any amount poses severe problems in an echo situation, however. If a terminal sends to the DH11 at a slightly fast rate and the DH11 sends the exact same characters back to the terminal at the correct rate, the DH11 silo will eventually fill with un-echoed characters. This problem would not occur with keyboard terminals, but high speed tape senders should have their transmission speeds carefully checked before use with the DH11 or any other asynchronous communications interface. The acceptable tolerance is $\pm 0, - 4\%$. In computing speeds, one may assume the DH11 receiver clock to be accurate within .05%.

Operation-Transmitter

Transmission on each line is also effected by means of UARTs. These 40-pin MOS/LSI chips perform all the necessary functions for double-buffered asynchronous character transmission. The transmitter section of the UART holds the serial output line at a Marking state when idle. When the transmitter loading leads have been conditioned with the character to be transmitted and the data strobe lead has been brought high (these functions are performed by the NPR control), the UART will generate a start space within one sixteenth of a bit time. The start space and all subsequent data bits are a full bit time each. The start space is followed by 5, 6, 7, or 8 data bits, as determined by the control bits holding register. (See Receiver Hardware for a description of the UART control bits holding registers and how they are loaded from the Line Parameter Register). The data bits are presented to the lines least significant bit first. The parity bit, if parity generation is enabled, is calculated by the transmitter and affixed after the last data bit, but before the stop marks.

The number of stop bits depends upon the setting of the control word. If the transmission of 6, 7, or 8 bits has been selected, the program may select either one or two stop bits. If the transmission is in 5-bit code, the program may select either one or one and a half stop bits.

If the transmitter's holding register has been loaded while a character was being transmitted, that second character will have its start bit commence immediately at the end of the preceding character's stop bit(s).

The transmitter timing circuit is driven by the same crystal clock as the receiver, and is accurate to .05%.

The Auto-Echo Feature

The DH11 hardware is capable of echoing received characters without software intervention. The feature may be enabled on any line by conditioning the line selection bits in the System Control Register and then setting the appropriate bits in the Line Parameter Register.

The auto-echo hardware is part of the receiver scanner and operates as follows:

- 1) If the receiver scanner finds a received character for a line on which auto-echo is NOT enabled, it loads that character into the silo and resumes scanning.
- 2) If the receiver scanner finds a received character for a line on which auto-echo IS enabled, it examines the error flags associated with that character.
 - a) If a framing error is detected, the remote terminal may be trying to gain the attention of the processor by sending a "Break." In this case, the auto-echo hardware dumps the received character and associated flag into the silo so that the system software will be alerted. The Break is not echoed to the remote terminal.

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- b) If an overrun error is detected, this may mean that the remote terminal is trying to gain the attention of the processor by typing characters. This case is treated identically to 2a, above.
- 3) If the receiver scanner finds a received character from a line upon which auto-echo is enabled and there are no error flags of the type mentioned above, the receiver scanner and auto-echo logic will attempt to echo the character. First, however, certain tests of internal logic conditions will be made.
- a) The UART transmitters are all loaded from a common internal data bus. Therefore, the auto-echo hardware must first check to see that no NPR cycles are in progress loading a UART transmitter from that bus. If a conflict is indicated, the receiver scanner is restarted and the process will be tried again on the scanner's next rotation.
 - b) If the above test indicates no problem, the one remaining check is to see if the Transmitter Holding Register for the line on which the character was received is available. If it is not, the scanner is restarted. If it is available, auto-echo commences.

It should be noted that it is not advisable to transmit messages on a line and auto-echo characters received on that line simultaneously. The auto-echo hardware will interlock these functions to some degree, but if more than two characters are received on a line while the scanner is waiting for the transmitter holding buffer to become available, a data overrun will occur and characters will be lost. In short, auto-echo and software-driven transmission should not be attempted on the same line simultaneously if input from that line is expected.

SILO INTERRUPT HANDLING

The DH11 provides increased received character throughput by averaging the received character interrupt routine entry/exit time over a number of received characters. If it takes 30 microseconds to enter and exit an interrupt routine and 30 microseconds to process a character, the average time per character in a conventional character interrupt device would be 60 microseconds. If it takes 30 microseconds to enter and exit an interrupt routine and 960 microseconds to process 32 characters in a silo, the average time per character in a DH11 would be 31 microseconds or roughly half that of a conventional device.

The above example of increased throughput suggests that the DH11 received character silo alarm level be set at 32. Certain cautions should be observed in doing this in an interactive system, however. Specifically, a real time clock should be used to insure that terminal users receive a response within a guaranteed maximum time interval. The operating program would service the silo whenever the alarm occurred or the clock ticked, whichever came first.

Alternately, the alarm level can be set at zero and still obtain many of the advantages of silo operation. Obviously, the silo permits a high de-

DH11

gree of latency by storing received characters whenever the operating program is unable to service the silo due to demands of other devices. Furthermore, when the operating program does service the silo there will be a great many characters stored there and the interrupt averaging effect described earlier will be used to full advantage. Thus the silo helps throughput the most in those situations when the most help is needed.

DMA Transmission

In a DMA transfer system, a computer peripheral, such as the DH11, obtains data from (or deposits data in) computer memory without the aid of the computer processor. This process is commonly called Direct Memory Access (DMA), although in the case of a PDP-11, it is referred to as a Non-Processor Request (NPR).

All that is required from a programming standpoint to perform NPR's is an indication of which memory location is desired, whether one wishes to read from that location or write into it, and to how many consecutive memory locations one wishes access.

For example, if one wished to transmit the letters A, B, C from computer memory to some distant location, one would prepare a message table in memory:

```
00 000 000 11 000 011 (Location 5002)
11 000 010 11 000 001 (Location 5000)
```

In this example, a sixteen bit PDP-11 word is shown containing two eight bit "bytes". The byte at location 5000 is the ASCII code for "A". The byte at location 5001 is the ASCII code for "B". (Note that the odd numbered locations are the left hand byte of the even numbered locations.) Finally, the byte at location 5002 is an ASCII "C". The all-zeroes byte at location 5003 is not to be sent.

In the DH11 or a similar device, one would load the transmitter "current address" register for the appropriate line with "5000" and the transmitted "byte count" register with "-3". Then one should set the BAR bit for the line on which transmission is to occur. The DH11 hardware would gain control of the Unibus, read the 11 000 001 from location 5000, transmit the "A", increment the current address to 5001, increment the byte count to -2, wait for the "A" to finish going out onto the line and then repeat this process. The process would continue until the byte count was incremented to "zero" and would then stop. It is because "zero" is an easy number for computer hardware to recognize that byte counts are usually loaded as negative quantities by the program and up-counted to zero by the hardware.

In the DH11, any memory location, including those with extended addresses may be used and message tables can cross extended address boundaries if desired. Any message length up to 32,768 bytes may be transmitted.

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Since no processor action is required for each character transferred by the NPR cycles, a very high data transfer rate is possible if message lengths are long enough to make the program time necessary to load the current address and byte count small relative to the number of characters transmitted.

Modem Control Multiplexer DM11-BB

In cases where the DH11 is used in public switched networks such as DDD, or TWX, the modem control multiplexer DM11-BB should be used. The control multiplexer provides the necessary control leads to interface with the Bell 103 and 202 type modems or equivalent. All leads meet EIA RS-232-C and CCITT electrical specifications. The DM11-BB is not required with the DH11-AD and cannot be used with the DH11-AE.

Channel Interfaces

Multiplexer Distribution Panel and Power Supply for DH11-AA, AC.

The DH11 provides a panel for level conversion and cabling of the individual lines. The panel uses a standard H911 style rack, with 6 connector blocks.

Note that the slot assignments follow the DF11 (standard level conversion and cable slot for all PDP-11 communications products) format. Slot A6 through A21 is used for level conversion and slot B6 through B21 is used for cabling out. Other slots provide inputs or special purpose outputs. The unit mounts on the standard 48.3 cm (19 in.) cabinet and connects to the PDP-11 via the BC08-S data cable.

Power for the distribution panel is provided by the H751-C power supply mounted on the rear door of the cabinet.

The H751-C provides the following voltages:

- + 5 V at 4 A
- + 15 V at 2 A
- 15 V at 2 A

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
USAGE	M971 CABLE*2	M971 CABLE*2	M971 CABLE*2	** 2	** 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	M594 1 * 2	
A				LINE 08 THRU LINE 11	LINE 12 THRU LINE 15	LINE 00 CONTROL LEADS	LINE 01 CONTROL LEADS	LINE 02 CONTROL LEADS	LINE 03 CONTROL LEADS	LINE 04 CONTROL LEADS	LINE 05 CONTROL LEADS	LINE 06 CONTROL LEADS	LINE 07 CONTROL LEADS	LINE 08 CONTROL LEADS	LINE 09 CONTROL LEADS	LINE 10 CONTROL LEADS	LINE 11 CONTROL LEADS	LINE 12 CONTROL LEADS	LINE 13 CONTROL LEADS	LINE 14 CONTROL LEADS	LINE 15 CONTROL LEADS	LINE 08 THRU LINE 11	
USAGE	M971 CABLE*2	M971 CABLE*2	M974 ▲▲ 2	** 2	** 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2	▲ 2
B	LINE 00 THRU LINE 15			LINE 00 THRU LINE 03	LINE 04 THRU LINE 07	LINE 00 OUTPUT	LINE 01 OUTPUT	LINE 02 OUTPUT	LINE 03 OUTPUT	LINE 04 OUTPUT	LINE 05 OUTPUT	LINE 06 OUTPUT	LINE 07 OUTPUT	LINE 08 OUTPUT	LINE 09 OUTPUT	LINE 10 OUTPUT	LINE 11 OUTPUT	LINE 12 OUTPUT	LINE 13 OUTPUT	LINE 14 OUTPUT	LINE 15 OUTPUT	LINE 00 THRU LINE 03	
USAGE	*** 2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
A	LINE 12 THRU LINE 15																						
USAGE	*** 2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
B	LINE 04 THRU LINE 07																						

* LEVEL CONVERSION OF CONTROL LEADS. ONE SLOT PER LINE. USE M594 ONLY WHEN DM11-BB IS IMPLEMENTED.
IF DM11-DB IS USED REPLACE M594 WITH W404-A [SUPPLIED WITH DM11-DB]. IF DM11-DA IS USED LEAVE BLANK.

** USE M594 FOR DM11-DB

*** USE M596 FOR DM11-DA

▲ USE ONLY IF DM11-BB IS IMPLEMENTED

▲▲ DATA CABLE FROM DH11-AA CONTROL LOGIC

▲▲▲ 16 CABLE SLOTS ONE PER LINE FOR DM11-DA USE M973, FOR DM11-DB USE BC01R-25

▲▲▲ JUMPER CARD USED FOR DIAGNOSTIC PROGRAMS ONLY, REMOVE FOR NORMAL OPERATION.

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Power drain of the distribution panel depends on the type of level conversion used. The maximum draw occurs when EIA levels are used with modem control (DM11-BB is implemented).

For this configuration the following power is used:

- + 15 V at 1.4 A
- 15 V at 1.4 A
- + 5 V at 1.7 A

Note that level converter types can be mixed on a 4-line basis by using different converters in slots A4, A5, B4 and B5. Also level converter types can be mixed on a single line basis by using slots A6 through A21 for level conversion on a single-line basis.

Programming

Double-Buffered Receivers—General

Double-buffered receivers contain two registers, one of which is a Shift Register. The character being received from the communications line is shifted into this register a bit at a time. The second register is a Holding Register. When the Shift Register has assembled a complete character, that character is transferred in a parallel fashion into the Holding Register. At that time a flag is set and the hardware or software using the double-buffered receiver can access the Holding Register and remove or copy the data stored there. When the Shift Register has assembled another character, that character will be transferred into the Holding Register, obliterating the character previously stored there. If this action takes place before the data in the Holding Register has been accessed, a Data Overrun flag will be set, indicating that data was lost.

Double-Buffered Receivers—DH11

The UARTs used in the DH11 are MOS/LSI units, each containing a double-buffered receiver and a double-buffered transmitter. In the DH11, the flags indicating presence of data in the receiver's Holding Registers are scanned by a automatic hardware scanner which copies data from the Holding Registers into the silo if storage space is available. (If that space is not available, and the scanner finds a flag indicating a holding register with data in it, the Storage Overflow bit (System Control Register, bit 14) is set, and an interrupt is generated. The setting of this bit does not necessarily mean that data has been lost. Rather, it indicates that data will be lost if the hardware scanner is unable to service (i.e. dump into the silo) the data in one or more Holding Registers before additional characters arrive on those lines. Actual data loss will become evident to the program when characters are received with the Data Overrun bit set. (See the description of the Next Received Character Register.)

Silo

The silo, actually more similar in operation to a granary, is a first-in first-out buffer store. A parallel-loaded 16-bit word (see Next Received Character Register for the format) automatically propagates downward into

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the first location not already containing a word. In the case where the silo is empty, this means that the word would propagate directly into the Next Received Character Register.

The propagation time from the top of the silo to the bottom may be as much as 32 microseconds. For this reason, the hardware is arranged such that the Receiver Interrupt is not generated until the number of characters in the silo exceeds the silo alarm level AND there is at least one character in the bottom of the silo. This arrangement is necessary because the up-down counter that indicates the number of characters in the silo counts both those resting in the bottom and those propagating downward. While the hardware arrangement protects the case where the silo is empty and the alarm level is zero, the fact still remains that the number of characters in the silo and the number actually available to be serviced may differ due to the propagation time. For this reason, character handling programs should not assume there is some particular number of characters in the silo when servicing begins. Rather, the program should extract a character, check the Valid Data Present bit (bit 15) and handle the character; then the program should extract the next character and repeat the process until bit 15 no longer tests as "1." At that time, the silo may be assumed to be empty (although there may be another character propagating downward) and the character handling routine may be terminated until another Receiver Interrupt is received.

On very fast processors, such as the PDP-11/45, the program should avoid reading the Next Received Character Register more often than once per microsecond, as it takes one microsecond for characters in the silo to shift downward one position. Since the typical program will be checking bit 15 and moving the character to some location in memory, it is not anticipated that this speed restriction will present a problem.

Zero Bauds

A speed selecton of zero bauds is provided so that the program may turn off any line. This is useful if excessive circuit noise on an unused line causes annoying quantities of bogus characters.

BREAK Signals

When the Break Control Register has been conditioned to transmit a break signal on a particular line, DH11 logic immediately forces the output on that line to the SPACE (0) condition. The duration of this signal may be timed as described below.

The generation of a Transmitter Interrupt occurs when the last character of a message is loaded into a UART transmitter from a message table in PDP-11 core. At that time the program sets up a new message in core and loads the appropriate current address and byte count so that the new message can begin when the old one is finished.

It is important to note that the former message is not finished when the Transmitter Interrupt is given. Rather, the use of the core table is finished. In terms of the serial communications line, there are two more

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characters left. One of these characters is in the UART transmitter's Shift Register; the other is in the UART transmitter's Holding Register.

Therefore, sending a Break signal requires loading two nulls and waiting for a transmitter interrupt before setting the appropriate bit in the Break Control Register. In this way, generation of a Break will not interrupt the transmission of any valid characters. In like manner, nulls should be used to time the transmission of a Break signal so that when the Break condition is terminated, no valid characters will be produced from the UART Shift and Holding Registers.

Interrupts

There are two kinds of receiver interrupts:

Receiver Interrupt (System Control Register, bit 7)

This interrupt, when enabled, occurs whenever the number of entries in the silo exceeds the silo status alarm level. (The program can determine the actual silo fill at any time by examining the high byte of the Silo Status Register.)

Storage Overflow Interrupt (System Control Register, bit 14)

This interrupt, when enabled, occurs whenever the character storage silo is full and the DH11 hardware needs to store an additional character. This does not necessarily mean that data has been lost. (See the section on "Programming.")

There are two kinds of transmitter interrupts; both are enabled by bit 13 of the System Control Register:

Transmitter Interrupt (System Control Register, bit 15)

This interrupt, if enabled, occurs when one or more lines finish the transmission of a complete string of characters. Specifically, it occurs after the NPR cycle that loads the last character to be transmitted (and hence that increments the byte count to zero).

Non-Existent Memory Interrupt (System Control Register bit 10).

This interrupt, when enabled, occurs whenever the DH11 addresses non-existent memory; specifically, this interrupt occurs if the DH11 enters an NPR cycle, places an address on the Unibus, and fails to receive a slave sync response for that request within 20 microseconds.

Address and Vector Assignment

The DH11 uses floating addresses and is located after DJ11's in the floating address space that begins at location 760 010. Because the DH11 has eight registers, it must be assigned an address that is a multiple of 20 (octal). All DH11's in a system should have consecutive addresses.

Example #1: A system with no DJ11's but two DH11's:

760 010 Cannot use for DH11's because not multiple of 20.

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760 020 First DH11
760 040 Second DH11
760 060 DH11 Gap (Indicates that there are no more DH11's).

Example #2: A system with one DJ11, two DH11's:

750 010 First DJ11
760 020 DJ11 Gap (Indicates that there are no more DJ11's).
760 030 Cannot use for DH11's because not multiple of 20.
760 040 First DH11
760 060 Second DH11
760 100 DH11 Gap (Indicates that there are no more DH11's).

The DH11 vectors (2) follow those of the DJ11 in the floating vector space that starts at address 300. The vectors starting at 300 are used in the following order: DC11; KL11/DL11-A, B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Readers; PA611 Punches; DT11; DX11; DL11-C, D, E; DJ11; DH11.

The receiver vector is the lower numbered vector. The priority of the receiver and transmitter interrupts are individually selectable by means of two standard PDP11 priority jumper plugs. BR level 5 is standard.

Register Definition

The following chart presents the bit assignments within each register: Bits marked Unused and Write Only are always read as zero. Attempting to write into Unused or Read Only bits has no effect on those bits. INIT refers to the Initialize signal generated by the processor (e.g. upon execution of a RESET instruction.) Transmit and Receive are with respect to the DH11. All bits in the accompanying diagrams are shown in the state they assume on POWER CLEAR or INIT.

The System Control Register—Address X00

15	14	13	12	11	10	9	8	7	6	5	4	3	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

The System Control Register is a byte-addressable register. The bit assignment is as follows;

BITS **DESCRIPTION**

00-03 Line Selection

Each of the 16 lines served by the DH11 has its own storage for line parameter information, current address, and byte count. These storage locations are loaded by the program via the Line Parameter Register, Current Address Register, and Byte Count Register, but the hardware must first be told which line is to have its line parameters, current address, or byte count changed. This routing is accomplished by setting the Line Selection bits to the binary address (0000-1111) of the desired line. These bits are read/write.

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- 04, 05 **Memory Extension**
The information stored in these bits becomes bits 16 and 17 respectively of any current address loaded by the program into the Current Address Register. These bits are read/write but, when read, represent only the status of bits 4 and 5 of the System Control Register, NOT the status of address bits 16 and 17 of the selected line. See the Silo Status Register for further information. This arrangement permits interrupt service routines to save the contents of the System Control Register accurately.
- 06 **Receiver Interrupt Enable**
This bit, when set, enables receiver interrupts (bit 7)
- 07 **Receiver Interrupt**
This bit, when set, indicates that the number of characters stored in the silo exceeds the "alarm level" specified by the low byte of the Silo Status Register. This bit is read only, except in maintenance mode, where it is read/write. Setting of this bit will generate an interrupt request if bit 6 (above) is also set.
- 08 **Clear Non-Existent Memory Interrupt**
This bit, when set, clears the non-existent memory interrupt flip-flop (bit 10) and clears itself. This bit is read/write.
- 09 **Maintenance**
This bit, when set, places the DH11 in maintenance mode.
- 10 **Non-Existent Memory**
This bit is set whenever the NPR hardware places the addresses of a memory location on the UNIBUS and no slave sync is received in 20 μ s. This indicates that the addressed location or device does not exist. This bit causes an interrupt request if set while Transmitter and Non-Existent Memory Interrupt Enable is set. This bit is read only, except in maintenance mode, where it is read/write.
- 11 **Master Clear**
This bit, when set, generates "Initialize" within the DH11, clearing the silo, the UARTs, and the registers. The exact bits cleared are discussed in the section on initialization. Read/Write.
- 12 **Storage Interrupt Enable**
This bit, when set, permits the setting of bit 14 to generate an interrupt request. This bit is read/write.
- 13 **Transmitter and Non-Ex-Mem Interrupt Enable**
This bit, when set, permits the setting of bit 10 or 15 to generate an interrupt request. This bit is read/write.
- 14 **Storage Interrupt**
This bit is set when the receiver scanner finds a receiver holding buffer with a character in it, tries to store that character in the silo, and cannot do so because of a lack of space. When set this

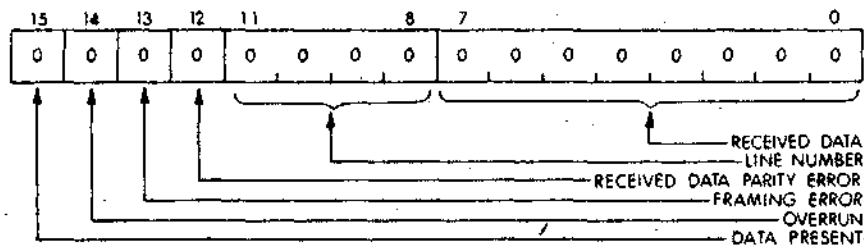
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bit will cause an interrupt request if bit 12 is set. This bit is read only, except in Maintenance Mode, where it is read/write.

15 Transmitter Interrupt

This bit is set when the DH11 concludes an NPR cycle that incremented a byte count to zero, indicating the last character in a message buffer was loaded into a UART transmitter Holding Register. This bit will cause an interrupt request if bit 13 is set. This bit is read/write. (It is set during an NPR cycle.)

Next Received Character Register Address X02



BITS DESCRIPTION

00-07 Next Received Character

These bits contain the next received character, right justified. The least significant bit is bit 00.

08-11 Line Number

These bits indicate the line number on which the next received character was received. Bit 8 is the least significant bit.

12 Parity Error

This bit is set if the parity of the received character does not agree with that designated for that line.

13 Framing Error

This bit is set if the receiver samples a line for the first stop bit, and finds the line in a spacing condition (logical 0). This condition usually indicates the reception of a Break.

14 Data Overrun

This bit is set when the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer. Refer to the section on Programming for further details on double-buffered reception.

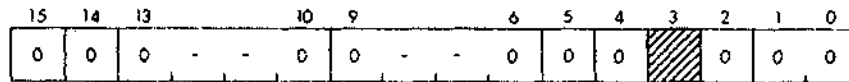
15 Valid Data Present

This bit indicates that the data presented in bits 14-00 is valid. It permits a character handling program to take characters from the silo until it is empty. This is done by reading this register and checking bit 15 until a word is obtained for which bit 15 is a zero.

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The entire Next Received Character Register is read-only and is addressable only on a word basis.

Line Parameter Register Address X04



This register should be loaded only after the line selection bits of the System Control Register have been set to select the line to which these parameters apply. This register is write only.

BITS DESCRIPTION

00-01 Character Length

These bits should be set as shown to receive and transmit characters of the length (excluding parity) shown:

bit 01 00

0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

02 Two Stop Bits

This bit, when set, conditions a line transmitting with 6-, 7-, or 8-bit code to transmit characters having two stop marks. If the line is transmitting 5-bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop marks. If this bit is not asserted, 1 stop mark is sent.

03 Not Used.

04 Parity Enabled

If this bit is set, characters transmitted on this line will have an appropriate parity bit affixed, and characters received on this line will have their parity checked.

05 Odd Parity

If this bit and bit 4 are set, characters of odd parity will be generated on this line and incoming characters will be expected to have odd parity. If this bit is not set, but bit 4 is set, characters of even parity will be generated on this line and incoming characters will be expected to have even parity. If bit 4 is not set, the setting of this bit is immaterial.

06-09 Receiver Speed

The state of these bits determines the operating speed for this line's receiver. The speed table below is applicable.

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10-13 Transmitter Speed

The state of these bits determines the operating speed for this line's transmitter. The speed table below is applicable.

Speed Table for Receiver and Transmitter Speeds:

	Bit				
Transmitter	13	12	11	10	
Receiver	9	8	7	6	
	0	0	0	0	Zero Baud
	0	0	0	1	50 Bauds
	0	0	1	0	75 Bauds
	0	0	1	1	110 Bauds
	0	1	0	0	134.5 Bauds
	0	1	0	1	150 Bauds
	0	1	1	0	200 Bauds
	0	1	1	1	300 Bauds
	1	0	0	0	600 Bauds
	1	0	0	1	1200 Bauds
	1	0	1	0	1800 Bauds
	1	0	1	1	2400 Bauds
	1	1	0	0	4800 Bauds
	1	1	0	1	9600 Bauds
	1	1	1	0	External Input A
	1	1	1	1	External Input B

14 Half Duplex/Full Duplex

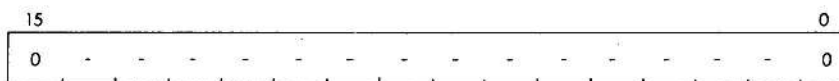
If this bit is set, this line will operate in half-duplex mode. If not set, this line will operate in full-duplex mode.

In this application half-duplex means that the DH11 receiver is blinded during transmission of a character.

15 Auto-Echo Enable

When this bit is set, characters received on this line will be hardware echoed. See the discussion of Auto-Echo for further details.

Current Address Register Address X06



This register should be loaded only after the System Control Register (SCR) has had the appropriate bits set to select the desired line number. When this register is loaded, address bits 00-15 are transferred into semiconductor memories in the DH11 from bits 00-15 of this register. Address bits 16-17 are transferred into semiconductor memories in the DH11 from bits 4-5 of the System Control Register.

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Interrupts must be inhibited or the SCR saved between the setting of the SCR bits 0-3 and the read or write of the Current Address Register.

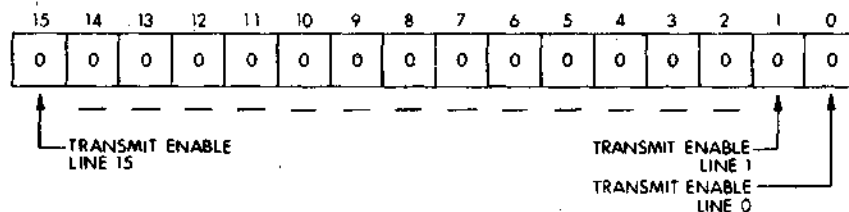
When this register is read, it will indicate the current address of the line selected by the System Control Register. Bits 16 and 17 will appear in the Silo Status Register, bits 6 and 7.

Byte Count Register Address X10

In the same fashion as the Line Parameter and Current Address registers, this register should not be loaded or read without first selecting a line number by means of the lower-order four bits of the System Control Register. This register should be loaded with the two's complement of the number of characters (bytes) to be transmitted on that line. The byte count register is read/write.

Interrupts must be inhibited or the SCR saved between the setting of the SCR bits 0-3 and the read or write of the Byte Count Register.

Buffer Active Register (BAR) Address X12



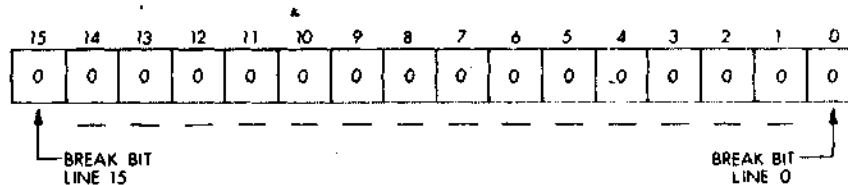
This register contains one bit for each line. The bits are individually set using BIS instructions. Setting a bit initiates transmission on the associated line. The bit is cleared by the hardware when the last character to be transmitted is loaded into the transmitter Data Holding Register of the UART for that line. It should be noted that while the clearing of a BAR does indicate that a message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters will be sent after the BAR bit clears. These are the last two characters of the message; one of them was just starting when the BAR was cleared and one was that final character that was loaded into the holding register, thus clearing the BAR bit. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request to Send. Request to Send (RTS) should not be dropped until at least two character times after the BAR bit for a given line clears.

This timing may be effected by sending two extra (null) characters in a message and dropping RTS when BAR clears.

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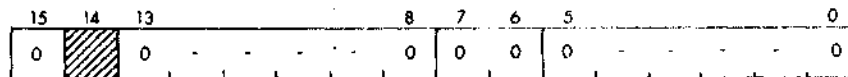
Clearing a BAR bit should not be used to abort transmission on a line. Rather, the byte count for that line should be set to zero. The Buffer Active Register bits are read/write.

Break Control Register Address X14



This register contains one bit for each line. Setting a bit in this register will immediately generate a Break condition on the line corresponding to that bit number. Clearing the bit will terminate the Break condition. The Break condition may be timed by sending characters during the Break interval, since these characters will never actually reach the line. Further comments concerning the transmission of Break signals may be found in the Break Signals Section.

Silo Status Register Address X16



This register is actually two byte-sized registers. The bit assignments are:

Bit Description and Operation

00-05 Silo Alarm Level

The program may load an integral power of 2 between 0 and 63 into this location (e.g., 0, 1, 2, 4, 8, 16, or 32). When the number of characters stored in the silo exceeds that number, an interrupt request (System Control Register bit 7) is generated, if System Control Register bit 6 is set. These bits are read/write.

06-07 Read Extended Memory

These bits are read only and contain the A16 and A17 bits of the current line address to which the line selection bits of the System Control Register are pointing.

08-13 Silo Fill Level

These bits are an up-down counter that indicates the actual number of characters in the silo. It should be noted that there are six bits, hence numbers between 0 and 63 can be represented. A full silo has 64 entries and the fill level appears as 00000, but one may easily tell the difference between an empty silo (00000) and a full silo (00000) by checking the Storage Overflow bit (bit 14 of System Control). These bits are read only.

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- 14 Unused
- 15 Reserved for Maintenance

MODEM CONTROL MULTIPLEXER DM11-BB

In cases where the DH11 is used in public switched networks such as DDD, or TWX, the modem control multiplexer DM11-BB should be used. The control multiplexer provides the necessary control leads to interface with the Bell 103 and 202 type modems or equivalent. All leads meet EIA RS-232-C and CCITT electrical specifications.

DM11-BB Modem Control Option

Each DM11-BB modem control multiplexer contains two registers and requires two addresses. Address space has been assigned for 16 DM11-BB modem control multiplexers. The first DM11-BB is at 770500. The second starts at 770510, etc. to the 16th at 770670. The two registers and their addresses are listed below for DM11-BB unit xx.

Register	Address
Control and Status Register	770xx0
Line Status Register	770xx2

Each DM11-BB requires one interrupt vector. The vector addresses are assigned from 300 to 777.

All units are shipped with the bus request line set to BR4.

Control and Status Register (770XX0)

BIT	NAME	DESCRIPTION
15	Ring Flag	When DONE is set, this flag indicates that a Ring OFF to ON transition has been detected at line #--. This bit is read only and is cleared by Initialize and Clear Scan.
14	Carrier Flag	When DONE is set, this flag indicates that a Carrier Flag transition has been detected at line #--. This bit is read only and cleared by Initialize and Clear Scan.
13	Clear to Send	When DONE is set, this flag indicates that a Clear to Send transition has been detected at line #--. This bit is read only and cleared by Initialize and Clear Scan.
12	Secondary Receive Flag	When DONE is set, this flag indicates that a Secondary Receive transition has been detected at line #--. This bit is read only and cleared by Initialize and Clear Scan.
11	Clear Scan	Clears all Read/Write functions. Additionally, the Scan Decoder is set to 0 and the Scan Memory Logic is cleared. This function is useful for having

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BIT	NAME	DESCRIPTION
		the Hardware Test and Interrupt on all lines that have an On condition (CO, CS, Sec T). Clear occurs when a ONE is written into this bit position.
10	Clear Multiplexer	Clear Multiplexer clears the request to Send, Terminal Ready, Secondary Transmit, and Line Enable flip flops when a ONE is written into this bit position.
9	Maintenance Mode	The Scan Input (Ring, Clear to Send, Carrier, and Sec Rx) to a ONE or ON state Utilizing Step or SCAN EN with MAINT MODE will exercise 100% of the Scan Logic (not the data multiplexers). This includes the Interrupt Circuits (M7820) and the Address Selector (M105). This mode provides a diagnostic feature, as well as an on line test facility for the DM11-BB's interaction with the Unibus. This bit is Read/Write and cleared by Initialize and by Clear Scan.
8	Step	STEP, when set to a ONE, causes the Scan to increment the Line Number and test that line for interrupts causing transitions. Step may be used in place of Scan Enable but care should be exercised that the Scan rate is great enough (milliseconds) such that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires $1 \mu\text{sec} \pm 10\%$ to execute. This bit is Write One's only.
7	Done	The DONE flag set to a ONE indicates that the hardware SCAN has detected a transition requiring an Interrupt to the program. An Interrupt will occur if Interrupt Enable is on (a ONE). Additionally, DONE set to a ONE inhibits the SCAN clock and makes available to the programmer: (a) the Line Number that caused the Interrupt; (b) the status of the flags (4 bits); (c) modem status (8 bits). The SCAN will be released again when DONE is reset. This bit is Read/Write and cleared by Initialize and Clear Scan.
6	Interrupt Enable	Allow Interrupts on Priority four if set to a ONE. This bit is Read/Write and cleared by Initialize and Clear Scan.
5	Scan Enable	A ONE allows the scan to test all lines for Ring, Carrier, Clear to Send, and Sec. Receive Interrupts. If the SCAN EN flip flop is negated while the Ring Counter is cycling (i.e. DONE not set), the Ring Counter will come to rest in $1 \mu\text{sec}$

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BIT	NAME	DESCRIPTION										
		$\pm 10\%$ (max). The LINE register must not be changed until BUSY (Bit 4) is cleared, or line number transitions may be lost. This bit is Read/Write and cleared by Initialize and Clear Scan.										
4	BUSY	Set when Scan is cycling, Reset at end of Clear Scan or Init. Read Only. Must be tested for 0 before changing the registers.										
3-0	Line Number	The LINE NUMBER bits are the Binary Addresses for the DM11-BB's 16 lines (0-15) as follows: <table><thead><tr><th>Bit 3210</th><th>Line #</th></tr></thead><tbody><tr><td>0000</td><td>0</td></tr><tr><td>0001</td><td>1</td></tr><tr><td>etc</td><td>etc</td></tr><tr><td>1111</td><td>15</td></tr></tbody></table> <p>If the Scan is cleared by Initialize or Clear Scan, the Line Number Register will settle in 16 μsec 10%. When settled, the Line Number Register will be set to Line #0 (0000). NOTE: When the Scan is Enabled (or STEP) the next line to be tested will always be Line #1. These bits are Read/Write and cleared by Initialize and Clear Scan.</p>	Bit 3210	Line #	0000	0	0001	1	etc	etc	1111	15
Bit 3210	Line #											
0000	0											
0001	1											
etc	etc											
1111	15											

Line Status (770XX2)

7	Ring	Modem status of the Ring lead. This bit is Read Only.
6	Carrier	Modem status of the Carrier lead. This bit is Read Only.
5	Clear to Send	Modem status of the Clear to Send lead. This bit is Read Only.
4	Secondary Receive	Modem status of the Secondary Receive lead. This bit is Read Only.
3	Secondary Transmit	When set, presents a MARK to the modem's Secondary Transmit lead. This lead is Read/Write and is cleared by Initialize and Clear Mux.
2	Request to Send	This lead is used to condition the modem to transmit if all other conditions are met. This bit is Read/Write and cleared by Initialize and Clear Mux.
1	Data Terminal Ready	This lead allows the modem to enter and maintain data mode. This bit is Read/Write and cleared by Initialize and Clear Mux.

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- 0 Line Enable This bit enables the state of Ring, Carrier, Clear to Send and Sec Rx to be sampled by the program and to be tested for transitions. This bit is Read/Write and cleared by Initialize and Clear Mux.

Maintenance Bits and Their Function

Setting of SCR 09 (Maintenance) does the following:

- 1.) It enables the program to write SCR07 (Receiver Interrupt), SCR 10 (Non-Ex-Memory Interrupt), and SCR 14 (Storage Overflow Interrupt) bits. This write capability is normally not enabled as it can produce hardware/software synchronization problems unless carefully done.
- 2.) It loops the Transmitted Data leads (Serial Out, line 00-15) to the Received Data leads (Serial In, line 00-15).

Setting of Silo Status Register 15 (Silo Maintenance):

The setting of bit 15 in SSR causes the inputs of the silo to be set to a 10101010101010 bit pattern, and a single 16-bit character made up of this pattern to be loaded into the silo. Successive clears and sets of SSR 15 will repeat this procedure. All receiver speeds should be set to 0 and the silo emptied before this is done, so that no data from the incoming serial lines will be placed in the silo while it is under test.

Specifications

Function:

The DH11 is a program-controlled interface between the PDP-11 UNIBUS and 16 asynchronous bit serial communications channels. The DH11 receiver section provides conversion of binary serial asynchronous (start-stop) signals to parallel binary data, and temporary buffering of that data. The DH11 transmitter section provides retrieval of parallel binary data from PDP-11 memory and conversion of that data to binary serial asynchronous (start-stop) signals for transmission over data communications channels.

Operating Modes:

Each individual channel may be set to operate in half- or full-duplex mode, under program control. In half-duplex, the receiver for a channel is disabled during transmission of a character on that channel. Any individual channel may be set, under program control, to echo (retransmit) received characters automatically.

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Individual receivers may be continuously disabled under program control.

Data Format:

Asynchronous, serial-by-bit to/from the communications channel. Parallel-by-character to/from the UNIBUS. The serial data format is one start bit; 5, 6, 7, or 8 data bits; none or 1 parity bit (odd or even); and 1, 1½ (5 level codes only), or 2 stop bits per character. All data format parameters are individually program selectable for each channel. The data format for the receiver and transmitter on a given channel, however, is the same.

A one in any bit of a character presented by the program to the DH11 for transmission will cause a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero presented by the program will cause a Spacing (logical 0) condition to appear. A Marking condition on the Received Data lead during any data bit sampling interval will be presented to the program as a one in the Next Received Character Register, and a Spacing condition will be presented as a zero.

Order of Bit Transmission and Reception:

Low order bit first

Data Rates:

The operating data rate (Baud rate) of the receiver and transmitter on each channel is independently program selectable from among the following 14 rates:

0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, and 9600 Baud. In addition, any two other speeds between 40 and 110 Baud, and between 312.5 and 9600 Baud may be added as options, by ordering an M405 or M401 clock module at the proper frequency (desired bit rate x 16).

Distortion:

The DH11 receiver will operate properly in the presence of up to 43% distortion between any two code elements (intersymbol distortion). The long term (within any one character) speed variation of the received data may not exceed $\pm 4.3\%$, provided that the auto-echo feature is not used. If auto-echo is used, the long term (greater than one character time) speed variation of the received data may not exceed 0 to -4% . The DH11 receiver clock is accurate to within $\pm .05\%$ of the nominal data rate. The DH11 transmitter will introduce less than 2% intersymbol distortion, with a long term stability of $\pm .05\%$.

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Physical Arrangement:	The DH11-AA and DH11-AC are comprised of a pre-wired, double PDP-11 system unit suitable for mounting in a PDP-11/40 or PDP-11/45 or equivalent cabinet; and all logic cards necessary to implement a 16-line multiplexer. Also included is an externally mounted distribution panel, 14 cm by 48.3 cm (5½ x 19 in.), with separate power supply for individual channel termination. The DH11-AA and -AC system unit and distribution panel are pre-wired for plug-in installation of the DM11-BB 16-line Data set Control Multiplexer. The DH11-AB is supplied without distribution panel, but with cables for connection to the DIGITAL DC08 Telegraph Line Subsystem Option.
Environmental Information:	The DH11 will operate at temperatures between +5° and +45° C, and at relative humidities between 0% and 95%, noncondensing.
Bus Loading:	Each DH11 presents 2 unit loads to the PDP-11 UNIBUS. The DM11-BB Data set Control Multiplexer, if present, represents one additional unit load. The DH11-AD is three loads and the DH11-AE is two loads.
Power Consumption:	The DH11 logic draws 8.4 A of +5 Vdc, and 240 mA of -15 Vdc. If the DM11-BB Data set Control Multiplexer is added, the total current drain is 11.2 A at +5 Vdc. The DH11-AD and DH11-AE use 10.8 A at +5 V, 0.4 A at +15 V, and 0.65 A at -15 V.
Electrical Interface:	Connection between the DH11 logic and the distribution panel is via a cable containing 16 input and 16 output data lines at Transistor-Transistor Logic levels (0, +5 Vdc). The logic levels are: Mark (logical 1) = 0V, Space (logical 0) = +3 V. Input leads from the distribution panel are equipped with pull up resistors which clamp open input lines in a logical 0 (space) condition. However, logic in the DH11 receiver section prevents this from assembling continuous all-zero characters. The electrical and physical interface to the external channels is provided by optional level conversion module sets (DM11-DA, -DB, -DC) that plug into the distribution panel. These options are described in the next section.

Models

Connection to Switched Network (DDD Net) Data sets

DEC No.	PREREQUISITE	DESCRIPTION
DH11-AA	PDP-11	Programmable 16-line asynchronous serial line multiplexer and distribution

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		panel, includes space for mounting up to four line adapters (16 line interfaces). Power requirement is 115 Vac, 60 Hz, 600 W.
DH11-AC	PDP-11	Same as DH11-AA except 230 V, 50 Hz, 600 W.
DM11-BB	DH11-AA or DH11-AC	16-line modem control multiplexer provides program operation of control leads for 103, 202 or equivalent data sets. Mounts in DH11-AA or DH11-AC.
DM11-DC	DM11-BB	Line adapter which implements four EIA/CCITT-compatible lines equipped with data set control features. Includes 25-foot data set cables.
or DH11-AD	PDP-11	Programmable 16-line asynchronous multiplexer and distribution panel with built-in level conversion for EIA/CCITT compatible lines equipped with data set control features. (Cables are not included).

Private Line Modems (No Control) or Local EIA Terminals

DH11-AA	PDP-11	See above -AA
DH11-AC	PDP-11	See above -AC
DM11-DB	DH11-AA or DH11-AC	Line adapter which implements four EIA/CCITT lines (data only). Includes four 25-foot modem cables. Note that the -DB can be used on a switched network system. This requires that the data set have Auto Answer strapped on. The data set will answer a call automatically. Not provided in this type of operation is the ability to not answer a call, the ability to initiate a disconnect by the computer, and the ability to sense an intermittent carrier.
or DH11-AE	PDP-11	Programmable 16-line asynchronous serial line multiplexer and distribution panel with built-in level conversion for EIA/CCITT compatible lines (data only). Cables are not included).

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Local Teletypes

DH11-AA	PDP-11	See above DH11-AA
DH11-AC	PDP-11	See above DH11-AC
DM11-DA	DH11-AA or DH11-AC	Line adapter for four 20 mA Teletype lines (data only).
DEC No.	Prerequisite	Description
DH11-AB	PDP-11	Programmable 16-line asynchronous serial line multiplexer and connecting cable to DC08CS mounting panel. (Does not include DC08CS.) Up to 2 DH11-AB's plug into one DC08CS.
DC08CS	DH11-AB	Telegraph or Telex line adapter distribution panel. Mounts line adapters for interfacing between the DH11-AB and telegraph or Telex lines. Accommodates up to 16 dual, solid-state telegraph line adapters, type DC08CM (Each DC08CM provides two telegraph line interfaces).
DC08CM	DC08CS	Dual solid-state telegraph line adapter; provides transmit and receive switching of two lines, in half duplex or duplex, neutral or polar operation. This unit is used with either externally supplied neutral or polar transmit and receive line power or internally supplied transmit line power (793 or 793A).
DC08EB	DC08CS	Line current adjusting option. Provides rheostats on each send and receive line for adjusting send and receive line current. Meter is provided for current monitoring.
DC08D	DC08CS	Line terminator panel. Provides screw terminal connection points for interfacing the DC08CM telegraph line adapters to telegraph lines. Can accommodate up to 32 lines with four connections provided for each.
793	DC08CM	Line power supply for driving a maximum of 32 telegraph lines (transmit only). Can drive unipolar or bipolar lines, ± 45 V to ± 80 V and 80 mA per line. For operation with 115 V, 60 Hz, 700 W.

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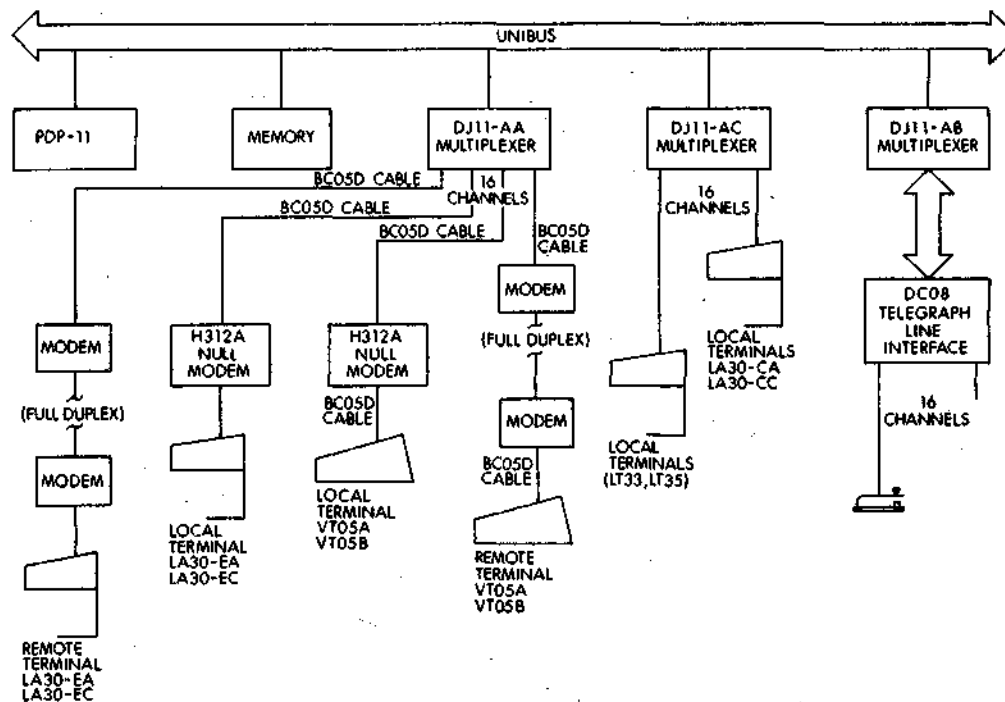
793A	DC08CM	Same as 793 except 230 V, 50 Hz, 700 W.
893	DC08CS, DC08CM.	Fuse panel for up to 32 lines. Fusing for both transmit and receive lines.

Related Options

The following options are useful in connecting various terminals and channels to the DH11.

Option No.	Prerequisite	Description
H312-A	None	Null modem. Required for local connection of terminals with EIA-compatible interfaces such as the DIGITAL VT05B, LA30EA, the Hazeltine 2000, etc., to the standard DM11-DB or DM11-DC modem interface.
BC05D-15	None	Modem cable. 7.6 m, 25-conductor cable terminated in Cinch DB25S socket at one end and Cinch DB25P plug at the other. Used with DH11-AD and DH11-AE to extend standard DM11DB or DM11DC modem cable.
DF11-BB	DH11-AA, DH11-AC	Integral Modem. Single line, answer-only, integral modem which plugs into the DH11-AA distribution panel. It is compatible with Bell 103A and 113A datasets. The DF11-BB connects to a Bell System type CBS or CDT Data Access Arrangement.
DF11-K	DH11-AA DH11-AC	Current mode interface. This is a TTL to active or passive 4-wire current mode (20 mA) loop converter. Connector provided is Amp Mate-n-Lok for connection with customer-supplied cable. Signalling rates up to 2400 Bauds, at distances up to 1500 feet.
M405		Clock Card. Required to provide non-standard speed (Ext. A or Ext. B) for DH11. M405 frequency ordered should be 16 x desired Baud rate. Minimum rate is 312.5 Bauds, maximum is 9600 Bauds.
M401		Clock Card—as above except minimum rate is 40 Bauds, maximum is 110 Bauds.

16-LINE ASYNCHRONOUS SERIAL LINE MULTIPLEXER, DJ11



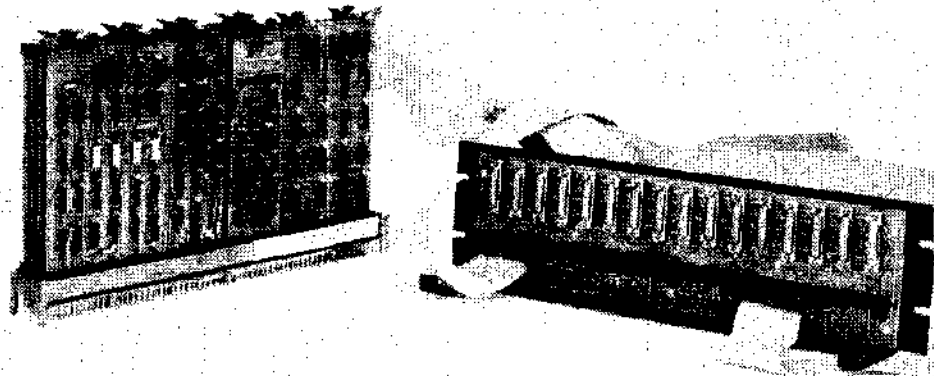
The DJ11 is a multiplexed interface between 16 asynchronous serial data-communications channels and the PDP-11 UNIBUS. The DJ11 is a low-cost, high-performance unit whose character formats and operating speeds are jumper or switch selectable in groups of four lines. The customer may select from 11 standard speeds (75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, or 9600 Bauds); four character sizes (5, 6, 7, or 8 data bits); three parity configurations generated and checked by the hardware (odd, even, or none); and three stop code lengths (1 and $1\frac{1}{2}$ stop bits for 5 data bits, 1 and 2 stop bits for 6, 7, or 8 data bits), also generated and stripped by the hardware.

MODELS AVAILABLE

Three models of the DJ11 are available, differing only in the type of input/output level conversion they provide.

The DJ11-AA furnishes level conversion conforming to the Electronic Industries Association (EIA) Standard RS232C, and to CCITT Recommendation V.24, supporting Transmitted and Received Data leads only. The Data Terminal Ready and Request To Send leads are permanently asserted (ON). The DJ11-AA is suitable for connection to local terminals with EIA interfaces, to private-line modems, and to dial network data sets, where computer control of the data set is not required. An externally mounted interface panel with 16 Cinch DB25P EIA connectors is provided for attachment of data set cables (not supplied).

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The DJ11-AB is supplied without level conversion, but with cables which bring the TTL signals out of the mounting cabinet. This allows connection to external signal-conditioning equipment, such as the DIGITAL-supplied DC08 Telegraph Line Interface Options, and customer-supplied special interface equipment.

The DJ11-AC furnishes 20-milliampere active neutral current-loop level conversion, suitable for operating DIGITAL-supplied terminals, such as the LA30-CA and LA30-CD DECwriters, VT05A and VT05B Display Terminals, LT33 and LT35 Teletypewriters, and RT01 or RT02 Data Entry terminals. An externally mounted distribution panel with 16 four-screw terminal strips is provided for connection of customer terminals.

OPERATION:

General

The DJ11 is a buffered, multiplexed interface between 16 asynchronous serial communications channels and the PDP-11 UNIBUS. It performs serial-to-parallel and parallel-to-serial conversion of serial start-stop data with double character buffered MOS/LSI circuits called UART's (Universal Asynchronous Receiver Transmitters). These circuits provide the logic necessary to double buffer characters in and out, to serialize-deserialize data, to provide selection of character length and stop code configuration, and to present status information about the UART and each character. A 64-character, first-in/first-out buffer is provided in the hardware to hold characters as they are received.

Receiver

The receiver section performs serial-to-parallel conversion of 5-, 6-, 7-, or 8-level codes. The desired character length is switch selectable in four-line groups. That is, all lines within each group of four lines (lines 0-3, 4-7, etc.) will expect the same character format, i.e., number of data bits, duration of stop element (stop code) and parity sense. For any line, the character format is the same for both the received and the transmitted data. The receiver data rate (Baud rate) is jumper selectable from among 11 standard speeds, also in four-line groups. These speeds are 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 Bauds. The receiver data rate for any four-line group may be different from the transmitter data rate for that group. Each receiver samples the line at 16 times the data rate.

The duration of the stop element is switch selectable, again in four-line groups. Values available are 1 or $1\frac{1}{2}$ bit times for characters with 5 data bits, and 1 or 2 bit times for characters with 6, 7, or 8 data bits.

As each character is received, it, along with the four-bit number of the line it came from and four bits of status information, is stored in a 16-bit wide by 64-word deep first-in/first-out hardware buffer, called a 'Silo.' This storage occurs at the time the center of the first stop bit of the character is sampled. Each complete character is loaded into the top of the silo and propagates (falls) automatically toward the 'bottom' of the silo, until it comes to rest against the bottom, or against the last previous character stored in the silo. The bottom of the silo is actually the Receiver Buffer Register (RBUF) and is seen, by the program, as a device register on the UNIBUS. Thus, there are no accesses to the UNIBUS at all until a complete character is received, stripped of start and stop bits, checked for proper parity (if required), and stored in a hardware buffer.

Indications of character words available from the silo and of device status are provided to the program by the Control Status Register (CSR).

The exact definition of each bit in CSR is given in the section on Programming, but the functions of the bits related to the DJ11 receiver section are discussed in the following paragraphs.

At the time a received character word appears in RBUF the Receiver Done bit (bit 7) is set in the CSR. If the Receiver Interrupt Enable bit (bit 7) is also set in CSR, an interrupt request is generated. The BR level is set by a priority jumper plug, and is the same for receive and transmit. BR 5 is standard.

In order to operate on received characters, the program tests bit 15 of RBUF for a 1 (data present). If bit 15 is set, the program moves the word from RBUF. This causes the silo to shift, automatically, all other characters it may contain 'down' one position, with the next received character appearing in RBUF not more than $1.4 \mu\text{s}$ later. Thus the program may disable received character interrupts, entering the receiver service routine on a timed basis and 'clearing out' the silo each time, or it may respond to an interrupt on each character.

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The parity sense for received data is switch selectable in four-line groups. The DJ11 offers a choice of odd, even, or no parity. If odd or even parity is selected, the receiver assumes that the bit received after the *n*th data bit (where *n* is the number of data bits selected) is the parity bit, and compares that bit with the parity of the *n* received data bits. If the parity is correct, the parity bit is discarded, and the *n* data bits are retained and placed in the received character buffer (silos). If the parity is incorrect, the hardware will set the Parity Error bit (PE, bit 12) of the received character word before storing it in the silo. If no parity is selected for a particular line group, parity is not checked and bit 12 will never be set.

Note that if odd or even parity is selected, the total character length is the sum of the start bit, plus the number of data bits selected, plus the parity bit, plus the number of stop bits selected.

If, at the time the center of the first stop bit should appear on a particular received data line, that line is found to be in a spacing (0) state, the Framing Error bit (FE, bit 13) will be set in the received character word. Such a condition may occur, for instance, if the data line goes open, or if the terminal connected to that line transmits a Break signal. In these cases all bits of the data character will be zero. Succeeding all-zero or Break characters, however, will not be assembled by the UART on that line or put into the silo. The received data line must return to a marking condition for 1/16 of a bit time before character assembly is resumed.

The Overrun bit (OR, bit 14) is an indication that the DJ11 receiver scanner has failed to remove a completed character from the UART before the next character was moved in on top of it. This only occurs if the silo has completely filled, and the program fails to respond to a FIFO Full flag. Since each UART is double buffered (32 complete characters), in addition to the 64-character silo buffer, this condition is unlikely to occur unless the program servicing the DJ11 is faulty. By means of a split-lug jumper, the DJ11 can be wired to give a Receiver Interrupt after having stored 5, 9, or 17 characters in the silo instead of interrupting on each character.

A Receiver Enable bit (CSR Bit 0) is provided which, when cleared, prevents the DJ11 from depositing characters in the silo.

The program can set the DJ11 for half-duplex operation (all channels simultaneously) by asserting bit 1 (Half-Duplex Select) in the CSR. Half-duplex, for the DJ11, means that if a character is in the process of being transmitted on a given line, the receiver associated with that line is disabled.

The entire silo and all 16 UART's may be cleared by assertion of CSR bit 3 (MOS Clear). Since more than one instruction time is required to clear the LSI circuits, CSR bit 4 (Busy Clear) is provided as a flag. Bit 4 is asserted any time the MOS Clear is in process. No load operations to the DJ11 or reads, of other than bit 4 of the CSR, should be attempted while bit 4 is set. MOS Clear causes all transmit lines to assume a marking (logical 1) state.

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It should be noted that 'clearing' the silo only clears the Data Present bit (bit 15) in the Receiver Buffer Register (RBUF) and does not affect the state of any RBUF bits. These RBUF bits may contain anything, and will be updated each time a new character is presented to the program.

The DJ11 hardware asserts CSR bit 13 (FIFO Full) anytime the receiver scanner finds a line with a character available, but cannot load the new character into the silo. If CSR bit 12 (Status Interrupt Enable) is also set, an interrupt request is generated. The assertion of FIFO Full does not necessarily mean data has been lost. On any given line, there will be one character time between the time the character is presented to the receiver scanner, and the time Overrun actually occurs. In the worst case (9600 Bauds, 7 bit characters) the program has approximately 700 μ s to respond to the FIFO Full Interrupt and remove characters from the silo before any data is actually lost. The receiver scanner runs at about a 1 MHz rate, and so scans each UART many times during one character time.

Transmitter

The transmitter section of the DJ11 performs parallel-to-serial conversion of data supplied to it from the UNIBUS. The character length and stop code for any given line are the same as for the receiver on that line. The transmitter data rate, however, is jumper selectable in four-line groups, independent of the receiver data rate.

The transmitter for each line is fully double buffered. That is, the program has a full character time to respond to the Transmit Ready (bit 15) flag from any line, and still transmit data on that line at its maximum character rate.

The transmitter section of the DJ11 is operated by the program through four registers on the UNIBUS: The Control Status Register (CSR) previously mentioned, the Transmitter Control Register (TCR), the Transmitter Buffer Register (TBUF), and the Break Control Register (BCR).

To initiate transmission, the program sets CSR bit 8 (MASTER TRANS SCAN ENB). If it is desired to have the transmitter section give an interrupt when a character is requested, the program also sets CSR bit 14 (TRANS INT ENB). The Transmitter Control Register (TCR) is used to select an individual line for transmission. In order to set and clear bits in TCR, it is required that CSR bit 10 (BREAK REG SEL) be cleared (0). If the line-select bit in TCR associated with a particular line is set, and the transmit character buffer (TBMT) in the UART for that line is empty, the DJ11 transmitter scanner stops when it reaches the selected line. CSR bit 15 (TRANS RDY) will be set, and, if CSR bit 14 (TRANS INT ENB) is set, an interrupt request is generated. The BR level is the same as for the receiver. BR 5 is standard. When the transmitter scanner stops, the line number to which it is pointing will be contained in the Transmitter Buffer Register (TBUF) in bits 8-11. These bits are read only.

The program may then read the line number and furnish a new character to be transmitted on that line, by loading the character in TBUF, or the

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program may clear the line select bit in TCR. Either action clears CSR bit 15 (TRANS RDY) and allows the transmitter scanner to continue.

It should be noted that the so-called 'transmitter scanner' is not really a scanner, but is, instead, a 16-level priority encoder. The practical effect of this is that when any line is serviced as described above, the next line requiring service will be found and the TRANS RDY bit (CSR bit 15) set in 1.3 μ s or less, independent of the line number. Thus, the hardware allows the program to perform transmit service in a very efficient manner on all active lines on one entry to the transmit service routine. The transmit character buffers in the UART's are sampled every 400 ns. Line 15 has the highest priority, and line 0 the lowest. For mixed-speed configurations, the highest-speed line should be connected to DJ11 lines 15-12, the next highest to lines 11-8, etc.

The normal rest condition of the Transmitted Data lead for any line is Marking (1). A continuous Spacing (0) signal may be applied to a line by means of the Break Control Register (BCR). The program addresses the BCR by setting CSR bit 10 (BREAK REG SEL). The program may then cause a continuous Spacing condition on a particular line by setting the Break Bit in BCR for that line. The Spacing condition remains on the Transmitted Data lead as long as the Break Bit is set for that line. If characters are supplied to the transmitter for that line, however, it continues to appear to the program as if they are being sent normally. This provides the facility for sending precisely timed spacing signals, by asserting the Break Bit and using the Transmit Ready Interrupts as a timer.

It should be remembered in this context that each line in the DJ11 is double buffered internally. This means that when the transmitter section gives a TRANS RDY and an interrupt, it has just started sending the last character loaded into TBUF (not finished). When the transmitter is used as a timer for sending Breaks, the program should ensure that the characters sent, or at least the final one, are all ones (Marks), else the line may remain in a spacing condition longer than desired.

Line Interfaces

The Line-Distribution Panels supplied with the DJ11-AA and DJ11-AC are used to fan out the lines to the outside world.

The DJ11-AA is supplied with an electrical interface and connectors which meet the specifications of Electronic Industries Association Standard RS232C, and CCITT Recommendation V.24, for the Transmitted Data (Circuit BA, pin 2) and Received Data (Circuit BB, pin 3) leads.

The DJ11-AC is supplied with an active electrical interface which furnishes a nominal 20 mA at 20 V dc, for operation of local neutral Teletype terminals and other terminals operating on 20 mA neutral current loops.

The DJ11-AB is supplied without level conversion (TTL input-output levels) and without a Line Distribution Panel, for control of DIGITAL-supplied DC08 Telegraph Line Interface equipment.

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The DJ11-AA and DJ11-AC Panels do not require that power be supplied to them, that is, they are completely passive. These panels can be mounted across a 19-in. rack or flat against a wall. Level conversion of the TTL signals is performed within the DJ11. The level-converted data are sent from the DJ11 to the Distribution Panel by two flat cables which terminate in Berg connectors. The Distribution Panel fans out the lines to Individual Cinch DB25P connectors (DJ11-AA) or four-wire screw terminal strips (DJ11-AC) for each line. The TTY Distribution Panel (DJ11-AC) contains several components of the TTY circuit.

Several jumper selections are available on the Distribution Panels. In the EIA case, the Data Terminal Ready lead (Circuit CD, pin 20) and the Request To Send lead (Circuit CA, pin 4) normally are strapped to a positive or 'ON' voltage. This strapping can be removed individually (on a per-line basis). The DJ11-AA Distribution Panel also contains a Jumper that connects together the Protective Ground (Circuit AA) and Signal Ground (Circuit AB) leads from each channel. The jumper can be cut to separate the two grounds.

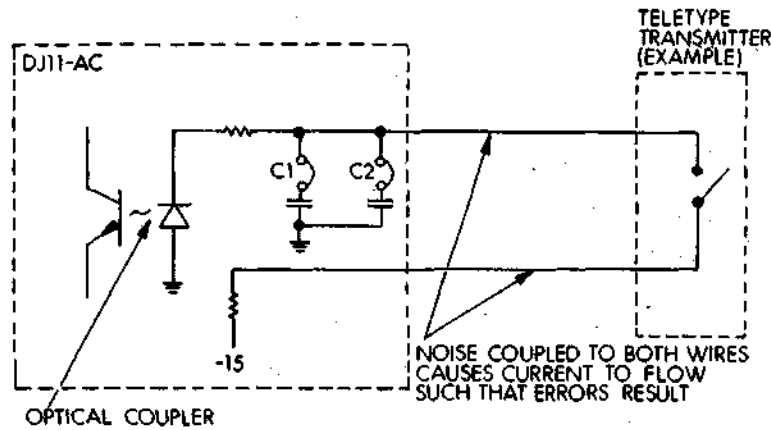
Two jumpers for each line exist on the DJ11-AC Panel (20-mA TTY). With these jumpers the receiver portion of the TTY circuit can be shifted from an active receiver (one that supplies the current source) to a passive one (where the remote equipment must supply the current). The active receiver is required for Teletypes and similar devices that provide a switch opening or closing for a binary one or zero. The disadvantage of this mode is that the signalling is single-ended and noise introduced on the line can cause errors. When wired as a passive receiver, the device has common-mode rejection, since any noise introduced on the wires appears on both wires and hence causes no net change in the current through the diode.

The DJ11-AC Panel also contains two other jumpers for each line. These are used to insert capacitors to filter out high frequency noise in the circuit. There are three speed ranges. The low-speed range is used for 300 Bauds and below; both capacitors are left in for this range. The filtering adds 10% distortion, maximum, to a 300-Baud signalling rate. The medium range is used for 2400 Bauds and below; capacitor C1 is removed, and the filtering causes 10% distortion, maximum, to a 2400-Baud signal. The high range is obtained when both capacitors are removed and should be used above 2400 Bauds. For the higher speed ranges it is preferable that the remote device be the current source so that the DJ11-AC receiver can be strapped as a passive receiver with common-mode rejection.

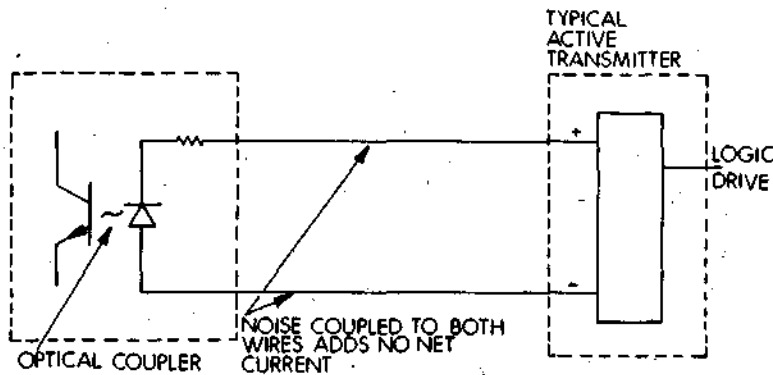
Maintenance Provisions

The DJ11 has a maintenance bit (CSR bit 2) which will, when set, loop back all 16 lines internally. Also, if split speed was selected on any or all of the groups, the transmitter speed will be forced to that of the receiver so that loop-back can occur.

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TTY RECEIVER WIRED AS ACTIVE



TTY RECEIVER WIRED AS PASSIVE

PROGRAMMING

General

The Interface between a program running in the PDP-11 processor and the DJ11 is via five device registers, two of which share a common address on the UNIBUS.

These registers are:

- Control Status Register (CSR), address 76XXX0
- Receiver Buffer Register (RBUF), address 76XXX2
- Transmitter Control Register (TCR), address 76XXX4
- Break Control Register (BCR), address 76XXX4
- Transmitter Buffer Register (TBUF), address 76XXX6

The functions of the bits provided in each register are defined below. Each register is assigned an 18-bit memory address, and may be read from or written into using any processor instruction that references these addresses, with the exceptions noted. Selection of BCR or TCR (BREAK REG SEL) is accomplished by setting or clearing CSR bit 10. If bit 10 is

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cleared (0) references to address 76XXX4 will reference TCR. If bit 10 is set (1), references to address 76XXX4 will reference BCR.

Interrupts

The DJ11 uses two interrupt vectors; vector address XX0 for the interrupt caused by Receiver Done (CSR bit 7) and FIFO Full (CSR bit 13), and vector address XX4 for Transmit Ready (CSR bit 15). Both interrupts operate independently, except that the receiver takes priority on simultaneous interrupt requests (is closer to the processor on the UNIBUS). Since the interrupt through vector address XX0 can come from two sources (Receiver Done and FIFO Full), it is necessary for the program to check both bits 15 and 13 each time the service routine for this interrupt is entered. The program must clear the bit which caused the interrupt request when exiting the service routine, else the occurrence of another interrupt-causing condition, while the first is being serviced, may fail to give an interrupt.

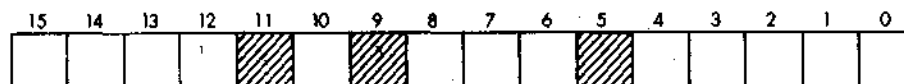
Address and Vector Assignment

The address assigned to the DJ11 is in the floating address space reserved for PDP-11 peripherals. The DJ11's for a system are assigned contiguous addresses in the range from 760 010₈ to 764 000₈. Each DJ11 requires 10₈ locations. Each unit uses two interrupt vectors, one for Receiver Done and FIFO Full (address XX0), and one for Transmit Ready (address XX4).

Register Definition

Bits marked 'Not Used' and 'Write Only' are always read as zero. Attempting to write into 'Not Used' or 'Read Only' bits has no effect on those bits. INIT refers to the initialize signal generated by the processor (e.g., upon execution of a RESET instruction). 'Transmit' and 'Receive' are with respect to the DJ11.

Control Status Register (CSR) 76XXX0



BIT DESCRIPTION AND OPERATION

- 15 Transmitter Ready. Read only. This bit is set whenever the transmitter scanner finds that the transmit-character buffer in the UART for line n (TBMTn) is able to accept a character for transmission and the line-select bit in the Transmitter Control Register (see below) for that line (TCRn) is set. The logical condition is then $CSR15 \leftarrow CSR8 * TMBTn * TCRn$ (*implies 'AND'). This bit is cleared by the hardware within 1 μ s after a character is loaded into the Transmitter Buffer Register (see below), negating TBMTn, or when TCRn is cleared. The transmitter scanner stops when Transmitter Ready is set, and resumes when it is cleared. If another line needs transmit service at the time bit 15 is cleared, bit 15 will be set

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again within 1.4 μ s of the completion of the bus cycle that loads TBUF or clears TCRn. This bit is cleared by INIT or by the actions described above.

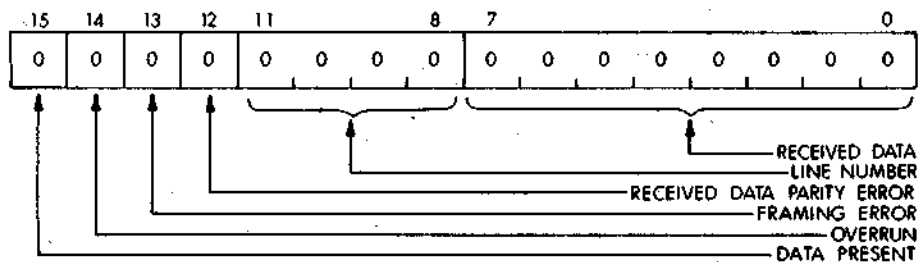
- 14 **Transmitter Interrupt Enable.** Read/Write. This bit, when set, causes an interrupt request to be generated whenever CSR bit 15 is set. This bit is cleared by INIT or by the program.
- 13 **FIFO Full.** Read only. This bit is set if the DJ11 receiver hardware attempts to load a character into the FIFO buffer and finds the buffer full. The receiver scanner continues to scan. This bit is cleared when the Receiver Buffer Register (see below) is read from, or by INIT.
- 12 **FIFO Buffer Status Interrupt Enable.** Read/Write. This bit, when set, causes an interrupt request to be generated whenever CSR bit 13 is set. This bit is cleared by INIT or by the program. The program servicing this interrupt should clear bit 12 upon entering the service routine, and should reset it upon exit, to make sure the hardware picks up all transitions of bit 13.
- 10 **Break Register Select.** Read/Write. This bit, when set, causes processor references to address 76XXX4, to access the Break Control Register (see below). When clear, this bit causes processor references to address 76XXX4 to access the Transmitter Control Register (see below). This bit is cleared by INIT or by the program.
- 8 **Master Transmit Scanner Enable.** Read/Write. This bit, when set, enables the transmitter hardware to scan the UART's for lines requiring transmit service. When clear, this bit prevents CSR bit 15 from being set. This bit is cleared by INIT or by the program.
- 7 **Receiver Done.** Read Only. This bit is set when a received character word appears in the Receiver Buffer Register (RBUF, see below). If CSR bit 6 is also set, an interrupt request is generated. This bit is cleared by an instruction which references RBUF. However, if another received character word is in the silo, this bit is reasserted and the new data appears in RBUF within 1.4 μ s. This bit is cleared by INIT or by the actions described above.
- 6 **Receiver Interrupt Enable.** Read/Write. This bit, when set, causes an interrupt request to be generated each time CSR bit 7 is set. This bit is cleared by INIT or by the program.
- 4 **Busy Clear.** Read only. This bit is set by the hardware whenever the MOS Clear process, initiated by CSR bit 3, is in progress. It is a flag to the program indicating that other bits in CSR and other registers of the DJ11 should not be accessed. This bit is set, then cleared, by the setting of CSR bit 3.
- 3 **MOS Clear.** Write only. This bit, when set, causes a 2 μ s clear pulse to be issued to the silo and all 16 UART's. During the clear pulse,

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CSR bit 4 is also set. This bit is set by the program and cleared by the DJ11 hardware.

- 2 Maintenance Mode: Read/Write. This bit, when set, causes all the Transmitted Data leads to be connected to their respective Received Data leads at the TTL outputs. The Transmitter data rate of each four line group is also forced to that of the receivers for that group. This bit is cleared by INIT or by the program.
- 1 Half-Duplex Select. Read/Write. This bit, when set, disables the receiver section of any line during the time the transmitter section of that line is active. This bit applies to all 16 lines. It is cleared by INIT or by the program.
- 0 Receiver Enable. Read/Write. This bit, when set, enables the receiver scanner to operate and enables received character words to be loaded into the silo. It is cleared by INIT or by the program.

Receiver Buffer Register (RBUF), 76XXX2



BIT DESCRIPTION AND OPERATION

- 15 Data Present. Read only. This bit, when set, indicates the presence of a received character and its associated line number and status bits in RBUF. This bit is cleared by the hardware when data is read from RBUF, but is set again within $1.4\mu\text{s}$ if more data is present in the silo. It is cleared by INIT or by setting CSR bit 3.
- 14 Overrun. Read only. This bit is set if data from the line specified in bits 11-8 of RBUF has been lost. This may occur if the silo fills up. The character in this received character word is the first good character after the data loss (rather than the last good character before the data loss). This bit is valid only for this character. All bits in RBUF are updated as each new received character word appears in RBUF.
- 13 Framing Error. Read only. This bit is set if the UART, at the time it samples the Received Data line in the center of the first stop bit, finds the line in a spacing (0) condition. This may indicate an open input line, a 'Break' signal, or excessive distortion of the Received Data character.
- 12 Received Data Parity Error. Read only. This bit is set by the UART

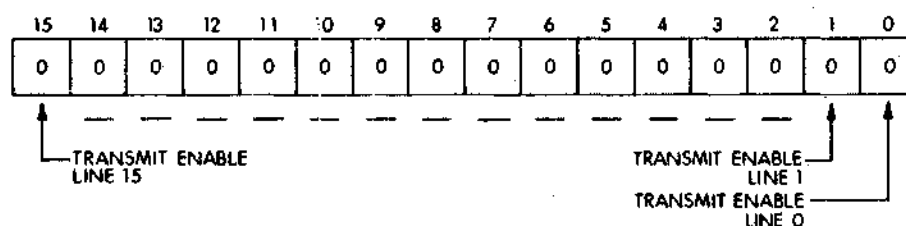
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if the parity of the received data character does not agree with the parity specified for this group of lines (odd or even). This bit is always zero if the 'no parity check' option is specified. Bits 14, 13, and 12 are updated for each new character.

11-8 Line Number. Read only. These bits are the binary number of the line from which the character in bits 7-0 of RBUF was received.

7-0 Received Data. Read only. These bits contain the complete character assembled by the UART. If the character length specified for this group of four lines is less than 8 bits, the character appears right justified (low-order bit in bit 0). The unused high-order bits will contain 0's.

Transmitter Control Register (TCR) 76XXX4

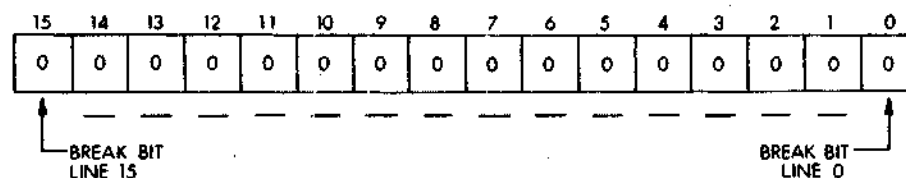


BIT DESCRIPTION AND OPERATION

15-0 Transmit Enable. Read/Write. Each bit in TCR enables the DJ11 transmitter scanner to flag that a character is required for transmission on one line. If the Transmit Enable bit in TCR is set for a particular line, CSR bit 8 is set, and the transmitted data buffer in the UART (TMBT) for that line is empty, then the scanner stops, CSR bit 15 is set, and, if CSR bit 14 is set, an interrupt request is generated. The line number at which the transmitter scanner is stopped appears in bits 11-8 of the Transmitter Buffer Register (TBUF, see below). The scanner restarts when TBUF is written into or when the TCR bit for the line whose number appears in bits 11-8 of TBUF is cleared. The bits in TCR are cleared by INIT or by the program.

Note that TCR may be accessed from the UNIBUS only if CSR bit 10 is cleared.

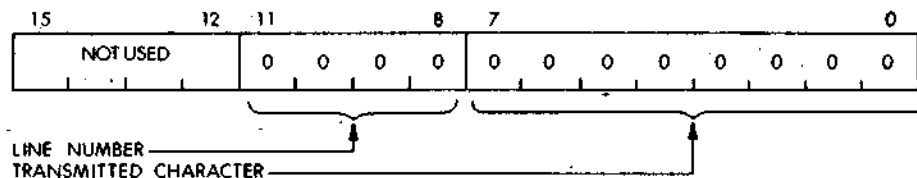
Break Control Register (BCR) 76XXX4



BIT DESCRIPTION AND OPERATION

15-0 Break Bit. Read/Write. Each bit in BCR controls the state of one Transmitted Data line. If the Break Bit in BCR is set for a particular line, that line is clamped in a Spacing (logical 0) state. This condition remains until the bit is cleared. The transmitter for that line appears to the program to function normally, however. This register may be accessed from the UNIBUS only if CSR bit 10 is set. BCR may be cleared by INIT or by the program.

Transmitter Buffer Register (TBUF) 76XXX6



BIT DESCRIPTION AND OPERATION

11-8 Line Number. Read only. If CSR bit 15 and the bit in TCR associated with the indicated line are set, these bits contain the four-bit number of the line requiring a character for transmission. Cleared by INIT. Note that bits 11-8 are valid only if CSR bit 15 is set.

7-0 Transmitted Character. Write only. The data character to be transmitted on the line whose number is contained in bits 11-8 of TBUF is loaded into these bits. If the data character contains fewer than 8 bits, the character must be right justified when loaded into TBUF. The bits of the data character are presented to the serial line low-order bit (bit 0) first. A bit set to a one in TBUF causes a marking condition to appear on the Transmitted-Data lead for the line whose number is in bits 11-8 of TBUF for one bit time. These bits are cleared by INIT. Note that bits 7-0 should only be loaded when CSR bit 15 is set. Loading TBUF with CSR bit 15 cleared results in the transmission of the character on line 0.

SPECIFICATIONS

- Function: The DJ11 provides an interface between the PDP-11 UNIBUS and 16 asynchronous bit serial communications channels.
- Connectability: A maximum of 16 DJ11's may be connected to a single PDP-11.
- Operating Mode: Half or Full duplex, under program control.
- Data Format: Asynchronous, serial by bit. One start and 1, 1½ (5-level codes only), or 2 stop bits supplied by the hardware. The DJ11 will accommodate characters of 5, 6, 7, or 8 bits, with or without even or odd parity.

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The data format is the same for transmitted and received data on any line. The data format is switch selectable in four-line groups.

A one (1) presented by the program to any bit in the Transmitter Buffer Register causes a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero (0) presented by the program causes a Spacing (logical 0) condition to appear. A Marking condition on the Received Data lead during any data-bit sampling interval is presented to the program as a one (1) in the Receiver Buffer Register, and a Spacing condition is presented as a zero (0).

**Order of Bit
Transmission and
Reception:**

Low-order bit first

Data Rate:

The DJ11 is supplied with 11 standard data rates: 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 Bauds. The data rate is jumper selectable in four-line groups. The data rate for the receivers in a group may be different from that of the transmitters in that group.

**Signalling
Performance:**

DJ11-AA: 15.2 m (50 ft) at up to 9600 Bauds with BC05D cable, or equivalent.

**DJ11 Distribution
Panel-to-Terminal
Distances:**

DJ11-AB: 3.7 m (12 ft) with supplied cable.
DJ11-AC: 5.5 m (18 ft) with DIGITAL BC04R-18 cable. With cable made with shielded twisted pairs, such as Belden no. 8777 or equivalent, the following rate/distance table may be used as a guide. This chart is for informational purposes only, and is not to be construed as a warranty by Digital Equipment Corp. of error-free operation of DJ11 at these speeds and distances under all circumstances.

150 m at 9600 Bauds
150 m at 4800 Bauds
450 m at 2400 Bauds
450 m at 1800 Bauds
450 m at 1200 Bauds
450 m at 600 Bauds
600 m at 300 Bauds and below

Distortion:

The DJ11 receiver operates properly in the presence of 40% space-to-mark or mark-to-space distortion between any two received-data bits, and up to

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$\pm 4.5\%$ long-term speed distortion, provided the data format contains a least $1\frac{1}{2}$ stop units. If the data format contains only one stop unit, the speed tolerance is $\pm 4\%$. The DJ11 transmitter operates with less than 3% bit-to-bit or long-term distortion.

Bus Loading: One DJ11 presents one unit load to the PDP-11 UNIBUS.

Physical Layout: The DJ11 consists of a single prewired PDP-11 system unit, suitable for mounting in a PDP-11/40, PDP-11/45, or equivalent cabinet, and all logic modules and cables necessary to implement a 16-line multiplexer. The DJ11-AA and DJ11-AC are supplied with an externally mounted, 14-cm high ($5\frac{1}{2}$ in.) Line Distribution Panel with connectors appropriate to type of channel to be connected. Cables to connect the Distribution Panel to data sets are not supplied but are available separately (see below).

The DJ11-AB is supplied with cables and connector cards that plug into the DC08 Telegraph Line Interface Option or into a standard DM11 Line Distribution Panel.

Note that the DJ11 cannot be mounted in a PDP-11/15 or PDP-11/20 processor box, or in a BA11ES extender box. See below for recommended mounting cabinet.

Electrical Interface: DJ11-AA: Provides a voltage-level interface for 16 lines whose signal levels and connector pinings conform to Electronic Industries Association Standard RS232C and CCITT Recommendation V. 24. The leads supported by the DJ11-AA are:

Protective Ground, Circuit AA (CCITT 101) pin 1.

Transmitted Data, Circuit BA (CCITT 103) pin 2.

Received Data, Circuit BB (CCITT 104) pin 3.

Signal Ground, Circuit AB (CCITT 102) pin 7.

Signal Ground and Protective Ground are connected together by a removable jumper on the DJ11-AA Distribution Panel:

In addition, the Data Terminal Ready lead, Circuit CD (CCIT 108.2) pin 20, and the Request to Send lead, Circuit CA (CCIT 105) pin 4, are clamped ON (logical 1). This condition may be removed on a per-line basis by removal of jumpers on the DJ11-AA Distribution Panel. If the jumpers are removed, how-

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ever, these leads are left floating (0 V dc). These circuits are terminated in 16 Cinch DB25P connectors mounted on a 14-cm-high by 48.3-cm-wide (5½ x 19 in.) Distribution Panel supplied with the DJ11-AA.

Cables with the proper connectors for connecting the Distribution Panel to modems or local terminals with EIA interfaces are available from DIGITAL as No. BC05D—25 (7.6m, 25 ft).

DJ11-AB: Provides standard Transistor-Transistor-Logic (TTL) Levels for 16 receive and transmit data leads on two cables 3m (10 ft) long, terminated in M971 cards. The pinning of these cards is such that they may be plugged into the DIGITAL-supplied DC08 Telegraph-Line Interface Option, or into the Distribution Panel supplied with the DM11 16-line Asynchronous Serial Line Multiplexer.

DJ11-AC: Provides 20-mA neutral active or passive (jumper option) current-loop circuits for 16 transmit and receive data leads. These circuits are terminated in 16 four-screw-terminal barrier strips mounted on a 14 cm-by-48.3 cm (5½ x 19 in.) Distribution Panel that can be mounted on the back door of a standard 48.3-cm (19 in.) rack, or mounted on any flat surface no farther than 3 m (10 ft) from the DJ11 logic.

Power Requirements:	DJ11-AA:	4.7 A at + 5 V dc
		0.25 A at - 15 V dc
		0.25 A at + 15 V dc
	DJ11-AB:	4.7 A at + 5 V dc
		0 A at + 15 V dc
		0.25 A at - 15 V dc
	DJ11-AC:	5.3 A at + 5 V dc
		0 A at + 15 V dc
		1.0 A at - 15 V dc

Heat Dissipation: 35 kg-cal/hr maximum

Environmental: The DJ11 operates at an ambient temperature of 5 to 50° C with relatively humidity of 10 to 95%, non-condensing.

Models

DJ11-AA: 16-line Asynchronous Serial Line Multiplexer, Full- or Half-Duplex operation. Electrical Interface meets Standards EIA RS232C and CCITT V.24. Supports Transmitted and Received-Supports Transmitted and Received-Data leads only.

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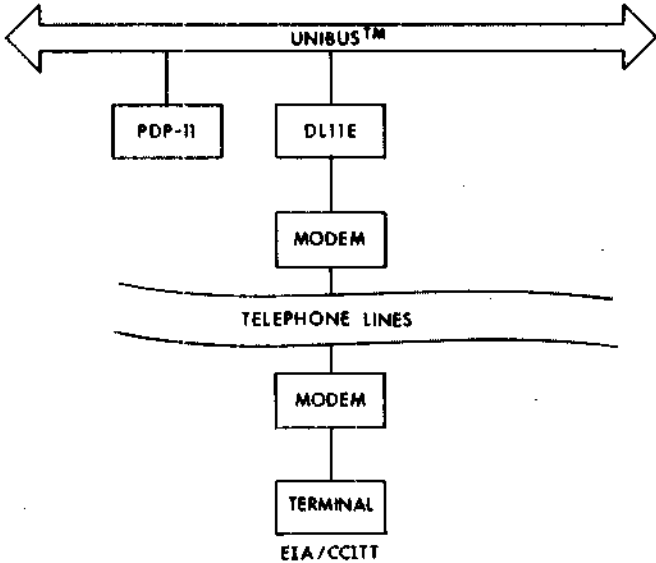
Request To Send and Data Terminal Ready leads clamped ON. Speed and character format strap selectable in four-line groups. Provides 5, 6, 7, or 8 data bits: 1, 1½, or 2 stop bits; even, odd or no parity. Provides standard data rates of 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 Bauds. Split-speed operation. Supplied with externally mounted Distribution Panel, but without modem cables. See Related Options for recommended cable.

- DJ11-AB:** As DJ11-AA above, except electrical interface is TTL levels (0,+5V) for Transmitted and Received Data leads only. Supplied without external Distribution Panel, but with cables and cards for connection to DC08 Telegraph Line Interface Options, or to the DIGITAL DM11-AA/AC Line Distribution Panel.
- DJ11-AC:** As DJ11-AA above, except electrical interface is 20-mA neutral active or passive current loop, for operation of local devices with 20-mA current-loop interfaces (Teletypes, LA30-CA and -CD, VT05-A and -B etc). Externally mounted Distribution Panel has screw-terminal strips to connect Transmitted and Received Data Leads from devices.

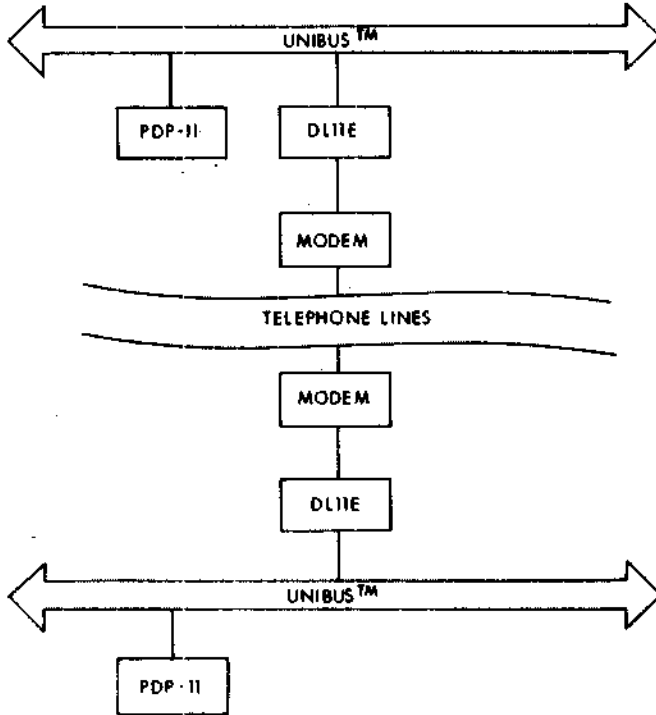
Related Equipment

- BC05-D-25 Cable** Modem Cable, 7.6 m (25 ft), 25-conductor cable terminated in Cinch DB25S socket at one end, and DB25P plug at the other end. For connection of one line from DJ11-AA Distribution Panel to modem, data set, or Null Modem listed below.
- H312A** Null Modem. Required for local connection of terminals with EIA interfaces, such as LA30-EA or -EC, Hazeltine 2000, etc. to BC05D cable from DJ11 Distribution Panel.
- BC04R-XX Cable** Four spade lugs to male Mate-N-Lok cable. For local connection of DIGITAL RT01 etc to DJ11-AC Distribution Panel. This cable is supplied in standard lengths of 3.7 m (12 ft, BC04R-12) and 5.5 m (18 ft, BC04R-18).
- H960-DA** Cabinet with single PDP-11/40 or PDP-11/45 Extension Mounting Box. Provides mounting space for nine system units (9 DJ11's). Includes power supply for 115-V, 60-Hz power.
- H960-DB** As above, except for 230-V, 50-Hz power.
- H960-EA** As H960-DA, except two boxes and two power supplies, providing space for 18 system units. For 115-V, 60-Hz power.
- H960-EB** As H960-DC above, except for 230-V, 50-Hz power.

SINGLE ASYNCHRONOUS SERIAL LINE INTERFACES, DL11

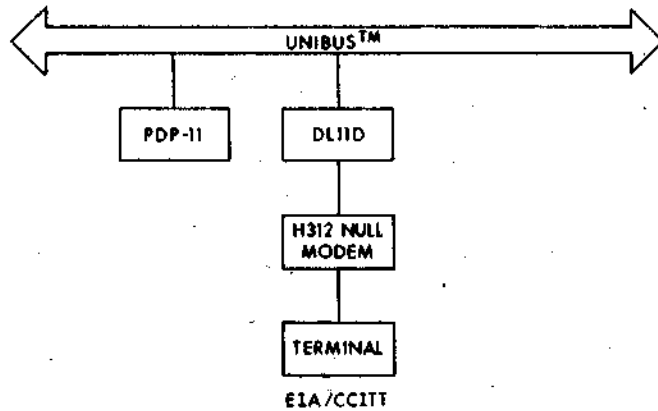
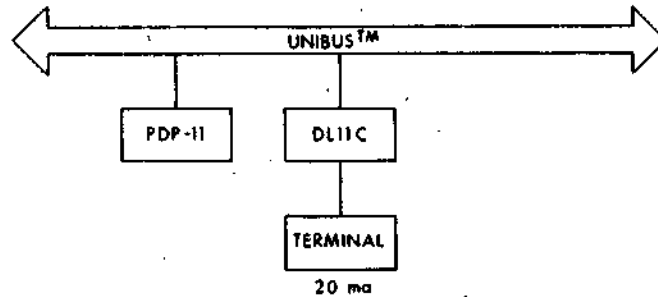


Interfacing a Remote Terminal



Interfacing a Remote PDP-11

DL11



Interfacing a Local Terminal

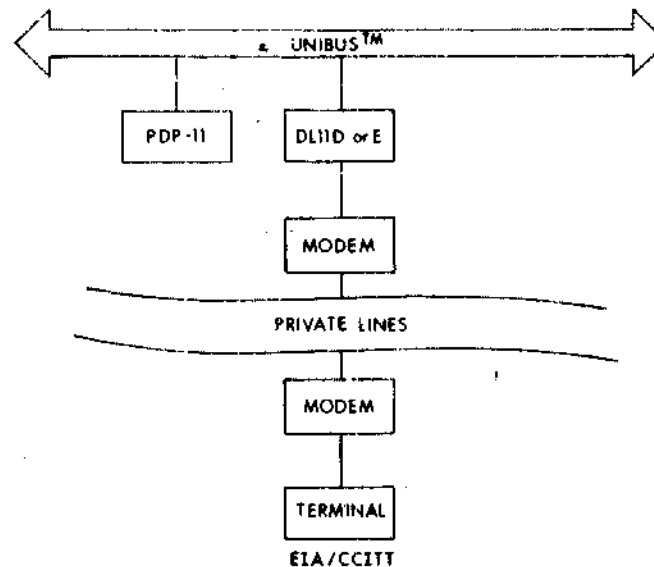
DESCRIPTION

The DL11 series of asynchronous single line interfaces handle full or half duplex communication between a wide variety of serial communication channels and a PDP-11 computer.

With a DL11 interface, a PDP-11 computer can communicate with a local terminal such as a console teleprinter, with a remote terminal via data sets and private line or public switched telephone facilities, or with another local or remote PDP-11 computer.

DL11 systems provide wide flexibility. The user can specify data rate from a selection of 13 standard rates between 40 and 9600 Baud, or he can order a non-standard rate device. With most of the standard rates, the interface can offer split-speed operation for faster, more efficient handling of computer output.

For additional flexibility, character size is strap selectable for 5, 6, 7, or 8-level codes. Also strap selectable are parity checking (even, odd, or none) and stop code length 1, 1.5, or 2 bits).



Remote Communication via Private Lines

There are five DL11 models.

Model DL11-A replaces and is compatible with DIGITAL's KL11 interface, handling 20 mA neutral current loop devices (such as console teleprinters) which use 8-level code and two stop bits.

The DL11-C handles the same current levels but provides the flexibility of a wide choice of speeds and stop bit configurations. This model is recommended for direct interfacing of DIGITAL-supplied teleprinters, the VT05 alphanumeric display, and the LA30-C DECwriter—a DIGITAL-designed electronic keyboard printer.

Model DL11-B meets the interface specifications of Electronic Industries Association Standard RS232C and CCITT Recommendation V.24 and handles either local or remote (data only) communication for 8-level code devices. With local devices, this model requires a null modem; in private line communication, modems are required.

Model DL11-D meets the specifications of and is applied in the same manner as Model DL11-B. However, like the C model, it gives the user a choice of operating speeds and stop bit configurations, so that it is easily adaptable to a wide range of terminals. With a null modem, this model may be used for local interfacing of a terminal or another PDP-11.

Model DL11-E meets the EIA and CCITT interface specifications cited for Models B and D. This interface provides the user with the full range of data rates as well as with complete dataset control for remote communication with either a terminal or another PDP-11 computer.

DL11

Using the PDP-11's versatile UNIBUS as a multiplexer, a PDP-11 can handle multiple DL11 interfaces. Assigned addressing space allows a single system to support up to 16 DL11-A and/or B models and up to 31 DL11-C, D, or E models. Each DL11 module represents one unit load to the UNIBUS and plugs into a standard small peripheral controller slot in a PDP-11 system unit.

With its exceptional versatility, the DL11 is ideally suited for such applications as numerical control and data acquisition and reduction, especially in such fields as biomedicine and physics where input and processing often require multiple asynchronous lines.

OPERATION

General

The DL11 is an interface between a single Asynchronous Serial Communication Channel and the PDP-11. It performs serial-to-parallel and parallel-to-serial conversion of serial start-stop data with a double character buffered MOS/LSI circuit called a UART (for Universal Asynchronous Receiver-Transmitter). This 40-pin dual-in-line package includes all of the circuitry necessary to double buffer characters in and out, serialize-deserialize data, provide selection of character length and stop code configuration, and present status information about the unit and each character.

Receiver

The receiver section performs serial to parallel conversion of 5, 6, 7 or 8-level codes. The character length is selectable by split-lug jumpers on the circuit card, and is specified by the customer at the time of the order. Each character appears right justified in the Receiver Data Buffer Register (RBUF), stripped of start, stop, and parity bits.

The data rate may lie anywhere in the range between 40 baud and 10,000 baud, and in many cases need not necessarily be the same for the receiver as for the transmitter. (See section on DATA RATES). The receiver samples the line at 16 times the data rate.

A complete character is formed in the UART and is transferred to the Receiver Data Buffer Register (RBUF) at the time the center of the first stop bit is sampled. At that time, the Receiver Done Bit (Bit 7) is set in the Receiver Status Register (RCSR). If the Receiver Interrupt Enable Bit (Bit 6) is also set in RCSR, an interrupt request is generated. The BR level is set by jumper plug. BR4 is standard.

The program then reads the RBUF. The character appears right justified in bits 7-0 of RBUF, stripped of start, stop, and parity (if odd or even is selected) bits. Unused high order bits (6 and 7 in the case of a 6-level code) are zero-filled. Bits 8-11 are always zero and bits 12-15 contain status information about the character supplied by the UART*. (See section on PROGRAMMING.)

* All references to the character status and error bits (12-15) apply to the DL11-C, D, and E models only. The DL11-A and B are KL11 compatible, and therefore have no such status bits.

MODEL	ELECTRICAL INTERFACE	LEVEL CODE	STOP BITS	PARITY CHECKING	BAUD RATE GROUPS*	APPLICATIONS
DL11-A	20 ma neutral current	8	2	None	1, 3	Models LT33 & LT35 teletypewriters with or without paper tape.
DL11-B	EIA/CCITT	8	2	None	1, 3	Local (needs null modem) Remote (private wire) via modems.
DL11-C	20 ma neutral current	5, 6, 7, 8	1, 1.5, 2	None, odd, even	All	Used as A, but choice of code etc. VT05, LA30-C, . . .
DL11-D	EIA/CCITT	5, 6, 7, 8	1, 1.5, 2	None, odd, even	All	Used as B, but choice of code etc. Can be used for local interfacing of a PDP-11 with a null modem.
DL11-E	EIA/CCITT	5, 6, 7, 8	1, 1.5, 2	None, odd, even	All	Bell 103, 202, 113 modems

* See data rate table later in this section.

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Note that the program has a full character time to remove the completed character from RBUF before the next character is put there by the UART. Should the program fail to remove a character before the next is available, the old one(s) will be lost, and the Overrun Bit and Error Bit (bits 14 and 15) are set in RBUF.

The customer may specify, at the time of ordering, that the DL11 will check received data characters for even parity (an even number of data bits are ones), odd parity, or no parity check. If even or odd parity is selected, the DL11 will compute the parity of the incoming character and set bits 12 and 15 in RBUF if an error is found. (Bit 15 is the logical OR of bits 12, 13 and 14.) Note that if odd or even parity is selected, the total character length is the sum of the start bit, plus the number of data bits selected, plus the parity bit, plus the number of stop bits selected.

If, at the time the center of the first stop bit should appear on the received data line, the line is found to be in a spacing condition, the Framing Error Bit (Bit 13) and Error Bit (Bit 15) are set in RBUF. Such a condition may occur, for instance, if the data line goes open, or if the terminal to which the DL11 is connected transmits a Break signal. Should this occur, RBUF will contain a character all of whose bits will be zero. Succeeding all-zero or Break characters, however, will not be assembled by the UART and presented to the program. The received data line must return to a marking condition before character assembly will be resumed.

Transmitter

The transmitter section performs parallel to serial conversion of data supplied to it from the UNIBUS. The character length and stop code (number of units of mark at the end of each character) are the same as for the receiver section. The transmitter section is also fully double buffered. Any time the Transmitter Ready Bit (bit 7) is set in the Transmitter Status Register (XCSR), the program may load the low-order eight bits of the Transmitted Data Buffer Register (XBUF) with a right justified data character. The Transmitter Ready Bit will be set any time the XBUF is available, whether or not a character is currently being transmitted. This is a natural result of the double buffering and means that if a character is not currently being transmitted and XBUF is empty, the program may provide two characters in succession (within less than one character time) to the transmitter.

As the first character is loaded, it is immediately transferred to the serializer register internal to the UART, and the Transmitter Ready Bit (bit 7) in XCSR is set again. If the Transmitter Interrupt Enable Bit (bit 6) is set in XCSR, an interrupt request will be generated any time the Transmitter Ready Bit (bit 7) is set. The BR level for the transmitter is the same as for the receiver.

The transmitter supplies the start bit, odd, even, or no parity bit, and the proper number of stop bits as specified by the customer at the time of order.** The code configuration (number of data bits, odd, even, or

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no parity, and number of stop bits) is the same for the transmitter as for the receiver section.

The normal rest condition of the transmitted data lead is marking. A continuous spacing signal may be applied to this lead by setting bit 0 or XCSR (the "BREAK" bit) to a one.** The Transmitted Data lead will remain in a spacing condition as long as this bit is asserted. If characters are supplied to the transmitter, it will, however, continue to appear to the program as if they were being sent normally. This provides the facility for sending precisely timed spacing signals, by asserting the "BREAK" bit and using the transmitter interrupts as a timer.

** Note that references to parity generation and "BREAK" bits are not applicable to the DL11-A and B, since these two are functionally and program compatible with the KL11.

Paper Tape Reader Control

The DL11-A and DL11-C have a 20 mA current loop electrical interface and are equipped to control the paper tape Reader Run Relay with which some DIGITAL-supplied teleprinters are equipped. If bit 0 of RCSR is set to a one, the lead controlling the Reader Run Relay is asserted, and a character will be read from paper tape. This bit is reset upon detection of a valid start bit by the UART receiver. The DL11-A is supplied with a 2¼ ft. cable (DIGITAL part #7008360) terminated in a female MATE-N-LOC connector which connects to the teleprinter supplied with a PDP-11, or to the cable supplied with the DIGITAL VT05 terminal, or DIGITAL LA30-C DECwriter.

Dataset Interface

The DL11-B and DL11-D are supplied with an electrical interface and connector whose signal levels and connector pinning conform to Electronic Industries Association Specification RS232C, and to CCITT Recommendation V.24. Their cables are terminated in a Cinch DB25P plug with protective hood. The DL11-B and DL11-D connect to the Protective Ground (EIA circuit AA, connector pin 1), Signal Ground (Circuit AB, pin 7), Transmitted Data (Circuit BA, pin 2), Received Data (Circuit BB, pin 3), Request to Send (Circuit CA, pin 4), and Data Terminal Ready (Circuit CD, pin 20) leads. The Data Terminal Ready lead (Circuit CD, pin 20) and Request to Send lead (Circuit CA, pin 4) are held asserted (ON, logical 1). It is therefore possible to connect the DL11-B and DL11-D to datasets such as the Bell 103A2, which will automatically answer incoming calls. It is not possible, however, to terminate the call, determine the presence of Data Carrier (Circuit CF), detect a Ring signal (Circuit CE), or operate the Secondary Transmitted and Received Data leads (Circuit SBA and SBB) with the DL11-B and DL11-D, under program control. These functions are provided by the DL11-E.

Dataset Control

The DL11-E is supplied with an electrical and physical interface as described above for the DL11-B and D, except as noted. However, the DL11-E is equipped for full dataset control, and supports the following dataset leads:

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Signal Name	EIA Circuit Designation	Connector Pin No.
Protective Ground	AA	1
Transmitted Data	BA	2
Received Data	BB	3
Request to Send	CA	4
Clear to Send	CB	5
Signal Ground	AB	7
Received Line Signal Detector (Carrier)	CF	8
*Secondary Transmitted Data	SBA	11
*Secondary Received Data	SBB	12
Data Terminal Ready	CD	20
Ring Indicator	CE	22

* The pinning convention for Secondary Transmitted and Secondary Received Data leads does NOT conform to the cited EIA and CCITT specifications, but rather to the Bell 202C, D Dataset Interface pinning. In order to make the connector pinning conform to the EIA/CCITT specifications for these two leads, it is necessary to move the wire connected to pin 11 in the Cinch DB25P connector to pin 14, and the wire connected to pin 12 to pin 16.

These leads are sensed (for signals from the dataset) and set/reset (for signals to the dataset) by the program via bits in RCSR. The operation and meaning of these bits is explained in the section on "Programming."

Note that it is not possible to convert one DL11 model to another in the field.

Data Rates

The DL11 is available with a wide range of standard data rates. The customer must specify on his order one of four groups of data rates for both the transmitter and receiver, in bits per second. The following table lists the standard rates available, and whether or not it is possible to operate the transmitter at a different speed from the receiver (split speed).

Speed Group	Speeds (Bits Per Sec)		Split Speed	Applicable Terminals
	Transmit	Receive		
1	110	110	No	Teletype Models 33, 35
2*	134.5	134.5	No	IBM 2740, 2741, Datel, etc.
3	50	50	Yes	DIGITAL LA30, VT05, M37 TTY Most CRT Terminals
	75	75		
	150	150		
	300	300		
	600	600		
	1200	1200		
	1800	1800		
2400	2400			

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4*	200	200	Yes	DIGITAL LA30-C,
	300	300		VT05,
	600	600		GE Terminet 300,
	1200	1200		Most CRT Terminals
	2400	2400		
	4800	4800		
	7200	7200		
	9600	9600		

* Not available on DL11-A and DL11-B.

It is possible to field change speeds within groups 3 and 4 to other speeds within the same group, but it is not possible to field change from one group to another group. Where the data rate specified by the customer may be either group 3 or 4 (e.g. 300 baud), the unit will be supplied with group 3 speeds.

PROGRAMMING

General

The interface between a program running in the PDP-11 processor and the DL11 is via four device registers. They are the 1) Receiver Status Register (RCSR); 2) Receiver Data Buffer Register (RBUF); 3) Transmitter Status Register (XCSR); and 4) Transmitter Data Buffer Register (XBUF). The functions of the bits provided in each register are described below. Each register is assigned an 18-bit memory address, and may be read from or written into using any processor instruction which references these addresses, with the exceptions noted.

Interrupts

The DL11 has two channels of interrupts: one for the receiver section (vector = XX0) and one for the transmitter section (vector = XX4). These two circuits operate independently, except that receiver takes priority on simultaneous interrupt requests (is closer to the processor on the bus).

However, it is very important to note that in the DL11-E (dataset operation), the receiver section handles a multiple source interrupt: RCVR DONE and DSET INT. Furthermore, DSET INT is set by several conditions (RING, CARRIER, etc.). If while servicing an interrupt for one condition, a second interrupt condition occurs, a unique second interrupt (and all subsequent ones as well) may not occur. To prevent this: 1) all possible interrupt conditions should be checked after servicing one particular condition, or 2) both interrupt enables (bits 5 and 6) should be cleared upon entry to the service routine for vector XX0, and set again at the end of service.

Address and Vector Assignments

The DL11-A and DL11-B follow the same address and vector assignments as the KL11:

DL11

	Address	Vector	Priority
Console	777 560 777 562 777 564 777 566	60/64	BR4
Additional Units	776 XX0 776 XX2 776 XX4 776 XX6	Floating	BR4

Since each DL11 unit has four registers, each requires four addresses. Address space assignment for the DL11-A and B is the same as that for the KL11; that is, unit 0 occupies addresses 777 560-777 566, and units 1-15 occupy from 776 500 through 776 676. For the DL11-C, D, and E, unit 0 will have address 775 610, unit 1, 775 620, etc., up to unit 30 at 776 170.

The four registers and their addresses are listed for DL11 unit 0, where XXX is 756 for DL11-A and B, and 561 for DL11-C, D, and E.

1. Receiver Status Register (RCSR) 77XXX0
2. Receiver Data Buffer Register (RBUF) 77XXX2
3. Transmitter Status Register (XCSR) 77XXX4
4. Transmitter Data Buffer Register (XBUF) 77XXX6

The interrupt vector addresses for the DL11-A and DL11-B follow the same scheme as for the KL11. That is, if one is used for the console teletype, it gets vector address 60 and 64. The next units occupy addresses beginning after all DC11's (if any) on the system are assigned, beginning at address 300. Any DP11, DM11, DN11, DM11-BB, DR11-A, DR11-C, and DT11's are then assigned. After all of the preceding are assigned, the DL11-C's, DL11-D's and DL11-E's are then assigned.

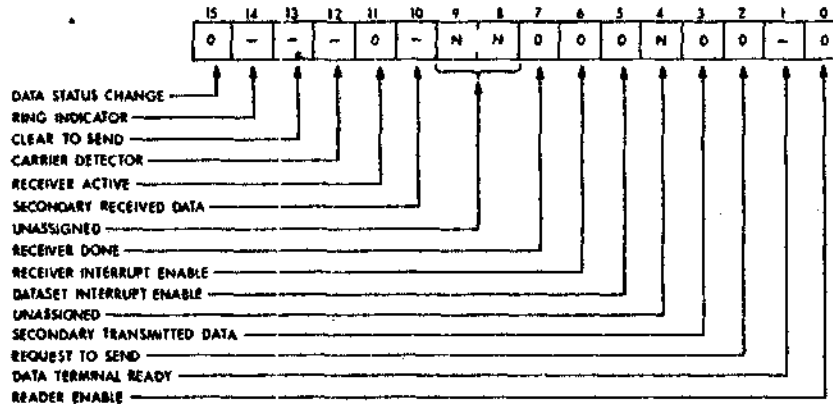
Register Definition

The following chart presents the bit assignments within each register. Bits marked "Unused" and "Write Only" are always read as zero. Attempting to write into "Unused" or "Read Only" bits has no effect on those bits. "INIT" refers to the initialize signal generated by the processor (e.g. upon execution of a RESET instruction.) "Transmit" and "Receive" are with respect to the DL11. All bits in the accompanying diagrams are shown in the state they assume on POWER CLEAR or INIT. A "dash" indicates that the bit is set by the terminal or dataset or the hardware and is not cleared by INIT.

BIT DESCRIPTION AND OPERATION

- 15* Dataset Status Change. Read only. This bit is set (1) by any change in the state of bits 10 (Secondary Receive Data), 12 (Carrier Det.), and 13 (Clear to Send) in RCSR, and by an off to on (0 to 1) change in the state of bit 14 (Ring Ind.) in RCSR. It is cleared (0) by INIT

Receiver Status Register (RCSR) 77XXX0



and by reading from RCSR. If bit 5 (Dataset Int. Enable) is set, the setting of bit 15 will cause an interrupt request to be generated.

- 14* Ring Indicator. Read only. The state of this bit follows the state of the Ring Indicator lead (Circuit CE, pin 22) from the dataset. It is set when the signal on Circuit CE is high, and cleared when that signal is low. A transition of this bit from 0 to 1 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.
- 13* Clear to Send. Read only. The state of this bit follows the state of the Clear to Send lead (Circuit CB, pin 5) from the dataset. It is set when the signal on Circuit CB is high, and cleared when that signal is low. Any transition of bit 13 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.
- 12* Carrier Detector. Read only. The state of this bit follows the state of the Received Line Signal Detector (Carrier) lead (Circuit CF, pin 8) from the dataset. It is set when the signal on Circuit CF is high, and cleared when that signal is low. Any transition of bit 12 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.
- 11 Receiver Active. Read only. This bit is set when the receiver section of the UART detects a valid start bit on the Received Data lead. In the case of the DL11B, D, and E, this lead will be Circuit BB, pin 3 from the dataset. It is cleared when bit 7 in RCSR (Receiver Done) is set, and by INIT.

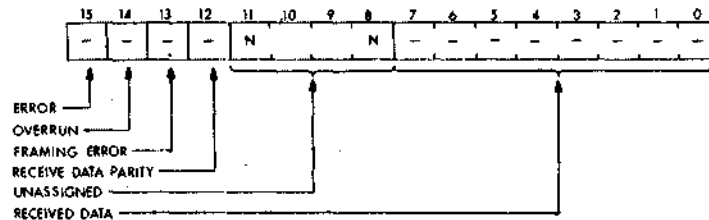
* Note that bits 15-12 in RBUF are not enabled in the DL11-A and DL11-B, and will appear as zero in these models when read by the program. This is to provide program compatibility with the DIGITAL KL11.

Note that all signals from the dataset will appear negated (low) to the program if the dataset is disconnected or loses power. This affects bits 14, 13, 12, and 10, all of which will appear as cleared under such conditions.

DL11

- 10 Secondary Received Data. Read only. The state of this bit follows the state of the Secondary Receive Data lead (Circuit SBB, pin 12) from a Bell 202 dataset. It is set when the signal on circuit SBB is high (spacing) and cleared when that signal is low (marking). Any transition of bit 10 will cause bit 15 in RCSR to be set, and if bit 5 in RCSR is set, will cause an interrupt request to be generated.
- 7 Receiver Done. Read only. This bit is set when the receiver section of the UART has transferred an incoming character to the Receiver Data Buffer Register (RBUF). It is cleared by setting bit 0 (Reader Enable) in RCSR, by addressing (read or write) RBUF, or by INIT. If bit 6 in RCSR is set, the setting of bit 7 will cause an interrupt request to be generated.
- 6 Receiver Interrupt Enable. Read/Write. This bit, when set, causes an interrupt request to be generated each time bit 7 in RCSR is set. It is cleared by INIT, or by the program.
- 5 Dataset Interrupt Enable. Read/Write. This bit, when set, causes an interrupt request to be generated each time bit 15 in RCSR is set. It is cleared by INIT, or by the program.
- 4 Unassigned
- 3 Secondary Transmitted Data. Read/Write. This bit, when set, causes the signal on Circuit SBA, pin 11, to the dataset to go high (spacing), and when cleared, causes that signal to go low (marking). It is cleared by INIT, or by the program.
- 2 Request to Send. Read/Write. This bit, when set, causes the signal on Circuit CA, pin 4, to the dataset to go high, and when cleared causes that signal to go low. There is a Jumper on the DL11-E Card such that this bit may be made to control the Forced Busy lead (pin 25) to the dataset instead of Circuit CA. It is cleared by INIT, or by the program.
- 1 Data Terminal Ready. Read/Write. This bit, when set, causes the signal on Circuit CD, pin 20 to the dataset to be asserted (high), and when cleared causes that signal to be negated (low). This bit is not cleared by INIT, and may be set/reset only by the program. It must be set or cleared as appropriate by the program after power is applied to the machine, since its state at that time is undefined.
- 0 Reader Enable. Write only. This bit, when set, causes the Reader Run Relay on certain DIGITAL-supplied teleprinters to advance the paper tape reader. It also clears Receiver Done (bit 7) in RCSR. It is cleared by INIT, or when bit 11 in RCSR is set. Operation of bit 0 is possible in all DL11's, but its associated 20 mA output circuit is used only on DL11-A and C.

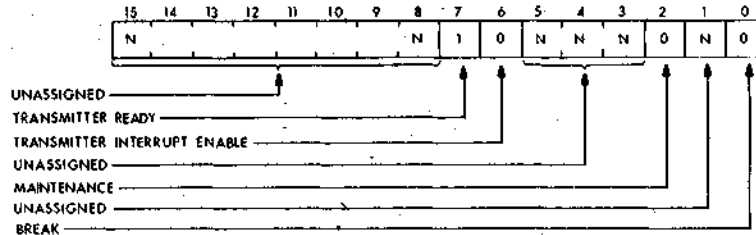
Receiver Data Buffer Register (RBUF) 77XXX2



BIT	DESCRIPTION AND OPERATION
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- 15* Error. Read only. This bit is set if bit 14, 13, or 12 (or any combination of these bits) in RBUF is set (logical OR of bits 14, 13, 12). It is cleared only if none of the above bits are set.
- 14* Overrun. Read only. This bit is set if bit 7 in RCSR (Receiver Done) is not cleared before the UART attempts to present a new character to RBUF, i.e., if the UART attempts to set bit 7 in RCSR, and it is already set. The previous character in RBUF is lost, and the new character replaces it.
- 13* Framing Error. Read only. This bit is set if the UART, at the time it samples the received data line in the center of the first stop bit, finds the line in a spacing (0) condition. This may indicate an open input line, "BREAK" signal, or excessive distortion of the received character.
- 12* Receive Data Parity Error. Read only. This bit is set by the UART if the parity of the received data character does not agree with the parity specified to the UART (odd or even). This bit is always zero if the "no parity check" option is specified. Bits 14, 13, and 12 are updated each time a character is received.
- 7-0 Received Data. Read only. These bits contains the last complete character assembled by the UART. If the character length specified to the UART is less than 8 bits, the character will appear right justified (low order bit in bit 0). The unused high order bits will contain 0.

* NOTE The state of bits 14, 13, and 12 applies to the character currently in RBUF, bits 7-0. It is not necessary to clear them in order to receive the next character. Also, these bits are not enabled in the DL11-A and DL11-B, and will appear as zero in these models when read by the program. This is to provide program compatibility with the DIGITAL KL11.

Transmitter Status Register (XCSR) 77XXX4**BIT DESCRIPTION AND OPERATION**

- 7** Transmitter Ready. Read only. This bit is cleared when a data character is loaded into XBUF. It is set when XBUF can accept another data character, and by INIT. If bit 6 in XCSR is set, this bit, when set, will cause an interrupt request to be generated. Note that this bit is set, not cleared, by INIT.
- 6** Transmitter Interrupt Enable. Read/Write. This bit, when set, will cause an interrupt request to be generated whenever bit 7 in XCSR is set. This bit is cleared by INIT and by the program.
- 5-3** Unassigned.
- 2** Maintenance. Read/Write. This bit, when set, causes data emitted at the serial output of the UART transmitter section to appear at the serial input of the receiver section. In addition, it forces the receiver to run at the same data rate as the transmitter, and disconnects the external serial line input to the receiver. It is cleared by INIT, and by the program.
- 1** Unassigned.
- 0**** BREAK. Read/Write. This bit, when set, clamps the serial data output of the UART transmitter to a spacing (logical 0) condition. The transmitter will appear to the program to function normally if characters are presented to XBUF, but a continuous spacing signal will appear on the Transmitted Data lead (Circuit BA). This bit is cleared by INIT, and by the program.

** Not available on DL11-A and DL11-B.

Transmitted Data Buffer Register (XBUF) 77XXX6**BIT DESCRIPTION AND OPERATION**

- 7-0** Transmitted Data. Write only. These bits contain the data character to be transmitted by the UART. If the data character contains fewer than 8 data bits, the character must be right justified when loaded into XBUF. The bits of the character are presented to the serial line low-order bit (bit 0) first. A bit set to one in XBUF will cause a marking condition to appear on the transmitted data lead for one bit time. Cleared by INIT.

DL11

SPECIFICATIONS

- Function:** Provides an interface between the PDP-11 UNIBUS and a single asynchronous bit serial communications channel.
- Mechanical:** The DL11 consists of one quad module and a connecting cable terminated in a plug appropriate to the data communications equipment to be connected.
- Operating Mode:** Full or half duplex under program control.
- Data Format:** Asynchronous, serial by bit. One start and one, one and one-half (5-level codes only), or two stop bits, supplied by the hardware. The DL11-A and B are supplied with 8 level, no parity, 2 stop bit code configuration. The DL11-C, D, and E will accommodate characters of 5, 6, 7, or 8 bits, with or without even or odd parity. The data format must be the same for transmitted and received data. The data format must be specified at the time of order.
- A one (1) presented by the program to any bit in the Transmitted Data Register will cause a Marking (logical 1) condition to appear on the Transmitted Data lead during the corresponding bit interval. A zero (0) presented by the program will cause a Spacing (logical 0) condition to appear. A Marking condition on the Received Data lead during any data bit sampling interval will be presented to the program as a one (1) in the Received Data Register, and a Spacing condition will be presented as a zero (0).
- Order of Bit Transmission:** Low order bit first.
- Distortion:** The DL11 receiver will operate properly in the presence of 40% space-to-mark or mark-to-space distortion between any two received data bits, and up to $\pm 4.5\%$, long-term speed distortion, provided the data format contains at least one and one-half stop units. If the data format contains only one stop unit, the speed tolerance is $\pm 4\%$. The DL11 transmitter operates with less than 3% bit-to-bit or long-term distortion.
- Bus Loading:** One DL11 presents one unit load to the PDP-11 UNIBUS.
- Electrical Interface:** DL11-A and DL11-C provide a 20 mA active current loop for both send and receive leads for connection to local teleprinters such as the DIGITAL LA30-C and Teletype Models 33 and 35, and displays such as DIGITAL VT05 Terminal.

DL11

The DL11-A and DL11-C are supplied with a 2 $\frac{1}{4}$ ft., 6-conductor cable terminated with a female MATE-N-LOC connector.

The DL11-B and DL11-D provide a voltage level interface and connector whose signal levels and connector pinning conform to Electronic Industries Association Standard RS232C and CCITT Recommendation V.24. The leads supported by the DL11-B and D are:

Protective Ground, Circuit AA, pin 1.

Transmitted Data, Circuit BA, pin 2.

Received Data, Circuit BB, pin 3.

Signal Ground, Circuit AB, pin 7.

Data Terminal Ready, Circuit CD, pin 20*.

Request to Send, Circuit CA, pin 4*.

* These leads are held ON (logical 1) by the hardware.

The DL11-B and D are supplied with a 25-ft., 25-conductor cable terminated in a Cinch DB25P plug with a protective hood.

The DL11-E provides a voltage level interface as described above for the DL11-B, but in addition supports the following leads, giving full dataset control capability to the computer program:

Data Terminal Ready, Circuit CD, pin 20.

Clear to Send, Circuit CB, pin 5.

Request to Send, Circuit CA, pin 4.

Received Line Signal Detector (Carrier), Circuit CF, pin 8.

Ring Indicator, Circuit CE, pin 22.

Secondary Transmitted Data, Circuit SBA, pin 11*.

Secondary Received Data, Circuit SBB, pin 12*.

* Note that the pin assignment of these two leads conforms to that of the Bell 202 Dataset, rather than to the cited EIA/CCITT* standard.

The DL11-E is supplied with a 25 ft., 25-conductor cable terminated in a Cinch DB25P plug with protective hood.

Power
Requirements:

The DL11 requires 1.8 amps of + 5v., .05 amps of + 15v., and .15 amps of - 15v.

DL11

- Data Rate:** The DL11 is supplied to customer order with 13 standard data rates in four groups.
- Group 1. 110 baud receive and transmit.
- Group 2.** 134.5 baud receive and transmit.
- Group 3. Following 8 speeds, which may be different for receive and transmit: 50, 75, 150, 300, 600, 1200, 1800, 2400 baud.
- Group 4.** Following 8 speeds, which may be different for receive and transmit: 200, 300, 600, 1200, 2400, 4800, 7200, 9600 baud.

** Not available on DL11-A and DL11-B.

Models

- DL11-A:** Single Asynchronous Serial Line Interface Unit. Full duplex operation, 20 milliampere neutral current loop electrical interface. Replaces and is program compatible with the DIGITAL KL11 for control of PDP-11 console teleprinters. Furnished with 2 $\frac{1}{4}$ -ft. cable terminated in female Mate-n-Loc connector, suitable for connection to DIGITAL terminals. Supplied only with code configuration of 8 data bits, 2 stop bits, no parity generation or checking. Customer must specify speed groups 1 (110 baud) or 3 (50, 75, 150, 300, 600, 1200, 1800, 2400 baud) only. If not specified, unit will be supplied at 110 baud.
- DL11-B:** As DL11-A above, except electrical interface conforms to EIA RS232C. Supports Transmitted and Received data leads. Request to Send and Data Terminal Ready leads are clamped always ON. Supplied with 25-foot cable terminated by Cinch DB25P plug for connection to modem (BC05C-25 cable).
- DL11-C:** Single Asynchronous Serial Line Interface Unit. Full duplex operation, 20 mA neutral current loop electrical interface. Code configuration (5, 6, 7, 8 data bits; 1, 1.5, 2 stop bits; odd, even, or no parity) and speed (Groups 1, 2, 3, or 4) customer specified. Furnished with 2 $\frac{1}{4}$ ft. cable terminated in female Mate-n-Loc connector, suitable for connection to DIGITAL LA30-C DECwriter, DIGITAL VT05 Display Terminal, or DIGITAL-supplied Teletype. If speed and code configuration are not specified, unit will be supplied as 8 data bits, no parity, 2 stop bits, 110 baud.
- DL11-D:** As DL11-C above, except EIA RS232C electrical interface. Supports Transmitted and Received Data leads, and clamps ON Request to Send and Data Terminal Ready leads. Furnished with 25 ft. cable terminated in Cinch DB25P plug, for connection to modem (BC05C-25 cable).
- DL11-E:** As DL11-D above, except supports full dataset control interface, including Data Terminal Ready, Clear to Send, Request to Send, Carrier, Ring, Secondary Received and Secondary Transmitted leads.

DL11-W

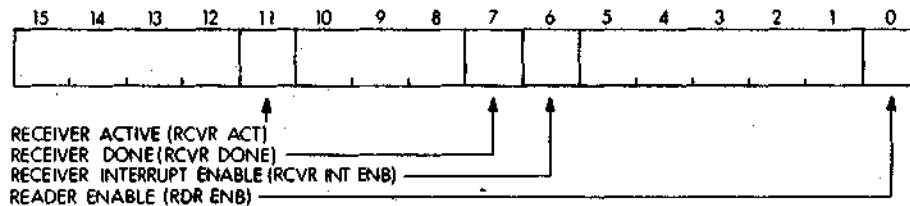
SERIAL LINE INTERFACE, DL11-W

The DL11-W is a serial-line interface and a real time clock. It translates parallel information to serial information (required by a communication device) and translates serial information to parallel information (required by the processor).

In the following description, "transmitter" refers to the registers and bits associated with accepting a parallel character from the Unibus for transmission to a communication device via the DL11-W, "Receiver" refers to the registers and bits associated with accepting serial information which is converted to a parallel character and sent to the Unibus.

REGISTERS

Receiver Status Register (RCSR)

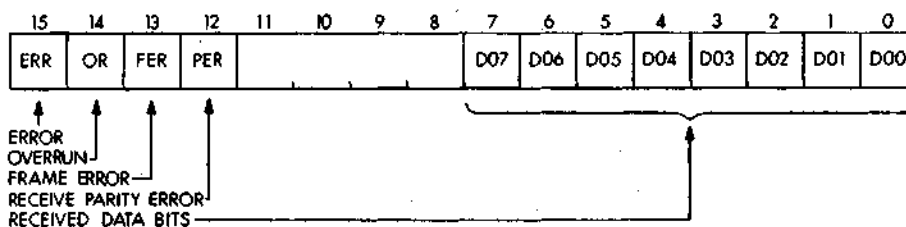


BIT

MEANING AND OPERATION

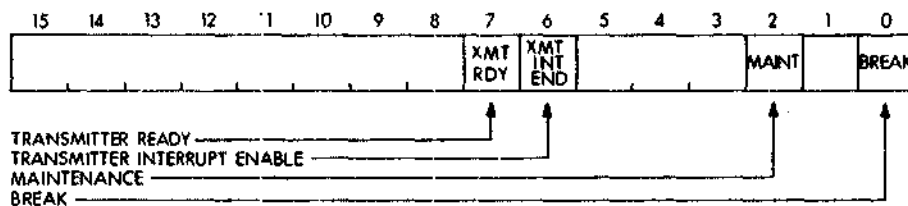
- 15-12 Unused.
- 7 RCVR DONE—Read Only. Set when an entire character has been received and is ready for transfer to the UNIBUS. Cleared by setting RDR ENB, addressing (READ or WRITE) RBUF or INIT. Starts an interrupt sequence when RECEIVER INTERRUPT ENABLE (bit 6) is also set.
- 6 RECEIVER INTERRUPT ENABLE—Read/Write. Cleared by INIT. Starts an interrupt sequence when Receiver DONE is set.
- 5-1 Unused.
- 0 READER ENABLE—Write Only. Cleared by INIT or at middle of a START bit. Advances paper tape reader of ASR teletypes. Clears RCVR DONE. 20 mA current loop circuit output associated with this bit.

Receiver Data Buffer (RBUF)



BIT	MEANING AND OPERATION
15	ERROR—Read Only. Logical "OR" of OR, FER, and PER. Cleared by removing the error conditions. ERROR is not tied to the interrupt logic, but RCVR DONE is.
14	OVERRUN—Read Only. Set if previously received character is not read (RCVR DONE not reset) before the present character is read.
13	FRAMING ERROR—Read Only. Set if the character read has no valid stop bit. Also used to detect break.
12	RECEIVE PARITY ERROR—Read Only. Set if received parity does not agree with the expected parity. Always 0 if no parity is selected.
<p>NOTE: Error conditions remain present until the next character is received, at which time, the error bits are updated. INIT does not necessarily clear the error bits. Error bits may be disabled via a switch.</p>	
11, 10, 9, 8	Unused.
7-0	RECEIVED DATA BITS—Read Only. These bits contain the character just read. If less than 8 bits are selected, the buffer will be right justified into the least significant bits with the higher unused bit or bits, reading as 0's. Not cleared by INIT.

Transmitter Status Register (XCSR)

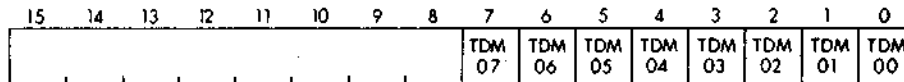


BIT	MEANING AND OPERATION
15-8	Unused.
7	TRANSMITTER READY—Read Only. Set by INIT. Cleared when XBUF is loaded; set when XBUF can accept another character. When set it will start an interrupt sequence if XMIT INT ENB is also set.
6	TRANSMITTER INTERRUPT ENABLE—Read/Write. Cleared by INIT. When set it will start an interrupt sequence if XMIT READY is also set.

DL11-W

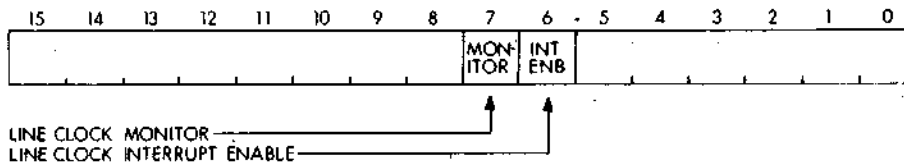
BIT	MEANING AND OPERATION
5, 4, 3	Unused.
2	MAINTENANCE —Read/Write. Cleared by INIT. When set it disables the serial line input to the RECEIVER and sends the serial output of the TRANSMITTER into the serial input of the RECEIVER. Forces receiver to run at transmitter speed.
1	Unused.
0	BREAK —Read/Write. Cleared by INIT. When set, it transmits a continuous space. May be disabled via a switch.

Transmitter Data Buffer (XBUF)



BIT	MEANING AND OPERATION
15-8	Unused.
	TRANSMITTED DATA BUFFER —Write Only. If less than 8 bits are selected then the character must be right justified into the least significant bits.

Clock Status Register (LKS)



BIT	MEANING AND OPERATION
15-8	Unused.
7	LINE CLOCK MONITOR —Read/Clear. Set only by the line frequency clock signal and cleared only by the program. Set by INIT.
6	LINE CLOCK INTERRUPT ENABLE —Read/Write. Cleared by INIT. When set, Starts an interrupt sequence if Line Clock monitor is also set.
5-0	Unused.

DL11-W

BIT

MEANING AND OPERATION

NOTE: Line Clock circuit must be disabled via a switch when serial line portion is used as other than console interface (Address 77756X).

Priorities are hardwired and are not selectable.

Floating vectors for serial line interface portion are switch selectable.

INTERRUPTS

The DL11-W has three channels of interrupts: one for the receiver section (vector = XX0), one for the transmitter section (vector = XX4) and one for the clock section (vector = 100). These circuits operate independently.

ADDRESS AND VECTOR ASSIGNMENTS

The DL11-W follows the same address and vector assignments as the KL11, DL11-A, B, C, D which are:

	ADDRESS	VECTOR	PRIORITY
LINE CLOCK	777546 777560	100	BR6
CONSOLE	777662 777564 777566 776XX0	60/64	BR4
ADDITIONAL UNITS	776XX2 776XX4 776XX6	Floating	BR4

Where XX = 50 to 67

77XXX0 77XXX2 77XXX4 77XXX6	Floating	BR4
--------------------------------------	----------	-----

Where XXX = 561 to 617.

TIMING CONSIDERATIONS

Receiver

The RCVR DONE flag sets when the UART has assembled a full character, which occurs at the middle of the first stop bit.

NOTE

The UART (Universal Asynchronous Receiver/Transmitter) is an asynchronous subsystem. The transmitter accepts parallel characters and converts them to a serial asynchronous output. The receiver accepts asynchronous serial characters and converts them to a parallel output.

Since the UART is double buffered, data remains valid until the next character is received and assembled. This allows one full character time for servicing the RCVR DONE flag.

Transmitter

The UART's transmitter section is also double buffered. After initialization, the XMIT RDY flag is set. When the buffer is loaded with the first character, the flag clears but sets again within a fraction of a bit time. A second character can then be loaded, clearing the flag again. The flag then remains clear for nearly a full character time.

Break Generation

Setting the break bit causes the transmission of a continuous space. Since the XMIT RDY flag continues to function as normal, the duration of break can be timed by the "pseudo-transmission" a number of characters. However, since the transmitter is double buffered, a null character (all zeros) should precede transmission of break to insure the previous character clears the line. Likewise, the last "pseudo-transmitted" character under break should be null.

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HIGHLIGHTS

- Local or remote interconnection of computers over a serial synchronous link.
- DDCMP communications protocol implemented by hardware for reliable data transmission, high throughput, low processor overhead and ease of programming.
- Pipelined operation for high throughput by overlapping data transmissions, program operation and propagation delays.
- Local operation at 1,000,000 bits per second (full or half duplex) over coaxial cable up to 6,000-feet long.
- Local operation at 56,000 bits per second (full or half duplex) over coaxial cable up to 18,000-feet long.
- Remote operation over synchronous modems at speeds up to 19,200 bits per second (full or half duplex) using EIA RS232C interface.
- Half-duplex local operation using a single coaxial cable.
- Private wire or switched network remote operation.
- Communication between DMC11s or between a DMC11 and other synchronous interfaces than can support the DDCMP protocol.
- Down-line loading of satellite computer systems.
- Ability to initialize an incorrectly functioning satellite computer system by command over the link (Remote Load Detect).
- Same PDP-11 software supporting local or remote, full- or half-duplex configurations.
- Recovery from power failures at either or both ends of a link without loss of data.
- 16-bit NPR (DMA) transfers for minimum interference with processor operation.

GENERAL DESCRIPTION

The DMC11 Network Link is designed for high-performance interconnection of PDP-11 computers in network applications. Where the computers are located in the same facility, DMC11s can be configured for high-speed operation (56,000 or 1,000,000 bits per second) over inexpensive coaxial cable. The necessary modems are built-in. Where the computers are located remotely and connected via common carrier facilities, DMC11s can be configured to interface to synchronous modems such as the Bell Models 208 and 209, or other synchronous modems conforming to the RS232C standard.

Two PDP-11 computers can be connected by a pair of DMC11s. For remote operation, a DMC11 can communicate with a different type of synchronous interface or even a different type of computer, provided that the remote system has implemented the DDCMP (Digital Data Communications Message Protocol) protocol.

The DMC11 ensures reliable data transmission by implementing the DDCMP protocol in hardware using a high-speed microprocessor. The

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DDCMP protocol detects errors on the channel interconnecting the systems by using a 16-bit Cyclic Redundancy Check (CRC-16). Errors are corrected, when necessary, by automatic retransmissions. Sequence numbers in message headers ensure that messages are delivered in proper order with no omissions or duplications.

Errors are commonplace on cables or other communications channels more than a few feet in length. Reliable data transmission requires a protocol. The DMC11 takes care of the details of protocol operation including character and message synchronization, header and message formatting, error checking and retransmission control. The PDP-11 program need not worry about these details.

The DMC11 offers a number of advantages over conventional interfaces which require a combination of hardware and software to implement a protocol. Programming is greatly simplified. Programming the DMC11 does not require extensive communications expertise. PDP-11 memory and processor time are not wasted with instructions implementing the protocol. Throughput is enhanced because the DMC11 microprocessor operates at high speed and is not delayed when the processor has to perform high-priority tasks.

FULL-DUPLEX OPERATION

The DMC11 supports full- or half-duplex operation. Full-duplex operation offers the highest throughput and is used when the communications facilities permit two-way simultaneous operation. Data and/or control messages can be exchanged between the two computer systems simultaneously in both directions. The DDCMP protocol permits continuous simultaneous transmission of data messages in both directions when buffers are available and there are no errors on the channels.

In order to take advantage of this pipeline capability, the DMC11 permits the PDP-11 program to queue as many as seven buffers containing messages for transmission and as many as seven empty buffers for reception. By queuing up multiple buffers, the programs can effectively overlap PDP-11 processing with data transmission.

Transmissions do not have to stop while the program responds to an end-of-message interrupt. The DMC11 will interrupt the PDP-11 when a message has been successfully transmitted or received. All this time the program can supply a new buffer to keep the pipeline filled.

HALF-DUPLEX OPERATION

Half-duplex operation is used where throughput requirements do not justify the added cost of cables or communications lines capable of simultaneous operation in both directions. Local operation requires two coaxial cables for full-duplex operation but only one coaxial cable for half-duplex operation. Remote operation requires a four-wire channel for full-duplex operation but only a two-wire channel for half-duplex operation. This is particularly important for dial-up operation when two calls would need to be placed for full-duplex operation.

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The PDP-11 program does not have to worry about the details of half-duplex operation. All it needs to do is specify half-duplex operation at device initialization. The DMC11 takes care of ensuring that both ends of the link are coordinated: one listening while the other is transmitting. The program queues transmit and receive buffers exactly as for full-duplex operation. The same program can be used for local and remote operations, private wire and dial backup operation because of this feature.

DOWN-LINE LOADING AND REMOTE LOAD DETECT

The DMC11 supports down-line loading of computer system software. Down-line loading is used when software is centrally stored (in a host system) and distributed over the network links to other systems (the satellite systems). These satellite systems are often small systems with no peripherals available for program loading. Sometimes the satellite systems have disks, but down-line loading is desired to maintain central control over software.

The DMC11 can send and receive down-line loading messages in the DDCMP Maintenance format. DMC11s can be used for down-line loading at the host, satellite, or both ends of a link. A special ROM (read-only memory) bootstrap is not needed for down-line loading when a DMC11 is used at the satellite end of a link.

Unattended operation of satellite systems in a network requires the host systems to be able to initialize an incorrectly-functioning satellite system and force it to execute a new program loaded down the communications link. A special DDCMP maintenance message is used for this purpose. A DMC11 at the satellite end of a link can recognize this message and initialize the associated computer system.

PHYSICAL DESCRIPTION

A DMC11 consists of two modules, a microprocessor module and a line unit module. The two modules are interconnected by a one-foot cable. The microprocessor and line unit modules are ordered separately. One version of the microprocessor module is available. Three versions of the line unit module are available: local operation at 1,000,000 bps (bits per second), local operation at 56,000 bps, and remote operation with RS232C-compatible synchronous modems (up to 19,200 bps).

The DMC11-AD microprocessor module is a hex-sized single PC board that fits into a hex small peripheral controller (SPC) slot. It includes a 300 ns bipolar microprocessor, a Read-Only Memory (ROM) implementing the DDCMP protocol, local scratch pad memory (RAM), and a UNIBUS interface.

The DMC11-MA, DMC11-MD and DMC11-DA line unit modules are hex-sized PC boards for use in SPC slots. They have a cut-out to fit over a UNIBUS connector so they can also be located in the end slots of a DD11 system unit, if an 8½-in-high UNIBUS terminator or cable connector isn't used. Each includes a one-foot cable for connection to the microprocessor module.

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The DMC11-MA line unit module includes serial-to-parallel conversion and a built-in modem for local operation at 1,000,000 bps over coaxial cable up to 6,000-feet in length. Coaxial cables are not included.

The DMC11-MD line unit module includes serial-to-parallel conversion and a built-in modem for local operation at 56,000 bps over coaxial cable up to 18,000-feet in length. Coaxial cables are not included.

The DMC11-DA line unit module includes serial-to-parallel conversion and an EIA RS232-C interface for use with Bell 208 or 209 synchronous modems or equivalent. Clocking is supplied by the modem and speeds up to 19,200 bps can be used. The DMC11-DA includes data set control for full-duplex or half-duplex, private wire or switched operation. A 25-foot cable with 25-pin EIA connector is included.

CONFIGURATIONS

Where two PDP-11s are to be interconnected locally by coaxial cable, a DMC11 is required at each end of the link. For operation at 1,000,000 bps, each DMC11 would include a DMC11-AD and a DMC11-MA. For operation at 56,000 bps, each DMC11 would include a DMC11-AD and a DMC11-MD. In addition, one coaxial cable is needed for half-duplex operation, two for full-duplex operation.

Where two PDP-11s are to be interconnected remotely by synchronous modems and common carrier facilities, DMC11s can be used at each end of a link. Each DMC11 would include a DMC11-AD and a DMC11-DA. The modems can be Bell 200 series synchronous modems or any equivalent synchronous modem conforming to the RS232C interface specification and compatible with the communications channel. Operation can be up to 19,200 bps.

A PDP-11 can be interconnected remotely to another computer system that can interface to synchronous modems and support the DDCMP protocol. The configuration would include a DMC11-AD, DMC11-DA, synchronous modems and compatible communications facilities. At the remote end would be the appropriate communication interface and computer system software implementing the DDCMP protocol.

CABLES

Local operation uses inexpensive coaxial cable and standard connectors. One cable is needed for half-duplex operation, two for full-duplex operation. The required cable, complete with connectors, is available from DIGITAL in a 100-foot length (BC03N-A0). When longer lengths are needed, or the systems are not located in the same room, the customer is responsible for supplying and installing the cable. It is suggested that the cable be installed well before delivery of the DMC11s.

MAINTENANCE FEATURES

The DMC11 contains a number of features that ensure reliable operation and ease of maintenance. During normal operation, the DMC11 keeps count of communications, errors and retransmissions. These counts are recorded in PDP-11 memory. Occasional retransmissions are handled

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automatically by the DMC11 but repeated errors will result in an interrupt to the PDP-11 to inform the program that action is needed (such as calling the common carrier).

The DMC11-AD microprocessor can be single-stepped by a diagnostic program to verify correct operation. The diagnostic program can supply special micro-instructions to thoroughly exercise the DMC11 logic. It can also verify the contents of the ROM program.

The DMC11-MA, DMC11-MD and DMC11-DA line units can be single-stepped by a diagnostic program to verify correct operation. Programmable loopback prior to the built-in modem or EIA level converters, together with a free-running maintenance clock, enable the majority of DMC11 logic to be exercised without disconnecting any cables. Special Coax and EIA turnaround connectors are supplied to provide a complete test of a DMC11.

DMC11 OPERATION

All communications between the PDP-11 and the DMC11 are through eight bytes of control and status registers. Four bytes of these registers are multipurpose. Their meaning is controlled by the other registers and their use is governed by the DMC11 microprocessor. All commands, command completions and status information pass through these registers.

The PDP-11 program is completely insulated by the DMC11 from the communications link and the DDCMP protocol. When the program initializes the DDCMP protocol it defines the characteristics of the link with a single command. From that point on, the DMC11 will perform all data-link control activities, notifying the user of failures only after an error threshold has been exceeded.

The program initializes the DMC11 by supplying the address of a core memory area which the DMC11 uses to keep a snapshot of protocol activity for powerfail recovery and defining the characteristics of the data link.

From that point on, all the program need do is to request and then use the multipurpose registers to provide the bus address and byte count of messages to be transmitted or buffers to be filled on reception. The DMC11 is multiple buffered. Up to seven messages for the transmitter and seven buffers for the receiver can be queued by the DMC11.

After a bus address/byte count has been assigned, the DMC11 assures error-free sequential message transfer by use of the DDCMP protocol. Transmit commands will be reported as completed when successfully acknowledged. Receive commands will be reported as completed when an entire message has been successfully received in correct sequence. Successful command completion will interrupt the PDP-11 processor, if enabled.

POWERFAIL RECOVERY

The DMC11 may be programmed to either cold start or warm start on powerfail recovery. Cold starting initiates the DDCMP startup sequence

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to make certain that the remote system is aware of the restart. A cold start resets all the DDCMP sequence numbers so the status of previously transmitted but unacknowledged messages is indeterminate.

To warm start, the DMC11 utilizes the snapshot of protocol operation kept in core memory. Restarting proceeds at the state indicated. Messages being transmitted at the time of power failure will be retransmitted as necessary. By using the DDCMP sequence numbers (stored in the core memory area) correct recovery of all messages without loss or duplication is assured, providing that neither end of the link does a cold start. Should only one end of a link experience a lengthy power failure, the other end will exceed an error threshold and cause a status interrupt. However, a remote DMC11 will not initiate a cold start unless commanded by the remote PDP-11 program. Recovery from lengthy power failures or communications outages is possible.

MULTIPLE DMC11s ON A SYSTEM

Up to 16 DMC11s may be connected to a system for operation at 56Kb or lower speeds. At 1Mb, two DMC11s may be connected for full-duplex operation, four for half-duplex operation.

DMC11 PROGRAMMING

Programming the DMC11 is best described at two levels. The first level describes how a PDP-11 program uses the DMC11 control and status registers together with the interrupt system for transfer of control and status information between the PDP-11 program and the DMC11 microprogram. The second level describes details of these transactions, including formats, details of device and protocol initialization, data transfer and unusual cases.

In order to successfully program the DMC11 it is not necessary to be familiar with the details of DDCMP protocol operation. These are handled by the DMC11 microprogram. However some familiarity with the protocol operation will be useful in interpreting the significance of the various error counters provided to assess the quality of the circuit connecting the two computers. If a DMC11 is to communicate with a different interface which uses a software implementation of DDCMP, the person programming the software implementation should consult the DDCMP protocol standard document.

CONTROL AND STATUS REGISTERS

Communication of control and status information between the PDP-11 and the DMC11 uses eight bytes of control and status registers (CSR's). These are addressed as 76XXX0, 76XXX1, 76XXX2, 76XXX3, 76XXX4, 76XXX5, 76XXX6, and 76XXX7. These device addresses will be subsequently referred to as Byte Select 0 to 7 (BSEL0-BSEL7) for indicating individual bytes and as SEL0, SEL2, SEL4, and SEL6 for indicating words.

NOTE

The Control and Status Registers are implemented with Random Access Memory (RAM). Thus at power on, the CSR's will come up in

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random states. As part of the microprocessor initialization the CSR's (SELO-6) will be cleared with the exception of bit 15 of SELO (RUN) which will be set. The lower order 8 bits of SELO (BSELO) will be cleared first. Due to the high speed of the microprocessor the registers will be cleared before access by the PDP-11 is possible.

BSEL4-7 comprise a 32 bit data port used to pass information between the microprocessor and the PDP-11. When the data port is used to transfer information from the PDP-11 to the microprocessor this will be called an Input Transfer, often abbreviated "IN" or "I". When the data port is used to transfer information from the microprocessor to the PDP-11 this will be called an Output Transfer, often abbreviated "OUT" or "O". These terms are not to be confused with sending and receiving data on the serial line which will be called "sending" or "transmission," "receiving" or "reception."

BSELO controls input transfers and BSEL2 controls output transfers. BSEL1 contains bits used for maintenance purposes which are not of concern to the programmer. It also contains the MASTER CLEAR bit which can be used to initialize the DMC11 microprocessor. BSEL2 is not used. A switch on the microprocessor module prevents the PDP-11 program from clearing RUN or performing other maintenance functions in BSEL1 which would disable the microprocessor's ability to initialize an unattended PDP-11 computer system.

INPUT TRANSFERS

Whenever the data port is not in use it is subject to being seized by the microprocessor for use in an output transfer. Therefore the PDP-11 program must request the microprocessor to assign it the port before proceeding with an input transfer. It must also specify the type of input transfer (a transmit buffer, a receive buffer, control information, etc.) so the microprocessor can make appropriate preparations.

The PDP-11 program should set bits 0-2 of BSELO to indicate the type of transfer and then set bit 5, Request in (RQI) to request the port. (These bits may be set by a single instruction.) The microprocessor will respond by setting bit 7, Ready In (RDYI) when the port has been assigned to the PDP-11 program. When RDYI has been set the PDP-11 program should load the desired data into the data port (BSEL4-7). Then it should clear RQI. The microprocessor will take the data and drop RDYI which completes the transfer.

Bit 6 of BSELO, Interrupt Enable Input (IEI), controls whether the PDP-11 program receives an interrupt (to Vector XX0) when the microprocessor has set RDYI. The microprocessor will respond to RQI immediately (within 10 microseconds) except when operating full duplex at 1 mb with both the transmitter and receiver active. It is most efficient for the PDP-11 to have interrupts disabled and simply scan RDYI one or more times until the microprocessor has set it. While the PDP-11 program is waiting it must be prepared to accept an output transfer because the microprocessor may have seized the port in the meanwhile.

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The microprocessor can not service certain types of input transfers immediately. (For example, the PDP-11 program may attempt to queue more than 7 buffers for transmission.) In these cases it is convenient to use interrupts. If the PDP-11 program finds RDYI clear after several scans it can enable interrupts by setting IEI with a BIS or MOV instruction. The DMC11 will interrupt the PDP-11 (to Vector XX0) when the microprocessor has set RDYI. The PDP-11 program will get the interrupt in all cases—even if the microprocessor had already set RDYI at the time the program sets IEI. The program can bypass any scanning if IEI is set when the program sets RQI.

Note

The PDP-11 program should not begin a new input transfer until the previous transfer has been completed, as indicated by the microprocessor clearing RDYI. The microprocessor will do this within 10 microseconds after the program has cleared RQI. If the PDP-11 program wishes to begin a new transfer immediately it should check that RDYI has been cleared before setting RQI. This can be done by scanning RDYI until it has been cleared.

OUTPUT TRANSFERS

The microprocessor initiates an output transfer when it has status or error information to transfer to the PDP-11 program or it wishes to return a full buffer on reception or an empty buffer on transmission. The microprocessor can initiate an output transfer at any time the data port is free, i.e. not assigned to the PDP-11 program for an input transfer and not in use for a previous output transfer. However if the PDP-11 has initialized the DMC11 by setting MASTER CLEAR or generating the INIT signal on the UNIBUS, the microprocessor will not generate any output transfers until it has been initialized by the PDP-11 program.

The microprocessor loads status or error information into the data port (BSEL4-7) and sets bits 0-2 of BSEL2 to indicate the format and significance of the data. It then sets bit 7 of BSEL2, Ready Out (RDYO) to indicate to the PDP-11 program that data is available. In response to RDYO setting, the PDP-11 program should note the type of output transfer as specified in bits 0-2 of BSEL2 and read the data in the data port. When the PDP-11 program has sampled all the data it must complete the output transfer by clearing RDYO. This frees the data port for a subsequent transaction.

If the PDP-11 program wishes, it can enable interrupts on output transfers by setting bit 6 of BSEL2, Interrupt Enable Output (IEO). If IEO is set the DMC11 will interrupt the PDP-11 (to Vector XX4) after the microprocessor has set RDYO. Since the PDP-11 program will usually not know when an output transfer will occur (for example, when a message will be received) an efficient PDP-11 program will ordinarily enable interrupts on output transfers.

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Note

The PDP-11 program must respond to RDYO being set by reading the data and clearing RDYO. Failure to do this will prevent the data port from being freed. If the PDP-11 program has requested an input transfer by setting RQI it must be prepared to respond to an output transfer prior to being given RDYI. If the PDP-11 program fails to respond to RDYO it will never get RDYI. The PDP-11 program should not spin on RDYI in a loop that doesn't also test RDYO unless interrupts on output transfers are enabled, and the loop executes at a lower priority than the DMC11 interrupt priority.

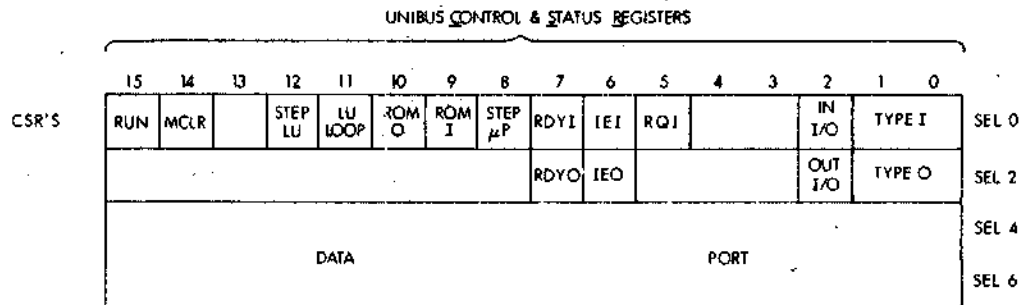


Figure 1

SELO

BIT	NAME	FUNCTION
1-0	TYPEI	Defines type of input transfer
		BIT 1 BIT 0
		0 0 Buffer Address/Character Count In (BA/CC I)
		0 1 Control In (CNTL I)
		1 0 reserved
		1 1 Base In (BASE I)
2	IN I/O	Set or cleared by PDP-11. 0 indicates transmission, 1 reception
3-4		reserved
5	RQI	Set by the PDP-11 to request an input transfer, cleared by the PDP-11 when data has been loaded
6	IEI	Set or cleared by PDP-11. If set the PDP-11 is interrupted to Vector XX0 when RDYI is set
7	RDYI	Set by the microprocessor in response to RQI to indicate the data port is available for an input transfer. Cleared by the microprocessor at the end of an input transfer
8	STEP μP	Maintenance only

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BIT	NAME	FUNCTION
9	ROM I	Maintenance only
10	ROM O	Maintenance only
11	LU LOOP	Maintenance only
12	STEP LU	Maintenance only
13		reserved
14	MASTER CLEAR	Setting this bit initializes the DMC11. This bit is self clearing
15	RUN	Maintenance only
SEL2		
1-0	TYPEO	Defines type of output transfer
		BIT 1 BIT 0
		0 0 Buffer Address/Character Count Out (BA/CC 0)
		0 1 Control Out (CNTL O)
		1 0 reserved
		1 1 reserved
2	OUT I/O	Set or cleared by the microprocessor. 0 indicates transmission, 1 reception
3-5		reserved
6	IEO	Set or cleared by PDP-11. If set the PDP 11 is interrupted to Vector XX4 when RDYO is set
7	RDYO	Set by the microprocessor when an output transfer is ready, cleared by PDP-11 when it has completed the output transfer
8-15		reserved
SEL4		
15-0	First half of the Data Port	
SEL6		
15-0	Second half of the Data Port	
		The format and contents of the data port depend on the transfer type. (TYPEI or TYPEO). Loaded by the PDP-11 on input transfers, loaded by the microprocessor on output transfers

INITIALIZATION

The power up sequence and UNIBUS INIT signal initialize the DMC11. The PDP-11 program can accomplish the same effect by setting MASTER CLEAR in BSEL1. Any of the above restart the microprocessor to the beginning of its microprogram. In this state the microprocessor will not send or receive messages on the serial line or generate output transfers.

When the PDP-11 program wishes the DMC11 to function it must perform an input transfer that specifies the base address of a 128 word table in PDP-11 memory subsequently called the Base Table. The PDP-11 program requests the BASEI transfer by setting TYPEI to 11. In response

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to RDYI, the program loads the low order 16 bits of the address into SEL4 and the high order 2 bits of the address into bits 15 and 14 of SEL6. If the DDCMP protocol operation is to be initialized, the RESUME bit (bit 13 of SEL6) must be clear.

Once the PDP-11 has specified a base address the 128 word base table "belongs" to the microprocessor until the DMC11 is master cleared by INIT or MASTER CLEAR. The PDP-11 program may examine the contents of the base table (for example, error counters relating to protocol operation) but must not alter its contents.

By supplying a base address with the RESUME bit clear the microprocessor is conditioned to respond to the DDCMP start-up sequence received from the remote system. However the microprocessor will not initiate the start-up sequence on its own accord unless the PDP-11 program supplies a buffer of data to be transmitted.

If the DMC11 is connected to a half-duplex channel the PDP-11 program must now perform an input transfer using the Control In format and set the Half Duplex bit (HD) in SEL6 (bit 10). In addition the program must specify whether the DMC11 is to operate as a half duplex Secondary station (3 second timer) or a half duplex Primary station (1 second timer) by setting or clearing the Secondary bit (SEC) in SEL6 (bit 11). A half duplex link must have one primary station and one secondary station. The only difference between the two is in the length of time spent before retransmitting in case of errors. Half duplex operation may be specified at any time by a Control In transfer to accommodate switching to a half duplex back up communications channel.

DDCMP START UP

Before data messages may be transmitted or received the DDCMP start-up sequence must be completed to make certain both ends of the link are correctly initialized and to place the protocol in the Running state. Either end may initiate the start sequence or both ends may do so simultaneously. If the PDP-11 program supplies a buffer of data to be transmitted, the local DMC11 will initiate the start sequence.

The PDP-11 program may ignore the details of the start sequence. However one important property of the sequence is significant. Once the local DMC11 has entered the Running state it will detect and flag as an error the fact that the other end has initiated the start sequence. The PDP-11 program will receive a Control Out transfer with SEL6 bit 7 (DDCMP START REC'D) set. If this happens, the PDP-11 program knows that the other end of the link has restarted. The PDP-11 program should initialize the DMC11 and begin again.

DATA TRANSMISSION

When the PDP-11 program wishes to transmit a buffer of data it clears bits 1 and 0 of BSEL0 to indicate a Buffer Address/Character Count In transfer and clears bit 2 of BSEL0, (IN I/O) to specify that this is a full buffer to be transmitted. It then requests an input transfer by setting RQI. In response to RDYI it loads SEL4 with the low order 16 bits of the buffer address, bits 15 and 14 of SEL6 with the high order bits of the

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address and bits 13 to 0 of SEL6 with the 14 bit character count. Buffers from 1 to 16,383 bytes long may be used for local operation. For remote operation buffers are limited to a practical maximum of about 512 bytes, depending on the error rate of the communications facilities. Each buffer corresponds to a single DDCMP data message.

When the message has been successfully transmitted and an acknowledgment received, the microprocessor will initiate an output transfer with bits 1 and 0 of BSEL2 clear to indicate the Buffer Address/ Character Count Out (BA/CC O) format. Bit 2 (OUT I/O) will be clear to indicate that a successfully transmitted buffer has been returned to the program.

The PDP-11 program may queue up to seven buffers for transmission by supplying buffers to the microprocessor faster than it returns them. An attempt to queue more than seven buffers will force the microprocessor to delay granting the request for the input transfer until a buffer has been returned.

Note

The PDP-11 program should not request an input transfer that will supply a transmit buffer if 7 are already outstanding unless it is certain that the other end of the link will supply enough buffers for reception. In particular, if two PDP-11's connected by DMC11's attempt to queue up 8 buffers while no receive buffers are queued they will be deadlocked and must initialize their DMC11's.

DATA RECEPTION

When the PDP-11 program has an empty buffer it wishes to fill with received data it clears bits 1 and 0 of BSEL0 to indicate a BA/CC I transfer and sets bit 2 of BSEL0 (IN I/O) to specify that an empty buffer has been made available for reception. It then requests an input transfer by setting RQI. In response to RDYI it loads SEL4 and SEL6 with the buffer address and character count, in the same format as for transmission. The character count must be large enough to accommodate the longest message expected.

When a message has been successfully received and stored in the buffer the microprocessor will initiate an output transfer with bits 1 and 0 of BSEL2 clear to indicate the BA/CC O format. Bit 2 (OUT I/O) will be set to indicate a full buffer has been received. SEL4 and SEL6 will contain the address of the buffer and the actual number of characters received.

If a message is received when no receive buffer is available the microprocessor will inform the PDP-11 by means of a Control Out transfer with bit 2 of SEL6 (O'RUN) set. The other end of the link will be informed of the error and will automatically retransmit the message. The PDP-11 program should supply a buffer as soon as possible.

The PDP-11 may queue up to seven empty buffers for reception by supplying them to the microprocessor faster than it returns buffers. An

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attempt to queue more than seven buffers will force the microprocessor to delay granting the request for input transfer until a full buffer has been returned.

Note

The PDP-11 program should not request an input transfer that will supply a buffer for reception if 7 are already outstanding unless it is certain that the other end of the link will be supplying buffers for transmission.

CONTROL OUT TRANSFERS

The microprocessor informs the PDP-11 program of unusual or error conditions involving the communications channel, remote end of the link, DMC11 hardware or PDP-11 program by means of an output transfer with bit 1 of BSEL2 clear and bit 0 set indicating a Control Out (CNTL 0) transfer. SEL6 contains bits that indicate the error condition. Some errors are advisory in nature and normal operation may continue. Others are fatal and require the PDP-11 program to initialize the DMC11.

Bit 0 (DATA CK) indicates that a retransmission threshold has been exceeded. (More than 7 consecutive retransmissions have occurred for transmission or reception.) This indicates a defective communications channel or that the other end of the link has failed to supply a buffer for reception. The PDP-11 can examine error counters in the base table for more details of the error. This is a non-fatal error. Should the cause of the error be corrected normal operation will continue with no messages lost in either direction. This error may appear repeatedly until the condition is corrected or until the DMC11 is initialized. Transient errors corrected before 7 retransmissions will not be reported to the PDP-11 program but will be counted in the base table.

Bit 1 (TIME OUT) indicates that the microprocessor has received no response from the remote end of the link for a specified period (21 seconds). This indicates a broken communications channel or a failure at the other end of the link (possibly a power failure). Like DATA CK, this is a non-fatal error which can occur repeatedly.

Bit 2 (O'RUN) indicates that a message was received but no buffer was available. This is a non-fatal error. The PDP-11 program can prevent this error from recurring repeatedly by supplying a buffer.

Bit 3 (DDCMP MAINT REC'D) indicates that a message in the DDCMP Maintenance format was received and that the protocol operation has entered the Maintenance state (see below).

Bit 4 (LOST DATA) indicates that a message was received that is longer than the buffer supplied by the PDP-11 program. This is a fatal error.

Bit 6 (DISCONNECT) indicates that an on to off transition of the modem data set ready lead has been detected (remote operation only). This is a non-fatal error. For dial up operation the PDP-11 program must con-

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sider the possibility that a new caller has connected to the DMC11 if this is required by security considerations.

Bit 7 (DDCMP START REC'D) indicates that a DDCMP Start message was received when the protocol was in the Running or Maintenance states. This indicates that the remote computer has initialized its end of the link. This is a fatal error. The PDP-11 program may initialize the DMC11 if it wishes to start over and complete the start-up sequence.

Bit 8 (NON EX MEM) indicates that a UNIBUS address time out has occurred. The PDP-11 program specified an invalid base address, buffer address, or count, stored illegally into the base table or PDP-11 memory is defective. This is a fatal error.

Bit 9 (PROC ERR) indicates a procedure error on the part of the PDP-11 program. The requested input transfer can not be honored due to a programming error. Requesting a BA/CC before supplying a base address, requesting a base address a second time, or specifying an invalid code in BSEL0 bits 1 and 0 will cause this error. This is a fatal error.

MAINTENANCE MESSAGES

A special DDCMP message format, the Maintenance message, is used for down line loading, restarting, or otherwise maintaining satellite computer systems. Messages in this format are subject to error checking but are unsequenced, unacknowledged, and not retransmitted automatically by the DMC11. Transmission is always half duplex.

Maintenance messages can only be sent and received while the microprocessor is in the DDCMP maintenance state. The PDP-11 program may cause the microprocessor to enter this state by a CNTL 1 transfer with bit 8 of SEL6 (DDCMP MAINT) set. The microprocessor will enter the Maintenance state if a maintenance message is received. In this case, the microprocessor will perform a CNTL 0 transfer with DDCMP MAINT REC'D set in SEL6 to indicate the state change and availability of a maintenance message.

Once in DDCMP maintenance mode, maintenance messages can be sent and received similarly to data messages. On transmission the data portion of the message is taken from the buffer with the DMC11 generating the header and CRC's. On reception only the data portion is placed in the buffer. Messages not in DDCMP maintenance format or having incorrect CRC's are simply discarded.

The data portion of the maintenance message may contain any data that is desired, but ordinarily will conform to the Digital Maintenance Operation Protocol (MOP) formats. When a host computer wishes to restart a satellite computer system it must send the appropriate MOP messages as described below. In order to leave Maintenance mode the PDP-11 program must initialize the DMC11 and supply a base address with the RESUME bit clear.

REMOTE LOAD DETECT AND DOWN LINE LOAD

Whenever the microprocessor is running it is constantly scanning the serial line for a DDCMP maintenance message containing an "ENTER

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MOP MODE" data field. What happens when this particular message is received depends on the setting of two switch packs on the DMC11 line unit. Depending on the setting of these switches, the DMC11 will either commence down line loading in MOP mode, trigger the PDP-11 to begin executing a program in a read only memory (ROM) bootstrap (BM873, M9301, etc.) or simply pass the data to the PDP-11 as an ordinary maintenance message. In case a ROM bootstrap is triggered, switches on the line unit specify an 8 bit word-offset to the bootstrap address space.

The data portion of the ENTER MOP MODE message is 5 bytes long. The first byte contains 6 and the remaining 4 bytes the same 8 bit value repeated four times. This value is specified by a switch pack on the DMC11 line unit and serves as a password to protect against inadvertent recognition of the ENTER MOP MODE message.

If an ENTER MOP MODE message is recognized and the switches specify to commence down line loading, the DMC11 microprocessor "takes over" the PDP-11 computer system. All peripherals on the system are initialized by an INIT sequence and the processor is placed into a tight loop where it remains until control is transferred to a program loaded down the line.

In response to the ENTER MOP MODE message the DMC11 will send a "REQUEST MOP SECONDARY MODE" message in DDCMP maintenance format containing a data field three bytes long equal to 8, 12, 1. This informs the remote end that the ENTER MOP MODE message was received.

The remote end should now send a "MEMORY LOAD WITH TRANSFER ADDRESS" message in DDCMP maintenance format. The first two bytes are zero, the next 4 bytes are an 18 bit memory address right justified, followed by a memory image to be loaded and four bytes of transfer address.

Once this message has been successfully received the DMC11 will start the PDP-11 program at the specified transfer address. The DMC11 must be initialized before it does anything else except recognize a subsequent ENTER MOP MODE maintenance message.

POWER FAIL RECOVERY

The DMC11 keeps all data necessary to recover from a power failure in its base table. When the PDP-11 program detects a power failure it should cease requesting input transfers and not respond to output transfers. When power has been restored the PDP-11 power recovery program can tell the DMC11 microprocessor to recover from the error by performing a BASE I transfer with the RESUME bit set. The original base address must be specified and the contents of the base table must be the same as they were when power was lost. Otherwise the program must start over. (RESUME bit clear). As part of the power recovery the PDP-11 program must repeat an uncompleted input transfer. It must set IEI and IEO as desired. The microprocessor will repeat an uncompleted output transfer.

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DATA SET CONTROL

If the switches on the DMC11 line unit specify bootstrap ROM triggering or down-line loading, the microprocessor will maintain Data Terminal Ready continuously, dropping it for a one second period following an on to off transition of Data Set Ready. Otherwise, the DMC11 will not turn Data Terminal Ready on until it has received a base address. It will drop Data Terminal Ready when initialized by INIT or MASTER CLEAR and it will drop it for one second following an on to off transition of Data Set Ready. An on to off transition of Data Set Ready will provide a CNTL 0 transfer as described above if the DMC11 has been given a base address.

DATA PORT MESSAGE FORMATS

1. BA/CC I and BA/CC 0 format

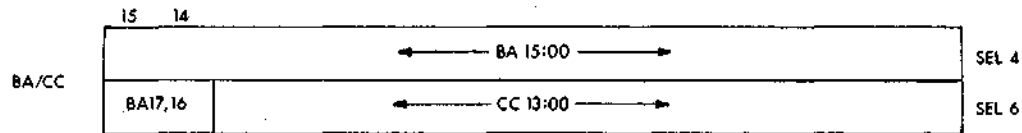


Figure 2

SEL4	bits 15-0	BA 15:00	The low order 16 bits of the 18 bit buffer address
SEL6	bits 15-14	BA 17:16	The high order 2 bits of the 18 bit buffer address
	bits 13-0	CC 13:00	The 14 bit character count (in positive notation, not complement form)

2. BASE I format

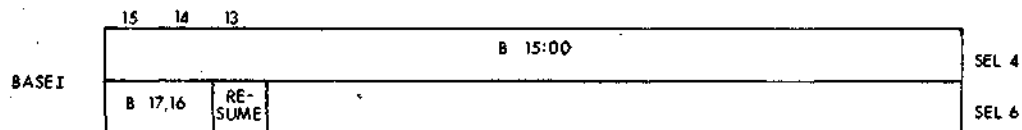


Figure 3

SEL4	bits 15-0	B 15:00	The low order 16 bits of the 18 bit base address of the 128 word base table
SEL6	bits 15-14	B 17:16	The high order 2 bits of the 18 bit base address
	bit 13	RESUME	If clear the microprocessor initializes the base table and protocol. If set the microprocessor resumes operation as specified by the contents of the base table

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3. CNTL I format

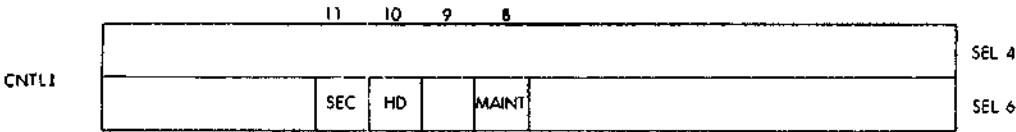


Figure 4

SEL6	bit 11	SEC	If set indicates a half duplex secondary station. If clear indicates a half duplex primary station. Not used for full duplex
	bit 10	HD	If set indicates half duplex DDCMP operation is required. If clear full duplex is required. Must be used with bit 11, SEC
	bit 8	MAINT	If set the microprocessor enters the DDCMP maintenance mode and remains in that mode until subsequently initialized

4. CNTL O format

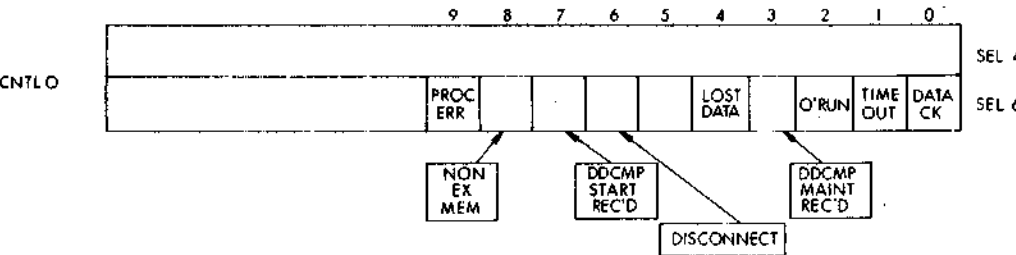


Figure 5

See the section on Control Out Transfers for the use of these bits.

SYSTEM ADDRESSES

The DMC11 uses eight (8) Bytes of floating address space. The addresses as used for DDCMP and SDLC are:

- 76XXX0 Control IN status register
- 76XXX1 Maintenance register

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76XXX2	Control OUT register
76XXX3	Reserved
76XXX4	I/O Transfer port
76XXX5	I/O Transfer port
76XXX6	I/O transfer port
76XXX7	I/O transfer port

The relative position of the DMC11 within the floating address system is number six, directly following DUP11.

VECTOR ASSIGNMENT

The DMC11 uses two vectors (mod 10) XX0 and XX4. Interrupts are vectored to XX0 for RYDI and to XX4 for RDYO if the respective interrupt enable is set. The vector assignment is within the floating vector system—relative position is number 24 directly following DWUN.

PROGRAM INTERRUPT PRIORITY

The DMC11 interrupt priority for Vectors XX0 and XX4 are controlled by one standard PDP-11 priority connector. The priority can be changed by substituting the appropriate priority connectors. DMC11's will be shipped with a priority 5 connector.

SPECIFICATIONS

DMC11-AD—DDCMP Microprocessor Module

Protocol	DDCMP
Type of Operation	Full duplex or half duplex, point to point
Data Format	8 bit bytes, DDCMP message formats
Data Transfers	16 bit NPR (8 bit NPR at beginning or end of buffers where required)
Status Area in PDP-11 Memory	Location: Programmable Size: 128 words
Mounting Space	One hex SPC slot in DD11-B, DD11-C, or DD11-D back-plane
Bus Loading	One UNIBUS load
Power Consumption	4.0 amps at +5V
Operating Temperature	+10 to +40°C
Humidity	10 to 90%
Reference	DEC STD 102—Class C device

DMC11-MA, DMC11-MD—Line Unit Modules (Local)

Operating Mode	Half duplex (single cable), full duplex (two cables)
Data Format	Synchronous serial by bit, LSB first
Character Size	8 bits
Block Check	16 bit CRC-16 polynomial
Data Rate	1,000,000 bps (DMC11-MA), 56,000 bps (DMC11-MD)
Maximum Distance	6,000 feet (DMC11-MA), 18,000 feet (DMC11-MD)
Modulation	Diphase (double freq.) NRZ
Transmitter Timing	RC Osc., trimmable $\pm 5\%$
Receiver Timing	From received signal

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Line Interface	Transformer coupled
Common Mode Rejection	500 to 1
Transmitter Signal	4 volts P-P
Receiver Signal	150 mv (min.) P-P
Cable Type	Belden 8232 or equivalent (not supplied)
Connector Type	AMP 20606X series
Mounting Space	One hex SPC slot (DD11B, C or D), cut out permits use in end slots of backplane as well
Power Consumption	2.5 amps at +5V .046 amps at -15V .018 amps at +15V

DMC11-DA—Line Unit Module (remote)

Operating Mode	Full or half duplex
Communications Channel	Private wire or switched
Data Format	Synchronous, serial by bit, LSB first
Character Size	8 bits
Block Check	16 bit CRC-16 polynomial
Data Rate	Up to 19,200 bps (clocked by modem)
Interface	RS232C or CCITT V.24 compatible
Modems	Bell 208, 209 or equivalent
Signals Supported	BA transmit data DB serial clock transmit (SCT) BB receive data DD serial clock receive (SCR) CC data set ready CD data terminal ready CA request to send CB clear to send
Cable	25 foot with EIA connector supplied
Mounting Space	One hex SPC slot (DD11B, C or D), cutout permits use in end slots of backplane as well
Power Consumption	2.5 amps at +5V .31 amps at -15V .03 amps at +15V

ORDERING INFORMATION

DEC No.	Prerequisite	Description
DMC11-AD	PDP-11	DDCMP Microprocessor
DMC11-MA	DMC11-AD	1 Mb local line unit
DMC11-MD	DMC11-AD	56 Kb local line unit
DMC11-DA	DMC11-AD	remote (EIA) line unit
BC03N-A0	DMC11-MA or MD	100 foot coax cable

RELATED DOCUMENTATION

DDCMP Protocol Specification V3.2

AUTOMATIC CALLING UNIT INTERFACE, DN11**DESCRIPTION**

With the DN11 and a Bell 801 Automatic Calling Unit (ACU), any PDP-11 can dial any telephone number in the Direct Distance Dial Network and establish a data link. The DN11 is a digit-buffered interface, and digits to be dialed are presented as four-bit binary numbers. The interface drives the ACU with EIA-232-C voltages and is connected via a standard 25-pin plug.

The programmer has access to all lines of the 801 through the DN11. The 801 presents the following leads to the DN11: Power Indicator, Data Line Occupied, Abandon Call and Retry, Data Set Status and Present Next Digit. The DN11 provides the following leads to the 801: Digit Present, Call Request and four Digit Leads.

Because the PDP-11 UNIBUS serves as a multiplexer, multiple automatic calling units can be added to the PDP-11. One PDP-11 System Unit accepts up to four 801 ACU Interfaces. Each interface looks like one device to the UNIBUS.

The Sequence of Operations

The following describes the use of the DN11 to originate a DDD call. This is an automated version of the procedure that everyone goes through when placing a telephone call.

1. Turn 801 power on (PWI = 0).
2. Check for unoccupied data line (DLO = 0).
3. Set Call Request bit (FCRQ = 1).
4. The 801 will seize the line on receiving the dial tone and assert Present Next Digit which causes a PDP-11 program interrupt (FPND = 1).
5. The line is now in use and the Data Line Occupied bit is set (DLO = 1).
6. The first digit to be dialed is provided by loading the four least significant bits of the byte into the digit bits (8 to 11) of the DN11 status register. The upper four bits of the byte are read-only and can have any value during the loading of the four low-order bits.
7. The 801 is informed that the 1st digit has been loaded by asserting the Digit Present Bit (FDPR = 1).
8. The 801 then reads Digit leads 1 through 4 and lowers Present Next Digit Lead (FPND = 0).
9. The hardware responds and lowers Digit Present Lead (FDPR = 0).
10. The 801 then dials the first digit and again raises Present Next Digit Lead (FPND = 1).

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11. The next digit is loaded and the Digit Present bit is asserted (FDPR = 1).
12. Sequences 6 through 10 are repeated until all digits have been dialed.
13. When the last digit has been dialed, one of two procedures must be used to complete the call.

- a) If "handshaking signals" are used (Bell 100 series modems or equivalent):

A Detect Answer option is used. The 801 retains line control and looks for an answering tone, from the called station. Upon receiving the tone the modem is connected to the line, Data Set Status is asserted and a program interrupt is generated (DSS = 1). This stops the Abandon Call and Retry timer which would have been initiated had no tone been received. These, in turn, would have generated a signal to the DN11 and cause a program interrupt with the Abandon Call and Retry bit set (ACR = 1). The program would then either retry or drop the call.

- b) If using modems without the automatic handshaking feature:

The End-of-Number (EON) mode must be used. EON is sent after the last digit has been dialed. This causes the 801 to connect the modem to the line and assert Data-Set Status (DSS = 1). However, the modem and its controller must be able to determine when the called station has answered and is sending data. To do this, it is necessary to use an 801 with option "Y" (available from the Telephone Company). This option lets the Abandon Call and Retry timer continue running even after the DSS bit has been set. When the ACR timer times out it will notify the user of the line to check if data is being received by the modem.

14. There are two options available when terminating a call:

- a) The Call Request bit is set to zero (FCRQ = 0). This will remain until the Data Line Occupied bit also goes to zero (DLO = 0), which is a necessary condition before a new call can be initiated.

- b) If the 801 option "Z" is used, the call can be terminated by clearing Data Terminal Ready in the modem. In this case, dropping Call Request will not terminate the call. However, it must be dropped before a new call can be attempted.

15. Should the 801 lose power during a call an interrupt will be generated and the Power Off bit will be set (PWI = 1). The interface will not return an interrupt if the Call Request bit is set with the power off (FCRQ = 1).

Programming

Each ACU interface contains one register and therefore requires one

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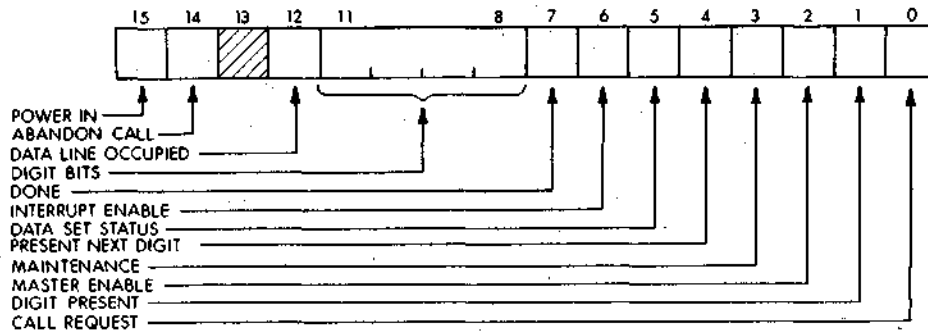
16-bit address. Address space has been assigned for 64 interfaces. The four addresses for the four interfaces that can be plugged into one system unit must be consecutive addresses starting with 775XX0 where XX = 20 for the first line. If only one line is in use, it uses address 775 200. Interface number 2 has address 775 202, and interface number 64 has address 775 376.

Note: In addition to the individual Interrupt Enable bit for each interface, there is a master enable bit associated with line number 1 of a given system unit. It enables the interrupts for the entire group. The master enable bit on lines 2 through 4 of a given system unit are ignored by the interface.

Each set of four DN11's require one interrupt vector. The vector address for communications options are assigned in the range from 300 to 777. (See Appendix A).

All units are shipped with the bus request line set to BR4. This can be changed in the field with a Bus Request Priority Jumper Plug.

ACU Interface Status Register



BIT	NAME	FUNCTION
15	Power Indicate (PWI)	This bit is normally zero and is set by the ACU whenever power is switched off at the unit. If a call is in progress at that time, DONE is set. This causes an interrupt if INTENB and MINAB = 1 (Read only).
14	Abandon Call and Retry (ACR)	A control lead from the ACU. This bit is set by the ACU whenever an internal timer times out. The timer is reset by the ACU whenever it gives PND and is for detecting wrong numbers and busy signals. It is inhibited by the presence of DSS except if

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		<p>the 801 option "Y" is in use; it times out even then and gives an interrupt (by setting DONE). This is used when the programmer wants a timer to detect wrong numbers and busy signals.</p>
12	Data Line Occupied (FDLO)	<p>This bit is set by the ACU whenever the line to the telephone central office is being used by the ACU. It allows the programmer to test the ACU to see if the last call was successfully terminated before he tries to use it for the next one (Read only).</p>
11-8	Digit Bits (NB1-4)	<p>These four bits are control leads to the ACU. These low order bits of the second byte make up the BCD digit to be dialed. Since the high-order four are read only, it does not matter what is in them during a load, and the programmer may use them as he wishes. In MAINT mode, these bits are used to drive the four control lines that can cause interrupts. See bit 3 for description (Read/Write).</p>
7	DONE	<p>This bit is set to indicate that the ACU is done with the previously requested action and ready to accept new data, usually the next digit in a sequence to be dialed.</p> <p>The conditions that set DONE are listed (CRQ must be a one):</p> <ol style="list-style-type: none">1. Transition of PND to one (after CRQ set or previous DPR set).2. Transition of DSS to one (after last DPR or EON).3. Transition of ACR to one (if timeout error—anytime).4. Transition of PW1 to one (if power switched off) (Read/Write)
6	Interrupt Enable (INTENB)	<p>This bit allows the setting of done to cause an interrupt if the master enable bit (bit 02 line # 1 of a system unit) is set (Read/Write).</p>
5	Data Set Status (DSS)	<p>Control lead from ACU. This is a statement by the ACU that the called party has answered and that the associated data set now has control of the line. It is accom-</p>

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panied by the setting of DONE to obtain an interrupt. It remains set until after the end of the call (or until the data terminal ready lead to the associated modem is dropped which then drops FDSS).

If the associated modem answers a call while the dialer is in use (CRQ = 1), then DSS will be enabled and DONE set. If interrupt Enable is set there will be an interrupt (Read only).

4 Present Next Digit (FPND)

Control lead from the ACU. This is a request by the ACU for the program to load another digit during dialing. It is accompanied by the setting of DONE to obtain an interrupt. It is cleared by the ACU when the digit is accepted (after DPR is set) and will remain off at least 600 ms before coming up for the next request (Read only).

3 Maintenance (MAINT)

This bit, when set, allows checking of the interface without a connected ACU. It allows FCRQ to be read and switches the ACU response lines—PND, DSS, PWI and ACR to the output of the digit lines for testing purposes.

Bit Digit ACU Line to Ctl Bit

08	NB1	PND	FPND	04
09	NB2	DSS	FDSS	05
10	NB4	PWI	PWO	13
11	NB8	ACR	FACR	14

This bit also forces CRQ (to ACU) off and forces FDLO (Bit 12) on. (Read/Write).

2 Master Enable (MINAB)

Allows the program to disable then re-enable all 4 ACU interrupts easily with one bit. This bit is connected for only one of the four possible lines which mount in one system unit (Read/Write).

1 Digit Present (FDPR)

Control lead to the ACU. This bit must be set by the program after it loads the next digit (in response to a PND request) to inform the ACU to continue dialing. The interface automatically clears this bit when the ACU clears PND to indicate acceptance of the digit (Read/Write).

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0 Call Request (FCRQ) Control lead to ACU. This bit starts the Automatic Calling Sequence (Write only).

SPECIFICATIONS

Control Signals: All control leads are brought into the DN11 from the Bell 801. All leads are EA RS-366 and CCITT compatible. All leads are fail-safe (i.e., they appear off if the 801 loses power).

Bus Load: One DN11 interface represents one unit load to the PDP-11 UNIBUS. Thus, four controls in one System Unit represent four unit loads.

Program Interrupts: Normal interrupts are caused during a call by:

1. Transition of PND to a one. Sets DONE. Digit desired.
2. Transition of DSS to a one. Sets DONE. Data set connected.
3. Transition of ACR to a one. Sets DONE. Busy or wrong number.

Error interrupts are caused during a call by:

1. Transition of PWI to off. Sets DONE. Power to ACU was switched off.

(Note: Appropriate Enable bits must be set.)

Physical Connection: 25-foot cable with RS-232-C compatible 25-pin male connector.

Power Required: 1.4 Amps of + 5V for the first line; 0.4 Amps of + 5V for the second through the fourth lines.

Temperature/Humidity: 0°-40°C with Relative Humidity of 20% to 90%, non-condensing.

Pin Numbers on the 801 Cable

		Output
Pin	Designation	Abbr.
4	Call Request	CRQ
5	Digit Present	DPR
14	Digit Lead	NB1

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15	Digit Lead	NB2
16	Digit Lead	NB4
17	Digit Lead	NB8

Input

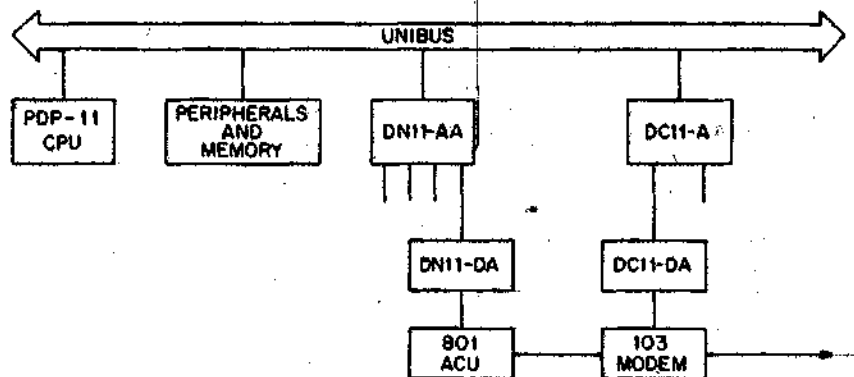
Pin	Designation	Abbr.
5	Present Next Digit	PND
6	Power Indication	PWI
22	Data Line Occupied	DLO
1	Frame GND	FGD
7	Signal GND	SGD

Models

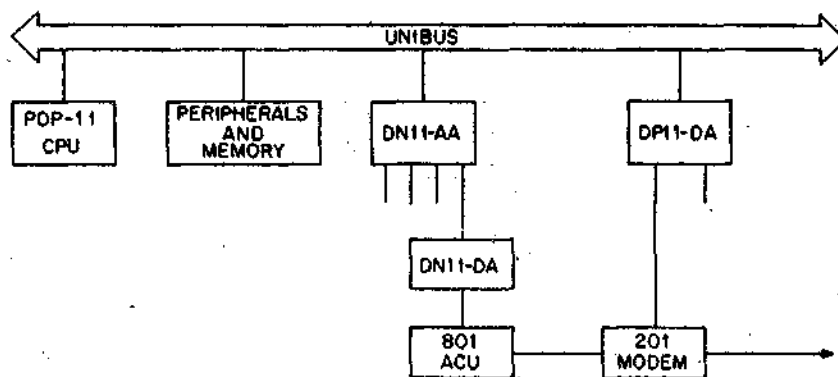
DN11-AA Prewired System Unit for up to four Bell 801 Automatic Calling Unit interfaces. (DN11-DA)

DN11-DA One Line Interface for a Bell 801 Automatic Calling Unit. Includes 25' Cable (Up to four DN11-DA's may be mounted in a DN11-AA).

CONFIGURATIONS

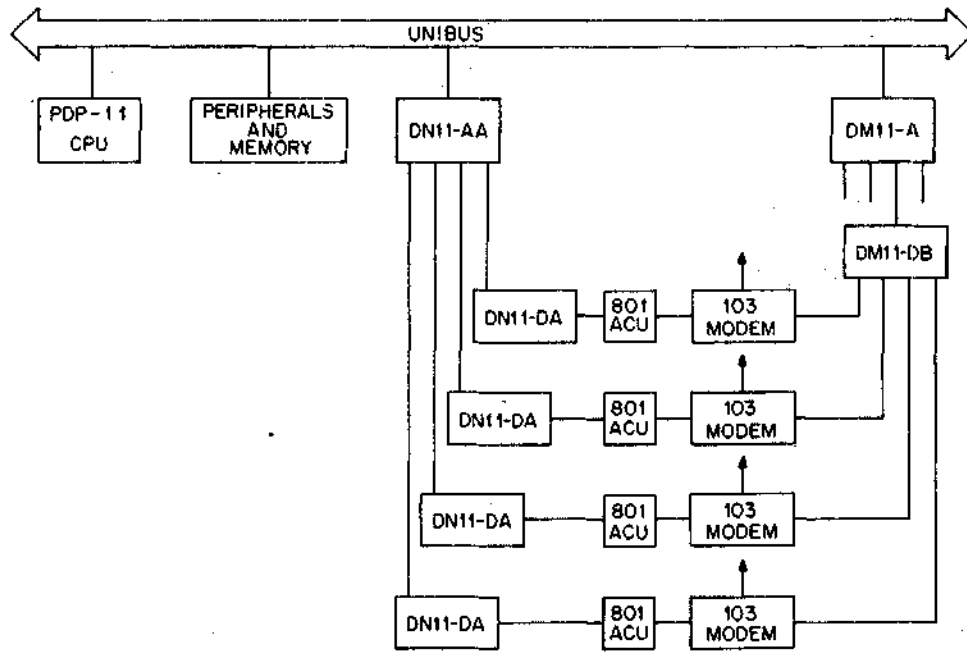


ASYNCHRONOUS SINGLE-LINE INTERFACE



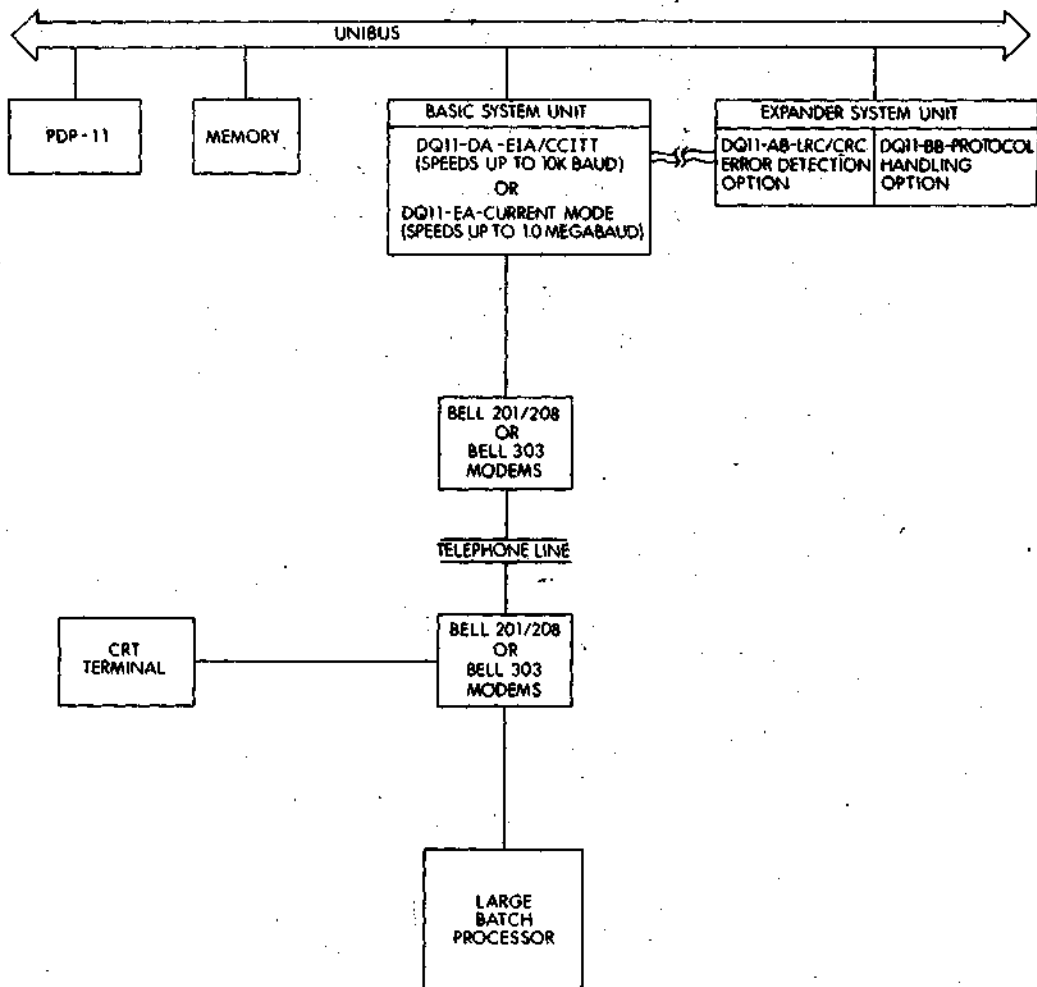
SYNCHRONOUS SINGLE-LINE INTERFACE

DN11



ASYNCHRONOUS MULTIPLE LINE INTERFACE

NPR SYNCHRONOUS LINE INTERFACE, DQ11



FEATURES

Standard

- Non-Processor Request (NPR) data transfers for transmit and receive.
- Transmission speeds up to 1.0 Megabaud when utilizing an appropriate protocol.
- Full- or half-duplex operation.
- Programmable parity (VRC) checking. Parity (odd or even) is switch selectable.
- Data Set control.
- Switch-selectable (one or two) Sync characters to character frame.
- Programmable Sync character.
- Programmable character size; up to sixteen bits per character with double character transfers for characters containing eight bits or less.

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- Double-buffered transmit and receive data registers.
- Double-buffered character count and bus address registers.
- Auto idle, strip Sync, and half-duplex program selectable.
- Diagnostic-controlled self-testing capabilities.
- Three switch-selectable control characters for program interrupts.
- Interfaces to Bell 201, 208, and 303 or equivalent modems.

Optional

- Internal Crystal Clock specified at Baud rate.
- Programmable up to 24-bit polynomial for Longitudinal Redundancy Checking (LRC) or Cyclic Redundancy Checking (CRC).
- Programmable character recognition and hardware sequence control to assist protocol implementation.

INTRODUCTION

The DQ11 is a high-speed, double-buffered communications device designed to interface the PDP-11 Processor to a serial synchronous communications channel. This interface allows the PDP-11 to be used for remote batch and remote concentrator applications. With the DQ11, the PDP-11 can also be used as a front-end synchronous line controller to handle remote and local synchronous terminals. The DQ11 sets a new performance standard for the industry with transmission speeds up to 1.0 Megabaud.

The DQ11 provides parallel-to-serial and serial-to-parallel data conversion, voltage or current level conversion, character recognition, error detection, and Data Set control for half- or full-duplex operation. The interface is compatible with the Bell 201, 208, and 303 modems, or their equivalents.

Transmit and receive data transfers between the PDP-11 UNIBUS and the DQ11 are handled as Non-Processor Requests (NPR). These are direct memory or device access data transfers without processor supervision. As an NPR device, the DQ11 provides extremely fast access to the PDP-11 UNIBUS and can transfer data at exceptionally high rates once it gains control. The PDP-11 Processor state is not affected by these types of transfers, since they occur on a cycle-steal basis.

The DQ11 contains diagnostic-controlled, self-testing facilities to ensure both the quality of the data converters and control logic, and to minimize on-line malfunctions.

The DQ11-DA furnishes level conversion conforming to Electronic Industries Association (EIA) standard RS232C and to CCITT Recommendation V.24. The DQ11-EA is designed for current mode operation, utilizing the Bell System 303, or an equivalent modem. The DQ11-DA is capable of transmitting data at speeds up to 10,000 Baud. Data may be transmitted at speeds up to 1.0 Megabaud with the DQ11-EA.

System Units

The complete DQ11 system consists of two units connected by one-foot-long cables. They are the "Basic System Unit" and the "Error Detection/

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Character Recognition Expander System Unit," the last of which is available as an option.

Complete DQ11 System

Basic System Unit

- Transmitter and Receiver (Double Buffered)
- Character Count and Bus Address Registers (Double Buffered)
- Data Set Control Facilities
- Crystal Clock (Optional)

Connecting
Cables

- Programmable Transmit and Receive 24-Bit Block Check Character (BCC) Registers for LRC or CRC Checking
- Programmable Character Recognition and Hardware Sequence Control to assist Protocol Implementation (Optional)

Error Detection/Character Recognition Expander System Unit (Optional)

Basic Unit

The basic DQ11 device is a single system unit and a basic module set. The basic module set includes all logic required to interact with the PDP-11 UNIBUS. It consists of a double-buffered Character Count Register, a double-buffered Bus Address Register, Transmitter, Receiver, and three switch-selectable characters (receive only) for character recognition. The Character Count and Bus Address Registers are maintained in the hardware, enabling data transfer rates up to 125,000 characters per second.

Error Detection/Character Recognition Expander System Unit

The Error Detection/Character Recognition Expander System Unit provides the user with sophisticated error detection and line protocol handling capabilities.

Error Detection

The Expander Unit includes a module for error detection of up to 24-bit polynomials for Longitudinal Redundancy Checking (LRC) or Cyclic Redundancy Checking (CRC). The error detection module contains both transmit and receive Block Check Character (BCC) Registers. Each register is 24-bits in length and is program selectable for bit length and polynomial. The BCC Register length must be a multiple of the character size and not greater than three (3) characters.

Programmable Character Recognition

Programmable Character Recognition is an optional feature of the Expander Unit. This feature provides:

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- Up to sixteen programmable single and/or double characters for character recognition. Detects single characters up to sixteen bits in length and/or double characters equal to or less than eight bits per character.
- Up to sixteen programmable characters for hardware sequence control. Activates hardware when characters are recognized.
- Jumper-selectable (one or two) PAD (all one's) characters.

With this option installed, the user is able to program a 16-by-16 matrix for detecting single or double characters. The hardware functions upon character detection are also programmable via a 16-by-16 matrix and are defined for both transmit and receive.

The Programmable Character Recognition option is ideally suited for handling line protocols, such as IBM's Binary SYNChronous (BISYNC) protocol.

The Programmable Character Recognition option is suited for assistance in the implementation of character-oriented line protocols such as IBM's Binary Synchronous (BISYNC) protocol. The effective speed of such an implementation is dependent upon the exact protocol implemented and the response characteristics of the total hardware/software system.

This option may be used without error detection to provide interrupts upon detecting any of the sixteen programmable characters, and also to provide the required hardware control. However, the error detection module must be installed. Conversely, the error detection module may function for block transfers when the character recognition option is installed (i.e., either may function independent of the other's presence).

DATA SET CONTROL

Data Set control is a standard feature of the DQ11 system. It includes the following functions:

- Request to Send (jumper inhibits initialize)
- Data Terminal Ready (jumper inhibits initialize)
- Ring Indicator (flag on leading and trailing edge)
- Carrier Detect Indicator (flag on leading and trailing edge)
- Clear to Send Indicator (flag on leading and trailing edge)
- Data Set Ready Indicator
- Data Set Flag Interrupt Enable
- Two optional bits for customer-defined interrupts and/or Data Set control functions.

INTERFACE CHARACTERISTICS

Each of the DQ11 System Units can be mounted in a PDP-11/05NC, PDP-11/10NC, PDP-11/35, PDP-11/40, PDP-11/45 processor box, or in an H960-type expansion box.

The DQ11 Basic Unit and the Error Detection/Character Recognition Expander Unit must be located next to each other and the Basic Unit must be first on the UNIBUS. Cables connect the two system units together.

Each of the two system units presents one load to the PDP-11 UNIBUS.

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DQ11 CONFIGURATIONS

Basic System Unit Only

DEC No.	Capabilities	Type of Interface	Modem Requirements
DQ11-DA	Block Transfers Data Set Control	EIA/CCITT	Bell 201, 208 or Equivalent
DQ11-EA	Block Transfers Data Set Control	Current Mode	Bell 303, or Equivalent

Basic System Unit with Expander System Unit

DQ11-AB (Optional)	LRC or CRC Error Detection	Available with DQ11-DA or DQ11-EA configurations.
DQ11-BB (Optional)	Program Character Recognition (Protocol)	Available with DQ11-AB.

Clock Option

DQ11-KA	Crystal Clock Specified at Baud Rate	Standard frequencies are 2.0 K, 2.4 K, 4.8 K, 9.6 K, and 19.2 K.
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NPR DATA TRANSFER RATES

**Basic System Unit (DQ11-DA or DQ11-EA) or
Basic Unit with Error Detection Expander Unit (DQ11-AB)**
Transfers per second (Half-Duplex/Full-Duplex) up to 125,000 8-bit characters.

**Basic System Unit with Character Recognition
Expander Unit (DQ11-BB)***
Transfers per second (Half-Duplex/Full-Duplex) up to 125,000 characters. The actual speed of the unit is a function of the protocol implemented and the total responsiveness of the hardware/software system.

* NOTE

When the BCC Exclude bit (bit 11 of the Sequence Register) is used, the baud rate must not exceed 250K. Intermediate blocking operations (like the Bisync ITB) may require responses which prove to be rate limiting.

OPERATION

General

The DQ11 is a double-buffered synchronous serial line interface capable of two-way simultaneous communications. It translates between serial data and parallel data. Output characters are transferred in parallel from the PDP-11 UNIBUS into the DQ11 where they are serially shifted

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to the communication line. Input characters from the modem are shifted into the DQ11 and made available to the PDP-11 on an NPR interrupt basis.

Synchronization between the DQ11 and the transmitting device is established by a Sync character code. Once synchronization is achieved, serial data can be transmitted and received continuously (no start or stop bits are required as in asynchronous communications). Both the receiver and transmitter are double buffered. Since the Character Count Register is also double buffered, a full buffer time is available to service character count overflow interrupts. The clocking necessary to serialize the data may be provided by the associated high-speed synchronous modem or by the DQ11's internal Crystal Clock Option (DQ11-KA).

BASIC SYSTEM UNIT

Transmitter Section

The Transmitter Section of the DQ11 performs parallel-to-serial conversion of data supplied to it from the PDP-11 UNIBUS.

After the Initialize pulse, the program must set the Miscellaneous Register (bits 11 through 8) for the desired character length (1 to 16 bits), and a desired word count and current address for transmit and receive. Before any required handshaking with the Data Set, the program may load the Sync Register with the desired Sync character. When the Sync Register is loaded, the Sync character will be used for both Receiver and Transmitter operations.

Any required handshaking to establish connection with the Data Set may be done at this time. Once handshaking is complete, the program can assert the Transmit GO (Tx GO) bit in the Transmit Status Register (Tx Stat) to commence NPR data transfers.

The Transmitter Section of the DQ11 allows the sending of IDLE characters whenever Tx GO is zero. In the non-transparent mode, the IDLE character is the content of the Sync Register. In the transparent text mode (requires DQ11-BB), the IDLE character is Data Link Escape (DLE) followed by the contents of the Sync Register, followed by DLE-SYNC, etc.

Receiver Section

The Receiver Section of the DQ11 performs serial-to-parallel conversion of incoming data arriving from the modem.

After any required handshaking with the Data Set, NPR receiver data transfers and framing will commence when the Receive GO (Rx GO) bit in the Receive Status Register is asserted by the program. The Receiver becomes synchronized with the incoming data when it recognizes one or two consecutive Sync characters.

Once synchronization is established and when the Receive Active (Rx Active) bit in the Receive Status Register is asserted, receiver data transfers commence. Clearing the Rx Active bit while Rx GO is asserted

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forces new Sync characters. Receive Active may be set following synchronization or on the first non-Sync character following synchronization. The standard shipping configuration will be synchronized on two consecutive Sync characters followed by Active on the first non-Sync character.

ERROR DETECTION/CHARACTER RECOGNITION EXPANDER SYSTEM UNIT

Error Detection—LRC and CRC

The Error Detection Expander System Unit (option DQ11-AB) includes a module for detection of up to 24-bit polynomials for Longitudinal Redundancy Checking (LRC) or Cyclic Redundancy Checking (CRC). The error detection module contains both transmit and receive Block Check Character (BCC) Registers. Each register is 24-bits in length and is program-selectable for bit length and polynomial. The BCC Register must be a multiple of the character size and not greater than three (3) characters. Bit 06 of the Miscellaneous Register is used to select the polynomial bits and the Block Check Characters if the desired BCC is greater than sixteen bits.

Refer to the description of the Rx/Tx Polynomial Register (Register 17) for an example of how this register may be programmed for either LRC or CRC error detection.

Protocol Handling

Protocol handling is achieved through the use of two programmable 16-by-16 bit registers housed in the Error Detection/Character Recognition Expander System Unit—the Character Detect Register and the Sequence Control Register (see Figure 1).

The hardware functions upon detection of a character in the Character Detect Register are defined by the Sequence Control Register. Two bits (bits 13 and 12) in the Sequence Control Register enable a program interrupt when a character is detected in the High Byte (HB), Low Byte (LB), or both. Four bits (bits 11 through 8) in the Receive Status Register reflect the binary address of the character detected at character flag time.

PROGRAMMING

General

The address assigned to the DQ11 is the floating address space reserved for PDP-11 peripherals. The DQ11 address assignment starts at 170010 and follows the DH11 in the order of assignments.

Each DQ11 requires four addresses to accommodate the following device registers:

Receive Status Register (Rx STAT)

Address: 76XXX0 (Addressable by word or byte)

Transmit Status Register (Tx STAT)

Address: 76XXX2 (Addressable by word or byte)

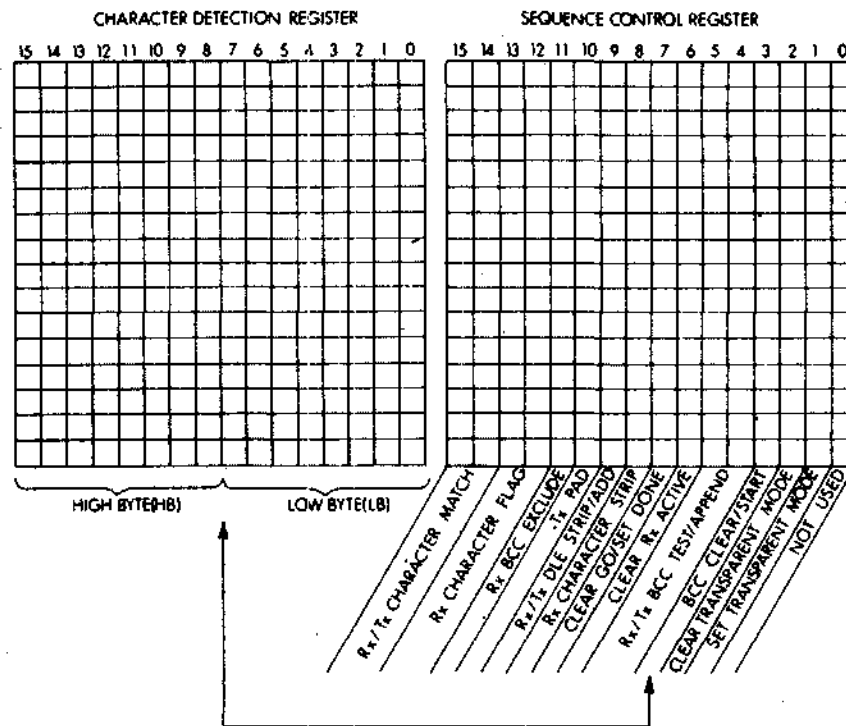


Figure 1

REG/ERR Register

Address: 76XXX4 (Addressable by word or byte)

Secondary Registers (SEC REG)

Address: 76XXX6 (Addressable by word only)

Sixteen secondary registers are provided for read/write operations. These registers are:

- Receive Bus Address (BA)—Primary
- Receive Character Count (CC)—Primary
- Transmit Bus Address (BA)—Primary
- Transmit Character Count (CC)—Primary
- Receive Bus Address (BA)—Secondary
- Receive Character Count (CC)—Secondary
- Transmit Bus Address (BA)—Secondary
- Transmit Character Count (CC)—Secondary
- Character Detect
- Sync
- Miscellaneous
- Transmit Buffer (Tx BUF)
- Sequence (SEQ)
- Receive Block Check Character (Rx BCC)
- Transmit Block Check Character (Tx BCC)
- Receive/Transmit Polynomial

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Interrupts and Vector Assignment

The interrupt service routine should service all flags within the interrupting vector before returning to the mainline program.

All interrupts are under two vectors, where vector "A" is XX0 and vector "B" is XX4. These interrupts are as follows:

Receive Status Register (XX0):
Receiver Done Primary (Rx Done P)
Receiver Done Secondary (Rx Done S)
Character Flag

Transmit Status Register (XX4):
Transmit Done Primary (Tx Done P)
Transmit Done Secondary (Tx Done S)
Error Flag
Data Set Flag

The DQ11 follows the DH11 in the floating vector assignment area. Vector assignment is from 300 to 777.

Register Definitions

The bit assignments within each register are presented in the following information.

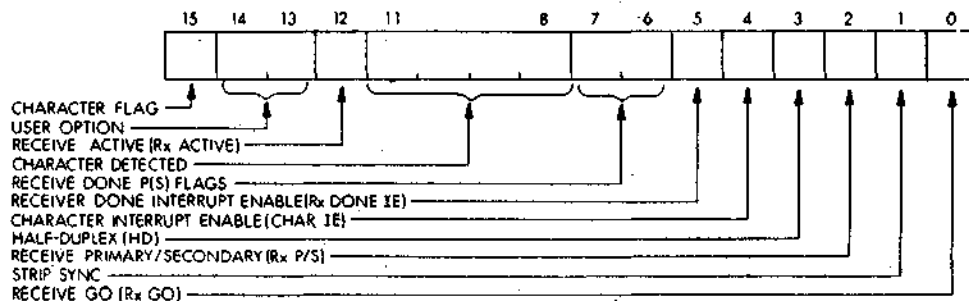
Programming Note:

Upon power up, the program must clear:

- The bus address registers (reg. pointer 0, 2, 4, 6) with the related extended bus address bits.
- The character count registers (reg. pointer 1, 3, 5, 7) with the related enter T/exit T bits.
- Sequence (SEQ) and character detect registers if the DQ11-BB option is selected.

RECEIVE STATUS REGISTER (Rx STAT)

Address: 76XXX0 (Addressable by word or byte)



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Bit	Function	Description
00	RECEIVE GO (Rx Go)	<p>When set, this bit enables receiver data transfers (NPR) and framing. When cleared, receiver data transfers are inhibited from being set by the hardware. Clearing Rx Go will also clear Receive Active.</p> <p>This bit is read/write and is cleared by:</p> <ol style="list-style-type: none">1) Initialize2) Master Clear3) The DQ11-BB Character Recognition option (bit 7 of the Sequence Register).4) If Rx Clock Loss, Rx Latency, or Rx Non-Existent Memory are set.5) If the Character Count (CC) goes to zero (Primary and Secondary registers).
		<p style="text-align: center;">NOTE</p> <p>Refer to bit 02 for Character Count Information.</p>
01	STRIP SYNC	<p>When this bit is set, all Sync characters following Receive Active are stripped from the incoming serial data. In transparent text and in total transparency the Strip Sync function is inhibited.</p> <p>This bit is read/write and is cleared by Initialize and Master Clear.</p>
02	RECEIVE PRIMARY/ SECONDARY (Rx P/S)	<p>Indicates which of the Bus Address (BA) and Character Count (CC) Registers are being used or will be used. A zero indicates that the Primary registers are active; a one indicates that the Secondary registers are active.</p> <p>If a transfer is prematurely ended (i.e., the CC did not increment to zero, as in negating GO, or by a transfer ending flag, or by bit 7 of the Sequence Register), the Rx P/S bit will not flip to the next CC or BA registers.</p>

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Bit	Function	Description
		This bit is read only and is cleared (set to Primary register) by Initialize and Master Clear.
03	HALF-DUPLEX (HD)	<p>The setting of this bit indicates that the DQ11 is in the half-duplex mode. When set, the Receiver is inhibited when Transmit Active is asserted.</p> <p>This bit is read/write and is cleared by Initialize and Master Clear.</p>
04	CHARACTER INTERRUPT ENABLE (CHAR IE)	<p>When set, this bit allows the Character Detected Flag to generate a program interrupt on Vector A.</p> <p>This bit is read/write and is cleared by Initialize and Master Clear.</p>
05	RECEIVER DONE INTERRUPT ENABLE (Rx DONE IE)	<p>If set, this bit allows interrupts to occur on Vector A, if Rx Done "P" or "S" is set.</p> <p>This bit is read/write and is cleared by Initialize and Master Clear.</p>
06 & 07	Rx DONE P(S) FLAGS	<p>These flags are set when their respective character counts (P or S) overflow. These bits are also set by the DQ11-BB Character Recognition option (bit 7 of the Sequence Register). Rx Done "P" is bit 7 and Rx Done "S" is bit 6.</p> <p>These bits are read/write and are cleared by Initialize and Master Clear.</p>
NOTE		
If Rx Done is set by the Sequence Register, the Rx P/S (bit 2) will not change state.		
08 thru 11	CHARACTER DETECTED (CHAR DET)	<p>These four bits are used to latch character status which caused a character flag. They represent the switch-selected character flags in the DQ11 Basic Unit if the Character Recognition option is not implemented. If the Character Recognition option is implemented, these four</p>

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Bit	Function	Description
		bits reflect the binary address of the character detected at Character Flag time.
		Character recognition is inhibited if transparency is forced (total transparency mode). Reference bit 14 of the REG/ERR Register for this function.
		The state of these four bits is guaranteed for one character time; i.e., $\frac{\text{Bits/Character}}{\text{Baud Rate}} = \text{Seconds}$
		If a protocol being implemented requires that the software must respond to a character-detect interrupt, the effective speed of the DQ11 will be limited by the ability of the system to respond. For example, if a protocol requires that action be taken when a record Separator is detected, the ability of the Software to respond before the state of the character-defected bits are changed is rate-limiting.
		BASIC UNIT ONLY When applied to the DQ11 Basic System Unit only, bits 8, 9, and 10 represent switch-selectable characters 0, 1, and 2, respectively.
		Bit 11 is connected to the Sync Detection Logic; with switch selection, detection of a Sync character will cause a Character Detected flag.
		CHARACTER RECOGNITION AND HARDWARE SEQUENCE CONTROL With the DQ11-BB Character Recognition option installed, bits 8, 9, 10, and 11 will contain the binary address (0-17) of the character detected (latched at CHARACTER DETECT Flag time). With this option installed, the character for recognition may be written,

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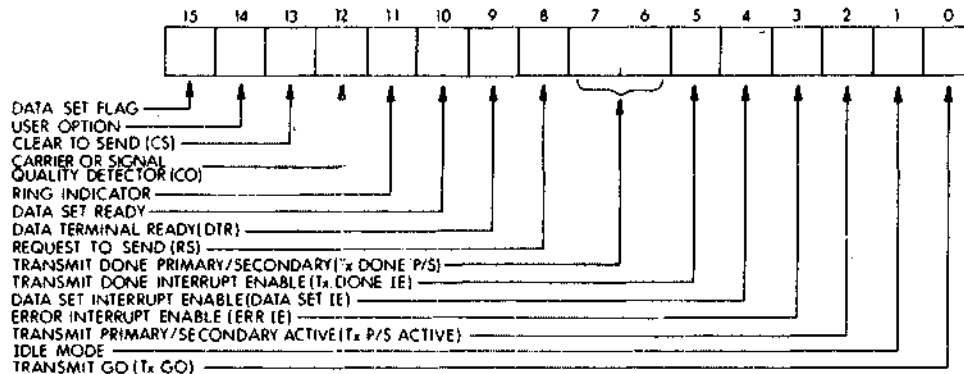
Bit	Function	Description
		<p>if not Transmit Active and not Receive Active. Reading and writing are accomplished by:</p> <ol style="list-style-type: none">1) Setting the Secondary Register Pointer (bits 11 through 08 of the REG/ERR Register) to CHARACTER DETECT (Octal 10).2) Writing the character address into Rx CHARACTER DETECT bits 11 through 8.3) Reading and/or writing the character with select 6. Select 6 (XXXXX6) is used to access the sixteen secondary registers. Reference description of bits 08 through 11 of the REG/ERR Register for additional information.4) Repeating steps 2 and 3 until all required characters are accessed. <p>These bits are read/write, if Receive or Transmit are not Active and the DQ11-BB Character Recognition option is installed. Bits 8 through 11 are cleared by Initialize and Master Clear.</p>
12	RECEIVE ACTIVE (Rx ACTIVE)	<p>The setting of this bit indicates that the Receiver is in the data transfer mode. The hardware becomes synchronized with the incoming data when it recognizes one or two consecutive Sync characters. Additionally, active is set when synchronized or at the first non-Sync character after becoming synchronized.</p> <p>Clearing Active forces re-synchronization if Rx GO is asserted.</p> <p>The shipping configuration will be synchronized on two consecutive synch characters followed by Active on the first non-sync character.</p> <p>This bit is read/write and is cleared by Initialize, Master Clear, bit 6 of the Sequence Register, and when Rx GO is cleared.</p>

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Bit	Function	Description
13 & 14	USER OPTION	<p>These bits are available as part of the Data Set control feature of the DQ11. They may be used for generating additional flags or for providing additional modem control.</p> <p>These bits are read/write and are cleared by Initialize and Master Clear.</p>
15	CHARACTER FLAG	<p>The Character Flag bit is set when a character is detected. (Reference description of bits 8 through 11.)</p> <p>The bit will cause an interrupt if the Character Interrupt Enable bit (bit 4) is set.</p> <p>The CHARACTER FLAG is read/write and is cleared by Initialize and Master Clear.</p>

TRANSMIT STATUS REGISTER (Tx STAT)

Address: 76XXX2 (Addressable by word or byte)



Bit	Function	Description
00	TRANSMIT GO (Tx GO)	When set, this bit enables transmit data transfers (NPR).

NOTE:

Reference bit 02 for Character Count (CC) information.

This bit is read/write and is cleared by:

- 1) Initialize
- 2) Master Clear

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Bit	Function	Description
		3) The DQ11-BB Character Recognition option (bit 7 of the Sequence Register). 4) By the setting of the Tx Non-Existent Memory, Tx Latency, or Tx Clock Loss flags. 5) If the Character Count goes to zero (Primary and Secondary registers).
01	IDLE MODE	If set, this bit allows the sending of IDLE* characters whenever Tx GO is zero. This bit is read/write and is cleared by Initialize and Master Clear.
02	TRANSMIT PRIMARY/ SECONDARY ACTIVE (Tx P/S ACTIVE)	Indicates which of the Character Count and Bus Address Registers will be or are being used. A zero indicates that the Primary "P" Register is active; a one indicates that the Secondary "S" Register is active. When Character Count Register overflow occurs, the Character Count Register will switch (i.e., P→S or S→P). If the transfers are prematurely ended, as when clearing Tx GO, the Character Count Register will not switch and will be used again when Tx GO is re-asserted. This bit is read only and is cleared (set to "P" register) by Initialize and Master Clear.
03	ERROR INTERRUPT ENABLE (ERR IE)	When set, this bit enables interrupts on Vector "B" from the error flag. The error flag will be asserted when any of the error indicators are ON. They are as follows: VRC error BCC error Non-Existent Memory Latency Clock Loss

*Non-transparent mode: The IDLE character is the content of the Sync Register.
*Transparent text mode: The IDLE character is Data Link Escape (DLE) followed by the contents of the Sync Register—followed by DLE-SYNC, etc. (Requires the DQ11-BB option.)

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Bit	Function	Description
		This bit is read/write and is cleared by Initialize and Master Clear.
04	DATA SET INTERRUPT ENABLE (DATA SET IE)	When set, this bit enables interrupts (Vector B) from the Data Set flag. The Data Set flag will be set from either the leading or trailing edge transitions of Carrier Detect (CO), Clear to Send (CS), or Ring.
		This bit is read/write and is cleared by Initialize and Master Clear.
05	TRANSMIT DONE INTERRUPT ENABLE (Tx DONE IE)	If set, this bit allows interrupts to occur on Vector B if the Tx Done bit is set.
		This bit is read/write and is cleared by Initialize and Master Clear.
06 & 07	TRANSMIT DONE & PRIMARY SECONDARY (Tx DONE P/S)	These bits are set when their respective character counts (P or S) overflow. These bits are also set by the DQ11-BB Character Recognition option—bit 7 of the Sequence Register.

NOTE:

If Tx DONE is set by the Sequence Register, the Tx P/S (bit 2) will not change state.

These bits are read/write and are cleared by Initialize and Master Clear.

NOTE

Bits 08 through 15 are Data Set Control functions (Request to Send, Clear to Send, etc.) The DQ11 hardware will transmit and/or receive data independent of these control functions.

The Data Set control module has a strap which, when removed, inhibits Initialize from clearing Data Terminal Ready (DTR) and Request to Send (RS). The user should be aware of required modem and/or hardware delays before Request to Send (RS) can be negated. For instance, Bell 201A modems require a one-bit time delay following the last bit of transmission before negating RS. Due to double-buffered hardware, Tx DONE indicates that data transfers have been completed but not all data has been transmitted. All data has been transmitted only when Tx Active is negated (one-to-four character times after Tx DONE).

The function of each of the following Data Set control bits is given in the format of NAME(EIA/CCITT/PIN).

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Bit	Function	Description
08	REQUEST TO SEND (CA/105/4)	<p>Request to Send (RS) is a transmit lead to the data communications equipment (Data Set). This control function is used to condition the local data communications equipment for data transmission and, on a half-duplex channel, to control the direction of data transmission.</p> <p>A program state change directed to RS will be presented to the Data Set on the next positive transition of the transmit clock.</p> <p>When the RS bit is set, an ON signal is transmitted. When cleared, an OFF signal is transmitted.</p> <p>This bit is read/write and is cleared by Initialize and Master Clear (if the jumper is in).</p>
09	DATA TERMINAL READY (CD/108.2/20)	<p>The Data Terminal Ready (DTR) bit controls switching of the data communications equipment to the communications channel. Auto dial and manual call origination; maintains the established call. Auto Answer; allows "handshaking" in response to a RING signal.</p> <p>This bit is read/write and is cleared by Master Clear and Initialize (if the jumper is in).</p>
10	DATA SET READY (CC/107/6)	<p>The Data Set Ready (also referred to as "Modem Ready" or "Interlock") bit reflects the current state of the Data Set Ready lead. The Data Set Ready lead indicates that the modem is powered up and is not in the test, talk, or dial mode.</p> <p>This bit is read only; it is not affected by Initialize or Master Clear.</p>
11	RING (CE/125/22)	<p>This bit reflects the state of the data set ring lead. The trailing and leading edge of the ring lead will cause the data set flag to be set, and an interrupt will follow if the Data Set Interrupt Enable (IE) bit is set.</p>

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Bit	Function	Description
12	CARRIER OR SIGNAL QUALITY DETECTOR (CF/109/8)	<p>This bit is read only; it is not affected by Initialize or Master Clear.</p> <p>This bit reflects the current state of the Modem Carrier (CO) Control lead. An OFF indicates that no signal is being received or that the received signal is unsuitable for demodulation.</p> <p>The leading and the trailing edge of CO will cause the Data Set flag to be set, and an interrupt will follow if the Data Set IE bit is set.</p>
13	CLEAR TO SEND (CB/106/5)	<p>This bit is read only; it is not affected by Initialize or Master Clear.</p> <p>This bit reflects the current state of the Modem Clear to Send (CS) lead. An ON state indicates that the modem is ready to transmit data. The state of this lead is a direct result of the Request to Send lead. Also, CS is delayed from RS as a function of the type of modem and the type of lines used (four wire or two wire).</p> <p>The leading and the trailing edge of CS will cause the Data Set flag to be set, and an interrupt will follow if the Data Set IE bit is set.</p>
14	USER OPTION	<p>This bit is read only; it is not directly affected by Initialize or Master Clear (indirectly via RS).</p> <p>This bit is provided at the back panel for user connection of a non-standard status bit and/or program interrupt via the Data Set Flag. The back panel connection is TTL only and represents two standard TTL loads.</p>
15	DATA SET FLAG	<p>This bit is read/write and is cleared by Initialize and Master Clear.</p> <p>If this bit is set and Data Set IE is asserted, an interrupt will occur on Vector "B". The Data Set flag is asserted by the leading or trailing transitions of Ring, CO, and CS.</p> <p>This bit is read/write and is cleared by Initialize and Master Clear.</p>

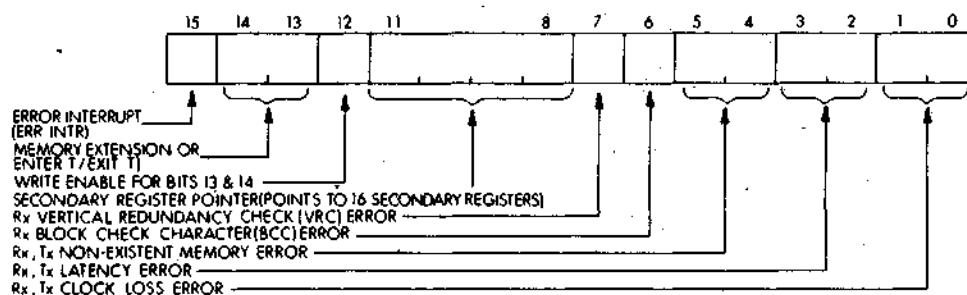
DQ11

REG/ERR REGISTER

Address: 76XXX4 (Addressable by word or byte)

NOTE

The error bits described below generate an interrupt request on Vector "B" if the Error Interrupt Enable (ERR IE) bit (bit 03 of the Transmit Status Register) is asserted.



Bit	Function	Description
00 & 01	Rx, Tx CLOCK & LOSS ERROR	These bits (Rx or Tx) are set if the clock stops with Active set (Rx or Tx). The clock loss flag will be set if GO is asserted without the clock or if the clock drops for more than 0.02 seconds while GO is true. Tx is bit 00, and Rx is bit 01. These bits are read/write and are cleared by Initialize and Master Clear.
02 & 03	Rx, Tx LATENCY & ERROR	These bits (Rx or Tx) are set if an NPR request is not serviced in less than one character time. The setting of this bit will clear the respective GO flip-flop. This error condition implies that the UNI-BUS is overloaded, is malfunctioning, or the Baud rate exceeds specifications. Tx is bit 02, and Rx is bit 03. These bits are read/write and are cleared by Initialize and Master Clear.
04 & 05	Rx, Tx NON- & EXISTENT MEMORY & ERROR	These bits (Rx or Tx) are set if the DQ11, during an NPR cycle, addresses itself to a non-existent core memory location. This condition implies a program or hardware

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Bit	Function	Description				
		<p>error and should be dealt with accordingly. Tx is bit 04, and Rx is bit 05.</p> <p>The setting of these bits will clear the respective GO flip-flop.</p> <p>These bits are read/write and are cleared by Initialize and Master Clear.</p>				
06	Rx BLOCK CHECK CHARACTER (BCC) ERROR	<p>This bit is asserted if the BCC generated by the received message and the received BCC do not compare.</p> <p>When this bit is set, the Rx BCC is cleared (hardware function) and ready for the next message. Additionally, this does not affect Rx GO.</p> <p>It is recommended that a message re-transmit be initiated when this form of error is detected.</p> <p>These bits are read/write and are cleared by Initialize and Master Clear.</p>				
07	Rx VERTICAL REDUNDANCY CHECK (VRC) ERROR	<p>This bit is set if the last received character had incorrect character parity.</p> <p>VRC is jumper selectable for even or odd parity; parity on/off is program selectable by bit 15 of the Miscellaneous Register.</p> <p>If VRC is used with the DQ11-BB Character Recognition option, the control characters transferred to the Transmit Buffer must have correct VRC.</p> <p>This bit is read/write and is cleared by Initialize and Master Clear.</p>				
08 thru 11	SECONDARY REGISTER POINTER	<p>These bits point to sixteen secondary registers for read/write operations. The selected register is accessed using select 6 (XXXXX6) with word transfers only. The following registers may be selected:</p> <p>Bits (11-8) Octal # Register (Selected Via 76XXX6)</p> <table border="1"> <tbody> <tr> <td>0</td> <td>Receive Bus Address (Rx BA)—Primary</td> </tr> <tr> <td>1</td> <td>Receive Character Count (Rx CC)—Primary</td> </tr> </tbody> </table>	0	Receive Bus Address (Rx BA)—Primary	1	Receive Character Count (Rx CC)—Primary
0	Receive Bus Address (Rx BA)—Primary					
1	Receive Character Count (Rx CC)—Primary					

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Bit	Function	Description
2		Transmit Bus Address (Tx BA)—Primary
3		Transmit Character Count (Tx CC)—Primary
4		Receive Bus Address (Rx BA)—Secondary
5		Receive Character Count (Rx CC)—Secondary
6		Transmit Bus Address (Tx BA)—Secondary
7		Transmit Character Count (Tx CC)—Secondary
10**		Character Detect
11		Sync
12		Miscellaneous
13		Transmit Buffer (Tx BUF)
14**		Sequence
15*		Receive Block Check Character (Rx BCC)
16*		Transmit Block Check Character (Tx BCC)
17*		Receive/Transmit (Rx/Tx) Polynomial
		*Registers at these addresses are always zero unless the DQ11-AB LRC or CRC Error Detection option is installed.
		**Registers at these addresses are always zero unless the DQ11-BB Character Recognition option is installed.
		These bits are read/write and are cleared by Initialize and Master Clear.
12	WRITE ENABLE FOR BITS 14 & 13 (14, 13 WRITE EN)	When set, this bit allows the data written into bits 14 and 13 to be transferred to the scratch pad memories (Bus Address and Character Count) the next time select 6 is used. This bit is also self-clearing when the write-to-scratch-pad memory occurs.
		This bit is read/write and is cleared by Initialize and Master Clear.
13 & 14	MEMORY EXTENSION OR ENTER T/EXIT T	The Bus Address (BA) and Character Count (CC) registers are 18-bit registers. Bits 14 and 13 with bit 12 provide a means of reading and/or writing the BA

Bit	Function	Description
		<p>and CC bits (bits 17, 16 are bits 14 and 13, respectively). In addition, the register pointer bits (bits 11 through 8) determine what CC or BA is to be accessed.</p> <p>MEMORY EXTENSION: Bits 14 and 13 are address lines A16 and A17, respectively. These two bits are the read/write ports for transmit and receive. The proper port is selected (Rx or Tx) when the register bits are addressed to the desired Bus Address Register. See description of bits 10 through 8.</p> <p>ENTER T (14): Enter transparency forces transparency (block transfers) and inhibits all character recognition. This function is used if a message to be transmitted (or received) is completely transparent to all data and control characters. Additionally, this function starts the BCC generation and requires the DQ11-AB LRC/CRC Error Detection option.</p> <p>EXIT T (13): If set, this exit transparency bit allows exit from the transparent mode and enables character recognition.</p> <p>This function is used as a companion to ENTER T or used in protocol hardware control (as in BISYNC or ASCII standards).</p> <p>When used as a companion to ENTER T, a jumper is provided to start the BCC generator which tests appends one, two, or three BCC characters. When used with protocol hardware control, EXIT T starts transmission of a DLE (Data Link EEscape) and enables the character recognition circuits to recognize ETX (End of Text), ITB (Intermediate Text Block), and other-control characters.</p> <p>The ENTER T and EXIT T bits execute their respective functions when the character counts are tested for non-zero by the hardware. This occurs when the current Character Count Register transitions to zero or at the first transfer following the assertion of GO.</p>

Bit	Function	Description
		Bits 14 and 13 Read always represent the contents of the respective addressed scratch pad memories. (Select 6 must be used to transfer a write to bits 14 and 13 into the scratch pad memories.)
15	ERROR INTERRUPT (ERR INTR)	This error flag is set if any of the error bits are asserted. The error bits are for VRC, BCC, Rx/Tx Non-Existent Memory, Rx/Tx Latency, and Rx/Tx Clock Loss. This bit is read only and presents a zero when all the error bits are zero and when Master Clear or Initialize has been issued.

SECONDARY REGISTERS (SEC REG)

Address: 76XXX6 (Addressable by word only)

The Secondary Registers listed below are addressed by setting bits 8 through 11 of the REG/ERR Register (Select 4) to the appropriate value.

Register Octal Address	Function
0	Receive Bus Address (Rx BA)—Primary
1	Receive Character Count (Rx CC)—Primary
2	Transmit Bus Address (Tx BA)—Primary
3	Transmit Character Count (Tx CC)—Primary
4	Receive Bus Address (Rx BA)—Secondary
5	Receive Character Count (Rx CC)—Secondary
6	Transmit Bus Address (Tx BA)—Secondary
7	Transmit Character Count (Tx CC)—Secondary
10	Character Detect
11	Sync
12	Miscellaneous
13	Transmit Buffer (Tx BUF)
14	Sequence
15	Receive Block Check Character (Rx BCC)
16	Transmit Block Check Character (Tx BCC)
17	Receive/Transmit (Rx/Tx) Polynomial

A functional description of each of the above secondary registers is presented in the remainder of this section.

CHARACTER COUNT (CC)—REGISTERS 1, 3, 5, and 7

BUS ADDRESS (BA)—REGISTERS 0, 2, 4, and 6

The BA register for transmit and receive must be started on even boundaries. However, the BA (and CC) registers may end on either odd or even boundaries.

DQ11

The CC and BA registers for transmit and receive are double buffered, thus reducing peak load response to CC overflow.

CC and BA are 16-bit registers. The BA Register is extended to 18 bits by the Memory-Extension bits; the CC Register is extended to 18 bits by the ENTER T and EXIT T bits in the REG/ERR Register.

These bits are read/write and are not cleared by Initialize or Master Clear. They must be cleared by a program initialization procedure.

When an Initialize or Master Clear is issued, the Primary/Secondary (P/S) flip-flops select the primary CC and BA registers. When CC overflow occurs, the Secondary Register (Tx or Rx—whichever overflowed) will be selected. Data transfers will cease, and GO will be cleared when the flip to the next Character Count (CC) register occurs and is found to be zero. The next "GO" will start with the last selected CC (the one that terminated the last "GO").

NOTE

The hardware does not require or expect the Primary/Secondary (P/S) registers for transmit and receive to be in phase except following Master Clear and Initialize.

CHARACTER DETECTION (CHAR DET)—REGISTER 10

The programmable Character Recognition Option can be Read or Write for up to sixteen single or double characters (16 bits maximum). The hardware reaction upon detection of the characters is also programmable.

Bits 15-8

Used for single character recognition or for the second character in double character recognition. Characters should be right-justified and unused bits must be zero.

Bits 7-0

Used for the first character of double-character recognition (i.e., DLE). Characters should be right-justified and unused bits must be zero.

Bits 15-0

Used for single characters equal to or greater than nine (9) bits per character. Characters should be right-justified and unused bits must be zero.

NOTE

When the DQ11-BB Character Recognition option is implemented, the three standard jumper-selectable characters are inhibited.

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Bits 15 - 8		Bits 7 - 10	
0	STX		DLE
1	ITB		
2	ETB		
3	ETX		
4	EOT		DLE
5	ENQ		DLE
6*	DLE		DLE
7	SOH		
8	NAK		
9	← ACK0 →	← →	
10	← ACK1 →	← →	
11	← RVI →	← →	
12	← WACK →	← →	
13	NOT USED (SEQ = 0)		
14	NOT USED (SEQ = 0)		
15	NOT USED (SEQ = 0)		

*Required for SEQ 9.

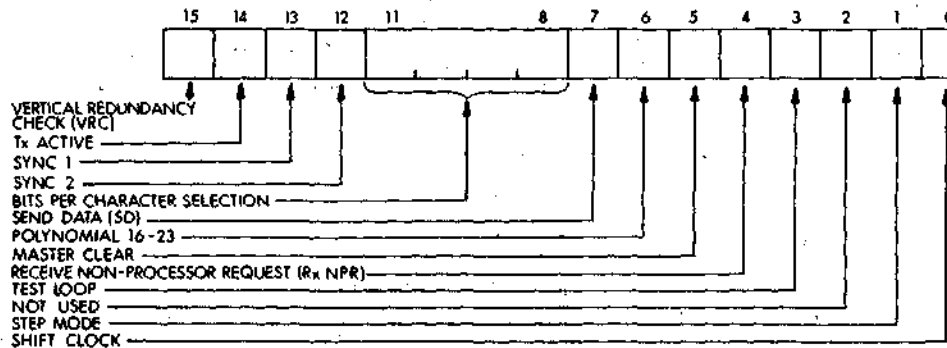
These bits are read/write and are NOT cleared by Initialize and Master Clear.

SYNC REGISTER—REGISTER 11

The Sync Register is programmable for up to sixteen bits. Unused bits must be set to zero. If characters less than or equal to eight bits are used, then the odd and even bytes should contain the same Sync character. The Least Significant Bit (LSB) is right-justified, as are the data bits.

These bits are Read Write and are cleared by Master Clear and Initialize.

MISCELLANEOUS REGISTER—REGISTER 12



Bit	Function	Description
00	SHIFT CLOCK	The Shift Clock is a maintenance function. The transmitter shifts when this bit is set

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Bit	Function	Description
		to ONE (transition to), and the receiver strobes data when this bit is set to zero (transition to).
		This bit is read/write and is cleared by Initialize and Master Clear.
01	STEP MODE	<p>This bit selects the clocking source for the test loop. See description of bit 3.</p> <p>If this bit is zero, the auto clock source is selected. The source for the auto clock is approximately 14KC RC clock if loop mode is also selected. If loop mode is not selected, the source clock will be the serial clock transmit and serial clock receiver leads.</p> <p>If this bit is a one, the Shift Clock (bit 00) will be the clock source.</p> <p>This bit is Read/Write and is cleared by Initialize and Master Clear.</p>
02	NOT USED	
03	TEST LOOP	<p>If set, this bit causes the transmitter to loop back to the receiver.</p> <p>This bit is Read/Write and is cleared by Initialize and Master Clear.</p>
04	RECEIVE NON-PROCESSOR REQUEST (Rx NPR)	<p>The Rx NPR bit is a maintenance function. It is intended for use when Receiver Active is zero.</p> <p>A one written into this bit forces an Rx NPR. The data transferred to core will be the contents of the receiving shift register (not the buffer) and the Bus Address (BA) and Character Count (CC) will be updated.</p> <p>This bit is a write ones only and always reads as a zero.</p>
05	MASTER CLEAR	<p>The Master Clear function resets all active functions and flags in the DQ11. The CC, BA, MEM EXT, ENTER T, EXIT T, CHAR DET, and the SEQ are not cleared by Master Clear.</p> <p>This bit is a write ones only and always reads as a zero.</p>

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Bit	Function	Description
06	POLYNOMIAL 16-23	<p>If set to zero, register pointer 17(8) will select polynomial bits 0 through 15. In addition, pointers 15 and 16 will select Block Check Characters (BCC) 0 through 15.</p> <p>If this bit is set to ONE, the register pointer 17(8) will select polynomial bits 16 through 23 while pointers 15 and 16 will select Block Check Characters 16 through 23.</p> <p>This bit is Read/Write and is cleared by Master Clear and Initialize.</p>
07	SEND DATA (SD)	<p>This bit always monitors the transmitted data if the test loop is selected. In addition, if the Transmit Active bit is a zero, this bit is Read/Write and can be used to directly test the receiver as a maintenance function. A zero equals MARK and a ONE equals SPACE.</p> <p>This bit is Read/Conditional Write and is cleared by Initialize and Master Clear.</p>
08 thru 11	BITS PER CHARACTER SELECTION	<p>Bits per character selection is made via bits 11, 10, 9, and 8 as follows:</p>

11	10	9	8	Bits per character
0	0	0	0	16
0	0	0	1	15
0	0	1	0	14
0	0	1	1	13
0	1	0	0	12
0	1	0	1	11
0	1	1	0	10
0	1	1	1	9
1	0	0	0	8
1	0	0	1	7
1	0	1	0	6
1	0	1	1	5
1	1	0	0	4
1	1	0	1	3
1	1	1	0	2
1	1	1	1	1

These bits are Read/Write and are cleared by Initialize and Master Clear.

Bit	Function	Description
12	SYNC 2	<p>SYNC 2 will be set if the receiver is synchronized (framed).</p> <p>This bit is read only and is cleared by Initialize, Master Clear, and by clearing Active.</p>
13	SYNC 1	<p>SYNC 1 will be set if the receiver has received one SYNC character.</p> <p>A jumper is provided to enable SYNC 1 to direct set SYNC 2, causing framing to be completed. If the jumper is not installed, SYNC 1 will condition SYNC 2 to be set if the next received character is another SYNC. If the next received character is not a SYNC, then SYNC 1 will be cleared, and a bit-by-bit search will continue for another SYNC character.</p> <p>This bit is read only and is cleared by Initialize, Master Clear, and by clearing Active.</p>
14	Tx ACTIVE	<p>When set, this bit indicates that the transmitter is in the process of transmitting a character; it will remain set until all characters and/or bits have been transmitted.</p> <p>This bit is cleared by Initialize, Master Clear, and lack of data to transmit.</p>
15	VERTICAL REDUNDANCY CHECK (VRC)	<p>When set, the VRC bit selects parity to be generated (transmit) and checked (receive) in the most significant bit position of the selected character. VRC odd/even is switch-selectable. When VRC is used, PAD or FILL characters must have correct VRC or an error will be flagged.</p> <p>This bit is Read/Write and is cleared by Master Clear and Initialize.</p>

TRANSMIT BUFFER (Tx BUF)—REGISTER 13

The Transmit Buffer is a 16-bit, read-only maintenance register which monitors the parallel input to the Transmit Shift Register (i.e., the Transmit Buffer).

These bits are cleared by Initialize and Master Clear.

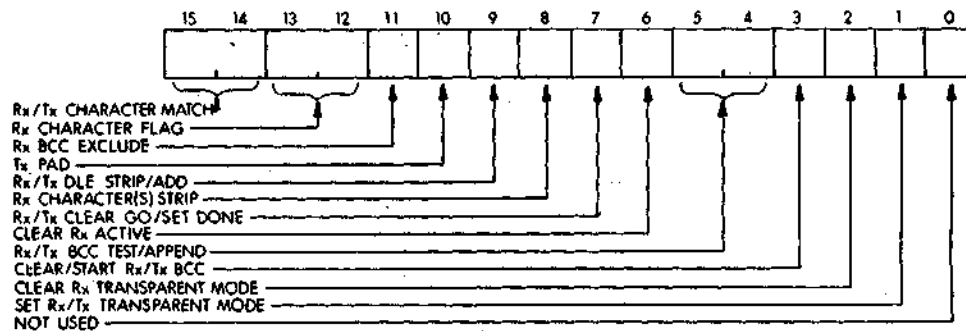
SEQUENCE (SEQ) REGISTER—REGISTER 14

The Sequence Register is a programmable 16-by-16 bit register which defines hardware functions when a control character is recognized. The character recognized and the programmed sequence for that character must be at the same character detected address.

NOTE:

If a character is detected and no bits are set in the respective Sequence Register, no hardware functions will take place and the receive (transmit) characters will be handled in the normal way.

All bits are Read/Write and are not cleared by Master Clear or Initialize. All Sequence Register bits must be initialized by the program following power up and preceding the transmission and/or receiving of data.



Bit	Function	Description
00	NOT USED	
01	SET Rx/Tx TRANSPARENT MODE	Requires double byte match, bit 14, to function; i.e., Low Byte and High Byte (LB and HB). RECEIVE: Enters receive transparent mode and inhibits strip sync. Strip idle in transparent mode will require the use of bit 9 of the Sequence Register. Character recognition is also disabled except when preceded by DLE which is stripped by bit 9. TRANSMIT: Enters transmit transparent mode which modifies idle from sync's to alternating sync and DLE characters. Using bit 9 will also allow DLE stuffing. All SEQ control is inhibited except bit 9. Reference REG/ERR Register for transmit exit transparency (EXIT T).

Bit	Function	Description										
02	CLEAR Rx TRANSPARENT MODE	<p>Requires single byte match, bit 15 to func- (HB) and must be preceded by a DLE strip (bit 09 of the Sequence Register). This is a pseudo double character match.</p> <p>This bit clears the transparent mode and allows auto strip sync.</p> <p>Reference REG/ERR Register, bit 13, for clearing Tx Transparent mode (EXIT T).</p>										
03	CLEAR/START Rx/Tx BCC	<p>Clears and starts the BCC generator with the next character (following the control character) if it is the first occurrence following Initialize, Master Clear, or GO (OFF to ON). In all other cases, the BCC will start with, and include, the current control character unless the "BCC exclude" bit (bit 11) is used.</p> <p>The first BCC start up control character (first STX) will be excluded from the BCC. However, the next BCC start-up control character within the same message will be included (second STX) in the BCC unless the BCC exclude bit is used.</p>										
04 & 05	Rx/Tx BCC TEST/ APPEND	<p>These bits give the numbers of BCC characters that will be tested (receive) or appended (transmit) following the control character (ETX). The bit positions are:</p> <table border="1" data-bbox="776 1381 1372 1564"> <thead> <tr> <th>5,4</th> <th>BCC CHARACTER</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>None</td> </tr> <tr> <td>10</td> <td>Three</td> </tr> <tr> <td>01</td> <td>Two</td> </tr> <tr> <td>11</td> <td>One</td> </tr> </tbody> </table> <p>Each BCC character is the same length as "bits per character." Also, the receiver BCC characters are not transferred to core and consequently do not affect the CC. Additionally, Tx/Rx interrupts are suspended while the respective BCC is being processed.</p>	5,4	BCC CHARACTER	00	None	10	Three	01	Two	11	One
5,4	BCC CHARACTER											
00	None											
10	Three											
01	Two											
11	One											
06	CLEAR Rx ACTIVE	Clears receive and is useful for forcing re-synchronization.										
07	Rx/Tx CLEAR GO/SET DONE	Clears the GO bit and sets DONE for the current CC register in use (P or S) after										

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Bit	Function	Description
		the control characters are transferred to core. The CC does not flip to the next register when this bit is used.
08	Rx CHARACTER(S) STRIP	<p>This bit strips characters from transfers to core but not from the BCC Register (see description of bit 11).</p> <p>If bit 15 is a one, a character less than or equal to eight bits which compares with the character register (right justified), will be stripped. If bit 14 is a one, a double character or a character greater than eight bits will be stripped. When both bits are set, bit 14 dominates hardware control.</p>
09	Rx/Tx DLE STRIP/ADD	<p>Receive: Single character match (bit 15) strips the first character as with DLE DLE when in the transparent mode. The next character following DLE is tested for "Exit Transparency" and SYNC character. If the next character does not exit transparency, all other SEQ functions will be ignored. If the next character was a SYNC, it will be stripped as was the DLE.</p> <p>Transmit adds another character which is used for DLE, DLE in the transparent mode.</p>
		<p style="text-align: center;">NOTE</p> <p>The Character Detect memory must contain DLE's in both bytes at the address where SEQ 9 is used.</p> <p>DLE stripped (Rx) or added (Tx) is always deleted from the error detection logic.</p>
10	Tx PAD	<p>Transmit only: Inserts pad character(s) following the last characters to be transmitted, as in EOT, PAD, or ETX, BCC, PAD.</p> <p>A jumper is available for selecting one or two pad characters.</p> <p>The DQ11 requires one NULL or PAD character following the last character to be received. This is due to the BCC registers and double-character transfers.</p> <p>The shipping configuration will always be set for one pad.</p>

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Bit	Function	Description
11	BCC EXCLUDE	This bit allows any single character (bit 15 if less than or equal to eight bits and bit 14 if greater than eight bits) to be excluded from the BCC accumulation when in the non-transparent mode. When this bit is used, the baud rate must not exceed 250K.
12 & 13	Rx CHARACTER & FLAG	<p>These bits will cause the character flag to be set and will also latch the address of the control character into four CHARACTER DETECT bits (bits 11 through 8) in the Receive Status Register. This address will remain in the CHARACTER DETECT latches for a minimum of one character time. The address changes when the next character is detected.</p> <p>Bit 13 will cause a character flag if a single (less than or equal to 8 bits) character is detected. Bit 12 will cause a character flag if a double or greater than 8-bit character is detected.</p>
14 & 15	Rx/Tx CHARACTER & MATCH	<p>These bits define bytes in the character detect memory for comparison with the transmit and receive shift registers.</p> <p>For example, bit 15 should be set to compare with a stored STX (HB character detect), and bit 14 should be set for DLE STX (HB, LB character detect, respectively).</p> <p>The effective character detect storage space can be increased by using bit 15 and 14 on a single character detect address. In this case, the SEQ control function will be dominated by bit 14 which is important for character flags, transparency control, etc.</p> <p>The advantage of using bits 15 and 14 on a single entry can be demonstrated on an entry such as DLE STX. If STX alone is detected, bit 15 will allow SEQ control functions to be executed. However, if both DLE and STX are detected, bit 15 will be ignored and bit 14 will allow the selected SEQ functions to be executed.</p>

RECEIVE/TRANSMIT BLOCK CHECK CHARACTER (Rx/Tx BCC)—REGISTERS 15 AND 16

The Rx/Tx Register (register pointers 15 and 16, respectively) provides a 16-bit read-only register for monitoring the BCC Register.

Rx BCC: The Rx BCC operates on a one-character delay from the incoming data. If an error is detected, the BCC Register will be cleared immediately, and the BCC error flag will be set.

Tx BCC: The Tx BCC functions one-bit time behind the transmitted data. The BCC is right-justified, and bit zero is the Least-Significant Bit (LSB).

Rx/Tx POLYNOMIAL—REGISTER 17

The Transmit and Receive Polynomial has a common 24-bit programmable register. This register may be programmed for either LRC or CRC for up to 24 bits as follows:

NOTE

The BCC length must be a multiple of the character size.

Step 1:

Relate exponent positions to bit positions by assigning the second highest exponent (X^7 for $X^8 + 1$) to bit 0 and assign the remaining exponents, in descending order, from bit 0 upwards with X^0 (one) as the last assigned position. If the BCC is greater than 16 bits, continue with bit 0 for polynomials 24-16 (see description of bit 6 in the Miscellaneous Register).

Step 2:

Set the Polynomial Register to a one in all bit positions where the desired polynomial matches the assigned exponent positions. Ignore the polynomials' highest exponent; the hardware automatically includes this bit.

Examples (BCC's up to 16 bits)

Required Polynomial	Polynomial Register (Octal)
$X^6 + 1$ (LRC 6)	000040
$X^8 + 1$ (LRC 8)	000200
$X^{16} + 1$ (LRC 16)	100000
$X^{12} + X^{11} + X^3 + X^2 + X + 1$ (CRC 12)	007401
$X^{16} + X^{15} + X^2 + 1$ (CRC 16)	120001
$X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT)	102010

SPECIFICATIONS

Function

The DQ11 provides a two-way communications interface between the PDP-11 UNIBUS and a serial synchronous transmission line.

Type

Double-buffered, Transmit and Receive, Serializer/Deserializer.

DQ11

Operating Mode

Full- or half-duplex.

Transmission Speeds

EIA RS232C—Up to 10,000 Baud; Current Mode Operation—Up to 1.0 Megabaud.

Clocking

Synchronous clock from the modem (internal Crystal clock optional).

Sync Character

Program selectable.

Sync Detection

Activates on first non-sync character following one or two successive sync characters, or immediately upon detecting one or two successive sync characters (switch selectable).

Order of Bit Transmission

Low order bit first.

Error Detection

VRC (odd or even) for transmit and receive; jumper selectable. VRC (ON/OFF) is a program function.

Programmable for up to 24-bit polynomials for LRC or CRC (Optional). Common selections are LRC 8, 16, CRC 12, 16 and CCITT.

Character Recognition

Three switch-selectable characters for generating program interrupts.

Programmable character recognition for up to sixteen single or double characters (optional). Hardware functions upon character detection are also programmable under this option.

Program Interrupts

Program interrupts on RING, Carrier Detect, Clear to Send, Transmit/Receive DONE, Character Flag, and errors.

Character Size

Up to 16 bits per character, program selectable.

Double character transfers when eight bits (or less) per character are selected.

Bus Address

Bus Address (BA) may be set to any 128K word address.

Character Count

Character Count (CC) may be set for up to 65,536 characters.

UNIBUS Loads

The DQ11 Basic System Unit presents one load to the PDP-11 UNIBUS.

The Error Detection/Character Recognition Expander System unit also presents one load to the PDP-11 UNIBUS.

DQ11

Power Requirements

Basic System Unit: +5 V at 6.0 A
+15 V at .04 A
-15 V at .07 A

Error Detection/Character Recognition Expander System Unit:

Error Detection +5 at 1.2 A
Character Recognition +5 at 1.6 A

Temperature & Humidity Range

10 to 50° C with up to 90% non-condensing relative humidity.

ORDERING INFORMATION

DEC No.	Description	Prerequisite
DQ11-DA	Full-half-duplex synchronous line module set. EIA/CCITT termination suitable for direct use with Bell System 201 or equivalent modems. Transmission speeds up to 10,000 Baud. Data Set control included. Supplied with 7.6m (25-foot) modem cable.	PDP-11
DQ11-EA	Full-half-duplex synchronous line module set. TTL to Bell System 303 or equivalent modems. Transmission speeds up to 1.0 Megabaud. Data Set Control included. Supplied with 7.6m (25-foot) modem cable.	PDP-11
DQ11-AB	Cable-connected second system unit (Error Detection Expander Unit), with provisions for error detection of up to 24-bit polynomials for LRC and CRC checking.	DQ-11DA or DQ11-EA
DQ11-BB	Cable-connected second system unit (Character Recognition Expander Unit), with provisions for character recognition and hardware sequence control for protocol handling.	DQ11-AB
DQ11-KA	Internal Crystal Clock specified at Baud rate. Standard frequencies are 2.0K, 2.4K, 4.8K, 9.6K and 19.2K.	

DR11-B

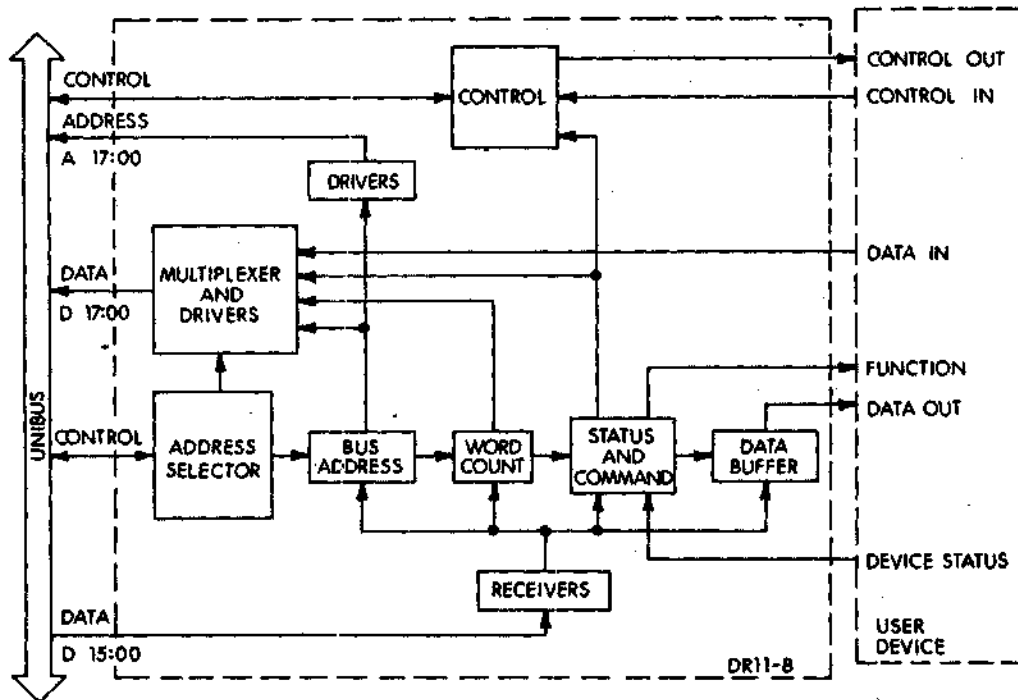
DIRECT MEMORY ACCESS INTERFACE, DR11-B

DESCRIPTION

The DR11-B is a general purpose direct memory access (DMA) interface to the UNIBUS. The DR11-B, rather than using program controlled data transfers, operates directly to or from memory, moving data between the UNIBUS and the user device.

The interface consists of four registers: command and status, word count, bus address, and data. Operation is initialized under program control by loading word count with the 2's complement of the number of transfers, specifying the initial memory or bus address where the block transfer is to begin, and by loading the command/status register with function bits. The user device recognizes these function bits and responds by setting up the control inputs. If the user device requests data from memory or a UNIBUS device, the DR11-B performs a UNIBUS Data In transfer (DATI) and loads its data register with the information held at the referenced bus address. The outputs of this register are available to the user device. (This output data is buffered.) If the user device requests data to be written into memory, the DR11-B performs a UNIBUS Data Out transfer (DATO), moving data from the user device to the referenced bus address. (This input data from the user is not buffered.) Transfers normally continue at a user defined rate until the specified number of words are transferred.

The user is given a number of control lines allowing for flexible operation. Burst modes, read-modify-restore operations, and byte addressing are possible with the control structure.

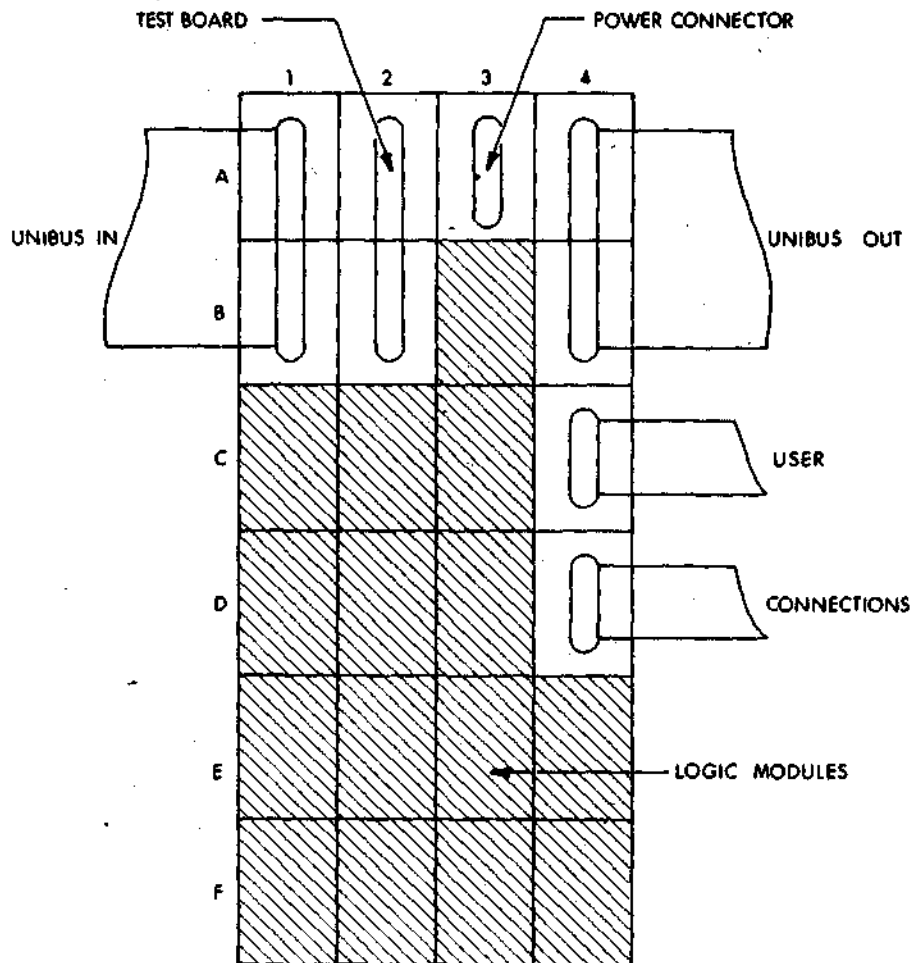


DR11-B

Physical Description

The DR11-B is packaged in one standard System Unit allowing convenient incorporation into a PDP-11 system. A UNIBUS jumper module (M920) is supplied with the unit.

Connections to the user device are made through two M957 split lug cable boards or one M9760 cable connector board (preferred over the M957's), which are supplied with the unit. Alternatively, an M920 can be used to jumper all user signals to an adjacent BB11 blank mounting panel, which can be used to hold some or all of the device logic. (Neither the additional M920 nor the BB11 is supplied with the unit.)



DR11-B System Unit

REGISTERS

Note: The INIT signal is held asserted internal to the DR11-B whenever an interlock error occurs (M9680 test board neither in slots AB02 for normal operation nor C004 for maintenance mode).

DR11-B

Word Count Register (DRWC) 772 410

DRWC is a 16-bit R/W register. It is initially loaded with the two's complement of the number of transfers to be made and normally increments up towards zero after each bus cycle. Incrementation can be inhibited by the user device; refer to the WC INC ENB user signal. When overflow occurs (all 1's to all 0's), the READY bit of DRST is set and bus cycles stop. DRWC is a word register; do not use byte instructions when loading this register. Cleared by INIT.

Bus Address Register (DRBA) 772 412

DRBA is a 15-bit R/W register. Bit 0, corresponding to address line A00 is provided by the user device. Along with XBA16 and 17 in DRST, DRBA is used to specify BUS A<17:01> in direct bus access. The register is normally incremented (by 2) after each cycle, advancing the address to the next sequential word location on the bus. If DRBA (corresponding to A<15:01>) overflows (all 1's to all 0's) the ERROR bit in DRST is set. This error condition (BAOF) is cleared by loading DRBA or INIT. Incrementation can be inhibited by the user device; refer to the BA INC ENB user signal. With this control signal and A00 provided externally, DRBA can be used to address sequential bytes. This is a word register; do not use byte instructions when loading this register. Cleared by INIT.

Status and Command Register (DRST) 772 414

The DRST is used to give commands to the user device and to provide status indicators of the DR11-B control and the user device.

BIT	NAME	FUNCTION
15	Error	Set to indicate an error condition: either NEX (BIT 14), ATTN (BIT 13), interlock error (test board is neither in slots AB02 nor CD04), or bus address overflow (BAOF:DRBA incremented from all 1's to all 0's). Sets READY (BIT 7) and causes interrupt if IE (BIT 6) is set. ERROR is cleared by removing all four possible error conditions: interlock error is removed by inserting test board in CD04 for diagnostic tests or in AB02 for normal operation; bus address overflow is cleared by loading DRBA; NEX is cleared by loading bit 14 with a zero; ATTN is cleared by user device. Read only.
14	Nonexistent Memory (NEX)	Set to indicate that as Unibus master, the DR11-B did not receive a Ssyn response 20 usec after asserting MSYN. Cleared by INIT or loading with a 0; can not be loaded with a 1. Sets ERROR. Read only.
13	Attention (ATTN)	Attention bit that reads the state of the ATTN user signal. Sets ERROR. (Used for

DR11-B

		device initiated interrupt.) Set and cleared by user control only. Read only.
12	Maintenance	Maintenance bit used with diagnostic programs. Cleared by INIT. Read/Write.
11-9	Device Status (DSTAT A,B,C)	Device status bits that read the state of the DSTAT A, B, and C user signals. (Not tied to interrupt.) Set and cleared by user control only. Read only.
8	Cycle	CYCLE is used to prime bus cycles; if set when GO is issued, an immediate bus cycle occurs. Cleared when bus cycle begins; cleared by INIT. Read/Write.
7	Ready	Set to indicate that the DR11-B is able to accept a new command. Set by INIT or ERROR; cleared by GO; set on word count overflow. Causes interrupt if bit 6 is set. Forces DR11-B to release control of the Unibus and prevents further DMA cycles. Read only.
6	Interrupt Enable (IE)	Set to allow ERROR or READY = 1 to cause an interrupt. Cleared by INIT. Read/Write.
5-4	Extended Bus Address	Extended bus address bits 17 and 16 that in conjunction with DRBA specify A(17:01) in direct memory transfers. Cleared by INIT. XBA17 & 16 do not increment when DRBA overflows; instead ERROR is set. Read/Write.
3-1	Function 3, 2, 1	Three bits made available to the user device. User defined. Cleared by INIT. Read/Write.
0	Go	Set to cause a pulse to be sent to the user device indicating a command has been issued. Clears READY. Always reads as a zero. Write only.

Data Buffer Register (DRDB) 772 416

The DRDB serves two functions: First, it is a 16-bit write only register. The outputs of this register are available to the user device (refer to the DATA OUT signals). The register can be loaded under program control, but is also used to buffer information when data is being transferred from the UNIBUS to the user device (when DR11-B does a DAT1 cycle). DRDB is a word register; do not use byte instructions when loading this register. Cleared by INIT.

DR11-B

Second, the DRDB functions as a 16-bit read only register. Information to be read is provided by the user device on the DATA IN signal lines. These lines are not buffered and must be held until either read under program control or transferred directly to memory (DATA bus cycle).

Maintenance Mode

Checkout and test of the DR11-B is accomplished by using a MAINT bit in DRST along with a special maintenance module which simulates the user's device. The maintenance module plugs directly into the two slots normally occupied by the cable boards and jumps the output and input signals. The maintenance module is included with the DR11-B.

SPECIFICATIONS

Usage: Direct memory access (DMA) data transfer

Input/output levels: logic 1 = +3 V
(user interface) logic 0 = 0 V

Register Addresses

Word Count (DRWC) 772 410
Bus Address (DRBA) 772 412
Status and Command (DRST) 772 414
Data Buffer (DRDB) 772 416

2nd DR11-B 772 430 to 772 436
3rd DR11-B 772 450 to 772 456
4th DR11-B 772 470 to 772 476

UNIBUS Interface

Interrupt vector address: 124 (1st DR11-B)
(for other DR11-B's, assigned by user)

Priority level: BR5

Data transfer: NPR

Bus loading: 1 bus load

Mounting: 1 System Unit (SU)

Input Current: 3.3 A at + 5 V
(no current needed at - 15 V)

DR11-C

GENERAL DEVICE INTERFACE, DR11-C

DESCRIPTION

The DR11-C is a general-purpose interface between the PDP-11 UNIBUS and a user's peripheral. The DR11-C provides the logic and buffer register necessary for program-controlled parallel transfers of 16-bit data between a PDP-11 System and an external device. The interface also includes status and control bits that may be controlled by either the program or the external device for command, monitoring, and interrupt functions.

The DR11-C interface consists of three functional sections: address selection logic, interrupt control logic, and device interface logic.

The address selection logic determines if the interface has been selected for use, which register is to be used, if a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control; the interrupt bits are under control of the user's device.

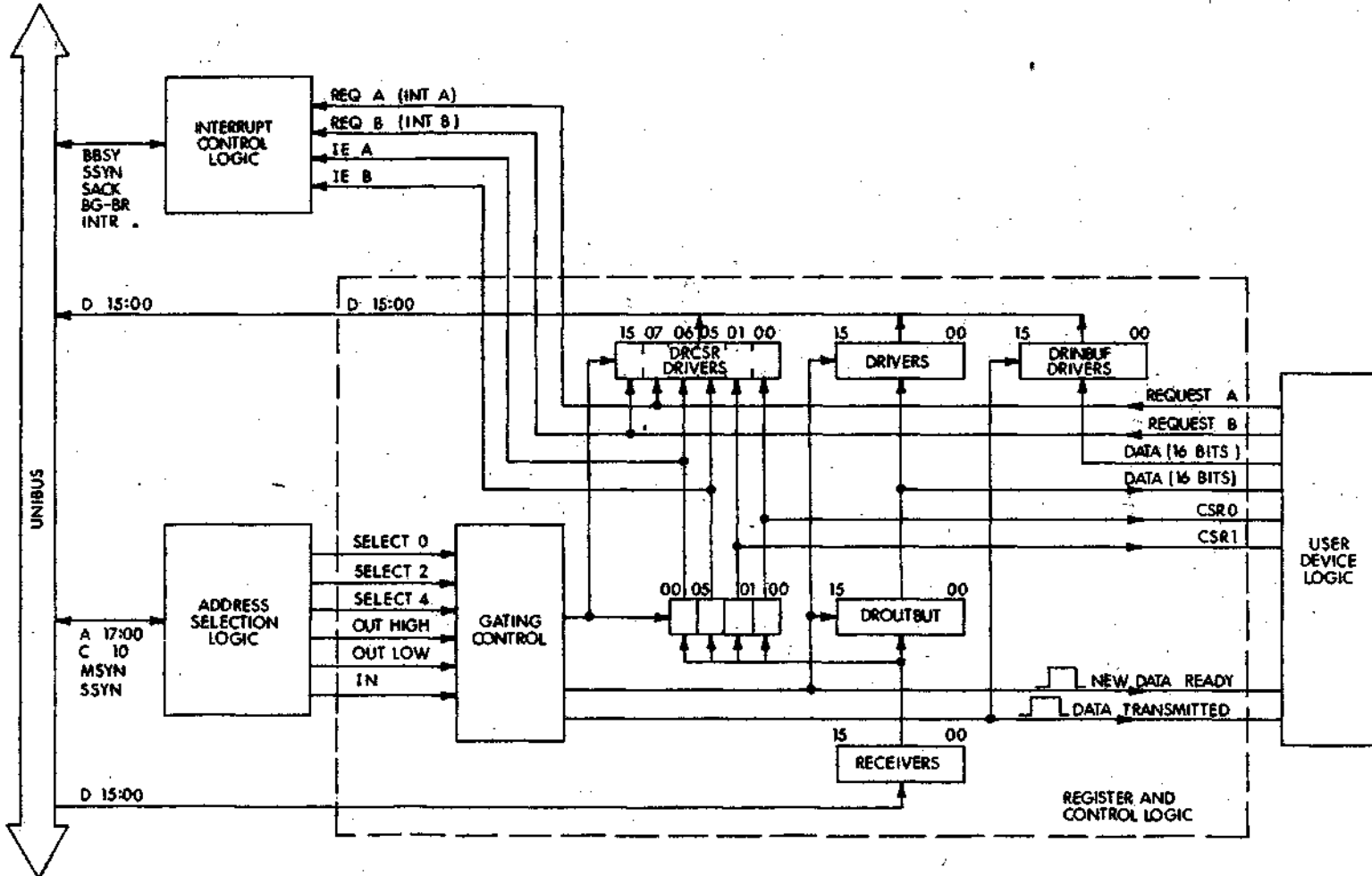
The DR11-C interface logic consists of three registers: control and status, input buffer, and output buffer. Operation is initialized under program control by addressing the DR11-C to specify the register and the type of operation to be performed.

If an output operation is specified, information from the UNIBUS is stored in a 16-bit register. Once this register has been loaded under program control (e.g., MOV R0, OUTBUF), the outputs are available to the device until the register is loaded with new data from the bus. The register can also be read onto the bus. Upon transfer of data to the buffer register, a NEW DATA READY control signal is supplied to indicate to the user's device that data has been loaded by means of a DATO or DATOB bus cycle and is read by means of a DATI or DATIP bus cycle.

When an input operation is specified, the DR11-C provides 16 lines of input to UNIBUS transmitters. This permits data from the user's device to be read onto the bus. A control signal, DATA TRANSMITTED, informs the device that the input lines have been read. The input lines, which are not buffered, can be read by a DAT bus cycle (e.g., MOV INBUF, R0).

The control and status register provides six bits that can be used to control and monitor user functions. Two of these bits are interrupt enable (INT ENB) bits under control of the program. Two bits (REQ A and B) are under direct control of the user's device and can only be read by the program. These bits can be used either to initiate interrupt requests or to provide flags that can be monitored by the program. The remaining two bits (CSR0 and CSR1) are read/write bits that can be controlled by the program to provide command or monitoring functions. In the main-

DR11-C



DR11-C Interface, Block Diagram

DR11-C

tenance mode, they are also used to check operation of the interface.

A maintenance cable, which is supplied with the interface, permits checking of the DR11-C logic by loading the input buffer from the output buffer rather than from the user's device. Thus, a word from the bus is loaded into the output register and the same word appears when reading the input buffer, provided the interface is functioning properly.

The DR11-C can also be used as an interprocessor buffer (IPB) to allow two PDP-11 processors to transfer data between each other. In this case, one DR11-C is connected to each processor bus and the two DR11-Cs are cabled together, thereby permitting the two processors to communicate.

Physical Description

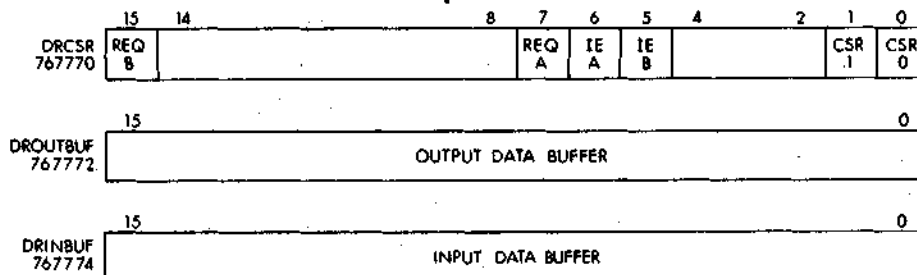
The DR11-C interface is packaged on a single quad module that can be plugged into a small peripheral slot (SPC).

The module has two Berg connectors for all user input/output signals. Two M971 connector boards, which are not supplied with each interface, can be used to bring all input/output lines to individual pins on a back panel via two H856 cables. Note that this cable is a "mirror image" rather than a straight one-to-one cable.

The following accessories are available for interfacing:

- BC08R (Berg-to-Berg) flat cable. Available in lengths of 1, 6, 8, 10, 12, 20, and 25 feet. When ordering, the dash number indicates the desired cable length; e.g., BC08R-1 or BC08R-25.
- M971 connector board. A single-height by 8-1/2 in. board that brings the signals from one Berg connector to the module fingers.
- BC11K-25 cable. Consists of a 20 twisted-pair cable with a Berg connector on one end only. Available in 25 ft lengths.
- H856 Berg connector. Includes an H856 Berg connector and 40 pins. Crimping tools are available from: Berg Electronics, Inc., New Cumberland, Pa. 17070.

REGISTERS



The register addresses can be changed by altering the jumpers on the address selection logic. However, any programs or other software re-

DR11-C

ferring to these addresses must also be modified accordingly if the jumpers are changed.

Control and Status Register (DRCSR) 767 770

The control and status register is used to enable interrupt logic and to provide user-defined command and status functions for the external device.

Two REQUEST bits, which are under device control, may be used to provide device status indications, or may be used to initiate interrupts when used with associated INT ENB (interrupt enable) bits which are under program control. Two other bits (CSR0 and CSR1) are controlled from the UNIBUS and serve as command bits.

Although the REQUEST and CSR bits can be used for any function the user desires, standard PDP-11 interface conventions attempt to allocate bit 15 for error conditions and bit 7 for ready indications and both of these bits can generate interrupt requests. In addition, bit 0 is normally used for start or go commands.

DRCSR Bit Assignments

BIT	NAME	FUNCTION
15	REQUEST B	<p>This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program.</p> <p>When used as an interrupt request, it is set by the external device and initiates an interrupt provided the INT ENB B bit (bit 05) is also set.</p> <p>When used as a flag, this bit can be read by the program to monitor external device status.</p> <p>When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 01). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value.</p> <p>Read-only bit. Cleared by INIT when in Maintenance Mode.</p>
07	REQUEST A	<p>Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set.</p> <p>When the maintenance cable is used, the state of REQUEST A is identical to that of CSR0 (bit 00).</p> <p>Read-only bit. Cleared by INIT when in Maintenance Mode.</p>

DR11-C

06	INT ENB A	<p>Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST A (bit 07) becomes set.</p> <p>Can be loaded or read by the program (read/write bit). Cleared by INIT.</p>
05	INT ENB B	<p>Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set.</p> <p>Can be loaded or read by the program (read/write bit). Cleared by INIT.</p>
01	CSR1	<p>This bit can be loaded or read (under program control) from the UNIBUS and can be used for a user-defined command to the device (appears only on Connector No. 1).</p> <p>When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program.</p> <p>Read/write bit (can be loaded or read by the program). Cleared by INIT.</p>
00	CSRO	<p>Performs the same functions as CSR1 (bit 01) but appears only on Connector No. 2.</p> <p>When the maintenance cable is used, the state of this bit controls the state of bit 07 (REQUEST A).</p> <p>Read/write bit. Cleared by INIT.</p>

Output Buffer Register (DROUTBUF) 767 772

The output buffer is a 16-bit read/write register that may be read or loaded from the UNIBUS. Information from the bus is loaded into this register under program control. At the time of loading, a pulsed signal (NEW DATA READY) is generated to inform the user's device that the register has been loaded. The trailing edge of the positive pulse should be used to allow the data to be loaded and settle on the user's input lines. Data from the buffer is transmitted to the user's device on the data OUT lines by means of a DATO or DATOB bus cycle.

The contents of the output buffer register may be read at any time by means of a DATI or DATIP bus cycle. During the read operation, the output of the buffer is fed directly to the bus data lines.

Whenever the maintenance cable is used, the data from the output buffer is also applied to the input buffer register. This permits checking operation of the interface logic.

The DROUTBUF is cleared by INIT.

DR11-C

Input Buffer Register (DRINBUF) 767 774

The input buffer is a 16-bit read-only register that receives data from the user's device for transmission to the UNIBUS. Information to be read is provided by the user's device on the data IN signal lines. Because the input buffer consists of gating logic rather than a flip-flop register, the data IN lines must be held until read onto the bus. The register is read by a DATI sequence and the data is transmitted on the UNIBUS for transfer to the processor or some other device. When the input lines are read during a DATI sequence, a pulsed signal (DATA TRANSMITTED) is sent to the user's device to inform it that the transfer has been completed. The trailing edge of the positive-going pulse indicates that this transfer is completed.

Whenever the maintenance cable is used, the input buffer register receives data from the output buffer register rather than from the user's device. This permits checking of the interface logic by loading a word from the bus into the output register and verifying that the same word appears in the input buffer.

Input and Output Signals

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN00	2	TT	OUT00	1	C
IN01	2	LL	OUT01	1	K
IN02	2	H	OUT02	1	NN
IN03	2	BB	OUT03	1	U
IN04	2	KK	OUT04	1	L
IN05	2	HH	OUT05	1	N
IN06	2	EE	OUT06	1	R
IN07	2	CC	OUT07	1	T
IN08	2	Z	OUT08	1	W
IN09	2	Y	OUT09	1	X
IN10	2	W	OUT10	1	Z
IN11	2	V	OUT11	1	AA
IN12	2	U	OUT12	1	BB
IN13	2	P	OUT13	1	FF
IN14	2	N	OUT14	1	HH
IN15	2	M	OUT15	1	JJ
REQ A	1	LL	NEW DATA RDY*	1	VV
REQ B	2	S	DATA TRANS.*	2	C
			CSR0	2	K
			CSR1	1	DD
			INIT	1	P
			INIT	2	RR, NN

* Pulse signals, approximately 400-ns wide. Width can be changed by user.

DR11-C

Pin Connections

M971		DR11-C				M971	
Board	Berg Header	Connector No. 2		Connector No. 1		Berg Header	Board
		Pin	Name	Name	Pin		
U2	A	VV	OPEN	OPEN	A	VV	A1
U1	B	UU	GND	OPEN	B	UU	A2
V2	C	TT	IN00	OUT00	C	TT	A1
V1	D	SS	GND	OPEN	D	SS	A2
T2	E	RR	INIT H	OPEN	E	RR	B1
T1	F	PP	GND	OPEN	F	PP	B2
T2	H	NN	INIT H	OPEN	H	NN	C1
T1	J	MM	GND	GND	J	MM	C2
S2	K	LL	IN01	OUT01	K	LL	D1
S1	L	KK	IN04	OUT04	L	KK	D2
R2	M	JJ	GND	GND	M	JJ	E1
R1	N	HH	IN05	OUT05	N	HH	E2
P2	P	FF	OPEN	INIT H	P	FF	F1
P1	R	EE	IN06	OUT06	R	EE	F2
N2	S	DD	GND	GND	S	DD	H1
N1	T	CC	IN07	OUT07	T	CC	H2
M2	U	BB	IN03	OUT03	U	BB	J1
M1	V	AA	GND	GND	V	AA	J2
L2	W	Z	IN08	OUT08	W	Z	K1
L1	X	Y	IN09	OUT09	X	Y	K2
K2	Y	X	GND	GND	Y	X	L1
K1	Z	W	IN10	OUT10	Z	W	L2
J2	AA	V	IN11	OUT11	AA	V	M1
J1	BB	U	IN12	OUT12	BB	U	M2
H2	CC	T	GND	GND	CC	T	N1
H1	DD	S	REQ B	CSR1	DD	S	N2
F2	EE	R	GND	GND	EE	R	P1
F1	FF	P	IN13	OUT13	FF	P	P2
E2	HH	N	IN14	OUT14	HH	N	R1
E1	JJ	M	IN15	OUT15	JJ	M	R2
D2	KK	L	GND	GND	KK	L	S1
D1	LL	K	CSR0	REQ A	LL	K	S2
C2	MM	J	GND	GND	MM	J	T1
C1	NN	H	IN02	OUT02	NN	H	T2
B2	PP	F	OPEN	GND	PP	F	T1
B1	RR	E	IN02	OUT02	RR	E	T2
A2	SS	D	OPEN	GND	SS	D	V1
A1	TT	C	DATA TRANS.	OPEN	TT	C	V2
A2	UU	B	OPEN	GND	UU	B	U1
A1	VV	A	OPEN	NEW DATA RDY	VV	A	U2

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BC11K Connections

Twisted Pair	Color	Pin	Connector No. 1	Connector No. 2
black/white-orange	black wh-org	A	OPEN	OPEN
		B	OPEN	OPEN
black/white-yellow	black wh-yel	C	OUT00	DATA TRANS.
		D	OPEN	OPEN
black/white-grey	black wh-gry	E	OPEN	IN02
		F	OPEN	OPEN
black/white-red	black wh-red	H	OPEN	IN02
		J	GND	GND
black/white-green	black wh-grn	K	OUT01	CSRO
		L	OUT04	GND
brown/green	brown green	M	GND	IN15
		P	INIT	IN13
brown/red	brown red	N	OUT05	IN14
		R	OUT06	GND
black/white-blue	black wh-blu	S	GND	REQ B
		T	OUT07	GND
black/orange	black orange	U	OUT03	IN12
		V	GND	IN11
black/white-violet	black wh-vio	W	OUT08	IN10
		X	OUT09	GND
black/red	black red	Y	GND	IN09
		Z	OUT10	IN08
brown/yellow	brown yellow	AA	OUT11	GND
		BB	OUT12	IN03
black/blue	black blue	CC	GND	IN07
		DD	CSR1	GND
brown/orange	brown orange	EE	GND	IN06
		FF	OUT13	OPEN
brown/blue	brown blue	HH	OUT14	IN05
		JJ	OUT15	GND
black/yellow	black yellow	KK	GND	IN04
		LL	REQ A	IN01
brown/violet	brown violet	MM	GND	GND
		NN	OUT02	INIT

DR11-C

black/violet	black violet	PP	GND	GND
		RR	OUT02	INIT
black/green	black green	SS	GND	GND
		TT	OPEN	IN00
pink/white-red	pink wh-red	UU	GND	GND
		VV	NEWDATA RDY	OPEN

SPECIFICATIONS

Usage:

Priority interrupt interface control

Input/output levels: (user interface)

logic 1 = +3 V
logic 0 = 0 V

Register Addresses

Control and Status (DRCSR) 767 770
Output Buffer (DROUTBUF) 767 772
Input Buffer (DRINBUF) 767 774

2nd DR11-C 767 760 to 767 764
3rd DR11-C 767 750 to 767 754
4th DR11-C (etc) (etc)

UNIBUS Interface

Interrupt vector addresses: floating (see Appendix A) (2 needed for each DR11-C)

Priority level: BR5 (may be changed)
Bus loading: 1 bus load

Mechanical

Mounting: 1 SPC slot
Size: quad module

Input Current: 1.5A at +5V
(no current needed at -15V)

Miscellaneous:

Inputs: One standard TTL unit load; diode protection clamps to ground and +5V

Outputs: TTL levels capable of driving 8 unit loads except for the following:

NEW DATA READY = 30 unit loads

DATA TRANSMITTED = 30 unit loads

INIT (initialize) = common signal on both connectors driven by one 30-unit load driver

DR11-C

Signals: NEW DATA READY—drives 30 units, positive pulse, 400-ns wide unless width changed by an external capacitor

DATA TRANSMITTED—drives 30 unit loads, positive pulse, 400-ns wide unless width changed by an external capacitor

INIT (initialize)—common signal on both connectors driven by one 30-unit load driver

Data Inputs: 16-bit word from the external device

Data Outputs: 16-bit word from the UNIBUS. Either a full word or an 8-bit byte (either high or low) may be loaded from the bus.

Maintenance Mode: A MAINT cable (supplied with basic system) jumpers the DROUTBUF outputs to the DRINBUF inputs and forces bits 15 and 7 to read as CSR1 and CSR0, respectively.

GENERAL DEVICE INTERFACE DR11-K

FEATURES

- 16-bits input and output
- Each input line can generate an interrupt
- Recoverable over-voltage protection
- Interface processor-to-processor within PDP-11 family
- Completely self-contained interface
- Supplies all needed control signals
- Operates in PDP-11 interrupt environment

DESCRIPTION

The DR11-K General Device Interface is an integral logic module which forms a self-contained digital input-output interface between the PDP-11 UNIBUS and a user's peripheral. The DR11-K performs all of the necessary tasks to communicate with the PDP-11, so that the user may easily interface a device or devices.

Under program control, the DR11-K permits bidirectional parallel transfer of up to 16 bits of information between a PDP-11 UNIBUS and a user's device or another DR11-K. All interfacing lines to and from the DR11-K are fused and have over-voltage protection.

Various options, which are hardware-selected by the user, are available for data inputting. Data can either be read off a user's device directly onto the UNIBUS or through the input register. The input register bits are transitionally set by its respective input line. Each of the input register bits can be hardware-selected to generate an interrupt to the UNIBUS.

The DR11-K can be used as an interprocessor buffer to allow two PDP-11 processors to exchange data.

OUTPUT—The output lines are driven from a 16-bit output register. Under program control, information from the UNIBUS can be loaded into the output register in byte or word format. The outputs are then made available to the user's device following an exchange of control signals. Once the external device accepts the data, a new transfer can be initiated. The output register can also be read onto the UNIBUS.

INPUT—The DR11-K also provides 16 lines of input for a transfer onto the UNIBUS. These signals can be hardware-selected to be directly read from the input lines or via the input buffer register. When going through the input buffer register each input line can be selected to individually interrupt the UNIBUS by simply presetting a micro switch mounted on the interface. The four most significant bits (15-12) have additional input buffer setting capabilities. Hardware-selectable, these buffer bits can be set by a negative input transition, a positive input transition, or by either a positive or negative transition. The bidirectional transition setting allows an interrupt to occur on an input change. This added

DR11-K

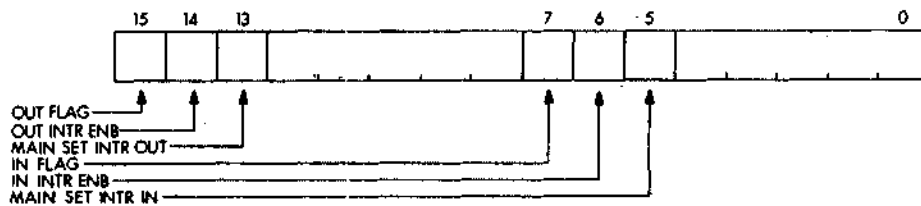
feature of bits 12 through 15 was specifically designed for interfacing to devices such as the Coulter Model "S" Blood Counter.

CONTROL—To transfer a word of data to the DR11-K, the external device places data on the input lines. The device, after allowing sufficient time for setting of transients, sends a Pulse on the External Data Ready line. If the Input Interrupt Enable (status register bit 06) is set, the External Data Ready Pulse will generate an interrupt to the UNIBUS. When the input lines are read by the software, a control signal is generated, called Internal Data Accept by the DR11-K. Once the external device receives this signal, new data can be transferred by repeating this operation. This method of interrupting is logically OR'd with the output of a circuit that allows for individual line interrupts.

After the data is loaded into the output register, a control signal is generated called Internal Data Ready High and Internal Data Ready Low, corresponding to a high- or low-byte transfer of data. If a full 16-bit word transfer is required, either line can be used. When the external device accepts the data, a control signal is sent back to the DR11-K called External Data Accept. This then causes an interrupt to the UNIBUS if the Output Interrupt Enable (status register bit 14) is set.

Input and Output interrupts provide the ability to make vectored interrupt requests to the PDP-11 processor through two unique vector addresses. Interrupt enable/disable circuits are controlled by bits 14 and 6 of the addressable DR11-K status register.

REGISTERS



Status Register

15	OUT FLAG	Indicates an External Data Accept has been received from an external device.
14	OUT INTR ENB	Enables an interrupt to occur when an External Data Accept has been received. Cleared when interrupt accepted by UNIBUS.
13	MAIN SET INTR OUT	Used for maintenance only. When set, an interrupt to the UNIBUS is generated.

DR11-K

7	IN FLAG	Indicates an External Data Ready has been received from an external device.
6	IN INTR ENB	Enables an interrupt to occur when an External Data Ready has been received. Cleared when interrupt accepted by UNIBUS.
5	MAIN SET INTR IN	Used for maintenance only. When set, an interrupt to the UNIBUS is generated.

Output Register All 16 bits may be read or loaded from the UNIBUS. Outputs available to user.

Input Register All 16 bits may be read from UNIBUS. Bit status determined by user input lines.

SPECIFICATIONS

Register Addresses

Status Register	767770	} May be changed by a micro switch register
Input	767772	
Output	767774	
Input Vector	300	} May be changed by a micro switch register
Output Vector	304	

Priority Level

BR4 normal

May be changed by priority jumper plug

Input Levels

0 volts = 1, + 3 volts = 0

Recoverable overvoltage protection for inputs between -10Vdc to +15Vdc, fusible resistor will open when current exceeds 250 mA.

In addition, lines 12 through 15 can be selected to sense transition polarity—shipped to sense negative pulse (+3V to ground)

May be changed by jumpers

Each input = 3 TTL unit loads or 4.8 mA

Output Levels

0 volts = 1, + 3 volts = 0
Capable of driving 18 TTL load

30 mA max @ zero volts output
5mA max @ +4V output, fusible resistor will open when current exceeds 250 mA.
Over-voltage protection for outputs between 0V to +5Vdc.

DR11-K

Signal Connections

Input, output, control and ground signals are available on two H854 40-pin I/O connectors. Connections are normally made using cables terminated with an H856 connector, such as the BC08R and BC04Z up to 50 feet. For longer distances (up to 300 feet) a combination of BC08R cable and H322 distribution panel is recommended. The H322 panel distributes the lines of two BC08R cables to 80 screw terminals allowing for connection to the screw terminals of both input and output lines by means of shielded twisted pair cable (such as Belden #8777, #8725, #8774, #8755 or equivalent). All cabling hardware is optional. A one-foot BC08R cable is shipped with the DR11-K for diagnostic purposes.

Environmental

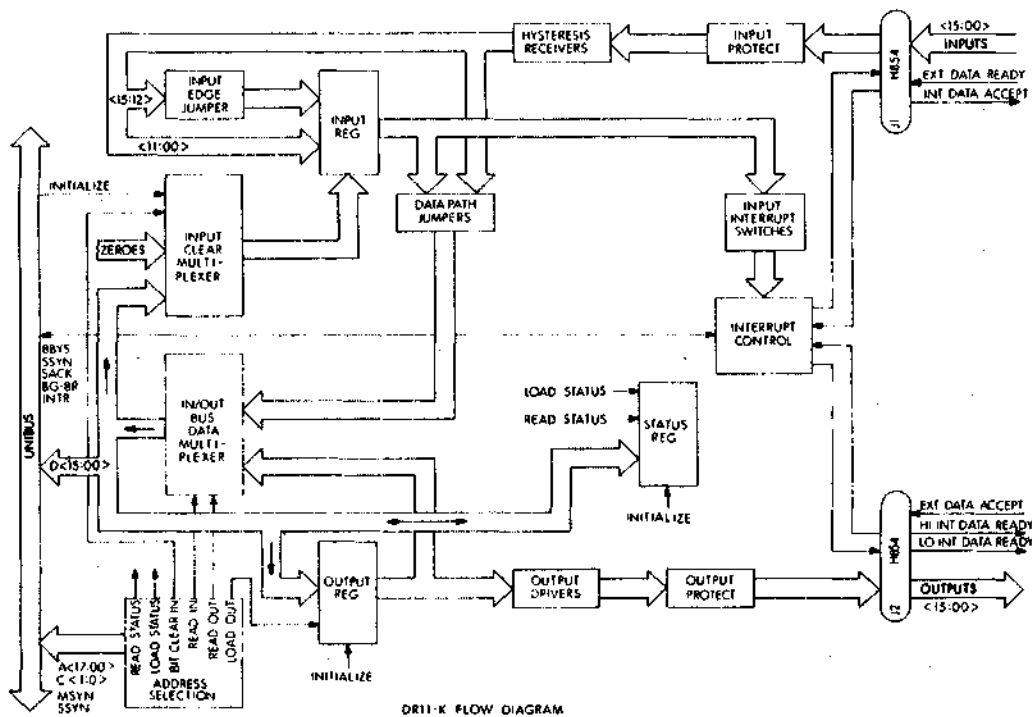
Temperature +5° C to +43°C
 Humidity 20% to 80% non-condensing

Physical

The DR11-K consists of one hex module (M7843) which mounts in one of the center SPC slots of a DD11-B.

Power Requirements and UNIBUS Loading

The DR11-K uses +5Vdc at 2.5A max. and poses one UNIBUS unit load.



UNIBUS SWITCH, DT03-F

The DT03-F UNIBUS Switch is an electronic switch that allows a single peripheral or a group of peripherals to be switched from one processor to another. It provides on-line system back-up and dynamic reconfiguration for systems where very high reliability is required.

The UNIBUS Switch implements a switched or "common" bus that can be selectively connected to the UNIBUS of any processor in a multi-processor system. Any device or devices except a processor may be connected to this common bus. When the switch is connected to a particular processor's UNIBUS, all peripherals and memory on the common bus operate just as though they were permanently connected to that bus. When the switch is disconnected, all peripherals on the common bus are removed from that UNIBUS and are available for connection to any other processor's UNIBUS. Once switched to a particular UNIBUS, the Bus Switch is transparent to the processor program. The switch is engineered to preserve the transmission properties of all busses attached to it regardless of the switch's position. Even during on-line switching all busses are synchronized to prevent interfering with individual programs. In order to guarantee bus operations, the switching elements are electronic circuits that receive and regenerate all bus signals passing through the switch. These electronic circuits not only eliminate impedance-mismatch and crosstalk problems, but also provide the long-term reliability inherent in solid-state circuits.

The bus switch is available in two versions:

DT03-FP—Both programmable and manual control

DT03-FM—Manual control only

Both models are constructed from modular sections, each of which is analogous to a multi-pole, single-throw switch that connects the shared bus to one processor bus at a time. The module consists of a UNIBUS isolation circuit, a bus repeater, bus-synchronization logic, and, in the case of the -FP version, a programmable controller.

Each DT03-F section (a DT03-F has one section for each processor that can attach to the common bus) has two switch positions: Connected and Neutral, defined as follows:

Connected: In this position the switched bus is connected directly to the processor associated with that section, and all of the devices on the switched bus are available to that processor. Only one section of a switch can be in the connected position at a time (i.e., the common bus can only be used by one processor at a time).

Neutral: In this position the switched bus is not connected to the processor. When the switches in all sections are in the neutral position, devices on the switched bus can then be serviced or repaired without disturbing operations on any processor busses.

In the manual-control mode, the operator can select either local- or remote-command inputs to the DT03-F. Local control is derived from a

DT03

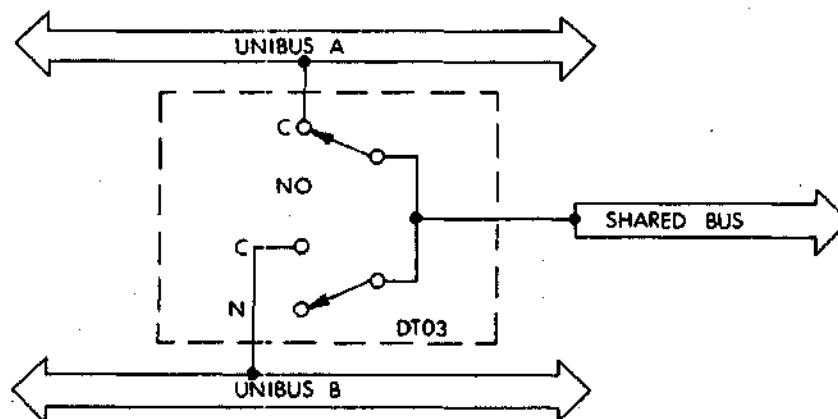
toggle switch that either enables or disables the bus signal-flow through the switch section. In the remote mode, the DT03-F position can be manually controlled via signal wires from a distant location.

The FP version includes a programmable control that allows switch operation under processor control.

In both manual and programmable modes, the bus synchronizer assures that the switch changes position without interfering with any operations on the processor bus, i.e., the switch can be thrown while a program is running. If two or more processors request use of the shared bus simultaneously, a priority-arbitration circuit within the switch specifies which processor will be serviced first. The priority-arbitration circuit assures that no more than one processor at a time is connected to the shared bus.

All DT03-F's include circuitry to isolate the switch itself from the processor buses in the event that either the switch power supply is de-energized or a peripheral-device power supply is de-energized on the shared bus. When the supply is off, a relay disconnects the +5 V and ground lines between the supply and the logic modules. The UNIBUS interface circuits are held in a high-impedance state that will not load down the processor busses. At the same time, another set of relays close and provide an alternate path to preserve continuity of the bus grant signals on each processor bus. The DT03-F logic panel can then be serviced without interfering with program operation.

An important feature of the bus switch in high-reliability applications is the ability to disconnect itself from a processor that is no longer operational. The DT03-FP contains a "watch-dog" timer that monitors the processor currently using the switch. If that processor does not reset the timer within the allotted interval (thereby indicating that the processor has halted or is executing an invalid program), the switch automatically disconnects. Similarly, a power failure in the system to which the common bus is connected automatically disconnects the switch. A back-up processor can then assume control of the switch and proceed to operate the devices on the shared bus.



Equivalent Circuit of DT03

PROGRAMMING

The DT03-FP has associated with it two programmable registers (one for each CPU), the Control and Status Registers, and one interrupt vector for each processor connected to it. The bits of the Control and Status Registers are defined as follows:

BIT	NAME	FUNCTION
15	Watch-Dog Timer Overflow	Set to indicate that the processor failed to clear the Common Bus Requested bit (bit 12) within 10 milliseconds. The common bus is automatically disconnected. Causes an interrupt if Interrupt Enable (bit 6) is set.
14	Power Failure	Set to indicate a power failure on the shared bus or in the switch itself. Setting of this bit also triggers a power-fail interrupt in the processor connected to this switch section and isolates the switch from the processor bus, thereby allowing the processor to restart.
13	Bus Active	Set to indicate that the shared bus is already connected to a processor.
12	Common Bus Requested	Set to indicate that some other processor wants to use the common bus, i.e., it has set its own Request bit (bit 0). Causes an interrupt if Interrupt Enable (bit 6) is set and also starts the watch-dog timer. (Clearing this bit stops the watch-dog timer.)
11		Not used.
10		Not used.
9	Reset	Set to send an initialize pulse to all devices on the common bus.
8		Not used.
7	Common Bus Connected	Set to indicate that the processor has been connected to the common bus. Causes an interrupt if Interrupt Enable (bit 6) is set.
6	Interrupt Enabled	Set by the processor to allow interrupts under the following conditions: 1. Common bus connected (bit 7) 2. Common bus requested (bit 12) 3. Watch-dog timer overflow (bit 15) 4. Connect request failed (see bit 0)
5-1		Not used.
0	Request Common Bus	Set to request connection to the common bus. If the common bus is not in use, the switch will connect the processor to it immediately. If the shared bus is in use, the Common Bus Requested bit (bit 12) is set for the processor connected to the common bus and the watch-dog timer is started for that processor. At the same time, a Request Timer in this DT03-F section is started. If the

DT03

processor using the shared bus does not relinquish the bus within the timer interval, the Request bit will be cleared and an interrupt will occur (if Interrupt Enable, bit 6, is set). If the other processor does release the shared bus in time, this DT03-FA will connect and will set the Connected bit (bit 7). The Request bit can be cleared by the processor to disconnect itself from the shared bus.

SPECIFICATIONS

Option Designations

DT03-FP UNIBUS Switch (Programmable and Manual Control).

DT03-FM UNIBUS Switch (Manual Control Only).

Interrupt Vector

Requires one vector assigned from either the User Reserved Vectors (170, 174, 270, 274) or from the Floating Vector Field.

Priority Level Switching Time.

BR7

Less than one microsecond; busses automatically synchronized.

Watch-dog Timer Latency

Interval set to approximately 10 milliseconds. Bus cycles that go through the switch (i.e., between a switched and a non-switched peripheral) are extended 450 nanoseconds. Each DT03-F module places a one-unit load on its processor UNIBUS and on the shared UNIBUS.

Bus Loading

Power Supply

Power supply is mounted on rear door of cabinet. Relay power isolation when de-energized.

AC Power Installation

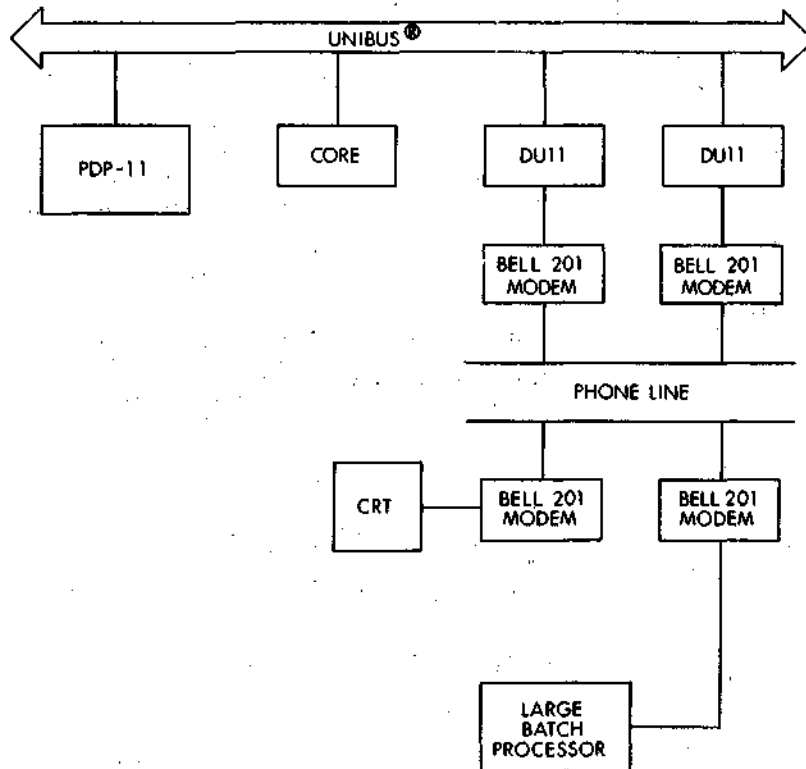
115/230 V, 50/60 Hz, 2 A.

Each DT03-F section is constructed on a standard 5 $\frac{1}{4}$ x 19-inch rack-mountable logic panel.

UNIBUS Compatibility

Can be used with any PDP-11 Family processor. (When used with the PDP-11/20, the KH11-A Large-System Capability Option must be installed in the processor).

SYNCHRONOUS LINE INTERFACE, DU11



FEATURES

- Transmission speeds up to 9600 Baud
- Double-buffered program interrupt
- Full- or half-duplex operation
- Programmable Sync character
- Programmable character size (5, 6, 7, or 8 bits)
- Receiving Sync character stripping program selectable
- Automatic transmit of Sync program selectable
- Interfaces to Bell Series 200 synchronous modems or equivalent
- Auto answering capability
- Parity checking and generation
- Modem control
- Simple, compact, single-board design

INTRODUCTION

The DU11 is a single-line, program-controlled, double-buffered communications device designed to interface the PDP-11 Processor to a serial synchronous line. The self-contained unit is fully programmable with respect to Sync character, character length (5 to 8 bits), and parity selection.

The DU11 is ideally suited for interfacing the PDP-11 to high-speed synchronous lines for remote batch, remote data collection, and remote

DU11

concentration applications. Multiple DU11's on a PDP-11 allow its use as a synchronous line concentrator or front-end synchronous controller to a larger computer.

The DU11 provides serial-to-parallel and parallel-to-serial data conversion, voltage level conversion, and modem control for half- or full-duplex operation. The Bell Series 200 synchronous modems or equivalent may be used with the DU11.

Modem control is a standard feature of the DU11. The necessary signals needed to establish communications with the Bell Series 200 synchronous modems are present in the Receive Status Register (RxCSR). No transition of control lines emanating from the modem directly cause a change in the state of the transmitter or receiver logic.

The DU11 is capable of transmitting data at the following speed:

EIA/CCITT: 9600 Baud maximum
(limited by modem and data set interface level converters)

The DU11 conforms to Electronic Industries Association (EIA) specification RS232C and CCITT Recommendation V.24.

OPERATION

General

The DU11 is a character buffered synchronous serial line interface capable of two-way simultaneous communications. The DU11 translates between serial data and parallel data. Output characters are transferred in parallel from the PDP-11 UNIBUS™ into the DU11 where they are serially shifted to the communication line. Input characters from the modem are shifted into the DU11 and made available to the PDP-11 on an interrupt basis.

Synchronization between the DU11 and the transmitting device is established by a Sync character code. Both the receiver and transmitter are double buffered. This allows a full character time in which to service transmitter and receiver interrupts. The clocking necessary to serialize the data is provided by the associated high-speed synchronous modem.

The DU11 consists of five registers: two status registers, two data buffer registers, and a Parameter Control Register which is used to control characteristics of the interface such as mode of operation (synchronous internal or external), number of bits per character, parity selection, and the Sync character.

For local connection (no modem) or for use with a modem without a clock, a clock option (DFC11-A) is available. The clock option requires a DF11 slot (provided in one of the two center slots of a DD11-B peripheral mounting panel).

Synchronous Mode—Transmitter Section

The transmitter section of the DU11 performs parallel-to-serial conversion of data supplied to it from the PDP-11 UNIBUS.

DU11

After the initialize pulse, the program must set the Parameter Control Register for the mode of operation (in this case synchronous), the desired character length (5, 6, 7, or 8 bits—parity not included), and the mode of parity.

Before any necessary handshaking with the data set, the program may load the Sync Register with the desired character. When the Sync Register is loaded, the character will be used for both the Receiver and Transmitter operations. Any required handshaking to establish connection with the data set may be done at this time.

Once handshaking is complete, the program can assert the Send bit in the Transmitter Status Register (TxCSR). When Send is asserted, the transmitter is enabled but will not start transmitting data until the first character is loaded into the Transmitter Data Buffer (TxDBUF). If Send is cleared during transmission, the character currently being transmitted will be completed, the line will go to a mark hold state, the internal transmitter logic will be reset, and synchronization will be lost. When Send is cleared, there is no guarantee that the Transmitter Done bit will assert upon completion of transmission of the current character.

When it is necessary to know when the last bit of the last character has been transmitted, the following steps may be taken: Prior to loading the Transmitter Data Buffer (TxDBUF) with the last character, the DNA INTR EN (Data Not Available Interrupt Enable) bit should be asserted in the Transmitter Status Register (TxCSR) and the Tx DONE INTR EN bit should be cleared. The interrupt in the transmitter logic subsequent to the loading of the TxDBUF will signify the completion of the transmission of the last character.

The transmission of initial Sync characters may be accomplished through either of the following two methods:

1. The program must arrange its data buffer such that the required number of Sync characters precedes any text. The Sync Register may or may not contain the Sync character. If the Sync Register is not loaded, it will contain an all-ones character subsequent to a master reset or initialize.

Assuming that any necessary handshaking has been completed with the data set and that Send has been asserted, the program can commence transmission from its data buffer.

When the first data bit is transferred to the communications line, the Transmitter Done bit will be asserted. If the Transmitter Interrupt Enable bit is set, an interrupt request will be generated.

If the Sync character was not initially loaded into the Sync register, then synchronization cannot be guaranteed unless the program response to the Transmitter Done Bit is less than $1/\text{Baud} \times (\text{bits per character} - 1/2 \text{ bit time})$ seconds. This can be verified by the absence of the Data Not Available (DNA) bit in the TxCSR and applies only to the transmission of the initial Sync characters.

DU11

Subsequent synchronization can be maintained by having the program insert Sync characters into the message at the established intervals.

An alternate method of maintaining subsequent synchronization would be to load the Sync Register with the Sync character and assert the Data Not Available Interrupt Enable bit in the TxCSR. The program could ignore the service of the Transmitter Done bit at certain intervals by clearing the Transmitter Done Interrupt Enable bit. During this interval, transmission would be from the Sync Register. When transmission from the Sync Register begins, the Data Not Available bit will assert, causing an interrupt request. As long as the program ignores the Transmitter Done Bit, transmission will emanate from the Sync Register.

If desired, the program can ignore the Data Not Available bit by clearing its Interrupt Enable.

2. Following any necessary handshaking procedure and the assertion of Send, the program loads the Sync Register with the Sync character and asserts Data Not Available Interrupt Enable. The program then clears the Transmitter Done Interrupt Enable (if it was set) and then loads TxDBUF with the Sync character. At this point, transmission begins. No interrupt request will be generated by the transmission of the first character unless the Transmitter Done Interrupt Enable bit is set. The first bit of the second character will cause an interrupt request. At this point, one Sync character has been transmitted. It is suggested that a minimum of five Sync characters be transmitted. In systems that are prone to error because of lost synchronization, as many as twelve Sync characters may be desired.

If more than one Sync character is required to achieve synchronization, the Data Not Available Interrupt requests can be monitored by the program. These requests will be continuous as long as the Transmitter Done bit goes unserviced and the Data Not Available Interrupt Enable bit is asserted.

Once synchronization has been established, subsequent synchronization can be maintained by delaying service of Transmitter Done and monitoring the Data Not Available bit.

Once synchronization is achieved, transmission of text will follow only if the program loads the text into the TxDBUF.

An intrinsic feature of the DU11 is its ability to maintain synchronization even if the TxDBUF has not been updated. This is done by the transmitter idling out the contents of the Sync Register if the TxDBUF has not been updated in $1/\text{Baud} \times (\text{bits per character} - 1/2 \text{ bit time})$ seconds).

This means that if the transmitter were not serviced in the previously stated time frame, transmission would include data from the Sync Register. If this situation occurs, the Data Not Available bit will be set in the

DU11

TxCSR. If desired, the program may set the DNA INTR EN bit and cause interrupt requests when Data Not Available comes true.

NOTE

The Send bit in the TxCSR must remain set for the duration of the message. An on-to-off transition will cause the transmitter to enter an idle state after completion of the character currently being transmitted.

Synchronous Mode—Receiver Section

The Receiver Section of the DU11 performs serial-to-parallel conversion of 5, 6, 7, and 8-level codes.

SYNC INTERNAL MODE

The Parameter Control Register (PARCSR) controls both the transmitter and receiver configurations. Once the program has completed any necessary handshaking with the data set, the receiver data handling logic can be enabled. This is done by the program asserting Search Sync in the Receiver Status Register (RxCSR). This also enables the receiver to compare incoming characters with the character held in the Sync Register.

For the receiver to become synchronized with the transmitter, either one or two consecutive Sync characters must be recognized by the receiver. The number of characters is jumper selectable.

NOTE

Standard configurations will be set for two characters.

When this has happened, the Receiver Active bit will assert. Any characters received after Receiver Active has been asserted will cause interrupt requests, providing Receiver Interrupt Enable is set and the Strip Sync bit is not asserted.

NOTE

Search Sync must remain set for the duration of the message. If not, the character being received at the time of the on-to-off transition will be lost along with synchronization.

In some instances, the user may want the receiver to ignore Sync characters. This can be accomplished, providing the Receiver Active bit is set. First, the Sync character must be loaded into the Sync Register; then the Strip Sync bit in the RxCSR must be asserted. No interrupt requests will be generated when this character is received, although it does appear in the RxDBUF until the next character is received. If bit 15 of the Receiver Data Buffer (RxDBUF) is asserted (signifying an error), the received Sync character will not be stripped and the RxDone bit will be asserted.

Overrun errors will occur in the receiver logic if the Receiver Done bit in the Receiver Status Register (RxCSR) is not serviced in $1/\text{Baud} \times (\text{bits})$

DU11

per character) seconds. When the overrun condition occurs, the character previously in RxDBUF is written over by the character causing the overrun.

SYNC EXTERNAL MODE

In this mode, the Parameter Control Register must be set for SYNC EXTERNAL. Refer to the description of the Mode Select bits for the actual setting. When the SYNC EXTERNAL mode has been selected, only the operation of the receiver logic differs; transmitter operation remains the same as described above. This is the only mode of operation in which the programs can force synchronization.

When the programmer asserts Search Sync, the Receiver Active bit will also assert even though no actual Sync characters have been received. If Search Sync is cleared, Receiver Active will also be cleared. Prior to the assertion of Search Sync the Receiver Data Buffer (RxDBUF) will appear as the serial line; that is, data will shift through the RxDBUF at the rate of the modem. No action in the receiver logic will result from this data being shifted, although the program can monitor this data stream. When the Search Sync bit is asserted, the receiver logic will start framing characters on the first bit received after Search Sync was asserted. The serial streams that appeared in the RxDBUF will be discontinued, and the Receiver Done bit will be asserted when the selected number of bits have been received. The received character will appear in the RxDBUF. Other than the differences mentioned, all other parameters and features of the synchronous receiver are applicable.

PROGRAMMING

The five registers and their addresses are listed below:

1. Receiver Status Register (RxCSR)	16XX10
2. Receiver Data Buffer Register (RxDBUF)	16XX12
3. Parameter Control Register (PARCSR)	16XX12
4. Transmitter Status Register (TxCSR)	16XX14
5. Transmitter Data Buffer Register (TxDBUF)	16XX16

All information between the DU11 and the PDP-11 CPU is transmitted in parallel fashion by byte or word. The RxCSR and TxCSR are addressable by word or byte. The PARCSR is write only by word operation. The RxDBUF is read only by word or byte. The TxDBUF is write only by word or byte to the even address only.

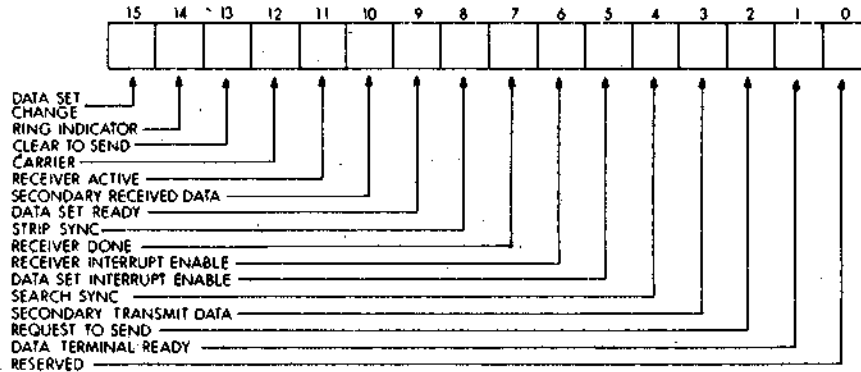
Data transfer is under program control. All data is transferred by the program (not an NPR device). Four contiguous UNIBUS addresses are required in the floating address area. Two contiguous interrupt vector addresses are required in the floating vector address area. The first vector of the set will have priority over the second if two interrupt requests are made simultaneously. The first vector will deal with conditions in the RxCSR. The second vector will deal with conditions in the TxCSR.

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The initialize signal from the UNIBUS will generate a Master Reset in the DU11. A description of the Master Reset bit and the bit assignments within each register are presented in the remainder of this section.

RECEIVER STATUS REGISTER (RxCSR)

Address: 16XX10 (Addressable by word or byte)



Bit 00 RESERVED

Bit 01 DATA TERMINAL READY

When set, this bit causes the data terminal lead to be asserted to the modem. Auto Dial and Manual call origination: maintains the established call. Auto Answer: allows hand-shaking in response to a ring signal.

This bit is program read/write and is optionally cleared by INIT or Master Reset.

Bit 02 REQUEST TO SEND

When set, this bit causes the Request to Send lead to be asserted at the modem interface.

This bit is program read/write and is optionally cleared by INIT and Master Reset.

Bit 03 SECONDARY TRANSMIT DATA

This bit is connected to the secondary transmit line of the modem. With certain modems, supervisory data can be transmitted over this line at a reduced rate. It can also be used as a control lead; e.g., acknowledgement of messages.

This bit is program read/write and is optionally cleared by INIT or Master Reset.

Bit 04 SEARCH SYNC

SYNC INTERNAL MODE: When asserted to the receiver, this bit causes the receiver to start examining incoming characters for the Sync code held in the Sync Register. After the selected number of Sync characters are recognized, the Receiver Active bit is set. Either one or two Sync characters may be selected. The characters must be contiguous.

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SYNC EXTERNAL MODE: In this mode, the Receiver Active bit will assert at the same time the Search Sync bit is asserted. Character framing will start with the first bit received after Search sync has been asserted; character framing ends after the number of bits per character specified in the word length (select bits of the PARCSR) have been received.

Once Receiver Active is asserted, this bit must stay asserted or synchronization will be lost, and the receiver will go into an idle state.

This bit program read/write and is cleared by INIT and Master Reset.

Bit 05 DATA SET INTERRUPT ENABLE
When set, this bit allows interrupt requests to be made to the receiver vector if the Data Set Change bit is asserted.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 06 RECEIVER INTERRUPT ENABLE
When set, this bit allows interrupt requests to be made to the receiver vector if the Receiver Done bit is set.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 07 RECEIVER DONE
This bit is set when a character is transferred into the Receiver buffer. If, however, the Receiver Active bit is set and the Strip Sync bit is a one, and the character received is a Sync character, the Receiver Done bit will not be set, providing bit 15 of the RxDBUF is clear.

This bit is program read/only and is cleared by reading RxDBUF, INIT, and Master Reset.

An Interrupt request will be generated if the Receiver Interrupt Enable bit is set when this bit is asserted.

Bit 08 STRIP SYNC
When this bit is set, characters that match the contents of the Sync Register will be ignored, provided bit 15 of the Receive Data Buffer Register is not asserted. In this case, the Receiver Done bit will not be asserted.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 09 DATA SET READY
This bit is a direct reflection of the Data Set Ready (or interlock) lead emanating from the modem. This line, when asserted, indicates that the modem is powered up, and is not

DU11

in the test, talk, or dial mode. Any transition of this bit will cause the Data Set Change bit to be asserted.

Program read only.

Bit 10 **SECONDARY RECEIVED DATA**
This bit reflects the state of the Secondary Received Data line emanating from the modem. Any transition on this line will cause the Data Set Change bit to assert. With certain modems, supervisory data can be received over this line at a reduced rate. It can also be used as a control lead; e.g., acknowledgment of messages.

Program read only.

Bit 11 **RECEIVER ACTIVE**
When operating in the synchronous mode using internal synchronization, this bit will be set when the selected number of contiguous Sync characters have been recognized (either 1 or 2). If the Sync EXTERNAL mode were selected, the Receiver Active bit will follow the state of the Search Sync bit.

This bit is program read and is cleared by INIT and Master Reset.

Bit 12 **CARRIER**
This bit is a direct reflection of the modem carrier. Any change in the status of this line causes the Data Set Change bit to be asserted.

Program read only.

Bit 13 **CLEAR TO SEND**
This bit reflects the state of the clear-to-send line of the modem. Any transition of this line causes the Data Set Change bit to set.

Program read only.

Bit 14 **RING INDICATOR**
This bit reflects the state of the modem ring line. Any transition of this line causes the Data Set Change bit to set.

Program read only.

Bit 15 **DATA SET CHANGE**
This bit is set by a transition on the following lines:

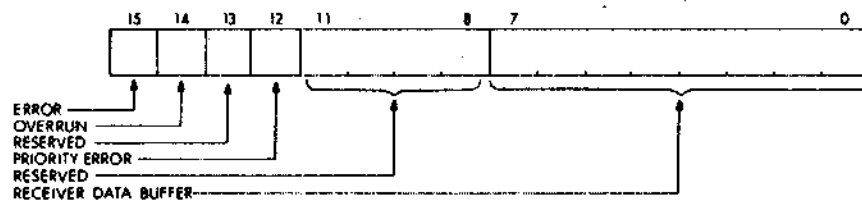
- Any transition on the Ring line.
- Any transition on the carrier line.
- Any transition on the Data Set Ready line.
- Any transition on the Clear-to-Send line.
- Any transition of the Secondary Received Data.

DU11

If bit 05 of this register is set, the assertion of this bit will cause an interrupt to the receiver vector. This bit is cleared only by INIT, Master Reset, or when the RxCSR is read.

RECEIVER DATA BUFFER REGISTER (RxDBUF)

Address: 16XX12 (Read Only—Addressable by word or byte)



Bits
00-07

RECEIVER DATA BUFFER

This buffer contains the data received from the modem with character lengths from 5-to-8 bits, plus parity if selected. The parity bit, if any, will be included as part of the received character and will appear as the bit following the most significant bit. In the case of 8-bit characters, no parity bit will be displayed.

The character in the RxDBUF is right-hand adjusted; bit 00 is the least significant bit of any character, and bit 07 is the most significant bit of an 8-bit character.

Subsequent to a Master Reset, this register contains all ones.

Program read.

Bits
08-11

RESERVED

Bit 12

PARITY ERROR

This bit is set when the receiver detects a parity error in the character received. The character will appear in the RxDBUF. The parity bit itself is available to the program for character length selection for less than 8 bits per character.

This bit is program read and is cleared by INIT, Master Reset, and by reading the RxDBUF low byte.

Bit 13

RESERVED

Bit 14

OVERRUN

When the receiver logic detects an overrun condition, this bit is set. An overrun is caused primarily by poor program response time.

Once the Receiver Done bit is set, the program must respond in $1/\text{BPS} \times (\text{Bits per character})$ seconds. If not, overrun will occur. This condition indicates the loss of at least one character. This bit will cause the error bit to assert.

DUI1

This bit is program read only and is cleared by reading the RxDBUF low byte, INIT, or Master Reset.

Bit 15

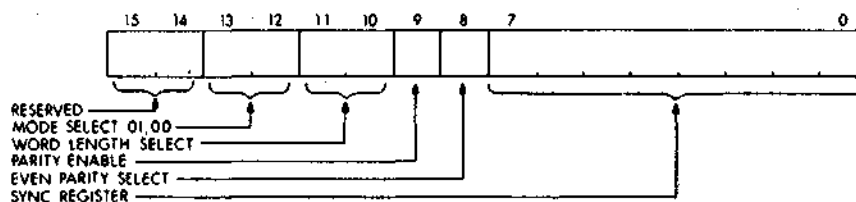
ERROR

This bit will be asserted if one of the three error bits in the RxDBUF are set (logical OR of bits 14 and 12).

This bit is program read only and is cleared only when bits 14 and 12 are clear.

PARAMETER CONTROL REGISTER (PARCSR)

Address: 16XX12 (Write only—addressable by word only)



NOTE:

If this register is inadvertently addressed with a byte operation, both bytes of the UNIBUS will be loaded. The unspecified byte may contain unwanted data.

The following bits are used to control the characteristics of the interface. These include mode of operation (synchronous internal or synchronous external), number of bits per character, and parity selection. These bits are in an undefined state after power-up until programmed.

Bits

00-07

SYNC REGISTER

This register contains the Sync character to be transmitted and used for receiver synchronization by the interface. The length of this character must correspond to the length of the data character. Parity does not have to be included if it has been selected.

Subsequent to a master reset, the internal transmitter Sync register will contain all ones; the receiver's internal Sync register will contain all zeros.

Character length is adjusted from right to left, with bit 00 being the least significant bit and bit 07 the most significant bit for an 8-bit character.

Program write only.

Bit 08

EVEN PARITY SELECT

When the Parity Enable bit (bit 09) is set, the sense of the parity is controlled by this bit. When set, even parity will be

DU11

generated by the transmitter and checked for by the receiver. The same will be done for odd parity when cleared.

Program write.

Bit 09 PARITY ENABLE

If this bit is set, parity generation and checking will be done. If bad parity is detected at the receiver, then the parity error flag will be set in the upper byte of the Receiver Data Buffer Register (RxDBUF).

Program write.

Bits 10 & 11

WORD LENGTH SELECT

These bits are used to select the number of bits per character, either 5, 6, 7, or 8. This selection does not include the parity bit, if parity is selected.

Bits Per Character	PARCSR 11	Bit 10
5	0	0
6	0	1
7	1	0
8	1	1

Program write.

Bits 12 & 13

MODE SELECT 01, 00

The function of these bits is to select the mode of operation: synchronous internal or synchronous external. The following table shows the legal configurations possible with the DU11. All other combinations of the mode select bits will produce errors in the interface.

MODE	PARCAR 13	Bits 12
Synchronous External	1	0
Synchronous Internal	1	1

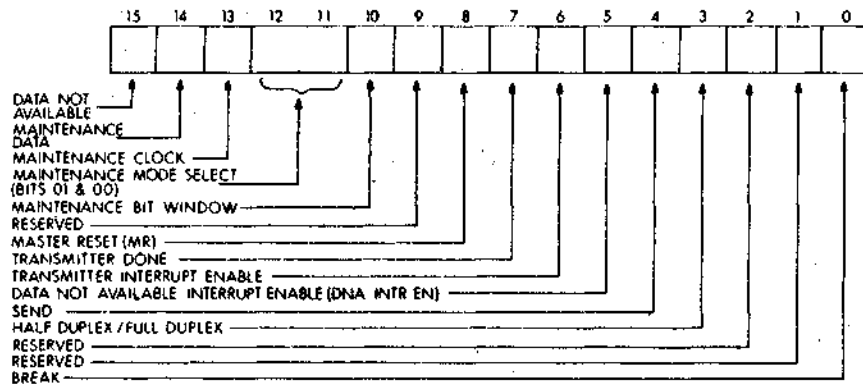
Program write.

Bits 14 & 15

RESERVED

TRANSMITTER STATUS REGISTER (TxCSR)
 Address: 16XX14 (Addressable by word or byte)

DU11



Bit 00 BREAK
 When this bit is asserted, the serial output of the transmitter is held in the space condition. If the program presents data to the transmitter during this period, the operations to the program will appear normal. An interrupt request will be generated at the normal time even though a character was never actually transferred.

NOTE:

The setting of this bit is not recommended when operating in the synchronous mode except for maintenance programming.

This bit is program read/write and is cleared by INIT or Master Reset.

Bit 01 RESERVED

Bit 02 RESERVED

Bit 03 HALF DUPLEX/FULL DUPLEX
 When this bit is set, operation will be in the half-duplex mode. In the half-duplex mode, the receiver will be disabled if the Send bit in the TxCSR is asserted.

This bit is read/write and is cleared by INIT or Master Reset.

Bit 04 SEND
 When asserted, this bit enables the transmitter. Once the transmitter is enabled, transmission will start when the first character has been loaded into the TxDBUF. This line must remain true for the length of the entire message. If not, the current character in the shift register will be transmitted, and the transmitter will go into an idle state.

This bit is used in all modes of operation.

This bit is program read/write and is cleared by Master Reset or INIT.

DU11

- Bit 05** **DNA INTR EN (DATA NOT AVAILABLE INTERRUPT ENABLE)**
Allows interrupt requests to be made to the transmitter vector if the Data Not Available bit is set. This bit is set if the user wants to know if a filler character was sent while in data mode via an interrupt or to notify the program when the last bit of a character has been transmitted.
- This bit is program read/write and is cleared by INIT or Master Reset.
- Bit 06** **TRANSMITTER INTERRUPT ENABLE**
When set, this bit will allow a program interrupt request to be generated by the Transmitter Done bit.
- This bit is program read/write and is cleared by INIT or Master Reset.
- Bit 07** **TRANSMITTER DONE**
This bit will be set when the first bit of the character contained in the TxDBUF is presented to the line. At that time, the program can load another character into the transmitter buffer.
- If the transmitter interrupt enable bit is set, this bit will generate an interrupt request to the transmitter vector.
- Program read. Cleared by writing a character into the TxDBUF. Reset by INIT or Master Reset.
- Bit 08** **MASTER RESET (MR)**
This bit is used to place the transmitter and receiver in an idle state (not to be confused with idle mode). The UNIBUS Initialize signal will also place the DU11 in an idle state.
- When the transmitter is placed in an idle state, the following conditions exist:
1. All internal timing is reset.
 2. The contents of the Sync register, internal to the transmitter, will be all ones.
 3. All the bits in the TxCSR may be reset except the Transmitter Done bit which will be set.
 4. The TxDBUF will contain all ones.
- When the receiver is in an idle state, the following conditions exist:
1. All internal timing is reset.
 2. The contents of the Sync register, internal to the receiver, will be all zeros.
 3. The following bits in the RxCSR will be cleared:

DU11

Data Set Change
Receiver Active
Strip Sync
Receiver Done
Receiver Interrupt Enable
Data Set Interrupt Enable
Search Sync

The following bits of the RxCSR may be optionally excluded from the bits cleared by a Master Reset or INIT signal:

Secondary Transmit Data
Request to Send
Data Terminal Ready

If the user decides to connect the option jumper to clear the above bits, then all of these bits will be cleared. The DU11 is shipped with this jumper in.

The contents of the RxDBUF will be all ones in the low byte. In the high byte, the Error, Overrun, Frame Error, and Parity Error bits will be cleared.

The contents of the high byte in the Parameter Control Register (PARCSR) will be unaffected by the Master Reset.

Immediately after power-up, these bits will be in an undefined state.

NOTE:

This bit is one-shot; that is, it will be asserted for 6 μ sec and then return to the zero state.

Bit 09 RESERVED

Bit 10 MAINTENANCE BIT WINDOW

When in the maintenance mode 01 or 00, this bit can be used to monitor the input to the receiver logic. The stimulus that creates the input could be either the Maintenance Data bit or the serial output of the transmitter, depending on the state of the Break bit.

Program read only.

Bits
11 & 12

MAINTENANCE MODE SELECT (BITS 01 & 00)

These bits are used to select anyone of three maintenance modes:

	BIT SETTING	
	12	11
1. Internal Maintenance Mode	0	1
2. External Maintenance Mode	1	0
3. Internal Maintenance Mode for Systems Testing	1	1

DU11

INTERNAL MAINTENANCE MODE (01)

Internal maintenance mode clocking comes from the Clock bit (bit 13) driven via the program. While using this mode, the following EIA level converters are disabled (this is done so that the majority of the logic can be diagnosed without disconnecting the modem cable):

- Receiver Clock
- Transmitter Clock
- Receiver Data
- Transmitter Data

Modem control flags should be cleared and not used in this mode. All inputs that were driven by the modem will now be simulated by the program setting the appropriate flags. The function of the half-duplex bit in the TXCSR cannot be tested in this mode. The external maintenance mode must be used to test this function.

EXTERNAL MAINTENANCE MODE (10)

When in the external maintenance mode, all lines connected to the data set must be removed at the data set interface. A special connector replaces the connector of the data set. The function of the special connector is to turn around specified signals after level conversion and bring them back to the DU11 as simulated inputs.

The test loop back connector to be used is the H315 connector.

Clocking in this mode is under control of the maintenance clock bit. Refer to clock bit description for its characteristics.

This is the only mode that can be used to check out the function of the Half-Duplex bit.

INTERNAL MAINTENANCE MODE FOR SYSTEMS TESTING (11)

With bits 12 and 11 both set to a one (mode 11), the internal maintenance mode provides an adequate method of clocking the receiver and transmitter. The clocking method should not be synchronous to the program. An RC clock is provided in the interface for this purpose. Mode 11 will be the same as mode 01 with respect to data set control lines. The only difference is that Receiver and Transmitter clocking is derived from an RC clock at 3 kC.

NOTE:

If bits 12 and 11 are zero, normal operating mode is assumed.

These bits are program read/write and are cleared by INIT or Master Reset.

DU11

- Bit 13** **MAINTENANCE CLOCK**
This bit is used to simulate the Transmitter and Receiver clock. It is used for diagnostic purposes only. With this bit, the diagnostic has the ability to single step the interface. A 0-to-1 transition of this bit causes the transmitter to transfer a bit from the internal shift register to the output of the transmitter.

A 1-to-0 transition of this bit causes the receiver to transfer the input of the receiver into the internal shift register.

This bit is program read/write and is cleared by INIT or Master Reset.
- Bit 14** **MAINTENANCE DATA**
This bit is used only in the maintenance mode by the diagnostic program. In either maintenance mode 01 or 10, this bit can be used to simulate data at the receiver input. When used as a simulated input to the receiver, the Break bit must be set to inhibit additional input from the transmitter. This bit should be cleared if it is not being used as the simulated input. If this bit were inadvertently set in maintenance mode and the Break bit was clear, the receiver input would have two sources of input.

This bit is program read/write and is cleared by INIT or Master Reset.
- Bit 15** **DATA NOT AVAILABLE**
This bit is set by the transmitter logic when a character is transmitted from the Sync register. This applies only to synchronous operation and is caused by late or no program response.

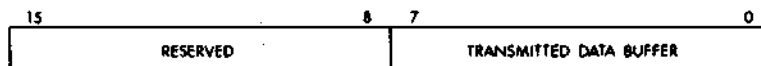
The program response to the Transmitter Done bit must be within $1/\text{Baud} \times (\text{bits per character}) - 1/2$ bits per second. If not, a character from the Sync register will be transmitted.

If the Data Not Available Interrupt Enable bit is set in the TxCSR, it will cause an interrupt to the transmitter interrupt vector.

This bit is program read and is cleared by reading the TxCSR, INIT, and Master Reset.

TRANSMITTER DATA BUFFER REGISTER (TxDBUF)

Address: 16XX16 (Addressable by word or byte to the even address only)



DU11

Bits
00-07

TRANSMITTER DATA BUFFER

This register is loaded by the program with the character to be transmitted. Character length is from 5 to 8 bits. The character is right-hand adjusted, with bit 00 being the least significant bit of any character and bit 07 the most significant bit of an 8-bit character. Any parity bit required is generated by the interface.

Subsequent to a Master Reset or INIT, this register will contain all ones.

Program write.

Bits
08-15

RESERVED

CONTROL LEADS

The modem control leads are provided to interface the DU11 to Bell series 200 synchronous modems or equivalent. These leads allow the DU11 to be used in switched or dedicated, full- or half-duplex configurations.

The DU11 is connected to a Bell model 201 synchronous modem (or equivalent) by a 7.6m (25-foot) cable terminated at the modem end with a 25-pin male connector. Interface signals versus connector pin assignments are given below.

PIN	SIGNAL
1	Signal or Protective Ground
2	Send Data
3	Receive Data
4	Send Request
5	Clear to Send
6	Interlock
7	Signal Ground
8	Carrier On-Off
15	Serial Clock Transmit
17	Serial Clock Receive
20	Data Terminal Ready
22	Ring Indicator 1
24	External Timing

SPECIFICATIONS

Function

Provides an interface between the PDP-11 UNIBUS and a single synchronous bit serial communications channel.

Mechanical

The DU11 consists of one quad (8½" x 10½") etched circuit card, and a 25-foot connecting cable terminated in a plug appropriate to the data communications equipment to be connected.

DU11

Operating Mode

Full- or half-duplex under program control.

Environmental

+10 to +50°C with a relative humidity of 20% to 95% (without condensation).

Power Requirements

+5 V at 2 A

-15 V at 0.15 A

+15 V at 0.05 A

UNIBUS Loads

The DU11 presents one unit load to the PDP-11 UNIBUS.

ORDERING INFORMATION

DU11-DA Full/half duplex synchronous line module set. Double buffered, 5, 6, 7, or 8-bit characters. EIA/CCITT termination suitable for use with Bell series 200 synchronous modems or equivalent. Includes 7.6-m (25-foot) modem cable.

DFC11-A* Clock option for the DU11-DA

APPLICATIONS

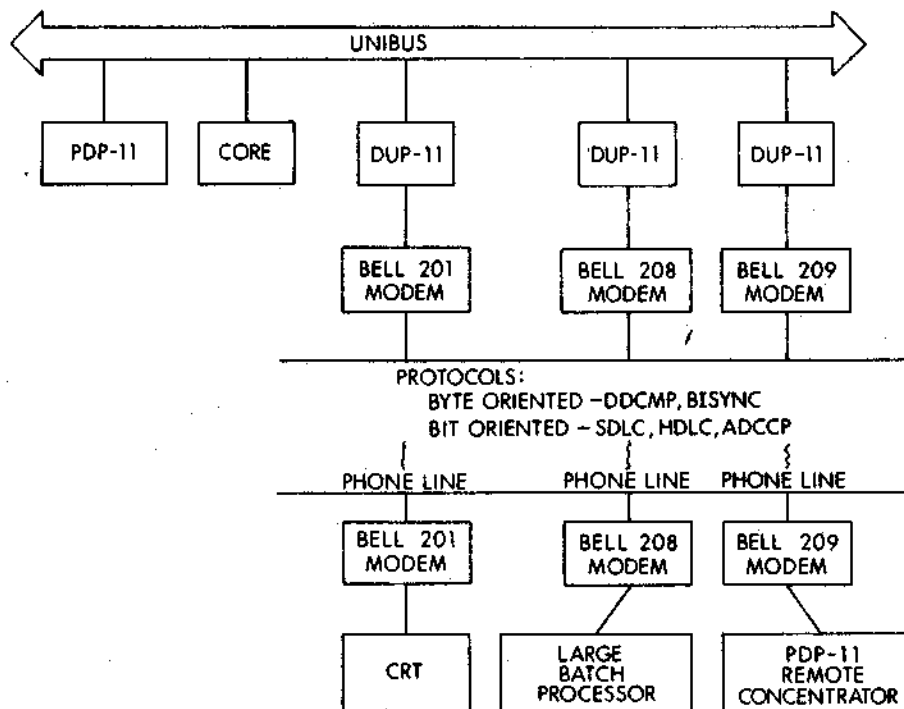
Applications for high-speed synchronous communications interfaces vary widely, and new applications are being developed every day. These applications span all user groupings—commercial, industrial, scientific, and government.

Functionally, these applications may be divided into a few fundamental classes, such as:

- **REMOTE DATA COLLECTION.** Gathering information at a number of remote locations and transmitting it to a central processing point.
- **REMOTE BATCH PROCESSING.** The processing of batch or production jobs at a location remote to where the job is generated and the results are needed.
- **REMOTE CONCENTRATION.** Multiple DU11's connected to a PDP-11 enable it to be used as a synchronous line concentrator or front-end synchronous controller to a larger computer. The concentrator helps reduce line costs by concentrating data from several lines onto one high-speed line.
- **COMPUTER-TO-COMPUTER COMMUNICATIONS.** The DU11 can be used to connect two PDP-11's together or a PDP-11 to another larger processor (e.g., an IBM 360). Intercomputer communication is used in such applications as load sharing, data base sharing, and remote job entry. It permits more effective utilization of the interconnected computers because the slack time in one computer's schedule can be used to help smooth out the peaks in another's.
- **ON-LINE TERMINAL PROCESSING.** The DU11 can connect a wide variety of remote terminals to the PDP-11.

* When clock option is used, DU11-DA and DFC11-A must be mounted in one of the two center slots of a DD11-8 peripheral mounting unit.

SYNCHRONOUS LINE INTERFACE, DUP11



FEATURES

- Transmission speeds up to 9600 baud
- Double-character-buffered receive & transmit
- Full- or half-duplex operation
- Byte-oriented operation (protocols such as DDCMP and BISYNC)
- Bit-oriented operation (protocols such as SDLC, HDLC, ADCCP)
- CRC-16 generation and checking for use with DDCMP protocol
- CRC/CCITT generation and checking for use with bit-oriented protocols
- Programmable SYNC character for byte-oriented operation
- Secondary address recognition for bit-oriented operation
- 8-bit character size
- SYNC stripping on receive operations under program control
- Interfaces to Bell 201, 208, and 209 series synchronous modems or equivalents
- Auto answering capability
- Modem control
- Simple, compact single-board design (i.e., SPC slot UNIBUS option)

DUP11

INTRODUCTION

The DUP11 is a single-line, program-controlled, double-buffered communications device designed to interface the PDP-11 processor to a serial synchronous line. The self-contained unit is capable of handling a wide variety of protocols, including byte-oriented protocols, such as DDCMP and BISYNC and bit-oriented protocols, such as SDLC, HDLC and ADCCP.

The DUP11 is ideally suited for interfacing the PDP-11 to medium-speed synchronous lines for remote batch, remote data collection, remote concentration and network applications. Multiple DUP11's on a PDP-11 allow its use in applications requiring several synchronous lines.

The DUP11 provides serial-to-parallel and parallel-to-serial data conversion, voltage level conversion, and modem control for half or full-duplex operation. The Bell Series 200 synchronous modems or equivalent may be used with the DUP11.

Modem control is a standard feature of the DUP11. The necessary signals needed to establish communications with the Bell Series 200 synchronous modems are present in the Receive Status Register (RxCSR). A transition of control lines emanating from the modem directly will not cause a change in the state of the transmitter or receiver logic.

The DUP11 is capable of transmitting data at the maximum speed of 9600 baud (limited by modem and data set interface level converters).

The DUP11 conforms to Electronic Industries Association (EIA) specification RS232C and CCITT Recommendation V.24.

DESCRIPTION

The DUP11 is a character-buffered, synchronous, serial-line interface capable of two-way simultaneous communications. The DUP11 translates between serial data and parallel data. Output characters are transferred in parallel from the PDP-11 UNIBUS into the DUP11 where they are serially shifted to the communication line. Input characters from the modem are shifted into the DUP11 and made available to the PDP-11 on an interrupt basis.

This allows a full character time in which to service transmitter and receiver interrupts. The clocking necessary to serialize the data is provided by the associated synchronous modem.

The DUP11 contains five registers: two status registers, two data buffer registers, and a Parameter Status Register.

SPECIFICATIONS

Function

The DUP11 provides an interface between the PDP-11 UNIBUS and a single, synchronous, bit-serial communications channel. It is capable of

DUP11

handling a wide variety of protocols, including bit-oriented protocols (such as SDLC, HDLC, ADCCP).

Mechanical

The DUP11-DA consists of one hex-size (15³/₄ inch x 8³/₈ inch) module, a 16 inch flat ribbon cable, and a 25 foot (7.6 meters) connecting cable. It requires one slot in a DD11-B mounting panel or equivalent. Only slots 2 and 3 of the DD11-B can be utilized with this device. Two DUP11-DAs can be mounted in one DD11-B.

Operating Mode

The DUP11 operates in half- or full-duplex mode, under program control.

Environmental

Temperature: +10 degrees C to +40 degrees C.

Relative Humidity: 10% to 90%

Power Requirements

+ 5V @ 3.6A

+15V @ 0.325A

-15V @ 0.6A

The DUP11 presents one unit load to the PDP-11 UNIBUS.

Ordering Information

DUP11-DA Full/half duplex synchronous-line module set. EIA/CCITT termination suitable for use with Bell Series 200 synchronous modems or equivalent. Supplied with 25-foot modem cable.

Prerequisite: DD11-B system unit, (slots 2 or 3 only).

DUP11 OPERATION

The operation of the DUP11 depends on whether it must handle a byte-oriented protocol, such as DDCMP or BISYNC, or a bit-oriented protocol, such as SDLC, HDLC, or ADCCP. This is determined by bit 15 (DEC MODE) of the Parameter Status Register.

The transmitter operation of the DUP11 performs parallel-to-serial conversion of 8-bit bytes supplied to it from the PDP-11 UNIBUS and optionally calculates and sends CRC-16 block check characters.

After the initialize or device reset pulse, the program must set the DEC MODE bit in the Parameter Status Register (PARCSR) to indicate that a byte-oriented protocol is in use. The program should also specify if CRC calculation is desired and set the CRC INHIBIT bit of the PARCSR register if not desired. For byte-oriented operation, the DUP11 uses the CRC-16 polynomial:

$$(X^{16} + X^{15} + X^2 + 1)$$

Protocols such as DDCMP can make efficient use of the DUP11 CRC capability. These protocols are characterized by the fact that all characters within the message are included in the CRC. For other byte-

DUP11

oriented protocols such as BISYNC, the CRC capability of the DUP11 must usually be inhibited.

Before transmitting, any necessary handshaking with the data set should be completed. Once this has been done, the program can enable the transmitter by setting the SEND bit of the Transmitter Status Register (TxCSR).

The program begins transmission by loading the desired SYNC character into the Transmitter Data Buffer Register (TxDBUF) and setting the TSOM bit. All transmitted SYNC characters must be loaded into the TxDBUF.

When TxDONE is set after the last SYNC character has been loaded, the program should load the first data character into the TxDBUF and clear the TSOM bit. This character and all subsequent data characters will be included in the CRC calculation.

The accumulated CRC check characters are transmitted by setting the TEOM bit. When the data character currently being transmitted is complete, the CRC check characters will be sent (unless inhibited). The TxDONE bit of the Transmitter Status Register (TxCSR) will be set at the start of transmission of the CRC check characters if the program has not cleared the SEND bit. The TxDONE bit can be cleared by again setting TEOM, or additional data characters can be sent by loading the first one into TxDBUF and clearing TEOM. SYNC characters can be idled by loading a SYNC character into TxDBUF, clearing TEOM and setting TSOM.

If the program wishes to idle the serial line to a mark, it should clear SEND immediately after setting the TEOM bit. In this case the TxDONE bit will not set until the entire CRC has been sent and the line has gone to the mark state for $\frac{1}{2}$ bit time.

The transmitter CRC register is initialized to zeros by the initialize pulse and by device reset. It is also held in the zero state by logic synchronized to the TSOM bit. It will be held in this state until the last character associated with TSOM has been transmitted. When the CRC has been sent in response to TEOM, the CRC register will be zero.

The DUP11 does not automatically idle SYNC characters if the transmitter data buffer is not serviced in time. Instead, the line will be held in the mark state. The DUP11 signals the error condition by setting the TxDAT LATE bit in the TxCSR. The TxDAT LATE bit is cleared by setting TSOM. While TSOM is true, TxDAT LATE will not set and the program can idle multiple SYNC characters without program intervention by disabling interrupts at this time. The DUP11 is double-buffered and the program has at least one character time to respond to the setting of TxDONE. The time available can be calculated according to the formula:

$$7.5 (1/\text{bits per second}) \text{ seconds}$$

DUP11

Byte-Oriented Operation—Receiver

The receiver operation of the DUP11 performs serial-to-parallel conversion of 8-bit bytes and optionally calculates and checks the CRC-16 block check characters.

After the initialize or device reset pulse, the program must set the DEC MODE bit of the PARCSR and set the CRC INHIBIT bit of the PARCSR if it does not wish the DUP11 to perform CRC verification. These bits affect both the transmitter and receiver. In addition, the program must load the desired SYNC character into the PARCSR. This SYNC character affects only the DUP11 receiver.

Before enabling the receiver, any necessary handshaking with the data set should be completed. Once this has been done, the program can enable the receiver by setting the RCVEN bit in the Receiver Status Register (RxCSR). Setting RCVEN causes the receiver to search the data stream for two consecutive SYNC characters. When two successive SYNCs have been recognized, the receiver is considered synchronized and subsequent information will be assembled as 8-bit characters.

Whenever a character is assembled, it will be transferred into the Receiver Data Buffer Register (RxDBUF). If the character is not a SYNC character, or if a non-SYNC character has been assembled subsequent to receiver resynchronization, then RxDONE will be set. If the character is a leading SYNC character, then RxDONE will be set unless the STRIP SYNC bit of the RxCSR is set. The program can bypass leading SYNC characters by setting STRIP SYNC.

Until RxDONE sets for the first time subsequent to receiver re-synchronization the receiver CRC register will be zero and the RxACT (receiver active) bit of the RxCSR will be clear. Upon assembling the first character to be presented to the program, RxACT and RxDONE will be set together. This character and all subsequent characters will be included in the receiver CRC calculation.

The RCRC ERROR + ZERO bit of the RxDBUF will be set whenever the receiver CRC calculation for characters up to and including the character in the RxDBUF has resulted in a zero result and the CRC INHIBIT bit in the PARCSR is clear. The program can check for a valid CRC by examining this bit when two characters, in addition to the data characters, have been assembled. The program should ignore this bit at other times. It is entirely possible that this bit may set during the middle of a message should the CRC register happen to assume a zero value at some point.

The program can shut down the receiver by clearing RCVEN. This will clear RxDONE, RxACT, the receiver data buffer, and the receiver CRC register and will disable the receiver. The program can force the DUP11 receiver to resynchronize by clearing RCVEN and then setting it.

DUP11

The program must respond to the RxDONE bit by reading the RxDBUF within one character time. If this is not done, the OVRUN ERR (over-run error) bit in the RxDBUF will set and the contents of the data buffer will contain the most recently received character. Any previous character(s) will be lost.

Bit-Oriented Protocol Message Formats

The DUP11 can operate with bit-oriented protocols such as IBM's SDLC protocol, ISO's HDLC protocol, and ANSI's ADCCP protocol. All these protocols use a particular 8-bit sequence, 01111110, called a FLAG, to mark the beginning and end of variable length messages, called frames, and thereby establish synchronization. Information between FLAGS is dependent on the protocol used, but typically consists of address and control information, user data, and block check characters (Fig. 1). These protocols place no restriction on the information between FLAGS.

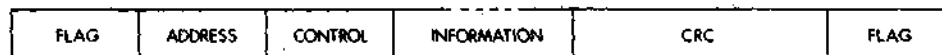


Figure 1. Frame Format

To ensure that a particular data sequence is never mistaken for a FLAG, a technique known as bit-stuffing is used on the information between FLAGS. Whenever five consecutive one bits have been sent, the transmitter inserts a zero bit into the data stream. When the five one bits followed by the zero bit are recognized by the receiver, the receiver removes the inserted zero bit. By this technique, any user-data pattern can be sent and received with no danger of its being mistaken for a FLAG character (Fig. 2). In principle, this technique can be used with frames any number of bits long. However, the DUP11 is restricted to operation with frames which are some number of 8-bit characters in length.

```
..011111001111101100...   user data bits
..011111000111110101100..  data on communication line
  stuffed bit   stuffed bit
..011111 001111 101100...   decoded user data
  stuffed bit removed
```

Figure 2. Example of Bit Stuffing

When one frame has been completed, another can follow immediately, sharing a single FLAG character. Alternatively, the communication line can be held active by sending multiple FLAG characters. If it is desired to shut down the line, the line can be idled to the mark state.

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Sometimes it is desired to abort a frame being transmitted. This can be done by sending an incorrectly formed frame, i.e., one containing seven or more consecutive one bits. The DUP11 transmitter can send a sequence of eight consecutive one bits, called an ABORT to indicate this condition. Following an ABORT, one or more FLAGs can be sent, or the line can be idled to the mark state. There is no danger that user information will be mistaken for an ABORT because of bit-stuffing.

For multipoint operation, secondary stations are distinguished by their addresses. A secondary station must accept and process only frames addressed to it. The DUP11 receiver contains logic to hold a secondary address and compare this address with the first character of a frame. For operation as a secondary station, the DUP11 will skip over all characters in frames intended for other stations, eliminating unnecessary program overhead. This feature can be disabled for operation as a primary station or with protocols which do not use the first character of a frame as an address.

The DUP11 does not process the control or information fields of a frame. These are treated as 8-bit characters and are passed to the program.

Most bit-oriented protocols use a 16-bit CRC block check, calculated according to the CRC/CCITT polynomial:

$$(X^{16} + X^{12} + X^5 + 1)$$

The CRC field is the last field of the frame.

The transmitter uses a 16-bit register to calculate CRC. The transmitter initializes the register to all ones prior to the start of the frame. The transmitter calculates the CRC on all data bits (not stuffed bits) beginning immediately following the FLAG and ending immediately prior to the block check field. The transmitted CRC is the complement of the register contents at the end of the calculation.

The receiver performs a similar calculation, using a separate 16-bit register. The receiver initializes this register to all ones and calculates the CRC on all data bits between the FLAGs (including the transmitted CRC). The receiver then checks for a special value that compensates for transmitting the complement of the calculated CRC. If the special value is not seen, an error is indicated.

The DUP11 CRC logic can be inhibited for protocols that do not use this method of generating and checking a block check. If the CRC logic is inhibited, any block checks will be treated as data by the DUP11 and are the responsibility of the program.

Bit-Oriented Operation—Transmitter

The transmitter section of the DUP11 generates FLAG and ABORT sequences, performs parallel-to-serial conversion of 8-bit bytes supplied to it from the PDP-11 UNIBUS, and optionally generates and sends the CRC/CCITT block check characters. Whenever the data stream between two FLAGs contains five consecutive one bits, the transmitter logic auto-

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matically inserts a zero bit to distinguish data and block check characters from FLAG and ABORT sequences.

After the initialize or device reset pulse, the program should clear the DEC MODE bit in the PARCSR. The program should also specify if CRC calculation is desired and set or clear the CRC INHIBIT bit of the PARCSR as desired. The DUP11 calculates and sends the block check characters as described above. For protocols calculating the block check differently, the CRC capability of the DUP11 should be inhibited and the program should generate the required block check characters.

Before transmitting, any necessary handshaking with the data set should be completed. Once this has been done, the program can enable the transmitter by setting the SEND bit of the TxCSR.

The program begins transmission by setting the TSOM bit in the TxDBUF. This initial access momentarily clears the TxDONE bit, which was initially set by the initialize pulse or reset. The transmitter will remain inactive for a period equal to two bit times and then the transmitter will become active. The TxACT (transmit active) and TxDONE bits will be set and a FLAG sequence will begin on the serial line.

Some devices that communicate with the DUP11 require that sixteen 0 bits precede the FLAG character beginning the first frame sent after enabling the transmitter. To accommodate these devices, the program should set TEOM together with TSOM immediately after setting the SEND bit. TxDONE and TxACT will set when the 0 bit sequence begins. When TxDONE sets for the first time the program should respond by clearing TEOM. This will clear TxDONE. TxDONE will set again when the sixteen 0-bits have been sent and a FLAG character has begun. Note that TEOM and TSOM can be used this way only immediately after the transmitter has been enabled.

If it is desired to send an additional FLAG, the program can clear TxDONE by accessing the TxDBUF and leaving TSOM set. TxDONE will set when the additional FLAG has begun. The program can send any desired number of FLAGS by counting.

When TxDONE has set as the last desired FLAG has begun, the program should clear TSOM and write the first character of the frame into the TxDBUF. Note that the DUP11 transmitter will not automatically send an address character, even in secondary address mode.

Writing a character into the TxDBUF will clear TxDONE. TxDONE will set again when the current character or sequence has been sent on the serial line and the new character has begun. The TxDBUF should be accessed only in response to TxDONE.

The program should write successive characters of the frame into the TxDBUF in response to TxDONE. This must be done within one character time or the TxDAT LATE bit will set in the TxCSR indicating an error condition. The time available may be calculated according to the following formula:

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$(1/\text{bits per second}) * (7.5 + n)$ seconds
where n is the number of bits stuffed (n = 0, 1, or 2)

Should TxDAT LATE set, the DUP11 transmitter will transmit an ABORT sequence on the serial line. Additional ABORTs will be sent until the program sets TSOM to begin a new frame or clears SEND. Clearing SEND will complete the current ABORT and place the line in mark hold.

When the program has loaded the final data character and TxDONE sets to indicate that this character has begun to be sent on the serial line, the program should set TEOM to inform the DUP11 transmitter that the message is complete. Subsequent events depend on whether CRC calculation is inhibited and whether the program wishes to send an additional frame following the terminating FLAG, or wishes to idle FLAGS, or marks.

If the program wishes to shut down transmission, it should clear SEND as soon as it has set TEOM. In this case, the DUP11 transmitter will complete the current data character, send the two block check characters (unless CRC INHIBIT is set in PARCSR) and send the terminating FLAG. The line will then go to the mark hold state. Setting TEOM clears TxDONE. When the line has been in the mark hold state for one-half bit time, TxACT will clear and TxDONE will set, indicating that the frame has been completely transmitted.

If the program wishes to transmit another frame that immediately follows the current frame and shares a single FLAG character, it should follow one of two procedures. If CRC INHIBIT is set, the program should wait for TxDONE to set indicating that the FLAG character has begun transmission. The program should then clear TEOM and load the first character of the new message into the TxDBUF. The FLAG will complete and then the new message will begin.

If CRC INHIBIT is not set, then the program should wait for TxDONE to set indicating that the block check has begun to be sent. It should then clear TEOM and set TSOM. This will clear TxDONE. TxDONE will set when the FLAG character has begun transmission. The program should clear TSOM and load the first character of the new frame into the TxDBUF. This procedure will correctly initialize the CRC calculation for the new frame.

If the program wishes to idle FLAGS between frames, it should leave TEOM set in response to TxDONE setting. TxDONE will not be cleared if the program does not touch the TxDBUF, so interrupts during the waiting period are avoided. When the program wants to begin a new frame, it should set TSOM. This clears TxDONE, reinitializes the CRC register and initiates the transmission of one additional FLAG. When this FLAG begins, TxDONE will set and the program should load the first data character of the new frame.

The program can count FLAGS by setting TEOM in response to TxDONE. This will clear TxDONE. TxDONE will set again when a FLAG has begun.

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The program can continue to set TEOM and count or clear TEOM and set TSOM to begin a new frame.

In some cases it may be desirable to send one or more ABORT sequences following a terminating FLAG. The program should set the TxABORT bit and clear TEOM when TxDONE sets at the time the FLAG has begun. If CRC INHIBIT is set, this will be the first time TxDONE sets after the program has set TEOM. If CRC INHIBIT is not set, TxDONE will set when the CRC begins. The program should set TEOM to clear TxDONE. TxDONE will set again when the FLAG begins. At this point, the program should clear TEOM and set TxABORT. Setting TxABORT will clear TxDONE. TxDONE will set when the ABORT begins.

If the program wishes to ABORT a frame it is in the process of sending, it should set TxABORT in response to TxDONE. An ABORT will be sent on the serial line as soon as the current character is completed.

The program can count ABORTs by setting TxABORT in response to TxDONE. Setting TxABORT will clear TxDONE, but TxDONE will set again when the requested ABORT begins. To shut the line down after the last desired ABORT has begun, the program should set TxABORT a final time, clear SEND, and wait for TxDONE to set indicating the ABORT has completed and the line is idle. To start a new message after the last desired ABORT has begun, the program should clear TxABORT and set TSOM. When the ABORT completes, a FLAG will begin and TxDONE will set. The program should clear TSOM and load the first data character.

Bit-Oriented Operation—Receiver

The receiver section of the DUP11 detects FLAG and ABORT sequences, performs serial-to-parallel conversion of 8-bit bytes of data, and optionally calculates and checks the CRC/CCITT block check characters. Whenever the data stream between two FLAGs contains five consecutive one bits followed by a zero bit, the receiver section automatically deletes the zero bit from the data stream being assembled into characters and checked in the CRC calculation. This restores the original transmitted data stream.

After the initialize or device reset pulse, the program must clear the DEC MODE bit of the PARCSR and set or clear the CRC INHIBIT bit of the PARCSR. These bits affect both the transmitter and receiver. In addition, the program can set the secondary mode select bit of the PARCSR if the DUP11 is operating as a secondary station with a protocol which uses the first data character as a secondary address. In this case, the program must load the desired secondary address into the PARCSR.

Before enabling the receiver, any necessary handshaking with the data set should be completed. Once this is done, the program can enable the receiver by setting the RCVEN bit in the RxCSR. The receiver will begin to search for a FLAG sequence.

Multiple FLAGs at the beginning of a frame are simply ignored. A frame begins following the last initial FLAG.

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If the DUP11 is not in secondary address mode when the first character of a frame has been assembled, the receiver will load the character into the RxDBUF, set the RSOM (receiver start of message) bit in the RxDBUF, and set the RxACT (receiver active) and RxDONE bits in the RxCSR. The program should read the RxDBUF in response to the setting of RxDONE. This will clear RxDONE. (Reading the RxDBUF always clears RxDONE.) RSOM will clear when the next data character has been assembled or if a FLAG or ABORT is received.

If the DUP11 is in secondary address mode, the first character assembled following the last FLAG is compared to the secondary station address register. If it does not match, the initial search for a FLAG begins anew. If it matches, the RxACT bit is set in the RxCSR and the RSOM bit is set in the RxDBUF to indicate the start of a frame. However, the received address character will not be presented to the program. When the subsequent character has been assembled, this character will be loaded into the RxDBUF. RSOM will remain set. RxDONE will be set. The program should read the RxDBUF. RSOM will clear when a third data character has been assembled or if the FLAG or ABORT is received.

Subsequent characters will be loaded into the RxDBUF and presented to the program by setting RxDONE. The program should read the RxDBUF and assemble the incoming frame. If the program does not read the RxDBUF by the time the next character has been assembled, the overrun bit in the RxDBUF will be set indicating an error condition. The time available can be calculated by the formula:

$$(1/\text{bits per second}) * (8 + n) \text{ seconds}$$

where n is the number of stuffed bits (n = 0, 1, or 2)

The DUP11 receiver will recognize the end of frame when it sees a terminating FLAG. The RxACT bit will be cleared and the REOM bit will be set in the RxDBUF. The RxDONE bit in the RxCSR will be set. If CRC INHIBIT is not set and the completed CRC calculation indicates an error, then the RCRC ERROR + ZERO bit will be set in the RxDBUF to inform the program of the error.

When the program reads the RxDBUF and sees REOM set, it should check the state of RCRC ERROR + ZERO if the DUP11 is doing CRC calculation. It must ignore the data buffer. The data buffer contains invalid information when REOM is set.

The DUP11 receiver presents characters as they are assembled. Consequently, even if CRC INHIBIT is not set, the two block check characters will be presented to the program.

If the transmitted data is not a multiple of 8 bits long, a FLAG will be detected in the middle of assembling a character. The program will be presented 8 bits consisting of the left-over data bits and bits derived from the beginning of the FLAG. When the FLAG is recognized, REOM and RxDONE will set as described above. RCRC ERROR + ZERO will set

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if an error was detected and CRC INHIBIT is not set. The FLAG may be recognized in much less than a character time following the presentation of the above 8 bits. If it occurs before the program has had time to read the RxDBUF, the RxDAT LATE bit will set, indicating an error. The DUP11 is designed to handle frames that are a multiple of 8 bits long, but an error on the serial line might cause the receiver to incorrectly decode stuffed bits creating a frame of incorrect length. The CRC calculation is always done on the actual bits between FLAG characters, regardless of frame length, so any error should be detected.

When the RxDBUF is read, RxDONE will clear and the DUP11 receiver will be ready for another frame. This can begin immediately following a single FLAG or it can follow multiple FLAGs as described above.

The DUP11 receiver will recognize seven consecutive one bits as an ABORT sequence when they appear in the middle of a frame, i.e., any time RCVEN and RxACT are both set. Receiving an ABORT sequence is equivalent to resetting the receiver except that RCVEN is not cleared, the RABORT (received abort) bit in the RxDBUF is set, and the RxDONE bit in the RxCSR is set. Reading the RxDBUF will clear the RABORT bit. When the program sees that RABORT was set, it should discard the partially assembled frame.

When an ABORT has been received, the DUP11 receiver reverts to searching for a synchronizing FLAG.

Half-Duplex Operation

The program may specify half-duplex operation by setting the HALF DUPLEX bit in the TxCSR.

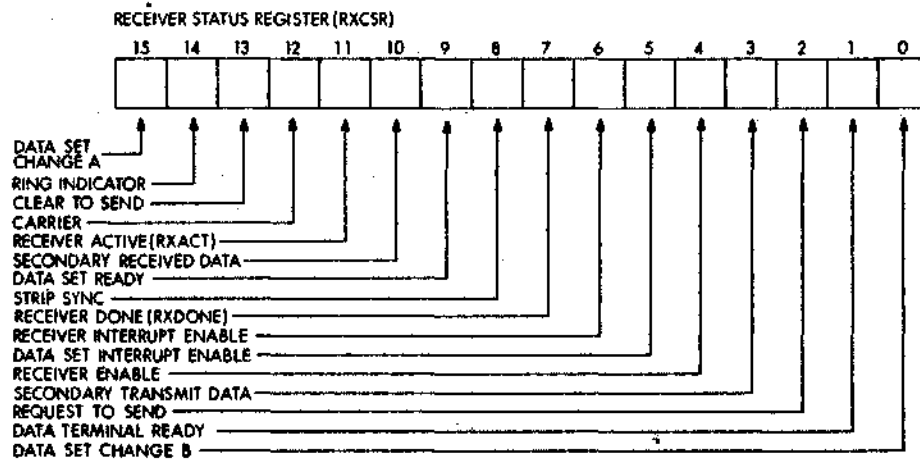
In this mode of operation, the receiver will be completely disabled while the SEND bit is set in the TxCSR. All other characteristics of the interface are maintained. This action is only required for half-duplex modems which provide local-copy.

REGISTERS

RECEIVER STATUS REGISTER (RxCSR)—ADDRESS: 16XXX0.

Addressable by word or byte

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Bits	Description
00	<p>Data Set Change B</p> <p>With normal jumper configuration, this bit will be asserted when any of the following transitions occur on the respective data set control lines:</p> <ul style="list-style-type: none"> —any transition on the Carrier line —any transition on the Data Set Ready line —any transition on the Secondary Received Data line <p>Two optional jumper modifications can be made in the field with respect to this bit:</p> <ol style="list-style-type: none"> 1. Removing the data set change jumper will inhibit the setting of this bit. 2. This bit will be inhibited and the signal transitions cited above will be combined with the ones that always assert Data Set Change A (refer to bit 15). <p>Program read only. Cleared by INIT, Device Reset or by reading the RxCSR.</p>
01	<p>Data Terminal Ready</p> <p>When set, this bit causes the Data Terminal Ready lead to be asserted to the modem.</p> <p>Program read/write. Optionally cleared by INIT or Device Reset.</p>
02	<p>Request to Send</p> <p>When set, this bit will cause the Request-to-Send lead to be asserted to the modem.</p> <p>Program read/write. Optionally cleared by INIT or Device Reset.</p>
03	<p>Secondary Transmit Data</p> <p>This bit is connected to the Secondary Transmit line of the modem. With certain modems, supervisory data can be transmitted over this line at a reduced rate.</p>

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- Program read/write. Optionally cleared by INIT or Device Reset.
- 04 Receiver Enable (RCVEN)
This bit controls the operation of the receiver logic. When initially asserted, the receiver is enabled to search for synchronization, regardless of the DUP11's operating mode.
Once synchronization has been achieved, the reception of data and the timing are controlled by this bit.
Clearing this bit at any time will cause all receiver timing and control functions to be reset asynchronously to the modem clock or the data stream currently being received.
The RxDONE bit will be cleared by the OFF transition of this bit.
Program read/write. Cleared by INIT or Device Reset.
- 05 Data Set Interrupt Enable
When set, this bit allows interrupt requests to be made to the receiver vector, if the Data Set Change A bit is asserted. Program read/write. Cleared by INIT or Device Reset.
- 06 Receiver interrupt Enable
When set, this bit allows interrupt requests to be made to the receiver vector, if the RxDONE bit is set.
Program read/write. Cleared by INIT or Device Reset.
- 07 Receiver Done (RxDONE)
This bit is set by the device when the RxACT bit is asserted and a character is transferred from the internal receiver shift register to the RxDBUF (receiver data buffer).
In byte-oriented mode, this bit will also be asserted whenever SYNC characters are received immediately subsequent to the actual synchronizing SYNC characters, unless the STRIP SYNC bit is set.
In bit-oriented operation, this bit will also be asserted if the RxACT bit is set when an ABORT sequence is received or when the REOM bit is set in the RxDBUF.
Program read only. Cleared by reading the RxDBUF, an off transition of RCVEN, INIT, and Device Reset.
An interrupt request will be generated if Receiver Interrupt Enable is set when this bit is asserted.
- 08 STRIP SYNC
This bit is used only with byte-oriented protocols. Once the receiver has achieved synchronization, any characters received that match the contents of the low byte of the PARCSR will not be presented to the program if they are contiguous to the initial SYNC characters (i.e., RxDONE will not be set) if this bit is set. As a result, any SYNC characters contiguous to the SYNC characters that caused the actual synchronization are stripped off. The function of this bit is automatically disabled while RxACT is set.

NOTE

This bit must be cleared when operating with bit-oriented protocols.

- Program read/write. Cleared by INIT or Device Reset.
- 09 Data Set Ready
This bit is a direct reflection of the Data Set Ready (or interlock) lead emanating from the modem. This line, when asserted, indicates the modem is powered up and is not in the test, talk, or dial mode. Any transition of this bit will cause the Data Set Change B bit to be asserted unless the data set change jumper modification has been made (refer to bit 15 of RxCSR).
Program read only.
- 10 Secondary Received Data
This bit reflects the state of the Secondary Received Data line of the modem. Any transition on this line will cause the Data Set Change B bit to assert unless the data set change jumper modification has been made (refer to bit 15 of this register).
With certain modems, supervisory data can be received over this line at a reduced rate. It can also be used as a control lead.
Program read only.
- 11 Receiver Active (RxACT)
In byte-oriented operation, this bit will set when the first character has been assembled subsequent to synchronizing on two SYNC characters if Strip SYNC is cleared. If Strip SYNC is set, this bit is asserted after receiving the first non-SYNC character. This bit controls whether incoming data is included in the receiver CRC calculation.
In bit-oriented operation, as a primary station, this bit will set when the first data character of a frame has been assembled. In bit-oriented operation, as a secondary station, this bit will set when the first character of a frame has been assembled and that character matches the contents of the Secondary Station Address Register. This bit will clear when a terminating FLAG is recognized or if the frame is aborted by receipt of seven consecutive one bits. This bit controls the operation of the receiver logic.
Program read, cleared by INIT, Device Reset, and clearing RCVEN.
- 12 Carrier.
This bit is a direct reflection of the modem carrier. Any change in the state of this line will cause Data Set Change B bit to be asserted, unless the Data Set Change jumper modification has been made. (Refer to bit 15 of this register).
Program read only.
- 13 Clear to Send.
This bit reflects the state of the Clear-to-Send line of the modem.

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Any transition of this line causes the Data Set Change A bit to set.

Program read only.

14 Ring Indicator

This bit reflects the state of the modem Ring line. Any positive transition of this line greater than 10 msec causes the Data Set Change A bit to set.

Program read only.

15 Data Set Change A

This bit is set by a transition on any of the following control lines:

- any positive transition on the Ring line greater than 10 msec.
- any transition on the Clear-to-Send line

An optional field installation change (consists of a jumper modification, supported by diagnostics) will allow this bit to be set by any of the following transitions:

- any transition on the Carrier line
- any transition on the Data Set Ready line
- any transition on the Secondary Received Data line.

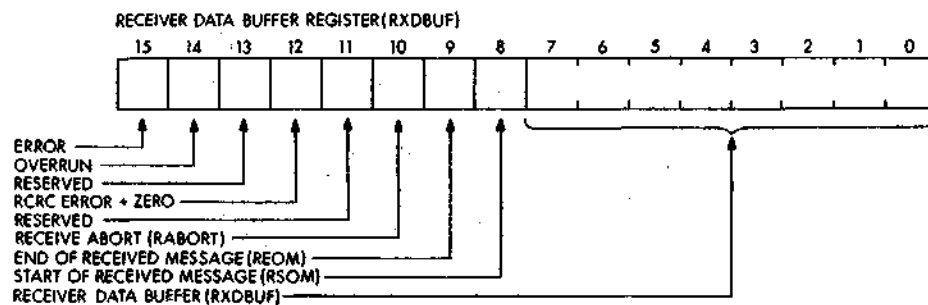
Normally these transactions cause bit 0 (Data Set Change B) to be set in this register. If the jumper modification is made, bit 0 will be disabled.

If bit 05 of this register is set, the assertion of this bit will cause an interrupt to the receiver vector.

Program read only. Cleared by INIT, Device Reset, or when the RxCSR is read.

RECEIVER DATA BUFFER REGISTER (RXDBUF)—ADDRESS: 16XXX2. Read only—addressable by word.

This register should be read only in response to RxDONE.



Bits	Description
00-07	Receiver Data Buffer This register contains 8-bit data received from the modem. Bit

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00 is the least significant bit and bit 07 the most significant bit. When the REOM bit is set, the data in this register is not valid.

Program read, cleared by INIT, Device Reset, RABORT or clearing RCVEN.

08 Start of Received Message (RSOM)

This bit is used only in bit-oriented mode. When in the primary mode, this bit is set when the first data character is received. In secondary mode, this bit is set when the character following an address character is received, providing that the address character matched the contents of the secondary station address register. The next transfer from the receiver shift register into the RxDBUF will clear this bit.

Program read. Cleared by INIT, Device Reset, and clearing RCVEN.

09 End of Received Message (REOM)

This bit is used only in bit-oriented operation. This bit will set when a terminating FLAG is recognized. The next transfer from the receiver shift register into the RxDBUF will clear this bit.

Program Read, closed by INIT, Device Reset, and RCVEN.

10 Received ABORT (RABORT)

This bit will set when an ABORT sequence (seven consecutive one bits) is detected while the receiver is active in bit-oriented operation. When this occurs, all the DUP11 receiver timing, internal control, and registers will be reset.

Setting this bit will cause the RxDONE and Receiver Error bits to be set.

Cleared by INIT, Device Reset, clearing RCVEN, and reading the RxDBUF.

11 Reserved

12 RCRC ERROR + ZERO

This bit will remain zero if CRC INHIBIT is set in PARCSR.

In byte-oriented operation, this bit will be set whenever the DUP11 receiver internal CRC register was zero at the completion of the character in the RxDBUF.

In bit-oriented operation, this bit will be set if the receiver logic detects an invalid block check. This bit will be set when the terminating FLAG is detected, i.e., the same time REOM is set.

When this bit has been set, it will remain set until the next transfer is made into the RxDBUF from the receiver internal shift register. This will normally be for at least one character time.

Program read only. Cleared by INIT, Device Reset, and clearing RCVEN.

13 Reserved.

14 Overrun

When the receiver logic detects an overrun condition, this bit is

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set. An overrun is caused primarily by poor program response time. Assertion of this bit will cause the Error bit to assert. Once the Receiver Done (RxDONE) bit is set, the program must respond within one character time; if not, Overrun will occur. This condition indicates the loss of at least one character.

This bit will be asserted for a minimum of one character time and will clear within one character time after the overrun condition has been relieved by resetting the RxDBUF.

Program read only. Cleared by INIT, Device Reset and clearing RCVEN.

15 Error

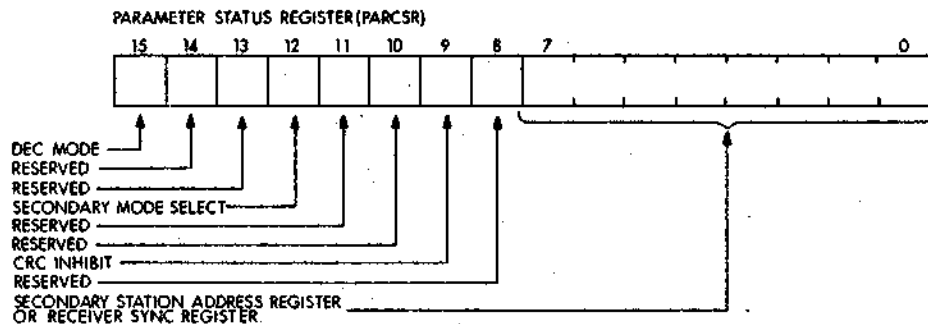
This bit will be set in byte-oriented operation while bits 14 or 12 of this register are set. This bit will be set in bit-oriented operation while bits 14, 12, or 10 of this register are set (logical OR).

Program read only.

PARAMETER STATUS REGISTER (PARCSR)—ADDRESS: 16XXX2

Write only—addressable by byte or word.

This register should be accessed only when both the transmitter and receiver are in idle state.



Bits	Description
00-07	Secondary Station Address Register or Receiver Sync Register. Used by the receiver logic only. When the DEC MODE bit is set (byte-oriented protocols) this register contains the SYNC character. Bit 00 is the least significant bit and 07 is the most significant bit. When operating in the secondary mode of bit-oriented protocols, this register contains the desired secondary station address. Program write. Cleared by INIT, or Device Reset.
08	Reserved.
09	CRC INHIBIT. Setting this bit inhibits transmitting the CRC check character and inhibits checking the received CRC check character.
10-11	Reserved

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12 Secondary Mode Select.

This bit is used with bit-oriented protocols only and affects the DUP11 receiver only. When this bit is cleared and DEC MODE is cleared, the DUP11 receiver will operate as a primary station and all data subsequent to the last received FLAG character will be presented to the program, until the terminating FLAG is detected.

When this bit is set and DEC MODE is cleared, secondary station operation is in effect—only messages that are prefixed with the correct secondary station address will be presented to the program. Note: This bit must be cleared when operating with byte-oriented protocols.

Program write. Cleared by INIT or Device Reset.

13-14 Reserved.

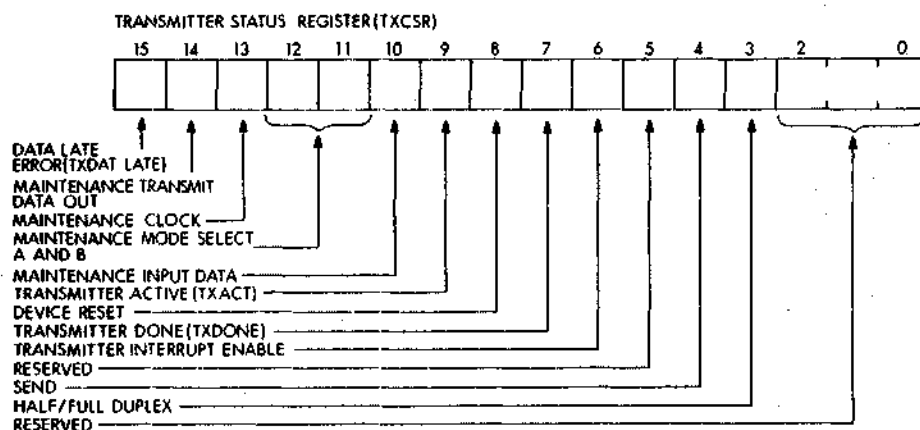
15 DEC MODE

When this bit is asserted, the DUP11 will operate in a manner compatible with the byte-oriented protocols (such as DDCMP and BISYNC). If this bit is clear, the device will operate with bit-oriented protocols (such as SDLC, HDLC, or ADCCP).

Program write. Cleared by INIT or Device Reset.

TRANSMITTER STATUS REGISTER (TxCSR)—ADDRESS: 16XXX4.

Addressable by word or byte.



Bits	Description
00-02	Reserved
03	Half-Duplex/Full-Duplex When this bit is set, the receiver will be disabled if the SEND bit in the TxCSR is set. Program read/write. Cleared by INIT or Device Reset.
04	SEND When set, this bit enables the transmitter logic. Once enabled,

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it will start the transmission of a message when the TSOM bit is detected in the TxDBUF.

Clearing SEND when TEOM is clear will cause the line to go to the mark hold following completion of the current character being sent. Clearing SEND when TEOM is set will cause the line to go to the mark hold state when the message being sent is complete (i.e., following the final characters, block check and flags, as required). Program read/write. Cleared by INIT or Device Reset.

05 Reserved

06 Transmitter Interrupt Enable

When set, this bit will allow a program interrupt request to be generated by the TxDONE bit.

Program read/write. Cleared by INIT or Device Reset.

07 Transmitter Done (TxDONE)

This bit is set when the Transmitter Data Buffer is available for a new character. This occurs either as a result of an INIT, Device Reset, or when a character is transferred from the TxDBUF into the transmit shift register. If the transmitter is entering the idle state, (i.e., SEND being cleared during the current message), the OFF transition of the TxACT bit will cause TxDONE to set, not the completion of the current character. The TxDONE bit will also set whenever a SYNC, FLAG, or ABORT character has completed transmission, providing the SEND bit is asserted.

Unless a SYNC, FLAG, or ABORT sequence is being transmitted, the program must respond to the assertion of this bit within the previously cited time frame in order to avoid Data Overrun errors.

If the Transmitter Interrupt Enable is asserted, the setting of this bit will create an interrupt request.

Program Read; cleared by writing the TxDBUF; set by INIT or Device Reset.

08 Device Reset

When this bit is set, all components of the device are initialized, unless the optional clear jumper is removed. In this case, the modem control signals from the device are not affected. Note that initializing the device sets TxDONE.

This bit is a 2 μ sec one-shot and will self-clear.

INIT and Device Reset perform identical functions with respect to this device. Program write.

Do not address the DUP11 while this bit is set.

09 Transmitter Active (TxACT)

This bit indicates that the serial line is in use. It is set when the first SYNC or FLAG begins to be sent in response to the

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program enabling the transmitter and setting TSOM. It is cleared one bit time after the serial line has reentered the mark hold state as a result of the program disabling the transmitter.

Program read. Cleared by INIT or Device Reset.

10 Maintenance Input Data

This bit is used in internal maintenance mode as the receiver serial input while SEND is clear. When this bit is set and the maintenance clock bit makes a 0-to-1 transition, a logical one bit will be transferred into the receiver shift register.

Program read/write. Cleared by INIT or Device Reset.

11-12 Maintenance Mode Select A and B

These two bits are used to select the maintenance mode. The program must leave these bits clear for normal operation.

Bit Setting

Select B (bit 12)	Select A (bit 11)	
0	0	Normal operation
0	1	System test mode
1	0	External maintenance mode
1	1	Internal maintenance mode

The external maintenance mode provides a means of checking all the interface components, including level converters and cables. In this mode a special turn-around connector (H325) must be attached in place of the modem at the end of the cable.

The internal maintenance mode provides a means of checking most of the interface without disconnecting the modem. The level converters and cables are not checked. The diagnostic program simulates the data set clocking using the maintenance clock bit. It monitors the transmitted data using the Maintenance Transmit Data Out bit. It can supply input to the receiver using the Maintenance Input Data bit or can cause the receiver to be stimulated by the output of the transmitter.

The system test mode provides a means of exercising most of the interface together with other devices on the PDP-11 UNIBUS without disconnecting the modem. The level converters and cables are not diagnosed. Transmitted data is internally looped to received data. Data set clocking is simulated by a free-running clock at 5KC plus or minus 20%.

Program read/write. Cleared by INIT or Device Reset.

13 Maintenance Clock

This bit is used to single step the transmitter and receiver clock for diagnostic purposes. A 0-to-1 transition of this bit causes the transmitter to transfer one bit of information to the serial line.

A 1-to-0 transition of the bit causes the receiver to shift the

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contents of the receiver shift register and sample the serial output line.

This bit must be cleared for normal user operation.

Program read/write. Cleared by INIT or Device Reset.

14 Maintenance Transmit Data Out

This bit is enabled only in internal maintenance mode and provides a monitoring point for serial output data from the transmitter.

Program read. Cleared by INIT or Device Reset.

15 Transmitter Data Late Error (TxDATA LATE)

This bit is set by the DUP11 transmitter logic when the program has failed to respond to the TxDONE bit in time.

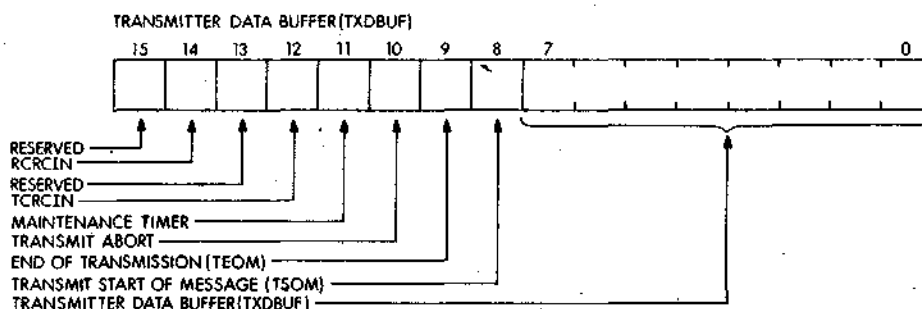
In byte-oriented operation when this bit is set, the serial line will be held in the mark state until TSOM is set and a new message is started.

In bit-oriented operations when this bit is set, the transmitter will idle ABORT characters until either TSOM is set to start a new message or the SEND bit is cleared.

Program read only. Cleared by INIT, Device Reset, or by setting the TSOM bit.

TRANSMITTER DATA BUFFER (TxDBUF)—ADDRESS: 16XXX6.

Addressable by word or byte.



Bits	Description
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00-07	Transmitter Data Buffer (TxDBUF)
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The program loads this register with the information to be transmitted, which is always treated as an 8-bit character.

For byte-oriented operation, the program must load this register with the SYNC character whenever it is desired to transmit SYNC characters.

Bit 07 is the most significant bit and bit 00 is the least significant bit.

Program read/write. Cleared by INIT or Device Reset.

- 08 Transmit Start of Message (TSOM)**
The program sets this bit to initiate transmission following the enabling of the transmitter. The program can also set this bit between messages to transmit SYNC characters or FLAGS.
In byte-oriented operation the program sets this bit to send SYNC characters. (The Transmitter Data Buffer must contain the desired SYNC character.) The transmitter CRC calculation is initialized. The SYNC characters are not included in the CRC calculation.
In bit-oriented operation the program sets this bit to send FLAG characters that precede a frame. The CRC calculation is initialized.
While this bit is set, Transmitter Data Late errors are inhibited.
Program read/write. Cleared by INIT or Device Reset.
- 09 Transmit End of Message (TEOM)**
This bit is set by the PDP-11 program to indicate that all data characters of a message have been previously loaded into the TxDBUF and the message should be completed. The transmitter completes the character currently being sent, and sends the block check character unless CRC INHIBIT is set.
In bit-oriented operation, the transmitter then sends FLAG characters while this bit remains set. In bit-oriented operation, Data Late errors are inhibited while this bit is set to permit the program to idle FLAG characters.
In bit-oriented operation, this bit is used together with TSOM immediately following the enabling of the transmitter when a 16 bit 0 sequence must precede the beginning FLAG.
Program read/write. Cleared by INIT or Device Reset.
- 10 Transmit ABORT (TxABORT)**
This bit is used only in bit-oriented operations. Assuming the transmitter is active, setting this bit will cause an ABORT to be sent when the current character or sequence completes.
Leaving this bit set will cause multiple ABORTs to be sent. While this bit is set, Transmitter Data Late errors are inhibited.
Program read/write. Cleared by INIT or Device Reset.
- 11 Maintenance Timer**
This bit is enabled only in the external or systems test maintenance modes and is used to provide a known timing reference for diagnostic programming.
Program read only. Cleared by INIT or Device Reset.
- 12 TCRCIN**
This bit is enabled only in internal maintenance mode and is used in diagnosing the transmitter CRC logic.
Program read only.

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- 13 Reserved
- 14 RCRCIN
This is enabled only in internal maintenance mode and is used in
diagnosing the receiver CRC logic.
Program read only.
- 15 Reserved

SYNCHRONOUS PREPROCESSOR, DV11**HIGHLIGHTS**

- 8- or 16-line synchronous multiplexer for use with PDP-11 family computers.
- NPR data transfers on transmission and reception.
- Total 16-line throughput of up to 38,400 characters per second (9600 baud full duplex for each line).
- Control table scheme provides programming flexibility, particularly for special character and protocol handling.
- Open-ended flexible design—hardware not committed to any specific protocol.
- 128-character first-in/first-out receiver buffer.
- Program-selectable block checks (LRC-8, CRC-16, CRC/CCITT) calculated by the hardware.
- Modem control.
- Choice of external or internal clock.
- Two program-selectable sync characters for each line.
- Switch-selectable character sizes.
- Up to 4 DV11's with total throughput of 76,800 characters per second can be connected to a PDP-11 depending on configuration and application.

GENERAL DESCRIPTION

The DV11 is a synchronous preprocessor which permits eight or sixteen synchronous lines to be interfaced to a PDP-11. It is designed to relieve the PDP-11 processor of almost the entire overhead associated with interrupt handling, character processing and CRC/LRC calculations.

It provides very high throughput (up to 38,400 characters per second total for all 16 lines) and extremely flexible handling of special data link characters. High throughput is achieved by use of direct memory (NPR) transfers on both transmission and reception. Flexibility is achieved, without committing hardware to any specific protocol, through the use of control bytes stored in core tables. The program can specify parameters in each control byte, thus providing flexibility for requirements within a specific application.

The DV11 contains provisions for up to eight reception modes for use with character-oriented protocols (for instance, there are modes for transparent data reception and for normal text reception). The action taken in each mode and the transition from one mode to another are controlled by control tables located in core memory. A control table for an individual reception state consists of 256 bytes—one for each of the possible characters that can be received during the reception.*

*Typically, control bytes are used to indicate how the character is to be handled, whether an interrupt is to be generated, and whether the character is to be included in the block check.

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The DV11 hardware can perform block check calculations for longitudinal redundancy checks (LRC) and cyclic redundancy checks (CRC-16 and CRC/CCITT).

The character size (5, 6, 7 or 8 bits) and character format (no parity, even, or odd parity) are switch-selectable for each 4-line group (0-3, 4-7, 8-11, 12-15). The DV11 can calculate LRC's for all character sizes, and CRC's for 8-bit characters.

Two sync characters may be manually pre-selected for each 4-line group. Then the program can select from either of those two sync characters for each individual line. For transmission, the same sync character is used as the transmitter fill-character or an "all 1's" condition can be sent.

PHYSICAL DESCRIPTION

The DV11 consists of a 9-slot double system unit (DV11-AA) which contains the basic logic modules, a microprocessor and modem control modules, plus a distribution panel and line cards for eight lines (DV11-BA).

Two DV11-BA 8-line units can be used with a DV11-AA.

BASIC OPERATION (Figure 1)

Sixteen Synchronous Receivers assemble characters received from serial communications lines and assert a flag as each character is received. Sixteen Synchronous Transmitters disassemble characters and transmit them on serial communications lines and assert a flag whenever they can accept another character for transmission. The Master Scanner sequentially checks the synchronous receivers and transmitters for each line to see if a flag exists.

The microprocessor handles all characters received or transmitted by the DV11. It controls all non-UNIBUS data transfers and steps the Master Scanner. Except for those occasions where a UNIBUS instruction or NPR transfer involving the DV11 is taking place, the microprocessor never stops.

The microprocessor system includes a 128-character first-in/first-out storage buffer. While most characters received by the DV11 will propagate through this buffer and be directly transferred to PDP-11 core by means of an NPR transfer, the occasion may arise when the attention of the PDP-11 program is required before this is done. To prevent the synchronous receivers from experiencing data overruns during the interval that the DV11 is awaiting program attention, the microprocessor will continue to load the received characters into the first-in/first-out buffer, but the action of the microprocessor in withdrawing characters from the buffer will cease until the PDP-11 program responds to the interrupt caused by the special character at the bottom of the silo buffer. The character which requires PDP-11 program attention is copied into the

The Receiver Interrupt Character Register is a UNIBUS-addressable register used by the microprocessor to show the PDP-11 program any re-

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Receive Interrupt Character Register at the time the interrupt is generated.

ceived character, along with line number and error flags for which the control logic requires assistance in processing.

The Receiver Control Byte Storage Register is a UNIBUS-addressable secondary register used to instruct the microprocessor how to process the character in the Receiver Interrupt Character Register.

The NPR control is the hardware which is used to gain control of the UNIBUS in order to store received characters, obtain characters for transmission, and to obtain control bytes that direct the character processing.

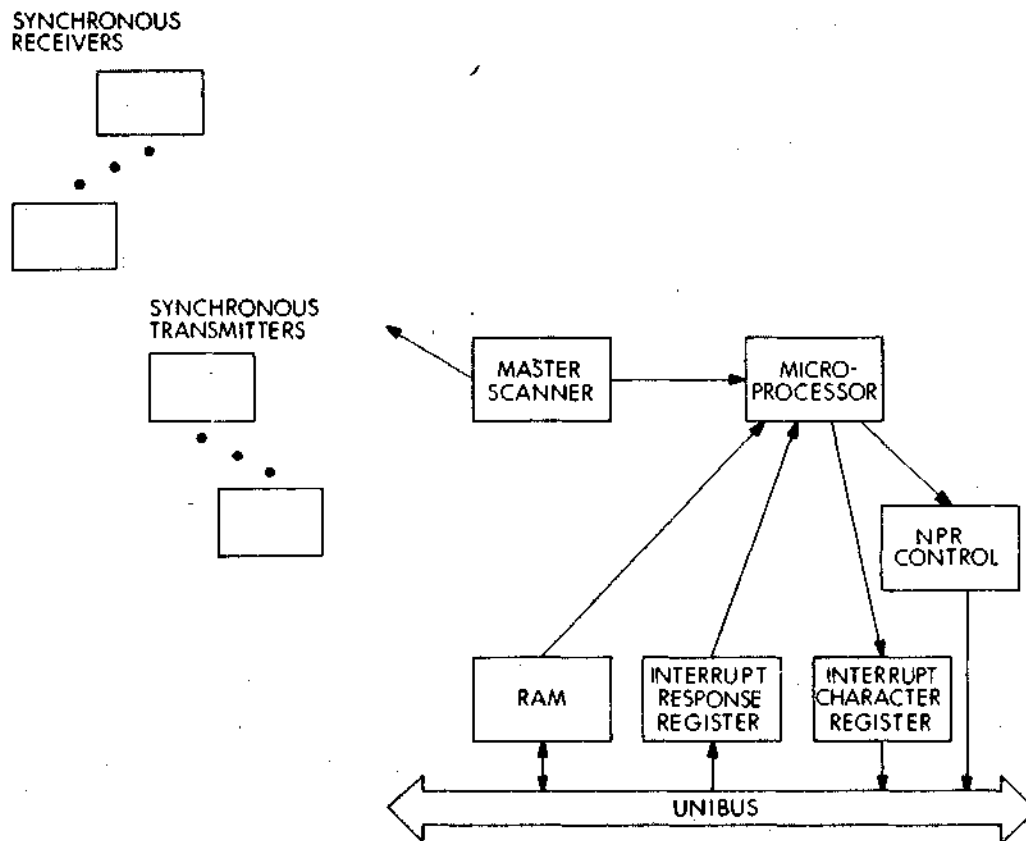


Figure 1. Basic Operation

The microprocessor read/write random access memory (RAM) contains current addresses and two's complement byte counts used in NPR transfers. The initial values are loaded by the PDP-11 program via the UNIBUS, and these values are subsequently updated by the microprocessor. The RAM also contains a line protocol word for each line by which the PDP-11 program can specify what action is to be taken when

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the byte count reaches zero and what type of block check polynomial should be used. In addition, a line state word is stored for each line providing a snapshot of what microprocessor activity is in progress at a particular line.

RECEPTION OPERATION (Figure 2)

Line synchronization and character assembly are accomplished by LSI synchronous receivers which initially compare groups of eight bits received on each line with the preselected sync character to achieve line synchronization. When line synchronization has been achieved, subsequently-received characters are placed into a first-in/first-out, 128-character silo storage buffer. Each line receiver appends the line number (four bits) and any error flags (two bits—parity error, overrun error) to the character prior to placing it in the receiver storage buffer.

The DV11 microprocessor removes characters from the silo along with their line number and error flags. If there is an error flag (as a result of the parity error or overrun error detected by the receiver) the character is placed in a UNIBUS-addressable register called the Receiver Interrupt Character Register and an interrupt request is generated.

If there is no error flag, the DV11 processing depends on whether a character-oriented protocol (example: BISYNC) or a byte-count-oriented protocol (example: DDCMP) is being used.

Character-Oriented Protocol Reception (Example: BISYNC)

If there is no error flag, the microprocessor affixes three mode bits at the high-order end of the received 8-bit character. This 11-bit character is then used as an offset in the PDP-11 control table to obtain a control byte that will indicate to the microprocessor what mode is to be used for subsequent reception on this line and any special handling information appropriate to this character (such as whether or not to generate an interrupt, whether or not to include the character in a block-check computation, whether or not to store the character in a PDP-11 core message buffer).

If the generation of an interrupt is indicated, the character and the line number are moved to the Receiver Interrupt Character Register along with an error bit code. The error bit code indicates that this interrupt is being generated because a control table control byte has indicated that this is a special character.

If the control byte indicates that this character should be included in a block check, the DV11 microprocessor performs the appropriate calculation (LRC, CRC-16, or CRC/CCITT).

If the control byte directs that a received character be discarded, the character is discarded. If it indicates that the character be stored, the DV11 microprocessor obtains the current address from a secondary register associated with this line and uses that address to store the received character in a message buffer. The DV11 microprocessor then

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increments the current address secondary register for that line. In addition, the DV11 microprocessor increments the byte count Secondary Register for that line. If the storage of the character caused the byte count to reach zero, the microprocessor checks to see whether a mode change has been requested. Such a change is indicated by the Byte Count Register being initially loaded with bit 15 cleared. The new mode is stored by the PDP-11 program in the high byte of the Line State Secondary Register in approximately the same format as a control byte. Having accomplished any actions requested in this pseudo control byte, a copy of the character is moved to the Receiver Interrupt Character Register along with the error bits that indicate that a new receive message buffer must be established for this line. In all cases where a character is moved to the Receive Interrupt Character Register, an interrupt is generated, and the DV11 microprocessor ceases to withdraw characters from the receiver silo storage buffer until the PDP-11 program indicates that such withdrawal can proceed again (by setting a bit in the DV11 System Control Register).

Byte-Count-Oriented Protocol Reception (Example: DDCMP)

If a byte-count-oriented protocol is used, Line Protocol Parameters bit 05 (DDCMP Receive) should be set by the PDP-11 program and the receiver mode should be set to 0. This will direct the DV11 microprocessor to skip the control byte process described above, include all characters in the Block Check Calculation, and store all characters (except BCC1 and BCC2). Details of character storage are the same as indicated above.

RECEIVER THROUGHPUT

The receiver throughput in the DV11 is dependent on the number of characters identified in the control bytes as being special (interrupt generating) and the size of the message buffers for received characters. It is intended that the ability of control bytes to accomplish reception mode changes relieves the necessity for received special characters generating an interrupt. When a receiver interrupt is generated, received characters are accumulated in a 128-character first-in/first-out (silo) storage buffer until the interrupt is handled. Assuming arrival of characters at a 19,200-character-per-second rate, it would take approximately 6.6 milliseconds for a silo overflow to occur. Thus, substantial worst-case interrupt latency can be accommodated.

In response to a receiver interrupt indication, the PDP-11 program should set the System Control Register (bit 08) indicating that the DV11 microprocessor may resume processing the character in the Receiver Interrupt Character Register and resume withdrawing characters from the receive silo storage buffer.

If the program so desires, it may alter the receiver control byte stored in the Receiver Control Byte Storage Register before setting bit 08 in the System Control Register.

TRANSMISSION OPERATION (Figure 3)

For each line there is a double-buffered serial transmitter. Whenever the transmitter buffer is empty, a flag is raised. The microprocessor scans

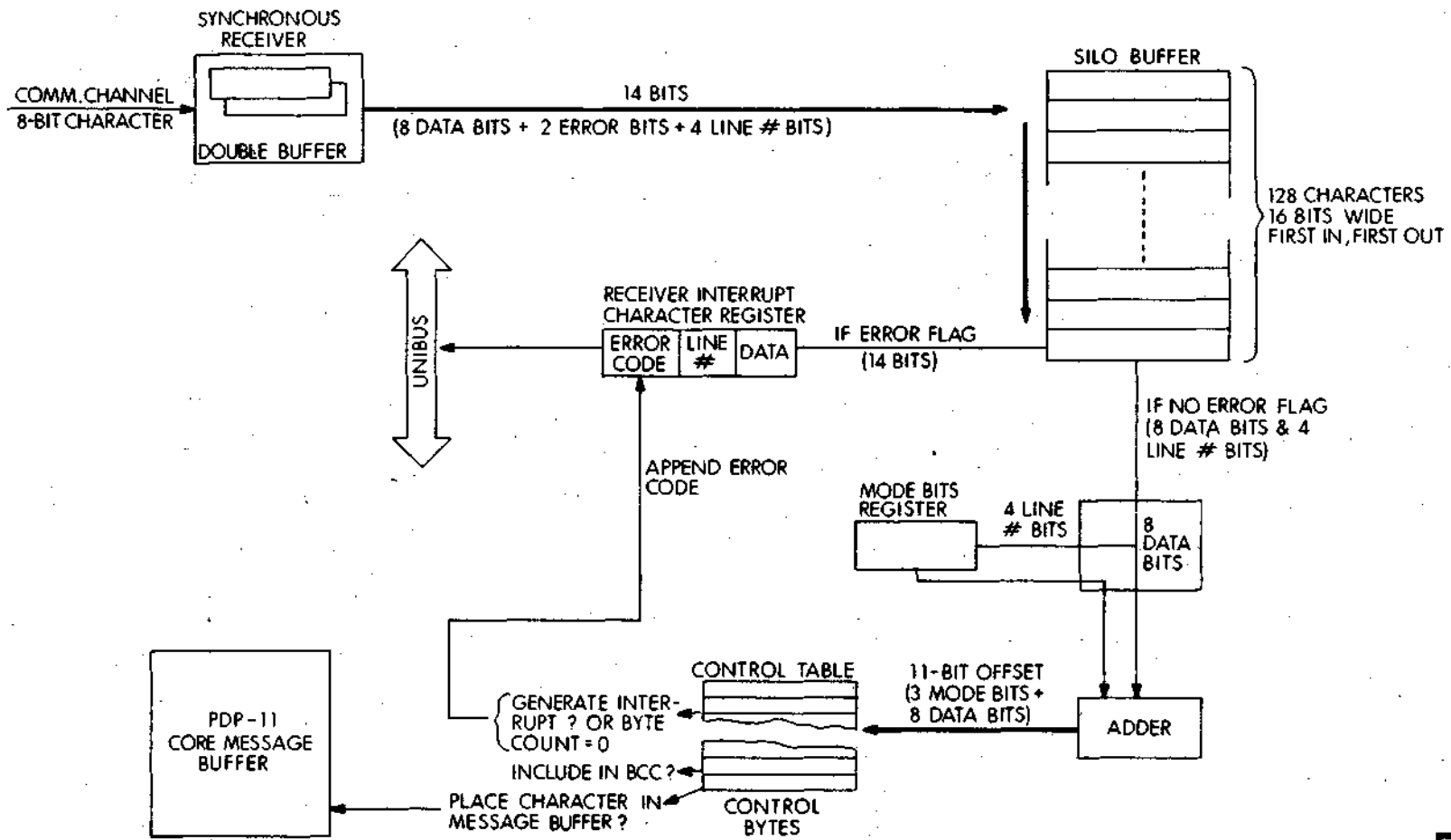


Figure 2. Reception

for transmitter flags and when it finds one, it checks a "worksheet" to determine whether any special action must be taken (e.g., send a block check character). If no special action is required, the microprocessor checks to see if the transmitter "GO" bit for the line is set. If it is set, the microprocessor uses the transmitter current address register to perform an NPR transfer and obtain—from a core message buffer—a character to be transmitted. The DV11 processing of this character depends on whether a Character-Oriented Protocol (example: BISYNC) or a Byte-Count-Oriented Protocol (example: DDCMP) is being used.

**Character-Oriented Protocol Transmission
(Example: BISYNC)**

Before transmitting the character, the microprocessor copies it, adds mode bits to the high-order end and performs an NPR to obtain a transmit control byte from a control table. This byte contains information indicating what new modes are to be used, whether to include the character in the block check, and whether to prefix the transmission of the character with a DLE (performed by microprocessor).

**Byte-Count-Oriented Protocol Transmission
(Example: DDCMP)**

If a byte-count-oriented protocol is used, Line Protocol parameters bit 06 (DDCMP Transmit) should be set by the PDP-11 program and the transmitter mode should be set to 0. This will direct the DV11 microprocessor to skip the control byte process described above and include all characters in the Block Check Calculation. The characters are transmitted as described below.

Transmission of Characters

The microprocessor then loads the character to be transmitted into the appropriate line transmitter and increments the byte count. It then checks the byte count to determine whether it has reached zero. If it has, a check is made to determine whether a mode change has been requested. (Such a change is indicated by the byte count register being initially loaded with bit 15 cleared). The new mode is stored by the PDP-11 program in the high byte of the Line Progress Secondary Register in approximately the same format as the control byte. Having accomplished any actions requested in this pseudo control byte, the microprocessor will switch to the other set of tables (i.e., from principal to alternate or vice versa). If the byte count that is just exhausted did not request a mode change via bit 15 on the Byte Count Register, the microprocessor will switch from principal to alternate (or vice versa) without reference to the upper byte of the Line Progress Secondary Register.

If, after the switch in registers, the microprocessor finds the new byte count is also zero, it will clear "Transmit Go" in the Line State Register and idle sync (or ones), depending on the setting of the "Idle Mark" bit in the Line Protocol Parameters Register.

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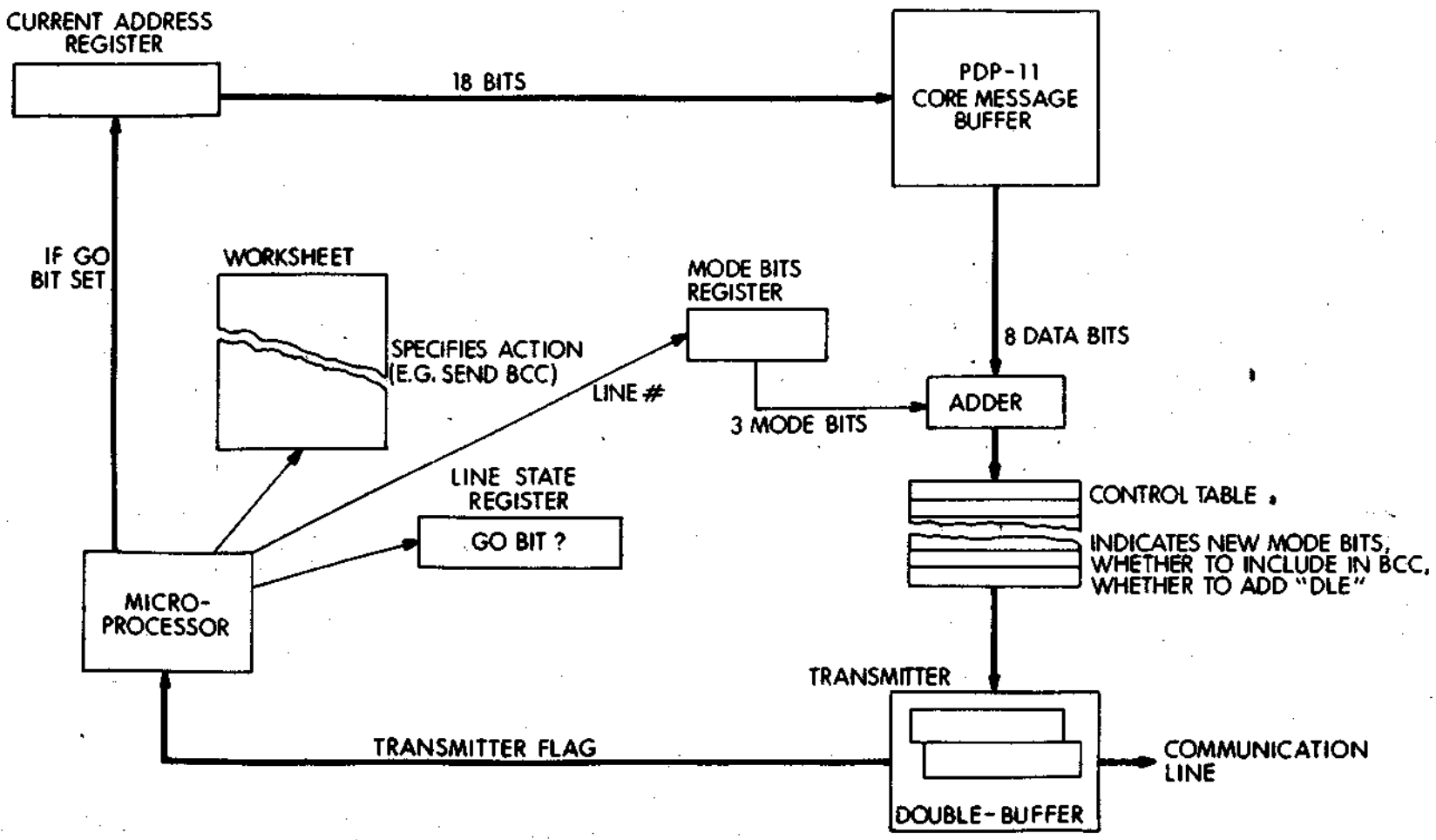
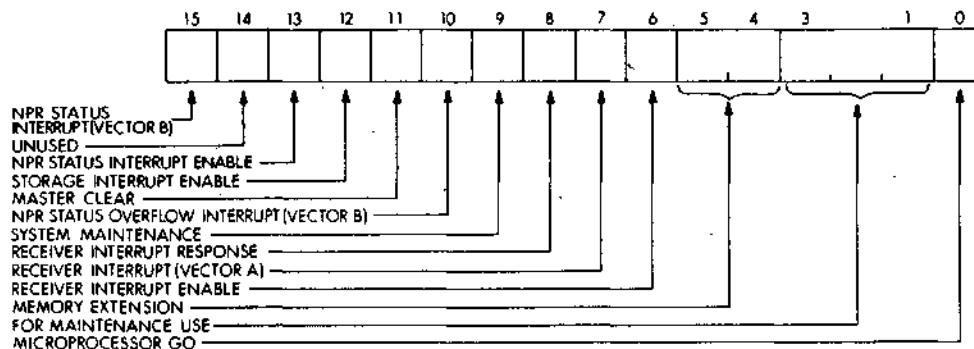


Figure 3. Transmission

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**SYSTEM CONTROL REGISTER (SCR)—ADDRESS 775000
(775040, 775100, 775140)**

The System Control Register is a byte-addressable register. The bit assignment is as follows:



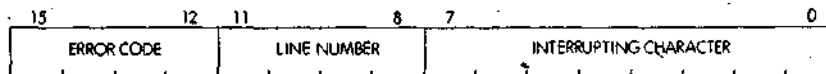
Bits	Description
00	Microprocessor Go This bit when set, permits the DV11 to operate the microprocessor that controls the DV11. This is read/write, CLEARED by Initialize. System programs must set this bit for the DV11 to function.
01	(For Maintenance Use) Do not write one's here
02	(For Maintenance Use) Do not write one's here
03	(For Maintenance Use) Do not write one's here
04-05	Memory Extension For the line number entered in bits 00-03 of the Secondary Register Selection Register, the information stored in these bits becomes bits 16 and 17, respectively, of any current address or control table base address loaded by the program into the RAM. These bits are read/write (cleared by Initialize) but when read, represent only the status of bits 4 and 5 of the System Control Register, not the status of address bits 16 and 17 of the selected line. See the Line Control Register for further information. This arrangement permits interrupt service routines to save the contents of the System Control Register accurately.
06	Receiver Interrupt Enable This bit, when set, permits the setting of bit 7 to generate an interrupt request. This bit is read/write, and is cleared by Initialize.
07	Receiver Interrupt (Vector A) This bit, when set, indicates that the microprocessor has either

Bits	Description
	(1) withdrawn a byte from a core control table indicating that an interrupt should be generated for the character presently being processed, or (2) the character presently being processed has one or more of its associated error flags set or (3) experienced a zero byte count, non-existent memory location, or memory parity error in processing this character. The program should respond to this interrupt by setting SCR08. (The program might wish to alter the control byte in the Receiver Control Byte Storage Register before setting SCR08.) This bit is read-only, except when SCR09 is set. It is clear by Initialize.
08	<p>Receiver Interrupt Response Completed</p> <p>The setting of this bit clear SCR07 and allows the microprocessor to take action on the character in the RICR (according to the information stored in the Receiver Control Byte Storage Register) and to continue removing characters from the receive silo for processing.</p>
09	<p>For Maintenance Use</p> <p>This bit, when set, permits the program to write bits 7 and 15 of this register. This bit is read/write and is cleared by Initialize. This register must be word-addressed when and while this bit is set.</p>
10	<p>NPR Status Overflow Interrupt (Vector B)</p> <p>This bit, when set, indicates that the DV11 hardware checked the NPR Status Register (a 64-entry silo) and found that there was no room for the entry due to insufficient program attention to servicing this register. All DV11 transmitter action in performing NPR transfers will cease until this condition is corrected. This bit is read/write and is cleared by Initialize.</p>
11	<p>Master Clear</p> <p>This bit, when set, generates "Initialize" within the DV11 data handling sections. (It does not affect the modem control.) The silos (both received character and NPR status*) are cleared. The secondary registers are not cleared. This bit is write-only, reads as zero, as it is self-clearing).</p> <p>* The NPR Status Register, bit 15 ("Entry Present"), is cleared by Initialize; the other bits are not.</p>
12	<p>Storage Interrupt Enable</p> <p>This bit, when set, permits the setting of bit 10 to generate an interrupt request. This bit is read/write and is cleared by Initialize.</p>
13	<p>NPR Status Interrupt Enable</p> <p>This bit, when set, permits the setting of bit 15 to generate an interrupt request. This bit is read/write and is cleared by Initialize.</p>

Bits	Description
14	Unused
15	NPR Status Interrupt (Vector B) This bit is set whenever there are one or more entries in the NPR Status Register, which is a silo-type register. The reading of that read-once register clears this bit, but it resets again if a new entry moves down into the register to replace the previously read entry. This bit is read-only except when SCR bit 09 is set, when it is read/write. This bit is cleared by Initialize.

**RECEIVER INTERRUPT CHARACTER REGISTER (RICR)—
ADDRESS 775002 (775042, 775102, 775142)**

This register is read-only and is cleared by Initialize.



Bits	Description
00-07	Interrupting character These bits contain the interrupting character, right-justified. The least significant bit is bit 00. On parity-equipped characters, less than eight bits, the parity bit will appear immediately to the left of the highest-order bit in the character. See special note associated with Error Code 0101 below.
08-11	Line Number These bits indicate the line number on which the interrupting character was received. Bit 8 is the least significant bit.
12-15	Error Code These bits indicate the reason that the character shown in bits 00-07 generated an Interrupt request.

Error Code Bits	Meaning
15 14 13 12 0 0 0 0	SPECIAL CHARACTER The receipt of this character caused the seizure of a control byte which had bit 00 (generate interrupt) set indicating that this is a special character.
0 0 0 1	PARITY ERROR This character was received with a parity sense opposite to that selected for this line by the parity sense switches on the line card.

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Error Code Bits				Meaning
0	0	1	0	OVERRUN The character(s) preceding this character on this line has (have) been lost due to failure of the DV11 receiver system to keep up with the incoming character rate on this line.
0	0	1	1	PARITY ERROR AND OVERRUN (see previous listings)
0	1	0	0	BYTE COUNT WARNING This character has been stored, but it is the last character that can be stored for this line as the byte count is now zero for reception on this line.
0	1	0	1	BLOCK CHECK COMPLETED A block of text or data and the associated block check characters have been received and the program should now check the accumulated receiver block check; the DV11 presents the OR of the high and low bytes of that register in bits 00-07 of this register.
0	1	1	0	UNDEFINED
0	1	1	1	UNDEFINED
1	0	0	0	BYTE COUNT ZERO This character was not stored, as the byte count for reception on this line is zero and thus there is no place to store this character.
1	0	0	1	UNDEFINED
1	0	1	0	UNDEFINED
1	0	1	1	UNDEFINED
1	1	0	0	PROCESSING ERROR 00 A nonexistent memory time-out occurred when the DV11 attempted to store this character.
1	1	0	1	PROCESSING ERROR 01 A nonexistent memory time-out occurred when the DV11 attempted to obtain the control byte associated with this character.
1	1	1	0	PROCESSING ERROR 10 A memory parity error occurred when the DV11 attempted to store this character.

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Error Code Bits	Meaning
	(NOTE: this error should never occur, as the memory parity logic gives alarms only on DATO transfers).
1 1 1 1	PROCESSING ERROR 11 A memory parity error occurred when the DV11 attempted to obtain the control byte associated with this character.

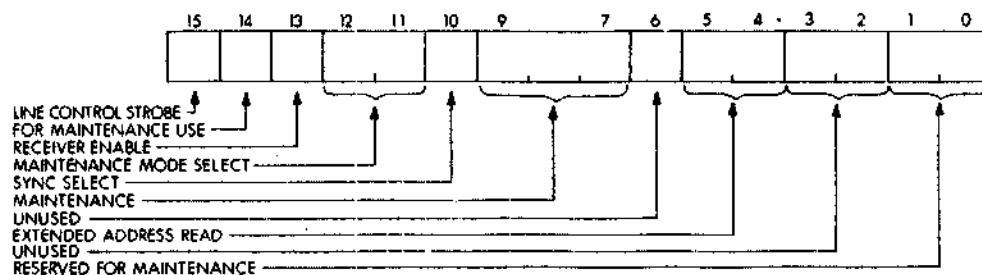
In response to a receiver interrupt (SCR07), the PDP-11 program should examine this register (Receiver Interrupt Character Register), make any desired changes in the Receiver Control Byte Storage Register, and then set SCR08.

In the case of code 0000, Special Character, the Receiver Control Byte Storage Register will contain the control byte associated with the Special Character, but with its bit 00 (generate interrupt) cleared to zero. Thus, for those characters where an interrupt is desired merely to advise the program of reception of a particular character, the program will typically wish to set SCR08 without changing the contents of the Receiver Control Byte Storage Register. For all other error codes, the microprocessor creates a special "remain in mode specified by last control byte fetched for this line, do not include in BCC, do not expect BCC1 next, do not store, do not interrupt" control byte and stores that in the Receiver Control Byte Storage Register before initiating a receiver interrupt request. Thus, for those characters or conditions specifying occurrence of an error, the PDP-11 program can dispose of the character by merely setting SCR08. If desired, the Receiver Control Byte Storage Register may be changed before SCR08 is set.

LINE CONTROL REGISTER (LCR)—ADDRESS 775004 (775044, 775104, 775144)

This register controls the maintenance features associated with each line in the DV11 and provides an opportunity for the PDP-11 program to read the extended address bits for each line. This register is word-addressable only.

Bits indicated to be "write-only" will be read back in the state they were



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last set. Since this is not a presentation of the corresponding bit for the selected line, the bit is referred to as "write-only."

The bit functional assignments are as follows:

Bits	Description
00-01	Reserved for Maintenance (CAUTION: Various bits may appear here during normal DV11 operation.)
02-03	Unused
04-05	Extended Address Read (Read-Only) For the line number entered in bits 00-03 of the Secondary Register Selection Register, these bits represent the status of bits 16 and 17 of the secondary register specified by bits 08-11 of the Secondary Register Selection Register. This permits the PDP-11 program to read the Extended Address bits of the Current Address and Control Table Base Address entries in the RAM.
06	Unused
07	Maintenance (Read-Only) (CAUTION: Various bits may appear here during normal DV11 operation.)
08	Maintenance
09	Maintenance (See bit 15)
10	Sync Select (See bit 15) Each four-line group of the DV11 (0-3, 4-7, 8-11, 12-15) has associated with it two switch-selectable sync/fill characters referred to as Sync A and Sync B. For each individual line in that group (as entered in bits 00-03 of the Secondary Register Selection Register), the setting of this bit determines whether Sync A (bit = 0) or Sync B (bit = 1) is used. This bit is write-only and is cleared by initialize.
11-12	Maintenance Mode Select (Maintenance) (See bit 15) Bits 11 and 12 are write-only and are cleared by Initialize. Normal operating mode is 00.
13	Receiver Enable (See bit 15) When this bit is set by the program, a sync search is initiated on this line by the receiver logic. After an initialize, this bit must be set by the program before any reception can begin on this line (i.e., Receiver Active (See "Line State" secondary register) will not set unless this bit has been set). A switch for each line determines whether the receiver searches for one sync character or for two in a row. A successful sync search results in the setting of Receiver Active (Line State bit 00) for this line. This bit is write-only and is cleared by Initialize.

Bits Description

NOTE

Should it be desired to resynchronize during the course of reception, the program could accomplish this by setting "Receiver Resynchronize" (Line State 01). To shut down reception on a line, the program should clear Receiver Enable and then set Receiver Resynchronize.

- 14 Maintenance (See bit 15)
- 15 Line Control Strobe

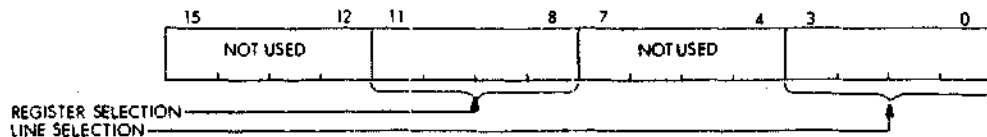
The setting of this bit records the status of bits 09, 10, 11, 12, 13, and 14 into the per-line status flip-flops associated with the line specified in bits 00-03 of the Secondary Register Selection Register. This bit is self-clearing, thus write-only. It may be set at the same time as the bits whose status it records, as its action is delayed until the conclusion of the instruction cycle which set it and the proper phasing of the DV11 internal clocks. This bit is necessary due to "reads" in the PDP-11/20 being "read/write" cycles and certain synchronization requirements associated with mode changes during clocking pulses. The bits marked "Maintenance" should be written to zero for normal DV11 use.

SECONDARY REGISTER SELECTION REGISTER—ADDRESS 775006 (775046, 775106, 775146)

The bits in this register provide a path for the program to access the various locations in the DV11 RAM. The PDP-11 program can read or write these locations. The various locations can be considered as indirectly addressable registers.

Interrupts must be inhibited or the contents of this register saved between the setting of bits in this register and the reading or writing of the Secondary Register Access Register—Address X10. This register is byte-addressable.

The bit assignments of the Secondary Register Selection Register are as follows:



Bits Description

- 00-03 Line Selection

For each type of register selected by bits 08-11 below, there are 16 registers, one per line. The setting of the Line Selection Bits determines exactly which of these line registers is to be ad-

Bits Description

dressed. The Line Selection Bits are also used to select the line to which the bits in the Line Control Register (X04) apply.

04-07 Unused

08-11 Register Selection

These bits determine which type of register is addressed for the line number specified in bits 00-03.

Bits				Register
11	10	09	08	
0	0	0	0	Transmitter Principal Current Address Register
0	0	0	1	Transmitter Principal Byte Count Register
0	0	1	0	Transmitter Alternate Current Address Register
0	0	1	1	Transmitter Alternate Byte Count Register
0	1	0	0	Receiver Current Address Register
0	1	0	1	Receiver Byte Count Register
0	1	1	0	Transmitter Accumulated Block Check Register
0	1	1	1	Receiver Accumulated Block Check Register
1	0	0	0	Transmitter Control Table Base Address Register
1	0	0	1	Receiver Control Table Base Address Register
1	0	1	0	Line Protocol Parameters Register
1	0	1	1	Line State Register
1	1	0	0	Transmitter Mode Bits Register
1	1	0	1	Receiver Mode Bits Register
1	1	1	0	Line Progress Register
1	1	1	1	Receiver Control Byte Storage Register

SECONDARY REGISTER ACCESS REGISTER—ADDRESS 775010 (775050, 775110, 775150)

This register should be loaded or read only after the appropriate bits of the Secondary Register Selection Register have been conditioned to select the type of register and line number within that type. Since this register is essentially a "window" through which the program may access a large number of other registers, no specific bit assignment may be given. See the individual register bit assignment listings. A list of the registers accessible through this register follows. This register is word-addressable only.

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These registers are not cleared by Initialize. The PDP-11 program must clear all of these registers before setting SCR00 (microprocessor go).

Code	Register
0000	<p>Transmitter Principal Current Address Secondary Register</p> <p>This register contains 18-bit entries that will indicate, for each line's transmitter hardware, where in a core memory message table to obtain the next character to load into the synchronous transmitter unit associated with that line. Two additional bits are initially loaded from bits 04 and 05 of the System Control Register (X00), permitting 18-bit addressing capability.</p> <p>When the byte count associated with this current address reaches zero, an entry will be made in the NPR Status Silo and transmission will continue using the Transmitter Alternate Current Address, provided that the "Transmitter Go" bit in the Line State Secondary Register for this line is still set.</p>
0001	<p>Transmitter Principal Byte Count Secondary Register</p> <p>This register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on this line. The 16th bit (bit 15) is used to indicate, when loaded clear, that the high byte of the Line Progress Register will control further action on this line when the principal byte count reaches zero. When a simple change to alternate byte count is desired, bit 15 should be set to one.</p>
0010	<p>Transmitter Alternate Current Address Secondary Register</p> <p>This register has exactly the same function as the Transmitter Principal Current Address Secondary Register described above.</p> <p>When the byte count associated with this current address reaches zero, and entry will be made in the NPR Status Silo and transmission will continue using the Transmitter Principal Current Address, provided the "Transmitter Go" bit in the Line State Secondary Register for this line is still set.</p>
0011	<p>Transmitter Alternate Byte Count Secondary Register</p> <p>This register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be transmitted on this line. The 16th bit (bit 15) is used to indicate, when loaded clear, that the high byte of the Line Progress Register will control action on this line when the alternate byte count reaches zero. When a simple change to principal byte count is desired, bit should be set to one.</p>

NOTE

The program can tell the DV11 whether to start from principal or alternate tables by loading the appropriate bits in the Line State Secondary Register.

Code	Register
0100	<p>Receiver Current Address Secondary Register</p> <p>This register contains 18-bit entries that will indicate, for each line's receiver hardware, where in a core memory message table to store the next character received on this line. Two additional bits are initially loaded from bits 04 and 05 of the System Control Register (X00).</p>
0101	<p>Receiver Byte Count Secondary Register</p> <p>This register contains a 15-bit word that is the two's complement of the number of bytes (characters) remaining to be received on this line. The 16th bit (bit 15) is used to indicate, when loaded clear, that the high byte of the Line State Register will control action on this line when the receiver byte count reaches zero.</p> <p>When the in-core message table for reception on this line has been filled with received characters, the byte count will have been up-counted to zero. An entry will then be made in the Receiver Interrupt Character Register, a receiver interrupt request will be generated, and the action of the microprocessor in retrieving characters from the received character storage silo will stop. Refer to Receiver Interrupt Character Register error code 1000 for further details.</p>
0110	<p>Transmitter Accumulated Block Check Secondary Register</p> <p>This register contains an up-to-date calculation of the block check character associated with transmission on each line. The type of polynomial used for each line is specified in the Line Protocol Parameters Secondary Register (1010). Characters to be included are specified by bit 03 of the control bytes obtained from the core transmission control tables during the NPR transmission of characters on this line if a character-oriented protocol such as BISYNC is being used. If a byte-count-oriented protocol such as DDCMP is being used and the transmitter mode is 0, all characters are included. The contents of this register may be checked at any time by the program. The program may also write into this register; this register can be cleared by writing zeroes into it. (The microprocessor will do this automatically when the BCC is transmitted). The contents of this register are sent out over the line as two 8-bit bytes (low order 8 bits first), except if LRC-8 is the selected protocol, in which cases only one byte is sent.</p>

NOTE

The DV11 calculates CRC-16 and CRC-CCITT on a byte-at-a-time basis (parallel); thus the character length must be eight bits if these block checks are to be used. LRC may be used for shorter characters.

Code	Register
0111	<p>Receiver Accumulated Block Check Secondary Register</p> <p>This register contains an up-to-date calculation of the block check character associated with reception on each line. The type of polynomial used for each line is specified in the Line Protocol Parameters Secondary Register (1010). Characters to be included are specified by bit 03 of control bytes withdrawn from the receiver control byte tables if a character-oriented protocol, such as BISYNC, is being used. If a byte-count-oriented protocol, such as DDCMP, is being used and the receiver mode is 0, all characters (except leading syncs which can be stripped) are included. The contents of this register may be checked at any time by the program. The program may also write into this register; this register can be cleared by writing zeroes into it. The program must do this after it has checked the block check at the end of the message as the microprocessor does not do this. (This would only be necessary if the block check were not zero—an error condition in most protocols).</p>
1000	<p>Transmitter Control Table Base Address Secondary Register</p> <p>This register contains an 18-bit word that indicates the starting address of the transmitter control table for this line. Extended address bits are initially loaded from bits 04 and 05 of the System Control Register (SCR). This address will have the character to be transmitted (with higher order mode bits appended) added to it by the transmitter hardware to obtain a byte address to which the NPR control hardware will go to obtain a control byte. The control byte will instruct the DV11 transmitter what to do with this particular character—whether to include it in the BCC, etc. If all lines in the DV11 are using the same protocol, the program could set all 16 Transmitter Control Table Base Addresses to the same value. In addition, if the protocol permits, the same base addresses could be used for both the transmit control table and for the receive control table.</p>
1010	<p>Line Protocol Parameters Register</p> <p>This register contains information concerning the protocol to be executed on this line. This register must be initially loaded by the PDP-11 program before reception or transmission begins on this line.</p> <p>The bit assignments are as follows:</p>
Bits	Function
00	<p>Idle Mark on Both Byte Counts Zero</p> <p>When this bit is set, the microprocessor will condition the synchronous transmitter on this line to idle MARK when both byte counts reach zero. If the bit is not set, SYNC will be idled. It is anticipated that this feature will be used in half-duplex systems</p>

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Bits	Function
	wherein the PDP-11 program will set this bit immediately after loading the last byte count.
01	Strip Leading Sync When this bit is set, all sync characters received between the time a line goes "active" and the time the first non-sync character arrives will be automatically stripped from the received message. Once a non-sync arrives, this feature is disabled until the line is resynchronized by the issuance of a Receiver Resynchronize command (see Line State Register, bit 01).
02	Reserved
03-04	Block Check Type These bits are conditioned by the PDP-11 program to indicate what type of block check calculation is to be done for transmissions and receptions on this line. 04 03 0 0 LRC-8 (XOR) 0 1 CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 1 0 Unused-16 1 1 CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)
05	DDCMP Receive If this bit is set and reception is in mode 0, the received character will be processed without reference to a control byte. A control byte calling an inclusion of all characters in the BCC and storage of all characters (excluding syncs stripped by bit 01 above) will be assumed. This bit is intended for use with byte-count-oriented protocols.
06	DDCMP Transmit If this bit is set and transmission is in mode 0, the transmitted character will be processed without reference to a control byte. A control byte calling for inclusion of all characters in the BCC will be assumed. This bit is intended for use with byte-count-oriented protocols.
07	Reserved
08-15	Data Link Escape Character In the process of transmitting on a line, the microprocessor fetches control bytes from core indicating what special action, if any, is applicable to the transmission of that character on that line. One of the possibilities is the necessity of transmitting a Data Link Escape Character before transmitting the actual character. The Data Link Escape Character used is retrieved by the microprocessor from the high byte of this secondary register.

Code	Register
1011	Line State Register
	This register is a scorecard with which the microprocessor keeps track of what it is doing with respect to the special actions required of it in executing various line protocols. The bit assignments are as follows:
Bits	Function
00	Receiver Active (set and cleared by microprocessor). This bit is set when an enabled line (LPR 12 set) has satisfied the synchronization conditions. This bit is cleared when the microprocessor finds Line State bit 01 "Receiver Resynchronize" set.
01	Receiver Resynchronize (set by PDP-11 program and cleared by microprocessor). This bit is set when the PDP-11 program desires to resynchronize a line or when it has cleared LPR 13 and is turning off reception on a line. The microprocessor upon finding this bit set will clear Receiver Active, clear this bit, send a resync pulse to the Synchronous Receiver for this line, and will insert a special flag character into the silo. It will also set bit 07 of the Line Progress Secondary Register to indicate that the special resynchronization character is in the silo.
02	Transmitter Go (set by PDP-11 program and cleared by microprocessor). The PDP-11 program will set this bit whenever it has prepared a message for transmission and desires that the DV11 transmit it. The microprocessor will clear this bit whenever Transmitter NXM sets, Transmitter MPE sets, or both byte counts associated with this line are zero. The PDP-11 program may clear this bit if it is desired that a transmission be aborted.
03	Transmitter Underrun (set by microprocessor and cleared by PDP-11 program). This bit is set if the microprocessor finds, upon loading a character for transmission, that a synchronous transmitter is exhibiting a "Data Not Available" flag. The setting of this bit does not generate an interrupt or clear any other bit; it is for the programmer's information only. When the bit has been read by the program, the program should clear it.
04	Transmitter NXM (set by microprocessor and cleared by PDP-11 program). This bit sets whenever a microprocessor transmitter service routine encounters an NXM condition. The PDP-11 program should empty the NPR Status Silo and then clear this bit. The setting of this bit clears Transmitter Go.
05	Transmitter MPE (same description as Transmitter NXM, but a Memory Parity Error occurred rather than an NXM).
06	Sync Strip On (set and cleared by microprocessor). This bit sets whenever Receiver Active sets on a line whose Line Protocol Parameters bit 01 (Strip Leading Sync) is set. This bit clears whenever the first non-SYNC character arrives on that line. This bit is for use by the microprocessor only.

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Bits	Function
07	Use Alternate Tables (set and cleared by microprocessor or by PDP-11 program). Before setting Transmitter Go., the PDP-11 program should condition this bit to indicate to the microprocessor whether to start the transmission from the principal or from the alternate tables. When a byte count runs out, the microprocessor will switch to the other current address and byte count. If the other byte count is also zero, this bit will remain in that second state and "go" will be cleared.
08-09	Unused.
10	Expect BCC1 Next on Byte Count Run-out. The PDP-11 program may load this bit to indicate to the DV11 that it should expect the first eight bits of the block check character when a "marked" reception byte count reaches zero. When the DV11 processes the last character and the "marked" byte count thus reaches zero, the microprocessor will set Line Progress Register bit 05 to tell the DV11 logic that the BCC is next. This information will be used when the DV11 services the next character that arrives on this line.
11-12	Unused.
13-15	Receiver Next Mode on Byte Count Run-out. The PDP-11 program may load these bits with the receiver mode to which it desires the DV11 hardware to go when a "marked" reception byte count reaches zero.
Code	Register
1100	Transmitter Mode Bits Register This register contains three bits (00-02) which indicate the "mode" of transmission on this line. These three bits determine which of the up to eight possible control tables will be used for transmission on this line. The transmitter logic appends these bits onto the high-order end of a copy of the character to be transmitted and uses the resulting 11-bit character as an offset from the transmitter control table base address to obtain a control byte from core. The control byte contains special instructions with regard to the character that is about to be transmitted.
1101	Receiver Mode Bits Register This register contains three bits (00-02) which indicate the "mode" of reception on this line. Specifically, these bits determine which of the up to eight possible control tables will be used for reception on this line. Refer to the section entitled "Control Tables."
1110	Line Progress Register The bit assignments for the Line Progress Secondary Register are as follows:

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Bits	Function
00	Send BCC1 Next This bit is set by the microprocessor when it runs out a "marked" transmission byte count (bit 15 loaded as zero) (typical use: DDCMP) or encounters a transmitter control byte with bit 02 (send BCC next) set, typically ITB, ETB, or ETX in BISYNC. It is cleared by the microprocessor when LRC is the selected block check and has been loaded for transmission, or when the BCC1 has been loaded for transmission.
01	Send BCC2 Next This bit is set by the microprocessor when the BCC1 has been loaded for transmission. This bit is cleared by the microprocessor when the BCC2 is loaded for transmission.
02	DLE Sending In Progress This bit is set by the microprocessor when it has just loaded a DLE for transmission in response to seizure of a control byte that says to prefix a DLE. This bit is used by the microprocessor to prevent stuffing DLE characters continuously. This bit cleared by the microprocessor when the DLE has been sent.
03-04	Unused.
05	Expect BCC1 Next This bit is set by the microprocessor when it runs out a "marked" reception byte count (bit 15 loaded as zero) (typical use: DDCMP) or encounters a receiver control byte with bit 02 expect BCC next) set, typically ITB, ETB, or ETX in BISYNC. This bit is cleared by the microprocessor when LRC is the selected block check and has been received, or when the BCC1 has been received.
06	Expect BCC2 Next This bit is set by the microprocessor when the BCC1 has been received. This bit is cleared by the microprocessor when the BCC2 has been received.
07	Resynchronization Flag Character Not Found (set and cleared by microprocessor). This bit is set when the microprocessor processes a resynchronization request for this line. It is cleared when the microprocessor finds the flag character that it inserted in the silo at the time that resynchronization was requested. Characters retrieved from the silo for this line while this bit is set are discarded.
08-09	Unused.
10	Send BCC1 Next on Marked Byte Count Run-out The PDP-11 program may load this bit to indicate to the DV11 that it should send the first eight bits of the block check character when a "marked" transmitter byte count reaches zero. If this

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Bits	Function
	bit is set, the microprocessor in the DV11 will, upon reaching zero, set Line Progress Register bit 00 (see above).
11-12	Unused.
13-15	Transmitter Next Mode on Marked Byte Count Run-out The PDP-11 program may load these bits with the transmitter mode to which it desires the DV11 hardware to go when a "marked" transmitter byte count reaches zero.
Code	Register

1111	Receiver Control Byte Storage Register
------	--

This register contains a copy of the control byte fetched from the receiver control table by the DV11. When a control byte is fetched that has bit 00 (generate interrupt) set, a copy of that control byte (but with bit 00 cleared) is stored here; the interrupt causing character and its line number are moved to the Receiver Interrupt Character Register; and an interrupt request is generated. The PDP-11 program may merely take note of the arrival of this character and set System Control Register bit 08 to direct the microprocessor to resume processing the character. The microprocessor will use this copy of the control byte for that processing. The PDP-11 program can alter the contents of this register before setting SCR08 if it desires to change the character processing from that originally dictated by the control byte.

In the case of receiver interrupts generated by causes other than the fetching of a control byte with bit 00 (generate interrupt) set, a special control byte arranged for character discard, no BCC inclusion, no BCC expectation, and same mode as control byte last fetched for reception on this line, is placed in this register by the microprocessor before conditioning the Receiver Interrupt Character Register and generating the receiver interrupt request.

SPECIAL FUNCTIONS REGISTER—ADDRESS 775012 (775052, 775112, 775152)

Reserved for Maintenance. Various bits may appear here during normal operations. This register is word-addressable.

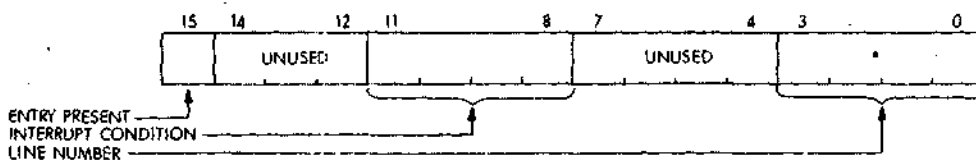
NPR STATUS REGISTER—ADDRESS 775014 (775054, 775114, 775154)

This register is a 64-entry silo-type register in that it is read once, and then a new entry "falls" into the register if additional "entries" exist at the time that the read of this register is completed.

This register reports various interrupt-causing conditions associated with the transmitter NPR hardware. Interrupt conditions related to various transmitter NPR operations are stacked in a first-in/first-out storage buffer along with the line number being serviced when this condition occurred. As soon as the program has finished reading this register once,

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a new entry is cycled into the register in place of the former entry. The interrupt is SCR 15 (NPR Status Interrupt). This register is read-only and is not clear by Initialize, except for bit 15 which is cleared by Initialize.



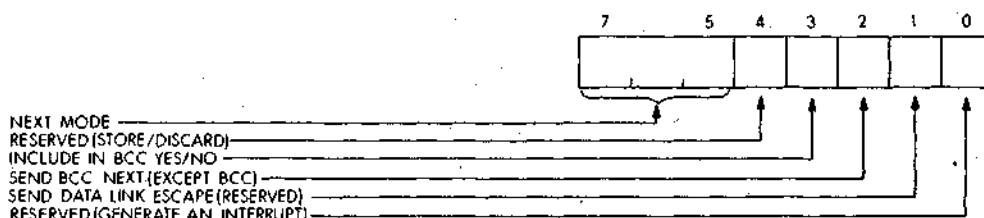
Bits	Description												
00-03	<p>Line Number</p> <p>These bits indicate which line was being serviced when the interrupt condition developed. The format of these bits is the same as bits 00-03 of the Secondary Register Selection Register (SRSR) so that the program can load these bits into the SRSR and read the appropriate current address or byte count.</p>												
04-07	<p>Unused</p>												
08-11	<p>Interrupt Condition</p> <p>These bits indicate the type of interrupt condition which occurred. The hardware is designed so that simultaneous occurrences on the same line create separate entries (Example: nonexistent memory and byte count zero both occur).</p> <p>Note that the condition codes are the addresses of the secondary registers which apply.</p> <table border="1"> <thead> <tr> <th>Code</th> <th>Condition</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>Transmitter Principal Current Address sent NPR hardware to a nonexistent memory location (NXM).</td> </tr> <tr> <td>0001</td> <td>Transmitter Principal Byte Count = 0.</td> </tr> <tr> <td>0010</td> <td>Transmitter Alternate Current Address sent NPR hardware to a nonexistent memory location.</td> </tr> <tr> <td>0011</td> <td>Transmitter Alternate Byte Count = 0.</td> </tr> <tr> <td>1000</td> <td>Transmitter Control Table Base Address—fetching control byte produced NXM or a memory parity error. The program should examine the Line State Secondary Register for further details.</td> </tr> </tbody> </table>	Code	Condition	0000	Transmitter Principal Current Address sent NPR hardware to a nonexistent memory location (NXM).	0001	Transmitter Principal Byte Count = 0.	0010	Transmitter Alternate Current Address sent NPR hardware to a nonexistent memory location.	0011	Transmitter Alternate Byte Count = 0.	1000	Transmitter Control Table Base Address—fetching control byte produced NXM or a memory parity error. The program should examine the Line State Secondary Register for further details.
Code	Condition												
0000	Transmitter Principal Current Address sent NPR hardware to a nonexistent memory location (NXM).												
0001	Transmitter Principal Byte Count = 0.												
0010	Transmitter Alternate Current Address sent NPR hardware to a nonexistent memory location.												
0011	Transmitter Alternate Byte Count = 0.												
1000	Transmitter Control Table Base Address—fetching control byte produced NXM or a memory parity error. The program should examine the Line State Secondary Register for further details.												
12-14	<p>Unused</p>												
15	<p>Entry Present</p> <p>When set, this bit indicates that bits 00-11 contain a valid entry. Reading the register or generating Initialize clears this bit. It resets when another status report entry reaches the "bottom" of the silo and can be read in bits 00-11. Bits 00-11 are meaningless unless this bit (15) is set.</p>												

RESERVED REGISTER—ADDRESS 775016 (775056, 775116, 775156)

Bits	Function
00-15	Reserved; word-addressable

CONTROL BYTE FORMATS

The DV11 achieves its high throughput and generalized operating capabilities by having both the transmitter and the receiver character-handling apparatus perform NPR cycles. The NPR cycles access byte tables in PDP-11 core to determine the next step to take with regard to the particular character being processed. The bit assignments in the control bytes are arranged such that the same control bytes may be used for both transmission and reception if the communications protocol being used progresses from mode to mode in a symmetrical fashion on both transmit and receive and provided that the same characters would be included in the Block Check Character in both transmission and reception.



Bits	Transmitter Control Byte Function	Receiver Control Byte Function
05-07	Next Mode Determines next transmission mode used on this line.	Next Mode Determines next reception mode used on this line.
04	Reserved	Store/Discard Determines whether this character is stored in message table or is discarded.
03	Include in BCC Yes/No Determines whether or not this character will be included in the BCC being accumulated for this line.	Include in BCC Yes/No Determines whether or not this character will be included in the BCC being accumulated for this line.
02	Send BCC Next Tells transmitter logic to send the 16-bit BCC after the character presently being handled. (8-bit if LRC selected).	Expect BCC Next Tells receiver logic to expect the 16-bit BCC after the character presently being handled (8-bit if LRC selected).
01	Send Data Link Escape Next	Reserved

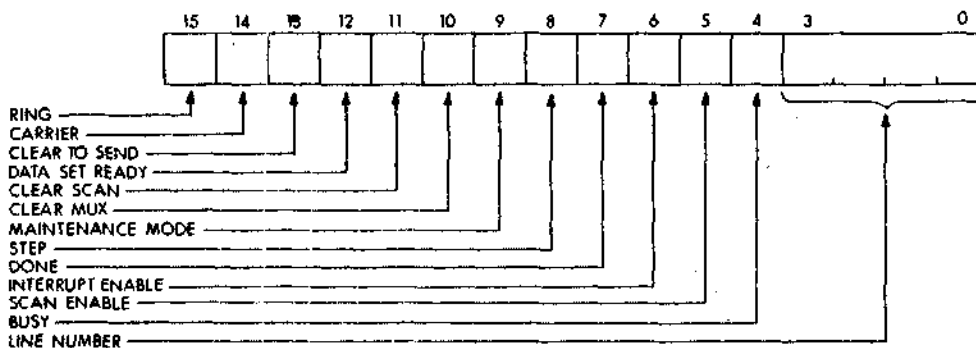
Bits	Transmitter Control Byte Function	Receiver Control Byte Function
	Tells transmitter logic to send Data Link Escape character from Secondary Register 1010 before sending the character presently being handled.	
00	Reserved	Generate an Interrupt The setting of this bit causes the character presently being processed to generate an interrupt. The microprocessor moves that character to the Receiver Interrupt Character Register and generates an interrupt request.

PROGRAMMABLE MODEM CONTROL DEVICE REGISTERS

The two programmable modem control device registers and their specific bit assignments are listed in the following paragraphs.

CONTROL STATUS REGISTER (CSR)—ADDRESS 775020 (775060, 775120, 775160)

CONTROL STATUS REGISTER (CSF)—ADDRESS 775020 (775060, 775120, 775160)



Bits	Status	Description																																										
00-03	LINE #	The LINE # bits are the binary addresses for the modem control's 16 lines (0-15) as follows:																																										
		<table border="1"> <thead> <tr> <th>Bit</th> <th>3</th> <th>2</th> <th>1</th> <th>0</th> <th>Line</th> </tr> </thead> <tbody> <tr> <td></td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td></td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td>•</td> <td>•</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td>•</td> <td>•</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td>•</td> <td>•</td> </tr> <tr> <td></td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>15</td> </tr> </tbody> </table>	Bit	3	2	1	0	Line		0	0	0	0	0		0	0	0	1	1					•	•					•	•					•	•		1	1	1	1	15
Bit	3	2	1	0	Line																																							
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				•	•																																							
	1	1	1	1	15																																							

Bits	Status	Description
		If the Scan is cleared by INITIALIZE or CLR SCAN, the Line # Register will settle in $16\mu\text{s} \pm 10\%$. When settled, the Line # Register will be set to Line #0(0000).

NOTE

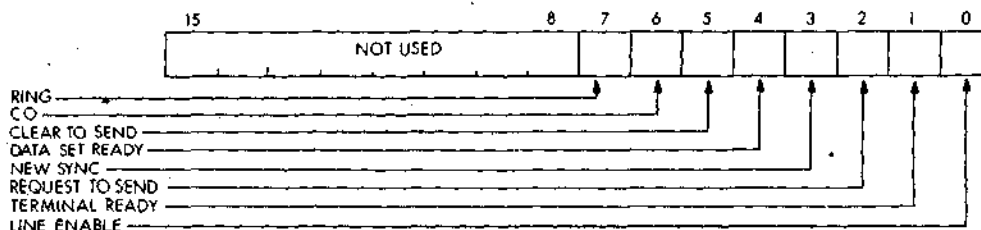
When the Scan is enabled (or STEP), the next line to be tested will always be Line # +1. These bits are Read/Write and are cleared by INITIALIZE and by CLR SCAN.

04	BUSY	<p>BUSY provides a program indicator that is set to 1 when the Scan is cycling. This bit is particularly useful to determine when a CLR SCAN (bit 11) has completed the task of cycling 0's into the Scanner's memory elements.</p> <p>In addition, this bit must be tested for 0 if SCAN ENABLE was turned off preparatory to changing the Line #.</p> <p>In Interrupt Mode, this procedure guarantees that detected transitions are serviced before the Line # is changed. (If functioning with interrupts OFF, then DONE should be tested after BUSY is found to be 0.)</p>
05	SCAN EN	<p>The SCAN ENABLE flip-flop allows the scan to "free run," testing all lines sequentially if the DONE flip-flop is cleared.</p> <p>When the SCAN EN flip-flop is set to 1 and DONE is 0, a ring counter is allowed to cycle in the following order (from Rest):</p> <ol style="list-style-type: none"> 1. Increment line counter. 2. Store contents of memory (Line # Address) in the HOLD flip-flop. 3. Write current modem status into memory. 4. Compare HOLD and contents of memory for interrupt conditions. <p>The ring counter continues to cycle (1 to 4) if DONE remains 0 and SCAN EN is set. If the SCAN EN flip-flop is negated while the ring counter is cycling (i.e., DONE not set) the ring counter will come to rest in $1.2\mu\text{s} \pm 10\%$. The Line # Register must not be changed until BUSY (bit 04) is found to be 0. This bit is read/write and cleared by INITIALIZE and CLR SCAN.</p>

Bits	Status	Description
06	INTER EN	If set to 1, Interrupt Enable allows DONE to cause an interrupt on priority four. This bit is read/write and cleared by INITIALIZE and CLR SCAN.
07	DONE	The DONE flag, when set to 1, indicates that the hardware Scan has detected a transition on CARRIER, SEC RX, CS, or the RING modem Status leads. Additionally, DONE freezes the SCAN which makes available to the programmer: <ol style="list-style-type: none"> 1. The Line # that caused the interrupt. 2. The state of the flags (four bits). 3. Modem Status (eight bits). This bit is read/write and cleared by INITIALIZE and CLR SCAN.
08	STEP	STEP, when set to 1, causes the Scan to increment the Line # and test that line for interrupts causing transitions. STEP can be used in place of SCAN EN, but care should be exercised that the Scan rate is great enough (milliseconds) so that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires $1.2\mu\text{s} \pm 10\%$ to execute. This bit is write 1's only.
09	MAINT MODE	When the MAINT MODE flip-flop is set to 1, it conditions the Scan Input (RING, CLEAR TO SEND, CARRIER, and SEC RX) to a 1 or ON state. Utilizing STEP or SCAN EN with MAINT MODE exercises 100 percent of the scan logic (not the data multiplexers). This includes the interrupt circuits and the address selector. <p>This mode provides a diagnostic feature, as well as an on-line test facility for the modem control's interaction with the UNIBUS. This bit is read/write and is cleared by INITIALIZE and CLR SCAN.</p>
10	CLEAR MUX	CLEAR MUX clears the REQUEST TO SEND, TERMINAL READY, SEC TX, and LINE EN flip-flops for all lines, when this bit is set to 1. This bit is write 1's only.
11	CLEAR SCAN	CLEAR SCAN clears all active functions (line #, SCAN EN, etc.) and the memory logic, when this bit is set to 1. The memory logic requires $18.8\mu\text{s} \pm 10\%$ to cycle a CLEAR through the memory locations. This function is especially

Bits	Status	Description
		useful if the programmer requires knowledge of the ON states of CARRIER, CLEAR TO SEND, RING and SEC RX. When the Scan is enabled (or STEP) following a CLR SCAN, an interrupt will occur for all ON states as they will appear (to the logic) as OFF-to-ON transitions.
12	DSR	The DATA SET READY flag is 1 if an ON-to-OFF or an OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED or CLR SCAN.
13	CS	The CLEAR TO SEND flag is 1 if an ON-to-OFF or OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED or CLR SCAN.
14	CO	The CARRIER flag is 1 if an ON-to-OFF or OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED and CLR SCAN.
15	RING	The RING flag is 1 if an OFF-to-ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is read-only and presents 0 when INITIALIZED and CLR SCAN.

**LINE STATUS REGISTER (LSR)—ADDRESS 775022
(775062, 775122, 775162)**



Bits	Status	Description
00	LINE EN	<p>The LINE ENABLE flip-flop, when asserted, enables RING, CO, CS, and SEC RX to be sampled (line status) by the program, and to be tested for transitions.</p> <p>This bit is read/write and is cleared by INITIALIZE and CLEAR MUX.</p>
01	TERM RDY	<p>Controls switching of the data communications equipment to the communication channel (via modem).</p> <p>Auto-Dial and Manual Call origination: Maintains the established call.</p> <p>Auto-Answer: Allows "handshaking" in response to a RING signal.</p> <p>This bit is read/write and is cleared by INITIALIZE and CLEAR MUX.</p>
02	RS	<p>When REQUEST TO SEND is set to 1, it conditions the modem for transmit if the communications channel has been established (switched network). This bit is read/write and is cleared by INITIALIZE and CLEAR MUX.</p>
03	NS	<p>The New Sync (201) flip-flop, when 1, presents a high to the New Sync lead. This bit is read/write and is cleared by INITIALIZE or CLEAR MUX.</p>
04	DSR	<p>When the state of the modem's Data Set Ready lead is a high, this bit is a 1. The DSR bit is inhibited when the LINE EN flip-flop is 0. This bit is read-only.</p>
05	CS	<p>This bit reflects the current state of the modem CLEAR TO SEND lead. An ON indicates that the modem is ready to transmit data. This lead is most often the result of the REQUEST TO SEND lead. The CS bit is inhibited when the LINE EN flip-flop is 0. This bit is read-only.</p>
06	CO	<p>This bit reflects the current state of the modem carrier detect lead. An OFF indicates that the received signal is unsuitable for demodulation. The CO bit is inhibited when the LINE EN flip-flop is 0. This bit is read-only.</p>
07	RING	<p>Set to 1 whenever the ring line from the modem selected by bits 00-03 of the CSR is on, provided that the line enable bit for that modem has been set.</p>

NOTE

The Line Status Register bits 04-07 are inhibited when LINE EN is 0.

DV11

SPECIFICATIONS

System Addresses

The DV11 uses the same address space as the DM11-A. The first DV11 in a system would be at 775000; the next at 775040; then 775100; and finally, 775140. If there are DM11-A's in the system already, the first DV11 would be at 775040. The DV11 data handling and modem control use a total of ten registers.

Interrupt Vectors

Each DV11 requires three interrupt vectors—two for the data handling section and one for the modem control. The interrupt vectors are in the floating vector space that starts at 300. The DV11 modem control follows the DM11-BB which follows the DN11. The DV11 data handling section follows the DUP11 which in turn follows the DU11.

Timing Considerations

The modem control timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan either to run free (SCAN EN) or to be sequentially stepped through the line counter line-by-line (STEP bit of CSR). The read/write cycles of the modem control scan logic force the program to wait, after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's read/write cycles prevent halting the scan and changing the line number with one machine cycle.

Programs should not spin on flags in the DV11 secondary registers using loops less than 30 (octal) instructions; to do so may interfere with DV11 RAM microprocessor/UNIBUS access interlocks.

Order Numbers

DV11-AA—Double System unit contains all DV11 logic except the line cards and distribution panels. No lines are implemented.

DV11-BA—Line cards and distribution panel for eight lines. Requires 5¼ inches of cabinet space. Two DV11-BA's can be used with one DV11-AA.

To configure an 8-line DV11, order one DV11-AA and one DV11-BA.

To configure a 16-line DV11, order one DV11-AA and two DV11-BA's.

Bus Loads

Two bus loads.

Power Consumption

15 amps @ +5 volts.

1 amp @ -15 volts.

0.5 amps @ +15 volts.

Environmental

+10° to +50°C. with a relative humidity of 20% to 95%.

DV11

Space Requirements

DV11-AA: two system units (SU's)

DV11-BA: 5¼ inches of cabinet space (SM PAN)

Cables

Order BC05D-25 modem cables. 7.6m 25-conductor cable terminated in cinch DB25S socket at one end and cinch DB25P plug at the other.

Internal Clock

The DV11 includes an internal clock which can be used when two PDP-11's are connected locally without modems. It is also useful for diagnostic purposes. The clock speed can be set at 1200, 2400, 4800, or 9600 baud, switch-selectable for each 4-line group (0-3, 4-7, 8-11, 12-15).

GT40

GRAPHIC DISPLAY SYSTEM, GT40



DESCRIPTION

The GT40 is a low-cost, high-performance graphic display system which operates through a powerful general-purpose computer. The GT40 is designed for applications which require both visualization and computation. The system can display either alphanumeric information or graphic information such as drawings, diagrams, or patterns. It is especially valuable for displaying dynamic, fast changing information such as wave forms. Designs and layouts can be plotted in minutes instead of hours, then instantly modified using the light pen. Designers are free to concentrate on layout while the system handles the calculations. And, the computer can easily monitor a check list to make sure every detail is included.

System

The GT40 is a multipurpose system. It is a graphic display system which

GT40

operates through a sophisticated terminal connected to a PDP-11 mini-computer. When not engaged in graphics tasks, it is a general-purpose computer which can operate as a stand-alone system or initiate dialogue with a central computer as part of a computer network.

The GT40 consists of seven parts: central processor, display processor, light pen, keyboard, communications interface, memory, and bootstrap read-only memory.

The central processor is a 16-bit processor with standard PDP-11 instruction set capability and 8K words of memory. Because the GT40 has its own programmable, general-purpose processor, expansion to keep pace with increased needs and changing requirements is always possible.

For example, the GT40 can be programmed to simulate any alpha-numeric or graphic terminal. A programmable terminal also permits the use of different line protocol and allows different interfacing requirements to be satisfied. The PDP-11 UNIBUS makes interfacing easy because the diversity of inexpensive peripheral and communications options simply plug in. All of the peripheral equipment available for use on PDP-11 family computers can be used by the GT40. As the system grows, it is only necessary to modify the software to meet almost any change.

The display processor performs the most popular graphic techniques quickly in hardware with minimum central processor overhead. The heart of the GT40, it fetches data and commands from memory, interprets and executes these commands, and performs all vector and character calculations. The display processor consists of the UNIBUS control, the data and instruction processor, the vector generator, the character generator and CRT monitor. A solid-state light pen is provided to facilitate interaction with the system.

The keyboard is free-standing, full-ASCII encoded with serial output coupling directly into the central processor. Character capability includes ASCII upper and lower case with italics and special characters. A separate eight-key function pad is located adjacent to the operator's keyboard for convenience in entering instructions.

The communications interface is a flexible, serial, asynchronous interface with both EIA level and 20 milliampere current loop output capability for unrestricted intercomputer dialogue and data flow. It also has multibaud rates and separate transmit and receive timing.

The 8K memory is supplemented by a 256-word read-only memory which contains the programming required to read in a program or initiate dialogue with a timesharing computer.

Operation

Because the GT40 uses digital techniques, it is a stable system which requires only minimum adjustments. The vector function operates through a combination of digital and analog techniques, providing a good compromise of speed and accuracy and assuring a precise digital vector

GT40

calculation. The presentation and accumulation of vectors mean that every point of the vector is available in digital form.

During plotting, the end-point position is automatically and accurately held, preventing accumulated errors or drift. The vectors are of near constant velocity and are time-efficient regardless of length. Four different vectors—solid, long dash, short dash, and dot/dash—are available in hardware. The smooth ramp deflection signal permits fast vectoring with moderate deflection of band width and power.

The GT40 character generator has both upper and lower case capability with a complete repertoire of displayable characters. The display is the automatically refreshing type rather than the storage type so that a bright, continuous image with excellent contrast ratio is provided during motion or while changes are being made in the elements of the picture. A hardware blink feature is applicable to any characters or graphics drawn on the screen. A separate line clock in the display permits the GT40 to be synchronized to line frequency of 60 Hz. Scope resolution is precise enough to allow overprinting.

The terminal includes logic for descender characters such as "p" and "g", positioning them correctly with respect to the text line. In addition to the 96 ASCII printing characters, 31 special characters are included which are addressed through the shift-in/shift-out control codes. These include some Greek letters, architectural symbols, and math symbols. Characters can be drawn in italics simply by selecting the feature through the status instruction bit. Eight intensity levels permit varying the brightness and contrast so that the scope can be viewed even in a normally lighted room.

The instruction set consists of four control-state instructions and five data-state formats. The control instructions set the mode of data interpretation, set the parameters of the displayed image, and allow branching of the instruction flow. Data can be interpreted in any of five different formats, allowing multiple tasks to be accomplished efficiently from both a core usage and time standpoint. The graph/plot feature of the GT40 automatically plots the X or Y axis according to preset distances as values for the opposite axis are recorded.

SPECIFICATIONS

CRT

Viewable Area	6.75" x 9"
Brightness	> 30 foot lamberts
Contrast Ratio	> 10:1
Spot Size	20 mils at 30 foot lamberts (FWHM)
Phosphor	P39 (medium-long persistence)
Pincushion	± 1% of full scale to best fit line

DISPLAY CONTROLLER

General

Resolution	10 bits (1024 words x 1024 words)
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GT40

Viewable Size	1024 words horizontal, 768 words vertical
Paper Size	12 bits (4096 words)
Hardware Blink	Programmable
8 Intensity Levels	Programmable
Line Frequency Synchronization	Programmable
Characters	
Font	6 by 8 dot matrix
Characters/Line	72
Lines/Frame	31
Character Set	96 ASCII—upper and lower case, 31 special symbols (Greek letters, math symbols, etc.)
	Italics for the above printing characters (programmable)
Control Characters	Carriage return, line feed, backspace & bell
Vectors	
Relative Vectors	Just give ΔX and ΔY of the move
Arbitrary Vectors	Can draw at any angle on the screen
Vector Writing Rate	~ 200 μs for full-screen vector (min)
Vector Types	4—solid, long dash, short dash, dot/dash—all programmable
Points	
Point Plotting Rate	~ 20 μs /point
GENERAL INFORMATION	
Word Length	16 bits
CPU Instruction	Entire PDP-11/10 Instruction Set
Display Processor Instruction	Set Graphic Modes (3 registers)
	Jump
	No-op
Data Formats	Character (2 char/word)
	Short Vector (1 word)
	Long Vector (2 words)
	Point Mode (2 words)
	Relative Point Mode (1 word)
	Graph Plot X, Y (1 word/point)
Keyboard	Full ASCII keyboard with separate function keys
Light Pen	Solid-state light pen
Communication Controller	Asynchronous dialogue
	Separate RECEIVE and TRANSMIT speeds up to 9600 baud
	Capable of driving EIA data leads, with full data set control

GT40

SPECIFICATIONS

Mechanical

Mounting: table top unit
 Size: 18"H x 20"W x 24"D
 Weight: 150 lbs.

Power

Input current: 15 A at 115 VAC
 Heat dissipation: 1500 W

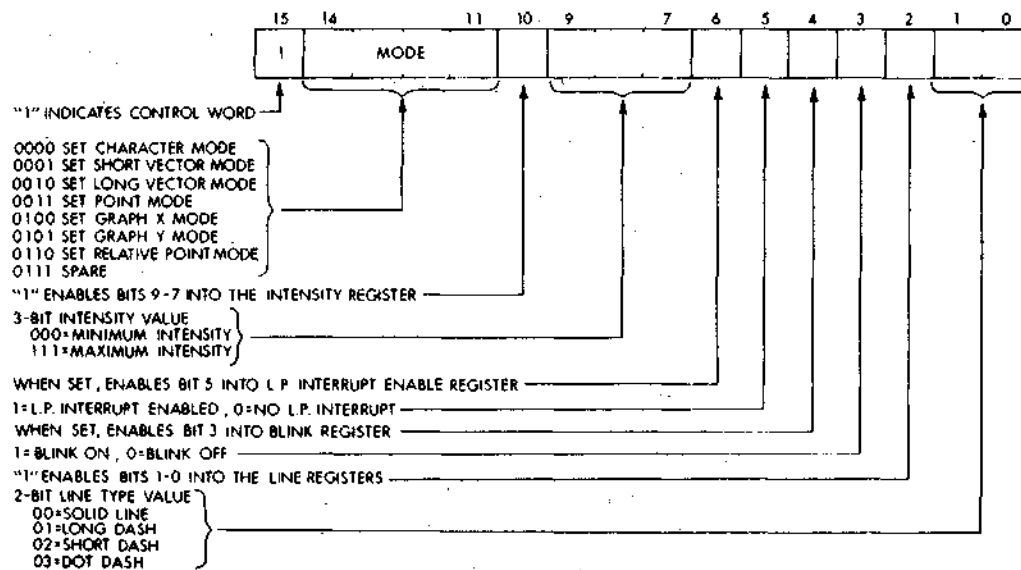
Environment

Operating temperature: 15°C to 32°C
 Relative humidity: 20% to 80%

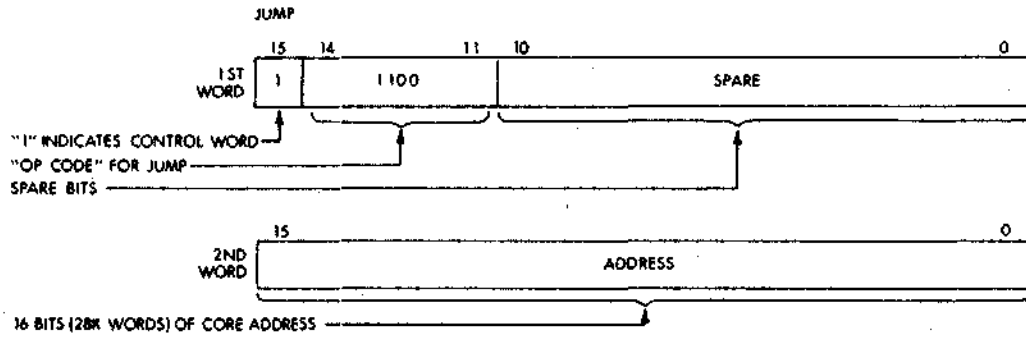
GT40 INSTRUCTION SET

The basic instruction set for the GT40—Set Graphic Modes, Jump, No-Op, and Load Status Registers—is simple, concise, and powerful. It is augmented by the versatility of the PDP-11 CPU instructions which are executable by the GT40.

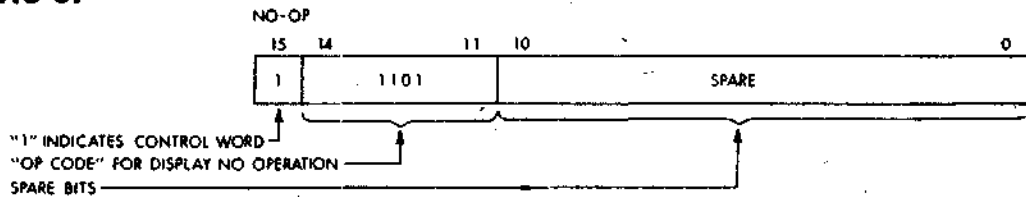
SET GRAPHIC MODE



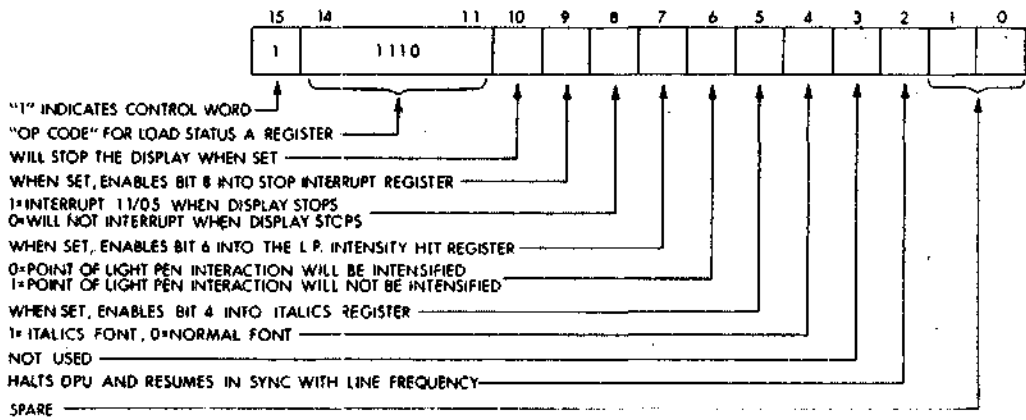
JUMP



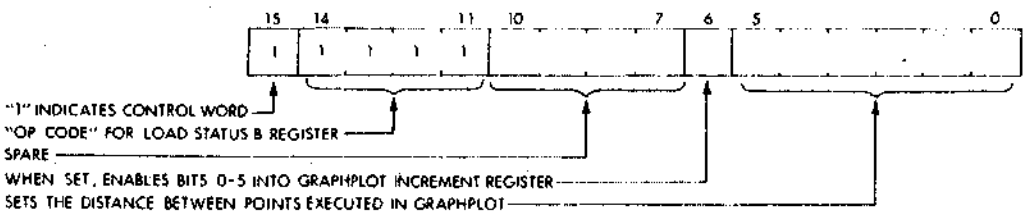
NO-OP



LOAD STATUS REGISTER A



LOAD STATUS REGISTER B



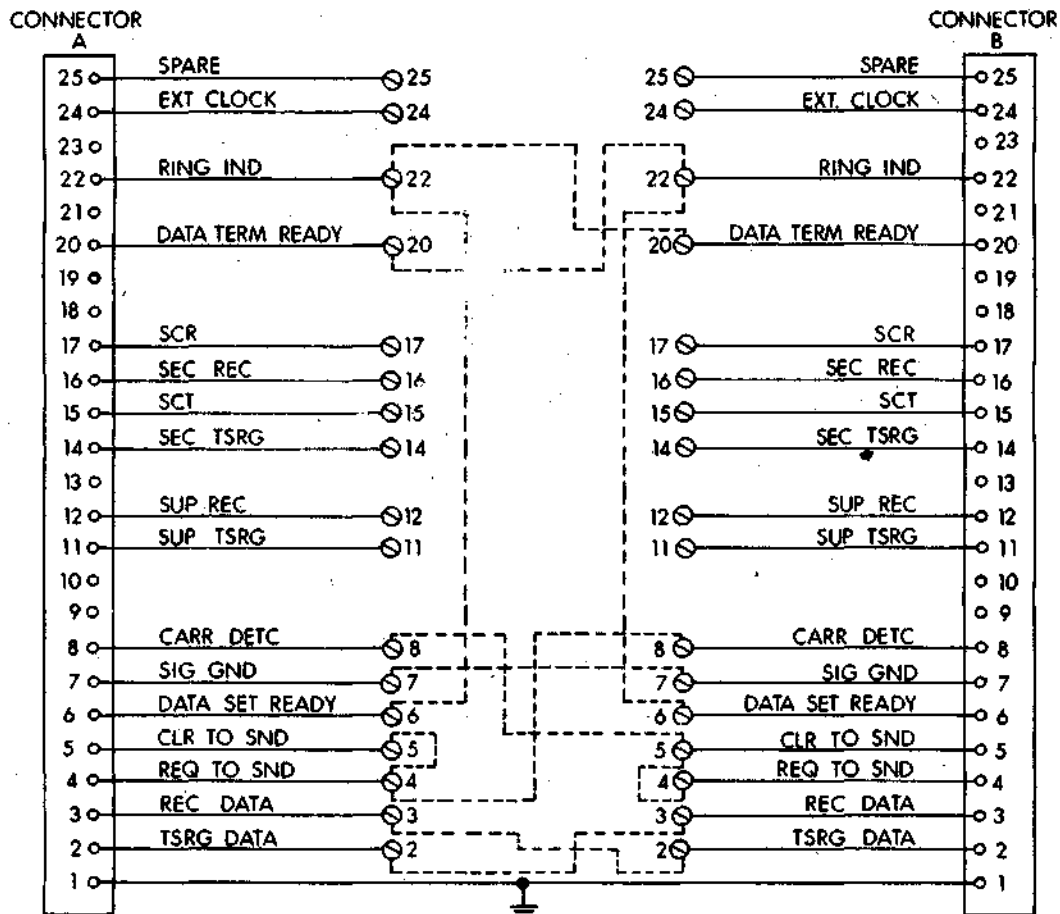
H312

ASYNCHRONOUS NULL MODEM, H312-A

ASYNCHRONOUS NULL MODEM, H312-A

The H312 null modem allows a user to connect a terminal device to a computer without the use of two modems as would be normally required. It consists of two female 25-pin data-phone sockets mounted on a printed circuit board with the 15 most commonly used wires brought out to split lugs in the center of the board. The split lug allows the user to interconnect the two sockets in any way he wishes as long as the pins used are on the split lug interconnection points.

The H312 is wired (as shown below) to simulate back-to-back Bell 103A's. However, the user may make wiring modifications.



UNLESS OTHERWISE INDICATED:
CONNECTORS ARE DB25S-3
⊗ = SPLIT LUGS
----- WIRE JUMPERS TO BE SOLDERED
TO SPLIT LUGS.

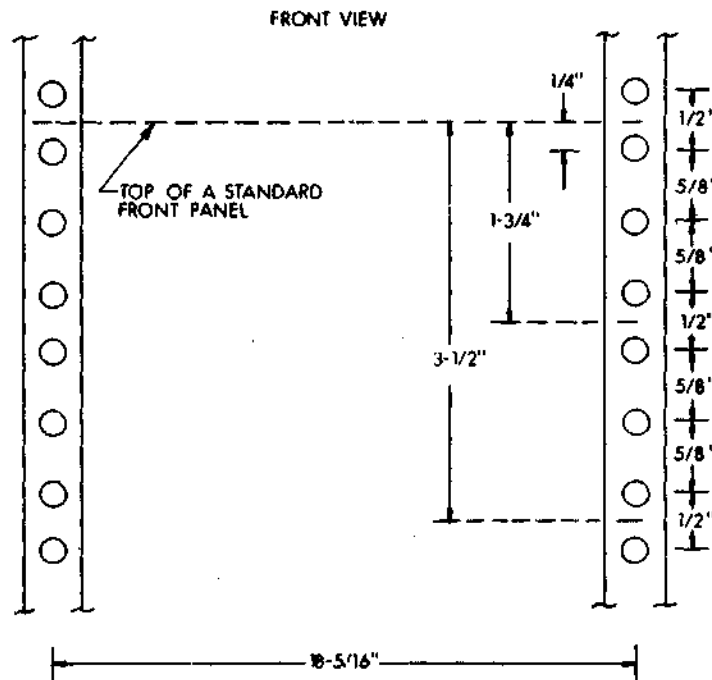
STANDARD PDP-11 CABINET, H960

Cabinets

The standard PDP-11 cabinet is 72" high by 21" wide by 30" deep. It has mounting space for six 10½" front panel units of equipment. Each cabinet contains a power control and switched AC outlets so that all equipment within the cabinet (and other connected cabinets) can have their power turned on and off together.

The cabinet can mount standard 19" wide equipment, and has two rows of mounting holes in the front, spaced 18⅝" apart. The holes are located at ½" or ⅝" apart from each other, see the following diagram. Standard front panel increments are 1¾".

$$(\frac{5}{8} + \frac{5}{8} + \frac{1}{2} = 1\frac{3}{4})$$



Standard PDP-11 Cabinet

H960-C

The H960-C is a basic PDP-11 cabinet with power control, fans, extension feet, but no power supplies.

H960-D

The H960-D cabinet has a sliding extension mounting box drawer which fits in the lower half of the cabinet. The sliding drawer provides mounting space for 9 System Units (SU). Power supplies are provided to furnish a total of:

H960

75 Amps at +5 V
1 Amp at +15 V
8 Amps at +20 V
1 to 8 A at -5 V
10 Amps at -15 V

Note: The current available from the -5 V supply is 1 Amp plus the amount of +20 V current being drawn, up to a maximum of 8 Amps.

The component parts are:

H742	Power supply with room for 5 regulators; includes input transformer and mechanical housing.
H744	+5 V regulator (3 per H960-D)
H745	-15 V regulator
H754	+20 V/-5 V regulator

Specifications

Size: 72"H x 21"W x 30"D

Weight: 120 lbs (H960-C)
300 (H960-D)

Input Power: 90 to 135 VAC, 47 to 63 Hz, 24 A max
180 to 270 VAC, 47 to 63 Hz, 16 A max

Models:

H960-CA:	Cabinet, 115 VAC
H960-CB:	Cabinet, 230 VAC
H960-DH:	Cabinet with sliding drawer and power supplies, 115 VAC
H960-DJ:	Cabinet with sliding drawer and power supplies, 230 VAC

EXTENDED ARITHMETIC UNIT—(EAE), KE11**FEATURES**

- Fast
- Plugs into UNIBUS
- Overlaps processor operations
- Provides signed integer multiply and divide
- Provides signed normalize and multiple shifts

DESCRIPTION

The PDP-11 EAE option executes high-speed arithmetic operations. This system performs signed integer multiply (16 bit x 16 bit), signed integer divide (32 bit/16 bit), and signed normalize and multiple shifts either with sign extension or filling with zeros.

Timing

The execution times for actual EAE operation are:

Multiply	6.6 μ sec.
Divide	7.4 μ sec.
Normalize	0.5 to 6.6 μ sec.
Logical Shift	0.5 to 6.6 μ sec.
Arithmetic Shift	0.5 to 6.6 μ sec.

This unit is a bus peripheral. Hence, there is overlap between its operation and the fetch and address decoding of the instruction used to fetch the results from it. This overlap provides an approximate 1.2-microsecond increase in system operational speed over a comparable "wait for completion" system.

Programming Considerations

The PDP-11 EAE option is a fast signed integer arithmetic unit on the UNIBUS. All registers are read/write and therefore it can be used by reentrant programs. This peripheral is driven by addressing its registers according to their significance as defined in the attached table. A multiply would be initiated by moving the multiplicand to 777306.

Addressable Registers

The registers, their significance and their addresses are:

Register Name	Bits	Address	Significance
DIVIDE	0-15	777300	When the divisor is moved to this address, the 32 bit dividend in the AC & MQ is divided by this number.
AC (Accumulator)	0-15	777302	High order word of arithmetic unit. Contains high order product on multiply, remainder or high order dividend on divide.

KE11

MQ (Multiplier Quotient)	0-15	777304	Low order word of arithmetic unit. Contains low order product or quotient on divide.
MULTIPLY	0-15	777306	When the multiplicand is loaded into this address, the EAE begins the multiplication of this number by the number in the MQ.
SC (Step Count)	0-5	777310	The step count contains the count for long shifts and the step count following normalize.
SR (Status Register)	0	777311	On shifts contains last bit shifted out of MQ or AC.
SR	1	777311	Indicates that result is single word and is in MQ.
SR	2	777311	Indicates that result is zero.
SR	3	777311	MQ is zero.
SR	4	777311	AC is zero.
SR	5	777311	AC is all 1's.
SR	6-7	777311	These bits indicate sign and overflow conditions.
NORMALIZE		777312	Writing into this address results in the 32 bit number in the AC being normalized. Reading this address fetches the shift count.
LOGICAL SHIFT	0-5	777314	Output to this address results in a logical shift of the AC & MQ (filling with zeros) the specified number of bits.
ARITHMETIC SHIFT	0-5	777316	Output to this address initiates an arithmetic shift of the AC & MQ (sign extension) with the shift count being the value moved to this address.

Multiply and divide operations would be programmed as follows:

```

MOV #MQ, R0                ;set up EAE address
.
.
.
MUL:  MOV A,(R0) +         ;put first number in MQ
      MOV B,(R0)          ;multiply by second number
      MOV -(R0), C        ;pick up low order product
      MOV -(R0), D        ;pick up high order product
      TST (R0) +         ;bump address back
      .
      .
      .

```

```

DIV:      MOV A,(R0)           ;load low order dividend
          MOV B, -(R0)        ;load high order dividend
          MOV C, -(R0)        ;divide
          TST (R0) +          ;MOV address back to AC
          MOV (R0) +, D       ;pick up remainder
          MOV (R0), E         ;pick up quotient

```

NOTES

On multiply, if there is only a one word product, the last two steps can be ignored.

This example shows the multiplication of 10-bit signed integers in a table by a constant scaling factor with a 16-bit product replacing the data in the table. This would be the case, for example, when scaling the signed output from a 10-bit A/D by a scale factor of up to 64. The total time for each multiplication is 22 μ sec.

Time

		TABLEADD = R0	;Table start address is
		MQADD = R1	;in R0. EAE MQ ad-
		SCALE = R2	;dress in R1. Scale fac-
			;tor in R2
			;EAE multiplicand ad-
			;dress in R3 and table
		LIMIT = R4	;limit in R4
5.2	MULTILOOP:	MOV (TABLEADD),	;Move multiplicand to
3.7		(MQADD) +	;MQ
		MOV SCALE, (MQADD)	;Move multiplier to
			;EAE and start multi-
			;plication
2.8		"EAE operation occurs	;For multiply there is
		here"	;overlap between next
			;instruction execution
			;and multiply
5.2		MOV (MQADD),	;Get low order product
		(TABLEADD) +	;and store in table
2.3		CMP TABLEADD, LIMIT	;Check whether done
2.6		BLE MULTILOOP	;If not done do next
			;multiplication

22.0 μ sec*

* Total time. All times listed are typical.

COMMUNICATIONS ARITHMETIC OPTION, KG11-A

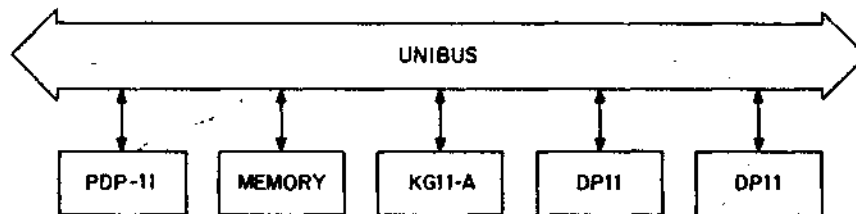
FEATURES

- Computes three different Cyclic Redundancy Check (CRC) polynomials and two Longitudinal Redundancy Checks (LRC)—CRC-16, CRC-12, CRC-CCITT, LRC-8, LRC-16
- Program selection of desired polynomial
- Fits in small peripheral slot
- Computes an 80-character message block in less than 100 microseconds

DESCRIPTION

The KG11-A is attached to the UNIBUS and is used to compute a Cyclic Redundancy Check (CRC) or Longitudinal Redundancy Check (LRC) for detecting errors in serially transmitted data. It is used with a DP11 serial synchronous line interface to compute the Block Check Character(s) (BCC) appearing at the end of a block of data transmitted over a serial synchronous line.

A typical configuration might be:



For received data, the characters are moved to the KG11-A and a BCC is computed for the data and compared to the BCC received. If they are equal, the data is assumed to be correct and is accepted. If they do not match, the message is not accepted and the data is retransmitted.

When data is being transmitted, the BCC is generated by moving all the characters to the KG11-A. The resulting BCC is transmitted at the end of the message.

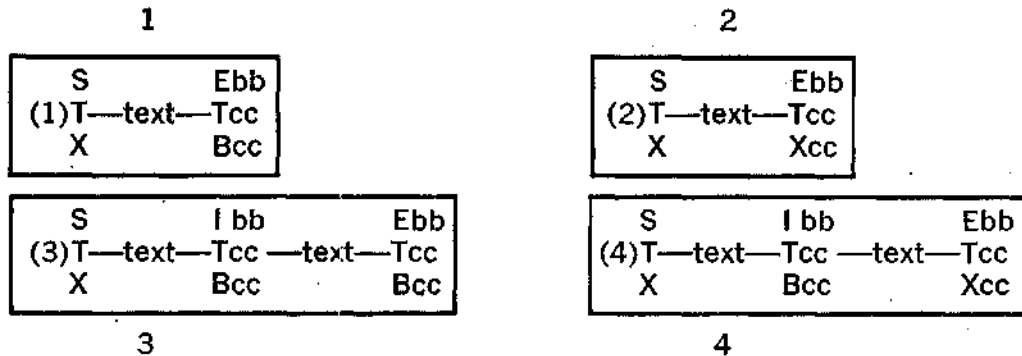
* Not all characters are included in the BCC. The exclusions will depend on the line protocol used.

The KG11-A, under program control, can compute the most popular CRC and LRC polynomials:

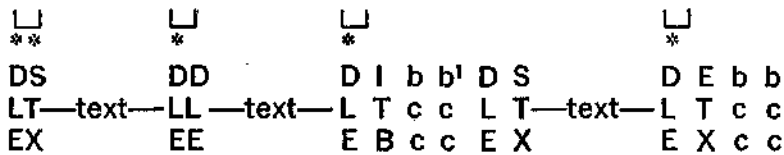
1. CRC-16 $X^{16} + X^{15} + X^2 + 1$
2. CRC-12 $X^{12} + X^{11} + X^3 + X^2 + X + 1$
3. CRC-CCITT $X^{16} + X^{12} + X^5 + 1$
4. LRC-8 $X^8 + 1$
5. LRC-16 $X^{16} + 1$

CRC-16

CRC-16 is used for synchronous systems that employ 8-bit characters. It is used in IBM binary synchronous systems when the transmission code is EBCDIC or 8-bit transparency. For IBM compatible systems, the message format is:



In the preceding examples, each character represents an 8-bit character. The first BCC character is the least significant 8 bits of the BCC computed in the KG11-A. The STX is not included in the BCC. The BCC includes the first text character through the ETB, ITB or ETX. In examples (3) and (4), the second BCC begins with the character following the first BCC in the block (even if it is an STX or DLE). The examples are for normal transmission. For transparent transmission, the characters indicated by (*) in the following example are not included in the BCC.



¹At this point, a new BCC sequence is begun which includes initialization of the BCC registers.

The DLE DLE indicates that the second DLE is really data and not the control character and is, therefore, included in the BCC. It may appear in text as often as that 8-bit representation is required. Because the DLE ITB sequence takes the system out of the transparent mode, the DLE STX following the BCC is included in the next BCC and also puts the system back into the transparent mode.

CRC-12

CRC-12 is used for six-bit characters. It is compatible with IBM Binary Synchronous Communications (BSC) when the transmission code used is Six-Bit Transcode. The characters included in or excluded from the BCC are the same as for CRC-16. The difference is only in the length of character (6 versus 8 bits).

CRC-CCITT

CRC-CCITT is the standard polynomial used to compute BCC for European systems. The characters included or excluded will depend on the line protocol used for the system in which the KG11-A is used.

KG11

LRC-8

Some systems use only an 8-bit LRC on the characters. LRC-8 performs an exclusive OR on an 8-bit or less character. The LRC is usually used in combination with a Vertical Redundancy Check (VRC). VRC is possible only when the characters are 7-bit or less plus one parity bit. LRC/VRC is used for IBM BSC when the transmission code is USACII. For IBM systems, the parity bit makes the character contain an odd number of bits.

LRC-16

LRC-16 performs an exclusive OR on a 16-bit or less character. It can be used to perform a word exclusive OR, or to compute LRC for 10, 11 and 12 bit characters transmitted via a DP11 with the DP11-CA option.

KG11-A Programming Techniques—Recommended Practice

There are two ways to use the KG11-A: Message Basis and Character by Character (Partial BCC). It is recommended that the KG11-A be used to compute on a message basis. The BCC register is Write Only. Therefore, a partial BCC has to be loaded through the data register in the LRC-16 mode. To do a partial polynomial computation (character by character), for example, a character is added to the accumulation as it is received. This can be done efficiently for one line (half duplex) because the BCC can be left in the KG11-A until all the characters have been processed. However, for full duplex and/or multiple lines, the BCC accumulation cannot be left in the KG11-A because it may have to be used for another line before the next character appears. Therefore, the partial BCC has to be saved and reloaded when the next character appears. The following sequence is required to load a partial BCC, add a character, and store the new partial BCC:

1. Set mode to LRC-16 and clear BCC
2. Load the partial BCC
3. Test DONE flag
4. Set mode to proper polynomial (don't clear BCC)
5. Load character
6. Test DONE flag*
7. Store partial BCC

* Depending on which PDP-11 processor is used, these tests may not be required for single-byte operations because the KG11-A completes the operation in one microsecond. For word operations, the maximum cycle time of the KG11-A is 2 μ sec. The KG11-A does not generate an interrupt so, if a programmer wants confirmation, he must test the DONE bit.

It is recommended that the message be passed through the KG11-A in one continuous loop operation after the entire message is received or prior to commencing transmission. If this method is undesirable, multiple KG11's can be used. For full duplex, two KG11-A's can be used, one for each direction. Addresses for eight KG11-A's have been allocated.

Figure 1 is a flow chart of the recommended practice (complete BCC). The numbers in parenthesis represent the KG11-A operations.

* Not required but may be used (see description).

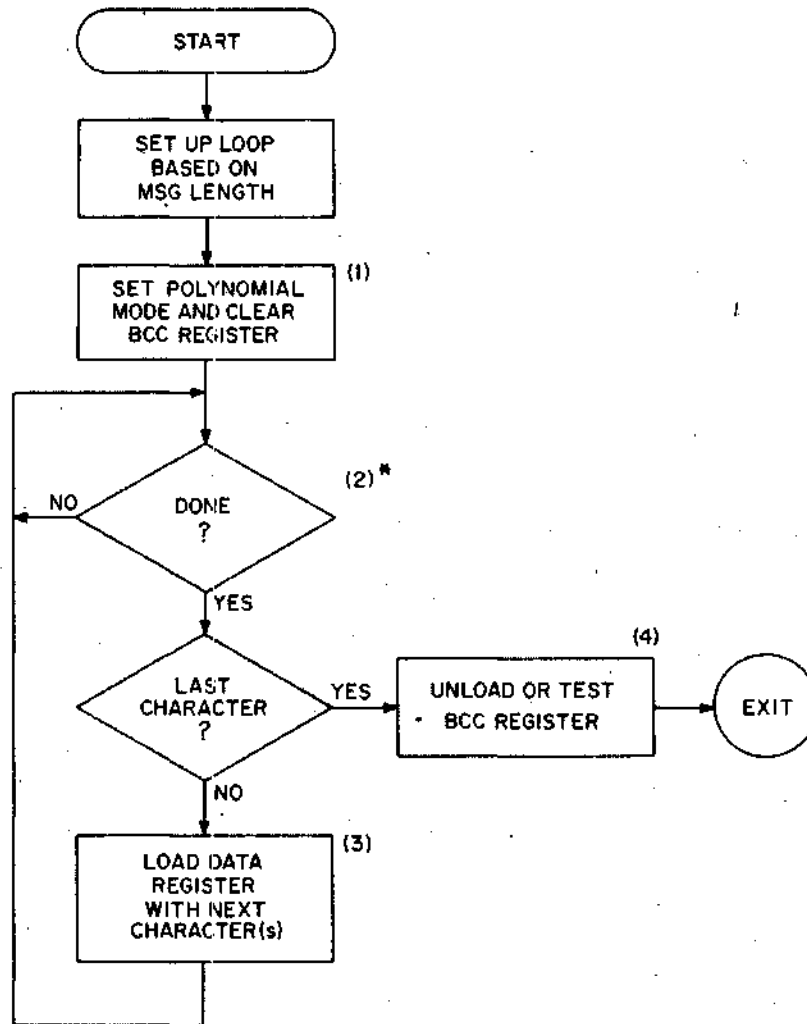


Figure 1

KG11-A Programming Registers

The KG11-A consists of these three registers:

Address	Description
7707x0	Status register
7707x2	BCC register
7707x4	Data register

Where x = 0-7, assignments for 8 KG11-A's.

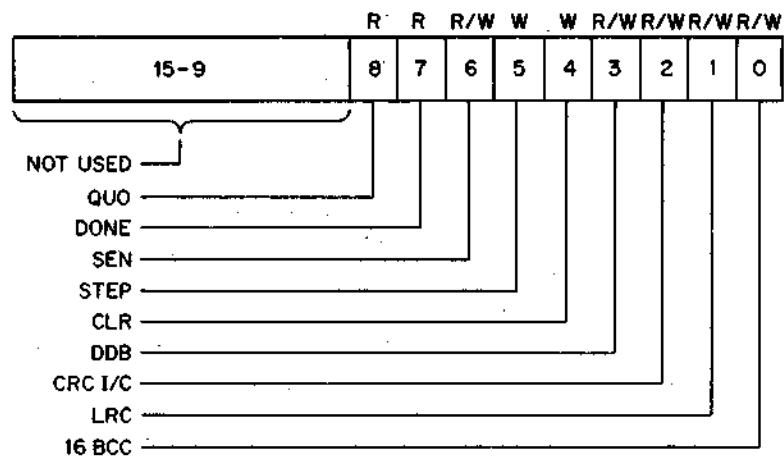
Status Register—This is a 16-bit register used to control (set mode) and to present status. Some bits are Read Only (QUO, DONE), some are Write Only (STEP, CLR) and the rest are Read/Write. Figure 2 describes the status register.

KG11

BCC Register—This is the result register and is Read Only. The format of this register will be described later for each KG11-A operational mode.

Data Register—This is a 16-bit Write Only register. It is used as the input register for the data on which the BCC is calculated. The format of the input data will be described later for each KG11-A operational mode.

STATUS REGISTER



R = Read Only
 W = Write Only (ONES)
 R/W = Read/Write

Figure 2

Initialize KG11-A ((1) in Figure 1)

The initialization procedure consists of moving a command word to the Status Register that selects the desired polynomial, indicates whether bytes or words will be presented for accumulation, indicates whether the unit is to cycle or be single stepped and clears the BCC register.

Select the Desired Polynomial

The polynomial is selected by a combination of bits 2, 1, 0 (CRCI/C, LRC, 16 BCC respectively) of the Status Register. The bit selection is as follows:

KG11

Polynomial	STATUS BIT		
	2 CRC I/C	1 LRC	0 16 BCC
1. CRC-12	0	0	0
2. CRC-16	0	0	1
3. LRC-8	0	1	0
4. LRC-16	0	1	0
5. Undefined*	1	0	0
6. CRC-CCITT	1	0	0
7. Undefined*	1	1	0
8. Undefined*	1	1	1

* The "undefined" polynomials mean the combinations will have undefined results.

Indicate Word or Byte Operation (DDB)

The purpose of this indicator is to tell the KG11-A if the data register will be loaded each time with a word (16 bits) or a byte (8 bits). Bit 3 (DDB) selects word (DDB = 1) or byte (DDB = 0). Even if characters are being accumulated, the program loop (Figure 1) is shorter if the characters can be presented two-at-a-time (WORD option).

Caution:

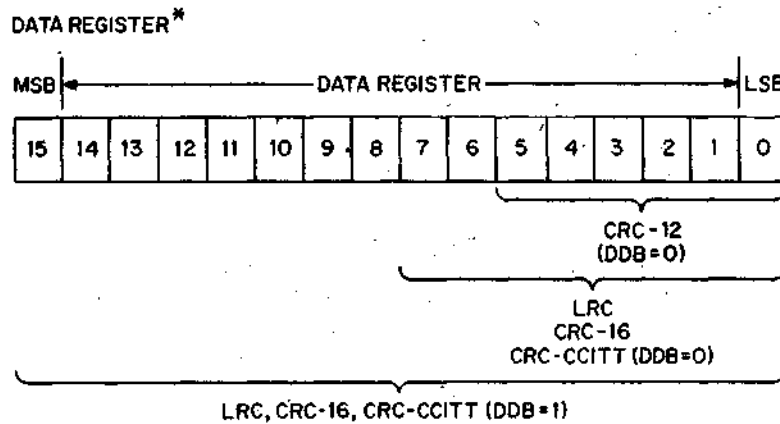
CRC computations are correct only if the characters are presented to the KG11-A in the order in which they are put on or received from the communications line. If the messages are formed (received) in byte mode, then a word move can be made to the Data Register. In other words, the message must be stored in memory in ascending order of byte address. Figure 3 shows the order of characters on the basis of words moved to the KG11-A.

Character Order

Relative Word Address		
0	2	1
2	4	3
4	6	5
6	8	7
.	.	.
.	.	.
.	.	.
.	.	.

Figure 3

The position of the data for the KG11-A option is given in Figure 4. Note that if CRC-12 is selected, double mode (DDB = 1) produces undefined results.



* Write Only
 MSB Most Significant Bit
 LSB Least Significant Bit
 CRC-12 (DDB 1) is not supported

Figure 4

Cycle or Single-Step Mode

For diagnostic purposes, the unit can be single stepped and the operation can be monitored at each step. For normal operation, a complete cycle can be initiated. The two states are set up as follows:

Operation	Status Bits	
	SEN	STEP
Cycle	1	Ignored
Single Step	0	1

Cycle Mode

Once the status register is initialized with SEN = 1, the KG11-A will perform a complete cycle each time the data register is loaded as specified in Figure 4. Once the data register is loaded, the DONE flag is inactivated until all shifting ceases and the new BCC is in the BCC Register. Elapsed time is 2 μ sec (max) for 16 data bits and 1 μ sec (max) for 8 or less data bits. The programmer can test the DONE flag (there is no interrupt unless requested) but it is not necessary for proper operation of the KG11-A.

Step Mode

The STEP bit is a gate, not a flip-flop. Each time it is set by a Bit Set instruction, the KG11-A performs one shift and exclusive OR.

The programmer can monitor the operation by examining the contents of the BCC register after each step and by testing the QUO bit (8) in the status register. The QUO bit is the result of the exclusive OR of the LSB Data Bit shifted out of the data register and the LSB Data Bit shifted out of the BCC register. This value is fed back and an exclusive OR is performed with bits in the BCC register as specified by the polynomial. By examining QUO and the BCC register, the programmer can determine whether the KG11-A is functioning properly.

KG11

Initialize BCC Register

To begin a new BCC accumulation, the BCC Register has to be cleared to zero. This can be done under program control by setting the CLR bit (4) at the same time (or independently) the polynomial is selected. CLR is a gate and the BCC register is reset each time CLR is set by the program.

Test for KG11-A Completion ((2) in Figure 1)

When the BCC register is cleared or a KG11-A cycle is complete, the DONE flag is set. When it is set, the contents of the BCC register can be used, or the data register can be loaded with the next character, pair of characters or word. On the flow chart (Figure 2), the DONE flag is set the first time because of the initialization in (1). Each time thereafter, it is set because a new character has been loaded into the data register and is added to the BCC accumulation.

If the programmer wishes, he does not have to test the DONE flag before proceeding. The KG11-A is fast enough to complete its cycle while the program is testing to see if there are more characters to accumulate.* The DONE flag is provided for testing purposes in case of malfunctions of the KG11-A.

* This may not be true for all PDP-11 processors.

Load Data Register With Next Character(s) ((3) in Figure 1)

The manner used to load the data register depends on the polynomial and the DDB flag. Figure 4 shows the bits that have to be loaded for each operation.

Once initialized, the act of loading the data register by a MOV(B) instruction initiates a cycle that results in the data being processed and added to the BCC accumulation in the BCC register. When shifting starts, DONE is cleared. When the shifting is complete, the data register is clear and DONE is set.

Note: The data is to be right justified in the data register. If double byte mode is used, the leading character is to be in the right byte and the trailing character in the left byte. The Data Register operation assumes the least significant bit of each byte to be to the right (low bit number of the register).

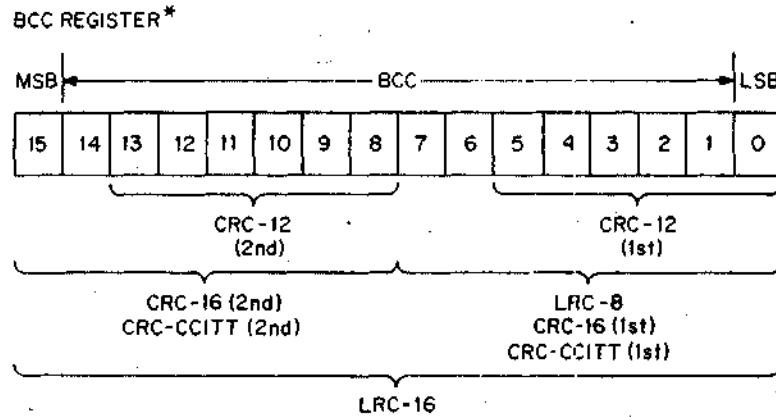
Unload BCC Register ((4) in Figure 1)

Once the CRC (or LRC) has been performed on the message, it is ready to use. If the value is the BCC of a received message, the value can be compared to the received BCC characters. In this case, the value does not have to be moved out of the register to perform the comparison. Alternatively, the received BCC may be included in the accumulation. A good BCC will result in a zero accumulation.**

** When ITB is used, the BCC that follows can be included in the accumulation. The results should be zero. If the rest of the message is accumulated without testing for zero, the only way the final BCC (after ETB or ETX) can compare is if the intermediate BCC's caused the accumulation to go to zero. This method will reduce the operations on the KG11 because the BCC does not have to be reset after the ITB, and only one loop has to be set up.

KG11

If the BCC is for a message to be transmitted, the contents of the BCC register can be moved to the message buffer for subsequent transmittal. The format of the data in the BCC register is different for each polynomial type. The formats are displayed in Figure 5.



* Read Only

Figure 5

Applications

The KG11-A can be used in any application where error detection and correction of serially encoded data are required. The source can be conventional communication channels, paper tapes or magnetic tape recording provided the required CRC or LRC polynomial is one of the options of the KG11-A.

Configurations

The number of KG11-A's required on a system will depend upon the number of messages requiring concurrent calculation of block check characters. When used in conjunction with the DP11, the following number of KG11-A's is recommended:

Number of DP11's at 3KB

Number of KG11-A's	
FULL DUPLEX	HALF DUPLEX
1-4	1
5-8	2

KW11-L

LINE TIME CLOCK, KW11-L

DESCRIPTION

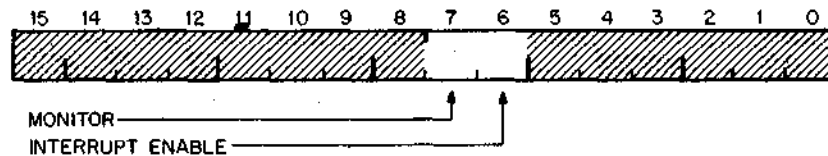
The KW11-L Clock divides time into intervals, $16\frac{2}{3}$ msec or 20 msec, determined by the line frequency, 60 Hz or 50 Hz. The accuracy of the clock period is that of the frequency source.

There are two modes of operation:

Interrupt Mode—An interrupt is generated for each cycle of the line frequency.

Non-Interrupt Mode—The program checks a Monitor bit for timing information.

Clock Status Register (LKS) 777 546



Effect of the Initialize (INIT) signal: clear bit 16, set bit 7.

BIT	NAME	FUNCTION
7	Monitor	Set by the line frequency clock signal and cleared by the program.
6	Interrupt Enable	Set to allow Monitor = 1 to cause an interrupt. Determines mode of operation; 1 = interrupt, 0 = non-interrupt.

SPECIFICATIONS

Main Specifications

Time intervals:	$16\frac{2}{3}$ msec at 60 Hz line frequency 20 msec at 50 Hz
Operating modes:	Interrupt Non-Interrupt

Register Address (LKS) 777 546

UNIBUS Interface

Interrupt vector address:	100
Priority level:	BR6
Bus loading:	1 bus load

Mechanical

Mounting:	(Within main CPU assembly)
Size:	1 single height module

Power 0.8 A at +5 V

KW11-P

PROGRAMMABLE REAL-TIME CLOCK, KW11-P

FEATURES

- Four clock rates, program selectable
- Crystal-controlled clock for accuracy
- Two external inputs
- Three modes of operation
- Interrupts at 50 or 60 Hz line frequency

DESCRIPTION

The KW11-P Clock provides programmed real-time interval interrupts and interval counting in 3 modes of operation. The major functional units of the Clock include:

16-bit Counter—Counts up or down at 4 selectable rates and can be read while operating. The interrupt sequence is initiated at zero (underflow) during a count down from a preset interval count. The count-up mode is used to count external events; an interrupt is initiated at 177 777 (overflow).

16-bit Count Set Buffer—Stores the preset interval count. At underflow, depending on the operating mode, the buffer automatically reloads the Counter or is cleared.

Control and Status Register—Provides various control and status signals related to the operation of the buffer and counter.

Clock—Provide 2 crystal-controlled signals of 100 kHz and 10 kHz to clock the counter. Two external clock inputs are provided: 50/60 Hz line frequency and a TTL-compatible signal input.

MODES OF OPERATION

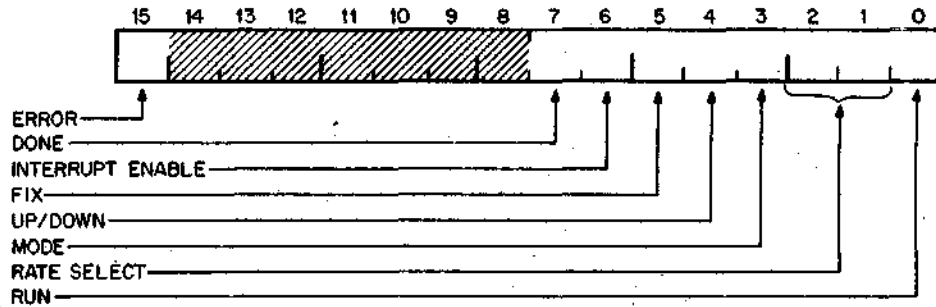
Single Interrupt Mode—A program specified time interval is preset and an interrupt is generated at the end of the interval. The time interval, represented as a specific count, is loaded into the counter. Count down or count up is initiated at 1 of 4 selectable rates, and at underflow or overflow an interrupt is generated. Clocking is stopped and the counter is reset to zero.

Repeat-Interrupt Mode—A program specified time interval is preset and repeated interrupts are generated at a rate corresponding to the time interval. Operation is similar to the Single-Interrupt Mode, except that after the interrupt is generated on underflow or overflow, the counter is automatically reloaded from the count set buffer, and clocking is restarted. At the next underflow or overflow, another interrupt is generated.

External Event Counter Mode—The external input is used to clock the counter in the count-up or count-down mode. The counter may be read during operation to determine the number of events that have occurred.

REGISTERS

Control and Status Register 772 540



Effect of the Initialize (INIT) signal: clear all bits.

Read only: bits 15 and 7

Write only: bit 5

BIT	NAME	FUNCTION															
15	Error	Set when, in Repeat-Interrupt Mode, a second underflow or overflow occurs before the interrupt of the preceding one has been serviced. It is cleared when the Status Register is addressed and by internal gating. It is only valid during the first serviced interrupt after the error.															
7	Done	Set on underflow or overflow.															
6	Interrupt Enable	Set to allow Done = 1 to cause an interrupt.															
5	Fix	Set to cause single clocking of the counter as a maintenance aid.															
4	Up/Down	Selects either count-up or count-down for the counter; 1 = up, 0 = down.															
3	Mode	Selects interrupt mode of operation; 1 = Repeat-Interrupt, 0 = Single-Interrupt.															
2,1	Rate Select	Selects 1 of 4 available clock rates.															
		<table border="1"> <thead> <tr> <th>Bit 2</th> <th>Bit 1</th> <th>Rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>100 kHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>10 kHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>Line frequency</td> </tr> <tr> <td>1</td> <td>1</td> <td>External</td> </tr> </tbody> </table>	Bit 2	Bit 1	Rate	0	0	100 kHz	0	1	10 kHz	1	0	Line frequency	1	1	External
Bit 2	Bit 1	Rate															
0	0	100 kHz															
0	1	10 kHz															
1	0	Line frequency															
1	1	External															
0	Run	Set to allow the counter to count. Cleared on underflow or overflow in Single-Interrupt Mode.															

Count Set Buffer Register 772 542

This 16-bit register is used for storage of the interval count. It allows automatic reloading of the Counter in Repeat-Interrupt Mode. The register is cleared by the INITIALIZE signal and by underflow or overflow in the Single Interrupt Mode. The bits are write only.

Counter Register 772 544

This 16-bit register is a binary up/down counter. It is cleared by the INITIALIZE signal. The bits are read only.

PROGRAMMING

1. Read the counter prior to stopping it. Stopping the counter might change its contents. If it is necessary to start the counter from a previous value, save the value which was read, and reload if required.
2. Do not loop on a counter read command.
3. The latest version is equipped with a hardware synchronization feature which will add from zero, up to one clock interval (of the selected rate) to the anticipated count time on the first interrupt, after the run bit is asserted.

SPECIFICATIONS**Main Specifications**

Clock rates:	100 kHz } 10 kHz } crystal-controlled
	Line Frequency External (Schmitt Trigger input)
	Oscillator stability: $\pm 0.01\%$
Operating modes:	Single Interrupt Repeated Interrupt External Event Counter Non-Interrupt

Register Addresses

Control and Status	772 540
Count Set Buffer	772 542
Counter	772 544

UNIBUS Interface

Interrupt vector address:	104
Priority level:	BR6
Bus loading:	1 bus load

Mechanical

Mounting:	1 SPC slot (quad module)
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Power	0.5 A at +5 V
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DECWRITER II PRINTER, LA35**FEATURES**

- True 30 character per second throughput via the use of a 16 character buffer and 60 cps catch up mode.
- 7 x 7 dot matrix impact technology print head
- Up to 6 part forms (.020 maximum pack thickness)
- Variable width forms handling—from 3" through 14 $\frac{7}{8}$ " wide forms via adjustable width tractor feed
- 132 column print; 10 characters per inch horizontal spacing
- 6 lines per inch vertical spacing
- 128 character ASCII upper/lower case set (95 printable characters)
- Extra quiet operation
- Crisp, clear and straight character formation
- Integrated 20 ma current loop interface. Passive mode standard with jumpers to activate the active mode
- Fine vertical adjustment for accurate forms placement
- Adjustable right and left hand tractors for margin positioning
- 90-132 VAC or 180-264 VAC operation to insure reliable operation in brown-out conditions
- Parity check prints replacement character (III). Strappable to odd, even, or none with mark or space
- Last character visibility (after 1300 ms timeout, head moves 4 columns to the right. Returns automatically when printing is resumed)
- Integral stand
- Rear door lock
- Top cover interlock
- Print window
- Power on indicator (Std. character lamp)
- Paper out (straps to send timed break or disconnect line)

OPTIONS AND ACCESSORIES

Paper stacking tray

Caster for rear of cabinet

Ribbons

Paper

Compressed font print (132 col. in 8")

EIA interface with timed disconnect, auto answer and modem control

DF11 mount to house Digital's DF11 series integral modem

Expansion options mounting kit

Variable length form feed/top of form control

Horizontal tab

Vertical tab

- Automatic line feed
- Automatic 20 character answerback using unique "DIP switches" as memory
- Selective addressing
- Acoustic coupler
- APL/ANSI dual character set

DESCRIPTION

The LA35 DECwriter II is an advanced technology teleprinter designed to offer fast reliable operation. The DECwriter II is equally at home in communications applications or in slave printer applications.

The DECwriter II is loaded with many practical functional and operator features. Among these are the true 30 cps throughput accomplished by a 60 cps catchup mode which is activated any time more than one character is present in the 16 character buffer. Also featured are quiet 48 db operation, infinitely variable vertical forms adjustment vernier, variable width and up to six part forms handling and countless other features.

The integral stand design always provides correct height for easy operator viewing of the printed line.

OPERATION

Simple elegant designs in all subassemblies allows the DECwriter II to perform like the precision machine it is.

CARRIAGE SYSTEM

The carriage system quietly transports the print head along a solid bar platen. An operator adjustable print gap allows the print head distance to be tuned for the highest quality print on every forms thickness. The carriage is driven by a quiet direct drive servo motor system at 3 or 6 inches per second (6"/second for catchup mode). A photo cell and slotted disk encoder system located right on the motor shaft provide oscillation free feed-back control to the micro-processor controlled servo system. Upon power up, the servo system is initialized by seeking out the left hand carriage stop and positioning .2 inches to the right to establish the location of column 1.

PAPER FEED

The DECwriter II paperfeed system uses a stepper motor drive system for positive line location. A direct gear drive linkage drives the two adjustable width pin feed paper tractors to straight line drive up to 6 parts of continuous forms with no loss of registration between the first and the sixth copies. Fine positioning of the paper is possible by pushing in on the line feed knob to release the gear drive linkage and rotating the knob to move the paper in the desired direction. A paper out sensor is also standard equipment on the DECwriter II. With the LAXX-EIA option, a paper out condition can be strapped to send a break signal or disconnect the telephone line.

Print Head

The print head system in the DECwriter II is a key element of the DECwriter II's success story. The print head uses a ruby jewel head bearing

to guide the seven solenoid driven print wires that make up the 7 x 7 character matrix. The DECwriter II's print head is designed to last a long time. In fact, with a typical head life of 5-7 years under average usage, you might call it a life time print head. Such reliability is possible because of sophisticated design details such as designing the curvature of the print wire guide tubes to match the natural curvature of the print wire.

RIBBON FEED SYSTEM

To prevent the ribbon from smudging the paper when the DECwriter II is not printing, the ribbon feed system is driven from the carriage servo system. Thus, ribbon motion only takes place with head motion. The DECwriter II's single plane ribbon travel system make the long lasting 40 yard spool of nylon ribbon easy to remove and replace. Ribbon reversing is automatically accomplished by the sensing of a metal eyelet located at either end of the ribbon.

POWER SUPPLY ASSEMBLY

The option upgradable DECwriter II's use a constant voltage transformer (CVT) to insure reliable operation over a wide voltage swing to allow continued operation under brown-out conditions. All 60 Hz upgradable DECwriter II's use the same transformer with simple tap changes to change from the 90-132V range to the 180-264 range. Likewise, all 50 Hz upgradable DECwriter II's use a dual voltage range transformer. The heavy duty supplies contain adequate power to handle all of the DECwriter II options.

OPERATOR CONTROLS

Power ON/OFF	This rocker switch located on the operators control panel applies or removes AC power to the entire machine.
Line/Local	This pushbutton on the operators control panel selects the on line or off line (local) mode of the DECwriter II.
Baud Rate 110, 150, 300	The two pushbuttons labeled 110 and 300 baud on the operators panel are used to select the communications line speed at which the DECwriter II will receive data. As indicated on the bezel above the keys, both depressed will select 150 baud operation.
Head of Form	This pushbutton located on the operator's panel is active only when one of the forms control options are installed in the DECwriter II. With one of the options installed, depressing this button will cause the forms to advance to the beginning of the next form as defined by the forms length control switch which is part of the forms control option.
Forms Thickness Adjustment	Located on the right side of the print head carriage, this adjustment selects the proper gap for 1 through 6 part form.

LA35

Tractor Position Adjustment	Located on each paper tractor assembly, these thumb screw adjustment allow movement of the paper tractors to set up margins and paper widths.
Fine Vertical Tractor Release	The line feed knob may be depressed inward and rotated in the appropriate direction for precise location of printing with respect to vertical zones.

CONTROL PANEL INDICATORS

Paper Out	This lamp indicates that the DECwriter II has run out of paper.
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SPECIFICATIONS

Main Specifications

Printing Speed:	10, 15 or 30 characters/second asynchronous
Number of Print Columns:	132
Printing Characters:	63/95 character ASCII (Excludes space)

Printing

Type Font:	Impact 7 x 7 dot matrix technology
Vertical Spacing:	6 lines per inch
Horizontal Spacing:	10 characters per inch

Paper

Type:	3"—14 ⁷ / ₈ " wide continuous forms tractor driven. One to six parts (up to 20 mils maximum pack thickness).
Slew speed:	30 lines per second

Mechanical

Mounting:	Self-contained unit with integral stand
Size:	33.2 inches H x 27.5 inches w x 24 inches D
Weight:	102 lbs. uncrated—140 lbs. crated

Power

Input Current:	Maximum no options—2A Maximum with options—5.5A
Heat dissipation:	300 watts printing maximum (no options) 700 watts printing maximum (options) 160 watts non printing (no options) 350 watts non printing (options)

Environment

Operating temperature:	10°C to 40°C
Relative humidity:	10% to 90%
Altitude:	0 Ft. to +8,000 ft. mean sea level
Ribbon:	Digital-specified nylon fabric, spool assembly 0.5 inches wide x 40 yds. Supply item #36-10558.

LA35

COMMUNICATIONS

Receive Only DECwriter II Models

LA35-CE DECwriter II, 20 ma interface 90-132 VAC, 60 Hz
LA35-CJ DECwriter II, 20 ma interface 180-264 VAC, 50 Hz

CODE	ANSI
Bit Structure	110 baud 1 start, 7 data, 1 parity, 2 stop bit 150 baud 1 start, 7 data, 1 parity, 1 stop bit 300 baud 1 start, 7 data, 1 parity, 1 stop bit
Parity	Parity. ODD, EVEN and no parity bit 8 marking or no parity with bit 8 spacing are number choices. A character with bad parity will force a substitute character (III) to be printed.

OPTIONS

The following options are available for use with the LA35. Refer to the LA36 section for descriptions of the options.

LAXX-KJ
LAXX-LG
LAXX-KH
LAXX-LB
LAXX-LA
LAXX-KX
LAXX-KV
LAXX-KY
LAXX-KW
LAXX-PK
LAXX-LM
LAXX-KB
LAXX-KD

DECWRITER II PRINTER TERMINAL, LA36**FEATURES**

- True 30 character per second throughput via the use of a 16 character buffer and 60 cps catch up mode.
- 7 x 7 dot matrix impact technology print head
- Up to 6 part forms (.020 maximum pack thickness)
- Variable width forms handling—from 3" through 14 $\frac{7}{8}$ " wide forms via adjustable width tractor feed.
- 132 column print; 10 characters per inch horizontal spacing
- 6 lines per inch vertical spacing
- 128 character ASCII upper/lower case set (95 printable characters)
- Extra quiet operation
- Crisp clear, and straight character formation
- Integrated 20 ma current loop interface. Passive mode standard with jumpers to activate the active mode.
- Fine vertical adjustment for accurate forms placement
- Adjustable right and left hand tractors for margin positioning
- 90-132 VAC or 180-264 VAC operation to insure reliable operation in brown-out conditions.
- Half or full duplex control on operators control panel
- Parity check on output prints replacement character (III). Strappable to odd, even, or none with mark or space.
- Last character visibility (after 1300 ms timeout, head moves 4 columns to the right. Returns automatically when printing is resumed).
- Integral stand
- ANSI—standard multi-key rollover typewriter-like keyboard
- 14 key numeric pad; 0-9, ., ', —, enter (CR).
- Column scale, line pointer, and column pointer
- Rear door lock
- Top cover interlock
- Print window
- Power on indicator (Std. character lamp)
- Paper out (straps to send timed break or disconnect line)

OPTIONS AND ACCESSORIES

Paper stacking tray
Caster for rear of cabinet
Right and/or left work surface
Ribbons
Paper

LA36

- Document holder
- Compressed font print (132 col. in 8")
- EIA interface with timed disconnect, auto answer and modem control
- DF11 mount to house Digital's DF11 series integral modem
- Expansion options mounting kit
- Variable length form feed/top of form control
- Horizontal tab
- Vertical tab
- Automatic line feed from carriage return key
- Automatic/Manual 20 character answerback using unique "DIP switches" as memory
- Selective addressing
- Vinyl dust cover for entire machine
- Acoustic coupler
- APL/ANSI dual character set

DESCRIPTION

The LA36 DECwriter II is an advanced technology teleprinter designed to offer fast reliable operation with the best price/performance ratio of any 30 cps teleprinter in the industry. The DECwriter II is equally at home in communications applications or computer console applications.

The DECwriter II is loaded with many practical functional and operator features. Among these are the true 30 cps throughput accomplished by a 60 cps catchup mode which is activated any time more than one character is present in the 16 character buffer. Also featured are quiet 48 db operation, infinitely variable vertical forms adjustment vernier, variable width and up to six part forms handling and countless other features.

The integral stand design always provides correct height for easy operator use of the typewriter-style keyboard.

OPERATION

Simple elegant designs in all subassemblies allows the DECwriter II to perform like the precision machine it is.

CARRIAGE SYSTEM

The carriage system quietly transports the print head along a solid bar platen. An operator adjustable print gap allows the print head distance to be tuned for the highest quality print on every forms thickness. The carriage is driven by a quiet direct drive servo motor system at 3 or 6 inches per second (6"/second for catchup mode). A photo cell and slotted disk encoder system located right on the motor shaft provide oscillation free feedback control to the micro-processor controlled servo system. Upon power up, the servo system is initialized by seeking out the left hand carriage stop and positioning 0.2 inches to the right to establish the location of column 1.

PAPER FEED

The DECwriter II paperfeed system uses a stepper motor drive system for positive line location. A direct gear drive linkage drives the two adjustable width pin feed paper tractors to straight line drive up to 6

parts of continuous forms with no loss of registration between the first and the sixth copies. Fine positioning of the paper is possible by pushing in on the line feed knob to release the gear drive linkage and rotating the knob to move the paper in the desired direction. A paper out sensor is also standard equipment on the DECwriter II. With the LAXX-LG EIA option, a paper out condition can be strapped to send a break signal or disconnect the telephone line.

Print Head

The print head system in the DECwriter II is a key element of the DECwriter II's success story. The print head uses a ruby jewel head bearing to guide the seven solenoid driven print wires that make up the 7 x 7 character matrix. The DECwriter II's print head is designed to last a long time. In fact, with a typical head life of 5-7 years under average usage, you might call it a life time print head. Such reliability is possible because of sophisticated design details such as designing the curvature of the print wire guide tubes to match the natural curvature of the print wire.

RIBBON FEED SYSTEM

To prevent the ribbon from smudging the paper when the DECwriter II is not printing, the ribbon feed system is driven from the carriage servo system. Thus, ribbon motion only takes place with head motion. The DECwriter II's single plane ribbon travel system make the long lasting 40 yard spool of nylon ribbon easy to remove and replace. Ribbon reversing is automatically accomplished by the sensing of a metal eyelet located at either end of the ribbon.

KEYBOARD ASSEMBLY

The DECwriter II features a multi-key rollover keyboard. The gold plated quadfurcated contact keyswitch array uses the experience learned from calculator keyboard designs to produce 100 million key strobe operations of reliability. Other features include a 14 key numeric pad. The new caps lock feature permits the operator to lock the alpha keys in uppercase mode while leaving the numerics and special symbols in lower case. This feature is not possible on conventional terminals using the shift lock technique.

POWER SUPPLY ASSEMBLY

The option upgradable DECwriter II's use a constant voltage transformer (CVT) to insure reliable operation over a wide voltage swing to allow continued operation under brown-out conditions. All 60 Hz upgradable DECwriter II's use the same transformer with simple tap changes to change from the 90-132V range to the 180-264 range. Likewise, all 50 Hz upgradable DECwriter II's use a dual voltage range transformer. The heavy duty supplies contain adequate power to handle all of the DECwriter II options.

OPERATOR CONTROLS

Power ON/OFF This rocker switch located on the operators control panel to the left of the main keyboard applies or removes AC power to the entire machine.

LA36

Line/Local	This pushbutton on the operators control panel selects the on line or off line (local) mode of the DECwriter II.
Half/Full Duplex	This pushbutton located on the operators control panel selects the communications mode of the DECwriter II. In full duplex mode, the keyboard is logically separated from the printer. In half duplex mode, the printer will copy all printable characters keyed on the keyboard.
Baud Rate 110, 150, 300	The two pushbuttons labelled 110 and 300 baud on the operators panel are used to select the communications line speed at which the DECwriter II will send or receive data. As indicated on the bezel above the keys, both depressed will select 150 baud operation.
ALT. CHAR SET	This pushbutton located on the operator's control panel is functional only when the dual character set option is installed in the machine. Operation of this pushbutton manually selects either the standard character set or the alternate set that is supplied as part of the dual character set option.
Char Set Lock	This pushbutton located on the operator's control panel is functional only when the dual character set option is installed in the DECwriter II. Its function is to either allow manual only or program only control of which character set is selected.
Auto LF	This pushbutton located on the operator's control panel is functional only when the auto line feed option is installed in the DECwriter II. When depressed, it will cause a CR and LF character to be transmitted whenever the CR key is depressed on the main keyboard.
Here is	Depressing this pushbutton, which is active only when the autoanswerback option is installed in the DECwriter II, will cause the contents of the answerback memory to be transmitted.
Forms Thickness Adjustment	Located on the right side of the print head carriage, this adjustment selects the proper gap for 1 through 6 part form.
Tractor Position Adjustment	Located on each paper tractor assembly, these thumb screw adjustments allow movement of the paper tractors to set up margins and paper widths.
Fine Vertical Tractor Release	The line feed knob may be depressed inward and rotated in the appropriate direction for precise location of printing with respect to vertical zones.

CONTROL PANEL INDICATORS

STD Char. Set	This indicator is used as a power on indication when the dual character set option is not present. With the option, either the standard character set or the alternate character set option are lit at all times to indicate the power on conditions.
ALT Char Set	This indicator when lit indicates that the dual character set option is installed in the DECwriter II and that the machine is under control of the second character set.
Paper Out	This lamp indicates that the DECwriter II has run out of paper.
Device Selected	This lamp, active only with the selective address option installed indicates that the DECwriter II has been selected.
Select Available	This lamp, active only with the selective address option installed indicates that the multiparty line is not in use and that the DECwriter may become the master and select one or more slaves on the line to transmit and/or receive a message.

SPECIFICATIONS**Main Specifications**

Printing Speed:	10, 15 or 30 characters/second asynchronous
Number of Print Columns:	132
Printing Characters:	63/95 character ASCII set (Excludes space)
Keyboard Characters:	96 or 128 selectable by caps lock switch

Printing

Type Font:	Impact 7 x 7 dot matrix technology
Vertical Spacing:	6 lines per inch
Horizontal Spacing:	10 characters per inch

Paper

Type:	3"-14 ⁷ / ₈ " wide continuous forms tractor driven. One to six parts (up to 20 mils maximum pack thickness).
Slew speed:	30 lines per second

Mechanical

Mounting:	Self-contained unit with integral stand
Size:	33.2 inches H x 27.5 inches W x 24 inches D
Weight:	102 lbs. uncrated—140 lbs crated

Power

Input Current:	Maximum no options—2A Maximum with options—5.5A
Heat dissipation:	300 watts printing maximum (no options) 700 watts printing maximum (options) 160 watts non printing (no options) 350 watts non printing (options)

LA36

Environment

Operating temperature: 10°C to 40°C
Relative humidity: 10% to 90%
Altitude 0 Ft to +8,000 ft. mean sea level

Ribbon Digital-specified nylon fabric, spool assembly
0.5 inches wide x 40 yds. Supply item
#:36-10558

COMMUNICATIONS

Models

LA36-CE DECwriter II, 20 ma interface 90-132 VAC 60 Hz
LA36-CJ DECwriter II, 20 ma interface 180-264 VAC 50 Hz

CODE ANSI

Bit Structure 110 baud 1 start, 7 data, 1 parity, 2 stop bit
150 baud 1 start, 7 data, 1 parity, 1 stop bit
300 baud 1 start, 7 data, 1 parity, 1 stop bit
Parity Input and output parity. ODD, EVEN and no parity bit
8 marking or no parity with bit 8 spacing are number
choices. An output character with bad parity will force
a substitute character (III) to be printed.

OPTIONS

LAXX-KJ—Compressed font option

This option changes the horizontal spacing from 10 characters per inch to approximately 16.5 CPI. This allows 132 columns to be printed in 8 inches space. A 40% reduction in paper usage is achieved allowing 132 column reports to be filed in standard file cabinets.

LAXX-LG—EIA/CCITT Interface option

This option provides an EIA RS232-C or CCITT-V24 interface for any LA36. The option includes auto answer, timed disconnect and half/full duplex logic to provide earlier LA36's with half duplex. A 9 foot cable with 25 pin data set type connector is also supplied with this option.

LAXX-KH—DF11 mounting kit

This option provides the capability to use the Digital DF11 series interface options in the DECwriter II.

LAXX-LB—Expansion options mounting kit

This option provides the expansion logic and 4 mounting spaces to mount the DECwriter II communications and forms handling options. This option also contains logic to automatically sense and activate new options as they are added to the DECwriter II.

LAXX-LA—Auto line feed option

This option allows the operator to depress the auto LF pushbutton on the operators control panel and while depressed causes the DECwriter II to transmit a carriage return and line feed character each time the carriage return button is depressed on the main keyboard. With the auto LF button up, the DECwriter reverts back to normal mode of operation. The

LA36

option also features an installers option, the ability to generate a LF automatically upon receipt of a carriage return code.

LAXX-KX—Automatic answerback/auto LF after CR

This option provides all the features of the LAXX-LA plus a manual and automatic answerback capability. The answerback option allows the terminal identification code in a mechanical memory which uses DIP switches as the memory element. The contents of this memory can be transmitted by the receipt of an enquiry (ENQ) code or by the operator depressing the "Here Is" button.

LAXX-KV—Forms Feed Option

NOTE

The host computer software must send fill characters or provide time delay to use this option.

This option consists of a single width double height flip chip module, a cable and a forms control switch unit. The forms length switch unit mounts inside the top cover above the speaker on the printer mechanism side plate. It contains an 11 position switch to select the desired forms length and a reset button which when depressed defines the present paper position as top of form. The receipt of a FF character (it can also be generated from the keyboard in HDX or local mode) causes the form to be advanced to the next top of form.

LAXX-KY—Forms Control Option

NOTE

The host computer software must send fill characters or provide time delays to use this option.

This option provides all the features of the LAXX-KV plus it provides Horizontal and Vertical tab capability. The Horizontal tab uses ESCAPE (ESC-1) to set a tab in any column (no maximum number) and an ESC-2 to clear all tabs. The vertical tab uses ESC-3 to set up to 88 vertical tabs per form and ESC-4 to clear all vertical tabs. These escape sequences can be generated from the keyboard in HDX or local mode or be received from the host computer system.

LAXX-KW—Selective Addressing Option

The selective addressing allows up to 125 DECwriter II's to share a multi party phone line. Under this scheme, each terminal printer has three addresses through which it must be selected before it will transmit or receive from the communications line. In this scheme, one station, usually a computer system acts as the master and all others perform as slaves. A DECwriter II may seize the line and act as master as well. The three address types are: 1. Broadcast address which is the BEL code. All terminals will activate when they receive this address. 2. Sub-group address—Here the customer may assign a subgroup of terminals this address and only these will activate upon receipt of this address. 3. Unique address—the customer uses this address to select only one terminal on the line. The software control of this option is too extensive

LA36

to address here. The specification should be followed closely when programming this option.

NOTE

LA35's can also use the line along with LA36's.

LAXX-PK—APL/ANSI dual character set

The APL/ANSI dual character set option allows the DECwriter II to be used as a bit pared ASCII APL terminal. With this option installed, the DECwriter II has two character sets and selection of the desired set is possible via the receipt of Switch In (SI) and Switch Out (SO) ASCII control codes or via the ALT. character set switch on the operator's control panel. The character set lock switch is used to either lock out manual control or host computer control of character set selection.

LAXX-LM—Acoustic Coupler

This option provides the DECwriter II with a built in low priced acoustic coupler capable of accepting the Western Electric Series 500 Handset or equivalent, as well as, most European handsets. It provides a capability which is similar to the Bell 103 originate only type of operation.

ACCESSORIES

LAXX-KA—Casters, Paper tray and Shelf Kit

This accessory provides a DECwriter II with two rear casters to allow the terminal to be easily moved, a paper stacking tray to catch the printer paper behind the DECwriter and a right and or left shelf area to provide operator work space.

LAXX-KB—Casters kit for DECwriter II

Kit of two casters as described in the LAXX-KA option.

LAXX-KD—Paper tray for DECwriter II

This accessory provides only the paper catcher as described in the LAXX-KA.

LAXX-KC—Shelf for DECwriter II

This accessory provides the operator work area as described in the LAXX-KA option. Two shelves can be mounted on the DECwriter II at one time.

LAXX-KN—Vinyl dust cover for DECwriter II

This accessory covers the entire top of the DECwriter II to protect it from dirt while not in use.

H981-A

This accessory provides the operator of a DECwriter II with an adjustable position document holder.

DECPRINTER I, LA180

FEATURES

- 180 characters per second
- Parallel interface
- Accommodates 6-part form (.020 maximum thickness)
- Handles variable-width forms, 3 through 14 $\frac{7}{8}$ inches wide
- 132-column print; 10-characters-per-inch horizontal spacing
- 6-lines-per-inch vertical spacing
- 128-character ASCII upper/lower case set
- 7 x 7 dot matrix
- Backspace capability
- Quiet operation
- Excellent character readability
- Fine vertical adjustment for accurate forms placement
- Paper-out switch
- Paper-out override
- Switch-selectable forms length (11 lengths)
- Drives 100-foot cable

Optional

- Paper stacking tray
- Casters for rear of cabinet

DESCRIPTION

The LA180 DECprinter I is a high-speed printer with an extensive array of standard features which makes it the most cost competitive in the industry. DECprinter I extends the field-proven technology of the LA36 DECwriter II into applications demanding higher speed capabilities.

DECprinter I has many operator features which enhance its ease of use. Included are a forms-length switch which sets the top-of-form to any of 11 common lengths, paper-out switch and alarm, and high reliability printhead. Also featured are quiet operation, infinitely variable forms adjustment, variable forms width, and multipart forms capability.

Operation

Seven solenoid-driven wires form the characters by scanning the page from left to right. The scanning motion is servo controlled, thereby assuring accurate dot placement and quiet, reliable operation. The machine prints a line at a time and automatically performs a carriage return upon receipt of a CR, LF, or FF command.

Power-Up

Upon power-up, the DECprinter I is initialized to execute incoming data. The head moves to the left and stops at column 1.

Carriage System

The carriage system transports the head along the horizontal axis of the machine, provides accurate horizontal positioning for character placement, and provides printhead adjustment for clean impressions on a variety of forms.

The carriage is controlled by a servo system which assures accurate dot placement. The servo operates in the forward direction at 18 inches per second and has a carriage return time of less than 275 ms.

Ribbon Feed System

The ribbon feed system is driven by the carriage motion only when the carriage is moving from left to right. This prevents ribbon smudging when the DECprinter is not printing.

Paper Feed System

The paper feed system is a stepping-motor-driven tractor feed. The tractor design provides 3-to-4-pin engagement of the form and a flat bed for control and positive feeding of multipart forms. Paper may be fine-positioned vertically by pushing the line feed knob inward and rotating it in the direction desired.

OPERATOR CONTROLS

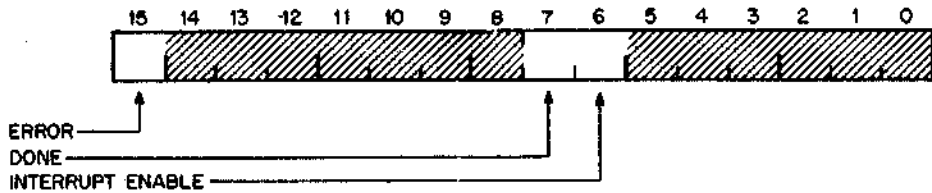
Power ON-OFF	Applies and removes AC power to entire machine.
Line/Off Line	Enables or disables communications.
Head of Form	Feeds form to the next top-of-form or single lines, if forms switch is set in single-line position. If paper is out, printing can be continued to next top-of-form by keeping Head-of-Form button depressed.
Length of Form	Selects any of 11 forms lengths.
Set VFU	Used in conjunction with Length-of-Form switch to reset forms length.
Test	Will run test pattern locally if set in this position.
Forms Thickness Adjustment	Located on right side of printhead carriage. Selects proper gap for 1-through-6-part form. Approximately 1 click for each part.
Right and Left Tractor Adjustment	Thumb screw may be loosened to allow movement of both tractors for various forms widths.
Fine Vertical Tractor Release	Line-feed knob may be depressed inward and rotated in the appropriate direction for precise location of printing with respect to vertical zones.

REGISTERS

Control and Status Register (LPS) 777 514

BIT NAME	FUNCTION
15 Error	ERROR asserted indicates the inclusive OR of one of the following line printer error conditions:

LA180

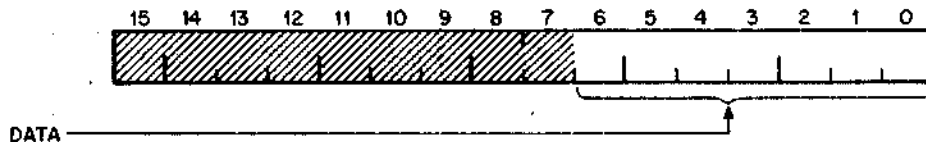


- a. Paper Empty
- b. Hardware Alarm
- c. Light Detection
- d. Select

ERROR is Read Only, and is reset only when the error condition is removed. If interrupt Enable is also set, the LA180 starts an interrupt sequence.

- 7 Done DONE is asserted when the line printer is ready to accept another character. DONE is set by INIT and cleared by loading the LPB. If interrupt Enable is also set, the LA180 starts an interrupt sequence.
- 6 Interrupt Enable Interrupt Enable is set or cleared by the program and cleared by INIT. Either DONE or ERROR set when IE is set initiates an interrupt sequence.

Data Buffer Register (LPB) 777 516



BIT NAME	FUNCTION
6-0 Data	The Data bits are the 7-bit characters transferred to the line printer. The characters are coded in ASCII and are Write Only.

SPECIFICATIONS

Main Specifications

Printing speed:	180 characters/second
Number of columns:	132
Printing characters:	96 characters ASC II set

Printing

Type:	Impact 7 x 7 dot matrix
Vertical spacing:	6 lines/inch
Horizontal spacing:	10 characters/inch

Paper

Type:	3 through 14 ⁷ / ₈ inches wide, continuous business form, original and 5 copies (.020 inch (.5 mm) maximum pack thickness)
-------	--

LA180

Single-line skip:	32 ms
Slew speed:	7.5 inches/second; 45 lines/second
Mechanical	
Mounting:	1 free-standing unit
Size:	33.2 inches (84.3 cm) high x 27.5 inches (69.9 cm) wide x 20 inches (50.8 cm) deep
Weight:	102 lbs. (46.3 kg)
Power	
Input current:	3.0A at 115 Vac 1.5A at 230 Vac
Heat dissipation:	400 W printing 200 W non printing
Environment	
Operating temperature:	10°C to 40°C
Relative humidity:	10% to 90% noncondensing, maximum wet bulb 29°C
Ribbon	
	DIGITAL-specified nylon fabric, spool assembly, (.5 inches wide x 60 yards long) Order #3612153

SPECIFICATIONS FOR CONTROL

Register Addresses

Control and Status	777514
Data Buffer	777516

UNIBUS Interface

Interrupt vector address:	200
Priority level:	BR4
Bus loading:	1 bus load

Mechanical

Size:	1 SPC slot (quad module)
Input Current:	1.5A at +5V

Models

LA180-PA:	Parallel I/O DECprinter, 115V, 60 Hz
LA180-PD:	Parallel I/O DECprinter, 230V, 50 Hz
LA11-PA:	Printer and control, 115V, 60 Hz
LA11-PD:	Printer and control, 230V, 50 Hz

HIGH-SPEED LINE PRINTER, LP11

LP11-V and LP11-W

- 300 lines per minute
- 132 columns
- Upper- and lower-case characters
- Self-test capability
- Static eliminator
- Variable-length forms switch
- Paper receptacle

DESCRIPTION

The LP11-V and LP11-W are 132-column line printers with 64 or 96 characters. The printer contains a paper advance mechanism, a top-of-form control, self-test capability, a switch to accommodate variable-length forms (11 positions, 3 to 14 inches), a static eliminator, and a paper receptacle. The printer is an impact-type using a revolving character drum and one hammer per two columns. Forms with up to six parts may be used for multiple copies. Included with the printer is a control unit for interfacing to a DIGITAL PDP-11 computer.

Operation

Paper and inked ribbon pass between a row of hammers and a continuously-rotating metal drum. The drum surface contains 132 columns of all print characters. Data to be printed is received and stored in a full line buffer. Printing starts when a control character (line feed, carriage return, or form feed) is sent. If more than 132 characters are sent before the control character, the extra characters are disregarded.

Printing is accomplished by scanning the stored characters in synchronization with the rotating drum characters and actuating the appropriate hammer as the desired characters move into the printing position. A 132-column line is printed in two drum revolutions; the odd-numbered columns in one revolution and the even-numbered columns in the other revolution.

PROGRAMMING

The LP11-V and LP11-W are program-compatible with previous LP11-series line printers. Within the control unit there are two registers, one for printer status, the other to hold the 7-bit ASCII-coded character to be printed. The same register addresses and bit definitions are used.

CONTROLS and INDICATORS

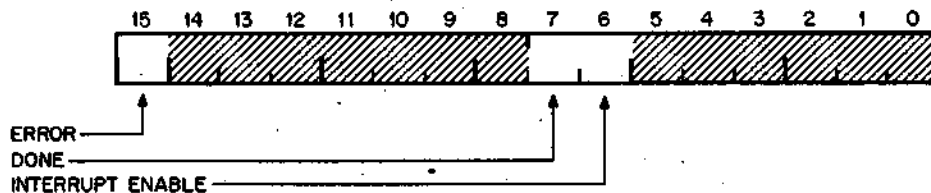
POWER ON indicator	Lights when primary power and dc voltages are ON in the printer.
READY indicator	Lights when interlocks are closed and no fault conditions exist.
ON/OFF-LINE indicator/switch	Lights when the printer is in the ready condition and the ON-LINE switch has been actuated.

LP11

SINGLE SPACE switch	Advances paper one line; disabled in ON-LINE mode.
TOP-OF-FORM switch	Advances tractors (and paper) in top-of-form position; disabled in ON-LINE mode.
VARIABLE FORMS LENGTH switch	Sets the forms length to one of 11 lengths: 3, 3½, 4, 5½, 6, 7, 8, 8½, 11, 12, and 14 inches.
ALARM/CLEAR indicator/switch	Lights when a fault condition exists, or the print-inhibit switch is ON. (The print-inhibit switch is an internal maintenance switch). Depressing the ALARM switch clears the printer logic.
Fault indicators (6 indicators)	HAMMER, FORMAT, RIBBON, GATE, PAPER, and TAPE indicators light when any of the above fault conditions exist.
Copies Control	Compensates for various forms thicknesses.
FORM ADJUSTMENTS	
Vertical Positioning	Two controls; one to move the form up or down at the print station for primary forms alignment, the second to provide line adjustment while printing.
Horizontal Positioning	Positions the forms by moving both tractors in synchronism.
6 LPI/8 LPI switch	Selects either 6- or 8-lines-per-inch to be printed.

REGISTERS

Line Printer Status Register (LPS) 777 514



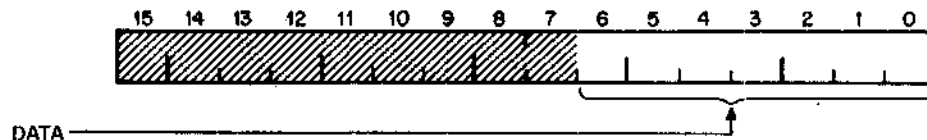
LP11

Effect of the Initialize (INIT) signal: clear bit 6

Read only: bits 15 and 7

BIT	NAME	FUNCTION
15	Error	Set when an error condition exists in the printer. Errors are: a) Power off b) No paper c) Printer drum gate open d) Over temperature alarm e) Printer placed OFF-LINE Reset only by manual correction of error condition.
7	Done	Set whenever printer is ready for next character to be loaded. Indicates that previous function is either complete or has been started and continued to a point when the printer may accept the next command. Set only by printer condition. Will not be set if printer is OFF-LINE.
6	Interrupt Enable	Set to allow Done or Error =1 to cause an interrupt.

Line Printer Data Buffer Register (LPB) 777 516



Bits 6 through 0 hold the 7-bit ASCII coded data for the character to be printed. To the processor, the data is write only.

PROGRAMMING EXAMPLE

Interrupt Service Routine

```
200:    LPSERV                ;VECTOR TO SERVICE ROUTINE
242:    200                  ;SERVICE AT PRIORITY 4
MAIN:   BIS #100,LPS         ;ENABLE INTERRUPT
LPSERV: TST LPS              ;CHECK FOR ERROR
        BMI ERROR           ;BRANCH IF ERROR
        MOV RO,-(SP)        ;SAVE RO
        MOV BUFADR,RO       ;GET BUFFER POINTER
```

LP11

```
LOAD:  MOVB (R0) + ,LPB      ;LOAD PRINTER BUFFER
        CMP R0,BUFEND        ;END OF DATA?
        BHI PRCOMP          ;YES, GO TO PRINT COMPLETE
        TSTB LPS            ;NO, CHECK DONE
        BMI LOAD            ;NOT FULL, GET ANOTHER CHAR.

EXIT:   MOV R0,BUFADR        ;SAVE BUFFER POINTER
        MOV (SP) + ,R0      ;RESTORE R0
        RTI
```

SPECIFICATIONS FOR LP11-V, W

Main Specifications

Number of columns: 132
Number of characters: 64 or 96
Printing speed: 300 lines/min. (230 lines/min. with 96 char)
Slew speed: 20 inches/sec
Line advance time: 45 msec

Printing

Method: drum
Size of characters: 0.095-inch high x 0.065-inch wide
Vertical spacing: 6 or 8 lines/inch (switch selectable)
Horizontal spacing: 10 char/inch

Character Set

64 characters: upper-case letters, numbers, symbols
96 characters: upper- and lower-case letters, numbers, symbols

Paper:

Type: standard fanfold, edge-punched, 11 switch-selectable positions between folds (3 to 14 inches), 15-lb bond for single copy, 12-lb bond with single shot carbon

Number of copies: 1 to 6
Width: 4 to 16³/₄ inches
Paper feed: One pair of pin-feed tractors for 1/2-inch-hole center, edge-punched paper

Ribbon:

Type: inked roll
Width: 15 inches
Length: 240 feet
Thickness: 0.004 inches

Register Addresses

Printer status (LPS) 777 514
Data buffer (LPB) 777 516

LP11

UNIBUS Interface

Interrupt vector
address: 200
Priority level: BR4
Bus loading: 1 bus load

Mechanical

Mounting: 1 free-standing unit +1 SPC slot
Size: 45"H x 33"W x 22"D
Weight: 340 lbs

Power

Input current: 4.5 at 115 Vac
Current for control: 1.5 at + 5 V
Power dissipation: 500 W

Environmental

Operating
temperature: 10°C to 40°C
Relative humidity: 10% to 90%, max wet bulb 28°C

Models

LP11-VA: Line printer and control, 64 characters, 115 VAC, 60 Hz
LP11-VD: Line printer and control, 64 characters, 230 VAC, 50 Hz
LP11-WA: Line printer and control, 96 characters, 115 VAC, 60 Hz
LP11-WD: Line printer and control, 96 characters, 230 VAC, 50 Hz

LP11-R and LP11-S

- Minimum wander in print line
- Simple rugged hammer mechanism
- Vernier adjustment for both horizontal and vertical paper tension
- Copies control to compensate for thickness
- Full line buffering

The LP11-R and LP11-S are fast, reliable, high quality drum printers with 64 and 96 characters respectively. Paper and inked ribbon pass between a row of hammers and a continuously rotating metal drum, containing 132 columns of all print characters. A 132-column line is printed in one drum revolution or less.

LP11

The LP11-R and S require minimum maintenance due to their modular design and integrated circuitry. Paper is loaded by opening the drum gate and placing the paper directly on the tractors. The wide swing of the gate provides complete access to the paper loading area and the print ribbon.

Operator Controls

The operator's control panel, externally located on top of the cabinet, contains the following switches and indicators.

Indicators:

Power—Illuminated when power is on.

Ready—Illuminated when power is on and all interlocks are closed.

On Line—Illuminated when printer is in the ready condition, the print inhibit switch is off, and the on line switch has been actuated.

Drum Gate—Indicates the drum gate is unlatched.

Print Inhibit—Indicates the print inhibit switch is on—Hammer Fault.

Paper Fault—Indicates the paper is torn or out: ribbon counter alarm or runaway is detected.

Switches

Top of Form—A momentary switch used to advance the tractors to a top of form position, i.e., channel zero of the tape reader. This switch is disabled when the printer is on line.

On Line/Off Line—A momentary switch that puts the printer on line and illuminates the on line indicator. In order to put the printer on line, the ready indicator must be on and the print inhibit switch must be off. If the printer is on line and the switch is actuated, the printer will go off line and extinguish the on line indicator.

Master Clear—A momentary switch that initializes the printer control electronics.

Main Power—A circuit breaker which allows the operator to enable or disable primary power to the printer.

SPECIFICATIONS FOR LP11-R, S

Main Specifications

Number of columns:	132
Number of characters:	64 or 96
Printing speed:	1200 lines/min. (900 lines/min. with 96 char)
Slew speed:	35 inches/sec
Line advance time:	20 msec

Printing

Method: drum

LP11

Size of characters: 0.095-inch high x 0.065-inch wide
Vertical spacing: 6 lines/inch
Horizontal spacing: 10 char/inch

Character Set

64 characters: upper-case letters, numbers, symbols
96 characters: upper- and lower-case letters, numbers, symbols

Paper

Type: standard fanfold, edge-punched, 11 inches between folds, 15-lb bond for single copy, 12-lb bond with single shot carbon

Number of copies: 1 to 6
Width: 4 to 19 inches

Register Addresses

Printer status (LPS) 777 514
Data buffer (LPB) 777 516

UNIBUS Interface

Interrupt vector address: 200
Priority level: BR4
Bus loading: 1 bus load

Mechanical

Mounting: 1 free-standing unit + 1 SPC slot
Size: 48"H x 49"W x 36"D
Weight: 800 lbs

Power

Input current: 17 A at 115 VAC
Current for control: 1.5 A at + 5 V
Power dissipation: 2000 W

Environmental

Operating temperature: 10°C to 40°C
Relative humidity: 10% to 90%

Models

LP11-RA: Line printer and control, 64 characters, 115 VAC, 60 Hz
LP11-RB: Line printer and control, 64 characters, 230 VAC, 50 Hz
LP11-SA: Line printer and control, 96 characters, 115 VAC, 60 Hz
LP11-SB: Line printer and control, 96 characters, 230 VAC, 50 Hz

LAB PERIPHERAL SYSTEM, LPS11**FEATURES**

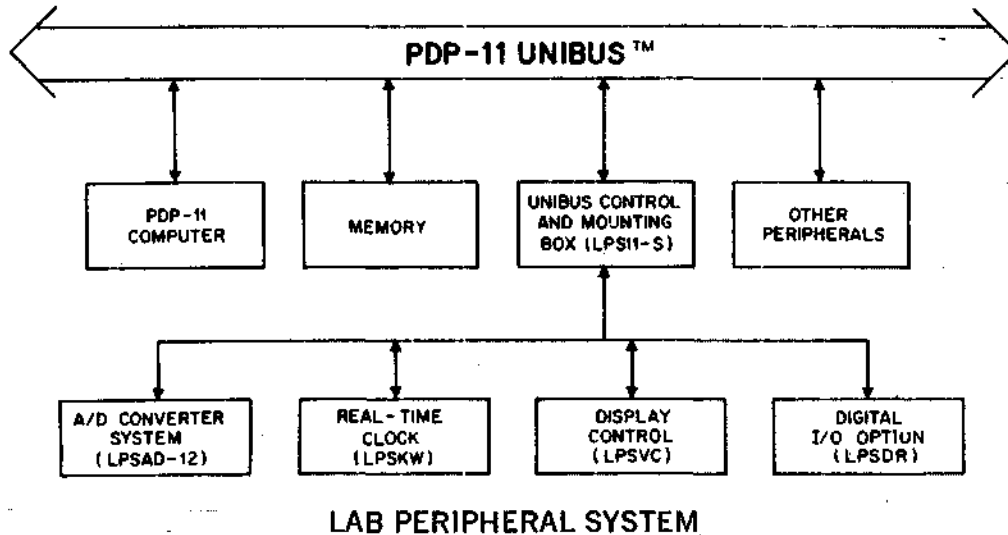
- Flexible
- Low cost
- Easy to Interface
- 5 $\frac{1}{4}$ Inches High
- 4 Plug-In Options
 - A/D Converter
 - Real Time Clock
 - Display Controller
 - Digital I/O Registers



LPS-11 Lab Peripheral System

The LPS-11 Lab Peripheral System is a high performance, modular, real-time subsystem which interfaces to the PDP-11 family of computers. The system houses a 12-bit A/D Converter, Programmable Real Time Clock, Display Controller and a 16-bit Digital I/O Option. The front panel is designed to permit easy interfacing with outside instrumentation. The LPS is 5 $\frac{1}{4}$ inches high and mounts in a standard 19-inch cabinet. All necessary power and cables are included.

The flexibility of the LPS makes it well-suited to a variety of applications including biomedical research, analytical instrumentation, data collection and reduction, monitoring, data logging, industrial testing, engineering and technical education.



A/D CONVERTER SYSTEM (LPSAD-12)

- Sample and Hold Circuitry
- Dual Sample and Hold Option
- DMA Option
- 8-Channel Multiplexer
- Optional Expansion Multiplexer
- Light Emitting Diode (LED) Display
- Differential Preamplifier Option

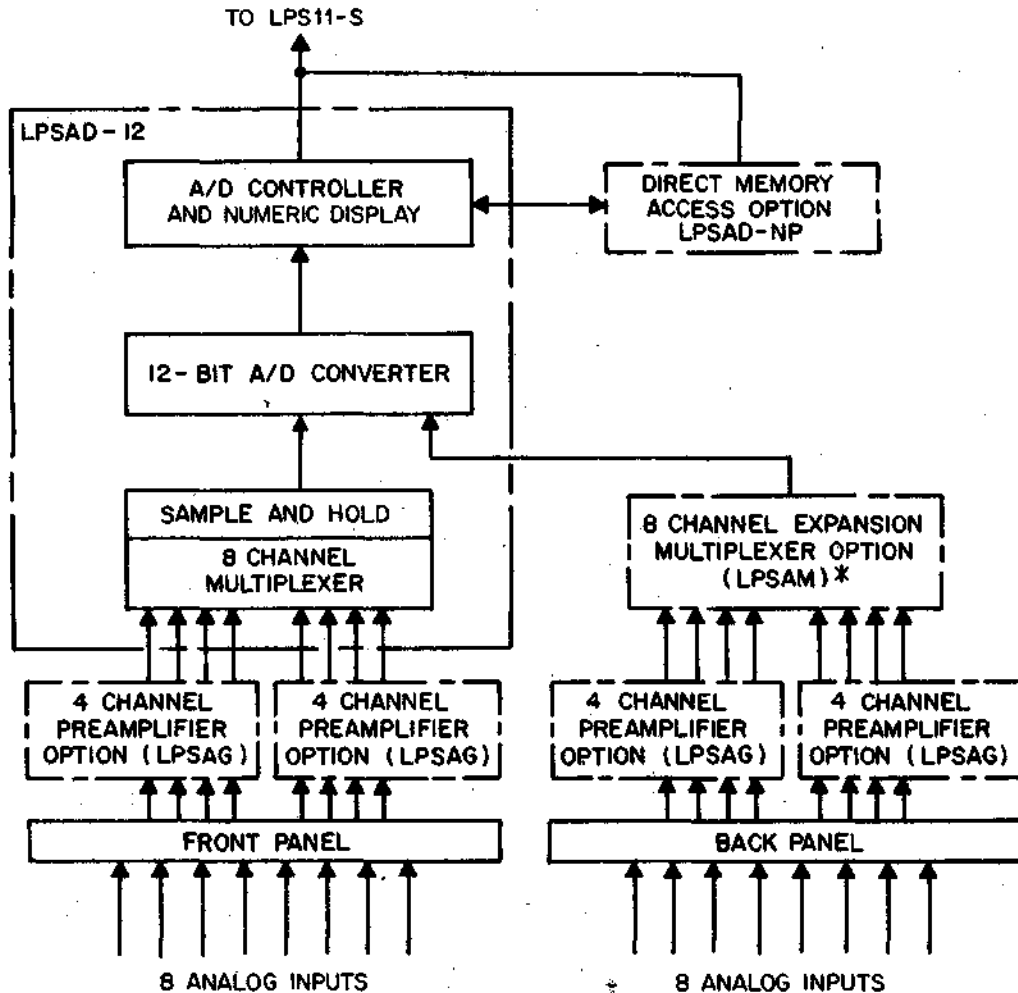
The 12-bit A/D Converter System enables the user to sample analog data at specified rates and store the equivalent digital value for subsequent processing. Sample and hold circuitry ensures accurate conversions, even on rapidly changing signals, by holding the input voltage constant until the process is completed. The throughput rate for a single channel is approximately 40 kHz.

Included in the system is an 8-channel multiplexer which provides 8 single-ended ± 5 volt inputs. Four of the channels are connected to phone jacks on the front panel and to potentiometer knobs, which can be used as program parameter inputs. The other four channels are also connected to phone jacks which permit direct interfacing with the laboratory equipment. An 8-channel expansion multiplexer option (LPSAM) may be added so that the system can handle a total of 16 channels.

The LPSAG option implements 4 channels with preamplifiers and provides a ± 1 volt differential input to the preamplifier-implemented channels. Ranges of 0 to 2, ± 5 , and 0 to 10 volts are optionally available.

A direct memory access (DMA) option (LPSAD-NP) to the A/D Converter allows the conversions to be stored in memory at maximum rates without processor intervention. The user can specify the buffer size (4K maximum) and location for the digitized data. This frees the central

LPS11



A/D CONVERTER SYSTEM (LPSAD-12)

processor for other tasks until an interrupt indicates the buffer has been filled. The throughput rate will depend on the number of bits used in the conversion. For example, for 12-bit single channel A/D operation, the throughput rate is 47 kHz; if only 10 bits are used, the rate is 75 kHz; for 8 bits, the rate is 100 kHz.

Also implemented in the system is a programmable 6-digit decimal numeric readout Light Emitting Diode (LED) display, which is mounted on the front panel of the LPS11-S. The LED display is useful for programmed visual indications.

* If a dual Sample and Hold configuration is required, the LPSSH option must be implemented. The LPSAM is prerequisite for the LPSSH.

LPS11

When speed as well as accuracy is of primary importance, a dual sample and hold configuration (LPSSH option) will enable the user to acquire data from two fixed and predetermined channels simultaneously.

PROGRAMMABLE REAL-TIME CLOCK (LPSKW)

- 5 Programmable Frequencies
- 4 Programmable Modes of Operation
- 2 Schmitt Triggers and Line Frequency
- Concurrent Operations

The LPSKW Programmable Real-Time Clock offers the user several methods for accurately measuring and counting intervals or events. It can be used to synchronize the central processor to external events, count external events, measure intervals of time between events or provide interrupts at programmable intervals. It can be used to start an analog to digital converter with the overflow from the clock counter or from the firing of a Schmitt trigger. Many of these operations can be performed concurrently.

The clock will operate in any one of four programmable modes: single interrupt, repeated interrupts, external event timing, and event counting from zero base.

The user can choose from five programmable frequencies: 1 MHz, 100 kHz, 10 kHz, 1 kHz, or 100 Hz. The real-time clock also provides an external (Schmitt trigger) input and a line frequency input.

Included with the real-time clock are two Schmitt triggers with the front panel slope and level adjusting knobs. The Schmitt triggers can start and read the clock, start the A/D converter, and cause program interrupts.

DISPLAY CONTROL (LPSVC)

- 4096 By 4096 Dot Array
- "Fast Intensification Enable" Feature
- 4 Program-Controlled Modes

The LPSVC Display Control will display data in the form of a 4096 by 4096 dot array. Under program control, a bright dot may be produced at any point in this array. A series of these dots may be programmed to produce graphical output. The display control is primarily used with DIGITAL's VR14 display. However, it has the capabilities to operate with the Tektronix RM503, 602 and 604 scopes and the 611 and 613 storage scopes.

The display control offers four program-controlled modes in which the scope can intensify a point. In addition, the "Fast Intensification Enable" feature enables X or Y register values to be changed by a small increment without a long scope settling time. This feature is useful in developing a software character generator. The display control includes two 12-bit D/A converters with ± 5 V full scale nominal output and all the necessary circuitry and controls.

DIGITAL I/O OPTION (LPSDR)

- Program Controlled Relays
- Two Modes of Program Control

LPS11

- Recoverable Overload Protection
- TTL Compatible Voltage Levels

The Digital I/O Option consists of a 16-bit buffered input register and a 16-bit buffered output register. The I/O Option features two program controlled relays which are normally left open. Using these relays, laboratory equipment such as recorders, oscillators, lamps, motors and general instrumentation may be conveniently controlled.

Program control of digital input/output can be achieved in either of two selectable modes.

Program Transfer Mode

The transfer of data between the digital I/O registers and memory may be accomplished through the use of a MOVE instruction. Flags are set when data has been received and accepted by either the input or output registers. The user program tests the data flag and determines what additional operations are necessary.

External Interrupt Mode

This mode allows an external device to initiate the transfer of data. A pulse is received from the external device and an interrupt is automatically initiated. The program is then vectored to a predetermined memory address and the user routine takes control. This mode frees the user program from having to read and clear the data transfer flags.

All voltage levels are TTL compatible with a recoverable overload protection of up to ± 20 volts. The circuits are equipped with fuse resistors to ensure protection above 20 volts.

PROGRAMMING

STANDARD* REGISTER ADDRESSES

Option	Register	Address
LPSAD-12	Status	770 400
LPSAD-12	Buffer/ Led	770 402
LPSKW	Status	770 404
LPSKW	Buffer/ Preset	770 406
LPSDR	Status	770 410
LPSDR	Input	770 412
LPSDR	Output	770 414
LPSVC	Status	770 416
LPSVC	X—D/A	770 420
LPSVC	Y—D/A	770 422
LPSVC	EXT D/A	770 424
Unused	—	770 426
Unused	—	770 430
Unused	—	770 432
Unused	—	770 434
LPSAD-NP	DMA	770 436

* The register address is jumper selectable in increments of 40 locations; however, the relative location of the various registers will remain the same (see Appendix A).

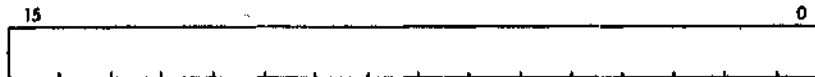
LPS11

VECTOR ADDRESSES** And PRIORITY LEVELS

Option	Address	BR Level
LPSAD-12	300	6
LPSKW	304	5
LPSDR (IN)	310	4
LPSDR (OUT)	314	4
LPSVC	320	4
UNDEFINED	324	4
LPSAD-NP	300	6

** The vector address field is jumper selectable, and will be assigned in conjunction with existing options. However, the relative positions of the option will remain constant once the initial location is determined.

LPSAD-12 STATUS REGISTER

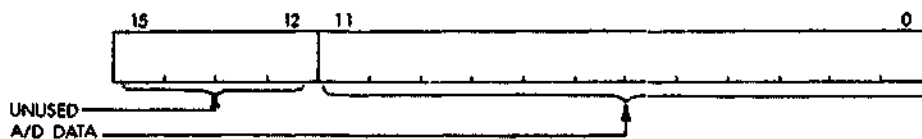


Bit	Function
15	Error Flag
14	Dual Mode Enable (LPSSH)
13-8	Multiplexer Channel
7	A/D Done Flag
6	Interrupt Enable
5	Clock Overflow Enable
4	Schmitt Trigger Enable
3	Burst Mode (LPSAD-NP)
2, 1	DMA Address Pointer (LPSAD-NP)
0	A/D Start

Bit 2	Bit 1	Function
0	0	Unused
0	1	DMA Status Register
1	0	DMA Word Count Register
1	1	DMA Current Address Register

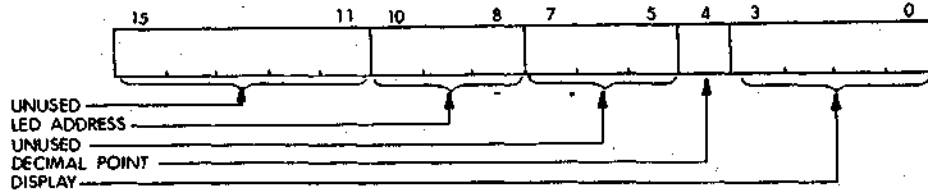
LPSAD-12 BUFFER/LED REGISTER

A/D Buffer (Read only)



LPS11

LED Register—Numeric Display (Write only)



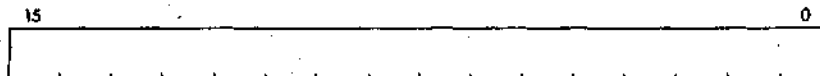
LED Address

Bit 10	Bit 9	Bit 8	Digit
0	0	0	LED 1 (Rightmost)
0	0	1	LED 2
0	1	0	LED 3
0	1	1	LED 4
1	0	0	LED 5
1	0	1	LED 6 (Leftmost)
1	1	0	Unused
1	1	1	Unused

Display

Bit 3	Bit 2	Bit 1	Bit 0	Numeric Value
0	0	0	0	Number 0
0	0	0	1	Number 1
0	0	1	0	Number 2
0	0	1	1	Number 3
0	1	0	0	Number 4
0	1	0	1	Number 5
0	1	1	0	Number 6
0	1	1	1	Number 7
1	0	0	0	Number 8
1	0	0	1	Number 9
1	0	1	0	Test Pattern
1	0	1	1	Blank
1	1	0	0	Blank
1	1	0	1	Minus Sign
1	1	1	0	Blank
1	1	1	1	Blank

LPSKW STATUS REGISTER



LPS11

Bit	Function
15	Schmitt Trigger #1 Flag
14	Schmitt Trigger #1 Interrupt Enable
13	Schmitt Trigger #1 Clock Start Enable
12	Maintenance Schmitt Trigger #1
11	Maintenance Count
10	Maintenance Schmitt Trigger #2
9, 8	Mode
7	Mode Flag
6	Mode Interrupt Enable
5, 4	Unused
3, 2, 1	Rate
0	Clock Enable

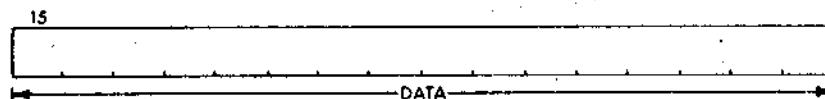
Mode

Bit 9	Bit 8	Function
0	0	Single Interval
0	1	Repeated Interval
1	0	External Interval (Schmitt Trigger #2)
1	1	External Interval from Zero Base

Rate

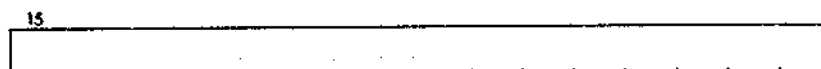
Bit 3	Bit 2	Bit 1	Base Frequency
0	0	0	Stop
0	0	1	1 MHz
0	1	0	100 kHz
0	1	1	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
1	1	0	External (Schmitt Trigger #1)
1	1	1	Line Frequency

LPSKW BUFFER/PRESET REGISTER



No byte operation is permitted. Data will simultaneously be loaded to the clock counter when Bit 0 of the status register is disqualified.

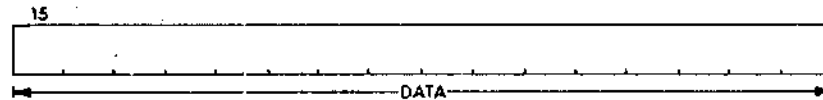
LPSDR STATUS REGISTER



LPS11

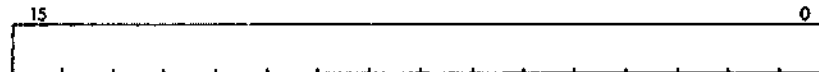
Bit	Function
15	Output Flag
14	Output Interrupt Enable
13	Maintenance Bit 2
12-9	Unused
8	Relay #2
7	Input Flag
6	Input Interrupt Enable
5	Maintenance Bit 1
4-2	Unused
1	Load Input Buffer
0	Relay #1

LPSDR INPUT and OUTPUT REGISTERS



Input — Read only
 Output — Read/Write

LPSVC STATUS REGISTER

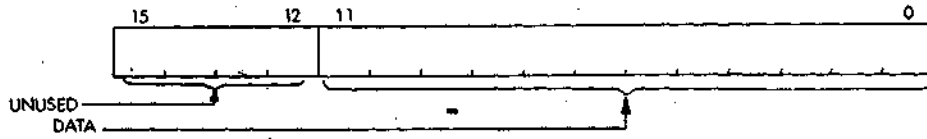


Bit	Function
15-13	Unused
12	Erase (Storage Scope)
11	Write thru (Storage Scope)
10	Store (Storage Scope)
9	Channel (VR14)
8	Unused
7	Ready Flag
6	Interrupt Enable
5	Unused
4	Ext Delay (Special Scopes)
2, 3	Mode
1	Fast Intensify
0	Intensify

Mode

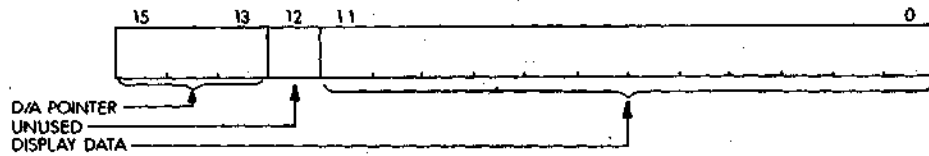
Bit 3	Bit 2	Function
0	0	Intensification with Bit 0 only
0	1	Intensification on Loading X Register
1	0	Intensification on Loading Y Register
1	1	Intensification on X or Y

LPSVC X and Y REGISTERS



Data is in offset binary format.

LPSVC EXT D/A REGISTER



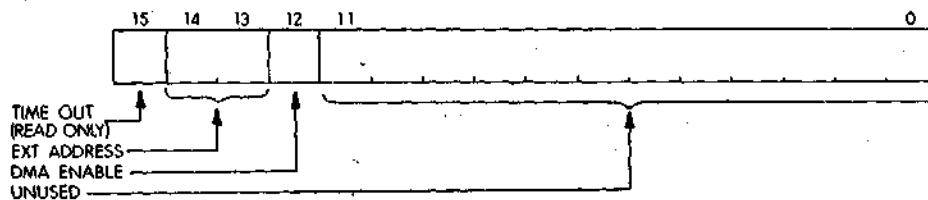
D/A Pointer

Bit 15	Bit 14	Bit 13	Expansion D/A Converter
0	0	0	DAC 0 (LPS DA #1)
0	0	1	DAC 1 (LPS DA #1)
0	1	0	DAC 2 (LPS DA #2)
0	1	1	DAC 3 (LPS DA #2)
1	0	0	DAC 4 (LPS DA #3)
1	0	1	DAC 5 (LPS DA #3)
1	1	0	DAC 6 (LPS DA #4)
1	1	1	DAC 7 (LPS DA #4)

LPSAD-NP DMA REGISTER

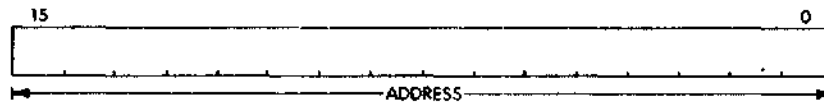
The DMA Register will function as defined by the DMA Pointer in the LPS AD-12 Status Register

DMA Status Register



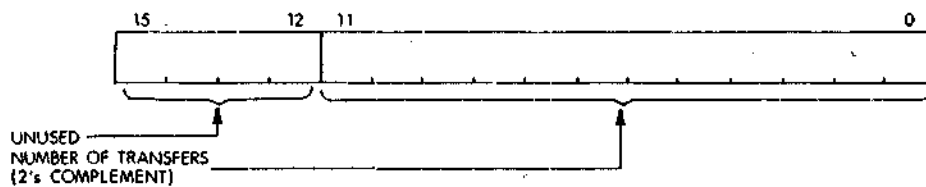
LPS11

DMA Current Address Register



Bit 0 will always be loaded as a zero.

DMA Word Count Register



SPECIFICATIONS FOR LPS11-S

Register Addresses: floating (see Appendix A)

UNIBUS Interface

Interrupt vector address: floating (see Appendix A)

Priority level: BR 4 to 6

Data transfer: NPR (optional)

Bus loading: 1 bus load

Mechanical

Mounting: 1 panel mounted unit

Size: 5 $\frac{1}{4}$ " front panel height
(5 $\frac{1}{4}$ "H x 19"W x 23"D)

Weight: 80 lbs.

Power

Input Current: 3 A at 115 VAC, max.

Heat dissipation: 300 W

Environment

Operating temperature: 5°C to 43°C

Relative humidity: 20% to 80%

Models

LPS11-SA: Lab Peripheral System, rack mount, 115 VAC, 60 Hz

LPS11-SB: " " " " rack mount, 230 VAC, 50 Hz

LPS11

Model	Description	Prerequisite
LPSAD-12:	12-bit ADC, sample & hold, 8 channel multiplexer, and LED (Light Emitting Diodes) 6-digit programmable decimal readout display.	LPS11-S
LPSAD-NP:	Direct memory access (DMA) option for LPSAD-12 ADC.	LPSAD-12
LPSAM:	8 channel expansion multiplexer (if more than 8 channels are implemented).	LPSAD-12
LPSSH:	Second Sample & Hold for a Dual Sample & Hold Configuration.	LPSAM
LPSAG:	Four differential preamplifiers with ± 1 volt input. Maximum of 4 LPSAGs per LPS11-S system.	LPSAD-12
LPSAG-VG:	Four independently selectable multigain differential preamplifiers. Ranges: $\pm 1V$, $\pm 5V$, 0 to + 2V, 0 to + 10V; and all differential inputs.	LPSAD-12
LPSKW:	Programmable real-time clock & two Schmitt triggers.	LPS11-S
LPSVC:	Display control including two 12-bit DACs. This controller is capable of handling a VR14; also, Tektronix's RM503, 602, 604, 611 & 613 scopes.	LPS11-S
LPSDR:	16-bit buffered digital I/O with drive capabilities and two programmable N.O. relays.	LPS11-S
LPS11-E:	Expander box for Laboratory Peripheral System. 5 $\frac{1}{4}$ " high assembly with prewired logic and power, for expansion to an additional 48 channels of A/D and 8 channels of D/A.	LPS11-S
LPSDA:	2 channels of 12-bit D/A output (maximum of 4 LPSDA's per LPS11-E).	LPS11-E and LPSVC
LPSAM-SG:	Programmable gain amplifier for LPS11. Gains of 1, 4, 16, and 64. Includes interconnecting hardware for rear panel access to the LPS11.	LPS11-S LPSAD-12 and BA408
BA408:	Programmable gain amplifier for LPS11. Gains of 1, 4, 16, and 64.	LPS11-S and LPSAD-12

ELECTROSTATIC PRINTER/PLOTTER, LV11**DESCRIPTION**

The LV11 high-speed Electrostatic Printer-Plotter provides quieter and more reliable operation than conventional impact printers and pen plotters, especially under heavy, continuous use. The entire ASCII character set (including upper- and lower-case alphabet) is printed in 132 columns per line at 500 lines per minute. The included control unit allows both printing and plotting, and accommodates most DIGITAL line printer software. In the plotting mode, the LV11 prints 122,880 dots per second (independent of picture complexity) with a resolution of 10 bits (1024 dots per line). The Printer-Plotter uses roll paper for continuous plots and printouts (up to 500 feet), or fanfold paper for easier handling.

The electrostatic printing technique employs a fixed writing head with 1024 addressable writing electrodes. As the paper passes over the writing head, any (or all) of the electrodes may be requested to deposit a charge on the coated paper. The charged paper then passes over a liquid toner containing carbon particles; the particles are attracted to the charged areas on the paper, causing the appearance of black dots.

The only moving parts in the LV11 are the paper-moving motor and a small toner pump—simplicity of design that guarantees long, trouble-free operation that more than offsets the small additional cost of the coated paper.

CONTROLS & INDICATORS

ON/OFF	Applies ac power to the LV11. When power is applied, the switch is illuminated and remains depressed. Depressing the switch a second time removes power from the unit.
PAPER ADVANCE	Depressing this switch causes paper to advance provided no data remains in the data buffer. The switch remains inoperative until the data is printed. Printing may be accomplished under computer control or by depressing the FORM FEED switch located just below the PAPER ADVANCE switch. Paper movement will continue until the switch is released.
FORM FEED	This switch causes the printer to enter a print cycle and print any data remaining in the data buffer. Upon completion of printing of the line, the paper is advanced to the top of the next page when using fanfold paper and the ROLL/FAN FOLD switch is in the FAN FOLD position, or for a distance of 2-1/2 inches when this switch is in the ROLL position.

LV11

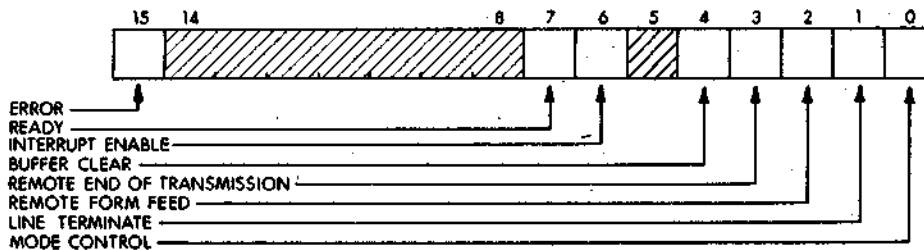
- LOW PAPER** This indicator is red in color and, when illuminated, indicates an out-of-paper condition in the printer. The LV11 will not accept data when this condition exists. An additional supply of paper should be loaded.
- CONTRAST ADJUSTMENT** The contrast adjustment is located inside the front panel and is labeled DARK. Its purpose is to allow the operator to compensate for variations in contrast due to humidity changes in the atmosphere. It should be turned as far clockwise as necessary to permit high contrast writing without excessive background writing.
- ROLL/FAN FOLD** This switch is located on the frame behind the front door. When this switch is in the ROLL position, the top-of-form detection circuit is disabled. The paper is advanced 2½ inches for an FF and 8 inches for an EOT. When in the FAN FOLD position, the printer commands are executed. Should this switch be placed in the FAN FOLD position when using roll paper, the top-of-form circuitry will be disabled following the first FF or EOT command. These commands will then be treated as an LF command when in print mode, or as a Line Terminate in the plot mode.

CAUTION

Should any of the manual controls be depressed while the LV11 is in operation, printing will be interrupted to perform the manual function indicated.

REGISTERS

Control and Status Register (LVCS) 777 514



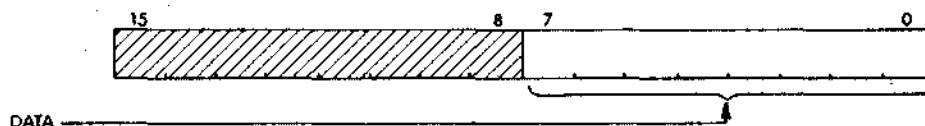
Effect of the Initialize (INIT) signal: clear bits 6 and 0

Read only: bits 15 and 7
Write only: bits 4 through 1

LV11

BIT	NAME	FUNCTION
15	Error	Set when an error condition exists in the printer. Error conditions are: <ol style="list-style-type: none"> 1. No Paper 2. Power off 3. No printer connected to control unit. <p>This bit is reset only by manual correction of the error condition.</p>
7	Ready	Set when the printer is ready to receive the next data transfer. Indicates that the previous function is either complete or has been started and continued to a point where the printer can accept the next data.
6	Interrupt Enable	Set to allow Ready or Error = 1 to cause an interrupt.
4	Buffer Clear	Set to clear the buffer indicated by the Mode Control bit.
3	Remote End of Transmission	Set to perform an EOT when in plot mode.
2	Remote Form Feed	Set to perform an FF when in the plot mode.
1	Line Terminate	Set to print the graphics line prior to receipt of a complete scan line.
0	Mode Control	Selects printer or plotter operation: 0 = printer, 1 = plotter.

Data Buffer Register (LVDB) 777 516



BIT	NAME	FUNCTION
7-0	Data	Eight-bit data buffer. Bits 6 to 0 contain the ASCII characters. Bit 7 is used only in the plot mode.

SPECIFICATIONS**Printing Specifications**

Number of columns: 132
 Number of characters: 96
 Printing speed: 500 line/min
 Type of printing: electrostatic, 7 x 9 dot matrix
 Vertical spacing: 8 lines/inch
 Horizontal spacing: 12.5 char/inch
 Memory: one-line buffer (132 char)

Plotting Specifications

Plotting area: 10.24 sq inches
 Total writing points: 1024
 Vertical spacing: 100 lines/inch
 Horizontal spacing: 100 points/inch
 Input: 8-bit parallel bytes
 Data transfer rate: 500,000 bytes/sec
 Plotting speed: 122,880 dots/second
 Memory: one-line buffer (1024 bits)

Paper

Type: roll, 11" wide x 500 ft long
 fanfold, 11" wide x 1000 sheets
 Slew speed: 1.2 inches/sec

Register Addresses

Control and Status (LVCS) 777 514
 Data Buffer (LVDB) 777 516

UNIBUS Interface

Interrupt vector address: 200
 Priority level: BR4
 Bus loading: 1 bus load

Mechanical

Mounting: 1 free-standing unit + 1 SPC slot
 Size: 38"H x 19"W x 18"D + quad module
 Weight: 160 lbs

Power

Input current: 5 A at 115 VAC
 1.5 A at +5 V (for control)
 Heat dissipation: 600 W

Environment

Operating temperature: 10°C to 40°C
 Relative humidity: 10% to 90%

Models

LV11-BA: Printer and control, 115 VAC, 60 Hz
 LV11-BB: " 230 VAC, 50 Hz

**PC11
PR11**

HIGH SPEED PAPER TAPE READER/PUNCH PC11

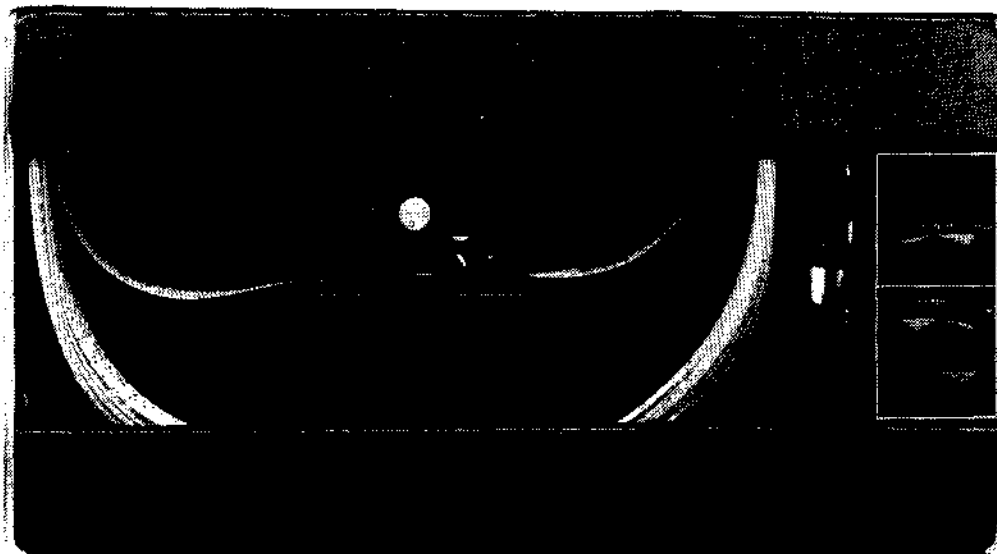
DESCRIPTION

The PC11 High Speed Reader & Punch is capable of reading eight-hole uncoiled perforated paper tape at 300 characters per second, and punching tape at 50 characters per second. The system consists of a Paper Tape Reader/Punch and Control. A unit containing a reader only (PR11) is also available.

Operation

In reading tape, a set of photodiodes translate the presence or absence of holes in the tape to logic levels representing 1's and 0's. In punching tape, a mechanism translates logic levels representing 1's and 0's to the presence or absence of holes in the tape. Any information read or punched is parallel-transferred through the Control. When an address is placed on the UNIBUS, the Control decodes the address and determines if the reader or punch has been selected. If one of the four device register addresses have been selected, the Control determines whether an input or an output operation should be performed. An input operation from the reader is initiated when the processor transmits a command to the Paper Tape Reader Status register. An output operation is initiated when the processor transfers a byte to the Paper Tape Punch Buffer Register.

The Control enables the PDP-11 System to control the reading or punching of paper tape in a flexible manner. The reader can be operated independently of the punch, either device can be under direct program control or can operate without direct supervision through the use of interrupts, to maintain continuous operation.



High-Speed Paper Tape Reader/Punch

PC11

Paper tape is loaded into the reader as explained below.

1. Raise tape retainer cover.
2. Put tape into right-hand bin with channel one of the tape toward the rear of the bin.
3. Place several folds of blank tape through the reader and into the left-hand bin.
4. Place the tape over the reader head with feed holes engaged in the teeth of the sprocket wheel.
5. Close the tape retainer cover.
6. Depress the **READER FEED** button until leader tape is over the reader head.

CAUTION

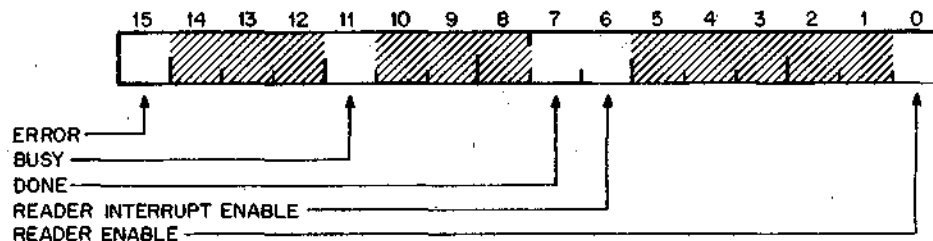
Oiled paper tape should not be used in the high-speed reader or punch. Oil collects dust and dirt which can cause reader or punch errors.

SWITCHES

PUNCH FEED		Punch leader tape.
READER	{ ON LINE	Allow reading of tape.
	{ OFF LINE	Disable reading of tape.
READER FEED		Manual feeding of tape through read station.

REGISTERS

Papertape Reader Status Register (PRS) 777 550



Effect of the Initialize (INIT) signal: clear bits 11, 7, and 6

Read only: bits 15, 11, and 7

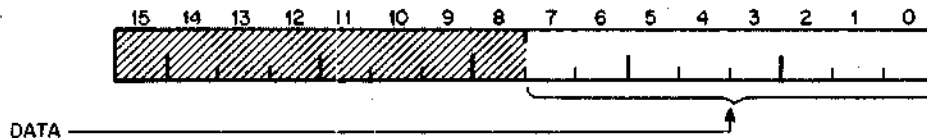
Write only: bit 0

BIT	NAME	FUNCTION
15	Error	Set when an error occurs; no tape in reader, reader is off-line, or reader has no power.

PC11

11	Busy	Set when a character is being read. It is set when Reader Enable is set, and cleared when the present operation is complete (Done is set).
7	Done	Set when a character is available in the Reader Data Buffer. It is cleared by any program reference to the Reader Data Buffer, or by setting Reader Enable.
6	Interrupt Enable	Set to allow Error or Done = 1 to cause an interrupt.
0	Reader Enable	Set to allow the Reader to fetch one character. The setting of this bit clears Done, sets Busy, and clears the Reader Buffer (PRB). Operation of this bit is disabled if Error = 1; attempting to set it when Error = 1 will cause an immediate interrupt if Interrupt Enable = 1.

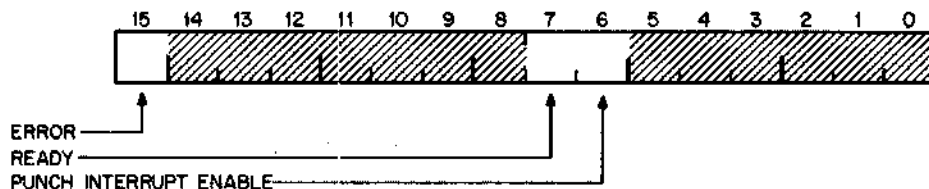
Papertape Reader Buffer (PRB) 777 552



Bits 7 through 0 hold the coded data for the character read. The bits are cleared when Reader Enable, bit 0 of PRS, is set. To the processor, the data is read only.

Any program reference to PRB (777 552 or 777 553) as a word or byte will clear Done, bit 7 of PRS.

Papertape Punch Status (PPS) 777 554



Effect of the Initialize (INIT) signal: clear bit 6, set bit 7

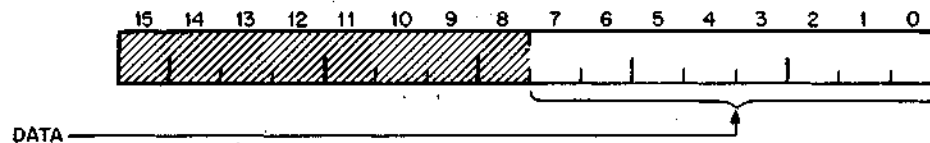
Read only: bits 15 and 7

BIT	NAME	FUNCTION
15	Error	Set when an error occurs; no tape in punch, or punch has no power.

PC11

- | | | |
|---|------------------|---|
| 7 | Ready | Set when ready to punch a character. It is cleared when the Punch Buffer is loaded, and is set when punching is done. |
| 6 | Interrupt Enable | Set to allow Error or Ready = 1 to cause an interrupt. |

Papertape Punch Buffer Register (PPB) 777 556



Bits 7 through 0 hold the coded data for the character to be punched. To the processor, the data is write only.

Any instruction that could modify PPB as a word or byte, clears Ready (bit 7 of PPS) and initiates punching. An immediate interrupt will occur when punching is initiated if Error = 1 and Interrupt Enable = 1.

PROGRAMMING

Program Control of the Reader

The sequence of instructions that follows reads one byte from the paper tape and deposits it in general register 0. If a reader error is sensed, the program branches to an error routine, which may type out a message and then wait for operator intervention.

```
READ: INC     PRS           ;SET RDR ENB
LOOP:  TST     PRS           ;LOOK FOR ERROR
      BMI     ERR           ;BRANCH ON ERROR = 1
      TSTB    PRS           ;LOOK FOR DONE
      BPL     LOOP         ;WAIT IF DONE = 0
      MOV     PRB, R0       ;READ CHARACTER
```

A shorter form of the test loop is possible, as shown below:

```
READ: INC     PRS
LOOP:  BIT     #100200, PRS ;TEST BITS 15 AND 7
      BEQ     LOOP         ;WAIT IF NO BITS SET
      BMI     ERR           ;ERROR IF BIT 15 SET
      MOV     PRB, R0       ;IF BIT THAT IS SET IS NOT BIT 15,
                          ;MUST BE BIT 7
```

Reader Interrupt Service

The PDP-11 System can combine PC11 operations with other processing by using the interrupt mode of device operation. When a device operation has been initiated, the PC11 continues without supervision until the operation is complete (or an error occurs); the remainder of the PDP-11 System is free to perform other operations. When the PC11 Control requires further service, the processor is notified by an interrupt.

PC11

The program that follows can be used to read a block of 128 characters from the paper tape to a buffer.

```
START:  MOV #-200,R0          ;INITIALIZE COUNTER
        MOV #101,PRS         ;SET INTR ENB AND RDR ENB
HANG:   BR HANG              ;HANG UP HERE UNTIL BLOCK IS
                                ;READ
70:     RDRINT               ;VECTOR TO INTERRUPT ROUTINE
72:     200                  ;SETS STATUS TO PRIORITY 4
RDRINT: TST PRS              ;TEST FOR ERROR
        BMI ERR              ;TYPE OUT MESSAGE IF ERROR
        MOVB PRB,BUFEND(R0)  ;FILL BUFFER STARTING AT 'BUF-
                                ;END-200(OCTAL)
        INC R0               ;COUNT ONE BYTE AND MOVE
                                ;POINTER
        BEQ OUT              ;WHEN COUNT IS ZERO, EXIT
                                ;LOOP
        INC PRS              ;ENABLE READER AGAIN
        RTI                  ;RETURN FROM INTERRUPT
OUT:    ADD #4,SP            ;UNSTACK INTERRUPT PC AND PS
        CLR PRS              ;INHIBIT FURTHER INTERRUPTS
        JMP HANG + 2         ;CONTINUE MAIN PROGRAM
```

NOTE

The position of the buffer used by this program is specified by the end of the buffer, not the beginning. The indexed address uses the negative counter values to access bytes at decreasing distances from this base address.

Two operations performed by this program require caution. When a program accesses the same or contiguous locations, the program operating speed increases if the locations are addressed through a register. If this is done either no other use can be made of this register or: a) the interrupt service routine must stack the former contents of the register, b) the counter must be moved from a temporary storage location to the register, c) the register must be used, and d) the storage operations reversed. In this example where the processor does not do any other processing, no conflicts with the use of the register occur.

A second caution refers to the terminating exit from the service routine. When the exit does not occur through an RTI instruction, the main pro-

gram PC (Program Counter) and PS (Processor Status) words that are stacked by the interrupt must be removed from the stack. The ADD instruction at OUT performs the operation. If this operation is not performed, the values stacked by other operations previous to the interrupt are not properly accessible.

Punch Programmed Service

The sequence of instructions that follows transfer one byte from register 0 to the paper tape. When controlling the punch, the READY bit of the PPS register is checked before the transfer; when controlling the reader, the DONE bit of the PRS register is checked after a command.

```
PUNCH: BIT #100200,PPS    ;CHECK PUNCH STATUS
        BEQ PUNCH         ;IF NOT READY OR ERROR, WAIT
        BMI ERROR        ;PROCESS ERROR IF ANY
        MOV R0,PPB       ;OUTPUT CHARACTER
```

Punch Interrupt Service

This interrupt service routine outputs 8-bit codes to the paper tape, unless they are ASCII representations of the formatting characters Line Feed, Rubout, or Form Feed. Line Feeds and Rubouts are ignored (not punched), and the program stops punching when the character read from the buffer is a Form Feed. The Form Feed is not punched. The program transfers the contents of a buffer: a) starting at a preselected address to paper tape, b) stopping automatically when it reads an end-of-buffer character, and c) performing simple character editing.

The interrupt service routine is called into operation when the following sequence of instructions is encountered in the main program:

```
R0 = %0                ;REGISTER ZERO
SP = %6                ;REGISTER SIX
PC = %7                ;REGISTER SEVEN
PS = 77776             ;PROCESSOR STATUS WORD
CLR PUNDON             ;CLEAR SOFTWARE FLAG
MOV #BUFFER,POINTER   ;SET UP BUFFER POINTER
MOV #100,PPS          ;SET PUNCH INTR ENB
```

This instruction sequence sets up the system by initializing the service routine and enabling interrupts from the punch.

If the punch is idle, an interrupt occurs immediately; otherwise, the first interrupt is delayed until the current operation is completed. The software flag is used by the main program to provide a check on the progress of the output. This occurs in the following manner: The main program continues with other processing until the use of the punch is re-

PC11

quired, or further processing is dependent on completion of the output. At this point the sequence of instructions shown below is executed.

```
LOOP:  TST PUNDON      ;CHECK SOFTWARE FLAG
        BPL LOOP
```

If the interrupt service routine has not set the flag, the processor stays in this wait loop, allowing interrupts for further output operations, until the routine signals that it is finished.

In this example, the interrupt routine to service the punch requires the following sequence of instructions:

```
74:      PCHINT          ;VECTOR TO ROUTINE
76:      200             ;NEW STATUS WORD
PCHINT:  MOV R0,-(SP)     ;SAVE REGISTER ZERO
          MOV POINTER,R0 ;SETUP REGISTER
          TST PPS        ;CHECK NO ERRORS
          BMI ERROR      ;IF ERROR, EXIT WITH LAST BUFFER
                          ;POSITION IN R0
RETEST:  CMPB (R0),#212  ;LINE FEED?
          BNE TEST2      ;NO, CONTINUE
          INC R0          ;YES, IGNORE CHARACTER
          BR RETEST      ;AND TEST NEXT CHARACTER
TEST2:   CMPB (R0),#377  ;RUBOUT?
          BNE TEST3      ;NO, CONTINUE
          INC R0          ;YES, IGNORE
          BR RETEST
TEST3:   CMPB (R0),#214  ;FORM FEED?
          BEQ OUT        ;YES, EXIT
          MOVB (R0) + ,PPB ;NO, OUTPUT CHARACTER
          MOV R0,POINTER ;SAVE REGISTER
          MOV (SP) + ,R0  ;UNSTACK PREVIOUS CONTENTS
          RTI            ;NORMAL RETURN
OUT:     MOV (SP) + ,R0  ;RESTORE TO PREVIOUS STATUS
          COM PUNDON     ;SET SOFTWARE FLAG
          CLR PPS        ;CLEAR INT ENB
          RTI
```

PC11

POINTER: 0

PUNDON: 0

SPECIFICATIONS

Main Specifications

Storage medium:	8-hole paper tape, uncoiled
Reader speed:	300 char/sec
Punch speed:	50 char/sec
Paper type:	fanfold
Data format:	8-bit characters

Register Addresses

Reader Status (PRS)	777 550
Reader Buffer (PRB)	777 552
Punch Status (PPS)	777 554
Punch Buffer (PPB)	777 556

UNIBUS Interface

Interrupt vector address:	70 (for reader) 74 (for punch)
Priority level:	BR4 (reader has precedence over punch)
Bus loading:	1 bus load

Mechanical

Mounting:	1 panel mounted unit + 1 SPC slot
Size:	10 $\frac{1}{2}$ " front panel height + quad module
Weight:	50 lbs

Power

Input current:	3 A at 115 VAC 1.5 A at +5 V
Heat dissipation:	350 W

Environment

Operating temperature:	10°C to 40°C
Relative humidity:	10% to 90%

Models

PC11:	Reader/punch and control, 115 VAC, 60 Hz
PC11-A:	" " " " , 230 VAC, 50 Hz
PR11:	Reader and control
H722:	Transformer (required for 230 VAC, 50 Hz operation of PC11-A or PR11)

DISK PACK, RJP04

FEATURES

- 44-million-word formatted capacity
- Expandable to more than 350 million words (8 disk drives)
- Dual Access Option
- Fast seek time, 28 milliseconds average
- Error detection and correction
- 2.5-microsecond-per-word transfer rate
- Overlapped positioning with multiple drives
- Programmable remote Standby (pack unload)
- First-in/first-out 66-word data buffer
- On-line pack formatting
- Parity checking on all data and control transfers between controller and disk drive

DESCRIPTION

The RJP04 is a mass storage system offering low cost per bit and high performance. Included are one disk drive and a buffered controller, expandable to 8 disk pack drives in a PDP-11 system. Each disk pack has a capacity of 44 million 16-bit words, or more than 350 million words total of on-line storage. The removable disk pack offers the flexibility of unlimited off-line storage capacity.

On multi-drive systems, positioning operations can be overlapped for efficiency. While one drive is reading or writing, one or more drives can be positioning to a new cylinder for the next transfer. All data transfers use the Non-Processor Request (NPR) facility of the UNIBUS for direct access to memory.

The RJP04 operates at a transfer rate of 403,000 words per second (2.5 microseconds per word). Data transfers can be made in block sizes of from 1 to 65,536 words. The system utilizes a first-in/first-out, 66-word data buffer to facilitate smooth UNIBUS data flow.

Parity checking is performed on both data and control information transfers for increased reliability. The controller also detects and flags memory parity errors. The disk system interrupts the processor on completion of a command and on error conditions. Extensive error indicators exist for easy on-line diagnosis. Numerous status indicators give complete program control.

The controller for the RJP04 requires two system unit mounting spaces in any PDP-11/35, -11/40, or -11/45 CPU or in an H960-D or -E expansion box.

The RP04 drive is a high-performance device, with a single head per surface. It enables the data processing system to store or retrieve information at any location on a rotating RP04-P (3336 type) disk pack.

RJP04 RP04

Average access time is 36 milliseconds, which includes the time for head positioning and rotational latency.

The disk drive is designed to provide a high level of data reliability. A phase-lock-loop clock system and modified frequency modulation (MFM) recording offer a reliable reading and recording technique. Error detection and correction hardware within each disk drive provides adequate information for correcting any error burst up to 11 consecutive bits within the data field. Correction of data-field errors under software control is achieved without a re-reading of data from the disk.

Program controlled head offset positioning corrects for slight mechanical misalignment between the RP04 read/write heads and the disk pack by moving the positioner about the track centerline in incremental steps. A powerful feature that facilitates recovery of data previously recorded on another disk whose read/write heads may have been slightly misaligned. Provides for data recovery and enhances data reliability.

To further increase data reliability, the disk drive has a hardware write-check capability for data verification. Hardware verification of sector, track, and cylinder on read and write operations increases data integrity. Built-in registers allow for disk path checkout for ease of maintenance.

DIAGNOSTIC SOFTWARE SUPPORT

Included with the RJP04 disk system are the following extensive diagnostic software capabilities which allow the user to:

Test all controller and disk-drive control electronics independent of drive mechanism and analog circuitry.

Perform read/write and mechanical tests utilizing the actual disk surfaces.

Pre-format disk packs and flag bad sectors.

Check and verify access times, sector addressing, data storage, and retrieval.

Stress and check read/write and servo systems.

Perform a test which exercises an RJP04 system having multiple disk drives in a rigorous and highly interactive random manner.

Construct and use RJP04 unit test programs (simple device troubleshooting loops) without having detailed knowledge of the processor.

Check and verify disk-drive head alignment accuracy.

Check and verify the Dual Access Option arbitration electronics.

PROGRAMMABLE FEATURES

The RJP04 has additional program-controlled hardware features which may be used to enhance computer systems.

- **Hardware-generated rotational position sensing (RPS).** Available for optimizing scheduling programs.
- **Implied Seek.** The read command causes automatic seek when not on the cylinder, for ease of programming.
- **Midtransfer seek.** Issues an automatic seek to the next cylinder, following the operation of the last track and sector of the current cylinder, to enhance spiral read/write operation.
- **Header-Compare Inhibit.** Data can be read with or without header information.
- **Error-Correction Inhibit.** Disables the error-correction process to allow for throughput flexibility.

DUAL ACCESS OPTION

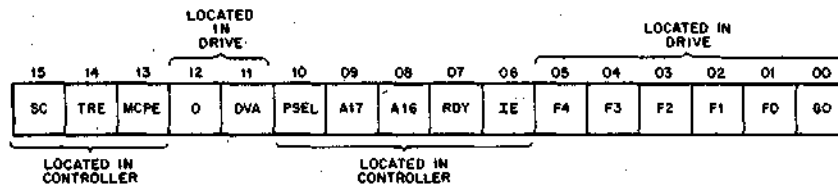
A Dual Access Option allows up to 8 disks to be shared by two different control units. The two control units may be connected to the same or two different processors. Each drive contains arbitration logic that resolves simultaneous requests from its two controllers. A disk drive may be dynamically assigned by program control to Controller A, Controller B, or a Neutral state. An operator-available switch on each disk drive permits manual override of its assignment to a controller.

With this option, the user can realize:

- Shared data bases with two computer systems.
- High computational power with two processors attached to a single data base.
- Remote access to a data base through a front-end processor without interfering with system integrity.
- Multi-path access to a disk for redundancy (fail-safe).
- High throughput for transaction-oriented systems.

The Dual Access Option greatly extends the capability and flexibility of multi-processor computer configurations.

CONTROL AND STATUS 1 (RPCS1) REGISTER (776700)



BIT NAME	FUNCTION
15 SC (Special Condition) Read only	Set by TRE or ATTN or I/O bus Control Parity Error. Cleared by Unibus A INIT, Controller Clear, or by removing the ATTN condition.
14 TRE (Transfer Error) Read/write	Set by DLT, WCE, UPE, NED, NEM, PGE, MXF, MDPE, or a drive error during a data transfer. Cleared by Unibus A INIT, Controller Clear, Error Clear, or by loading a data transfer command with GO set.
13 MCPE (Mass I/O Control Bus Parity Error) Read only	Set by parity error on control bus while reading a remote register (located in the drive). Cleared by Unibus A INIT, Controller Clear, Error Clear, or by loading a data transfer command with the GO set. Parity errors which occur on the I/O control bus while writing a drive register are detected by the drive and cause the PAR error (RPER1 register, bit 03) to set.
12 Not used	Always read as a 0.
11 DVA (Drive Available) Read only	Set when device is not busy on other port. Reset by device from other port when device is busy on that port. This bit is used in dual controller configurations.
10 PSEL (Port Select) Read/write	When PSEL = 1, data transfer is via Unibus B; when PSEL = 0, data transfer is via Unibus A. Cleared by Unibus A INIT, Controller Clear, or by writing a 0 in this bit position.
9 A17	Upper extension bits of the BA register. Cleared by Unibus A INIT, Controller Clear, or by writing 0s in these bit positions.
8 A16 (Unibus Address Extension Bits) Read/write	
7 RDY (Ready) Read only	RDY normally = 1. During data transfers, RDY = 0 When a data transfer command code (51 _h - 77 _h) is written into RPCS1, RDY is reset. At the termination of the data transfer, RDY is set.

BIT NAME

6 IE
(Interrupt Enable)
Read/write

IE is a control bit which can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by Unibus A INIT, Controller Clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.

5 F4-F0
— and GO bit
0 Read/write

F4-F0 and the GO bit (F0) are function (command) code control bits.

F4	F3	F2	F1	F0	
0	0	0	0	0	No Operation
0	0	0	0	1	Unload (Standby)
0	0	0	1	1	Recalibrate
0	0	1	0	0	Drive Clear
0	0	1	0	1	Release (Dual Port Operation)
0	1	1	0	0	Search Command
1	0	1	0	0	Write Check Data
1	0	1	0	1	Write Check Header and Data
1	1	0	0	1	Write Data
1	1	0	0	1	Write Header and Data
1	1	1	0	0	Read Data
1	1	1	0	1	Read Header and Data
0	0	0	1	0	Seek Command
0	0	1	1	0	Offset Command
0	0	1	1	1	Return To Centerline
0	1	0	0	1	Pack Acknowledge
0	1	0	0	0	Read-in-Preset
1	1	0	1	0	} Illegal Functions
1	1	1	1	0	
1	1	1	1	1	

The GO bit (RPCS1, bit 0) must be set to cause the controller or drive to respond to a command. The GO bit is reset by the drive after command execution. The function code bits are stored in the selected drive.

Cleared by Unibus A INIT or Controller Clear (will abort command execution in all drives).

WORD COUNT (RPWC) REGISTER (776702)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC 00

BIT	NAME	FUNCTION
WC	(15:00) (Word Count) Read/write	Set by the program to specify the number of words to be transferred (2's complement form). This register is cleared only by writing 0s into it. Incremented for each data transfer.

UNIBUS ADDRESS (RPBA) REGISTER (776704)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	0

BIT	NAME	FUNCTION
01-15	BA(01:15) (Unibus Address) Read/write	Loaded by the program to specify the starting memory address of a transfer. Cleared by Unibus A INIT or by Controller Clear. The BA register is incremented by 2 after each transfer of a word to or from memory.

DESIRED SECTOR/TRACK ADDRESS (RPDA) REGISTER (776706)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	TA5	TA4	TA3	TA2	TA1	0	0	0	SA5	SA4	SA3	SA2	SA1

BIT	NAME	FUNCTION
12-08	TA(05:00) (Track Address) Read/write	Set by the program to specify the track on which a transfer is to start. Cleared by Unibus A INIT, Controller Clear, or by performing a Drive Clear function. Incremented by the drive when sector 21 (16-bit format) or sector 19 (18-bit format) is reached.
05-00	SA(05:00) (Sector Address) (Read/write)	Set by the program to specify the sector on which a transfer is to start. Cleared by Unibus A INIT, Controller Clear, or by performing a Drive Clear function. Incremented by the drive after each sector has been transferred.

CONTROL AND STATUS 2 (RPCS2) REGISTER (776710)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

BIT	NAME	FUNCTION
15	DLT (Data Late) Read only	<p>Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Also set when the controller is performing a data transfer operation over the second Unibus (PSEL = 1) and a Unibus B INIT is received on that port. Cleared by Unibus A INIT, Controller Clear, 1 Error Clear, or loading a data transfer command with GO set.</p> <p>DLT causes TRE. A DLT error indicates a severely overloaded bus. Can also be set by the program reading or writing the RPDB register.</p>
14	WCE (Write Check Error) Read only	<p>Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.</p> <p>WCE causes TRE. If a mismatch is detected during a Write-Check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RPBA (and extension) is the address of the word following the one which did not match (if BAI is not set). The mismatched data word from the disk is displayed in the data buffer (RPDB).</p>
13	PE (Parity Error) Read/write	<p>Set if the parity lines indicate a parity error while the controller is performing a Write or Write-Check command. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.</p> <p>PE causes TRE. When the Unibus is selected to do 18-bit data transfers, the PE error is disabled. When a parity error occurs, the RPBA register contains the ad-</p>

RJPC4

BIT	NAME	FUNCTION
		dress +2 of the memory word with the parity error (if BAI is not set). This bit may be set by program control for diagnostic purposes.
12	NED (Nonexistent Drive) Read only	Set when the program reads or writes a drive register in a drive [selected by U(02:00)] which does not exist or is powered down. (The drive fails to assert TRA within 1.5 μ s after assertion of DEM.) Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. NED causes TRE.
11	NEM (Nonexistent Memory) Read only	Set when the controller is performing a DMA transfer and the memory address specified in RPBA is nonexistent (does not respond to MSYN within 10 μ s. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. NEM causes TRE. The RPBA contains the address +2 of the memory location causing the error.
10	PGE (Program Error) Read only	Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. PGE causes TRE. The data transfer command code is inhibited from being written.
09	MXF (Missed Transfer) Read/write	Set if the drive does not respond to a data transfer command within 250 ms. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. MXF causes TRE. This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive which has ERR set, or if the drive fails to initiate the command for any reason (such as a parity error).
08	MDPE (Mass Data Bus Parity Error) Read only	Set when a parity error occurs on the I/O bus data while doing a read or write-check operation. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.

RJP04

BIT	NAME	FUNCTION
		MDPE causes TRE. Parity errors on the data bus during write operations are detected by the drive and cause the PAR error (RPER1 register, bit 03).
07	OR (Output Ready) Read only	<p>Set when a word is present in RPDB and can be read by the program. Cleared by Unibus A INIT, Controller Clear, or by reading DB.</p> <p>Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to read the DB register before OR is asserted will cause a DLT error.</p>
06	IR (Input Ready) Read only	<p>Set when a word may be written in the DB register by the program. Cleared by reading the DB.</p> <p>Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to write the DB register before IR is asserted will cause a DLT error.</p>
05	CLR (Controller Clear) Write only	When a 1 is written into this bit, the controller and all drives are initialized. Unibus A INIT also causes Controller Clear to occur.
04	PAT (Parity Test) Read/write	While PAT is set, the controller generates even parity on both the control bus and data bus of the I/O bus. When clear, odd parity is generated. Cleared by Unibus A INIT or Controller Clear. While PAT is set, the controller checks for even parity received on the data bus but not on the control bus.
03	BAI (Unibus Address Increment Inhibit) Read/write	When BAI is set, the controller will not increment the BA register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by Unibus A INIT or Controller Clear. When set during a data transfer, all data words are read from or written into the same memory location.
02-00	U(2:0) (Unit Select) Read/write	<p>These bits are written by the program to select a drive. Cleared by Unibus A INIT or Controller Clear.</p> <p>The unit select bits can be changed by the program during data transfer operations</p>

RJP04

BIT NAME

FUNCTION

without interfering with the transfer. The RP04 registers contain bits which come from the selected drive.

DRIVE STATUS (RPDS) REGISTER (776712)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	DE1	DL64	GRV	DI68	DF28	DF5

BIT NAME

FUNCTION

15 ATA
(Attention
Active)
Read only

An Attention condition in a drive will set the ATA bit and the ATA summary line. It is cleared by Unibus A INIT, Controller Clear, loading a command with the GO bit set, or loading a 1 in the RPAS register corresponding to the drive's unit number. The last two methods of clearing the ATA bit will not clear the error indicators in the drive.

An Attention condition is caused by: any error in the error registers (except during data transfers); the completion operation; the completion of a start up cycle (with the MOL bit set); dual controller operation with drive presently available (drive was requested before but was not available); correct sector identification (Search command only).

NOTE

The ATA bit will not set if the drive was switched from a neutral position. The ATA bit may be reset by writing a 1 into the Attention Summary register. Writing a 0 into the register has no effect.

14 ERR
(Error)
Read only

Set when one or more of the errors in the Error registers (RPER1, RPER2, or RPER3) in a selected drive is set. Cleared by Unibus A INIT, Controller Clear, or Drive Clear.

A composite error bit which is the logical OR of all the error conditions in the RPER1, RPER2, or RPER3 registers. This ERR bit is not cleared by loading a command other than Drive Clear. While ERR is asserted, commands other than Drive Clear are not accepted by the drive.

RJP04

BIT NAME	FUNCTION
13 PIP (Positioning In Progress) Read only	Set by the drive when a positioning command is accepted. These commands are Seek, Offset, Return to Centerline, Recalibrate, Unload, and Search. The PIP bit will not be set during implied seeks or mid-transfer seeks. Cleared when the moving function is completed. The DRY and ATA bits are also set at this time (normal termination).
12 MOL (Medium On-Line) Read only	Set by the drive upon the successful completion of the startup cycle. Cleared when the spindle is powered down or the device is switched off-line (with the spindle still up to speed) for diagnostic purposes.
11 WRL (Write Lock) Read only	Set when the RP04 will not accept Write commands.
10 LST (Last Sector Transferred) Read only	Set by the drive on rising edge of EBL pulse when last addressable sector on the disk pack has been read or written. Cleared when a new function command is received.
09 PGM (Programmable) Read only	Set when the CONTROLLER SELECT switch is in the A/B position, indicating that the device is accessible from either Port A or Port B. Cleared when the CONTROLLER SELECT switch is in PORT A or PORT B position.
08 DPR (Drive Present) Read only	Always set for single controller operation. In dual controller operation, this bit is set for the controller which has seized the RP04 and is reset for the other controller. When the RP04 switches from one controller to a second controller and the ATA line (bit 15) is high, DPR is set. This indicates that the RP04 is connected to the asynchronous control bus of this controller. If the RP04 is in the programmable state (PGM bit = 1) when requested, DPR will be set and the drive will switch immediately, regardless of the ATA bit.
07 DRY (Drive Ready) Read only	Set at the completion of every command, data handling or mechanical motion. Cleared at the initiation of a command. If this bit is reset, the controller cannot issue another command. When set, this bit indicates the readiness of the RP04 device to accept a new command.

RJP04

BIT	NAME	FUNCTION
06	VV (Volume Valid) Read only	Set by the Pack Acknowledge or Read-In Preset command from either port. Cleared by the drive whenever it cycles up from the off state. When reset, this bit indicates when the drive has been put off-line and on-line and a disk pack may have been changed.
05	DE1 (Difference Equals 1) Read only	Set when the device has detected a value equal to 1 in the difference counter during a head load sequence. Cleared by a File Ready at the completion of a head load sequence.
04	DL64 (Difference Less Than 64) Read only	Set when the device has detected a value less than 64 in the difference counter during the reverse seek of the head load sequence. Cleared by a File Ready at the completion of a head load sequence.
03	GRV (Go Reverse) Read only	Set when the device has detected the GO Reverse signal during a head load sequence. Cleared by File Ready at the completion of a head load sequence.
02	DIGB (Drive to Inner Guard Band) Read only	Set when the drive has detected the drive to inner guard band signal during a head load sequence. Cleared by File Ready at the completion of a head load sequence.
01	DF20 (Drive Forward 20 in./sec) Read only	Set by the drive when it has detected the DF20 signal during a head load sequence. Cleared by File Ready at the completion of a head load sequence.
00	DF5 (Drive Forward 5 in./sec) Read only	Set when the drive has detected a DF5 signal while in the head load mode after a sequence start pulse was recognized. Cleared by File Ready at the completion of a head load sequence.

ERROR (RPER1) REGISTER 01 (776714)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	TAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

BIT	NAME	FUNCTION
15	DCK (Data Check) Read/write	Set during a read operation when the ECC hardware has detected an ECC error after the ECC bytes have been looked at. Cleared by a Drive Clear command,

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BIT NAME	FUNCTION
	Unibus A INIT, Controller Clear, or by writing 0s into the register. If Error Correction Code/Inhibit (ECI) bit is off, the RPO4 will go into the error correction process. DCK will remain set. If ECI bit is on, the error correction process is inhibited even though an ECC error was detected at the end of a data transmission.
14 UNS (Unsafe) Read/write	Set when the drive detects a condition which prevents it from operating. Cleared by a Drive Clear or by writing 0s into the register. If this does not cause the UNS condition to disappear, the RPO4 must be powered down and cycled up to ensure clearing of all the errors including the UNS bit. This bit is a composite error bit of the unsafe error conditions in the RPER2 and RPER3 registers.
13 OPI (Operation Incomplete) Read/write	Set when a Read or Write command involving header search has not begun transmitting data (sync clocks) within three index pulses. OPI will also set during a search operation where a sector count match is not made after a maximum of three index pulses have been encountered. Cleared by a Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.
12 DTE (Drive Timing Error) Read/write	Set when a failure has occurred in the clocking or timing circuits of the drive. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.
11 WLE (Write Lock Error) Read/write	Set when the operating system attempts to issue a write command on a write-locked device (device in WRITE PROTECT mode). A manual (WRITE PROTECT) switch can place the device in WRITE PROTECT mode during normal operations. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.
10 IAE (Invalid Address Error) Read/write	Set when the address in the Desired Cylinder register (RPDC) and the Desired Sector/Track Address register (RPDA) is invalid and a seek or search operation is initiated. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.
09 AOE (Address Overflow Error) Read/write	Set when the Desired Cylinder register (RPDC) overflows during a read or write. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register. Setting of this bit indicates that the Desired Cylinder Address register has exceeded cylinder address 410.

BIT	NAME	FUNCTION
08	HCRC (Header CRC Error) Read/write	Set by a CRC error in the header. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.
07	HCE (Header Compare Error) Read/write	If the sector counter is equal to the desired sector field, the header associated with that sector is compared with the desired header words. If the header matches the desired cylinder and desired sector/track address, the header field is the required one. If the header does not match the desired cylinder and sector/track address, the HCE bit is set. If the sector address and sector count match but a CRC error is detected following the header compare, the HCE bit is reset and the HCRC bit is set. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.
06	ECH (ECC Hard Error) Read/write	Set when the conclusion of the error correction procedure indicates that the error was a noncorrectable ECC error. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.
05	WCF (Write Clock Fail) Read/write	Set during a write operation when the Write Clock signals are not received by the drive. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register. Upon recognizing a WCF condition, the drive will abort the command.
04	FER (Format Error) Read/write	Set where the prerecorded (pack formatting) flag bit on the header is not equal to the corresponding flag bit in the Offset register (bit location 12, RPOF). Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.
03	PAR (Parity Error) Read/write	Set when a parity error is detected during data transmission over the asynchronous control bus (odd parity) or over the synchronous data bus. Cleared by a Drive Clear command, an Initialize pulse, or by writing 0s into the register.
02	RMR (Register Modification Refused) Read/write	Set when a write is attempted into any register (except RPAS) during an operation. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.
01	ILR (Illegal Register) Read/write	Set when the device control logic decodes a non-existent register address from the register select lines (RS00-RS04). Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.

BIT NAME	FUNCTION
	Attempting to write into a read-only register will not cause the ILR to set. The bits received will be ignored and no other error will be flagged.
00 ILF (Illegal Function) Read/write	Set when the function code in the Control register does not correspond to an implemented command on this drive. Cleared by Unibus A INIT, Drive Clear, Controller Clear, or by writing 0s into the register.

ATTENTION SUMMARY (RPAS) REGISTER (776716)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 07	ATA 06	ATA 05	ATA 04	ATA 03	ATA 02	ATA 01	ATA 00

BIT NAME	FUNCTION
07:00 ATA(07:00) (Attention Active) Read/write	<p>Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by Unibus A INIT or Controller Clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect.</p> <p>Each drive's ATA bit is displayed individually in bit 15 of RPDS. Each drive responds in the bit position which corresponds to its unit number; e.g., drive 02 responds in bit position 02.</p>

LOOK-AHEAD (RPLA) REGISTER (776720)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
∅	∅	∅	∅	∅	SC4	SC3	SC2	SC1	SC∅	EXT1	EXT∅	∅	∅	∅	∅

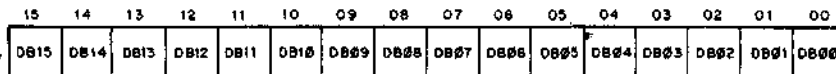
BIT NAME	FUNCTION
10-6 SC(4:0) (Sector Count) Read only	<p>This five-bit register addresses the required sector on the data track through an exclusive-OR network with the RPDA register. The sector count is continually being incremented on the rising edge of each sector pulse and reflects the exact location of the data track in relation to the head. Each time the rising edge of the index pulse is encountered, the sector count field resets to zero. The maximum sector count is 21 for the 16-bit word format and 19 for the 18-bit data word format. If a sector</p>

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BIT NAME	FUNCTION
5-4 EXT (1:0) (Encoded Extension Field)	<p>count malfunction occurs during an operation, the RJP04 will set the Operation Incomplete (OPI) error bit, after three index pulses, without a sector count/desired sector field match. A malfunctioning sector count field is a catastrophic error since the required sector cannot be recovered. The RJP04 looks at every header on the data track. In the event of an error condition, no error is reported until after the sector counter matches the sector field, which is an indication that the desired sector has been found.</p> <p>These two bits are used to specify the approximate location of the heads within a sector.</p>

EXT 1	EXT 0	Head Location
0	0	< 20% (in first 20% of sector)
0	1	20 to 40%
1	0	40 to 80%
1	1	> 80% (in last 20% of sector)

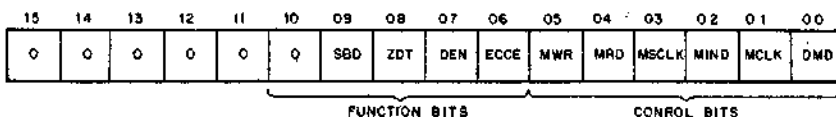
DATA BUFFER (RPDB) REGISTER (776722)



BIT	NAME	FUNCTION
15-00	DB(15:00) (Data Buffer Read/write)	When read, the contents of OBUF (internal register) are delivered. Upon completion of the read, the next sequential word in the Silo will be clocked into OBUF. When written, data is loaded into IBUF (internal register) and allowed to sequence into the Silo if space is available. Used by the program for diagnostic purposes.

MAINTENANCE (RPMR) REGISTER (776724)

The Maintenance register simulates various signals from the disk for diagnostic testing.



DRIVE TYPE (RPDT) REGISTER (776726)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NBA	TAP	MOH	0	DRQ	0	0	DT08	DT07	DT06	DT05	DT04	DT03	DT02	DT01	DT00

BIT	NAME	FUNCTION
15-14		Always 0.
13	MOH (Moving Head) Read only	Always 1.
11	DRQ (Drive Request Required) Read only	DRQ = 1 Dual controller option available DRQ = 0 Dual controller option not available
8-0	DT(08:00) (Drive Type Number) Read only	The device type number for the RP04 is 20 ₈ - 27 ₈ .

SERIAL NUMBER (RPSN) REGISTER (776730)

The purpose of this register is to distinguish a drive from similar drives attached to the same controller. The serial number provides a means of distinguishing between different RP04s with identical characteristics and which are connected to the same controller.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SN	SN	SN	SN	SN	SN	SN	SN	SN	SN	SN	SN	SN	SN	SN	SN
38	34	32	31	28	24	22	21	18	14	12	11	08	04	02	01

HIGH ORDER (FOURTH) DECADE
THIRD DECADE
SECOND LOWEST DECADE
LOW ORDER DECADE

OFFSET (RPOF) REGISTER (776732)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SCG	0	0	FMT	ECJ	HCI	0	0	OFS	OFS	OFS	OFS	OFS	OFS	OFS	OFS
			22					07	06	05	04	03	02	01	00

BIT	NAME	FUNCTION
15	SCG (Sign Change) Read/write	Used when a DDU and alignment (CE) pack are available to verify head alignment. Beginning from a known offset position and issuing continuous Offset commands toward the actual track centerline, the bit is guaranteed to

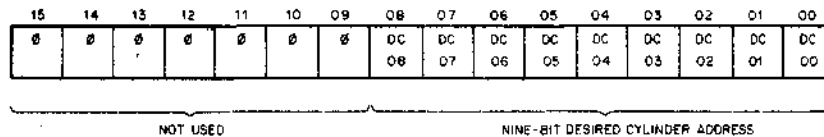
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BIT	NAME	FUNCTION
		change states when the head R/W gap is actually over the true track centerline.
12	FMT 22 (Format Bit) Read/write	<p>Set to a 1 when 16-bit/word format is used (16 bits/word \times 256 words/sector). Set to a 0 when 18-bit/word format is used (18 bits/word \times 256 words/sector). Cleared by Read-In Preset command.</p> <p>This bit will be written in the cylinder address sector recorded on the data pack. Normally, this bit will be written during the format operation (write header and data). Upon reading a header from the pack, the recorded bit will be compared with bit 12 of the Offset register. If the bits do not compare, the Format Error (FER) bit will be set.</p>
11	ECl (Error Correction Code Inhibit) Read/write	<p>Set when the software desires to inhibit error correction. If ECl is set, error correction code is disallowed; if ECl is reset, the error correction process is allowed. Cleared by Read-In Preset command.</p> <p>If a data error is detected at the end of the data transmission in the read mode with the ECl bit reset, the RPO4 device will immediately go into the ECC correction process. Prior to beginning the correction routine, the device will also set the Data Check (DCK) error bit, which will remain set until a Drive Clear command or an INIT pulse is received.</p>
10	HCl (Header Compare Inhibit) Read/write	<p>Set when the software desires to inhibit header compare. Cleared by Read-In Preset command. When the RPO4 sees this bit asserted, it will ignore the header compare logic and CRC check. With HCl set, the device logic depends only on the sector count field/desired address field comparison for sector identification. If the sector count field is out of sequence, the wrong sector may be affected.</p>
7-0	OFS(7:0) (Offset Information) Read/write	<p>Set under software control. Cleared by Read-In Preset command or at the completion of the offset operation.</p>

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Position	Code Word OF0-OF7					Value/Direction (microinches)
	OF7	OF6	OF5	OF4	OF3-OF0	
1st offset	0	0	0	1	0	+400
2nd offset	1	0	0	1	0	-400
3rd offset	0	0	1	0	0	+800
4th offset	1	0	1	0	0	-800
5th offset	0	0	1	1	0	+1200
6th offset	1	0	1	1	0	-1200
Return to Track Centerline						

DESIRED CYLINDER (RPDC) REGISTER (776734)



This register is a read/write register and contains the address of the cylinder to which the positioner is to move. The desired cylinder address is loaded in the Desired Cylinder Address register via the interface.

The device logic will immediately compare the contents of the Desired Cylinder Address register with the Current Cylinder Address register through the subtract logic.

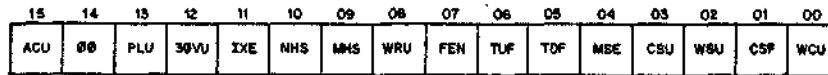
The Current Cylinder Address register reflects, at all times, the address of the cylinder which the positioner presently is addressing. The results of the subtraction between the two registers will specify the magnitude and direction of seek.

After the Desired Cylinder Address register has been loaded, a function code (Read, Write, or Seek command) specified, and the GO bit set in the Control register, the following events will take place:

1. If the subtract logic output equals 0, the *desired* cylinder address equals the *current* cylinder address and the positioner will not move.
2. If the subtract logic output is not equal to 0, the RPO4 device will initiate a seek whose *direction* and *magnitude* are specified by the output of the subtract logic. Consequently, when the GO bit sets with a Read, Write, Search, or Seek command in the Control register, the contents of the Desired Cylinder Address register are presumed valid.

Prior to informing the controller that the seek was completed, the RPO4 Drive will internally transfer, in parallel, the contents of the Desired Cylinder Address register into the Current Cylinder Address register, so that the Current Cylinder Address register reflects the actual cylinder the positioner is addressing.

ERROR (RPER2) REGISTER 2 (776740)

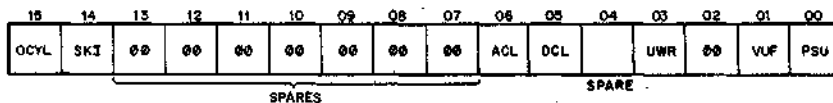


BIT	NAME	FUNCTION
15	ACU (AC Unsafe) Read/write	When set, this bit indicates that the RP04 has detected an interruption of ac power for the dc power supply. Cleared by a Drive Clear command or an INIT pulse.
14	Not used	
13	PLU (PLO Unsafe) Read/write	Set when the RP04 has detected a loss of synchronization of the read/write phase-locked oscillator (PLO). Cleared by a Drive Clear or an INIT pulse.
12	30 VU (30 Volts Unsafe) Read/write	Set when the drive has detected a loss of unregulated 30-volt dc power. Cleared by a Drive Clear or an INIT pulse.
11	IXE (Index Error) Read/write	Set when the RP04 detects a missing index pulse or an invalid index pulse. Cleared by the next valid pulse.
10	NHS (No Head Selection) Read/write	Set when the RP04 detects the absence of head selection when a Read or Write command is present. Cleared by a Drive Clear or an INIT pulse.
9	MHS (Multiple Head Select) Read/write	Set when the RP04 has detected the concurrent selection of more than one head. Cleared by a Drive Clear or an INIT pulse.
8	WRU (Write Ready Unsafe) Read/write	Set when the RP04 detects the presence of a Write command when the heads are not on the cylinder. Cleared by a Drive Clear or an INIT pulse.
7	FEN (Failsafe Enabled) Read/write	Set when the RP04 detects an open circuit breaker in the 48-volt power driver supply. Upon detecting this error bit, the only way to reset it is to physically reset the circuit breaker and initiate a new start sequence.
6	TUF (Transitions Unsafe)	Set when the RP04 detects the absence of write transitions during a write operation. Cleared by a Drive Clear or an INIT pulse.

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BIT	NAME	FUNCTION
5	TDF (Transitions Detector Failure) Read/write	Set when the RP04 detects write transitions without the presence of a Write command. Cleared by a Drive Clear or an INIT pulse.
4	MSE (Motor Sequence Error) Read/write	Set if any of the following unsafe conditions are detected. SSR (Solid State Relay) failure Power Sequence Failure Brush in Pack error. Cleared by initiating a new start sequence successfully.
3	CSU (Current Switch Unsafe) Read/write	Set when the RP04 detects an incorrect write current level during a write operation. Cleared by a Drive Clear or an INIT pulse.
2	WSU (Write Select Unsafe) Read/write	Set when the RP04 detects that both even-side and odd-side heads are simultaneously enabled for writing. Cleared by a Drive Clear or an INIT pulse.
1	CSF (Current Sink Failure) Read/write	Set when the RP04 detects the current sink non-operative without the presence of a Write command. Cleared by a Drive Clear or an INIT pulse.
0	WCU (Write Current Unsafe) Read/write	Set when the RP04 detects the presence of write current without the presence of a Write command.

ERROR (RPER3) REGISTER 03 (776742)



BIT	NAME	FUNCTION
15	OCYL (Off Cylinder) Read/write	Set when an invalid off cylinder condition is detected resulting in a Seek Incomplete. Cleared by a Drive Clear or an INIT pulse. An off cylinder error will also cause an automatic recalibrate operation to occur.

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BIT	NAME	FUNCTION
14	SKI (Seek Incomplete Read/write)	<p>Set when a seek operation fails to complete within 85 ms from a seek initiation.</p> <p>Due to a positioner malfunction it is possible for the seek not to complete. The RPO4 will assume a positioner hardware problem and will:</p> <ul style="list-style-type: none">Set the SKI bitSet the ATA bitReset the PIP bitSet the RDY bit. <p>This indicates to the software that the seek operation did not complete and the exact positioner location is unknown.</p> <p>A SKI condition will cause the RPO4 to determine that the drive is unsafe to operate and will cause the UNS (RPER1, bit 14) bit to set. The software can diagnose the trouble by monitoring the Error register.</p>
6	DCL (DC Low) Read/write	<p>Set when the RPO4 detects a loss of regulated 5 Vdc power, which powers the interface electronics. Cleared by a Drive Clear or an INIT pulse. The detection of the DCL error condition will cause an automatic head retraction.</p>
5	ACL (AC Low) Read/write	<p>Set when the RPO4 detects an interruption of primary ac power for the dc power supply which powers the interface electronics. Cleared by a Drive Clear or an INIT pulse. The detection of the ACL error condition will cause an automatic head retraction.</p>
3	UWR (Any Unsafe Except Read/Write) Read/write	<p>Set if any of the following unsafe conditions are detected (indicates a head retract has occurred):</p> <ul style="list-style-type: none">Pack Speed Unsafe30 Volt UnsafeVelocity UnsafeServo UnsafeAC UnsafeDC unsafe <p>Cleared by a DC Clear or an INIT pulse.</p>
1	VUF (Velocity Unsafe) Read/write	<p>Set when the RPO4 detects an excessive positioner velocity. Cleared by a DC Clear or an INIT pulse.</p>

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BIT NAME	FUNCTION
0 PSU Pack Speed Unsafe) Read/write	Set when the RP04 detects the pack speed to be below approximately 80% of normal while the heads are positioned within the pack area. Cleared by a Drive Clear or an INIT pulse.

ECC POSITION (RPEC1) REGISTER (776744)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	00	00	BLC 4096	BLC 2048	BLC 1024	BLC 512	BLC 256	BLC 128	BLC 64	BLC 32	BLC 16	BLC 08	BLC 04	BLC 02	BLC 01

The RP04 has an ECC (error correction code) capability which will generate, detect, and correct an error by reconstructing a portion of the data. Within the specified code word length, which is fixed, the burst ECC code will correct an error which must fall within the specified length of the burst. The actual location of the burst within the code word (data field of a sector) is irrelevant.

Any errors outside the specified burst length will be detected but not corrected. The ECC hardware, in this case, will yield an ECC uncorrectable error. The RP04 logic contains the hardware to find the burst within which the read error is included and determine the exact location of the burst within the data field.

The ECC Pattern register contains the actual error burst and the ECC Position register contains the address for determining the actual location of the error burst within the data field.

NOTE

The actual correction of the data field is done by the software with the help of the ECC Position and ECC Pattern registers.

The ECC Position register contains the exact location of the error burst within the data field following the completion of the error correction procedure.

Upon completion of the ECC process, the device will load this register with the necessary information. The EXC line is raised upon initiation of the error correction procedure and the ATA bit is set at the trailing edge of EBL and EXC.

ECC PATTERN (RPEC2) REGISTER (776746)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
00	00	00	00	BIT 11	BIT 10	BIT 09	BIT 08	BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00

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This register is used in conjunction with the ECC Position register and contains the actual error burst available at the completion of the ECC internal to the RP04 device logic error correction process.

The software will use the contents of the ECC Position register to find the actual location of the error burst in the data field. Then the error burst itself will determine the bits in error within the 11-bit field.

REGISTER SUMMARY

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	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RPCS1 (776700)	SC	TRE	MCPE	∅	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F∅	GO
RPWC (776702)	WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 9	WC 8	WC 7	WC 6	WC 5	WC 4	WC 3	WC 2	WC 1	WC ∅
RPBA (776704)	BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 9	BA 8	BA 7	BA 6	BA 5	BA 4	BA 3	BA 2	BA 1	BA ∅
RPDA (776706)	∅	∅	∅	TA 16	TA 8	TA 4	TA 2	TA 1	∅	∅	∅	SA 16	SA 8	SA 4	SA 2	SA 1
RPCS2 (776710)	DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U∅
RPDS (776712)	ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	DE1	DL64	GRV	DIGB	DF20	DF5
RPER1 (776714)	DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

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RPAS (776716)	∅	∅	∅	∅	∅	∅	∅	∅	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA ∅
RPLA (776720)	∅	∅	∅	∅	∅	SC 4	SC 3	SC 2	SC 1	SC ∅	EXT 1	EXT ∅	∅	∅	∅	∅
RPOB (776722)	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB ∅
RPMR (776724)	∅	∅	∅	∅	∅	∅	SBD	ZDI	DEN	ECCE	MWR	MRD	MSCLK	MIND	MCLK	DMD
RPDT (776726)	NBA	TAP	MOH	∅	DRQ	∅	∅	DT 8	DT 7	DT 6	DT 5	DT 4	DT 3	DT 2	DT 1	DT ∅
RPSN (776730)	SN 38	SN 34	SN 32	SN 31	SN 28	SN 24	SN 22	SN 21	SN 18	SN 14	SN 12	SN 11	SN 8	SN 4	SN 2	SN 1
RPOF (776732)	SGCH	∅	∅	FMT 22	ECCI	HCI	∅	∅	OFS 7	OFS 6	OFS 5	OFS 4	OFS 3	OFS 2	OFS 1	OFS ∅
RPDC (776734)	∅	∅	∅	∅	∅	∅	∅	DC 256	DC 128	DC 64	DC 32	DC 16	DC 8	DC 4	DC 2	DC 1

RJP04 RP04

RJP04 SPECIFICATIONS

Main Specifications

Storage medium:	Disk pack (3336 type)
Capacity/pack:	43,980,288 words
Data transfer speed:	2.5 μ sec/word
Time for $\frac{1}{2}$ revolution:	8.3 msec
Disk rotation speed:	3600 RPM
Drives/control, maximum:	8

Track Positioning Time

One cylinder seek:	7 msec
Average seek:	28 msec
Maximum seek (typ):	50 msec

Data Organization

Surfaces/pack:	19
Tracks/surface:	411
Sectors/track:	22
Words/sector:	256
Bits/words:	16
Recording method:	Modified frequency modulation (MFM)
Recording density:	4040 bits/inch, max.
Access with single R/W:	1 to 65,536 words

UNIBUS Interface

Interrupt vector address:	254
Priority level:	BR5
Data transfer:	NPR
Bus loading:	1 bus load, each controller port

Mechanical

Mounting:	Disk 1 free-standing unit	Control Unit 2 systems units (mounts in a CPU or expander box)
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Size: 40"H x 31"W or 32"D

Weight: 600 lbs

Cables:

Control-to-drive	25 ft standard, 40 ft optional
Drive-to-drive	2 ft standard, 10 ft optional
All cables, total	60 ft max.

Power			
Frequency:	60 Hz \pm 1%	50 Hz \pm 1%	50 Hz \pm 1%
Phasing:	3 phase delta	3 phase WYE	3 phase delta
Voltage:	208/230 \pm 10%	380/400/415 \pm 10%	220/230/240 \pm 10%
Starting Current: (10 seconds max)	30A/phase	16A/phase	26A/phase
Running Current:	6A/phase @ 208 VAC	3.1A/phase @ 400 VAC	5.2A/phase @ 240 VAC
Current for control:	16A at +5V 0.6A at -15V		
Heat Dissipation:	2100 watts (7000 Btu/hr)		
Environmental			
Operating temperature:	15°C to 32°C		
Relative humidity:	20% to 80%, maximum wet bulb 25°C and minimum dew point 2°C		
Models			
Disk drive	60 Hz RP04-AA	50 Hz RP04-AB	
Dual-access disk drive	RP04-BA	RP04-BB	
RP04-A & controller	RJP04-AA	RJP04-AB	
RP04-B & 2 controllers	RJP04-BA	RJP04-BB	
Spare data pack		RP04-P	
10 ft cable		BC06S-10	
40 ft cable		BC06S-40	

**RJS04
RJS03
RS04
RS03**

FIXED-HEAD DISK, RJS04 & RJS03

FEATURES

- Fast access—8.5 milliseconds average (10.2 milliseconds at 50 Hz).
- High-speed transfer rate—4 microseconds per word maximum (4.8 microseconds per word at 50 Hz).
- Dual port control with programmable data port.
- 256K (RJS03) or 512K (RJS04) words of storage per disk, expandable to over four million words.
- Real-time look-ahead on multidrive systems with interrupts on sector-compare for up to eight drives at the same time.
- Overlapped data transfer and look-ahead operations.
- High data reliability.

The RJS03 and RJS04 fixed-head disk systems have been designed specifically for applications requiring fast, reliable, on-line storage. With an average access time of 8.5 milliseconds and a transfer rate of 4 microseconds per word, the RJS03 and RJS04 increase throughout substantially for timesharing applications which involve significant amounts of program swapping. Phase lock loop reading techniques and CRC error detection make these disk systems ideal for real-time data acquisition and control systems requiring a high level of reliability.

DESCRIPTION

The RJS03 includes a controller and a rack-mounted RS03 fixed-head disk drive with a storage capacity of 256K 16-bit words. The RJS04 includes a controller and an RS04 fixed-head disk drive with a storage capacity of 512K 16-bit words. The RJS03 and RJS04 are expandable by adding either RS03 and RS04 drives, up to a total of eight drives per controller. A single controller may have a mix of RS03 and RS04 drives. For instance, a requirement for 768K words of fixed-head disk storage can be met with a combination of an RJS03 and RS04 or an RJS04 and an RS03. Two drives may be mounted in a single cabinet.

The controller for the RJS03 and RJS04 requires two system unit mounting spaces in any PDP-11/35, 11/40, or 11/45 CPU or in an H960-D or -E expansion box.

To minimize start-up current on multiple-drive systems, drives are automatically started in sequence when power is turned on.

The controller for both the RJS03 and RJS04 includes a large (66-word) data buffer. This data buffer maximizes configuration flexibility on large PDP-11 systems where several high-speed DMA devices are not uncommon.

OPERATION

Data is stored in blocks of 64 words for the RS03 and in blocks of 128

**RJS04
RJS03
RS04
RS03**

words for the RS04. The RS03 uses one read/write head at a time; the RS04 uses two heads in parallel. There are 64 heads for the RS03 and 128 heads for the RS04. The higher-capacity RS04 records information on both surfaces of the disk, whereas the RS03 uses only one surface. The number of sectors, 64, is the same, but the RS04 achieves double capacity by recording odd-numbered bits on one surface and even-numbered bits on the other surface.

Fast track-switching time permits "spiral" read/write from one track to the adjacent track in a single transfer operation. When the last sector on a track has been transferred, the disk automatically advances to the next track without any delay in the transfer rate. Up to 64K words can be transferred in a single operation.

The RJS03 and RJS04 also feature real-time look-ahead. This feature permits the program to monitor the current angular position of the disk and thereby minimize access time in a multidrive system when multiple requests are pending. Through the use of interrupts when comparing sectors, program time can be kept to a minimum. Except for the drive currently engaged in a data transfer, all drives can perform searches simultaneously.

Each disk drive has a set of six Write-Lock switches and a Write-Lockout Enable/Disable switch. The settings of the six Write-Lock switches correspond to the number of a track. When the Write-Lock Enable/Disable switch is enabled, all tracks numbered, inclusively, from 0 to the track number selected by the six Write-Lock switches are write-protected.

Each controller has two UNIBUS ports. The first port can be used for both control and data; the second port is used for data only. Data transmission can be switched from one port to the other under program control.

RELIABILITY

The RJS03 and RJS04 offer a high level of data reliability. They have been designed to provide a recoverable error rate of less than 1 in 10^{11} bits read, and a nonrecoverable error rate of less than 1 in 10^{12} bits transferred.

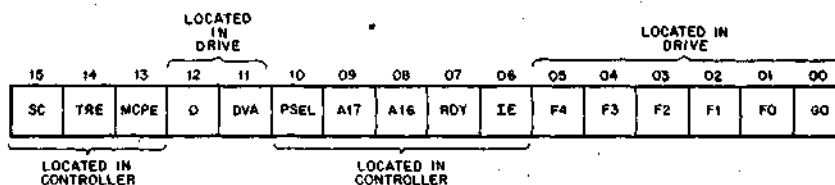
The use of a 16-bit Cyclic Redundancy Check (CRC) character per data block reduces the probability of undetected error to a negligible value. To ensure maximum reliability in the transmission of information between disk drive and control, a differential bus is used with parity generated and checked at the drive and at the control for both control and data transfers.

A phase lock loop clock system and MFM recording offer the latest in reliable reading and recording techniques. In addition, a write-check capability is used to verify data written on any disk without modifying

either the disk or the memory data, and without the overhead of a programmed comparison between the original data in memory and the data written on the disk.

For maximum disk life and minimum downtime, a prefilter and a high-efficiency air filter are used to keep the disk enclosure at a positive pressure. This air system maintains a clean room environment for the disk and heads.

CONTROL AND STATUS 1 (RSCS1) REGISTER (772040)



BIT NAME	FUNCTION
15 SC Special Condition Read only	Set by TRE or ATTN or I/O bus Control Parity Error. Cleared by Unibus A INIT, Controller Clear, or by removing the ATTN condition.
14 TRE Transfer Error Read/Write	Set by DLT or WCE or UPE or NED or NEM or PGE or MXF or MDPE or a drive error during a data transfer. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.
13 MCPE Mass I/O bus Control Bus Parity Error Read only	Set by parity error on control bus while reading a remote register (located in the drive). Cleared by Unibus A INIT, Controller Clear, or Error Clear or loading a data transfer command with the GO set. Parity errors which occur on the I/O control bus while writing a drive register are detected by the drive and cause the PAR error (RSER register, bit 03) to set.
12 Not used	Always read as a 0.
11 DVA Drive Available Read only	Always a 1 in the RS04/RS03 when read from an existing drive.

BIT NAME	FUNCTION
10 PSEL Port SElect Read/write	When PSEL = 1, data transfer is via Unibus B; when PSEL = 0, data transfer is via Unibus A. Cleared by Unibus A INIT, Controller Clear, or by writing a 0 in this bit position.
9 A17 8 A16 Unibus Address Extension Bits Read/Write	Upper extension bits of the BA register. Cleared by Unibus A INIT, Controller Clear, or by writing 0s in these bit positions.
7 RDY ReaDY Read/Only	RDY normally = 1. During data transfers, RDY = 0. When a data transfer command code (51 ₈ - 77 ₈) is written into RSCS1, RDY is reset. At the termination of the data transfer, RDY is set.
6 IE Interrupt Enable Read/write	IE is a control bit which can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by Unibus A INIT, Controller Clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.
5-0 F4-F0 and GO bit Read/write	F4-F0 are function (command) code control bits which determine the action to be performed.

F4	F3	F2	F1	F0	Function
0	0	0	0	0	No operation
0	0	1	0	0	Drive Clear
0	1	1	0	0	Search
1	0	1	0	0	Write Check
1	1	0	0	0	Write
1	1	1	0	0	Read

The GO bit (RSCS1, bit 0) must be set to cause the controller or drive to respond to a command. The GO bit is reset by the drive after command execution.

The function code bits are stored in the selected drive.

Cleared by Unibus A INIT or Controller Clear (will abort command execution in all drives).

WORD COUNT (RSWC) REGISTER (772042)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC 00

BIT	NAME	FUNCTION
WC (15:00)	Word Count Read/write	Set by the program to specify the number of words to be transferred (2's complement form). This register is cleared only by writing 0s into it. Incremented for each data transfer.

UNIBUS ADDRESS (RSBA) REGISTER (772044)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	0

BIT	NAME	FUNCTION
01-15	BA(01:15) Unibus Address Read/write	Loaded by the program to specify the starting memory address of a transfer. Cleared by Unibus A INIT or by Controller Clear. The BA register is incremented by 2 after each transfer of a word to or from memory.

DESIRED ADDRESS (RSDA) REGISTER (772046)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SP 03	SP 02	SP 01	SP 00	TA 05	TA 04	TA 03	TA 02	TA 01	TA 00	SA 05	SA 04	SA 03	SA 02	SA 01	SA 00

BIT	NAME	FUNCTION
15-12	SP(03:00) SPare Read/write	If set when an operation is begun by setting the GO bit, an IAE error (RSER bit 10) will be posted. Cleared by Unibus A INIT, Controller Clear, or by performing a Drive Clear function. Spare bits for future expansion. The bits are incremented by a carry from the track address.
11-06	TA Track Addr (05:00) Read/write	Set by the program to specify the track on which a transfer is to start. Cleared by Unibus A INIT, Controller Clear, or by performing a Drive Clear function. Incremented by the drive when a carry out of SA (05) occurs.
05-00	SA Sector Addr (05:00) Read/write	Set by the program to specify the sector on which a transfer is to start. Cleared by Unibus A INIT, Controller Clear, or performing a Drive Clear function. Incremented by the drive after each sector has been transferred.

CONTROL AND STATUS 2 (RSCS2) REGISTER (772050)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	UD

BIT	NAME	FUNCTION
15	DLT Data LaTe Read only	Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Also set when the controller is performing a data transfer operation over the second Unibus (PSEL = 1) and a Unibus B INIT is received on that port. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. DLT causes TRE. A DLT error indicates a severely overloaded bus. Can also be set by the program reading or writing the RSDB register.
14	WCE Write Check Error Read only	Set when the controller is performing a write-check operation and a word on the disk does not match the corresponding word in memory. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. WCE causes TRE. If a mismatch is detected during a Write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in RSBA [and extension is the address of the word following the one which did not match (if BAI is not set)]. The mismatched data word from the disk is displayed in the data buffer (RSDB).
13	PE Parity Error Read/write	Set if the parity lines indicate a parity error while the controller is performing a Write or Write-check command. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. PE causes TRE. When the Unibus is selected to do 18-bit data transfers, the PE error is disabled. When a parity error occurs, the RSBA register contains the address +2 of the memory word with the

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BIT	NAME	FUNCTION
		parity error (if BAI is not set). This bit may be set by program control for diagnostic purposes.
12	NED Non-Existent Drive Read only	Set when the program reads or writes a drive register (CS1, DA, DS, ER, LA, MR, or DT) in a drive [selected by U(02:00)] which does not exist or is powered down. (The drives fails to assert TRA within 1.5 μ s after assertion of DEM.) Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. NED causes TRE.
11	NEM Non-Existent Memory Read only	Set when the controller is performing a DMA transfer and the memory address specified in RSBA is nonexistent (does not respond to MSYN within 10 μ s. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. NEM causes TRE. The RSBA contains the address +2 of the memory location causing the error.
10	PGE ProGram Error Read only	Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. PGE causes TRE. The data transfer command code is inhibited from being written.
09	MXF Miss Transfer Read/write	Set if the drive does not respond to a data transfer command with 250 ms. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set. MXF causes TRE. This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive which has ERR set, or if the drive fails to initiate the command for any reason (such as a parity error).
08	MDPE Mass I/O bus Data Bus Parity Error Read only	Set when a parity error occurs on the Massbus data while doing a read or write-check operation. Cleared by Unibus A INIT, Controller Clear, Error Clear, or loading a data transfer command with GO set.

RJS04

BIT	NAME	FUNCTION
		MDPE causes TRE. Parity errors on the I/O bus data bus during write operations are detected by the drive and cause the PAR error.
07	OR Output Ready Read only	<p>Set when a word is present in RSDB and can be read by the program. Cleared by Unibus A INIT, Controller Clear, or by reading DB.</p> <p>Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to read the DB register before OR is asserted will cause a DLT error.</p>
06	IR Input Ready Read only	<p>Set when a word may be written in the DB register by the program. Cleared by reading the DB.</p> <p>Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to write the DB register before IR is asserted will cause a DLT error.</p>
05	CLR Controller CLear Write only	When a 1 is written into this bit, the controller and all drives are initialized. Unibus A INIT also causes Controller Clear to occur.
04	PAT PARity Test Read/write	While PAT is set, the controller generates even parity on both the control bus and data bus of the I/O bus. When clear, odd parity is generated. Cleared by Unibus A INIT or Controller Clear. While PAT is set, the controller checks for even parity received on the data bus but not on the control bus.
03	BAI UniBus Address Increment Inhibit Read/write	When BAI is set, the controller will not increment the BA register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by Unibus A INIT or Controller Clear. When set during a data transfer, all data words are read from or written into the same memory location.
02-00	U(2:0) Unit Select (2:0) Read/write	<p>These bits are written by the program to select a drive. Cleared by Unibus A INIT or Controller Clear.</p> <p>The unit select bits can be changed by the program during data transfer operations</p>

BIT NAME FUNCTION

without interfering with the transfer. The CS1, DA, DS, ER, LA, MR, and DT registers contain bits which come from the selected drive.

DRIVE STATUS (RSDS) REGISTER (772052)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LBT	0	OPR	DRY	0	0	0	0	0	0	0

BIT NAME FUNCTION

- 15 ATA
Attention Active
Read only

Set by the drive when there is an Attention condition in that drive. Cleared by Unibus A INIT, Controller Clear, loading a command with the GO bit set, or loading a 1 in the RSAS register in the bit position corresponding to the drive's unit number. (The last two methods of clearing the ATA bit will not clear the error indicators in the drive.)

An Attention condition occurs 1) at the completion of a Search command, 2) at the completion of a data transfer in which the drive detected an error, 3) if an error condition occurs while the drive is not performing a command, and 4) if there is any change in status of MOL. When the ATA bit of any drive is set, the ATTN line is asserted.
- 14 ERR
(ERROR Summary)
Read only

Set when one or more of the error bits is set in the RSER register of the selected drive. Cleared by Unibus A INIT Controller Clear, or by Drive Clear.

This bit is the logical OR of all the bits in the RSER register. This bit is not cleared by loading a command other than Drive Clear. While ERR is asserted, commands other than Drive Clear are not accepted by the drive.
- 13 PIP
Positioning In Progress
Read only

Set by the drive while a Search command is underway. Cleared at the completion of the search operation.
- 12 MOL
Medium On Line
Read only

Set by the drive when the drive up to speed and power is within limits. Cleared when the drive is powered down, and during power-up sequencing.

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BIT	NAME	FUNCTION
11	WRL Write Locked Read only	Set by the drive when the address in the RSDA register is among those which are write protected (and the write lock switch is in the enable position). Cleared by loading RSDA with an address which is not write protected.
10	LBT Last Block Transferred Read only	Set by the drive at the end of the data transfer to the highest address sector. Cleared by Unibus A INIT, Controller Clear, loading a new address in the RSDA register, or performing a Drive Clear function.
09	Not Used	Always read as a 0.
08	DPR Drive PResent Read only	Always read as a 1. This bit is for use in dual-controller configurations.
07	DRY Drive Ready Read only	Set whenever the drive is on-line and prepared to accept a command. Cleared whenever a valid command (with GO set) is loaded into RSCS1.
06-00	Always read as 0. Not Used.	

ERROR (RSER) REGISTER (772054)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AO	0	0	0	0	0	PAR	RMR	ILR	ILF

BIT	NAME	FUNCTION
15	DCK Data Check Read/write	Set by the drive when an error in the cyclic redundance check is detected during a read or write-check operation. Cleared by Unibus A INIT, Controller Clear, or Drive Clear.
14	UNS UNSafe Read/write	Set by the drive upon detection of low power. Cleared upon restoration of power. If a transfer is in progress when ac power loss occurs in the drive, the transfer is aborted. ATTN is asserted by this drive for as long as dc power lasts, whether or not a transfer was in progress.
13	OPI Operation Incomplete Read/write	Set when the drive fails to complete an operation within the expected time. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. A data transfer operation is considered incom-

BIT NAME	FUNCTION
12 DTE Drive Timing Error Read/write	plete if the RUN line is not asserted within two disk revolutions after a data transfer command was loaded. This would indicate a failure. A Search command is considered incomplete if not terminated within two disk revolutions. This would indicate a drive failure. Set by the drive when it detects a timing fault (loss of clock or index pulse, dropping or picking up clock pulses). Cleared by Unibus A INIT, Controller Clear, or Drive Clear.
11 WLE Write Lock Error Read/write	Set by the drive when a write function is attempted at an address which is write protected. Cleared by Unibus A INIT, Controller Clear, or Drive Clear.
10 IAE Invalid Address Error Read/write	Set by the drive when a data transfer or Search command is loaded while an invalid address is in the RSDA (desired address) register. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. In the RS04/RS03, an invalid address is one which is larger than the maximum address.
09 AO Address Overflow Read/write	Set by the drive when the controller attempts to continue to transfer data after the last sector on the last track has been written or read. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. When this error occurs, no further data transfer occurs. The RSDA register contains an invalid address.
03 PAR Bus PARity Error Read/write	Set when incorrect parity is detected by the drive during a register write operation or on a data transfer during a write operation. Cleared by Unibus A INIT, Controller Clear, or Drive Clear. If a control bus parity error is detected when writing into any drive register, that register will not be modified.
02 RMR Register Modify Refused Read/write	Set by the drive when an attempt is made by the program to write into the RSDA, RSER, or RSCS1 registers, while the drive is busy (DRY bit is negated). Cleared by Unibus A INIT, Controller Clear, or Drive Clear. Drive operation can be aborted by program control only by performing Controller Clear or Reset. These must be used with caution due to their effects on other devices.
01 ILR ILlegal Register Read/write	Set by the drive when the program attempts to read or write a drive register whose address is not recognized by the drive. Cleared by

RJS04

BIT NAME	FUNCTION
00 ILF ILlegal Function Read/write	Unibus A INIT, Controller Clear, or Drive Clear. Indicates a hardware failure in the controller or drives address logic. Set by the drive when the GO bit is set and the core in the Function register (RSCS1, bits 05-01) is not an implemented code. Cleared by Unibus A INIT, Controller Clear, or Drive Clear.

ATTENTION SUMMARY (RSAS) REGISTER (772056)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 07	ATA 06	ATA 05	ATA 04	ATA 03	ATA 02	ATA 01	ATA 00

BIT	NAME	FUNCTION
07:00	ATA 07-00 ATtention Active (07:00) Read/write	Each bit sets when the corresponding drive asserts its ATA bit. All bits are cleared by Unibus A INIT or Controller Clear. Individual bits are cleared by loading a function code with the GO bit in the corresponding drive or by writing a 1 in the ATA bit positions of this register. Writing a 0 has no effect. Each drive's ATA bit is displayed individually in bit 15 of RSDS. Each drive responds in the bit position which corresponds to its unit number; e.g., drive 02 responds in bit position 02.

LOOK-AHEAD (RSLA) REGISTER (772060)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	CS 05	CS 04	CS 03	CS 02	CS 01	CS 00	SF 05	SF 04	SF 03	SF 02	SF 01	SF 00

BIT	NAME	FUNCTION
11-06	CS(05:00) Current Sector Addr Read only	Indicates the sector address currently under the read/write heads of the drive whose unit number appears in RSCS2(2:0).
05-00	SF(05:00) Sector Fract Read only	Indicates the fraction of the current sector which has passed the read/write heads in 64ths of a sector.

DATA BUFFER (RSDB) REGISTER (772062)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 09	DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00

BIT	NAME	FUNCTION
15-00	DB(15:00) Data Buffer (15:00) Read/write	When read, the contents of OBUF (internal register) are delivered. Upon completion of the read, the next sequential word in the Silo will be clocked into OBUF. When written, data is loaded into IBUF (internal register) and allowed to sequence into the Silo if space is available. Used by the program for diagnostic purposes.

MAINTENANCE (RSMR) REGISTER (772064)

The Maintenance register is a 16-bit register which simulates various signals from the disk to allow diagnostic testing of the drive logic circuits.

*15	*14	13	*12	11	10	09	*08	07	06	05	04	03	02	01	00
SDCLK	MWDT	CRCW	MWDB	SB	LSR	AC	SP	WRT	RD	MRDT	MIND	MCLK	MRDS	O	DMD
READ ONLY										READ/WRITE					

* Located in the encode/decode logic.

DRIVE TYPE (RSDT) REGISTER (772066)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NSA	TAP	MCH	TCH	DRQ	SPR	O	DT 08	DT 07	DT 06	DT 05	DT 04	DT 03	DT 02	DT 01	DT 00

BIT	NAME	FUNCTION
15-9		Always 0 in RS04/RS03.
08-00	DT(08:00) Drive Type Read only	These bits contain a unique number for each drive type. The following drive type numbers are assigned to RS04/RS03. 000 ₈ RS03 001 ₈ RS03 with sector interleave 002 ₈ RS04 003 ₈ RS04 with sector interleave

REGISTER SUMMARY

RSCS1-772040

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	TRE	MCPE	O	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	FO	GO

RSWC-772042

WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC 00
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RSBA-772044

BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	0
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RSDA-772046

SP 03	SP 02	SP 01	SP 00	TA 05	TA 04	TA 03	TA 02	TA 01	TA 00	SA 05	SA 04	SA 03	SA 02	SA 01	SA 00
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RSCS2-772050

DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0
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RSDS-772052

ATA	ERR	PIP	MOL	WRL	LBT	0	DPR	DRY	0	0	0	0	0	0	0
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RSER-772054

DCK	UNS	OPI	DTE	WLE	IAE	AO	0	0	0	0	0	PAR	RMR	ILR	ILF
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RSAS-772056

0	0	0	0	0	0	0	0	ATA 07	ATA 06	ATA 05	ATA 04	ATA 03	ATA 02	ATA 01	ATA 00
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RSLA-772060

0	0	0	0	CS 05	CS 04	CS 03	CS 02	CS 01	CS 00	SF 05	SF 04	SF 03	SF 02	SF 01	SF 00
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RSDB-772062

DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 09	DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00
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RSMR-772064

RWCLK	MWDT	CRCW	MWDB	SB	LSR	AC	SP	WRT	RD	MRDT	MIND	MCLK	MRDB	0	DMD
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RSDT-772066

NSA	TAP	MOH	7CH	DRQ	SPR	0	DT 08	DT 07	DT 06	DT 05	DT 04	DT 03	DT 02	DT 01	DT 00
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RJS04
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RS03

SPECIFICATIONS

Main Specifications	RJS03	RJS04 (when different)
Storage medium:	Fixed-head disk	
Capacity/disk:	262,144 words (256K)	512K words
Data transfer speed:	4 or 8 μ sec/word (4.8 or 9.6 μ sec/ word at 50 Hz)	4 μ sec/word (4.8 μ sec/word at 50 Hz)
Average access time (1/2 rev):	8.5 msec (10.2 msec at 50 Hz)	
Minimum access time:	6.4 μ sec (7.7 μ sec at 50 Hz)	
Disk rotation speed:	3530 RPM (2940 RPM at 50 Hz)	
Controller data buffer size:	66 words	
Disks/control, maximum:	8	
 Data Organization		
Tracks:	64	
Sectors/track:	64	
Words/sector:	64	128
Bits/word:	16	
Recording method:	MFM (modified frequency modulation)	
Recording density:	2200 bits/inch, maximum	
Spare Tracks:	1 timing +4 data	1 timing +8 data
 Register Addresses		
Control/status 1	(RSCS1) 772 040	
Word count	(RSWC) 772 042	
UNIBUS address	(RSBA) 772 044	
Desired block address	(RSDA) 772 046	
Control/status 2	(RSCS2) 772 050	
Drive status	(RSDS) 772 052	
Error	(RSER) 772 054	
Attention summary	(RSAS) 772 056	
Look-ahead	(RSLA) 772 060	
Data buffer	(RSDB) 772 062	
Maintenance	(RSMR) 772 064	
Drive type	(RSDT) 772 066	

RJS04
RJS03
RS04
RS03

UNIBUS Interface

Interrupt vector address: 204
Priority level: BR5
Data transfer: NPR
Number of ports: 2
Bus loading: 1 bus load, each controller port

Mechanical

Mounting: Disk drive mounts in a standard PDP-11 cabinet (supplied): Controller is 2 system units, mounting assembly is not supplied
Size: 15-3/4-inch front panel height for disk drive
Weight (cab and 1 drive): 350 lbs
Weight (drive only): 120 lbs (RS04), 110 lbs (RS03)

Power Requirements

Drive

DC: none
AC: 90-132 VAC, 60 ± 1 Hz or 50 ± 1 Hz
180-264 VAC, 60 ± 1 Hz or 50 ± 1 Hz
Starting current: 13 A max at 115 VAC
6.5 A max at 230 VAC for 25 sec max
Running current: 6 A max at 115 VAC
3 A max at 230 VAC
Dissipation: 350 Watts

Controller

DC: 16 A at +5V
0.6 A at -15V
AC: none

Environment

	Operating	Non-Operating
Temperature:	10°C to 40°C	-40°C to +66°C
Relative humidity:	10% to 90% Maximum wet bulb 28°C Minimum dew point 2°C	0% to 90% Maximum Wet Bulb 29°C
Altitude:	8,000 ft.	30,000 ft.

Models

RJS03-BA: Disk drive and control, 256K words, 115 VAC, 60 Hz
RJS03-BD: Disk drive and control, 256K words, 230 VAC, 50 Hz
RJS04-BA: Disk drive and control, 512K words, 115 VAC, 60 Hz
RJS04-BD: Disk drive and control, 512K words, 230 VAC, 50 Hz
RS03-AA: Add-on Disk, 256K words, 115 VAC, 60 Hz
RS03-AD: Add-on Disk, 256K words, 230 VAC, 50 Hz
RS04-AA: Add-on Disk, 512K words, 115 VAC, 60 Hz
RS04-AD: Add-on Disk, 512K words, 230 VAC, 50 Hz

DECPACK DISK CARTRIDGE, RK11-D

DESCRIPTION

The RK11-D DECpack cartridge disk drive and control is a complete mass storage system, offering an economical solution for large volume, random-access data storage. The system includes a modular mass storage device utilizing removable disk cartridges and a complete easy-to-program control.

A disk cartridge holds over 1.2 million words. The DECpack is ideal where a large volume of programs and data are developed and maintained for one or more users. The system is expandable up to 9.6 million words per Control (8 disks).

An RK11-D includes a Control Unit and the first Disk Drive.

Operation

The removable disk cartridge offers the flexibility of virtually unlimited off-line capacity with rapid transfers of files between on-line and off-line without copying operations. It utilizes a cartridge similar to the IBM 2315, but with 12 sectors and twice the bit density.

Average total access time on each drive is 70 milliseconds. On expanded systems, operations are overlapped for efficiency; one drive may read or write while one or more additional drives are seeking new head positions for the next transfer. All data transfers utilize the Non-Processor Request facility during transfers.

Each disk is permanently mounted inside a protective case that automatically opens when inserted in the disk drive. While on-line, dust contamination is prevented by a highly-efficient continuous "absolute" air filtration system.

The DECpack provides accurate data storage and transfers by means of a write check function, correct cylinder verification by hardware, hardware checksum, and hardware maintenance features. There are no mechanical detents, thus a major source of wear and critical adjustment is eliminated.

CONTROLS & INDICATORS

RUN/LOAD
(rocker switch) Placing this switch in the RUN position (providing all interlocks are safe):

- a. locks the drive front door
- b. accelerates the disk to operating speed
- c. loads the read/write heads
- d. lights the RDY indicator.

Placing this switch in the LOAD position:

- a. unloads the read/write heads
- b. stops the disk rotation
- c. unlocks the drive front door
- d. lights the LOAD indicator.

CAUTION

Do not switch to the LOAD position during a write operation, as this results in erroneous data being recorded.

WT PROT
(rocker switch—
spring-loaded off)

Placing this momentary contact switch in the WT PROT position lights the WT PROT indicator and prevents a write operation as well as turns off the FAULT indicator if lit.

Placing this switch in the WT PROT position a second time turns off the WT PROT indicator and allows a write operation.

PWR
(indicator)

Lights when operating power is present. Goes off when operating power is removed.

RDY
(indicator)

Lights when:

- a. the disk is rotating at the correct operating speed
- b. the heads are loaded
- c. no other conditions are present (all interlocks safe) to prevent a seek, read, or write operation.

Goes off when the RUN/LOAD switch is set to the LOAD position.

ON CYL
(indicator)

Lights when:

- a. the drive is in the Ready condition
- b. a seek or restore operation is not being performed
- c. the read/write heads are positioned and settled.

Goes off during a seek or restore operation.

RK11

FAULT
(indicator)

Lights when:

- erase or write current is present without a WRITE GATE or,
- the linear positioner transducer lamp is in-operative.

Goes off when the WT PROT switch is pressed or when the drive is recycled through a RUN/LOAD sequence.

WT PROT
(indicator)

Lights when:

- the WT PROT switch is pressed (every other time) or,
- the operating system sends a Write Protect command.

Goes off when the WT PROT switch is pressed a second time or when the drive is recycled through a RUN/LOAD sequence.

LOAD
(indicator)

Lights when the read/write heads are fully retracted and the spindle has stopped rotating.

Goes off when the RUN/LOAD switch is set to the RUN position.

WT
(indicator)

Lights when a write operation occurs. Goes off when the write operation terminates.

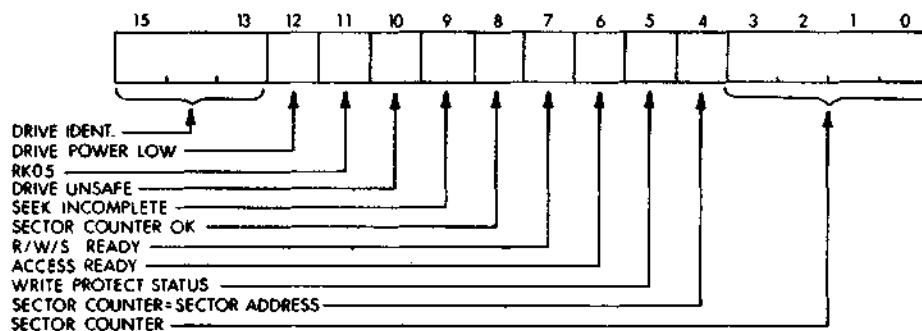
RD
(indicator)

Lights when a read operation occurs. Goes off when the read operation terminates.

REGISTERS

Drive Status Register (RKDS) 777 400

Contains the current selected drive status and current sector address.



Read only: all bits

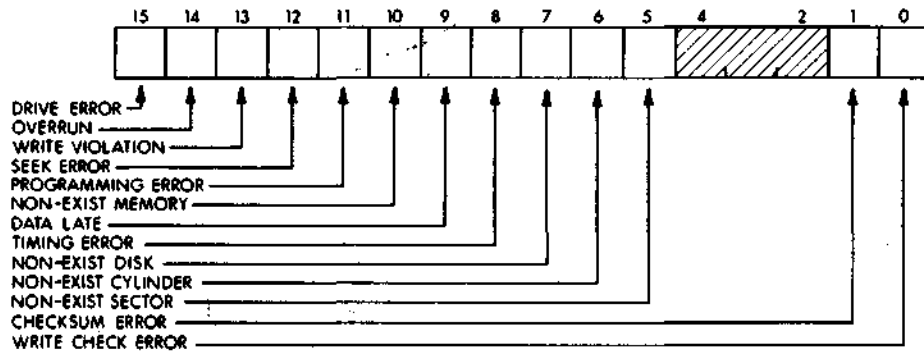
RK11

BIT	NAME	FUNCTION
15-13	Ident. of Drive (ID)	If an interrupt is caused as a result of a SEARCH COMPLETE (Bit 13 RKCS) or a SEEK INCOMPLETE (Bit 9 RKDS) these bits will contain the binary representation of the logical drive number that caused the interrupt.
12	Drive Power Low (DPL)	Set when an attempt is made to initiate a new function or a function was actively in progress when the control sensed a loss of power to one of the disk drives. This bit can be accompanied by bit 15 RKER (DRE) and is reset by a BUS INIT or a CONTROL RESET function.
11	RK05	Set to identify the selected disk drive as an RK05.
10	Drive Unsafe (DRU)	Set to indicate that an unusual condition has occurred in the drive and it is unable to properly perform any operations. Putting the RUN/LOAD switch in the LOAD position will reset the condition. If, upon putting the RUN/LOAD switch back to the RUN position the condition reoccurs the drive or associated power supply is inoperative and corrective maintenance procedures should be begun. Can be accompanied by bit 15 RKER.
9	Seek Incomplete (SIN)	Set to indicate that due to some unusual condition a SEEK function was not completed within 180ms of initiation. A DRIVE RESET function clears this condition. This bit can be accompanied by bit 15 RKER
8	Sector Counter OK (SOK)	Indicates that the selected drive sector counter (Bits 0-3 RKDS) is not in the process of changing and is ready for examination.
7	Drive Ready (DRY)	Set to indicate that the selected disk drive complies with the following conditions: a) properly supplied with power b) loaded with a disk cartridge c) door is closed

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- d) LOAD/RUN switch is in the RUN condition
 - e) the disk is spinning
 - f) the heads are properly loaded
 - g) the disk is not in a DRU condition (Bit 10 RKDS)
- | | | |
|-----|-----------------------------------|--|
| 6 | Read/Write/Seek Ready | Set when the selected drive head mechanism is not in motion and the drive is ready to accept a new function. |
| 5 | Write Protect Status (WPS) | Set when the selected disk is in WRITE PROTECTED mode |
| 4 | SC = SA | Set when the disk heads are currently positioned over the disk addresses currently held in bits 0-3 RKDA. |
| 3-0 | Sector Counter (SC) | Indicates the current sector address of the selected drive. This is the look ahead. Sector address 00 is defined as the sector which follows the sector that contains the index pulse. |

Error Register (RKER) 777 402



Read only: all bits.

BIT	NAME	FUNCTION
15	Drive Error (DRE)	Set when an attempt is made to initiate a function, or when a function is actively in progress, while the selected drive is not ready or in some error condition or if any of the drives in the system senses a loss of either AC or DC power. If this bit is found set the RKDS should immediately be referenced to discover the cause of the condition.

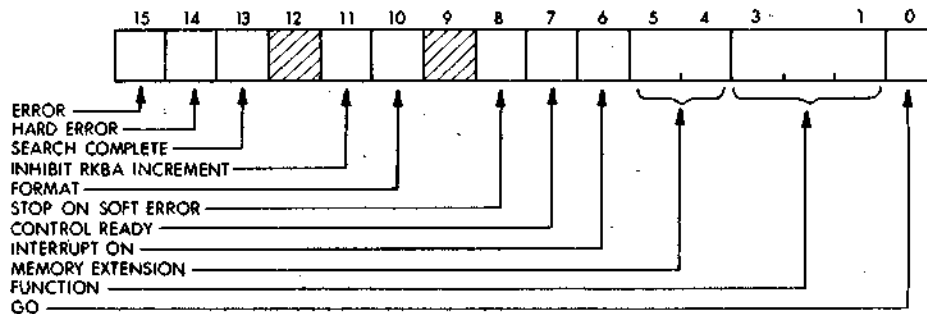
RK11

14	Overrun (OVR)	Set if during a READ, WRITE, RD/CHK or WT/CHK, operations on sector 13, surface 1 of cylinder address 312, were finished and the RKWC had not yet overflowed. This essentially is an attempt to overflow out of a disk drive.
13	Write Lock Out Violation (WLO)	Set if an attempt is made to write on a disk which is currently being write protected.
12	Seek Error (SKE)	Set if the disk head mechanism is not properly positioned while executing a normal READ, WRITE, RD/CHK or WT/CHK function.
11	Programming Error (PGE)	Set if the FMT bit (Bit 10 RKCS) is set while initiating some function other than a READ or WRITE.
10	Non-Existent Memory (NXM)	Set if memory does not respond within 20 μ s of the time when the RK11 becomes Bus Master during a DATI or DATO NPR sequence. Because of the speed of the disk drive, it is possible that if a NXM does occur it will be accompanied by a DLT (Bit 7 RKER).
9	Data Late (DLT)	Set when an NPR sequence is required before the previous one has completed.
8	Timing Error (TE)	Set if a loss of timing pulses for 5 μ sec has been detected.
7	Non-Existent Disk (NXD)	Set if an attempt was made to initiate a function on a non-existent drive.
6	Non-Existent Cylinder (NXC)	Set if an attempt was made to initiate a function on a cylinder larger than 312.
5	Non-Existent Sector (NXS)	Set if an attempt was made to initiate a transfer on a sector larger than 13.
1	Checksum Error (CSE)	Set while performing a RD/CHK or READ function as a result of faulty recalculation of the checksum. Cleared at the initiation of any new function. This is a soft error.
0	Write Check Error (WCE)	Set if an error was encountered during a WT/CHK function as a result of faulty bit comparison between disk data and memory data. Clears at the initiation of a new function. This is a soft error.

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Note: Bits 5 through 15 are all hard errors. They are cleared only by a BUS_INIT or a CONTROL CLEAR function.

Control Status Register (RKCS) 777 404



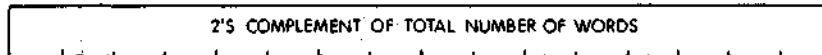
BIT	NAME	FUNCTION
15	Error	Set when any bit in the RKER is set. Processor reaction is dictated by Bits 6 and 8 RKCS. This read-only bit clears if all the bits in RKER are cleared and if Bit 14 RKCS is cleared.
14	Hard Error (H.E.)	Set when any of Bits 5-15 RKER are set by the control. Stops all controller action and processor reaction as dictated by bit 6 RKCS. This READ ONLY bit, along with bits 5-12 RKER, is cleared only by a BUS INIT or a CONTROL RESET function.
13	Search Complete (SCP)	Signifies that the previous interrupt was caused as a result of some previous SEEK or DRIVE RESET function. READ ONLY bit. Clears at the initiation of any new function.
11	Inhibit Inc. (INH BA)	Setting this bit inhibits incrementing the RKBA during a data transfer. This allows data to be transferred to or from any one bus address for the entire operation.
10	Format (FMT)	FORMAT Mode must be used only in conjunction with the normal READ and normal WRITE function. This mode is used to format a new disk pack or to reformat any sector that may have been erased or damaged due to control or drive failure. In the FORMAT mode the normal WRITE operation is altered only in that the servo positioner is not checked for proper position before the write operation. During a WRITE the header is re-written each time

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the associated sector is written. In this mode, the normal READ operation is altered in that only one word is transferred to memory per sector; the header word. Therefore, a 3-word READ function in the FORMAT mode will transfer 3 contiguous header words to 3 consecutive memory locations for software checking. For a 200-word transfer, 200 consecutive header words from 200 consecutive sectors will be read, and so on.

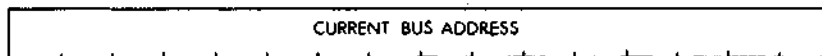
8	Stop on Soft Error (SSE)	If a soft error is encountered while this bit is set: a. and Bit 6 RKCS (IDE) is reset, all controller action will stop at the end of the current sector. b. and Bit 6 RKCS (IDE) is set, all controller action will stop and a Bus Request will occur at the end of the current sector.
7	Control Ready (RDY)	Signifies that the control is no longer engaged in actively executing a function and is ready to accept a command.
6	Int. on Done Enable (IDE)	The control will issue a Bus Request and interrupt to vector address 220 if: 1. A function has completed its activity; 2. A hard error is encountered; 3. A soft error is encountered and bit 8 RKCS is set.
5-4	Memory Extension (MEX)	Reserved for extended bus addresses and is used in conjunction with the RKBA. These bits make up a two-bit counter that increments each time the RKBA overflows. A bus DATO to these bits overrides any overflow from the RKBA.
3-1	Function	These bits indicate the binary representation of the function to be performed. The functions are: CONTROL RESET (000) WRITE (001) READ (010) WRITE CHECK (011) SEEK (100) READ CHECK (101) DRIVE RESET (110) WRITE LOCK (111)
0	Go	Initiates the function encoded in bits 1 through 3 of RKCS. Write only bit.

Word Count Register (RKWC) 777 406



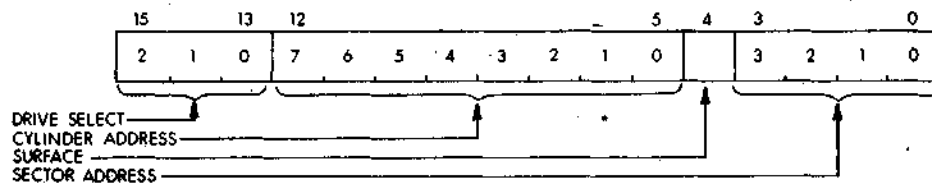
Contains the two's complement of the total number of words to be affected by a given function. It increments by one after each word transfer.

Current Bus Address Register (RKBA) 777 410



Contains the Bus Address to or from which data will be transferred. The register is incremented by two at the end of each transfer.

Disk Address Register (RKDA) 777 412



NOTE

All RKDA bits are loaded from the bus data lines only in RK11 READY state, and cleared by BUS INIT and Control Reset. The RKDA is incremented automatically at the end of each disk sector.

BIT	NAME	FUNCTION
15-13	Drive Select (DR SEL)	These bits contain the binary representation of the logical drive number currently being selected.
12-5	Cylinder Address (CYL ADD)	Binary representation of the cylinder address currently being selected. The largest valid address or number for the cylinder address is 312.
4	Surface (SUR)	When set, the lower disk head is enabled and operation is performed on the lower surface. When clear, the upper disk head is enabled.
3-0	Sector Address (SC)	Binary representation of the disk sector to be addressed for the next function.

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Data Buffer Register (RKDB) 777 416

BIT	NAME	FUNCTION
15-0	Data	This register is a general data handler. It is loaded from the bus only while the RK11 is bus master during an NPR sequence. The RKDB is constructed of a 6-word register file capable of sustaining a UNIBUS NPR latency of 55 μ sec every 85 μ sec.

Cross Cylinder Operation

Surface 0 is defined as the upper surface and is active when RKDA 04 is reset. If a transfer is initiated that requires an overflow from surface 0, the control will automatically change to sector 0 of surface 1 with no time loss. If a transfer is initiated that requires an overflow from surface 1, the control will automatically move the heads to the next cylinder, check for proper head positioning, and continue the transfer on sector 0 and surface 0 of the new cylinder. An attempt to overflow out of the last sector of the last cylinder will result in an error condition.

At the end of each sector of data transfer the RKDA is automatically incremented.

Hardware Poll

The control is capable of having any or all of the drives performing a SEEK or DRIVE RESET operation at any one time. A HARDWARE POLL feature will identify the logical drive number in bits 13, 14 and 15 of the RKDS of any drive that has completed a SEEK or DRIVE RESET operation and cause an interrupt if bit 6 RKCS is set (IDE) and the control is in the READY state (bit 7 RKCS is set) and the control was not already attempting to cause an interrupt as a result of some other operation. This will occur even if Bit 6 RKCS (IDE) was not set when first initiating the SEEK or DRIVE RESET function. If two or more drives complete the function simultaneously, the control will interrupt once for each drive and identify each one in turn in the RKDS. Care should be taken in this situation to raise the processor interrupt status to a level equal to or greater than that currently held by the RK11 or else a second interrupt will occur immediately after the first and the end result will be that the interrupt service routine has been interrupted. This situation will also occur if an attempt is made to initiate a SEEK to an address that the drive is already at since one interrupt will occur as a result of the SEEK function having been successfully initiated and another to report that the heads have reached their destination, which will occur immediately because the heads are already there.

Interrupts

Because of the format structure of the RK11, any interruption of a write sequence cannot be tolerated until the end of the sector because this would result in essentially an unformatted disk. Therefore, any outside intervention of this operation is held off until the end of the current sector, which includes the CONTROL RESET function and the PROCES-

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SOR or BUS INITIALIZE signals. Therefore, all those functions, such as CONTROL RESET, SEEK and WRITE LOCK, which normally take only a few microseconds to initiate can actually take up to 3.3ms if initiated while writing. For this reason the SEEK and WRITE LOCK functions will cause an interrupt (if bit 6 RKCS is set) as soon as the function has been successfully initiated. The CONTROL RESET, which cannot cause an interrupt under any circumstances, can, therefore, take up to 3.3ms to complete.

SPECIFICATIONS FOR RK11-D

Main Specifications

Storage medium:	disk cartridge
Capacity/cartridge:	1,228,800 words
Data transfer speed:	11.1 μ sec/word
Time for $\frac{1}{2}$ revolution:	20 msec
Disk rotation speed:	1500 RPM
Drives/control, max:	8

Track Positioning Time

One track move:	10 msec
Average:	50 msec
Maximum:	85 msec

Data Organization

Surfaces/drive:	2
Tracks/surface:	200 + 3 spare
Sectors/track:	12
Words/sector:	256
Recording method:	double frequency
Recording density:	2040 bits/inch, max
Access with single R/W:	1 to 65,536 words

Register Addresses

Drive Status	(RKDS)	777 400
Error	(RKER)	777 402
Control Status	(RKCS)	777 404
Word Count	(RKWC)	777 406
Current Bus Address	(RKBA)	777 410
Disk Address	(RKDA)	777 412
Data Buffer	(RKDB)	777 416

UNIBUS Interface

Interrupt vector address:	220
Priority level:	BR5
Data transfer:	NPR
Bus loading:	1 bus load

Mechanical

Mounting:	A standard cabinet is supplied for the drive
Disk drive:	Panel mounted, 10 $\frac{1}{2}$ " high
Disk control:	1 System Unit (SU)

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Power

Starting current: 10 A at 115 VAC for 2 seconds
Running current for drive: 2 A at 115 VAC
Current for control: 7.5 A at + 5 V
Heat dissipation: 160 W

Environmental

Operating temperature: 10°C to 40°C
Relative humidity: 10% to 90%

Models

RK11-DE: Disk drive and control, 115 VAC, 60 Hz
RK11-DJ: " 230 VAC, 50 Hz

SPECIFICATIONS FOR RK05

Mechanical

Mounting: mounts in a standard PDP-11 cabinet
Size: 10½" front panel height
Weight: 110 lbs.

Power

Starting current: 10 A at 115 VAC for 2 seconds
Running current: 2 A at 115 VAC
Heat dissipation: 160 W

Prerequisite: RK11-D

Models

RK05-AA: Disk drive, 115 VAC, 60 Hz
RK05-BB: " 230 VAC, 50 Hz
RK05-KA: Disk cartridge

DISK PACK, RP11-C

DESCRIPTION

The RP11-C is a complete mass storage system using a magnetic disk pack with 20 data surfaces and a moving read/write head. The RP11-C includes a Control Unit and the first Disk Pack Drive. The system is expandable up to 8 drives, each having a capacity of 20,480,000 16-bit words. Access times are 29 msec. average lateral (cylinder to cylinder) and 12.5 msec. half rotational. Record lengths of 1 to 65,536 words may be accessed with one read, write, or write check command. The RP11-C will read and write disk packs compatible with the PDP-10 and PDP-15 disk pack format.

The RP11-C provides hardware for execution of eight different functions.

Function	Code	Type
Idle	0	initiate
Write	1	execute
Read	2	execute
Write Check	3	execute
Seek	4	initiate
Write (no seek)	5	execute
Home Seek	6	initiate
Read (no seek)	7	execute

Initiate functions require only a small portion of the controller's time. For example, Home Seek and Seek require only 16 μ sec. of controller time for their execution. For this period of time, the controller is busy. Initiate commands require that the target unit be selected only for this busy period, i.e., although a Seek may require 50 msec. for completion, the unit need only be selected for the busy period. Idle (reset) requires only 4 μ sec. of RP11-C time. Execute instructions, however, require all the controller's time necessary to complete the function. The controller is busy for the entire operation and, therefore, cannot be interrupted for Initiate-type functions.

Functions are selected by loading a 3-bit FUNCTION REGISTER with an octal number equal to the function code.

There are three data registers and a silo memory in the RP11-C which provide compatibility between disk packs read and/or written by the RP10 or RP15 (PDP-10 and PDP-15 counterparts of the RP11-C). These registers are each 36-bits in length and provide multi-buffering between the PDP-11 and the RP03.

Silo Memory—The first-in first-out silo memory provides 64 words of buffering between the UNIBUS and the Disk. During write operations, the silo is loaded at UNIBUS rates with up to 64 16-bit data words. These are unloaded asynchronously into the 36-bit buffer register in

RP11

synchronism with the shift register load commands. During read operations, the silo is loaded in two or three separate cycles from the buffer register and initiates a UNIBUS memory cycle whenever a new data word "bubbles" to the output.

Buffer Register—During Write operations, data is transferred from the silo memory in two or three 16-bit memory cycles.

During Read operations, the contents of the buffer register is broken into two or three 16-bit bytes which are transferred to the silo memory in two or three consecutive operations.

Shift Register—For Write Operations, the contents of the buffer register are loaded into the shift register where it is serialized and transferred to the disk.

During Read operations, the serial data from the disk is assembled in the shift register and then transferred to the buffer register.

A 37th bit, which works in conjunction with the shift register, generates and checks odd word parity for Write and Read operations.

Longitudinal Parity Register—During Write operations, each 36-bit word of the buffer register is Exclusive ORed into the longitudinal parity register. At the end of each sector the contents of the longitudinal parity registers are written on the disk. This word is actually a bit position parity check.

During Read operations, each assembled word of the shift register is Exclusive ORed into the longitudinal parity register. At the end of each sector, the longitudinal parity register is checked for comparison with the longitudinal parity word written. Note that the RP11-C generates and checks both row and column parity in each sector.

REGISTERS

Device Status Register (RPDS) 776 710

The Device Status Register (RPDS) holds the current state of the selected drive and the Attention signals from each of the eight possible drives. The eight attention bits are read/clear. They can be selectively cleared by moving a 1 to the desired bit location(s). The other bits of RPDS are read only. The RPDS bits are shown with the significance of each bit when set.

RPDS 776 110

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SU RDY	SU OL	SU RPO3	HNF	SU SI	SU SU	SU FU	SU WP	ATTN 7	ATTN 6	ATTN 5	ATTN 4	ATTN 3	ATTN 2	ATTN 1	ATTN 0

INDICATES
READ/CLEAR

Device Status Register (RPDS)

Bit	Function
00-07	DRIVE 00-07 ATTENTION. ATTENTION is set by a drive when a Seek is successfully completed or a 100-ms period elapses after Seek initiation indicating an incomplete Seek.
08	SELECTED UNIT WRITE PROTECTED. This bit is set when the WRITE PROTECT switch on the selected drive is set and when contents of RPCA and RPDA fall within the bounds of the selected address lockout if the WRITE LOCKOUT switch is set.
09	SELECTED UNIT FILE UNSAFE. The selected drive has detected a self-error condition and is prohibiting all operations.
10	SELECTED UNIT SEEK UNDERWAY. The selected drive has initiated a Seek operation, but the Attention signal has not yet been returned.
11	SELECTED UNIT SEEK INCOMPLETE. The selected drive has failed to successfully complete a Seek operation.
12	HEADER NOT FOUND. The selected drive has completed a full revolution without locating the addressed sector.
13	SELECTED UNIT RP03. The selected drive is an RP03.
14	SELECTED UNIT ON LINE. The selected drive ENABLED/DISABLE switch is set to ENABLE.
15	SELECTED UNIT READY. The selected drive is capable of performing another operation.

Error Register (RPER) 776 712

The Error Register (RPER) contains all error conditions generated within the RP11-C controller. In the normal mode, RPER is a read only register; in the maintenance mode, Write into RPER capability is provided.

RPER 776 712

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WPV	FUV	NXC	NXT	NXS	PROG	FMTE	MODE	LPE	WPE	CSME	TIMEE	WCE	NXME	EOP	DSK ERR

RP11

Error Register (RPER)

Bit	Function
00	DISK ERROR. OR condition of header has not been found and the selected unit Seek is incomplete.
01	END OF PACK. Data transfer (Read or Write) is attempted across the end of the last sector of the pack.
02	NON-EXISTENT MEMORY. More than 10 μ s were required to complete a UNIBUS transaction.
03	WRITE CHECK ERROR. Data read from the disk pack does not compare with data read from memory during the Write Check operation.
04	TIMING ERROR. Data is lost because the UNIBUS did not respond in time to meet disk requirements.
05	CHECKSUM ERROR. Calculated checksum does not compare with that read from the disk.
06	WORD PARITY ERROR. Calculated word parity does not compare with that read from the disk.
07	LONGITUDINAL PARITY ERROR. Calculated longitudinal parity does not compare with that read from the disk.
08	MODE ERROR. Header operation was attempted while the RP11-C is in the PDP-11 mode.
09	FORMAT ERROR. Parity error was detected in a sector's header word.
10	PROGRAM ERROR. Data transfer operation was attempted with the content of the RPWC equal to zero, or an operation was attempted on an off-line drive, or while another instruction was still in progress.
11	NON-EXISTENT SECTOR. Disk operation was attempted when the content of the Sector Address Register was not within the 0 through 9 ₁₀ range.
12	NON-EXISTENT TRACK. Disk operation was attempted when the content of the Track Address Register was not within the 0 through 19 ₁₀ range.
13	NON-EXISTENT CYLINDER. Disk operation was attempted when the content of the Cylinder Address Register was not within the 0 through 405 ₁₀ range.
14	FILE UNSAFE VIOLATION. Disk operation was attempted when SUFU was true.
15	WRITE PROTECT VIOLATION. Disk Write operation was attempted when SUWP was true.

RP11

Control Status Register (RPCS) 776 714

The bit configuration loaded into the Control Status Register (RPCS) initiates and controls a disk function. All bits are read/write unless noted otherwise.

RPCS 776 714

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EER	HE	AIE	MODE	HDR	DRV SEL 2	DRV SEL 1	DRV SEL 0	RDY	IDE	MEX 1	MEX 0	COM 2	COM 1	COM 0	GO

Control Status Register (RPCS)

Bit	Function
00	GO. Set from the bus causes the RP11-C to initiate the operation encoded in bits 03 through 01 of the RPCS. This write-only bit is always read as a 0.
01-03	FUNCTION BITS. Specify the operation to be performed.
04-05	MEMORY EXTENDED ADDRESS. Specifies the 32K field of PDP-11 memory used in data transfer.
06	INTERRUPT ON DONE (ERROR) ENABLE. Causes the RP11-C to raise an interrupt request when a disk operation is complete, or if an error occurs.
07	READY. The RP11-C is in a condition to accept and execute a new operation. READY is a read-only bit.
08-10	DRIVE SELECT. Specify the disk drive which is to be the subject of any controller action.
11	HEADER. The function of the Function Register is a Header operation.
12	MODE. The RP11-C is conditioned to read or write disk packs in DECsystem-10 or PDP-15 format.
13	ATTENTION INTERRUPT ENABLE. Causes the RP11-C to raise an interrupt request whenever any drive raises its Attention line.
14	HARD ERROR. OR of all errors except data errors. This is a read-only bit.
15	ERROR. OR of all errors. This is a read-only bit.

NOTE

The RP11-C device handler software must include routines that will test the ERR and HE flags to validate the current operation before proceeding.

RP11

Word Count Register (RPWC) 776 716

The Word Count Register (RPWC) is loaded from the bus and specifies the number of words to be transferred during Read, Write, or Write Check operations. Incrementation takes place after a memory transaction has occurred and the RPWC, therefore, must be loaded with the 2's complement of the number of words to be transferred. The RPWC is a read/write register containing 16 bits.

NOTE

Because the disk pack system uses 36-bit disk words, the word count must be equal to a multiple of the number of PDP-11 memory words per disk word; i.e., in PDP-11 mode, there are two PDP-11 words per disk word and the word count must be a multiple of two. In PDP-10 or PDP-15 mode, there are three PDP-11 words per disk word, and the word count must be a multiple of three.

Bus Address Register (RPBA) 776 720

The Bus Address Register (RPBA) is loaded from the bus and specifies the bus address of data transferred during Read, Write, or Write Check operations. Incrementation takes place after a memory transaction has occurred. The RPBA, therefore, is loaded with the address of the first data word to be transferred (not first data word address minus one). The RPBA is a read/write register containing 16 bits.

Cylinder Address Register (RPCA) 776 722

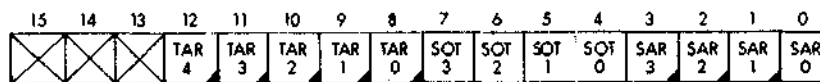
Bits 08-00 of the Cylinder Address Register (RPCA) are loaded from the bus and specify the disk cylinder for any disk operation. Bits 08-00 are read/write bits. Bits 15-09 are not used.

Disk Address Register (RPDA) 776 724

Bits 03-00 of the Disk Address Register (RPDA) are loaded from the bus and specify the disk sector address for any operation other than Seek or Home Seek. Bits 03-00 are read/write. Bits 07-04 are read-only bits which contain the current physical sector (number of sectors past index) of the selected drive.

Bits 12-08 are loaded from the bus to specify the track address for any disk operation. Bits 12-08 are read/write.

RPDA 776 724



SAR= SECTOR ADDRESS
SOT= PHYSICAL SECTOR
TAR= TRACK ADDRESS

RP11

Selected Unit Cylinder Address (SUCA) 776 734

The Selected Unit Cylinder Address (SUCA) register stores the contents of the selected RP03 cylinder address register in bits 08-00.

Maintenance 1 Register (RPM1) 776 726

The Maintenance 1 Register (RPM1) is read-only and provides a means for the PDP-11 to examine the state of the RP11-C's interface to the RP03 Disk Pack Drive. This register may be read at any time, but because of the asynchronous operation of the interface, meaningful results cannot be expected unless the RP11-C is in the maintenance mode.

Maintenance 1 Register, Address 776 726

Bit	Function
00-07	BUS OUT 00-07. BUS OUT 00-07 signals to the RP03 Disk Pack Drive.
08	SET CYLINDER. State of the control tag SET CYLINDER.
09	SET HEAD. State of the control tag SET HEAD.
10	CONTROL. State of the control tag CONTROL.
11	SILO IN READY. Silo is ready to receive data.
12	SILO OUT READY. Silo has data ready for output.

Maintenance 2 Register (RPM2) 776 730

The Maintenance 2 Register (RPM2) is write-only and, in conjunction with RPM3, allows the PDP-11 to simulate the RP03 Disk Pack Drive while in the maintenance mode. Loading this register in the normal mode has no effect.

Maintenance 2 Register

Bit	Function
00-07	MAINTENANCE ATTENTION 00-07. Simulate the Attention signals from the eight possible disk drives.
08-15	MAINTENANCE CYLINDER ADDRESS REGISTER. Set by the bus, simulate the lower eight bits of the Cylinder Address Register signals from the selected drive.

Maintenance 3 Register (RPM3) 776 732

The maintenance 3 Register (RPM3) is write-only and, in conjunction with RPM2, allows the PDP-11 to simulate the RP03 Disk Pack Drive

RP11

while in the maintenance mode. Loading this register in the normal mode has no effect.

Maintenance 3 Register

Bit	Function
00	MAINTENANCE CLOCK. When set by the bus causes one cycle of the RP11-C control clock to be generated.
01-07	Not Used
08	MAINTENANCE SECTOR. When set by the bus simulates a Sector Pulse from the selected drive.
09	MAINTENANCE END OF CYLINDER. When set by the bus simulates the selected drive signal End of Cylinder.
10	MAINTENANCE SEEK INCOMPLETE. When set by the bus simulates the selected drive signal Seek Incomplete.
11	MAINTENANCE FILE UNSAFE. When set by the bus simulates the selected drive signal File Unsafe.
12	MAINTENANCE INDEX. When set by the bus simulates an Index Pulse from the selected drive.
13	MAINTENANCE ON LINE. When set by the bus simulates the selected drive signal On Line.
14	MAINTENANCE READY. When set by the bus simulates the selected drive signal Ready.
15	MAINTENANCE READ ONLY. When set by the bus simulates the selected drive signal Read Only.

Silo Memory (SILO) 776 736

The Silo Memory is a 64-word, 16-bit, first-in/first-out (FIFO) MOS storage device. It can be loaded from the UNIBUS whenever the SILO IN READY bit in the Maintenance 1 Register is logic 1. If no readout is performed, the silo will accept 64 words before dropping SILO IN READY. The silo may be read whenever the SILO OUT READY bit in the Maintenance 1 Register is logic 1. As soon as all words previously stored have been read out, SILO OUT READY will go low and remain low until further data is stored. A transit time of 32 μ s maximum is required for an input word to "bubble" to the output.

For maintenance purposes, the Silo Memory is assigned a Unibus device register address, 776736. This allows maintenance personnel to check out that portion of the RP11-C by moving a data word to and from the Silo Memory.

RP11

SPECIFICATIONS FOR RP11-C

Main Specifications

Storage medium: disk pack
Capacity/pack: 20,480,000 words
Data transfer speed: 7.5 usec/word
Time for 1/2 revolution: 12.5 msec
Disk rotation speed: 2400 RPM
Drives/control, max: 8

Track Positioning Time

One track move: 7.5 msec
Average: 29 msec
Maximum: 55 msec

Data Organization

Surfaces/drive: 20
Tracks/surface: 400 (plus 6 spares)
Sectors/track: 10
Words/sector: 256
Bits/word: 16
Recording method: double frequency, NRZ
Recording density: 2200 bits/inch, max
Access with single R/W: 1 to 65,536 words

Register Addresses

Device Status (RPDS)	776 710
Error (RPER)	776 712
Control Status (RPCS)	776 714
Word Count (RPWC)	776 716
Bus Address (RPBA)	776 720
Cylinder Address (RPCA)	776 722
Disk Address (RPDA)	776 724
Maintenance 1 (RPM1)	776 726
Maintenance 2 (RPM2)	776 730
Maintenance 3 (RPM3)	776 732
Selected Unit (SUCA)	776 734
Cyl Adrs	
Silo Memory (SILO)	776 736

UNIBUS Interface

Interrupt vector address: 254
Priority level: BR5
Data transfer: NPR
Bus loading: 1 bus load

Mechanical

Mounting:	Disk	Control
Size:	1 free-standing unit	1 std PDP-11 cab.
Weight:	40"H x 30"W x 24"D	(supplied)
	415 lbs	325 lbs

RP11

Power

Input current: 7 A at 115 VAC
6 A at 230 VAC (3-phase)
Heat dissipation: 2100 W

Environment

Operating temperature: 15°C to 32°C
Relative humidity: 20% to 80%

Models

RP11-CE: Disk pack drive and control, 115 VAC, 60 Hz (for control)
RP11-CJ: " " 230 VAC, 50 Hz

SPECIFICATIONS FOR RP03

Mechanical

Mounting: 1 free-standing unit
Size: 40" H x 30" W x 24"D
Weight: 415 lbs

Power

Starting current: 30 A at 230 VAC, 60 Hz (3-phase)
Running current: 6 A at 230 VAC, 60 Hz (3-phase)
Heat dissipation: 1300 W

Prerequisite: RP11-C

Models

RP03-AS: Disk pack drive, 230 VAC, 60 Hz
RP03-BS: " " 230 VAC, 50 Hz

FLOPPY DISK SYSTEM, RX11

FEATURES

- High reliability
- Industry compatibility
- Ease of maintenance
- Simple operation
- Use as an I/O device or a random-access file device
- Low-cost, compact, removable diskettes
- 256,256 bytes of data storage capacity per diskette
- Average access time of 483 milliseconds
- Head loaded only when reading or writing
- Extensive operating system and diagnostic software support

DESCRIPTION

The RX11 Floppy Disk System is a highly reliable, low-cost, mass storage subsystem, capable of storing up to 256,256 8-bit bytes per drive in an industry-compatible format. The RX11 provides a compact data interchange and software distribution medium for critical I/O applications. In addition, the RX11's random-access capability allows configuring very low-cost, disk-based systems with small PDP-11 processors. Such systems can satisfy the needs of applications that could never before afford random access storage.

The RX11 Floppy Disk System consists of an RX01 Floppy Disk drive unit and a PDP-11 quad interface module which requires a single SPC slot. The RX01 includes either one or two drives, a microprogrammed controller module, and a read/write electronics module, all housed in a 10 $\frac{1}{2}$ inch, rack-mountable chassis. Up to two drives can be supported by each controller for a total storage capacity of 512,512 bytes.

Given an absolute sector address, the RX01 locates the desired sector and performs the indicated function. It automatically verifies head position and generates and verifies the cyclic redundancy check (CRC) character.

Track-to-track moves require ten milliseconds for the move plus twenty milliseconds for settling time if the head is loaded for a read or write. The rotational speed of the diskette is 360 rpm, which results in an average latency time of 83 milliseconds. The track-to-track move, head settling, and latency time produce an average access time of 483 milliseconds. During a sequential access, the whole diskette can be read in about thirty seconds.

THE MEDIA

The RX01 Floppy Disk uses the industry-standard "diskette" or "floppy" media, which are thin, flexible, oxide-coated disks similar in size to a

RX11

45-rpm phonograph record. The disk is recorded on one side only and is permanently contained in an 8-inch square, flexible envelope.

The envelope has a large center hole for the drive spindle, a small hole for track index sensing, and a large slit for the read/write head. A solenoid contact load pad is located on the opposite side of the envelope. The inside of the envelope is covered with a soft material, designed to wipe the disk surface clean just before reading.

The diskette contains 77 tracks and 26 sectors per track. Each sector can store 128 8-bit bytes for a total formatted capacity of 256,256 8-bit bytes.

The diskette is an ideal storage, interchange, and software distribution medium. Compared to disk cartridges or disk packs, it is very inexpensive. Because it is flat and thin, the diskette is compact, enabling large amounts of data to be conveniently stored in a small space. Diskettes can also be easily transported in a briefcase or in a manila envelope.

Because the diskette is preformatted in the industry-standard format, it ensures industry compatibility and drive-to-drive interchangeability. The RX01 can read diskettes written on other standard floppy disk equipment and vice versa. Preformatted diskettes also reduce hardware costs by eliminating the circuitry required to generate the correct format.

RELIABILITY

The RX01 provides exceptional reliability as well as low cost. The simple mechanical construction of the drive and the use of a microprogrammed controller that reduces hardware complexity contribute to the design goal MTBF (Mean Time Between Failures) of 5000 hours. To enhance disk life, the head contacts the disk only during reading or writing. With the head loaded on a given track, the media can withstand one million passes.

The RX01 performs parity checks and provides error indications. Each sector has a cyclic redundancy check (CRC) character as part of the header field and another CRC character as part of the data field. The RX01 generates and verifies the CRC characters and provides error indications.

OPERATION

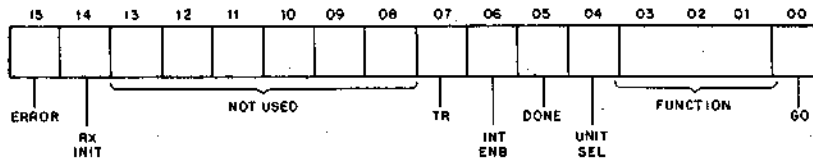
The RX01 Floppy Disk drive unit is simple to operate. When the door is opened, the diskette, properly oriented, can be inserted. When the door is closed, the diskette is engaged on the registration hub. Once the diskette drive attains operating speed, the software takes over. The diskette removal procedure is the reverse of the insertion procedure. Elimination of any other operator controls greatly simplifies operation.

REGISTERS

Command and Status (RXCS) 777 170

Loading this register while the RX01 is not busy and with bit 0 = 1 will initiate a function as described below. Bits 0—4 are write-only bits.

RX11



BIT

DESCRIPTION

- 0 Go—Initiates a command to RX01. This is a write-only bit.
- 1-3 Function Select—These bits code one of the eight possible functions. These are write-only bits.

Code	Function
000	Fill Buffer
001	Empty Buffer
010	Write Sector
011	Read Sector
100	Not used
101	Read Status
110	Write Deleted Data Sector
111	Read Error Register

- 4 Unit select—This bit selects one of the two possible disks for execution of the desired function. This is a write-only bit.
- 5 Done—This bit indicates the completion of a function. Done will generate an interrupt when asserted if Interrupt Enable (RXCS bit 6) is set. This is a read-only bit.
- 6 Interrupt Enable—This bit is set by the program to enable an interrupt when the RX01 has completed an operation (Done). The condition of this bit is normally determined at the time a function is initiated. This bit is cleared by Initialize and is a read/write bit.
- 7 Transfer Request—This bit signifies that the RX11 needs data or has data available. This is a read-only bit.
- 8-13 Unused
- 14 RX11 Initialize—This bit is set by the program to initialize the RX11 without initializing all of the devices on the Unibus. This is a write-only bit.

CAUTION

Loading the lower byte of the RXCS will also load the upper byte of the RXCS.

Upon setting this bit in the RXCS, the RX11 will negate Done and move the head position mechanism of drive 1 (if two are available) to track 0. Upon completion of a successful Initialize, the RX01 will zero the Error and Status register, set Initialize Done, and set RXES bit 7 (DRV RDY) if unit 0 is ready. It will also read sector 1 of track 1 on drive 0.

RX11

- 15 Error—This bit is set by the RX01 to indicate that an error has occurred during an attempt to execute a command. This read-only bit is cleared by the initiation of a new command or an Initialize.

Data Buffer Register (RXDB) 777 172

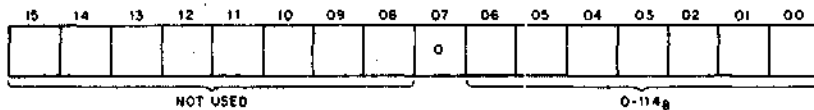
This register serves as a general purpose data path between the RX01 and the interface. It may represent one of four RX01 registers according to the protocol of the function in progress.

This register is read/write if the RX01 is not in the process of executing a command; that is, it may be manipulated without affecting the RX01 subsystem. If the RX01 is actively executing a command, this register will only accept data if RXCS bit 7 (TR) is set. In addition, valid data can only be read when TR is set.

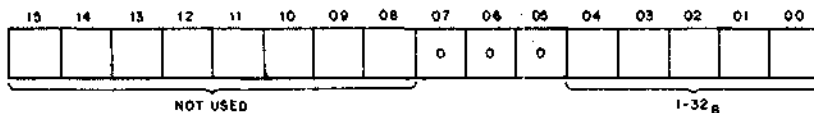
CAUTION

Violation of protocol in manipulating of this register may cause permanent data loss.

RXTA—RX Track Address—This register is loaded to indicate on which of the 114_8 tracks a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.



RXSA—RX Sector Address—This register is loaded to indicate on which of the 32_8 sectors a given function is to operate. It can be addressed only under the protocol of the function in progress. Bits 8 through 15 are unused and are ignored by the control.

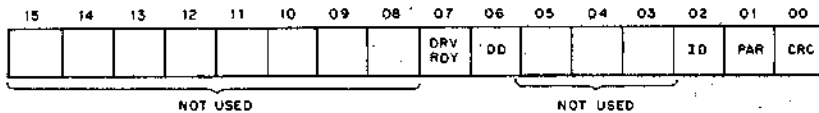


RXDB—RX Data Buffer—All information transferred to and from the floppy media passes through this register and is addressable only under the protocol of the function in progress.



RX11

RXES—RX Error and Status—This register contains the current error and status conditions of the drive selected by bit 4 (Unit Select) of the RXCS. This read-only register can be addressed only under the protocol of the function in progress. The RXES is located in the RXDB upon completion of a function.



BIT	DESCRIPTION
0	CRC Error—A cyclic redundancy check error was detected as information was retrieved from a data field of the diskette. The RXES is moved to the RXDB, and Error and Done are asserted.
1	Parity Error—A parity error was detected on command or address information being transferred to the RX01 from the Unibus interface. A parity error indication means that there is a problem in the interface cable between the RX01 and the interface. Upon detection of a parity error, the current function is terminated; the RXES is moved to the RXDB, and Error and Done are asserted.
2	Initialize Done—This bit is asserted in the RXES to indicate completion of the Initialize routine which can be caused by RX01 power failure, system power failure, or programmable or Unibus Initialize.
3-5	Unused
6	Deleted Data Detected—During data recovery, the identification mark preceding the data field was decoded as a deleted data mark.
7	Drive Ready—This bit is asserted if the unit currently selected exists, is properly supplied with power, has a diskette installed correctly, has its door closed, and has a diskette up to speed.

NOTES

The Drive Ready bit is only valid when retrieved via a Read Status function or at completion of Initialize when it indicates status of drive 0.

If the Error bit was set in the RXCS but Error bits are not set in the RXES, then specific error conditions can be accessed via a Read Error Register function.

SPECIFICATIONS

Main Specifications

Storage medium: preformatted diskette (industry-compatible)
Capacity per diskette: 256,256 8-bit bytes

RX11

Data transfer speed: 18 μ sec per byte
Time for half revolution: 83 msec
Diskette rotation speed: 360 rpm
Drives per control: 2 (maximum)

Track Positioning Time

One track move: 10 msec
Average track seek: 380 msec
Maximum track seek: 760 msec
Head settling: 20 msec
Average access time: 483 msec

Data Organization

Surfaces per diskette: 1
Tracks: 77
Sectors: 26
Capacity per sector: 128 8-bit bytes
Recording method: double frequency
Recording density: 3200 bits per inch maximum

Register Addresses

Command status (RXCS): 777170
Data buffer: 777172

UNIBUS Interface

Interrupt vector address: 264
Priority level: normally BR5
Data transfer: programmed I/O
Bus loading: 2 bus loads

Mechanical

Mounting: RX01 mounts in a standard PDP-11 cabinet. Interface requires one SPC slot.
Size: 10 $\frac{1}{2}$ inch front panel height + 1 SPC
Weight: 60 lbs. (dual drive)

Power

Running current: 5A maximum at 115V, 60 Hz (dual drive)
2.5A maximum at 230V, 50 Hz (dual drive)
Interface current: 1.5A maximum at +5 VDC
Heat dissipation: 500 watts maximum (dual drive)

Environmental

Temperature: 15° C (59° F) to 32° C (90° F) with a maximum temperature gradient of 20° F per hour or 11° C per hour
Relative humidity: 20% to 80% with a maximum wet bulb of 25° C (77° F) and a minimum dew point of 2° C (36° F)

RX11

Models

RX11-AA:	Single-drive system, 115Vac, 60 Hz
RX11-AD:	Single-drive system, 230 Vac, 50 Hz
RX11-BA:	Dual-drive system, 115Vac, 60 Hz
RX11-BD:	Dual-drive system, 230 Vac, 50 Hz

TAPE CASSETTE, TA11**DESCRIPTION**

The TA11 Magnetic Tape Cassette System is a reliable, inexpensive, dual-drive, reel-to-reel unit designed to replace paper tape. Its two drives run non-simultaneously using proprietary Digital Equipment Corporation Philips-Type cassettes. Engineered to provide users with optimum price/performance, the system offers the following features:

- **1 MIL TAPE.** Heavy mylar backing eliminates edge damage and resultant tape failure.
- **REEL-TO-REEL DRIVE.** Increases tape life. Only two driving elements. No pinch rollers, capstans, brakes, clutches, pulleys or belts.
- **SINGLE TRACK RECORDING.** Differentially balanced head eliminates external noise sensitivity. Low density and wide track recording ensure reliability.
- **DC MOTORS.** Linear servos provide precise, gentle tape acceleration and deceleration. Eliminate stretching and guarantees gap spacing.
- **SOLID-CASTING DRIVE.** All elements needed to control tape position, skew and motion are mounted on precision solid casting.
- **MODIFIED HUB.** Optimizes data capacity, simplifies loading.
- **LEADER DETECTION.** Optical, foolproof, failsafe.
- **CASSETTES INTERCHANGEABLE.** Assured by precision construction and frequency-independent read electronics.
- **ERROR CHECKING CIRCUITS.** 16-bit cyclic redundancy check.
- **PHASE-ENCODED RECORDING.** Read by sensitive, noise-immune peak detection circuits and phase lock loop.
- **SERVICEABLE.** Electronics, drives and power supply are easily accessible plug-in subassemblies.

The TA11 includes a Control Unit and a Dual Tape Transport.

Data Organization

In the TA11 Cassette System, data is recorded on tape in a single bit-serial track of data. Since there is no prerecorded timing or format track (such as in DECtape), data must be sequentially recorded and retrieved as in conventional magnetic tape systems.

The cassette medium is an oxide coated tape with sections of clear leader (no oxide) appended to both ends. Data can not be recorded in these clear leader sections, but they identify BOT (beginning of tape) and EOT (end of tape). Placement of data onto the recordable region of the cassette tape is organized into units called files. Adjacent files are separated by file gaps, which are generated under software control. Each file consists of one or more blocks separated by block gaps. Block gaps are generated automatically. Each block consists of one or more bytes of data and two cyclic redundancy check (CRC) bytes. Under program control, the CRC bytes are appended when a block is written and checked when a block is read. Each byte consists of eight bits (no parity). The number of files, blocks per file, and bytes per block is unrestricted, ex-

TA11

cept for tape capacity. Tape capacity is 92,000 bytes, minimum. This is reduced by 300 bytes per file gap and 46 bytes per block gap.

CONTROLS & INDICATORS

There are three manual controls on the tape drive. Each drive contains a separate REWIND pushbutton and a Power-On indicator. The Power ON/OFF toggle switch for the entire transport is located on the chassis rear panel. These manual controls and indicators perform the following functions:

REWIND—Pressing this momentary contact pushbutton on one of the two drives, rewinds the tape on that drive, at high speed, to the Beginning-of-Tape (BOT) marker provided:

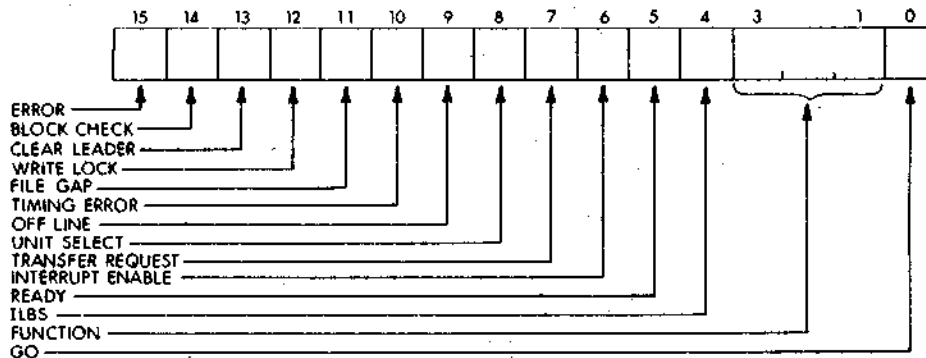
- a. a cassette is loaded.
- b. tape is not moving under program control.

Pressing this switch during a program controlled operation has no effect. thick, mylar substrate

Power ON/OFF—Placing this switch in the ON position lights both Power-On indicators (located opposite the REWIND pushbuttons on the lower door of each drive) and activates the internal dc power supply. Conversely, placing this switch in the OFF position de-activates the power supply and turns off both Power-On indicators.

REGISTERS

Control and Status Register (TACS) 777 500



Effect of the Initialize (INIT) signal: clear bits 8 to 6, 4 to 1; set bit 5

Read only: bit 15 through 9, 7, and 5

Write only: bit 0

BIT NAME	FUNCTION
15 Error	Set to indicate an error condition determined by the current status indicators of TACS, bits 14 through 9 and the current function, bits 3 through 1. Error bit is valid only when ready is set.

TA11

BIT	NAME	FUNCTION
14	Block Check	Set to indicate a CRC error for READ and SFB. During a READ function, Block Check sets Error. During an SFB function, the bit is normally expected and does not set Error. Cleared when the next function is successfully initiated.
13	Clear Leader	Set when the currently selected cassette is at EOT or BOT. The bit sets Error for all functions except REWIND.
12	Write Lock	Set to indicate that the currently selected cassette is write-protected if and only if the current function bits are set for WRITE or WFG. The bit sets Error.
11	File Gap	Set when a file gap has been entered during a READ, SFB, SRF or SFF function. The bit sets Error only on READ and SFB. Cleared when the next function is successfully initiated.
10	Timing Error	Set when the program's response to Transfer Request was not quick enough and signifies loss of data during READ or WRITE function. The bit sets Error. Cleared when the next function is successfully initiated.
9	Off Line	Set when the currently selected cassette is not present or when there is no power in the cassette transport. The bit sets Error on all functions.
8	Unit Select	Specifies which transport is under program control 0 for left (unit 0); 1 for right (unit 1).
7	Transfer Request	Set when data is available in Data Buffer, TADB, during READ, or request for data during WRITE. Cleared when TADB is addressed. The bit is held clear by ILBS. It inhibits Ready from setting and must be serviced prior to Ready.
6	Interrupt Enable	Set to enable Ready or Transfer Request = 1 to cause an interrupt.
5	Ready	Set when the Cassette is ready to accept and execute a command. It is cleared when a function is initiated and set when the function is completed as long as Transfer Request is clear.
4	ILBS	Initiate Last Byte Sequence. Set to terminate WRITE function by causing the transport to write the CRC bytes, and to terminate READ function by causing the transport to read and check the next two bytes on tape as CRC characters. For an n-byte block, ILBS is set in response to the $n + 1$ Transfer Request. The bit holds Transfer Request clear.

TA11

Tape Characteristics

Length: 150 ft.
Type: computer-grade, 100% certified, 1 mil thick, mylar substrate

Register Addresses

Command and Status
(TACS) 777 500
Data Buffer (TADB) 777 502

UNIBUS Interface

Interrupt vector address: 260
Priority level: BR6
Bus loading: 1 bus load

Mechanical

Mounting: 1 panel mounted unit + 1 SPC slot
Size: 5 1/4" front panel height + quad module
Cable: 15 ft., supplied; 25 ft., max.

Power

Input current: 1 A at 115 VAC
1.5 A at + 5 V
Heat dissipation: 120 W

Environmental

Operating temperature: 10°C to 40°C
Relative humidity: 20% to 80%

Models

TA11-AA: Dual cassette unit and control, 115 VAC, 60 Hz
TA11-AB: " " " " 230 VAC, 50 Hz
TU60-K: Cassette with 150 ft. of certified tape

Miscellaneous

Error control: 16-bit cyclic redundancy check (CRC), hardware generated and appended to data at time of writing. Tested during read by hardware via program command.

Read electronics: Peak detection/phase lock loop (low threshold read).

Typical block format:

Pre-Gap	Pre-amble	"N" Data Bytes	CRC Character	Post-Gap
.25"	32 bit		$(x^{16} + x^{15} + x^2 + 1)$.25"

DECTAPE, TC11-G

DESCRIPTION

The TC11-G is a dual-unit, bidirectional magnetic-tape transport system for auxiliary data storage. Low cost, low maintenance and high reliability are assured by:

- Simply designed transport mechanisms which have no capstans and no pinch rollers.
- Hydrodynamically lubricated tape guiding (the tape floats on air over the tape guides while in motion)
- Redundant recording
- Manchester phase recording techniques (virtually eliminate drop outs)

Each transport has a read/write head for information recording and playback on five channels of tape. The system stores information at fixed positions on magnetic tape as in magnetic disk or drum storage devices, rather than at unknown or variable positions as in conventional magnetic tape systems. This feature allows replacement of blocks of data on tape in a random fashion without disturbing other previously recorded information. In particular, during the writing of information on tape, the system reads format (mark) and timing information from the tape and uses this information to determine the exact position at which to record the information to be written. Similarly, in reading, the same mark and timing information is used to locate data to be played back from the tape.

A DECTape system consists of up to 4 dual transports, a Control Unit (which will buffer and control information for up to four dual transports) and DECTape 3/4-inch magnetic tape on 3.9-inch reels. A TC11-G includes a Control Unit and the first dual Tape Transport.

Operation

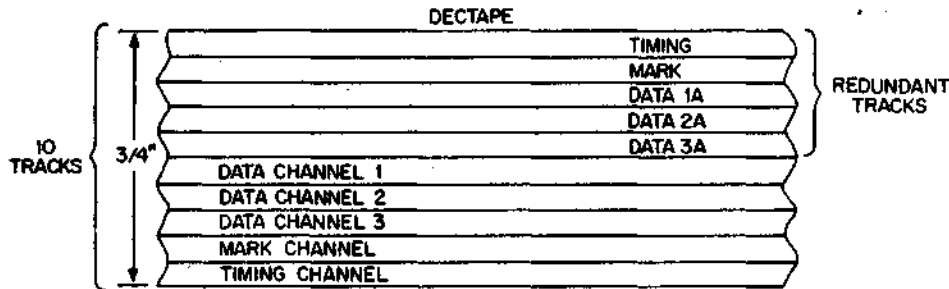
The system utilizes a 10-track read/write head. The first five tracks on the tape include a timing track, a mark track, and three data tracks. The other five tracks are identical counterparts and are used for redundant recording to increase system reliability. The redundant recording of each character bit on non-adjacent tracks materially reduces bit dropouts and minimizes the effect of skew. The use of Manchester phase recording, rather than amplitude sensing techniques, virtually eliminates dropouts.

The timing and mark channels control the timing of operations within the Control Unit and establish the format of data contained on the information channels. The timing and mark channels are recorded prior to all normal data reading and writing on the information channels. The timing of operations performed by the tape drive and some control functions are determined by the information on the timing channel. Therefore, wide variations in the speed of tape motion do not affect system performance.

The standard format tape is divided into 578 blocks. The structure of

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each block is symmetric: block numbers and checksums are recorded at both ends of a block and thus searching, reading, or writing can occur in either direction. However, a block read in the opposite direction than it was written will have the order of the data words reversed.



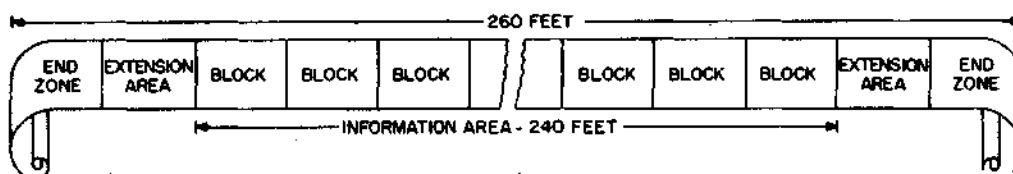
DECTape Format

Information read from the mark channel is used during reading and writing data to indicate the beginning and end of data blocks and to determine the functions performed by the system in each control mode. The data tracks are located in the middle of the tape where the effect of skew is minimum. The data in one bit position of each track is referred to as a line or as a character. Since six lines make up a word, the tape can record 18-bit data words. During normal data writing, the Control disassembles the 18-bit word and distributes the bits so they are recorded as six 3-bit characters. Since PDP-11 words are 16-bits long, the Control writes the extra two bits as 0's and ignores them when reading. However, during special modes, the extra two bits can be written and recovered.

A 260-foot reel of DECTape is divided into three major areas: end zones (forward and reverse), extension zones (forward and reverse), and the information zone. The two end zones (each approximately 10 feet) mark the end of the physical tape and are used for winding the tape around the heads and onto the take-up reel. These zones never contain data.

The forward and reverse extension areas mark the end of the information region of the tape. Their length is sufficient to ensure that once the end zone is entered and tape motion is reversed, there is adequate distance for the transport to come up to proper tape speed before entering the information area.

The information area, consists of blocks of data. The standard is a nominal 578 blocks, each containing 256 data words (nominally). In addition each block contains 10 control words.

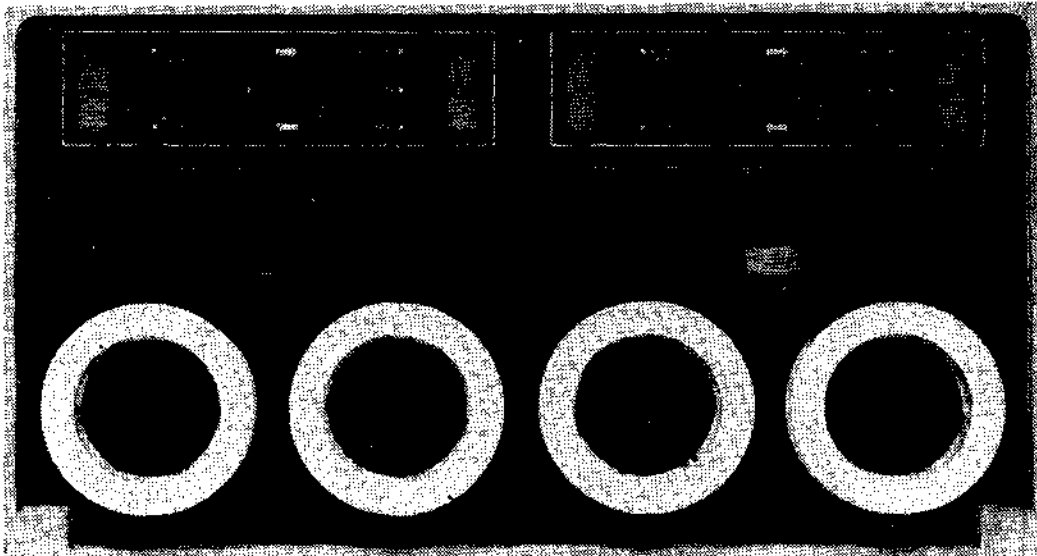


DECTape Block Arrangement

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The blocks permit digital data to be partitioned into groups of words which are interrelated while at the same time reducing the amount of storage area that would be needed for addressing individual words. A simple example of such a group of words is a program. A program can be stored and retrieved from magnetic tape in a single block format because it is not necessary to be able to retrieve only a single word from the program. It is necessary, however, to be able to retrieve different programs which may not be related in any way. Thus, each program can be stored in a different block on the tape.

Since DECTape is a fixed address system, the programmer need not know accurately where the tape has stopped. To locate a specific point on tape he must only start the tape motion in the search mode. The address of the block currently passing over the head is read into the DECTape Control and loaded into an interface register. Simultaneously, a flag is set and a program interrupt can occur. The program can then compare the block number found with the desired block address and tape motion continued or reversed accordingly.



DECTape Unit

CONTROLS & INDICATORS

REMOTE/OFF/LOCAL
(rocker switch)

Placing this switch in one of the following positions accomplishes:

- a. REMOTE—disables the Fwd/Hold/Rev switch and places the transport under computer control (on-line).

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- b. **LOCAL**—enables the Fwd/Hold/Rev switch and removes the transport from computer control (off-line).
- c. **OFF**—removes power from the reel motors and removes the transport from computer control.

→ ←
Fwd/ Hold/ Rev
(rocker switch: spring-loaded to Hold)

Placing this switch in the Fwd position (provided **REMOTE/OFF/LOCAL** is in **LOCAL**) moves the tape from left to right across the read/write head.

When this switch is in the spring-loaded Hold position (provided **REMOTE/OFF/LOCAL** is in **LOCAL**), the tape remains stationary.

Placing this switch in the Rev position (provided **REMOTE/OFF/LOCAL** is in **LOCAL**) moves the tape from right to left across the read/write head.

Address Select
(0 to 7 thumbwheel switch)

Configures the transport logic to respond to the address indicated on the thumbwheel.

WRITE ENABLE/WRITE LOCK
(rocker switch)

Placing this switch in the **WRITE ENABLE** position lights the **WRITE** indicator and allows a write operation.

Placing this switch in the **WRITE LOCK** position turns off the **WRITE** indicator and prevents a write operation.

REMOTE SELECT
(indicator)

Lights when the transport is in the remote (on-line) mode and is selected by the controller.

Goes off when the transport is in the off or local (off-line) modes or is deselected by the controller.

WRITE
(indicator)

Lights when the **WRITE ENABLE/WRITE LOCK** switch is in the **WRITE ENABLE** position.

Goes off when the **WRITE ENABLE/WRITE LOCK** switch is in the **WRITE LOCK** position.

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PROGRAMMING

All transport operations are controlled by the Control Unit from program instructions. The Control selects the transport, controls tape motion and direction, selects a read or write operation and buffers data transferred.

The Control can select any one of eight commands that control operation of the DECTape system. When the system is operated on-line, these commands are used for reading or writing data on the tape and for controlling tape motion. The desired command is selected by the program which sets or clears bits 3, 2, and 1 in the command register (TCCM) to specify an octal code representing the desired command.

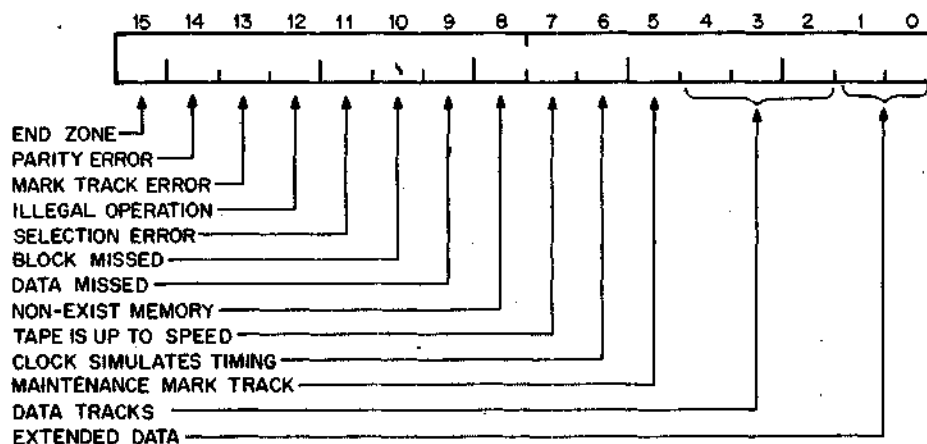
The commands are:

OCTAL CODE	MNEMONIC	FUNCTION
0	SAT	Stops all tape motion.
1	RNUM	Finds the mark track code that identifies the block number on the tape in the selected tape unit. Block number found is available in the data register (TCDT).
2	RDATA	Assembles one word of data at a time and transfers it directly to memory. Transfers continue until word count overflow, at which time data is read to the end of the current block and parity is checked.
3	RALL	Reads information on the tape that is not read by the RDATA function.
4	SST	Stops all tape motion in selected transport only.
5	WRTM	Writes timing and mark track information on blank DECTape. Used for formatting new tape.
6	WDATA	Writes data into the three data tracks. 16 bits of data are transferred directly from memory.
7	WALL	Writes information on areas of tape not accessible to WDATA function.

All software control of the TC11 DECTape system is performed by means of five device registers. They can be read or loaded using any PDP-11 instruction that refers to their address.

REGISTERS

Control and Status Register (TCST) 777 340



Effect of the Initialize (INIT) signal: clear bits 15, 14, 13, 10 through 7, 5, 1 and 0.

BIT	NAME	FUNCTION
15	End Zone (ENDZ)	Set to indicate that the selected tape unit is in an end zone region of the tape. It is cleared by loading a 0 into bit 15 (ERROR) of command register (TCCM), cleared by loading a 1 into bit 0 (DO) of the command register. Stops selected tape unit.
14	Parity Error (PAR)	Set to indicate a parity error. The parity error occurs during RDATA function if the calculated and written checksums disagree. Cleared in the same manner as ENDZ (bit 15).
13	Mark Track Error(MTE)	Set when an error occurred during decoding of the mark track. Stops selected tape unit. Cleared in the same manner as ENDZ.
12	Illegal Operation(ILO)	Set to indicate an illegal operation caused by a conflict in switch positions of the WRITE ALL, WRITE T&M, and WRITE ENABLE/WRITE LOCK switches. These conflicts are: a. WRITE LOCK on during WRTM, WALL, or WDATA modes

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- b. WRITE T&M switch off during WRTM mode
- c. WRITE ALL switch off during WALL mode

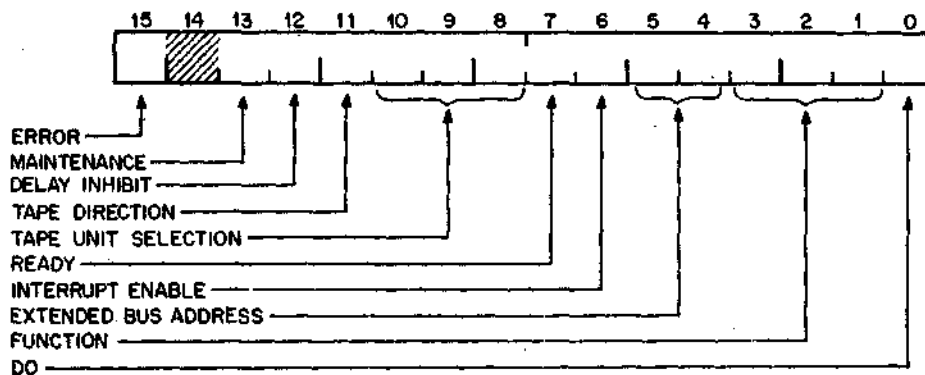
Stops selected tape unit. Cleared when switches reset to valid positions or when a non-conflicting operation is selected.

- 11 Selection Error(SELE) Set when the program has either selected a non-existent tape unit or has attempted to select more than one tape unit. Stops selected tape unit. Disabled if MAINT bit (bit 13 in TCCM) is set or if function is SAT (bits 3, 2, and 1 in TCCM cleared). Cleared when unit selection switches set to valid positions or when another unit is selected.
- 10 Block Missed(BLKM) Set when a block was missed. The transfer from read block number (RNUM) to read data (RDATA) or write data (WDATA) functions occurred too late. Also, indicates switch to RDATA from WDATA was too late. Cleared in the same manner as ENDZ.
- 9 Data Missed(DATM) Set when data was missed. Request for data transfer not honored in time during RDATA, WDATA, WALL, or RALL. Cleared in the same manner as ENDZ.
- 8 Non-Existent Memory(NEX) Set to indicate non-existent memory. This occurs when TC11 Controller is bus master and does not receive a SSYN response within 20 μ s after asserting MSYN. Cleared in the same manner as ENDZ.
- 7 Tape Is Up To Speed(UPS) Set when selected tape unit is up to speed required for proper operation. Cleared when UNIT SELECT or REV bit is changed. Set when unit is up to speed; set when MAINT bit (bit 13 in command register) is set, or when the selected function is WRTM.

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- | | | |
|---|-----------------------------|---|
| 6 | Clock Simulates Timing(CLK) | Used to simulate timing track. May be loaded when MAINT bit is set. When CLK is set, produces TP1; when cleared, produces TPO. |
| 5 | Maint Mark Track(MMT) | Used to simulate the bit read from the mark track. May be loaded when MAINT bit is set. |
| 4 | Data Track 0(DT0) | Used to simulate output of the read amplifier when loaded; when read, reads the input to the write amplifier. When MAINT bit is set, DT0 loads into RWB2 and reads as RWB5. |
| NOTE | | |
| Bits 4, 3, and 2 function as six bits. When loaded, they simulate the read amplifier and are loaded into RWB2, RWB1, and RWB0. When read, they read the write amplifier inputs from RWB5, RWB4, and RWB3. | | |
| 3 | Data Track 1(DT1) | Functions the same as DT0 except loads into RWB1, reads as RWB4. |
| 2 | Data Track 2(DT2) | Functions the same as DT0 except loads into RWB0, reads as RWB3. |
| 1 | Extended Data 17(XD17) | Allows reading and writing on areas of the tape not accessible during 16-bit word transfers. |
| 0 | Extended Data 16(XD16) | |

Command Register (TCCM) 777 342



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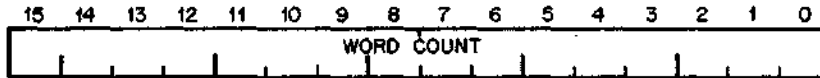
Effect of the Initialize (INIT) signal: clear bits 13 through 8, 6 through 1; set bit 7

Read only: bit 7

Write only: bit 0

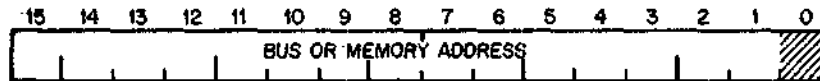
BIT	NAME	FUNCTION
15	Error	Set to indicate an error condition which is the inclusive OR of all error conditions (bits 15-8 in TCST). Causes an interrupt if enabled (see bit 6). Clears errors (except ILO and SELE) when loaded with zero. Sets READY bit (bit 7).
13	Maintenance(MAINT)	Used for maintenance functions. When set, enables operation of bits 6-2 in the TCST.
12	Delay Inhibit(DINHB)	Set to inhibit the delay associated with bringing a tape unit up to speed when reselecting a tape unit known to be up to speed by a previous command.
11	Tape Direction(REV)	Specifies direction of tape motion. When set, specifies reverse motion; when cleared, specifies forward motion.
10-8	Unit Select	Specifies the number of the tape unit which is to receive the desired command. These three bits are set or cleared to represent an octal code which corresponds to the unit number of the tape unit to be used.
7	READY	Set when the Control is ready to receive a new command. Cleared when DO (bit 0) is set. Set when command execution is complete; set by ERROR (bit 15).
6	Interrupt Enable(IE)	Set to allow either READY (bit 7) or ERROR (bit 15)=1 to cause an interrupt.
5-4	Ext Bus Address(XBA)	Used to specify address line 17 (bit 5) or address line 16 (bit 4) in direct memory transfers. Increments with the TCBA.
3-1	Function Bits	Specifies a command to be performed upon the selected transport. Cleared by INIT to SAT.
0	DO	Set when a new function is given. Clears READY.

Word Count Register (TCWC) 777 344



BIT	NAME	FUNCTION
15-0	Word Count	Contains two's complement of the number of words to be transferred. This register counts the number of word transfers made during RDATA (read data) and WDATA (write data) functions. When one of these functions is initiated, the word count register is loaded. The register is incremented by 1 after each transfer. When the contents of the register equals all zeros, further transfers are inhibited. Cleared by INIT. (Note: This register must not be modified by using byte instructions. Use only word instructions when loading).

Bus Address Register (TCBA) 777 346



BIT	NAME	FUNCTION
15-1	Address	Specifies the bus or memory address to or from which data is to be transferred during RDATA (read data) and WDATA (write data) operations. These bits are used in conjunction with bits XBA17 and XBA16 in the command register. After each transfer (during RDATA and WDATA) is made, this register is incremented to advance it to the next word location. The XBA bits in TCCM participate in the incrementation; they are a logical extension to this register. Cleared by INIT. (Note: the bus address register must not be modified by using byte instructions when loading this register).

Data Register (TCDT) 777 350

BIT	NAME	FUNCTION
15-0	Data	Contains data word read from or to be written on the magnetic tape. These bits and bits XD17 and XD16 in the status

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register form the 18 bits which correspond one to one with the six 3-bit characters read or written on the tape.

The data register accepts information under program control during WALL (write all) and WRTM (write timing and mark) operations. During RALL (read all) and RNUM (read block number) operations, the data register contains data read from the tape. During WDATA (write data) and RDATA (read data) operations, the data register is used to buffer information between the controller and memory. Cleared by INIT.

Note: The data register must not be modified by using byte instructions. Use only word instructions when loading this register.

PROGRAMMING EXAMPLES

The following two examples represent typical methods of programming the TC11 Control. The first example finds a specified block. The second example is a routine for writing data into a specific block.

Routine to find a specified block

;ENTER WITH R0 = BLOCK WANTED
;FINDS BLOCK IN FORWARD DIRECTION

```
SEARCH:  MOVE R0, BWANT
          SUB #3, BWANT          ;OFFSET
          MOV #4003, TCCM        ;UNIT 0, REVERSE, RNUM, DO

LOOP1:   BIT #100200, TCCM      ;CHECK READY AND ERROR
          BEQ LOOP1
          BMI ERROR
          SUB TCDT, #BWANT      ;CHECK BLOCK FOUND
          BLT SEARCH

FORWRD:  MOV R0, BWANT
          MOV #3, TCCM          ;UNIT 0, FORWARD ,RNUM, DO

LOOP2:   BIT #100200, TCCM      ;CHECK FOR READY AND
          ;ERROR
          BEQ LOOP2
          BMI ERROR
          SUB TCDT, BWANT      ;CHECK BLOCK FOUND
          BGT FORWRD
          BLT SEARCH
          RTS PC                ;RETURN WHEN BLOCK IS
          FOUND
```


TC11

Tape Characteristics

Length: 260 ft
Type: 1 mil, Mylar sandwich, Mylar protected on both sides
Reel diameter: 3.9 inches
Handling: Direct drive hubs and specially designed guides float the tape over the head. No capstans or pinch rollers.

Register Addresses

Control and Status	(TCST)	777 340
Command	(TCCM)	777 342
Word Count	(TCWC)	777 344
Bus Address	(TCBA)	777 346
Data	(TCDT)	777 350

UNIBUS Interface

Interrupt vector address: 214
Priority level: BR6
Data transfer: NPR
Bus loading: 1 bus load

Mechanical

Mounting: mounts in a std PDP-11 cabinet (supplied)
Size: 10 $\frac{1}{2}$ " panel height for tape drive
+ 10 $\frac{1}{2}$ " for control unit

Power

Input current: 9 A at 115 VAC
Heat dissipation: 870 W

Environmental

Operating temperature: 15°C to 32°C
Relative humidity: 20% to 80%

Models

TC11-GA: Dual tape drive and control, 115 VAC, 60 Hz
TC11-GB: " " , 230 VAC, 50 Hz

SPECIFICATIONS FOR TU56

Mechanical

Mounting: mounts in a std PDP-11 cabinet
Size: 10 $\frac{1}{2}$ " front panel height
Weight: 80 lbs

Power

Input current: 3 A at 115 VAC
Heat dissipation: 350 W

Prerequisite:

TC11-G

Model

TU56: Dual tape drive

MAGNETIC TAPE SYSTEM, TJU16

FEATURES

- 1600-bpi, 9-track data storage
- Program-selectable recording at 1600 bpi (phase encoded) or 800 bpi (NRZI)
- Data formats are industry compatible
- 72,000-character/second transfer rate
- Up to 40-million characters of storage per reel
- Reading in reverse (in addition to forward)
- Expandable to eight tape drives in a single system
- Vacuum column for tape buffer
- High reliability

DESCRIPTION

The TJU16 is a fully integrated, high-performance magnetic tape storage system that is specifically designed to operate with DIGITAL's PDP-11 computers. It uses standard recording formats, with densities of 1600 and 800 bits per inch, selectable under program control. Reading and writing are performed at 45 inches/second. Since the industry standard format is used, data may be easily transferred between computers. For example, a PDP-11 system might be used to collect and record data for later processing on another, larger computer. Use of magnetic tape permits unlimited off-line data storage.

There are two distinct TJU16 models: phase-encoded at 1600 bpi and NRZI at 800 bpi, and NRZI only (both with 9 tracks). The TJU16 includes a control unit plus the master tape control electronics and the first tape drive supplied in a standard cabinet. One control unit can handle up to eight tape drives.

Data Organization

Each vertical frame of the 9-track tape represents one character and contains eight data bits plus one parity bit. Since the 16-bit PDP-11 word contains two 8-bit bytes, one byte corresponds to one tape character, for efficient data storage.

Groups of characters form a record. The industry standard has 18 to 2048 characters in a single record. Each record block is separated by an interrecord gap (IRG) that is a minimum distance of one-half inch.

Parity is checked character-by-character when reading and writing on tape to verify the accuracy of data transfer. With NRZI, there is also a cyclic redundancy check (CRC) character generated or checked at the end of each record, plus a longitudinal parity check (LPC) character. If an error is detected, an error indication is made.

Operation

Reading can be performed while tape is moving in the forward or reverse direction, but writing occurs only in forward. The control unit can move the tape to new positions in forward or reverse. The control unit

also monitors tape operation. Interrupts are generated when processor attention is required, or when an error occurs.

Tape motion is controlled by vacuum columns and a servo-controlled single capstan. Long tape life is possible because the only contact with the oxide surface is at the magnetic head and at a rolling contact on one low-friction, low-inertia bearing. The half-inch mylar-base tape is coated on one side with an iron oxide composition. The load and end points of the tape are marked by reflective strips which are detected by photo diodes. Approximately 10 feet of blank tape are wound on a reel, preceding the beginning of tape (BOT) and end of tape (EOT) strips. A gap of about three inches is left from the load point before writing can begin, with NRZI. With PE, an identification burst (IDB) is written in this gap.

The tape drive can be controlled locally by the control panel. Local (off-line) controls are: On-line/Off-line, Forward/Reverse/Rewind, Unit Select, Start/Stop, and Brake Release/Load. When on-line, program commands accepted by the transport are: Rewind and Go Off-line, Read Forward, Read Reverse, Write, Write Tape Mark, Space Forward, Space Reverse, Erase, and Rewind to BOT.

There is a provision to prevent accidental writing on a particular tape reel. An industry-standard write-protect ring on the reel is sensed by the tape drive.

Reliability

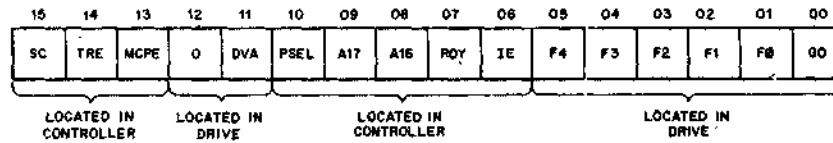
Data reliability of the TJU16 tape system is enhanced by the 1600-bpi, phase-encoding, self-clocking feature which is not dependent on precise tape skew control. In addition, the 800-bpi NRZI mode includes a tight read-after-write check. The written data is checked to insure that it far surpasses the minimum allowable reading level.

Bad tape error problems are minimized by a "runaway timer" which allows the system to recover from bad tape sections on the reel. If no reading or writing is performed within a tape distance of approximately 25 feet, tape movement will stop and an error will be indicated. Data will not be acknowledged as comprising a data block unless there are at least 12 characters in the block.

Upgrading

An NRZI 800-bpi-only tape system can be upgraded to have the 1600-bpi phase-encoded capability. An upgrade option is available for installation by Digital Field Service at the customer's site.

Control and Status 1 (MTCS1) Register (772440)



BIT	NAME	FUNCTION
15	SC Special condition Read only	Set by TRE, ATTN, or I/O bus control parity error. Cleared by Unibus A INIT, controller clear, or by removing the ATTN condition.
14	TRE Transfer error Read/write	Set by DLT, WCE, UPE, NED, NEM, PGE, MXF, MDPE, or a drive error during a data transfer. Cleared by Unibus A INIT, controller clear, error clear, or loading a data transfer command with GO set.
13	MCPE Mass I/O bus control bus parity error Read only	Set by parity error on control bus while reading a remote register (located in the drive). Cleared by Unibus A INIT, controller clear, error clear, or loading a data transfer command with the GO bit set. Parity errors that occur on the I/O control bus while writing a drive register are detected by the drive and cause the PAR error (MTER register, bit 03) to set.
12	Not used	Always read as a 0.
11	DVA Drive available Read only	Always a 1 in the TM02 when read from an existing drive.
10	PSEL Port select Read/write	When PSEL = 1, data transfer is via Unibus B; when PSEL = 0, data transfer is via Unibus A. Cleared by Unibus A INIT, controller clear, or by writing a 0 in this bit position.
9	A17	Upper extension bits of the MTBA register. Cleared by Unibus A INIT, controller clear or by writing 0s in these bit positions.
8	A16 Unibus address Read/write	
7	RDY Ready Read/only	RDY normally = 1. During data transfers, RDY = 0. When a data transfer command code (51 _s - 77 _s) is written into MTCS1, RDY is reset. At the termination of the data transfer, RDY is set.

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BIT	NAME	FUNCTION
06	IE Interrupt enable Read/write	IE is a control bit which can be set only under program control. When IE = 1, an interrupt may occur due to RDY or ATTN being asserted. Cleared by Unibus A INIT, controller clear, or automatically cleared when an interrupt is recognized by the CPU. When a 0 is written into IE by the program, any pending interrupts are cancelled.
05-00	F4-F0 and GO bit Read/write	<p>F4-F0 are function (command) code control bits that determine the action to be performed. The function code bits are stored in the selected drive.</p> <p>The GO bit (MTCS1, bit 0) must be set to cause the controller or drive to respond to a command. The GO bit is reset by the drive after command execution.</p> <p>Cleared by Unibus A INIT or controller clear (will abort command execution in all drives).</p>

Function Code F(0-5) (octal)	Operation
01	No Op
03	Rewind Off-line*
07	Rewind
11	Drive Clear
25	Erase
27	Write Tape Mark
31	Space Forward
33	Space Reverse
51	Write Check Forward
57	Write Check Reverse
61	Write Forward
71	Read Forward
77	Read Reverse

* Requires manual intervention to return transport on-line.

Word Count (MTWC) Register (772442)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC	WC
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

BIT	NAME	FUNCTION
15-00	WC Word count Read/write	Set by the program to specify the number of words to be transferred (2's complement form). This register is cleared only by writing 0s into it. Incremented for each data transfer.

Unibus Address (MTBA) Register (772444)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	BA	0
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

BIT	NAME	FUNCTION
15-01	BA 15-01 Unibus address Read/write	Loaded by the program to specify the starting memory address of a transfer. Cleared by Unibus A INIT or by controller clear. The BA register is incremented by 2 after each transfer of a word to or from memory.

Frame Count (MTFC) Register (772446)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC	FC
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

BIT	NAME	FUNCTION
15-00	FC 15-00 Frame count Read/write	Cleared by writing 0s in the bit locations. Designates in 2's complement form the number of records to be spaced over, characters to be written, or characters that have been read. Initiating a write or space command when the frame count register is loaded with zeros implies a count of 2 ¹⁶ .

Control and Status 2 (MTCS2) Register (772450)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	LPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	FAT	BAI	U2	U1	U0

BIT	NAME	FUNCTION
15	DLT Data late Read only	Set when the controller is unable to supply a data word during a write operation or accept a data word during a read or write-check operation at the time the drive demands a transfer. Also set when the controller is performing a data transfer

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BIT	NAME	FUNCTION
		operation over the second Unibus (PSEL = 1) and a Unibus B INIT is received on that port. Cleared by Unibus A INIT, controller clear, error clear, or loading a data transfer command with GO set. DLT causes TRE. A DLT error indicates a severely overloaded bus. Can also be set by the program reading or writing the MTDB register.
14	WCE Write check error Read only	Set when the controller is performing a write-check operation and a word on the tape does not match the corresponding word in memory. Cleared by Unibus A INIT, controller clear, error clear, or loading a data transfer command with GO set. WCE causes TRE. If a mismatch is detected during a write-check command execution, the transfer terminates and the WCE bit is set. The memory address displayed in MTBA [and extension] is the address of the word following the one which did not match (if BAI is not set). The mismatched data word from the tape drive is displayed in the data buffer (MTDB).
13	PE Parity error Read/write	Set if the parity lines indicate a parity error while the controller is performing a write or write-check command. Cleared by Unibus A INIT controller clear, error clear, or loading a data transfer command with GO set. PE causes TRE. When the Unibus is selected to do 18-bit data transfers, the PE error is disabled. When a parity error occurs, the MTBA register contains the address +2 of the memory word with the parity error (if BAI is not set). This bit may be set by program control for diagnostic purposes.
12	NED Non-existent drive Read only	Set when the program reads or writes a drive registers (CS1, DS, ER, MR, FC, DT, CK, TC, or SN) in a drive [selected by U(02:00)] which does not exist or is powered down. (The drive fails to assert TRA within 1.5 μ s after assertion of DEM.) Cleared by Unibus A INIT, controller clear, error clear, or loading a data transfer command with GO set. NED causes TRE.

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BIT	NAME	FUNCTION
11	NEM Non-existent memory Read only	Set when the controller is performing a DMA transfer and the memory address specified in MTBA is nonexistent (does not respond to MSYN within 10 μ s). Cleared by Unibus A INIT, controller clear, error clear, or loading a data transfer command with GO set. NEM causes TRE. The MTBA contains the address +2 of the memory location causing the error.
10	PGE Program error Read only	Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. Cleared by Unibus A INIT, controller clear, error clear, or loading a data transfer command with GO set. PGE causes TRE. The data transfer command code is inhibited from being written.
09	MXF Missed transfer Read/write	Set if the drive does not respond to a data transfer command within 250 ms. Cleared by Unibus A INIT, controller clear, error clear, or loading a data transfer command with GO set. MXF causes TRE. This bit can be set or cleared by the program for diagnostic purposes. This error occurs if a data transfer command is loaded into a drive which has ERR set, or if the drive fails to initiate the command for any reason (such as a parity error).
08	MDPE Mass I/O bus data bus parity error Read only	Set when a parity error occurs on the data bus while doing a read or write-check operation. Cleared by Unibus A INIT, controller clear, error clear, or loading a data transfer command with GO set. MDPE causes TRE. Parity errors on the bus data bus during write operations are detected by the drive and cause the PAR error.
07	OR Output ready Read only	Set when a word is present in MTDB and can be read by the program. Cleared by Unibus A INIT, controller clear, or by reading DB. Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to read the DB register before OR is asserted will cause a DLT error.

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BIT	NAME	FUNCTION
06	IR Input ready Read only	Set when a word may be written in the DB register by the program. Cleared by reading the DB. Serves as a status indicator for diagnostic check of the Silo buffer. An attempt to write the DB register before IR is asserted will cause a DLT error. This bit is for diagnostic purposes only.
05	CLR Controller clear Write only	When a 1 is written into this bit, the controller and all drives are initialized. Unibus A INIT also causes controller clear to occur.
04	PAT Parity test Read/write	While PAT is set, the controller generates even parity on both the control bus and data bus of the I/O bus. When clear, odd parity is generated. Cleared by Unibus A INIT or controller clear. While PAT is set, the controller checks for even parity received on the data bus but not on the control bus.
03	BAI Unibus address increment inhibit Read/write	When BAI is set, the controller will not increment the BA register during a data transfer. This bit cannot be modified while the controller is doing a data transfer (RDY negated). Cleared by Unibus A INIT or controller clear. When set during a data transfer, all data words are read from or written into the same memory location.
02-00	U 02-00 Unit select Read/write	These bits are written by the program to select a drive. Cleared by Unibus A INIT or controller clear. The unit select bits can be changed by the program during data transfer operations without interfering with the transfer. The CS1, DS, ER, MR, FC, DT, CK, TC, and SN registers contain bits that come from the selected drive.

Drive Status (MTDS) Register (772452)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	EOT	NOT USED	DPR	DRY	SSC	PES	SDWN	IOB	TM	BOT	SLA

BIT NAME	FUNCTION
15 ATA Attention active Read only	<p>Set by the drive when there is an attention condition in that drive. Cleared by Unibus A INIT, controller clear, drive clear, loading a command with the GO bit set, or loading a 1 in the MTAS register in the bit position corresponding to the drive's unit number. (The last two methods of clearing the ATA bit will not clear the error indicators in the drive.)</p> <p>An attention condition indicates one of the following:</p> <ol style="list-style-type: none"> 1. The TM02 and the selected transport require servicing due to SSC (see bit 6 in this Table). 2. The TM02 and the selected transport have become ready after a non-data transfer operation. 3. At the completion of any operation with EOT asserted.
14 ERR Error summary Read only	<p>Set when one or more of the error bits is set in the MTER register of the selected drive. Cleared by Unibus A INIT, controller clear, or by drive clear.</p> <p>This bit is the logical OR of all the bits in the MTER register. This bit is not cleared by loading a command other than drive clear. While ERR is asserted, commands other than drive clear are not accepted by the drive.</p>
13 PIP Positioning in progress Read only	<p>Set by the drive while the space or rewind command is under way. Cleared at the completion of the operation.</p>
12 MOL Medium on-line Read only	<p>Set when the selected slave is loaded and the on-line switch activated. This condition is necessary for response to any commands—if GO = 1 and MOL = 0, the command is aborted and UNS and ATA are asserted. This bit is not affected by drive clear or INIT. Indicates selected slave is ready for immediate use. Any change in status of MOL will set ATA.</p>
11 WRL Write locked Read only	<p>Set whenever a reel of tape without a write enable ring is loaded on the selected slave. This bit is not affected by drive clear or INIT. Indicates that the selected slave transport is write protected.</p>

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BIT	NAME	FUNCTION
10	EOT End of tape Read only	Set when the EOT marker is recognized during forward tape motion. Cleared when the EOT marker is passed over during reverse tape motion. This bit is not affected by drive clear or INIT, however, execution of a rewind command causes EOT to be cleared.
08	DPR Drive present Read only	Always a 1.
07	DRY Drive ready Read only	Set by INIT or at the completion of a command. Cleared whenever a valid command (with the GO bit asserted) is loaded into MTCS1. Indicates that the drive is on-line and prepared to accept a command.
06	SSC Slave status change Read only	Set when any slave transport requires attention due to one of the following conditions: a) Completion of a rewind b) Power failure c) Coming on-line d) Going off-line Cleared by INIT. Drive clear will clear this bit if the SSC condition was raised by the selected slave and no other slaves are posting SSC.
05	PES Phase encoded status Read only	Set when the selected slave is in PE mode. Cleared when the selected slave is in NRZI mode. This bit is not affected by drive clear or INIT.
04	SDWN Slowing down Read only	Set during the period when tape motion is stopping. This bit is not affected by drive clear or INIT.
03	IDB Identification burst Read only	Set in PE mode on recognition of the PE identification burst. Cleared when another command is issued, or cleared by drive clear or INIT. In the forward direction, the bit remains set through the reading, writing, or spacing operation. On a PE tape, IDB should be asserted after any tape motion operation which began from BOT.
02	TM Tape mark Read only	Set when a tape mark is detected and remains set until the next tape motion operation is initiated. Cleared by INIT or drive clear.
01	BOT Beginning of tape Read only	Set when the selected slave detects the BOT marker. This bit is not affected by drive clear or INIT. Cleared by passing BOT (Beginning of Tape) in the forward direction.

BIT	NAME	FUNCTION
00	SLA Slave attention Read only	Set by a selected slave which requires attention due to coming on-line. Cleared by drive clear or INIT.

Error (MTER) Register (772454)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
COR/ UNS	OP1	DTE	NEF	CS/ ITM	FCE	NSG	PEF/ LRC	INC/ VPE	OPAR	FMT	CPAR	RMR	ILR	ILF	

BIT	NAME	FUNCTION
15	COR/CRC Correctable data error/CRC error Read only	PE mode—set on a tape character. Therefore, PE error correction logic was able to correct the data on-the-fly and good data was transferred to memory. NRZ mode—set when the CRC character generated from read back data does not agree with the CRC read from tape. Cleared by drive clear or INIT.
14	UNS Unsafe Read only	Set if the GO bit in the MTCS1 register is set, the MOL bit in the MTDS register is reset, and a command code other than drive clear is issued. Also set if the TM02 detects an imminent power fail condition (AC LO asserted, DC LO not asserted). If UNS is caused by GO = 1 while MOL = 0, it is cleared by CLR or DRIVE CLEAR. If UNS is caused by a transient voltage-low condition, it can be cleared by INIT or drive clear when voltage returns to an acceptable level. If UNS is caused by a permanent voltage-low condition, it cannot be cleared.
13	OPI Operation incomplete Read only	A read or space operation indicates that a tape record has not been detected within 7 sec from command initiation. A write operation indicates that a read-after-write tape record has not been detected within 0.7 sec from command initiation. Can also indicate that NSG > 0.08 inches. Cleared by INIT or drive clear.
12	DTE Drive timing error Read only	Set (1) during a write operation if WCLK was not received from the controller in time to provide a valid tape character, or (2) when a data transfer is attempted when the bus is already occupied (OCC = 1). Cleared by

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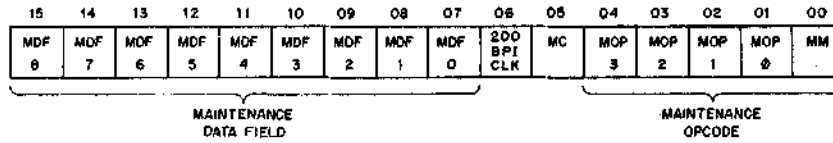
BIT NAME	FUNCTION
11 NEF Non-executable function Read only	<p>INIT or drive clear. When DTE is asserted, the drive also asserts EBL and EXC and aborts the command.</p> <p>Set when:</p> <ol style="list-style-type: none">1. A write operation is attempted on a write-protect transport.2. A space reverse, read reverse, or write check reverse is attempted when the tape is at BOT.3. The DEN 2 bit in the tape control register does not agree with the PES status bit (i.e., selected drive not capable of selected density).4. A space or write operation is attempted when $FCS = 0$ in the tape control register.5. A read or write operation is attempted with $DEN2 = 0$ in the tape control register and the 2's complement of a number less than 13 is in the frame count register. <p>Cleared by drive clear or INIT.</p>
10 CS/ITM Correctable skew/ illegal tape mark Read only	<p>In PE mode, this bit is set when excessive but correctable skew is detected in data read back from tape. It is a warning only, and does not indicate that bad data was read from tape.</p> <p>In NRZ mode, this bit is set when a bit pattern is detected on tape which has the general characteristics of an NRZ filemark (specifically, two single characters separated by seven blank character spaces) but which does not contain the exact data expected in an NRZ filemark. Cleared by drive clear or INIT.</p>
09 FCE Frame count error Read only	<p>Set when a space operation has terminated and the frame counter is not cleared. Also set when the controller fails to negate RUN when the TM02 asserts EBL. Cleared by drive clear or INIT.</p>
08 NSG Non standard gap Read only	<p>Set after a data transfer operation whenever any tape characters are read while the read head is scanning the first half of the inter-record gap. Cleared by drive clear or INIT.</p>

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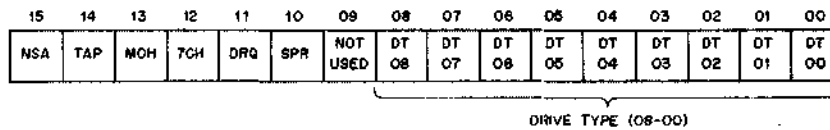
BIT NAME	FUNCTION
07 PEF/LRC PE format error/LRC Read only	Set in PE mode when an invalid preamble or postamble is detected. Set in NRZ mode when the LRC character generated from read-back data does not match the LRC character read from tape. Cleared by drive clear or INIT.
06 INC/VPE Incorrectable data/vertical parity error Read only	A PE read operation indicates that one of the following has occurred: <ol style="list-style-type: none">1. Multiple dead tracks2. Parity errors without dead tracks3. Skew overflow During an NRZ read operation, indicates that a vertical parity error has occurred or that data has occurred after the skew delay is over. Cleared by drive clear or INIT.
05 DPAR Data bus parity error Read only	Set when a parity error is detected on the data lines during a write operation. Cleared by drive clear or INIT.
04 FMT Format error Read only	Set when a data transfer is attempted with an incorrect format code (i.e., the tape format code loaded in the MTTC register is not implemented on that TM02). Cleared by drive clear or INIT.
03 CPAR Control bus parity error Read only	Set when a parity error is detected on the control lines during a control bus write operation. Cleared by drive clear or INIT.
02 RMR Register modification refused Read only	Set when the controller attempts to write into any implemented TU16 register except the maintenance register or the attention summary register while the GO bit is asserted. If RMR occurs, the addressed register is not modified. Cleared by drive clear or INIT.
01 ILR Illegal register Read only	Set when a read or write from a non-existent register is attempted. Cleared by drive clear or INIT.
00 ILF Illegal function Read only	Set when the GO bit is asserted and a function code not implemented by the TM02/TU16 is attempted. Cleared by drive clear or INIT.

Maintenance (MTMR) Register (772464)

The maintenance register is a 16-bit read/write register for diagnostic testing.



Drive Type (MTDT) Register (772466)

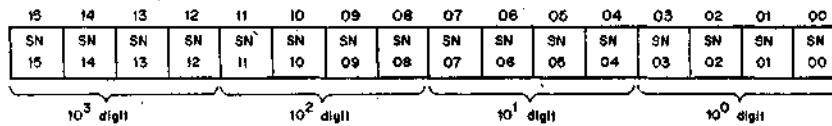


BIT	NAME	FUNCTION
15-14		Always a 1.
13	MOH Moving head Read only	Always a 0.
12	7CH 7 Channel Read only	Always a 0.
11	DRQ Drive request required Read only	Always a 0.
10	SPR Slave present Read only	Asserted when a transport is powered up and has been assigned the selection code contained in the MTTC tape control register.
08-00	DT 08-00 Drive type Read only	Contains the drive type number for the selected slave (11 _s for the TM02/TU16). If no slave is assigned in bit 0-2 of the MTTC tape control register, the drive type code readback is 010 _s . If a slave has been assigned a select code in bits 0-2 of this register, the drive type code will be a code from 11 _s to 17 _s . Drive clear or INIT do not affect these bits.

Serial Number (MTSN) Register (772470)

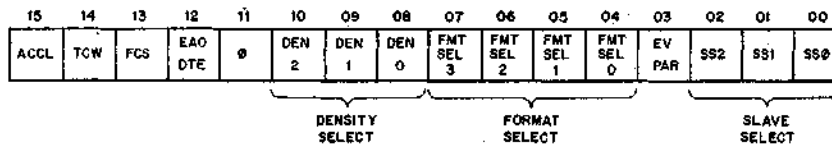
The serial number register is a 16-bit, read-only register which contains a BCD representation of the four least significant digits of the transport serial number.

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BIT	NAME	FUNCTION
15-12	SN15-SN12	Most significant BCD digit (10^3) of slave serial number. Read only
11-08	SN11-SN08	10^2 digit of slave serial number. Read only
07-04	SN07-SN04	10^1 digit of slave serial number. Read only
03-00	SN03-SN00	Least significant BCD digit of slave serial number. Read only

Tape Control (MTC) Register (772472)



BIT	NAME	FUNCTION
15	ACCL Acceleration	Set when the transport is not actively reading or writing data. ACCL is not affected by drive clear or INIT. Read only
14	FCS Frame count status	Normally set at the end of a write into the frame count register. Cleared when frame count register overflows. Cleared by drive clear or INIT. Read only
		Loading a space or write command with the GO bit asserted and FCS equal to 0 will cause a non-executable function (NEF-bit 11 of drive status register) to be asserted and will cause the command to be aborted. No tape motion will occur.
13	TCW Tape control write	Set when a control bus write operation to the tape control register is performed. Cleared by the initiation of any command requiring tape motion. Read only
		TCW is used by the TM02 to determine whether or not to wait for the completion of the settle down process (SDWN-bit 4 of the drive status register). If TCW is asserted,

BIT	NAME	FUNCTION																							
		SDWN should be negated before issuing a new command to the selected slave.																							
12	EAODTE Enable abort on data transfer errors Read/write	This bit, when written to a 1, will cause a data transfer operation to be aborted as soon as one of the following errors is detected: a. DPAR-bit 5 of MTER register b. COR/CRC-bit 15 of MTER register c. FMT/LRC-bit 7 of MTER register d. INC/VPE-bit 6 of MTER register																							
10-8	DEN2-DEN0 Density select	Specifies the tape character density during read or write operations. <table border="1"> <thead> <tr> <th>DEN 2</th> <th>DEN 1</th> <th>DEN 0</th> <th>bpi</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>200</td> <td rowspan="3">} NRZ</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>556</td> </tr> <tr> <td>0</td> <td>1</td> <td>0 or 1</td> <td>800</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1600</td> <td>PE</td> </tr> </tbody> </table> Drive clear and INIT do not affect the density select bits.	DEN 2	DEN 1	DEN 0	bpi		0	0	0	200	} NRZ	0	0	1	556	0	1	0 or 1	800	1	0	0	1600	PE
DEN 2	DEN 1	DEN 0	bpi																						
0	0	0	200	} NRZ																					
0	0	1	556																						
0	1	0 or 1	800																						
1	0	0	1600	PE																					
07-04	FMT SEL 3-0 Format select Read/write	Specifies I/O bus-to-tape character formatting during a write operation, or tape character-to-I/O bus formatting during a read operation. If the FMT SEL bits specify a format not implemented on a TM02/TU16 system and a valid data transfer command is loaded in the MTCS1 register with the GO bit asserted, the format error bit (FMT-bit 4 of the MTER register) will be asserted and the operation will abort.																							
03	EV PAR Even parity Read/write	If this bit is set in NRZ mode, even parity will be written on tape and even parity is expected on read-back. If this bit is reset, odd parity will be written on tape and will be expected on read-back. When the TM02 is operating in NRZ with EV PAR set, it will not allow an all zeros character to be written on tape. If an all zeros character is presented to the TM02, the TM02 will invert binary bit 4 and the parity bit before writing the character on tape. This converts 000 ₈ to 020 ₈ . This bit is ignored in phase encoded (PE) mode (DEN2 = 1). In PE mode, odd parity is always used.																							
02-00	SS2-0 Slave select Read/write	Specifies the unit number of the transport to be used. Drive clear or INIT does not affect SS2-0.																							

REGISTER SUMMARY

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		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MTCSI	772440	SC	TRE	MCPE	O	DVA	PSEL	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO
MTWC	772442	WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 09	WC 08	WC 07	WC 06	WC 05	WC 04	WC 03	WC 02	WC 01	WC 00
MTBA	772444	BA 15	BA 14	BA 13	BA 12	BA 11	BA 10	BA 09	BA 08	BA 07	BA 06	BA 05	BA 04	BA 03	BA 02	BA 01	BA 00
MTFC	772446	FC 15	FC 14	FC 13	FC 12	FC 11	FC 10	FC 09	FC 08	FC 07	FC 06	FC 05	FC 04	FC 03	FC 02	FC 01	FC 00
MTCS2	772450	DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0
MTDS	772452	ATA	ERR	PIP	MOL	WRL	EOT	Ø	DPR	DRY	SSC	PES	SDWN	IOB	TM	BOT	SLA
MTER	772454	COR/ CRC	UNS	OPI	DTE	NEF	CS/ ITM	FCE	NSG	PEF/ LRC	INC/ VPE	DPAR	FMT	CPAR	RMR	ILR	ILF

MTAS	772456	0	0	0	0	0	0	0	0	ATA 07	ATA 06	ATA 05	ATA 04	ATA 03	ATA 02	ATA 01	ATA 00	
MTCK	772460	0	0	0	0	0	0	0	0	CRC6 /DTP	CRC7 /DT7	CRC6 /DT6	CRC5 /DT5	CRC4 /DT4	CRC3 /DT3	CRC2 /DT2	CRC1 /DT1	CRC0 /DT0
MTDB	772462	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 09	DB 08	DB 07	DB 06	DB 05	DB 04	DB 03	DB 02	DB 01	DB 00	
MTMR	772464	MDF 08	MDF 07	MDF 06	MDF 05	MDF 04	MDF 03	MDF 02	MDF 01	MDF 00	200 BPI CLK	MC	MOP 03	MOP 02	MOP 01	MOP 00	MM	
MTDT	772466	NSA	TAP	MOH	7CH	DR0	SPR	0	DT 08	DT 07	DT 06	DT 05	DT 04	DT 03	DT 02	DT 01	DT 00	
MTSN	772470	SN 15	SN 14	SN 13	SN 12	SN 11	SN 10	SN 09	SN 08	SN 07	SN 06	SN 05	SN 04	SN 03	SN 02	SN 01	SN 00	
MTTC	772472	ACCL	TCW	FCS	EAO DTE	0	DEN 02	DEN 01	DEN 00	FMT SEL 03	FMT SEL 02	FMT SEL 01	FMT SEL 00	EV PAR	SS 2	SS 1	SS 0	

SPECIFICATIONS FOR TAPE AND CONTROL

Main Specifications

Storage medium: 1/2-inch wide magnetic tape (industry std)
Capacity/tape reel: 32 million characters (at 1600 bpi)
Data transfer speed: 72,000 characters/sec., max.
Drives/control: 8, max.

Data Organization

Number of tracks: 9
Recording density: 800 or 1600 bits/inch, program selectable
Interrecord gap: 0.50 inches, min.
0.60 inches, nom.
Recording method: NRZI for 800 bpi
phase encoded for 1600 bpi

Tape Motion

Read/write speed: 45 inches/sec.
Rewind speed: 150 inches/sec.
Rewind time: 3 minutes, typical

Tape Characteristics

Length: 2,400 feet, max.
Type: Mylar base, iron-oxide coated
Reel diameter: 10 1/2 inches, max.
Handling: direct-drive reel motors, servo-controlled single capstan, vacuum tape buffer columns with constant tape winding tension

Mechanical

Mounting: Tape drive and master tape electronics mount in a standard PDP-11 cabinet (supplied)
Control unit is a 2 system units (mounts in a separate assembly)
Size: 31-inch front panel height for drive and master electronics.
Weight: 500 lbs. (including cabinet)
Cable length: 80 feet max., for total tape system (control unit to furthest drive)

Power

Tape drive current: 8A at 115 VAC
Surge current: 85A at 115 VAC
Current for control: 16A at +5V
0.6A at -15V
Heat dissipation: 900W

TJU16 TU16

Environment

Operating temperature: 15°C to 32°C
Relative humidity: 20% to 80%, max. wet bulb 25°C

Miscellaneous

BOT, EOT detection: Photoelectric sensing of reflective strip, industry compatible
Skew control: Deskewing electronics included in tape transport to eliminate static skew
Write protection: Write-protect ring sensing on tape transport
Data checking: Read-after-write parity checking of characters; Longitudinal Parity Check, and Cyclic Redundancy Check at 800 bpi
Testing: Off-line exerciser included in tape drive electronics; on-line check of control data paths accomplished by diagnostics
Reading: Data can be read in forward or reverse direction
Error correction: (phase-encoding only), On-the-fly error correction for a single-track dropout
Magnetic head: Dual-gap, read-after-write

Models

TJU16-EA: Tape transport and control, 1600/800 bpi, 115 VAC, 60 Hz
TJU16-ED: Tape transport and control, 1600/800 bpi, 230 VAC, 50 Hz
TJU16-EK: Tape transport and control, 800 bpi, 115 VAC, 60 Hz
TJU16-EN: Tape transport and control, 800 bpi, 230 VAC, 50 Hz

SPECIFICATIONS FOR TAPE DRIVE (TU16)

Mechanical

Mounting: Mounts in a standard PDP-11 cabinet (supplied)
Size: 26-inch front panel height

Prerequisite: TJU16

Models

TU16-EE: Tape transport, 115 VAC, 60 Hz
TU16-EJ: Tape transport, 230 VAC, 50 Hz

**TM11
TU10**

MAGNETIC TAPE, TM11

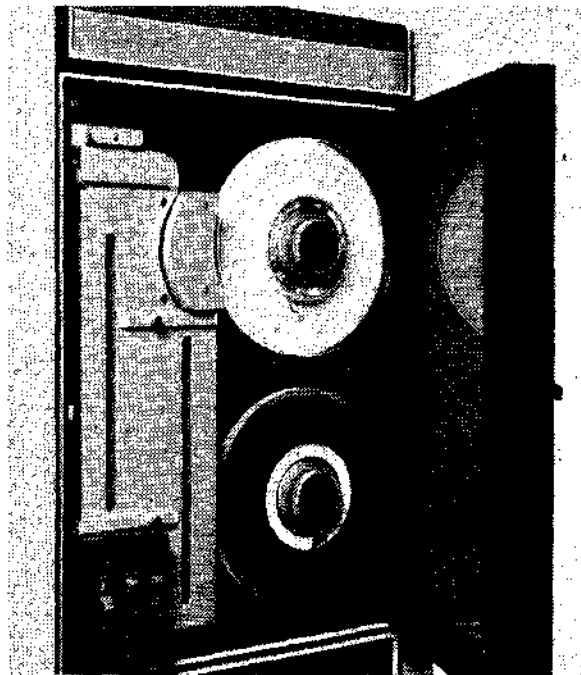
DESCRIPTION

The TM11 is a high-performance, low-cost magnetic tape system ideally suited for writing, reading, and storing large volumes of data and programs in a serial manner. Because the system reads and writes in industry-compatible format, information can be transferred between a PDP-11 and other computers. For example, a PDP-11 might be used to collect data and record it for later processing on a large-scale computer. The 10 1/2-inch tape reels contain up to 2400 feet of tape upon which over 180 million bits of data can be stored on high density 9-track tape or over 140 million bits can be stored on high density 7-track tape.

The TM11 employs read after write error checking to verify that proper data is written on the tape. Should a tape dropout be detected, appropriate action can be taken to insure no loss of data.

Tape motion is controlled by vacuum columns and a servo-controlled single-capstan. Long tape life is possible because the only contact with the oxide surface is at the magnetic head and at a rolling contact on one low-friction, low-inertia bearing.

A Magtape System consists of up to 8 tape transports and a Control Unit. Transports are capable of operation with seven or nine-track tape and a system can contain any combination of 7- and 9-track units. A TM11 includes a control unit and the first Tape Transport.



TU10 MAGTAPE UNIT

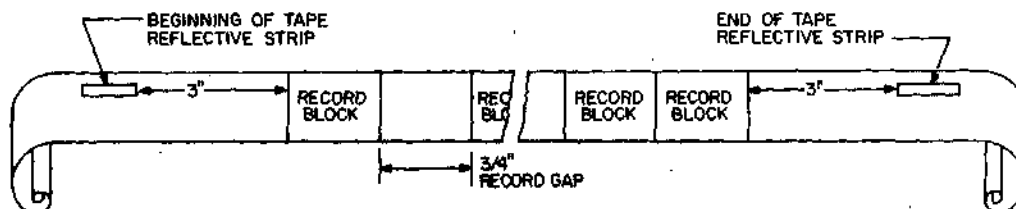
4-501

Operation

Reading and writing occurs when the tape is moving forward, but the control can move the tape to new positions in forward or reverse. For writing on tape, 8-bit data words are transferred from memory to a data buffer in the controller. The data buffer logic supplies the character to the tape transport write logic. For reading, the sequence is reversed; and information is read from tape as 6-bit characters for 7 track tape; (8 bits for 9 track tape) which are sent to the data buffer. When a word has been assembled in the data buffer, an NPR transfer is initiated to transfer the data buffer word into memory.

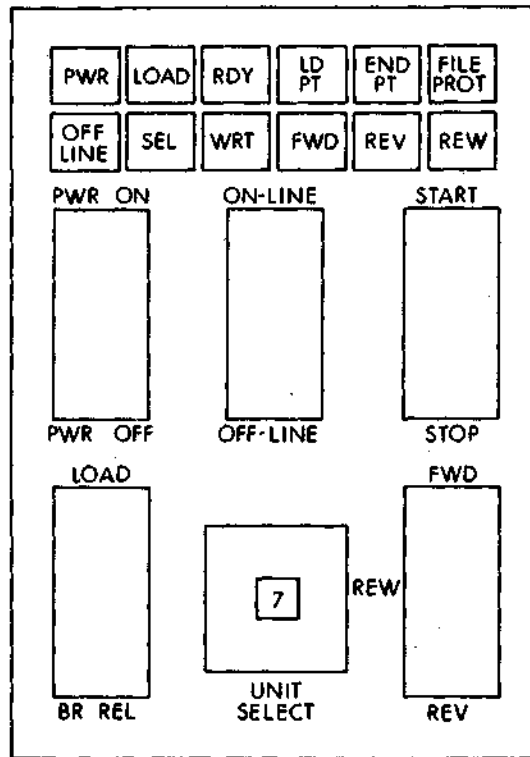
The 7- and 9-track system use 1/2-inch mylar base tape which is coated on one side with an iron oxide composition. The method of recording is non-return-to-zero (NRZ). A seven track tape includes six data channels and a lateral parity channel. Density modes of 200, 556, and 800 bytes per inch are selectable. Nine-track tape is similar to the 7-track tape, but operation is only in the 800 bpi mode and it has the industry standard cyclic redundancy character at the end of each record. The load and end points of the tape are marked by reflective strips which are detected by photo diodes. About 10 inches of blank tape is wound on a reel and precedes the BOT and EOT strips; a gap of about 3 inches is left from the load point before writing can begin.

Each computer word contains two 8-bit tape characters. Record blocks are separated by $\frac{3}{4}$ inch gaps on 7-track units and $\frac{1}{2}$ inch gaps on 9-track units. The industry standard format has 7-track tape records containing from 24 to 4008 characters, and 9-track tape records from 18 to 2048 characters.



Magtape Format

CONTROLS & INDICATORS



Operator Control Box

Control Box Switches

-
- PWR ON/PWR OFF** Applies power to entire TU10. Also, supplies power to the bus terminators if the tape transport is the most remote unit on the bus.

 - LOAD/BR REL**
 - LOAD Position** Enables vacuum motor, which draws tape into the buffer columns.
 - Center Position** Disables vacuum motor; brakes are full-on.
 - BR/REL** Release brakes.

 - ON-LINE/OFF-LINE**
 - ON-LINE Position** Selects remote operation.
 - OFF-LINE Position** Selects local operation.

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FWD/REW/REV

FWD Position	Selects, but does not initiate, forward tape motion when transport is off-line
REW Position	Selects, but does not initiate, tape rewind when transport is off-line.
REV Position	Selects, but does not initiate, reverse tape motion when transport is off-line.

START/STOP

START Position	Initiates tape motion selected by FWD/REW/REV switch when transport is off-line.
STOP Position	Clears any motion commands when transport is off-line.

UNIT SELECT

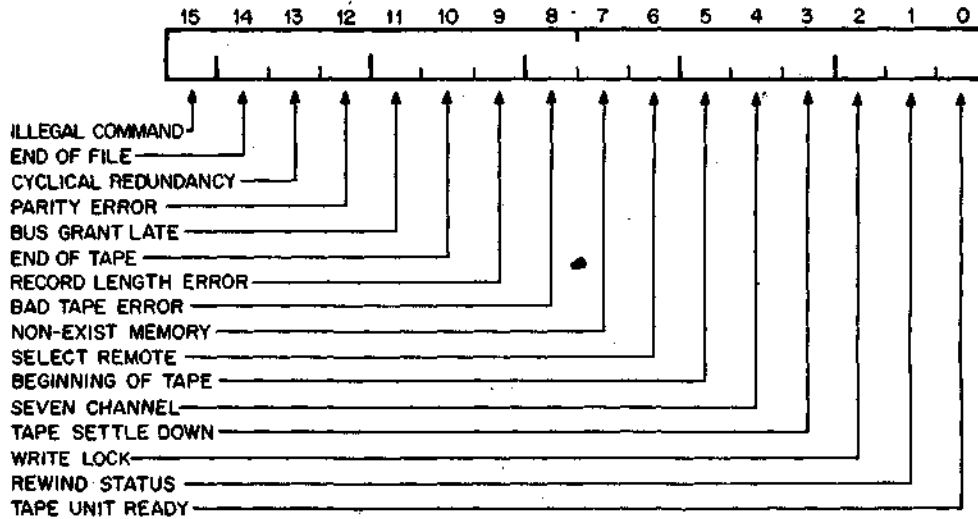
Selects the tape transport unit by number (0-7). This number is used in the program to address the tape transport.

Status Indicators

PWR	Indicates power has been applied to the transport.
LOAD	Indicates that vacuum is on and the tape is loaded into the buffer columns.
RDY	Indicates that the tape transport is ready (vacuum on and settledown delay complete); there is no tape motion.
LD PT	Indicates that the tape is at load point (Beginning of Tape)
END PT	Indicates that the tape is at end point (End of Tape).
FILE PROT	Indicates that write operations are inhibited because the write enable ring is not mounted on the file reel.
OFF-LINE	Indicates local operation by the control box.
SEL	Indicates the tape transport is selected by the controller (program).
WRT	Indicates that the program has initiated a write operation in the tape transport.
FWD	Indicates that a forward command has been issued.
REV	Indicates that a reverse command has been issued.
REW	Indicates that a rewind command has been issued.

REGISTERS

Status Register (MTS) 772 520



BIT	NAME	FUNCTION
15	Illegal Command	Set by any of the following illegal commands: 1. Any DATO or DATOB to the Command Register MTC during the tape operation period 2. A Write, write EOF, or write with extended IRG operation when the FILE PROTECT bit is a 1 3. A command to a tape unit whose SELECT REMOTE bit is a 0 4. The SELECT REMOTE (SELR) bit becoming a 0 during an operation.
14	End of file (EOF)	Set when an EOF character is detected during a read, space forward or space reverse operation. During the read or space forward operation, the EOF bit is set when the LPC (longitudinal parity check) character following the EOF character is read. During a space reverse operation, the EOF bit is set when the EOF character following its LPC character is read. The ERR bit

In error conditions 1 through 3, the command is loaded into the MTC, but the GO pulse to the tape unit is not generated. In addition the CU ready bit remains set.

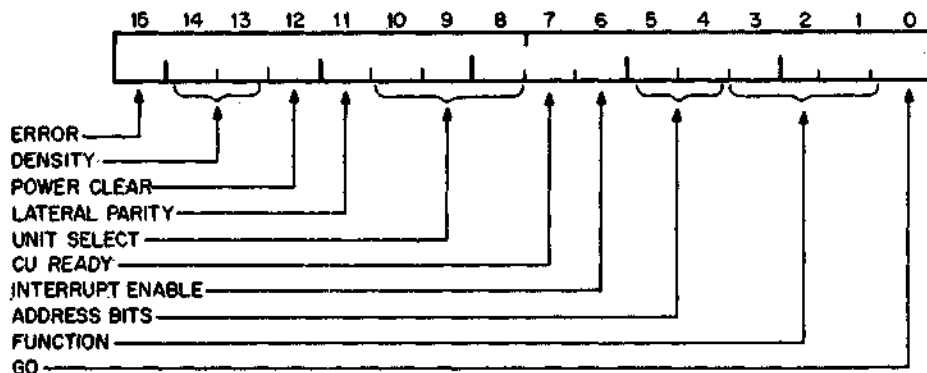
TM11

- sets when the LPC character strobe is generated with the FILE MARK signal upon EOF detection.
- 13 Cyclical Redundancy Error (CRE) Detected only during a read operation. It compares the CRC character read from tape with that regenerated during the same read operation. If they are not the same, CRC ERROR from the tape unit becomes a 1 which forces the CRE bit to a 1. However, the ERR bit does not become a 1 until the LPC character is detected.
- 12 Parity Error (PAE) The OR of the lateral and longitudinal parity errors. A lateral parity error is indicated on any character in the record while a longitudinal parity error occurs only when the LPC character is detected.
- A parity error does not affect the transfer of data; that is, in a write operation, the entire record is transferred to tape and in a read operation, the entire record is written into core memory.
- For all parity errors, the ERR bit sets only when the LPC character is detected. Both lateral and longitudinal parity errors are detected during a read, write, write EOF, and write with extended IRG operations. The entire record is checked including the CRC and LPC characters. Longitudinal parity error occurs when an odd number of 1's is detected on any track in the record. A lateral parity error occurs when an even number of 1's is detected on any character when PEVN is a 0, or an odd number of 1's is detected on any character when PEVN is a 1.
- 11 Bus Grant Late (BGL) Set when the control unit, after issuing a request for the bus, does not receive a bus grant before the control unit receives the bus request for the following tape character. The condition is tested only for NPR (non-processor request) operations. The ERR bit sets

TM11

- | | | |
|---|-------------------------|--|
| 6 | Select Remote (SELR) | Cleared when the tape unit addressed does not exist, is off line, or has its power turned off. |
| 5 | Beginning Of Tape (BOT) | Set when the BOT marker is read, and cleared when the BOT marker is not read. BOT at a 1 does not produce a 1 in the ERR bit. |
| 4 | Seven Channel (7 CH) | Set to indicate a 7-channel tape unit; cleared to indicate a 9-channel unit. |
| 3 | Tape Settle Down (SDWN) | Set whenever the tape unit is slowing down. The master will accept and execute any new command during the SDWN period except if the new command is to the same tape unit as the one issuing SDWN and if the direction implied in the new command is opposite to the present direction. |
| 2 | Write Lock (WRL) | Set to prevent the control unit from writing information on tape. Controlled by presence or absence of the write protect ring on the tape reel. |
| 1 | Rewind Status (RWS) | Set by the master as soon as it receives a rewind command from the control unit. Cleared by the master as soon as the tape arrives at the BOT marker in the forward direction. (It overshoots BOT in the reverse direction.) |
| 0 | Tape Unit Ready (TUR) | Set when the selected tape unit is stopped and when the SELECT REMOTE is false. Cleared when the processor sets the GO bit and the operation defined by the function bit occurs. |

Command Register (MTC) 772 522



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BIT	NAME	FUNCTION																				
15	Error (ERR)	Set as a function of bits 7-15 of the Status Register MTS. Cleared on INIT or on the GO command to the tape unit.																				
14-13	Density (DEN 8, DEN 5)	Cleared on INIT. <table><thead><tr><th>BIT 14</th><th>BIT 13</th><th></th><th></th></tr></thead><tbody><tr><td>0</td><td>0</td><td>200 bpi</td><td>7 channel</td></tr><tr><td>0</td><td>1</td><td>556 bpi</td><td>7 channel</td></tr><tr><td>1</td><td>0</td><td>800 bpi</td><td>7 channel</td></tr><tr><td>1</td><td>1</td><td>800 bpi</td><td>9 channel</td></tr></tbody></table>	BIT 14	BIT 13			0	0	200 bpi	7 channel	0	1	556 bpi	7 channel	1	0	800 bpi	7 channel	1	1	800 bpi	9 channel
BIT 14	BIT 13																					
0	0	200 bpi	7 channel																			
0	1	556 bpi	7 channel																			
1	0	800 bpi	7 channel																			
1	1	800 bpi	9 channel																			
12	Power Clear (PCLR)	Provides the means for the processor to clear the control unit and tape units without clearing any other device in the system. The PCLR bit is always read back by the processor as 0.																				
11	Lateral Parity (PEVN)	Set for even parity. Cleared for odd parity. A search for parity error is made in all tape moving operations except space forward, space reverse, and rewind.																				
10-8	Unit Select	Specifies one of the eight possible magnetic tape units. All operations defined in the MTC and all status conditions defined in the MTS pertain to the unit indicated by these bits. Cleared on INIT.																				
7	CU Ready (CUR)	Cleared at start of a tape operation, and set at end of tape operation. The control unit accepts as legal all commands it receives while the CU Ready bit is 1.																				
6	Interrupt Enable (INT ENB)	When set, an interrupt occurs whenever either the CU ready bit or the ERR bit change from 0 to 1 or whenever a tape unit that was set into rewind has arrived at the beginning of tape. In addition, an interrupt occurs on an instruction that changes the INT ENB from 0 to 1 and does not set the GO bit. (i.e. CU READY or ERROR = 1)																				
5-4	Address Bits	Extended memory bits for an 18-bit bus address. Bit 5 corresponds to XBA17, and bit 4 to XBA16. They are																				

an extension of the MTCMA, and increment during a tape operation if there is a carry out of MTCMA.

3-1 Function Bits

Selects 1 of 8 functions (programmable commands).

BIT 3	BIT 2	BIT 1	
0	0	0	Off line
0	0	1	Read
0	1	0	Write
0	1	1	Write EOF
1	0	0	Space Forward
1	0	1	Space Reverse
1	1	0	Write with Extended Interrecord Gap
1	1	1	Rewind

0 Go

When set, begins the operation defined by the function bits.

Byte Record Counter (MTBRC) 772 524

The MTBRC is a 16-bit binary counter which is used to count bytes in a read, write, or write with extended IRG operation, or records in a space forward or space reverse operation. When used in a write or write with extended IRG operation, the MTBRC is initially set by the program to the 2's complement of the number of bytes to be written on tape. The MTBRC becomes 0 after the last byte of the record has been read from memory. Thus, when the next WDS (Write Data Strobe) signal occurs from the master, the control unit will not send the WDR (Write Data Request) to the master indicating that there are no more data characters in the record.

When the MTBRC is used in a read operation, it is set to a number equal or greater than the 2's complement of the number of words to be loaded into memory. A record length error (RLE) occurs for long records only, and is indicated when a read pulse for data (RDS occurring when CRCS or LPCS does not occur) occurs when the MTBRC is 0. The MTBRC increments by 1 immediately after each memory access.

When the MTBRC is used in a space forward or space reverse operation, it is set to the 2's complement of the number of records to be spaced. It is incremented by a 1 at LPC time, whether the tape is moving in the forward or reverse direction. A new GO pulse is sent to the tape unit during the SDWN time if the MTBRC is not 0 during that time. When the tape unit is moving in reverse, the LPC character is detected before SDWN, but before the entire record has been traversed. Thus, both SDWN and LPC character appear to be in different positions on tape from those when the tape unit is moving forward.

Current Memory Address Register (MTCMA) 772 526

The MTCMA contains 16 of the possible 18 memory address bits. It is

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used in NPR operations to provide the memory address for data transfers in read, write, and write with extended IRG operations. Prior to issuing a command, the MTCMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write, or write extended IRG operation. The MTCMA is incremented by 1 immediately after each memory access. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address plus 1 of the last character in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the MTCMA contains the address of the location in which the failure occurred.

The MTCMA is available to the processor on a DATI except bit 0 which always reads as a zero under program control. Bit 0 can be asserted during NPR's to determine the selected byte. The bits are set or cleared on a processor DATO. INIT clears all bits in the MTCMA.

Data Buffer (MTD) 772 530

The data buffer is an 8-bit register which is used during a read, write, or write with extended IRG operation. In a read operation, the data buffer is a temporary storage register for characters read from tape before being stored into memory. In a processor read, all nine bits are stored into memory. Bits 0 through 7 in memory correspond to channels 7 through 0 respectively from tape, and bit 8 corresponds to the parity bit. In an NPR operation only the data bits are read into memory, and are alternately stored into the low and high bytes. In a write or write with extended IRG operation, the data buffer is a temporary storage register for characters read from core memory before they are written on tape. The polarity of the parity bit is determined by the PEVN bit in the MTC.

In a read operation, the LPC character enters the data buffer when bit 14 of MTRD is a 1, and inhibited from doing so when bit 14 is a 0. Thus, after reading a nine-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the CRC character when bit 14 is a 0. After reading a seven-channel tape, the data buffer contains the LPC character when bit 14 is a 1 and the last data character when bit 14 is a 0. After reading an EOF character, the data buffer contains all 0's when bit 14 is a 1 and the LPC character when bit 14 is a 0. The MTD is available to the processor on a DATI. Bits 9 through 15 are read identically to bits 1 through 7 respectively. Bits 0 through 7 are set or cleared on a processor DATO. Bits 8 thru 15 are not affected by a processor DATO. INIT clears all bits in the MTD.

TU10 Read Lines (MTRD) 772 532

The memory locations allocated for the TU10 read lines are:

Bits 0-7 for the channels 7-0 respectively.

Bit 8 for the parity bit.

Bit 12 for the gap shutdown bit.

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Bit 13 for the BTE error generation.

Bit 14 for the CRC, LPC character selector.

Bit 15 for the timer.

For correct longitudinal parity, bits 0-8 are 0 after writing a record or reading a record from tape. For a longitudinal parity error, one or more of the bits 0-8 remains at a 1, the bit(s) at a 1 indicating the channel(s) containing the error which sets the CU ready bit. Thus, if the pulse is set during a tape operation, CU ready sets prematurely thus producing the gap shutdown period when characters are still being read. Bits 0-8 are set and cleared by the tape unit. Bit 13 is a pulse generated by the processor. Bit 14 is set and cleared by the processor and cleared by INIT. Bit 15 is uniquely controlled by the 100 microsecond timer. The MTRD is available to the processor on a DATI except that bit 13 reads back as a 0.

Timer

TIMER is a 10 KHz signal with a 50% duty cycle. The signal is used for diagnostic purposes in measuring the time duration of the tape operations. The timer is read as bit 15 in the MTRD.

SPECIFICATIONS FOR TM11

Main Specifications

Storage medium:	1/2" wide magnetic tape (industry compatible)
Capacity/tape reel:	5 to 20 million characters
Data transfer speed:	36,000 char/sec
Drives/control, max:	8

Data Organization

Number of tracks:	7 or 9
Recording density, 7 track:	200, 556, or 800 bits/inch; program selectable
9 track:	800 bits/inch
Interrecord gap, 7 track:	0.75 inches, min.
9 track:	0.50 inches, min.
Recording method:	NRZI

Tape Motion

Read/write speed:	45 inches/sec
Rewind speed:	150 inches/sec
Rewind time:	3 minutes, typ

Tape Characteristics

Length:	2,400 ft.
Type:	Mylar base, iron-oxide coated
Reel diameter:	10 1/2 inches
Handling:	direct-drive reel motors, servo-controlled single capstan, vacuum tape buffer changers with constant tape winding tension.

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Register Addresses

Status	(MTS)	772 520
Command	(MTC)	772 522
Byte Record Counter	(MTBRC)	772 524
Current Mem Address	(MTCMA)	772 526
Data Buffer	(MTD)	772 530
TU10 Read Lines	(MTRD)	772 532

UNIBUS Interface

Interrupt vector address:	224
Priority level:	BR5
Data transfer:	NPR
Bus loading:	1 bus load

Mechanical

Mounting:	mounts in a std PDP-11 cabinet (supplied)
Size:	26" panel height for tape drive + 10 $\frac{1}{2}$ " for control unit
Weight (incl. cab):	500 lbs.

Power

Input current:	9 A at 115 VAC
Heat dissipation:	1000 W

Environmental

Operating temperature:	15°C to 32°C
Relative humidity:	20% to 80%

Miscellaneous

BOT, EOT Detection:	Photoelectric sensing of reflective strip, industry compatible
Skew Control:	Deskewing electronics included in tape transport to eliminate static skew
Write Protection:	Write protect ring sensing on tape transport
Data Checking Features:	Read after write parity checking of characters; Longitudinal Redundancy Check (7- and 9-channel); Cyclic Redundancy Check (9-channel)
Extended Features:	Self-test of Control with tape transport offline; core dump for 7-channel units.
Magnetic Head:	Dual gap, read after write.

Models

TM11-EA:	Tape transport and control, 9 track, 115 VAC, 60 Hz
TM11-ED:	" 9 track, 230 VAC, 50 Hz
TM11-FA:	" 7 track, 115 VAC, 60 Hz
TM11-FD:	" 7 track, 230 VAC, 50 Hz

SPECIFICATIONS FOR TU10

Mechanical

Mounting:	mounts in a std PDP-11 cabinet (supplied)
Size:	26" front panel height
Weight (incl. cab):	450 lbs.

TM11

Power

Input current: 9 A at 115 VAC
Heat dissipation: 1000 W

Prerequisite: TM11

Models

TU10-EE: Tape transport, 9 track, 115 VAC, 60 Hz
TU10-EJ: " 9 track, 230 VAC, 50 Hz
TU10-FE: " 7 track, 115 VAC, 60 Hz
TU10-FJ: " 7 track, 230 VAC, 50 Hz

MAGNETIC TAPE, TS03**FEATURES AND BENEFITS**

The TS03 is a low-cost, 9-track magnetic tape system that uses industry-standard 800-bpi NRZI recording format. The basic system consists of a master tape drive, controller and power supply. A second tape drive can be added at the cost of the tape drive only, because the second (slave) drive uses the master drive's controller and power supply.

The major features of the TS03 are high reliability, low cost, small size, and low power consumption. The major benefit is that, despite its low cost, the TS03 does not sacrifice reliability. It uses the same techniques to record data in the same manner as larger, more expensive transports, but it does this with a slower, extremely simple mechanism.

Cost savings result from small size because the TS03 frequently fits into existing cabinets. The TS03 with controller can fit into a processor cabinet with spare room left over for another subsystem.

Small size also means lower power consumption because:

- There is no vacuum motor.
- The TS03 uses very low standby power—about the same as a medium-sized light bulb.
- It takes less power to drive the TS03's seven-inch diameter reels.
- Lower power consumption means a smaller load if back-up generator or batteries are used.
- Heat dissipation is so low that no cooling fans are needed.

Reliability

The TS03 is designed to read and write data to industry standards with high reliability. The calculated MTBF (Mean Time Between Failures) is 5,080 hours for the tape drive.

A unique feature of the TS03 eliminates the writing of hard errors on tape. If an error is detected in the read-after-write check, programming can cause the entire record to be rewritten. Hardware within the TS03 automatically senses that this is a retry and the read-checking margins are tightened up to ensure distinguishing between a transient error and a bad tape area. If the data passes on a second (or subsequent) try the written data is guaranteed to exceed the read thresholds. If there was a bad section of tape, the faulty record can be erased, then recorded correctly further down the tape.

DESCRIPTION

The TS03 is a 9-track, 800 bpi magnetic tape drive. Each tape drive is a self-contained unit including read and write electronics, low inertia friction capstan and two linear-drive reel servos. The reel servos use mechanical servo arms for controlling the tape storage loops. Magnetic arm transducers are employed to sense the arm position and control

TS03

tape tension. The linear servos provide gentle tape handling to prolong tape life.

The recording head assembly includes an open-loop tape path with single edge guiding, tape cleaner, EOT/BOT station and a 9-track read-after-write head. The recorder has a transparent plastic door enclosing the tape path and recording area to allow viewing while still excluding airborne dust.

The 7-inch diameter tape reel is mounted on a quick-release tape hub. A fixed take-up hub is provided and does not require a separate tape reel.

The master drive is mounted on slides and occupies 10½-inches of panel height in a standard DIGITAL cabinet.

The master drive includes portions of controller circuitry (adapted on a printed circuit board) mounted beneath the drive mechanism enclosure. The board is hinged to facilitate access for servicing and maintenance.

Master Controller Functions

The TS03 Master Controller performs the following tasks:

- **Tape Format**

A Cyclic Redundancy Check character is generated on write data passing to the TS03 and is strobed onto tape. This CRC character is generated in accordance with ANSI standard for 800-bpi NRZI recording. Data is also checked for errors while reading the tape.

A Longitudinal Redundancy Check character is also written onto the tape.

An industry-compatible tape mark is generated when a Write Tape Mark instruction (also known as Write EOF or Write File Mark) command is in progress.

- **Record Detection**

Once tape motion has been initiated on a tape transport, motion will not be halted until either a valid record is detected or the INITIALIZE signal is given.

- **Data Checking**

A vertical parity bit is attached to each data character written. Whenever the TS03 is moving tape read/write speed, it checks data for correct vertical parity and a correct Longitudinal Redundancy Check character for each record read.

The TS03 also contains logic for detecting industry-compatible tape marks (END-OF-FILE mark).

Operation

All operation is controlled and monitored through four switches and associated indicators on the front panel:

POWER
ON-LINE

**LOAD
REWIND**

An additional indicator, **WRITE ENABLE**, shows the operator whether the tape is write-protected or not. Each of the indicators uses solid-state illuminators (as opposed to light bulbs). The advantage of the solid-state indicators is that they will last indefinitely while standard bulbs burn out from time to time.

There is extensive software available for operating the TS03. The software is compatible with the TU10 Tape Drive.

REGISTERS

The TS03 Register descriptions are the same as for the TU10 Tape Drive. Refer to the TU10 section for this information.

SPECIFICATIONS FOR TS03 DRIVE**Main Specifications**

Storage medium:	1/2-inch wide magnetic tape (industry compatible)
Capacity/tape reel:	5 million characters
Data transfer speed:	10,000 char/sec
Drives/control, max:	2

Data Organization

Number of tracks:	9
Recording density:	800 bits/inch
Inter-record gap:	0.5 inches, min.
Recording method:	NRZI

Tape Motion

Read/write speed:	12 1/2-inches/sec
Rewind time:	1 minute, max.
Tape drive:	single capstan
Reel braking:	dynamic servo control
Speed variation:	3% instantaneous; 1% long term
Start/stop distance:	0.19 inch
Start/stop time:	30 msec

Tape Characteristics

Length:	600 ft
Type:	Mylar base, iron-oxide coated
Reel diameter:	7 inches

Mechanical

Mounting:	mounts on slides in a std 19-inch cabinet
Size:	10 1/2-inch front panel height
Weight:	37 lbs

Power

Input current:	1A at 90 to 132 Vac, or 0.5A at 180 to 240 Vac
Heat dissipation:	100 W

TS03

Environmental

Operating temperature: 15°C to 32°C
Relative humidity: 20% to 80%, with max wet bulb
25°C and min dew point 2°C
Altitude: 10,000 feet

Miscellaneous

BOT, EOT detection: photoelectric sensing of reflective strip, industry compatible
Magnetic head: dual gap, read after write, 0.15-inch gap

Models

TS03-SA: tape drive, 115 Vac, 60 Hz
TS03-SB: tape drive, 230 Vac, 50 Hz

SPECIFICATIONS FOR CONTROL

(similar to the TU10 control)

Registers Addresses

Status	772 520
Command	772 522
Byte Record Counter	772 524
Current Memory Address	772 526
Data Buffer	772 530
Read Lines	772 532

UNIBUS Interface

Interrupt vector address: 224
Priority level: BR5
Data transfer: NPR
Bus loading: 1 bus load

Mounting: 1 System Unit (SU)

Power: 5 A at + 5 V

UDC11

UNIVERSAL DIGITAL CONTROL SUBSYSTEM, UDC11

DESCRIPTION

The UDC11 is a unique, highly flexible digital information input/output option for industrial and process control applications that use the PDP-11 computers.

The UDC11 interrogates or drives up to 252 directly addressable digital sense and control functional I/O modules or up to 4032 individual digital points. I/O functions include relay output, contact sense/interrupt counters, D/A converters, etc.

Automatic hardware logic within the UDC11 rapidly identifies interrupting inputs according to input module type and address, typically within 5 μ sec.

The subsystem has been designed to take full advantage of the PDP-11 processor including the UNIBUS, and permits data to be read or loaded with a single move instruction.

Modular design and industrial packaging, including provisions for two wire, screw terminal input connectors, permit the UDC11 to be configured and modified according to application needs. The UDC11 is normally supplied as part of an IDACS-11 system; however it may be easily field added to existing PDP-11 systems.

Operation

The UDC11 operates under computer program control as a high level digital multiplexer, interrogating digital inputs and driving digital outputs located on directly addressable functional modules.

Sixteen bit data words are transferred directly between a functional module and a preassigned address location in the PDP-11 core memory by a single MOVE instruction when reading data in, or conversely from core to a module when sending data out.

Depending upon the module type selected, a 16-bit data output word can represent the single 16-bit digital word required by a D/A converter or 16 individual parts for contact closures, pulse outputs, etc.

Signal Conditioning and Functional I/O Modules

Each UDC11 system is tailored to meet a specific application by modularly assembling the appropriate modules.

Functional Input/Output Modules include Contact Interrupt, Contact Sense, Single Shot Driver, Flip-Flop Driver, Latching Relay, Single Shot Relay, Flip-Flop Relay, D/A Converters, and I/O Converters. Each of these modules plug interchangeably into the DD02 File Units which serve as universal interface units. The logical address of each unit can be determined by simple jumper wire connections, so that addresses are completely independent of the unit's physical location. Thus hardware additions or system program changes do not require the rewiring of input terminals.

Each Functional I/O Module requires a Signal Conditioning Module to normalize input voltages, provide fusing, and distribute field-supplied excitation and control power to the Functional I/O Modules.

Signal Conditioning Modules

- a. **Isolated Power BW400**—Provides the interface between individual points on the functional I/O modules and field signals. Differential pair field wiring is terminated on screw terminals, one pair for each of the 16 points on the functional module.
- b. **Common Power BW402**—Is similar to the BW400 except that a 17th input pair permits field supplied excitation or control power to be brought directly to the Signal Conditioning Module and distributed in parallel (common) to each of the 16 circuits on the module. The input is fused for 4 amperes. As with the BW400, the BW402 can supply signal conditioning and arc suppression, if required.
- c. **Output Driver Module BW403**—Is similar to the BW402 Common Power Module except that a common ground return is provided for the open collector devices of the Single Shot Driver and Flip-Flop Driver (used with BW685 and BW687 only).
- d. **Contact Sense BW731**—Provides electrically isolated, differential inputs for 16 external customer contacts or voltages. Isolation of up to 250 volts is achieved by a miniature read relay buffer on each input point. This module provides reliable and trouble free digital sensing in high noise environments. Also, its differential input characteristics are particularly suited for those applications where the ground of the customer's excitation voltage power supply may be different from (i.e., not directly strapped to) computer system ground.
- e. **Contact Interrupt BW733**—Provides 16 electrically isolated, differential inputs for external customer contacts or voltages. It is electrically and mechanically similar to the BW731 Contact Sense Module. The BW733 is used to economically and reliably interface asynchronous devices requiring fast service from the processor because of priority or short duration.

Functional I/O Modules

- a. **Flip Flop Driver BM685**—Provides 16 solid state buffered driver circuits for control of solenoid valves, relays, lamps, displays, etc. Capable of switching control voltages of up to + 55 VDC, the BM685 will switch up to 250 ma of field supplied power per point, when set by a logical "1." The driver includes diode protection for inductive loads.
- b. **Single Shot Relay BM807**—Provides 16 electrically isolated normally open mercury wetted contact outputs for initiating alarms, controls, and field relays. Normally closed operation can be achieved through a module jumper change performed in the field by the customer or at the factory on a special order basis. The duration of the output is trimpot adjustable from 2 msec to 2 seconds. A logical "1" energizes the relay coil for the pre-set pulse duration.

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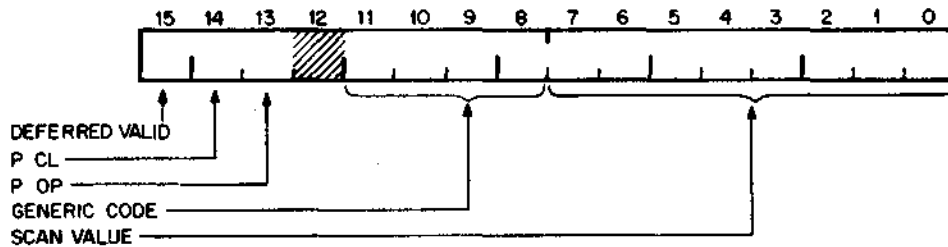
- c. **Single Shot Driver BM687**—Provides a solid state pulse output to activate up to 16 field circuits such as lights, buzzers, or external control relays. Capable of switching control voltages of up to + 55 VDC, the BM687 will switch up to 250 ma of field supplied power per point, when set by a logical "1." The driver also provides diode protection against inductive loads.
- d. **Latching Relay BM803**—Provides "fail-safe" operation of 16 electrically isolated mercury wetted relay outputs. Magnetically latched, the relays remain set in the event of power failure, insuring the continuity and integrity of field circuits. Change of state can be effected only by a logical "1" or "0." Relay contacts are open when the relay is set by a logical "0," and closed when set by a logical "1." Contacts are rated at 2 amps, 250 volts, the product not to exceed 100 va.
- e. **Flip-Flop Relay BM805**—Provides 16 electrically isolated normally open mercury wetted relay output contacts for buffered control of relays, contactors, displays, lamps, etc. Normally closed operation is possible by a module jumper change performed in the field by the customer or at the factory on a special order basis.
- f. **BW734 Counter Module**—Is a 16-bit asynchronous binary up counter. An output buffer register is included which is updated after each counter increment. When the buffer is read (under program control), the update is inhibited, preventing any data change. The counter is parallel loading, enabling it to be preset under program control. Count down is accomplished by presetting 2's complement. May be used for Input or Output counting functions, stepping motor control, etc.
- g. **BA633 Digital-to-Analog Converter**—Is interchangeable with any functional I/O module in the UDC11. It contains four complete channels of 10-bit digital-to-analog conversion. Single-ended output current or voltage is provided by one of the four signal conditioning modules listed below. Selection of a channel (1 of 4) and loading of data into the D/A buffer is accomplished by a single move instruction. The analog output remains constant until the channel is readdressed with new data. A separate H738A analog power supply is required for each group of up to four (16 channels) BA633. Power fail backup can be provided to maintain the analog output at its constant last value in the event of system or line power failure.
- h. **Digital-to-Analog Converter BA633 Signal Conditioning Modules**—A signal conditioning module is required for each BA633. Each module contains four channels of signal conditioning and scales the four analog outputs of the BA633 to the required current or voltage range.

BA233	0 to + 10v @ 15 ma
BA234	+ 1v to + 5v @ 15 ma
BA235	4 ma to 20 ma into 750 ohms
BA236	10 ma to 50 ma into 300 ohms

REGISTERS

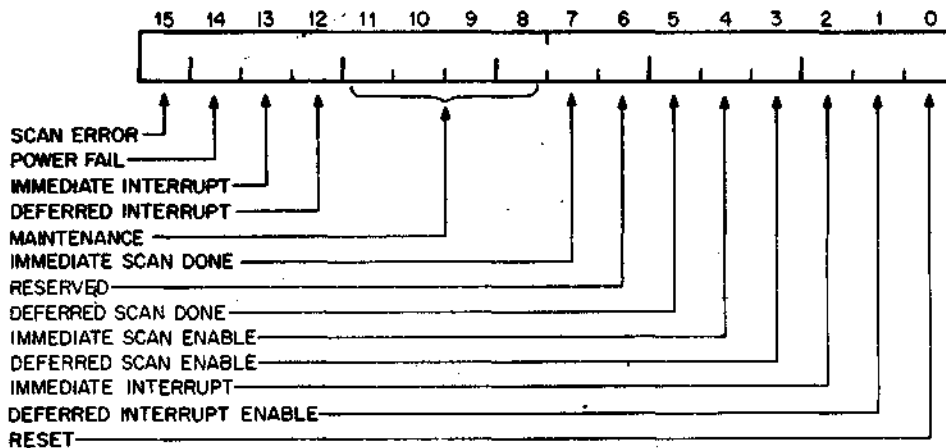
Scan Register (UDSR) 771 774

UDC11



BIT	NAME	FUNCTION
15	Deferred Valid	Set to indicate that a deferred scan done was displaced by an immediate scan.
14	P CL	Set to indicate interest in contact closures from interrupt module.
13	P OP	Same as P CL but for contact openings.
11-8	Gen 3, 2, 1, 0	Generic code of interrupt module.
7-0	Scan Value	Address of interrupt module found as result of scan.

Control And Status Register (UDSR) 771 776



BIT	NAME	FUNCTION
15	Scan Error	Set by scan overflow in x, y, or wd; reset by initialize. Read only.
14	Power Fail	Set by power fail from expander H721B power supply; reset by initialize. Read only.
13	Intermediate Interrupt (IM INT)	Set by interrupt class I/O module; reset when interrupt class I/O module is reset; immediate. Read only.

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12	Deferred Interrupt (DEF INT)	Same as IM INT but for deferred interrupt. Read only.
11	Maintenance Mode Word (M STP WD)	Maintenance mode of generating an interrupt module word address stop to test scanner. Read/Write.
10	Maintenance Mode Y (M STP Y)	Same as M STP WD but for Y address stop. Read/Write.
9	Maintenance Mode X (M STP X)	Same as M STP WD but for X address stop. Read/Write.
8	Maintenance Mode (M MODE)	Maintenance mode bit when set enables bit 02 to cause an IM INT or Bit 01 a DEF INT. Read/Write.
7	Immed. Scan Done	Set by an end of scan and IM INT; reset by initialize, clear done, or RIF. Read only.
5	Deferred Scan Done	Set by an end of scan and DEF INT; reset by initialize, clear done, or RIF.
4	Immed. Scan Enable (IM SCAN)	Set to enable immediate scan. Read/Write.
3	Deferred Scan Enable (DEF SCAN ENABLE)	Set to enable deferred scan. Read/Write.
2	Immediate Interrupt (IM INT)	Set to enable immediate interrupt; reset-set transition generates clear done signal. Read/Write.
1	Deferred Interrupt Enable (DEF INT ENABLE)	Set to enable deferred interrupt; reset-set transition generates clear done signal. Read/Write.
0	Reset (RIF)	Reset-set transition generates clear done and resets interrupting module; reset by initialize or delayed clear done. Read/Write.

NOTE: Initialize Resets All Bits.

Two types of service requests exist for interrupt producing functional I/O modules. These are "immediate" and "deferred."

The type of request serviced by the UDC11 is governed by program selection. If both requests are enabled the UDC11 will always service the immediate requests before servicing deferred requests.

Upon receipt of a service request by a functional module, the UDC11 controller determines the type of request and automatically initiates a scan to determine the address of the interrupt. Since the search is com-

UDC11

pletely asynchronous and software overhead to test the controller with each data transfer prohibitive, programmed data transfer will take precedence over the hardware search.

Upon locating the address of the I/O module requesting service a hard-wired four bit generic code is transferred to the scan register.

When the address and generic code are located the PDP-11 is interrupted on level BR6 if immediate service is required, or BR4 if deferred service is required. In either case the address and code may be read to the pre-assigned vector address to determine and call the appropriate subroutine for processing of the interrupt.

SPECIFICATIONS

Main Specifications

Modes of Operation:	Programmed Digital Output Programmed Digital Input Interrupt Controlled Input Interrupt Controlled Counting
Data Format:	16-bit I/O Data Words
Digital Inputs/Outputs:	252 16-bit words (4032 digital points) maximum
Type of Input/Output:	(see Functional I/O Modules and Signal Conditioning Modules)
I/O Module Selection:	Directly addressable
Interrupt Module:	Module type code and Module address
Interrupt Scan:	Locates address and type in 5 μ sec typical (20 μ sec, worst case)
I/O Data Rate:	10 ⁵ 16-bit words/sec
System Clock Rates:	3 available to each I/O word Line frequency; 6.3v AC 175 Hz—1.75 KHz adjustable 1.75 KHz—17.5 KHz adjustable
Cooling/Filtering:	Dust filters and blower fans in system cabinet.
Input Cabling:	Top or bottom entry, screw terminal connections. #18 A.W.G. 2 wire twisted pair/point max. size for fully wired cabinets. (Screw terminals will accommodate #14 A.W.G. wires.)

Register Addresses

Scan Register (UDSR)	771 774
Control and Status (UDCS)	771 776

UDC11

UNIBUS Interface

Interrupt vector address: 234
Priority level: BR4 or 6
Bus loading: 2 bus loads

Mechanical

Size: each cabinet is 72"H x 21"W x 30"D
Weight: 750 lbs. (dual cabinet, 64 words or 768 points)

Power (per cabinet)

Input current: 15 A at 115 VAC, 40 to 440 Hz, single phase
Heat dissipation: 1700 W

Environment

Operating temperature: 10°C to 40°C
Relative humidity: 10% to 90%

VR01

OSCILLOSCOPE, VR01-A

DESCRIPTION

The VR01, a modified Tektronix type RM503 oscilloscope, provides accurate measurements in DC-to-450 kHz applications. It is a low-frequency, high sensitivity display and can be used for accurate curve plotting in the X-Y mode of operation.

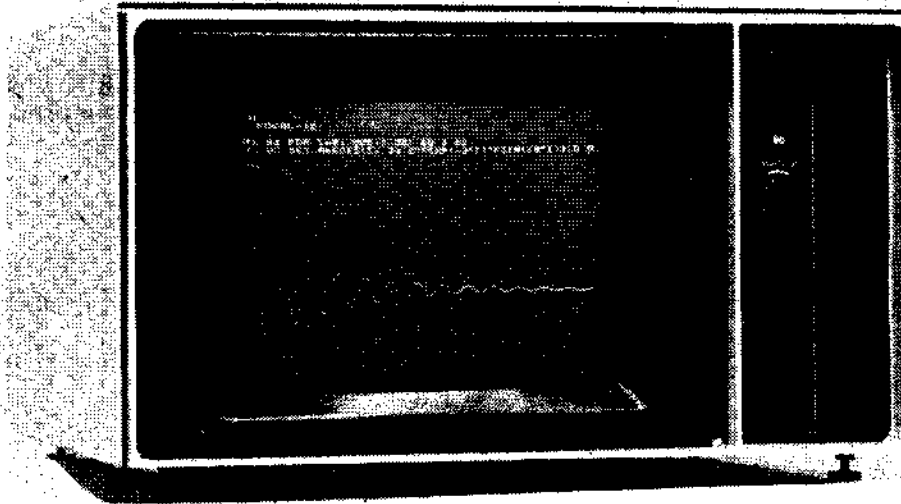
For information concerning the control and programming refer to the AA11-D subsystem.

SPECIFICATIONS

Display Area:	8 x 10cm
Height:	7 in.
Width:	19 in.
Rack Depth:	17 in.
Net Weight:	30 lbs.
Display Rate:	45 kHz max. 50 Hz min.
Display Time:	20 μ s deflection time 2 μ s intensification time
Intensification Levels:	2

VR14

POINT PLOT DISPLAY VR14



VR14 POINT PLOT DISPLAY

DESCRIPTION

The VR14 Point Plot Display is a completely self-contained CRT display with a 6.75 x 9-inch viewing area in a compact 19-inch package. The VR14 requires only analog X and Y position information with an intensity pulse to generate sharp, bright point plot displays. Except for the CRT itself, the unit uses all solid state circuits with high speed magnetic deflection to enhance brightness and resolution. The intensity pulse may be time multiplexed or gated by a separate input to allow the screen to be timeshared between two inputs.

The VR14 is interfaced to the UNIBUS and controlled through the AA11-D digital/analog conversion subsystem.

SPECIFICATIONS

Main Specifications

Viewable Area:	6 ³ / ₄ x 9 in.
Spot Size:	≤ 20 mils inside the usable screen area at a brightness of 30 foot-lamberts.
Jitter:	≤ ± 1/2 spot diameter
Repeatability:	• ≤ ± 1 spot diameter (Repeatability is the deviation from the nominal location of any given spot)

VR14

Gain Change:	From a fixed point on the screen, less than $\pm 0.3\%$ gain change for each $\pm 1\%$ line voltage variation.
Brightness:	≥ 30 foot-lamberts: measured using a shrinking raster technique.
Linearity:	Maximum deviation of any straight line will be $\leq 1\%$ of the line length measured perpendicular to a best fit straight line.
Deflection Method:	Magnetic (70° diagonal deflection angle)
Focus Method:	Electrostatic
Shielding:	CRT is fully enclosed in a magnetic shield.
Overload Protection:	Unit is protected against fan failure or air blockage by thermal cutouts.

Mechanical

Mounting:	1 panel mounted unit
Size:	10 $\frac{1}{2}$ " front panel height
Weight:	75 lbs.

Power

Input current:	4 A at 115 VAC
Heat dissipation:	400 W

Environment

Operating temperature:	10°C to 50°C
Relative humidity:	10% to 90%

STORAGE DISPLAY, VT01-A**DESCRIPTION**

The VT01-A Storage Display is a Tektronix Model 611 direct-view storage tube with a resolution of 400 stored line pairs vertically and 300 stored line pairs horizontally. Dot writing time is 20 μ s, with a full screen erase time of 500 ms. The VT01 can display 30,000 discrete resolvable points.

The VT01-A is interfaced to the UNIBUS and controlled via the AA11-A and AA11-D conversion subsystem.

SPECIFICATIONS**Main Specifications**

Resolution:	Equivalent to 400 stored line pairs along the vertical axis; 300 stored line pairs along the horizontal axis.
Erase Time:	0.5 seconds
Display Time:	Storage Mode—80 μ s deflection time, 20 μ s intensification time Non-Storage Mode—80 μ s deflection time, 2 μ s intensification time
Display Size:	8 $\frac{1}{4}$ Vertical x 6 $\frac{5}{8}$ Horizontal
Display Rate:	10 kHz max. (storage mode)

Mechanical

Mounting:	1 table top unit
Size:	12"H x 12"W x 23"D
Weight:	50 lbs.

Power

Input current:	2 A at 115 VAC (1 A at 230 VAC)
Heat dissipation:	250 W

Environment

Operating temperature:	0°C to 50°C
Relative humidity:	10% to 80%

ALPHANUMERIC TERMINAL, VT05B**DESCRIPTION**

The VT05B Alphanumeric Display Terminal, consisting of a CRT display and self-contained keyboard, can be used as a peripheral I/O device with a computer or as a stand-alone closed-circuit television monitor. In computer applications, the VT05 (with system software) can be used to compose, edit, and forward messages to the computer; retrieve and update alphanumeric data contained in the computer files; receive instructions and data from the processor; and perform on-line debugging. When performing these functions, the VT05 operates similarly to a teletypewriter, except that it is a soft copy device. The advantages of using the VT05 are: it is faster, quieter, more compact, easier to maintain, and considerably more reliable than an electromechanical teletypewriter.

Design Features

The VT05 is a totally self-contained desk-top unit. For ease of maintenance, seven easily replaced solid-state modules make up the entire circuitry of the VT05.

The VT05 has a human engineered CRT screen and input keyboard. The CRT can display up to 1440 very large characters (0.22" x 0.10") at one time. It can be read under most ambient light conditions. Brightness and contrast controls are readily accessible for individual operator adjustment. A special tinted glass shield eliminates glare. The input keyboard offers high input capability with virtually noiseless operation.

The distinctive flowing lines of the VT05 blend well with any decor.

Operational Characteristics

The VT05 is logically and electrically equivalent to the teletypewriter. It can be connected directly to modems, data phones, acoustic couplers and other EIA compatible devices. Or the VT05 may be connected directly to the computer via its 20 milliamp current loop teletypewriter interface. All the functions of the teletypewriter are duplicated so there is no need to modify program codes.

A single switch on the rear of the VT05 allows the operator to select transfer rates of 110, 150, 300, 600, 1200 and 2400 Baud. At the flick of another switch, the VT05 will change from a full duplex terminal to a half duplex one.

The VT05 keyboard can transmit in either of two modes — half ASCII or full ASCII. Half ASCII means that the terminal transmits in upper case alpha codes only. Full ASCII indicates the ability to transmit in both upper and lower alpha codes as well as all control characters.

A unique feature of the VT05 is direct cursor addressing. The cursor is a blinking underline showing where the next character will be displayed on the CRT. With direct cursor addressing, the cursor may be placed at any position on the screen by a computer instruction. This is very useful for filling in of fixed input formats.

CONTROLS AND INDICATORS

Control or Indicator	Location	Function
Power ON/OFF Switch	Right-front	Applies power to the terminal.
LOCAL/REMOTE Switch	Right-front	In LOCAL mode, the terminal is off-line and data transmitted from the keyboard is input to the receiver logic by connecting the transmitter output to the receiver input. In REMOTE mode, data is transmitted from the VT05 to the computer while simultaneously receiving data from the computer for entry into the VT05 buffer memory (full duplex operation). If inputs are received from both the VT05 transmitter and the computer simultaneously (half duplex), the two inputs will be mixed or garbled.
FULL/HALF DUPLEX Switch	Rear Panel	Used to select FULL DUPLEX or HALF DUPLEX operation when LOCAL/REMOTE switch is in the REMOTE position.
CONTRAST Control	Right-hand side	Used to adjust the picture for contrast.
BRIGHTNESS Control	Right-hand side	Used to adjust the CRT brightness (intensity).
VERTICAL Control	Right-hand side	Used to synchronize the raster in the vertical direction.
HORIZONTAL Control	Right-hand side	Used to synchronize the raster in the vertical direction.
BAUD RATE Switch	Rear Panel	A ten-position switch used to select the terminal transmit/receive baud rates.

Baud Rate Switch

Switch Position	Transmit Rate	Receive Rate
Fully Counterclockwise	110	110
	150	150
	300	300
	600	600
	1200	1200
through	2400	2400
Fully Clockwise	150	2400
	110	2400
	150	1200
	110	1200

REGISTERS

The VT05 interfaces to the PDP-11 via the DL11 Controller. All software control of the DL11 Asynchronous Line Interface is performed by four device registers. These registers are assigned UNIBUS addresses and can be read or loaded with PDP-11 instructions that refers to their address.

Register	Mnemonic	Function
Receiver Status Register	RCSR	Provides detailed information on the keyboard status of the VT05, and the DL11 receiver logic. Status information includes such bits as receiver active (RCVR ACT) and receiver done (RCVR DONE). Also includes the interrupt enable bit that can be used to initiate interrupt sequences when RCVR DONE sets.
Receiver Buffer Register	RBUF	Holds the character received from the VT05 keyboard prior to transfer to the UNIBUS.
Transmitter Status Register	XCSR	Provides the interrupt enable bit and the transmitter ready (XMIT RDY) bit (meaning VT05 is ready to accept a character to be displayed). The transmitter logic can be monitored and an interrupt sequence initiated, if desired.
Transmitter Buffer Register	XBUF	Holds the character to be transferred to (displayed by) the VT05.

SPECIFICATIONS**Main Specifications**

Transmission speed:	110 to 2400 Baud
Number of columns:	72
Number of lines:	20
Number of printing characters:	63 (upper case ASCII subset)
Data transmission:	EIA and 20 ma current loop compatible
Interface to PDP-11:	DL11

CRT Display

Screen size:	10 $\frac{1}{8}$ " x 7 $\frac{5}{8}$ "
Character displayable area:	8" x 6 $\frac{1}{4}$ "
Character generation method:	5 x 7 matrix
Character Size	0.22 in. \times 0.11 in.
Phosphor	P4 (white)
Deflection Type	Magnetic
Deflection Method	Raster Scan
Input Impedance (at VIDEO IN input)	75 Ω \pm 5%
Video Input Signal	0.9 to 2.2V with separate horizontal and vertical SYNC.
Sinusoidal Frequency Response	15 Hz to 12 MHz @ 3 dB point
Video Pulse Rise and Fall Time	30 ns (10% to 90% point), measured at cathode with 1.0V p-p input and 30V p-p output.
Video Output Amplitude	< 30V p-p (minimum), measured at cathode with 1.0V p-p input.
Resolution	Screen Center — 600 lines (minimum) Screen Corners — 400 lines (minimum) (using shrinking raster method)
Horizontal Sweep Frequency	15.6 kHz
Vertical Sweep Frequency	50 or 60 Hz (selectable)
Horizontal Retrace	11 μ s (maximum)
Vertical Retrace	21 horizontal lines @ 15.6 kHz
High Voltage	11 kV (minimum) @ 50 μ A beam current @ 24 Vdc power supply adjustment
High Voltage Regulation	12 M Ω (maximum), with a beam current change from 50 to 150 μ A @ 24 Vdc power supply adjustment.
Horizontal Linearity	\pm 5%, measured at 0.5 in. intervals.
Vertical Linearity	\pm 7%, measured 0.75 in. intervals.
CRT Refresh Rate	50 or 60 Hz

Mechanical

Mounting:	1 table top unit
Size:	12"H x 19"W x 30"D
Weight:	55 lbs.

VT05

Power

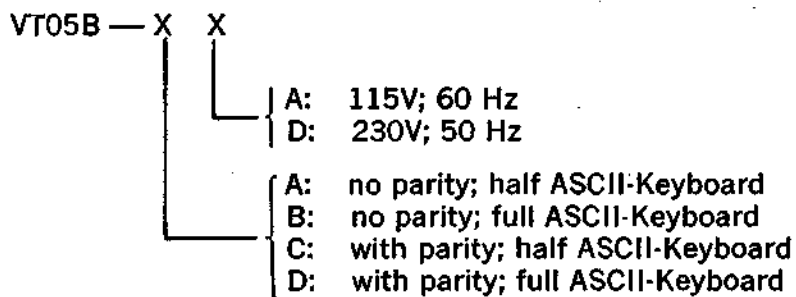
Input current: 2 A at 115 VAC
Heat dissipation: 130 W

Environment

Operating temperature: 10°C to 40°C
Relative humidity: 10% to 90%

Models

Optional variations available in the VT05 Alphanumeric Display Terminal are listed below.



VIDEO DISPLAY TERMINAL, VT50

DESCRIPTION

The VT50 is a microprocessor driven alphanumeric display terminal priced to be competitive with standard 10 character per second mechanical teletypewriter devices. The VT50 (with system software) can be used to compose, edit, and forward messages to a host computer; retrieve and update alphanumeric data contained in computer files; receive data and instructions from the processor; and perform on-line debugging. The interface to the computer is logically the same as for a teletypewriter except the VT50 is 1) a soft copy device, 2) markedly faster, 3) quieter, 4) easier to use and maintain, and 5) considerably more reliable than an electromechanical device.

Screen and Keyboard

Alphanumeric data received at the screen is displayed within a 5 by 7 dot matrix. Up to 12 lines of text can be displayed at any one time—maximum line length is 80 characters. P4 phosphor is used for optimum character resolution. This means the VT50's display gives better resolution than a consumer-grade television set. The screen is recessed and tilted to avoid glare from overhead lighting. The VT50 will accept color filters.

Key placement is similar to a typewriter, rather than a teletypewriter. The keyboard is designed to give the operator an audio/tactile response to reinforce the feel of normal typewriter operation. This mechanism can be disabled if absolute quiet is necessary. Another keyboard feature is 3-key rollover to help eliminate errors that might occur due to fast typing; up to three keys can be depressed and transmission will be correct if one of the first two keys is released before the third. The keyboard and tactile response unit are the only mechanical moving parts in the VT50. Keyswitches are composed of inlaid, rolled gold to ensure positive connection. Extensive keyboard testing (over 100,000,000 failure-free keystrokes) proves switch reliability.

Operator Interaction

Operator interaction with the VT50 is based on the cursor—a flashing underline that shows where the next character will appear. The cursor serves as a fast positional indicator for operator response. Programmers can direct the computer to display a form on the screen and move the cursor to its proper location so the operator can fill in responses. The screen's 80 character per line format allows the exact display of FORTRAN and COBOL full-card images.

The cursor can be moved from the keyboard or under program control . . . to the home position (top left corner of the screen), right one position, left one position, up one line, and down one line. The VT50 has tabs that are fixed at every eight spaces, as well as the ability to erase characters from the cursor to the end of a line and from the cursor to the end of the screen.

Character Processing

As each ASCII character is received at the terminal, it is monitored to determine whether it is a displayable letter, number, or symbol (octal 000 through 037). Displayable characters are stored in memory to be scanned and displayed on the screen. ASCII code for both upper and lower case letters can be stored, but lower case letters are converted to upper case before they are displayed.

The algorithm for translating lower case input to upper case display is "if bit number 7 is 1, then force bit number 6 to 0." For example, a lower case "b" is received and stored in the terminal's memory as 1 100 010 (octal 142). Between the memory and the screen, octal 142 is converted to octal 102 (1 000 010)—the ASCII code for an upper case "B." This conversion algorithm means special care must be taken if octal codes 140, 173, 174, 175, or 176 are transmitted to the VT50, because these codes generate the @, [, /,], and ~ symbols, respectively.

OCTAL CODE	ASCII CHARACTER	ACTUAL DISPLAY
140	,	@
173	{	[
174		\
175	}]
176	~	^

If the terminal receives octal 177, it is treated as a no-op (or filler) character. This feature makes the VT50 compatible with certain applications software written to interface with slower mechanical devices. For example, it takes a mechanically designed terminal much longer to effect a TAB operation than the internal clocking of a host computer. In order to preclude the condition of data backing up until mechanical functions are completed, some software programs use filler characters to take up the slack time.

An octal 177 is transmitted if the DEL key is typed. If the key is used to direct a previously typed character to be deleted on the screen, the host system software must translate the incoming 177 into a sequence such as "BACKSPACE, SPACE, BACKSPACE," which is echoed to the terminal. This operation is often used with existing software.

Commands and Escape Sequences

In 7-bit ASCII, codes 000 through 037 are defined as control codes (commands.) The following six control codes are recognized by the VT50:

Octal Code	Action Taken
007	Rings the buzzer.
010	Backspaces the cursor.
011	(Horizontal Tab) Moves the cursor to the next TAB stop. TAB stops are set every eight spaces to the 72nd char-

VT50

	acter position. After the 72nd position, TAB moves the cursor one position to the right.
012	(Line Feed) Moves the cursor down one line
015	Carriage return.
033	Puts the terminal in Escape Mode if the terminal is currently in normal mode. If the terminal is in Escape mode, receipt of 033 puts it back in normal mode.

A command protocol is built around the Escape code (033) to implement those commands needed by the VT50 but not found in 7-bit ASCII. Upon receiving the Escape code 033, the terminal is set to Escape mode and treats the next character received as a command. Commands created in this manner are called Escape Sequences. The VT50 recognizes the following Escape Sequences.

ESC (033) Followed By:

OCTAL Code	Char	Action Taken
033	ESC	Sets the terminal in normal mode if the terminal is in normal mode before the first is received. Sets the terminal in Escape mode before the first 033 is received. The first 033 changes the mode, the second 033 changes it back.
101	A	Moves cursor up one line.
103	C	Moves cursor right one position.
110	H	Moves cursor to the Home position.
112	J	Erases from cursor position to end of screen.
113	K	Erases line from cursor to right margin.
132	Z	Requests the terminal to identify itself. The terminal will respond with: <ul style="list-style-type: none">• ESC / A (033 057 101) if it is a VT50 with no copier.• ESC / B (033 057 102) if it is a VT50 with copier.
133	[Enables Hold Screen Mode.
134	\	Disables Hold Screen Mode.

Two control dials let the programmer select transmission rates from 75 to 9600 baud (75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud). These control dials can be set so the VT50 transmits data at one speed and receives data at another speed.

Communication Rates

Two rotary switches on the VT50 allow selection of communication rates from 75 to 9600 baud, and the related operational modes.

VT50

Mode	Baud Rate Transmit	Receive	Switch S1*	Switch S2**
Local	9600	9600	1	G
	4800	4800	1	F
	2400	2400	1	E
	1200	1200	1	D
	600	600	1	C
	110	110	1	B
Full Duplex with Local Copy	9600	9600	2	G
	4800	4800	2	F
	2400	2400	2	E
	1200	1200	2	D
	600	600	2	C
	110	110	2	B
Full Duplex	9600	9600	3	G
	4800	4800	3	F
	2400	2400	3	E
	1200	1200	3	D
	600	600	3	C
	300	300	4	A
	150	150	5	A
	110	110	3	B
	75	75	6	A
Full Duplex (Split Speeds)	300	9600	4	G
	150	9600	5	G
	75	9600	6	G
	300	4800	4	F
	150	4800	5	F
	75	4800	6	F
	300	2400	4	E
	150	2400	5	E
	75	2400	6	E
	300	1200	4	D
	150	1200	5	D
	75	1200	6	D
	300	600	4	C
	150	600	5	C
	75	600	6	C

* Switch S1 Labels

1 = Local
 2 = 1/2
 3 = Full Duplex
 4 = 300 Baud
 5 = 150 Baud
 6 = 75 Baud

** Switch S2 Labels

A = Bell 103
 B = 110 Baud
 C = 600 Baud
 D = 1200 Baud
 E = 2400 Baud
 F = 4800 Baud
 G = 9600 Baud

VT50

Up to 12 lines of information can be displayed at one time. When the bottom line on the screen is displayed, and the cursor is directed to move to the next line, the top line automatically "scrolls" off the screen to allow space for the new line. When receiving data at high baud rates, scrolling can occur so rapidly a visual inspection of screen information is impossible. For example, at 9600 baud, the VT50 can receive 960 characters per second—enough to fill the whole screen. A simple command directs the VT50 to give the operator or host computer control over scrolling so the display can be updated on a line-by-line or screen-by-screen basis.

The VT50 operates in either off-line or on-line mode. Off-line mode is useful for training, troubleshooting, and maintenance. In on-line mode, the VT50 can be set for Full Duplex operation or for Full Duplex with Local Copy operation. Full Duplex with Local Copy is used if software was written to operate in half duplex. Data entered at the keyboard is displayed on the screen for visual confirmation at the same time it is sent to the host computer.

Programmer-assigned functions can be written into system software and accessed by using the VT50's ESC key. (Commands created in this way are called *Escape Sequences*.) The host computer can be programmed so that the receipt of ESC 1 implements one routine, ESC 2 another, and so on.

A means of identifying unique Escape Sequence functions is incorporated into the VT50's architecture. Labels above the top ten keys direct the operator to the proper key for each sequence. Labels can be easily changed to accommodate new functions and applications.

SPECIFICATIONS

Main Specifications

Transmission speed:	Switch-selectable Full Duplex: 75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud Full Duplex with Local Copy: 110, 600, 1200, 2400, 4800, and 9600 baud
Keyboard:	Character set: 64 ASCII upper case, alpha, numeric, and punctuation characters Typewriter format keyboard Audio/tactile response mechanism for fast operator feedback 3-key rollover feature to minimize typing er- rors BREAK key included for half duplex software
Number of columns:	80
Number of lines:	12

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Data transmission:	20 ma current loop standard; EIA or CCITT interface optional
Interface to PDP-11:	DL11
Mechanical	
Mounting:	1 table-top unit
Size:	14" H x 21" W x 28" D
Weight:	45 lbs
Power	
Input current:	1 A at 100 to 126 VAC, 60 ± 1 Hz
Heat dissipation:	110 W
Environmental	
Operating temperature:	10°C to 40°C
Relative humidity:	10% to 90%
Miscellaneous	
Terminal modes:	Off-line mode On-line mode: Full Duplex or Full Duplex with Local Copy
Operator controls:	Power on/off, intensity control, baud rate switches, Full Duplex or Full Duplex with Local Copy Switch
Cursor:	Control: up or down one line, right or left one position, home, erase from cursor to end of line, erase from cursor to end of screen Type: non-destructive, underscore
Page overflow:	Upward Scroll
Character matrix:	5 x 7
Character size:	0.11 in x 0.20 in
Screen size:	8.7 in x 4.3 in
Display capabilities:	control data transmission at high baud rates; will contain FORTRAN or COBOL full-card images, operator adjustable character intensity
Case material	Noryl SE-100 plastic (polythethylene oxide modified with polystyrene)
Overload protection	Thermal switch in line transformer
Transmission code	USASCII extended through Escape Sequence
Parity	Even or mark (no parity) switch-selectable

DECSCOPE VIDEO DISPLAY TERMINAL, VT52

DESCRIPTION

The VT52 is an upper-and-lower-case ASCII video terminal whose display holds 24 lines of 80 characters.

The VT52 is upward-compatible with the VT50, but an identification feature allows software to distinguish between the two models. Software which uses Hold-Screen Mode to produce operator-controlled, screenful-by-screenful output to the VT50 will work on the VT52 without modification, despite the different screen capacities.

The VT50's human-engineering features carry over to the VT52: A clicking sound provides feedback to the operator when keys are typed; a rollover feature lets the terminal get the message straight even if two or three keys are pressed at once; the keyboard follows the standard typewriter layout.

The VT52 goes beyond the VT50, however, to provide a "two-way" auxiliary keypad. In one mode, the keypad is used to generate program-compatible numeric codes. Applications which require much numeric input can use the VT52 without modifying hardware or software, while the operator uses the convenient "numeric pad." Or, software may place the VT52 in the alternate mode, in which each key on the keypad transmits a unique Escape Sequence. This allows the host computer to distinguish between keys typed on the auxiliary keypad and similar keys on the main keyboard. In this mode, each key on the keypad can be used to invoke a user-defined function.

The VT52 has a wide range of cursor-positioning functions. As well as moving the cursor one position in any direction, software can move the cursor to any position on the screen with a Direct Cursor Addressing command which specifies the destination for the cursor. The VT52 also offers fixed horizontal tabs, a "Cursor-to-Home" command, and two screen-erasure functions. Data on the screen scrolls up when a Line Feed function is performed with the cursor on the bottom line; it scrolls down when a Reverse Line Feed function is performed with the cursor on the top line.

APPLICATIONS

A Window on a File. The VT52's full character set (upper-and-lower-case) makes it an excellent terminal for text entry and editing. Its design suggests a new method of editing text: a method in which the operator, rather than having to learn a new command language for text-editing, simply arranges text on the screen the way the file is to read. The computer, which maintains an image of the text displayed on the VT52's screen in memory, responds to special commands from the operator and performs advanced features involving text compression or expansion.

The VT52, with 24 lines, lets the operator view a large portion of the file. To move about in files containing more than 24 lines, the VT52 can scroll the information on its screen up and down.

VT52

When the operator gives the host a command to end the editing session, the host writes its screen image onto a storage device. This text-editing system is "error-proof," since there is never any doubt as to what the file contains at any time.

A Dynamic Display System. The 24 lines of the VT52's screen can be used to monitor 24 separate processes, or more. Consider a situation in which the VT52 is displaying the status of 24 scheduled airline flights, one on each line. If some of the information changes, it is possible to change the field on the screen which displays that information without rewriting the whole screen.

The VT52 fits this application with its Direct Cursor Addressing, a feature which allows software to move the cursor from any position on the screen to any other position with a single command.

To replace any information on the screen, the host sends the Direct Cursor Addressing command, two characters which select the line and column number, and the new data.

A File Display System. In its Hold-Screen Mode, the VT52 allows the operator to control the flow of data onto the screen. With most terminals, whatever the host sends to the terminal goes on the screen immediately. But the VT52 can operate at such a rapid speed that 12 full lines of data could be scrolled off the top of the screen every second, as new data enters the screen at the bottom. In Hold-Screen Mode, the VT52 will not perform a scroll until requested to do so by the operator. In a situation where any data would be scrolled off the screen, the VT52 buffers incoming data rather than processing or displaying it, and sends signals to the host telling it to stop or resume transmitting.

If the operator types the SCROLL key, the terminal will allow one line of data through to the screen. The operator can also use the SCROLL key to request the VT52 to accept 24 new lines, one new screenful, from the host.

Business Data Entry. In addition to providing keys for the numerals and decimal point, the VT52's 19-key numeric pad contains an ENTER key (which transmits the control code CR), and three blank keys. These keys transmit unique, multiple-character Escape Sequences which can be interpreted by software. The four remaining keys are labeled with arrows pointing up, down, right, and left. The host can respond to these keys by positioning the cursor, or, since these keys transmit Escape Sequences as the blank keys do, they can be relabeled and used to transmit special commands to software. If these Escape Sequences are echoed back literally, the cursor will move one position in the corresponding direction on the screen. Software can place the VT52 in a mode where all 19 keys on the numeric pad transmit unique Escape Sequences.

A key-click sound system, the layout of the keyboard, and 2½-key roll-over are all designed to give the VT52 the look and feel of a regular type-

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writer. This improves the efficiency of the typist and minimizes training time.

Changing Configurations. The VT52 is plug-compatible and functionally upward-compatible with the VT50. When VT52s and VT50s are used in the same computer system, software can send each terminal a command to identify itself. The T52 will automatically transmit a three-character Escape Sequence which identifies it as a VT52. The host thus determines which features can be used with the terminal presently attached.

The significance of this feature is that VT50s, VT52s and future VT models can be freely interchanged within a system, with the software responding correctly to each different type of terminal.

TECHNICAL INFORMATION

Commands

The following table lists the actions which the terminal takes upon receipt of the corresponding codes from the host computer.

Character(s) and Octal Code(s)	Action Taken
BEL (007)	Sounds the audible alarm.
BS (010)	Moves the cursor left one position, unless it was at the start of a line to begin with.
TAB (011)	Moves the cursor rightward to the next TAB stop, unless the cursor was at the end of a line to begin with. (TAB stops are fixed in columns 9, 17, 25, 33, 41, 49, 57, 65, 73, 74, 75, 76, 77, 78, 79, and 80.)
LF (012)	Moves the cursor down one line—performs an upward scroll if the cursor was on the bottom line.
CR (015)	Moves the cursor to the start of the same line it was on.
ESC (033)	Serves as a signal that the following character is to be interpreted rather than displayed; ESC introduces multicharacter commands—"Escape Sequences"—which are listed below.
Space (040) and the displayable characters (041-176)	The character is displayed at the cursor position; then the cursor is moved right one column, unless it was at the end of a line to begin with. In particular, Space (040) blanks the character at the cursor position and moves the cursor right.
NUL (000) and DEL (177)	The terminal does not respond to NUL or DEL, in order to be compatible with slower electromechanical devices that use these characters as fillers.

Escape Sequences	Effect
ESC = (033 075)	ENTERS Alternate-Keypad Mode. In Alternate-Keypad Mode, keys on the numeric pad transmit unique Escape Sequences to distinguish them from similar keys on the main keyboard, and to invoke user-defined functions.
ESC > (033 076)	EXITs Alternate-Keypad Mode—returns to Numeric-Keypad Mode. (Alternate-Keypad Mode remains in effect until this command disables it.)
ESC A (033 101)	Moves the cursor up one line, unless it was already on the top line—does not perform a scroll.
ESC B (033 102)	Moves the cursor down one line, unless it was already on the bottom line—does not perform a scroll.
ESC C (033 103)	Moves the cursor right one column, unless it was already at the end of a line—does not erase the character at the old cursor position.
ESC D (033 104)	Moves the cursor left one column, unless it was already at the start of a line—same as BS (010).
ESC H (033 110)	Moves the cursor HOME: to the start of the top line.
ESC I (033 111)	Moves the cursor up one line—performs a downward scroll if the cursor was on the top line.
ESC J (033 112)	Erases all data from the cursor position to the end of the screen.
ESC K (033 113)	Erases all data from the cursor position rightward on the same line.
ESC Y (033 131)	Direct Cursor Addressing feature—moves the cursor to any specified position on the screen, regardless of where it was before. (The format of this command is shown below.)
ESC Z (033 132)	Requests the terminal to identify itself. The terminal will respond with a three-character Escape Sequence unique to its own configuration.
ESC [(033 133)	Enters Hold-Screen Mode. In Hold-Screen Mode, data will not be scrolled off the screen until the operator requests it by typing the SCROLL key.
ESC \ (033 134)	EXITs Hold-Screen Mode. (Hold-Screen Mode remains in effect until this command disables it.)

Direct Cursor Addressing Command

Format:

```
ESC   Y   Line#   Column#
Line# is one character; octal code 040 to refer
to the top line, 041 to refer to the second line,
```

... 067 to refer to the bottom line. Column# can legally range from 040 (leftmost column) to 157 (rightmost column). The cursor is moved to the specified column of the specified line.

033 110 (move the cursor HOME) is equivalent to
033 131 040 040 (move the cursor to column 1 of line 1)

Summary of Basic Cursor Movements

UP:	ESC A	does not scroll
	ESC I	scrolls text down*
DOWN:	ESC B	does not scroll
	LF	scrolls text up*
RIGHT:	ESC C	does not erase
	space	erases
LEFT:	ESC D	(these two are equivalent)
	BS	

The BREAK Key

Typing the BREAK key causes the transmission line to be forced to its zero state for as long as the BREAK key is held down.

The BREAK function is commonly used to forcibly interrupt the flow of data coming to the terminal. It is provided for users with older software written to operate in Half Duplex. In Half Duplex, only one data communication line exists between terminal and computer. If the computer has control of this line, BREAK is the only means of forcing an interrupt. However, because DESscopes have both input and output lines, the forcible BREAK is normally unnecessary.

The REPEAT Key

Any key which transmits a code (or codes) to the computer will transmit that code (or codes) repeatedly if pressed while the REPEAT key is down. The keys on the numeric pad which transmit more than one character apiece will transmit their sequence repeatedly, if pressed with the REPEAT key down. The rate of repetition may attain 30 characters per second (on 50 Hz models, 25 characters per second), or it may be limited to a slower rate if the baud rate is not set to accommodate such rapid transmission.

The SHIFT Keys

On keys which have more than one symbol, the code for the top symbol will be transmitted if either or both of the SHIFT keys are pressed; the code for the bottom symbol will be transmitted if neither SHIFT key is down.

Typing any alphabetic key when either or both of the SHIFT keys are down will cause an upper-case code to be transmitted. Typing an alphabetic key when neither SHIFT key is down will cause a lower-case code

*If the cursor cannot move any further in the specified direction.

to be transmitted. The SHIFT keys also affect the function of the SCROLL key.

The CAPS LOCK Key

When the CAPS LOCK key is down, typing any alphabetic key (A through Z) will cause an upper-case code to be transmitted, regardless of whether a SHIFT key was down. But unlike a typewriter's SHIFT LOCK key, CAPS LOCK does not affect the codes transmitted by keys other than the alphabetic keys.

The CONTROL Key

When the CONTROL key is pressed, the two high-order bits of each character are masked out, allowing "control codes"—in the range 000-037—to be generated from the keyboard.

The Auxiliary Keypad

The VT52's auxiliary keypad operates in one of two modes. Software can place the terminal in a mode in which the keypad can be used for data entry, just as the main keyboard's numeral keys can be used. If it is desired to distinguish between the typing of keys on the keypad and keys on the main keyboard, software can select a mode in which each key on the keypad transmits a unique Escape Sequence.

Typing the key labeled. . .	IN NUMERIC- KEYPAD MODE, transmits the following code(s)	IN ALTERNATE- KEYPAD MODE, transmits the following code(s)
0	0	ESC ? p
1	1	ESC ? q
2	2	ESC ? r
3	3	ESC ? s
4	4	ESC ? t
5	5	ESC ? u
6	6	ESC ? v
7	7	ESC ? w
8	8	ESC ? x
9	9	ESC ? y
.	.	ESC ? n
ENTER	CR	ESC ? M
(up arrow)	ESC A	ESC A
(down arrow)	ESC B	ESC B
(right arrow)	ESC C	ESC C
(left arrow)	ESC D	ESC D
(left blank key)	ESC P	ESC P
(center blank key)	ESC Q	ESC Q
(right blank key)	ESC R	ESC R

If the codes transmitted by the "arrow" keys are echoed back to the terminal, they will cause the cursor to move one position in the direction the arrow points in.

The CONTROL, SHIFT, and CAPS LOCK keys do not affect the codes transmitted by the keys on the auxiliary keypad, in either Keypad Mode.

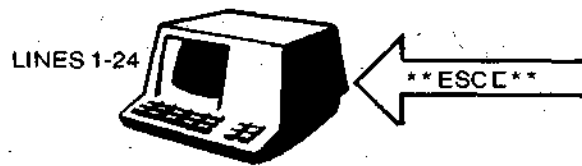
The SCROLL Key

(Significant only with the terminal in Hold-Screen Mode.)

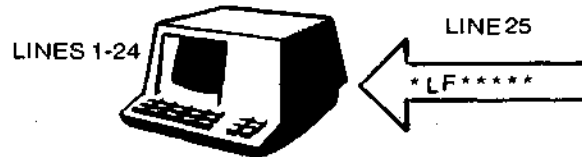
UNSHIFTED Directs the terminal to allow one scroll to occur, admitting one new line of data to the screen.

SHIFTED Directs the terminal to allow 24 scrolls to occur, admitting one new screenful of data to the screen.

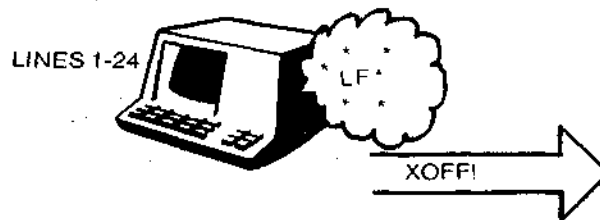
Hold-Screen Mode



Host is transmitting data to VT52—transmits proper codes to place VT52 in Hold-Screen Mode.



Host transmits LF to VT52. Cursor is on the bottom line, but VT52 may not perform a scroll.



VT52 buffers LF and subsequent characters. Since it cannot process them without scrolling the display, it sends XOFF (023) to request that the host suspend transmission.



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Operator, having finished reading the display, types the SCROLL key to see more lines.



Data from the buffer is now processed. In particular, LF is processed, causing a scroll. Line 1 leaves the screen; line 25 begins to appear at the bottom.



If the entire buffer is exhausted without encountering a second LF, the VT52 sends XON (O21) to the host to request it to resume transmission. XOFF, XON; and the VT52 buffer are completely transparent to the user.

SPECIFICATIONS

Dimensions:	Height: 360mm (14.1 in.) Width: 530mm (20.9 in.) Depth: 690mm (27.2 in.) Minimum Table Depth: 450mm (17.7 in.)
Weight:	20 kg (44 lbs)
Operating Environment:	10°C to 40°C (50°F to 104°F) Relative humidity 10% to 90% Maximum wet bulb 28°C (82°F) Minimum dew point 2°C (36°F)
Line Voltage:	(US model) 100-126 volts (European model) 191-238 volts or 209-260 volts
Line Frequency:	(US model) 60 ± 1 Hz (European model) 60 ± 1 Hz or 50 ± 1 Hz
Power Consumption:	110 Watts
Power Line Hash Filter:	Low Leakage Balun type
Display:	Format: 24 lines x 80 characters Character Matrix: 7 x 7 Character Size: 2.0mm x 4.0mm (0.08 in. x 0.16 in.)

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	<p>Screen Size: 210mm x 105mm (8.3 in. x 4.1 in.) Character Set: 96-character displayable ASCII subset (upper and lower-case, numeric, and punctuation).</p>
Keyboard:	<p>Character Set: Complete 7 bit ASCII set (128 codes) Key layout: Typewriter—rather than keypunch—format, 63 keys. Auxiliary keypad: 19-keys: numerals, cursor-movement, 3 user-definable function keys. CAPS LOCK Key: Locks alphabetic keys to upper-case state, but does not affect non-alphabetic keys.</p>
Audible Signals:	<p>Key-click: Switch-controlled Bell: Sounds (a) upon receipt of control characters BEL; (b) when Keyboard input approaches right margin (output from host approaching right margin does not cause bell to ring).</p>
Page Overflow:	<p>LF causes upward scroll; Reverse Line Feed causes downward scroll.</p>
Parity:	<p>Even or mark (no parity) switch-selectable. Odd or space possible with rewiring.</p>
Cursor:	<p>Type: Blinking underline. Control: Up or down one line; right or left one character; home; tab (fixed tab stops every 8 spaces); direct cursor addressing (allows cursor to be moved to any character position on the screen).</p>
Functions:	<p>Erase display from cursor position to end of line; erase to end of screen; scroll up; scroll down.</p>
Hold-Screen Mode:	<p>Allows operator to halt transmission from host, preserving data on display. Operator can request new data, line- or screenful-at-a-time. Enabled/disabled by Escape sequences sent by system software.</p>
Terminal Self-Identification:	<p>Terminal transmits on command a sequence unique to its model; software can identify features available on any terminal it is in contact with.</p>
Communications:	<p>20mA current loop or EIA interface; specify at time of order. Code: USASCII extended through Escape Sequences. Speed: Switch-selectable. Transmission rates, full duplex (switch selec-</p>

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table) 75, 110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud.
Switch-selectable local copy.

Synchronization: Automatically transmits control codes to host, requesting suspension and resumption of transmission, when unable to process data.

Operator Controls: Power On/Off, Intensity Control, Baud Rate Switch, Terminal Mode Switch, Key-Click On/Off, Even/No Parity.

Overload Protection: Thermal cutout.

Case Material: Injection molded Noryl thermoplastic.

Screen Phosphor: P4

UNIBUS THEORY AND OPERATION

5.1 INTRODUCTION

5.1.1 Single Bus

The UNIBUS is a single, common set of signal wires that connects the processor, memory, and all peripherals. Addresses, data, and control information are transmitted along the 56 lines of the bus. Figure 5.1 is a simplified block diagram of the PDP-11 System and UNIBUS.

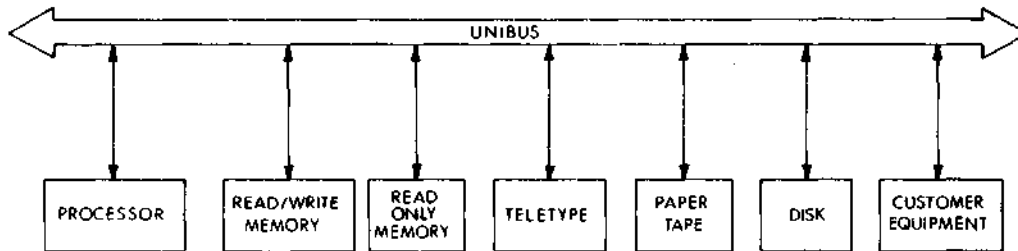


Figure 5.1 PDP-11 System Simplified Block Diagram

The form of communication is the same for every device on the UNIBUS. The processor uses the same set of signals to communicate with memory and peripheral devices. Peripheral devices also use this set of signals when communicating with the processor, memory, or other peripheral devices.

All instructions applied to data in memory can be applied equally well to data in peripheral device registers. Therefore, peripheral device registers may be manipulated as flexibly as memory by the processor. This is an especially powerful feature, considering the special capability of PDP-11 instructions to process data in any memory location as though it were an accumulator.

5.1.2 UNIBUS Lines

UNIBUS signals may be divided into two general categories with respect to the manner in which they are transmitted. The majority of signals use lines that are, in effect, wired-OR circuits to which the inputs to the bus receivers and the outputs of the bus drivers are connected. These lines are thus available along the length of the UNIBUS to any device which needs to receive or to assert the signals transmitted on the lines. Devices which do not wish to assert a signal should remain inactive. It should be noted, however, that some of the signals transmitted on lines of this type are logically, if not electrically, "unidirectional."

5.1.3 Master-Slave Relation

Communication between two devices on the bus is in a master-slave relationship. During any bus operation, one device has control of the bus. This device, the bus master, controls the bus when communicating with another device on the bus, called the slave. A typical example of this relationship is the processor, as master, transferring data to memory, as slave. Master-slave relationships are dynamic. The processor, for ex-

ample, can pass bus control to a disk. The disk, as master, then communicates with a slave memory bank.

The UNIBUS is used by the processor and all I/O devices; thus, a priority structure determines which device obtains control of the bus. Consequently, every device on the UNIBUS capable of becoming bus master has an assigned priority. When two devices which are capable of becoming bus master have identical priority levels and simultaneously request use of the bus, the device that is electrically closest to the processor receives control.

5.1.4 Interlocked Communication

Communication on the UNIBUS is interlocked between devices. Each control signal issued by the master device must be acknowledged by a response from the slave to complete the transfer. Therefore, communication is independent of the physical bus length and the response time of the master and slave devices. The maximum transfer rate on the UNIBUS with optimum device design, is one 16-bit word every 400 ns, or 2.5 million 16-bit words per second.

5.2 PERIPHERAL DEVICE ORGANIZATION AND CONTROL

Registers in peripheral devices are assigned addresses similar to memory; thus, all PDP-11 instructions that address memory locations can become I/O instructions. Data registers in devices can take advantage of all the arithmetic power of the processor. The PDP-11 controls devices differently than most computer systems. Control functions are assigned to addressable registers, and then the individual bits within that register can cause control operations to occur. For example, the command to make the paper-tape reader read a frame of tape is provided by setting a bit (the reader enable bit) in the control register of the device. Status conditions are also handled by the assignment of bits within this register, and the status can be checked by program instructions. There is no limit to the number of registers that a device may have, providing an unlimited flexibility in the design and control of peripheral equipment.

5.3 TRANSFER OF BUS MASTER

A device (other than the processor) that is capable of becoming bus master generally requests use of the bus for one of two purposes:

- a. To make a non-processor transfer of data directly to or from memory, or
- b. To interrupt program execution and force the processor to jump to a specific address where an interrupt service routine is located.

5.3.1 Transfer Request Handling

The request and granting of bus mastership is performed in parallel with data transfers on a completely independent set of bus lines. Thus, while one device is using the bus, the next request is being checked for priority and the next user is being assigned. Because of this time parallelism, successive data transfers by different master devices can occur at the full UNIBUS speed.

5.3.2 Priority Structure

The use of the data section of the bus is granted to requesting devices according to a priority scheme. The priority of a device is a function of

(1) the priority level assigned to the device, and (2) its position on the bus with respect to other devices of the same priority level.

All devices, with the exception of the processor, may be assigned to one (or more) of five priority levels. A signal line is dedicated to each of these levels. Each of these lines is driven by all bus devices assigned to the priority level. These five lines are referred to as "request lines" and are monitored by the arbitrator. A device that requires the use of the data section of the bus asserts a request on one of these lines. This request is received by the arbitrator. The arbitrator also monitors the priority level of the processor. There are five relevant processor levels.

If no request at a level higher than the current processor level is being received at the arbitrator, the data section of the bus is available to the processor. The arbitrator, however, may issue a grant at the level of the highest priority active request if the processor is not at a higher priority level.

A grant is a signal that informs a requesting device that it may become bus master after the current master releases the data section of the bus.

A grant asserted by the arbitrator is received by the first device on the bus assigned to the same priority level as the grant. If this device is requesting the use of the data section of the bus, it accepts and acknowledges receipt of the grant and blocks the grant. If the device is not requesting the use of the data section, it passes the grant to the next device on the same grant line. This procedure is repeated until a device accepts the grant or until the end of the bus is reached. In this last case, the grant is cancelled and the arbitration process is re-started. It can be seen from the above discussion that each device on a UNIBUS is assigned a discrete position in the priority scheme. This position is determined:

- a. By the priority level assigned to the device, and
- b. By the position of the device on the grant line (with respect to the other devices of the same priority level).

All devices assigned to a given priority level have higher priority than any device at a lower level. Within a given priority level, the device closest to the origin of the grant signal has the highest effective priority.

5.3.3 Data Transfer

Direct memory or device access data transfers can be accomplished between any two peripherals without processor supervision. These are called NPR level data transfers. Normally, NPR transfer are made between the memory and a mass storage device, such as a disk.

During NPR transfers, it is not necessary for the processor to transfer the information between the memory and the mass storage device. The bus structure enables device-to-device transfers, thereby allowing customer-designed peripheral controllers to directly access other devices (such as disks) on the bus. This direct access capability permits operations such as a disk directly refreshing a CRT display.

An NPR device provides extremely fast access to the bus and can transfer data at high rates once it gains control. The processor state is not

affected by this type of transfer; therefore, the processor can relinquish bus control while an instruction is in progress. This release of the bus can occur in general, whenever the processor is not using the bus. However, the bus can never be released between cycles of a read-modify-write sequence. An NPR device in control of the bus transfers 16-bit words or 8-bit bytes to memory at the same speed as the memory cycle time.

5.3.4 Interrupt Requests

Devices that gain bus control with one of the bus request lines (BR7, BR6, BR5, BR4) can take full advantage of the power and flexibility of the processor by requesting an interrupt. The entire instruction set is then available for manipulating data and status registers. When a device servicing program is to be run, the task being performed by the processor is interrupted, and the device service routine is initiated. After the device request has been satisfied, the processor returns to its former task. Note that interrupt requests can be made only if bus control has been gained through a BR priority level. An NPR level request must not be used for an interrupt request.

5.3.5 Interrupt Procedure

This paragraph provides an example of an interrupt operation. Assume that a peripheral requires service and requests use of the bus at one of the four BR levels. The operations required to service the device are as follows:

- a. Priorities permitting, the processor relinquishes bus control to the device.
- b. When the device gains control of the bus, it sends the processor an interrupt command and a unique address of a memory location which contains the starting address of the device routine. (This is called the interrupt vector address.) Immediately following this pointer address is a word (located at vector address + 2) to be used as the new processor status (PS) word.
- c. The processor pushes the current processor status word and then the program counter (PC) value on the processor stack. The stack is pointed to by register R6.
- d. The new PC and PS (the interrupt vector) are taken from the address specified by the device, and the device service routine is initiated.

NOTE

These operations are performed automatically and no device polling is required to determine which service routine to execute.

- e. The device service routine can cause the processor to resume the interrupted process by executing the Return from Interrupt (RTI) instruction which pops the two top words from the processor stack and transfers them back to the PC and PS registers.
- f. A device service routine can, in turn, be interrupted by a higher priority bus request any time after the first instruction of the routine has been executed.

- g. If such an interrupt occurs, the PC and PS of the current device service routine are automatically pushed onto the stack, and the new device routine is initiated as before. This nesting of priority interrupts can continue to any level; the only limitation is the amount of memory available for the processor stack.

5.4 UNIBUS SIGNAL LINES

The UNIBUS consists of 56 signals. Simplified and standardized control logic is made possible by using separate dedicated lines for all signals. For example, in a data transfer, the master device provides the address of the location which it wishes to access. The device which responds is the slave device. Control and timing signals are provided. Address, control and data and timing functions are each transmitted on a distinct set of bus lines.

All bus activity is asynchronous and depends on interlocked control signals. In every case, a control signal transmitted by the initiator of a transaction is positively acknowledged by the receiver of that signal, and vice-versa.

Although the UNIBUS is a single communication path for all devices in a PDP-11 computer system, the bus actually consists of three interrelated parts. These parts may be referred to as the priority arbitration section, the data transfer section, and the initialization section. These sections use the signal lines shown in Figure 5-2.

NAME	MNEMONIC	NO. OF LINES	FUNCTION	ASSERTION LEVEL
a. DATA TRANSFER SECTION				
Address	A <17:00>	18	Selects slave device and/or memory address	Low
Data	D <15:00>	16	Information transfer	Low
Control	C0, C1	2	Type of data transfer	Low
Master Sync	MSYN	1	Timing control for data transfer	Low
Slave Sync	SSYN	1		Low
Parity	PA, PB	2	Device parity error	Low
Interrupt	INTR	1	Interrupt	Low
		<u>41</u>		
b. PRIORITY ARBITRATION SECTION				
Bus Request	BR4, BR5, BR6, BR7	4	Requests use of bus (usually for interrupt)	Low
Bus Grant	BG4, BG5, BG6, BG7	4	Grants use of bus (usually for interrupt)	High
Non-Processor Request	NPR	1	Requests use of bus for data transfer	Low
Non-Processor Grant	NPG	1	Grants use of bus for data transfers	High
Selection Acknowledge	SACK	1	Acknowledges grant	Low
Bus Busy	BBSY	1	Indicates that the data section is in use	Low
		<u>12</u>		

c. INITIALIZATION SECTION

Initialize	INIT	1	System reset	Low
AC Low	AC LO	1	Power monitoring	Low
DC Low	DC LO	1		Low
		<u>3</u>		

Figure 5-2 UNIBUS Signals

All transactions on the priority arbitration section and on the data transfer section are interlocked dialogs between devices. On the priority arbitration section, the devices are the requesting devices and the arbitrator. On the data transfer section, the devices are the bus master and the bus slave.

The signals that delimit data and priority arbitration operations are:

- a. Data Transfer: MSYN, SSYN, Interrupt: INTR, SSYN
- b. Priority Arbitration: [NPR, NPG] or [BRn, BGn], SACK, BBSY

5.5 DATA TRANSFER

5.5.1 Signals used in Data Transfer

Forty-one signal lines are used for data transfer. In a data transfer, one device is a bus master and controls the transfer of data to or from a slave device.

All signals in the Data Transfer Section are transmitted on type 1 lines.

DATA LINES, D <15:00>

The 16 data lines contain the word of information that is being transferred between the master and the slave devices. A word consists of two eight-bit bytes. The low order byte contains bits 00 through 07 and the high order byte, bits 08 through 15.

The bit format is shown in Figure 5-3.

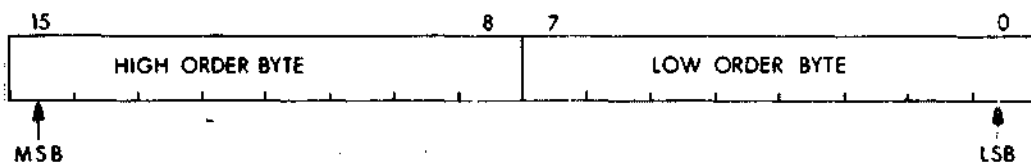


Figure 5-3 Format for Data Lines

ADDRESS LINES, A <17:00>

The 18 address lines carry the 18 A bits from the master during a data transfer transaction. These bits specify a location. The device which contains the specified location responds as the slave for this data transaction.

The address format is shown in Figure 5-4.

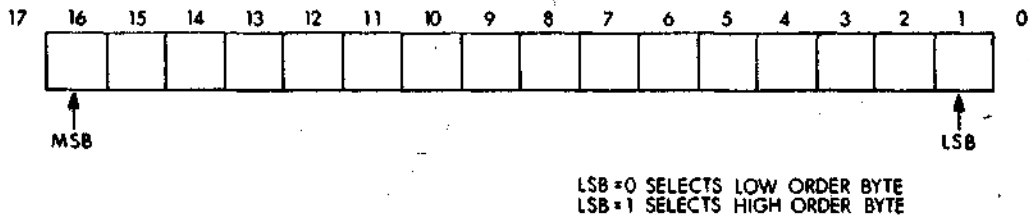


Figure 5-4 Format for Address Lines

The 17 address lines A <17:01> specify a unique location. All locations contain a 16 bit word which is at an even address. A byte is half of a word. In byte operations, bit A00 specifies which byte is being addressed. If a word is located at address X where X is even (i.e., its LSB = 0), the low order byte is addressed at X and the high order byte at X plus 1.

CONTROL LINES, C0, C1

These signals are sent by the master to the slave and indicate one of four possible data transfer operations:

NAME	MNEMONIC*	VALUE (C lines)		FUNCTION
		C1	C0	
Data In	DATI	0	0	One word of data from slave to master.
Data In, Pause	DATIP	0	1	Same as DATI, but Inhibits restore cycle in destructive read-out devices. Must be followed by DATO or DATOB to the same location.
Data Out	DATO	1	0	One word of data from master to slave.
Data Out, Byte	DATOB	1	1	One byte of data from master to slave Data transferred on: D <15:08> for A00 = 1 D <07:00> for A00 = 0

* The notations "DATI/P" and "DATO/B" are equivalent to "DATI or DATIP" and "DATO or DATOB."

The direction of data transfer is always specified with reference to the master device; data-in is from slave to master, and data-out is from master to slave.

DATA-IN TRANSACTIONS

The DATI and DATIP transactions request transfer of data from a slave to a master. Both transactions use the D lines to carry the data. These transactions are always a full word transfer, i.e., the slave places the data on D<15:00>. If the master wants only one byte, it must retrieve

the data from the proper lines: low-order byte from D<07:00>; high-order byte from D <15:08>. For these byte operations, the master should not assert, and the slave should ignore, bit A00.

DATIP TRANSACTION

The DATIP operation is identical to the DATI, except that DATIP informs the slave device that the present transfer is the first part of a read/modify/write cycle.

A pause flag is set in a destructive read-out device (e.g., core memory) which inhibits the restore cycle. The DATIP must be followed by a data-out cycle (DATO or DATOB) to the same word address.

Since address bit A00 may change between a DATIP and a DATOB, the slave must check the bus address at the beginning of the DATOB. The master must retain bus control until this DATO/B is completed, i.e.: it must remain bus master (assert BBSY) without interruption from the start of the DATIP cycle to the end of the DATO/B cycle. No other data transfer transaction may be executed between the DATIP and the DATO/B cycles.

In nondestructive readout devices (i.e., flip-flops), the DATI and DATIP are treated identically by the slave.

NOTE

In the case of locations which can be accessed by more than one UNIBUS or other bus (e.g.: the PDP-11/45 semiconductor memory), a DATIP on one bus must prevent the slave from responding on any other bus until the DATO/B cycle has been completed. This is necessary in order to avoid problems in multiple processor systems.

DATA-OUT TRANSACTIONS

The DATO and DATOB operations transfer data from the master to the slave. A DATO is used to transfer a word to the address specified by A <17:01>. The slave ignores A00 and the master places data on D <15:00>. A DATOB is used to transfer a byte of data to the address specified by A <17:00>. Line A00 = 0 indicates the low-order byte, and the master places the data on lines D <07:00>; A00 = 1 indicates the high order byte, and the master places the data on lines D <15:08>.

PARITY ERROR INDICATORS, PA, PB

PA and PB are generated by a slave and received by a master. They indicate parity error in a device. The slave negates PA and asserts PB to indicate a parity error on a DATI/P; PA and PB both negated indicates no parity error. PA asserted and PB asserted or negated are conditions reserved for future use. PA and PB are not defined in a DATO transaction. PA and PB may be used by the bus master's parity error logic.

The following table is a summary of the possible combinations of the parity error indicators.

PA	PB	
0	0	no error in a slave in DATI/P

0	1	error in slave in DATI/P
1	x	reserved

The protocol for PA and PB is the same as that for D<15:00>.

MASTER SYNC, MSYN

MSYN is a signal issued by a bus master and received by a slave. MSYN has two functions, depending on whether it is being asserted or negated.

ASSERTION OF MSYN

The assertion of MSYN requests that the slave that is defined by the A lines perform the function required by the C lines.

NEGATION OF MSYN

The negation of MSYN indicates to the slave that the master considers the data transfer concluded.

SLAVE SYNC, SSYN

SSYN is a signal issued by a slave and received by a master. SSYN has two functions, depending on whether it is being asserted or negated. It should be noted that, in an interrupt transaction, the interrupt processor is the slave and the interrupting device is the master.

ASSERTION OF SSYN

In a master-slave data transfer, the assertion of SSYN informs the bus master that the slave has concluded its part of the data transfer, i.e.: for a DATI or DATIP that the requested data has been put on the D lines, and for a DATO or DATOB that the data on the D lines has been accepted.

In an interrupt operation, SSYN is asserted by the processor. In this case, SSYN signifies that the interrupt vector has been accepted by the processor.

NEGATION OF SSYN

The negation of SSYN informs all bus devices that the slave has concluded the data transfer. In the case of a DATI/P the negation of SSYN signifies that the negation of MSYN has been received and the data removed from the D lines. In the case of a DATO/B the negation of SSYN means that the negation of MSYN has been received. In the case of an interrupt the negation of SSYN signifies that the negation of INTR has been received by the processor.

INTERRUPT REQUEST, INTR

INTR is a signal asserted by an interrupting device, after it becomes bus master, to inform the processor that an interrupt is to be performed and that the interrupt vector is present on the D lines.

INTR is negated upon receipt of the assertion of SSYN from the processor at the end of the transaction. INTR may only be asserted by a device which obtained bus mastership under the authority of a BG4, BG5, BG6 or BG7.

5.5.2 Conventions and Definitions

Signal Transmission

All UNIBUS signals are buffered by Transmitter and Receiver circuits before being used by any interfacing device. Most signals are bi-directional, having both a Transmitter and a Receiver within the same device. Figure 5-5 shows a typical signal. Note that within the same device, a bi-directional signal appears in two different physical places, at the input of a Transmitter and at the output of a Receiver. All UNIBUS signals mentioned in this chapter will imply reference within the Transmitter/Receiver device interface, and signals will be differentiated by:

(T) = transmitted signal (at input of Transmitter)
(R) = received signal (at output of Receiver)

Levels

A signal, such as MSYN, will be considered activated when asserted. For simplicity, timing waveforms will be shown for logic levels, rather than voltage levels. The higher level will correspond to the assertion level, and the lower level will be the cleared level.

Asserted = Logic 1 = TRUE = higher level
Cleared = Logic 0 = FALSE = lower level = (negation)

Skew

When two separate signals are sent from one device to another device starting at the same time, there can be a time difference in the receipt of these signals by the second device, even if similar circuitry and transmission medium are used. This time difference (or time uncertainty) is called skew. It is guaranteed to be less than 75 nsec for the UNIBUS. Figure 5-6 shows an example.

If signals A & B represent 2 Data lines on the UNIBUS, there could be a maximum time difference (skew) of 75 nsec in the receipt of these signals. Signal A could precede signal B by 75 nsec, or it could arrive later than B by 75 nsec.

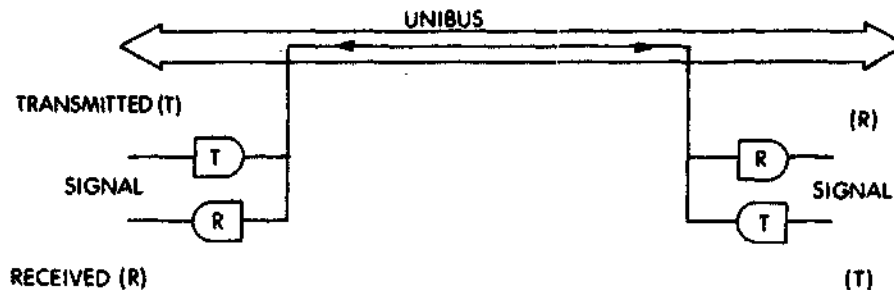


Figure 5-5 Bi-directional Signal

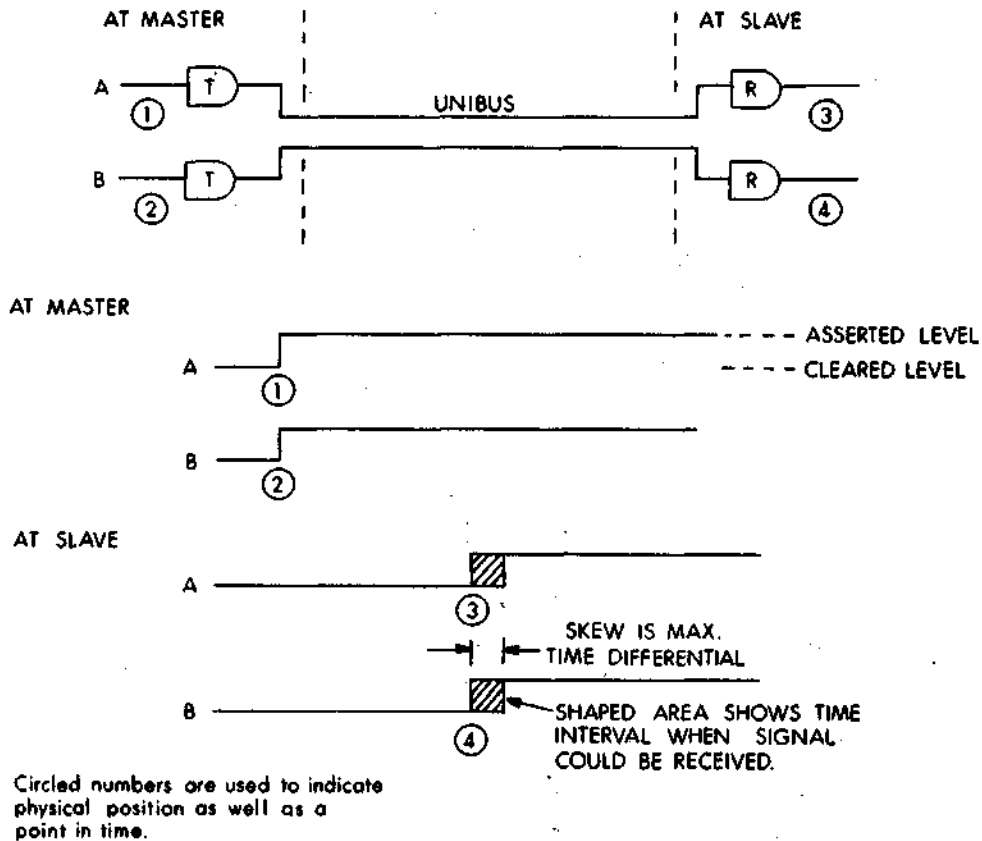


Figure 5-6 Example of Skew

5.5.3 Equivalent Logic at the Slave

To allow asynchronous data transfer between master and slave, 2 inter-dependent timing signals are used, MSYN and SSYN. Simplified, equivalent logic at the slave interface to the UNIBUS is shown in Figure 5-7.

The sequence of events is:

1. Address, Control, (and Data) are sent from the master.
2. After a delay, to make sure lines have settled and address decoding has been performed, MSYN is sent. MSYN is a gating (or strobing) signal for the Address and Control lines. It is always cleared before Address and Control are changed.
3. SSYN is the acknowledging response to MSYN and means that
 - (a) Address has been recognized by a device register (or memory), and
 - (b) The action requested has been performed; data has been accepted or data has been placed on the UNIBUS.

The logic shows 2-input AND gates and D-type flip-flops. The information present on the D (data) input is stored in the flip-flop when the C (clock) input is activated.

Single lines have been shown for the different groups of signals (A,C, & D) to simplify the diagram.

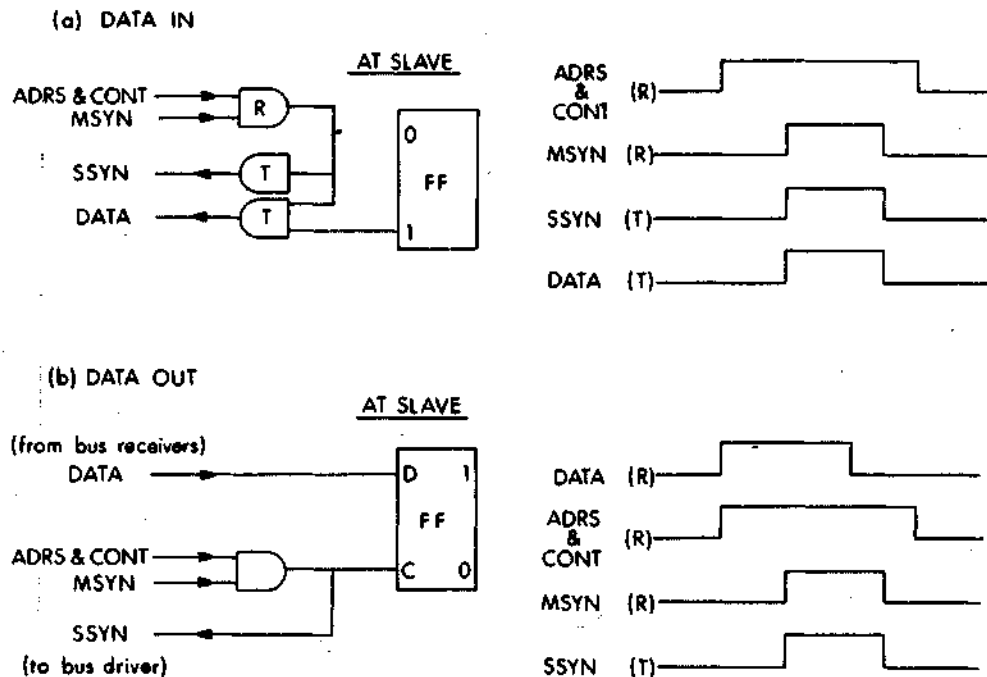


Figure 5-7 Simplified Slave Logic

5.5.4 Data Transfer Timing

The design of the UNIBUS imposes certain timing restrictions although transfers are interlocked. Responsibility for these timing restrictions has been assigned to the master to simplify the slave design.

In all transfers, it is assumed that there can be a maximum 75-ns skew due to driver, receiver, and transmission line tolerances. In other words, the coincident assertion of two lines at the transmitter inputs of one device could result in a maximum difference of 75-ns in the occurrence of those signals at the receiver outputs in another device.

Because of this possible skew, the master always delays its MSYN signal to ensure that MSYN does not reach the slave device prior to valid data or addresses. In addition, the MSYN signal is further delayed to allow 75 ns for decoding by the slave device. The master also must not drop the A (address) or C (control) lines until 75 ns after MSYN has been dropped to guarantee that there are no spurious selections. Note, however, that when a slave transmits data to a master (DATI or DATIP), the deskew and decode time delay must be made by the master.

5.5.5 DATA-IN, DATI OR DATIP

General Description, Data-In Transaction

Data-In is defined as a data transfer from a slave to a master. DATI and DATIP are similar data-in operations.

The selected slave, after receiving the assertion of MSYN, places the requested data on the D lines and asserts SSYN.

The master deskews the D lines after receiving the assertion of SSYN, strobes the data, and negates MSYN.

The receipt of the negation of MSYN informs the slave that the master has accepted the data. The slave then removes the data from the D lines and negates SSYN. This ends the slave's part of the data transfer cycle.

The master, after negating MSYN, deskews the A and C lines. This ensures that the negation of MSYN is received by all devices before the A and C lines become invalid, and thus prevents false selection by another device. After the deskew, the master ends its part of the data transfer by removing the address and control bits from the A and C lines.

If the master is not going to use the bus for another data transfer at this time, it negates BBSY. This releases the data section of the bus for possible use by another device. If there is to be another transfer (e.g.: a DATO or DATOB after a DATIP), BBSY is held asserted by the current master.

Detailed Description, DATI and DATIP

The numbers of the steps in this paragraph correspond to the numbers on timing diagram, Figure 5-9.

1. The bus master (BBSY asserted) puts the address and the control bits on their respective UNIBUS lines.
2. After a propagation delay, each device on the bus receives the address and control bits, and decodes them.
3. The master waits for at least 150 nanoseconds after putting the address and control bits on the A and C lines (front-end deskew); then, if SSYN is negated, it asserts MSYN. This means that the master must not assert MSYN at the driver input until 150 nanoseconds have elapsed since the A, C and enable lines have become valid at the A and C driver inputs.

NOTE

The front-end deskew consists of 75 nanoseconds to compensate for the skew of the A and C lines at the slave, plus 75 nanoseconds to allow the slave to decode these lines.

4. After a propagation delay, each device on the bus receives the assertion of MSYN. One of them has decided, after having decoded the address, that it is the slave for this transaction.
5. Some time after receiving the assertion of MSYN, the slave puts the requested data on the D lines, then asserts SSYN. This means that the slave must not assert SSYN at the driver input before the data and enable lines are valid at the D driver inputs.

NOTE

SSYN must not be asserted before the data is put on the D lines. This is to insure that the master will be able to deskew the data with respect to SSYN and then strobe it while it is valid.

6. After a propagation delay, the assertion of SSYN arrives at the master.

NOTE 1

If the assertion of SSYN is not received by the master during a specified time after its assertion of MSYN (timeout delay), step 7 below may be executed, and steps 8 and 9 must be executed by the master. An error bit may be set.

NOTE 2

The timeout delay is typically 10 to 20 microseconds in processors. The use of some devices (e.g.: bus window, DL10) requires much longer times which can be up to several hundreds of microseconds. These devices are used in multi-processor or multi-bus systems.

7. After waiting for at least 75 nanoseconds after the receipt of the assertion of SSYN (data deskew) the master strobes in the data.

NOTE

The data deskew compensates for the skew of the D lines at the master.

8. The master negates MSYN.
9. After a 75 nanosecond minimum wait, called tail-end deskew, the master removes the address and control bits from the A and C lines. If this is the last data transfer under the current grant, the master then negates BBSY.

NOTE

The tail-end deskew guarantees that the A lines will not change at any bus device while the device is receiving the assertion of MSYN. This prevents false selection of a device due to changing A lines while MSYN is asserted.

10. After a propagation delay, the slave receives the negation of MSYN.
11. The slave removes the data from the D lines, and then negates SSYN.

NOTE

SSYN must not be negated before the data is removed from the D lines. This ensures that the negation of SSYN is a valid indication of the fact that the data bits have been removed from the D lines.

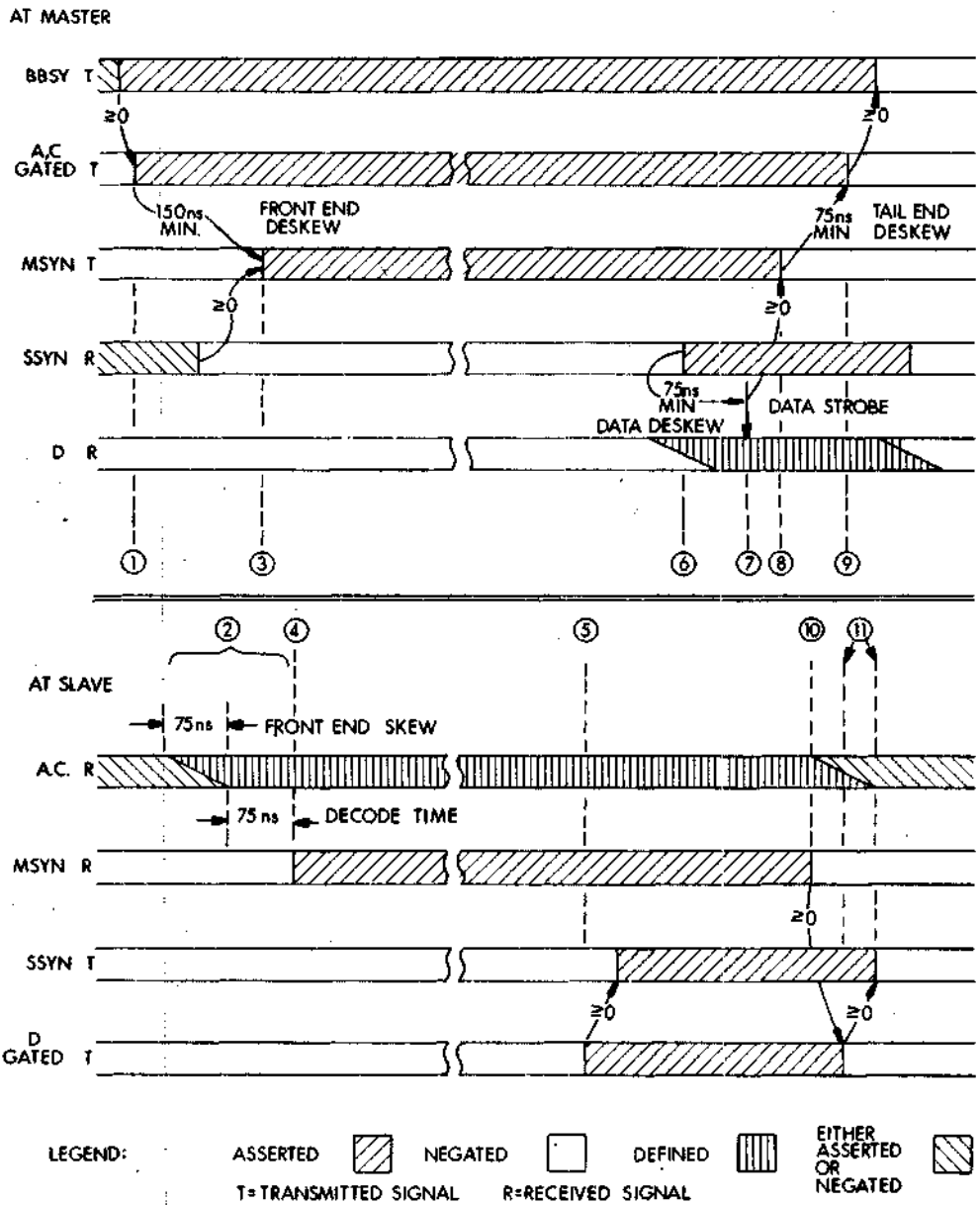


Figure 5-9 Typical DATI Transaction

5.5.6 DATA-OUT, DATO OR DATOB

General Description, Data-Out Transaction

Data out is defined as a data transfer from a master to a slave. DATO and DATOB are Data-Out operations. The timing and protocol for both of these operations is identical.

Figure 5-10 shows the interaction between master and slave for a typical DATO or DATOB. A bus master (BBSY asserted) places the slave address, the required control bits and the data on the A, C and D UNIBUS lines. All devices decode A and C to see if they are selected as the slave for this transaction.

The master asserts MSYN after two conditions are met:

- An appropriate delay is allowed for deskewing of the A, C and D lines, and for address and control decoding by the slave.
- An appropriate delay is allowed after the receipt of the negation of SSYN, to ensure that the previous slave is no longer driving the D lines.

The device selected as slave, after receiving the assertion of MSYN, strobes the data on the D lines and asserts SSYN.

The master, after receiving the assertion of SSYN, negates MSYN, then deskews the A and C lines. This ensures that the negation of MSYN is

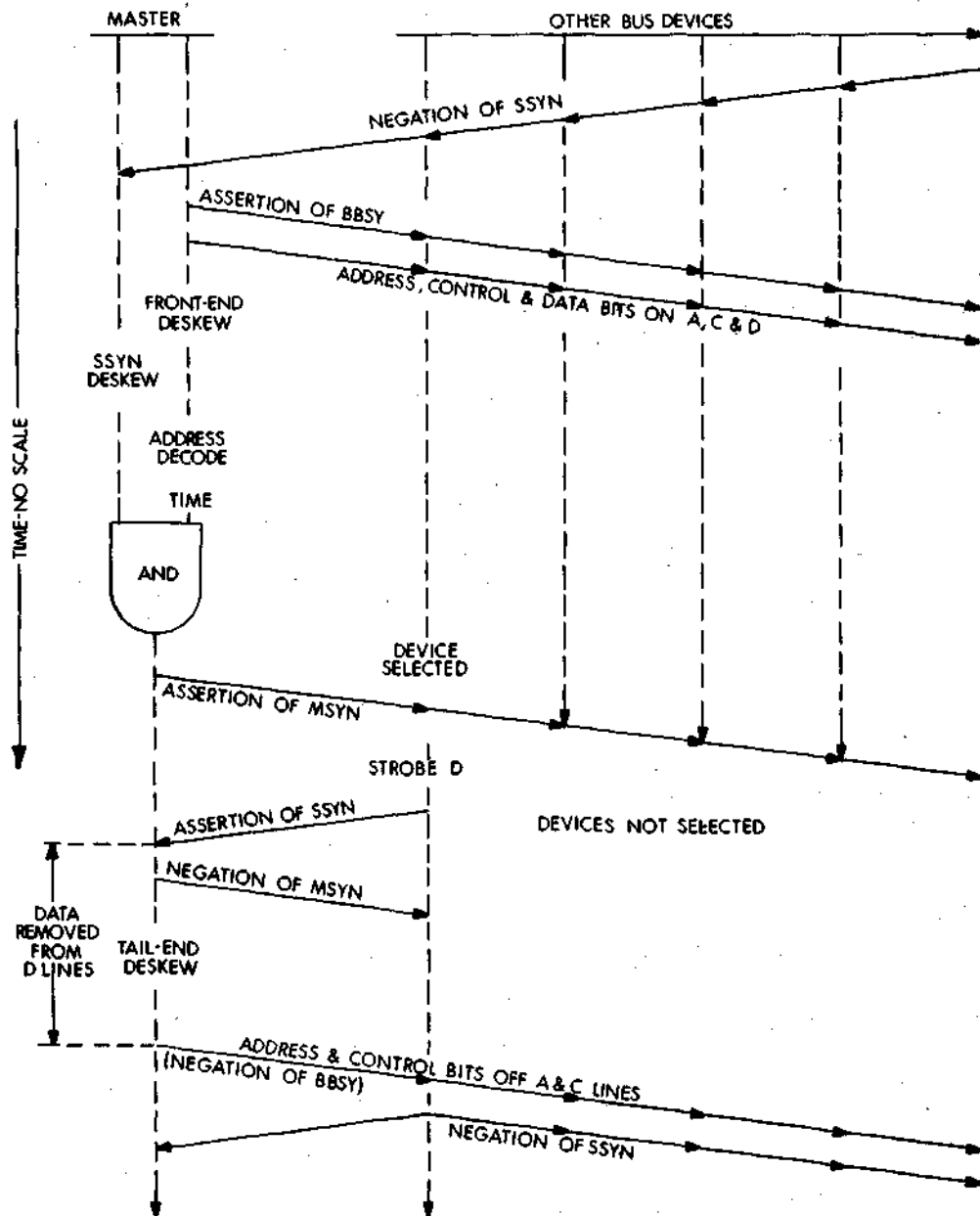


Figure 5-10 Typical DATO or DATOB cycle

received by all devices before the A and C lines lose their validity, and thus prevents false selection by another device. After the deskew, the master ends its part of the data transfer by removing address and control bits from the A and C lines.

Data may be removed from the D lines by the master at any time after its receipt of the assertion of SSYN, but no later than its removal of the address and control bits from the A and C lines.

The slave, upon receipt of the negation of MSYN, ends its part of the data transfer cycle by negating SSYN.

If the master is not going to use the bus for another data transfer after removing the address and control bits from the A and C lines, it then negates BBSY. This releases the data section of the bus for possible use by another device. If there is to be another transfer, BBSY is held asserted by the current master.

Detailed Description, DATO and DATOB

The numbers of the steps in this paragraph correspond to the numbers on timing diagram, Figure 5-11.

1. The bus master (BBSY asserted) puts the address, control, and data bits on their respective UNIBUS lines.
2. After a propagation delay, each device on the bus receives the address and control bits, and decodes them.
3. After putting the address, control and data bits on the A, C and D lines, the master waits for at least 150 nanoseconds (front end deskew). This means that the master must not assert MSYN at the driver input until 150 nanoseconds have elapsed since the A, C, D and enable lines have become valid at the A, C and D driver inputs. See Note 1, step 5.
4. The master waits for a minimum of 150 nanoseconds after receiving the negation of SSYN (SSYN deskew). See Note 2, step 5.
5. After the conditions in steps 3 and 4 above have been met, the master asserts MSYN.

NOTE 1

The front-end deskew consists of 75 nanoseconds to compensate for the skew of the A and C lines at the slave, plus 75 nanoseconds to allow the slave to decode these lines.

NOTE 2

The 150 nanosecond SSYN deskew consists of: (1) 75 nanoseconds to ensure that the data from a previous DATI or DATIP transaction has been removed from the D lines and (2) 75 nanoseconds to allow set-up time for such devices as may require it.

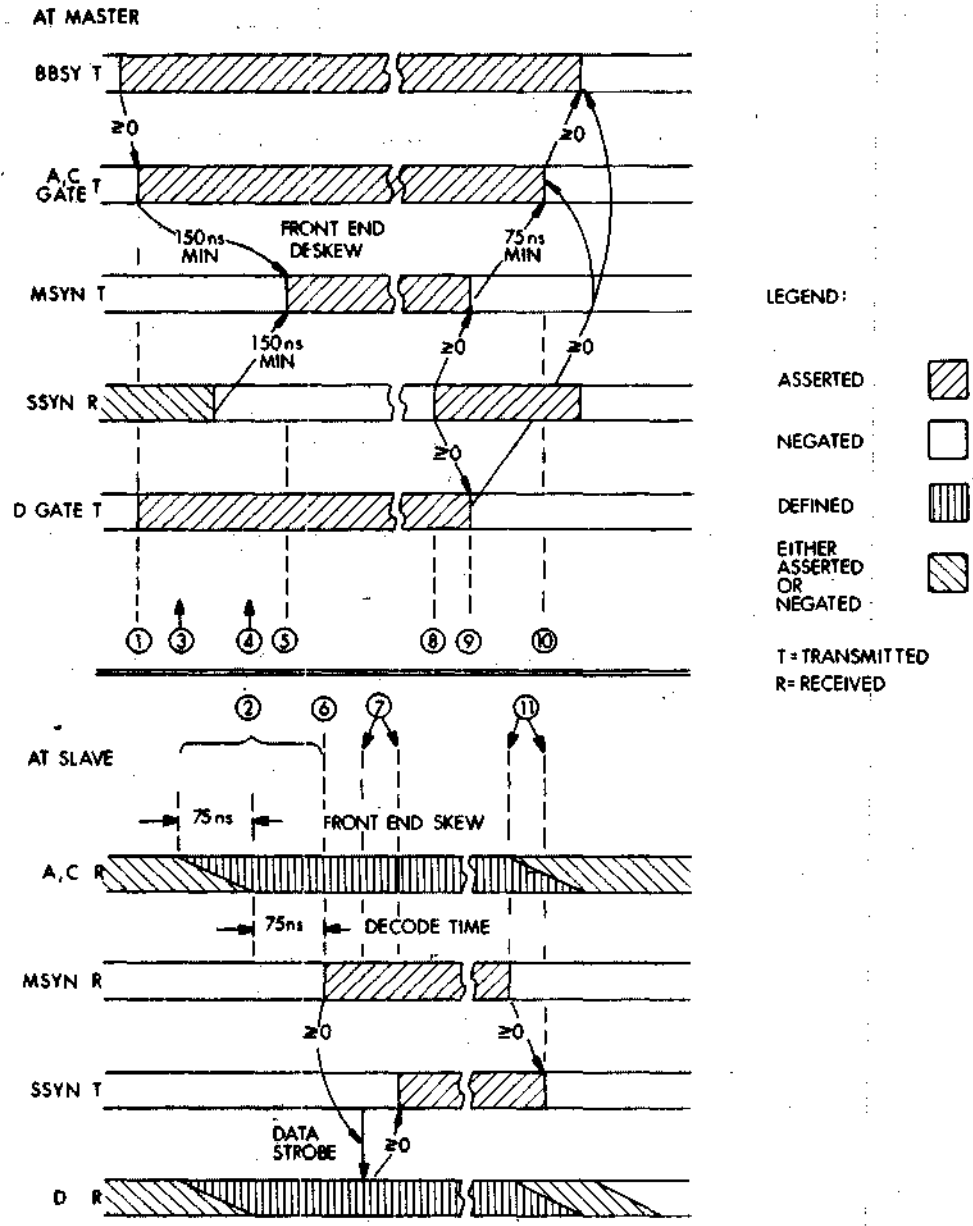


Figure 5-11 Typical DATO Transaction

6. After a propagation delay, each device on the bus receives the assertion of MSYN. One of them has decided, after having decoded the address, that it is the slave for this transaction.
7. Upon receiving the assertion of MSYN, the slave strobbs the data from the D lines and asserts SSYN.

NOTE

The data must be strobed by the slave either at the same time as, or previous to, the assertion of SSYN. This is required because the master may remove the data from the D lines upon receipt of the assertion of SSYN.

8. After a propagation delay, the master receives the assertion of SSYN.

NOTE 1

If the assertion of SSYN is not received by the master during a specified time after its assertion of MSYN (timeout delay), the steps that follow are executed and an error bit may be set.

NOTE 2

The timeout delay is typically 10 to 20 microseconds in processors. The use of some devices (e.g.: bus window DL10) require much longer times which can be up to several hundreds of microseconds. These devices are used in multi-processor or multi-bus systems.

9. Upon receipt of the assertion of SSYN, the master negates MSYN, and may remove the data from the D lines.
10. After a 75 nanosecond minimum wait, called tail-end deskew, the master removes the address and control bits from the A and C lines. If this is the last transfer under the current grant, the master then negates BBSY. If the data has not previously been removed from the D lines, it must be removed: (a) if another transfer will be done under the current grant, no later than the removal of the A and C bits from the bus, or, (b) if this is the last transfer under the current grant, before the negation of BBSY.

NOTE

The tail-end deskew guarantees that the A lines will not change at any bus-device while the device is receiving the assertion of MSYN. This prevents false selection of a device due to changing A lines while MSYN is asserted.

11. After a propagation delay, the slave receives the negation of MSYN and then negates SSYN.

5.6 PRIORITY ARBITRATION TRANSACTIONS

5.6.1 Introduction

It is assumed in all the descriptions in Section 5.6 that the arbitrator is allowed to issue a grant of the level at which the request is made. This implies: (1) that no device request having a priority level higher than the level of the request under consideration is present at the arbitrator, and (2) that the present priority level of the interrupt fielding processor is lower than the priority level of the request under consideration.

General Description

Refer to Figure 5-12, Typical Arbitration Sequence. At the start (top) of the diagram, device 1, having been granted the use of the data section of the bus, asserts RBSY and becomes bus master. After a time, device 1 negates SACK. The arbitrator is enabled when it receives the negation

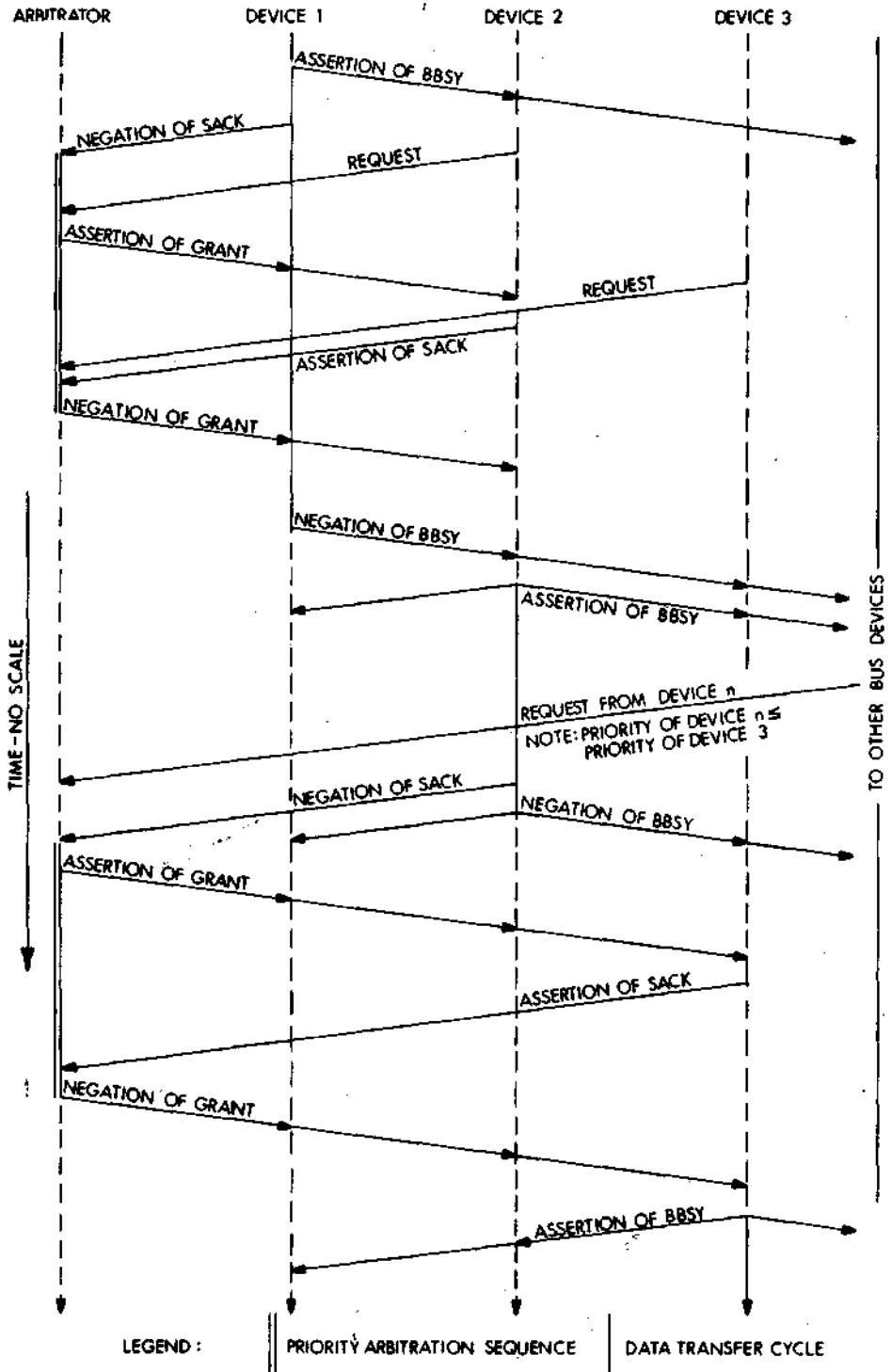


Figure 5-12 Typical Arbitration Sequence

of SACK, and a new priority arbitration sequence starts. When the request from device 2 reaches the arbitrator, a grant of the same priority level as the request is asserted. The assertion of this grant disables the

arbitrator, and the request from device 3 is ignored. Device 2 acknowledges the grant by asserting SACK, Receipt of the assertion of SACK keeps the arbitrator disabled. Device 2 is now designated as next bus master.

The arbitrator acknowledges the receipt of the assertion of SACK by negating the grant. This action signals the end of the arbitration sequence.

Device 1 ends its data transfer and relinquishes the bus by negating BBSY.

As soon as device 2 has received the negation of BBSY, device 2 becomes bus master, asserts BBSY, and starts its data transfer cycle.

Requests are not honored by the arbitrator while a grant is asserted, nor while the assertion of SACK is seen at the arbitrator. The request from Device 3 is an example of the first case. The request from Device N illustrates the second case, because device 2 waited too long before negating SACK.

A priority arbitration sequence may or may not occur at the same time as a data transfer cycle. In the case of devices 1 and 2 above, it does. The arbitration sequence for device 3, however, does not start until the data transfer by device 2 is almost ended.

All UNIBUS signals used in the above sequence are transmitted on type 1 lines, with the exception of the grants, which are transmitted on type 2 lines. Thus, a grant asserted by the arbitrator is received by the first device on the bus wired to this particular grant line. If this device requires the use of the data section of the bus at this time, it blocks the grant and asserts SACK. If the device does not require the use of the data section of the bus upon receipt of the assertion of a grant. It asserts (passes) the grant, which is then received by the next device of the same priority level on the bus. A device may not accept a grant (assert SACK) after it has passed the grant.

5.6.2 Detailed Description, Priority Arbitration Transactions Preliminary Conditions

The arbitrator responds to signals from bus devices requesting the use of the data section of the UNIBUS, and to enabling signals from the interrupt fielding processor.

The processor prohibits the arbitrator from issuing BGs during an interrupt transaction and for such time after this transaction that the processor is determining its new priority level. The processor cannot service, and the arbitrator may not grant, any more BGs until the processor has established what this new level is and saved the old level. This sequence typically requires four bus cycles, after which the arbitrator is again allowed to grant BGs at a level higher than that of the new processor level.

The "Grant Status" lines on the timing diagrams show which types of grants may be issued by the arbitrator at any given time during the arbitration sequence.

5.6.3 Detailed Description, NPR Arbitration Sequence

The numbers of the steps in this paragraph correspond to the numbers on timing diagram, Figure 5-13.

1. The requesting device asserts NPR.
2. After a propagation delay, the assertion of NPR is received by the arbitrator.
3. If the negation of SACK from the previous priority arbitration sequence has been received by the arbitrator for at least 75 nanoseconds, the arbitrator asserts NPG and the arbitration process is stopped.

NOTE 1

No grants may be issued by the arbitrator while SACK is asserted, and for a minimum of 75 nanoseconds after receipt of the negation of SACK.

The delay ensures that the negation of NPR or BR from the previous arbitration sequence has arrived at the arbitrator before arbitration is resumed. This prevents the issue of a grant in response to the request from the previous arbitration sequence in the case that the request is negated at the same time as SACK. See step 5.

In the case of a single word transfer, the master typically negates SACK immediately after asserting BBSY. The SACK delay ensures, in this case, that the assertion of BBSY is sensed before the negation of SACK. This prevents the processor from asserting BBSY upon seeing the bus free.

NOTE 2

No other grant (NPG or BG) may be issued by the arbitrator while an NPG is asserted.

4. After a propagation delay, NPG is received at the requesting device.
5. The requesting device then asserts SACK. In the case of a single word transfer, NPR must be negated by the requesting device after the assertion of SACK, but before SACK is negated. If another transfer is required after the current one, NPR may remain asserted.
6. After a propagation delay, the assertion of SACK is received at the arbitrator.

NOTE 1

If the assertion of SACK is not received by the arbitrator during a specified time after its assertion of NPG (timeout delay), NPG is negated and arbitration resumes. The timeout delay is typically 5 to 10 microseconds.

NOTE 2

Systems may avoid the timeout delay by having, at the end of the bus opposite to the arbitrator, a terminator that asserts SACK if it receives the assertion of NPG.

The arbitrator upon receipt of the assertion of SACK, negates NPG. The negation of NPG is propagated along the bus to the terminator, which negates SACK upon receipt of the negation of NPG. Steps 11 and 12 below are then executed.

7. The arbitrator then negates NPG.
8. After a propagation delay, the requesting device receives the negation of NPG.
9. After receiving the negation of BBSY the requesting device asserts BBSY. The requesting device becomes bus master at the time of its assertion of BBSY, and starts its data transfer cycle(s).

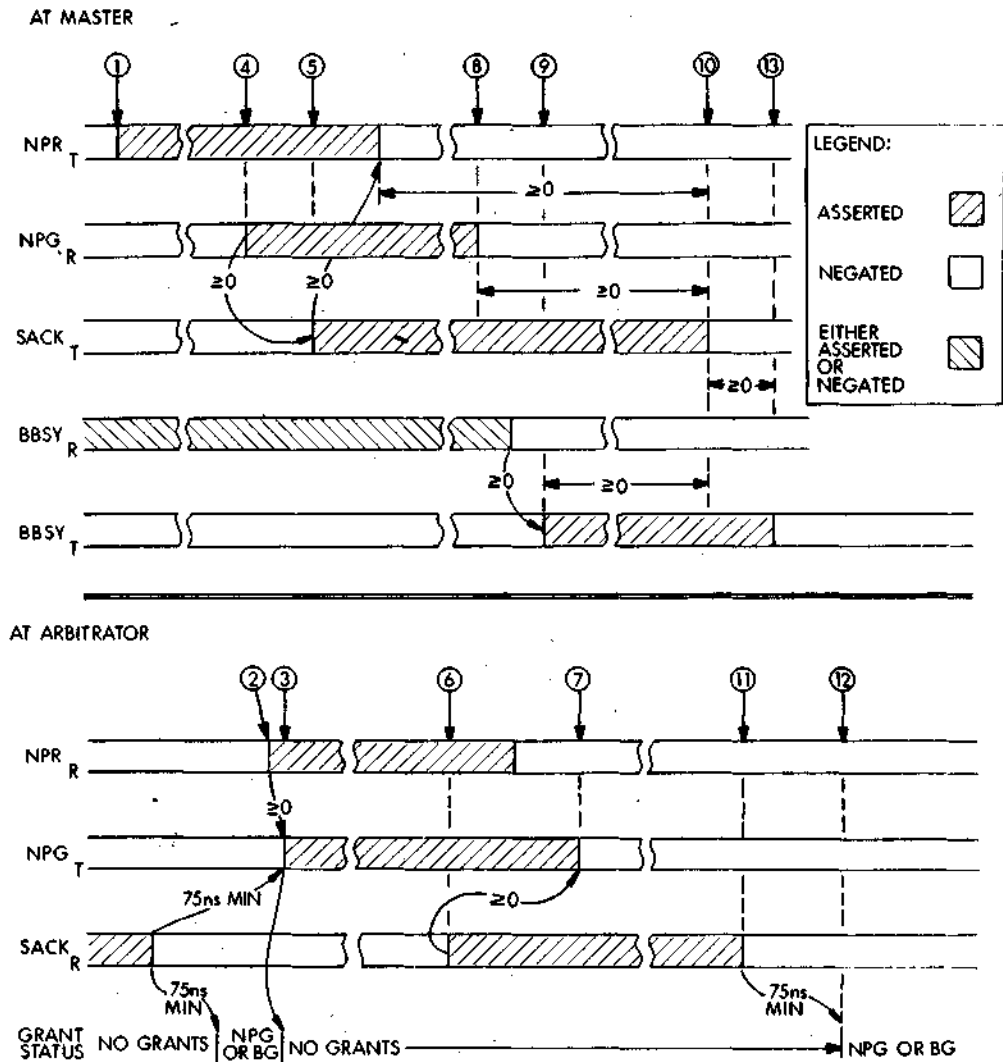


Figure 5-13 Typical NPR Arbitration Sequence

10. After it has asserted BBSY and at some time before it has finished transferring data, the bus master may negate SACK, if it has received the negation of BGn.

NOTE 1

If a single word transfer is intended, a device typically asserts BBSY and negates SACK at the same time.

NOTE 2

The master must not negate SACK prior to its receipt of the negation of NPG. This provides the interlock that ensures that the arbitrator has received the assertion of SACK.

11. After a propagation delay, the arbitrator receives the negation of SACK.
12. The arbitrator waits a minimum of 75 nanoseconds, then resumes arbitration. See Note 1, step 3.
13. At the end of its last data transfer cycle, the master waits at least 75 nanoseconds after negating MSYN, then removes any A, C, D, bits it has put on the bus. It then negates BBSY, thus releasing the bus. SACK must be negated before BBSY may be negated.

5.6.4 General Description, Interrupt Transaction

A bus master that has obtained control of the data section of the UNIBUS through a BRn-BGn arbitration transaction may issue an interrupt command to the processor. This forces entry into a sub-program whose vector is given to the processor by the bus master. The vector is asserted on the D lines.

Figure 5-14 shows the interaction between master, processor, and arbitrator for a typical interrupt transaction. A bus master puts the vector on the D lines and, if SSYN is negated, asserts INTR and negates SACK if BGn is negated.

The processor, upon receipt of the assertion of INTR, delays to deskew the D lines, then strobes the vector and asserts SSYN.

Upon receipt of the assertion of SSYN, the master removes the vector from the D lines and negates INTR and BBSY.

When the processor receives the negation of INTR, it negates SSYN.

Upon receipt of the assertion of INTR, the arbitrator ceases to issue BGs. It grants no BGs until authorized to do so by the processor. NPGs, however, may be granted during this time.

5.6.5 Detailed Description, BR Interrupt Arbitration Sequence

The numbers of the steps in this paragraph correspond to the numbers on timing diagram, Figure 5-15.

1. The requesting device asserts BRn.

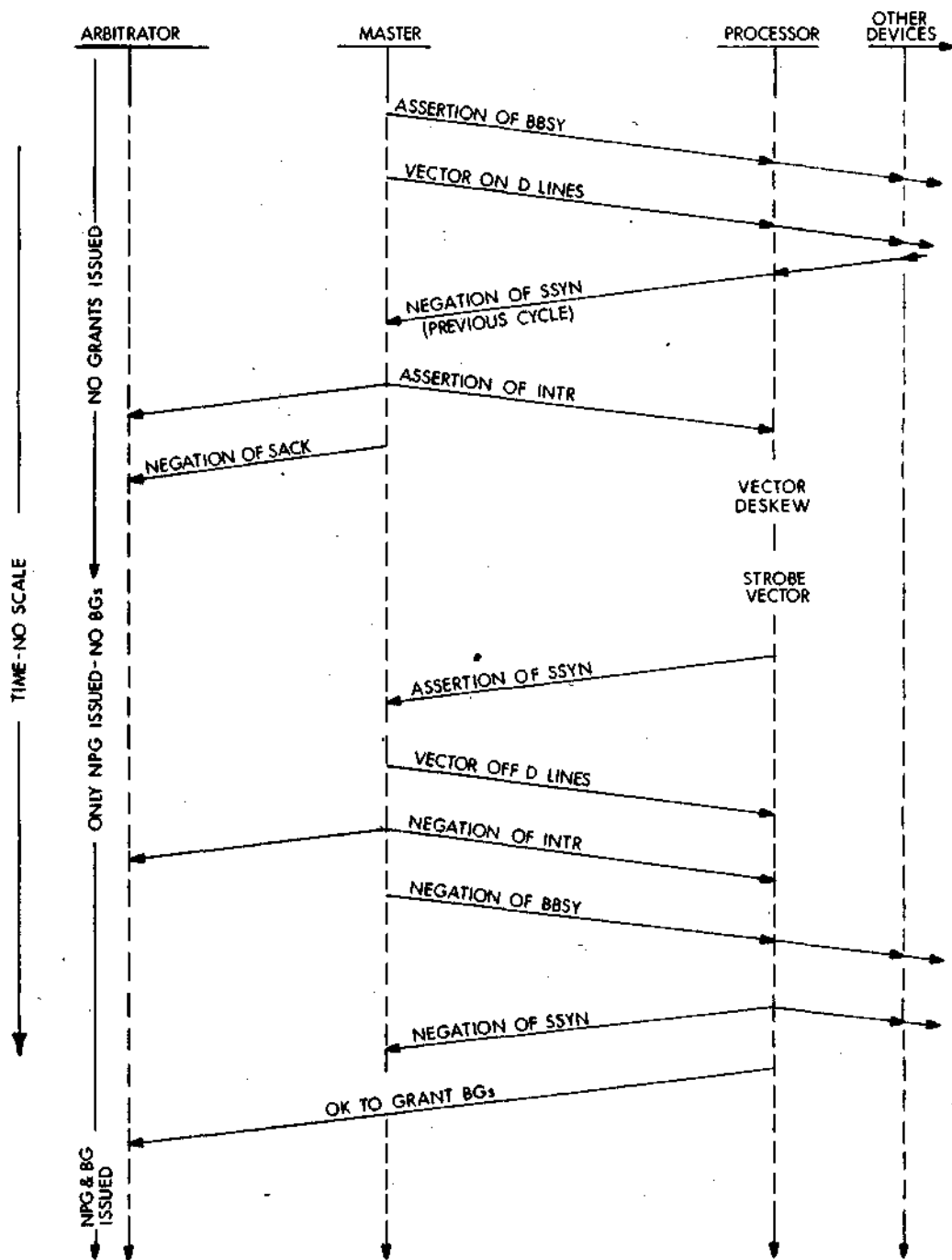


Figure 5-14 Typical INTR Cycle Diagram

2. After a propagation delay, the assertion of BRn is received by the arbitrator.
3. If the negation of SACK from the previous priority arbitration sequence has been received by the arbitrator for at least 75 nanoseconds and if the processor is ready to accept an interrupt vector at the level of the interrupting device, the arbitrator asserts BGr and the arbitration process is stopped.

NOTE 1

No grants may be issued by the arbitrator while SACK is asserted, and for a minimum of 75 nanoseconds after receipt of the negation of SACK.

The delay ensures that the negation of NPR or BR from the previous arbitration sequence has arrived at the arbitrator before arbitration is resumed. This prevents the issue of a grant in response to the request from the previous arbitration sequence in the case that the request is negated at the same time as SACK. See step 5.

In the case of a single word transfer, the master typically negates SACK immediately after asserting BBSY. The SACK delay ensures, in this case, that the assertion of BBSY is sensed before the negation of SACK. This prevents the processor from asserting BBSY upon seeing the bus free.

NOTE 2

No other grant (NPG or BG) may be issued by the arbitrator while a BG is asserted.

4. After a propagation delay, BGn is received at the requesting device.
5. The requesting device then asserts SACK. In the case of a single transaction, BRn must be negated by the requesting device after the assertion of SACK, but before SACK is negated. If another transaction is required after the current one, BRn may remain asserted.
6. After a propagation delay, the assertion of SACK is received at the arbitrator.

NOTE 1

If the assertion of SACK is not received by the arbitrator during a specified time after its assertion of BGn (timeout delay), BGn is negated and arbitration resumes. The timeout delay is typically 5 to 10 microseconds.

NOTE 2

Systems may avoid the timeout delay by having, at the end of the bus opposite to the arbitrator, a terminator that asserts SACK if it receives the assertion of BGn. The arbitrator, upon receipt of the assertion of SACK, negates BGn. The negation of BGn is propagated along the bus to the terminator, which negates SACK upon receipt of the negation of BGn. Steps 11 and 12 of Section 5.6.3 (NPR Sequence) are then executed.

7. The arbitrator then negates BGn.
8. After a propagation delay, the requesting device receives the negation of BGn.
9. The requesting device, after receiving the negation of BBSY, asserts BBSY. The requesting device becomes bus master at the time of its assertion of BBSY.
10. The bus master, which must have been granted the use of the data section of the UNIBUS by a BG but not by an NPG, puts the interrupt vector on the D lines.
11. After the master receives the negation of SSYN (which is typically already negated), it asserts INTR. After the master has asserted INTR and received the negation of BGn it negates SACK.

NOTE 1

INTR must be asserted before SACK is negated to ensure receipt of the assertion of INTR before the end of the SACK delay at the arbitrator. The SACK delay compensates for skew between INTR and SACK at the arbitrator.

NOTE 2

The master must not negate SACK prior to its receipt of the negation of BGn. This provides the interlock that ensures that the arbitrator has received the assertion of SACK.

NOTE 3

The master may already have negated INTR or BBSY (step 16 below) by the time it receives the negation of BGn (not typical, but possible). In this case, the master negates SACK when the negation of BGn is received.

12. After a propagation delay, the arbitrator and the processor receive the assertion of INTR.
13. The processor waits for at least 75 nanoseconds (vector deskew), then strobes the vector from the D lines.

NOTE

The vector deskew compensates for the skew between INTR and the D lines at the processor.

14. The processor asserts SSYN.
15. After a propagation delay, the master receives the assertion of SSYN.
16. The master then removes the vector from the D lines and then negates INTR. The master then typically negates BBSY. This constitutes active release of the data section of the bus by the master.

17. After a propagation delay, the arbitrator and the processor receive the negation of INTR.
18. The processor then negates SSYN.
19. After receiving the negation of SACK (step 11 above), the arbitrator waits for 75 nanoseconds (SACK delay), then may resume issuing NPGs, but not BGs.

NOTE

Typically, the processor reads a new program counter and status word from the memory locations designated by the interrupt vector. This is done immediately following the interrupt transaction. From this the processor determines its new priority level.

20. The processor informs the arbitrator that it may start issuing BGs.

NOTE 1

Data may be transferred by a device that has become bus master through a BR_n-BG_n sequence. In this case, the procedure is the same as that described for NPR in Section 5.6.3.

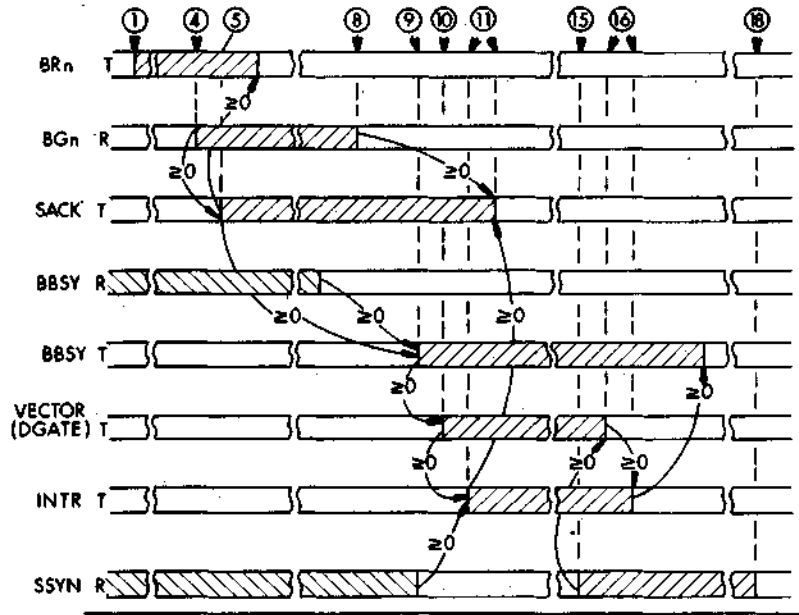
NOTE 2

A master may only execute one INTR transaction per BG.

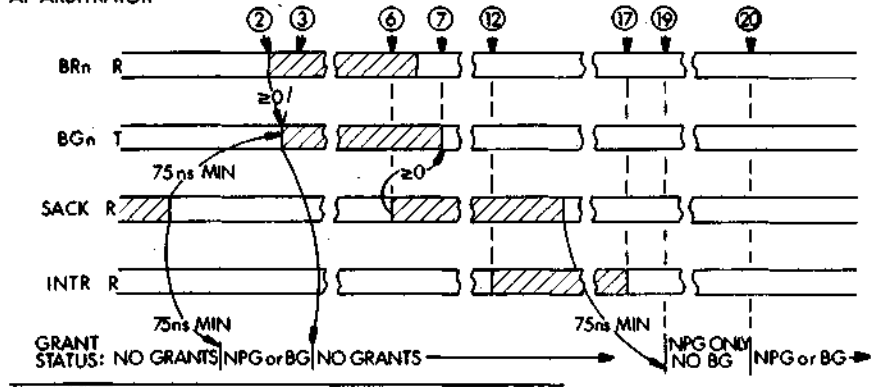
NOTE 3

If a master does data transfer(s) but no interrupt transaction under the authority of a BG, then releases the data section, this release constitutes passive release of the data section of the bus.

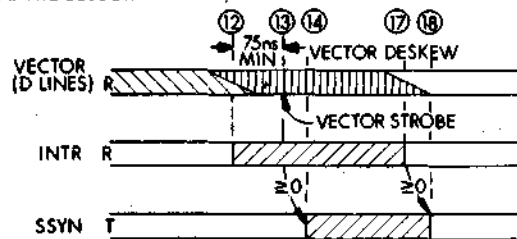
AT REQUESTING DEVICE:



AT ARBITRATOR



AT PROCESSOR



LEGEND

- ASSERTED
- NEGATED
- DEFINED
- EITHER ASSERTED OR NEGATED
- T=TRANSMIT, R=RECEIVE

Figure 5-15 Typical Interrupt Transaction

5.7 MISCELLANEOUS CONTROL LINES

There are three additional lines on the UNIBUS which may be used by all devices. These lines are: Initialize, AC low, and DC low:

INIT

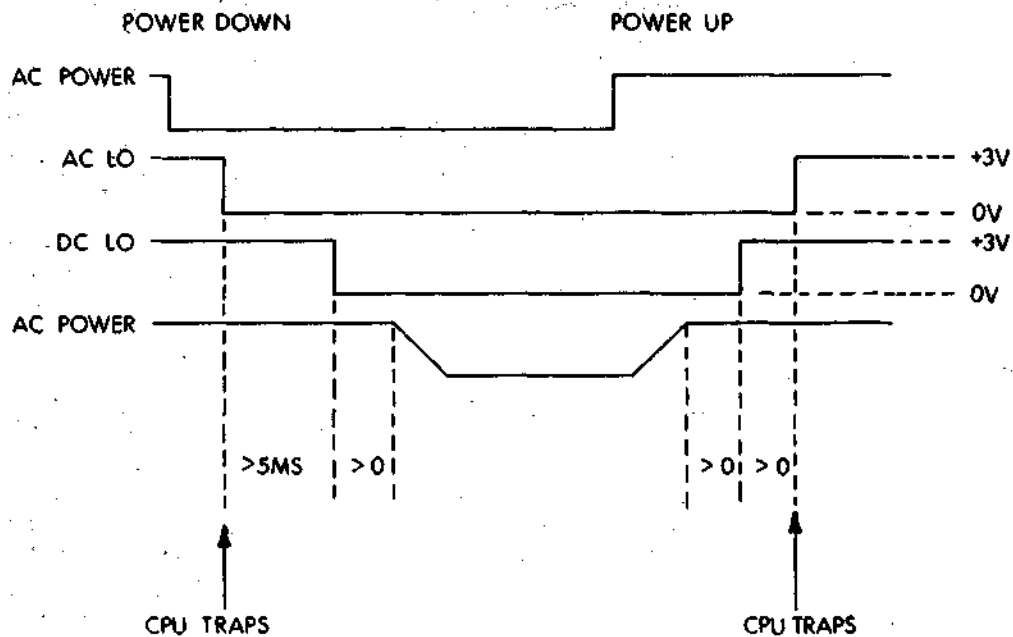
Initialize. This signal is asserted by the processor when the START key on the console is depressed, when a RESET instruction is executed, or when the power fail sequence occurs. In the latter case, INIT is asserted following the

power fail service routine while power is going down, and again when power comes up. INIT may also be used to clear and initialize all peripheral devices at the same time by means of the RESET instruction.

AC LO AC Line Low. This is an anticipatory signal which starts the power fail trap sequence, and may also be used in peripheral devices to terminate operations in preparation for power loss. When AC LO is cleared, the power up instruction sequence in the processor begins. It is the programmer's responsibility to make certain that the trap vector is loaded with a pointer to the power fail routine. If this is not done, an undefined sequence results.

DC LO DC Line Low. This signal, which emanates from the power supply, is available to all System Units on the UNIBUS. Each power supply must furnish both AC LO and DC LO signals, and be able to hold these lines at ground (less than 0.8 volts) when power is off to that supply, even if other equipment tries to pull up the lines. This signal remains cleared as long as all dc voltages are within specified limits. If an out-of-voltage condition occurs, DC LO is asserted by the power supply. Devices such as core memories use the DC LO signal to inhibit further operations. The DC LO signal is normally cleared before AC LO when power is coming up and is asserted after AC LO when power is going down. Note that the power fail trap is initiated by AC LO only and that the DC LO signal is used by the processor to cause INIT on the bus.

Refer to Figure 5-16.



NOTE: 5 msec is needed between the AC LO and DC LO signals on Power Down to guarantee the program 2 msec of running time.

Figure 5-16 Power Fail Sequence

5.8 UNIBUS

5.8.1 Timing

Although all bits of an information signal are transmitted simultaneously, differences in bus path lengths and speeds of individual gate responses may cause variations in transmission time and in the elapsed time before reception. To allow for slow signals to arrive, and to permit settling of levels which have encountered transmission noise, the strobing or gating of this data is delayed a nominal 75 ns. This delay is greater than the worst case signal skew encountered in practice.

A further delay may be necessary to allow an information signal within a device to qualify gates that accept a strobing signal. A 75-ns delay allows for this gating and must be provided by any device which acts as a bus master for a data transfer. Thus, a slave is always guaranteed that address and data are valid at its interface (the device side of the

receivers) 75 ns in advance of the MSYN signal at the output of the MSYN receiver. If a slave requires more decoding time, it must provide its own delay for the MSYN signal, or trigger a delayed strobe from the MSYN signal.

To simplify slave device design in a DATI or DATIP sequence, the slave may place the data on the D lines coincident with the assertion of SSYN. The deskewing (75 ns) and decoding delay is the master's responsibility. In the INTR sequence, the interrupting device may place the vector address on the D lines coincident with the INTR signal. The processor allows for the 75-ns skew.

5.8.2 Time-Out Protection

A precaution must be taken when designing peripheral devices that gain control of the bus for the purpose of transferring data to another element on the UNIBUS. Normally, such a device contains a bus address register, which is loaded by the program as one of the initialization steps. This address must then be incremented by the device upon completion of each data transfer. If the program loads an erroneous address or if the register increments beyond the available core memory in the existing system, no SSYN response is generated for the data transfer. To prevent this problem from hanging up the system, it is recommended that a 10- to 25- μ s integrating one-shot be triggered each time the master device asserts MSYN. If this one-shot times out before SSYN is received, the master should stop the transfer by clearing MSYN, BBSY, and any other signals it has asserted. The master should then set an error flag in its status register.

5.8.3 Priority Chaining

The PDP-11 uses electrical chaining of devices to assign minor priority levels. These levels separate devices of the same major priority level to provide a full array of priority servicing. Figure 5-17 illustrates the mode of operation and advantages of this system. Six devices are shown in order of their electrical distance from the processor. Three devices are at major priority level 4: device A, device C, and device D. The remaining three are at major priority level 5.

If the processor is at priority level 5 or above, no bus requests are granted from any of these devices. At a processor priority of 4, only requests from devices B, E, or F are granted. Assume that the processor priority is 2 and also that during one instruction cycle, devices C, E, and F assert bus requests. At the end of the instruction, the processor conducts a PTR operation. Since BR 5 is asserted, the processor does not respond to BR 4 (device C). When BG 5 is asserted, the signal first goes to device B. The signal is passed on, since device B was not asserting BR and does not block the pulse. Next, the signal goes to device E, which blocks the pulse, drops BR 5, and takes control of the bus. Device F still has BR 5 asserted, however, and device C has BR 4 asserted. These requests remain on the bus until granted or actively cleared by the processor. If device E does an INTR operation, device F gains control of the bus after the first instruction of the handling routine has been executed, unless the INTR operation raises the processor priority.

Changing the processor priority is accomplished easily since the trap

sequence following the INTR operation provides a new PS word, which includes a new processor priority. If the priority is set to 5, the processor ignores the current bus request but grants requests from other devices with higher major priority levels (if there are any).

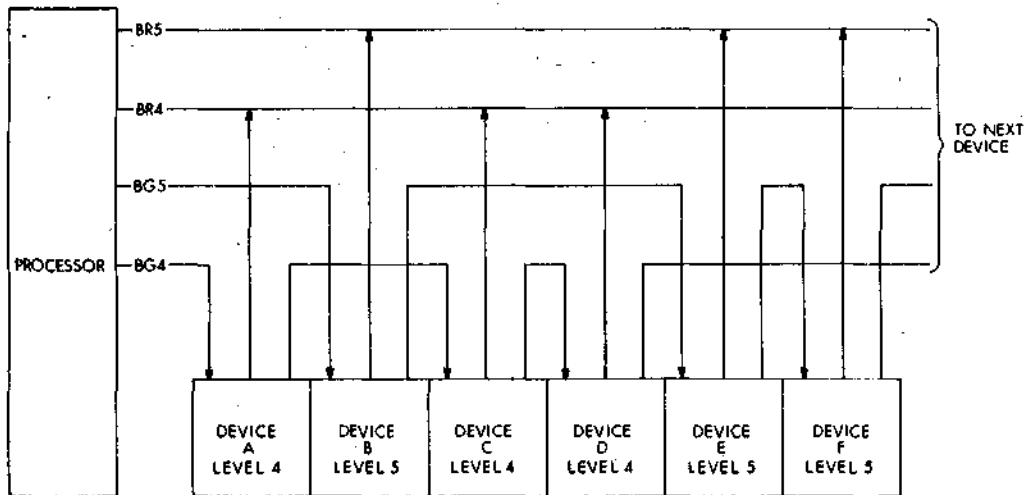


Figure 5-17 Priority Chaining Example

At the conclusion of the interrupt handling routine, the original processor priority is restored and normal processing is resumed. After one instruction, device F gains control of the bus. When normal processing resumes again, device C, which is still waiting for bus service, gains control in a similar manner.

Higher priorities are assigned to devices that require faster service to avoid destruction or loss of data. Slower devices, which can afford to wait, operate with low priorities. Therefore, service can be provided to all devices in an equitable manner, with no lost data and maximum speed and bus efficiency.

5.8.4 Address Mapping

A PDP-Address Map is shown in Appendix A. Observe that, in the following discussion, all addresses are numbered in octal. The letter K, which is normally used to denote 1000 (decimal), is used in this discussion to denote 1024 (decimal).

The UNIBUS addresses 2^{18} locations (262,144₁₀ or 256K), and each location contains eight bits. On the basic PDP-11 systems only 16 bits of address information are under program control. This limits the processor to an address map of 64K locations. Since the word length and bus width are two bytes, most bus operations access two locations at once; the address supplied on the bus is that of the even-numbered location, and the next higher odd location is selected as well. Byte operations can explicitly address any byte. For example, a DATI to location 400 transfers the information in locations 400 and 401, while a DATOB to location 400 loads only location 400. In all cases, a full-word operation cannot address an odd-numbered location.

The address map (Appendix A) contains full, 18-bit wide bus addresses. Without the Memory Management option, hardware in the processor forces A(17:16) to ones if A(15:13) are all ones when the processor is master; thus, the last 8K byte locations are relocated to be the highest locations accessible by the bus. All device addresses and internal processor locations are assigned in these 8K locations.

Interrupt and Trap Vector Locations

The first 1000 (octal) locations in the address map are reserved for trap and interrupt vectors. The stack pointer overflow feature of the processor warns the user that the data in these locations may be subject to destruction if the system stack expands downward into this area. Locations 0 through 37 are used for trap vectors for internal processor use, locations 40 through 57 are reserved for use as system software communications words, and the remaining locations are used for device interrupt vectors. There is no limit to interrupt vectors above 400 except that they are not protected from stack overflow, except with the Programmable Stack Limit option.

To prevent customer-designed interfaces from interfering with standard DEC products, the vector addresses (170, 174, 270, and 274) are reserved for customer interfaces.

Each vector requires four locations (two words), and the vector addresses are constrained to even-word boundaries; that is, each vector must end in 4 or 0. (This is implemented by providing vector addresses which do not specify bits 0 or 1. Since the low bits are always 0, address bit 2 specifies either 0 or 4.)

Memory Locations

Memory locations, either read/write or ROM, begin at 0 and proceed to 757777. The highest numbered 8K-block in the map is used by device registers and by internal processor register addresses.

Device Register Locations

Each device has one or more device registers. Device register addresses are always even (A00 is 0), although byte operations may address either half of a register.

The top 4K word locations are allocated for device register assignment. The top 2K words (770000-777777) is reserved by Digital for processor addresses and standard peripheral devices. The 1K word addresses (764000-767777) are reserved for customer allocation. It is recommended that customer-built interfaces be given addresses in this area.

5.8.5 Devices Registers

The actual transfer of data between a device and the UNIBUS takes place through one or more registers in the device. These registers may be either flip-flop storage registers or dynamic signals which are simply gated to the bus during a transfer. In addition, it is not necessary for the exact nature of the register bits to be the same. Some bits may be used for read/write (transferred on both DATI and DATO transactions); some may be write only (participate only in DATO transactions, and appear as 0s for DATI's); and some may be read only (participate only in DATI's, unaffected by DATO's). Exercise caution when assigning bit usage. For

example, a BIS (Bit Set) instruction to a word containing a write-only bit does not set the bit, but clears it. This is because a BIS performs a DATIP, DATO sequence and, if the bit reads as a 0, it is rewritten as a 0. Examples of all three types are usually found in control and status registers. A typical example of a read write bit is an interrupt enable bit; an example of the write bit is a go command bit; an example of a read bit is an indicator of an error condition requiring operator intervention.

To standardize register format types, Digital has adopted some preferred bit assignments which are shown in Figure 5-18. The preferred order of register address assignments is given in the table. These preferences are included for reference only and should not be construed as mandatory requirements for interfacing to the UNIBUS. The exact nature of register assignments varies with each device.

- FUNCTION:** Device Function (read, write, punch, search, etc.) Single function devices should use bit 0 because INC CSR (an operate instruction) performs the command with less program storage and is also faster than a conventional MOV.
- EXTENDED MEM:** Used to specify A(17:16) when doing device controlled data transfers to locations not in the first 64K block of addresses.
- INTR ENB:** Interrupt Enable. Inhibits Interrupt on done or error if not set.
- READY or DONE:** Bit set by device when internal processing is completed and the device is ready to participate in a transfer. Can be checked by the instruction sequence LOOP: TSTB CSR, BPL LOOP.
- UNIT SELECT:** Used to select multiple devices connected to a single controller (such as DECTape units with operator set unit numbers).
- BUSY:** Indicates that the device is doing internal processing and cannot participate in a new operation. Need not be used in many devices, READY may be adequate.
- ERROR:** Indicates the source or cause of an Error Interrupt. Bit 15 is used for single-error conditions or may be the logical OR of several error condition to allow the TST instruction to check error status.

Preferred Order of Device Register Assignments

ADDRESS (OCTAL)		
N	CSR	CONTROL STATUS REGISTER
N + 2	DBR	DATA BUFFER REGISTER
N + 4	MAR	MEMORY ADDRESS REGISTER
N + 6	WCR	WORD COUNT REGISTER
N + 10	DAR	DEVICE ADDRESS REGISTER

CSR—Device function, status interrupt control.
 DBR—Data register for information transfer.
 MAR—Memory location for block transfer. Incremented by device logic each word transfer.
 WCR—Set by program to control length of block transfer.
 DAR—Track or block number for mass storage devices.

When several registers are used for the same function, they should be assigned contiguous addresses, and be followed by registers of other functions in the same order as for single registers of each function.

CSR1
 CSR2
 DBR1
 DBR2
 DBR3
 MAR
 WCR
 DAR

All register types are optional; only implemented registers should be assigned addresses.

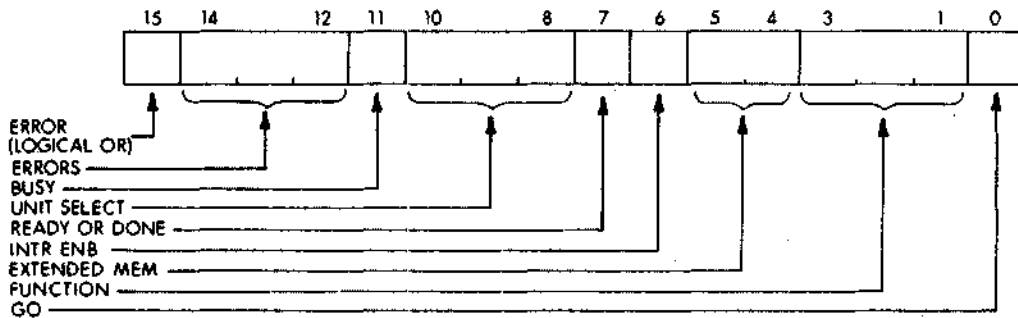


Figure 5-18 Preferred CSR Bit Assignments

5.9 COMPARISON BETWEEN NPR & BR OPERATION

	NPR	BR
Operation	data transfer (Direct Memory Access)	program interrupt
When granted	during an instruction	at end of an instruction
Condition for grant	always.	higher priority than CPU
Signals		
Request	NPR	BR7, BR6, BR5, BR4
Grant	NPG	BG7, BG6, BG5, BG4
Select Acknowledge	SACK	SACK
Bus Busy	BBSY	BBSY
Typical Registers used		
Command & Status (CSR)	X	X
Data Buffer (DBR)	X	X
Word Count (WCR)	X	
Data Address (DAR)	X	
Memory Address (MAR)	X	
Usage	critical data	plenty of time
Trade off	inexpensive in time, expensive in hardware, hardware does the work	inexpensive in hardware, expensive in time, software does the work
If wrong choice	higher cost	lose data or bad data
Typical devices	disk tape A/D (high speed) communications MX scopes	paper tape terminal A/D (low speed) communications single line

CHAPTER 6

UNIBUS INTERFACING

6.1 GENERAL

This chapter discusses the specific circuits and modules used for interfacing devices to the UNIBUS.

The UNIBUS, a high-speed data transmission facility, imposes certain restrictions when attaching other devices to it. The actual bus is a matched and terminated transmission line which must be received and driven with devices designed for that specific application. The following paragraphs describe bus transmission, bus signal levels, bus length, and bus receiver and transmitter circuits.

6.1.1 UNIBUS Transmission

The actual bus medium consists of several types of cable. The standard cabling is composed of short jumper modules that interconnect the system units within a mounting assembly. The M920 Module serves as the jumper module. Critical ground signals are also carried on this module. Cables used between mounting assemblies consist of a flat ribbon cable assembly with alternating signals and grounds. The characteristics necessary for proper UNIBUS transmission are:

Characteristic Impedance:	$120\Omega \pm 18\Omega$
Resistance:	0.135 Ω /ft, maximum

Either twisted pair or coaxial cable laid for minimum crosstalk is recommended for long cable lengths and for applications requiring extreme physical durability of the cable.

The UNIBUS is terminated at each end by a resistive divider for each signal except the grant signals (see Figure 6-1). The grant signals are terminated with a single resistor. Two M930 Terminator Modules are included in every system to provide these functions.

6.1.2 UNIBUS Signal Levels

For most UNIBUS signals:

- logic 1 = 0 volts (LOW)
- logic 0 = + 3.4 volts (HIGH)

Note that the polarity is opposite to that normally used with TTL integrated circuits.

The rest state for all UNIBUS signal lines, except the grant lines BG < 7:4 > and NPG, is a logic 0 of + 3.4V. The asserted state (logic 1) is between ground and + 0.8V, which is the saturation voltage of the

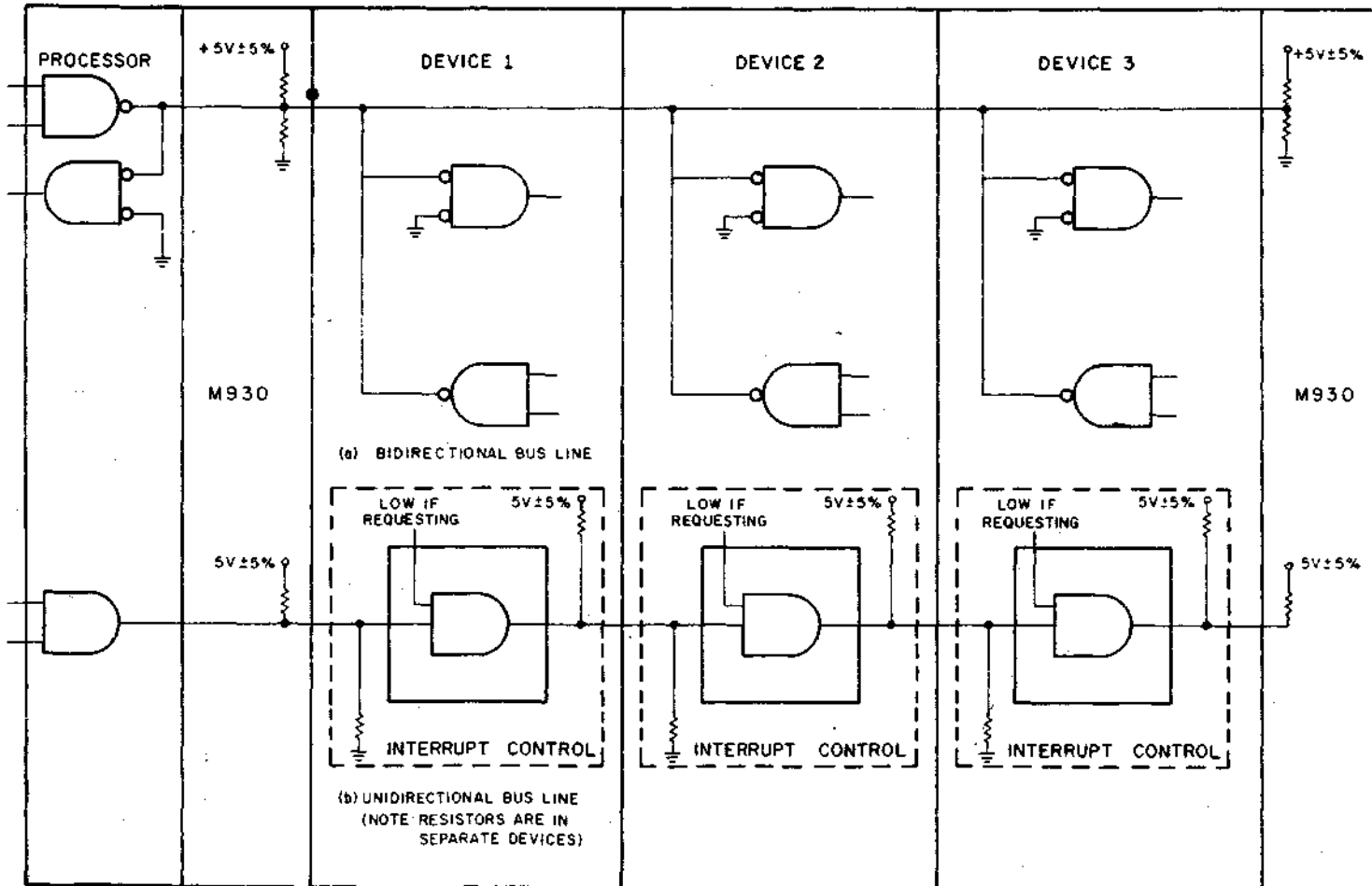


Figure 6-1 Bus Terminations for Bidirectional (a), and Unidirectional (b) Bus Lines

transistor driving the bus. The rest state for the grant signals is ground (logic 0) and the asserted state (logic 1) is + 3.4V. To guarantee operation under worst case conditions, receivers should have a switching threshold of approximately + 1.5V.

Digital Equipment Corporation uses standard terminology to name signal lines to aid the reader in determining their active state. Either an H or L follows the signal name mnemonic and is separated by a space. This letter indicates the asserted (logic 1) state of the signal to be either high (approximately + 3V) or low (ground). Thus, a UNIBUS data line is called BUS D00 L and a grant line is called BUS BG4 H.

With flip-flops, a 1 or 0 in parentheses is often used following the signal name to indicate the assertion state, see Figure 6-2.

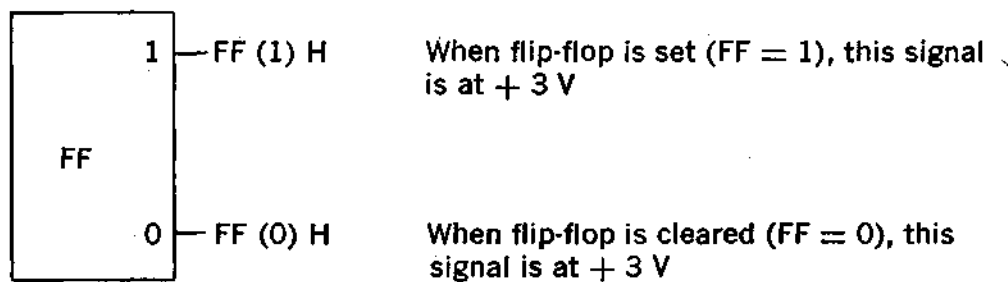


Figure 6-2 Flip-flop signals

Note that:

$$\begin{aligned}
 & \text{FF (1) H} = \text{FF (0) L} \\
 & \text{and} \quad \text{When FF is a 0, this signal is at 0 V.} \\
 & \text{FF (0) H} = \text{FF (1) L}
 \end{aligned}$$

All signals which are not UNIBUS signals are characterized in terms of standard transistor-transistor logic (TTL) loads. These devices, which are similar to the 7400 Series, have a low state input load of - 1.6 mA and a high state leakage current of 40 μ A. Outputs are characterized by the number of inputs they can drive (called fanout).

A standard TTL gate can drive 10 unit loads.

6.1.3 Bus Receiver and Transmitter Circuits

The equivalent circuits of the standard UNIBUS receivers and transmitters are shown in Figure 6-3. Any device which meets these requirements is acceptable. To perform these functions, Digital Equipment Corporation uses two monolithic integrated circuits with the characteristics listed in Table 6-1. A typical transmitter circuit is shown in Figure 6-4.

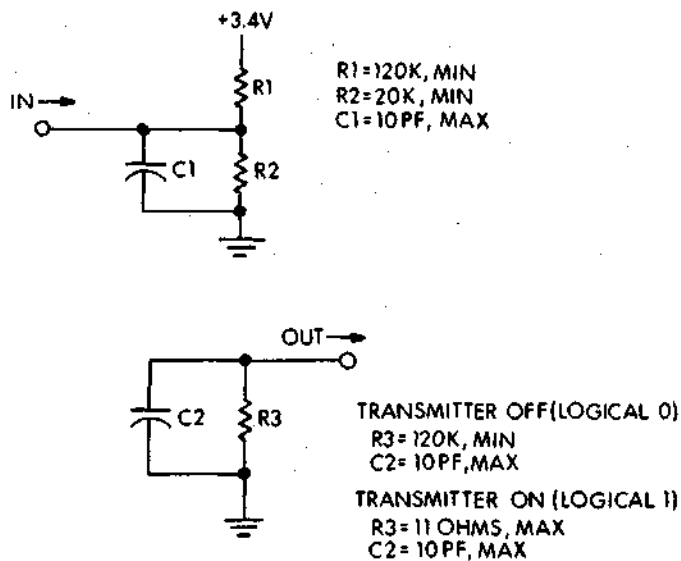


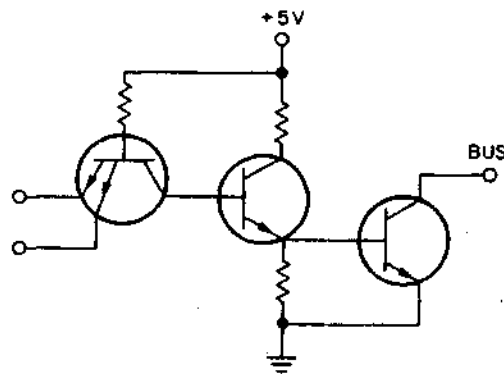
Figure 6-3 Transmitter and Receiver Equivalent Circuits

Table 6-1 Unibus Receiver and Transmitter Characteristics

	Characteristic		Specifications	Notes
Receiver (DEC 8640)	Input high threshold	VIH	1.7V min.	1
	Input low threshold	VIL	1.3V max.	1
	Input current @ 2.5V	IIH	80 μ A max.	1, 3
	Input current @ 0V	IIL	-10 μ A max.	1, 3
	Output high voltage	VOH	2.4V min.	2
	Output high current	IOH	(16 TTL loads)	2, 3
	Output low voltage	VOL	0.4V max.	2
	Output low current	IOL	(16 TTL loads)	2, 3
	Propagation delay to high state	TPDH	10 ns min. 35 ns max.	4, 5
	Propagation delay to low state	TPDL	10 ns min. 35 ns max.	4, 5
Transmitter (DEC 8881)	Input high voltage	VIH	2.0V min.	6
	Input low voltage	VIL	0.8V max.	6
	Input high current	IIH	60 μ A max.	6
	Input low current	IIL	-2.0 mA max.	6
	Output low voltage @ 70 mA sink	VOL	0.8V max.	1
	Output high leakage current @ 3.5V	IOH	25 μ A max.	1, 3
	Propagation delay to low state	TPDL	25 ns max.	5, 7
	Propagation delay to high state	TPDH	35 ns max.	5, 8

NOTES:

1. This is a critical parameter for use on the UNIBUS. All other parameters are shown for reference only.
2. This is equivalent to being capable of driving 16 unit loads of standard 7400 series TTL integrated circuits.
3. Current flow is defined as positive if into the terminal.
4. Conditions of load are 390Ω to $+5V$ and $1.6K\Omega$ in parallel with 15 pf to ground for 10 ns min and 50 pf for 35 ns max.
5. Times are measured from 1.5V level on input to 1.5V level on output.
6. This is equivalent to 1.25 standard TTL unit loading of input.
7. Conditions of 100Ω to $+5V$, 15 pf to ground on output.
8. Conditions of $1K\Omega$ to ground on output.



TYPICAL UNIBUS DRIVER

Figure 6-4 Typical Transmitter Circuit

Transmitter

If both inputs to a UNIBUS Transmitter are logic 1 (HIGH), there will be a logic 1 (LOW) on the UNIBUS. Refer to Figure 6-5. Logically, the Transmitter is an AND gate; there is voltage inversion, but no logic inversion.

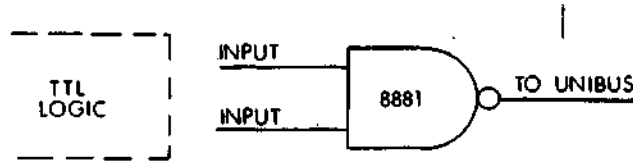


Figure 6-5 UNIBUS Transmitter

If any 8881 Transmitter has both its inputs at logic 1, there is a logic 1 on the UNIBUS. The logical operation is AND-OR.

Receiver

If the UNIBUS line is a logic 1 (LOW), the output will also be a logic 1 (HIGH). Refer to Figure 6-7. Logically, the Receiver has no effect on the signal; but there is voltage inversion, thereby cancelling the effect of the first voltage inversion by the Transmitter.

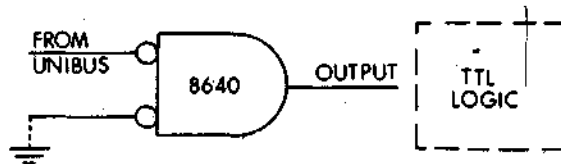


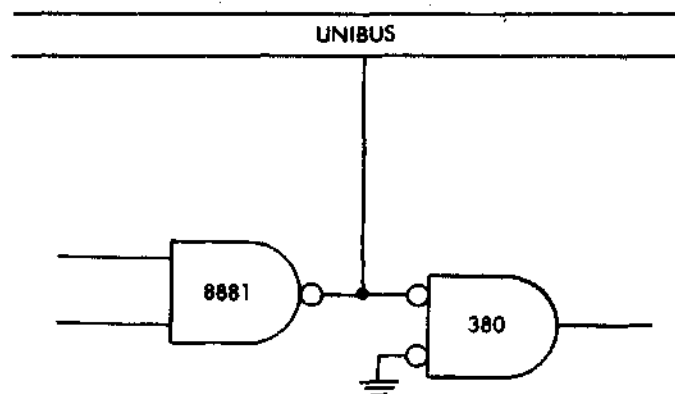
Figure 6-6 UNIBUS Receiver

If the inputs were connected to separate UNIBUS signals, the Receiver would logically be a 2-input OR gate. The inputs can also be connected to TTL outputs.

6.1.4 UNIBUS Length and Loading

Since the UNIBUS is a transmission line, and the transfers are asynchronous and interlocked, the electrical delay imposed by length is not a factor.

With ribbon cable the maximum length is 50 ft. For proper operation, the length of taps or stubs must be minimized. The UNIBUS signals should have receivers and transmitters in one place (near the UNIBUS cable) to act as a buffer between the UNIBUS and the signal lines carrying UNIBUS signals within the equipment. The maximum length of ribbon cable is obtainable only if the individual tap lengths are less than 2 inches, including printed circuit etches and if the loading is not more than one standard bus load. One bus load is defined as 1 transmitter and 1 receiver, see Figure 6.8.



1 BUS LOAD = 1 TRANSMITTER + 1 RECEIVER

Figure 6-7 1 Bus Load

The UNIBUS is limited to a maximum of 20 bus loads. This limit is set to maintain a sufficient noise margin. For more than 20 bus loads, a UNIBUS repeater option (DB11-A) is used.

6.2 UNIBUS INTERFACE MODULES

This section describes modules used for UNIBUS interfacing.

Module	Name	Description
BC11A	UNIBUS Cable	120-conductor ribbon cable, 56 signals plus 64 grounds, alternating.
M105	Address Selector	Address decoding for 4 devices.
M783	Bus Transmitter	12 drivers, mixed logic.
M784	Bus Receiver	16 receivers; single input, single output.

M785	Bus Transceiver	8 drivers plus 8 receivers.
M795	Word Count & Bus Address	2 16-bit counters.
M796	Bus Master Control	Complex control logic.
M920	Bus Jumper	Connects SU to SU; 56 signals plus 14 grounds.
M930	Bus Terminator	180 ohms to + 5V and 390 ohms to ground.
M7820	Interrupt Control	2 Master Control circuits.
M7821	Interrupt Control	NPR plus BR circuits.

6.2.1 BC11A, UNIBUS Cable

The BC11A (see Figure 6-9) is a 120-conductor ribbon cable used to connect System Units in different mounting drawers or assemblies.

The 120 signals include all the 56 UNIBUS lines plus 64 grounds. Signals and grounds alternate to minimize crosstalk. Cable types and lengths are listed below:

Type	Length (ft.)
BC11A-2	2.0
BC11A-5	5.0
BC11A-8F	8.5
BC11A-10	10.0
BC11A-15	15.0
BC11A-25	25.0

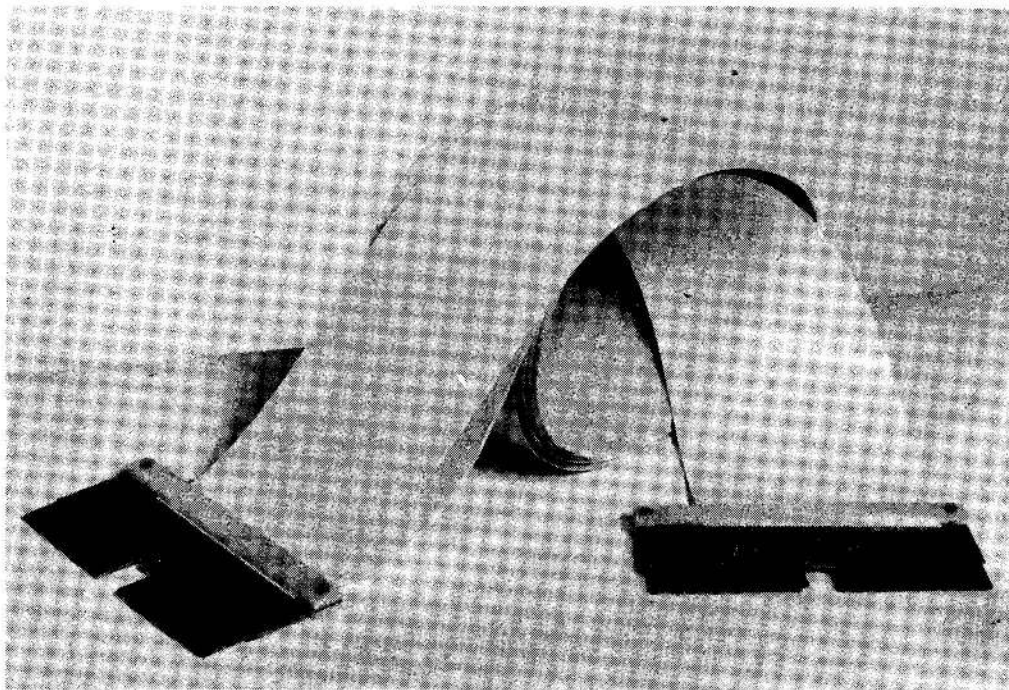


Figure 6-9 UNIBUS Cable BC11A

6.2.2 M105 Address Selector Module

The M105 Address Selector Module provides gating signals for up to 4 full 16-bit device registers. A block diagram of this module is shown in Figure 6-10. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the M105 is used in a peripheral device, an OUT transfer is a transfer of data out of the master (such as the processor) and into the device. Likewise, an IN transfer is the operation of the peripheral furnishing data to the processor.

Inputs: The M105 Module input signals consist of 18 address lines, A <17:00>; 2 bus control lines, C <1:0>; and a master synchronization MSYN line. The address selector decodes the 18-bit address on lines A <17:00> as described below. This address format, used for selecting a device register, is shown in Figure 6-11. Note that all inputs are standard bus receivers.

- a. Line A00 is used for byte control.
- b. Lines A01 and A02 are decoded to select one of the four addressable device registers.
- c. Decoding of lines A <12:03> is determined by jumpers on the module. When a given line contains a jumper, the address selector searches for a zero on that line. If there is no jumper, the address selector searches for a one.
- d. Address lines A <17:13> must be all ones. This specifies an address within the top 8K byte address bounds for device registers.

Slave Sync (SSYN): When SSYN INH is grounded, it inhibits the acknowledgment signal (SSYN) normally generated by the M105. In this case, the SSYN must be generated by another source. When SSYN INH is not grounded, SSYN is returned to the master 100 ns after register select becomes true. This time may be extended to a maximum of 400 ns by adding an external capacitor between SSYN INH and ground. SSYN INH can also be driven with an open collector gate.

Outputs: The M105 Select Signals permit selection of four 16-bit registers and provide three signals used for gating information to and out of the master device. The M105 may be used instead to select up to eight 8-bit registers, or any appropriate combination of byte and word registers.

The input signals select the M105 control output line states as shown in Tables 6-2 and 6-3.

Table 6-2 M105 Select Lines

Input Lines A <02:01>	Select Lines True (+ 3V)
00	0
01	2
10	4
11	6

NOTE

1. Lines A <17:13> must be all 1's (OV on UNIBUS).
2. Lines A <12:03> are selected by jumpers.

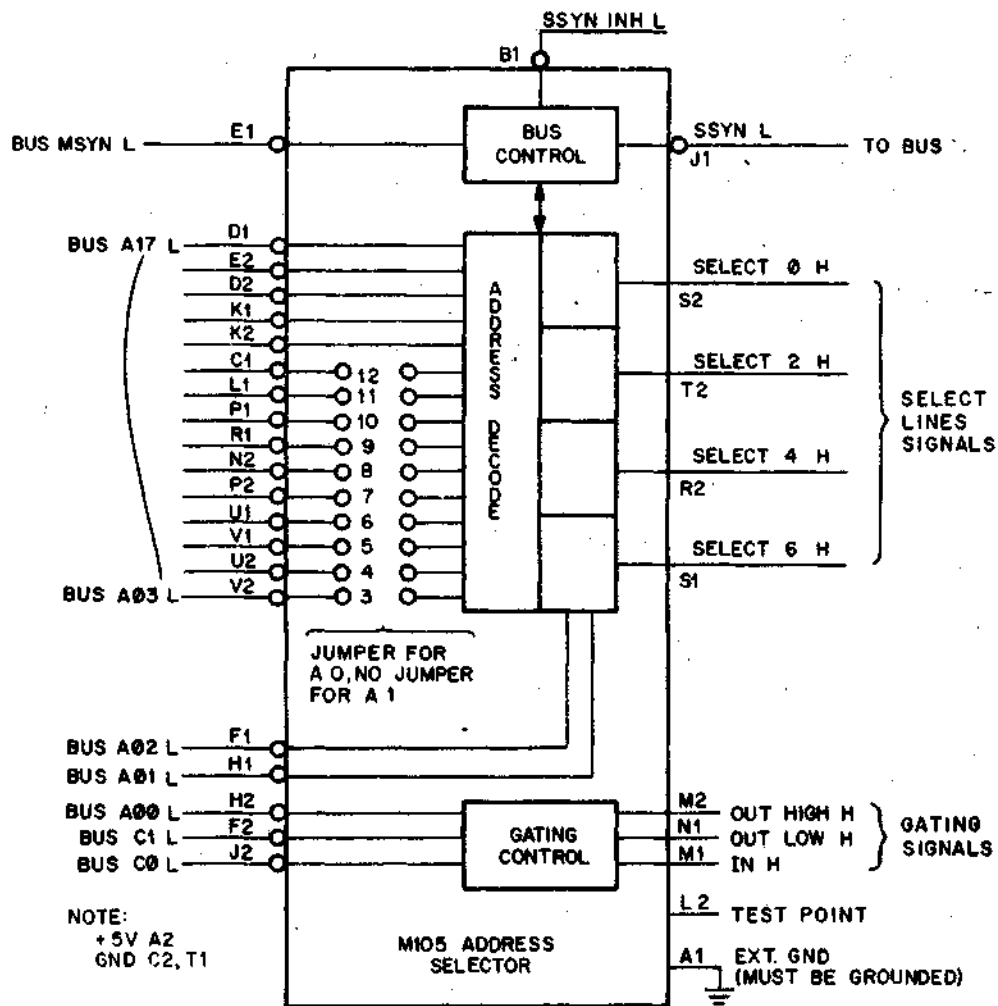


Figure 6-10 M105 Address Selector

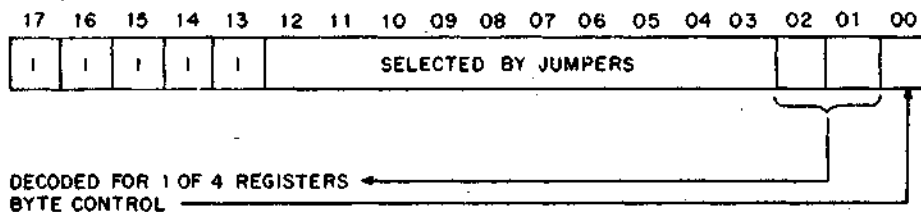


Figure 6-11 Device Register Select Address Format

Table 6-3 Gating Control Signals

Mode Control C <1:0>	Byte Control A00	Gating Control Signals True (+ 3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW, OUT HIGH	DATO
10	1	OUT LOW, OUT HIGH	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH	DATOB

NOTE

Gating control signals may become true although select lines are not.

Specifications: The M105 output fanout is ten standard TTL loads for register select lines and eight standard TTL loads for gating control lines. The module is single-height. A circuit schematic for this module is shown in Figure 6-12. Note that pin A1 (EXT GND) must be grounded by the user.

When using the output signals of the M105 to load registers that comprise storage elements that are edge-triggered, insure that this edge is derived from the positive transition of the SELECT line, i.e. the leading edge of MSYN.

If the storage elements are loaded by a strobing pulse (not edge-triggered), then the entire pulse must be generated prior to the assertion of SSYN. The length of the loading pulse can be lengthened by adding capacitance to SSYN INHB on the M105.

6.2.3 M783 UNIBUS Transmitter Module

This transmitter module contains 12 drivers; 8 drivers have a common gate line, 4 have 2-input positive AND gating. Input loading is 1.25 standard TTL load. The module is single-height. A circuit schematic of the M783 Transmitter is shown in Figure 6-13.

6.2.4 M784 UNIBUS Receiver Module

This receiver module consists of 16 DEC 8640 inverting circuits which receive bus signals and provide a buffered bus signal output. The output fanout is seven standard TTL unit loads. The receiver module is single-height. A circuit schematic of the M784 Receiver Module is shown in Figure 6-14.

6-12

REQUIRES 340mA MAX. @ +5V

NOTE
UNLESS OTHERWISE INDICATED
RESISTORS ARE 1K, 1/4W, 5%
+5V A2
GND C2, T1

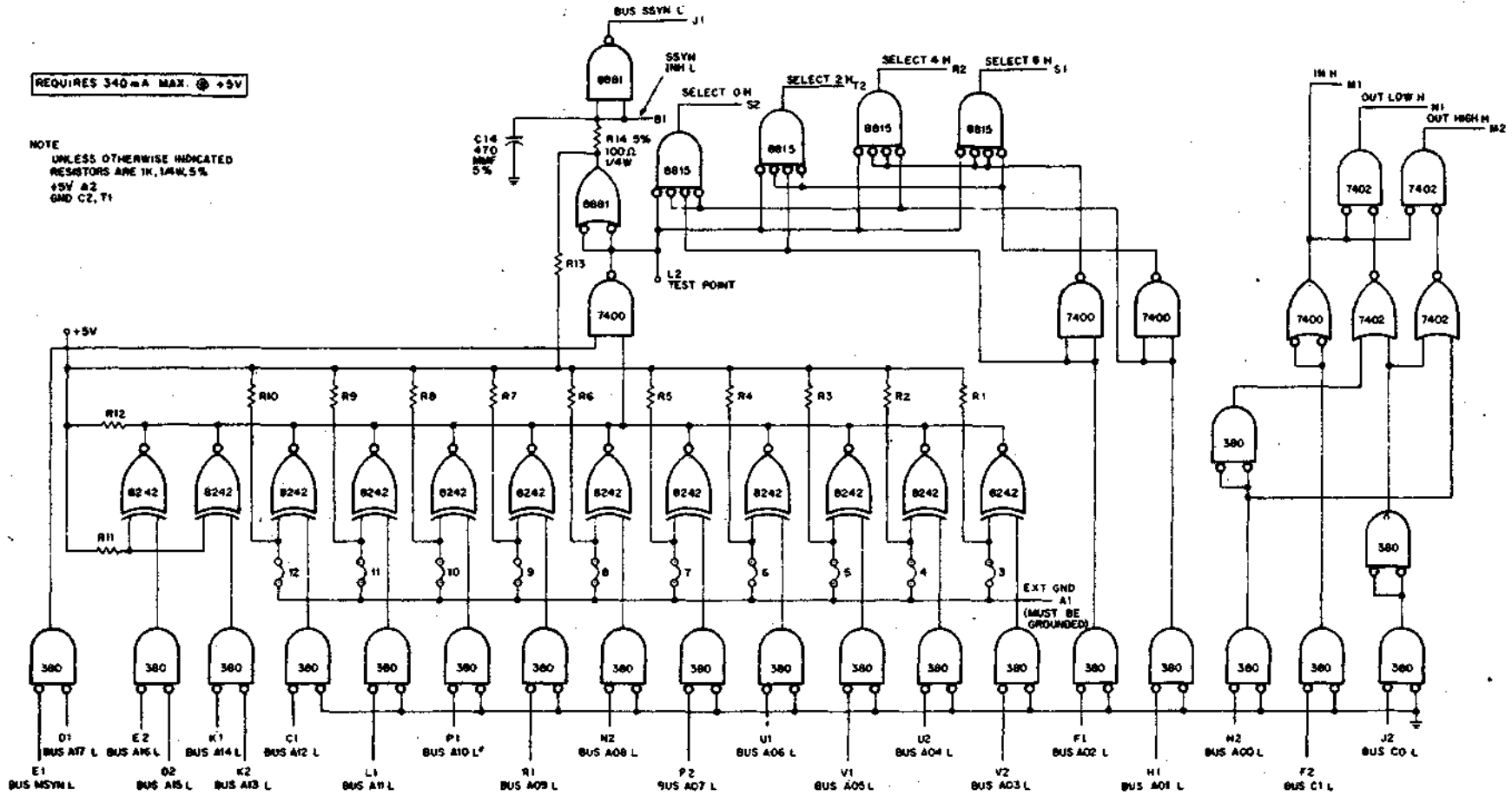


Figure 6-12 M105 Address Selector (schematic diagram)

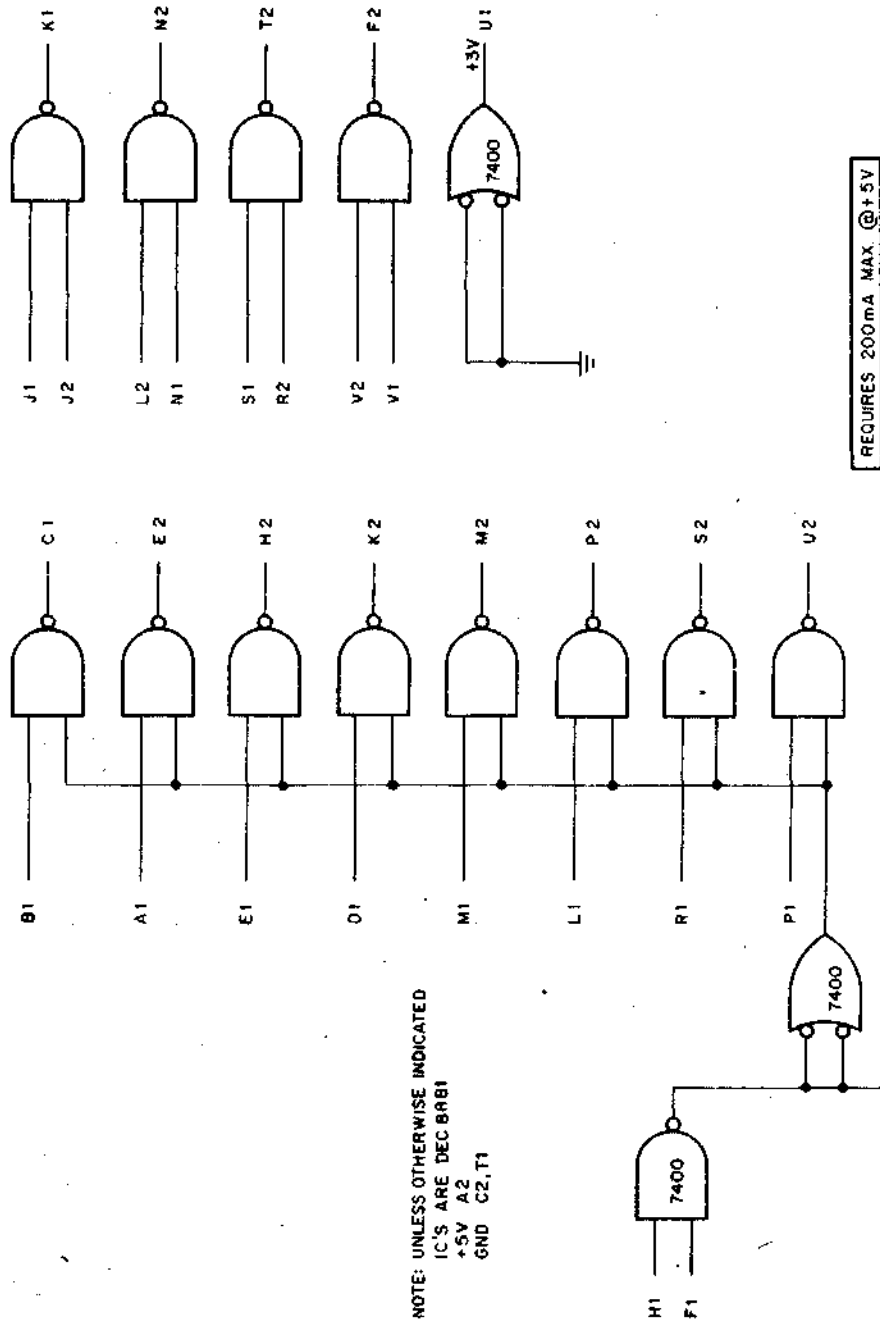
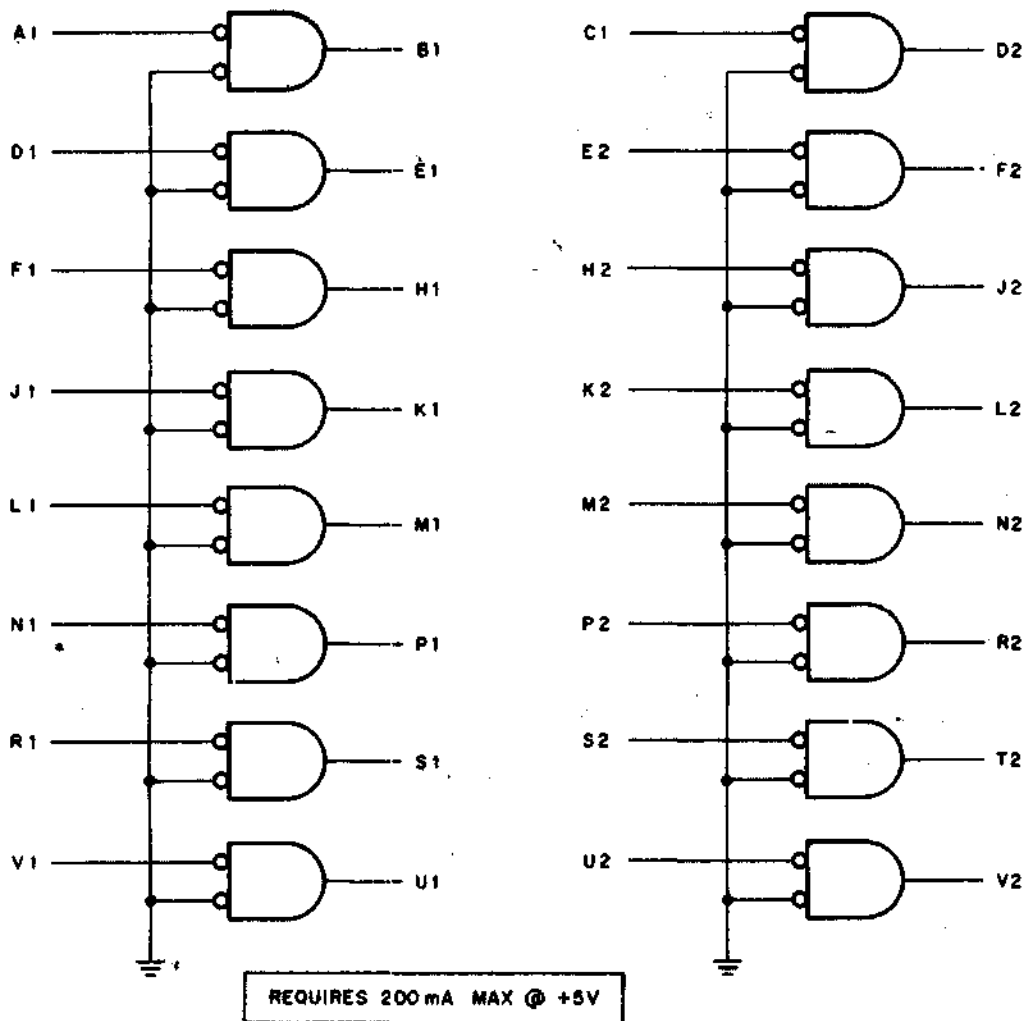


Figure 6-13 M783 UNIBUS Transmitter (schematic diagram)

6.2.5 M785 UNIBUS Transceiver Module

This module consists of eight pairs of DEC 8881 Drivers and DEC 8640 Receivers which are used for bidirectional interfacing to the UNIBUS. The drivers and receivers have two common gate lines: one for receivers, one for drivers. The driver input loading is 1.25 standard unit load and the receiver fanout is 7 standard TTL unit loads. The module is single-height. A circuit schematic of the M785 Transceiver Module is shown in Figure 6-15.



NOTE: UNLESS OTHERWISE INDICATED
 IC'S ARE DEC 8640
 +5V A2
 GND C2,T1

Figure 6-14 M784 UNIBUS Receiver (schematic diagram)

6.2.6 M795 Word Count and Bus Address Module

The M795 Word Count and Bus Address Module is used to interface direct memory access (DMA) devices to the UNIBUS. This module contains two 16-bit counters: one counter is used to count the number of data transfers that occur; the other counter is used to specify the bus address of the data to be transferred.

Block transfer devices that function as bus master during data transfers usually require two registers to hold the parameters of the transfer. One parameter is transfer count. Initially, a register is loaded with the 2's complement of the number of items to be transferred to or from memory. After each transfer is complete, the register is incremented. If the new value of the register is 0 (indicated by an overflow), further transfers are

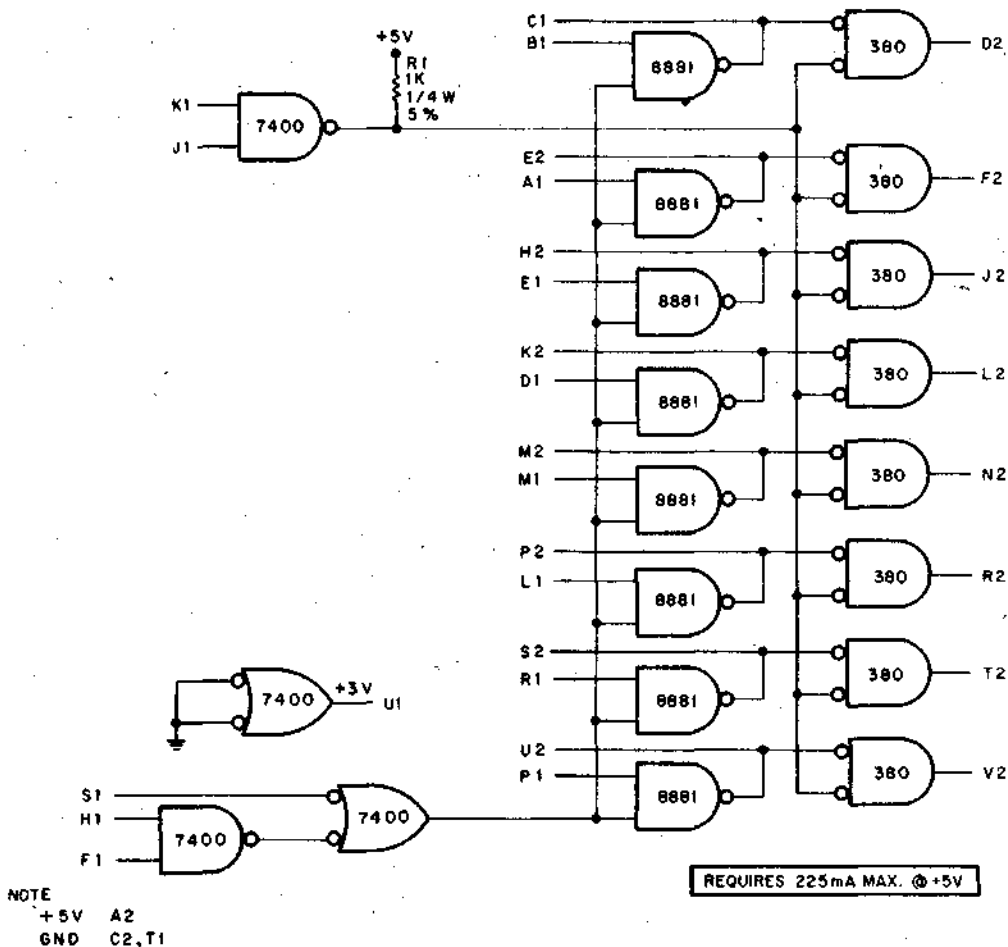


Figure 6-15 M785 UNIBUS Transceiver (schematic diagram)

Inhibited and the block transfer is complete. Since information can be transferred in words (16 bits each) on the UNIBUS the name Word Count (WC) is usually assigned to this register. However, the UNIBUS is also capable of transferring 8-bit bytes of data at a time, and this register may be used equally as well as a Byte Count register.

The second parameter used in block transfers is the transfer address. Initially, a register is loaded with an address that specifies the memory location to, or from, which data is to be transferred. The register is incremented after each transfer; thus, the register continually "points" to sequential memory locations. Since memories and devices have addresses on the UNIBUS, this register is usually called the Bus Address (BA) register.

A simplified block diagram of the M795 module is shown in Figure 6-16. Both the word count (WC) and bus address (BA) registers consist of 16 flip-flops. These flip-flop registers can be loaded by placing data on the 16 data line inputs common to both registers and asserting the appropriate loading signal. There are four independent loading signals: WC high byte, WC low byte, BA high byte, and BA low byte. Each of the outputs of the 16 bits in the WC register are connected to a set of DEC 8881 UNI-

BUS drivers. The contents of the WC register can be gated to the data bus when the appropriate gate signal is activated. The BA register also has a set of UNIBUS drivers connected to each output so that the register contents can be gated to the data bus. Note that the driver outputs of both the WC and BA registers are wire ORed together. In addition, the BA register has a set of drivers with independent outputs to allow it to drive the address bus.

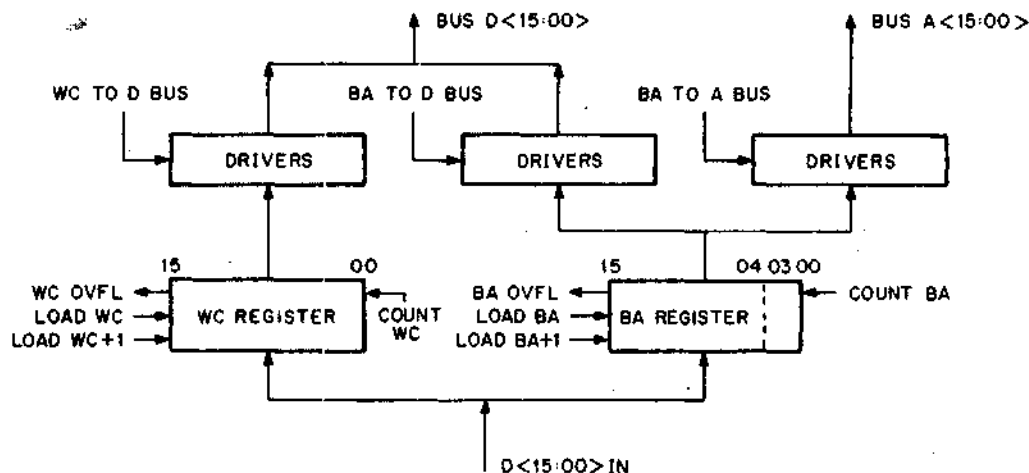


Figure 6-16 M795 Word Count and Bus Address (block diagram)

The storage element on the M795 is not an edge-triggered device; data must be established and held for the duration of the loading pulse.

The BA register can be incremented by either 1 or 2 as a function of a control input (+3V = 1; ground = +2). This incrementation capability allows addressing of either sequential bytes or words. The register is incremented on the trailing edge of a positive pulse applied to the count input of the register. The carry between bits 3 and 4 is broken and brought out to pins on the module. Normally, these pins are jumpered together externally to allow for a full 16-bit count. However, they can be controlled to inhibit the carry and to force repeated addressing of 16 sequential byte addresses. This feature can be used in device-to-device transfers. An overflow pulse is provided as an output whenever the register is incremented from all 1's to all 0's.

The WC register is incremented by either 1 or 2 as a function of its control input. The register increments on the trailing edge of a positive pulse applied to the count input of the register. An overflow pulse is also available. Both registers are reset to all 0s whenever the CLEAR signal is asserted.

Table 6-4 M795 Input Signals

Signal Name	Assertion Level	No. of Signals	of Loading	Operation
D<15:00>IN	+3V	16	1.5	Data inputs to register.
LOAD WC LOAD WC + 1	OV	4	1	Loads data on input into selected byte of register.

LOAD BA LOAD BA + 1				Low pulse of 250 ns minimum duration
WC TO D BUS BA TO D BUS BA TO A BUS	OV	3	2	Gates selected register to bus.
CLEAR WC + BA	+3V	1	2	Clears all bits. High level of 1 μ s minimum dura- tion.
BA INC CONTROL WC INC CONTROL	+3V = incr by 1 OV = incr by 2	2	3	Controls amount of incrementation.
COUNT WC COUNT BA	+3V	2	4	Trailing edge of positive pulse increments register (100 ns minimum).
BA CARRY IN	OV	1	3	Carry into upper bits of BA.

Table 6-5 M795 Output Signals

Signal Name	Assertion Level	No. of Signals	Drive Capability	Operation
BA CARRY OUT	OV	1	10	Carry out of low four bits.
BA OVFL WC OVFL	OV	2	10	Register overflow; low level pulse.
BUS D<15:00>	OV	16	UNIBUS	Data lines.
BUS A<15:00>	OV	16	UNIBUS	Address lines.

6.2.7 M796 UNIBUS Master Control Module

The M796 UNIBUS Master Control Module provides extremely flexible control logic that is used to control data transfer operations on the UNIBUS when a device is functioning as bus master. In addition to controlling the four transfer operations (DATI, DATIP, DATO, and DATOB), the M796 module generates strobe and gating signals which transfer both addresses and data to and from the bus; handles deskewing of data received from the bus; protects against data transfers to nonexistent devices by the use of time-out circuits; and provides a flip-flop and integrating one-shot that can be used for special control functions.

Devices in the PDP-11 system may have the capability of gaining control of the bus and, as bus master, of transferring data to and from other slave devices on the bus. This operation is performed with minimum processor control and is usually referred to as Direct Memory Access (DMA). The logic necessary to gain control of the bus is provided by the M7820 Interrupt Control Module. The M7820 module requests use of the bus (usually by means of an NPR request), receives the bus grant signal

from the processor, asserts selection acknowledge (SACK), waits until the current bus master releases control of the bus, and then asserts BUS BUSY, thereby gaining bus control.

Upon becoming bus master, the device is free to conduct a data transfer. A DATI cycle is performed if the device needs the data (either a word or byte) from memory; a DATO cycle is performed if the device is storing a word of data in memory (DATOB cycle for byte storage); a two-cycle DATIP, DATO(B) operation is performed if data held in memory is to be modified as in the case of increment memory or add to memory functions.

In order to execute one of these transfer cycles, the device must set BUS C<1:0> for the required type of data transfer, specify the address of the slave device participating in the transfer, assert the MSYN signal, and then wait for the SSYN response from the slave. Data must either be gated to D<15:00> on a DATO cycle or be received and strobed at the proper time on a DATI cycle. The M796 module performs these functions.

Figure 6-17 is a block diagram of the M796 UNIBUS Master control module. The BUS C1 and BUS C0 outputs can directly drive the UNIBUS and are asserted as a function of the control inputs. Table 6-6 lists the states of the control inputs for the four possible bus cycles.

Table 6-6 Control Line Input States for M796

C1	C0	Bus Cycle
0	0	DATI
0	1	DATIP
1	0	DATO
1	1	DATOB

The data transfer sequence is triggered by meeting the AND condition of two low levels (pins H1 & H2). Usually these two inputs are tied together and are connected to the MASTER signal produced by the M7820 Interrupt Control Module. When the AND condition is met, it produces the START signal, which is an internal signal in the M796 module. At the transition of the START signal, both BUS C1 and BUS C0 are asserted as determined by their respective control inputs. The ADRS TO BUS signal is also asserted and is used to gate the address of the slave onto BUS A<17:00>. If an output cycle is specified (C1 = 1), the DATA TO BUS signal is asserted and is used to gate the data to be transferred to the slave onto BUS D<15:00>. The BUS MSYN signal is asserted 200 ns after START becomes true. The master device then waits for a response from the slave.

In a data output cycle (DATO), assertion of SSYN causes BUS MSYN to be negated immediately. After a 100-ns delay, BUS C1, BUS C0, ADRS TO BUS, and DATA TO BUS are negated. When these signals drop, an END CYCLE pulse appears and is usually used to release control of the bus.

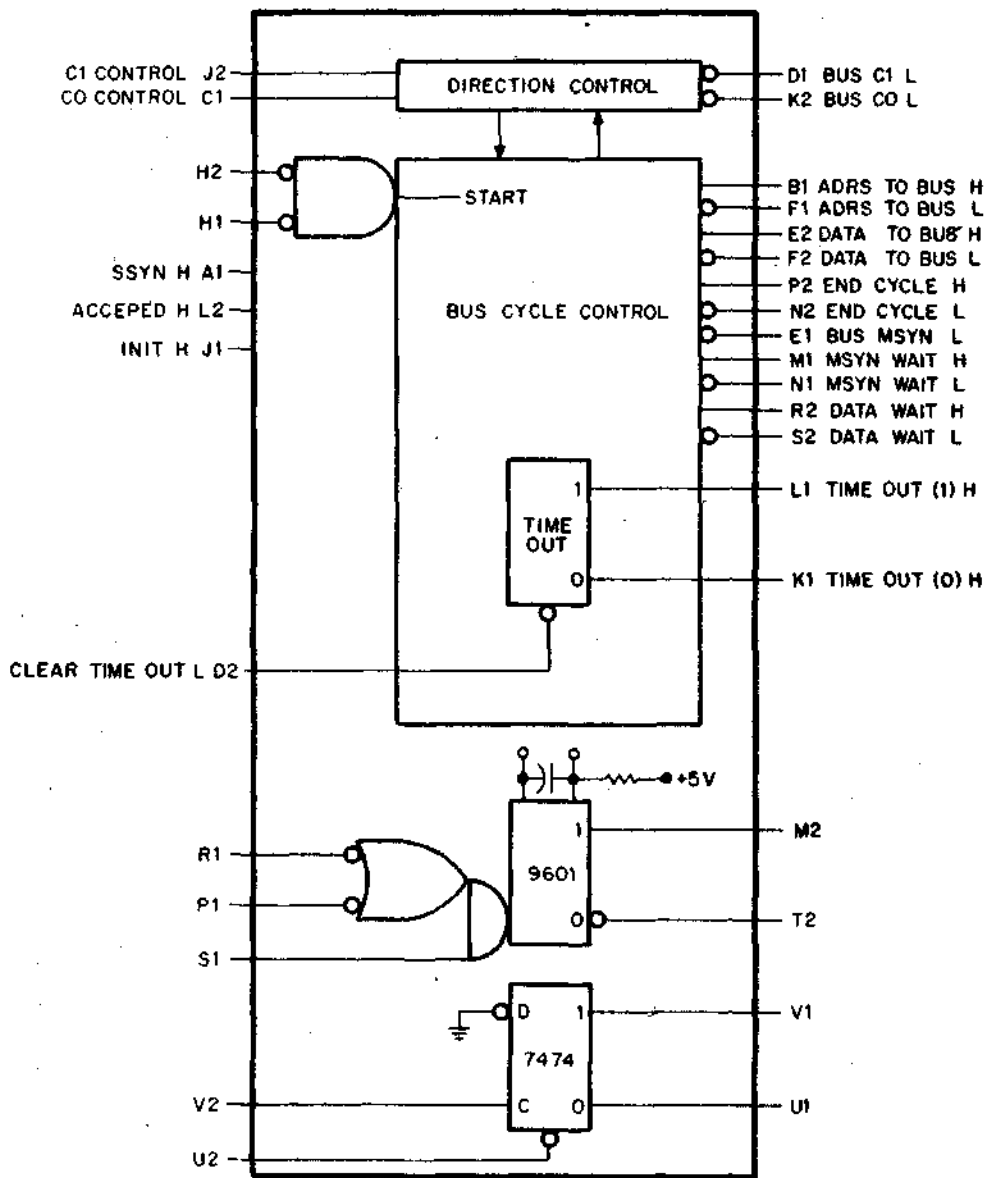


Figure 6-17 M796 UNIBUS Master Control (block diagram)

In a data input cycle (DATI), the assertion of SSYN produces a 200-ns pulse that appears as DATA WAIT. This delay allows time for the incoming data to deskew and settle. The trailing edge of the DATA WAIT pulse can be used to clock data from the slave into the master device. If a strobe pulse is necessary, the trailing edge of DATA WAIT can be used to trigger the one-shot provided on the module. In either case, once data is received, a positive-going edge is applied to DATA ACCEPTED, causing BUS MSYN to be negated initially, followed by negation of ADRS TO BUS, BUS C1, and BUS CO 100 ns later.

A TIME-OUT flip-flop on the module is set if a SSYN response fails to occur within 20 μ s after BUS MSYN is asserted. When this flip-flop is set,

the bus cycle is not performed. The TIME-OUT flip-flop is cleared by asserting the CLEAR TIME-OUT signal.

The M796 module provides a special flip-flop that has the clock, reset, 1 side, and 0 side available. The flip-flop is clocked by a positive transition on the clock input.

An integrating one-shot is also provided on the module. This one-shot is triggered whenever the output of the gating input becomes true: $(\overline{R1} + \overline{P1}) \cdot S1$. The output pulse width of this one-shot is 150 ns but can be lengthened by adding capacitance across the pair of split lugs on the module.

Note that all times mentioned represent nominal values with a tolerance of $\pm 25\%$. The delays and pulses provided by the module are controlled by simple RC circuits. Therefore, if there are any special requirements, part substitutions can be made to alter these time constants.

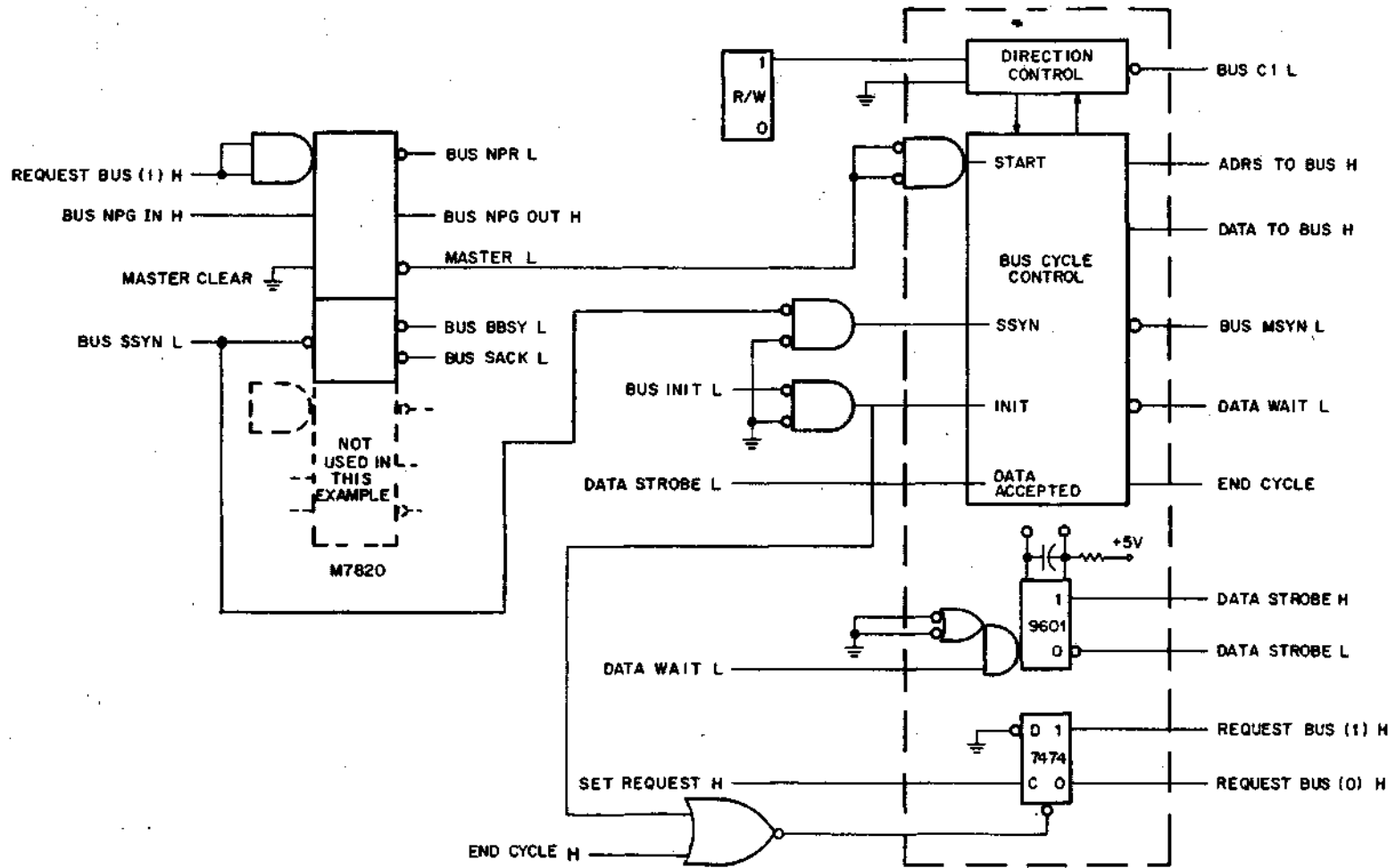
Figure 6-18 illustrates a typical interconnection schematic for the M796 UNIBUS Master Control module used in conjunction with the M7820 Interrupt Control module. The read/write (R/W) flip-flop is part of the device interface logic and determines the direction of the data transfer (set for a DATO, clear for a DATI). The data transfer is initiated by pulsing SET REQUEST which sets REQUEST BUS. The REQUEST BUS signal generates an NPR request which, when granted, gives bus control to the device as indicated by the MASTER signal. The MASTER signal causes the internal START signal to be generated. This signal triggers the sequence of timing signals. Timing diagrams for DATO and DATI cycles are shown in Figures 6-19 and 6-20 respectively.

Note that in a DATI operation, the DATA WAIT signal is generated when BUS SSYN is received. The trailing edge of DATA WAIT fires the one-shot that produces the DATA STROBE signal. This signal gates the data present on the bus data lines into the device. The trailing edge of DATA STROBE produces a positive transition at the DATA ACCEPTED input that results in the clearing of BUS MSYN.

The input signals to the module are listed in Table 6-7 and the output signals are listed in Table 6-8.

Figure 6-18 M796 UNIBUS Master Control (typical use)

6-21



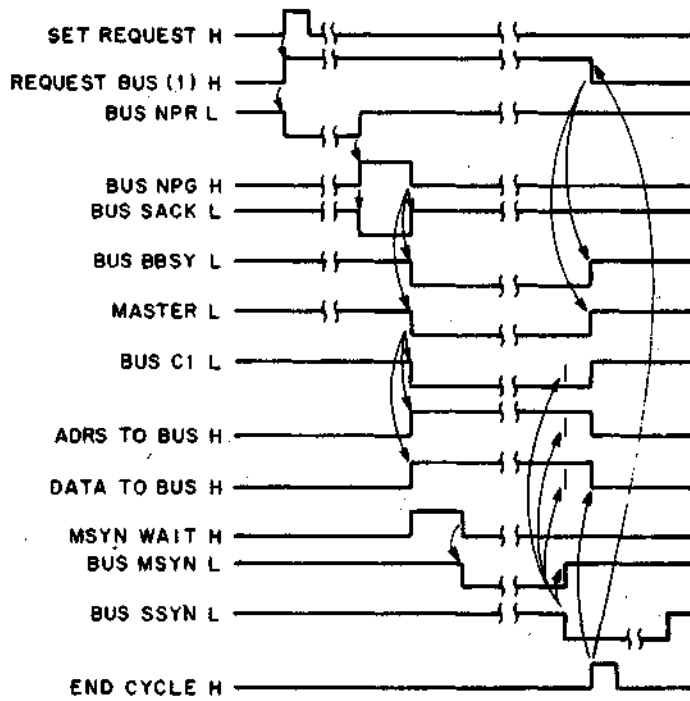


Figure 6-19 M796 Timing Diagram for DATO

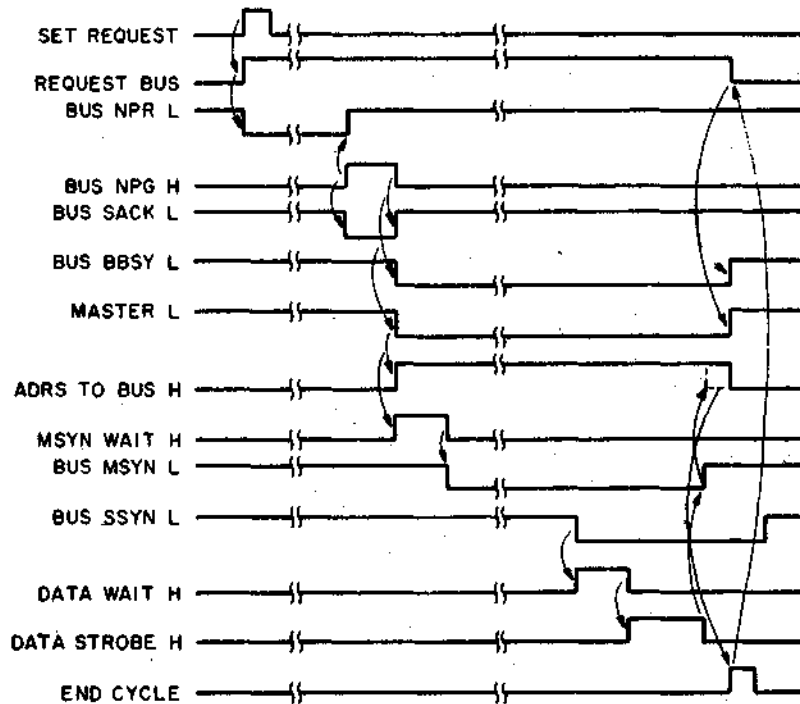


Figure 6-20 M796 Timing Diagram for DATI

Table 6-7 M796 Input Signals

Signal Name	Assertion Level	No. of Signals	Loading	Operation
C1 CONTROL		1	5	Controls Bus C1
C0 CONTROL		1	1	Controls BUS C0
PIN H2				
PIN H1	L	2	1	Produces START
SSYN	H	1	2	Negates MSYN on DATO
DATA ACCEPTED	H	1	2	Negates MSYN on DATI
INIT	H	1	1	Initializes control
CLEAR TIME OUT	L	1	2	Clears TIME-OUT Flip-Flop
PIN P1				
PIN R1	L	2	1	Negative edge triggers one-shot
PIN S1	H	1	2	Positive edge triggers one-shot
PIN V2	H	1	2	Clock input to flip-flop
PIN U2	L	1	2	Clears flip-flop

Table 6-8 M796 Output Signals

Signal Name	Assertion Level	No. of Signals	Drive Capability	Operation
BUS C<1:0>	L	2	UNIBUS	Drives UNIBUS control line
ADRS TO BUS	H	1	8	Gates BA to address bus
ADRS TO BUS	L	1	10	
DATA TO BUS	H	1	10	Gates data to bus on DATO or DATOB
DATA TO BUS	L	1	8	
END CYCLE	H	1	10	100 ns pulse indicating end of bus cycle
END CYCLE	L	1	8	
BUS MSYN	L	1	UNIBUS	Drives UNIBUS MSYN line
MSYN WAIT	H	1	10	200 ns pulse that delays assertion of MSYN
MSYN WAIT	L	1	8	
DATA WAIT	H	1	10	Allows for deskewing of DATA on DATI. Approximately 200 ns
DATA WAIT	L	1	8	
TIME OUT (1)	H	1	10	1 and 0 side of TIME-OUT Flip-Flop
TIME OUT (0)	H	1	10	

PIN M2	H	1	10	Output of one-shot
PIN T2	L	1	10	Output of one-shot
PIN V1	H	1	10	Outputs of flip-flop
PIN U1	L	1	10	

6.2.8 M920 UNIBUS Jumper Module

The M920 Module (see Figure 6-21) is a double module that connects the UNIBUS from one System Unit to the next. The printed circuit cards are on one-inch centers. A single M920 Module carries all 56 UNIBUS signals and 14 grounds.

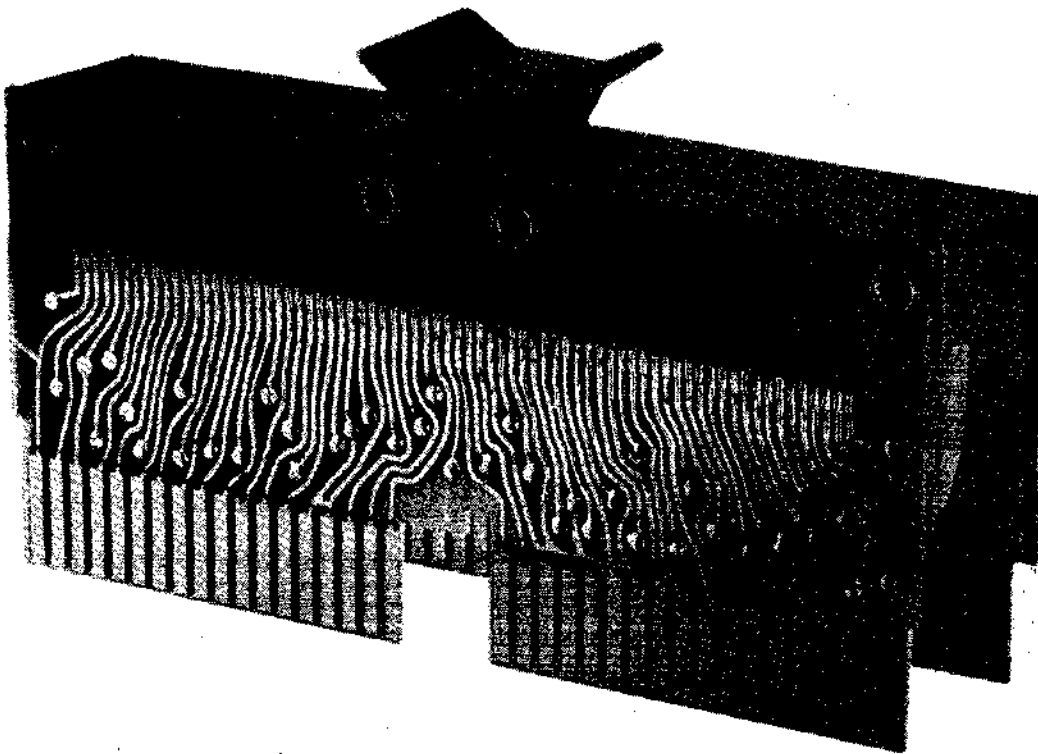


Figure 6-21 UNIBUS Jumper Module M920

6.2.9 M930 UNIBUS Terminator Module

The M930 UNIBUS Terminator Module is a short, double-size module that terminates all signal lines on the UNIBUS. This module requires 1.25 amps at $5V \pm 5\%$. All pins have a resistive divider termination of 178Ω to $+5V$ and 383Ω to ground, except those listed below:

383 Ω in parallel with 0.001 μ f to +5V (for AC LO, DC LO)	178 Ω +5V (for grant lines)	Ground Pins		+5V Input Pins
BF1 BF2	AV1 AU1 BA1 BB1 BE2	AB2 AC2 AN1 AP1 AR1 AS1 AT1 AV2	BB2 BC2 BD1 BE1 BT1 BV2	AA2 BA2

6.2.10 M7820 Interrupt Control Module

The M7820 Interrupt Control Module provides the circuits and logic required to make bus requests and to gain control of the bus (become bus master). The module also includes circuits needed to generate an interrupt, if desired. The module contains two completely independent request and grant acknowledge circuits (channels A and B) for establishing bus control. The interrupt control circuit can be used with either, or both, of the request channels and provides a unique vector address for each channel. Figure 6-22 is a block diagram of the M7820 Module, which is single-height.

The master control section (either channel A or B) is used to gain control of the bus. When the INTR and INTR ENB requesting inputs are asserted, a bus request is made on the BR level corresponding to the level of the BR line wired to the BR pin of the module. When the priority arbitration logic in the system recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the device has fulfilled all requirements to become bus master, the master control circuit asserts BBSY and then asserts a MASTER signal.

Once the device has gained bus control by means of a BR request, an interrupt can be generated. If an interrupt is desired, the module is interconnected as shown in Figure 6-23. This figure illustrates the use of the two channels to first generate requests for bus control and then initiate interrupts. The request from channel A is a slightly higher priority than the channel B request because the bus grant signal first enters A, then enters B.

The vector address is selected by jumpers on the M7820 Module. Since the vector is a two-word (four-byte) block, it is not necessary to determine the state of bits 0 and 1. The seven selectable lines determine vector address. The least significant line is controlled by the VECTOR BIT 2 input signal. If this input is asserted, then bus line D02 is asserted. Thus, the interrupt on channel A uses a vector at location 100 and channel B uses a vector at location 104.

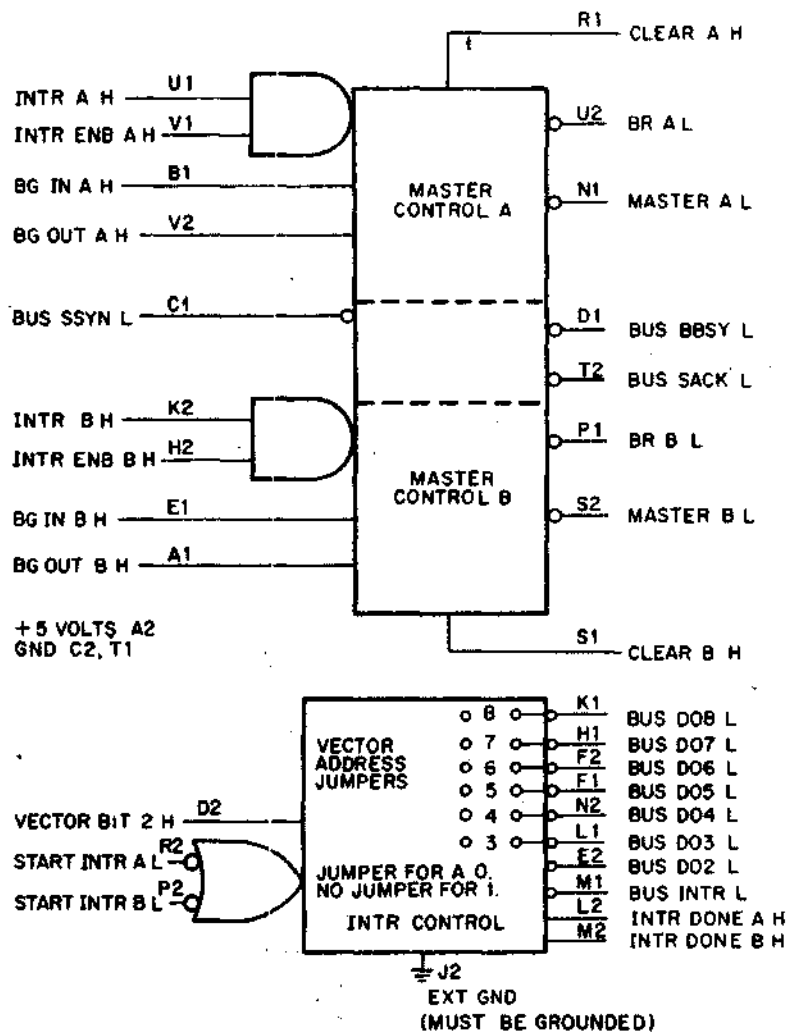


Figure 6-22 M7820 Interrupt Control (block diagram)

Figure 6-24 illustrates an M7820 Module used for bus control in a device that directly transfers data to memory and then causes an interrupt when the transfer is completed. Channel A is connected to the NPR and NPG lines and is used to gain bus control for direct to memory, or device-to-device, transfers. Channel B is used to gain bus control for an interrupt.

Each M7820 Module master control section contains two flip-flops that sequence through four states, thereby controlling the request for bus control. Figure 6-25 is a state diagram of this sequence and Figure 6-26 shows a circuit schematic of the M7820. The BG IN signal is allowed to pass through the module to BG OUT when the device is not issuing a request (state A), is master (state D), or has had the request honored (state E). To request bus use, the AND condition of INTR and INTR ENB must be satisfied. These levels must be true at least until the request is granted. Once bus control has been attained, it can be released by either asserting CLEAR or by negating either INTR or INTR ENB. The first

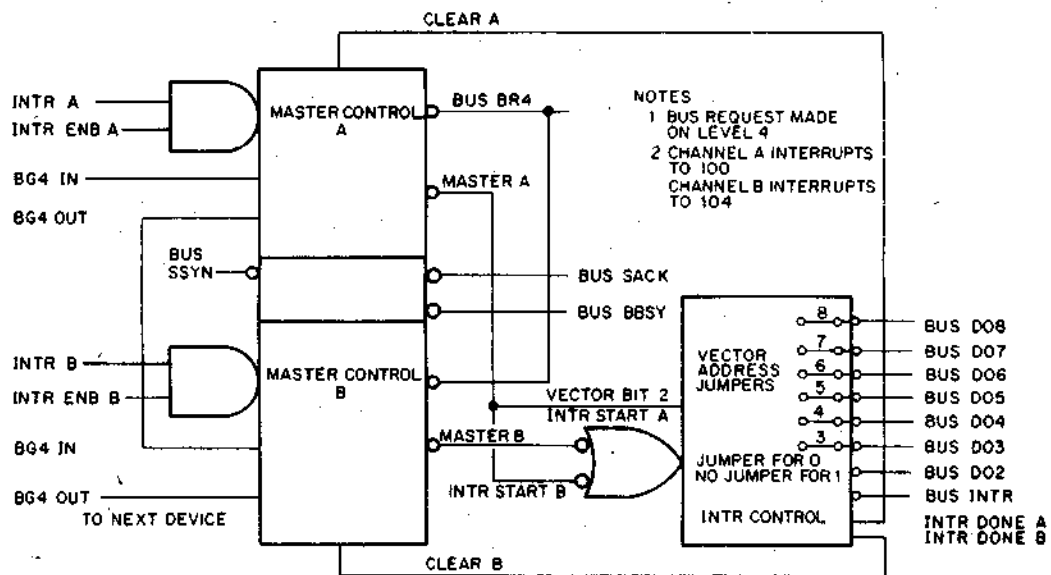


Figure 6-23 M7820 Interconnection for 2-Channel Interrupt

method leaves the master control in state E, thereby inhibiting further bus requests even if INTR and INTR ENB remain asserted. In order to make another bus request, INTR or INTR ENB must be dropped and then reasserted to cause the module to advance from state E through state A to state B where it asserts the request line. This prevents multiple interrupts when the master control is used to generate interrupts. The second method is used to release the bus after NPR use. Note that pin J2 (EXT GND) must be grounded by the user. A summary of all M7820 signals is listed in Table 6-9.

6-28

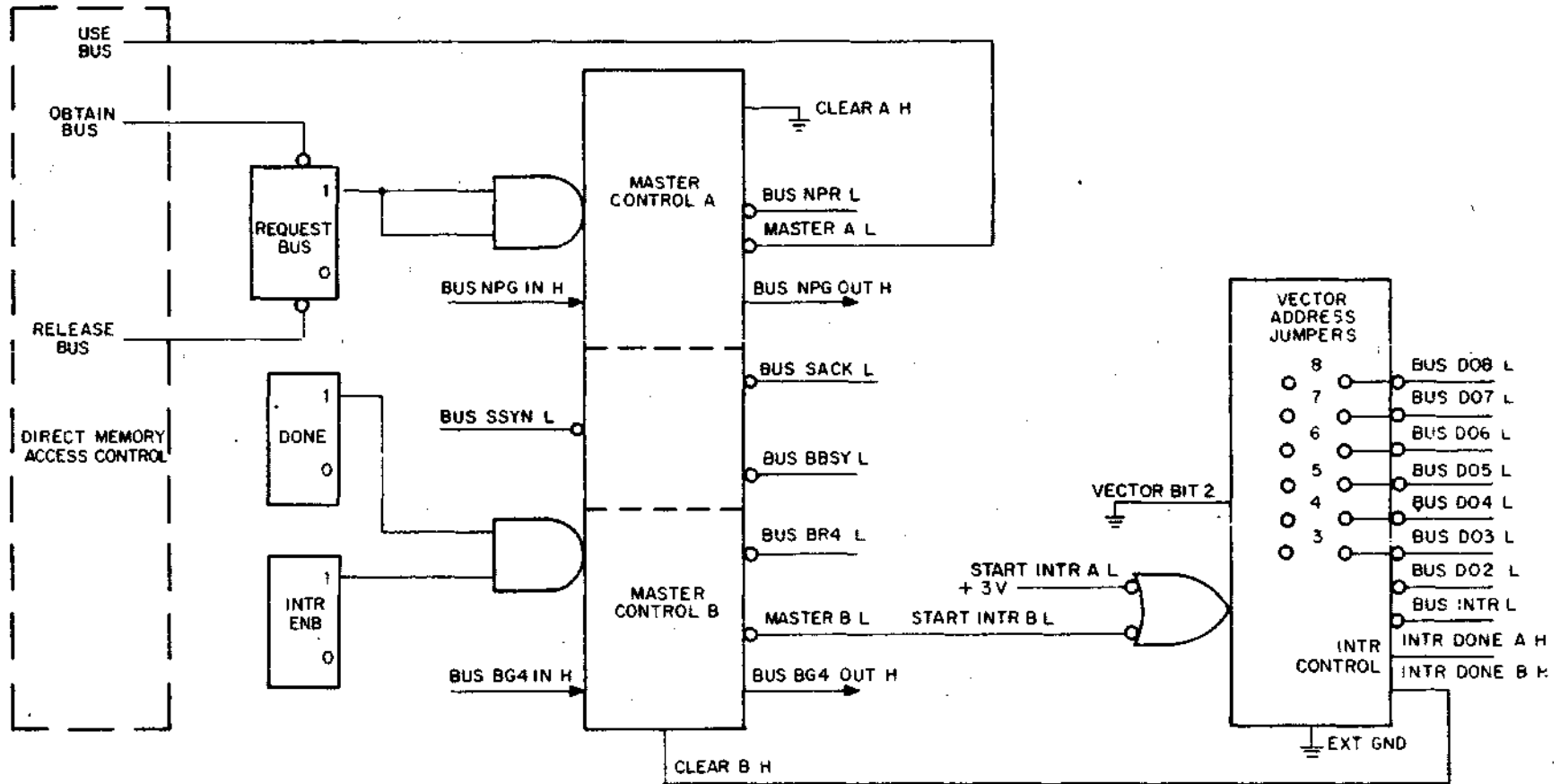
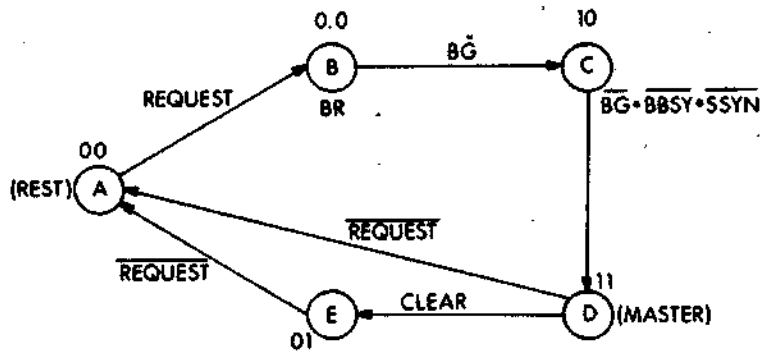


Figure 6-24 M7820 Interconnection for Direct Memory Access



The 2 binary numbers next to each circled state indicate the state of flip-flops FFA1 & FFA2 respectively, as shown in Figure 6-26.

Figure 6-25 State Diagram of M7820

Table 6-9 Summary of M7820 Signals

Signal	Assertion Level	Input Loading	Output Drive
INTR A, B	H	1 TTL (each)	
INTR ENB A, B	H	1 TTL	
CLEAR A, B	H	1 TTL	
MASTER A, B	L		10 TTL
START INTR A, B	L	2 TTL	
INTR DONE A, B	H		10 TTL
BG IN A, B	H	1 R*	
BG OUT A, B	H		2 D**
BR A, B	L		1 D
VECTOR BIT 2	H	1 TTL	
BUS SSYN	L	1 R	
BUS BBSY	L	1 R	2 D
BUS SACK	L		2 D
BUS INTR	L		1 D
BUS D <08:02>	L		D

* R = Standard UNIBUS receiver load.

** D = Standard UNIBUS transmitter (driver) output.

6.2.11 M7821 Interrupt Control Module

The M7821 Interrupt Control Module is a replacement for the M7820 that improves PDP-11 system performance. In almost all cases, it may be used directly in place of the M7820, without making any changes to hardware or software. A block diagram of the module is shown in Figure 6-27.

NOTE

The following description assumes the reader understands the function and operation of an M7820.

6-30

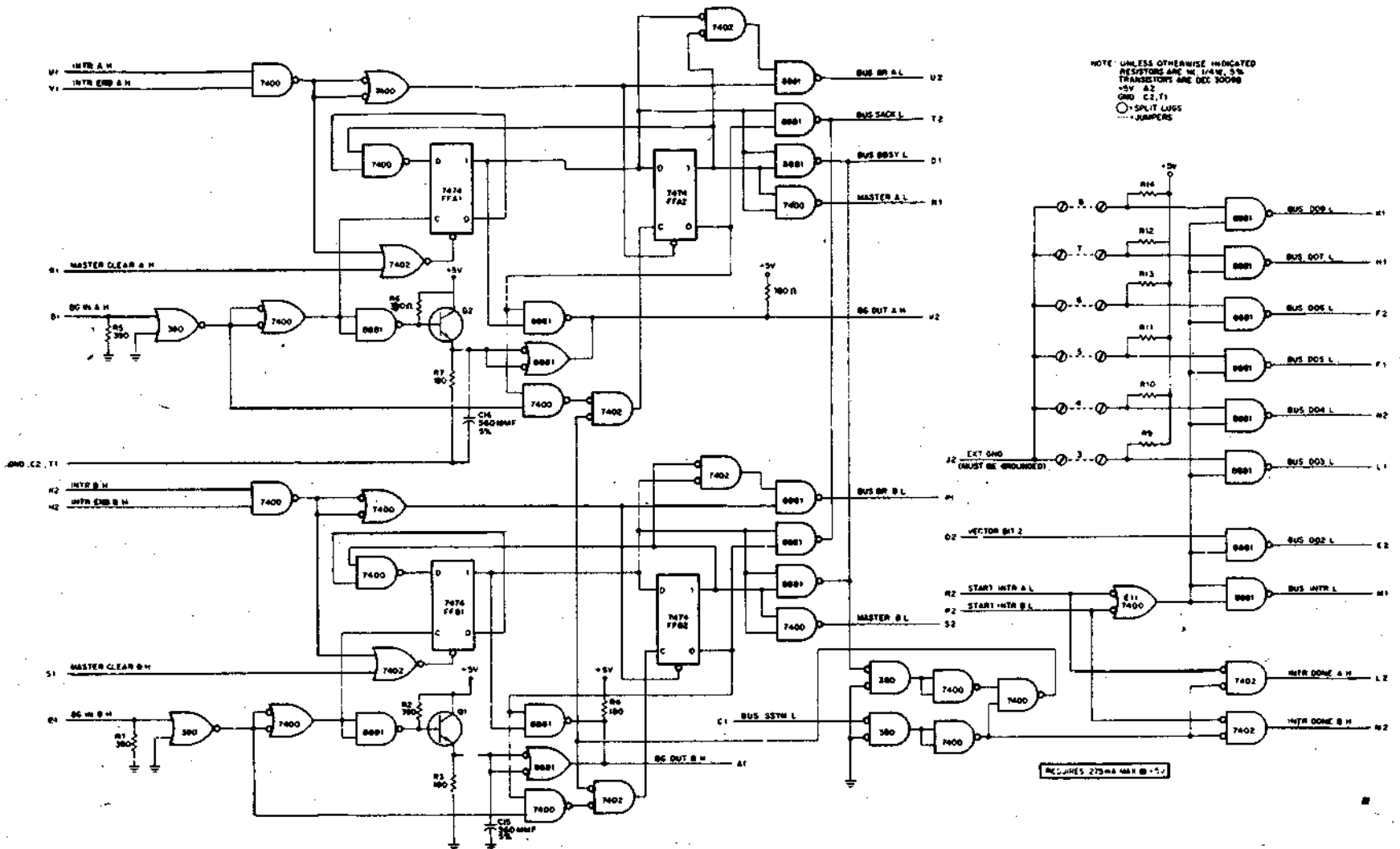


Figure 6-26 M7820 Interrupt Control (schematic diagram)

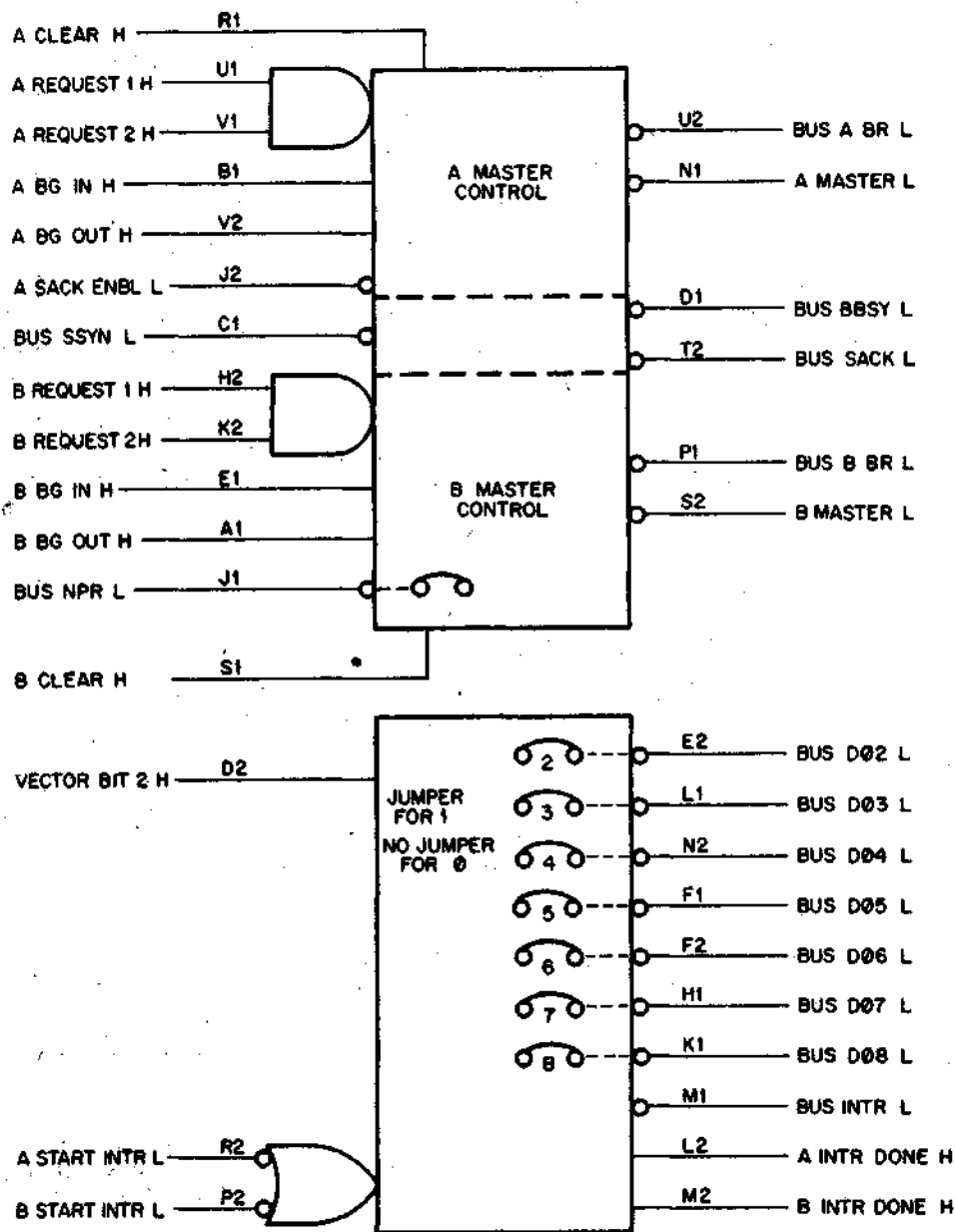


Figure 6-27 M7821 Interrupt Control Block Diagram

The M7821 does not have two identical Master Control halves. For devices which use one half of the module to become master with an NPR and one half for a BR, the top half (Request Bus pins U1 and V1) must be used for NPR and the bottom half (Request Bus pins H2 and K2) must be used for BR.

The NPR half of the module has the ability to prevent the un-assertion of BUS SACK for devices that do more than one data cycle each time they request the bus. This is done by holding pin J2 high until the beginning of the last bus cycle. SACK will be unasserted as soon as pin J2 goes low, and the input on J2 can, therefore, be a pulse or a level. Pin J2

is active only when the Master signal is asserted (pin N1 is low), and, therefore, pin J2 may be permanently grounded if only one bus cycle is done for each request.

NOTE

The M7820 requires pin J2 to be grounded for the interrupt section of the module to work, so the M7821 is compatible.

The BR half of the module does not have the ability to hold BUS SACK asserted and always drops SACK when BUS BBSY is asserted. However, this section of the module does have some special circuitry that looks at the BUS NPR line, which must be wired to pin J1 on the M7821. This circuitry, if it sees the assertion of the bus grant line to which the module is wired while BUS NPR is asserted, will block the grant and return SACK. When BBSY becomes unasserted from the last bus master, the M7821 will then clear SACK off the bus. The processor will then be able to service the NPR, improving the latency time for NPR devices.

CAUTION

Only some PDP-11 processors will work with the special circuitry described above. There is a jumper on the M7821 module which, when cut, prevents the special circuitry from working.

NOTE

Pin J1 is unused on the M7820 module, and if BUS NPR is not wired to this pin, the special jumper noted above must be cut.

If both halves of the M7821 are used for BR requests, pin J2 must be grounded and the jumper may be cut as required. If both halves are used for NPR requests, pin J2 may be used as required, and the jumper must be cut. Note that if the normally BR half (Request Bus pins H2 and K2) are used for NPR's, only one bus cycle may be done per request.

The interrupt section of the module has been changed slightly also. The jumpers on the M7821 module must be left in to generate a "one" in that bit position of the vector, and cut out to generate a "zero." This is the reverse of the M7820. A jumper has also been added to vector bit 2. If the module is to be used the same way as an M7820, the jumper for bit 2 must be left in. However, if only one vector is being generated by the module, pin D2 should be permanently wired to a high level, and then the jumpers can be used to assign vectors to every vector location (4 bytes) without changing backpanel wiring. Note that the jumper for bit 2 must also be in for a one and cut for a zero.

Summary of Compatibility Considerations

On the M7820, pin J2 must be grounded for the interrupt section to work. If pin J2 is grounded, then an M7821 module can be directly plugged in if the special jumper is cut, the vector bit 2 jumper is left in, and the rest of the jumpers are cut appropriately.

CHAPTER 7

INTERFACE EXAMPLES

Examples of interface designs in Paragraphs 7.1 to 7.9 use the techniques and equipment described in previous chapters. To draw attention to the design features of each interface type, a series of related examples is presented. The first example is a simple basic interface. Each additional example implements several features by adding logic circuits to the previous example. Thus, the first example is the simplest possible read/write interface. This circuit is then used with additional logic to form a program-controlled interface, which in turn is used with additional circuits to form an interrupt-serviced interface, until finally, the circuit is used with additional circuits to form a direct-memory-access interface.

The examples cover input and output transfers and also illustrate techniques for combining the two functions into one interface. Each example includes a description of the operation and logic of the interface, a typical implementation, and programming methods that might be used to operate a device with the interface.

7.1 BASIC INTERFACE

The simplest possible interface, a basic read/write interface, is used when data is transferred to and from the register during bus operations. This particular read/write interface consists of only a storage register and bus gating circuits. The register may be used either as a data register or may be used to drive an output device, such as a set of indicator lights.

7.1.1 Interface Operation

When the basic read/write is used, data transfers are under control of the program and the register is assigned an address on the UNIBUS. During execution of an instruction that addresses the interface, the processor conducts a bus data transfer with the interface register, which responds as a slave. Since a 16-bit register is used, it may be addressed as either a one word register or as two byte (8-bit) registers.

As shown in Figure 7-1, the basic interface uses an M105 Address Selector module to decode the UNIBUS address lines and to control the clocking of information into the register and the gating of output information from the register to the bus data lines. The register is interfaced to the bus input data lines by ungated receivers, and the inputs are clocked into the register by a strobing signal derived from the M105 Address Selector. The register outputs are gated through the drivers by the GATE REGISTER TO BUS signal. This output gating is necessary to prevent the register from affecting the UNIBUS data lines when the interface is not participating in a bus data transfer operation.

7.1.2 Data Transfer Operation

The read/write interface can participate in both DATI (or DATIP) and DATO (or DATOB) transfers. Whenever the processor conducts a DATO transfer to the bus address assigned to the read/write register, the data

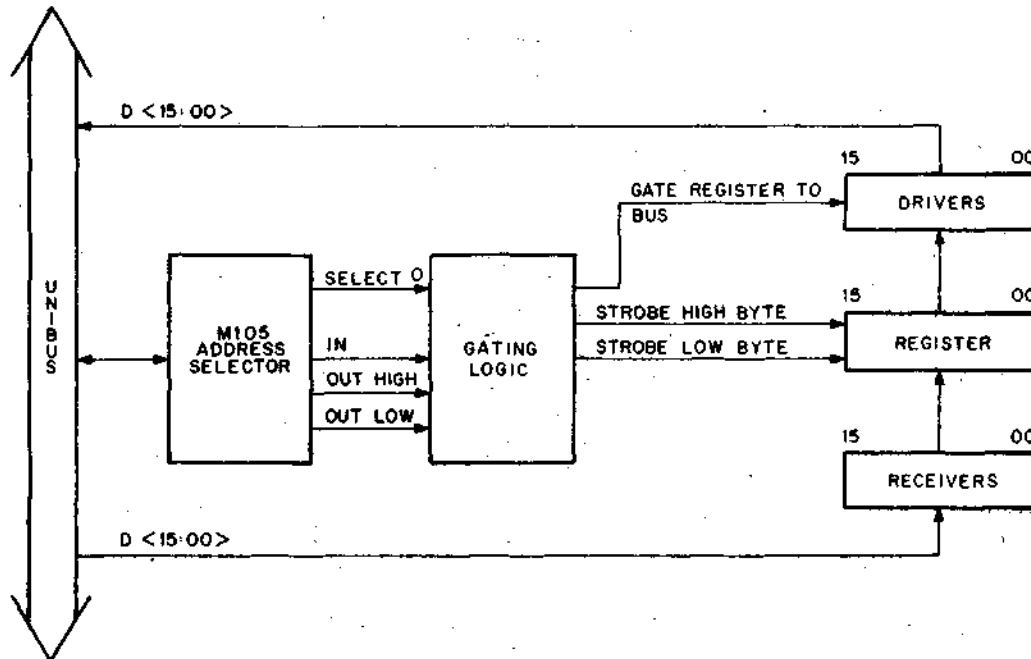


Figure 7-1 Basic Interface (block diagram)

is applied through the bus receivers to the register input. At this time, both the OUT HIGH and OUT LOW signals are produced by the M105 Address Selector. When MSYN is asserted by the processor, the decoded address causes the M105 to produce a SELECT 0 signal which is gated by the two OUT signals to clock data into the register. The UNIBUS timing guarantees that at the slave device data is valid 75 ns prior to assertion of MSYN. Therefore, the inputs have settled before the positive-going transition of the clock signal occurs.

A DATOB transfer functions in a similar manner, except that only one byte of the register is clocked. If address line A00 is 0, the M105 Module asserts OUT LOW but not OUT HIGH. If A00 is 1, then only OUT HIGH is asserted. In either case, data is only strobed into the appropriate byte of the register.

When a DATI transfer occurs, the processor addresses the interface and asserts MSYN. In addition, the M105 Module asserts the same SELECT 0 signal. However, in this case, the SELECT 0 is gated by the IN rather than the OUT signals. The IN signal is generated by the state of the bus C lines. Gating of the SELECT 0 signal by the IN signal produces a GATE REGISTER TO BUS signal that gates the output data from the register to the UNIBUS. The M105 Module generates SSYN to indicate that data is ready on the output bus data lines.

7.1.3 Circuit Implementation

Figure 7-2 illustrates a possible method of implementing the circuits in the basic read/write interface. The types and quantities of modules used are: the M105 Address Selector Module (one); the M785 Bus Transceiver Module (two); the M206 General-Purpose Flip-Flop Module (three); and the M617 4-Input Power NAND Gate Module (one). The modules are interconnected and may be mounted in a BB11 System Unit as shown in the insert on Figure 7.2.

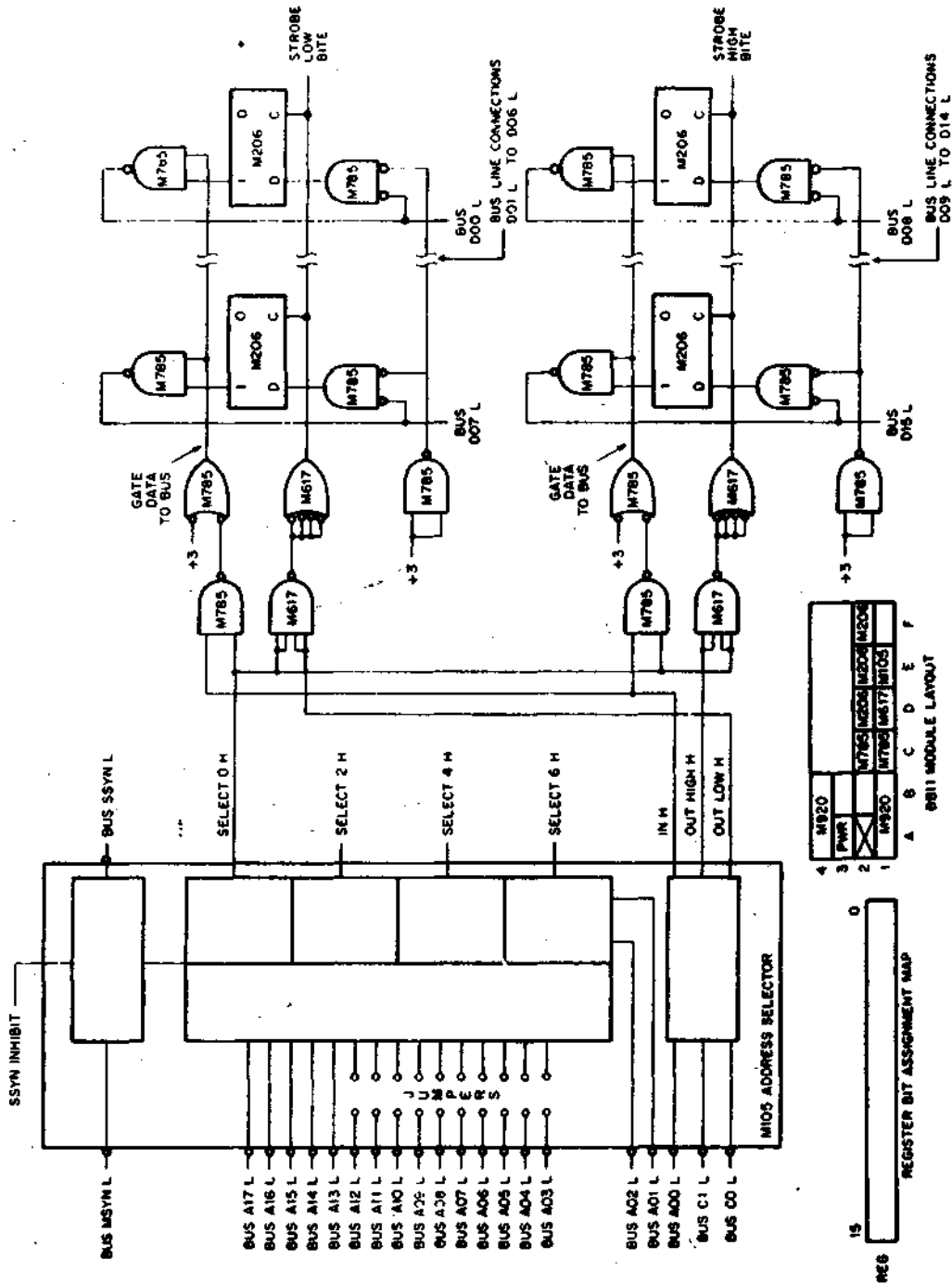


Figure 7-2 Basic Interface (schematic diagram)

Input data flows from the UNIBUS, through the input gates on the M785 Modules, to the data inputs of the M206 Flip-Flops comprising the register. The gating provided on the M785 Receivers is not used, and all gates are wired to continuously receive data. Data stored in the register is protected from these changing inputs by the requirement for a clocking signal to load data into the register.

The output data from the register is gated to the bus data lines through the driver sections of the M785 Modules. The M785 Modules are used in this example because the M785 provides the exact combination of input and output gates needed for an 8-bit read/write register. When the number of receivers differs from the number of drivers required in a specific interface, combinations of M783 Bus Driver Modules and M784 Bus Receiver Modules may be used. This example is devoted to illustrating the use and interconnection of bus drivers and receivers rather than indicating the specific modules used in implementation.

7.1.4 Programming the Interface

All data transfers in the basic read/write interface are under processor control, and all memory reference instructions may directly address the interface. If the mnemonic REG is assigned to the register address, the instruction MOV REG, R4 reads the data stored in the register (a DATI operation) and places the data in general register 4 of the processor. The instruction MOV R4, REG reverses the data flow so that the data in general register 4 is placed in the interface register (a DATIP, DATO operation). Any instruction that can access a bus address can conduct data transfers with the interface register. Therefore, the contents of the register may be incremented by an INC REG instruction or summed with an arbitrary value by an ADD VALUE, REG instruction.

7.2 PROGRAMMED DEVICE INTERFACE

A circuit similar to the one in the preceding example is used as the basis for the program controlled interface to an analog-to-digital converter (ADC). The ADC is simply a representative example of many possible external devices that may be interfaced with a design similar to the one discussed in this section. The ADC input and output signals, however, are covered in the following paragraph because of the requirements they place on the interface.

7.2.1 Analog-to-Digital Converter

The analog-to-digital converter used in this example consists of a multiplexer and converter. (See Figure 7-3.) The multiplexer selects one of 64 analog inputs and applies it to the converter, which produces the digital equivalent of the analog input.

The interface must provide seven input control signals to the ADC. One input is the START CONVERSION signal, which is a positive transition that causes the ADC to begin the conversion process. The other six control signals are applied to multiplexer address lines so the ADMUX register can be used to select one of the 64 analog inputs.

The interface receives 11 output signals from the ADC. One of these is the CONVERSION COMPLETE signal. When the conversion process starts, the CONVERSION COMPLETE signal becomes OV and remains at that level until the conversion is finished. At that time the signal becomes + 3V to

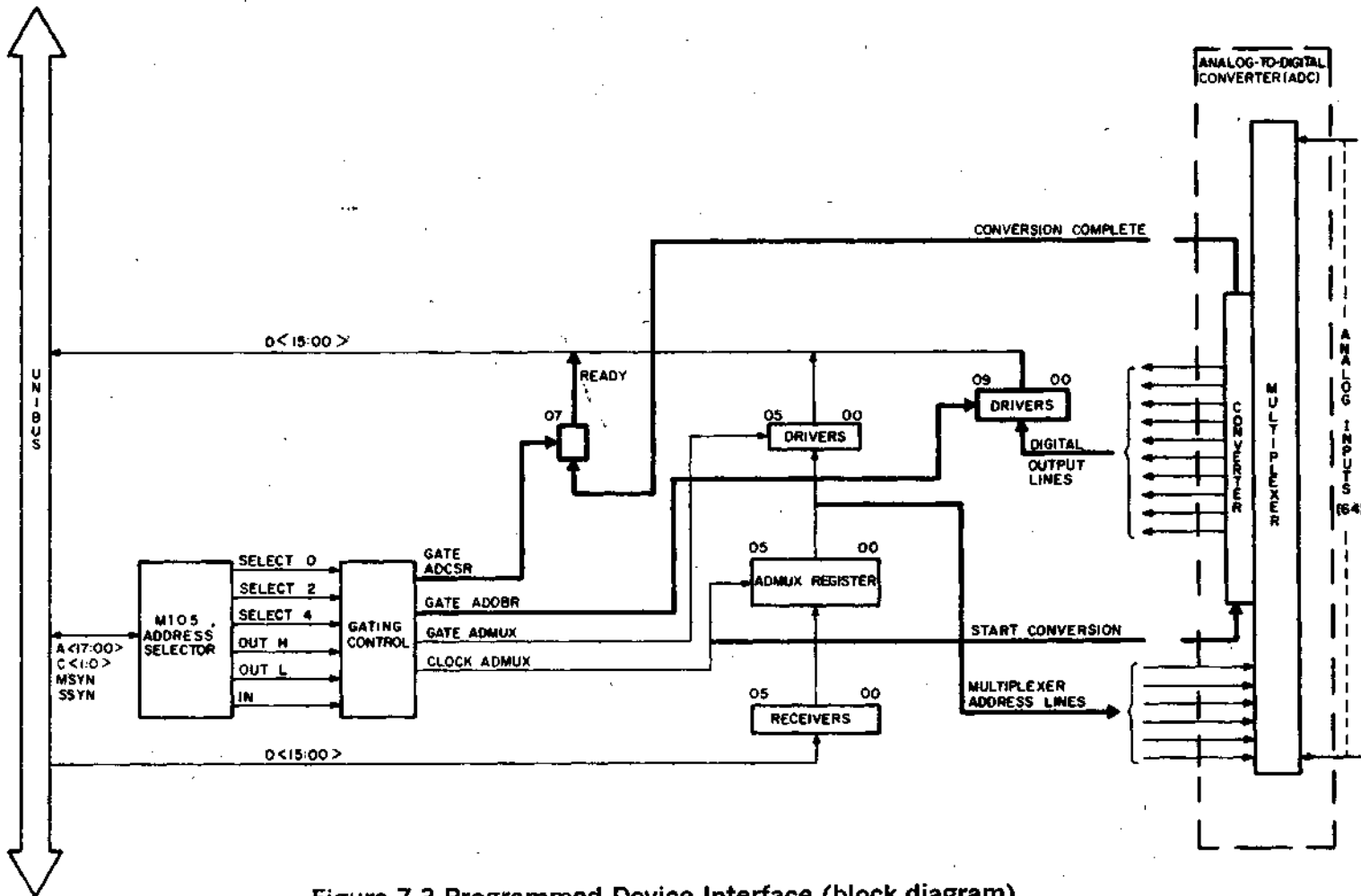


Figure 7-3 Programmed Device Interface (block diagram)

indicate that the digital output reflects the analog input (the conversion is complete).

The remaining ten output lines represent the digital equivalent to the analog input. A zero on any line is indicated by OV and a one is indicated by + 3V.

Signal levels used in the interface are standard DEC levels.

7.2.2 Interface Description

The program controlled interface allows the program to select a specified analog input for application to the ADC and then causes the resultant digitized output and conversion complete signal to be placed on the UNIBUS data lines to transfer data into the bus master.

The heavy lines in Figure 7-3 indicate logic added to the interface of the previous example. The interface functionally operates with three bus addresses. One address is assigned for the multiplexer (ADMUX) register, which is similar in design to the register in the previous interface example. The second address is for the converted digital output (ADDBR) of a read-only register, and the third address is assigned to a 1-bit control and status register (ADCSR).

The M105 Module decodes the bus address to produce one of three select signals depending on which register is being accessed. The three select signals are gated by IN and OUT LOW to produce the four signals (GATE ADCSR, GATE ADDBR, GATE ADMUX and CLOCK ADMUX) shown in Figure 7-3. Only the ADMUX register accepts inputs from the UNIBUS through the receivers. However, the outputs of all three registers are gated to the bus through separate sets of bus drivers.

Connections between the ADC and interface may be made by a cable connector such as the M908 Module.

7.2.3 Transfer Operations

The program controlled interface participates in bus data transfers in substantially the same manner as the basic interface described in Paragraph 7.1. Each of the three interface registers can be read during a DATI operation. In addition, the multiplexer (ADMUX) register can be loaded by a DATO operation. Although only the multiplexer register accepts data during a DATO, the other two registers respond when a DATO cycle occurs. If any of the three registers is addressed during a DATO, the M105 Module produces SSYN to complete the bus operation. This is necessary to operate the interface with the processor because the destination operand of all instructions that reference data (except TST, CMP, and BIT) is transferred by a DATIP, DATO sequence of bus operations. If the interface does not respond to the DATO operation, the processor cannot continue with the program.

7.2.4 Circuit Implementation

Figure 7-4 includes a map of bit assignments for the three registers and a layout for mounting the logic modules in a BB11 System Unit. Neither the M105 Address Selector Module nor the ADC is shown on the figure, but the signals generated by these units are indicated. The connections to the UNIBUS can be implemented with one M785 UNIBUS Transceiver Module for the multiplexer register and one M783 UNIBUS Transmitter

Module for the data and control registers. Separate gating must be supplied to use one of the four individual bus drivers on the M783 for a READY bit. The CONVERSION COMPLETE signal is renamed to READY after it passes through the bus transmitter.

7.2.5 Programming the Interface

The START CONVERSION signal, which begins the device cycle, is generated in this interface by the CLOCK ADMUX signal, which loads the multiplexer register. In normal operation, the processor loads the multiplexer register; this action starts the ADC; tests the READY (CONVERSION COMPLETE) bit until the bit is set; and then transfers the data from the digital output lines of the ADC to the processor. A possible sequence of instructions to perform this task is given below. This program selects an input, waits for the device to complete the conversion, and then transfers the result to register 4.

```

READY:   MOV   INPUT, ADMUX   ;SELECT ANALOG INPUT
         TSTB  ADCSR         ;CHECK FOR CONVERSION COMPLETE
         BPL   READY         ;NO, TEST AGAIN
         MOV   ADDBR, R4     ;YES, OBTAIN DATA

```

INPUT IS A LOCATION CONTAINING THE NUMBER OF THE DESIRED ANALOG INPUT LINE.

A SUBROUTINE TO EXAMINE A SERIES OF INPUTS MIGHT BE WRITTEN AS FOLLOWS:

```

MUXSCN:  MOV   BUFADR, R4    ;INITIALIZE DATA POINTER
         CLR   ADMUX        ;SELECT INPUT LINE ZERO
LOOP:    TSTB  ADCSR        ;CHECK FOR CONVERSION COMPLETE
         BPL   LOOP        ;NO, TEST AGAIN
         MOV   ADDBR, (R4) + ;YES, PLACE DATA IN BUFFER
         CMP   ADMUX, #77   ;LAST LINE?
         BEQ   DONE        ;YES, GO TO DONE
         INC   ADMUX        ;NO, GO TO NEXT INPUT
         BR    LOOP        ;GO TO LOOP
DONE:    RTS   R7           ;EXIT FROM SUBROUTINE

```

WHERE: BUFADR IS A LOCATION IN CORE CONTAINING THE ADDRESS OF THE FIRST WORD ON A 64-WORD BUFFER
 ADCSR IS THE INTERFACE STATUS REGISTER
 ADMUX IS THE MULTIPLEXER REGISTER
 ADDBR IS THE DATA REGISTER

This subroutine is called by the instruction: JSR R7, MUXSCN. The subroutine initializes general register 4 as a pointer to the buffer; initializes the multiplexer register to zero; and sequentially reads the 64 inputs into the corresponding buffer location. When each input has been read once, control returns to the calling program with the contents of general register 4 as the address of the word after the last word of the buffer.

Since loading the multiplexer register starts operation of the device cycle, ADMUX should not be accessed as a destination operand except by a TST, BIT, or CMP instruction. In addition, the INC ADMUX instruction should follow the CMP instruction. This avoids initiating unwanted device operation and allows the subroutine to be immediately recalled.

7.3 INTERRUPT SERVICED INTERFACE

The interface to an analog-to-digital converter would be more versatile if it included an interrupt capability. An interrupt serviced interface with this capability can be formed simply by adding an M7820 Interrupt Control Module and one bit to one of the registers in the programmed device interface described in Paragraph 7.2.

The interrupt serviced interface allows the processor to concurrently execute instructions of another program while the analog-to-digital converter (ADC) performs a cycle of operation. The processor responds to a READY (CONVERSION COMPLETE) signal from the ADC by interacting with the device and analyzing the data after it has been collected. This interface eliminates requiring the processor to spend time testing for a ready signal, such as in the case of the programmed device interface.

Whenever a device interface is required, the designer must compare the cost of additional interrupt hardware with the device requirements in terms of transfer speed, frequency of transfers, and amount of use, to determine whether a programmed device interface or interrupt serviced interface is more economical.

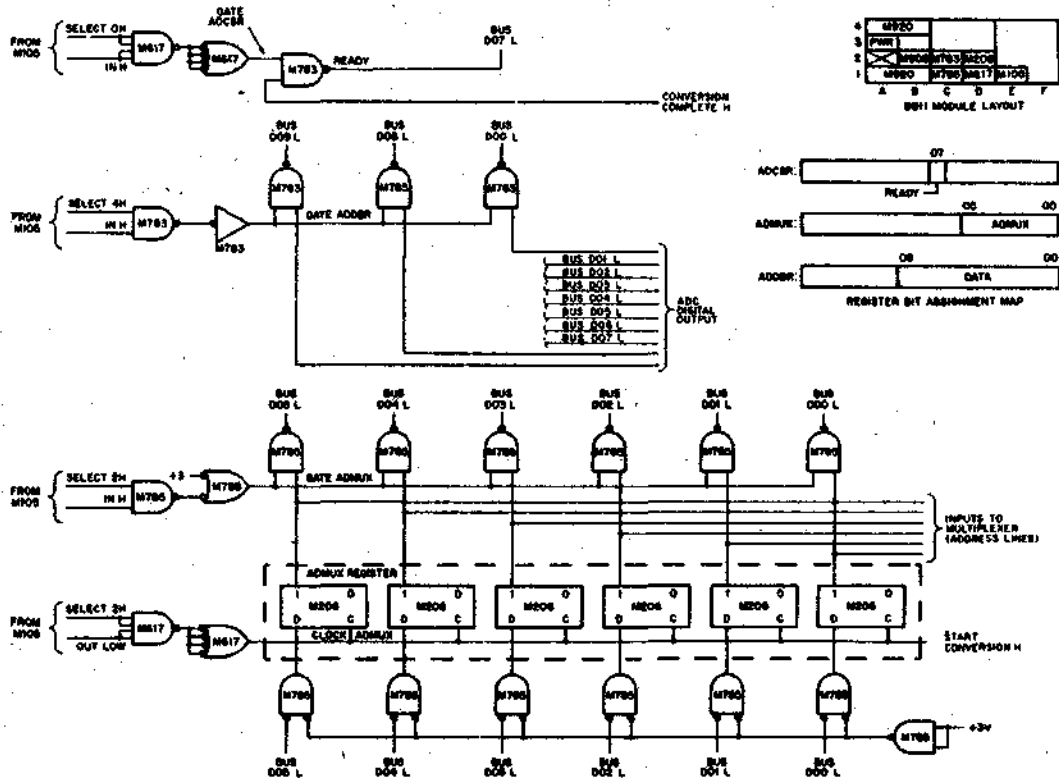


Figure 7-4 Programmed Device Interface (schematic diagram)

7.3.1 Interface Description

Figure 7-5 is a block diagram of the interrupt serviced interface which consists of the programmed device interface with the addition of an M7820 Interrupt Control Module, one flip-flop, and one bus driver. This interface can operate either in the same manner as the interface de-

scribed in Paragraph 7.2 or in an interrupt mode. The additional flip-flop is used to enable or disable interrupt operations. If the flip-flop (which is bit 6 of the control status register) is set by the program, the CONVERSION COMPLETE signal from the ADC causes the M7820 Interrupt Control Module to initiate an interrupt.

7.3.2 DR11-C Implementation

A convenient method of implementing an interrupt serviced interface is to use a DR11-C 16-Bit General Interface, Figure 7-6. A layout of the module mounted in a DD11-A System Unit, shows the savings in space and interconnections. The DR11-C is functionally equivalent to an M105, M7820, and M786. The DD11-A System unit is prewired to accept four small peripheral interfaces; e.g., DR11-C. A discussion of the DR11-C, including specifications, is presented in Chapter 4.

Figure 7-7 is similar to Figure 7-5 because the DR11-C logic is used in the same manner and with the same programs as any other logic used to implement an interrupt serviced interface. The DR11-C provides cable connectors; therefore, no additional wiring or connectors are required.

Connections between the ADC and the DR11-C are made as follows:

<u>CONNECTOR</u>	<u>DR11-C</u>	<u>ADC</u>
1	OUT (06:00) NEW DATA READY	Multiplexer inputs Start conversion
2	IN (09:00) REQUEST A	Digital outputs Conversion complete

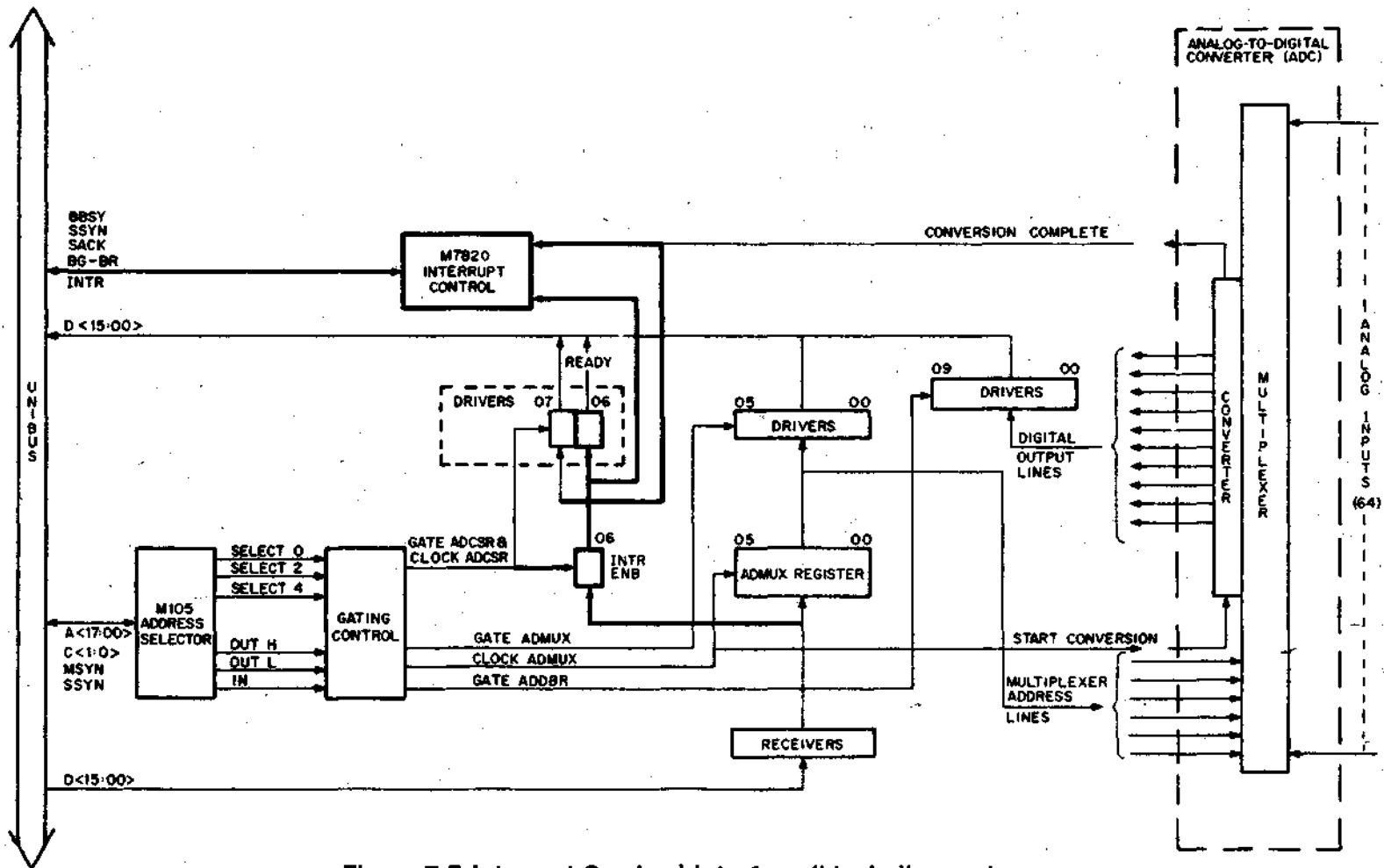


Figure 7-5 Interrupt Serviced Interface (block diagram)

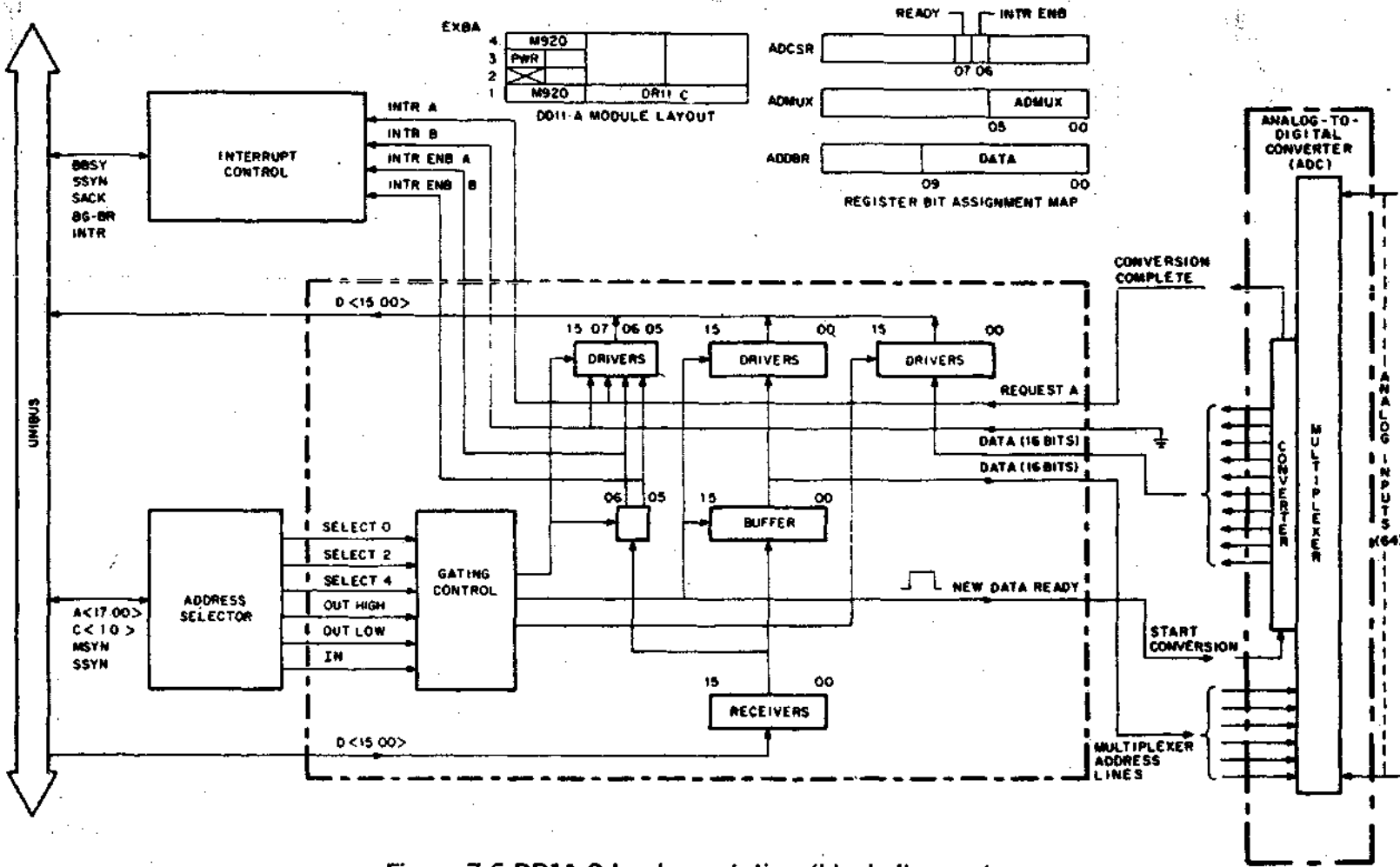


Figure 7-6 DR11-C Implementation (block diagram)

7.3.3 Interface Programming

The following program is a typical interrupt service routine that collects data from the ADC and enters an evaluation routine after the final conversion cycle.

```
ADCVEC: ADCSER                                ;SET UP ADC VECTOR AREA
        240                                ;STATUS INCLUDES PRIORITY
        .                                  LEVEL 5
        .
        .
BEGIN:  MOV BUFSTRT, BUFADR                    ;MAIN PROGRAM FOLLOWS
        CLR ADMUX                            ;INITIALIZE BUFFER POINTER
        MOV #100, ADCSR                       ;START MULTIPLEXER AT
        .                                    CHANNEL 0
        .                                    ;ENABLE INTERRUPT
        .
ADCSER: MOV ADDBR, @BUFADR                    ;COLLECT DATA
        CMP BUFADR, BUFSTRT + 174            ;LAST ONE?
        BEQ DONE                             ;YES, GO TO DONE
        ADD #2, BUFADR                       ;NO, INCREMENT POINTER
        INC ADMUX                            ;INCREMENT MULTIPLEXER AND
        .                                    ;START CONVERSION
        .                                    ;RETURN TO MAIN LINE
DONE:  RTI                                    ;CLEAR INTERRUPT ENABLE
        CLR ADCSR
        .
        .                                    ;FOLLOW THIS WITH THE
        .                                    ;EVALUATION ROUTINES
```

WHERE: ADCSR, ADMUX AND ADDBR ARE THE DEVICE REGISTERS
IN THE INTERFACE
BUFSTRT CONTAINS THE STARTING ADDRESS OF A BUFFER
ADCVEC IS THE ADDRESS SPECIFIED BY JUMPERS ON THE
M782 MODULE AND CONTAINS THE ADDRESS OF
THE DEVICE SERVICE ROUTINE TAGGED ADCSER
ADCSER DEVICE SERVICE ROUTINE

BUFADR IS A LOCATION TO BE USED BY THE DEVICE SERVICE ROUTINE

After the initiation instructions in the main program are executed, the interrupts cause the processor to execute the ADCSER routine. The last time this is performed, the evaluation routine is also executed.

The CLR ADMUX instruction should precede the MOV #100, ADCSR instruction to prevent the interface from causing an immediate interrupt, which could occur if the interrupt enable bit is set when the device has the CONVERSION COMPLETE signal asserted.

If the evaluation routine is to return control to the interrupted main program, this may be accomplished by terminating the evaluation routine with an RTI instruction. If any other type of return is used, the program must remove the old PC and PS that were placed on the stack by the interrupt operation. Removal is accomplished by executing an ADD #4, R6 instruction.

The direct memory access (DMA) interface conducts data transfer operations to place data from the device directly into memory. A DMA interface performs a large number of transfers with minimal processor intervention thereby reducing program and execution time overhead. After the interface device registers are initialized, all transfers take place under control of the interface, thereby eliminating processing time. The processor is notified by an interrupt when all the data has been transferred and the program responds appropriately.

Figure 7-7 is a block diagram of a DMA interface for the Analog-to-Digital Converter (ADC). The DMA is designed by adding circuits to the interrupt serviced device interface. The Interface is composed of two interface registers: the ADCSR register, which contains flag and error bits; and the combined ADBAR/ADMUX register, which holds the bus address and multiplexer bits.

7.4.1 Interface Description

Interface operation begins when the program loads the bus address register (ADBAR) with the address of the first memory location where data is to be stored. The interface starts an ADC conversion cycle. When the digital data is available from the ADC, the interface requests bus use by asserting an NPR request. When the device becomes bus master, it transfers the data to core memory. Completion of the bus transfer causes the multiplexer register (ADMUX) to be incremented, thereby selecting the next input channel. The multiplexer register is part of the bus address register; therefore, the next memory location is also selected. At this point, a new conversion cycle begins. This process is repeated until each input channel is read and the digital data is stored in a core memory location. The interface then sets the ready flip-flop, which causes an interrupt.

7.4.2 Interface Implementation

The DMA interface is constructed by adding one set of bus drivers and the bus transfer control logic to the interrupt serviced interface; therefore, the functions assigned to the registers differ in this case, and implementation differs accordingly. The multiplexer register, expanded to 15 bits, also serves as a bus address register. Nine of these bits (15:07) are under program control and serve as a base address for a series of locations used as a data collection buffer by the interface. The remaining six bits (06:01) are implemented as a counter that steps through the 64 inputs and also addresses 64 successive word locations in the core memory. The six multiplexer bits are not accessible from the bus and cannot be read nor altered by the program. Whenever the high or low byte of the address register is loaded, the six multiplexer bits are cleared to zero; therefore, transfers always start on 64 word boundaries.

The interface uses an interrupt to signal completion of the series of transfers. The interrupt enable (INTR ENB) and READY bits of the ADCSR operate similar to the interrupt serviced interface. Refer to Figure 7-7.

Loading the ADBAR register (SELECT 2 · OUT HIGH and/or SELECT 2 · OUT LOW) also clears the multiplexer counter and the READY flip-

START CONVERSION H to become asserted.

When the conversion is complete, the CONVERSION COMPLETE H signal sets the REQUEST BUS flip-flop, which causes the M7820 Interrupt Control to assert an NPR request. When bus control is granted, the M7820 asserts BBSY on the UNIBUS and asserts the MASTER A L signal. The MASTER A L signal is tied to the M796 UNIBUS Master Control module in order to produce the START signal. Since the C1 control line is high and the C0 control line is grounded, the M796 performs a DATO bus cycle. An ADRS TO BUS H is produced to gate the nine bits of the ADBAR register and the six bits of the ADMUX register to bus address lines A<15:01>. DATA TO BUS places the converted digital value on bus data lines D<09:00>. After a minimum delay of 150 ns, BUS MSYN L is asserted.

When the slave device responds with BUS SSYN L, both ADRS TO BUS and DATA TO BUS are negated and BUS MYN L is dropped. The END CYCLE H pulse is used to clear the REQUEST BUS flip-flop, which in turn causes the M7820 Interrupt Control to drop BUS BBSY.

END CYCLE L is used to trigger a one-shot to produce the COUNT DELAY H signal. This signal serves as the count input (COUNT IN) to the multiplexer counter (ADMUX). After 600 ns, the one-shot times out and its output returns to a low (0V) level. If the READY flip-flop has not been set by a count overflow from the ADMUX counter, START CONVERSION H is asserted to start the next conversion cycle. If, however, the ADMUX counter has overflowed and set the READY flip-flop, no ADC operation is started and an interrupt bus request is made.

A TIME-OUT flip-flop is provided on the M796 module. This flip-flop is set if the slave does not respond within 20 μ s to the BUS MSYN L signal that is produced by the M796 module. If TIME OUT becomes set, the bus cycle is stopped, READY is set, and further conversions are inhibited. The TIME-OUT ERROR is indicated by a 1 in bit 15 of the ADCSR. TIME-OUT is cleared by loading bit 15 of the ADCSR with a 0.

The modules required to implement this interface fit into one BB11 System Unit. All interface modules, including the M7820 Interrupt Control, M105 Address Selector, and a device cable connector, can be inserted into the logic slots of one system unit containing power and UNIBUS connectors.

7.4.3 Programming the Interface

The following is an instruction sequence to initiate device operation:

```
MOV #BUFADR, ADBAR ;LOAD ADDRESS AND START  
MOV #100, ADCSR ;ENABLE INTERRUPT
```

WHERE: BUFADR IS THE ADDRESS OF THE FIRST WORD OF A BUFFER AND IS RESTRICTED TO ALL 0'S IN BITS 0 THROUGH 6.

The interrupt routine for this interface is equivalent to the data evaluation routine suggested in the interrupt serviced interface. The routine should begin with a CLR ADCSR instruction to disable further interrupts

(unless serviced at a higher priority level) and should terminate with an RTI instruction.

The ADBAR register can be read as a source operand without spurious clocking of the device operation cycle, but the ADMUX counter is not accessible from the bus.

The interrupt enable flip-flop (bit 6 of the ADCSR) is entirely under program control but the TIME-OUT flip-flop is set by TIME-OUT ERROR conditions in the interface. The ready bit of the ADCSR (bit 7) is not under program control. It may be read by the program but cannot be altered except by initiating operation of the device.

7.4.4 Interface Operation Timing

Figure 7-8 illustrates the timing relationship among signals in the DMA interface. The curved lines indicate the changes in signal level that generate the indicated results.

7.4.5 Interface Options

As described above, operation of the DMA interface is restrictive, because it must always scan 64 channels. A simple method of reducing the number of channels scanned is to alter the set/reset inputs to the M211 Binary Counter module, thereby preloading it with a non-zero constant from which it can begin counting up.

An even more flexible arrangement could be designed by separating the ADBAR and ADMUX registers, thereby allowing independent bus addressing and multiplexer scanning.

7.5 OUTPUT INTERFACE WITH INTERRUPT CONTROL

Preceding examples have illustrated various types of interfaces for peripheral devices that provide inputs to the UNIBUS data lines. This example, as well as the example in Paragraph 7.6, covers interface design for a device that accepts UNIBUS outputs. The device shown is meant to be typical of output devices which may be interfaced by designs similar to the following examples.

7.5.1 Device Description

A digital-to-analog converter (DAC) is a device that accepts UNIBUS outputs. The DAC converts a binary weighed number into a scaled analog voltage. The device is single-buffered and the analog output corresponds to the digital input.

The interface provides 10 binary level inputs to the DAC. These inputs represent the digital value equivalent to the analog voltage desired as an output. The binary levels are 0V for logic 0 and + 3V for logic 1.

The DAC provides an update request output signal for the interface. This signal requests a new digital input from the interface. At intervals determined by the DAC, a high level (+ 3V) pulse is provided as the update request signal. This level remains low (0V) between pulses.

7.5.2 Interface Description

The output interface with interrupt control provides a buffer register for outputs to the DAC and an interrupt control to service the DAC with an interrupt service routine. Figure 7-9 is a block diagram of the output interface.

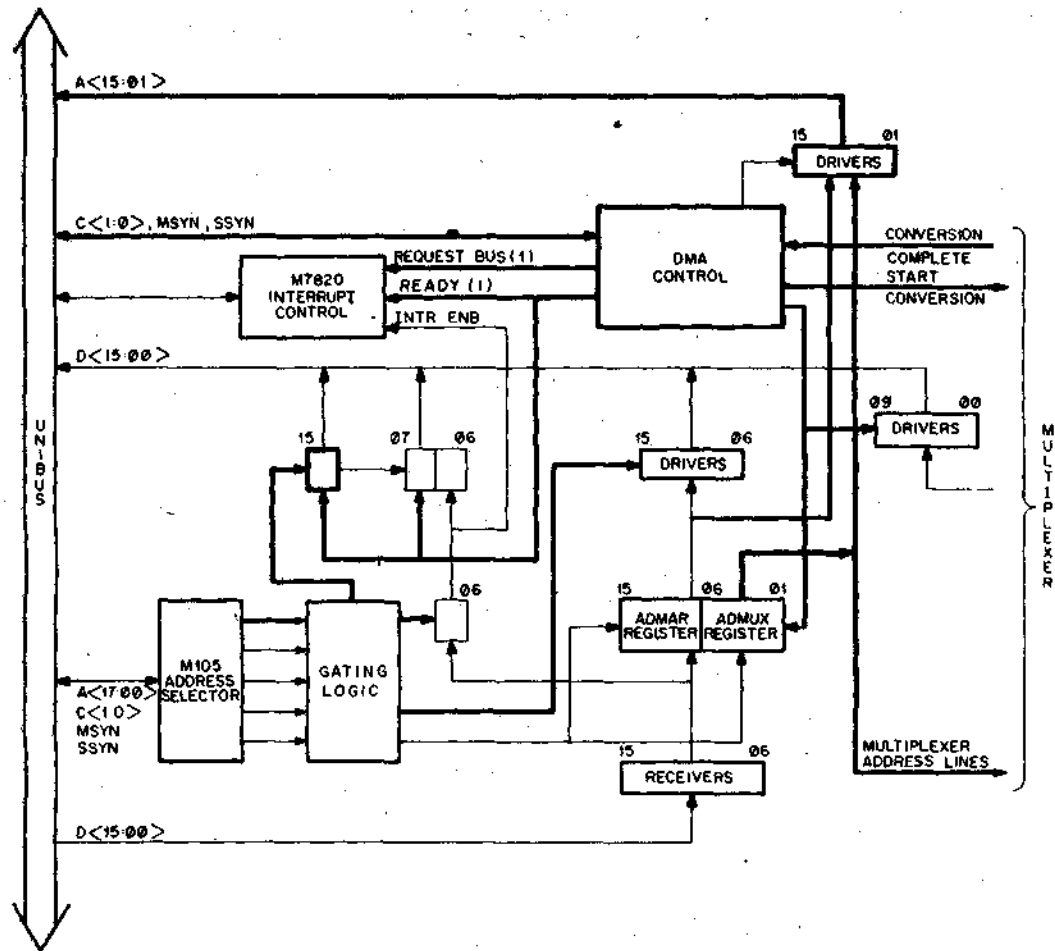


Figure 7-7 DMA Interface (block diagram)

The interface consists of two registers, an M105 Address Selector Module, an M7820 Interrupt Control Module, bus receivers, and two sets of bus drivers. The two registers are the data buffer register (DADBR) and the control status register (DACSR). The request bit (bit 7) of the DACSR can be read by the bus but cannot be loaded directly from the bus. All other register bits are under direct bus control.

7.5.3 Interface Operation

When the UNIBUS addresses the data buffer register during a DATO transfer, the interface clocks the information from the bus data lines into the register, which then applies the information to the DAC as the 10 binary level inputs. At the same time data is clocked into the register, the REQUEST flip-flop (bit 7 of the DACSR) is cleared. After this transfer is complete, when the peripheral device requests another value, the REQUEST flip-flop is clocked high by an UPDATE REQUEST signal from the DAC. If the interrupt enable flip-flop (bit 6 of the DACSR) is set, the interface asserts a bus request line. On becoming bus master, the interface performs an interrupt operation to transfer program control to a service routine. This routine loads new data into the buffer register and then returns control to the interrupted program.

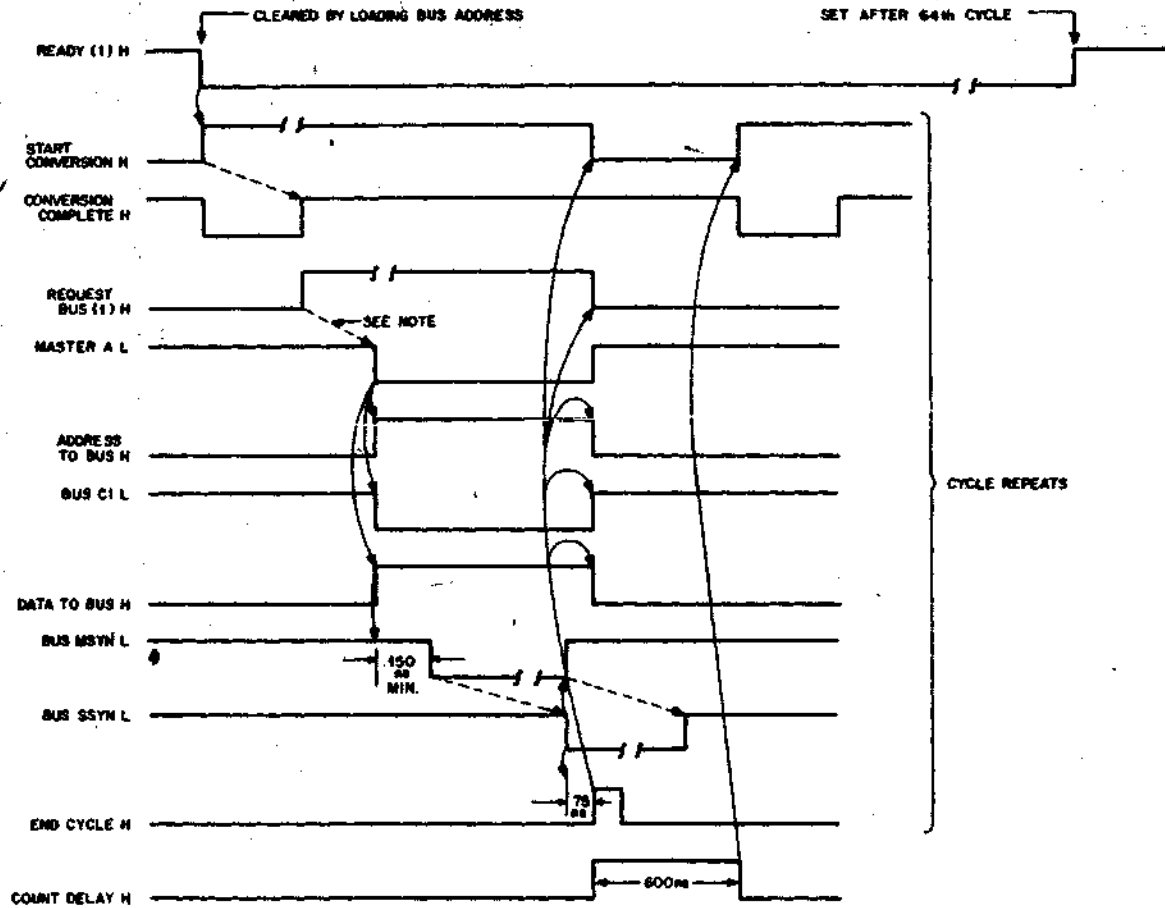


Figure 7-8 DMA Interface (timing diagram)

During normal operation, data is loaded into the buffer register and transferred to the peripheral device. When an UPDATE REQUEST from the DAC starts an interface cycle, the interrupt vector is transferred to the processor. The processor again initiates the data flow by transferring a new word of data into DADBR.

7.5.4 Interface Programming

The programs described in this paragraph cause the DAC to output a time-varying signal by loading the DADBR with an initial value and then changing that value by small increments until it reaches a final value determined by the program. The analog output is 100 cycles of a triangular waveform (actually, a stepped triangular waveform) with the slope of the ascending portion equal to half the slope of the descending portion. The period of the waveform is 150 times the period between update request pulses.

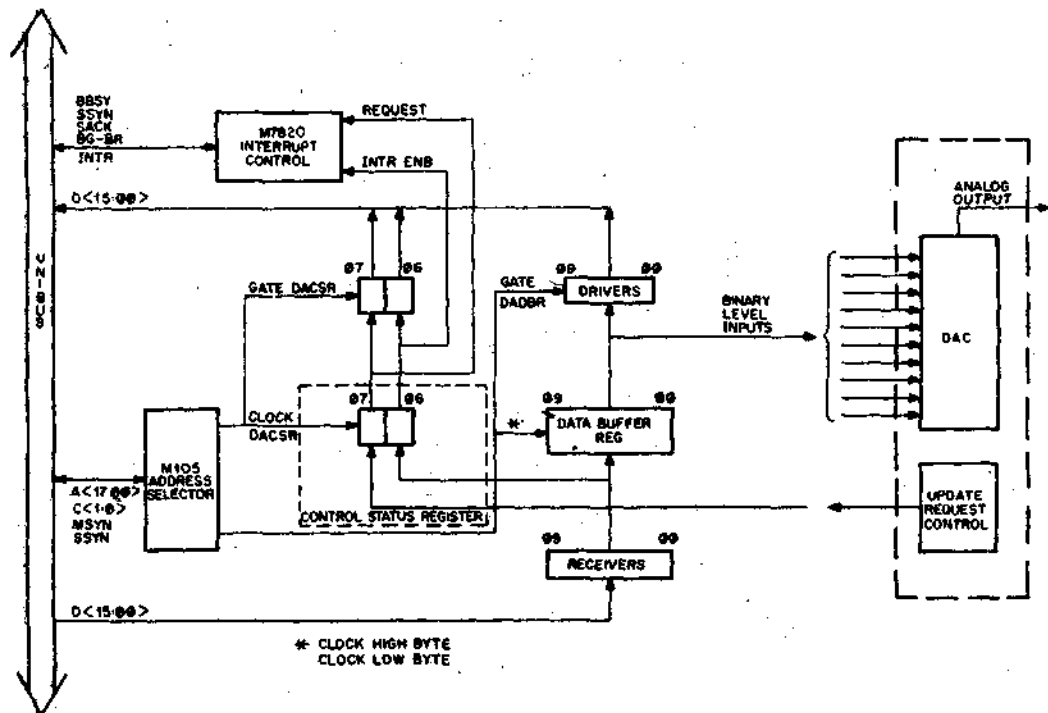


Figure 7-9 Output Interface with Interrupt Control (block diagram)

In the interface program, the DAC output is reset to a higher value by the ADD #10, DADBR instruction or reset to a lower value by the SUB #20, DADBR instruction. In either case, the value in the DADBR is read, modified by an arithmetic operation, and the new value is stored in the DADBR. All these operations are under processor control.

The ability of the UNIBUS to access device registers as though they were memory locations allows the processor to directly perform tests and modifications on the device register. This program compares the value in the DADBR with the test values. The program uses a minimum of stored data because it is not necessary to use memory locations for counters or storage of temporary values.

The processor initializes operation by executing the following sequence of instructions:

```

CLR    DADBR           ;CLEAR DATA BUFFER REGISTER
CLR    DASW            ;RESET UP/DOWN SWITCH
MOV    #144, DACNT     ;INITIALIZE CYCLE COUNTER
MOV    #100, DACSR     ;SET INTERRUPT ENABLE

```

The interrupt service routine includes the following instructions:

```

DAVEC:  DASERV          ;POINTER TO SERVICE ROUTINE
        240             ;PROCESSOR PRIORITY = 5

DASERV: TST    DASW      ;SWITCH SET?
        BPL    UP        ;NO, GO UP
        SUB    #20, DADBR ;YES GO DOWN
        BNE    CONT      ;OUTPUT VALUE EQUALS 0?
        CLR    DASW      ;YES, RESET SWITCH
        DEC    DACNT     ;REDUCE COUNT BY ONE
        BNE    CONT      ;COUNT EQUALS 0?
        CLR    DACSR     ;YES, DISABLE INTERRUPT
                          AND EXIT
        RTI

UP:     ADD    #10, DADBR ;OUTPUT VALUE GOES UP
        CMP    DADBR, #1000 ;1000 IS TOP LIMIT ON VALUE
        BNE    CONT      ;DOES VALUE EQUAL TOP LIMIT
        COM    DASW      ;YES, SET SWITCH

CONT:   RTI             ;EXIT FOR INTERMEDIATE
                          VALUES

```

7.6 DAC-DMA INTERFACE

A direct memory access (DMA) interface designed for a digital-to-analog converter (DAC) allows a specified number of words from memory to be transferred directly to the interface without processor intervention.

The previous interface example (paragraph 7.5) described a digital-to-analog converter interface that was serviced (controlled) by the vectored interrupt structure. In a real-time system where the time to service repetitive interrupts demands too much processor time, it may become necessary to expand the control section of the interface, so that the interface is less dependent on processor control, thereby reducing processor overhead.

This interface example uses the same DAC as the one discussed in the previous example. However, the interface to the UNIBUS differs. Added to the interface control section are direct bus access logic circuits, a word count register, and a bus address register. These additions allow a specified number of words from a particular group of memory addresses to be transferred directly to the interface, independent of processor control. This interface may be used, for example, to drive the X-Y deflection circuits of a CRT display scope in a refresh direct from memory mode.

7.6.1 Interface Description

A block diagram of the DAC-DMA interface is shown in Figure 7-10. The

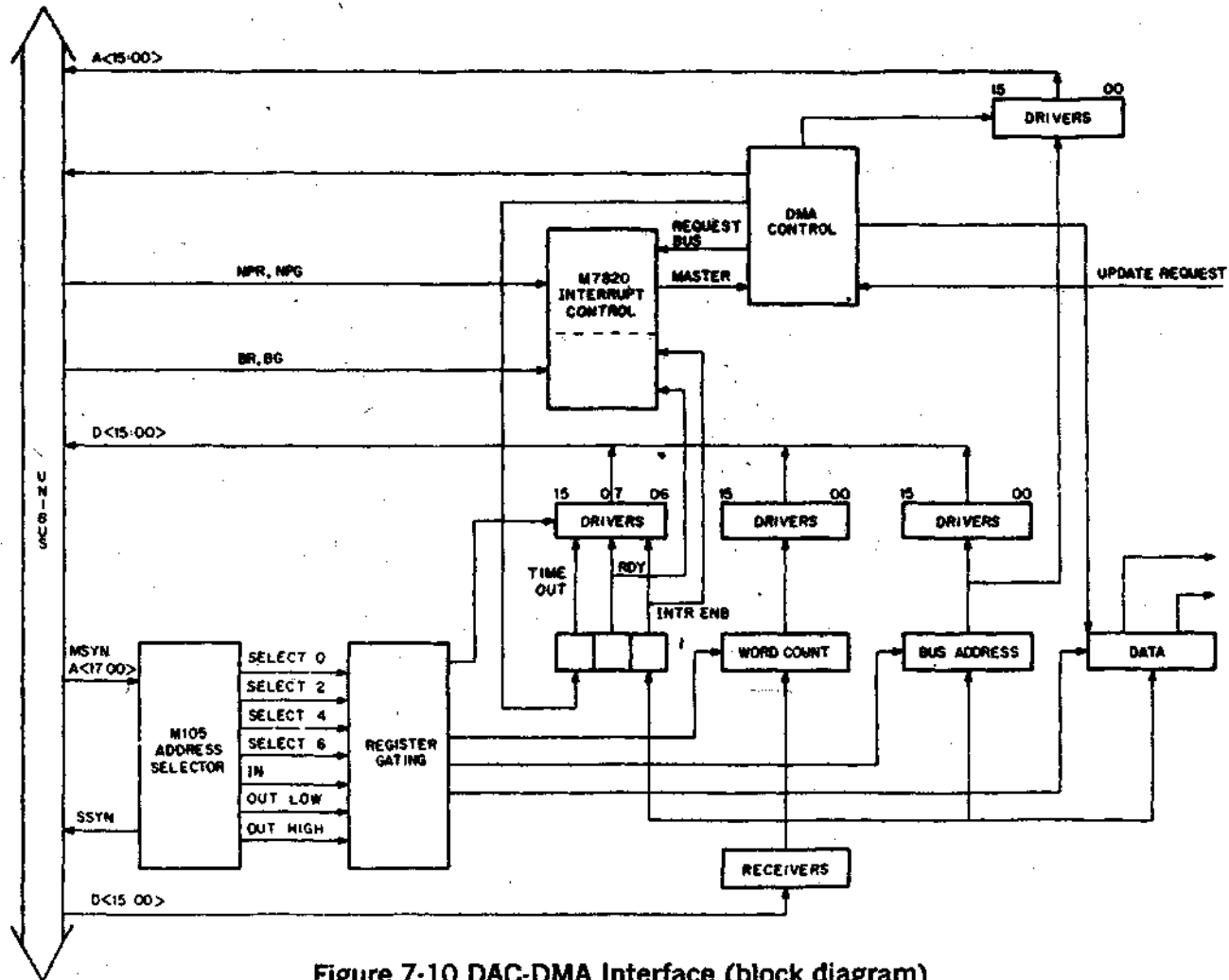


Figure 7-10 DAC-DMA Interface (block diagram)

interface contains four registers: a DAC control and status register (DACSR) which contains control and status information; a DAC word count register (DAWC) which holds the 2's complement of the number of words to be transferred; a DAC bus address register (DABA) which indicates where the block of information is held in memory; and a DAC data buffer register (DADB) which buffers information during bus cycles and which can also be loaded under program control.

A typical method of programming this interface is to first initialize the control by loading the DAWC and DABA registers. The next step is to set the GO bit in the DACSR. Words of data are then sequentially taken from memory and loaded into the DADB register at a rate set by the DAC or by an external clock. After each transfer (which is under the control of the interface rather than the processor), the DAWC and DABA registers are incremented. Data transfers continue until the DAWC register overflows (goes to all 0s). At this point, a READY bit in the DACSR is set. The READY bit can cause an interrupt to occur (provided INTR ENB is set), thereby notifying the processor that the block transfer is now complete, and another block transfer can be started.

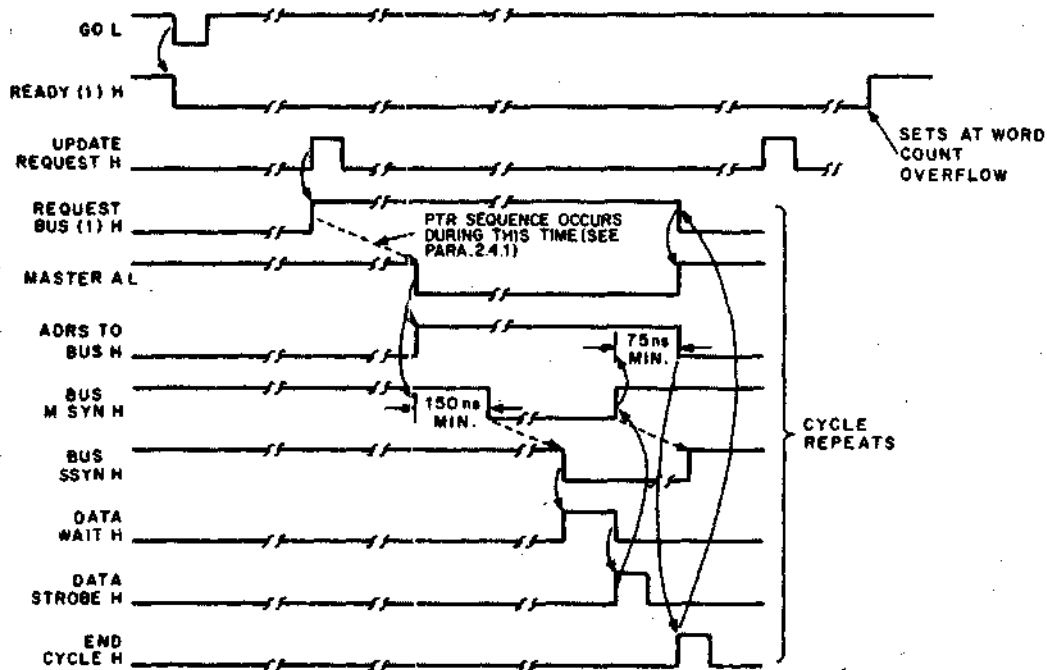


Figure 7-11 DAC-DMA Interface (timing diagram)

APPENDIX A

UNIBUS ADDRESSES

A.1 INTERRUPT & TRAP VECTORS

000	(reserved)
004	CPU errors
010	Illegal & reserved instructions
014	BPT, breakpoint trap
020	IOT, input/output trap
024	Power Fail
030	EMT, emulator trap
034	TRAP instruction
040	System software
044	System software
050	System software
054	System software
060	Console Terminal, keyboard/reader
064	Console Terminal, printer/punch
070	PC11, paper tape reader
074	PC11, paper tape punch
100	KW11-L, line clock
104	KW11-P, programmable clock
110	
114	Memory system errors
120	XY Plotter
124	DR11-B DMA interface; (DA11-B)
130	ADO1, A/D subsystem
134	AFC11, analog subsystem
140	AA11, display
144	AA11, light pen
150	
154	
160	
164	
170	User reserved
174	User reserved
200	LP11/LS11, line printer; LA180
204	RS04/RF11, fixed head disk
210	RC11, disk
214	TC11, DECTape
220	RK11, disk
224	TU16/TM11/TS03, magnetic tape
230	CD11/CM11/CR11, card reader
234	UDC11, digital control subsystem
240	PIRQ, Program Interrupt Request (11/45)

244	Floating Point Error
250	Memory Management
254	RP04/RP11 disk pack
260	TA11, cassette
264	RX11, floppy disk
270	User reserved
274	User reserved
300	(start of floating vectors)

A.2 FLOATING VECTORS

There is a floating vector convention used for communications (and other) devices that interface with the PDP-11. These vector addresses are assigned in order starting at 300 and proceeding upwards to 777. The following Table shows the assigned sequence. It can be seen that the first vector address, 300, is assigned to the first DC11 in the system. If another DC11 is used, it would then be assigned vector address 310, etc. When the vector addresses have been assigned for all the DC11's (up to a maximum of 32), addresses are then assigned consecutively to each unit of the next highest-ranked device (KL11 or DP11 or DM11, etc.), then to the other devices in accordance with the priority ranking.

Priority Ranking for Floating Vectors

(starting at 300 and proceeding upwards)

Rank	Device	Vector Size (in octal)	Max No.
1	DC11	(10) ₈	32
2	KL11, DL11-A, DL11-B	10	16
3	DP11	10	32
4	DM11-A	10	16
5	DN11	4	16
6	DM11-BB	4	16
7	DR11-A	10*	32
8	DR11-C	10*	32
9	PA611 Reader	4*	16
10	PA611 Punch	4*	16
11	DT11	10*	8
12	DX11	10*	4
13	DL11-C, DL11-D, DL11-E	10	31
14	DJ11	10	16
15	DH11	10	16
16	GT40	10	1
17	LPS11	30*	1
18	DQ11	10	16
19	KW11-W	10	1
20	DU11	10	16

*—The first vector for the first device of this type must always be on a (10)₈ boundary.

A.3 FLOATING ADDRESSES

There is a floating address convention used for communications (and other) devices interfacing with the PDP-11. These addresses are assigned in order starting at 760 010 and proceeding upwards to 763 776.

Floating addresses are assigned in the following sequence:

Rank	Device	First Address (if only floating address device in the system)
1	DJ11	760 010
2	DH11	760 020
3	DQ11	760 030
4	DU11	760 040

A.4 DEVICE ADDRESSES

777 776	Processor Status word (PS)	
777 774	Stack Limit	
777 772	Program Interrupt Request (PIRQ)	
777 716	} CPU registers	
777 710		
777 707		R7 (PC)
777 706		R6 (SP)
777 705		R5
777 704	General registers,	R4
777 703		R3
777 702		R2
777 701		R1
777 700		R0
777 676	} Memory Management	
777 600		
777 576		(SR2)
777 574	Memory Mgt status regs,	(SR1)
777 572		(SR0)
777 570	Console Switch & Display Register	
777 566		printer/punch data
777 564	Console Terminal,	printer/punch status
777 562		keyboard/reader data
777 560		keyboard/reader status
777 556		punch data (PPB)
777 554	PC11/PR11, punch status (PPS)	
777 552	reader data (PRB)	
777 550	reader status (PRS)	

777 546	KW11-L, clock status (LKS)
777 516	LA180 printer data
777 514	LP11/LS11/LV11, printer status
777 512	
777 510	
777 506	
777 504	
777 502	TA11, cassette data (TADB)
777 500	cassette status (TACS)
777 476	look ahead (ADS)
777 474	maintenance (MA)
777 472	disk data (DBR)
777 470	RF11, adrs ext error (DAE)
777 466	disk address (DAR)
777 464	current mem adrs (CMA)
777 462	word count (WC)
777 460	disk status (DCS)
777 456	disk data (RCDB)
777 454	maintenance (RCMN)
777 452	current address (RCCA)
777 450	RC11, word count (RCWC)
777 446	disk status (RCCS)
777 444	error status (RCER)
777 442	disk address (RCDA)
777 440	look ahead (RCLA)
777 436	#8
777 434	#7
777 432	#6
777 430	DT11, bus switch #5
777 426	#4
777 424	#3
777 422	#2
777 420	#1
777 416	disk data (RKDB)
777 414	maintenance
777 412	disk address (RKDA)
777 410	RK11, bus address (RKBA)
777 406	word count (RKWC)
777 404	disk status (RKCS)
777 402	error (RKER)
777 400	drive status (RKCS)
777 356	
777 354	
777 352	
777 350	TC11, DECTape data (TCDT)
777 346	bus address (TCBA)
777 344	word count (TCWC)
777 342	command (TCCM)
777 340	DECTape status (TCST)

777 336	}	KE11-A, EAE #2		
777 320				
777 316			arithmetic shift	
777 314			logical shift	
777 312			normalize	
777 310	}	KE11-A, EAE #1,	step count/status register	
777 306			multiply	
777 304			multiplier quotient	
777 302			accumulator	
777 300			divide	
777 172	}	RX11,	data buffer	
777 170			command status	
777 166			data (CDDB)	
777 164	}	CR11/	data (CRB2) comp	
777 162			CM11,	data (CRB1)
777 160			status (CRS)	CD11,
			col count (CDCC)	
			status (CDST)	
776 776				
776 774				
776 772	}	AD01,	A/D data (ADDB)	
776 770			A/D status (ADCS)	
776 766			register 4 (DAC4)	
776 764			register 3 (DAC3)	
776 762			register 2 (DAC2)	
776 760	}	AA11 #1,	register 1 (DAC1)	
776 756			D/A status (CSR)	
776 754				
776 752				
776 750				
776 736			silo memory (SILO)	
776 734			sel unit cyl adrs (SUCA)	
776 732			maintenance 3 (RPM3)	
776 730			maintenance 2 (RPM2)	
776 726			maintenance 1 (RPM1)	
776 724	}	RP11,	disk address (RPDA)	
776 722			cylinder address (RPCA)	
776 720			bus address (RPBA)	
776 716			word count (RPWC)	
776 714			disk status (RPCS)	
776 712			error (RPER)	
776 710			disk status (RPDS)	
776 676	}	DL11-A, -B,	#16	
776 500			#1	
776 476	}	AA11,	#5	
776 400			#2	

776 376	}	DX11	
776 200			
776 176	}	DL11-C, -D, -E,	#31
775 610			#1
775 576	}	DS11,	#4
775 400			#1
775 376	}	DN11,	#16
775 200			#1
775 176	}	DM11,	#16
775 000			#1
774 776	}	DP11,	#1
774 400			#32
774 376	}	DC11,	#32
774 000			#1

773 776	}	Maintenance Loader	
773 700			
773 676			

773 400	}	BM792-YH cassette	
773 376			
773 300			

773 276	}	BM792-YC card	
773 200			
773 176	}	BM792-YB disk/DEctape	MR11-DB
773 100			

773 076	}	BM792-YA paper tape	
773 000			

M792 diode ROM

772 776	}	PA611 typeset punch
772 700		
772 676	}	PA611 typeset reader
772 600		
772 576		maintenance (AFMR)
772 574		AFC11, MX channel/gain (AFCG)
772 572		flying cap data (AFBR)
772 570		flying cap status (AFCS)
772 556	}	XY11 plotter
772 550		
772 546		
772 544		counter
772 542	KW11-P,	count set
772 540		clock status
772 536		
772 534		
772 532		read lines (MTRD)
772 530		tape data (MTD)
772 526	TM11,	memory address (MTCMA)
772 524		byte record counter (MTBRC)
772 522		command (MTC)
772 520		tape status (MTS)
772 516		Memory Mgt status reg (SR3)
772 436	}	DR11-B #2
772 430		

772 416 data (DRDB)
 772 414 DR11-B #1, status (DRST)
 772 412 bus address (DRBA)
 772 410 word count (DRWC)

772 376 }
 772 200 } Memory Management

772 136 }
 772 110 } Memory Parity

771 776 status (UDCS)
 771 774 UDC11, scan (UDSR)
 771 772
 771 770

771 776 }
 771 000 } UDC functional I/O modules

770 776 } #8
 KG11,
 770 700 } #1

770 676 } #16
 DM11-BB,
 770 500 } #1

767 776
 767 774
 767 772 DR11-C #1, input buffer
 767 770 status output buffer
 status

767 766 }
 767 760 } DR11-C #2

767 756 }
 767 750 } DR11-C #3

764 000 (start here and assign upwards to 767 776)

763 776 (top of floating addresses)

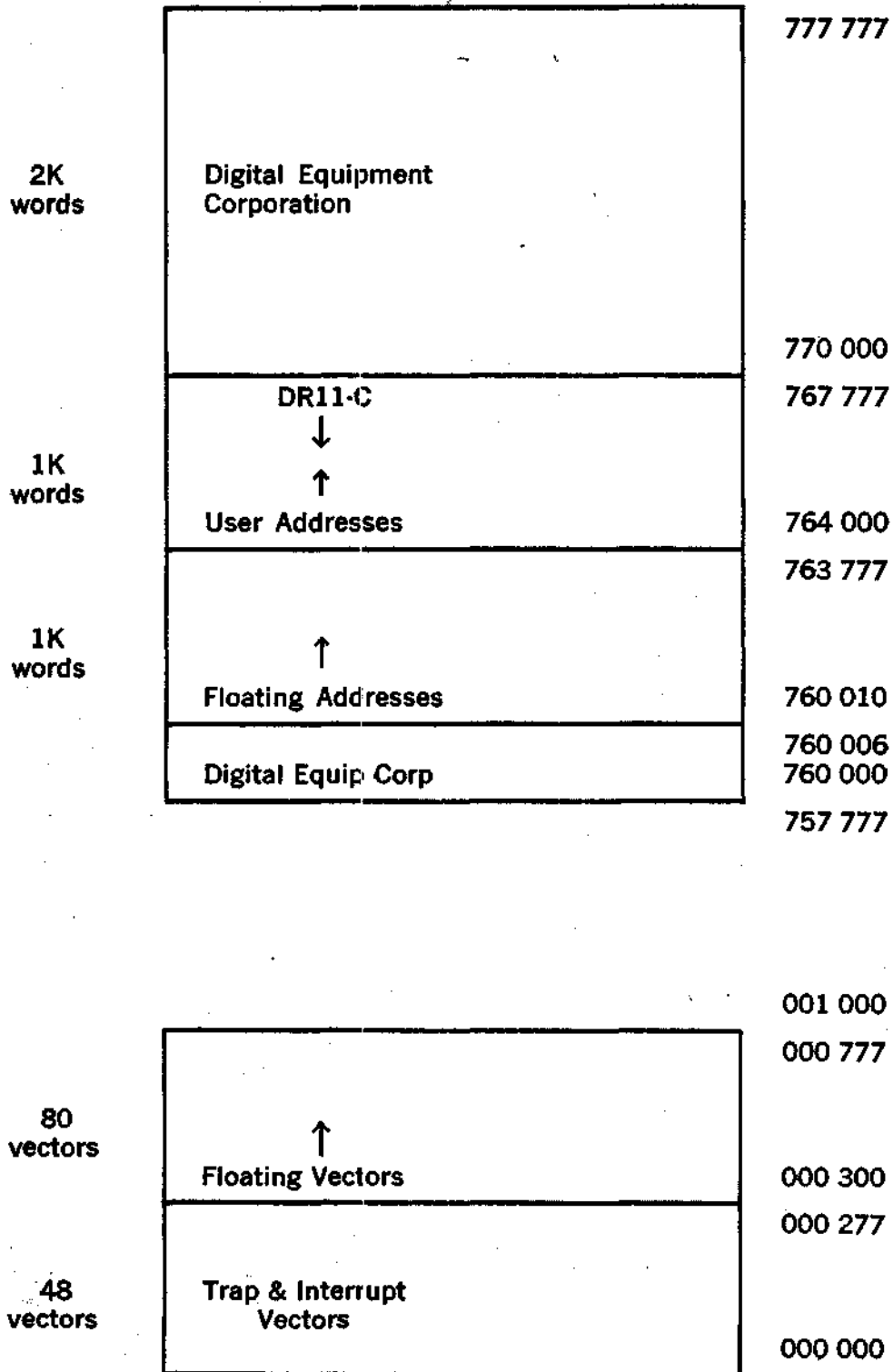
760 010 (start here and assign upwards to 763 776)

User Addresses

Floating Addresses

760 006 }
 760 000 } (diagnostics)

A.5 ADDRESS MAP



APPENDIX B

MISCELLANEOUS TABLES AND DATA

SLOTS A1 AND B1 (A4 AND B4) ARE WIRED AS SHOWN IN TABLES B-1 AND B-2.

TABLE B-1 UNIBUS PIN ASSIGNMENTS (BY PIN NUMBERS)

PIN	SIGNAL	PIN	SIGNAL
AA1	INIT L	BA1	BG 6 H
AA2	POWER(+ 5V)	BA2	POWER(+ 5V)
AB1	INTR L	BB1	BG 5 H
AB2	GROUND	BB2	GROUND
AC1	DOO L	BC1	BR 5 L
AC2	GROUND	BC2	GROUND
AD1	DO2 L	BD1	GROUND
AD2	DO1 L	BD2	BR 4 L
AE1	DO4 L	BE1	GROUND
AE2	DO3 L	BE2	BG 4 H
AF1	DO6 L	BF1	ACLO L
AF2	DO5 L	BF2	DCLO L
AH1	DO8 L	BH1	A01 L
AH2	DO7 L	BH2	A00 L
AJ1	D10 L	BJ1	A03 L
AJ2	DO9 L	BJ2	A02 L
AK1	D12 L	BK1	A05 L
AK2	D11 L	BK2	A04 L
AL1	D14 L	BL1	A07 L
AL2	D13 L	BL2	A06 L
AM1	PA L	BM1	A09 L
AM2	D15 L	BM2	A08 L
AN1	GROUND	BN1	A11 L
AN2	PB L	BN2	A10 L
AP1	GROUND	BP1	A13 L
AP2	BBSY L	BP2	A12 L
AR1	GROUND	BR1	A15 L
AR2	SACK L	BR2	A14 L
AS1	GROUND	BS1	A17 L
AS2	NPR L	BS2	A16 L
AT1	GROUND	BT1	GROUND
AT2	BR 7 L	BT2	C1 L
AU1	NPG H	BU1	SSYN L
AU2	BR 6 L	BU2	CO L
AV1	BG 7 H	BV1	MSYN L
AV2	GROUND	BV2	GROUND

TABLE B-2 UNIBUS PIN ASSIGNMENTS (BY SIGNAL NAME)

SIGNAL	PIN	SIGNAL	PIN
A00 L	BH2	D06 L	AF1
A01 L	BH1	D07 L	AH2
A02 L	BJ2	D08 L	AH1
A03 L	BJ1	D09 L	AJ2
A04 L	BK2	D10 L	AJ1
A05 L	BK1	D11 L	AK2
A06 L	BL2	D12 L	AK1
A07 L	BL1	D13 L	AL2
A08 L	BM2	D14 L	AL1
A09 L	BM1	D15 L	AM2
A10 L	BN2	GROUND	AB2
A11 L	BN1	GROUND	AC2
A12 L	BP2	GROUND	AN1
A13 L	BP1	GROUND	AP1
A14 L	BR2	GROUND	AR1
A15 L	BR1	GROUND	AS1
A16 L	BS2	GROUND	AT1
A17 L	BS1	GROUND	AV2
ACLO L	BF1	GROUND	BB2
BBSY L	AP2	GROUND	BC2
BG4 H	BE2	GROUND	BD1
BG5 H	BB1	GROUND	BE1
BG6 H	BA1	GROUND	BT1
BG7 H	AV1	GROUND	BV2
BR4 L	BD2	INIT L	AA1
BR5 L	BC1	INTR L	AB1
BR6 L	AU2	MSYN L	BV1
BR7 L	AT2	NPG H	AU1
CO L	BU2	NPR L	AS2
C1 L	BT2	PA L	AM1
D00 L	AC1	PB L	AN2
D01 L	AD2	+5V*	AA2
D02 L	AD1	+5V*	BA2
D03 L	AE2	SACK L	AR2
D04 L	AE1	DCLO L	BF2
D05 L	AF2	SSYN L	BU1

* +5V IS WIRED TO THESE PINS TO SUPPLY POWER TO THE BUS TERMINATOR ONLY.

+5V SHOULD NEVER BE CONNECTED VIA THE UNIBUS BETWEEN SYSTEM UNITS.

TABLE B-3 BB11 POWER PIN ASSIGNMENTS

PIN	POWER
A1	-15V
A2	+5V
B1	-15V
B2	-15V
C1	-15V
C2	GND
D1	-15V
D2	GND
E1	-15V
E2	GND
F1	-15V
F2	GND
H1	-15V
H2	+5V
J1	-15V
J2	+5V
K1	-15V
K2	+5V
L1	-15V
L2	+5V
M1	-15V
M2	+5V
N1	GND
N2	-25V
P1	GND
P2	LTC L
R1	GND
R2	ACLO L
S1	GND
S2	DCLO L
T1	GND
T2	+8V
U1	GND
U2	+8V
V1	GND
V2	+8V

NOTE

POWER IS IN MODULE SLOT A3 OF ALL SYSTEM UNITS MOUNTED IN BA11 MOUNTING BOXES EQUIPPED WITH H720 POWER SUPPLIES.

B.4 ASCII CODE

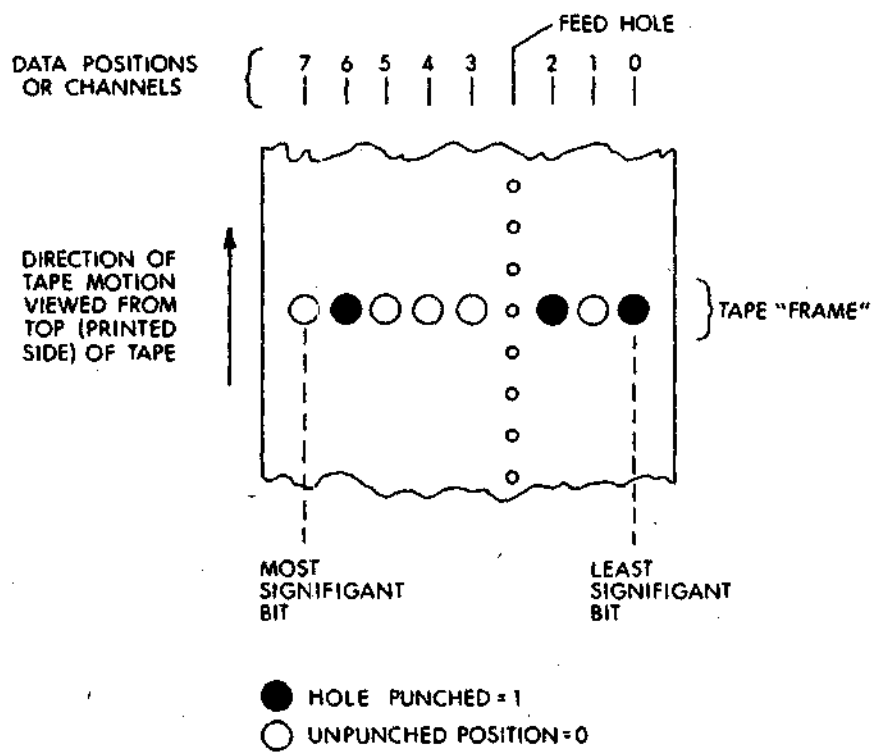
7-BIT ASCII CODE

Octal Code	Char	Octal Code	Char	Octal Code	Char	Octal Code	Char
000	NUL	040	SP	100	@	140	\
001	SOH	041	!	101	A	141	a
002	STX	042	"	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	\$	104	D	144	d
005	ENQ	045	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	'	107	G	147	g
010	BS	050	(110	H	150	h
011	HT	051)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	-	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	064	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[173	{
034	FS	074	<	134	\	174	
035	GS	075	=	135]	175	}
036	RS	076	>	136	^	176	~
037	US	077	?	137	_	177	DEL

To convert to the modified ASCII code used by the LT33:

8-Bit Teletype Code = (7-Bit ASCII Code) + (200)

B.5 PAPER TAPE FORMAT



NOTE:
FRAME SHOWN IS PUNCHED WITH OCTAL CODE 105

Paper-Tape Format

