# ** ST/S Users Manual **

X C O M P  I N C O R P O R A T E D

7566 Trade Street
San Diego, Cal. 92121
Phone: (714) 271-8730
619
TELEX: 182786 (XCOMP INC SDG)

Rev. A1

## 1.0 INTRODUCTION

The XCOMP ST/S hard disk controller is a custom designed microprogrammable controller which consists of two S-100 bus printed circuit boards. The controller employs writable control store which gives the user the ability to load and run fault isolation microcode from the host computer.

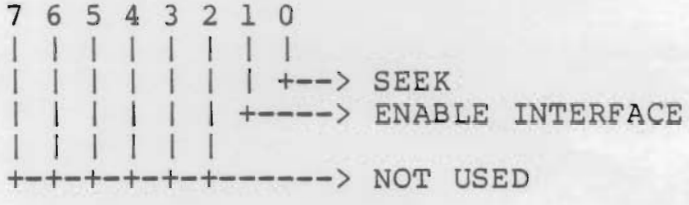
The ST/S controller is compatible with the Shugart Technology ST-506 disk drive. The ST-506 is formatted with 32 256-byte sectors per track. The drive has four heads and 153 cylinders which provides a formatted capacity of 5.0 megabytes.

## 2.0 DRIVE INTERFACE

The first four I/O addresses, as defined in Figure 1, are devoted to the disk drive interface.

### 2.1 DISK COMMANDS (BASE+0)

This I/O port is used to command the ST-506 to seek.




#### 2.1.1 SEEK (Bit 0)

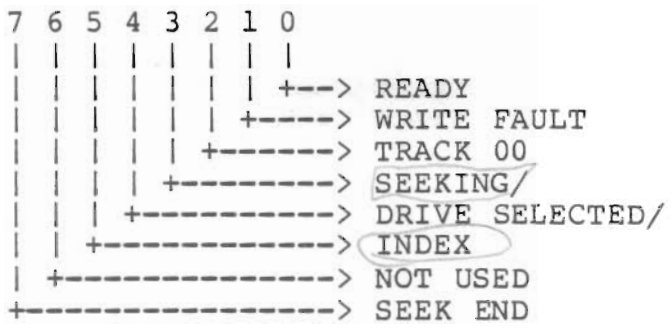
Causes the ST-506 to seek. The number of cylinders to move the heads is specified by I/O ports BASE+2 & BASE+3 (See Section 2.5). The direction the heads will move is specified by Bit 1 of I/O port BASE+1 (See Section 2.3.2)

#### 2.1.2 ENABLE INTERFACE (Bit 1)

Enables interface signals to be passed from the Interface Board to the Data Board. This bit must be maintain true (1) as long as it is required to attach the Interface Board to the Data Board. In a single drive/single interface system this bit would be set true at all times.

## 2.2 DRIVE STATUS (BASE+0)

This I/O port is used to read drive status.




### 2.2.1 READY (Bit 0)

This bit indicates that the drive has been selected and is ready to read, write, or seek.

### 2.2.2 WRITE FAULT (Bit 1)

This bit indicates that the drive has detected a write fault. Write fault is cleared by deselecting and reselecting the drive (See Section 2.3.1).

### 2.2.3 TRACK 00 (Bit 2)

This bit indicates that the heads are currently positioned at Track 00. Note that the ST-506 automatically positions the heads to Track 00 when power is applied to the drive.

### 2.2.4 SEEKING/ (Bit 3)

A low-true signal that indicates that the drive is seeking. Reading or writing should not be attempted if SEEKING/ is true (0).

### 2.2.5 DRIVE SELECTED/ (Bit 4)

A low-true signal that indicates that the drive has been selected. It is possible to have DRIVE SELECTED/ true (0) and READY false (0) when power is first applied to the drive.

### 2.2.6 INDEX (Bit 5)

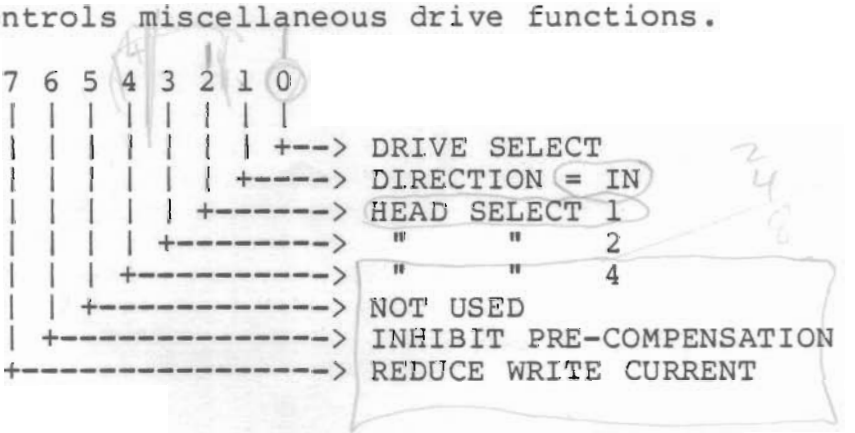
Indicates that the drive has detected the index marker. This bit is latched by the controller and it can be cleared by doing an input to I/O port BASE+1.

### 2.2.7 SEEK END (Bit 7)

Indicates the completion of a seek command.

## 2.3 EXTENDED DRIVE COMMANDS (BASE+1)

This I/O port controls miscellaneous drive functions.




### 2.3.1 DRIVE SELECT (Bit 0)

Used to select the drive. This bit must be maintained true as long as it is desired to select the drive.

### 2.3.2 DIRECTION = IN (Bit 1)

Used to set the direction of seeks. Set this bit true (1) if the desired direction of seeks is inward. Conversely, set this bit false (0) if the desired direction is outward.

### 2.3.3 HEAD SELECT (Bits 2 thru 4)

Used to select one of eight heads. Note that the ST-506 currently has four heads.

### 2.3.4 INHIBIT PRE-COMPENSATION (Bit 6)

This bit is used to inhibit write precompensation. This bit must be set false (0) at all times.

### 2.3.5 REDUCE WRITE CURRENT (Bit 7)

This bit is used to reduce write current. This bit must be set false (0) when writing on cylinders 0 thru 76 and it must be set true (1) when writing on cylinders 77 thru 152.

## 2.4 CLEAR INDEX (BASE+1)

Inputting from this I/O port clears the Index latch (See Section 2.2.6). It does not return any useful data.

## 2.5 SEEK COUNT (BASE+2 & BASE+3)

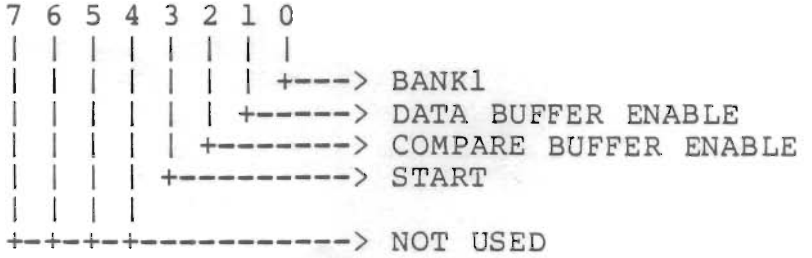
These I/O ports are used to set a 9-bit positive seek count. BASE+2 sets the least significant 8 bits of the seek count. Note that the ST-506 currently has 153 cylinders.

# 3.0 CONTROLLER I/O

The last four I/O addresses, as defined in Figure 1, are used for controller I/O.

## 3.1 CONTROLLER COMMANDS (BASE+4)

This I/O port is used to send commands to the controller.



### 3.1.1 BANK1 (Bit 0)

Selects either BANK0 OR BANK1. BANK0 typically contains read microcode, while BANK1 typically contains write microcode.

### 3.1.2 ENABLE DATA BUFFER (Bit 1)

Allows reading from, or writing to, the Data Buffer.

### 3.1.3 ENABLE COMPARE BUFFER (Bit 2)

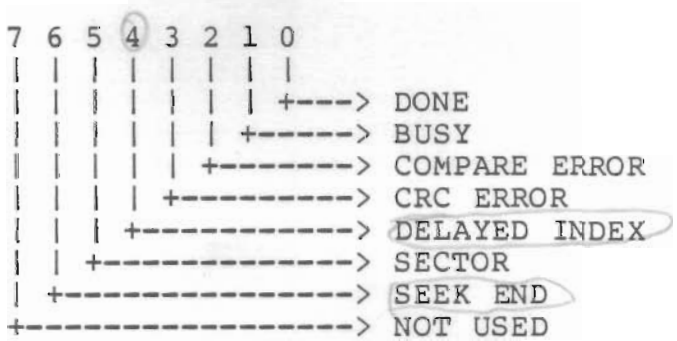
Allows writing into the Compare Buffer. The contents of the Compare Buffer are used, when reading or writing, to compare against the sector header for correct cylinder, head, and sector.

### 3.1.4 START (Bit 3)

Initiates microcode execution; i.e., starts a read or write operation.

## 3.2 CONTROLLER STATUS (BASE+4)

This I/O port is used to read controller status.




### 3.2.1 DONE (Bit 0)

Indicates the completion of a read or write operation. Can be used to interrupt the CPU.

### 3.2.2 BUSY (Bit 1)

Indicates that a read or write operation is in progress. If this signal is true (1) when DONE is true (1), the desired sector can not be found.

### 3.2.3 COMPARE ERROR (Bit 2)

Indicates that the header of the current sector does not match the information in the Compare Buffer.

### 3.2.4 CRC ERROR (Bit 3)

Indicates an error was detected in the data portion of the sector just read. Can, when a sector is not found, also indicate an error in one or more sector headers.

### 3.2.5 DELAYED INDEX (Bit 4)

Indicates detection of an index pulse. The raw index from the drive is delayed to coincide with the occurrence of the first sector pulse. Reset by any output to I/O port BASE+4.

### 3.2.6 SECTOR (Bit 5)

Indicates the detection of a sector pulse. Reset by any output to I/O port BASE+4.

### 3.2.7 SEEK END (Bit 6)

Indicates that one or more drives have finished a seek or a rezero operation. Can be used to interrupt the CPU.

## 3.3 CONTROLLER BUFFER ADDRESS (BASE+5)

Write only. Used to set a buffer address.

## 3.4 CONTROLLER DATA PORT (BASE+6)

Read and write. Used to move data into or out of BANK0, BANK1, or the Data Buffer. Used to write into the Compare Buffer.

## 4.0 I/O ADDRESSING

The ST/S controller requires a block of eight contigious I/O addresses. Address selection is accomplished via a DIP switch on the interface board at location G2; the interface board has three connectors along the top edge of the board. Setting a switch on (I) will compare for an I/O address bit as being true (1). Switch positions compare with address bits as follows:

```
SWITCH POSITION:  1 2 3 4 5 6 7
                  : : : : : : :
I/O ADDRESS BIT:  7 6 5 4 3 - -
                  |
                  |
                  +---->  (MSB)
```

As an example, to set the I/O address block to 70H thru 77H (XCOMP standard), set switches 1 & 5 OFF and switches 2 thru 4 ON. Switch 7 must be set ON. Switch 6 is not used.

## 5.0 DRIVE SPECIFICATIONS

```
      Formatted capacity = 5.0 megabytes
           Transfer rate = 5.0 megabits/second
Track-to-Track seek time = 18 milliseconds
       Maximun seek time = 500 milliseconds
        Rotational speed = 3600 RPM
       Recording density = 7690 BPI
```

## 6.0 POWER REQUIREMENTS

6.1 XS Data Board: +8v @ 700ma

6.2 STS Interface Board: +8V @ 500ma
-16v @ 35ma

| I/O ADDRESS | INPUT | OUTPUT |
|---|---|---|
| BASE+0 | DRIVE STATUS | DRIVE COMMANDS |
| BASE+1 | CLEAR INDEX LATCH | EXTENDED DRIVE COMMANDS |
| BASE+2 | ... | SEEK COUNT, LSB |
| BASE+3 | ... | " " , MSB |
| BASE+4 | CONTROLLER STATUS | CONTROLLER COMMANDS |
| BASE+5 | ... | BUFFER ADDRESS |
| BASE+6 | DATA IN | DATA OUT |
| BASE+7 | ... | ... |

FIGURE 1. I/O ADDRESSES