

## Soldering PC Boards

Two common causes of trouble with PC boards are bad solder joints or solder bridges. Usually, bad solder joints are caused by either a cold solder joint or contamination. A good solder joint is characterized by a bright shiny and smooth surface ( see figure 1).

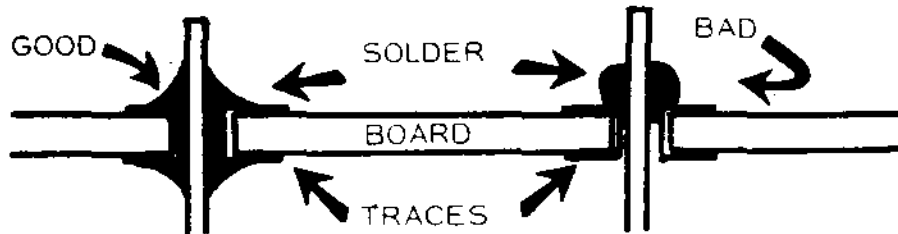


Figure 1. CROSS-SECTION OF A PC BOARD SHOWING GOOD AND BAD SOLDER CONNECTIONS

A cold solder joint is characterized by a dull surface and usually a lumpy or balled appearance. It takes practice and patience to obtain a good solder joint consistently. However, the first step is to apply flux to all connections before the solder. Second, heat the connection for a second or two with the soldering iron. Third, apply solder to the opposite side of the connection. Don't touch the solder to the iron. Flux has a "wetting" effect on solder which causes the solder to flow smoothly, completely filling the connection. If flux is not used or the metal around the connection is contaminated (dirty) it is almost impossible to have a good solder joint.

Solder bridges are usually caused by using a soldering iron tip that's too large, solder wire that's too large, or trying to rush the job. Use a small spade tip iron (see figure 2). Touch the connection with the flat side of the tip. After the flux bubbles, touch the solder to the opposite side of the connection. Again, don't touch the solder to the iron. The connection is hot enough to melt the solder causing it to flow around the connection. Do not use too much solder. Use a little and watch it flow. Solder is like spice for cooking, don't use too much.

Applying heat for extended periods will cause either or both of the following: the trace or pad will lift from the board or the board material will turn brown. Remove the iron before this happens. One hobbyist counts the bubbles that pop in the solder. He found seven to nine bubbles insured good solder flow without over heating.

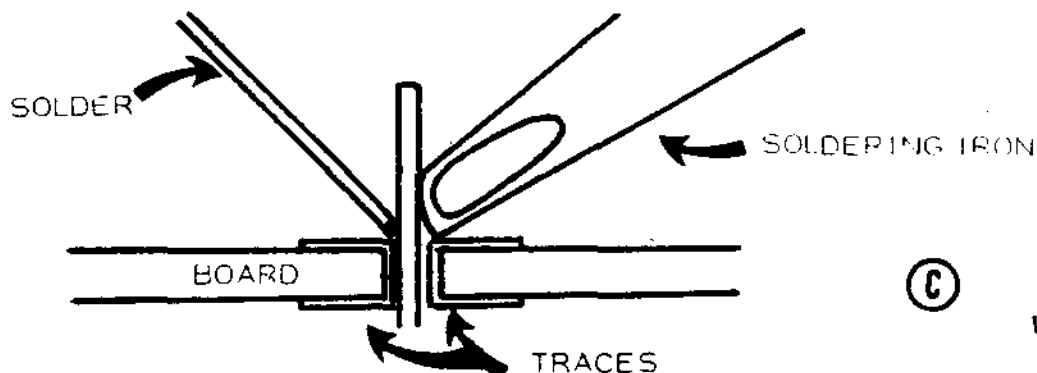


Figure 2.

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The MEM-1 is designed to operate with the S100(WAMECO)bus (see figure 3A,B). There are 19 pins not otherwise used in this bus. These pins are available for non-standard configurations. It is advisable to carefully consider any modification since this will limit board usage to a modified system.

### Parts List

C1	1	15 $\mu$ f tantalum electrolytic capacitor
C2-C6	5	.1 $\mu$ f disc ceramic capacitors
C7-C25	19	.01 $\mu$ f disc ceramic capacitors
R1-R7, R9, R10	9	2.7K $\Omega$ 1/4W carbon resistor
R8	1	1.0K $\Omega$ 1/4W carbon resistor
T1-T7	1	7 position dip switch
U1-U64	64	2102AL4 500ns 1024 x 1 static ram memory
U65	1	7400 quadruple 2-input positive-NAND gates
U66, U67	2	74LS74 dual d-type positive-edge-triggered flip-flops with preset and clear
U68	1	8131 six-bit unified bus comparators
U69, U70, U72	3	7404 hex inverters
U71, U73	2	8098 tri-state inverting hex buffers
U74	1	74LS02 quadruple 2-input positive-NOR gates
U75	1	7442 four-line-to-ten-line decoders (1-of-10)
U76-U79	4	7805 positive five volt regulators
	4	TO220 heatsinks
	68	16 pin sockets
	7	14 pin sockets
	4	6-32 x 3/4" screws and nuts

### Tools and Supplies Needed to Assemble and Test MEM-1

1	Q Tip cotton swab
1	pair needle nosed pliers
1	pair diagonal cutting pliers
1	bottle rosin flux
1	tube silicone thermal heat grease
1	jar solder cleaner
1	roll solder wick
1	phillips screwdriver
1	small adjustable wrench or socket to fit regulator nuts
1	roll (.031" or .040") SN60/40 rosin core solder
1	25 to 40 Watt soldering iron with small spade tip
1	strong light
1	magnifying glass
1	Xacto knife
1	multimeter
1	variable 15V power supply

### I Assembly of MEM-1

I-1. Before placing any parts on the board, check the board for any hair-line shorts (slivers). All boards have been inspected at least three times before shipping. Still, a good hobbyist checks any board he buys.

S-100 (WAMECO) BUS DESCRIPTION

1	+5V	
2	+15V	
3	XRDY	X
4	VI0	X
5	VI1	X
6	VI2	X
7	VI3	X
8	VI4	X
9	VI5	X
10	VI6	X
11	VI7	X
12		
13		
14		
15		
16		
17		
18	STAT DISABLE	X
19	CIC DISABLE	X
20	UNPROTECT	X
21	SS	X
22	ADDR DSBL	X
23	DO DSBL	X
24	02	X
25	01	X
26	PHLDA	X
27	PWAIT	
28	PINTE	
29	A5	
30	A4	
31	A3	
32	A15	
33	A12	
34	A9	
35	DO1	X
36	DO0	X
37	A10	
38	DO4	X
39	DO5	X
40	DO6	X
41	DI2	X
42	DI3	X
43	DI7	X
44	SMI	
45	SOUT	
46	SINP	
47	SMEMR	
48	SHLTA	
49	CLOCK (2MHz)	
50	GND	

51	+5V	A	
52	-15V	B	
53	SSW DSB	C	
54	EXT CLR	D	X
55		E	
56		F	
57		H	
58		J	
59		K	
60		L	
61		M	
62		N	
63		P	
64		R	
65		S	
66		T	
67	PHANTOM	U	
68	MWRITE	V	X
69	PS	W	
70	PROTECT	X	X
71	RUN	Y	X
72	PRDY	Z	X
73	PINT	a	X
74	PHOLD	b	X
75	PRESET	c	X
76	PSYNC	d	X
77	PWR	e	X
78	PDBIN	f	X
79	A0	h	
80	A1	j	
81	A2	k	
82	A6	l	
83	A7	m	
84	A8	n	
85	A13	p	
86	A14	r	
87	A11	s	
88	DO2	t	X
89	DO3	u	X
90	DO7	v	X
91	DI4	w	X
92	DI5	x	X
93	DI6	y	X
94	DI1	z	X
95	DI0	AA	X
96	SINTA	AB	
97	SWO	AC	
98	SSTACK	AD	
99	POC	AE	
100	GND	AF	

PIN MNEMONIC TERM.

PIN MNEMONIC ALTER. PIN DESIG. TERM.

Figure 3A

### S-100 (WAMECO) BUS DESCRIPTION

Pin #	Mnemonic	Enabled State	Description
1	+8 Volts	NA	Unregulated +8 Volts DC. This voltage should not be less than +8 or greater than +11 volts.
2	+16 Volts	NA	Unregulated +16 Volts DC. This voltage should not be less than +16 or greater than +20 Volts.
3	XRDY	Low	Causes CPU to enter WAIT state when enabled.
4	<u>VI0</u>	Low	Vectored Interrupt priority 0
5	<u>VI1</u>	Low	Vectored Interrupt priority 1
6	<u>VI2</u>	Low	Vectored Interrupt priority 2
7	<u>VI3</u>	Low	Vectored Interrupt priority 3
8	<u>VI4</u>	Low	Vectored Interrupt priority 4
9	<u>VI5</u>	Low	Vectored Interrupt priority 5
10	<u>VI6</u>	Low	Vectored Interrupt priority 6
11	<u>VI7</u>	Low	Vectored Interrupt priority 7
12	---	NA	Not used
13	---	NA	Not used
14	---	NA	Not used
15	---	NA	Not used
16	---	NA	Not used
17	---	NA	Not used
18	STAT DISABLE	Low	The eight status line buffers on the CPU board enter the high impedance state when enabled.
19	C/C DISABLE	Low	The six command/control line buffers on the CPU board enter the high impedance state when enabled.
20	UNPROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be cleared.
21	SS	High	Indicates the CPU is single stepping.
22	<u>ADDR DSBL</u>	Low	The 16 address line buffers on the CPU board enter the high impedance state when enabled.
23	<u>DO DSBL</u>	Low	The eight data-out lines on the CPU board enter the high impedance state when enabled.
24	Ø 2	High	Buffered TTL CPU phase 2 clock.
25	Ø 1	High	Buffered TTL CPU phase 1 clock.
26	PHLDA	High	CPU board "Hold Acknowledge" to HOLD-H input.
27	PWAIT	High	CPU output showing a WAIT state is occurring.

Figure 3B.

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
28	PINTE	High	CPU output showing that Interrupts are enabled.
29	A5	High	Address Bit 5
30	A4	High	Address Bit 4
31	A3	High	Address Bit 3
32	A15	High	Address Bit 15
33	A12	High	Address Bit 12
34	A9	High	Address Bit 9
35	DO1	High	CPU Data Out Bit 1
36	DO0	High	CPU Data Out Bit 0
37	A10	High	Address Bit 10
38	DO4	High	CPU Data Out Bit 4
39	DO5	High	CPU Data Out Bit 5
40	DO6	High	CPU Data Out Bit 6
41	D12	High	Data In Bit 2 to CPU
42	D13	High	Data In Bit 3 to CPU
43	D17	High	Data In Bit 7 to CPU
44	SM1	High	CPU output indicating it is performing Fetch Instruction.
45	SOUT	High	CPU output showing it is in an output cycle.
46	SINP	High	CPU output showing it is in an input cycle.
47	SMEMR	High	CPU status signal indicating the current cycle is a Memory Read cycle.
48	SHLTA	High	CPU status signal indicating the CPU is halted.
49	CLOCK(2MHz)	Low	A buffered 2 MHz clock for general use.
50	GND	NA	Ground (common)
51	+8 Volts	NA	(Same as pin 1)
52	-16 Volts	NA	Unregulated -16 Volts DC. This voltage should not be greater than -16 or less than -20 Volts.
53	<del>SSW DSB</del>	Low	Sense Switch Disable disables CPU board data input buffers so that CPU can read sense switches.
54	<del>EXT CLR</del>	Low	Front panel generated I/O clear signal.
55	---	NA	Not used
56	---	NA	Not used
57	---	NA	Not used
58	---	NA	Not used
59	---	NA	Not used
60	---	NA	Not used
61	---	NA	Not used
62	---	NA	Not used
63	---	NA	Not used
64	---	NA	Not used
65	---	NA	Not used
66	---	NA	Not used
67	PHANTOM	NA	Used for Memory Bank Selection (or for SOL. © Systems)

Figure 3B (continued)

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
68	MWRITE	High	CPU output showing Data Out Bus data is to be written into the memory selected by the address lines.
69	$\overline{PS}$	Low	Shows Protect Status of selected memory.
70	PROTECT	High	Combined with address in an AND gate on a memory board which causes the PROTECT flip-flop to be set.
71	RUN	High	Front panel indication that CPU run instruction has been input.
72	PRDY	Low	Causes the CPU to enter the WAIT state when enabled.
73	$\overline{PINT}$	Low	If interrupts have been enabled causes the CPU to enter the Interrupt Acknowledge condition at the conclusion of the current instruction.
74	$\overline{PHOLD}$	Low	CPU input which causes a HOLD status to occur. DMA transfer request signal is $\overline{PHOLD}$ .
75	$\overline{PRESET}$	Low	CPU board system reset signal.
76	PSYNC	High	CPU output showing the start of a new machine cycle. This signal is used on the CPU board to enable the loading of the System Status Latch.
77	$\overline{PWR}$	Low	Indication that data on the Data Out Bus is to be written either to a memory or an I/O device.
78	PDBIN	Low	Indication to the selected memory or I/O device that the CPU expects data on the Data In Bus.
79	A0	High	Address Bit 0
80	A1	High	Address Bit 1
81	A2	High	Address Bit 2
82	A6	High	Address Bit 6
83	A7	High	Address Bit 7
84	A8	High	Address Bit 8
85	A13	High	Address Bit 13
86	A14	High	Address Bit 14
87	A11	High	Address Bit 11
88	DO2	High	CPU Data Out Bit 2
89	DO3	High	CPU Data Out Bit 3
90	DO7	High	CPU Data Out Bit 7
91	DI4	High	Data In Bit 4 to CPU
92	DI5	High	Data In Bit 5 to CPU
93	DI6	High	Data In Bit 6 to CPU

Figure 3B (continued)

S-100 (WAMECO) BUS DESCRIPTION (Cont.)

Pin #	Mnemonic	Enabled State	Description
94	DI1	High	Data In Bit 1 to CPU
95	DI0	High	Data In Bit 0 to CPU
96	SINTA	High	CPU Interrupt Acknowledge Signal
97	SWO	Low	CPU output indicating the current cycle involves writing to a memory or I/O device.
98	SSTACK	High	CPU output indicating the address bus contains the stack address and the current cycle will have a stack operation.
99	$\overline{\text{POC}}$	Low	Power On Clear reset signal
100	GND	NA	Ground (common)

Figure 3B (continued)

I-2. Using a strong light and a magnifying glass, very carefully check all leads on the top of the board (this is the side marked "MEM-1"). If any slivers are found, carefully cut and scrape them with an Xacto knife. The underside of the board will be checked after assembly.

I-3. Place all the 14 and 16 pin sockets in their positions on the top side of the board.

**CAUTION**

DO NOT PUT A SOCKET IN THE POSITION OF THE SEVEN POSITION DIP SWITCH (T1-T7). THIS SWITCH MUST NOT BE SOCKETED. THE SWITCH WILL NOT STAY IN A SOCKET WHEN THE BOARD IS IN USE.

I-4. After positioning all sockets in place, put a book or other flat stiff object on top of the sockets. Hold the book tight against the board and turn them over so that the underside of the board is up. Press down on the board and solder one pin on each end of each socket. This will ensure the sockets are flat against the board. When tacking all sockets is completed, finish soldering all the other pins of the sockets.

**NOTE**

DO NOT PUT IC'S IN SOCKETS AT THIS TIME. THEY WILL BE INSTALLED LATER.

I-5. Bend the leads on R1-R7, R9, R10 (2.7K $\Omega$  RED, VIOLET, RED) and place in board. Check parts placement drawing (figure 4) for correct locations. Bend the leads on the resistors on the underside of the board to retain them in place until they are soldered. Turn the board over and solder all the resistors. Clip the leads of the resistors flush with the underside of the board with the diagonal pliers.

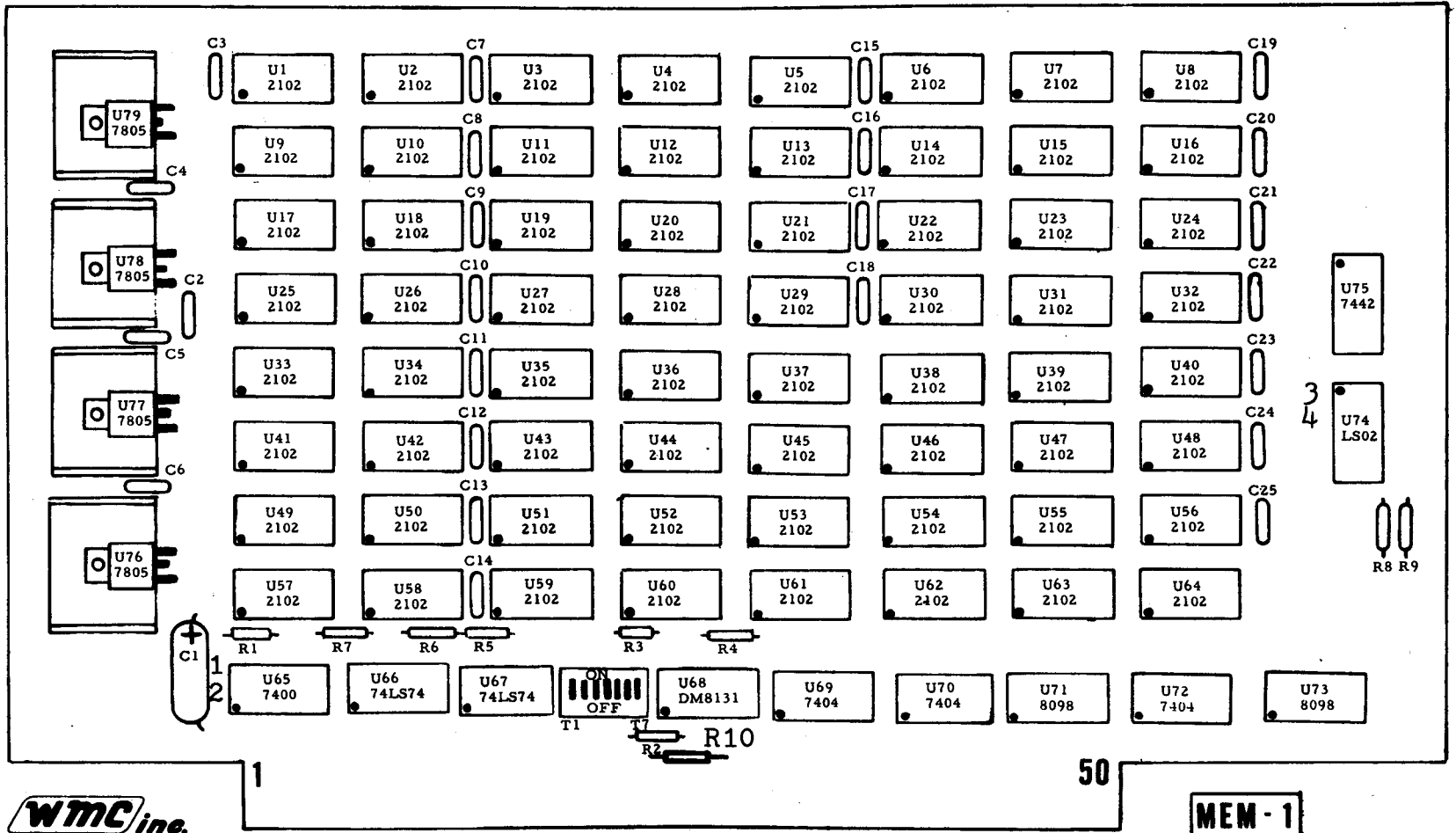
I-6. Bend the leads of R8 (1.0K $\Omega$  BROWN, BLACK, RED) and place in board. Check parts placement drawing (figure 4) for correct location. Bend the leads of the resistor to retain it in place until it is soldered. Turn the board over and solder the resistor in place. Clip the leads flush with the underside of the board with the diagonal pliers.

**CAUTION**

CHECK DISC CAPACITORS FOR PROPER VALUE BEFORE INSERTING IN BOARD. ENSURE .01 $\mu$ F AND .1  $\mu$ F DISC CAPACITORS ARE NOT INTERCHANGED.



Figure 4. MEM-1 PARTS PLACEMENT DIAGRAM



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MEM-1  
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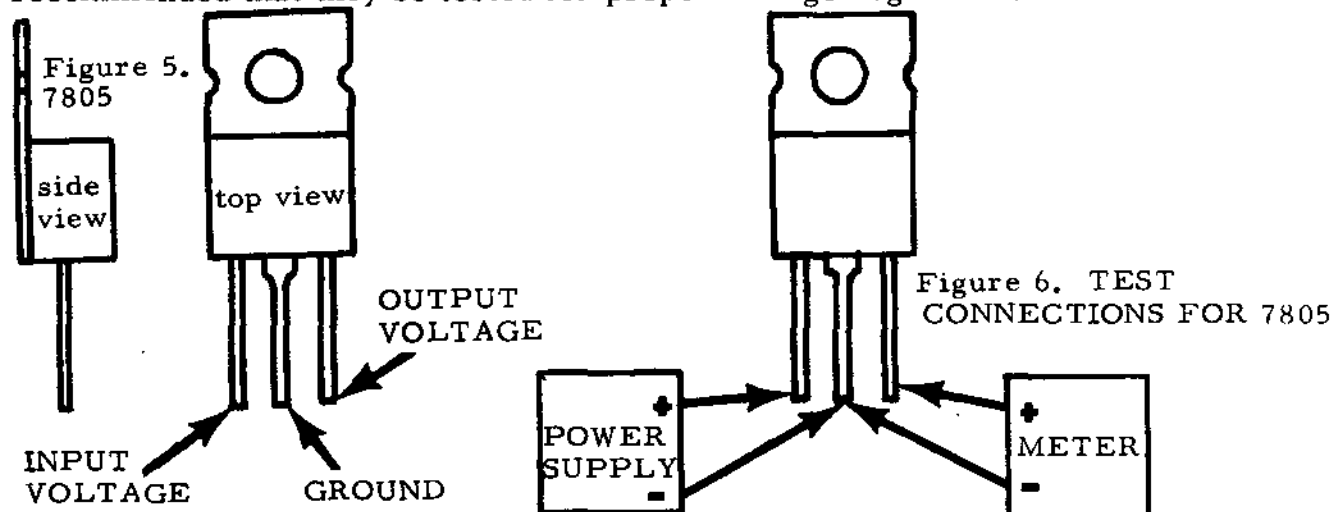
I-7. Put the leads of C7-C25 (.01 $\mu$ f) disc capacitors in the board. Check parts placement drawing (figure 4) for correct locations. Bend the leads of the capacitors to retain them in place until they are soldered in place. Turn the board over and rest each end on books. The disc capacitors are higher than the sockets and will bend if the board is not supported. Solder all the capacitors in place. Clip the leads flush with the underside of the board with the diagonal pliers.

I-8. Put the leads of C2- C6 (.1 $\mu$ f) disc capacitors in the board. Check parts location drawing (figure 4) for proper locations. Bend the leads of the capacitors to retain them in place until they are soldered. Turn the board over and rest it on books as before. Solder all the .1 $\mu$ f capacitors. Clip the leads flush with the underside of the board with the diagonal pliers.

I-9. Place C1 (15 $\mu$ f tantalum electrolytic) in place. Ensure that the polarity of C1 is correct. Check parts placement drawing (figure 4) for correct placement and polarity. Bend the leads of the capacitor to retain it in place until it is soldered. Turn the board over and rest it on books as before. Solder the capacitor in place. Clip the leads flush with the underside of the board with the diagonal pliers.

I-10. Put the seven position dip switch in place. Ensure that the switch is installed so that the off position is toward the gold fingers of the board. Bend the two pins on each end of the switch to retain it in place until it is soldered. Turn the board over and rest it on books as before. Solder the seven position dip switch in place.

I-11. Before installing the 7805 five volt regulators, it is recommended that they be tested for proper voltage regulation.



Attach the power supply and multimeter leads to the 7805 as shown in figure 6. Place the multimeter in a DC range that will allow 10 volts to be displayed. The 7805 needs a 2.0 volt minimum difference between the input voltage and the regulated output voltage. If the power supply has a voltmeter, observe the input voltage during the test. If the power supply does not have a voltmeter, switch the + meter lead between the output lead and the input lead of the 7805. The input and regulated voltages can then be observed.

I-12. Slowly increase the input voltage and observe the output voltage. When the input voltage is between 7.0 and 7.5 volts, the regulated output of a properly operating 7805 should be between 4.8 and 5.2 volts. Replace any 7805 that does not meet these limits.

I-13. When the 7805's have been tested as outlined in I-12, place the 7805's on the board so that the mounting hole on the 7805 lines up with the corresponding hole on the MEM-1. Note where the leads on the 7805's pass over the connection holes on the MEM-1. Bend the leads on the 7805's so that the leads can be inserted into the proper holes. Mount the 7805's on the board using a #6 nut and 5/8" 6-30 screw. Insert a heatsink between the board and the 7805. Solder the leads of the 7805's in place.

I-14. Remove the nuts and screws from the 7805's. Bend the 7805's upward and remove the heatsinks. Place a moderate amount of silicone thermal heat grease on the underside of the 7805's and the underside of the heatsinks with a Q tip cotton swab. Coat all of the area mentioned with an even coating of the heat grease. Reinstall the heatsinks, nuts, and screw. Ensure the nuts are tight.

I-15. This board can be configured for either of two systems. For systems with a front panel, jumper 1 to 2 (lower left side of board), leave 3 to 4 unjumped. For systems without a front panel, jumper 3 to 4 (left of U74), leave 1 to 2 unjumped.

I-16. Clean off the flux on the underside of the board with flux cleaner.

## II. Inspection and Testing

II-1. Use a bright light and magnifying glass to inspect all the traces on the underside of the board. If any slivers are found, cut and scrape them with an Xacto knife. Use the solder wick and soldering iron to remove any solder bridges found. Cover the solder bridge with flux and place a clean flux and then place a clean piece of solder wick on top of the bridge. Place the soldering iron on top of the solder wick and hold until solder is seen flowing up into the solder wick. Remove the iron and wick. Check to see if the bridge has been completely removed. If not, repeat the process until the bridge has been removed. Clean the flux off the board with flux cleaner.

### **NOTE**

AT THIS TIME NO IC'S HAVE BEEN INSTALLED ON THE BOARD.  
DO NOT INSTALL IC'S ON THE BOARD UNTIL CALLED FOR IN THE  
CHECKOUT PROCEDURE.

II-2. Place all switches of the seven position dip switch in the OFF position. Place the multimeter in the R x 1 scale. Place one probe on the gold finger for pin 1. Place the other probe on all the other fingers sequentially to check for shorts. Repeat this procedure for each pin. There should be only two sets of pins that are shorted; 1 to 51 and 50 to 100. If any other pair of pins are shorted, use a strong light and magnifying glass to locate the solder bridge or sliver causing the short. When the short has been located, correct it as outlined in II-1.

## WARNING

DO NOT INSTALL OR REMOVE ANY BOARD IN COMPUTER WITH POWER ON. DAMAGE TO BOARDS AND COMPUTER MAY RESULT.

II-3. Ensure computer is OFF. Plug the MEM-1 into the mother-board. Check that MEM-1 is correctly plugged in and the board is fully seated in the connector. Turn computer power ON and check outputs of all four regulators on MEM-1. If any regulator does not have an output voltage of 4.8 to 5.2 volts, turn computer power OFF and replace defective regulator. Repeat II-3 until all regulator voltages are good. If voltages are good, turn computer power OFF and remove MEM-1 from mother board.

II-4. Install all IC's on MEM-1. Check parts placement drawing (see Figure 4) for proper location and correct polarity of IC's.

## CAUTION

ENSURE ALL IC'S ARE INSTALLED CORRECTLY. INCORRECT POLARIZATION OF IC WILL RESULT IN DAMAGE TO IC AND CAUSE SUBSEQUENT TROUBLES TO APPEAR ON BOARD.

### III. CHECKOUT AND TROUBLESHOOTING

III-1. Set the seven position dip switch settings as follows:

T1 ON

## NOTE

FOR COMPUTER SYSTEMS WITHOUT FRONT PANEL CONTROLLERS T1 SHOULD BE IN OFF POSITION.

T2 Set according to Figure 7  
T3 Set according to Figure 7  
T4 OFF  
T5 OFF  
T6 OFF  
T7 Don't care (not used)

III-2. Reinstall the board in the computer. Ensure the board is plugged in correctly and is fully seated in the connector.

## ADDRESS SELECTION

<u>Address Range (Hex)</u>		<u>Dip Switch Setting</u>		
8K	0000-1FFF	T4	T5	T6
16K	2000-3FFF	ON	ON	ON
24K	4000-5FFF	ON	OFF	ON
32K	6000-7FFF	OFF	ON	ON
40K	8000-9FFF	OFF	OFF	ON
48K	A000-BFFF	ON	ON	OFF
56K	C000-DFFF	ON	OFF	OFF
64K	E000-FFFF	OFF	ON	OFF
		OFF	OFF	OFF
		A13	A14	A15

## WAIT STATES

<u>Ram Access Time</u>	<u>Dip Switch Setting</u>		<u>Wait Cycles</u>
Less than 550ns	T2	T3	None
550ns to 1050ns	ON	ON	1
1050ns to 1550ns	OFF	ON	1
	OFF	OFF	2

## MEMORY PROTECT

<u>Protect</u>	<u>Dip Switch Setting</u>
Protect Enable	T1
Unprotect	ON
	OFF

For computer systems without front panel controllers, T1 should be in the OFF position.

## PHANTOM

<u>Phantom</u>	<u>Dip Switch Setting</u>
ON (SOL <sup>TM</sup> systems)	T7
OFF (ALTAIR <sup>TM</sup> , IMSAI <sup>TM</sup> , etc.)	ON
	OFF

## MWRITE

<u>MWRITE Generation</u>	<u>Jumper Shorted</u>	<u>Jumper Open</u>
Systems with front panels	1 to 2	3 to 4
Systems without a front panel	3 to 4	1 to 2

Incorrect operation of board will result if both 1 to 2 and 3 to 4 are jumpered at the same time.

III-3. Ensure that no other memory board in the system is addressed to the first 8K of memory. The MEM-1 settings on T4-T6 have addressed this board for memory locations 0000-1FFF (see figure 7).

III-4. Turn computer power ON.

**NOTE**

THE NEXT SIX STEPS ARE FOR SYSTEMS HAVING A FRONT PANEL CONTROLLER. IF THE SYSTEM IS NOT SO EQUIPPED, MAKE THE NECESSARY INPUTS AS DICTATED BY YOUR PARTICULAR CONFIGURATION.

III-5. Press RESET. The computer address should indicate location 0000.

III-6. Press PROTECT. The PROTECT light should illuminate.

III-7. Set address switches to location 0000. Press EXAMINE, the PROTECT light should remain illuminated.

III-8. Press UNPROTECT. The PROTECT light should extinguish.

III-9. Press EXAMINE. The PROTECT should remain extinguished.

III-10. Deposit data into various memory locations and verify that the data deposited is correct. Ensure that PROTECT is not enabled (LIT).

III-11. For a memory diagnostic test that will check the address portion of MEM-1 and will detect stuck bit failures in the memory section of the board, load the program shown in Figure 8 into your computer.

III-12. The diagnostic program has the following data at locations 42 and 43:

42=B5  
43=20

III-13. When the program is entered in the computer, doublecheck entries to ensure the program is correct.

III-14. Press RESET, then RUN. Read locations 44-47. If there were no failures, all four addresses will read 0 0.

III-15. The program writes, then reads the information immediately to see if the data was correctly written.

III-16. After the first complete run during which all locations have been written into and verified, the program will then read all locations again during a second run. The entire test takes less than 1 second to run. The test stops at the first error located. The test will have to be rerun after each problem has been cleared until a successful test is run.

III-17. If any address for 44 through 47 was not  $\emptyset \emptyset$ , 44 and 45H will contain the failing address.

III-18. Address location 46 will contain the failing bit number. This is a direct reading, it is not in binary, octal, or hexadecimal.

Example:

Address 44 reads  $\emptyset \emptyset$   
45 reads 1B  
46 reads data bit 3  
Bit 3 of address 1B  $\emptyset \emptyset$  has failed.

III-19. Select the failing address and exercise the failing bit (s) to verify the failure.

III-20. If the memory board has malfunctioned, check the following:

A. Recheck the settings on T1-T6 to ensure they are set per step III-1.

B. Address Problems

- 1) Check U69, U70 (7400) for address bits A0 through A9.
- 2) Check U75 (7442) for address bits A10 through A12.
- 3) Check U68 (DM8131) for address bits A13 through A15.

C. Data Problems (a particular bit is always failing)

- 1) Check U70, U72 (7400) for data failing to enter memory.
- 2) Check output buffers U71, U73 (DM8098) for failure of data to be placed on the data bus.

D. Protect Problems

- 1) Check U65 (7400), U66 (74LS74) for failure of the memory to be PROTECTED/UNPROTECTED.
- 2) Check data output buffer U71 (DM8098) always or never lights DATA OUT light on the front panel.

E. If data cannot be written into memory, check the protect circuitry chips (III-20.D) and U65 (7400).

F. If there is a failure in the wait cycles, check U67 (74LS74) and U74 (74LS02).

G. If all the memory support circuitry is functional, the failures are memory chip malfunctions U1-U64 (2102AL-4). A memory map is given in figure 9. The memory is divided into eight 1K word (byte) pages. Page 0 is the left column (when component side of board is facing you with gold fingers toward you). Page 7 is on the far right side of the board. Bit 0 is at the top of the board (farthest away from gold fingers). Bit 7 is at the bottom.

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; SAME BOARD TESTER
;
; THIS PROGRAM WILL TEST OUT THE ADDRESSING OF THE RAM PAGE

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```

0000 2A4200  MMTST:  LHLD STOPA
0003 EB      XCHG      ; GET COUNTER TO DE
0004 2A4000  LHLD STRTA  ; START ADDRESS-1
0007 23      MEM1A:  INX H      ; INCREMENT ADDR
0008 7D      MOV A, L    ; LO BYTE TO ACC
0009 84      ADD H      ; ADD ADDR OFFSET
000A 77      MOV M, A    ; SAVE DATA
000B 7E      MOV A, M    ; READ DATA
000C 94      SUB H      ; SUBTRACT OFFSET
000D BD      CMP L      ; COMPARE TO LO BYTE
000E C23000  JNZ MEM1C    ; BAD LOC. - ERROR PASS I
0011 1D      DCR E      ; DONE WITH PASS I?
0012 C20700  JNZ MEM1A    ; NO, DO NEXT ADDR
0015 15      DCR D      ; MAYBE!
0016 C20700  JNZ MEM1A    ; NO, DO NEXT ADDR
0019 2A4200  LHLD STOPA  ; YES, DONE WITH PASS II
001C EB      XCHG
001D 2A4000  LHLD STRTA
0020 23      MEM1B:  INX H
0021 7E      MOV A, M    ; READ DATA
0022 94      SUB H      ; SUBTRACT OFFSET
0023 BD      CMP L      ; COMPARE LO BYTE TO ACC
0024 C23800  JNZ MEM1D    ; BAD LOC. - ERROR PASS II
0027 1D      DCR E      ; DONE WITH PASS II?
0028 C22000  JNZ MEM1B    ; NO, DO NEXT ADDR
002B 15      DCR D      ; MAYBE!
002C C22000  JNZ MEM1B    ; NO, DO NEXT ADDR
002F 76      HLT        ; YES, DONE, GOOD STUFF
                ; FOR A MONITOR SYSTEM INSERT A
                ; RESTART STATEMENT FOR THE HLT
                ; SAVE ADDR, PASS I ERROR

0030 224400  MEM1C:  SHLD ERRA
0033 6F      MOV L, A
0034 224600  SHLD ERRD  ; SAVE ERRONEOUS DATA
0037 76      HLT        ; PASS I ERROR HLT LOC
                ; FOR A MONITOR SYSTEM INSERT A
                ; RESTART STATEMENT FOR THE HLT
                ; SAVE ADDR, PASS II ERROR

0038 224400  MEM1D:  SHLD ERRA
003B 6F      MOV L, A
003C 224600  SHLD ERRD  ; SAVE ERRONEOUS DATA
003F 76      HLT        ; PASS II ERROR HLT LOCATION
                ; FOR A MONITOR SYSTEM INSERT A
                ; RESTART STATEMENT FOR THE HLT

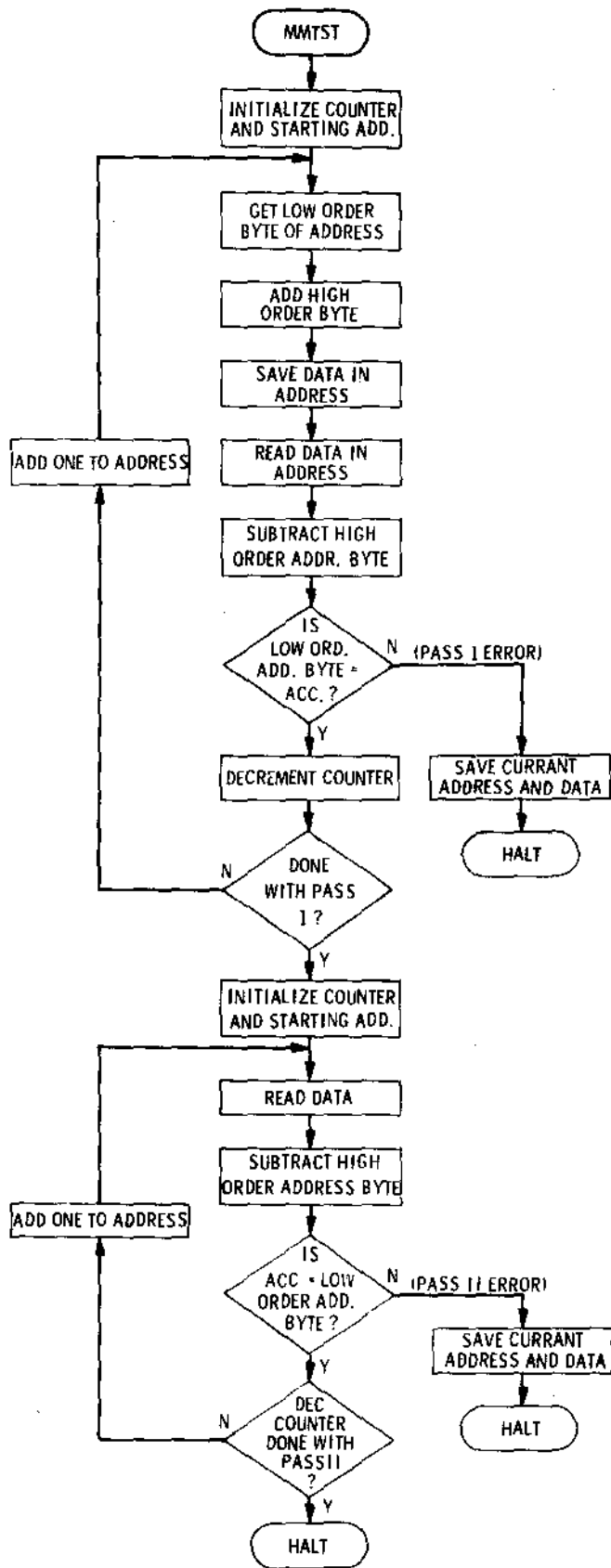
0040 4800    STRTA:  DW 48H      ; START ADDR -1
                STOPA:  DW 20B5H  ; MEMORY COUNTER=1FFF-START ADDR+ 100H
0044 0000    ERRA:   DW 0        ; ERROR - ADDRESS
0046 0000    ERRD:   DW 0        ; ERROR - DATA

0000      END

```

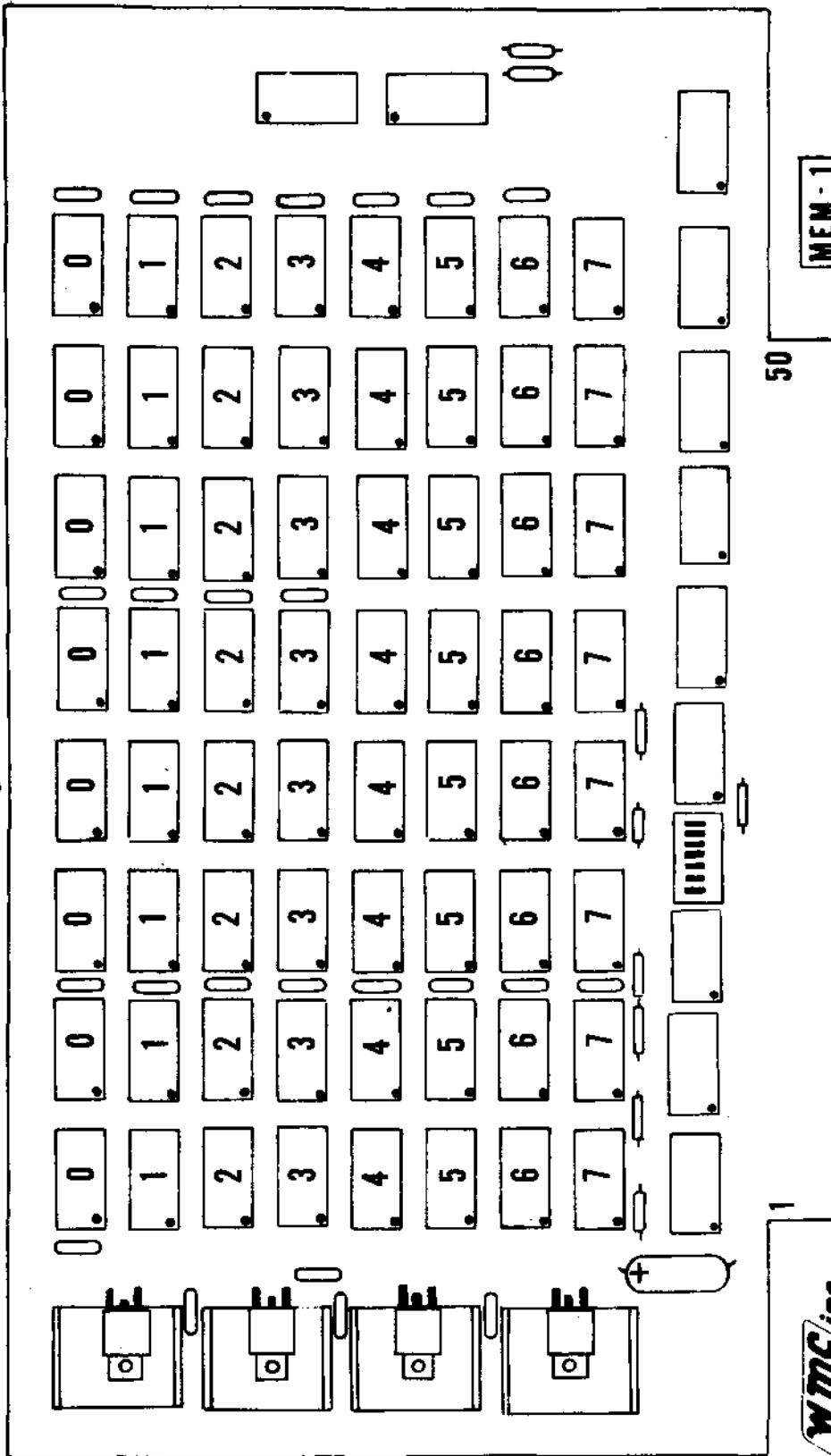
Figure 8A. DIAGNOSTIC PROGRAM LISTING





DIAGNOSTIC PROGRAM FLOWCHART Figure 8B.

PAGE 0 1 2 3 4 5 6 7



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MEM-1

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Figure 9. MEMORY MAP OF MEM-1

#### IV. GENERAL

IV-1. This WAMECO product is guaranteed for a period of ninety (90) days from date of purchase from your dealer against defects in manufacturing. Upon receipt of the defective board by WAMECO INCORPORATED, pre-paid freight or mailing, the defective board will be cheerfully replaced. The guaranty is limited to replacement of the board with an equivalent board even though the board may be defective through negligence in manufacturing or through other fault.

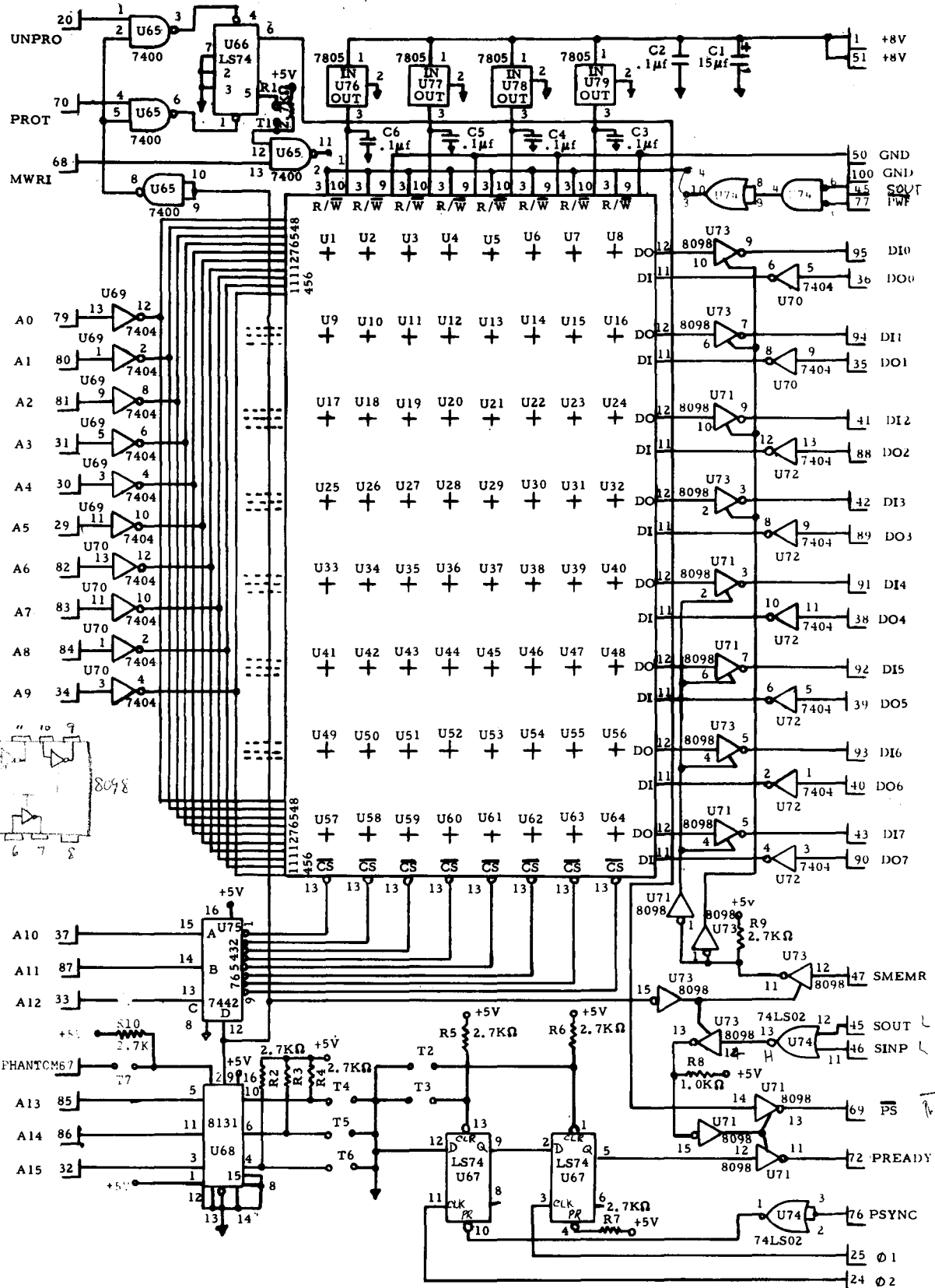
IV-2. For reference, front and rear photos of the MEM-1 board before parts installation are furnished (see Figures 11A, B).

IV-3. A detailed schematic of MEM-1 is shown in figure 10.

IV-4. We sincerely hope that MEM-1 will give you long and satisfactory service. If you have any problems with MEM-1, or if you just want to comment on the board, please write to me personally.

*Norm Walters*

Norm Walters  
President  
WAMECO INC.  
3107 Laneview Drive  
San Jose, Ca. 95132



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TM

**MEM-1**

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Figure 10. SCHEMATIC OF MEM-1

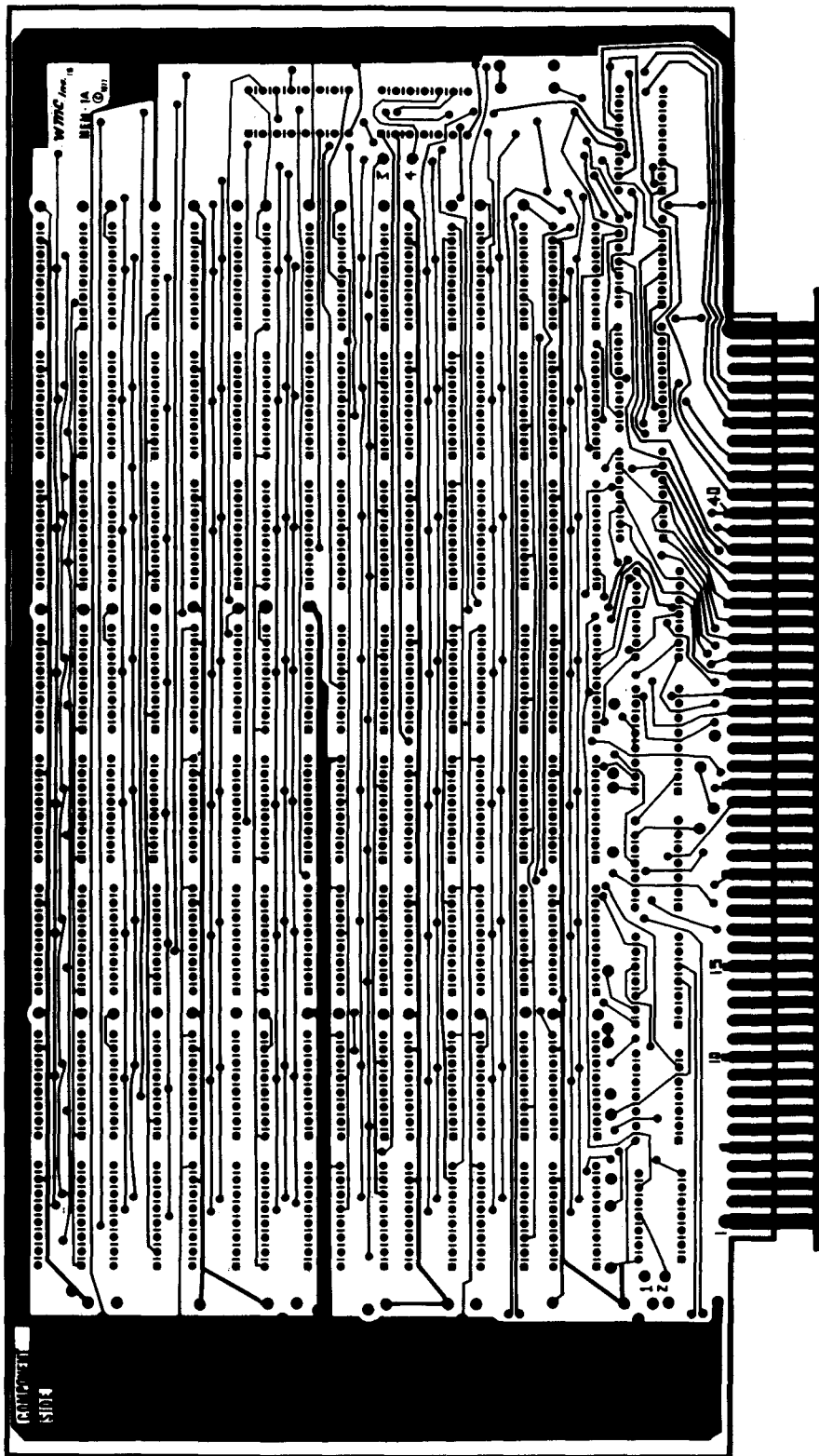
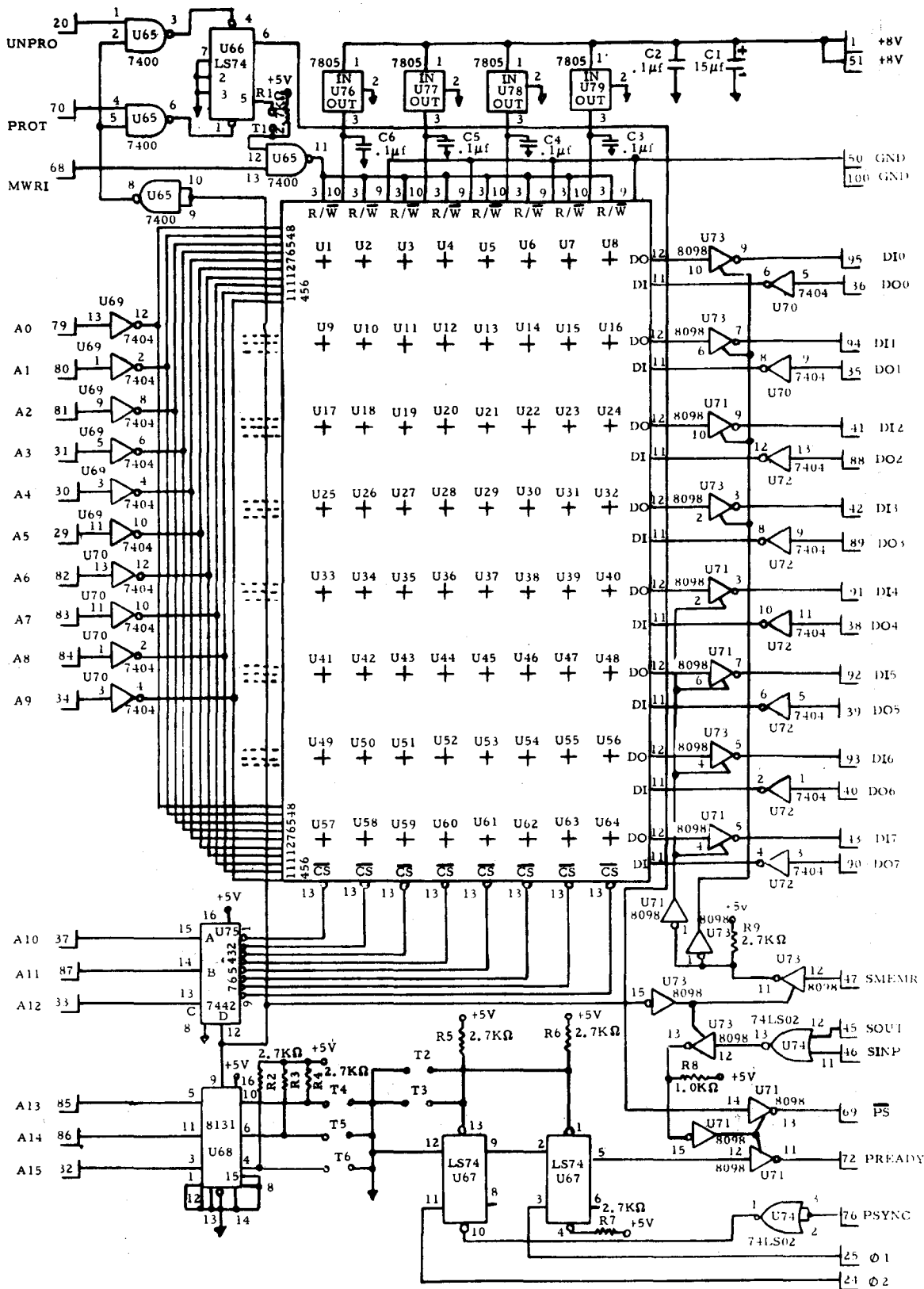


Figure 11A. COMPONENT SIDE OF MEM-1



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**MEM-1**

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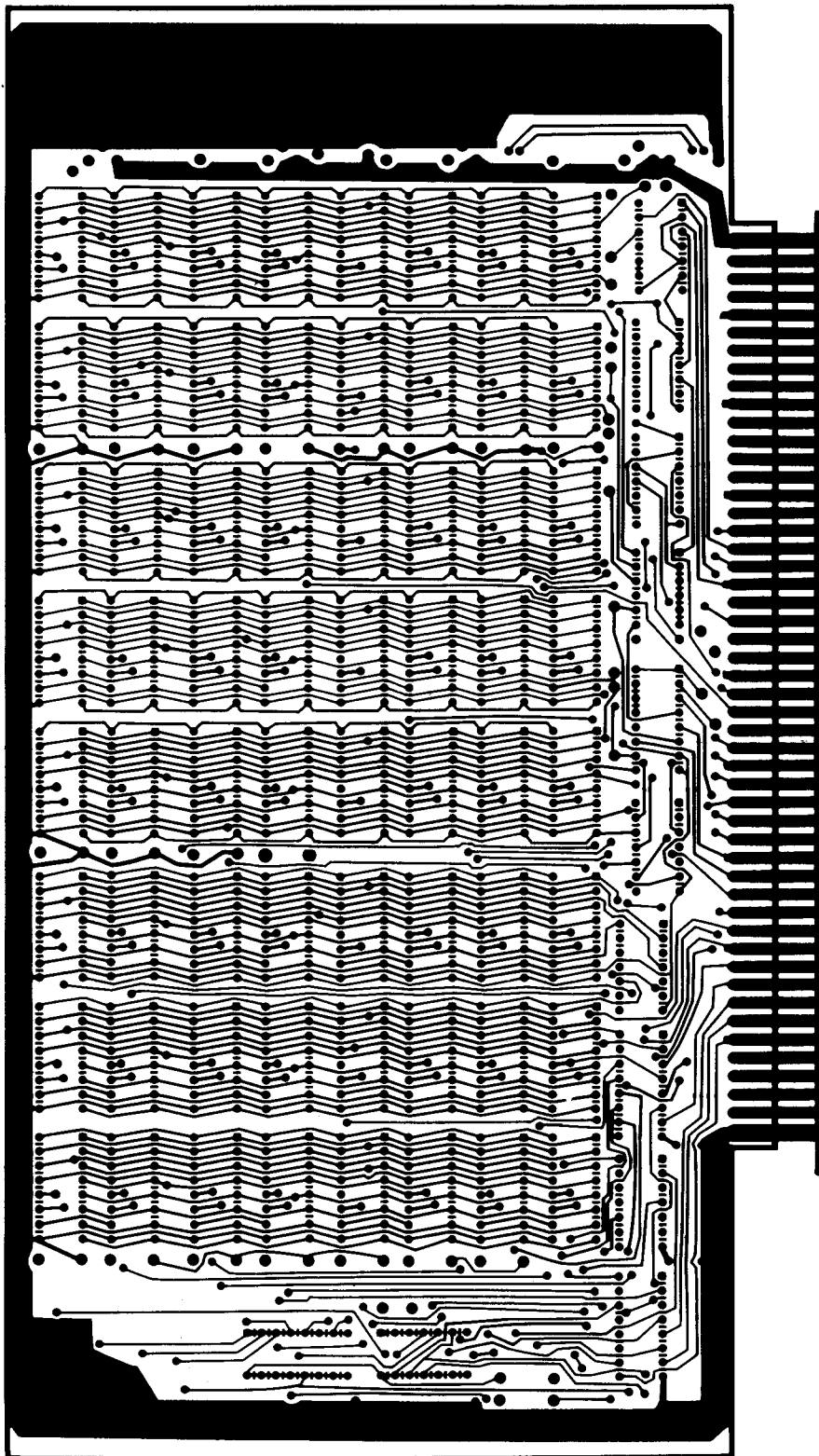


Figure 11B. REVERSE SIDE OF MEM-1