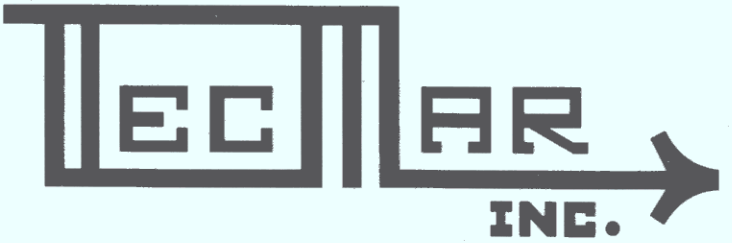

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S-100 HIGH SPEED FOUR CHANNEL 12 BIT D/A CONVERTER BOARD

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S-100 HIGH SPEED FOUR CHANNEL 12 BIT D/A CONVERTER BOARD

INTRODUCTION

The Tecmar S-100 D/A board is designed for applications requiring high speed accurate digital to analog conversion including real time applications. This board supports four independent high speed digital to analog converters (DACs) with associated latches. Each DAC operates completely independent of the rest. The DACs have a conversion time of 3 µsec which enables them to operate at maximum computer speed. A 12 bit latch drives the inputs of each DAC. Another 4 bit latch for each DAC holds the four new most significant bits waiting for the arrival of the new least significant byte. This allows the DAC to hold its previous value until an entire new word is presented to it. All the latches are set to zero by reset. To modify the contents of a latch, and hence the output of a DAC, it is necessary to send two bytes to the device. The input is a 12 bit two's complement number. User selectable output ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V are available. The user has the option of adjusting offset and gain through external pots. The board may be addressed as I/O ports or memory mapped. Only four lines of software are required to program these DACs.

FEATURES

1. I/O device
   or
   Memory mapped device.
2. Four output channels.
3. 12 bit D/A conversion.
4. S-100 compatible.
5. Three μsec conversion time.
6. ±1/2 LSB liniarity worst case.
7. Gain Error ±.1% of FSR* (adjustable to 0).
8. Offset Error ±.05% of FSR (adjustable to 0).
9. Temperature Range for Guaranteed Montonicity 0 to +70^{o}c.
10. Gain Drift ±30ppm/^{o}c maximum.
11. Jumper selectable output ranges (±2.5, ±5, ±10, 0 to +5 and 0 to +10 volts).
12. Only two instructions required in software for operating the board.
13. Each DAC operates completely independent of the rest.
14. DAC holds previous value until an <u>entire</u> new word is presented to it.
15. All the latches are set to zero by reset.
16. All voltages regulated on board.

*FSR means "full scale range".

SYSTEM REQUIREMENTS

1. The ±18 volt supply must remain above ±17 volts since it is being regulated to ±15 volts.

2. 8-I/O ports or 8 memory locations.

3. S-100 bus computer.

THEORY OF OPERATION AND HARDWARE OPERATION

The board consists of four independent D/A converters, 12 bits each, with associated latches. There is a 12-bit latch driving the inputs of the DAC itself for each DAC, and there is also a 4-bit latch for each DAC to hold a new msn (most significant nibble) waiting for the arrival of the new lsb (least significant byte). This scheme allows the D/A to hold its previous value until an entire new word is presented to it, rather than passing through an intermediate state where the output represents some bits of the old value and some bits of the new value.

Addressing is decoded using standard open-collector circuitry to achieve wired-OR operations (see Figure 1). Blocks Memory Address Select, I/O Address Select refer to this. The Latch Select uses A0 through A2 to determine which channel and whether the high or low latch will capture the incoming data.

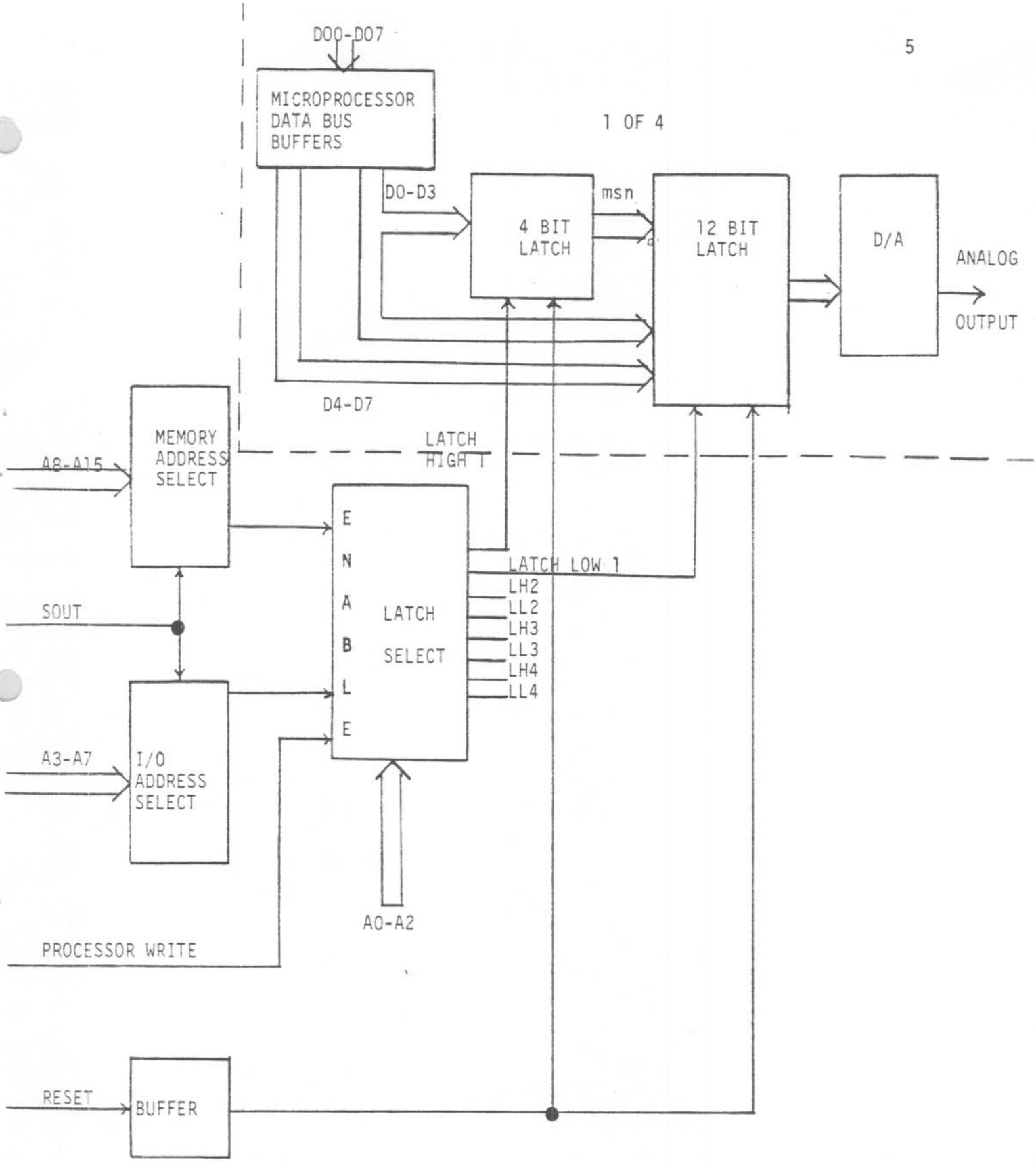
As stated earlier, each D/A has a 12 bit latch 74LS175-(N,S,R) on its inputs which is updated in two halves, a high order byte, and a low order byte. The high order byte is written first, and is stored in the four bit latch 74LS175-(P). Then when the low order byte is written, all 12 bits of the new data are updated simultaneously. The data bus is buffered with 74LS04-(A and B).

The reset line on the S-100 bus is buffered through 74LS04-(B) and goes to all latches, setting them to zero.

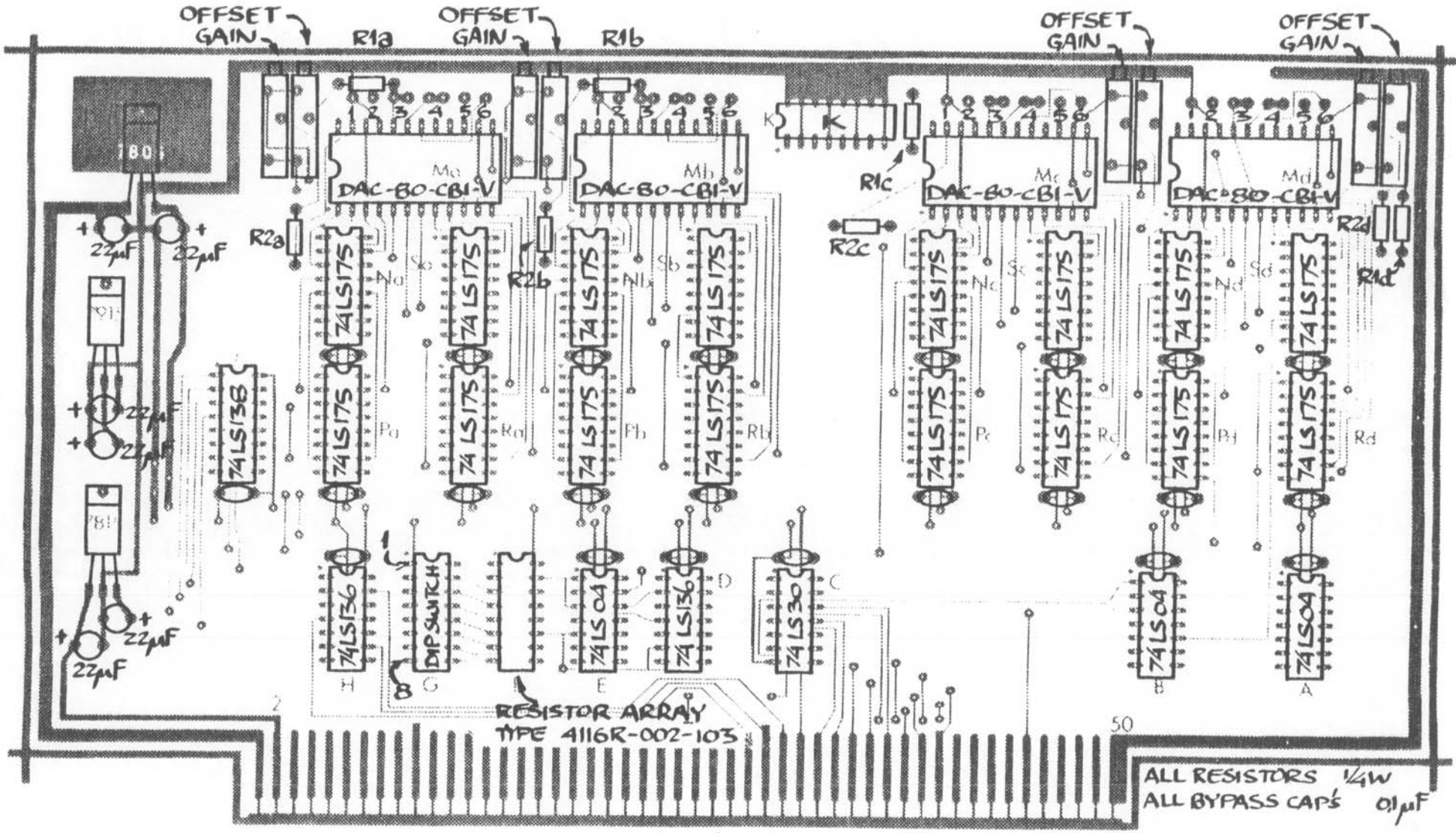
The selection of which latch to latch is done by the latch select 74LS138-(J). The choice is determined by address bits 0 through 2, and enabled by the address select circuitry. Latching is only enabled if the processor is writing and the output of both memory select blocks is true.

The memory address select is accomplished with 74LS30-(C), part of 74LS136-(D), and 74LS04-(E). It is true if memory is selected, A8 is as specified by S3, and SOUT is false (not an I/O instruction); or if memory is not selected and SOUT is true (is an I/O instruction). The switch S1, is necessary to prevent the case where SOUT=1 (I/O instruction) and the output of gate C(pin8) is true occurring as input to the XOR gate. This condition would be valid addressing in I/O mapped mode on channels FE or FF depending on the state of switch S3, but the XOR gate would incorrectly decide that another device was being addressed.

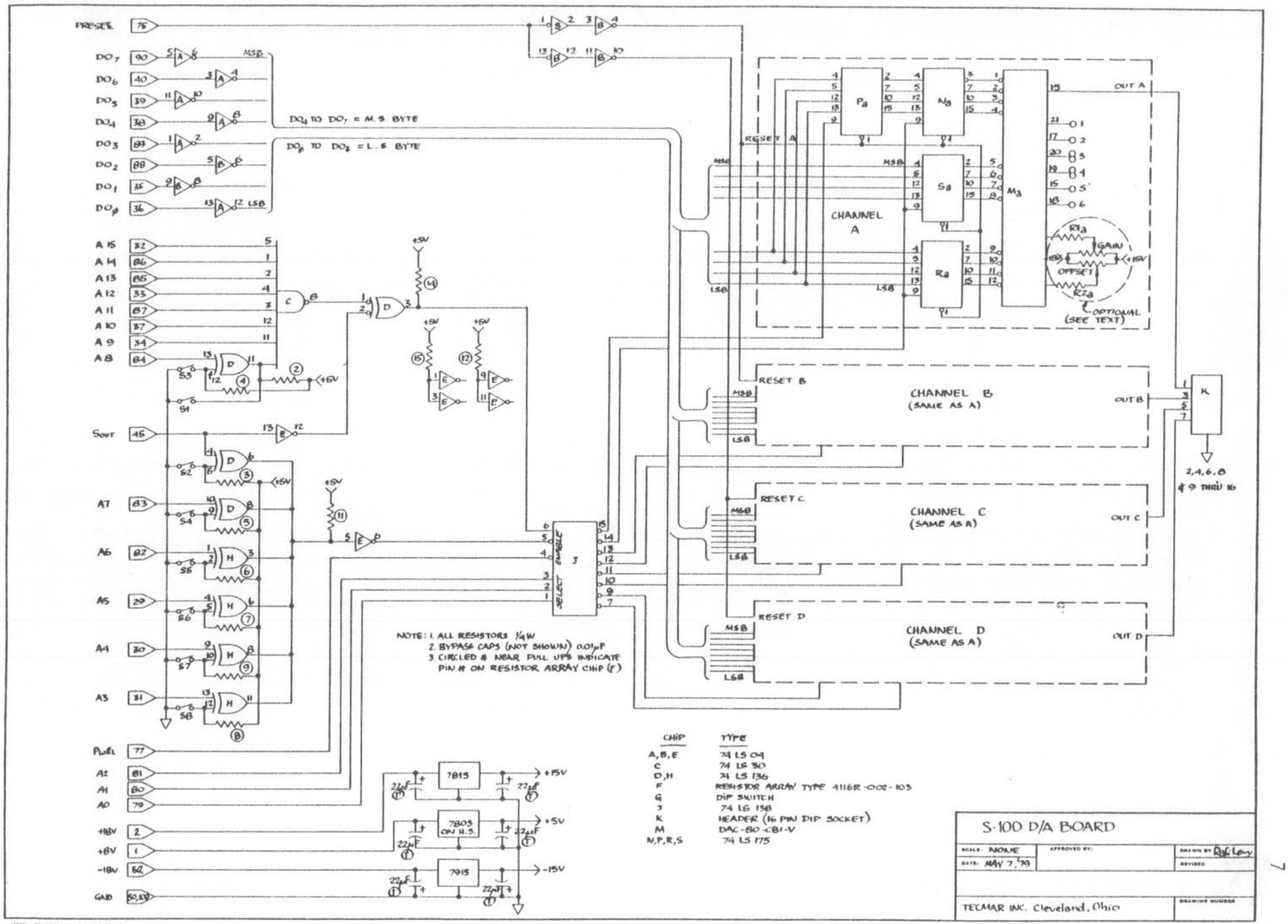
The I/O address select is accomplished with 74LS136-(H), and parts or 74LS136-(D) and 74LS04-(E). Its output is true if address bits A3 - A7 are as set in switches S8 - S4, and memory is selected and SOUT is false, or I/O is selected and SOUT is true.



FUNCTIONAL BLOCK DIAGRAM OF S-100 HIGH SPEED 12 BIT D/A CONVERTER



S-100 D/A BOARD
COMPONENTS PLACEMENT



CHIP	TYPE
A,B,E	74 LS 04
C	74 LS 30
D,H	74 LS 136
F	RESISTOR ARRAY TYPE 4116R-002-103
G	DIP SWITCH
J	74 LS 138
K	HEADER (16 PIN DIP SOCKET)
M	DAC-80-CBI-V
N,P,R,S	74 LS 175

S-100 D/A BOARD

SCALE: NONE | APPROVED BY: | DRAWN BY: Ray Levy

DATE: MAY 7, '79 | REVISED

TECMAR INC. Cleveland, Ohio | DRAWING NUMBER

NOTES ON DIGITAL TO ANALOG CONVERTERS

The D/A used is a micro networks DAC-80-CBI-V.

The input code for the D/A converters is complementary offset binary (COB). To convert 2's complement numbers to complementary offset binary, each bit is complemented except the sign bit. Examples:

	2's Complement	C.O.B.	Voltage Output
$-\infty$	1000 0000 0000	1111 1111 1111	-10V
-1	1111 1111 1111	1000 0000 0000	-.005V
0	0000 0000 0000	0111 1111 1111	0V
+1	0000 0000 0001	0111 1111 1110	+.005V
$+\infty$	0111 1111 1111	0000 0000 0000	+9.995V

$2^{10} = 1024 \setminus 2047$

The board accepts 2's complement as input and converts to COB by first inverting all incoming data (uses 74LS04 as bus receivers) and then re-inverting the sign bit by taking the $\overline{Q}$ output at the 74LS175 latch.

The system reset switch sets the D/A to -1 (-0.0049V on the ±10 volt range).

The scale of the outputs of the D/A may be strapped for:

-10V to +10V

-5V to +5V

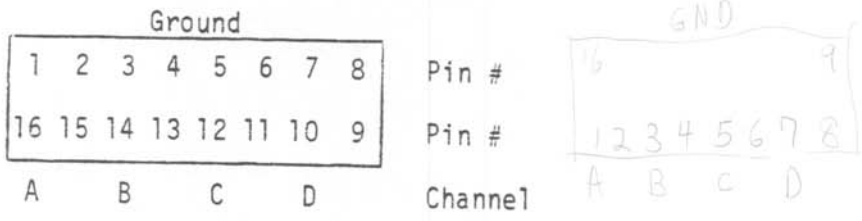
-2.5V to +2.5V

0 to +5V

0 to +10V

SWITCH AND JUMPER SUMMARY

All analog outputs are provided on one socket at the top and in the middle of the board. All pins at the top of the socket are ground. The output channels are shown below.



Channel	Pin #
A	1
B	3
C	5
D	7
GND	8 - 6

There are 8 switches in one package on the board used to determine the mode of addressing and the actual address of the D/A converters. Switch one is at the top and switch 8 is closer to the edge connector.

The switch package is marked with the word "OPEN" at one setting of each switch. (That is, the rocker switch is open when the side of it closest to the word "open" is depressed.) The opposite setting will be referred to as "closed".

Memory Mapped Operation

Switch assignments

1	Open	
2	Open	
3	A_8	(Open=0, closed=1)
4	A_7	"
5	A_6	"
6	A_5	"
7	A_4	"
8	A_3	"

Where the block of length 8 bytes, as described later, starts with location

F E
1111 111A_8 $A_7A_6A_5A_4$ $A_3$000

and ends with location

1111 111A_8 $A_7A_6A_5A_4$ $A_3$111

The memory locations correspond to the high-order and low-order bytes (Ao=0, high; Ao=1, low) of the 4 D/A registers (specified by A_2A_1). The high order byte must be stored first and any time one byte is changed both bytes have to be changed!

I/O mapped operation

Switch assignments

1	Closed
2	Closed
3	X (don't care)
4	A_7 (Open=0, closed=1)
5	A_6 (Open=0, closed=1)
6	A_5 (Open=0, closed=1)
7	A_4 (Open=0, closed=1)
8	A_3 (Open=0, closed=1)

Where the block of I/O ports, as described later, starts with port

$A_7A_6A_5A_4A_3$ 000

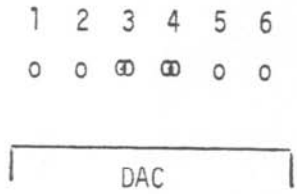
and ends with port

$A_7A_6A_5A_4A_3$ 111

The I/O ports correspond to the high-order and low-order bytes (Ao=0, high, Ao=1, low) of the 4 D/A registers (specified by A_2A_1). The high order byte must be stored first and any time one byte is changed both bytes have to be changed!

JUMPERS TO SELECT RANGE

The jumpers to select the scale are located above each DAC. The scale on each DAC must be specified and is independent of the other DACs. The jumpers are numbered from left to right as you face the board from 1 through 6 where jumpers 3 and 4 are dual jumpers. See below:



The scale can be specified as indicated below:

Scale	Connections
±10V	4-5 and 2-3
±5V	5-6 and 2-3
±2.5V	5-6 and 2-3 and 3-4
0 to +10V	5-6 and 1-2
0 to +5V	5-6 and 1-2 and 3-4

SYSTEM SET-UP (OPTIONAL)

If precision gain and offset is required the optional gain and offset pots may be installed. There are provisions for these two pots just to the left of each DAC. The pot most to the left is for gain adjustment. The pot next to the DAC (on the left) is for offset adjustment. The gain and offset pots are the same and are Bourns Part #300LP-1-503, 50KΩ multiturn parts. See component layout. R1 is 6.8 MΩ and R2 is 33 MΩ.

To adjust offset and gain:

1. Jumper DAC for ±10V range.
2. Output data F800H to appropriate DAC
3. Adjust offset pot for output of -10.000 volts
4. Output data 07FFH to appropriate DAC
5. Adjust gain pot for output of +9.951 volts

PROGRAMMING THE S-100 D/A BOARD

Each D/A board contains four D/A units and associated latches. These are accessed through a series of eight sequential addresses. Each D/A operates completely independent of the rest. All the latches are reset to zero by pressing the reset button on the console. To modify the contents of a latch, and hence the output of a D/A, it is necessary to send two bytes to the device. The first byte is sent to the lower of the two addresses associated with the particular D/A. Its lowest order four bits are the highest order four bits of the 12-bit output. The second byte is then sent to the higher of the two addresses; it contains the lowest order eight bits of the 12-bit output. The output value is a 12-bit 2's complement number which will be mapped onto the specified voltage range with the algebraically smallest (most negative) number corresponding to the smallest voltage and the largest (positive) number (2"-1) corresponding to the largest voltage. The ordering of the bytes is necessary because the board buffers the high order byte so that there are not any "glitches" in the output.

Program examples follow.

S-100 D/A BOARD

Programming - Memory mapped operation at locations FFF8-FFFF

FFF8	msb on D/A #1
FFF9	lsb on D/A #1
FFFA	msb #2
FFFB	lsb #2
FFFC	msb #3
FFFD	lsb #3
FFFE	msb #4
FFFF	lsb #4

Assume that number to be output is in register pair B-C

```
LXI  HL,0FFF8H
MOV  M,B
INX  HL
MOV  M,C
```

results in number appearing on D/A #1 after last instruction is executed.

S-100 D/A BOARD

Programming - I/O operation on channels 0 to 7

0	msb* on	D/A #1
1	lsb on	D/A #1
2	msb	#2
3	lsb	#2
4	msb	#3
5	lsb	#3
6	msb	#4
7	lsb	#4

Assume that number to be output is in register pair B-C

```
MOV  A,B
OUT  0
MOV  A,C
OUT  1
```

results in number appearing on D/A #1 after last instruction.

*msb=most significant byte
lsb=least significant byte

BOARD DEBUGGING

The board is quite straightforward. If it doesn't work, there are two places the bug could be - the S-100 interface or the latches/D/As. Set up a program to send something out to the D/A such as a ramp generated by the program.

```
Start:  MOV  A,B
        OUT  00          [or 02,04,06]
        MOV  A,C
        OUT  01          [or 03,05,07]
        INX  BC
        JMP  START
```

Putting an oscilloscope trace on the corresponding D/A output, a logic probe with a pulse detector (or another oscilloscope trace) can be used to inspect the outputs of the decoder in j. If the outputs are valid, the problem is in the latches or D/A for the particular unit in use. If you can establish which bits are incorrect, check the trace and/or replace the latch in question. If all the D/A's on one board are incorrect, put a scope trace on the power supply at the input of the chip (+15, -15, +5) while the chip is in operation. If that is OK, check the reset signal and the inverters used as bus receivers.

If the address is not being decoded directly, review the switch settings to ensure that the device is in fact addressed where it is supposed to be. On an IMSAI the addressing logic can be tested by performing an EXAMINE on the memory location corresponding to the device address and then inspecting the outputs of C, D(3), and E(6). Note that the device cannot be written to from the front panel since $\overline{PWR}$ is its strobe and $\overline{PWR}$ is not strobed by the front panel.