

TARBELL

4S - 2P

board

owner's manual

Tarbelle
Electronics

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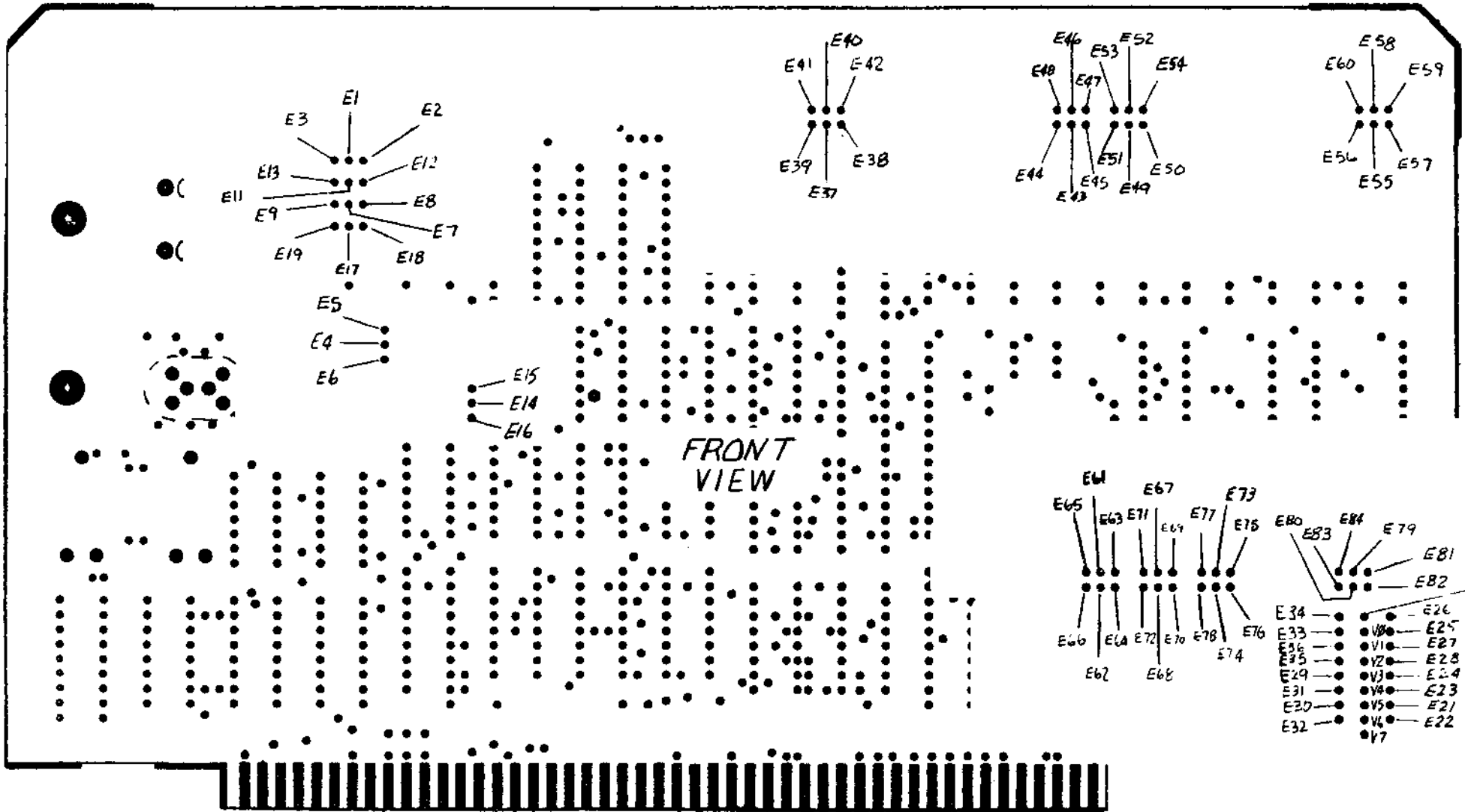
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TOP



FRONT VIEW

BOTTOM

JUMPER OPTIONS

- | | | | |
|-----|---|-----|-----|
| E34 | ● | E26 | |
| E33 | ● | V8 | E25 |
| E36 | ● | V1 | E27 |
| E35 | ● | V2 | E28 |
| E29 | ● | V3 | E24 |
| E31 | ● | V4 | E23 |
| E20 | ● | V5 | E21 |
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TAT

Introduction

The Tarbell 4 Serial, 2 Parallel board is based on 4 8251 usarts for the serial ports, and 2 parallel ports using 74LS373 octal latches. The base address for the 4 serial ports is addressed in any 8 block boundary, and the parallel ports is addressed in any 4 block boundary. The serial ports and parallel ports may be addressed independently and therefore placed in any address space you wish. The 4 serial ports may be set up in a modem configuration or left as is in a EIA RS-232 configuration. Baud rate for each port is set individually from 50 baud to 19.2 kilobaud. Full handshaking is provided at each serial port. The parallel ports likewise have full handshaking capability. Synchronous operation with the 8251's is provided by using options on the board. Full interrupt capability with both the serial and parallel ports is also provided.

Board Options (Serial Section)

1.) Address Selection (switch A9)

The 4 port serial section occupies 4 pairs of addresses as each usart takes 2 I/O port for data and I/O initialization. Therefore, the 4 port board takes a total of 8 consecutive I/O address spaces of the CPU's address space. The I/O address of the serial section is controlled by S1,S2,S3,S4,S5 of A9. S1 decodes address line A3, S2 decodes address line A4, S3 decodes Address line A5, S4 decodes address line A6, and S5 decodes address line A7. Below is a chart showing all combinations of switch settings for all possible I/O port decodes for switch A9.

(1 = on, 0 = off)

I/O Range	S1	S2	S3	S4	S5	I/O Range	S1	S2	S3	S4	S5
00 - 07 hex	1	1	1	1	1	08 - 0F hex	0	1	1	1	1
10 - 17 hex	1	0	1	1	1	18 - 1F hex	0	0	1	1	1
20 - 27 hex	1	1	0	1	1	28 - 2F hex	0	1	0	1	1
30 - 37 hex	1	0	0	1	1	38 - 3F hex	0	0	0	1	1
40 - 47 hex	1	1	1	0	1	48 - 4F hex	0	1	1	0	1
50 - 57 hex	1	0	1	0	1	58 - 5F hex	0	0	1	0	1
60 - 67 hex	1	1	0	0	1	68 - 6F hex	0	1	0	0	1
70 - 77 hex	1	0	0	0	1	78 - 7F hex	0	0	0	0	1
80 - 87 hex	1	1	1	1	0	88 - 8F hex	0	1	1	1	0
90 - 97 hex	1	0	1	1	0	98 - 9F hex	0	0	1	1	0
A0 - A7 hex	1	1	0	1	0	A8 - AF hex	0	1	0	1	0
B0 - B7 hex	1	0	0	1	0	B8 - BF hex	0	0	0	1	0
C0 - C7 hex	1	1	1	0	0	C8 - CF hex	0	1	1	0	0
D0 - D7 hex	1	0	1	0	0	D8 - DF hex	0	0	1	0	0
E0 - E7 hex	1	1	0	0	0	E8 - EF hex	0	1	0	0	0
F0 - F7 hex	1	0	0	0	0	F8 - FF hex	0	0	0	0	0

2.) Baud Rate Selection

Each of the 4 serial ports has it's own baud rate generator. There are 2 8 position dip switches which allow the setting of the baud rate for each of the 4 serial ports. A2 positions 1,2,3,4 control channel D, A2 positions 5,6,7,8 control channel C, A4 positions 1,2,3,4 control channel B, and A4 positions 5,6,7,8 control channel A. Below is a table of all baud rate settings for which all channels may be set.

Switch	A2 and A4
1	[--] -----
2	[--] Chan B
3	[--] or D
4	[--] -----
5	[--] -----
6	[--] Chan A
7	[--] or C
8	[--] -----

Baud Rate	1 or 5	2 or 6	3 or 7	4 or 8
50	on	on	on	on
75	off	on	on	on
110	on	off	on	on
134.5	off	off	on	on
150	on	on	off	on
300	off	on	off	on
600	on	off	off	on
1200	off	off	off	on
1800	on	on	on	off
2000	off	on	on	off
2400	on	off	on	off
3600	off	off	on	off
4800	on	on	off	off
7200	off	on	off	off
9600	on	off	off	off
19200	off	off	off	off

3.) Interrupt Options for Serial Ports

Interrupts may be used with each of the 4 serial ports for Receive Ready, Transmit Ready, Transmit Empty, and Sync Detect / Break detect. These 4 lines each drive a 7406 open collector inverters. The outputs of these inverters may be wired-OR to any of the vector interrupt lines (VI0 - VI7) on the S-100 bus. Below is a table showing the interrupt outputs which are provided for each channel.

Signal	Chan D	Chan C	Chan B	Chan A
Sync/Brk Detect	E33	E29	E25	E21
Transmit Empty	E34	E30	E26	E22
Transmit Ready	E35	E31	E27	E23
Receive Ready	E36	E32	E28	E24

4.) Asynchronous / Synchronous Options

Several jumpers are provided to allow the choice of either Synchronous or Asynchronous operation with the 4 serial ports. below is a table showing all the possible jumper options for each serial port.

Channel	Synchronous	Asynchronous
A	E40 to E42	E40 to E41
	E37 to E38	E37 to E39
	E62 to E66	E62 to E64
	E61 to E65	E61 to E63
B	E46 to E48	E46 to E47
	E43 to E44	E43 to E45
	E68 to E72	E68 to E70
	E67 to E71	E67 to E69
C	E52 to E54	E52 to E53
	E49 to E50	E49 to E51
	E74 to E78	E74 to E76
	E73 to E77	E73 to E75
D	E58 to E60	E58 to E59
	E55 to E56	E55 to E57
	E80 to E84	E80 to E82
	E79 to E83	E79 to E81

Note - If you are going to run Synchronous operation, you must provide external transmit and receive clocks from the device attached to that channel.

5.) Modem Options

The 4 serial ports may be configured as modem ports instead of RS-232 ports which is the standard way the board is shipped. 4 user definable areas are provided (1 for each serial port), which allow the the option of setting any or all serial ports in the modem configuration. Below is a table of the options which show the modem and standard RS-232 mode.

Channel	Socket	Std. RS-232	Pins	Modem	Pins
		A1 - A2 -->	1 - 16	A1 - D2 -->	1 - 13
		B1 - B2 -->	2 - 15	B1 - E2 -->	2 - 12
A	(P4)	C1 - C2 -->	3 - 14	C1 - F2 -->	3 - 11
B	(P3)	D1 - D2 -->	4 - 13	D1 - A2 -->	4 - 16
C	(P2)	E1 - E2 -->	5 - 12	E1 - B2 -->	5 - 15
D	(P1)	F1 - F2 -->	6 - 11	F1 - C2 -->	6 - 14
		G1 - G2 -->	7 - 10	G1 - H2 -->	7 - 9
		H1 - H2 -->	8 - 9	H1 - G2 -->	8 - 10

Handshaking for the serial ports is provided by the RS-232 line drivers and line receivers which are 1488's and 1489's by way of connectors J1 and J2. A break down of these connectors is as follows:

J1 and J2 pin #	Channel	Function	In/Out
1	A - C	ground / Ext TxC	input
2	A - C	ground / Ext RxC	input
3	A - C	transmit	output
4	A - C	data terminal ready	output
5	A - C	request to send	output
6	A - C	receive data	input
7	A - C	data set ready	input
8	A - C	clear to send	input
9		+ 5 volts	
10		+ 12 volts	
11		- 12 volts	
12		ground	
13	B - D	transmit data	output
14	B - D	data terminal ready	output
15	B - D	request to send	output
16	B - D	receive data	input
17	B - D	data set ready	input
18	B - D	clear to send	input
19	B - D	ground / Ext TxC	input
20	B - D	ground / Ext RxC	input

The I/O cable coming from the 20 pin connectors (J1 and J2) on the 4 Port Serial board to the DB-25 configuration blocks is defined as follows for RS-232 operation asynchronous mode:

	RS-232 pin connector	Asynchronous Mode -----	20 pin connector
---	(2)	Xmit Data (from I/O board)	3
	(3)	Recv Data (to I/O board)	6
A - C	(4)	Rts	5
Ports	(5)	Cts	8
	(6)	Dsr (handshake line)	7
	(7)	Gnd	1,2
---	(20)	Dtr	4
		+ 5 volts	9
Pull up's		+12 volts	10
		-12 volts	11
---	(2)	Xmit Data (from I/O board)	13
	(3)	Recv Data (to I/O board)	16
B - D	(4)	Rts	15
Ports	(5)	Cts	18
	(6)	Dsr (handshake line)	17
	(7)	Gnd	19,20
---	(20)	Dts	14

The I/O cable coming from the 20 pin connectors (J1 and J2) on the 4 Port Serial board to the DB-25 configuration blocks is defined below for RS-232 operation synchronous mode external Trans/Recv clocks:

	RS-232 pin connector	Synchronous Mode -----	20 pin connector
---	(15)	Ext Recv Clock input	1
	(2)	Xmit Data (from I/O board)	3
	(3)	Recv Data (to I/O board)	6
A - C	(4)	Rts	5
Ports	(5)	Cts	8
	(6)	Dsr (handshake line)	7
	(7)	Gnd	12
	(17)	Ext Xmit Clock input	2
---	(20)	Dtr	4
		+ 5 volts	9
Pull up's		+12 volts	10
		-12 volts	11
---	(15)	Ext Recv Clock input	20
	(2)	Xmit Data (from I/O board)	13
	(3)	Recv Data (to I/O board)	16
B - D	(4)	Rts	15
Ports	(5)	Cts	18
	(6)	Dsr (handshake line)	17
	(7)	Gnd	12
	(17)	Ext Xmit Clock input	19
---	(20)	Dts	14

Software Interface

In order to use the 4 Port Serial board, the Usarts must be initialized after a reset is performed by your system. Below is a typical routine to perform this initialization in your software. The code is written in 8080 assembly language and may be included in your software. The I/O port for this example is assumed to be at 10 hex base address. Also shown is a typical subroutine to handle a printer with handshaking. Please note that this routine is important in order that the printer handshake correctly with the Usart.

```

;
;program to initialize the 4 8251A usarts
;after a system reset has been performed.
;
BASE      EQU      10H                ;base port starting address
CCOMA     EQU      BASE + 01H         ;channel A init command port
CSTATA   EQU      BASE + 01H         ;channel A status port
CDATA    EQU      BASE + 00H         ;channel A data port
CIMSKA   EQU      00000010B         ;channel A input mask value
COMSKA   EQU      00000001B         ;channel A output mask value
;
CCOMB     EQU      BASE + 03H         ;channel B init command port
CSTATB   EQU      BASE + 03H         ;channel B status port
CDATB    EQU      BASE + 02H         ;channel B data port
CIMSKB   EQU      00000010B         ;channel B input mask value
COMSKB   EQU      00000001B         ;channel B output mask value
;
CCOMC     EQU      BASE + 05H         ;channel C init command port
CSTATC   EQU      BASE + 05H         ;channel C status port
CDATC    EQU      BASE + 04H         ;channel C data port
CIMSKC   EQU      00000010B         ;channel C input mask value
COMSKC   EQU      00000001B         ;channel C output mask value
;
CCOMD     EQU      BASE + 07H         ;channel D init command port
CSTATD   EQU      BASE + 07H         ;channel D status port
CDATD    EQU      BASE + 06H         ;channel D data port
CIMSKD   EQU      00000010B         ;channel D input mask value
COMSKD   EQU      00000001B         ;channel D output mask value
;
;this is the init subroutine
;
;entry parameters:      none
;exit parameters:      8251's initialized
;registers used:       HL, B, A
;
INIT:     LXI      H,ITABLE           ;point to init table
          MVI      B,4                ;4 entries in the table
INITL:    MOV      A,M               ;get a byte from table
          OUT      CCOMA              ;send to channel A
          OUT      CCOMB              ;send to channel B
          OUT      CCOMC              ;send to channel C
          OUT      CCOMD              ;send to channel D
          INX      H                  ;bump pointer to next byte

```

```

        DCR      B           ;decrease byte count
        JNZ     INITL      ;jump to init loop till done
        RET                          ;return to caller
;
;init byte table
;
ITABLE: DB      0AAH,040H,0CEH,037H
;
;this subroutine may be used for the CP/M
;console status checking. This example applies
;to all 4 ports, even though only chan. A is shown.
;
;entry parameters:      none
;exit parameters:      reg = CP/M ready condition
;registers used:       reg A
;
CONST:  IN      CSTATUS   ;get status byte
        ANI     CSTATUS   ;check for ready
        MVI     A,0       ;00 = not ready
        RZ                          ;return if not ready
        CMA                          ;else flip to FF hex
        RET                          ;and return it's ready
;
;this subroutine may be used for the CP/M console
;input routine. This example applies to all 4 Ports,
;even though only chan. A is shown.
;
;entry parameters:      none
;exit parameters:      reg A = the character for CP/M
;registers used:       reg A
;
CONIN:  IN      CSTATUS   ;check status byte
        ANI     CSTATUS   ;check if key pushed
        JZ      CONIN     ;jump if no key pushed
        IN      CSTATUS   ;else, get the char in usart reg.
        ANI     7FH       ;strip parity bit off
        RET                          ;return to caller
;
;this subroutine may be used for the CP/M console
;output routine. This example applies to all 4 Ports,
;even though only chan. A is shown.
;
;entry parameters:      reg C = output character
;exit parameters:      reg A = output character
;registers used:       reg C, A
;
CONOT:  IN      CSTATUS   ;check for output ready
        ANI     COMSKA    ;check output ready bit
        JZ      CONOT    ;jump if not ready to output
        MOV     A,C       ;else, get the character to reg A
        OUT    CDATA     ;and send it to console
        RET                          ;return to caller

```

```

;
;this subroutine may be used for the CP/M list status check.
;
;entry parameters:      none
;exit parameters:      reg A = ready condition
;registers used:       reg A
;
PRDY    EQU    10000001B    ;this byte is I M P O R T A N T
;
PSTAT:  IN      CSTATUS    ;check status byte
        ANI    PRDY        ;mask off ready bits
        XRI    PRDY        ;this is I M P O R T A N T !
        MVI    A,0         ;return not ready byte
        RNZ
        CMA                ;else flip to FF hex if ready
        RET                ;return to caller
;
;this subroutine may be used for the CP/M list
;output routine.
;
;entry parameters:     reg C = output character
;exit parameters:     reg A = output character
;registers used:      reg A
;
POUT:   IN      CSTATUS    ;check status byte
        ANI    PRDY        ;mask ready condition
        XRI    PRDY        ;this is I M P O R T A N T !
        JNZ    POUT        ;observe the jump instruction
        MOV    A,C         ;if ready, get the character
        OUT    CSTATUS     ;send to lister device
        RET                ;return to caller

```

Parallel Interface

Parallel Port I/O Decode (switch A7)

The parallel interface is comprised of two (2) parallel input ports and two (2) parallel output ports with full handshaking and interrupt capability. The I/O base address may be set anywhere within the processors I/O address space on 4 block boundaries. Below is a table of all legal address decodes for the parallel ports.

Note (1 = on, 0 = off)

I/O Range	S6	S5	S4	S3	S2	S1	I/O Range	S6	S5	S4	S3	S2	S1
00 - 03 hex	1	1	1	1	1	1	04 - 07 hex	1	1	1	1	1	0
08 - 0B hex	1	1	1	1	0	1	0C - 0F hex	1	1	1	1	0	0
10 - 13 hex	1	1	1	0	1	1	14 - 17 hex	1	1	1	0	1	0
18 - 1B hex	1	1	1	0	0	1	1C - 1F hex	1	1	1	0	0	0
20 - 23 hex	1	1	0	1	1	1	24 - 27 hex	1	1	0	1	1	0
28 - 2B hex	1	1	0	1	0	1	2C - 2F hex	1	1	0	1	0	0
30 - 33 hex	1	1	0	0	1	1	34 - 37 hex	1	1	0	0	1	0
38 - 3B hex	1	1	0	0	0	1	3C - 3F hex	1	1	0	0	0	0
40 - 43 hex	1	0	1	1	1	1	44 - 47 hex	1	0	1	1	1	0
48 - 4B hex	1	0	1	1	0	1	4C - 4F hex	1	0	1	1	0	0
50 - 53 hex	1	0	1	0	1	1	54 - 57 hex	1	0	1	0	1	0
58 - 5B hex	1	0	1	0	0	1	5C - 5F hex	1	0	1	0	0	0
60 - 63 hex	1	0	0	1	1	1	64 - 67 hex	1	0	0	1	1	0
68 - 6B hex	1	0	0	1	0	1	6C - 6F hex	1	0	0	1	0	0
70 - 73 hex	1	0	0	0	1	1	74 - 77 hex	1	0	0	0	1	0
78 - 7B hex	1	0	0	0	0	1	7C - 7F hex	1	0	0	0	0	0
80 - 83 hex	0	1	1	1	1	1	84 - 87 hex	0	1	1	1	1	0
88 - 8B hex	0	1	1	1	0	1	8C - 8F hex	0	1	1	1	0	0
90 - 93 hex	0	1	1	0	1	1	94 - 97 hex	0	1	1	0	1	0
98 - 9B hex	0	1	1	0	0	1	9C - 9F hex	0	1	1	0	0	0
A0 - A3 hex	0	1	0	1	1	1	A4 - A7 hex	0	1	0	1	1	0
A8 - AB hex	0	1	0	1	0	1	AC - AF hex	0	1	0	1	0	0
B0 - B3 hex	0	1	0	0	1	1	B4 - B7 hex	0	1	0	0	1	0
B8 - BB hex	0	1	0	0	0	0	C0 - C3 hex	0	0	1	1	1	1
C4 - C7 hex	0	0	1	1	1	0	C8 - CB hex	0	0	1	1	0	1
CC - CF hex	0	0	1	1	0	0	D0 - D3 hex	0	0	1	0	1	1
D4 - D7 hex	0	0	1	0	1	0	D8 - DB hex	0	0	1	0	0	1
DC - DF hex	0	0	1	0	0	0	E0 - E3 hex	0	0	0	1	1	1
E4 - E7 hex	0	0	0	1	1	0	E8 - EB hex	0	0	0	1	0	1
EC - EF hex	0	0	0	1	0	0	F0 - F3 hex	0	0	0	0	1	1
F4 - F7 hex	0	0	0	0	1	0	F8 - FB hex	0	0	0	0	0	1
FC - FF hex	0	0	0	0	0	0							

Note that you should not place either the Serial ports or the Parallel ports at the same address base as the decode on board does not distinguish between the two sections and therefore may cause unpredictable results.

Parallel Connector Definition

The Parallel interface connectors, J3 and J4 provide data input/output, power, ground, and handshaking. Below is a break down of J3 and J4.

Note (J3 is parallel port 0 and J4 is parallel port 1)

<u>J3 and J4 pins</u>	<u>Function</u>
3	data out 0,1 (bit 0)
5	data out 0,1 (bit 1)
7	data out 0,1 (bit 2)
9	data out 0,1 (bit 3)
11	data out 0,1 (bit 4)
13	data out 0,1 (bit 5)
15	data out 0,1 (bit 6)
17	data out 0,1 (bit 7)
19	data out ack (active low)
21	data out strobe (active high/low)
4	data in 0,1 (bit 0)
6	data in 0,1 (bit 1)
8	data in 0,1 (bit 2)
10	data in 0,1 (bit 3)
12	data in 0,1 (bit 4)
14	data in 0,1 (bit 5)
16	data in 0,1 (bit 6)
18	data in 0,1 (bit 7)
20	data in strobe (active high)
22	data in ack (active low)
1	ground
25	ground
23	+ 5 volts
24	+ 5 volts
2	reset (active high)

Parallel Port to DB-25 Definition

The interface between the 26 pin connectors in the I/O board and the DB-25 connectors provided is defined below:

<u>J3 and J4 Connector</u>	<u>DB-25 Connector</u>
3	2 (data out bit 0)
5	3 (data out bit 1)
7	4 (data out bit 2)
9	5 (data out bit 3)
11	6 (data out bit 4)
13	7 (data out bit 5)
15	8 (data out bit 6)
17	9 (data out bit 7)
19	10 (data out ack)
21	11 (data out strobe)
4	15 (data in bit 0)
6	16 (data in bit 1)
8	17 (data in bit 2)
10	18 (data in bit 3)
12	19 (data in bit 4)
14	20 (data in bit 5)
16	21 (data in bit 6)
18	22 (data in bit 7)
20	23 (data in strobe)
22	24 (data in ack)
1	1 ground
2	14 reset
25	13 ground
23	12 + 5 volts
24	25 + 5 volts

Parallel Port Options

1.) Parallel output enable option

The output side of the parallel ports (D6 and D8) has two (2) options for data out enable. Below is a table showing these options.

Chan 0 and 1 Function	Jumper option
Output data Strobed by <u>OUTACK</u>	E1 to E3 (for chan 0) E11 to E13 (for chan 1)
Output data always enabled (no strobe used)	E1 to E2 (for chan 0) E11 to E12 (for chan 1)

2.) Parallel input enable option

The input side of the parallel ports (D5 and D7) has two (2) options for data input enable. Below is a table showing these options.

Chan 0 and 1 Function	Jumper option
Input data Strobed by INSTB	E7 to E9 (for chan 0) E17 to E19 (for chan 1)
Input data passed straight through	E7 to E8 (for chan 0) E17 to E18 (for chan 1)

3.) Parallel Interrupt Option

Interrupts may be used with the input side of the two (2) parallel ports if wanted. The interrupt drivers are open collector 7406 inverters which may be wired-OR to any of the vector interrupt lines (VI0 - VI7) on the S-100 bus. The interrupt, once set, is latched by flip-flops C6 for parallel port channel 0, and C5 for parallel port channel 1. The interrupt will be cleared by reading the data at each port respectively. below is a table for interrupt selection for each parallel port.

Channel	Jumper	Channel	Jumper
0	E10	1	E20

4.) Parallel Output Strobe Polarity Option

The polarity of the output strobe is user selectable by means of jumpers. Below is a table showing the jumper options for channel 1 and 2.

Channel	Polarity	Jumper	Channel	Polarity	Jumper
0	positive	E4 to E5	0	negative	E4 to E6
1	positive	E14 to E15	1	negative	E14 to E16

Parallel Port Software Example

This is an example of an Input / Output routine for the Parallel Ports.

Note: If you are going to use the parallel ports in strobed mode, you must first do a dummy READ on the data in ports of each channel to arm the strobe lines. This may be done in your initialization routine in your program.

```

;
;define Equates
;
PSTAT0 EQU 061H ;status port channel 0
PDATA0 EQU 060H ;data port channel 0
PSTAT1 EQU 063H ;status port channel 1
PDATA1 EQU 062H ;data port channel 1
INRDY EQU 0000001B ;mask value for input ready
OTRDY EQU 1000000B ;mask value for output ready
;
;example of initialization for
;strobed parallel port operation
;
.
.
initialization body
.
.
IN PDATA0 ;dummy read to prime strobes chan 0
IN PDATA1 ;dummy read to prime strobes chan 1
.
.
initialization body

```

```

;
;parallel port in routine
;
;INPUT routine
;
;entry parameters:      none
;exit parameters:      reg A = character
;registers used:       reg A
;
INPUT:  IN          PSTATO          ;check channel 0 status port
        ANI         INRDY          ;is there a char there?
        JNZ         INPUT          ;retry again if no char waiting
        IN          PDATA0         ;yes, get the character
        RET         ;return to caller
;
;parallel port output routine
;
;OUTPUT routine
;
;entry parameters:      reg C = character to output
;exit parameters:      reg A = character
;registers used:       reg C, A
;
OUTPUT: IN          PSTATO          ;check channel 0 status port
        ANI         OTRDY          ;is latch busy from previous out?
        JZ          OUTPUT         ;jump and retry if yes
        MOV         A,C            ;else, get character to output
        OUT         PDATA0         ;send to output latch
        RET         ;return to caller

```

Parts List

IC's

Qty	Type	Description	Location
1	7402	Quad 2 input NOR gate	C9
2	7404	Hex inverter	B3,B5
3	7406	Hex inverter (O.C.)	A13,A14,A15
1	7408	Quad 2 input AND gate	B6
3	7432	Quad 2 input OR gate	B7,B8,C8
3	7474	"D" toggle flip-flop	B9,C5,C6
2	8131	6 bit comparator	A6,A10
4	1488	EIA converter (tran)	C10,D12,D14,D16
5	1489	EIA converter (recv)	B10,D9,D11,D13,D15
4	8251A	Usart	B11,B13,B14,B16
2	5016 / 1941	Baud rate generator	A1,A5
1	74125	Quad tri-state buffer	C7
1	74LS139	Dual 4 line decoder	B9
2	74LS244	Tri-state octal driver	A11,A12
4	74LS373	Tri-state octal latch	D5,D6,D7,D8
1	LM-323	+ 5 Volt regulator	
1	7812	+ 12 Volt regulator	
1	7912	- 12 Volt regulator	

Resistors

2	220 ohm 1/4W or 1/8W	R5,R6
4	330 ohm 1/4W	R1,R2,R3,R4
3	4.7K ohm resistor pack (NW154.7)	A3,A8,D10

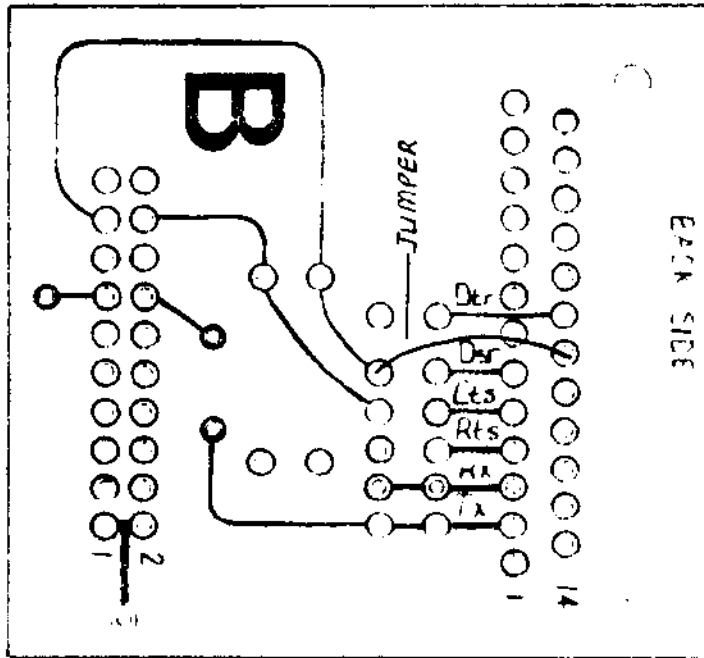
Capacitors

2	100 pf	C1,C17
10	.1 mfd @ 12 volts	
6	10 mfd @ 16 volts	

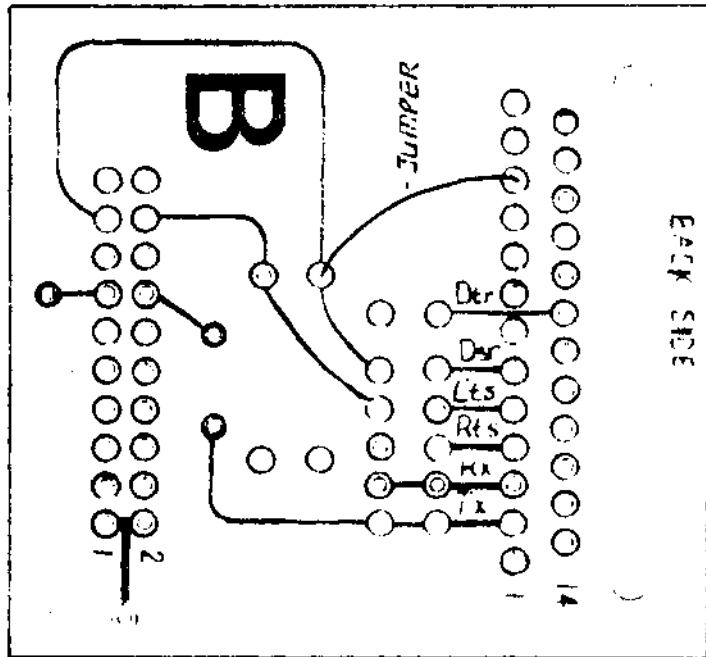
Hardware

1	4 MHz crystal	Y2
1	5.0688 MHz crystal	Y1
4	8 position dip switch	A2,A4,A7,A9
2	20 pin connector (male)	J1,J2
2	26 pin connector (male)	J3,J4
1	heatsink (for LM-323)	
2	heatsink (for 7812 and 7912)	
84	jumper pins (male)	"E" jumpers
22	jumper blocks (female)	"E" jumpers
2	20 pin Serial Cables	J1,J2
2	26 pin Parallel Cables	J3,J4

ANADEx 9501

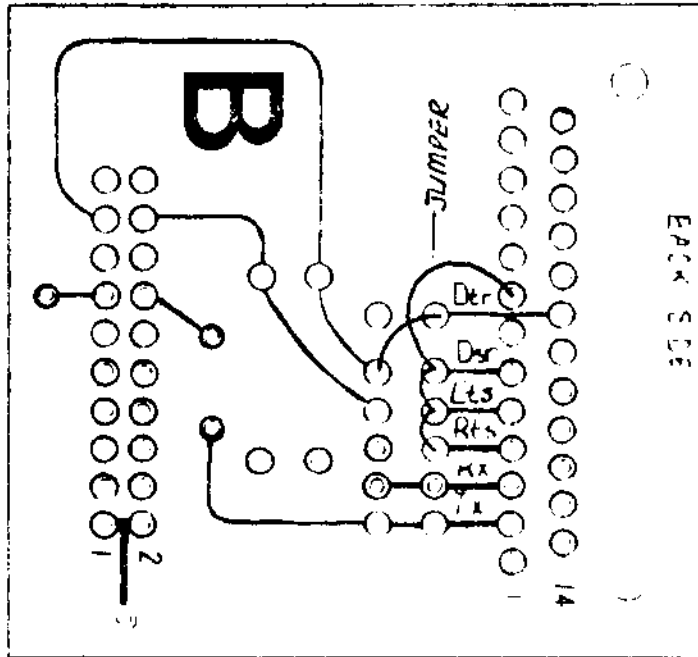


EPSON MX-80

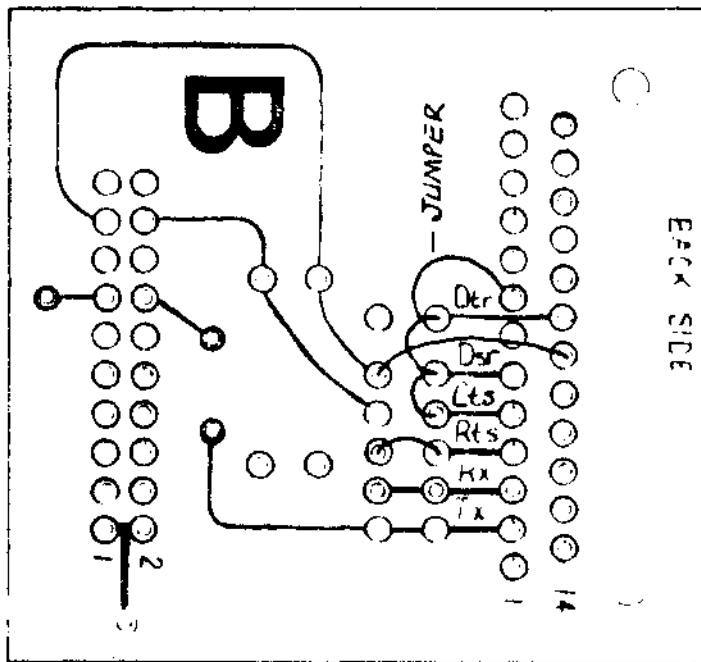


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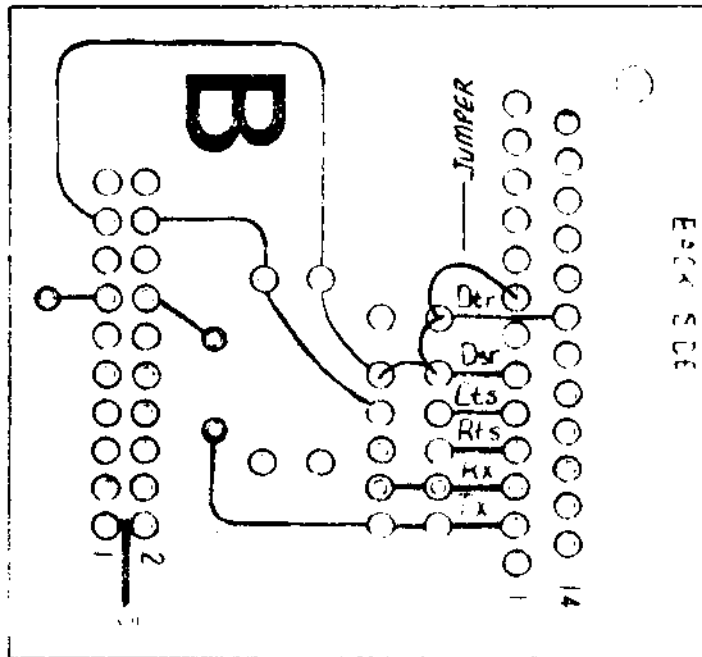
1640



NEC SPINWRITER



TI - 810



4 Port Serial board Full Warranty

Any faulty component part purchased from Tarbell Electronics, which is returned within 6 months after the date of purchase will be replaced at no charge. Components returned under this part of the warranty should be with a letter explaining what is wrong with the part.

Any factory-assembled 4 Port Serial board which does not work correctly, and is returned within 6 months after the date of purchase, will be restored to proper operating condition or replaced without charge.

Any 4 Port Serial board not covered by the above condition will be subject to a charge commensurate with the work and parts required, but in no case will exceed \$100 without notification of the owner.

Parts can be returned directly to the address below for replacement. Complete 4 Port Serial boards should be returned to the place of purchase. If this is not possible, or if it is very inconvenient, it may be returned to the address below, with proof of purchase.

Tarbell Electronics assumes no responsibility for consequential damages to other connected equipment, or for time lost, or programs or data lost, because of board malfunction or incorrect documentation.

If you are dissatisfied with the operation of a factory-assembled Tarbell 4 Port Serial board for any reason, your money will be cheerfully refunded, provided the unit is returned within the six month warranty period.

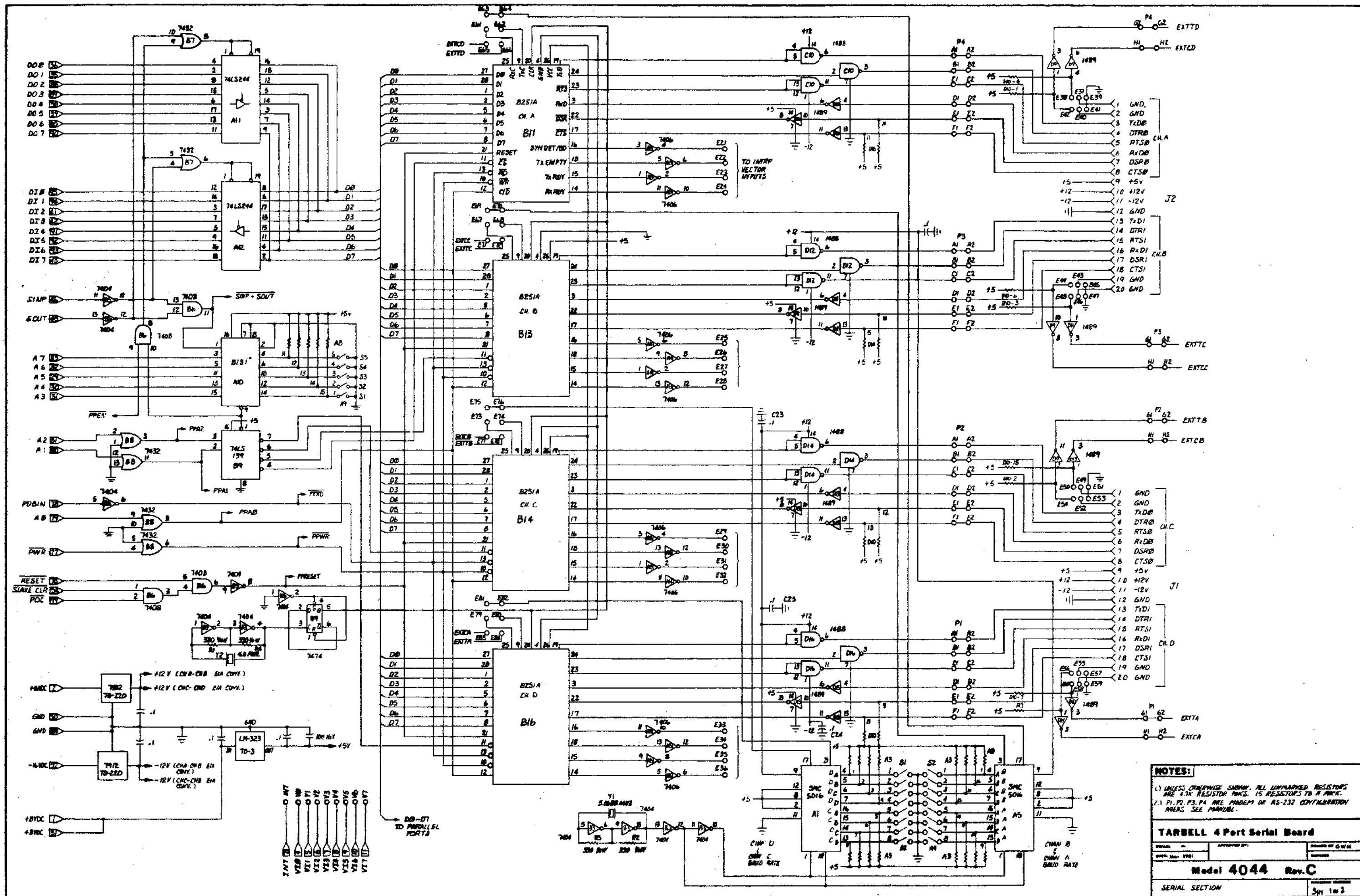
Tarbell Electronics does not warrant that the 4 Port Serial board will work with all "S-100" computer systems. Call the factory or ask your local dealer about any possible conflicts in your system.

This warranty does not cover parts, or 4 Port Serial boards built from parts, which are not traceable to Tarbell Electronics.

A 4 Port Serial board which is assembled from a kit by a Tarbell dealer has only the parts covered by this warranty, not the labor. All interfaces which were sold as kits, will have a "K" marked on the solder side. The dealer may provide his own warranty in this case.

Defective parts or interfaces covered under this warranty should be sent WITH PROOF OF PURCHASE (like a receipt) to:

Tarbell Electronics
950 Dovlen Place, Suite B
Carson, California 90746



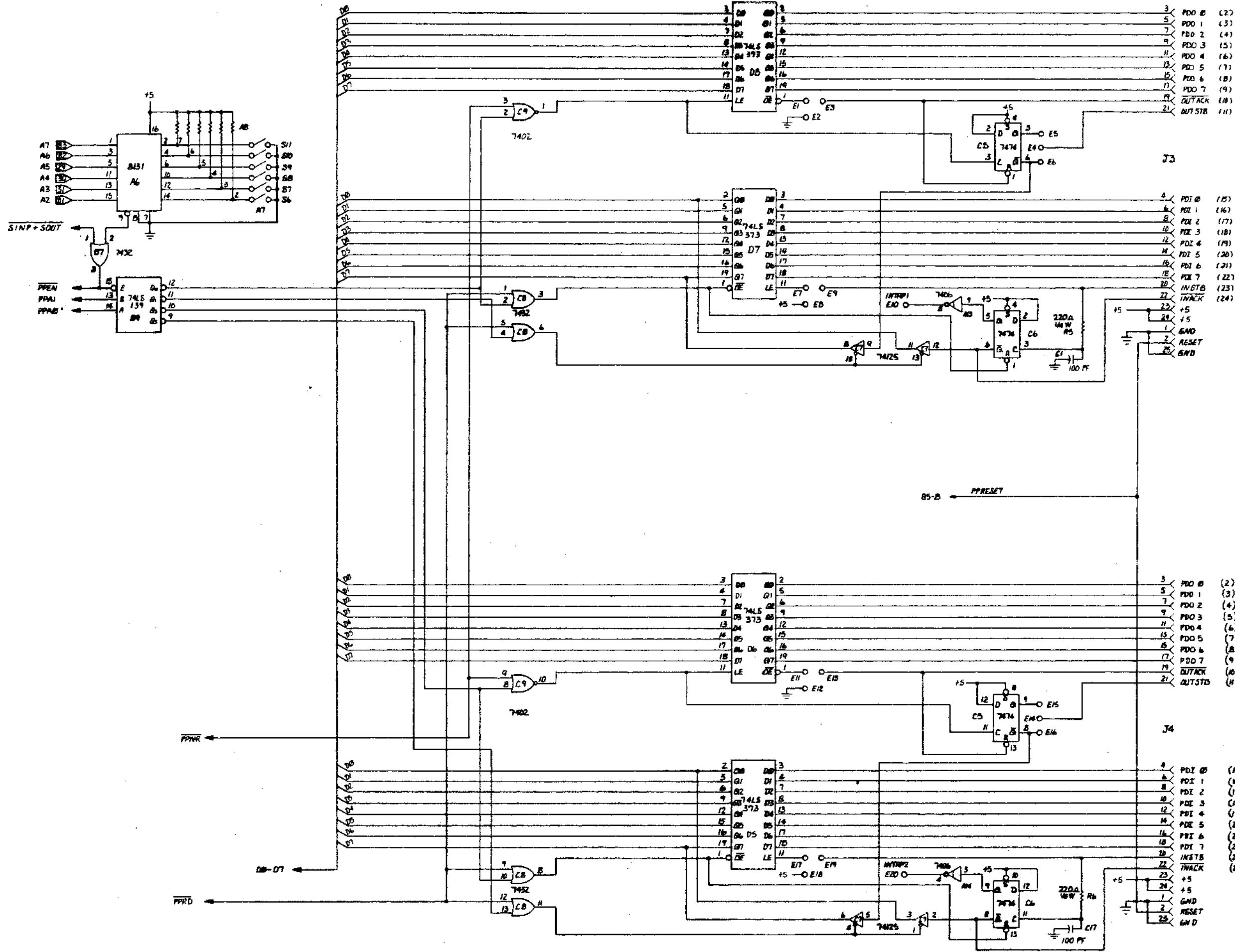
NOTES:

- UNLESS OTHERWISE SHOWN, ALL UNMARKED RESISTORS ARE 1/4W RESISTOR PKGS. 1% RESISTORS TO A PREC.
- P1, P2, P3, P4 ARE MADE UP OF RS-232 COMBINATIONS AREAS. SEE MANUAL.

TARBELL 4 Port Serial Board

Model 4044 Rev. C

SERIAL SECTION



6-7-R2	PARALLEL PORT SECTION
	MODEL 4044 REV C
	MODEL 4044 REV C SAT 2-2