TARBELL

DOUBLE DENSITY FLOPPY DISK INTERFACE

owner's manual

Tarbell Electronics

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TARBELL DOUBLE DENSITY NEWSLETTER July 23, 1981

DFORMAT problem (7-23-80 version):
The inter-record gaps are a little bit long, so if the drive is running fast when formatting, the last byte on the track may run into the first. Symptom snows under DTEST, as track 0 OK, track 1 sector 51 bad, tract 2 and all further tracks with sector 48 (last phsical track) bad. This may easily be corrected by a one-byte mod to the DFORMAT program. In the assembly-language, at PUTZERO:, should be MVI B,9 instead or B,10. The problem will not be evident if your drive is running correct or slow.

DEBLOCK BIOS AVAILABLE
This bios is set up to work with a mix of disks, single or double density, 128-byte or 512-byte sectors, single or double-sided. The 512-byte sectors provide more space on the disk: 600 kilobytes per side instead or 500. In most applications, the system will run a little faster. There are two main disadvantages: 1) the blocking/deblocking routines and buffers take up space in the bios, so you have 1k less of memory available; 2) For systems doing a lot of random-access writing, the sector must be read into memory, then modified with the 128-byte CP/M sector, then written back out to disk. This requires 2 revolutions of the disk for one sector write, whereas with the normal bios, several random sectors could be written in one revolution.

This situation is true for any CP/M system that uses sectors larger than 128 bytes, and could slow the system considerably if many random writes are being done. For random reads, it should be about the same speed. If you want this system, order the DEBLOCK BIOS for $25. The disk includes new routines to format, test, and sysgen, in addition to the BIOS and BOOT.

PUBLIC DOMAIN DISK #2
This always contains the latest standard support software for the double-density interface. It includes the bios, boot, format, and test programs, and costs $15. The current date on this disk is 6-30-81.

FORMAT problem.
Symptom is a message: "...Check for write protected disk." Correct by changing line after DONE: in assembly language source from ANI 0FFH to ANI 0C1H.

CROMEMCO ZPU rev e & f users:
Symptom: difficulty in booting. Correct by removing leg or U47 pin 12 on our board, and reducing or removing C17.

If you are having any problems, be sure to let us know. Happy customers sell more interfaces!

NEW PRODUCTS
We have been delivering CPU/IO boards since December, 1980, and people seem very happy with them. See the enclosed data sheet for more info. Our EMPIRE series computers, based on this CPU, also is selling well. Our next board will be a 4-serial/2-parallel I/O port board. We expect to start shipping this fall, as it is now in the layout stage. We are still in the process or evaluating different hard disk systems. Any ideas or suggestions would be appreciated. We are now selling the complete line or fine MICROPRO software, including WORDSTAR and WORDMASTER.

TARBELL DOUBLE DENSITY FLOPPY DISK INTERFACE TECHNICAL BULLETIN

August 11, 1980

We have found the source of a problem which has haunted some of our double density customers from time to time. The symptom is that while doing large transfers, such as a PIP *.* with verify, the routine would report a verify error, yet there was no error reported from the BIOS. Other times, the system would just lock up, with no message at all. If you don't have one of these symptoms, you probably don't have this problem, so you may choose to ignore this part of the bulletin.

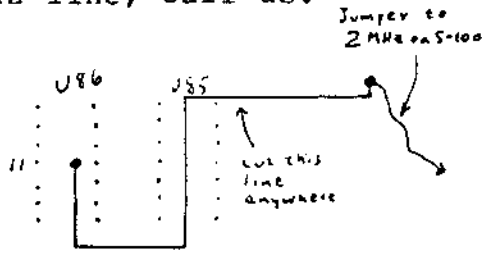
We determined that the fault was with the way that the 8257 DMA IC samples the HLDA (hold acknowledge) line. Since the clock for the 8257 is generated on-board, and is asynchronous with the 8080 or Z80 system clock, the HLDA line may be sampled during it's transition. If this happens, one circuit in the 8257 may think that the HLDA line is true, while another circuit in it may think that it's false. This can cause the 8257 to go into an undefined state.

Since the problem is caused by sampling during a transition, there are several factors which determine whether and how often it will show. One is the rise-time of the PHLDA signal on the bus, the longer the worse. This may be affected by position of the interface on the bus relative to the CPU (the closer the better), and whether or not the bus is terminated (unterminated busses usually have faster rise-times). Another factor is the manufacturer of the 8257. Tarbell has used 8257's from three manuafacturers: AMD's always have the problem, NEC's have it sometimes, and Intel's have it the least.

This fix works by using a clock signal from the bus which is syncronous with the PHLDA line to run the 8257 instead of the on-board clock.

1. Determine if you have a 2 Mhz clock signal on pin 49 of the S-100 bus. This is the frequency that is specified by the IEEE standard, but older CPU's, especially some Z-80 ones, may have some other frequency, such as 4 Mhz, on this line. This may be determined by consulting the manual or the manufacturer of your CPU board, or by measuring it with an oscilloscope or frequency counter. It is also very important that the line chosen be syncronous with the CPU, that is, derived from the same clock that is used by the CPU IC. This is NOT a requirement of the IEEE standard, so some CPU boards, especially those using the 8085, 8088, or 8086 processors may not have a syncronized 2 Mhz signal available. Pin 24 may also be a good source for 2 Mhz. The IEEE standard DOES specify this line to be syncronized with the CPU, but does NOT specify that it is to be 2 Mhz. If you can't find a syncronized 2 Mhz line, call us.

2. After you have found a 2 Mhz syncronized clock on the S-100 bus, cut the line from pin 11 of U86 (7493) on the solder side of the board as shown. Then connect a jumper from the hole to the selected S-100 2 Mhz pin.



(over)

To all revision D board owners:

You may have a cut missing from the modifications that brought your board up to revision E. Check to the right of U41. There should be a cut on each of three traces there. If there are only two, cut the trace between those two that are cut.

A note about the MWRITE line:

The MWRITE option available on our board is only for those computers where the MWRITE is not generated directly from the bus signals PWR and SOUT (as the S-100 standard specifies). It is not intended as a substitute for the normal MWRITE line, which must be implemented somewhere on the bus (usually on the CPU or front panel).

A note on dynamic memory boards:

Since we started business in 1976, we have been warning people to avoid using dynamic memory boards, and to use static boards instead. Although the new dynamic IC's seem to be more reliable, they still have a higher susceptibility to alpha particles, causing more soft errors. They are almost always cheaper and operate cooler. However, they are harder to troubleshoot, and have a MUCH higher probability of not being compatible with other boards, such as floppy disk interfaces.

To memory-bank switching customers using extended address lines:

If you are using the extended address register on our interface, it is important to initialize this register before any DMA transfers take place, preferably at the beginning of our coldstart loader (DBOOT). An example: XRA A OUT FD which would set it to zero.

To our double-sided customers:

We now have support for double-sided drives in the BIOS's for both CP/M 1.4 and 2.2, and in our DFORMAT program. We have also recently been testing the double-density interface with the PerSci 299B double density double-sided dual floppy disk drive. It has been working very well! Much better than the earlier models. If you are interested in the set-up for any of the PerSci drives, call or write us.

Notes on using different sector lengths:

Several customers have asked about using different sector lengths with their Tarbell interface. Although we do not yet have support for this in our standard BIOS, some of our customers have worked it out. We can offer one in particular, which uses 512 byte sectors, as is, for a ten dollar copying/handling/diskette charge. "As is" means minimally supported, since we don't have much experience with it yet. Also note that this version was written for the Z80, so customers with 8080 CPU's will not be able to use it. Using the larger sector lengths give two advantages: more disk storage, and faster operation. There are also two disadvantages: uses more main memory (for the buffer and blocking/deblocking routines), and the disks will not be compatible with those generated by our other BIOS's.

Persci 299 Jumpers 8-13-80

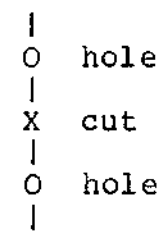
The Double density interface has provisions on the 50 pin drive connector at the top to allow the connector to modified for small differances between drive manufactures. In particular, Persci drives.

You will notice that each connection has a double feed through hole with a short etch line connecting each end. By cutting this line with a sharp ex-acto blade, the line may may be be broken open. To allow the persci 299 to work with our interface, some of these lines must be cut, and jumpers put on for the differences between Shugart and Persci. Below is a list of cuts and jumpers to make to this connector.

CUTS

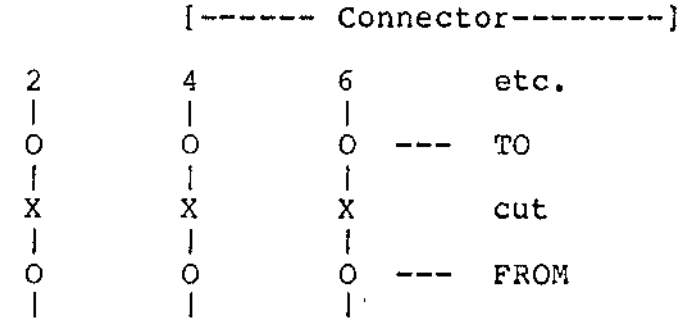
(revision C to revision F only)

Back side of board, cut trace connecting pin 2 and pin 16 of 50 pin connector.
Front side of board, cut the following lines between feed-through holes:



Cut 2,4,6,8,12,14,16,18,24,30,32 as shown above.

Jumpers are referenced as being placed in a FROM - TO fashion as shown below.



Jumpers to install:

FROM	TO
14	2
32	4
18	16
30	18

Engineering Change Notice for Double Density Interface
Date 8-8-80

This interface requires that you have a 2 MHz clock on pin 49 of the S-100 bus in order for it to work correctly. If you have 4 MHz on this pin, you will have to divide it by 2 in order to comply with the IEEE spec which says it must be a 2 MHz clock on this line. Our interface uses this line (49) to correct a problem we have found which occurs during a DMA cycle.

If you have any problems, please feel free to call us.

G.W.Mulchin
G.W. Mulchin
Engineering

DD-ASM REV.F
SN 185
R 10/14/80

Tarbell Double Density Floppy Disk Interface

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INTRODUCTION TO THE TARBELL DOUBLE DENSITY FLOPPY DISK INTERFACE

The Tarbell Double Density Interface is an IBM soft sector floppy disk interface using the Western Digital 1791/1793 Floppy Disk controller chip and built to the IEEE S-100 Standard.

This interface is very similar to the now popular Tarbell Single Density Interface in function, but with many added new features.

These features include operation as either single or double density, or both, direct memory access (DMA), and extended memory addressing capability, with processor speeds of either 2 or 4 Mhz. The on-board BOOTSTRAP feature allows full system memory of 64K by using the PHANTHOM line on the bus.

Software available to run the double density controller is the widely used CP/M(R) disk operating system, and the new MP/M multi-tasking operating system. Both operating systems use an enhanced I/O system utilizing the new direct memory access capability, and automatic density select features that this product offers.

The capacity of the Disk Operating System running under CP/M in Double Density will be 476 Kbytes for an empty disk, or 243 Kbytes Single Density for an empty disk. The break down is as follows:

Double Density:

The disk will appear to CP/M as 77 tracks of 51 sectors, each sector containing 128 bytes. Because the first two tracks are used by CP/M for the operating system, there will only be 75 tracks available for Directory and data storage. This total space then equals approx. 476 Kbytes.

Single Density:

While running Single Density, the disk will appear to CP/M as 77 tracks of 26 sectors, each containing 128 bytes. The first two tracks are used for the CP/M operating system, leaving 75 tracks available for Directory and data storage, about 243 Kbytes of disk space.

It should be noted that the capacities listed above are realized as a result of using the CP/M operating system. If this operating system were not used, then the disk could hold more data, because the disk may be formatted with sectors of 256,512,1024 bytes in length. For further information about this, consult the 1791/1793 data sheet for sector lengths that may be used.

Note: CP/M and MP/M are trademark and tradenames of Digital Reaserch Post Office Box 579, Pacific Grove, California 93950.

SECTION 2: GETTING CP/M RUNNING WITH THE INTERFACE

One of the major problems confronting the implementers of new micro-computer systems, has been the lack of input/output (I/O) standards. The emergence of Digital Research's CP/M(r) disk operating system as a standard I/O environment has contributed greatly to aleviating this problem. Now the problem is reduced to implementing CP/M on the target hardware system, which consists of tailoring the BIOS part of CP/M to the situation. Unfortunately, since we can't assume any particular console interface at the factory, there is no way to make the system generation completely automatic.

Because of all the different possible system configurations, and because we try to update our hardware and software as quickly as possible, it has been difficult to create and maintain a set of documentation that is useful and correct for getting our double-density floppy disk interface working under CP/M. These instructions represent a major rewrite effort in this direction. We hope that most of the faults in the earlier instructions have been corrected in this set.

These instructions explain how to get the Tarbell Double Density Floppy Disk Interface going with Digital Research's CP/M 1.4 or 2.x disk operating system. It is important not to try and make more than one change in your system at a time. For example, if you wish to go from our single density interface operating under CP/M 1.4, to our double density interface operating DMA under CP/M 2.2 with a different memory size, DON'T try to do it all at once. First the single-density to double density, then to DMA, then to 2.2, then to different memory size.

Be sure that the title of the instructions you are going to use, matches the situation you have. If it doesn't, and you can't seem to find one that does match, call or write to us, and we'll try to help. If you don't think you are capable of carrying out the required instructions yourself, we can generate a customized system for you. Just have us send you an I/O tailoring questionaire. The cost is usually about $50.

INSTALLATION NOTES

1. If you have a revision D board (revision letter is at bottom of board), and the board has been modified according to earlier addendums, make a cut on the trace to the right of U41, which is the second trace down. The traces above and below this trace should already be cut.

2. The MWRITE option available on our board is only for those computers where the MWRITE is not generated directly from the bus signals PWR and SOUT. It is not intended as a substitute for the normal MWRITE line, which must be implemented somewhere on the bus (usually on the CPU or front panel).

3. Install the double density board as close to the CPU as possible, between the CPU and memory board(s).

INSTRUCTIONS FOR GETTING THE TARBELL DOUBLE DENSITY INTERFACE OPERATING WITH CP/M 1.4 WHEN YOU HAVE CP/M 1.4 ALREADY GOING ON A TARBELL SINGLE-DENSITY INTERFACE

1. First make sure that your situation matches the title above. If it doesn't, find another sheet that does match.

2. Check the option jumpers on your double-density interface board against the manual to make sure the board is addressed for E0 through F8 (hex), and that all other options are correct.

Use your current single-density interface, operating under CP/M 1.4 to do the following steps:

3. Use the FORMAT91 program on the public domain #2 disk (provided with the interface) to format at least two disks. DON'T use any of your old format programs to do this. When it says "READY TO FORMAT?" be SURE to get the public domain disk out of there before typing Y. Test the disks using the DISKTEST program.

4. Put one of the newly formatted disks in drive B. Put a disk with your normal CP/M 1.4 system and system programs in drive A. Now perform the following steps:

a) logged into drive A, type SYSGEN. Answer source as drive A, destination as drive B. Reboot.
b) type PIP with no arguments, then the following steps.
```
*B:=A:DDT.COM
*B:=A:ASM.COM
*B:=A:SYSGEN.COM
*B:=A:ED.COM
```
c) while still in PIP program, remove your system diskette from drive A, and insert into drive A the Public Domain #2 diskette that came with the double-density interface. Then continue as shown below:
```
*B:=A:ABIOS24.ASM
*B:=A:DBOOT24.ASM
```

5. Now take out the public domain disk #2 and put it aside. Take the newly formatted disk out of drive B and put it into drive A. Boot up on it. It should come up normally, since a copy of your system was just put onto it.

6. Using ED.COM, edit the ABIOS24.ASM to change the EQU's for your memory size, console, printer, drives, etc. Leave the DMACNTL and DUBSID EQU's set to FALSE. Set the MSIZE EQU to the same size as the CP/M 1.4 system you are now running on this disk. Be sure to set the console port numbers correctly. Exit from the editor. Rename the file to ABIOSxx.ASM, where xx is your MSIZE.

8. Assemble ABIOSxx with ASM.COM. Print the .PRN file if desired, then erase it.

9. Using ED.COM, edit DBOOT24.ASM. Set the MSIZE EQU to the

size used above. Leave the DOUBSID, DOUBDEN, and DMACNTL EQU's set to FALSE. Exit from the editor. Rename the file to DBOOTxx.ASM.

10. Assemble DBOOTxx.ASM with ASM.COM. Print the .PRN file if desired, then erase it.

11. Use SYSGEN to put a copy of your current CP/M 1.4 system onto the disk as a file. When it asks for source, answer A. When it asks for destination, press carriage-return to reboot. Then do a SAVE 32 CPMxx.COM, where xx is your system size.

12. Use DDT to bring in the CPMxx.COM file and to overlay the BIOS and BOOT hex files onto it. Type DDT CPMxx.COM . Then type IABIOSxx.HEX . Then type Rbias where bias is in the table below:

xx	bias	xx	bias	xx	bias	xx	bias
20	D480	24	C480	28	B480	32	A480
36	9480	40	8480	44	7480	48	6480
52	5480	56	4480	60	3480	64	2480

Now type IDBOOTxx.HEX . Then type R900 . Then do Ctl-C.

13. Next enter SYSGEN. When it asks for source, press return to skip. When it asks for destination, type A. At this point you may write this system onto more than one disk. After you are finished writing onto the disk(s), DON'T press return to reboot.

14. You can now shut off your computer, remove the single density interface, and put the double-density interface in. Then turn your computer back on.

15. The system you have just written onto one or more disks should now boot up correctly on the double-density interface. If it doesn't, check over the BIOS and BOOT .PRN files to make sure all EQU's were set correctly. Check your board to verify again that all the jumper options are right. If you still can't get it going, read section 2-3 of these instructions.

16. If the system does come up correctly, congratulations! You are now running the double-density interface in non-DMA mode. If you want to operate double-density next, see section 2-2 of these instructions. If you want to try operating in DMA mode, go to step 6 in this section, changing the DMACNTL EQU to TRUE in both the BIOS and the BOOT .ASM files. The rest of the instructions are the same.

17. Finally, if you notice any errors in this documentation, PLEASE call or write about it.

HOW TO MAKE THE TARBELL DOUBLE DENSITY INTERFACE OPERATE IN THE DOUBLE DENSITY MODE ASSUMING YOU HAVE THE DOUBLE DENSITY INTERFACE OPERATING IN THE SINGLE DENSITY MODE.

1. Check your situation against the title above. If it doesn't match, look for other instructions that do. In order to operate in double density mode, you will either need to be operating at 4 or above 4 Mhz (Z80 or 8085), or you need to be operating in DMA mode. To set DMA mode, see step 16 of the instructions in section 2-1.

2. Format some disks double density with DFORMAT, and test them using DTEST.

3. If you boot up on a single density system which was created using the auto-select I/O section (ABIOS or 2ABIOS), all you have to do is put the formatted double-density diskette in drive B. Files may be transferred to the new double density disk using PIP. Don't try to use the COPY utility to copy from single density to double density or vise-versa.

4. If you want to put a system from the first two tracks on the single density disk onto a double density disk, SYSGEN alone will not work. This is because the first sector of the first track contains a byte which has to be DD (hex) for double density, and your single-density disk doesn't have that byte. To perform this operation correctly, follow these steps:

a) On your single density disk, edit the file called DBOOTxx.ASM to change the DOUBDEN EQU from FALSE to TRUE. It is important that the MSIZE match your current CP/M system size (xx).
b) Assemble the new file: ASM DBOOTxx
c) Do a SYSGEN, answering source on A, skip the destination and reboot. Enter SAVE 34 CPMxx.COM where xx is system size.
d) Then overlay the CPMxx.COM system image with the new DBOOT:
```
DDT CPMxx.COM
IDBOOTxx.HEX
R900
```
e) Then press control-C to return to CP/M.
f) Then do another SYSGEN, this time skipping the source, and answering B to the destination. (This assumes you still have your double-density disk in B.)

5. Now you can take the double density disk out of drive B and put it into drive A and boot up on it.

WHAT TO DO IF YOUR TARBELL DOUBLE DENSITY FLOPPY INTERFACE IS NOT WORKING

1. Recheck the jumper options on the interface board against your manual in section 6. Note that manuals of boards rev B and earlier have an error in the board addressing section. People with these manuals can get a new manual free by sending us the cover of their old manual.

2. Recheck the EQU's in the BIOS and BOOT .ASM files to make sure that all are set correctly.

3. If you have a friend with a working Tarbell Double Interface, try using your interface in his computer. If his works and yours doesn't, there is probably something actually wrong with your interface. If so, you might want to consider sending it back to Tarbell for repair. If your interface does work in your friend's computer, the problem might be in your software, or in some other component of your system. Just because the other components of your system work under other circumstances, doesn't mean that there is nothing wrong with them.

4. Another thing to check is the diskette that you're using. Is it formatted correctly? How do you know it is?

5. Do you have dynamic memory in your computer. If so, how is it refreshed? It is possible that the way it is refreshed interferes with our interface, or that the way our interface works interferes with the memory's refresh circuitry.

6. Does your CPU board fully implement the new IEEE S-100 standard? In particular, does it use pin 67 (the phantom line) for anything besides phantom? Does it implement the control-disable, data-disable, and status-disable lines? Does it implement the PSYNC, PHOLD, and PHLDA lines? Neither the SDS SBC-100 or SBC-200 CPU boards meet this requirement.

7. Does the memory which occupies address 0000 in your system have a phantom line on pin 67?

8. Do you have other boards in your system that use the XRDY and PRDY lines (pins 3 and 72) besides the Tarbell interface and the CPU? If so, it might be best to disconnect those lines completely.

9. Since the Tarbell Double Density Floppy Disk Interface uses lines on your motherboard that aren't normally used, some of these lines could be shorted or open, or the connector pins could be dirty.

10. Check your system power supply, with a scope if possible, to make sure that all your voltages are steady, clean, and the right level, both on the drives and the motherboard. It is very important that on the drive power supply, the 24 volt, 5 volt, and -5 volt returns be connected together at the power supply end.

11. If you are having problems with the bootstrap, it's possible that C17 is not a high enough value to reduce the effects of ringing on the bus. You might try 220, 390, 470, or 680 pf capacitors, in that order. The symptom is that the bootstrap flip-flop gets reset before it has a chance to read a complete sector. This can be seen by looking at pin 19 on the 8257. This DRQ line should be a series of short pulses that should happen over a period of about 2 ms. If they don't last that long, you may have this problem.

12. If the DRQ line mentioned above never goes high at all, that means the interface is never receiving a valid data byte. This could be caused by a variety of factors, including a bad data separator component, bad 1793, bad drive, etc.

13. If the interface is picking up excessive errors after warming up, it could be the 1793. We are now testing these IC's more carefully.

*** NOTE ***

If you decide to send the interface back for repair, be sure to include a copy of your receipt, showing the date you bought it. Note that only the parts are warrantied on kits.

INSTRUCTIONS FOR GETTING THE TARBELL DOUBLE DENSITY INTERFACE OPERATING WITH CP/M 2.x WHEN YOU HAVE CP/M 2.x ALREADY GOING ON A TARBELL SINGLE-DENSITY INTERFACE

1. First make sure that your situation matches the title above. If it doesn't, find another sheet that does match.

2. Check the option jumpers on your double-density interface board against the manual to make sure the board is addressed for E0 through F8 (hex), and that all other options are correct.

Use your current single density interface, operating under CP/M 2.x to do the following steps:

3. Use the FORMAT91 program on the public domain #2 disk (provided with the interface) to format at least two disks. DON'T use any of your old format programs to do this. When it says "READY TO FORMAT?" be SURE to get the public domain disk out of there before typing Y. Test the disks using the DISKTEST program.

4. Put one of the newly formatted disks in drive B. Put a disk with your normal CP/M 2.x system and system programs in drive A. Now perform the following steps:

a) logged into drive A, type SYSGEN. Answer source as drive A, destination as drive B. Reboot.
b) type PIP with no arguments, then the following steps.
```
*B:=A:CPM.COM
*B:=A:DDT.COM
*B:=A:ASM.COM
*B:=A:SYSGEN.COM
*B:=A:ED.COM
```
c) while still in the PIP program, remove your system diskette from drive A, then insert into drive A the Public Domain #2 diskette that came with the double-density interface. Then continue as shown below:
```
*B:=A:2ABIOS24.ASM
*B:=A:2DBOOT24.ASM
```

5. Now take out the public domain disk #2 and put it aside. Take the newly formatted disk out of drive B and put it into drive A. Boot up on it. It should come up normally, since a copy of your system was just put onto it.

6. Using ED.COM, edit the 2ABIOS24.ASM to change the EQU's for your memory size, console, printer, drives, etc. Leave the DMACNTL and DUBSID EQU's set to FALSE. Set the MSIZE EQU to the same size as the CP/M 2.x system you are now running on this disk. Be sure to set the console port numbers correctly. If you have Shugart 800 drives, don't set the step rate any faster than 10 ms. Exit from the editor. Rename the file to 2ABIOSxx.ASM, where xx is your MSIZE.

8. Assemble 2ABIOSxx with ASM.COM. Print the .PRN file if desired, then erase it.

9. Using ED.COM, edit 2DBOOT24.ASM. Set the MSIZE EQU to the size used above. Leave the DOUBSID, DOUBDEN, and DMACNTL EQU's set to FALSE. Exit from the editor. Rename the file to 2DBOOTxx.ASM.

10. Assemble 2DBOOTxx.ASM with ASM.COM. Print the .PRN file if desired, then erase it.

11. Use SYSGEN to put a copy of your current CP/M 2.x system onto the disk as a file. When it asks for source, answer A. When it asks for destination, press carriage-return to reboot. Then do a SAVE 34 CPMxx.COM, where xx is your system size.

12. Use DDT to bring in the CPMxx.COM file and to overlay the BIOS and BOOT hex files onto it. Type DDT CPMxx.COM . Then type I2ABIOSxx.HEX . Then type Rbias where xx is MSIZE and bias is in the table below:

xx	bias	xx	bias	xx	bias	xx	bias
20	D580	24	C580	28	B580	32	A580
36	9580	40	8580	44	7580	48	6580
52	5580	56	4580	60	3580	64	2580

Now type I2DBOOTxx.HEX . Then type R900 . Then do Ctl-C.

13. Next enter SYSGEN. When it asks for source, press return to skip. When it asks for destination, type A. At this point you may write this system onto more than one disk. After you are finished writing onto the disk(s), DON'T press return to reboot.

14. You can now shut off your computer, remove the single-density interface, and put the double-density interface in. Then turn your computer back on.

15. The system you have just written onto one or more disks should now boot up correctly on the double-density interface. If it doesn't, check over the BIOS and BOOT .PRN files to make sure all EQU's were set correctly. Check your board to verify again that all the jumper options are right. If you still can't get it going, read section 2-3 of these instructions.

16. If the system does come up correctly, congratulations! You are now running the double-density interface in non-DMA mode. If you want to operate double-density next, see section 2-2 of these instructions. If you want to try operating in DMA mode, go to step 6 in this section, changing the DMACNTL EQU to TRUE in both the BIOS and the BOOT .ASM files. The rest of the instructions are the same.

17. Finally, if you notice any errors in this documentation, PLEASE call or write about it.

GETTING THE TARBELL VERSION OF CP/M 1.4 OR 2.X RUNNING ON YOUR TARBELL DOUBLE-DENSITY FLOPPY DISK INTERFACE WITHOUT A CURRENTLY RUNNING CP/M SYSTEM OF ANY KIND

1. First make sure that your situation matches the title above. If not, you may find that another set of instructions will get your system going sooner.

2. You need to have the following hardware installed:

   a) An assembled and tested Tarbell Double Density Interface
   b) At least 24k bytes of random access memory, of which at least the first 32 bytes can be disabled by phantom line pin 67 going low.
   c) A Z-80, 8085, or 8080 CPU board which conforms to the IEEE S-100 standard.
   d) A console interface of some type, preferably not memory-mapped video, which supports an alphanumeric keyboard and a CRT display or teleprinter. If possible, this interface should be addressed for status on port 0, data on port 1, with bit 0 of the status low meaning keyboard ready, and with bit 7 of the status low meaning CRT display ready. If these port and status requirements are met, the Tarbell CP/M 1.4 or 2.x disks for the DD controller should boot up with no further work. Just put the disk in, push reset, and run. Skip to step 8 if so. If not, you will need to fulfill the requirements of substep (e) below and continue.
   e) Either a front panel or a ROM monitor (any ROM should be outside the 24k RAM), which allows depositing bytes into specified RAM addresses and executing at an address.

3. If possible, have a friend make a copy of your original CP/M disk, and don't use it except to make further copies. Then use the copy for the following steps.

4. Turn the computer on, then the CRT-keyboard, then the drive power.

5. Put the CP/M disk into the disk drive (on most drives, the label on the disk should face the door of the drive). Close the door. Push reset (and run if you have one) buttons on the computer.

6. The head should load against the disk and move in one track. If it doesn't do this, something is wrong with the hardware setup, and you should try a few times more. If it still doesn't do it, FIRST remove the diskette, then shut down the system. Something is either wrong with the hardware or the diskette. If so, have someone look at it or call Tarbell. If it does load and step ok, go onto the next step.

7. Either stop the computer from running, if you have a front panel, or jump into your ROM monitor, if you have one.

8. Look at the BIOS (Basic Input Output System) listing that

came with our CP/M. Find the label BOOT. After the LXI SP instruction, you will see a series of NOP's. This area is reserved for initializing console interfaces that require it. Using either front panel or ROM, deposit the initialization routine required, if any, at the address indicated by the listing. There should be a copy of any required initialization routine in the manual on your console interface. Assembly language code for the initialization of some common console interfaces can be seen in the following lines on the page.

9. Still looking at the BIOS listing, find the label CONST. Examine the code there for our "standard" interface. Put the code here to do a status check on your console interface. Notice that if your status bits are true when high, instead of low like ours, you will need to change the RNZ to an RZ. Other changes which might be required are the port number after the IN, and the mask after the ANI. Check your console interface manual for examples and instructions.

10. The next routine is labeled CONIN. Deposit the code to read a byte from your console keyboard into register A. Notice that you might need to make similar changes, such as JNZ to JZ, mask, and port numbers.

11. The last routine to change is labeled CONOT. Deposit the code to write the byte in register C to your console. Again, you might need to replace our JNZ with a JZ and make port number and mask changes. Be sure to end each of these routines with an RET instruction.

12. This should be all the patches you need to make to the CP/M system residing in memory, to get going temporarily. Now examine the content of address 5A00 (hex), which should be a C3 (hex for JMP) and execute (run) at that location.

13. Our BIOS should give you an opening message. If so, you're on the air, so go to step 14. If not, the system may not have loaded properly, and something may be wrong with the diskette or hardware setup. In that case, refer to section 2-3.

14. If you haven't already done so, copy the system and files onto another disk. In order to do this, keep your system disk in drive A and put a blank disk into drive B. Then type: COPY ALL. This will copy your original disk onto the blank disk. Note that the system you are running is only in memory, and the system on the disk hasn't yet been modified. Leave the new disk in drive B until you press return to reboot. Then take the original disk out of drive A and never use it again except to copy it. Now remove the copy you made from drive B and label it exactly the same as the original. You will find that it is important to keep the disk labels current, as it is easy to get confused and make a mistake. Put the new copy into drive A for further work. Then press Ctl-C.

15. The next thing to do is edit the BIOS and BOOT .ASM files and overlay them onto your system. Use the method described in the

Tarbell CP/M 1.4 or 2.x User's Guide, as this will properly document all your changes and allow you to make use of memory larger than 24k.

16. The latest ABIOS (Auto-density select Basic Input Output System) is always available from Tarbell for $15. Just ask for Public Domain Disk # 2.

CONTENTS OF PUBLIC DOMAIN DISK #2 May 2, 1980

This is a disk which is regularly updated with our latest ABIOS and 2ABIOS for the Tarbell Double Density Floppy Disk Interface. Other utilities are also maintained on this disk, such as format and test routines. We also had room to include the source for the FORTH language from the Forth Interest Group. Their name and address are included on the .ASM file. Following is a short description of each file. For further information, see the comments in the file itself, or the Tarbell CP/M User's Guide. The latest version of this disk is always available within 1 week from Tarbell for $15. If you are having problems, it's always wise to see if there is a newer version of this disk available than the one you have.

1. DBOOT24.ASM

THIS IS THE SAME AS THE NORMAL SBOOT PROGRAM USED IN SINGLE DENSITY, WITH THE EXCEPTION OF A DENSITY CONDITIONAL STATEMENT. AT THE PRESENT TIME SETTING THIS EQU TO EITHER TRUE OR FALSE WILL MAKE NO DIFFERENCE TO THE BOOTING OPERATION. THE REASON IT IS THERE IS FOR DOING AUTO-DENSITY SELECTION DURING BOOTING.

2. DDUMP.ASM & DDUMP.COM

THIS IS A MODIFIED DUMP.COM FROM SAM SINGER AND FROM THE CP/M USERS GROUP. THIS PROGRAM WILL ALLOW YOU TO VIEW ONLY TRACKS 2 - 76 OF A DOUBLE DENSITY DISK. THE ONLY LIMITATION IN THE PROGRAM IS THAT IT WILL NOT DUMP BY GROUP NUMBERS. ALL OTHER FEATURES ARE USEABLE.

3. DFORMAT.ASM & DFORMAT.COM

THIS PROGRAM IS THE DOUBLE DENSITY FORMAT PROGRAM. IT WILL FORMAT THE DISK IN MANY WAYS DEPENDING ON WHICH EQU'S YOU SET TRUE OR FALSE.

For example:

SETTING TRK1SD = TRUE,
FORMATS TRACK 0 AND 1 SINGLE DENSITY.
TRACK 2 - 76 DOUBLE DENSITY.

OR

SETTING TRK1DD = TRUE,
FORMATS TRACK 0 IN SINGLE DENSITY.
TRACKS 1 - 76 DOUBLE DENSITY.

*** NOTE ***

ONLY ONE (1), TRK1SD OR TRK1DD MAY BE TRUE AT A TIME. THE SKEW FACTOR IS EASILY CHANGEABLE IN THE DFORMAT PROGRAM TO ALLOW FOR OPTIMIZING DISK SPEED.

AS SIDE SELECT IS ONLY SUPPORTED BY CHANGING YOUR DRIVE SELECT IF YOU HAVE DOUBLE SIDED, FORMATTING SIDE B WITH THE DFORMAT PROGRAM MAY OR MAY NOT WORK FOR YOU.

4. DTEST.ASM & DTEST.COM

THIS PROGRAM IS USED TO TEST A DOUBLE DENSITY DISK FOR ERRORS. WHEN THE PROGRAM FIRST COMES UP IT WILL ASK YOU FOR A "TITLE:". YOU

MAY TYPE IN ANYTHING YOU WANT SUCH AS <FORMATTED WITH 62.5 NSEC,187.5 NSEC> AND THEN A CNTL-P, CARRIAGE RET, OR IF YOU DON'T WANT TO TYPE ANYTHING, JUST TYPE A CARRIAGE RET. THE TITLE ALLOWS YOU TO KEEP A RUNNING TAB ON THE ERRORS AND USING CNTL-P WILL TURN ON THE LIST DEVICE FOR MAKING A HARDCOPY LISTING. THE NEXT QUESTION WILL BE STARTING TRACK. YOU MUST ANSWER THIS WITH A TRACK NUMBER OF 0 OR GREATER. THE REST OF THE PROGRAM SHOULD BE CLEAR. THIS PROGRAM READS A TRACK AT A TIME AND KEEPS A RUNNING TAB OF ERRORS FOUND. DURING THE READING OF THE TRACK, IF A SECTOR IS BAD IT WILL DISPLAY THE SECTOR NUMBER AND THE NUMBER OF RETRYS IT TOOK TO READ IT. IT SHOULD BE NOTED THAT IT WILL DO 11 RETRYS MAX, AND THEN GO ON TO THE NEXT SECTOR. IF IT TAKES MORE THAN 10 RETRYS, THEN YOU SHOULD REFORMAT THE DISK AND CHECK IT AGAIN, AS OUR DBIOS ONLY DOES 10 RETRYS BEFORE INDICATING A FAILURE. RETRYS ON THE ORDER OF 1 TO 5 IS TYPICAL, IF THEY OCCUR AT ALL, WITH THIS INTERFACE. THIS PROGRAM DOES NOT WRITE ON THE DISK, IT IS READ ONLY.

5. FORMAT.ASM & FORMAT.COM

IF YOU ARE USING OUR OLD SINGLE DENSITY FORMAT PROGRAM, YOU WILL NOT BE ABLE TO READ THEM ON THE NEW INTERFACE IN SINGLE DENSITY. THIS IS BECAUSE THERE IS A BYTE IN THE INNER RECORD GAPS THAT THE 1771 WILL READ BUT THE 1791/1793 WON'T. THIS FORMAT PROGRAM FIXES THAT PROBLEM FOR BOTH THE 1791/1793 AND WILL STILL ALLOW YOU TO USE IT WITH YOUR PRESENT 1771 CONTROLLER ALSO. YOU SHOULD DESTROY AND OLD COPIES OF THE OLD FORMAT PROGRAM YOU HAVE, AND USE THIS ONE FROM HERE ON OUT.

*** NOTE ***

THIS FORMATS SINGLE DENSITY ONLY, 26 SECTORS OF 128 BYTES AND ONLY RUNS ON THE NEW CONTROLLER BOARD.

6. FORMAT91.ASM & FORMAT91.COM

This program will only run on the single-density interface. It will format disks in standard IBM single-density format, to read correctly on the double density interface.

7. DFRAND.ASM

This is another format program, which only runs on the double-density interface, and which formats disks double-density in a random format. This is very useful to use in conjunction with the DTEST program, while setting up precomp. It gives a more realistic representation of the way that data may be present on the disk. Do NOT use this program to format disks that are to be used next with CP/M, as the directory needs to be filled with E5's.

8. MACRO.LIB & SKEW.LIB

THIS LIBRARY IS NECESSARY IF YOU HAVE DIGITALS MACRO ASSEMBLER AND WISH TO CHANGE AND ASSEMBLE DDUMP.ASM AND DTEST.ASM. THESE PROGRAMS USE MACROS.

9. STAT.COM (FOR CPM V1.4 ONLY)

THIS IS AN UPDATED VERSION OF THE STAT PROGRAM FOR THE ORIGINAL DISTURBUTION. IT FUNCTIONS THE SAME AS THE OLD ONE. THE ONLY IMPROVEMENT WAS TO MAKE IT DISPLAY THE CORRECT CAPACITY OF A DOUBLE DENSITY DISK. IT WILL STILL WORK SINGLE DENSITY.

10. ABIOS24.ASM

THIS IS THE AUTO-DENSITY SELECT VERSION OF THE BIOS FOR CPM V1.4. THIS BIOS WILL AUTOMATICALLY SELECT THE DENSITY OF THE DISK YOU ARE USING IN EITHER DRIVE, AND WILL ALLOW YOU TO CHANGE THE DENSITY AT ANY TIME. IF YOU ARE GOING TO CHANGE THE DENSITY OF THE "A" DRIVE, YOU MUST HAVE A DISK WITH THE SAME SYSTEM SIZE AS THE ONE YOU REMOVED. FILE TRANSFERS FROM SINGLE TO DOUBLE OR DOUBLE TO SINGLE IS COMPLETELY AUTOMATIC. YOU MUST SET DOUBDEN = TRUE IN THE DBOOT24.ASM FILE BEFORE YOU USE THE AUTO-DENSITY CAPABILITY OF ABIOS24.ASM, AS THIS IS THE ONLY WAY THE PROGRAM KNOWS IT IS LOOKING FOR A DOUBLE DENSITY DISK IN ANY DRIVE.

11. 2ABIOS24.ASM

THIS IS THE AUTO-DENSITY SELECT VERSION FOR CPM V2.x AND THE NEW INTERFACE. THIS BIOS MUST BE USED WITH 2DBOOT24.ASM TO BRING UP THE SYSTEM. PLEASE NOTE THAT 2ABIOS24 AND 2DBOOT24 ARE ONLY FOR CPM V2.x AND WILL NOT RUN ON CPM V1.4 OR CONVERSELY. THIS BIOS IS SHIPPED READY TO RUN IN THE AUTO SELECT MODE. YOU MAY CHANGE THIS AFTER YOU GET A RUNNING SYSTEM SO THAT IT WILL NOT RUN AUTO SELECT BY SETTING DOUBDEN = FALSE. YOU MAY ALSO DEFEAT THE DMA PORTION BY SETTING DMACNTL = FALSE, WHICH WILL ALLOW THE BIOS TO RUN IN PROGRAM DATA TRANSFER.

*** NOTE ***

YOU MUST SET DMACNTL = TRUE AND DOUBDEN = TRUE IF AUTO DENSITY SELECT IS NEEDED AND YOU WILL BE RUNNING DOUBLE DENSITY at 2 MHz.

12. 2DBOOT24.ASM

THIS IS THE SECONDARY COLD START LOADER FOR CPM V2.x FOR USE WITH 2ABIOS24.ASM. SEVERAL EQU'S APPEAR IN THIS LOADER. DMACNTL - SETTING THIS TRUE WILL ALLOW THE PROGRAM TO BOOT IN THE SYSTEM USING DMA CONTROL. IF FALSE, BOOTS SYSTEM UNDER PROGRAM DATA TRANSFER. DOUBDEN - SETTING THIS TRUE PUTS THE SPECIAL ID BYTE INTO THE DISK DURING GENERATION OF A DOUBLE DENSITY SYSTEM DISK THAT WILL BE BOOTED IN FROM DRIVE 'A'. SETTING THIS FALSE ALLOWS BUILDING A SYSTEM ON A SINGLE DENSITY DISK. THIS BYTE IS HOW THE SYSTEM KNOWS WHETHER OR NOT A SINGLE OR DOUBLE DENSITY IS ON LINE.

**** NOTE ****

IF YOU HAVE TROUBLE READING A SINGLE DENSITY DISK ON THIS CONTROLLER, YOU MAY HAVE A DISK WITH THE WRONG SECTOR FORMATTING. TO FIND OUT, TAKE ANOTHER DISK AND USE THE NEW FORMAT.COM FILE ON THIS DISK TO REFORMAT IT. THEN USING YOUR OLD CONTROLLER, TRANSFER ALL THE PROGRAMS YOU WISH TO SAVE FROM THE DISK THAT WOULD NOT RUN ON THE NEW

CONTROLLER BOARD TO THE NEWLY FORMATTED DISK. WE REALIZE THAT THIS IS ALSO A REAL HASSEL TOO, BUT IT IS A NECESSARY EVIL. BESIDES, THE NEW FROMATTED DISK WILL STILL WORK WITH THE OLD CONTROLLER BOARD.

*** NOTE ***

IF ALL ELSE FAILS, EVEN AFTER READING THE DIRECTIONS, FEEL FREE TO CALL ME HERE AT TARBELL ELECTRONICS. AND IF YOU WOULD LIKE TO DISCUSS ANYTHING ABOUT THE BOARD OR SOFTWARE, CALL ME.

THANKS FOR INPUTS AND OUTPUTS ON THIS PRODUCT AND HOPE YOU WILL FIND THIS PRODUCT BOTH INFORMATIVE AND FUN TO WORK WITH.

GERALD.W.MULCHIN
ENGINEERING DEPT.
TARBELL ELECTRONICS
213 538 4251

GENERAL THEORY of OPERATION

The internal operation of a floppy disk operating system is probably the most complicated part of a micro-computer system. The hardware and software interact very closely, and therefore a very strong knowledge of 8080 assembly language and common logic operations is desirable to understand this section. Knowledge of the IEEE S-100 standard is also desirable, as there are some changes that have been made to the S-100 bus with this new specification. The IEEE S-100 Standard has been enclosed with this manual in the appendix, along with the data sheets for the rest of the integrated circuits used on the interface.

The heart of the Double Density interface is the 1791/1793 Floppy Disk Controller Chip. This chip is very similar to the 1771 in operation, but now includes all the functions necessary to run Double Density. For your convenience, the 1791/1793 data sheet is included in the appendix.

The interface may be broken down into subsections as follows:

1. 1791/1793 disk controller chip.
2. 8257 Direct Memory Access Controller chip.
3. Phase Locked Loop circuit.
4. Write Precompensation circuit.
5. General Drive and Computer interface.

The 1791/1793 controls the actual reading or writing to the floppy disk, and in which density this will happen. The floppy controller chip contains 4 internal registers which are programmed by the computer through it's data and address lines. the four registers are as follows:
1. status register
2. track register
3. sector register
4. data register

Review of the data sheet will help in understanding each function of these 4 registers.

DDEN is used to control in which density the floppy disk controller chip will be operating. Low equals Double Density, High equals Single Density.

EARLY and LATE control the Write Precompensation of the data being written to the disk. These two signals along with the TRK > 43 line control the amount of shift in time the bit that is being written to the disk is subjected. Precompensation during writing is a must because of the bit packing on the medium of the disk.

This interface also has provisions for precompensation on tracks < 43, and it is recommended that a small amount be used. The amount of precompensation is a switch selection, and will be explained in the jumper options.

READ GATE is an output used for synchronization of the data seperator circuit during read operations. A high on this pin indicates

that a field of 'ones' (or zeros) has been found in the inner record gaps of the disk.

The 8257 Direct Memory Access Controller chip controls the actual transfer of computer data between the disk and computer. This device can be thought of as a high speed semi-intelligent cpu in its operation. It contains 16 registers of which only 3 are used by this floppy disk interface board. One is a command register, and the other two are byte pair data registers. During read and write operations, the 8257 must be initialized with the byte transfer count, the address of where the data is to go, and the type of transfer that is to occur, such as read or write. The 8257 can transfer up to 16384 bytes of data, and put it into any memory locations within a normal 8080's addressing range. The important aspect about the 8257 is that it will transfer data to or from memory without the need of any cpu intervention other than being initally programmed by the cpu. After it has been programmed, it alone transfers the data, and in fact removes the cpu from the S-100 bus during these transfers. In-depth information about the 8257 is available in the INTEL data catalog and in the appendix of this manual.

The Phase Locked Loop circuitry on this interface is necessary for reliable data recovery, especially while running under double density. It's function is to remove effects of data fluctuations during READ operations which may be the result of drive speed or power line changes, and general system noise. The Phase Locked Loop is used during Single and Double Density operation. This is accomplished by logic on the interface and is controlled by the DDEN line and an internal hardware latch. Tri-state switching is used to select the master oscillator timing clock. When in Single Density, the master clock is equal to 8 Mhz. Double Density selection causes the master clock to change to 16 Mhz. A close examination of the schematic will show these logic changes during density selects.

The write precompensation is in general terms really a count down circuit, controlled by the EARLY, LATE, and TRK > 43 lines during writing operations. This applies only when operating in double density, as the EARLY and LATE signals are not active during single density. The count down circuit is clocked by the 16 Mhz master oscillator circuit. The amount of precompensation is determined by the preset value jammed into the 74LS161 from the EARLY or LATE pins of the floppy chip. After this value is loaded, the 74LS161 counts until it reaches zero, at which time it writes the data to the disk. The effect of this is to delay the time the bit would have been written to the disk, until it is actually written. The smallest amount of precompensation that may be realized from this circuit is:
1 / 16 Mhz = 62.5nsec.
Jumpers provided on the interface have been selected for optimum drive performance. Selection is based on manufacturer's recommendations for the drive in use, and our testing here at Tarbell Electronics.

The computer interface for this board is based on the IEEE S-100 bus interface specification. It is not radically different from the old S-100 bus design, and should run with most S-100 products on the

market. If you have any questions about your interface cards, check the section on S-100 compatible products in our manual.

The Disk Interface occupies an address range from E0-EF hex for the DMA controller portion and F8-FD hex for the disk controller portion. A jumper is provided to allow the address range to be moved to 60-6F hex and 78-7D hex respectively, to avoid address conflicts with exsiting computer boards you may have in your system. This is explained in the jumper options section. The address ports are used as follows:

E0 hex 8257 address register (must be two bytes to this port)
E1 hex 8257 word count register (must be two bytes to this port)
E8 hex 8257 command register (1 byte)
F8 hex disk command port (input)
F8 hex disk status port (output)
F9 hex disk track port (input/output)
FA hex disk sector port (input/output)
FB hex disk data port (input/output)
FC hex wait control port (input)
FC hex drive select port (output)
FD hex DMA end of operation port (input)
FD hex extended address port (output)

The extended address port (FD hex), allows the DMA controller to transfer data to and from memory beyond the normal 64k range of the 8080 cpu. This function is avalible for both read and write operations using the disk interface. The extended address lines are provided on the S-100 bus as described in the IEEE S-100 bus interface specification. The extended lines are A16-A23.

To use the extended address function, user written software must supply an 8 bit value corresponding to the bank of memory you want to access, out to port FD hex before any read or write operations occur with the disk interface. During DMA operation, this 8 bit latch is enabled, placing its contents onto the extended address lines. The output of this latch is normally tri-state until the DMA controller becomes active. Also, this latch may be programmed at any time with any value you wish, except during an actual transfer by the DMA controller. You could even change this latch value between byte transfers if you wish. With optional decoding on memory boards, possible memory capacities can be theoretically 8 banks of 64k (512kbytes), to 256 banks of 64k (16 Megabytes).

The interface is set up for Shugart 8" compatible drives, which means drives with a Shugart interface such as Shugart 800/801 and Siemens FDD 100-8,120-8, and 220-8 will interface directly to the controller board. There are many drives which fall into this catagory and we will be supplying updates as we go along for your convenience. At this time we at Tarbell Electronics have run the Shugart 800/801 and all 8" drives made by Siemens. This includes both single and double density. Persci drives model 270/277's are now supported with this interface. See the section on jumpers for an explanation and changes which must be made to support Persci drives.

DETAIL THEORY of OPERATION

This section of the manual will deal in depth with the theory of operation of the double density board. The explanation will be broken down into sections within the board design.

The following logic notation will be used:
XX' = The logic name XX not, or the inversion of XX.

1. RESET circuit

The floppy disk interface receives it's reset from line 75 (PRESET) on the S-100 bus whenever a power on sequence is initiated or whenever a RESET on the front panel of the computer is pushed. This line is active low (0) whenever a reset is pushed. The result of pushing a reset is to cause the floppy disk controller chip to do a restore of drive 0 to the home position, reset the DMA controller chip to the idle state, and the latch (U46), which is used for drive select, density select, and side select, to be cleared to the following condition, (a.) select drive 0, (b.) select single density, and (c.) select side 0.

The reset line from the bus is first inverted by U9 (7404) to provide an active high (1) signal for the DMA controller chip U29 (8257). This signal is inverted again to provide an active low (0) reset for floppy controller chip, U31 (1791/1793), and for U46 (74LS174) an 6 bit latch. This active low reset signal also turns on the bootstrap circuit by pulling the preset line of U35 low.

2. BOOTSTRAP Circuit

The bootstrap circuit is enabled during a power up sequence or from the front panel reset switch. The reset causes a preset of flip-flop U35, a 7474 D-toggle flip flop, causing it's output, pin 5, to go high (1). This output is tied to one of three (3) inputs of U33, a 7411 3-input AND gate. The two other inputs come from the S-100 bus interface pins 47 (SMEMR), and 78 (PDBIN). The output of U33 is tied to the input of a 7406 (U87), which drives the PHANTOM line (67) low. U33 also also drives a hex inverter U34, which drives the chip select line on the Bootstrap Prom low, enabling the data outputs of the prom on to the data bus. When run is enabled on the computer, the contents of the prom are read onto the data bus and into the cpu as instructions. Because this prom is only 32 bytes long, the method of disabling it when it has completed all its instructions, is to look at address line 5 of the S-100 bus. This address line is fed to one of the inputs of U47, a 7421 4-input AND gate. The other three (3) lines in to U47 are PHASE l (25),PSYNC (76), and SMI (44). When the computer has read all 32 bytes of the prom, and an attempt to read the 33rd byte is tried, address line 5 will go high (1), which causes one input of U47 to go high. The three other inputs of U47 will also go high, causing its output to go high. This output line then causes the output of U26, a 7404 inverter, to go LOW (0), resetting U35. When this flip flop is reset, its output, pin 5, will go low, disabling

both the PHANTOM line and the Bootstrap Prom chip select. This action releases the the bus data lines back the their normal operating condition. During power up of your system, if you wish to disable the bootstrap circuitry, and have a front panel, you may raise address-data switch 5 and hit examine. This will turn off the bootstrap circuit, allowing you to access all computer memory. The bootstrap may be defeated entirely by using jumpers E8 to E9 on the disk interface. Using jumpers E9 to E10 enables the bootstrap during each reset. Below is a listing of the bootstrap prom for both the standard Tarbell disk ports, and for our non-standard disk ports. Our standard prom is model # 100 and our non-standard prom is model # 101. Model 101 is for people who wish to run the disk interface at addresses 60 to 7D hex.

STANDARD PROM BOOTSTRAP LISTING

```
0000                    ORG     0       ;PROM RUNS AT LOC ZERO.
                ;
00F8 =          DISK    EQU     0F8H    ;BASE ADDRESS OF DISK PORTS.
00F8 =          DCOM    EQU     DISK    ;COMMAND PORT.
00F8 =          DSTAT   EQU     DISK    ;DISK STATUS PORT.
00FA =          SECT    EQU     DISK+2  ;SECTOR PORT.
00FB =          DDATA   EQU     DISK+3  ;DATA PORT.
00FC =          WAIT    EQU     DISK+4  ;WAIT PORT.
007D =          SBOOT   EQU     007DH   ;START OF SBOOT.
                ;
0000 DBFC       BOOT:   IN      WAIT    ;WAIT FOR HOME.(caused by reset)
0002 AF                 XRA     A       ;CLEAR ACCUM.
0003 6F                 MOV     L,A     ;CLEAR REG L.
0004 67                 MOV     H,A     ;CLEAR REG H.
0005 3C                 INR     A       ;SET A = 1.
0006 D3FA               OUT     SECT    ;START AT SECTOR 1.
0008 3E8C               MVI     A,8CH   ;READ THE SECTOR.
000A D3F8               OUT     DCOM    ;ISSUE THE COMMAND.
000C DBFC       RLOOP:  IN      WAIT    ;WAIT FOR DRQ OR INTRQ.
000E B7                 ORA     A       ;SET FLAGS.
000F F21900             JP      RDONE   ;DONE IF INTRQ.
0012 DBFB               IN      DDATA   ;ELSE,GET A BYTE FROM DISK.
0014 77                 MOV     M,A     ;PUT IT INTO MEMORY.
0015 23                 INX     H       ;BUMP POINTER.
0016 C30C00             JMP     RLOOP   ;LOOP TILL DONE.
0019 DBF8       RDONE:  IN      DSTAT   ;READ DISK STATUS.
001B B7                 ORA     A       ;SET THE FLAGS.
001C CA7D00             JZ      SBOOT   ;IF ZERO, GOTO SBOOT.
001F 76                 HLT             ;ELSE, DISK ERROR
```

NON-STANDARD BOOTSTRAP PROM LISTING

```
0000                    ORG     0       ;PROM RUNS AT LOC ZERO.
                ;
0078 =          DISK    EQU     078H    ;BASE ADDRESS OF DISK PORTS.
0078 =          DCOM    EQU     DISK    ;COMMAND PORT.
0078 =          DSTAT   EQU     DISK    ;DISK STATUS PORT.
007A =          SECT    EQU     DISK+2  ;SECTOR PORT.
007B =          DDATA   EQU     DISK+3  ;DATA PORT.
007C =          WAIT    EQU     DISK+4  ;WAIT PORT.
007D =          SBOOT   EQU     007DH   ;START OF SBOOT.
                ;
0000 DB7C       BOOT:   IN      WAIT    ;WAIT FOR HOME.(caused by reset)
0002 AF                 XRA     A       ;CLEAR ACCUM.
0003 6F                 MOV     L,A     ;CLEAR REG L.
0004 67                 MOV     H,A     ;CLEAR REG H.
0005 3C                 INR     A       ;SET A = 1.
0006 D37A               OUT     SECT    ;START AT SECTOR 1.
0008 3E8C               MVI     A,8CH   ;READ THE SECTOR.
000A D378               OUT     DCOM    ;ISSUE THE COMMAND.
000C DB7C       RLOOP:  IN      WAIT    ;WAIT FOR DRQ OR INTRQ.
000E B7                 ORA     A       ;SET FLAGS.
000F F21900             JP      RDONE   ;DONE IF INTRQ.
0012 DB7B               IN      DDATA   ;ELSE,GET A BYTE FROM DISK.
0014 77                 MOV     M,A     ;PUT IT INTO MEMORY.
0015 23                 INX     H       ;BUMP POINTER.
0016 C30C00             JMP     RLOOP   ;LOOP TILL DONE.
0019 DB78       RDONE:  IN      DSTAT   ;READ DISK STATUS.
001B B7                 ORA     A       ;SET THE FLAGS.
001C CA7D00             JZ      SBOOT   ;IF ZERO, GOTO SBOOT.
001F 76                 HLT             ;ELSE, DISK ERROR
```

3. ADDRESS SELECTION

The double density controller board is selected based on the low order 8 address line values presented to the interface during an input or output instruction. The normal address range for this board is from E0 hex to FD hex. There are provisions for changing the address range from 60 hex to 7D hex by means of jumpers E4,E5,and E6.

The base address for the DMA controller (8257) is E0 hex, with all possible 16 address from E0 to EF hex available for use by the DMA controller chip. U33, a three input AND gate, is used to determine the base address of E0 hex by tying address lines A7,A6,and A5 to its three inputs. You will notice that an inverter, U34, is in between one input of U33, and address line A7. By selecting the proper jumper at E4,E5, and E6, you may select a base address of either E0 hex or 60 hex. By using the inverter, U34, you will select the base address of 60 hex. By not using the U34, but using the jumper which bypasses U34, you will select a base address of E0 hex. The output of U34 is next

AND'ed with the inversion of A4 through U26. This gate (U48) is used to allow selections from E0 hex to EF hex for I/O operations with the DMA controller. The output of U48 drives one of the inputs to U43 for selecting the DMA controller chip select line. The other input for U43 (7400), comes from U45 (7432). U45 determines whether the current I/O operation is an Input or an Output with the interface board. The signals SINP and SOUT are two status lines from the CPU card used to determine the I/O operation. Because these two signals will not occur together, they may be OR'ed together through U43 to provide just one general signal for I/O operation decoding.

Disk I/O ports for the 1791/1793 floppy controller chip are decoded by U47, a 4 input AND gate. One input to U47 comes from U33's output, which is the address decode for the base address of Ex hex or 6x hex. Address lines 4 and 3 are tied to two of the other inputs of U47. Address line 2 is inverted through U26 (7404) and is the fourth input to U47. The Output of U47 goes high whenever any of the following address appear on the address bus,F8,F9,FA,and FB hex.

Ports FC and FD hex are decoded by U27 (74LS138). The output of gate U33 is used for the enable input of U27. The other two enables of U27 are an enable when low function and are derived from the inversion of address lines 3 and 4 through two inverters U26. The output of inverter U26 pin 10 also goes to one input of gate U48. If address line 4 is high (eg. Port FC), The output of U26 pin 10 will be low (0),causing the output of gate U48 to be low, disabling the selection of any port with the base address of Ex hex. The 3 low address lines, A0,A1, and A2 determine which port is selected on the output of U27. Also, even though the low 3 lines of the address bus are used by U27, only two of the possible 8 ports are used by the disk interface board. Port decodes from U27 for F8,F9,FA, and FB are not used. Only Ports FC and FD hex are used.

4. DISK CONTROL circuit

The 1791/1793 Floppy disk formatter/controller chip performs all the functions necessary to read or write data to a floppy disk drive. Both single and double density storage capabilities are supported. The chip is compatible with the IBM 3740 (FM) data format,IBM System 34 (MFM), or may be operated non-standard by using the controllers variable length sector capability.

The floppy controller chip contains five (5) internal registers that can be read or be written to. These registers are used to write commands, read status, and read and write data to and from the floppy disk drive. These five registers are selected by providing the proper binary code on the A0 and A1 lines of the floppy chip in conjunction with either a read or write operation. The registers and their addresses are as follows:

CS'	A1	A0	RE'= 0	WE'=0
0	0	0	Status Reg	Command Reg
0	0	1	Track Reg	Track Reg
0	1	0	Sector Reg	Sector Reg
0	1	1	Data Reg	Data Reg
1	x	x	Deselected	Deselected

The five internal registers of the floppy controller chip are accessed through the internal interface data bus. The internal data bus is buffered by U71 (8208) and U72 (8208). U71 and U72 are 8 bit bi-directional transcievers which are used as bi-directional data buffers between the computer S-100 bus and the floppy disk interface internal data bus. These transceivers allow data travel in either direction depending upon whether the TRANS/REC' pin (11) is high or low. To program the floppy controller chip, A0,A1 are selected for the desired operation. Write enable of U31 is made active low by processor signal SOUT and PWR' gated together by U23 (7400). The data that the CPU wishes to program the floppy controller with, is now placed on the DO0 - DO7 lines of the CPU card. This data is then presented to U71. Because we are not in the DMA mode of operation, the TRANS/REC' pin is already pulled low, causing the transceiver to be in the receive mode. The data is then passed through U71 onto the internal data bus and into the floppy chip DAL0 - DAL7 lines. Chip select, pin 3, of U31 is made active low by U48 (7408) output. One input of U48 comes from the DMA controller and the other input is from U43 which is the gating of the address port and the I/O mode desired. In this case, since we are programming the floppy controller, any port address in the range of F8 - FB hex gated together with SOUT will cause the data to be written to the controller chip.

5. Direct Memory Access

The sequence of operations for a DMA access is as follows:

A. The Basic Input Output System (BIOS part of CP/M) program sends a series of initialization bytes to the 8257. These include the starting address in memory for the data, the number of bytes to transfer, and the type of command (read, write, verify) which is being requested. The port numbers for these and other transfers are listed on page 3-3 in this manual.
B. The BIOS then sends track number, sector number, and type of command (read or write) to the 1793.
C. The 1793 then causes the head to load against the media (we are assuming we're already on the correct track). When the 1793 finds a sector header that matches the track and sector number in it's registers, and is ready to write or read the first byte, it activates its DRQ line, which is fed to the 8257. This signifies that it is ready to transfer a byte.
D. Soon after receiving the input on its DRQ0 line, the 8257 makes its HRQ line go high. This is fed through an OR gate

to S-100 bus line PHOLD'. This notifies the CPU that there is a DMA request pending.

E. When the CPU finishes the cycle it is currently in, it sends back a PHLDA signal over the S-100 bus to the HLDA input on the 8257. This tells the 8257 that its DMA request has been granted, and that the CPU is in a HOLD state.

F. The 8257 then activates its AEN line, which indicates that it has a valid address on A0 to A7 and D0 to D7. This signal is ORed with the HRQ to keep PHOLD' active, and disables the CPU address and data lines using S-100 bus lines DO DSB' and ADR DSB'. AEN also is fed to (U41) and (U67), which gates the DD board's own status and control lines onto the S-100 bus (PWR', PDBIN, SMEMR, SINP, SOUT, PSYNC, MWRITE, SINTA, SHLTA, SM1).

G. A short time later, the 8257 activates its DACK0' line, which disables the CPU's status and control lines, using S-100 bus lines STAT DSB' and C/C DSB'. The time between step F and G provides the overlap time, during which both our DD board and the CPU board have control of these status and control lines.

H. At the same time as the DACK0' line is activated, the 8257 activates either its MEMR' line, or its I/OR' line, depending upon whether it's going to do a write or read respectively, to disk. Step I will explain what happens for a write operation, Step J for a read (from disk) operation.

I. For a write operation: The MEMR' line coming from the 8257 is used for several things. It is fed through U67 to S-100 lines PDBIN and SMEMR to the system memory to gate the memory onto the S-100 bus. It is also used to activate U72 so that the S-100 DI bus is fed into the DD board's internal data bus and therefore providing a path from the memory output to the 1793. A short time after the MEMR' signal, the I/OW' signal is fed from the 8257 to the WE' input on the 1793, which strobes the data into the 1793. The 1793 then writes the data onto the disk.

J. For a read operation: The I/OR' signal from the 8257 is fed to the 1793, gating the data in its register onto the data bus. This signal is also used to activate U71 in the outward direction, so that the data is fed onto the S-100 DO bus out to the system memory. (mod for rev-e) A short time after the I/OR' signal, the MEMW' signal is generated by the 8257. This is used to generate the S-100 bus line PWR', which strobes the data into memory.

K. After either step I or J above, the reverse sequence occurs, turning over control of the bus back to the CPU.

6. Write Precompensation

The Write Precompensation circuit consists of a programmable counter, (U36), for delaying or advancing write data pulses during disk writes, a dip switch (SW-1) for adjusting the precompensation value, and the necessary decoding logic for early, late, and TRK > 43 (U12).

DETAIL THEORY of OPERATION

The 1793 produces along with it's write data pulses, two signals called 'early' and 'late'. These two signals, along with TRK > 43, are decoded by a 1 of 4 decoder circuit (U12) to select the switch setting from SW-1 for loading into the counter (U36).

Loading the counter starts the counter down counting. If there is no early or late signal generated (no precomp needed), the programmable counter is loaded with a positive (0111) 7, which is the zero precompensation center reference value.

Values from (0110) 6 through (0000) 0 are increasing late times, and values (1000) 8 through (1110) -2 are increasing early times. The programmable counter is clocked with 16 MHz during double density. Therefore, the minimum resolution is 62.5 nsec.

After the counter has been loaded with the desired value of precompensation, the counter down counts until a carry is produced.The carry, delayed one (1) clock cycle by a D-toggle flip-flop(U35), is used to trigger a 250 nsec. one-shot. The output of the one-shot, after buffering, is the precompensated data which is written to the drive. The counter then remains stopped until a new data pulse is sent from the 1793, starting the whole process again.

7. Data Recovery

Data recovery is provided by an on board Phase Locked Loop circuit. This circuit allows for maximum data recovery reliability, while rejecting drive speed variations and bit crowding. One shot (U74) conditions the data being read from the disk and provides RDATA* to the 1793. It also provides data to the phase comparator (U55) which is part of the phase locked loop. The active filter network which consist of U55,R5,R6,R7,R8, C5,C6 and Q2 removes noise and jitter from the incoming data and provides a correction voltage to the voltage controlled oscillator (U53). This oscillator provides the master clock frequency necessary for a stable read clock signal (RCLK) for the 1793. This output is either divided by 2 or divided by 4, controlled by the DDEN line, to provide the necessary 500 KHz or 250 KHz RLCK signal for double density or single density operation.

ASSEMBLY INSTRUCTIONS

Before attempting any assembly operations, it is recommended that you read this section and the parts list section first. This will help put your mind into a comfortable state about what you are going to be doing with the board.

1. ( ) Locate and confirm that your kit contains all the parts listed in the parts list in this manual. Any errors found should be reported to Tarbell Electronics for corrective measures. Also, you should make any necessary changes which you receive from Tarbell Electronics, on your board at this time.

2. ( ) If you are using sockets, install them at this time.

3. ( ) Locate the 50 pin header connector and install it at the top of using the 2 2-56 x 3/8 mounting screws and hardware.

4. ( ) Locate Q1, an LM-323 votage regulator, and the heatsink. Mount the regulator and heatsink on the board using the 4-40 x 3/8 screws and hardware.

5. ( ) Locate Q2, an MPS6571 transistor, and mount it as indicated by outline on the board.

6. ( ) Locate the 220 uhy choke, L1, and mount it on the board. This part may appear to you as looking like an resistor. It is not a resistor but is in fact a RF. coil. Use caution if you are in doubt about which one L1 is.

7. ( ) Locate the crystal, Y1, and mount it on the board. Mount the crystal down close to the board. Then take a small piece of wire and push it through the hole that is to the left of crystal, and solder it. Then, take the other end of this wire and bend it over the top of the crystal and cut off all but 1/8" of it. Then solder the wire to the crystal can. Do not over heat the crystal can, or you may open the hermetic seal.

8. ( ) Using the parts list and using the board layout drawing, start mounting all the capacitors on the board. Be sure to observe the polarity of the tantalum capacitors C13,C14,C15. The little square block on the board is the end that the plus (+) lead of the capacitor goes into.

9. ( ) Using the parts list and board layout drawing, mount all the resistors on the board.

10. ( ) Locate the dip switch and mount it. Note, if the dip switch you have has only 8 positions, you will have to mount the switch on the board starting at position 2 at the location on the board. There should be one open location at the top of the switch that is not used after you mount the switch.

11. ( ) Do not mount the IC's at this time, as you will need to check the voltage regulators for proper output voltages.

ASSEMBLY INSTRUCTIONS

12.( ) After all the components are mounted, plug the board into your computer and check the voltage regulators for proper operation. CAUTION** Be sure your computer is turned off before you plug in the board. The output of Q1 should be approx. 5 volts +/- .5 volts. The output of CR1 should be approx. 12 volts +/- .75 volts.

13.( ) Using the parts list and board layout drawing, mount the IC's into their respective locations. Use ''GREAT'' caution with the two 40 pin IC's when mounting them as it is possible to bend or break some of the leads on the part.

14.( ) This completes the assembly of the unit. On the following pages are the jumper options for setting up the board for your system.

JUMPER OPTIONS

This board has very little jumpering required to get it running. The only jumpers that need setup are for address selection, XRDY or PRDY line, and Write Precompensation value.

1. Normal Board Setup

The normal configuration is as follows:
a. Board address set for base address of E0 hex.
b. PRDY line used for processor wait.
c. SW-1 set for 62.5 nsec on trk < 43 and 187.5 nsec for trk > 43.

NOTE **
The write precompensation may be the only adjustment you will have to make for your drives.

2. Address Selection

This board may be addressed in one (1) of two (2) address areas in your computer. Either an address range of 60 - 7D hex or E0 - FD hex may be selected. You should beware of existing computer boards in your system which use these address ports for I/O operations, as a conflict may exist. Our I/O section for CP/M uses an address range of E0 - FD hex, as does our Standard bootstrap prom.

PORT	JUMPER
E0 - FD Hex	E19 to E20
60 - 7D Hex	E19 to E18

3. XRDY or PRDY selection

Three possible configurations exist in the selection of the right line to use. These are, no front panel, front panel, and if you have a front panel, who made it.

No Front Panel	Jumper E1-E2 or E3-E2
Imsai Front Panel	Jumper E1-E2
Altair Front Panel	Jumper E3-E2

NOTE **
Be sure that other boards in your system do not use either the XRDY or PRDY lines improperly, as this would cause improper operation of this interface board. Things to beware of are memory boards which activate a tri-state driver in anticipation of memory wait states, or dynamic memory boards which require the use of this line for refresh operations, or memory boards which use slow memorys such as old, old 2102's.

4. Write Precompensation Selection

The selection of the write precompensation is based on the type of drive you are using and the amount of errors you are getting from the disk when you run our special disk test program. To properly set

the precompensation, first set the dip switch S1 for a value of 62.5nsec for < 43 and 187.5 nsec for > 43 as shown in the Precomp Table in Fig.1 Next, format a good certified double density disk with our DFRAND.COM program. Then read the disk for errors using our DTEST.COM program. If you find any errors, then change the precompensation switch settings to another value in the table and run the sequence again. The initial values of 62.5nsec for < 43 and 187.5nsec for > 43 were found to be midrange values here at Tarbell Electronics. These values are with the switch positions 5 and 8 on (if there is a 9 position switch), or positions 4 and 7 on (if there is an 8 position switch).

After you have found the proper settings for the precompensation switches, reformat the disk using the DFORMAT.COM program so that the disk will have the proper data in each sector required for CP/M operation. (E5 data fill)

	SW - 1 settings									
	Trk < 43						Trk > 43			
	--Early--		--Late--		----Early-----			----Late----		
Pos	1		2	3		4	5	6		7	8	9
	ns		ns			ns			ns			
ns		ns			ns							
62.5	1	62.5	0	0	62.5	0	1	1	62.5	0	0	0
x	x	x	x	x	187.5	0	1	0	187.5	0	1	0
x	x	250.0	0	1	250.0	0	0	1	250.0	0	1	1
x	x	x	x	x	312.5	0	0	0	312.5	1	0	0
x	x	375.0	1	0	x	x	x	x	375.0	1	0	1
x	x	x	x	x	x	x	x	x	437.5	1	1	0
x	x	500.0	1	1	x	x	x	x	500.0	1	1	1

FIG 1

Note: x = not adjustable, 1 = on, 0 = off

5. Bootstrap

The on-board bootstrap may be enabled or disabled by jumpers E8,E9,and E10 as follows.

Bootstrap enabled - Jumper E9 to E10
Bootstrap disabled - Jumper E9 to E8

6. Persci drives

If you have a Double Density board Rev. D or Rev. E, and want to run a Persci model 277/270 with it, then do the following changes to the board.

1. On the double density interface:

a. on back side, cut the trace connecting E4 to E6 and jumper E4 to E5. (bypasses step one-shot)

b. Jumper E11 to E12. (1793 test pin)

c. Jumper E13 to E14. (seek complete line)

Now you must make the Persci 277/270 look like a Shugart compatible drive. Thanks to John Hock of Bits & Bytes of Fullerton, we now have the all the changes. These are changes which you must make to the drive and in some cases will involve making trace cuts on the Persci drive.

Cuts to make:
---

1. Trace to P1-16 (back side)
2. Trace between BL-BC (front side)
3. Trace between U11-12 and U11-13 (back side)
4. Trace between U11-10 and U11-11 (back side)
5. Trace from P1-2 to U1-8 (front side)
6. Trace to P1-30 (back side)
7. Trace to P1-32 (back side)

Jumpers to add:
---

1. U11-12 to P1-32 (back side)
2. U11-10 to P1-30 (back side)
3. H to M (for head load)
4. H to EL (for head load)

Persci jumpers: (board assy.200263-007 rev N/S)

1( ) A - B 2( ) J - Z 3( ) K - L 4( ) N - P 5( ) T - S
6( ) U - V 7( ) BK-BM 8( ) BA-BB 9( ) AK-AH 10( ) X - W
11( ) AD-AE 12( ) AP-AR 13( ) AS-AT 14( ) AM-AN 15( ) BE-BD

Jumpers E-D and G-F and AC-AB should be open.

Drive select:

Drive 1 (A & B)	Drive 2 (C & D)
U11 13 to 2	U11 12 to 2
U11 11 to 4	U11 10 to 4
	Remove U1

Our bios packages for CP/M use with the double density board must have some of the equates changed for proper operation with the Persci 277/270.

JUMPER OPTIONS

In the bios change HLAB EQU 0 to HLAB EQU 8 for head load at beginning of seeks.

Set DUAL to TRUE as there are two heads moving together.

These changes were tried on our Persci model 277/270 here at Tarbell Electronics which has a revision number of N/S. We are not sure about other revisions which Persci makes or about there operation in Double Density. You should probably consult the factory about any revisions you have which do not agree with our own. Operation with the Persci has been quite good in Single Density operation on the new controller. But Double Density has been poor. This is probably due to the fact that our Persci 277/270 is not rated for Double Density operation. This is probably due to head design. Adjusting the precompensation may help some what.

For normal operation with Shugart compatible drives, install jumpers as follows:

( ) E13 to E15
( ) E4 to E6 <-- normally etched on the board

7. Phase Locked Loop circuit

The Phase Locked Loop circuit has provisions for a second order low pass filter if needed. At this time, we have found no need to incorporate this feature. Therefore the following jumpers or components are used.

R7 install a jumper
C4 will be missing
R2 and R4 will be missing

8. Interrupt option

Interrupts from the Floppy controller may be used to generate a interrupt to the CPU if desired. The large hole (E23) just above pin 8 of the S-100 connector is the output for the interrupt line. This is an active low signal and is normally tri-state. This line may be connected to any of the S-100 vector interrupt lines on the bus. You will need a vector interrupt card if you plan on using interrupts other than RST 7. The vector interrupt lines are defined in the S-100 standard on pages 10-1 to 10-5 of this manual.

9. MWRITE option

If your memory boards require the MWRITE signal to write data into memory, and this signal is not generated on the cpu or front panel, then you will have to jumper E16 and E17 together. If your memory boards use PWR' for writing data into memory, then leave E16 to E17 open.

JUMPER OPTIONS

10. 8257 Clock option

An option has been provided on the board for running IC U29 at either 2MHz or 4MHz. This option is provided so that people who wish to use the AMD 9517 at full speed may do so. Otherwise, if you are using the 8257 supplied in our interface, then you will have to run it at 2MHz.

Jumpers are as follows:

device	jumpers	
8257	E23 - E25	2MHz clock
9517	E24 - E25	4MHz clock

** Note ** Software programming for the 9517 is different than the 8257. They are pin compatible only.

11. 1793 Read delay

The 1793 has a hold time restriction when reading data or status from it. A one-shot has been provided to stall the CPU during any reading from ports F8 - FB Hex (78 - 7B Hex). This option is provided allready connected on the board. This is the only WAIT, when running DMA operation, generated on the board. This option may be defeated by cutting the trace between E26 and E27 on the board. The only problem you may find if you cut this trace is that while running with a Z-80 at 4MHz, you may read the 1793 too fast. This is also a function of the 1793 you are using at the time. You may have to replace the jumper if you find you have any problems reliably reading the 1793.

12. Extra buffer chip

Located at U41 is an extra buffer for use as you may see fit. This buffer is an enabled Tri-state buffer of the non-inverting type. Jumpers are provided so you may use it.

E22 = buffer input
E21 = buffer output

PARTS LIST

Qty.	Descriptor	Desiginator
Resistors		
1	120 ohm 1/2 watt	R29
1	220 ohm 1/8 watt	R6
3	330 ohm 1/4 watt	R1,R3,R36
5	470 ohm 1/4 watt	R10,R11,R12,R13,R14
1	470 ohm 1/8 watt	R8
1	510 ohm 1/8 watt	R39
5	1 k ohm 1/4 watt	R19,R24
1	1 K ohm 1/8 watt	R7
7	2.2kohm 1/4 watt	R15,R16,R30,R31,R38
2	2.4Kohm 1/8 watt	R9,R11
2	4.3Kohm 1/4 watt	R40,R43
5	4.7kohm 1/4 watt	R17,R18,R23,R25,R26
2	5.1Kohm 1/8 watt	R41,R42
1	6.2Kohm 1/8 watt	R5
4	10 kohm 1/4 watt	R21,R27,R28
2	33 kohm 1/4 watt	R37,R35
1	4116-003-221-331	U8
Capacitors		
2	18 pf cap	C9
2	56 pf cap	C3,C4
2	100 pf cap +/- 5%	C7,C8
2	220 pf cap	C12,C17
1	680 pf cap	C1
1	.0015 mfd cap	C6
1	.0039 mfd cap	C5
28	.1 mfd cap	C11,C20,C21,C22,C23,C24,C25,C26,C27,C28 C29,C30,C31,C32,C33,C34,C35,C36,C37,C38 C39,C40,C41,C42,C43
1	4.7 mfd @ 10 volts	C10
2	10 mfd @ 16 volts	C13,C15
1	22 mfd @ 10 volts	C14
Misc.		
1	16 MHz crystal	Y1
1	MPS 6571 Transistor	Q2
1	1N4742 12 volt 1 watt zener	CR1
1	9 position dip switch	SW-1
Hardware		
1	TO-3 Heatsink	
2	4-40 x 3/8 screw	
2	4-40 x 1/4 nut	
2	# 4 washer	
2	2-56 x 3/8 screw	
2	2-56 x 3/16 nut	
2	# 2 washer	

PARTS LIST

Connectors

1	50 pin connector		J1
1	16 pin dip-socket		U52
2	40 pin dip-socket		U29,U31

IC's

** Note ** Equiv. 74LS parts may be used where indicated in list.

3	7400/74LS00	Quad Nand gate	U12,U23,U43
5	7404/74LS04	Hex Inverter	U9,U26,U34,U44
1	7404	Hex Inverter	U66
1	74S04	Schottky Hex Inverter	U85
1	7406	O.C.Hex Inverter	U87
2	7407	Hex Buffer	U13,U16
2	7408/74LS08	Quad And Gate	U42,U48
1	7411/74LS11	3 Input And Gate	U33
1	7413/74LS13	4 Input Schmitt Trigger	U47
2	7432/74LS32	Quad Or Gate	U45,U73
2	7438	O.C.Quad Nand Gate	U21,U22
2	7474/74LS74	D Toggle Flip Flop	U35,U77
1	7493	4 Bit Binary Counter	U86
1	74LS109	Dual J-K Flip Flop	U76
1	74LS113	Dual J-K Flip Flop	U56
3	74LS123	Dual One Shot	U10,U32,U64
1	82S123/5331	Bootstrap Prom	U52
3	74125/74LS125	Quad Tri-state Buffer	U25,U65
1	741S138/8205	Octal Decoder	U27
1	74145	1 of 10 Decoder	U24
1	74LS153	Dual 4 to 1 mux.	U75
1	74LS161	Preset Counter	U36
1	74174/74LS174	6 Bit Latch	U46
2	74LS221	Dual One-shot	U53,U74
2	74LS373	Octal Tri-state Latch	U68,U69
3	8T97	Hex Tri-state Buffer	U7,U67,U41
3	8208/8286/8304	Octal Transciever	U28,U71,U72
1	MC4044	Phase Comparator	U55 (Motorola)
1	LM 323	5 Volt 3 Amp Regulator	Q1

LSI chips

1	8257	DMA Controller Chip	U29
1	1793	Floppy Controller	U31

** Note ** U70 is not used

TARBELL DOUBLE DENSITY FLOPPY DISK INTERFACE FULL WARRANTY

1. Any faulty component part purchased from Tarbell Electronics, which is returned within 6 months after the date of purchase will be replaced at no charge. Components returned under this part of the warranty should be with a letter explaining what is wrong with the part.

2. Any factory-assembled floppy disk interface, which does not work correctly, and is returned within 6 months after the date of purcnase, will be restored to proper operating condition or replaced without charge.

3. Any floppy disk interface kit, which in the opinion of the manufacturer has been assembled with reasonable care, and is returned for repair within 6 months after the date of purchase, will be repaired for a charge commensurate with the work required. (parts will be free) but in no case will exceed $100 without notification of the owner.

4. Any floppy disk interface not covered by the above condition will be subject to a charge commensurate with the work and parts required, but in no case will exceed $100 without notification of the owner.

5. Parts can be returned directly to the address below for replacement. Complete floppy disk interfaces should be returned to the place of purchase. If this is not possible, or if it is very inconvenient, it may be returned to the address below, with proof of purchase.

6. Tarbell Electronics assumes no responsibility for consequential damages to other connected equipment, or for time lost, or programs or data lost, because of interface malfunction or incorrect documantation.

7. If you are disatisfied with the operation of a factory-assembled Tarbell Double Density Floppy Disk Interface for any reason, your money will be cheerfully refunded, provided the unit is returned within the six month warranty period.

8. Tarbell Electronics does not warrant that the disk interface will work with all "S-100" computer systems, or with all floppy disk drives. Call the factory or ask your local dealer about any possible conflicts in your system.

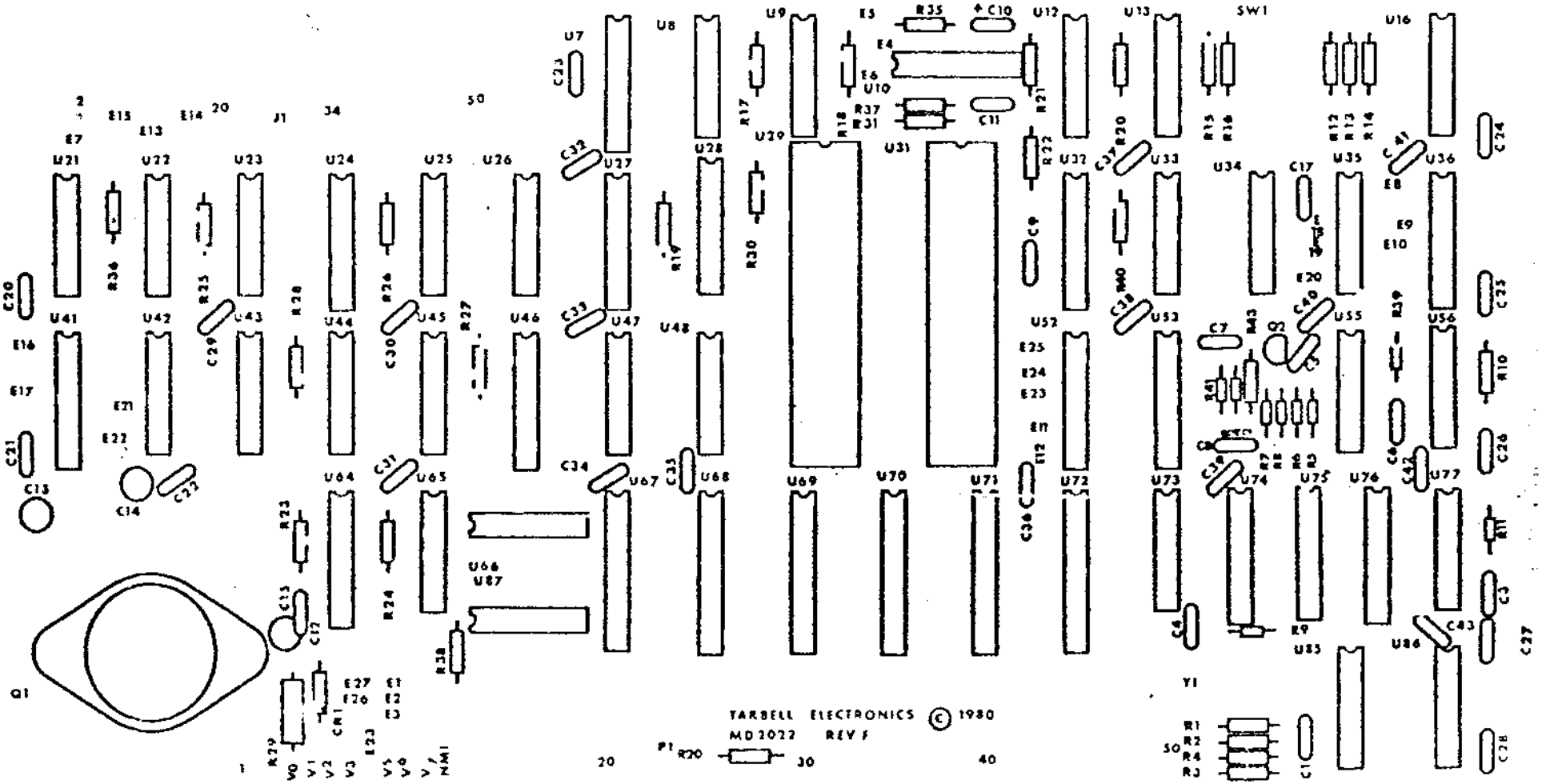
9. This warranty does not cover parts, or interfaces built from parts, which are not traceable to Tarbell Electronics.

10. An interface which is assembled from a kit by a Tarbell dealer has only the parts covered by this warranty, not the labor. All interfaces which were sold as kits, will have a "K" marked on the solder side. The dealer may provide his own warranty in this case.

TARBELL DOUBLE DENSITY FLOPPY DISK INTERFACE FULL WARRANTY

Defective parts or interfaces covered under this warranty should be sent WITH PROOF OF PURCHASE (like a receipt) to:

Tarbell Electronics
950 Dovlen Place, Suite B
Carson, California 90746



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IEEE Specification, IEEE Task 696.1/D2

The following is a list of the IEEE pin functions, signals, type of signal, active level, and a description of the signal.

The following conventions will be used:

1. * = inverted signal or the NOT function.
2. M = master.
3. B = bus.
4. S = slave.
5. O.C. = open collector.
6. H = high or logic level 1
7. L = low or logic level 0

Pin	Signal	Type	Active Level		Description
1	+8 volts	B			Instantaneous min greater than 7 volts, instantaneous max less than 25 volts, average max less than 11 volts.
2	+16 volts	B			Instantaneous min greater than 14.5 volts, instantaneous max less than 35 volts, average max less than 21.5 volts.
3	XRDY	S	H		One of two ready inputs to the current bus master. The bus is ready when both inputs are true (H). see pin 72.
4	VI0*	S	L	O.C.	Vectored interrupt line 0.
5	VI1*	S	L	O.C.	Vectored interrupt line 1.
6	VI2*	S	L	O.C.	Vectored interrupt line 2.
7	VI3*	S	L	O.C.	Vectored interrupt line 3.
8	VI4*	S	L	O.C.	Vectored interrupt line 4.
9	VI5*	S	L	O.C.	Vectored interrupt line 5.
10	VI6*	S	L	O.C.	Vectored interrupt line 6.
11	VI7*	S	L	O.C.	Vectored interrupt line 7.
12	NMI*	S	L	O.C.	Non-maskable interrupt line.
13	PWRFAIL*	B	L		Power fail bus signal.
14	DMA3*	M	L	O.C.	Temporary master priority bit 3.
15	A18	M	H		Extended address bit 18.

16	A16	M	H		Extended address bit 16.
17	A17	M	H		extended address bit 17.
18	SDSB*	M	L	O.C.	Disable signal for 8 status lines.
19	CDSB*	M	L	O.C.	Disable signal for 8 control lines.
20	GND	B			Common with pin 100
21	NDEF				Not to be defined. Manufacturer must specify any use in detail.
22	ADSB*	M	L	O.C.	Disable signal for 16 address lines.
23	DODSB*	M	L	O.C.	Disable for 8 data out lines.
24		B	H		Master timing signal for bus.
25	pSTVAL*	M	L		Status valid signal.
26	pHLDA	M	H		Control signal used in conjunction with HOLD* to coordinate bus/master transfer operations.
27	RFU				Reserved for future use.
28	RFU				Reserved for future use.
29	A5	M	H		Address bit 5.
30	A4	M	H		Address bit 4.
31	A3	M	H		Address bit 3.
32	A15	M	H		Address bit 15.
33	A12	M	H		Address bit 12.
34	A9	M	H		Address bit 9.
35	DO1/DATA1	M/MS	H		Data out bit 1,bidirectional bit 1.
36	DO0/DATA0	M/MS	H		Data out bit 0,bidirectional bit 0.
37	A10	M	H		Address bit 10.
38	DO4/DATA4	M/MS	H		Data out bit 4,bidirectional bit 4.
39	DO5/DATA5	M/MS	H		Data out bit 5,bidirectional bit 5.
40	DO6/DATA6	M/MS	H		Data out bit 6,bidirectional bit 6.
41	DI2/DATA10	S/MS	H		Data in bit 2,bidirectional bit 10.

42	DI3/DATA11	S/MS	H		Data in bit 3,bidirectional bit 11.
43	DI7/DATA15	S/MS	H		Data in bit 7,bidirectional bit 15.
44	sM1	M	H		Status signal indicating current cycle is op-code fetch.
45	sOUT	M	H		Status signal indicating data transfer bus cycle to output device.
46	sINP	M	H		Status signal indicating data transfer bus cycle from input device.
47	sMEMR	M	H		Status signal identifying bus cycles which transfer data from memory to a bus master, which are not interrupt acknowledge instruction fetch cycles.
48	sHLTA	M	H		Status signal indicating a HALT instruction has been executed.
49	CLOCK	B			2 MHz (0.5%) 40-60% duty cycle. Not required to be synchronous with any other bus signal.
50	GND	B			Common with pin 100.
51	+8 volts	B			Common with pin 1.
52	-16 volts	B			Instantaneous max less than -14.5 volts,instantaneous min greater than -35 volts, average min greater than -21.5 volts.
53	GND	B			Common with pin 100.
54	SLAVE CLR*	B	L	O.C.	Reset signal to reset bus slaves. Must be active with POC* and may also be generated by external means.
55	DMA0*	M	L	O.C.	Temporary master priority bit 0.
56	DMA1*	M	L	O.C.	Temporary master priority bit 1.
57	DMA2*	M	L	O.C.	Temporary master priority bit 2.
58	sXTRQ*	M	L		Status signal which requests 16-bit slaves to assert SIXTN*.
59	A19	M	H		Extended address bit 19.
60	SIXTN*	S	L	O.C.	Signal generated by 16-bit slaves in response to the 16-bit request signal

					sXTRQ*.
61	A20	M	H		Extended address bit 20.
62	A21	M	H		Extended address bit 21.
63	A22	M	H		Extended address bit 22.
64	A23	M	H		Extended address bit 23.
65	NDEF				Not to be defined signal.
66	NDEF				Not to be defined signal.
67	PHANTOM*	M/S	L	O.C.	Bus signal which disables normal slave devices and enables phantom slaves. Primarily used for bootstrapping systems without hardware front panels.
68	MWRT	B	H		Gating of pWR*-sOUT. Signal must follow pWR* by no more than 30 ns.
69	RFU				Reserved for future use.
70	GND	B			Common with pin 100.
71	RFU				Reserved for future use.
72	RDY	S	H	O.C.	See comments for pin 3.
73	INT*	S	L	O.C.	Primary interrupt request bus signal.
74	HOLD*	M	L	O.C.	Control signal used in conjuction with pHLDA to coorodinate bus master transfer.
75	RESET*	B	L	O.C.	Signal used to reset bus master devices. This signal must be active with POC* and may be generated by external means.
76	pSYNC	M	H		Control signal identifying BSl.
77	pWR*	M	L		Control signal signifying the presence of valid data on DO bus or data bus.
78	pDBIN	M	H		Control signal that request data on the DI bus or data bus from the currently addressed slave.
79	A0	M	H		Address bit 0.
80	A1	M	H		Address bit 1.
81	A2	M	H		Address bit 2.

82	A6	M	H		Address bit 6.
83	A7	M	H		Address bit 7.
84	A8	M	H		Address bit 8.
85	A13	M	H		Address bit 13.
86	A14	M	H		Address bit 14.
87	A11	M	H		Address bit 11.
88	DO2/DATA2	M/MS	H		Data out bit 2,bidirectional bit 2.
89	DO3/DATA3	M/MS	H		Data out bit 3,bidirectional bit 3.
90	DO7/DATA7	M/MS	H		Data out bit 7,bidirectional bit 7.
91	DI4/DATA12	S/MS	H		Data in bit 4,bidirectional bit 12.
92	DI5/DATA13	S/MS	H		Data in bit 5,bidirectional bit 13.
93	DI6/DATA14	S/MS	H		Data in bit 6,bidirectional bit 13.
94	DI1/DATA9	S/MS	H		Data in bit 1,bidirectional bit 9.
95	DI0/DATA8	S/MS	H		Data in bit 0,bidirectional bit 8.
96	sINTA	M	H		Status signal identifying the bus input cycles that may follow an accepted interrupt request presented on INT*.
97	sWO*	M	L		Status signal identifying a bus cycle which transfers data from a bus master to a slave.
98	ERROR*	S	L	O.C.	Bus status signal signifying an error condition during the present bus cycle.
99	POC*	B	L		Power-on clear signal for all bus devices. During active condition, this signal must stay low for at least 10 msecs.
100	GND	B			System ground bus.

Compatible S-100 Products

As a service to our customers, we have decided to provide information about other S-100 products that will work correctly with our new double density interface.

The list below only represents those products that We here at Tarbell Electronics have tested ourselves, and does not imply that these are the only S-100 that the double density interface will work with, and it is hoped that our customers will provide us with additional information about other S-100 products that they have found works with our interface.

CPU's

Imsai 8080, Delta Products Z-80, Cromemco Z-80, S.D.Sales Z-80, Vector Graphics Z-80.

** NOTE ** S.D.Sales SBC-100 and SBC-200 will not work because there are no bus disable lines on their board.
Ithica Audio Z-80 cpu's have been found to be unreliable with our double density interface when running with the DMA mode of operation.

MEMORY

Tarbell 32K static, Seals 32K static, Spacebyte 16K static, Industrial Microsystems 16K static, Godbout 32K static, Measurement System & Control DM 6400 and DMB 6400 dynamic boards

I/O interfaces

Processor Tech 3P+S, MITS SIO2, Thinker Toys Switcher, Vector Graphics Bit streamer, Dynabyte Intelligent CRT, S.D.Sales VDB-8024.

Drives

Shugart SA-800/801, Siemens FDD 100-8, FDD 100-8D / 120-8 / 220-8, CDC 9606 2/3, Remex RFD 4000/4001, MFE model 700.

NOTE *****

In order to use the Delta Products CPU, you must disable the Power-on-jump to the prom. The following modification to the CPU card will allow you to use the bootstrap on the floppy interface.

1.( ) Remove IC10c, bend pin 11 out away from the socket, and put IC10c back in.
2.( ) Ground pin 13 of IC13c.

This modification now allows you to boot up our disk controller by pushing the front panel reset button.

The Measurement System & Control dynamic memory card is not guaranteed to run with an 8080 cpu and our double density interface at 2 Mhz. They will run ok at 2 or 4 Mhz using Z-80 CPUs.

Compatible S-100 Products

Some dynamic memory cards require PSYNC to control refreshing on their cards. As our double density interface does not supply PSYNC during a DMA cycle, there may be a problem in refreshing on these memory cards.

DISK TEST ROUTINES

1. Test routines

The following routines are provided so that you may test your interface for proper operation. These routines involve both the TYPE 1 and TYPE 2 commands for the floppy disk controller chip. *** Note *** These routines assume that you have a front panel on your computer. If you do not have one, you will have to modify these programs to work with a system monitor, or whatever.

```
0000                    ORG     0
                    ;
                    ; define disk i/o ports.
                    ;
00F8 =              DCOM    EQU     0F8H            ;DISK COMMAND PORT
00F8 =              DSTAT   EQU     DCOM            ;DISK STATUS PORT
00F9 =              TRACK   EQU     DCOM+1          ;TRACK PORT
00FA =              SECT    EQU     DCOM+2          ;SECTOR PORT
00FB =              DDATA   EQU     DCOM+3          ;DATA PORT
00FC =              WAIT    EQU     DCOM+4          ;WAIT PORT
                    ;
                    ;The following routine will allow you to
                    ;check for any internal shorts or opens
                    ;with in the floppy interface. The routine
                    ;reads the front panel switches, writes it
                    ;to the floppy disk data port, then reads
                    ;it back from the floppy disk data port, and
                    ;writes it back out to the front panel lights.
                    ;there should be a one to one match of the
                    ;switches to the data lights. If more than
                    ;one light comes on at a time, there is an
                    ;internal short on the floppy data lines. If
                    ;a light does not come on when a switch it
                    ;turned on, then there is an open line on that
                    ;data bit.
                    ;
                    ; TEST ROUTINE FOR CHECKING
                    ; DISK INTERNAL DATA BUS.
                    ;
0000 DBFF           BUSS:   IN      0FFH            ;GET FRONT PANEL DATA
0002 D3FB                   OUT     DDATA           ;SEND IT TO CONTROLLER
0004 DBFB                   IN      DDATA           ;GET DATA BACK AGAIN
0006 2F                     CMA                     ;INVERT FOR FRONT PANEL
0007 D3FF                   OUT     0FFH            ;SHOW IT ON FRONT PANEL
0009 C30000                 JMP     BUSS            ;LOOP AGAIN
```

DISK TEST ROUTINES

```
                        ;
                        ;The following routine allows testing the
                        ;seek operation of the interface. You will
                        ;need to put in blank disk into the drive
                        ;and close the door. Do not put in a disk
                        ;which contains any important data, as you
                        ;may wipe it out. Do not set the front panel
                        ;switches for anything higher than 3F hex,
                        ;as this will cause the head to slam up past
                        ;track 76, possibly causing damage.
                        ;
                        ; SEEK TEST ROUTINES
                        ; DON'T SET FRONT PANEL
                        ; SWITCHES FOR A HEX VALUE
                        ; HIGHER THAN 3F OR YOU WILL
                        ; SLAM THE HEAD BEYOND TRACK
                        ; 76.
                        ;
000C DBFF               SEEK:   IN      0FFH            ;READ FRONT PANEL
000E D3FB                       OUT     DDATA           ;SEND TRACK NUMBER
0010 3E13                       MVI     A,13H           ;GET SEEK COMMAND
0012 D3F8                       OUT     DCOM            ;SEND IT
0014 C30C00                     JMP     SEEK            ;LOOP AGAIN
                        ;
                        ;The following routine test for step in
                        ;and step out. You will need to mount a
                        ;disk into the drive and shut the door.
                        ;DO NOT PRESS RUN !!! for this test. Use
                        ;single step operation.
                        ;The program as listed will step in toward
                        ;track 76. To step out toward track 0, you
                        ;need to change the 43H to a 63H.
                        ;
                        ; STEP IN/OUT ROUTINE
                        ;
0017 3E43               STEP:   MVI     A,43H           ;STEP IN COMMAND
0019 D3F8                       OUT     DCOM            ;ISSUE COMMAND
001B C31700                     JMP     STEP            ;LOOP AGAIN
                        ;
                        ;The following routine checks for head
                        ;load command. You will need to mount a
                        ;disk and shut the door to run this test.
                        ;DO NOT USE A VALUABLE DISK !!! for this
                        ;test.
                        ;
                        ; TYPE 2 COMMAND
                        ; HEAD LOAD ROUTINE
                        ;
001E 3E8C               HEAD:   MVI     A,8CH           ;HEAD LOAD COMMAND
0020 D3F8                       OUT     DCOM            ;ISSUE COMMAND
0022 C31E00                     JMP     HEAD            ;LOOP AGAIN
```

```
                        ;
                       ;The following routine reads a sector
                       ;from the disk and puts the data into
                       ;a buffer call RAMADD. This buffer can
                       ;be anywhere in memory you wish.
                       ;The routine saves the status of the disk
                       ;operation at the location called STAT.
                       ;If you have problems, check the bits at
                       ;this location against the status bits
                       ;shown in the data sheet for the floppy
                       ;controller chip, in Appendix A (1793).
                       ;You will need to mount a blank disk into
                       ;the drive and shut the door.
                       ;DO NOT USE A VALUABLE DISK !!! for this
                       ;test.
                        ;
                        ; READ A SECTOR ROUTINE
                        ;
1000 =                  RAMADD EQU     1000H           ;CAN BE ANYWHERE
                        ;
0025 3ED0               READ:  MVI     A,0D0H          ;ISSUE FORCE INTERRUPT
0027 D3F8                      OUT     DCOM            ;SEND IT
0029 E3                        XTHL                    ;SOME
002A E3                        XTHL                    ;DELAY
002B 210010                    LXI     H,RAMADD        ;POINT TO MEMORY BUFFER
002E 3E01                      MVI     A,1             ;LOAD SECTOR NUMBER
0030 D3FA                      OUT     SECT            ;SEND IT TO SECTOR PORT
0032 3E8C                      MVI     A,8CH           ;GET READ COMMAND
0034 D3F8                      OUT     DCOM            ;ISSUE READ COMMAND
0036 DBFC               RLOOP: IN      WAIT            ;WAIT FOR DRQ OR INTRQ
0038 B7                        ORA     A               ;SET FLAGS FOR OPERATION
0039 F24300                    JP      RDONE           ;DONE IF INTRQ
003C DBFB                      IN      DDATA           ;ELSE, READ A BYTE FROM DISK
003E 77                        MOV     M,A             ;PUT IT INTO THE BUFFER
003F 23                        INX     H               ;BUMP BUFFER POINTER
0040 C33600                    JMP     RLOOP           ;READ NEXT BYTE FROM DISK
0043 DBF8               RDONE: IN      DSTAT           ;CHECK DISK STATUS
0045 324B00                    STA     STAT            ;SAVE THE STATUS
0048 C34800             HJMP:  JMP     HJMP            ;HARD LOOP
004B 00                 STAT:  DB      0               ;SAVE STATUS HERE WHEN DONE
```

```
                        ;
                        ;The following routine writes one
                        ;sector of the disk. If you have
                        ;a problem, check the status bits
                        ;at location WSTAT against the bits
                        ;in the data sheet for the 1793 in
                        ;the appendix.
                        ;This routine is similar in operation
                        ;to the read a sector routine above.
                        ;You must mount a blank disk into the
                        ;drive and shut the door.
                        ;DO NOT USE A VALUABLE DISK !!! as
                        ;this routine does write on the disk,
                        ;and you will lose any data on the
                        ;sector you write to.
                        ;
                        ; WRITE A SECTOR ROUTINE
                        ;
004C 3ED0       WRITE:  MVI     A,0D0H          ;FORCE INTERRUPT COMMAND
004E D3F8               OUT     DCOM            ;ISSUE IT
0050 E3                 XTHL                    ;SOME
0051 E3                 XTHL                    ;DELAY
0052 3E01               MVI     A,1             ;GET SECTOR NUMBER
0054 D3FA               OUT     SECT            ;TELL SECTOR PORT
0056 3EAC               MVI     A,0ACH          ;GET WRITE COMMAND
0058 D3F8               OUT     DCOM            ;ISSUE IT
005A DBFC       WLOOP:  IN      WAIT            ;WAIT FOR DRQ OR INTRQ
005C B7                 ORA     A               ;SET FLAGS FOR OPERATION
005D F26700             JP      WDONE           ;JUMP WHEN INTRQ
0060 7E                 MOV     A,M             ;GET DATA FROM BUFFER
0061 D3FB               OUT     DDATA           ;PUT IT TO DISK
0063 23                 INX     H               ;BUMP BUFFER POINTER
0064 C35A00             JMP     WLOOP           ;LOOP FOR MORE DATA
0067 DBF8       WDONE:  IN      DSTAT           ;CHECK DISK STATUS
0069 E6FD               ANI     0FDH            ;MASK OFF NON ERROR BITS
006B 327100             STA     STATW           ;SAVE STATUS BITS
006E C36E00     WJMP:   JMP     WJMP            ;HARD LOOP WHEN DONE
0071 00         STATW:  DB      0               ;SAVE STATUS BITS HERE
```

2. Port and bit explanation

The explanation for the disk controller ports are covered in the 1793 data sheet and will not be covered here. The extended ports FC and FD Hex will be explained.

An input from port FC Hex is a combination hardware-software port which allows the disk controller to stall the CPU with a wait state to allow the disk controller chip time to access the data bus. This is generated by the gating of DRQ and INTRQ from the floppy chip onto either the XRDY or PRDY lines of the bus. Bit 7 of port FC is also used in the software during programmed data transfers to tell the software read/write and seek routines when an interrupt from the floppy chip has occurred. When this bit is a '1' an interrupt has occurred, and the status port of the 1793 must be read to clear it back to a '0'.

An output to port FC Hex is also the drive select, density select, and side select port. A break down of the port is as follows:

```
LSB  (bit 0)  x      not used
 ^
 |   (bit 1)  x      not used
 |
 |   (bit 2)  x      not used
 |
 |   (bit 3)  1/0    0 = single density, 1 = double density
 |
 |   (bit 4)  1/0    binary value for drive select  |
 |                                                  } 4 drives max
 |   (bit 5)  1/0    binary value for drive select  |
 |
 |   (bit 6)  1/0    0 = side 0, 1 = side 1 (side select)
 v
MSB  (bit 7)  x      not used
```

An input from port FD Hex is the software port for checking the INTRQ of the floppy chip while running under DMA operation. This port polls bit 7 of this port looking for a low (0), which tells the CPU that the DMA operation is complete. A one (1) means that the DMA is busy. All the rest of the bits in this port are not used.

An output to port FD hex may be used to change the extended addressing bits on A16 - A23 during a DMA read or write operation. This port is an latched 8 bit port and is enabled on to the S-100 bus only during DMA read or write operations. The bits which are placed into the latch, (U68), should be written only when the DMA controller is in-active, (not doing disk transfers). A typical example might be:

```
        MVI     A,1             ;select bank # 1
        OUT     0FDH            ;set extended port latch
```

```
        .
dma operation           ;transfer to/from new bank now
        .
        .               ;dma operation complete
        .
MVI     A,0             ;select bank # 0
OUT     0FDH            ;set extended port latch
        .
    etc
```

TROUBLE-SHOOTING

This section of the manual is to help you trouble-shoot the interface in case you are having problems.

1. Interface between computer cards.

Compare the section on the IEEE S-100 pin functions (section 10), to the pin function list in your cpu manual, to find out if there are any conflicts with your computer and the new bus specification. If there are, you should make any necessary corrections for compatibility.

2. Compatible interfaces

Review the section on S-100 compatible interfaces (section 11). The computer cards listed in section 11 only represents those products that we here at Tarbell Electronics have tested ourselves, and in no way defines any not in this list as not working with out interface. We would like to encourge our customers to send in any information with regard to other manufactures products that do or 'do not' work with our interface. If they don't work, maybe a reason as to why could be sent along also. Also, some Z80 cpu cards will not boot up correctly at 4Mhz with our board. We have found that in some cases cutting the phase 1 line (25) of the bus on the controller card may help.

3. Jumper selections

Review the section on jumper selection. If you are going to be running our software, then you must select the address jumper from the table in section 6 for the address range of E0 - FD hex. If you are going to use the on-board bootstrap prom, you "MUST" use the phantom line (pin 67) to disable your first memory card (addressed at 0000 hex). If you are going to use your own bootstrap program, then you must defeat our on-board bootstrap prom. If you have a revision B or below, you can turn off the on-board bootstrap by pulling out U35 pin 5 from it's socket, and then ground U33 pin 13 to U33 pin 7. For revision C and above, follow the instructions listed in the jumper options section.

4. XRDY or PRDY line

If you are getting lost data errors, besure to check which line you are using for the processor wait line. This is important during a cold start load, as the on-board prom bootstrap uses this line during the booting of the system. If you are using the wrong line, you will more than likely get lost data errors. If you are not sure which line to use, review the section on jumper options (section 6).

5. Disk Problems

Be sure that the disk you are trying to read has the correct format on it. It must be an IBM soft sector disk, 128 bytes/sector. Most disks shipped from the manufacturer that claim to be soft sector, are. But if you have reformatted the disk with the wrong format program, then you will have trouble reading it on this interface. If

you have any questions about this, review the documentation that is supplied with the interface. I can not over stress this point.

6. Drives

This interface is Shugart compatible only. That means drives which comply with the Shugart pin functions will more than likely work with no probblems. If you do have problems, consult the OEM drive manual or the factory for information. The drives that have been tested here at Tarbell Electronics are the Siemens, Shugart, and Persci drives. Also, be sure that the drive is set up for soft sector operation. We have recieved drives from the factory, set up for hard sector in the past. So look carefully at your drives for this possibility.

7. Review

Be sure and review section 2-3 in the front of this manual very carefully, as it can not be over stressed enough.

8. Symptoms vs Possible causes

This table is a list of possible troubles with possible causes to look at.

Symptom	Possible cause
1. Won't boot.....	Check pin 67. Must use Phantom line on first memory card. Make sure jump enables to system proms is defeated. Check for disk with correct format. Check C17, may have to change the value of this capacitor as outlined in section 2-3 of this manual. Check disk drive power supply lines for all voltage return lines tied to one commen place at power supply. Is there an operating system on the disk you are trying to boot from?
2. Won't run DMA	Check IEEE standard for compatibility with memory cards, cpu, and i/o cards in your system. If you are using a dynamic memory are there any problems with refreshing and control lines necessary to initiate the refreshing signals and our interface? Check for slow memory chips, e.g. old 2102's. Check our compatibility list.
3. Double density errors .	Are you using a good certified double denstiy disk? Have you adjusted the pre-comp settings for your drive using the DFRAND.COM program? Is your drive rated for double denstiy operation?

4. Won't run at all	Check voltage regulator on interface for correct voltage of +5 volts. Are any changes required to the board in the way of corrections to mistakes on the board? If not a factory assembled unit, are the changes on correctly?

DISK DRIVE SETUP

This interface is designed for Shugart compatiable drives. This includes Siemens drives also. Jumpers and power requirements for both drives are listed below.

Power requirements:

Shugart and Siemens

DC Power		AC power	
Pin 1	+24 volts DC	Pin 1	110 volts AC
Pin 2	+24 volt return	Pin 2	frame ground
Pin 3	- 5 volt return	Pin 3	110 volts AC
Pin 4	- 5 volts DC		
Pin 5	+ 5 volts DC		
Pin 6	+ 5 volt return		

Be sure all return lines are connected solidly together at the power supply end. If they are not, you may experience actual disk data errors.

Shugart Drive Jumpers

The following jumpers should be installed on each drive used:

Drive 0 (A)	Drive 1 (B)	Drive 2 (C)	Drive 3 (D)
A	A	A	A
B	B	B	B
C	C	C	C
Y	Y	Y	Y
T2	T2	T2	T2
DS	DS	DS	DS
800 (not 801)	800	800	800
DS1	DS2	DS3	DS4
T1			
T3			
T4			
T5			
T6			

Note : Some drives may have a jumper installed at X. If so, remove it.

DISK DRIVE SETUP

Siemens -------

Drive select:

Drive A	Drive B	Drive C	Drive d
Radial Sel 0	Radial Sel 1	Radial Sel 2	Radial Sel 3

Note :
Some drives may come with Radial Sel 0 etched on the board. You will have to cut this etch if you wish to use it for a drive other than Drive A.
If you are using more tan one drive, you must remove all the terminating resistor packs but the last one in the daisy chain.
Be sure that the drive is jumpered for SOFT SECTOR options.
If you have any doubts, consult the OEM manual for your drive.
Siemens model FDD 100-8D drives may come from the manufacture with jumper G installed. You must change this jumper to location H for proper operation with our interface.

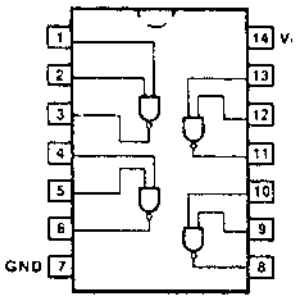
Persci drives

Changes are required to the Persci drive to make it look like a Shugart compatible drive. These changes are listed in the Jumper section of this manual.

54/7400
54H/74H00
54S/74S00
54LS/74LS00

QUAD 2-INPUT NAND GATE

CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7400PC, 74H00PC 74LS00PC, 74S00PC		9A
Ceramic DIP (D)	A	7400DC, 74H00DC 74LS00DC, 74S00DC	5400DM, 54H00DM 54LS00DM, 54S00DM	6A
Flatpak (F)	A	74LS00FC, 74S00FC	54LS00FM, 54S00FM	3I
	B	7400FC, 74H00FC	5400FM, 54H00FM	

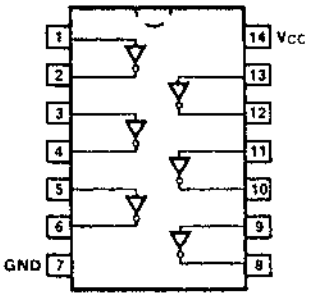
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

54/7404
54H/74H04
54S/74S04
54S/74S04A
54LS/74LS04

HEX INVERTER

CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7404PC, 74H04PC 74S04PC, 74S04APC 74LS04PC		9A
Ceramic DIP (D)	A	7404DC, 74H04DC 74S04DC, 74S04ADC 74LS04DC	5404DM, 54H04DM 54S04DM, 54S04ADM 54LS04DM	6A
Flatpak (F)	A	74S04FC, 74S04AFC 74LS04FC	54S04FM, 54S04AFM 54LS04FM	3I
	B	7404FC, 74H04FC	5404FM, 54H04FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

54/7406

HEX INVERTER BUFFER/DRIVER

(With Open-Collector High-Voltage Output)

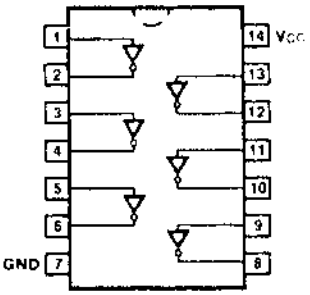
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7406PC		9A
Ceramic DIP (D)	A	7406DC	5406DM	6A
Flatpak (F)	A	7406FC	5406FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/10

CONNECTION DIAGRAM
PINOUT A



54/7407

HEX BUFFER/DRIVER

(With Open-Collector High-Voltage Output)

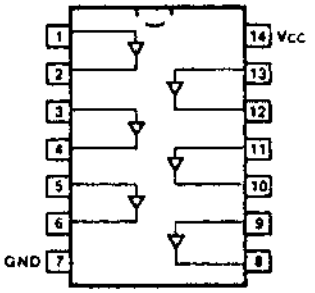
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7407PC		9A
Ceramic DIP (D)	A	7407DC	5407DM	6A
Flatpak (F)	A	7407FC	5407FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW
Inputs	1.0/1.0
Outputs	OC**/10

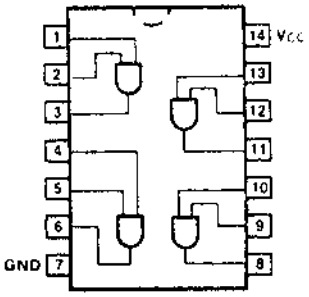
CONNECTION DIAGRAM
PINOUT A



54/7408
54H/74H08
54S/74S08
54LS/74LS08

QUAD 2-INPUT AND GATE

CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7408PC, 74H08PC 74S08PC, 74LS08PC		9A
Ceramic DIP (D)	A	7408DC, 74H08DC 74S08DC, 74LS08DC	5408DM, 54H08DM 54S08DM, 54LS08DM	6A
Flatpak (F)	A	7408FC, 74S08FC 74LS08FC	5408FM, 54S08FM 54LS08FM	3I
	B	74H08FC	54H08FM	

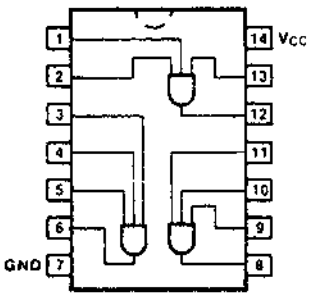
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

54/7411
54H/74H11
54S/74S11
54LS/74LS11

TRIPLE 3-INPUT AND GATE

CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7411PC, 74H11PC 74S11PC, 74LS11PC		9A
Ceramic DIP (D)	A	7411DC, 74H11DC 74S11DC, 74LS11DC	5411DM, 54H11DM 54S11DM, 54LS11DM	6A
Flatpak (F)	A	74S11FC, 74LS11FC	54S11FM, 54LS11FM	3I
	B	7411FC, 74H11FC	5411FM, 54H11FM	

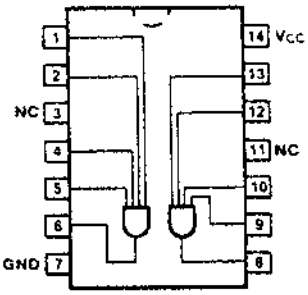
INPUT LOADING/FAN-OUT: See Section 3 for U.L definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	25/12.5	10/5.0 (2.5)

54/7421
54H/74H21
54LS/74LS21

DUAL 4-INPUT POSITIVE AND GATE

CONNECTION DIAGRAMS
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7421PC, 74H21PC 74LS21PC		9A
Ceramic DIP (D)	A	7421DC, 74H21DC 74LS21DC	5421DM, 54H21DM 54LS21DM	6A
Flatpak (F)	A	7421FC, 74LS21FC	5421FM, 54LS21FM	3I
	B	74H21FC	54H21FM	

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74H (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	12.5/12.5	10/5.0 (2.5)

54/7432
54S/74S32
54LS/74LS32

QUAD 2-INPUT OR GATE

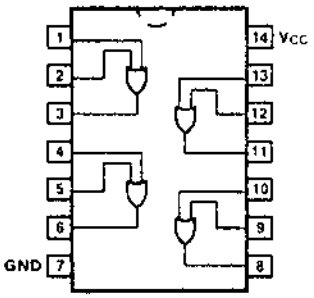
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7432PC, 74S32PC 74LS32PC		9A
Ceramic DIP (D)	A	7432DC, 74S32DC 74LS32DC	5432DM, 54S32DM 54LS32DM	6A
Flatpak (F)	A	7432FC, 74S32FC 74LS32FC	5432FM, 54S32FM 54LS32FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	20/10	25/12.5	10/5.0 (2.5)

CONNECTION DIAGRAM
PINOUT A



54/7438
54LS/74LS38

QUAD 2-INPUT NAND BUFFER
(With Open-Collector Output)

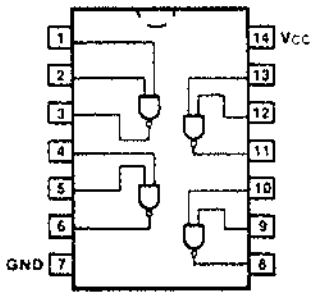
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0° C to +70° C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55° C to +125° C	PKG TYPE
Plastic DIP (P)	A	7438PC, 74LS38PC		9A
Ceramic DIP (D)	A	7438DC, 74LS38DC	5438DM, 54LS38DM	6A
Flatpak (F)	A	7438FC, 74LS38FC	5438FM, 54LS38FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	OC**/30	OC**/15 (7.5)

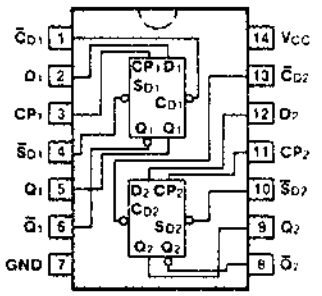
CONNECTION DIAGRAM
PINOUT A



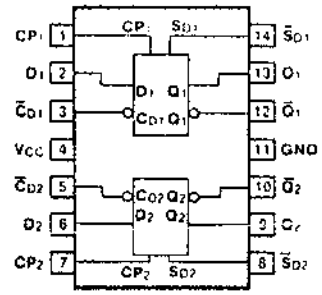
54/7474
54H/74H74
54S/74S74
54LS/74LS74

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

CONNECTION DIAGRAMS
PINOUT A



PINOUT B



DESCRIPTION — The '74 devices are dual D-type flip-flops with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

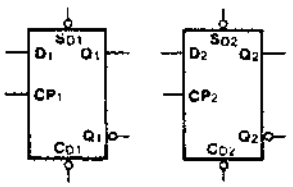
TRUTH TABLE
(Each Half)

INPUT	OUTPUTS	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Asynchronous inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14 (4)
GND = Pin 7 (11)

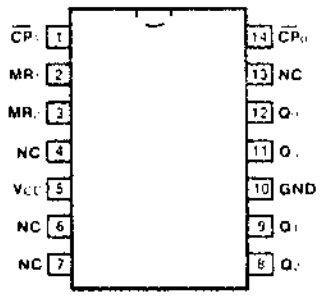
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP P	A	7474PC, 74H74PC 74S74PC, 74LS74PC		9A
Ceramic DIP (D)	A	7474DC, 74H74DC 74S74DC, 74LS74DC	5474DM, 54H74DM 54S74DM, 54LS74DM	6A
Flatpak (F)	A	74S74FC, 74LS74FC	54S74FM, 54LS74FM	3I
	B	7474FC, 74H74FC	5474FM, 54H74FM	

54/7493A
54LS/74LS93

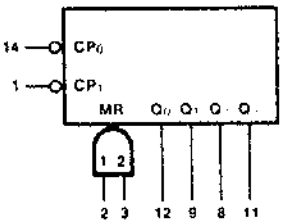
DIVIDE-BY-SIXTEEN COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '93 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-eight. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state.

LOGIC SYMBOL



VCC = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7493APC, 74LS93PC		9A
Ceramic DIP (D)	A	7493ADC, 74LS93DC	5493ADM, 54LS93DM	6A
Flatpak (F)	A	7493AFC, 74LS93FC	5493AFM, 54LS93FM	3I

7493

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level

TRUTH TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 connected to $\overline{CP}_1$.

54S/74S113
54LS/74LS113

DUAL JK EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The '113 offers individual J, K, Set and Clock inputs. When the clock goes HIGH the inputs are enabled and data may be entered. The logic level of the J and K inputs may be changed when the clock pulse is HIGH and the bistable will perform according to the Truth Table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the falling edge of the clock pulse.

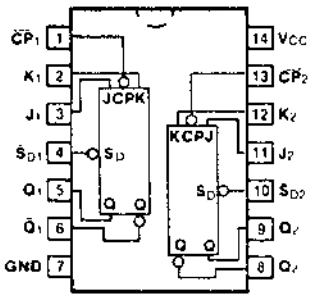
TRUTH TABLE

INPUTS		OUTPUT
@ t_n		@ t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

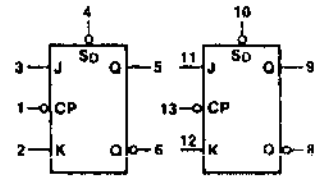
Asynchronous Input:
LOW input to $\overline{S}_D$ sets Q to HIGH level
Set is independent of clock

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

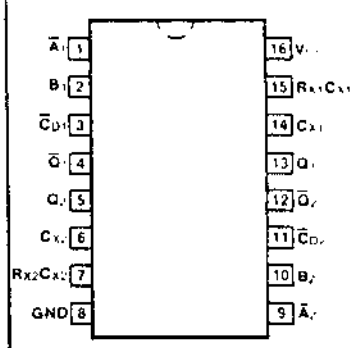
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE: V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S113PC, 74LS113PC		9A
Ceramic DIP (D)	A	74S113DC, 74LS113DC	54S113DM, 54LS113DM	6A
Flatpak (F)	A	74S113FC, 74LS113FC	54S113FM, 54LS113FM	3I

54/74123

DUAL RETRIGGERABLE RESETTABLE MULTIVIBRATOR

CONNECTION DIAGRAM
PINOUT A

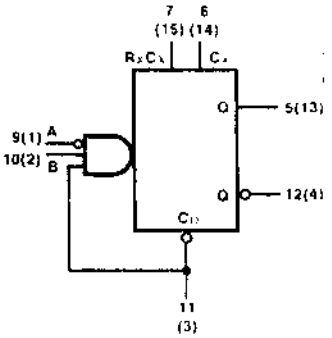


DESCRIPTION — Each half of the '123 features retriggerable capability, complementary dc level triggering and overriding Direct Clear. When a circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per the Truth Table) will cause the delay period to start again, without disturbing the outputs. By repeating this process, the output pulse period (Q HIGH, $\overline{Q}$ LOW) can be made as long as desired. Alternatively, a delay period can be terminated at any time by a LOW signal on $\overline{C}_D$, which also inhibits triggering. An internal connection from $\overline{C}_D$ to the input gate makes it possible to trigger the circuit by a positive-going signal on $\overline{C}_D$, as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows.

$$t_w = 0.28\ R_X C_X\ (1.0 + 0.7/R_X)$$

Where t_w is in ns, R_X is in kΩ and C_X is in pF.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74123PC		9B
Ceramic DIP (D)	A	74123DC	54123DM	6B
Flatpak (F)	A	74123FC	54123FM	4L

54/74125
54LS/74LS125A

QUAD BUS BUFFER GATE

(With 3-State Outputs)

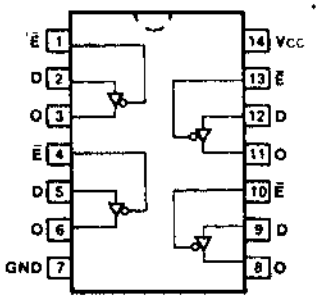
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74125PC, 74LS125APC		9A
Ceramic DIP (D)	A	74125DC, 74LS125ADC	54125DM, 54LS125ADM	6A
Flatpak (F)	A	74125FC, 74LS125AFC	54125FM, 54LS125AFM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	130/10 (50)	65/15 (25)/(7.5)

CONNECTION DIAGRAM
PINOUT A



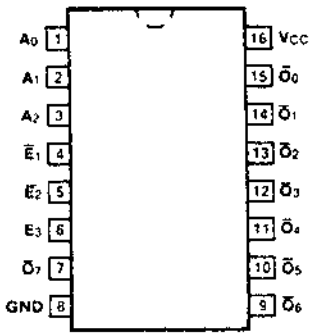
TRUTH TABLE

INPUTS		OUTPUT
Ē	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

54S/74S138
54LS/74LS138
1-OF-8 DECODER/DEMULTIPLEXER

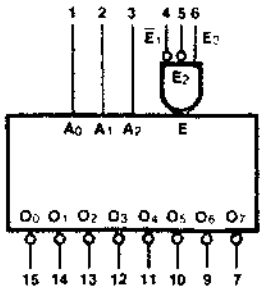
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '138 is a high speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three '138 devices or to a 1-of-32 decoder using four '138 devices and one inverter. The '138 is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **DEMULTIPLEXING CAPABILITY**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S138PC, 74LS138PC		9B
Ceramic DIP (D)	A	74S138DC, 74LS138DC	54S138DM, 54LS138DM	6B
Flatpak (F)	A	74S138FC, 74LS138FC	54S138FM, 54LS138FM	4L

74LS138

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

54/74145

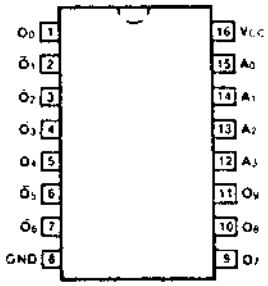
1-OF-10 DECODER/DRIVER

(With Open-Collector Outputs)

DESCRIPTION -- The '145 decoder/drivers are designed to accept BCD inputs and provide appropriate outputs to drive 7-segment numerical displays. All outputs remain OFF for all invalid binary input conditions. These devices are designed for use as indicator/relay drivers or as open-collector logic circuit drivers. Each of the high breakdown (15 V) output transistors will sink up to 80 mA of current.

- **OPEN-COLLECTOR OUTPUTS**
- **80 mA CURRENT SINKING**
- **15 V GUARANTEED BREAKDOWN**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

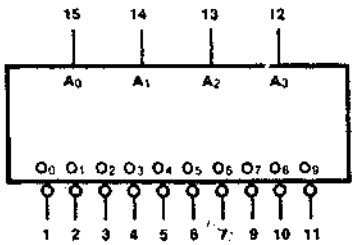
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74145PC		9B
Ceramic DIP (D)	A	74145DC	54145DM	7B
Flatpak (F)	A	74145FC	54145FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
A_0 — A_3	BCD Inputs	1.0/1.0
$\overline{O}_0$ — $\overline{O}_9$	Outputs (Active LOW)	OC*/12.5

*OC = Open Collector

LOGIC SYMBOL



74145

TRUTH TABLE

INPUTS				OUTPUTS									
A_0	A_1	A_2	A_3	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$	$\bar{O}_4$	$\bar{O}_5$	$\bar{O}_6$	$\bar{O}_7$	$\bar{O}_8$	$\bar{O}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

54/74161 • 54LS/74LS161
54/74163 • 54LS/74LS163

SYNCHRONOUS PRESETTABLE BINARY COUNTERS

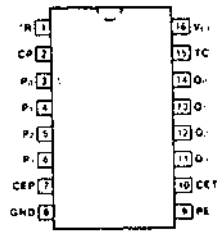
DESCRIPTION — The '161 and '163 are high speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The '161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The '163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. For functional description and detail specifications please refer to the '160 data sheet. For S-TTL and LP-TTL versions please see the 9316 data sheet.

- **SYNCHRONOUS COUNTING AND LOADING**
- **HIGH SPEED SYNCHRONOUS EXPANSION**
- **LS VERSIONS FULLY EDGE TRIGGERED**

ORDERING CODE: See Section 9

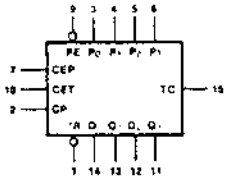
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74161PC, 74LS161PC 74163PC, 74LS163PC		9B
Ceramic DIP (D)	A	74161DC, 74LS161DC 74163DC, 74LS163DC	54161DM, 54LS161DM 54163DM, 54LS163DM	7B
Flatpak (F)	A	74161FC, 74LS161FC 74163FC, 74LS163FC	54161FM, 54LS161FM 54163FM, 54LS163FM	4L

CONNECTION DIAGRAM
PINOUT A



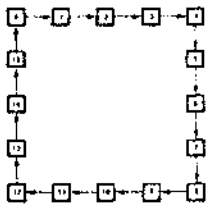
*$\overline{MR}$ for '161
*$\overline{SR}$ for '163

LOGIC SYMBOL



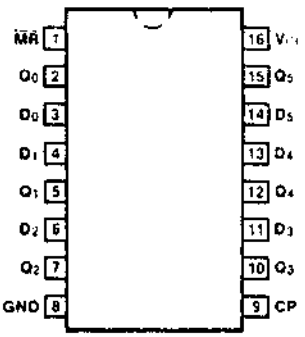
*$\overline{MR}$ for '161 V_{CC} = Pin 16
*$\overline{SR}$ for '163 Gnd = Pin 8

STATE DIAGRAM



54/74174
54S/74S174
54LS/74LS174
HEX D FLIP-FLOP

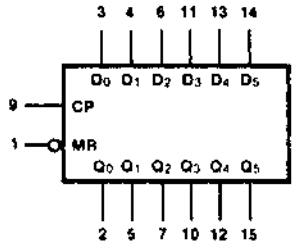
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '174 is a high speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **ASYNCHRONOUS COMMON RESET**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74174PC, 74S174PC, 74LS174PC		9B
Ceramic DIP (D)	A	74174DC, 74S174DC, 74LS174DC	54174DM, 54S174DM, 54LS174DM	6B
Flatpak (F)	A	74174FC, 74S174FC, 74LS174FC	54174FM, 54S174FM, 54LS174FM	4L

TRUTH TABLE

INPUTS	OUTPUTS
@ t_n, $\overline{MR}$ = H	@ $t_n + t$
D_n	Q_n
H	H
L	L

t_n = Bit time before positive-going clock transition
$t_n + t$ = Bit time after positive-going clock transition
H = HIGH Voltage Level
L = LOW Voltage Level

54/74193
54LS/74LS193

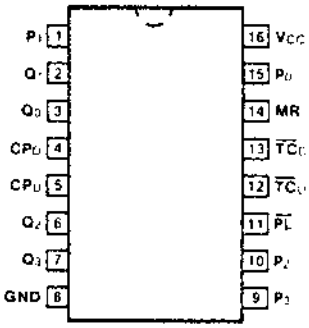
UP/DOWN BINARY COUNTER
(With Separate Up/down Clocks)

DESCRIPTION — The '193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks. For functional description and detail specifications please refer to the '192 data sheet.

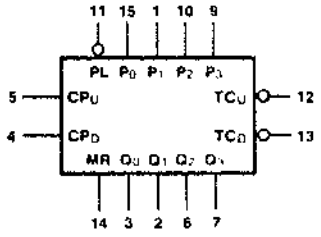
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74193PC, 74LS193PC		9B
Ceramic DIP (D)	A	74193DC, 74LS193DC	54193DM, 54LS193DM	6B
Flatpak (F)	A	74193FC, 74LS193FC	54193FM, 54LS193FM	4L

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



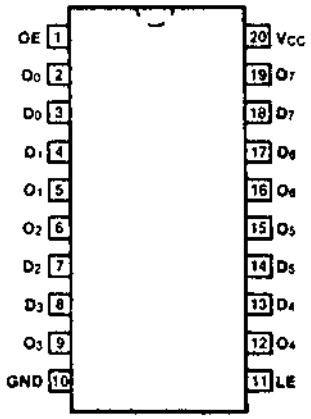
VCC = Pin 16
GND = Pin 8

54LS/74LS373

OCTAL TRANSPARENT LATCH

(With 3-State Outputs)

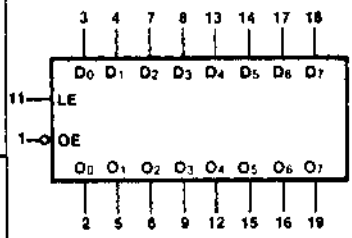
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**

LOGIC SYMBOL

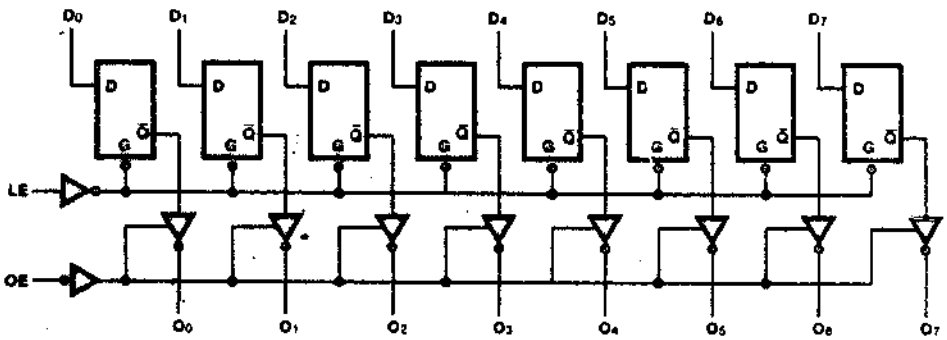


VCC = Pin 20
GND = Pin 10

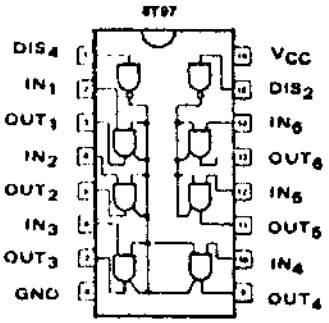
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS373PC		9Z
Ceramic DIP (D)	A	74LS373DC	54LS373DM	4E
Flatpak (F)	A	74LS373FC	54LS373FM	4F

LOGIC DIAGRAM



8T97 HEX TRI-STATE INVERTERS



INPUTS		OUTPUT
DIS	IN	OUT
H	X	Hi-Z
L	H	H
L	L	L

7-1-2

82S123 256-BIT BIPOLAR TRI-STATE PROGRAMMABLE ROM

DESCRIPTION

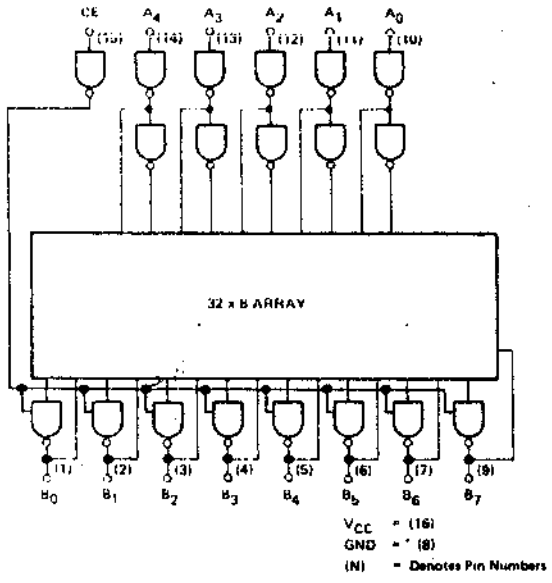
The 82S23 (open Collector Outputs) and the 82S123 (Tristate Outputs) are Bipolar 256 Bit Read Only Memories organized as 32 words by 8 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the simple fusing procedure given in this data sheet. A chip enable line is provided and the outputs are bare collector or Tristate to allow for memory expansion capability.

The 82S23 and 82S123 are fully TTL compatible and include on-the-chip decoding. Typical access time is 35 nS.

FEATURES

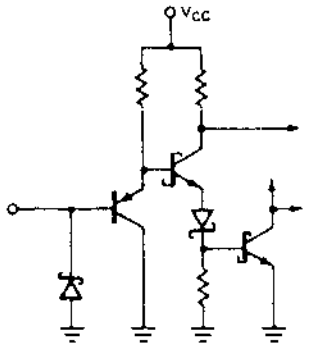
- PNP INPUTS
- BUFFERED ADDRESS LINES
- ON THE CHIP DECODING
- A CHIP ENABLE LINE
- OPEN COLLECTOR OR TRISTATE OUTPUTS
- DIODE PROTECTED INPUTS
- NO SEPARATE "FUSING" PINS
- BOARD PROGRAMMABLE

LOGIC DIAGRAM

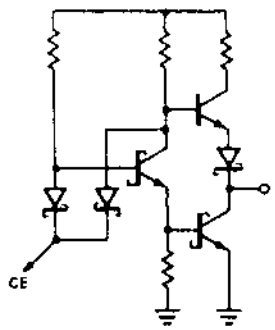


INPUT/OUTPUT SCHEMATIC DIAGRAMS

INPUT SCHEMATIC



OUTPUT SCHEMATIC



82S123

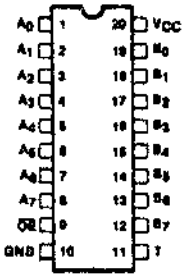
8208 /8287
8-BIT PARALLEL BIDIRECTIONAL BUS DRIVERS

- **Data Bus Buffer Driver for MCS-86™, MCS-80™, MCS-85™, and MCS-48™**
- **High Output Drive Capability for Driving System Data Bus**
- **Fully Parallel 8-Bit Transceivers**
- **3-State Outputs**
- **20-Pin Package with 0.3" Center**
- **No Output Low Noise when Entering or Leaving High Impedance State**

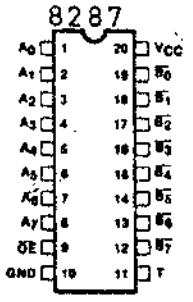
The 8208 and 8287 are 8-bit bipolar transceivers with 3-state outputs. The 8287 inverts the input data at its outputs while the 8208 does not. Thus, a wide variety of applications for buffering in microcomputer systems can be met.

PIN CONFIGURATIONS

8208



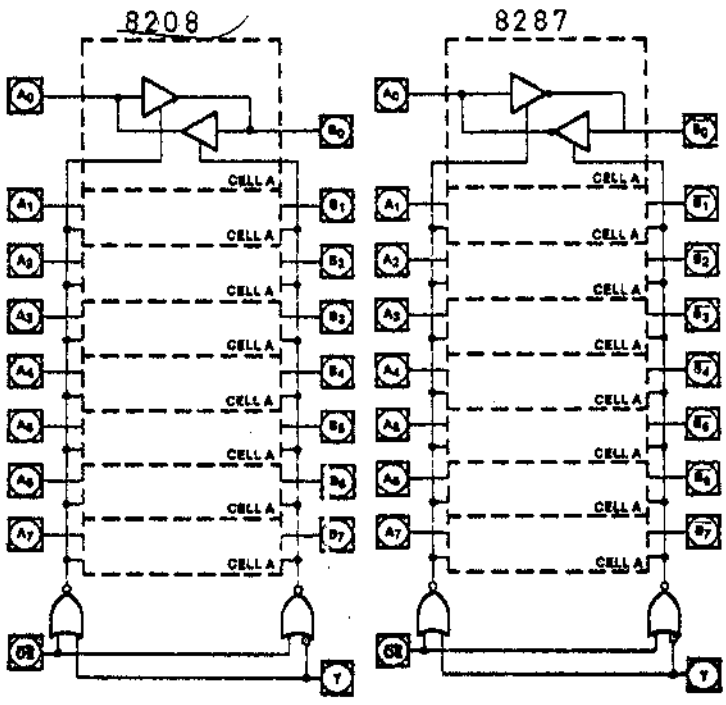
8287



PIN NAMES

A_0-A_7	LOCAL BUS DATA
B_0-B_7	SYSTEM BUS DATA
$\overline{OE}$	OUTPUT ENABLE
T	TRANSMIT

LOGIC DIAGRAMS



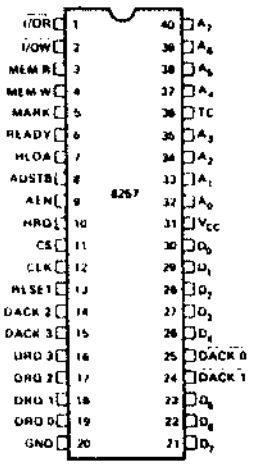
8257/8257-5
PROGRAMMABLE DMA CONTROLLER

- MCS-85™ Compatible 8257-5
- 4-Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Single TTL Clock
- Single +5V Supply
- Auto Load Mode

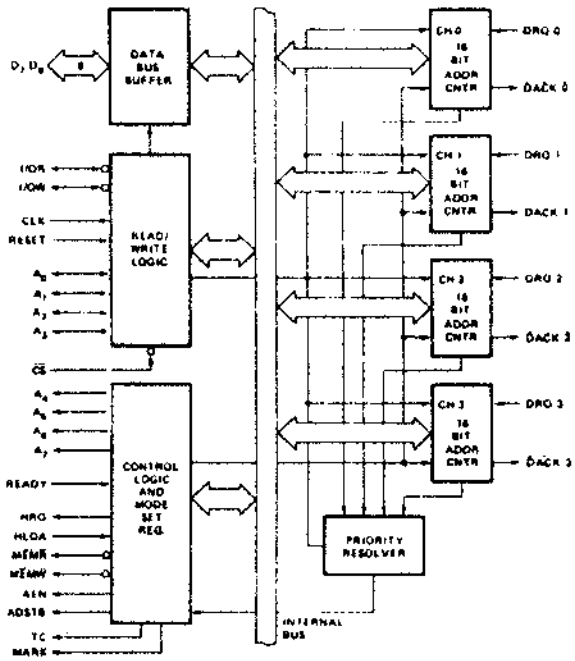
The Intel® 8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus is accomplished via the CPU's hold function. The 8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers. The 8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

MCS-80/85

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_7-D_0	DATA BUS
A_7-A_0	ADDRESS BUS
I/OR	I/O READ
I/OW	I/O WRITE
MEMR	MEMORY READ
MEMW	MEMORY WRITE
CLK	CLOCK INPUT
RESET	RESET INPUT
READY	READY
HRQ	HOLD REQUEST (TO 8080A)
HLDA	HOLD ACKNOWLEDGE (FROM 8080A)

AEN	ADDRESS ENABLE
ADSTB	ADDRESS STROBE
TC	TERMINAL COUNT
MARK	MODULO 128 MARK
DRQ_3-DRQ_0	DMA REQUEST INPUT
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA ACKNOWLEDGE OUT
$\overline{CS}$	CHIP SELECT
V_{CC}	+5 VOLTS
GND	GROUND

FUNCTIONAL DESCRIPTION

General

The 8257 is a programmable, Direct Memory Access (DMA) device which, when coupled with a single Intel® 8212 I/O port device, provides a complete four-channel DMA controller for use in Intel® microcomputer systems. After being initialized by software, the 8257 can transfer a block of data, containing up to 16,384 bytes, between memory and a peripheral device directly, without further intervention required of the CPU. Upon receiving a DMA transfer request from an enabled peripheral, the 8257:

1. Acquires control of the system bus.
2. Acknowledges that requesting peripheral which is connected to the highest priority channel.
3. Outputs the least significant eight bits of the memory address onto system address lines A_0-A_7, outputs the most significant eight bits of the memory address to the 8212 I/O port via the data bus (the 8212 places these address bits on lines A_8-A_{15}), and
4. Generates the appropriate memory and I/O read/write control signals that cause the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

The 8257 will retain control of the system bus and repeat the transfer sequence, as long as a peripheral maintains its DMA request. Thus, the 8257 can transfer a block of data to/from a high speed peripheral (e.g., a sector of data on a floppy disk) in a single "burst". When the specified number of data bytes have been transferred, the 8257 activates its Terminal Count (TC) output, informing the CPU that the operation is complete.

The 8257 offers three different modes of operation: (1) DMA read, which causes data to be transferred from memory to a peripheral; (2) DMA write, which causes data to be transferred from a peripheral to memory; and (3) DMA verify, which does not actually involve the transfer of data. When an 8257 channel is in the DMA verify mode, it will respond the same as described for transfer operations, except that no memory or I/O read/write control signals will be generated, thus preventing the transfer of data. The 8257, however, will gain control of the system bus and will acknowledge the peripheral's DMA request for each DMA cycle. The peripheral can use these acknowledge signals to enable an internal access of each byte of a data block in order to execute some verification procedure, such as the accumulation of a CRC (Cyclic Redundancy Code) checkword. For example, a block of DMA verify cycles might follow a block of DMA read cycles (memory to peripheral) to allow the peripheral to verify its newly acquired data.

Block Diagram Description

1. DMA Channels

The 8257 provides four separate DMA channels (labeled CH-0 to CH-3). Each channel includes two sixteen-bit registers: (1) a DMA address register, and (2) a terminal count register. Both registers must be initialized before a channel is enabled. The DMA address register is loaded with the address of the first memory location to be accessed. The value loaded into the low-order 14-bits of the terminal count register specifies the number of DMA cycles minus one before the Terminal Count (TC) output is activated. For instance, a terminal count of 0 would cause the TC output to be active in the first DMA cycle for that channel. In general, if N = the number of desired DMA cycles, load the value N-1 into the low-order 14-bits of the terminal count register. The most significant two bits of the terminal count register specify the type of DMA operation for that channel.

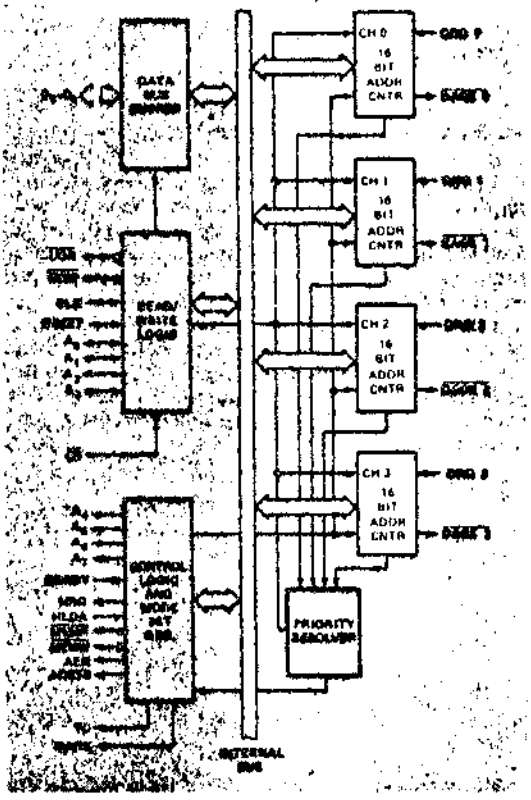


Figure 1. 8257 Block Diagram Showing DMA Channels

These two bits are not modified during a DMA cycle, but can be changed between DMA blocks.

Each channel accepts a DMA Request (DRQn) input and provides a DMA Acknowledge (DACKn) output.

(DRQ 0-DRQ 3)

DMA Request. These are individual asynchronous channel request inputs used by the peripherals to obtain a DMA cycle. If not in the rotating priority mode then DRQ 0 has the highest priority and DRQ 3 has the lowest. A request can be generated by raising the request line and holding it high until DMA acknowledge. For multiple DMA cycles (Burst Mode) the request line is held high until the DMA acknowledge of the last cycle arrives.

($\overline{DACK}$ 0 - $\overline{DACK}$ 3)

DMA Acknowledge: An active low level on the acknowledge output informs the peripheral connected to that channel that it has been selected for a DMA cycle. The $\overline{DACK}$ output acts as a "chip select" for the peripheral device requesting service. This line goes active (low) and inactive (high) once for each byte transferred even if a burst of data is being transferred.

2. Data Bus Buffer

This three-state, bi-directional, eight bit buffer interfaces the 8257 to the system data bus.

(D_0-D_7)

Data Bus Lines: These are bi-directional three-state lines. When the 8257 is being programmed by the CPU, eight-bits of data for a DMA address register, a terminal count register or the Mode Set register are received on the data bus. When the CPU reads a DMA address register, a terminal count register or the Status register, the data is sent to the CPU over the data bus. During DMA cycles (when the 8257 is the bus master), the 8257 will output the most significant eight-bits of the memory address (from one of the DMA address registers) to the 8212 latch via the data bus. These address bits will be transferred at the beginning of the DMA cycle; the bus will then be released to handle the memory data transfer during the balance of the DMA cycle.

BIT 15	BIT 14	TYPE OF DMA OPERATION
0	0	Verify DMA Cycle
0	1	Write DMA Cycle
1	0	Read DMA Cycle
1	1	(Illegal)

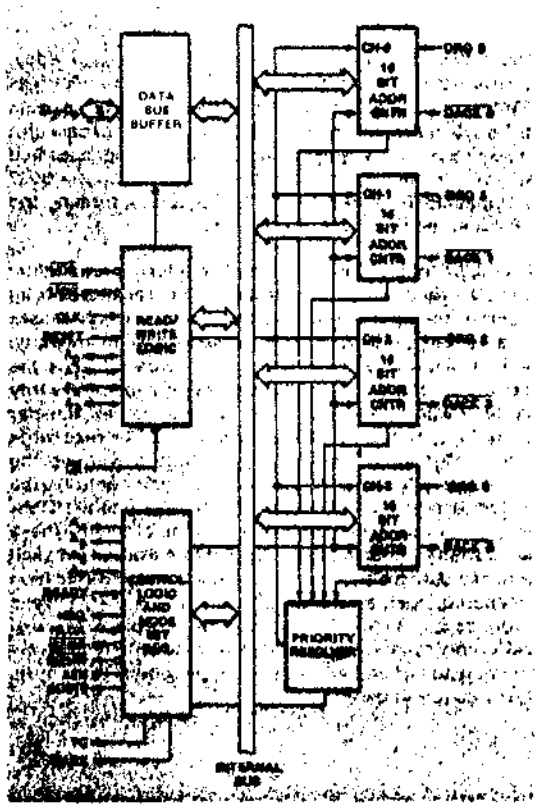


Figure 2. 8257 Block Diagram Showing Data Bus Buffer

3. Read/Write Logic

When the CPU is programming or reading one of the 8257's registers (i.e., when the 8257 is a "slave" device on the system bus), the Read/Write Logic accepts the I/O Read ($\overline{I/OR}$) or I/O Write ($\overline{I/OW}$) signal, decodes the least significant four address bits, (A_0-A_3), and either writes the contents of the data bus into the addressed register (if $\overline{I/OW}$ is true) or places the contents of the addressed register onto the data bus (if $\overline{I/OR}$ is true).

During DMA cycles (i.e., when the 8257 is the bus "master"), the Read/Write Logic generates the I/O read and memory write (DMA write cycle) or I/O Write and memory read (DMA read cycle) signals which control the data link with the peripheral that has been granted the DMA cycle.

Note that during DMA transfers Non-DMA I/O devices should be de-selected (disabled) using "AEN" signal to inhibit I/O device decoding of the memory address as an erroneous device address.

($\overline{I/OR}$)

I/O Read: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the 8-bit status register or the upper/lower byte of a 16-bit DMA address register or terminal count register to be read. In the "master" mode, $\overline{I/OR}$ is a control output which is used to access data from a peripheral during the DMA write cycle.

($\overline{I/OW}$)

I/O Write: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the contents of the data bus to be loaded into the 8-bit mode set register or the upper/lower byte of a 16-bit DMA address register or terminal count register. In the "master" mode, $\overline{I/OW}$ is a control output which allows data to be output to a peripheral during a DMA read cycle.

(CLK)

Clock Input: Generally from an Intel® 8224 Clock Generator device. (ϕ2 TTL) or Intel® 8085A CLK output.

(RESET)

Reset: An asynchronous input (generally from an 8224 or 8085 device) which disables all DMA channels by clearing the mode register and 3-states all control lines.

(A_0-A_3)

Address Lines: These least significant four address lines are bi-directional. In the "slave" mode they are inputs which select one of the registers to be read or programmed. In the "master" mode, they are outputs which constitute the least significant four bits of the 16-bit memory address generated by the 8257.

($\overline{CS}$)

Chip Select: An active-low input which enables the I/O Read or I/O Write input when the 8257 is being read or programmed in the "slave" mode. In the "master" mode, $\overline{CS}$ is automatically disabled to prevent the chip from selecting itself while performing the DMA function.

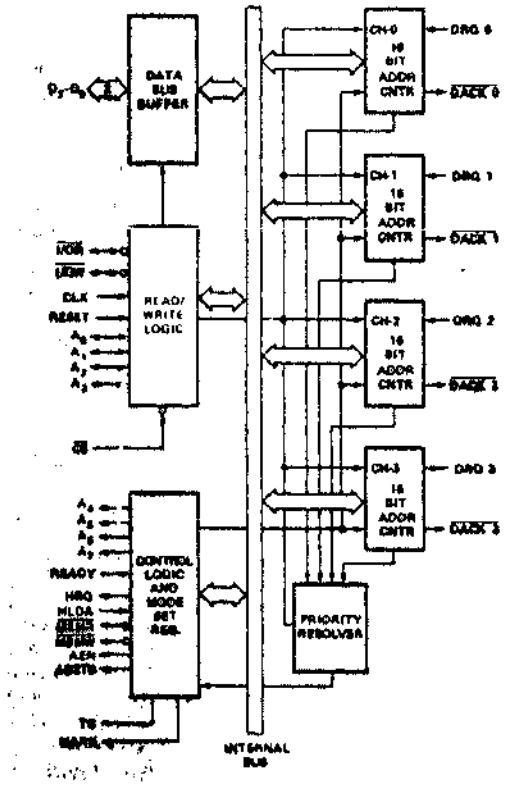


Figure 5. 8257 Block Diagram Showing Read/Write Logic Function

4. Control Logic

This block controls the sequence of operations during all DMA cycles by generating the appropriate control signals and the 16-bit address that specifies the memory location to be accessed.

(A_4-A_7)

Address Lines: These four address lines are three-state outputs which constitute bits 4 through 7 of the 16-bit memory address generated by the 8257 during all DMA cycles.

(READY)

Ready: This asynchronous input is used to elongate the memory read and write cycles in the 8257 with wait states if the selected memory requires longer cycles.

(HRQ)

Hold Request: This output requests control of the system bus. In systems with only one 8257, HRQ will normally be applied to the HOLD input on the CPU.

(HLDA)

Hold Acknowledge: This input from the CPU indicates that the 8257 has acquired control of the system bus.

($\overline{MEMR}$)

Memory Read: This active-low three-state output is used to read data from the addressed memory location during DMA Read cycles.

($\overline{MEMW}$)

Memory Write: This active-low three-state output is used to write data into the addressed memory location during DMA Write cycles.

(ADSTB)

Address Strobe: This output strobes the most significant byte of the memory address into the 8212 device from the data bus.

(AEN)

Address Enable: This output is used to disable (float) the System Data Bus and the System Control Bus. It may also be used to disable (float) the System Address Bus by use of an enable on the Address Bus drivers in systems to inhibit non-DMA devices from responding during DMA cycles. It may be further used to isolate the 8257 data bus from the System Data Bus to facilitate the transfer of the 8 most significant DMA address bits over the 8257 data I/O pins without subjecting the System Data Bus to any timing constraints for the transfer. When the 8257 is used in an I/O device structure (as opposed to memory mapped), this AEN output should be used to disable the selection of an I/O device when the DMA address is on the address bus. The I/O device selection should be determined by the DMA acknowledge outputs for the 4 channels.

(TC)

Terminal Count: This output notifies the currently selected peripheral that the present DMA cycle should be the last cycle for this data block. If the TC STOP bit in the Mode Set register is set, the selected channel will be automatically disabled at the end of that DMA cycle. TC is activated when the 14-bit value in the selected channel's terminal count register equals zero. Recall that the low-order 14-bits of the terminal count register should be loaded with the values (n-1), where n = the desired number of the DMA cycles.

(MARK)

Modulo 128 Mark: This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block. Only if the total number of DMA cycles (n) is evenly divisable by 128 (and the terminal count register was loaded with n-1), will MARK occur at 128 (and each succeeding multiple of 128) cycles from the beginning of the data block.

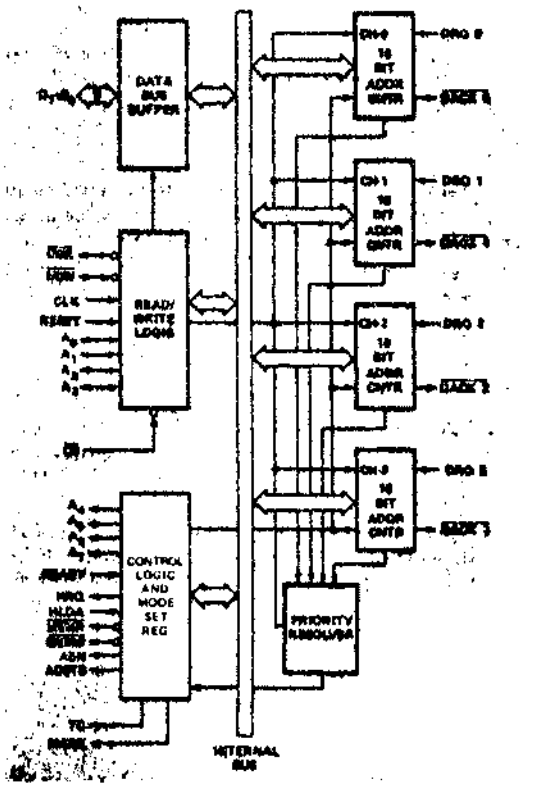
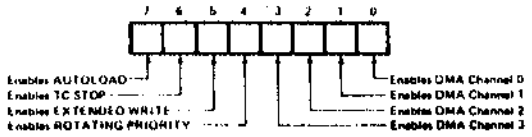


Figure 4. 8257 Block Diagram Showing Control Logic and Mode Set Register

5. Mode Set Register

When set, the various bits in the Mode Set register enable each of the four DMA channels, and allow four different options for the 8257:

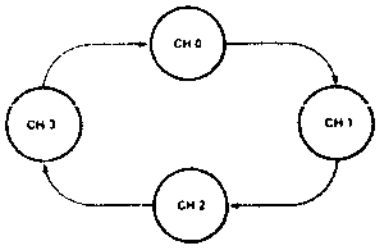


The Mode Set register is normally programmed by the CPU after the DMA address register(s) and terminal count register(s) are initialized. The Mode Set Register is cleared by the RESET input, thus disabling all options, inhibiting all channels, and preventing bus conflicts on power-up. A channel should not be left enabled unless its DMA address and terminal count registers contain valid values; otherwise, an inadvertent DMA request (DRQn) from a peripheral could initiate a DMA cycle that would destroy memory data.

The various options which can be enabled by bits in the Mode Set register are explained below:

Rotating Priority Bit 4

In the Rotating Priority Mode, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which had just been serviced will have the lowest priority.



If the ROTATING PRIORITY bit is not set (set to a zero), each DMA channel has a fixed priority. In the fixed priority mode, Channel 0 has the highest priority and Channel 3 has the lowest priority. If the ROTATING PRIORITY bit is set to a one, the priority of each channel changes after each DMA cycle (not each DMA request). Each channel moves up to the next highest priority assignment, while the channel which has just been serviced moves to the lowest priority assignment.

	CHANNEL→ JUST SERVICED	CH-0	CH-1	CH-2	CH-3
Priority → Assignments	Highest	CH-1	CH-2	CH-3	CH-0
		CH-2	CH-3	CH-0	CH-1
		CH-3	CH-0	CH-1	CH-2
	Lowest	CH-0	CH-1	CH-2	CH-3

Note that rotating priority will prevent any one channel from monopolizing the DMA mode; consecutive DMA cycles will service different channels if more than one channel is enabled and requesting service. There is no overhead penalty associated with this mode of operation. All DMA operations began with Channel 0 initially assigned to the highest priority for the first DMA cycle.

Extended Write Bit 5

If the EXTENDED WRITE bit is set, the duration of both the $\overline{\text{MEMW}}$ and $\overline{\text{I/OW}}$ signals is extended by activating them earlier in the DMA cycle. Data transfers within microcomputer systems proceed asynchronously to allow use of various types of memory and I/O devices with different access times. If a device cannot be accessed within a specific amount of time it returns a "not ready" indication to the 8257 that causes the 8257 to insert one or more wait states in its internal sequencing. Some devices are fast enough to be accessed without the use of wait states, but if they generate their READY response with the leading edge of the $\overline{\text{I/OW}}$ or $\overline{\text{MEMW}}$ signal (which generally occurs late in the transfer sequence), they would normally cause the 8257 to enter a wait state because it does not receive READY in time. For systems with these types of devices, the Extended Write option provides alternative timing for the I/O and memory write signals which allows the devices to return an early READY and prevents the unnecessary occurrence of wait states in the 8257, thus increasing system throughput.

TC Stop Bit 6

If the TC STOP bit is set, a channel is disabled (i.e., its enable bit is reset) after the Terminal Count (TC) output goes true, thus automatically preventing further DMA operation on that channel. The enable bit for that channel must be re-programmed to continue or begin another DMA operation. If the TC STOP bit is not set, the occurrence of the TC output has no effect on the channel enable bits. In this case, it is generally the responsibility of the peripheral to cease DMA requests in order to terminate a DMA operation.

Auto Load Bit 7

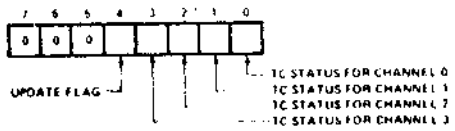
The Auto Load mode permits Channel 2 to be used for repeat block or block chaining operations, without immediate software intervention between blocks. Channel 2 registers are initialized as usual for the first data block; Channel 3 registers, however, are used to store the block re-initialization parameters (DMA starting address, terminal count and DMA transfer mode). After the first block of DMA cycles is executed by Channel 2 (i.e., after the TC output goes true), the parameters stored in the Channel 3 registers are transferred to Channel 2 during an "update" cycle. Note that the TC STOP feature, described above, has no effect on Channel 2 when the Auto Load bit is set.

If the Auto Load bit is set, the initial parameters for Channel 2 are automatically duplicated in the Channel 3 registers when Channel 2 is programmed. This permits repeat block operations to be set up with the programming of a single channel. Repeat block operations can be used in applications such as CRT refreshing. Channels 2 and 3 can still be loaded with separate values if Channel 2 is loaded before loading Channel 3. Note that in the Auto Load mode, Channel 3 is still available to the user if the Channel 3 enable bit is set, but use of this channel will change the values to be auto loaded into Channel 2 at update time. All that is necessary to use the Auto Load feature for chaining operations is to reload Channel 3 registers at the conclusion of each update cycle with the new parameters for the next data block transfer.

Each time that the 8257 enters an update cycle, the update flag in the status register is set and parameters in Channel 3 are transferred to Channel 2, non-destructively for Channel 3. The actual re-initialization of Channel 2 occurs at the beginning of the next channel 2 DMA cycle after the TC cycle. This will be the first DMA cycle of the new data block for Channel 2. The update flag is cleared at the conclusion of this DMA cycle. For chaining operations, the update flag in the status register can be monitored by the CPU to determine when the re-initialization process has been completed so that the next block parameters can be safely loaded into Channel 3.

6. Status Register

The eight-bit status register indicates which channels have reached a terminal count condition and includes the update flag described previously.



The TC status bits are set when the Terminal Count (TC) output is activated for that channel. These bits remain set until the status register is read or the 8257 is reset. The UPDATE FLAG, however, is not affected by a status register read operation. The UPDATE FLAG can be cleared by resetting the 8257, by changing to the non-auto load mode (i.e., by resetting the AUTO LOAD bit in the Mode Set register) or it can be left to clear itself at the completion of the update cycle. The purpose of the UPDATE FLAG is to prevent the CPU from inadvertently skipping a data block by overwriting a starting address or terminal count in the Channel 3 registers before those parameters are properly auto-loaded into Channel 2.

The user is cautioned against reading the TC status register and using this information to reenable channels that have not completed operation. Unless the DMA channels are inhibited a channel could reach terminal count (TC) between the status read and the mode write. DMA can be inhibited by a hardware gate on the HRQ line or by disabling channels with a mode word before reading the TC status.

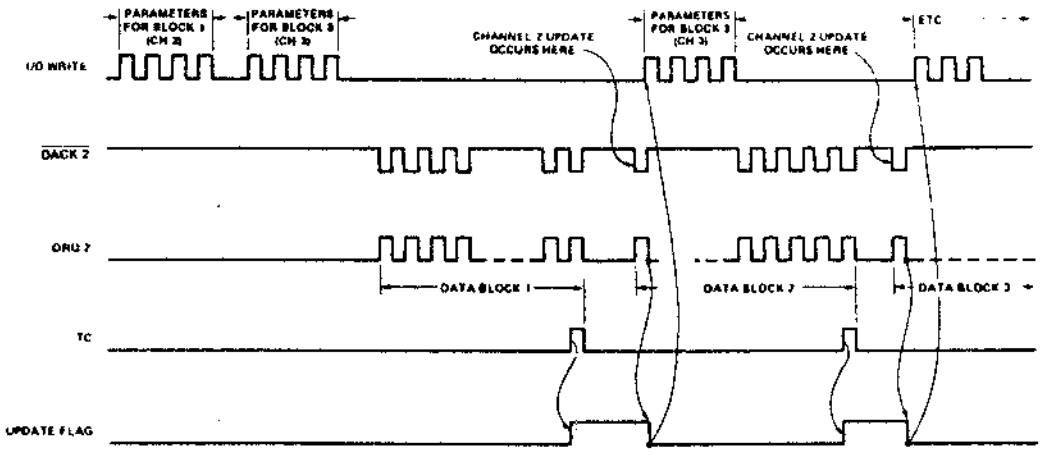


Figure 5. Autoload Timing

OPERATIONAL SUMMARY

Programming and Reading the 8257 Registers

There are four pairs of "channel registers": each pair consisting of a 16-bit DMA address register and a 16-bit terminal count register (one pair for each channel). The 8257 also includes two "general registers": one 8-bit Mode Set register and one 8-bit Status register. The registers are loaded or read when the CPU executes a write or read instruction that addresses the 8257 device and the appropriate register within the 8257. The 8228 generates the appropriate read or write control signal (generally I/OR or I/OW while the CPU places a 16-bit address on the system address bus, and either outputs the data to be written onto the system data bus or accepts the data being read from the data bus. All or some of the most significant 12 address bits A_4-A_{15} (depending on the systems memory, I/O configuration) are usually decoded to produce the chip select ($\overline{CS}$) input to the 8257. An I/O Write input (or Memory Write in memory mapped I/O configurations, described below) specifies that the addressed register is to be programmed, while an I/O Read input (or Memory Read) specifies that the addressed register is to be read. Address bit 3 specifies whether a "channel register" (A_3 = 0) or the Mode Set (program only)/Status (read only) register (A_3 = 1) is to be accessed.

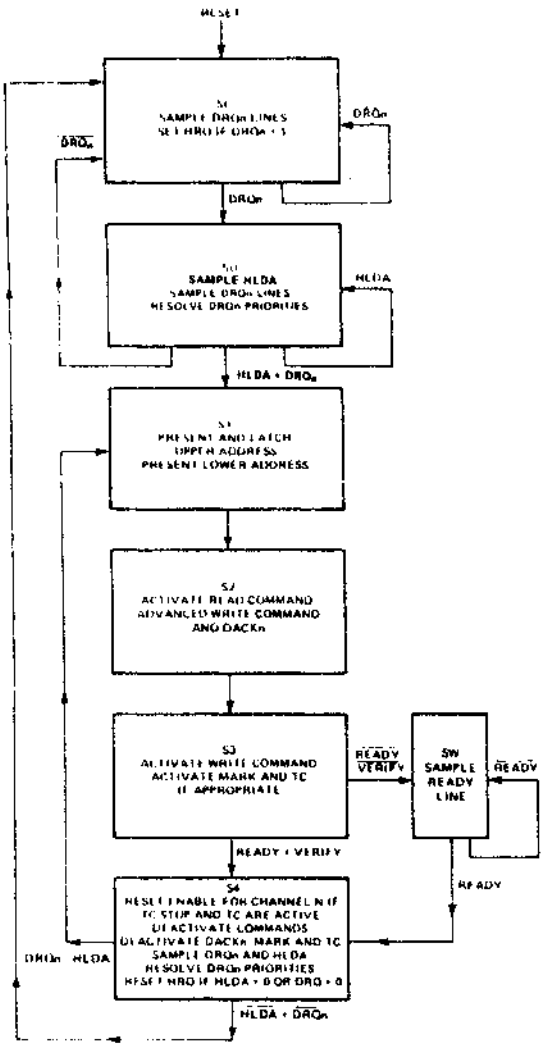
The least significant three address bits, A_0-A_2, indicate the specific register to be accessed. When accessing the Mode Set or Status register, A_0-A_2 are all zero. When accessing a channel register bit A_0 differentiates between the DMA address register (A_0 = 0) and the terminal count register (A_0 = 1), while bits A_1 and A_2 specify one of the four channels. Because the "channel registers" are 16-bits, two program instruction cycles are required to load or read an entire register. The 8257 contains a first/last (F/L) flip flop which toggles at the completion of each channel program or read operation. The F/L flip flop determines whether the upper or lower byte of the register is to be accessed. The F/L flip flop is reset by the RESET input and whenever the Mode Set register is loaded. To maintain proper synchronization when accessing the "channel registers" all channel command instruction operations should occur in pairs, with the lower byte of a register always being accessed first. Do not allow $\overline{CS}$ to clock while either $\overline{I/OR}$ or $\overline{I/OW}$ is active, as this will cause an erroneous F/L flip flop state. In systems utilizing an interrupt structure, interrupts should be disabled prior to any paired programming operations to prevent an interrupt from splitting them. The result of such a split would leave the F/L F/F in the wrong state. This problem is particularly obvious when other DMA channels are programmed by an interrupt structure.

CONTROL INPUT	$\overline{CS}$	$\overline{I/OW}$	$\overline{I/OR}$	A_3
Program Half of a Channel Register	0	0	1	0
Read Half of a Channel Register	0	1	0	0
Program Mode Set Register	0	0	1	1
Read Status Register	0	1	0	1

8257 Register Selection

REGISTER	BYTE	ADDRESS INPUTS				F/L	*BI-DIRECTIONAL DATA BUS							
		A_3	A_2	A_1	A_0		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CH-0 DMA Address	LSB	0	0	0	0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
	MSB	0	0	0	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
CH-0 Terminal Count	LSB	0	0	0	1	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	MSB	0	0	0	1	1	Rd	Wr	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8
CH-1 DMA Address	LSB	0	0	1	0	0	Same as Channel 0							
	MSB	0	0	1	0	1								
CH-1 Terminal Count	LSB	0	0	1	1	0								
	MSB	0	0	1	1	1								
CH-2 DMA Address	LSB	0	1	0	0	0	Same as Channel 0							
	MSB	0	1	0	0	1								
CH-2 Terminal Count	LSB	0	1	0	1	0								
	MSB	0	1	0	1	1								
CH-3 DMA Address	LSB	0	1	1	0	0	Same as Channel 0							
	MSB	0	1	1	0	1								
CH-3 Terminal Count	LSB	0	1	1	1	0								
	MSB	0	1	1	1	1								
MODE SET (Program only)	—	1	0	0	0	0	AL	TCS	EW	RP	EN3	EN2	EN1	EN0
STATUS (Read only)	—	1	0	0	0	0	0	0	0	UP	TC3	TC2	TC1	TC0

*A_0-A_{15}: DMA Starting Address, C_0-C_{13}: Terminal Count value (N-1), Rd and Wr: DMA Verify (00), Write (01) or Read (10) cycle selection, AL: Auto Load, TCS: TC STOP, EW: EXTENDED WRITE, RP: ROTATING PRIORITY, EN3-EN0: CHANNEL ENABLE MASK, UP: UPDATE FLAG, TC3-TC0: TERMINAL COUNT STATUS BITS.



1 DRQn refers to any DRQ line on an enabled DMA channel.

Figure 6. DMA Operation State Diagram

DMA OPERATION

Single Byte Transfers

A single byte transfer is initiated by the I/O device raising the DRQ line of one channel of the 8257. If the channel is enabled, the 8257 will output a HRQ to the CPU. The 8257 now waits until a HLDA is received insuring that the system bus is free for its use. Once HLDA is received the $\overline{DACK}$ line for the requesting channel is activated (LOW). The $\overline{DACK}$ line acts as a chip select for the requesting I/O device. The 8257 then generates the read and write commands and byte transfer occurs between the selected I/O device and memory. After the transfer is complete, the $\overline{DACK}$ line is set HIGH and the HRQ line is set LOW to indicate to the CPU that the bus is now free for use. DRQ must remain HIGH until $\overline{DACK}$ is issued to be recognized and must go LOW before S4 of the transfer sequence to prevent another transfer from occuring. (See timing diagram.)

Consecutive Transfers

If more than one channel requests service simultaneously, the transfer will occur in the same way a burst does. No overhead is incurred by switching from one channel to another. In each S4 the DRQ lines are sampled and the highest priority request is recognized during the next transfer. A burst mode transfer in a lower priority channel will be overridden by a higher priority request. Once the high priority transfer has completed control will return to the lower priority channel if its DRQ is still active. No extra cycles are needed to execute this sequence and the HRQ line remains active until all DRQ lines go LOW.

Control Override

The continuous DMA transfer mode described above can be interrupted by an external device by lowering the HLDA line. After each DMA transfer the 8257 samples the HLDA line to insure that it is still active. If it is not active, the 8257 completes the current transfer, releases the HRQ line (LOW) and returns to the idle state. If DRQ lines are still active the 8257 will raise the HRQ line in the third cycle and proceed normally. (See timing diagram.)

Not Ready

The 8257 has a Ready input similar to the 8080A and the 8085A. The Ready line is sampled in State 3. If Ready is LOW the 8257 enters a wait state. Ready is sampled during every wait state. When Ready returns HIGH the 8257 proceeds to State 4 to complete the transfer. Ready is used to interface memory or I/O devices that cannot meet the bus set up times required by the 8257.

Speed

The 8257 uses four clock cycles to transfer a byte of data. No cycles are lost in the master to master transfer maximizing bus efficiency. A 2MHz clock input will allow the 8257 to transfer at a rate of 500K bytes/second.

Memory Mapped I/O Configurations

The 8257 can be connected to the system bus as a memory device instead of as an I/O device for memory mapped I/O configurations by connecting the system memory control lines to the 8257's I/O control lines and the system I/O control lines to the 8257's memory control lines.

This configuration permits use of the 8080's considerably larger repertoire of memory instructions when reading or loading the 8257's registers. Note that with this connection, the programming of the Read (bit 15) and Write (bit 14) bits in the terminal count register will have a different meaning.

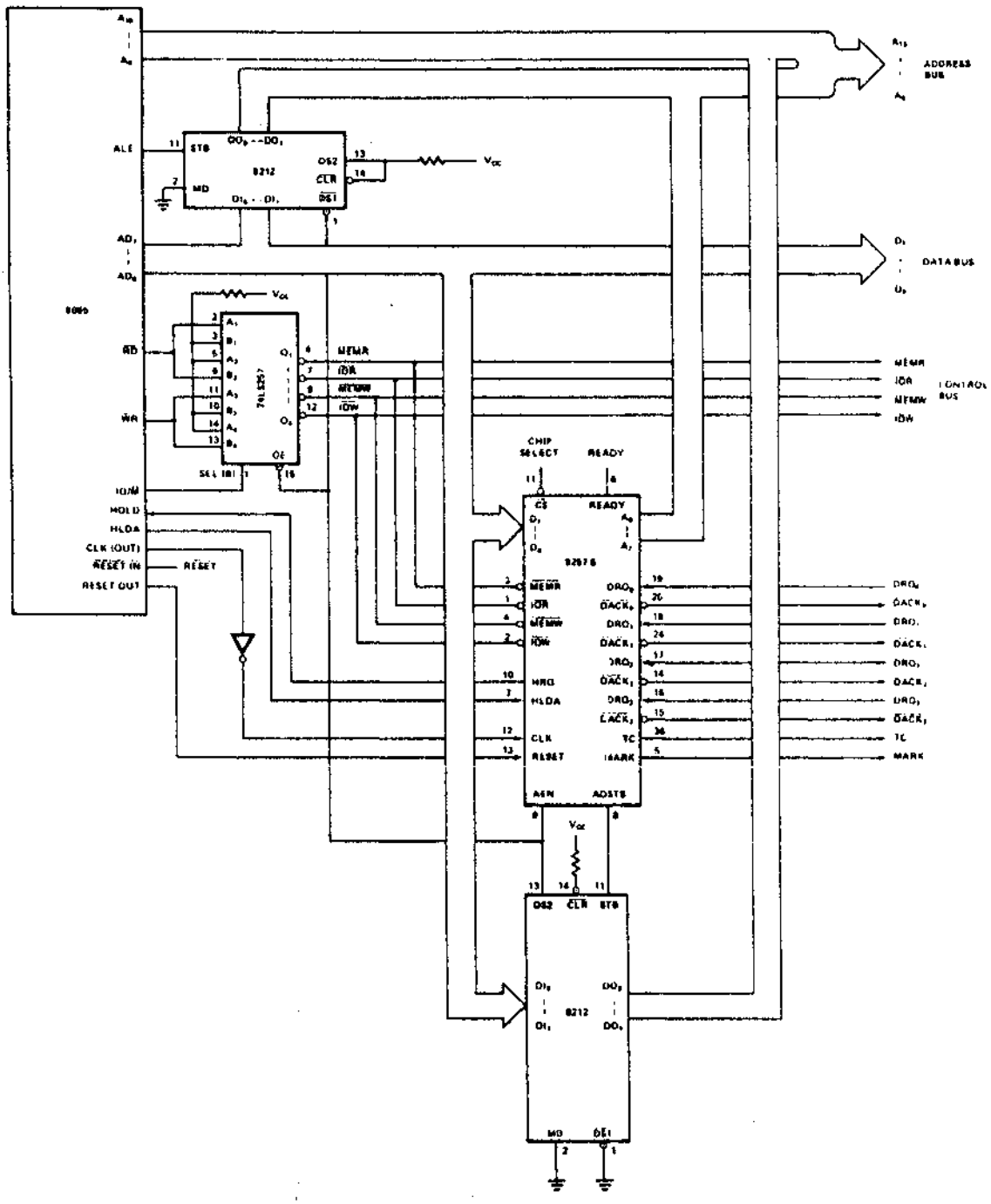


Figure 11. Detailed System Interface Schematic

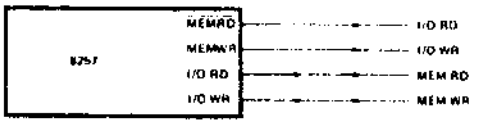


Figure 7. System Interface for Memory Mapped I/O

BIT 15 READ	BIT 14 WRITE	
0	0	DMA Verify Cycle
0	1	DMA Read Cycle
1	0	DMA Write Cycle
1	1	Illegal

Figure 8. TC Register for Memory Mapped I/O Only

SYSTEM APPLICATION EXAMPLES

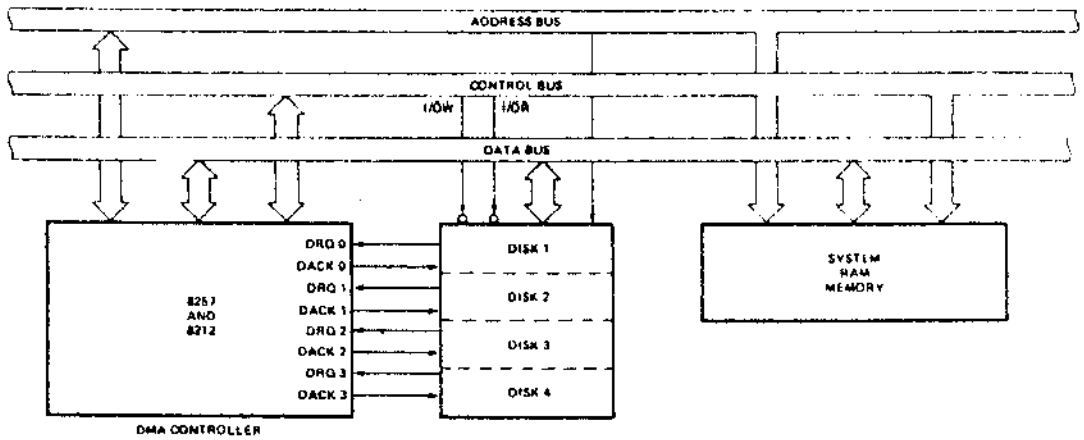


Figure 9. Floppy Disk Controller (4 Drives)

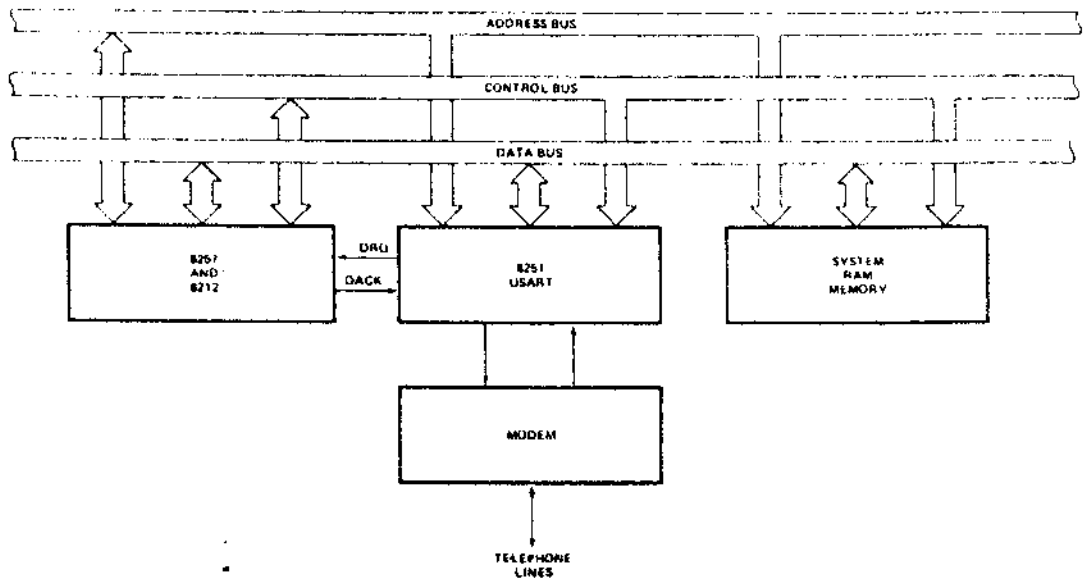


Figure 10. High-Speed Communication Controller

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . −0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{CC}+.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH}=-150μA for AB, DB and AEN I_{OH}=-80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = -80μA
I_{CC}	V_{CC} Current Drain		120	mA	
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Leakage During Float		±10	μA	V_{OUT} = V_{CC} to 0V

CAPACITANCE

T_A = 25°C: V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS: PERIPHERAL (SLAVE) MODE

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%; GND = 0V (Note 1).

8080 Bus Parameters

Read Cycle:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AR}	Adr or $\overline{CS}$↓ Setup to $\overline{RD}$↓	0		0		ns	
T_{RA}	Adr or $\overline{CS}$↑ Hold from $\overline{RD}$↑	0		0		ns	
T_{RD}	Data Access from $\overline{RD}$↓	0	300	0	200	ns	(Note 2)
T_{DF}	DB→Float Delay from $\overline{RD}$↑	20	150	20	100	ns	
T_{RR}	$\overline{RD}$ Width	250		260		ns	

Write Cycle:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AW}	Adr Setup to $\overline{WR}$↓	20		20		ns	
T_{WA}	Adr Hold from $\overline{WR}$↑	0		0		ns	
T_{DW}	Data Setup to $\overline{WR}$↑	200		200		ns	
T_{WD}	Data Hold from $\overline{WR}$↑	0		0		ns	
T_{WW}	$\overline{WR}$ Width	200		200		ns	

Other Timing:

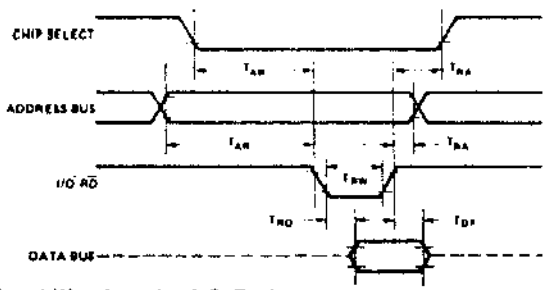
Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{RSTW}	Reset Pulse Width	300		300		ns	
T_{RSTO}	Power Supply↑ (V_{CC}) Setup to Reset↓	500		500		μs	
T_r	Signal Rise Time		20		20	ns	
T_f	Signal Fall Time		20		20	ns	
T_{RSTS}	Reset to First $\overline{I/O}\overline{WR}$	2		2		T_{CY}	

Notes: 1. All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V; Output "1" at 2.0V, "0" at 0.8V
2. 8257 C_L = 100pF, 8257-5: C_L = 150pF.

8257 PERIPHERAL MODE TIMING DIAGRAMS

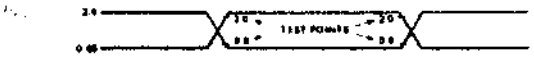
Write Timing:

Read Timing:



Reset Timing:

Input Waveform for A.C. Tests:



A.C. CHARACTERISTICS: DMA (MASTER) MODE T_A = 0°C to 70°C, V_{CC} = +5V ±5%, GND = 0V.

Timing Requirements

SYMBOL	PARAMETER	8257		8257-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
T_{CY}	Cycle Time (Period)	0.320	4	0.320	4	μs
T_ϕ	Clock Active (High)	120	$.8T_{CY}$	80	$.8T_{CY}$	ns
T_{QS}	DRQ↑ Setup to ϕ↓ (S1, S4)	120		30		ns
T_{QH}	DRQ↓ Hold from HLDA↑[4]	0		0		ns
T_{HS}	HLDA↑ or ↓Setup to ϕ↓(S1, S4)	100		100		ns
T_{RS}	READY Setup Time to ϕ↑ (S3, Sw)	30		30		ns
T_{RH}	READY Hold Time from ϕ↑ (S3, Sw)	20		20		ns

Note: 4. Tracking Parameter.

Tracking Parameters

Signals labeled as Tracking Parameters (footnotes 4-7 under A.C. Specifications) are signals that follow similar paths through the silicon die. The propagation speed of these signals varies in the manufacturing process but the relationship between all these parameters is constant. The variation is less than or equal to 50 ns.

Suppose the following timing equation is being evaluated,

$$T_{A(MIN)} + T_{B(MAX)} \leq 50 \text{ ns}$$

and only minimum specifications exist for T_A and T_B. If $T_{A(MIN)}$ is used, and if T_A and T_B are tracking parameters, $T_{B(MAX)}$ can be taken as $T_{B(MIN)}$ + 50 ns.

$$T_{A(MIN)} + (T_{B(MIN)}^* + 50 \text{ ns}) \leq 150 \text{ ns}$$

*if T_A and T_B are tracking parameters

A.C. CHARACTERISTICS: DMA (MASTER) MODE $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V

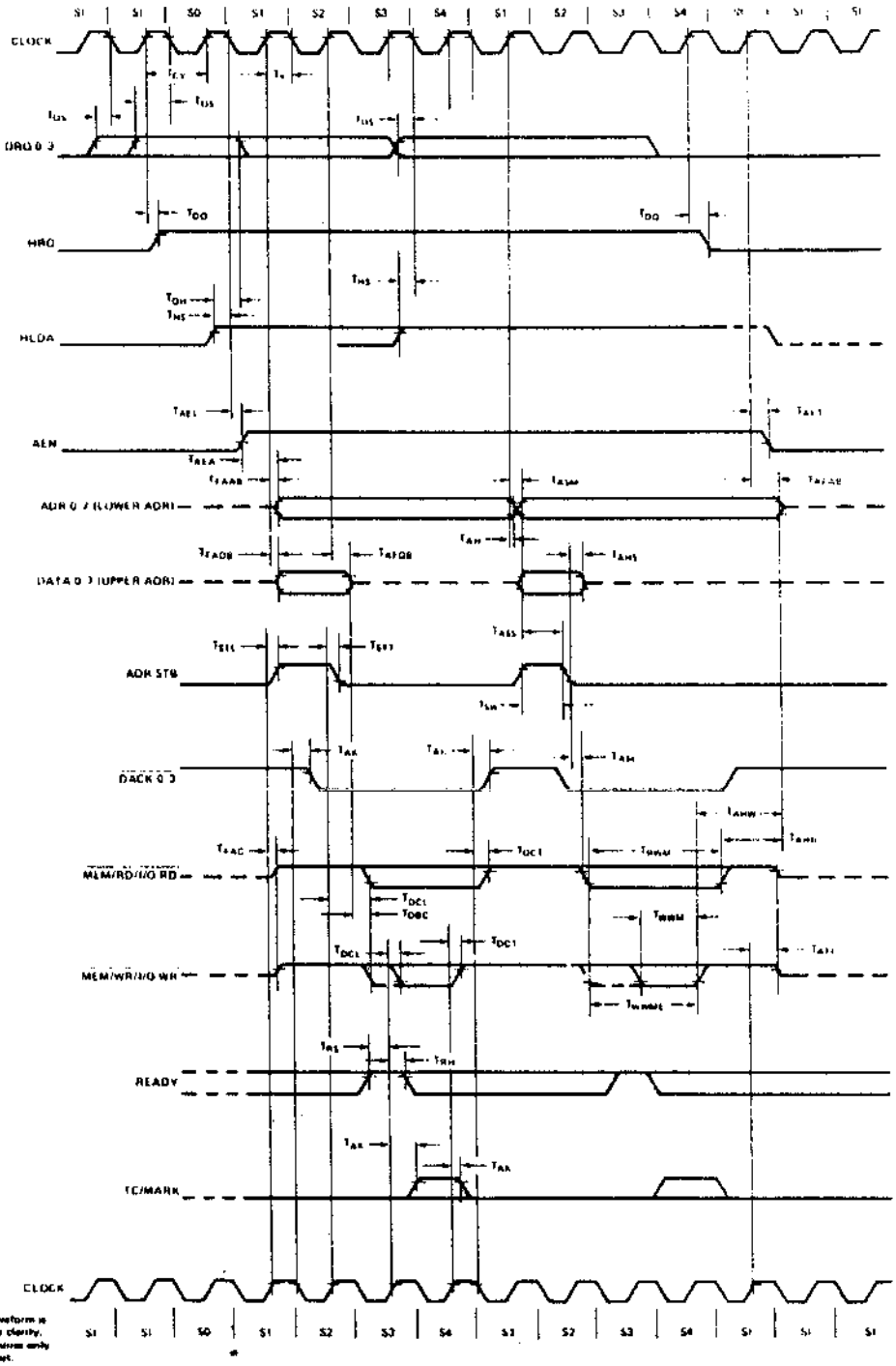
Timing Responses

SYMBOL	PARAMETER	8257		8257-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
T_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 2.0V)[1]		160		160	ns
T_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)[3]		250		250	ns
T_{AEL}	AEN↑ Delay from θ↓(S1)[1]		300		300	ns
T_{AEF}	AEN↓ Delay from θ↑(SI)[1]		200		200	ns
T_{AEA}	Adr(AB)(Active) Delay from AEN↑(S1)[4]	20		20		ns
T_{FAAB}	Adr(AB)(Active) Delay from θ↑(S1)[2]		250		250	ns
T_{AFAB}	Adr(AB)(Float) Delay from θ↑(SI)[2]		150		150	ns
T_{ASM}	Adr(AB)(Stable) Delay from θ↑(S1)[2]		250		250	ns
T_{AH}	Adr(AB)(Stable) Hold from θ↑(S1)[2]	T_{ASM}-50		T_{ASM}-50		ns
T_{AHR}	Adr(AB)(Valid) Hold from $\overline{Rd}$↑(S1,SI)[4]	60		60		ns
T_{AHW}	Adr(AB)(Valid) Hold from $\overline{Wr}$↑(S1,SI)[4]	300		300		ns
T_{FADB}	Adr(DB)(Active) Delay from θ↑(S1)[2]		300		300	ns
T_{AFDB}	Adr(DB)(Float) Delay from θ↑(S2)[2]	T_{STT}+20	250	T_{STT}+20	170	ns
T_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)[4]	100		100		ns
T_{AHS}	Adr(DB)(Valid) Hold from AdrStb↓(S2)[4]	50		50		ns
T_{STL}	AdrStb↑ Delay from θ↑(S1)[1]		200		200	ns
T_{STT}	AdrStb↓ Delay from θ↑(S2)[1]		140		140	ns
T_{SW}	AdrStb Width (S1-S2)[4]	T_{CY}-100		T_{CY}-100		ns
T_{ASC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from AdrStb↓(S2)[4]	70		70		ns
T_{DBC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from Adr(DB) (Float)(S2)[4]	20		20		ns
T_{AK}	DACK↑ or ↓Delay from θ↓(S2,S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)[1,5]		250		250	ns
T_{DCL}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from θ↑(S2) and $\overline{Wr}$↓ Delay from θ↑(S3)[2,6]		200		200	ns
T_{DCT}	$\overline{Rd}$↑ Delay from θ↓(S1,SI) and $\overline{Wr}$↑ Delay from θ↑(S4)[2,7]		200		200	ns
T_{FAC}	$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑(S1)[2]		300		300	ns
T_{AFC}	$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑(SI)[2]		150		150	ns
T_{RWM}	$\overline{Rd}$ Width (S2-S1 or SI)[4]	$2T_{CY}+T_\theta$-50		$2T_{CY}+T_\theta$-50		ns
T_{WWM}	$\overline{Wr}$ Width (S3-S4)[4]	T_{CY}-50		T_{CY}-50		ns
T_{WWME}	$\overline{Wr}$(Ext) Width (S2-S4)[4]	$2T_{CY}$-50		$2T_{CY}$-50		ns

Notes: 1. Load = 1 TTL. 2. Load = 1 TTL + 50pF. 3. Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V. 4. Tracking Parameter. 5. $\Delta T_{AK} < 50$ ns. 6. $\Delta T_{DCL} < 50$ ns. 7. $\Delta T_{DCT} < 50$ ns.

DMA MODE WAVEFORMS

CONSECUTIVE CYCLES AND BURST MODE SEQUENCE



NOTE: The clock waveform is duplicated for clarity. The 8257 requires only one clock input.

Figure 12. Consecutive Cycles and Burst Mode Sequence

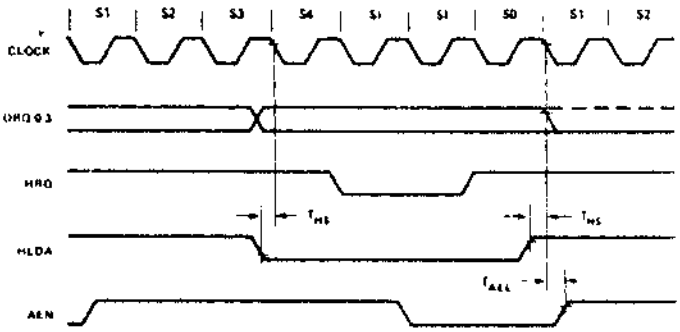


Figure 13. Control Override Sequence

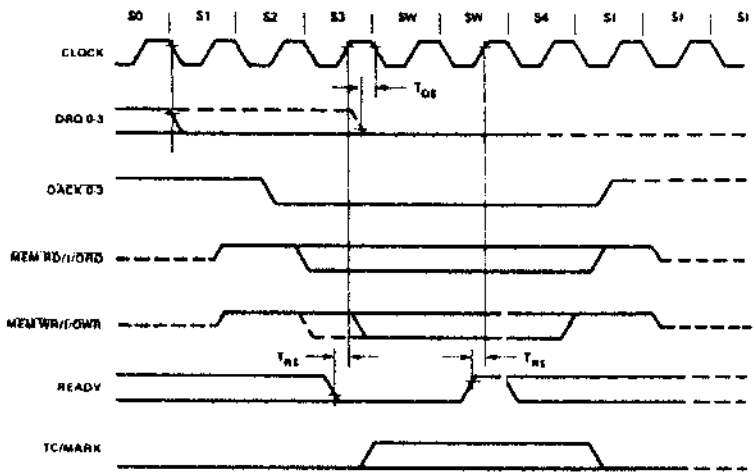


Figure 14. Not Ready Sequence

WESTERN DIGITAL
CORPORATION

FD 179X-01 Floppy Disk Formatter/Controller Family

FEATURES

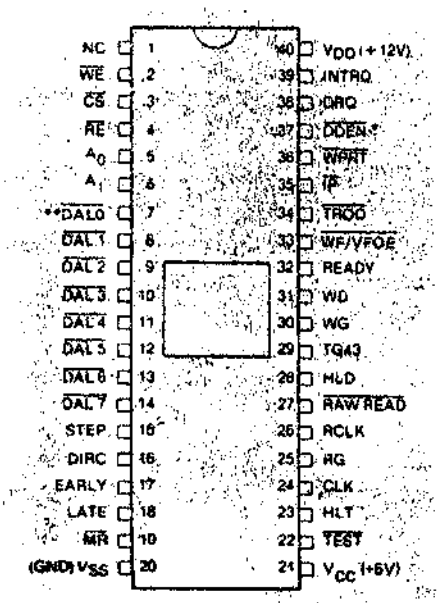
- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable length Sector
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION (MFM AND FM)
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1793/4 HAS TRUE DAL LINES

179X-01 FAMILY CHARACTERISTICS

FEATURES	1791-01	1792-01	1793-01	1794-01
Single Density (FM)	X	X	X	X
Double Density (MFM)	X		X	
True Data Bus			X	X
Inverted Data Bus	X	X		
Write Precomp	X	X	X	X
Window Extension	X	X	X	X

APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/ FORMATTER
NEW MINI-FLOPPY CONTROLLER



*FD1792/4 PIN 37 MUST BE LEFT OPEN
**FD1793/4 TRUE BUS

PIN CONNECTIONS

FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	WRITE FAULT VFO ENABLE	WF/VFOE	This input detects writing fault indications from the drive. When WG = 1 and WF goes low the current Write command is terminated and the Write Fault status bit is set. The WF input should be made inactive (high) when WG becomes inactive. When WG = 0, this pin functions as a VFO enable output. VFOE is made active when the head is fully engaged and data is being inspected off of the diskette.
34	TRACK 00	TR00	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	INDEX PULSE	IP	This input informs the FD179X when the index hole is encountered on the diskette.
36	WRITE PROTECT	WPRT	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	DOUBLE DENSITY	DDEN	This pin selects either single or double density operation. When DDEN = 0, double density is selected. When DDEN = 1, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input (RAW READ) during Read operations and transfers serial data to the Write Data output during Write operations.

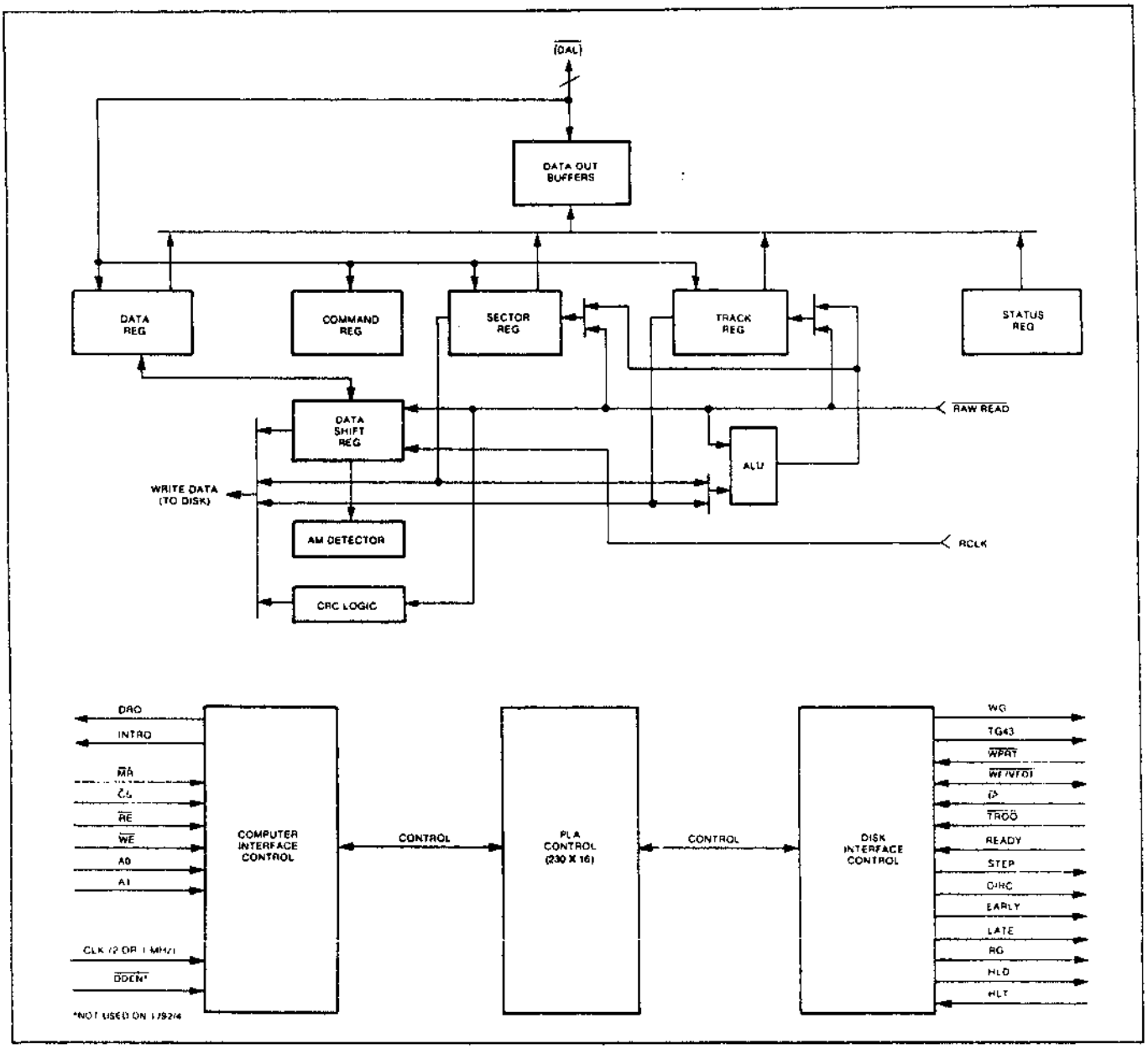
Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00) if the verify flag is on. The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.



FD179X BLOCK DIAGRAM

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and

Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 1791 and 1793 have two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled. The 1792/4 operates in the single density mode only, with Pin 37 left open by the user.

HEAD POSITIONING

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

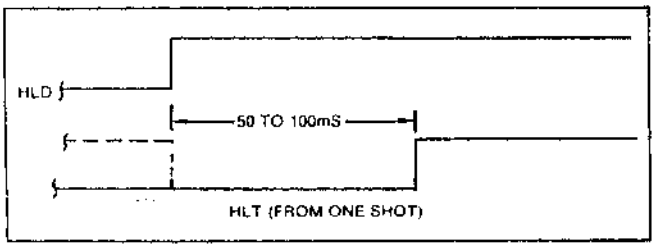
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	x	x
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	200 μs	400 μs
0 1	6 ms	6 ms	12 ms	12 ms	200 μs	400 μs
1 0	10 ms	10 ms	20 ms	20 ms	200 μs	400 μs
1 1	15 ms	15 ms	30 ms	30 ms	200 μs	400 μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations, the FD179X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WF}}/\overline{\text{VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	S	E	C	0
II	Write Sector	1	0	1	m	S	E	C	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I COMMANDS

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on destination track
V = 0, No verify

r_1r_0 = Stepping motor rate*(Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

Table 4. FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)

a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)

E = 1, 15 ms delay

E = 0, no 15 ms delay

S = Side Select Flag

S = 0, Compare for Side 0
S = 1, Compare for Side 1

C = Side Compare Flag

C = 0, disable side select compare
C = 1, enable side select compare

Table 5. FLAG SUMMARY

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)

I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to Not-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt

I_3-I_0 = 0, Terminate with no Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_1r_0), which determines the stepping motor rate as defined in Table 1.

The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD179X receives a command that specifically disengages the head. If the FD179X is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the

ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD179X terminates the operation and sends an interrupt, (INTRQ).

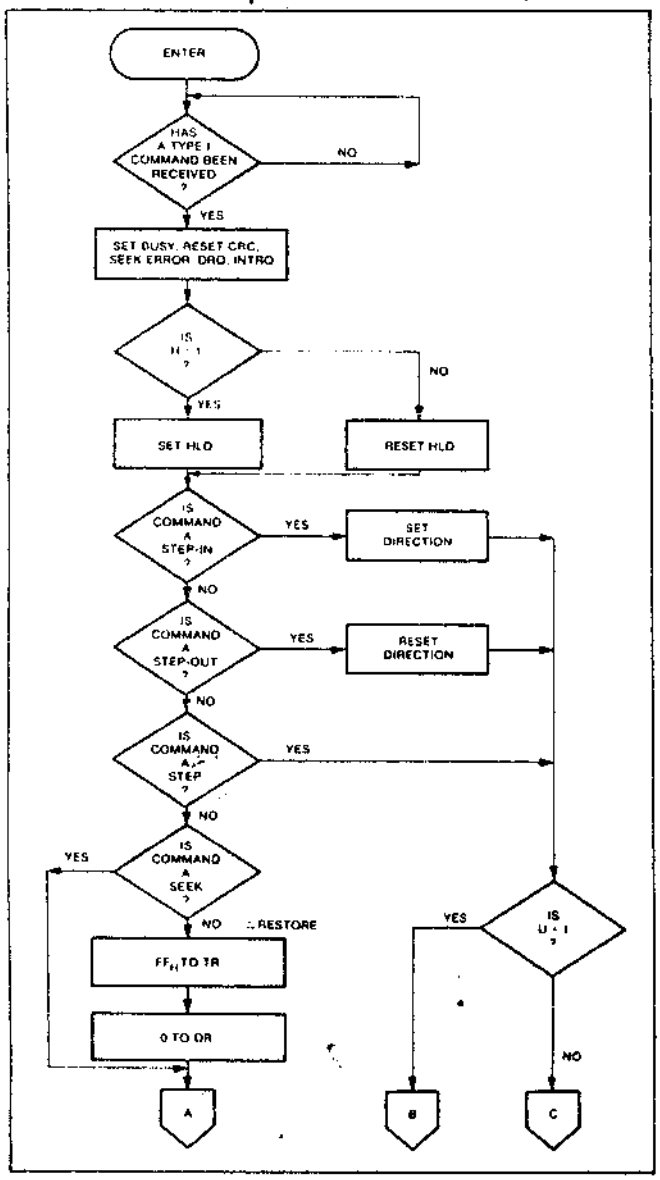
The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

RESTORE (SEEK TRACK 0)

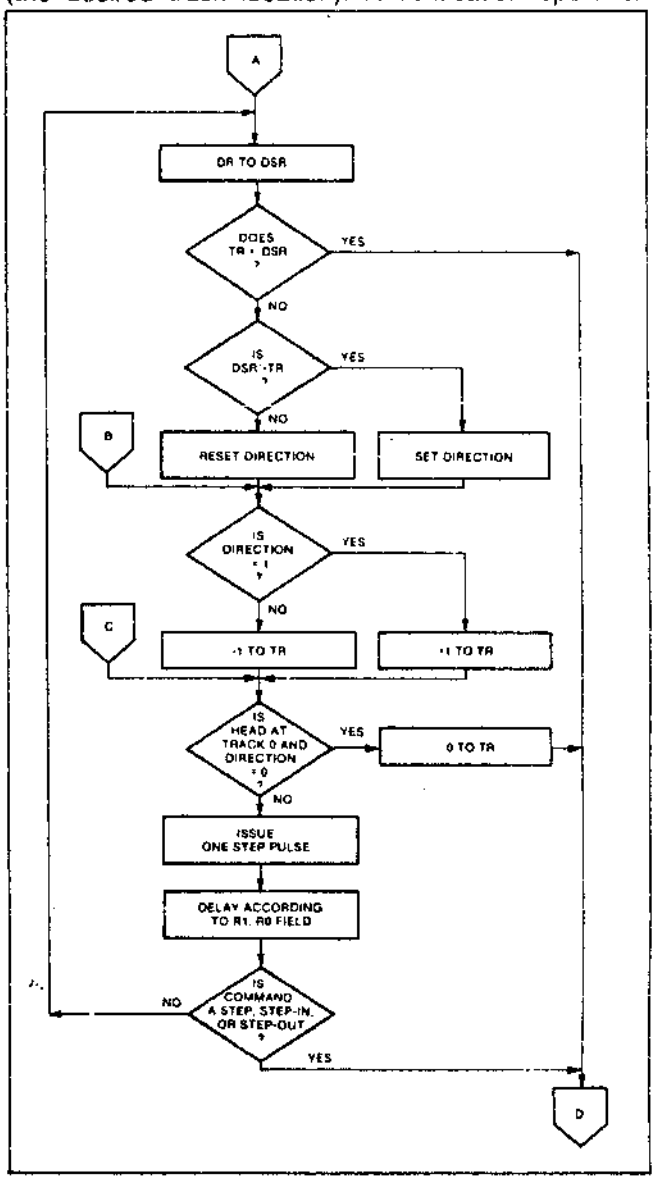
Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the rr0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation



TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

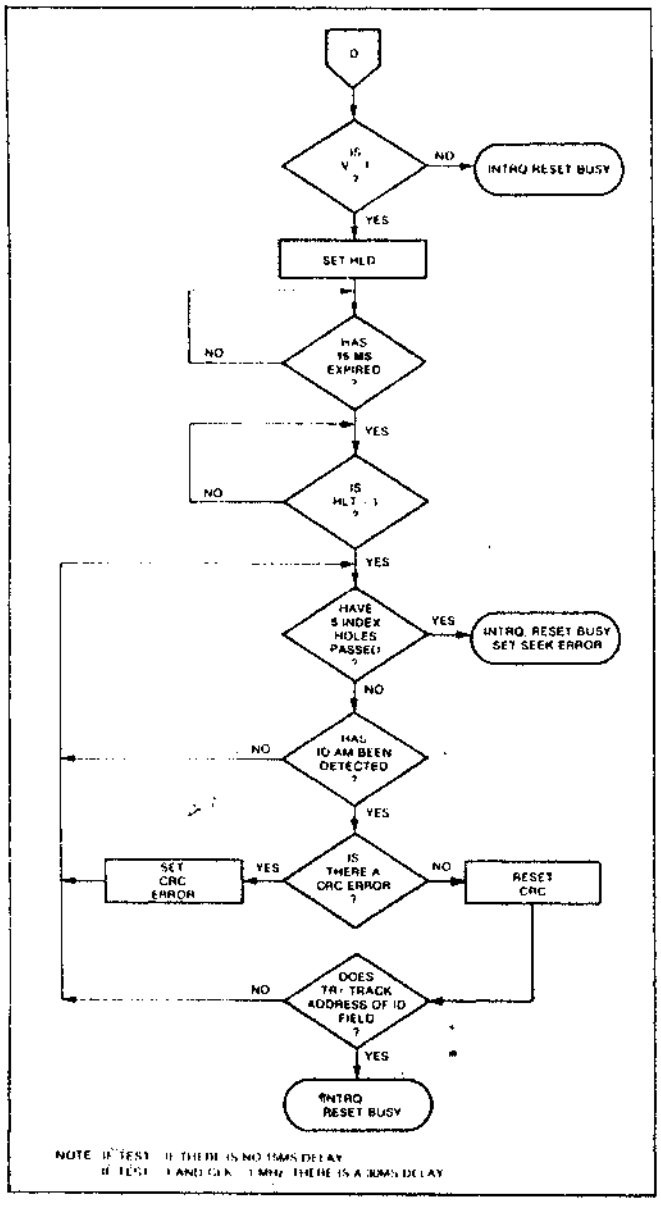
takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.



TYPE I COMMAND FLOW

STEP-OUT

Upon receipt of this command, the FD179X issues one s epping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 12.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Sector Length Table

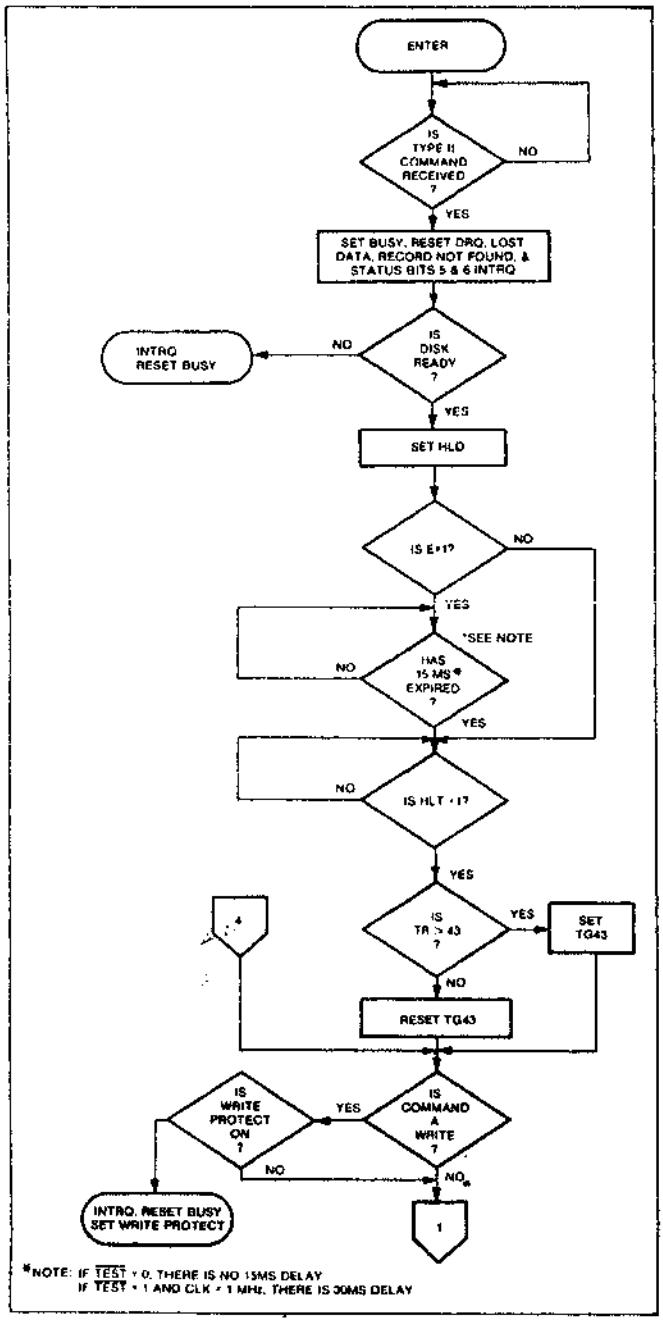
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0 a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register until the sector regis-

ter exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

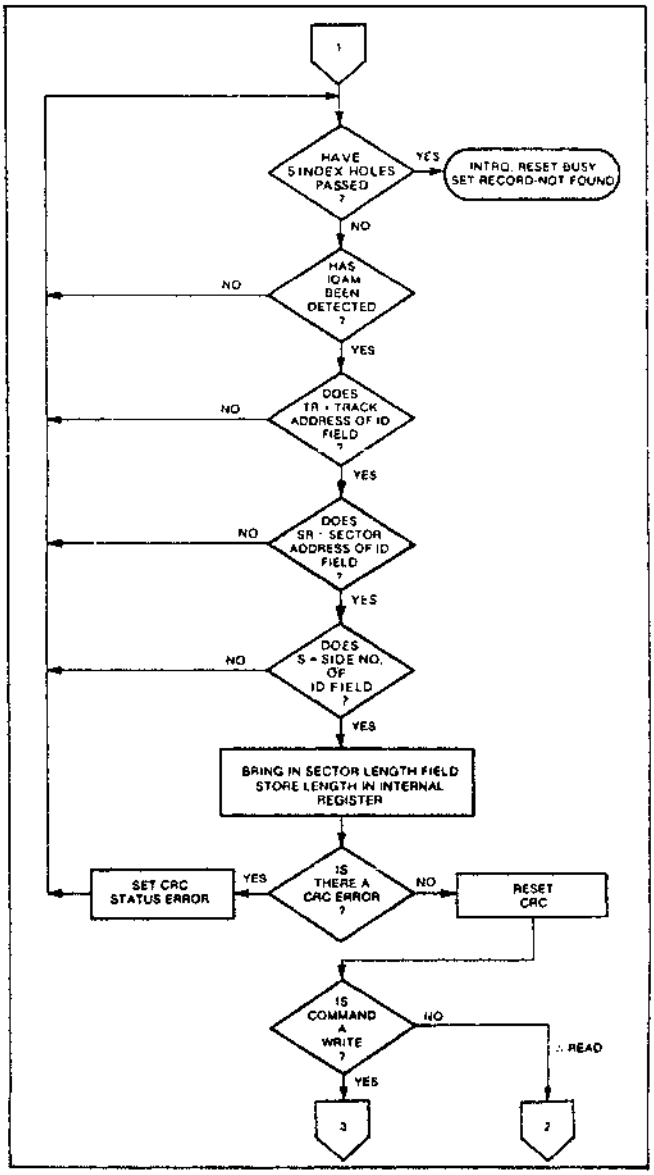


TYPE II COMMAND

READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

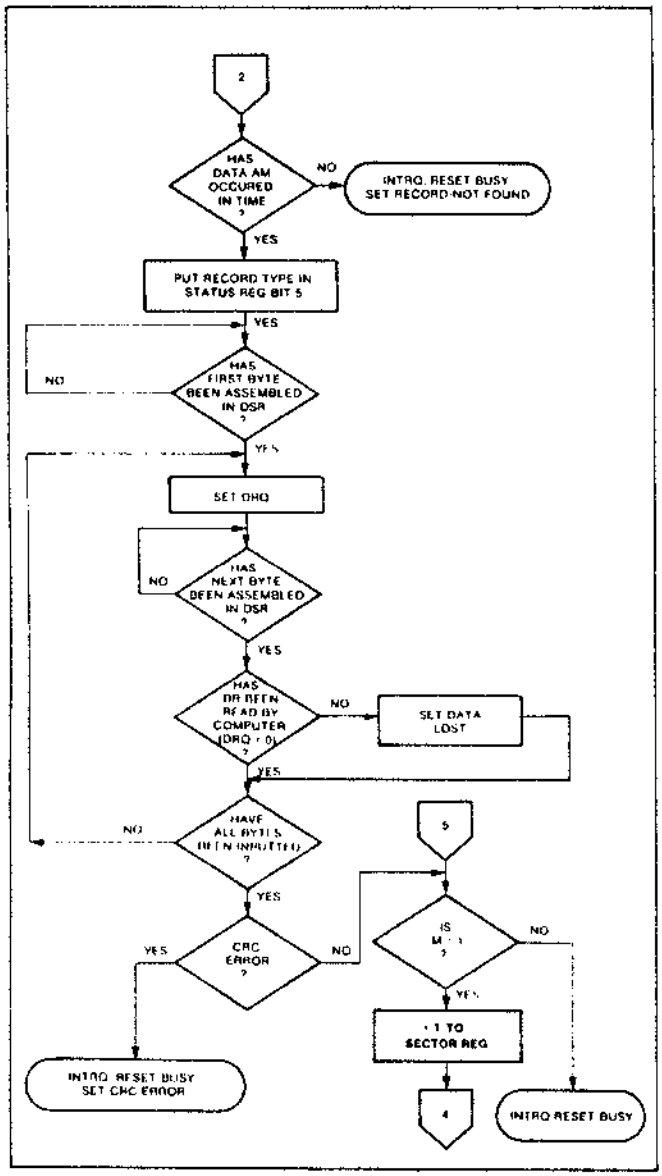
When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and



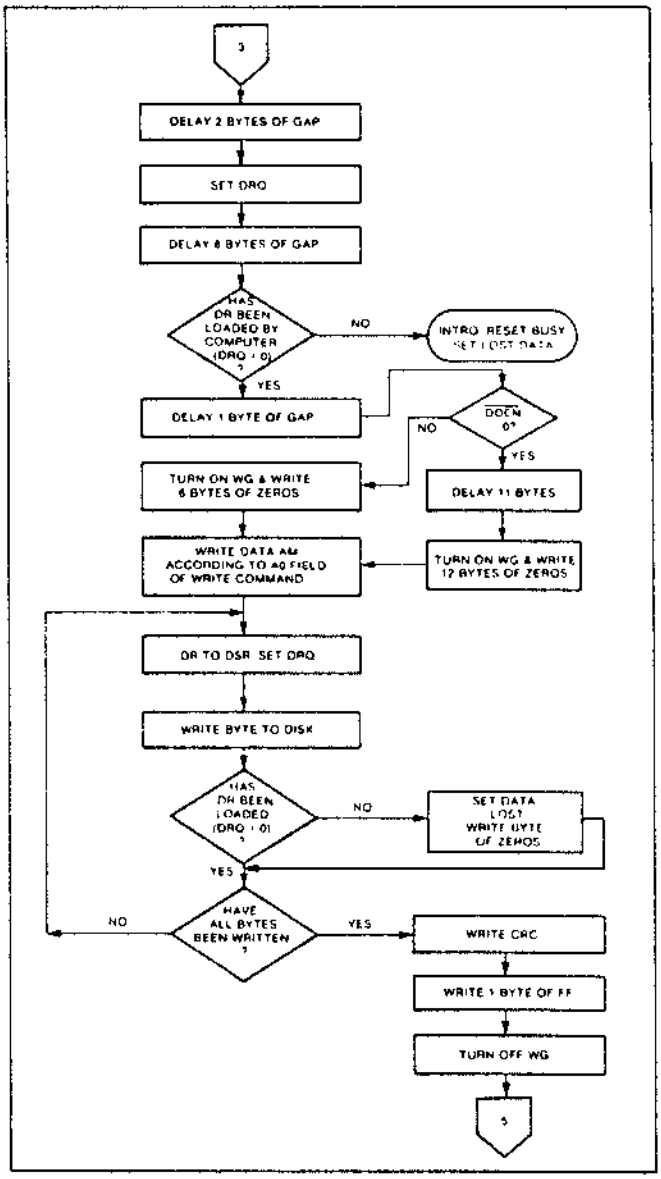
TYPE II COMMAND

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
				ID FIELD						DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.



TYPE II COMMAND



TYPE II COMMAND

the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

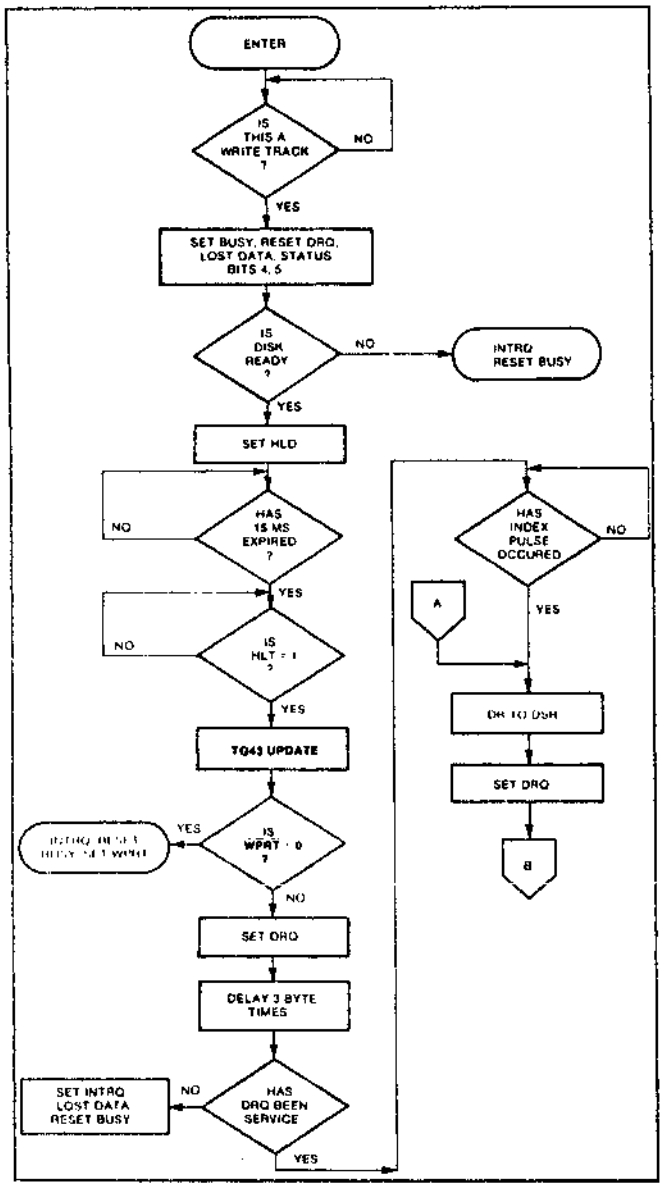
STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are

then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark



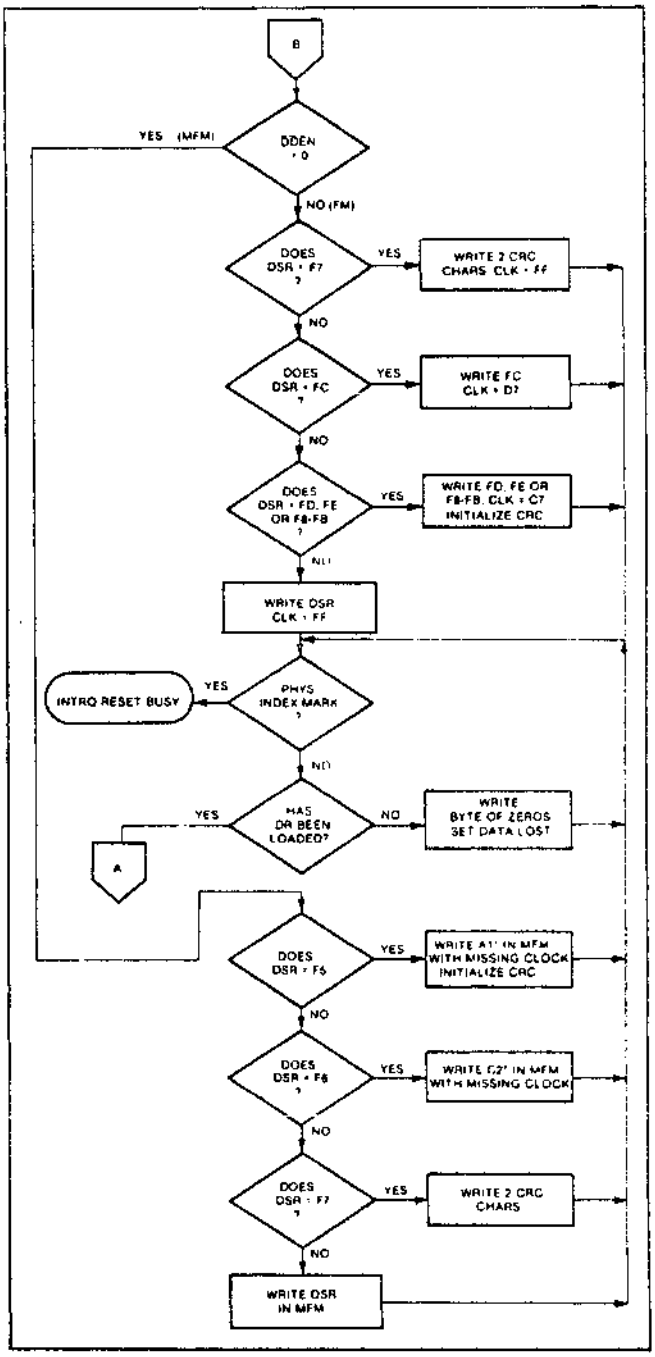
TYPE III COMMAND WRITE TRACK

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The



TYPE III COMMAND WRITE TRACK

next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track command.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5
**Missing clock transition between bits 3 & 4

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. *This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.*

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

Table 6. STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set; it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD179X raises the Data Request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, in FM an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

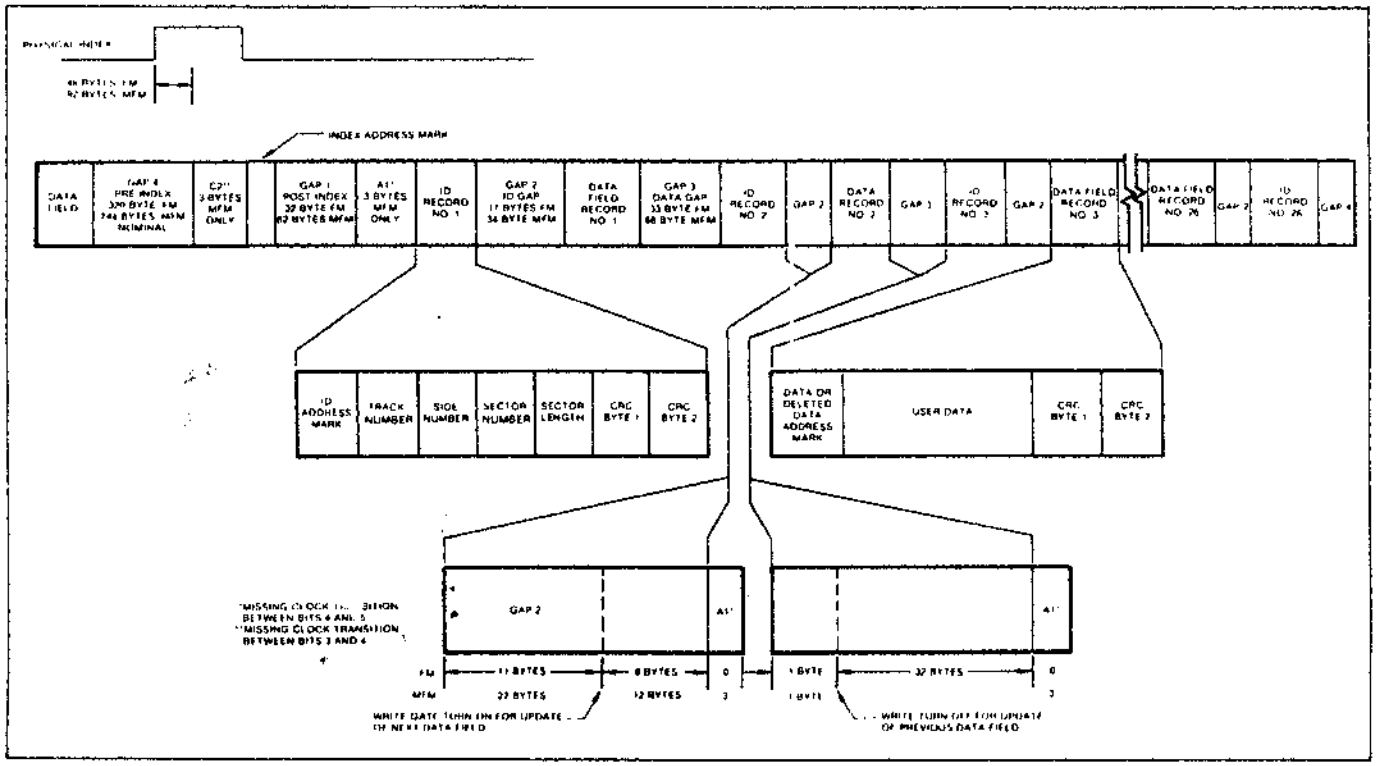
IBM 3740 FORMAT—128 BYTES/SECTOR

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF
6	00
1	FC (Index Mark)
26*	FF
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF
247**	FF

*Write bracketed field 26 times

**Continue writing until FD1791 interrupts out. Approx. 247 bytes.



IBM TRACK FORMAT

IBM SYSTEM 34 FORMAT-256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6
1	FC (Index Mark)
50*	4E
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01
1	F7 (2 CRCs written)
22	4E
12	00
3	F5
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times
** Continue writing until FD179X interrupts out. Approx. 598 bytes.

NON-IBM FORMATS

Variations in the IBM format are possible to a limited extent if the following requirements are met: sector size must be a choice of 128, 512 or 1024 bytes; gap size must be according to the following table. Note that the Index Mark is not required by the FD179X. All gap sizes shown are the minimum values required by the 179X.

	FM	MFM
Gap I	16 bytes FF	16 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00
		3 bytes A1
Gap III	10 bytes FF	16 bytes 4E
**	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground) =15 to −0.3V

Max. Voltage to Any Input With Respect to V_{SS} =15 to −0.3V

Operating Temperature 0°C to 70°C

Storage Temperature −55°C to +125°C

OPERATING CHARACTERISTICS (DC)

T_A = 0°C to 70°C, V_{DD} = +12.0V ±.6V,
V_{SS} = 0V, V_{CC} =+5V ±.25V
V_{DD} = 10 ma Nominal, V_{CC} = 35 ma Nominal

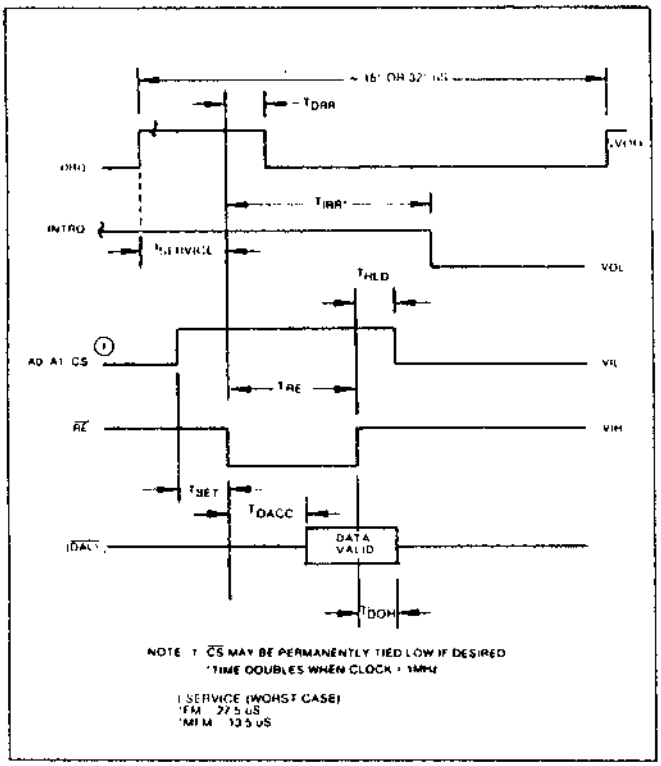
SYMBOL	CHARACTERISTIC	MIN.	TYPE.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{OL}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = 100 μA
V_{OL}	Output Low Voltage			0.45	V	I_O = 1.6 mA
P_D	Power Dissipation			0.5	W	

TIMING CHARACTERISTICS

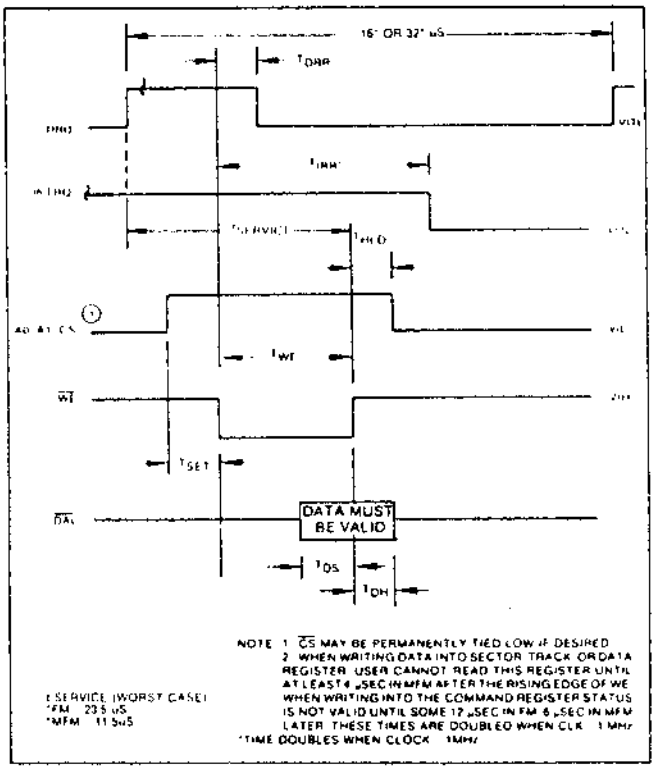
T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} =+5V ± .25V

READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	0			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 6
TDACC	Data Access from $\overline{RE}$			300	nsec	C_L = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 50 pf



READ ENABLE TIMING



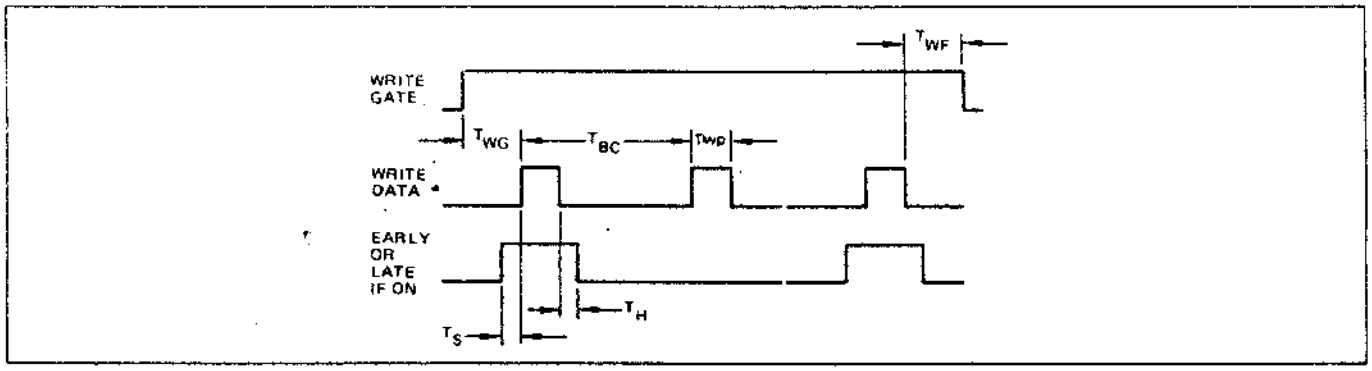
WRITE ENABLE TIMING

WRITE ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 6
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	20			nsec	

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{Raw\ Read}$ Pulse Width	100	200		nsec	See Note 1,2
tbc	$\overline{Raw\ Read}$ Cycle Time	1600	2000		nsec	See Note 3
Ta	RCLK Duty (High)	800			nsec	See Note 4, 5
Tb	RCLK Duty (Low)	800			nsec	
Tc	RCLK Cycle Time	1600			nsec	
T_{x1}	RCLK hold to $\overline{Raw\ Read}$	40			nsec	
T_{x2}	$\overline{Raw\ Read}$ hold to RCLK	40			nsec	See Note 1



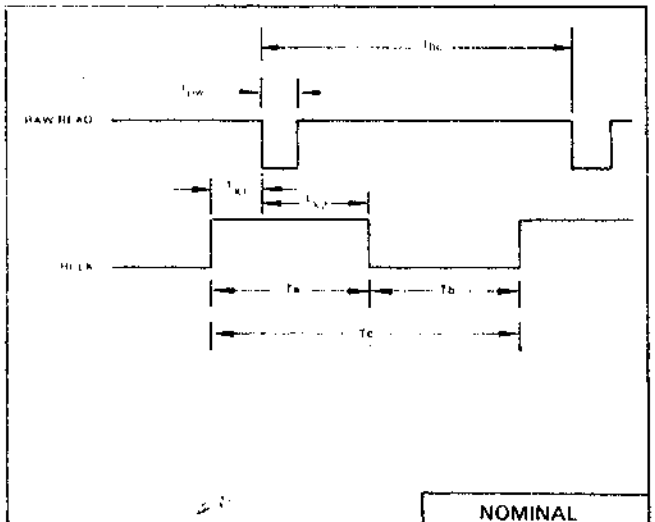
WRITE DATA TIMING

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width	450	500	550	nsec	FM
		150	200	250	nsec	MFM
Twg	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
Tbc	Write data cycle Time		2,3, or 4		μsec	±CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM

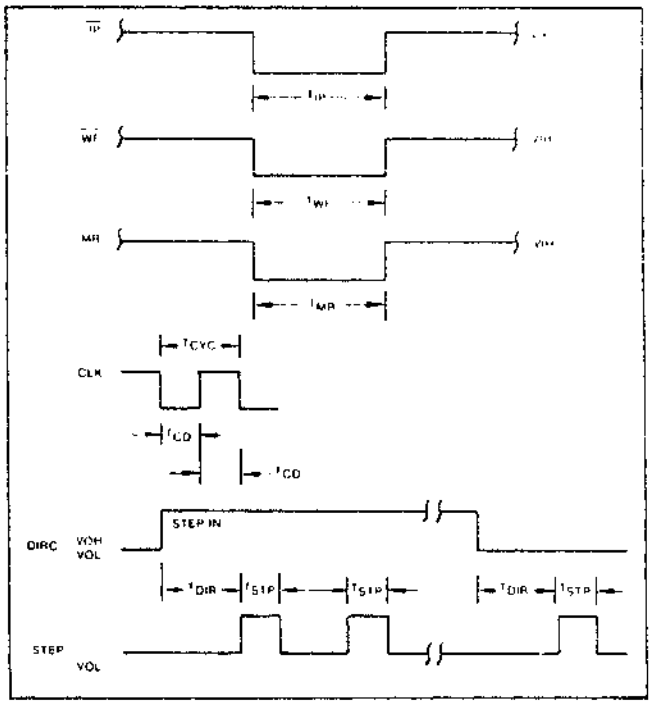
MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230	250	20000	nsec	
TCD_2	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	See Note 6
TDIR	Dir Setup to Step	12			μsec	
TMR	Master Reset Pulse Width	50			μsec	
TIP	Index Pulse Width	10			μsec	See Note 6
TWF	Write Fault Pulse Width	10			μsec	



				NOMINAL		
DISKETTE	MODE	$\overline{DDEN}$	CLK	T_a	T_b	T_c
8"	MFM	0	2 MHz	1 μS	1 μS	2 μS
8"	FM	1	2 MHz	2 μS	2μS	4 μS
5"	MFM	0	1 MHz	2 μS	2μS	4 μS
5"	FM	1	1 MHz	4 μS	4 μS	8 μS

INPUT DATA TIMING



MISCELLANEOUS TIMING

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. 100 ns. pulses are recommended for 8" MFM.
3. tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during $\overline{RAW\ READ}$ (Polarity is unimportant).
5. RCLK should be forced low when $\overline{VFOE}$ = 1 and free-running when $\overline{VFOE}$ = 0.
6. Times double when clock = 1 MHz.

WESTERN DIGITAL
CORPORATION

179X-01 Application Notes

INTRODUCTION

The FD179X Floppy Disk Formatter/Controller performs all the functions necessary to read or write data to any type of floppy disk drive. Both 8" and 5" (mini-floppy) drives with single or double density storage capabilities are supported. These MOS/LSI devices will replace a large amount of discrete logic required for interfacing a host processor to a floppy disk. The FD179X is ideally suited for microprocessor interfacing, either in a stand-alone computer system, or as a slave processor for mini-computer applications. The chip has been designed to be compatible with the IBM 3740 (FM) data format, or IBM System 34 (MFM). Provisions for non-standard variable length sectors have been included to provide more data storage capability per track. Programmable stepping rates via a 2-bit setting in the Command Register allows for interfacing to disk drives with different track-to-track access times. Requiring standard +5V, +12V power supplies, the FD179X is available in a standard 40-pin dual-in-line package.

When $\overline{DDEN}$ 1, the FD1791/3 reads and writes data in a frequency-modulated format. Both clock and data are recorded serially on each track of the disk. A data pulse or flux transition recorded between two clock pulses indicates a Logic "1"; the absence of a pulse between clocks indicates a Logic "0". Recorded on each track are unique combinations of data and clock bits called Address Marks. These address marks do not appear elsewhere on the disk and are used for synchronization. Four distinct address marks used are:

Description	Data	Clock
Index Address Mark	FC	D7
ID Address Mark	FE	C7
Data Address Mark	FB	C7
Deleted Address Mark	F8	C7

Figure 1A illustrates a typical recording in FM format. Note that a clock bit is always written before the data bit, regardless if the data written is a 1 or 0. The 1792 and 1794 have been designed for single density applications. Pin 37 must be left open by the user for proper operation.

When the Double Density Enable ($\overline{DDEN}$) pin of the 1791/3 is brought low, MFM recording is enabled. This modified-frequency-modulated technique uses a self-clocking feature to allow for recording at higher densities. Figure 1B illustrates this format. A clock pulse is written to the disk only if the preceding and present data bit written is zero. Without the use of this encoding scheme, recording densities at this higher speed would not be possible.

PROCESSOR INTERFACE

The FD179X contains five internal registers that can read or be written to. These registers are used to write commands, read status, and read and write data to and from the floppy disk. They are selected by a proper binary code on the A0, A1 lines in conjunction with the RE and WE lines when the device is selected. The registers and their addresses are:

$\overline{CS}$	A_1	A_0	$\overline{RE}$ = 0	$\overline{WE}$ = 0
0	0	0	STATUS REG	COMMAND REG
0	0	1	TRACK REG	TRACK REG
0	1	0	SECTOR REG	SECTOR REG
0	1	1	DATA REG	DATA REG
1	X	X	Deselected	Deselected

X = don't care

REGISTER ACCESS

Because of internal clock synchronization, certain delays are required when accessing registers in read and write conditions. These time delays are:

OPERATION	NEXT OPERATION	TIME DELAY REQ'D
Write to Command Register	Read from Status Register	MFM = 4 µs FM = 8 µs Before Status is Valid
Write to Command Register	Read Busy Bit in Status Register	MFM = 6 µs FM = 12 µs
Write to any Register	Read from a Different Register	No Delay Req'd.

Note: All time delays double for mini-floppy (CLK = 1MHz) operation.

MASTER RESET

The $\overline{MR}$ line of the FD179X is used during a power-up condition when processor initialization is to take place. During the trailing edge of $\overline{MR}$, a RESTORE command (HEX 03) is jammed into the command register and executed at the slowest stepping rate. If a faster stepping rate is desired, this can be loaded

into the command register during the RESTORE, in which case the remainder of the steps will occur at the new selected rate until Track 00 is sensed. The minimum pulse width of $\overline{MR}$ is 50 μs.

DATA REQUEST

The Data Request line (pin 38) and the Data Request bit of the status register indicate valid data transfers. When performing any read command, it indicates that valid data is contained in the data register and the host processor may read this byte. In any write command, it indicates that the data register is empty and may be loaded by the host processor with a new data byte. If it is desired to have separate DRQ's to indicate "read" and "write" mode, the circuit of figure 2 may be used. Whenever RG is true, DRQ will be caused by a read operation. When false, DRQ must have been caused by a write operation.

DRQ is always reset when the Data Register is read or written to. DRQ is also reset when the Command Register is loaded with a new command, providing the FD179X is IDLE (Busy = 0).

HEAD LOAD TIMING

The Head Load Output (HLD) controls the movement of the R/W head against the media. When HLD = 1, the head is to be loaded against the disk. An internal 15 ms. delay allows for the head to fully engage. If the drive used requires more head load time, an external circuit must be used to increase this time delay. Figure 3 illustrates the use of a one-shot to perform this function. When the E flag of any Type II or III command is reset (E = 0), the internal 15 ms. delay is disabled and the HLT line is sampled immediately. The duration of the one-shot pulse width set by the Resistor/Capacitor combination selected will prevent a Logic "1" from appearing on HLT until the preset time has expired. The "AND" function of HLT and HLD appears in the status register as BIT 5 and may be used to avoid another time delay by informing the host processor that the R/W head is already engaged. This will speed up access when doing 2 consecutive READ SECTOR commands, for example. Regardless of the head load configuration used, HLT is always sampled for a Logic "1" before the current command is continued.

$\overline{TEST}$ INPUT

The $\overline{TEST}$ input of the FD179X is used when interfacing to voice-coil activated motors. In most applications, it may be tied high or simply left open by the user. When $\overline{TEST}$ = 0, the internal stepping rates are decreased to about 400 microseconds, the HLT internal 15 ms. delay is disabled, and acts as if the E flag was reset. Figure 4 shows a typical implementation of $\overline{TEST}$ when used with a voice-coil activated drive.

$\overline{DDEN}$ INPUT (1791 and 1793 only)

The Double Density Enable ($\overline{DDEN}$) pin is used to select single and double density operation. When $\overline{DDEN}$ = 1, single density is selected; when $\overline{DDEN}$ = 0, double density is selected. This line can be switched from 0 to 1 or from 1 to 0 at any time except when WRITE GATE (WG) is activated. IBM double density diskettes have TRACK 00 side 0 recorded in single density instead of double density. The "ANDING" of the $\overline{TR00}$ and a side 0 signal can be used to force $\overline{DDEN}$ to a Logic "1" when on TRACK 00. The $\overline{DDEN}$ (pin 37) of the 1792 and 1794 must be left open for proper operation.

COMMAND USAGE

Whenever a command is successfully or unsuccessfully completed, the busy bit of the status register is reset and the INTRQ line is forced high. Command termination may be detected either way. The INTRQ can be tied to the host processor's interrupt line, causing a system interrupt with an appropriate service routine to terminate commands. The busy bit may be monitored with a user program and will achieve the same results through software. Performing both an INTRQ and a busy bit check is not recommended because a read of the status register to determine the condition of the busy bit will reset the INTRQ line. This can cause an INTRQ from not occurring.

RESTORE COMMAND

On some disk drives, it is possible to position the R/W head outward past Track 00 and prevent the $\overline{TR00}$ line from going low unless a STEP IN is first performed. If this condition exists in the drive used, the RESTORE command will never detect a $\overline{TR00}$. Issuing several STEP IN pulses before a RESTORE command will remedy this situation. The RESTORE and all other Type 1 commands will execute even though the READY bit indicates the drive in not ready (NOT READY = 1).

READ TRACK COMMAND

The READ TRACK command can be used to manually inspect data on a hard copy printout. Gaps, address marks, and all data are brought in to the data register during this command. The READ TRACK command may be used to inspect diskettes for valid formatting and data fields as well as address marks. Since the 179X does not synchronize clock and data until the Index Address Mark is detected, data previous to this ID mark will not be valid. READ GATE (RG) is not actuated during this command.

READ ADDRESS COMMAND

In systems that use either multiple drives or sides, the read address command can be used to tell the

host processor which drive or side is selected. The current position of the R/W head is also denoted in the six bytes of data that are sent to the computer.

Track	Side	Sector	CRC Length	CRC 1	CRC 2

The READ ADDRESS command as well as all other Type II and Type III commands will not execute if the READY line is inactive (READY = 0). Instead, an interrupt will be generated and the NOT READY status bit will be set to a 1.

FORCED INTERRUPT COMMAND

The Forced Interrupt command is generally used to terminate a multiple sector command or to insure Type I status in the status register. The lower four bits of the command determine the conditional interrupt as follows:

I_0 = NOT-READY TO READY TRANSITION
I_1 = READY TO NOT-READY TRANSITION
I_2 = EVERY INDEX PULSE
I_3 = IMMEDIATE INTERRUPT

Regardless of the conditional interrupt set, any command that is currently being executed when the Forced Interrupt command is loaded will immediately be terminated and the busy bit will be reset indicating an idle condition. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred.

The conditional interrupt is enabled when the corresponding bit positions of the command (I_3-I_0) are set to a 1. If I_3-I_0 are all set to zero, no interrupt will occur, but any command presently under execution will be immediately terminated upon receipt of the Force Interrupt command (HEX D0).

As usual, to clear the interrupt a read of the status register or a write to the command register is required. The exception is when using the immediate interrupt condition (I_3= 1). If this command is loaded into the command register, an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the command register will not automatically clear the interrupt; another forced interrupt command with I_3-I_0 = 0 must be loaded into the command register in order to reset the INTRQ from this condition.

More than one condition may be set at a time. If for example, the READY TO NOT-READY condition (I_1 = 1) and the Every Index Pulse (I_2 = 1) are both set, the resultant command would be HEX "DA". The "OR" function is performed so that either a READY TO NOT-READY or the next Index Pulse will cause an interrupt condition.

FLOPPY DISK INTERFACE

READ GATE

The Read Gate output from the FD179X is used to inform the external data separator circuitry that a field of ones or zeros has been read off the disk. In FM mode, the RG signal will go high only after the following conditions are met:

1. The Head is loaded
2. HLT is at a Logic "1"
3. Settling time, if programmed, has elapsed
4. A field of zeros has been read off the disk

RG will be reset back to a zero upon a Master Reset ($\overline{MR}$) or upon receipt of any command including the Force Interrupt command when BUSY = 0, or upon a Force Interrupt command when terminating a multiple sector Read/Write command. For double density operation (MFM), the RG characteristics are as follows: Assume the FD1791/3 is searching for an ID field. When 4 consecutive bytes of zeros are detected, RG will be made active. RG will be reset upon any one of the following conditions:

1. 3 A1's with missing clocks not found within 16 bytes
2. HEX "FE" not found within the next byte
3. One byte after CRC
4. Invalid TRACK/SECTOR Address (only during a READ/WRITE sector command)

If the ID search was unsuccessful, the FD1791/3 will then continue the search for the specified ID field. When the correct ID field is encountered and if the current command was a WRITE SECTOR, RG will remain at a Logic "0". If the current command was a READ SECTOR, the FD1791/3 will then look for 4 consecutive bytes of zeros. If 4 bytes of zeros were not found, the FD1791/3 will do an internal retry. If 4 bytes are found within the next 33 bytes, RG will then be set to a Logic "1".

RG is now deactivated (RG = 0) upon one of the following conditions:

1. 3 A1's with missing clocks found within 16 bytes
2. HEX "FB" or "F8" not found within the next byte
3. After the CRC is read (successful completion)

Items 1 and 2 will result in an internal retry. RG is not activated during the Read Track command.

$\overline{VFOE}/\overline{WF}$

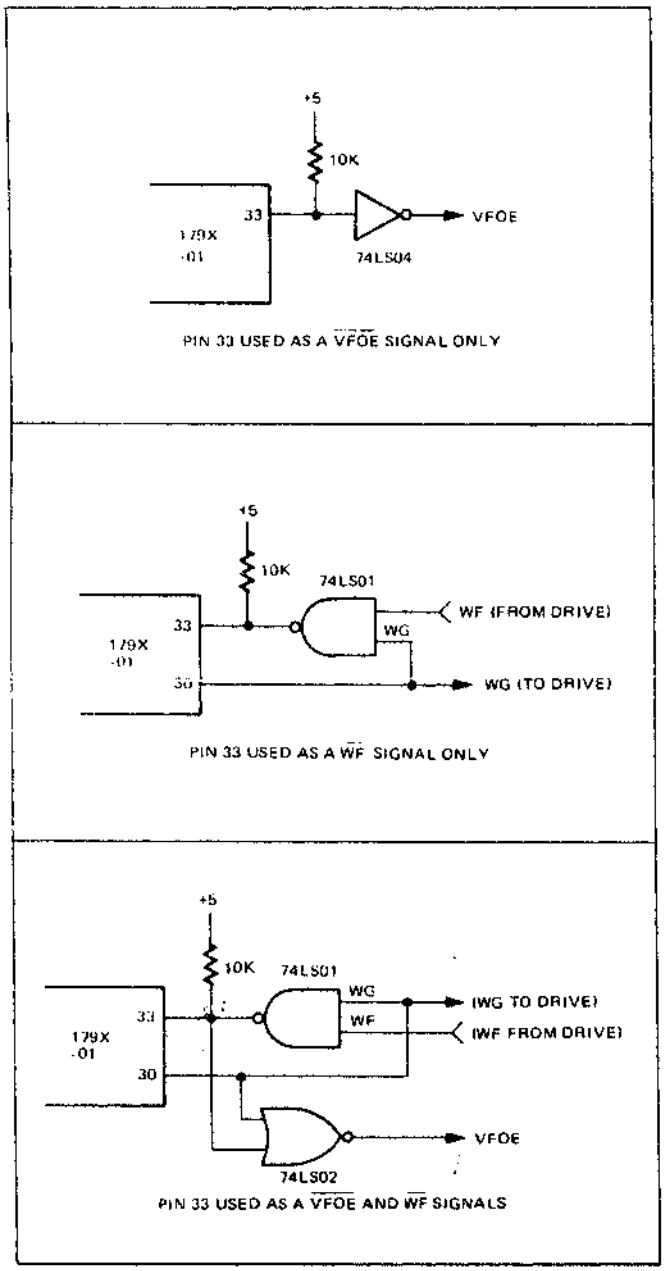
The 179X provides an additional signal that can be used to control the external data separator, $\overline{VFOE}/\overline{WF}$ (pin 33) is an input/output pin that functions as a VFO enable and a write fault signal.

When Write Gate (WG) = 1, pin 33 functions as an input to detect write fault conditions at the drive. If pin 33 is brought low when WG = 1, the current Write command is terminated and the INTRQ is activated. The write fault status bit is then set indicating a failure in drive electronics.

When WG = 0, pin 33 functions as an output, pin 33 will go active (Logic "0") when the following conditions are met:

1. Head is loaded
2. Settling time, if programmed, has elapsed
3. Data is being inspected off the disk

The VFOE signal can be used to control RCLK. When VFOE = 0, RCLK should be allowed to free run; when VFOE = 1, RCLK should be forced low. The following circuits can be used to separate $\overline{VFOE}$/$\overline{WF}$ signals.



RAW READ

The $\overline{RAW\ READ}$ input should be supplied a negative going pulse for every clock or data bit recorded on the media. The normal pulse width is 100 to 200 ns. but may be any pulse width providing the pulse occurs entirely in the read clock window.

When flux reversals are totally non-existant (i.e., head is disengaged), the external separator should ensure that the $\overline{RAW\ READ}$ is held at a Logic "1".

RCLK

The READ CLOCK signal must be supplied from an external data separator and is used to "frame" each $\overline{RAW\ READ}$ transition. The FD179X will determine whether the $\overline{RAW\ READ}$ pulse is clock or data, so the active state of RCLK is unimportant (i.e., high or low during $\overline{RAW\ READ}$). RCLK transitions must be phased with $\overline{RAW\ READ}$ either by a counter/separator, or phase lock loop configuration.

For proper operation, RCLK must be a minimum of 800 ns. high and 800 ns. low. For 8" MFM, this requires a 50-50 RCLK window. VFO's that operate in the 8-16 MHz range are recommended. When switching RCLK from one source to another, great care must be exercised to ensure this 800 ns. margin. Figure 5 shows the $\overline{RAW\ READ}$ and RCLK timing relationships. When $\overline{VFOE}$ = 1 RCLK should be forced low, and free-running when $\overline{VFOE}$ = 0.

WRITE PRECOMPENSATION

Write precompensation is a technique where the WRITE DATA (both clock and data) is written in a direction opposite of the anticipated bit shift. It is generally required for 8" MFM recording and is usually not used for FM single density. Write precompensation may be obtained by the use of external circuitry in conjunction with WD, EARLY and LATE. The algorithm for write precompensation is shown in figure 6. The external logic required is in the form of delay circuits or one shots. As a general rule, write precompensation is done only on Tracks 44-77, but may be required on all tracks if specified by the drive manufacturer.

Figure 8 illustrates a precomp circuit using the Western Digital 2143 4-phase clock generator. The timing relationships are shown in figure 9. The early, late or nominal condition is latched into the 74LS175 on the rising edge of WD. This fires the 2143 via its OSC in (pin 11) line and starts the 4-phase generation. Depending upon the condition, the resultant WD is generated by Ø2 on nominal, Ø1 on early, or Ø3 on late. The Ø4 output resets the latch in anticipation of the next WD pulse. The 7438 is an open collector device and requires a pull-up resistor if not supplied at the drive. A 5K potentiometer is used to adjust the desired pulse width.

DATA SEPARATION

The FD179X requires an external data separator. Data separators range from the counter/one-shot

technique to phase lock loops. The choice of separator design is dependent upon data reliability and system cost.

The FD179X requires a $\overline{\text{RAW READ}}$ signal which is a negative going pulse for every flux reversal, and a Read Clock (RCLK) signal to indicate flux reversal spacing. $\overline{\text{RAW READ}}$ must be a minimum of 100 ns. and RCLK (high or low) at 800 ns. Because of high flux reversal rates, Write Precompensation with a Phase Lock Loop separator is recommended for 8" MFM applications.

Figure 10 illustrates a counter separator. This circuit uses a crystal clock and Read Gate (RG) is not used. Figure 11 shows the timing of the circuit. Any negative $\overline{\text{RAW READ}}$ transition loads the counter with a "5". When the counter counts down to zero, the RCLK flip-flop (74LS74) toggles, producing a RCLK. If the next data bit is zero (no $\overline{\text{RAW READ}}$ pulse), the counter continually counts down until another $\overline{\text{RAW READ}}$ pulse occurs. Then it is loaded again and the process repeats. Many users are using this circuit and are achieving error rates better than 10^{-8}, even for 8" MFM with write precompensation. This circuit may also be used for the 5" mini-floppy.

Figure 12 illustrates a phase lock loop method of data separation. The advantage of this scheme over counter/separators is its excellent data recovery and high reliability. The RCLK "tracks" the $\overline{\text{RAW READ}}$ transitions, allowing for greater flexibility in bit shifts and overall system margins. Although the PPL arrangement is preferred, its added component count generally limits its use to 8" MFM and FM applications.

DATA RECOVERY

Occasionally, the R/W head of the disk drive may get "off track", and dust or dirt may get trapped on the media. Both of these conditions will cause a RECORD NOT FOUND and/or a CRC error to occur. This "soft error" can usually be recovered by the following procedure:

1. Issue the command again
2. Unload and load the head and repeat step
3. Issue a restore, seek the track, and repeat step 1

If RNF or CRC errors are still occurring after trying these methods, a "hard error" may exist. This is usually caused by improper disk handling, exposure to high magnetic fields, etc. and generally results in destroying portions or tracks of the diskette.

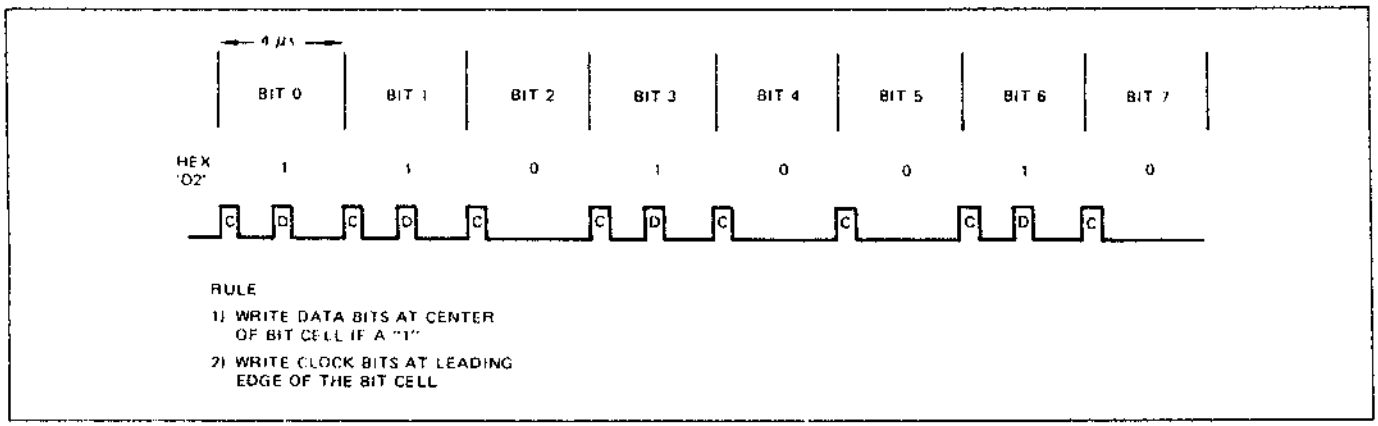


FIGURE 1A. FM RECORDING

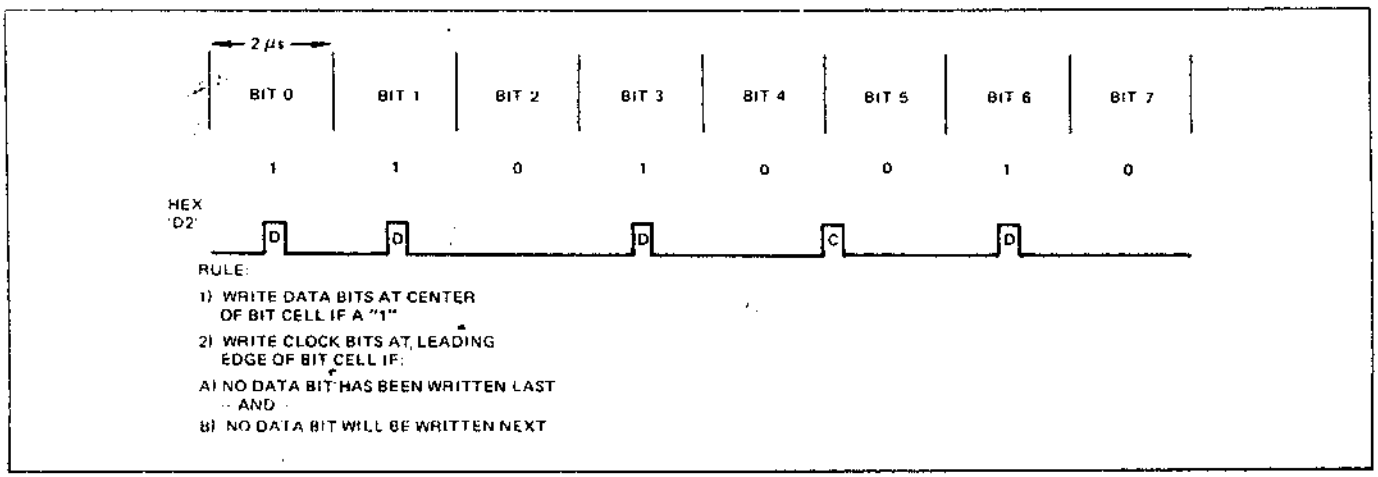


FIGURE 1B. MFM RECORDING

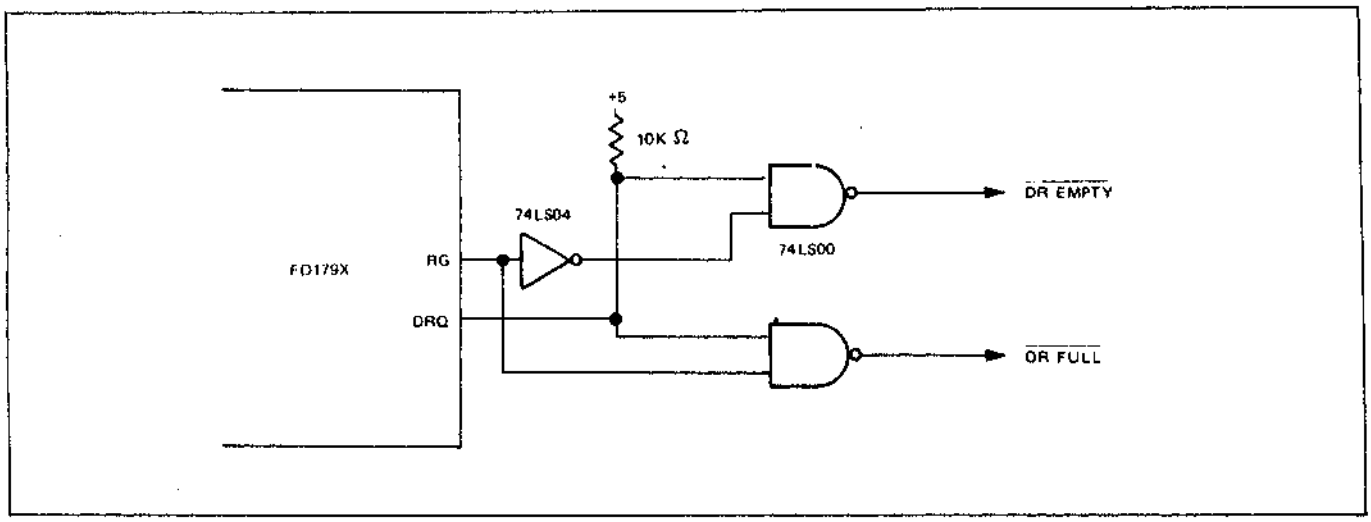


FIGURE 2. FORMING SEPARATE READ AND WRITE MODE SIGNALS FROM DRQ

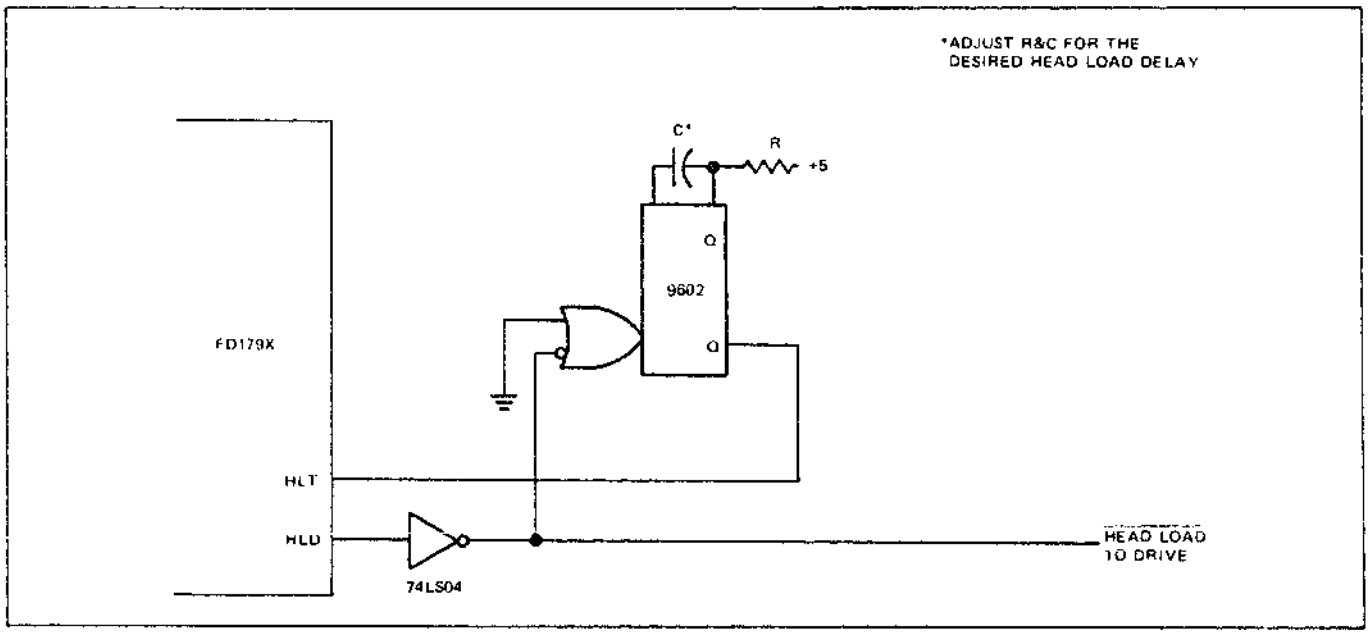


FIGURE 3. CONTROLLING HEAD LOAD TIMING

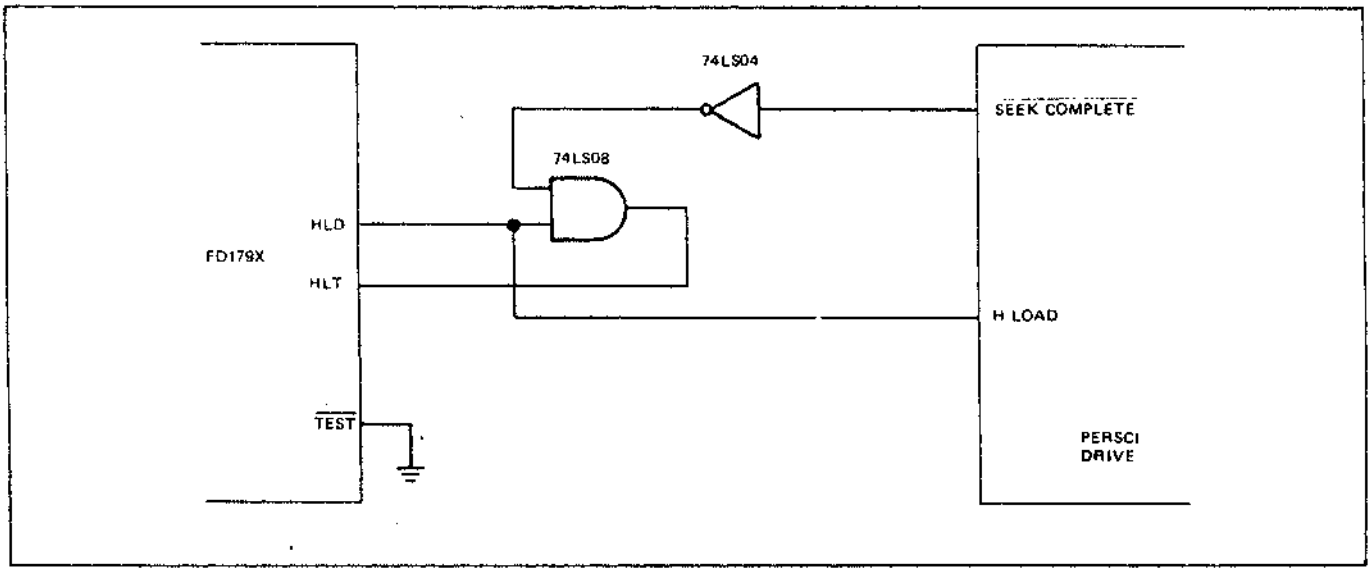
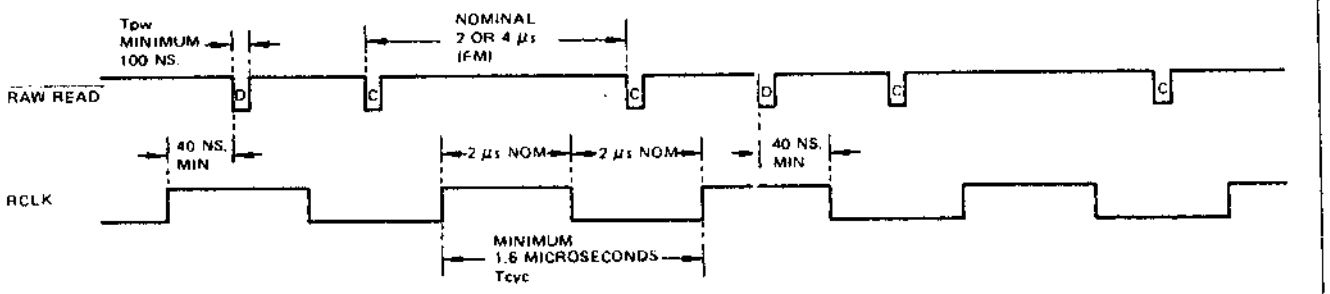


FIGURE 4. INTERFACING TO VOICE-COIL ACTIVATED DRIVES



NOTES

1) Tcyc SHOULD NEVER FALL BELOW 1.6 MICROSECONDS (50-50 DUTY CYCLE)

2) RCLK MUST BE FREE RUNNING WHEN $\overline{VFOE}$ = 0

3) Tpw MAY OVERLAP IN BOTH WINDOWS IF Tpw < 300 NS. (MFM) OR Tpw < 600 NS. (FM)

FIGURE 5. READ DATA TIMING

Already Sent		Sending	To Be Sent	MFM	FM
X	1	1	0	Precomp Early	Precomp Early [1]
X	0	1	1	Precomp Late	Precomp Late [1]
0	0	0	1	Precomp Early (Inhibit During A1 & C2) [2]	N/A
1	0	0	0	Precomp Late (Inhibit During A1 & C2) [2]	N/A

X = Don't Care
N/A = Not Applicable
1 = Inhibited during missing clocks
2 = With missing clock transitions (Address marks)

FIGURE 6A. INTERNAL WRITE PRE-COMP ALGORITHM

Early	Late	Precomp Required
1	0	Do not Delay WD
0	0	Delay WD By Δ
0	1	Delay WD by 2 Δ

Notes:
All other Early/Late conditions are illegal. Δ = 100 — 150 ns. depending upon drive manufacturer. See figure 7 for timing with Early/Late.

FIGURE 6B. PRE-COMP CIRCUIT REQUIREMENTS

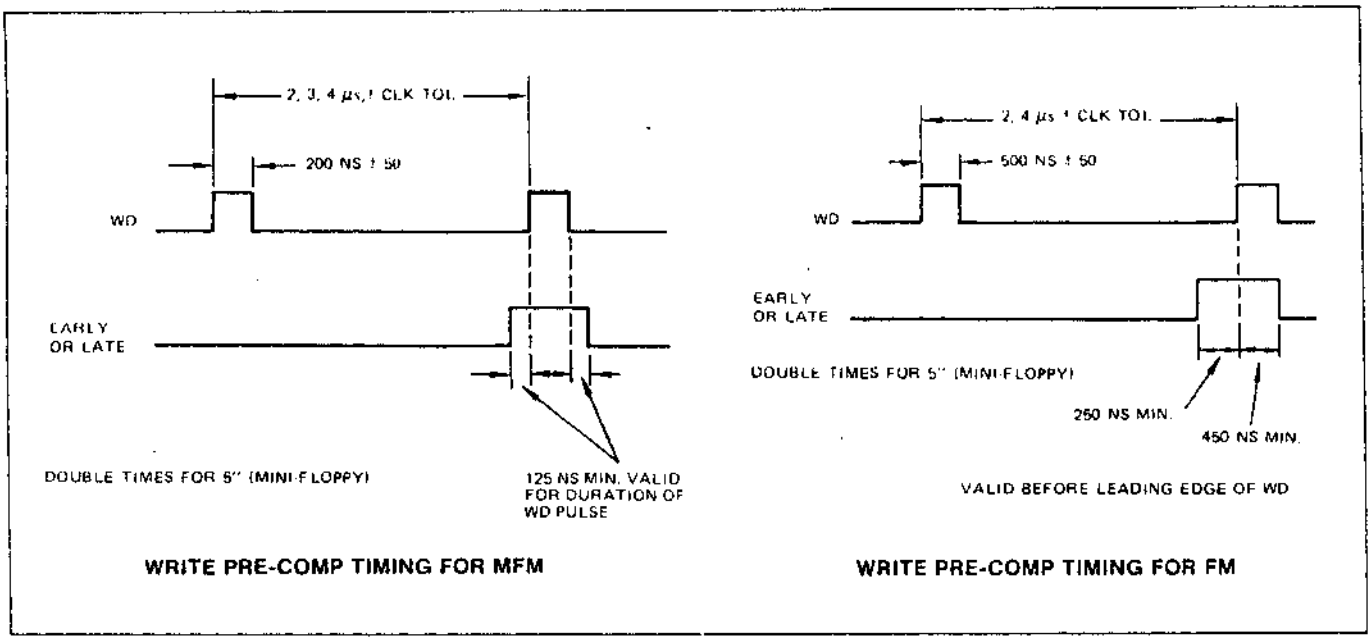


FIGURE 7. WRITE PRE-COMP TIMING

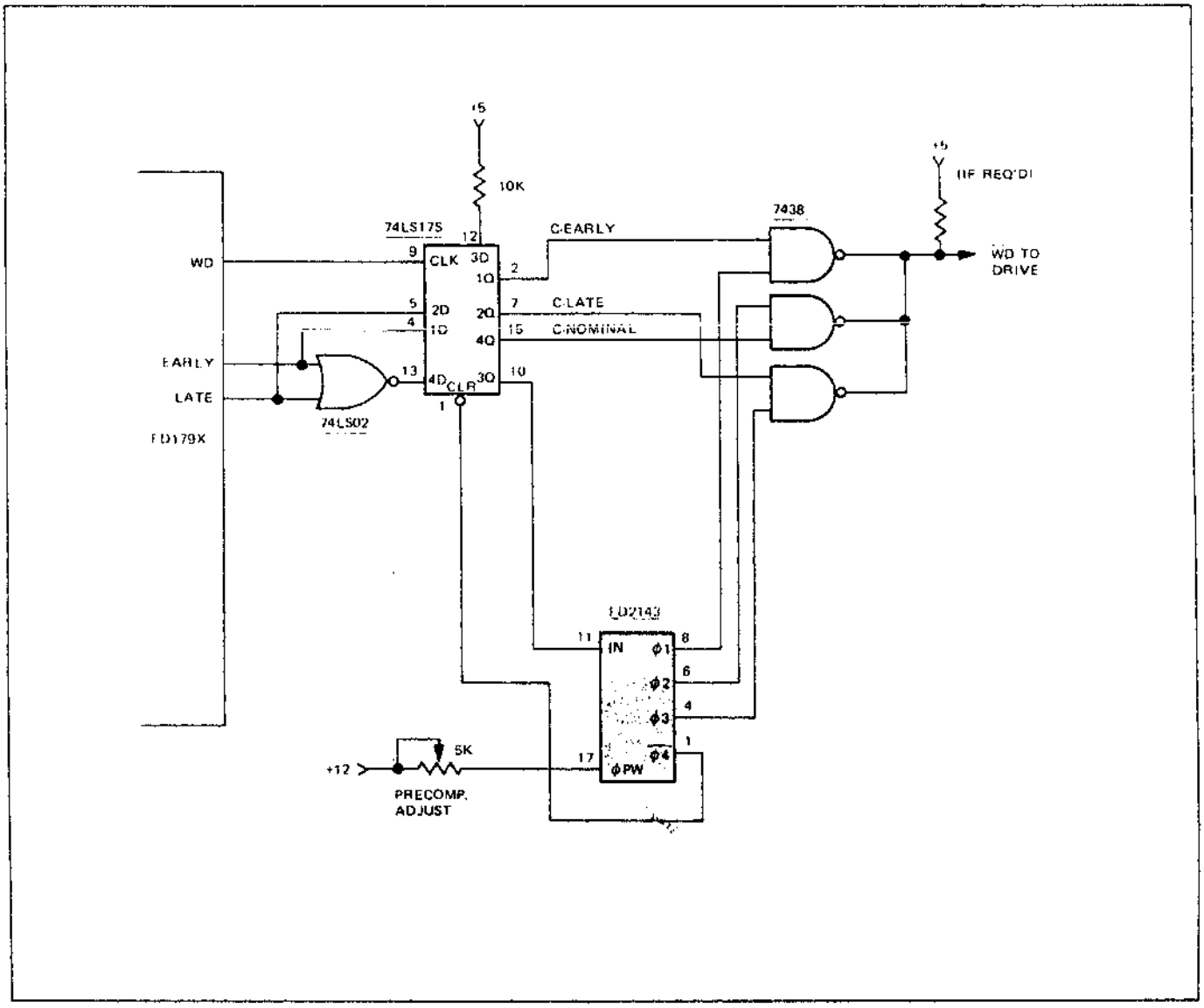


FIGURE 8. 179X WRITE PRE-COMP

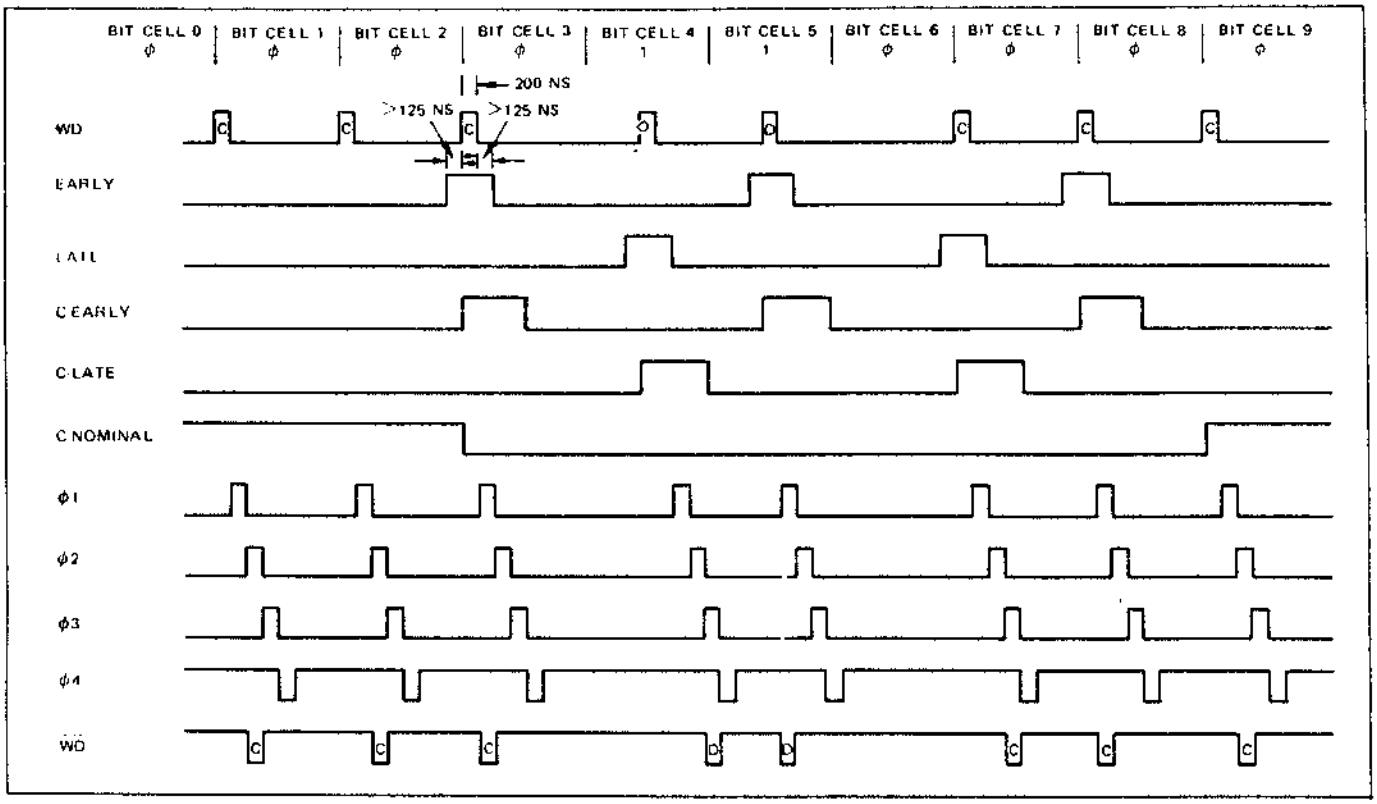
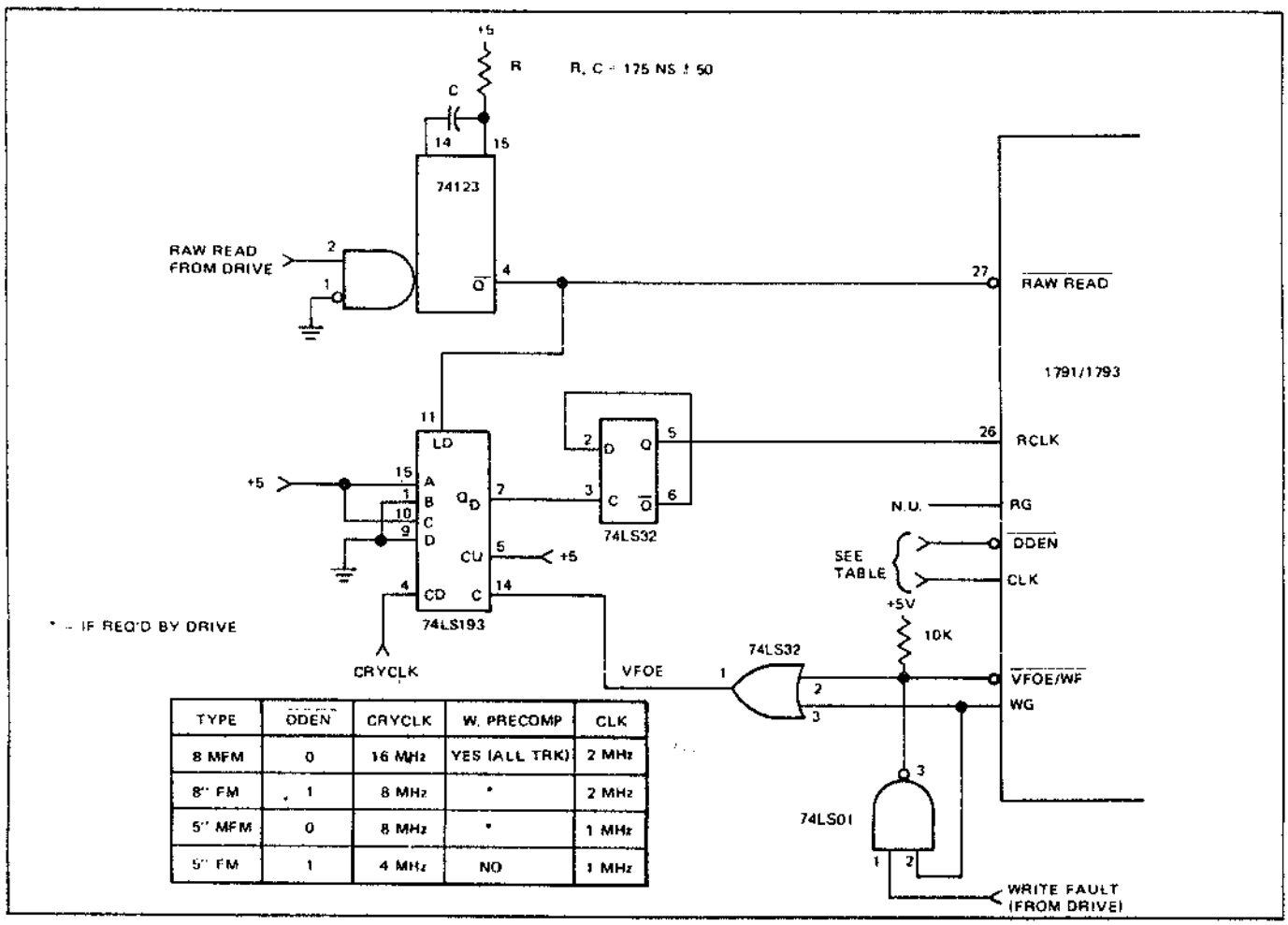


FIGURE 9. WRITE PRE-COMP TIMING



TYPE	ODEN	CRYCLK	W. PRECOMP	CLK
8 MFM	0	16 MHz	YES (ALL TRK)	2 MHz
8" FM	1	8 MHz	*	2 MHz
5" MFM	0	8 MHz	*	1 MHz
5" FM	1	4 MHz	NO	1 MHz

FIGURE 10. COUNTER/SEPARATOR

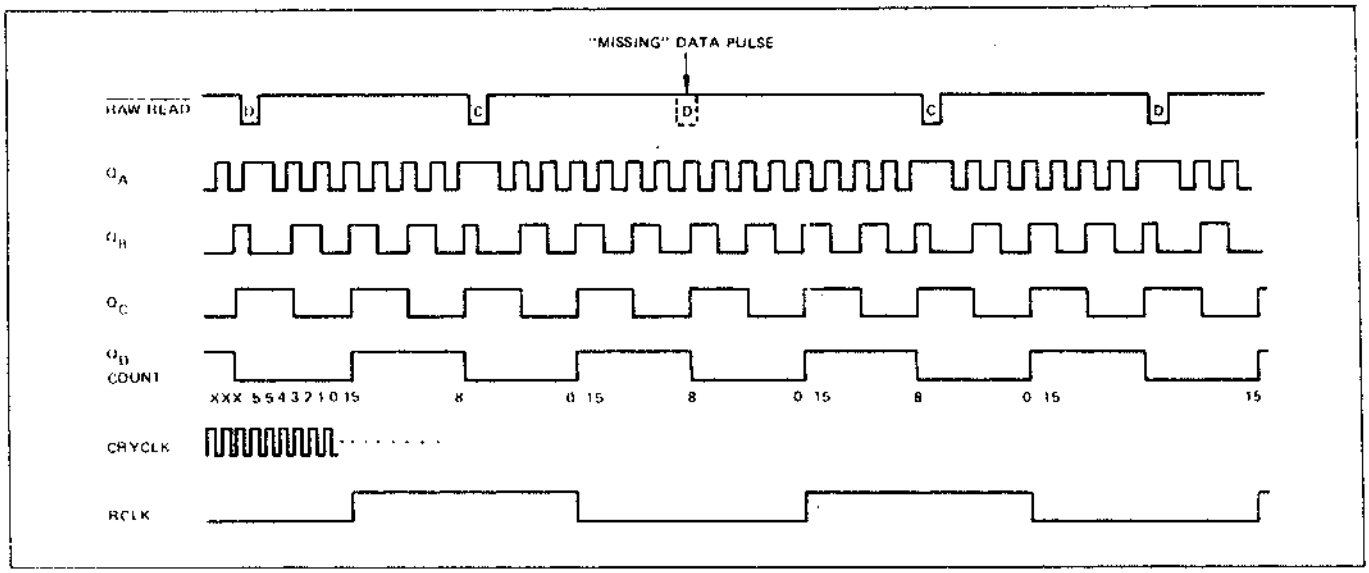


FIGURE 11. COUNTER/SEPARATOR TIMING (8" FM SHOWN)

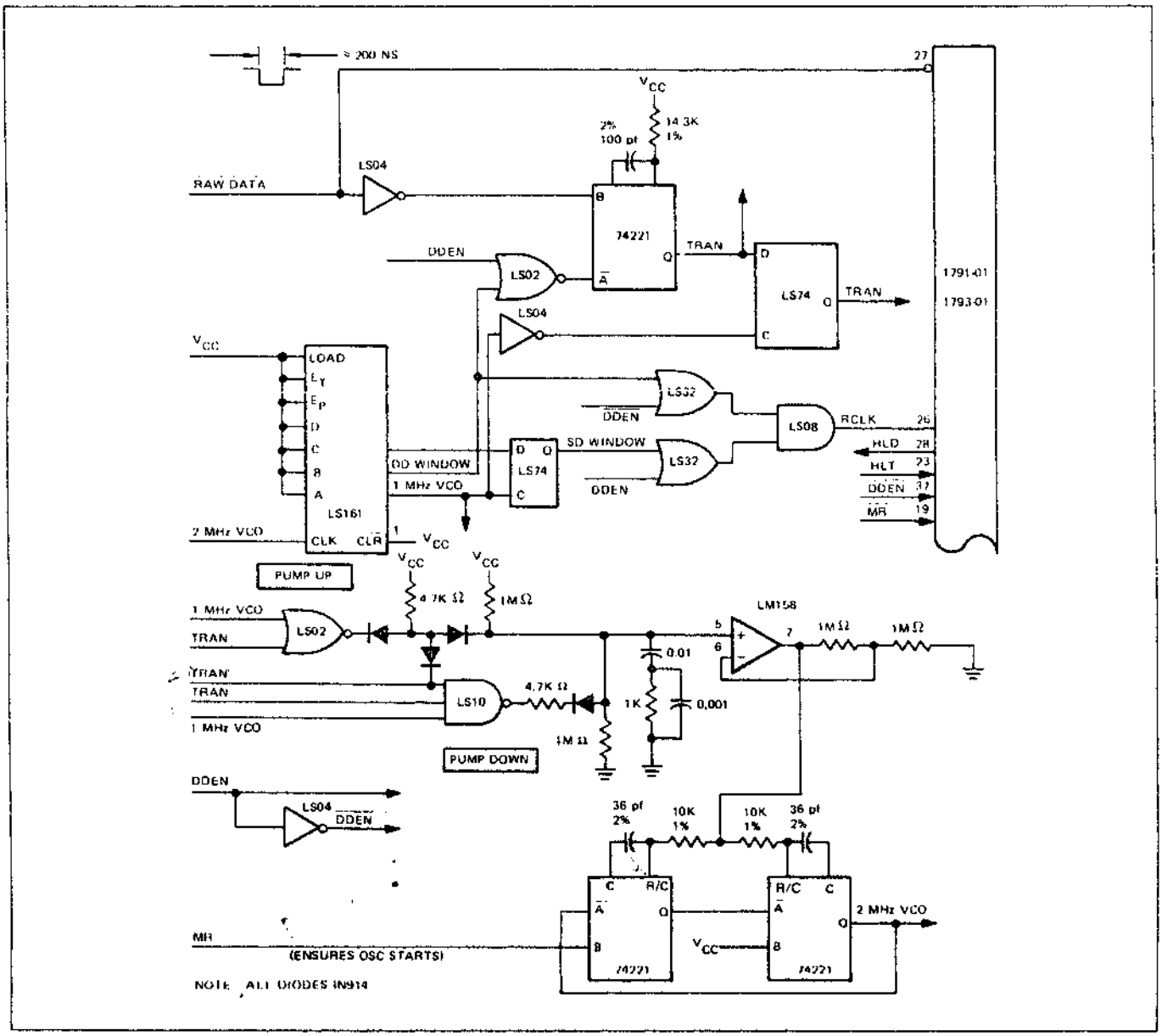


FIGURE 12. ANALOG PLL (FM & MFM) FOR 1791-01 OR 1793-01

REV	DESCRIPTION	DATE	APPR.
E	CORRECT U71 ENABLE PROBLEM DURING MEMORY WRITING	12/5/79	B Tarbell
F	BOOTSTRAP CIRCUIT CHANGE IMPROVED DATA SEPERATOR	6-21-80	B Tarbell

SPARE LOGIC

CLOCK DATA SEPERATOR PRECOMPENSATION CIRCUITS

U31 1793

U29 8257

U28 8208 · U69 74LS373 · U68 74LS373 · U72 8208 · U71 8208

TARBELL DOUBLE DENSITY DISK INTERFACE

SCALE: ~ · APPROVED BY: · DRAWN BY Mitchell

DATE: 3-11-80 · REVISED

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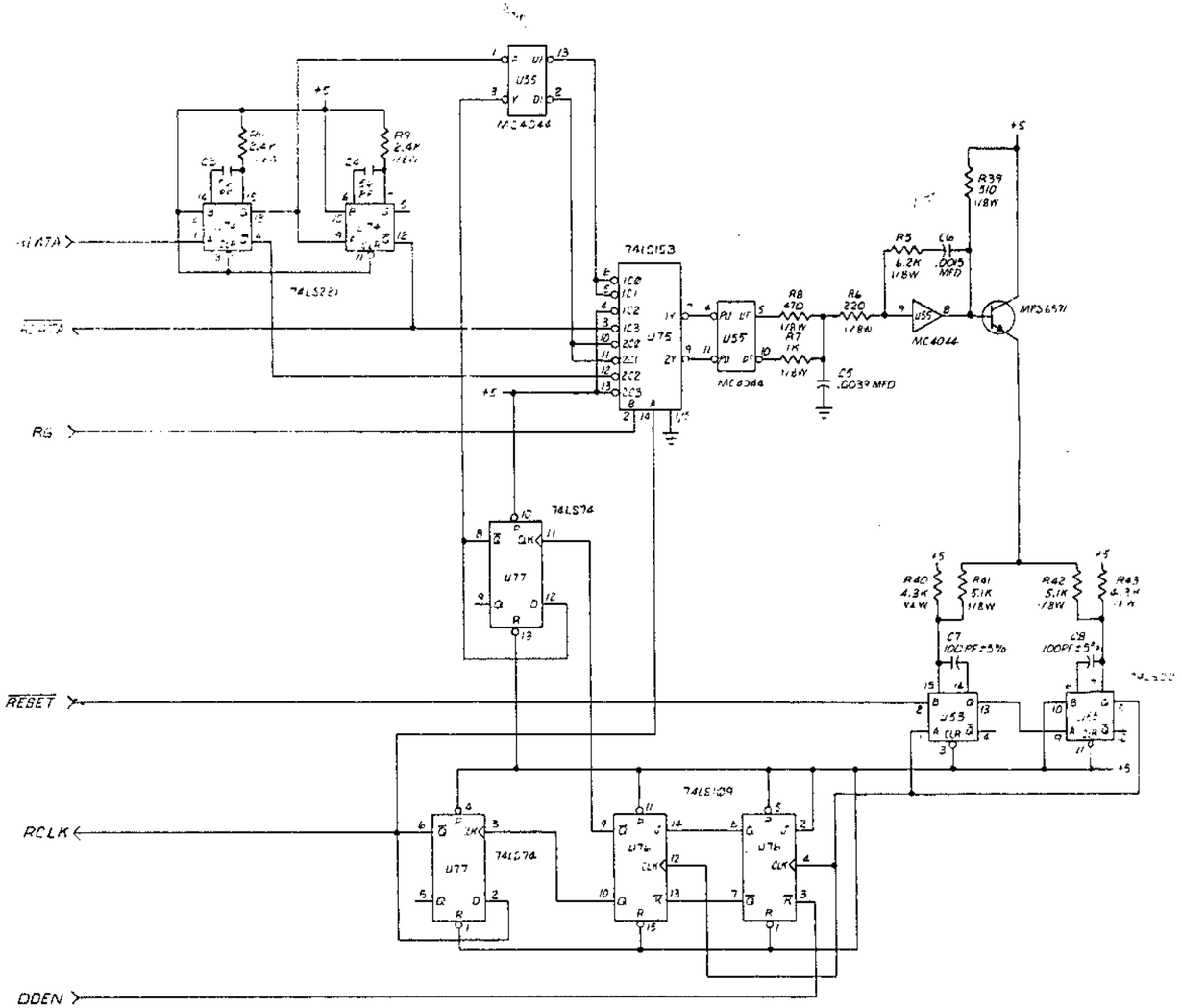

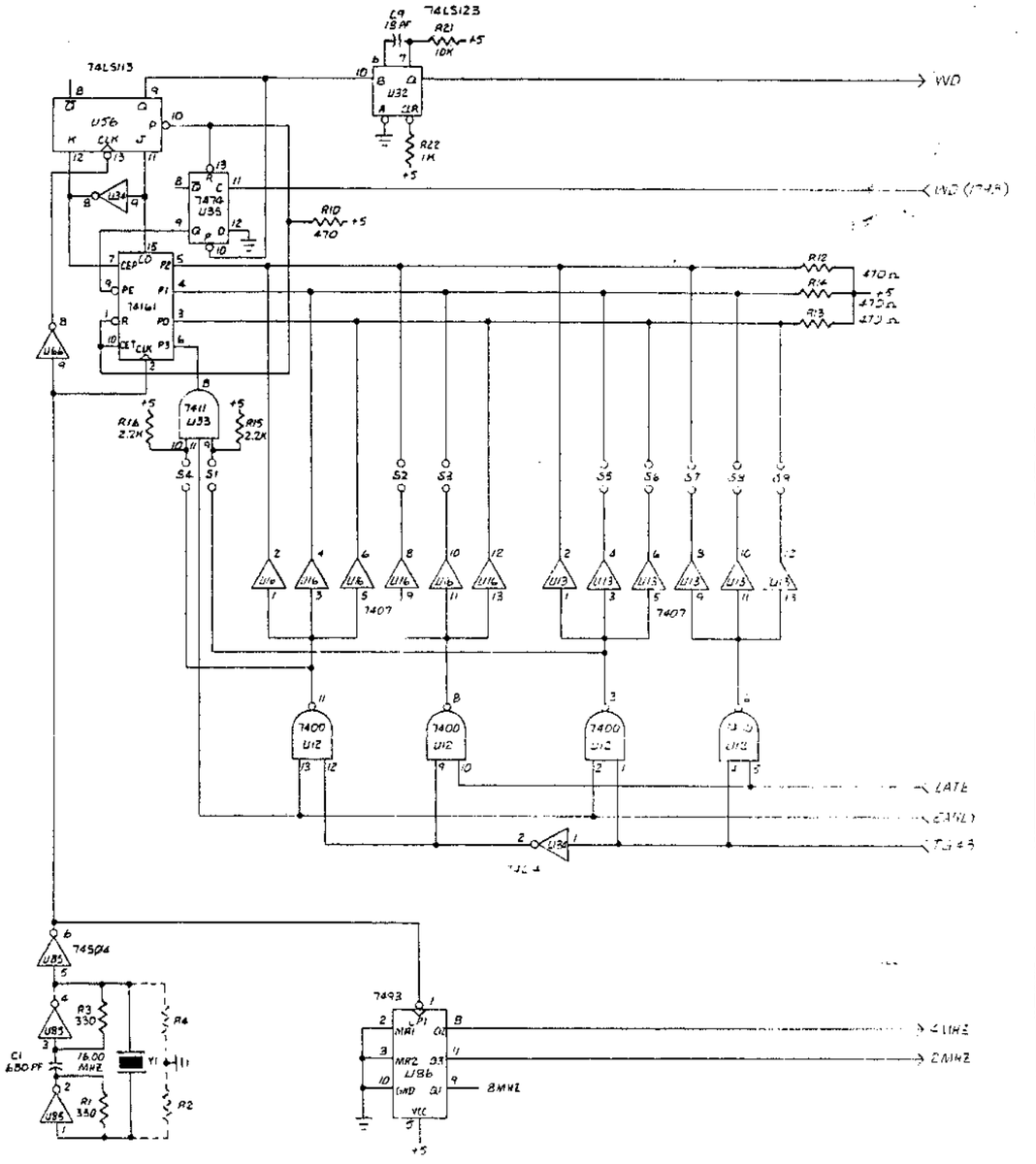

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DATE: 6-[illegible]-80		REVISED

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