My "HomeBrew" I/O card

My "homebrew" I/O card began life as a "Solid State Music" I/O-PROM-UNIVERSAL card. It had a couple of "open" areas and was designed so that you could add a little circuitry if you needed to.

Originally intended to have a single AY-5-1013 UART added to it, I instead put on two 8251 uarts with associated baudrate clock generator and RS-232 interfaces (made with op-amps).

Fortunately the original card was designed to be flexible, and even chips which had been "designated" were on general purpose pads - as you can see from the photos, I modified the circuitry quite extensively...

The following pages contain the original documentation for the Solid State Music card. The last handwritten page contains a few notes on my changes, which appears to be the only documentation that I have remaining.

B 6/23/77

Solid State Music
Assembly Instructions © 1976 I/O-PROM-UNIVERSAL CARD

This card was designed to provide an I/O interface for the Altair 8800 computer. Additional pads have been provided to facilitate the addition of EROMs, a UART, RAMs or other circuits as required. The basic kit provides the necessary parts for the implementation of two I/O ports. Other kit options are being prepared for supplementary functions such as TTY interface, video monitor interface, etc.

Figure 1 shows the layout of the committed areas for the I/O and the uncommitted areas for other circuitry.

1.0 I/O Card Connections (refer to figures 2,4 & 5)

1.1 Jumpers. If this card is used for I/O functions a few connections have to be made on the board with jumpers first.

(a) Connect "SM" (U5, pin 12) to the 1K ohm pull-up resister (5 pads-1.25" to the right of the letters "SM" and up 0.625" on the front side of the board.)
(b) Connect "SO" (edge conn. pin 45) to "SOUT" (U6 pin 5).
(c) Connect "SI" (edge conn. pin 46) to "SINP" (U6, pin 9).
(d) Connect "OUT STB" (5 pads) to pin 13(DS2) of all of the 8212 IC's that will be used as output ports.
(e) Connect "INP STB" (5 pads) to pin 13(DS2) of all of the 8212 IC's that will be used as input ports.

1.2 Port (address) Selection. The Altair Computer can drive up to 256 input or output ports by decoding eight of the sixteen output address lines from the Intel 8080 CPU chip. The 8-line address decoder (SN74L42) on the Universal Card can enable up to eight consecutive port devices in the range of "0" to "255".

As shown on figure 4, U3 drives up to eight ports in a group range selected by jumpers (or Dip Switch) at U7. If you want to select ports numbered 0 thru 7, then the code for U7 is "00000" and no jumpers are needed for U7 (pins 12 thru 16 connected over to pins 5 to 1). Note: U7, pin 16 is the most significant bit and U7, pin 12 is the least significant bit of the group address for the ports.

kBD = 07

1.2 Cont'd

	U7 selects the group address, pins					U3 selects the port address within a group		
	16	15	14	13	12	C	B	A
Binary value	MSB 128	64	32	16	LSB 8	4	2	1

To connect the addressing circuit to the port, place a jumper from 1 (DS1) of the 8212 IC to pins 1 thru 7 or pin 9 depending on what address you want that port to be.

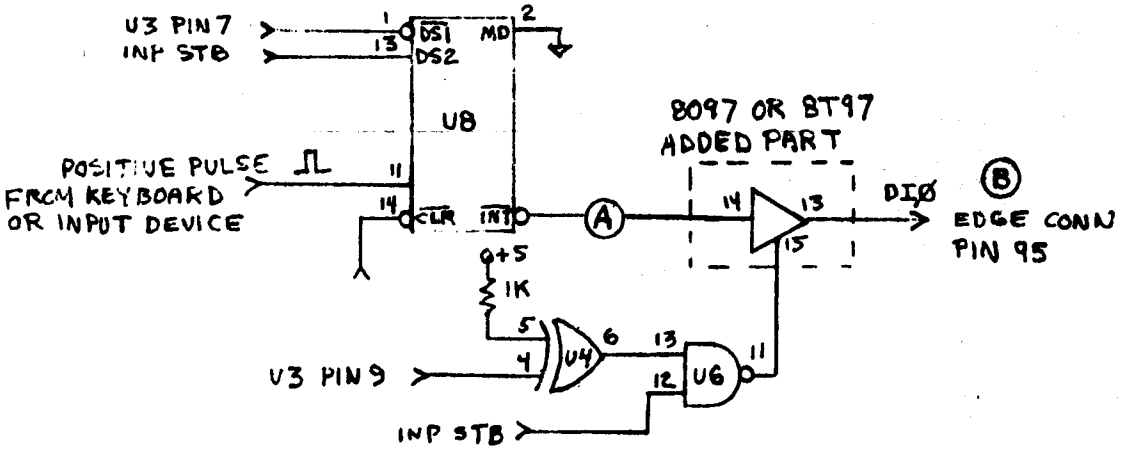
1.3 To select PORT RANGE	JUMPERS, U7 pins 16 to 1	pins 15 to 2	pins 14 to 3	pins 13 to 4	pins 12 to 5
0 thru 7	none	none	none	none	none
8 thru 15	no	no	no	no	yes
16 thru 23	no	no	no	yes	no
24 thru 31	no	no	no	yes	yes
32 thru 39	no	no	yes	no	no
248 thru 255	yes	yes	yes	yes	yes

1.4 To select PORT NUMBER within a selected range:

Make port drive connections to the following pins of U3 (74L42)

1st port - pin 9
2nd port - pin 7
3rd port - pin 6
4th port - pin 5
5th port - pin 4
6th port - pin 3
7th port - pin 2
8th port - pin 1

1.5 PARALLEL INPUT PORT (MITS Rev. 1)



The 8212 (U8) is used as an input port at address 001 in this configuration. The keyboard or inputing device should provide a positive pulse for a DAV (data available) strobe to place data into the 8212. If your DAV is negative, invert it with a 7404. The added DM8097 device is used as a one-bit input port at address 000 as a status flag.

1.6 PARALLEL INPUT PORT (Processor Tech. Corp compatible)

The same as MITS Rev. 1 circuit except at Ⓐ, add an inverter (7404) between U8 pin 23 and the DM8097 pin 14. Also, move Ⓑ connection to pin 93 (instead of 95) which will give a "DI6" bit.

1.7 PARALLEL INPUT PORT (IMSAI 8080 compatible)

Same as MITS Rev. 1 circuit except add an inverter (7404) between pin 23 of U8 and pin 14 of the DM8097. Then change Ⓑ connectinn to pin 93. Then connect pin 1 of U8 to pin 6 of U3 and pin 4 of U4 to pin 5 of U3.

1.8 Types of Ports. For additioal information on some port configurations that can be constructed with the 8212 IC get a copy of the "8212 Eight-Bit Input/Output Port..... Microcomputer Peripherals-Schottky Bipolar" pamphlet from Intel Corp., 3065 Bowers Ave., Santa Clara Ca.

2.0 1K/2K PROM CARD CONNECTIONS (refer to figures 3 & 4)

2.1 Jumpers. If this card is used for PROM functions, a few connections have to be made on the board with jumpers first.

(a) Connect "SM" (U5, pin 12) to pin 47 (edge conn. pin near "SI").
(b) Connect the data outputs of the 1702A type PROM to the appropriate data input lines (edge conn. pins) of the Altair bus.
(c) Connect the address lines (edge conn. pins) A0 to A7 to the appropriate address pins on the 1702A.

2.2 Speed Considerations. The Altair Computer uses a 2 MHZ clock to time all its functions which gives a single cycle period of 500 nsec. If the PROM you are using has an output data access time of greater than 500 nsec, then a slow-down circuit has to be built on the unused part of this card or the computer will not be able to read the PROM. (See appendix 1 for a slow-down circuit.)

2.3 PROM Addressing. The addressing of PROM is similar to Port Selection as described in this pamphlet.

	U7 selects the starting page (256 bytes) address, pins					U3 selects up to 8 pages (PROMs).		
	16	15	14	13	12	C	B	A
Binary value	MSB 32, 768				2048			LSB 1024 256

2.3 Cont'd

Connect the outputs of U3 (pins 1 thru 7 and 9) to the chip select (CS) pin of the PROM. Note: U3 pin 9 is the enable for the first page, U3 pin 7 is the second page enable, etc.

3.0 Parts List

	preferred part	alternate
U1	SN7485	
U2	SN74LS04	SN74L04,
U3	SN74L42	SN7442, 74LS42
U4	SN7486	
U5	SN74L00	74LS00
U6	SN74L00	74LS00
U7	Dip Switch (8)	Jumper
U8	Intel 8212	74S412
U10	Intel 8212	74S412

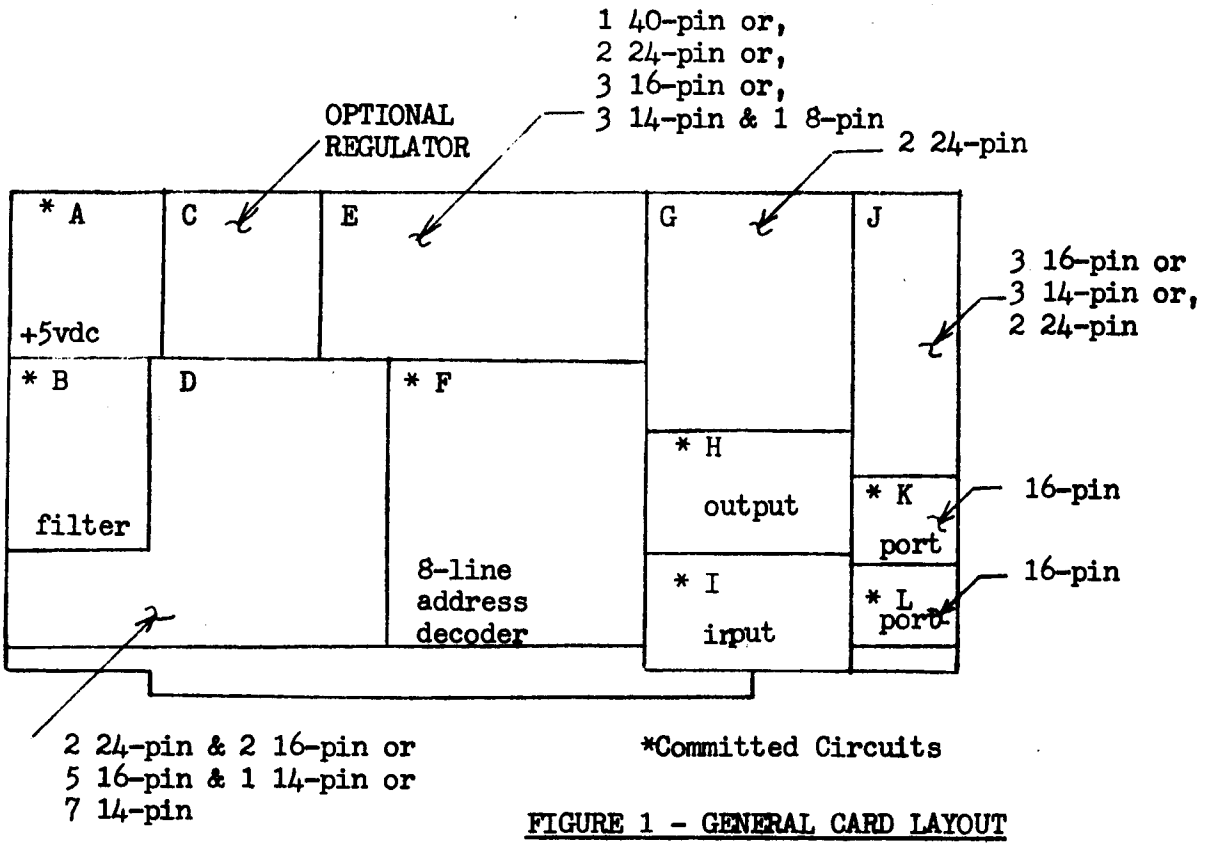


FIGURE 1 - GENERAL CARD LAYOUT

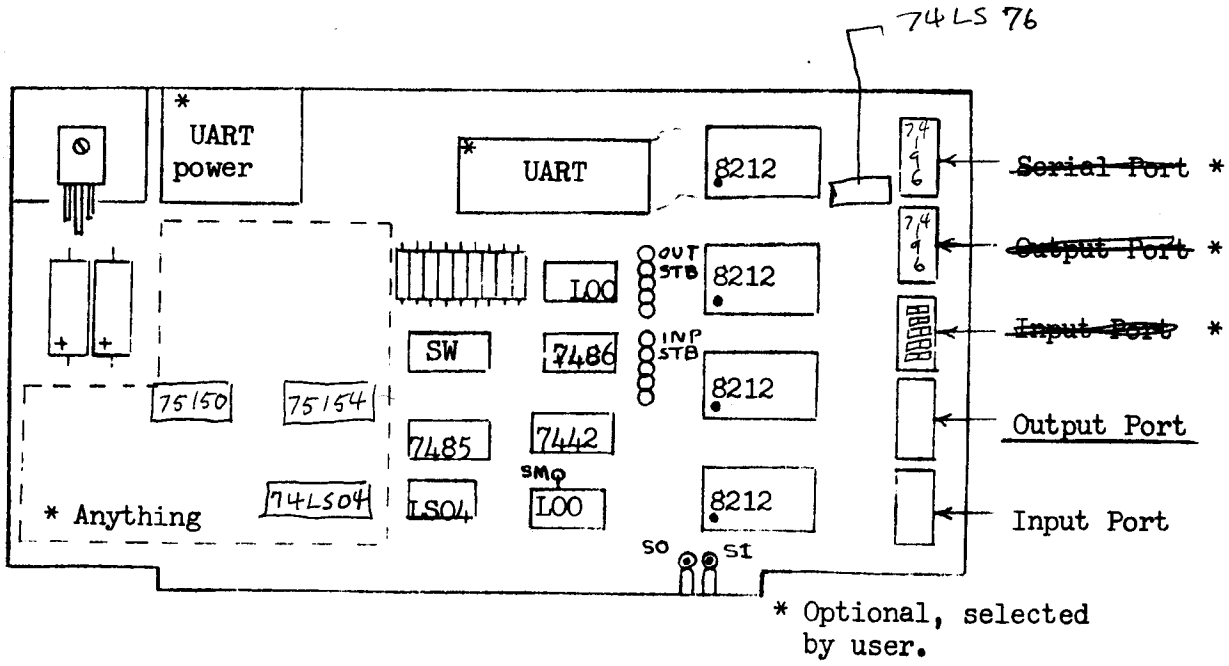
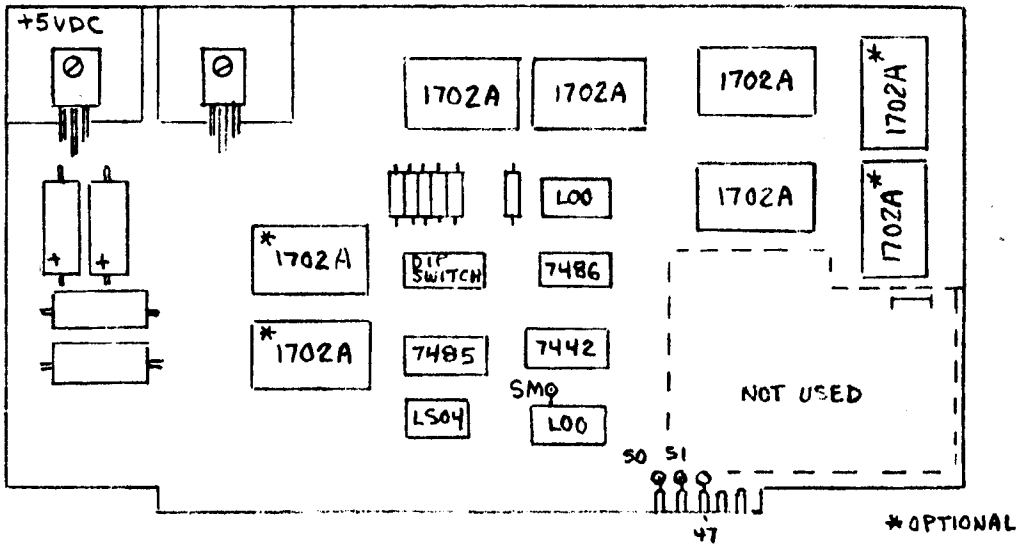
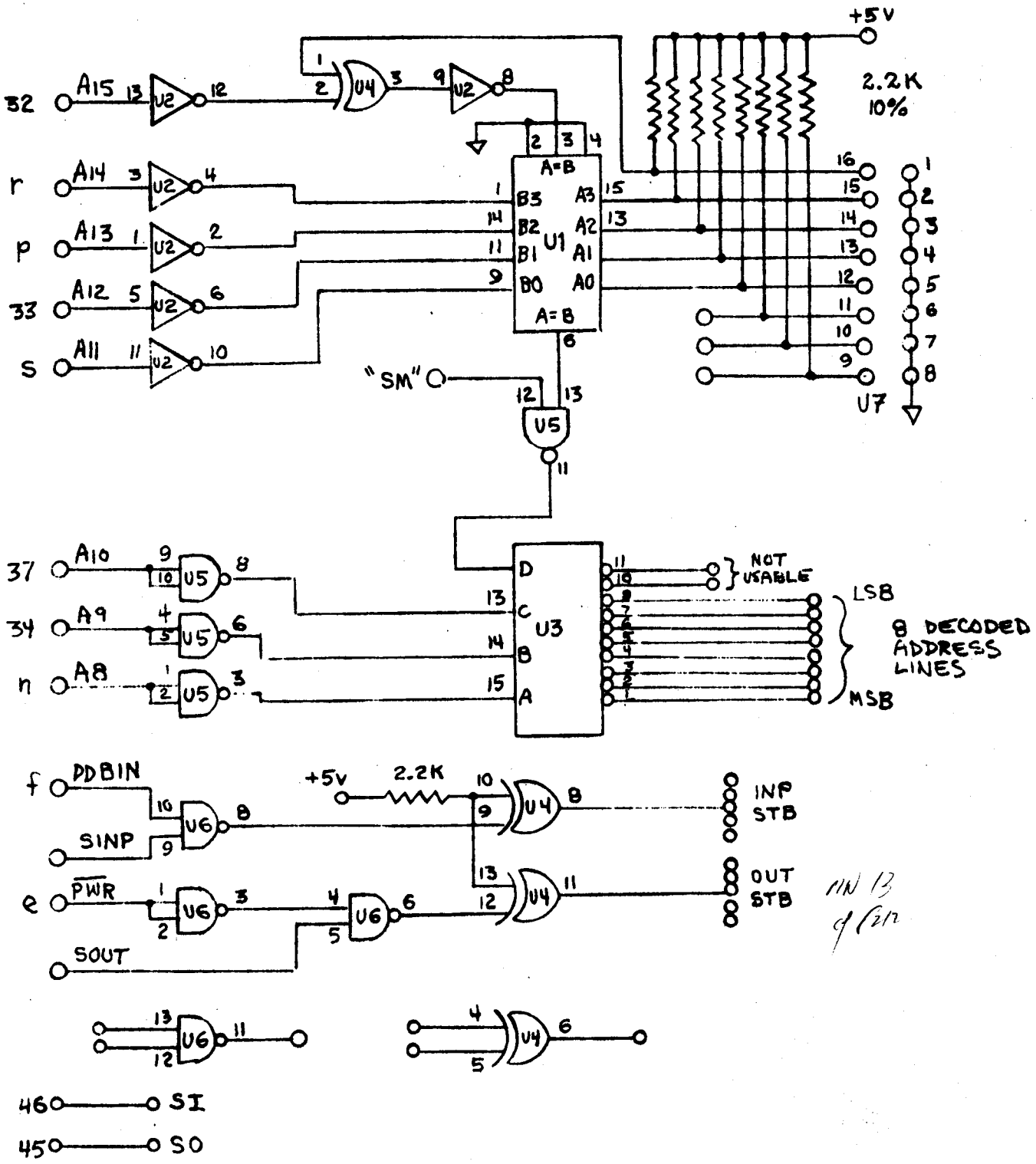


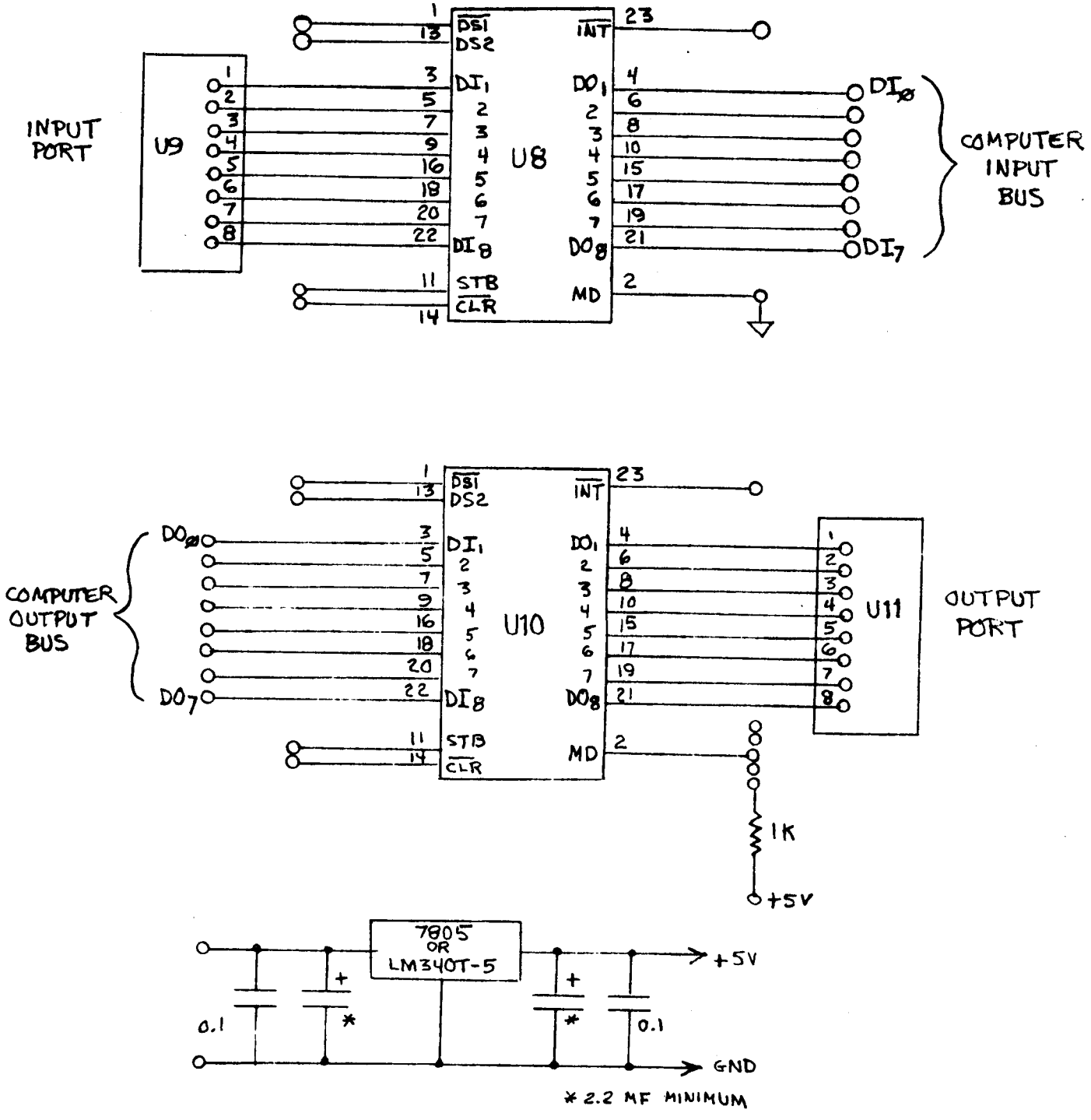
FIGURE 2 - I/O CARD LAYOUT



1K/2K PROM CARD LAYOUT - FIG 3

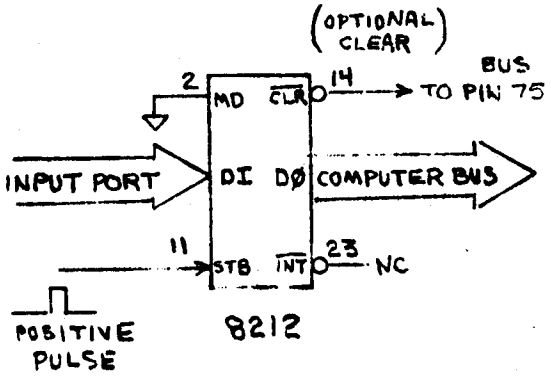


8-LINE ADDRESS DECODER-FIG 4



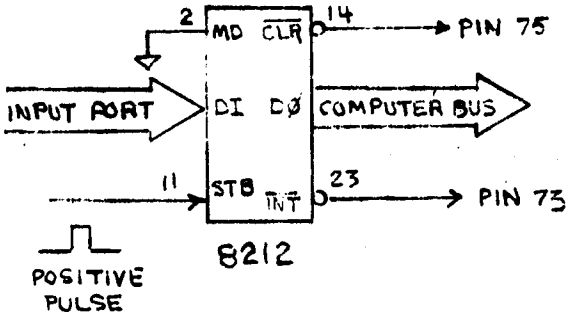
I/O IC SCHEMATIC-FIG. 5

The 8212 IC is an eight-bit Latch with a special moda control circuit and tri-state outputs. With pin 2 (MD) of the 8212 connected to ground the IC will act as an input device with data loaded in to the latch on trailing edge of a positive pulse to pin 11 (STB).



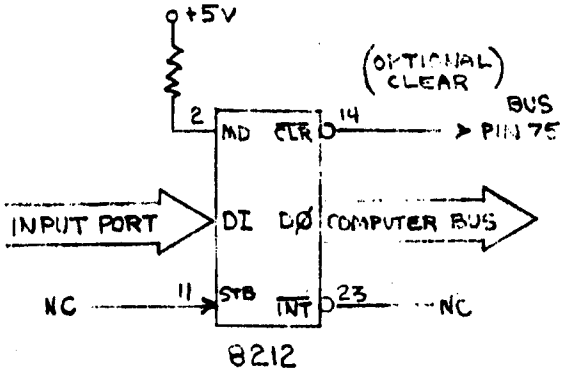
Input Port

Using the above input port circuit and connecting pin 23 (INT) to pin 73 of the computer bus, a port with interrupt is created. When the CPU is interrupted it will execute the eight-bit mach. instruction on the bus after it has finished its present instruction. If you do not have a special interrupt system, the interrupt will place an RST-7 instruction into the CPU.

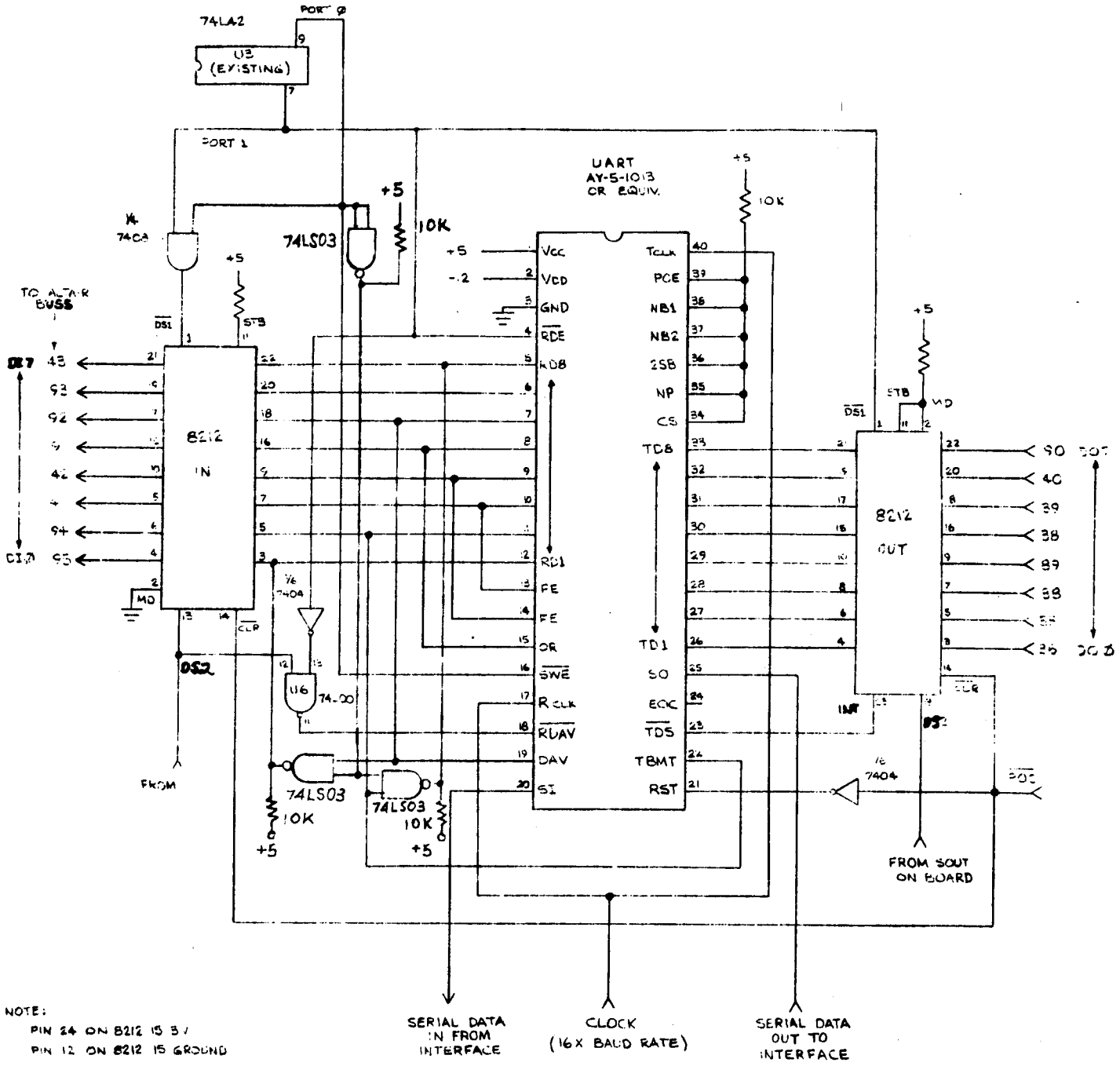


Input Port with Interrupt

The output port function is selected by connecting pin 2(MD) to a logic "one." The 8212 will be loaded with data from the bus when it is addressed by the computer thru pins 13 and 1.

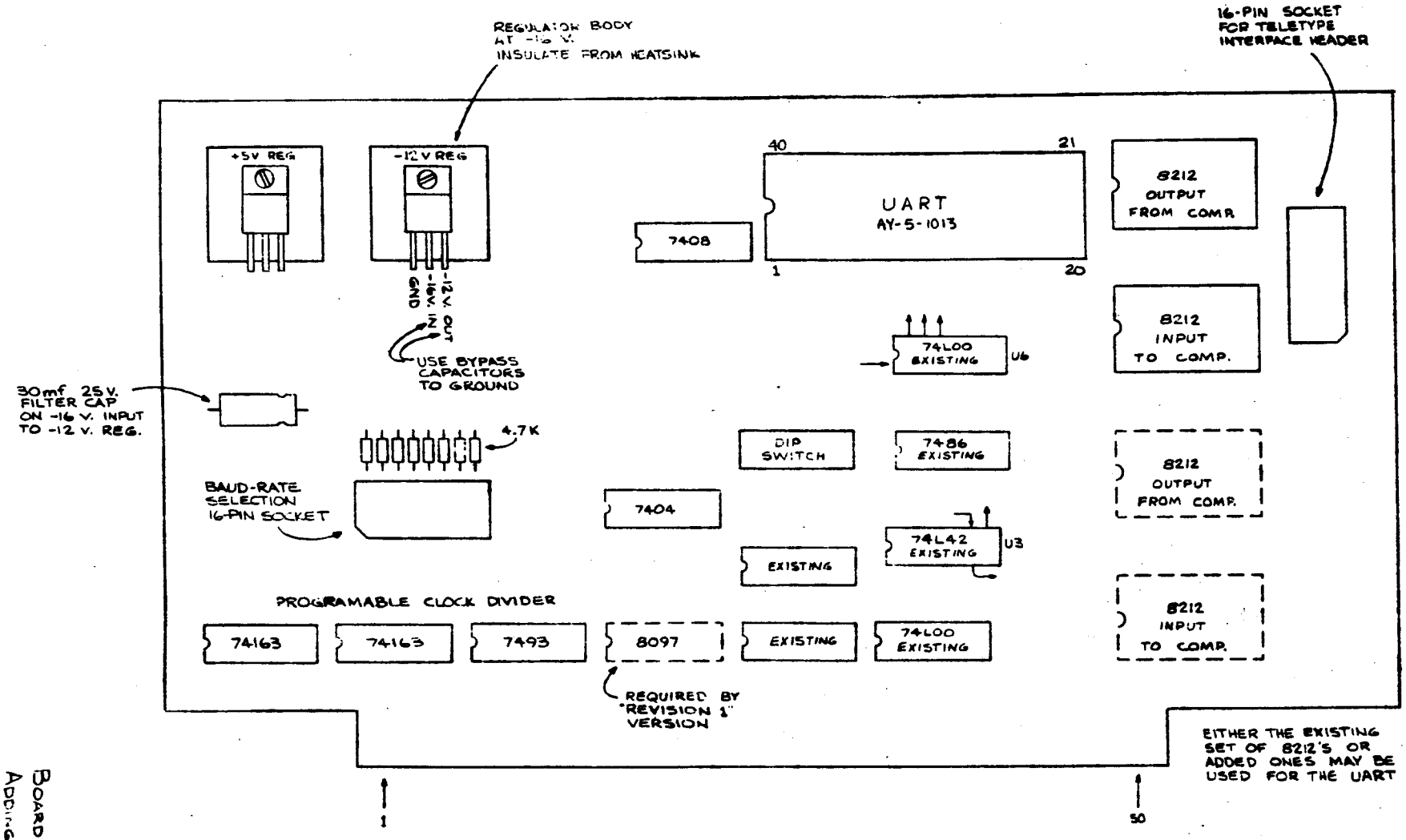


Output Port



UART Wiring Compatible
With Altair Software For
Rev. 0 & Rev. 1 Serial I/O
(w/o modif)

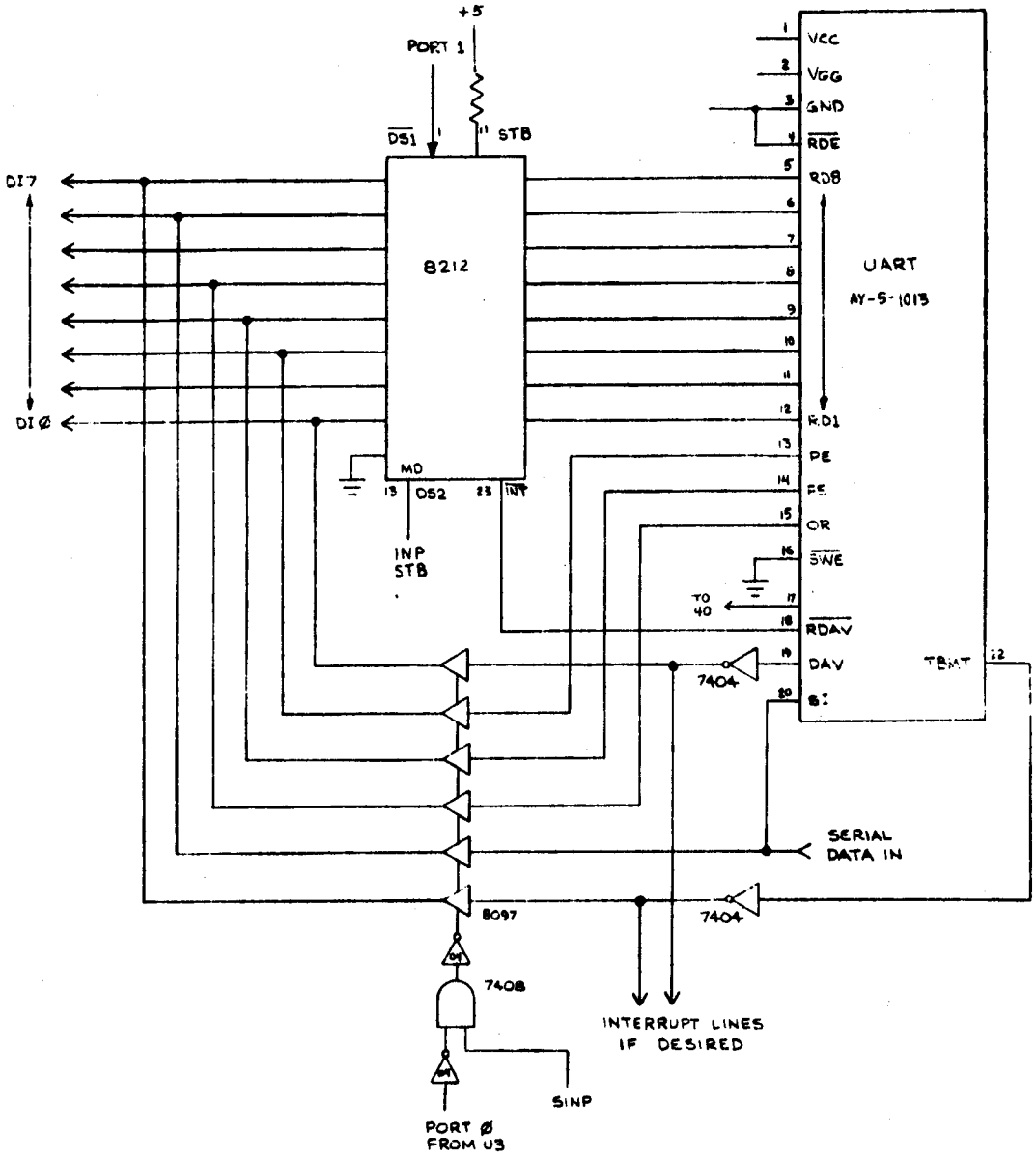
Solid State Music IO-2



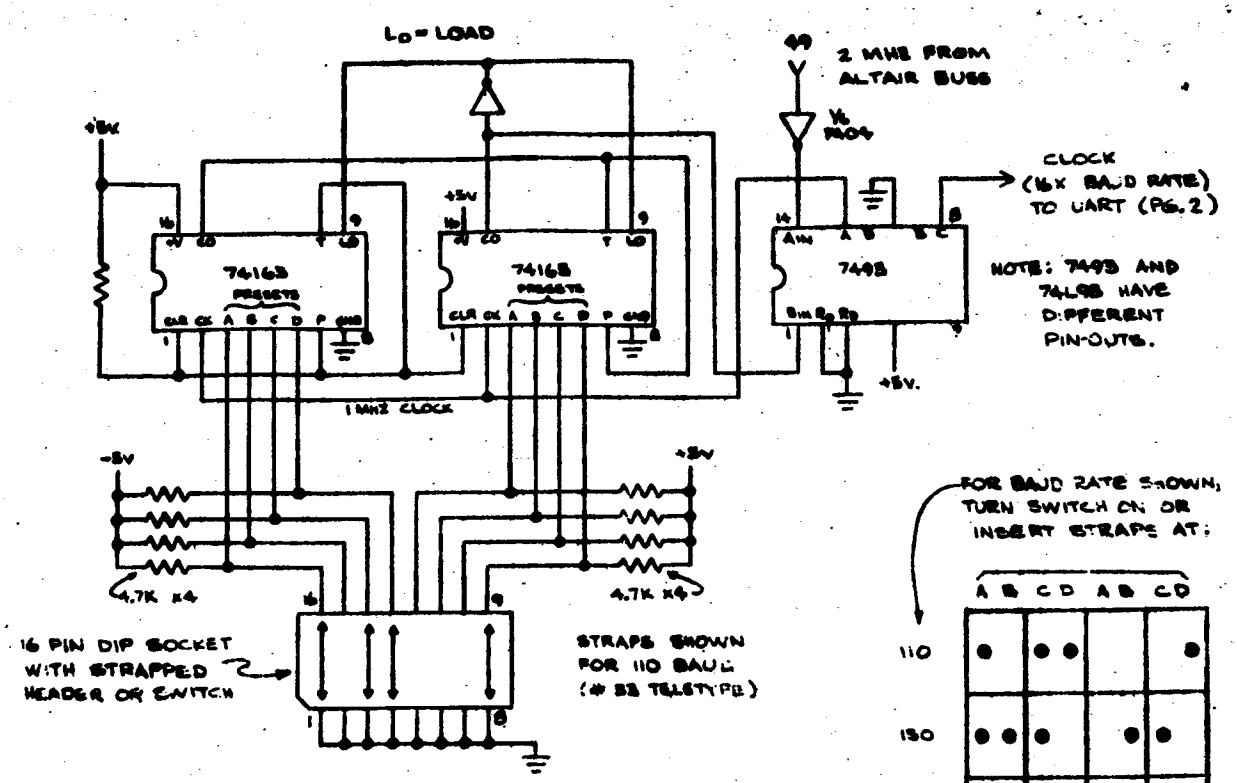
Board Layout For Adding a UART To The I/O #2 Kit

Solid State Music IO-2

SOLID STATE MUSIC IO-2



UNTESTED VARIATION WHICH SHOULD BE COMPATIBLE WITH REV 1 SERIAL I/O ALTAIR SOFTWARE

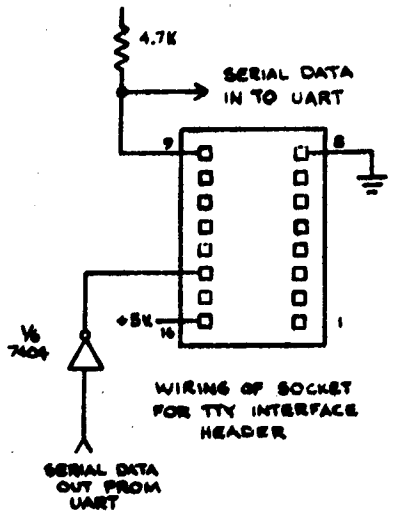


IF THE EIGHT LEADS WERE CONTROLLED BY AN OUTPUT PORT INSTEAD OF A SWITCH, THE COMPUTER COULD SELECT THE BAUD RATE BY ITSELF. IT SHOULD PUT ZEROS WHERE THE STRAPS TO GROUND ARE SHOWN.

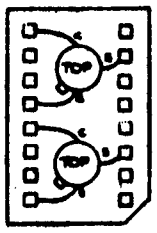
SELECTABLE BAUD RATE CLOCK FOR UART

TTY INTERFACE HEADER

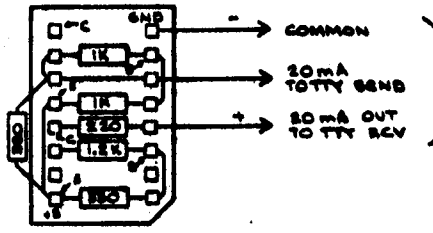
20 mA CURRENT LOOP



WIRING OF SOCKET FOR TTY INTERFACE HEADER



2N2907 PLACEMENT ON TOP OF HEADER

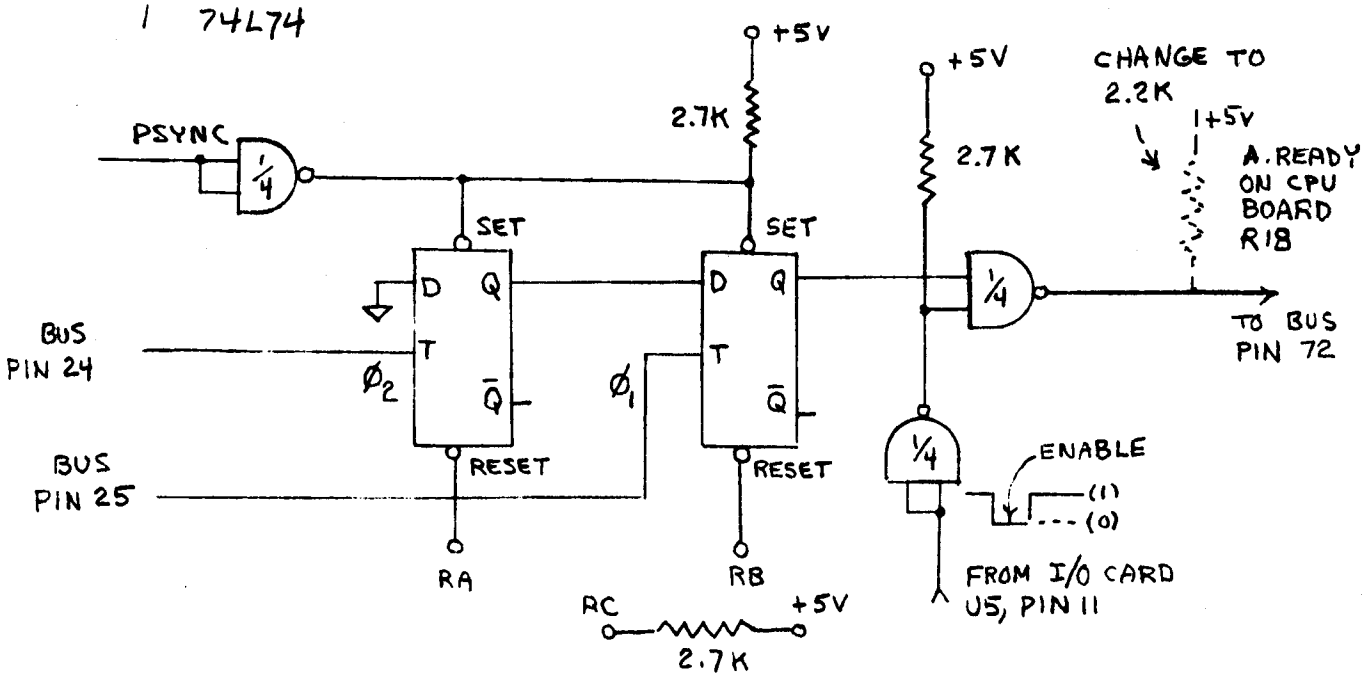


RESISTOR PLACEMENT

TOP VIEW OF 16-PIN HEADER CARRYING TELETYPE INTERFACE

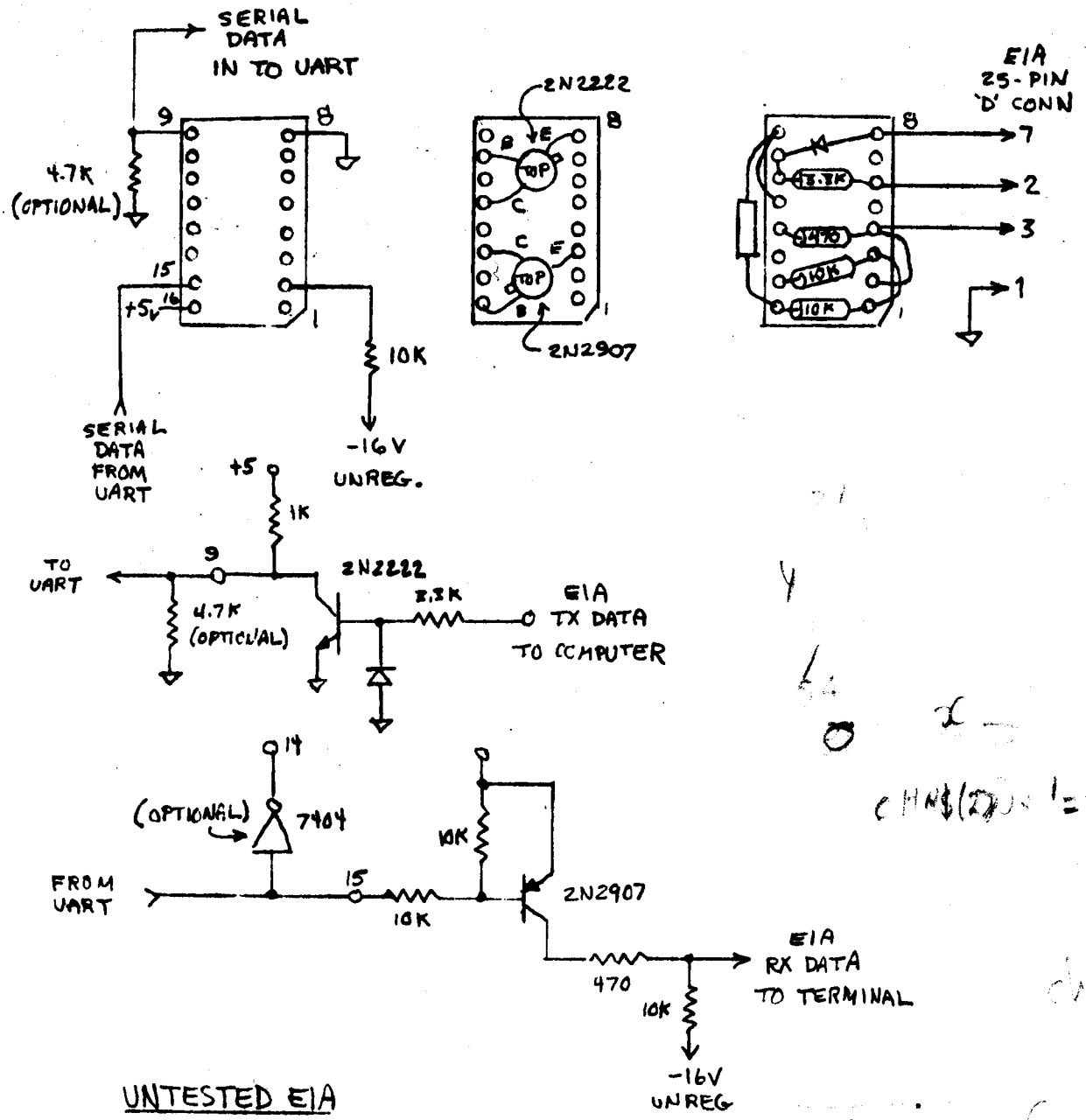
ICs REQUIRED:

1 74L03
1 74L74

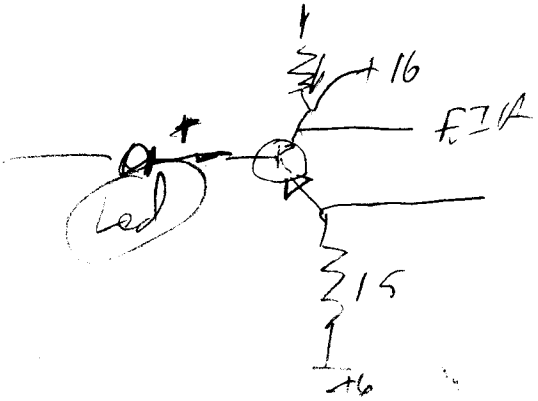


PROM SPEED	RA	RB	NUMBER OF WAIT CYCLES ADDED
.5 us	GND RC	GND GND	NO WAIT CYCLES (Circuit not required)
1 us	GND	RC	ONE WAIT CYCLE - 0.5 us added per byte
1.5 us	RC	RC	TWO WAIT CYCLES - 1.0 us added per byte

The IO-2 concept and tape master were created by Malcolm Wright. Important contributions were made by Lynn Cochran - The UART circuits and TTY interfaces, for example.



UNTESTED EIA INTERFACE



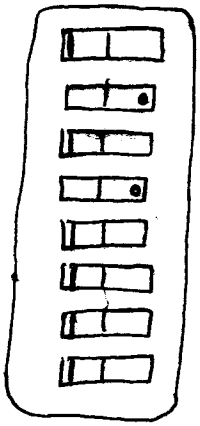
Serial Port Dip Sw. Settings 2 MHz clock From Backplane

Low speed

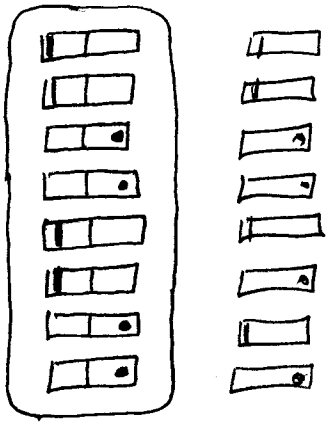
(150 - 600 Bps Low strap
300 - 1200 Bps High strap)

High speed

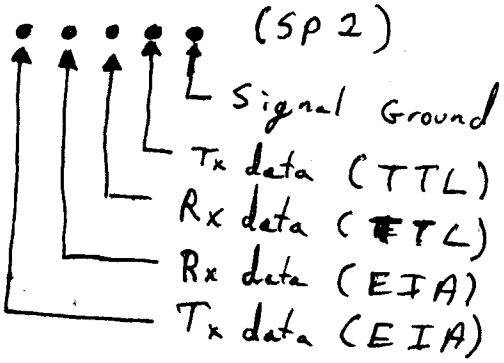
(300 - 1200 Bps Low strap
600 - 2400 Bps High strap)

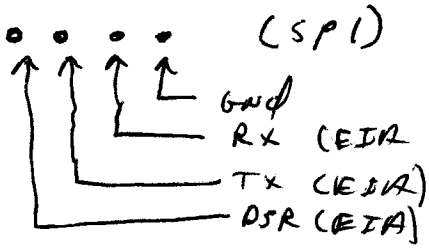


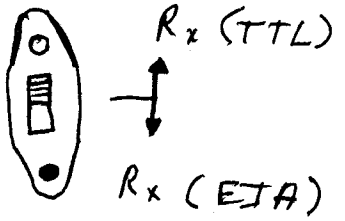
Serial Port 2 is 1/8 Times speed of serial port #1



Connector Identification







Ports

0
1
2 - Serial Data 1
3 - Serial Status 1
4 - Parallel out
5 - Serial Data 2
6 - Serial Status 2
7 - Parallel in

9.6 with OC=

Counter CLK → Pin 8 of OSC