CB2

Z-80 CPU Board
S-100 Bus

Instruction Manual

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S-100 Bus

INSTRUCTION MANUAL

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1.0 INTRODUCTION

The CB2 is a CPU board, based on the powerful Z-80 microprocessor, for the S-100 computer bus structure. The CB2 is designed to implement as many of the S-100 signals as possible, with the exception of the following: Stack, Interrupt Enable, and CPU status on the data bus during PSYNC.

The CB2 provides the following user-selectable options through on-board switches and wire-wrap jumpers:

- 2 or 4 MHz CPU clock.
- 2/4 MHz clock under XRDY/PRDY/RUN control signals.
- Two on-board sockets for 2716's, 2732's and/or 4016's, with independent addressing for each socket.
- One wait state on each M1 cycle or on each PSYNC.
- On-board MWRITE generation.
- Emulate 8080 I/O addressing.
- Firmware vector jump on power-up/reset.
- On-board RUN/STOP and SINGLE-STEP switches.
- Eight lines of extended addressing or an 8-bit output port.
- Phase One or $\overline{\text{STVAL}}$* signals available.
- $\overline{\text{NMI}}$ and Refresh signals available.

The PSYNC/Ø1/Ø2 signals are probably the most critical and difficult to generate on a Z-80 based S-100 CPU board. These signals are used by many of the other S-100 boards you may want to use and therefore must maintain the correct timing relationship between themselves and other S-100 signals. Considerable design effort went into the generation of these signals by the CB2 in order to guarantee its operation with the majority of the S-100 boards being manufactured. To obtain a more detailed description of these and the other S-100 signals, see the theory of operation section of this manual.

Many users may have heard of the proposed new IEEE 696.1 bus standard. The CB2 is designed to conform to this new

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* $\overline{\text{STVAL}}$ is a new IEEE 696.1 bus signal.

standard as much as possible and yet remain compatible with the old S-100 standard. The new IEEE standard eliminates many of the old S-100 signals that are needed by many of the systems with front panels. The CB2 is compatible with the old standard and with systems that have front panels, while maintaining the ability to be converted over to the new IEEE standard in the future. Details of this optional capability and other user-selectable options are described in the set-up section of this manual.

2.0 ASSEMBLY INSTRUCTIONS (refer to Assembly Drawing)

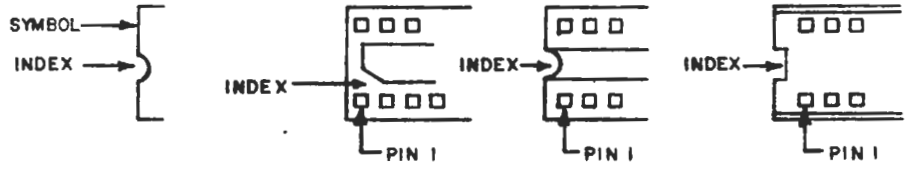
☐ Check kit contents against parts list.

☐ Check PC board for possible warpage and straighten if required. To straighten the board, bend with the hands (not a vise) against the warp. Sight down the edge of the board after bending to check if the warp was removed; if not, try bending again.

☐ Insert the sockets into the component side of the board with the "pin 1" index as indicated in the Assembly Drawing. (The component side is the side on which SSM ©1979 is printed.)

• One (1)	8-pin socket	at Location U13
• Thirty-three (33)	14-pin sockets	at U1-12,14,15, 20-24,26-31, 33-35,37-39,41,46
• Seven (7)	16-pin sockets	at U25,36,40,42,43, W1 & W2
• Eight (8)	20-pin sockets	at U18,19,44,45, 47-50
• Two (2)	24-pin sockets	at U16,17
• One (1)	40-pin socket	at U32

Example sockets:



☐ Place a flat piece of stiff cardboard of appropriate size on top of the board to hold them in place.

☐ Holding the cardboard in place against the sockets, turn the board over and lay it on a flat surface. (Be sure that all of the socket pins are through the holes.)

☐ NOTE: Keep soldering iron tip clean to prevent rosin and sludge from being deposited on traces. Wipe tip frequently on a damp cloth, damp sponge or steel wool.

☐ On each socket, solder two of the corner pins, choosing two that are diagonally opposite of each other.

/7 Once the sockets are secured, lift the board and check to see if they are flat against the board. If not, seat the sockets by pressing on the top while reheating each soldered pin.

/7 Complete soldering the remaining pins of each socket. Touch pin and pad with iron tip, allowing enough solder to flow to form a filet between pin and pad. Keep the tip against the pin and pad just long enough to produce the filet. Too much heat can cause separation of pad and trace from the board. A 600 degree iron is recommended.

/7 Insert and solder seven 2.7K SIP's (RP1 thru RP6, and RP9). Observe polarity. The end with pin 1 is marked with a dot, notch or bump, and should be installed pointing to the left or upper edge of the PCB.

/7 Insert and solder one 10K SIP (RP8).

/7 Insert and solder the following resistors:

9 - 2.7K ohm (red, violet, red) at R1 thru R3, R6, R8, R10, R12, R13, and R18.

2 - 620 ohm (blue, red, brown) at R7 and R9.

2 - 470 ohm (yellow, violet, brown) at R4 and R5.

1 - 3.3 Meg ohm (orange, orange, green) at R11.

1 - 330 ohm (orange, orange, brown) at R14.

3 - 10K ohm (brown, black, orange) at R15 thru R17.

/7 Insert and solder the following capacitors:

28 - 0.1 uf at C1 thru C3, C5 thru C7, C9 thru C22, and C24 thru C31.

1 - 100 pf at C4.

2 - 4.7 uf at C8 and C23 (observe polarity).

/7 Insert and solder the 16 MHz crystal (Y1). Two holes have been provided on either side of the crystal to solder a strap over the crystal to hold it down.

/7 Insert and solder the following Dip switches with the numbers right side up (position 1 to the left; position 4 or 7 to the right).

2 - 4 position switches at SE and SF.

2 - 7 position switches at SC and SD.

☐ Insert and solder a large momentary two position toggle switch (red handle/with spring return) at SB (right of SA at the top of the board). NOTE: The toggle lever should spring back when pushed.

☐ Insert and solder a large two position toggle switch (red handle/non-spring return) at SA (left side at the top of the board).

☐ Install and solder a two pin right angle molex connector at the top of the board (J1).

☐ Cut, install and solder 46 header pins. To cut the pins off, place the header strip on its side on some wood and press down on the indentation with a sharp blade (X-acto blade). BE CAREFUL. THE PARTS WILL COME APART WITH ENOUGH FORCE TO SHOOT OFF THE WORKBENCH.

2 - 4 pin headers (E6 thru E13)
18 - 2 pin headers (E2-E5, E14-E27, E29-E46)
2 - 1 pin headers (E1, E28)

☐ Place regulators on the board so that the mounting hole in the regulator is in line with the hole in the board. Mark leads for proper bending to match the board holes (allow for a bend radius).

☐ Bend regulator leads to match holes in board.

☐ If available, apply thermal compound to the back side of each regulator case (the side that will contact the heat sink). Use just a little thermal compound. Too much is worse than none at all.

☐ Next, position heatsink and insert regulator IC for each of the 3 regulators (X1, X2 & X3). Finally, position the nut and lockwasher on top of regulator and secure from behind with screw in each case. Be sure regulators and heatsinks fit flat on board and then solder all regulator leads.

☐ Do not install any IC's at this time.

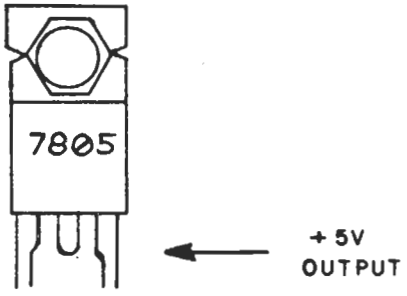
3.0 FUNCTIONAL CHECK

WARNING! DO NOT INSTALL OR REMOVE BOARD WITH POWER ON. DAMAGE TO THIS AND OTHER BOARDS COULD OCCUR.

This functional check does not examine or verify every signal or feature of the CB2, but does verify proper operation of the on-board regulators, the clock, RUN/STOP and SINGLE STEP circuits.

3.1 If an ohmmeter is available, measure the resistance between pin 50 (-) and pin 1 (+) on the edge connector and verify resistance of 20 ohms or greater. If your reading is below 20 ohms, check your board for possible shorts.

3.2 Apply power (+8v to +10v) to board by plugging into the computer or by connection to a suitable power supply. Measure the outputs of the +5v regulators.



The voltage should be between +4.8v and +5.2v. If the regulator doesn't meet this test, check the board for shorts or errors.

CAUTION: WHILE IT HAS NEVER HAPPENED TO US, SHORTED REGULATORS HAVE BEEN KNOWN TO EXPLODE WITH POSSIBLE INJURY TO EYES OR HANDS. BETTER SAFE THAN SORRY--KEEP FACE AND HANDS CLEAR OF THE REGULATOR SIDE OF THE BOARD DURING THIS TEST.

3.3 Observing polarity, insert the following IC's into their sockets: U6, U7, U11, U12, and U38. Close all the contacts on switch SF.

3.4 Reapply power to the CB2 and verify that U32 pin 6 (Z-80 IC socket) is toggling between logic 0 and 1 at 2 MHz. (Be sure SF, position 4 is closed.) This can be done using either an oscilloscope, counter, or logic probe (or even a DVM set to measure volts; the DVM would read approximtely +2.5 Vdc).

3.5 Next, verify that the 2/4 MHz circuit is operating. Set switch SF, all positions, to the open or OFF position and

verify a logic 0 at U38 pin 6 and U6 pin 8. Then set switch SF, position 4, to closed or ON position (this sets the CB2 to 2 MHz) and verify a logic 1 at U38 pin 6, and that U6 pin 8 is toggling between logic 0 and logic 1.

3.6 If the clock measurements in paragraphs 3.4 and 3.5 were OK, insert the rest of the IC's into their sockets except the Z-80 (U32). Examine the board carefully for any bent IC pins, then reapply power to the board and verify that the three regulators are still working properly.

NOTE: Set SC and SD position 1 to the ON position to disable the on-board EPROM and RAM for testing purposes.

3.7 Now turn off the power and insert the Z-80 IC (U32).

3.8 For testing purposes, temporarily wire-wrap the following connections (refer to Jumper Drawing):

Connection	Comment
E6 to E7	Put 2 MHz on bus pin 49.
E16 to E17	Disable vector jump circuit.
E22 to E23	Enable 8080 type of I/O.
E26 to E27	POC the Z-80 CPU.

If you have a S-100 front panel, connect:	Comment
E31 to E32	Front panel Sense-Switch disable.
E37 to E38	Front panel SINGLE-STEP signal.
E39 to E40	Front panel RUN signal.

If you don't have a front panel, connect:	Comment
E35 to E36	Generate MWRITE signal.

3.9 Set the RUN/STOP switch (SA) to the stop position (to the left). Verify that U32 pin 24 is at a logic 0, that U28 pin 6 is at a logic Ø, and that U25 pin 3 is at a logic 0.

3.10 Toggle the SINGLE-STEP switch (SB) and verify that U28 pin 6 toggles once (a pulse).

3.11 Set the RUN/STOP switch (SA) back to the right (RUN position) and toggle the SINGLE-STEP switch (SB) once. Verify that U28 pin 6 is pulsing continuously.

3.12 Run a small program to output all zeroes to port FE; such as:

```
AF              LOOP:  XRA A
D3,FE                  OUT  ØFEH
18,FB                  JR   LOOP
```

Then verify logic 0's at W1 pins 9 thru 16.

Then, run a similar program to output all 1's to port FE and verify logic 1's at W1 pins 9 thru 16.

4.0 SET-UP

There are a large number of user-selectable options on the CB2 Z-80 CPU board. These options give the user flexibility to configure the board to best meet individual system requirements. The options are selected in one of three ways: (1) by Dip switch, (2) by wire-wrapping, or (3) by header.

4.1 Jumper Options

The jumper pads are indicated as E numbers on the jumper drawing and the schematic.

4.1.1 Hold Acknowledge Option (PHLDA)

The PHLDA signal can be jumpered to come off the CB2 with the normal Z-80 timing for BUSAK, or it can be jumpered to delay the PHLDA signal turnoff by one-half cycle into the T1 state of the Z-80. The delayed mode guarantees an overlap of the control signals from slave and master during the exchange. See Figure 5.1.5.

	Jumper	Function Selected
(a)	E2 to E3	Delayed turnoff.
(b)	E4 to E5	Normal Z-80 operation. (If in doubt of which set-up to use, then use the NORMAL MODE until your DMA device is known.)

4.1.2 Clock Option ($\overline{CLK}$)

This option allows the user to select either a 2, 4, 8, or 16 MHz clock to come out on the $\overline{CLK}$ bus line (S-100 pin 49). This clock signal does not change when the CPU is switched between 2 and 4MHz as Phase 1 and Phase 2 do. This clock is not synchronized to the Phase 1 or Phase 2 signals.

	Jumper	Function Selected
(a)	E6 to E7	2 MHz (S-100 & IEEE standard)
(b)	E8 to E9	8 MHz
(c)	E10 to E11	16 MHz
(d)	E12 to E13	4 MHz

4.1.3 Fixed CPU Wait State Option

This option allows the user to select either no extra wait states or one extra wait for M1 (Op-Code Fetch) cycles only, or one extra wait state for all data transfer (Memory and I/O) cycles. The extra wait state for M1 cycles may be necessary with some memory boards because the Z-80 M1 cycle is faster than the 8080 M1 cycle.

	Jumper	Function Selected
(a)	E14 to E15 and E20 to E21	Extra wait state for M1 only
(b)	E14 to E15	Extra wait state for all data transfers
(c)	No jumpers	No extra wait status

4.1.4 Power-On/Reset Vector Jump Option

This option allows the user to execute one instruction at the beginning of ROM A (a ROM must be in the U16 position) like a "jump instruction" after applying power and/or when the CPU receives a reset (from bus pin 75). The CPU is forced to read the first instruction no matter where the ROM is addressed and then reverts back to normal operation.

The first instruction in the user's ROM should be a "jump" to the main entry point of the ROM program which initializes and brings up the computer system.

	Jumper	Function Selected
(a)	E16 to E17	Vector Jump Disabled
(b)	E24 to E25	Vector Jump on RESET
(c)	E18 to E19	Vector Jump on $\overline{POC}$
(d)	E24 to E25 and E18 to E19	Vector Jump on either RESET or $\overline{POC}$

4.1.5 I/O Address Multiplexing Option

This option allows the user to multiplex the low order address onto the high order address bus during I/O operations to simulate the way the 8080 CPU operates. The user may or may not want this feature depending on how his I/O cards operate.

The Z-80 CPU puts the accumulator contents on the high order address bus during normal I/O, and the B register (byte counter) is put on the high order address bus during block I/O operations. If the user wants this information to come out on the high address bus, he can disable the multiplexer circuit.

	Jumper	Function Selected
(a)	E22 to E23	8080 configuration ($Addr_L \rightarrow Addr_H$)
(b)	No jumper	Z-80 configuration

4.1.6 Power-On Reset Option

The user can prevent $\overline{POC}$ (pin 99) from resetting the CPU (Z-80) at the application of power to the board. ($\overline{POC}$ will still occur at pin 99 as usual.)

	Jumper	Function Selected
(a)	E26 to E27	$\overline{POC}$ resets Z-80 (most common connection)
(b)	No jumper	$\overline{POC}$ does not reset Z-80

4.1.7 Dynamic Memory Refresh Option

The Refresh signal is not part of the S-100 standard signals, but it is possible to bring this signal out to one of the S-100 bus lines if it is needed.

	Jumper	Function Selected
(a)	No jumpers	Refresh not available on S-100 bus
(b)	E28 to E29 and E30 to a solder connection at the top of the desired bus finger	Buffered Refresh signal to desired bus line

4.1.8 Spare Buffer

A spare buffer is located at U42 which may be used (if not used elsewhere as in 4.1.7 above). This buffer is not tri-stateable (the tri-state control line is always at logic 0). E29 is the buffer input, and E30 is the buffer output.

4.1.9 Front Panel Sense Switch Option

The IEEE bus standard deleted this function and put a ground on this line (bus line 53). The old S-100 bus standard used this line in conjunction with front panel operations to disable data from coming in from the bus.

	Jumper	Function Selected
(a)	E31 to E32	$\overline{\text{SSW}}$ enabled (old S-100)
(b)	No jumper	$\overline{\text{SSW}}$ disabled

4.1.10 Non-Maskable Interrupt Option

The Z-80 microprocessor has a non-maskable interrupt input which the 8080 does not have. Therefore, the original S-100 bus did not have this signal. The IEEE standard has set bus pin 12 for a $\overline{\text{NMI}}$ line.

	Jumper	Function Selected
(a)	No jumper	$\overline{\text{NMI}}$ disabled
(b)	E33 to E34	$\overline{\text{NMI}}$ enabled on bus line 12

4.1.11 MWRITE Option

Systems with front panels have the MWRITE signal generated by the front panel circuit. Therefore, they do not need

this signal from the CPU board. Turnkey systems and other systems without a front panel may need this signal generated by the CPU in order to write into RAM memory.

	Jumper	Function
(a)	No jumper	MWRITE Disabled (front panel system)
(b)	E35 to E36	MWRITE Enabled (no front panel)

4.1.12 RUN and SINGLE-STEP Options

These are signals on the original S-100 bus to provide front panels with RUN and SINGLE-STEP control lines to the CPU board. These signals are being eliminated in the new IEEE bus standard.

	Jumper	Function
(a)	E37 to E38	SINGLE-STEP enabled on bus line 21
(b)	E39 to E40	RUN signal enabled on bus line 71

These signals, when disabled, will default to the normal CPU run mode. The CB2's RUN/STOP and SINGLE-STEP switches will work no matter how E37 thru E40 are connected.

4.1.13 Spare Tri-State Buffer

A spare tri-state buffer is located in U43 pins 9 and 10. This buffer is tri-stated by the $\overline{\text{C/C DSBL}}$ control signal on S-100 bus line 19. E44 is the input, and E43 is the output.

4.1.14 2/4 MHz Clock Flag Option

In the original S-100 bus, bus line number 98 is the STACK STATUS line. The Z-80 does not produce a STACK status. Therefore, this line was used by *Cromemco to indicate when the CPU is in 2 or 4 megahertz operation. The CB2 will also indicate 2/4 MHz operation status on this line if E45 and E46 are connected. The new IEEE uses bus line 98 as an error signal line. Therefore, if you are using the IEEE standard, E45 and E46 must not be connected.

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* Cromemco, 280 Bernardo Avenue, Mountain View, CA. Manufacturer of Z-80 based products.

	Jumper	Function
(a)	No jumper	2/4 MHz STATUS disabled
(b)	E45 to E46	2/4 MHz STATUS enabled on bus line 98

4.1.15 Ø1 $\overline{\text{STVAL}}$ $\overline{\text{STROBE}}$ Option

The original S-100 bus has Phase 1 clock on bus line 25. The new IEEE standard has a new signal $\overline{\text{STVAL}}$ on this line which indicates when the status lines are valid.

	Jumper	Function
(a)	E41 to E42	Phase 1 clock on bus line 25
(b)	E1 to E44 and E43 to E42	$\overline{\text{STVAL}}$ on bus line 25

4.2 Switch Settings

There are six switches/Dip switches on the CB2. The switches are labelled SA through SF on the schematic and assembly drawings. The individual switch positions on the Dip switches are labelled 1, 2, 3, etc. Position 1 is located on the left side of a Dip switch.

4.2.1 RUN/STOP and SINGLE-STEP

The two large toggle switches at the upper left side of the CPU board are SA and SB, the RUN/STOP and SINGLE-STEP switches respectively. These switches and their circuitry are provided so the user can stop the processor and single step it if he does not have a front panel. This is a valuable tool when trying to troubleshoot the hardware or software in case of difficulty.

4.2.1.1 RUN/STOP (SA)

When thrown to the left, switch SA stops the processor. This allows the user to make logic measurements and to single step the processor with switch SB.

When SA is thrown to the right and SB is toggled, the CPU will go into the run state until SA is again thrown to the left position.

Normally, switch SA will be in the RUN position (to the right), and the processor will come up running when powered up ($\overline{\text{POC}}$ resets the RUN/STOP flip-flop).

4.2.1.2 SINGLE-STEP (SB)

This is a spring-loaded momentary switch that will single step the CPU when the RUN/STOP switch (SA) is in the STOP position (to the left). The CPU is single-stepped once each time SB is toggled. SB is used to start the processor when SA is returned to the RUN position (to the right).

4.2.2 On-Board Memory Addressing

Dip switches SC and SD provide address selection for memory sockets U16 and U17 respectively.

	FUNCTION	
Position	ON/Closed	OFF/Open
1*	Disable Memory	Enable Memory
2	Select 2716/4016**	Select 2732 (A11/Position 3 = don't care)
3	A11 logic 0	A11 logic 1
4	A12 logic 0	A12 logic 1
5	A13 logic 0	A13 logic 1
6	A14 logic 0	A14 logic 1
7	A15 logic 0	A15 logic 1

Hex	Switch Position				
Memory Address	3	4	5	6	7
ØØØØ	On	On	On	On	On
Ø8ØØ	Off	On	On	On	On
1ØØØ	On	Off	On	On	On
1800	Off	Off	On	On	On
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
E800	Off	On	Off	Off	Off
F000	On	Off	Off	Off	Off
F800	Off	Off	Off	Off	Off

---

* Disable if there is no memory IC in the socket.
** 2716-pin-compatible RAM memory.

4.2.3 On-Board Memory Type Selection

Dip switch SE allows the user to select between three types of memory IC's (2716 - 2K EPROM, 2732 - 4K EPROM, and 4016 or equivalent 2K RAM) for each memory socket (U16 and U17).

Memory Type	Socket U16		Socket U17	
	Position 1	Position 2	Position 3	Position 4
2716	Open	Open	Open	Open
2732	Open	Closed	Open	Closed
4016	Closed	Open	Closed	Open

Open = OFF Closed = ON

(Positions 1 & 3 enable MWRITE to U16 & U17 respectively for RAM memory only.)

(Positions 2 & 4 enable address bit A11 to U16 & U17 respectively for 2732 - 4K EPROM's only.)

4.2.4 CPU Clock Rate Control

Dip switch SF controls the user-selectable clock rate options. This switch is located at the lower left side of the CPU board.

Position	Function
1	When closed (ON), this switch causes the CPU to go to 2 MHz operation when a front panel stops the computer. This is provided because some front panel circuits cannot operate at 4 MHz. This switch is tied to the S-100 RUN signal on line 71 and will function only if E39 and E40 are jumpered together.
2	When closed (ON), this switch allows XRDY (S-100 line 3) to slow the processor to 2 MHz during wait states. Therefore, if the user has slow memory with wait states set for 2 MHZ operation, this will allow him to maintain the same wait time delay.
3	Same as Position 2 above, except for PRDY (S-100 line 72).

Position	Function
4	When closed (ON), this switch selects 2 MHz operation. If this switch position is open (OFF), then 4 MHz is selected.

When all four switches are open (OFF), the CB2 will run at 4 MHz all of the time.

4.3 Short Form Setup Worksheet/Record

Due to the large number of options, a short form setup record is provided so the user can record how his board has been set up. This allows you to recall the features and addresses selected at a glance. It also allows you to return the CB2 to its original setup if it is changed temporarily to use it in another system. To use the short form provided, place a check mark in the right-hand box corresponding to the features and switch settings you use. Indicate, with 0's and 1's, the addresses selected for memories in U16 and U17 and write the Hex address in the right-hand box. The numbers on the left are the paragraphs which describe each one.

TABLE OF SWITCH SETTINGS

REFERENCE PARAGRAPH 4.2.2 ON BOARD MEMORY ADDRESS SETTINGS

Switch SC (Address for memory A - IC U16).

Switch position	1	2	3	4	5	6	7
Address (A)	-	-	11	12	13	14	15

0=2716/4016 addressing
1=2732 addressing

0=Memory enabled
1=Memory disabled

BACKWARDS?

Switch SD (Address for memory B - IC U17).

Switch position	1	2	3	4	5	6	7
Address (A)	-	-	11	12	13	14	15

0=2716/4016 addressing
1=2732 addressing

0=Memory enabled
1=Memory disabled

REFERENCE PARAGRAPH 4.2.3 ON BOARD MEMORY TYPE SELECTION

Switch SE

Switch position		1	2	3	4	
IC U16	2716	1	1	-	-	
	2732	1	0	-	-	
	4016	0	1	-	-	
IC U17	2716	-	-	1	1	
	2732	-	-	1	0	
	4016	-	-	0	1	

TABLE OF SWITCH SETTINGS (continued)

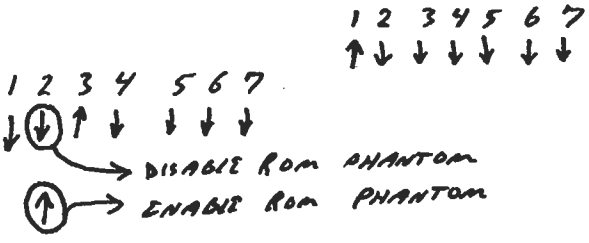
REFERENCE PARAGRAPH 4.2.4 CPU CLOCK RATE CONTROL SETTINGS

Switch SF

2 MHz on RUN		Pos 1	
	Enabled	0	
	Disabled	1	
2 MHz on XRDY		Pos 2	
	Enabled	0	
	Disabled	1	
2 MHz on PRDY		Pos 3	
	Enabled	0	
	Disabled	1	
2 MHz only		Pos 4	
	Enabled	0	
	Disabled	1	

1=OFF=OPEN
0=ON=CLOSED
-=NOT APPLICABLE

FOR BOOT @ F000H
DOUBLE-D @ FC00H



SHORT FORM SETUP WORKSHEET/RECORD OF JUMPER SELECTIONS

Ref. Para.					
4.1.1	PHLDA OPTION		E2-3	E4-5	
	Normal Z-80 operation			X	
	½ cycle turnoff delay		X		
4.1.2	CLK FREQUENCY OPTION				
	2 MHz*			E6-7	
	4 MHz			E12-13	
	8 MHz			E8-9	
	16 MHz			E10-11	
4.1.3	WAIT STATE OPTIONS		E14-15	E20-21	
	No added wait states*				
	1 extra M1 wait state		X	X	
	1 wait state per PSYNC		X		
4.1.4	VECTOR JUMP OPTION	E16-17	E18-19	E24-25	
	Vector jump disabled*	X			
	Vector jump on RESET			X	
	Vector jump on POC		X		
	Vector jump on RESET and POC		X	X	
4.1.5	I/O ADDRESS OPTION			E22-23	
	8080 configuration*			X	
	Z-80 configuration				
4.1.6	POWER-ON RESET OPTION			E26-27	
	POC resets the Z-80*			X	
	POC does not reset the Z-80				
4.1.7	DYNAMIC MEMORY REFRESH (Note 1)		E28-29	E30-( )	
	Refresh signal on bus line ( )		X	X	
	No refresh signal*				
4.1.9	SSW DSBL OPTION			E31-32	
	Enabled*			X	
	Disabled				
4.1.10	NMI OPTION			E33-34	
	Enabled			X	
	Disabled*				
4.1.11	MWRITE OPTION			E35-36	
	Enabled			X	
	Disabled*				
4.1.12	RUN/SINGLE-STEP OPTION		E37-38	E39-40	
	Both enabled*		X	X	
	SINGLE-STEP enabled only		X		
	RUN enabled only			X	
	Both disabled				
4.1.14	2/4 MHz FLAG OPTION			E45-46	
	Enabled			X	
	Disabled*				
4.1.15	Ø1 STVAL OPTION (Note 1)	E1-44	E43-42	E41-42	
	Ø1 on bus line 25*			X	
	STVAL on bus line 25	X	X		

* Indicates a standard S-100 set-up.

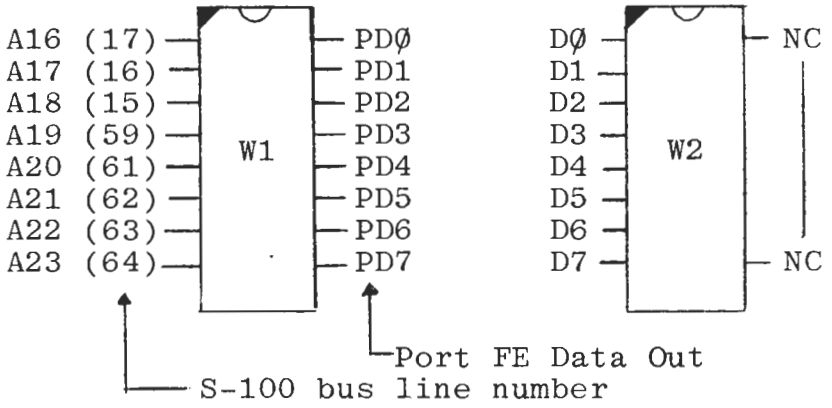
X Indicates a connection between the indicated E pads.

Note 1: The STVAL and REFRESH signals must be put on the S-100 bus through a tri-state buffer so they can be disabled when necessary. There is only one available tri-stateable buffer (U43). Therefore, only one of these signals can be used.

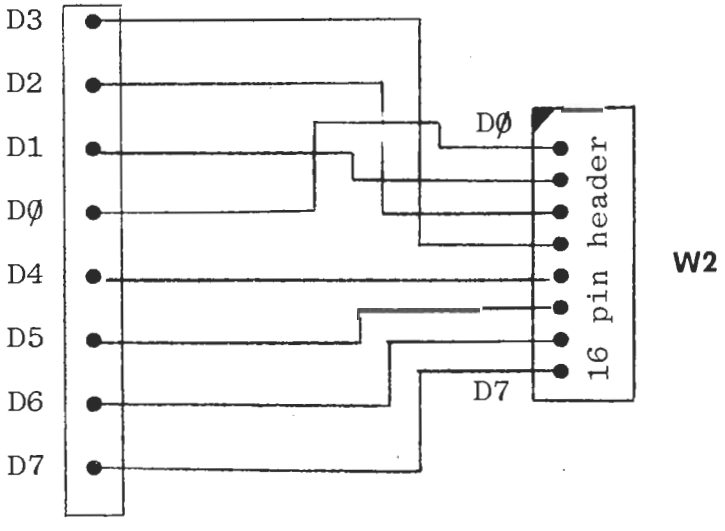
4.4 Header Description

There are two headers (W1 & W2) on the CB2. W1 allows the user to connect port FE to the S-100 bus to be used as extended addressing or to a header with ribbon cable to be used as an output port to an external device. Connecting Pin 1 to Pin 16, Pin 2 to Pin 15, etc., on W1 will provide the user with extended addressing on the S-100 bus through port FE.

W2 is the front panel socket for IMSAI and ALTAIR* type front panels. W1 and W2 sockets are arranged as follows:



If the user wishes to make an adapter for the CB2 to the ALTAIR connector, it should be connected as follows:



ALTAIR connector

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*ALTAIR owners will have to adapt their front panel to CPU board connector to plug into W2.

5.0 CIRCUIT DESCRIPTIONS

This section is a short description of the various circuits of the CB2. Some of the circuits described will refer to partial schematics contained within this section, others will refer to the complete CB2 schematics at the back of the manual. The CB2 circuits will be described in the following order: CPU "P" signals, CPU clock circuits, CPU status "S" signals, external control circuits (i.e., RDY, Hold, INT, and Reset), Address Bus circuits, Data Bus circuits, extended address port, on board memory, and vector jump circuit.

5.1 CPU "P" Signals

The S-100 "P" signals generated by the CB2 consist of the following signals: PSYNC, PDBIN, $\overline{\text{PWR}}$, PWAIT, PHLDA, and $\overline{\text{PSTVAL}}$.

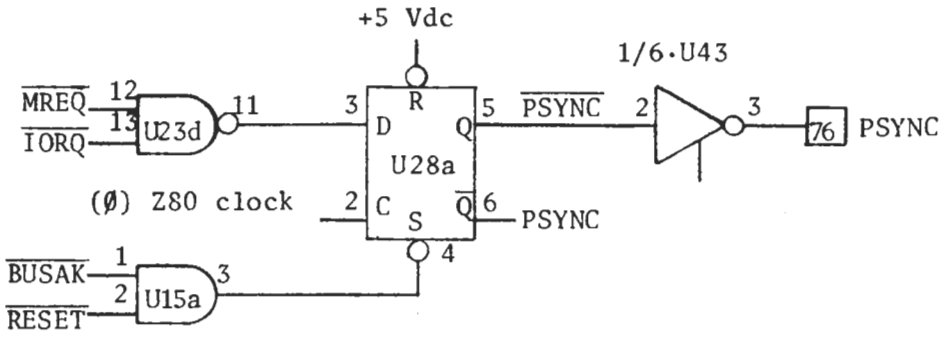
5.1.1 PSYNC

PSYNC is used by many of the S-100 cards and is the only signal on the S-100 bus that indicates the beginning of each byte processed by the CPU board (i.e., memory read or write, I/O read or write, and interrupt acknowledges). The falling edge of PSYNC indicates that the status "S" signals are valid and that the CPU will look for the $\overline{\text{WAIT}}$ (XRDY and PRDY) signals a half cycle later, if wait states are needed. (See Figures 5.1.1a & b).

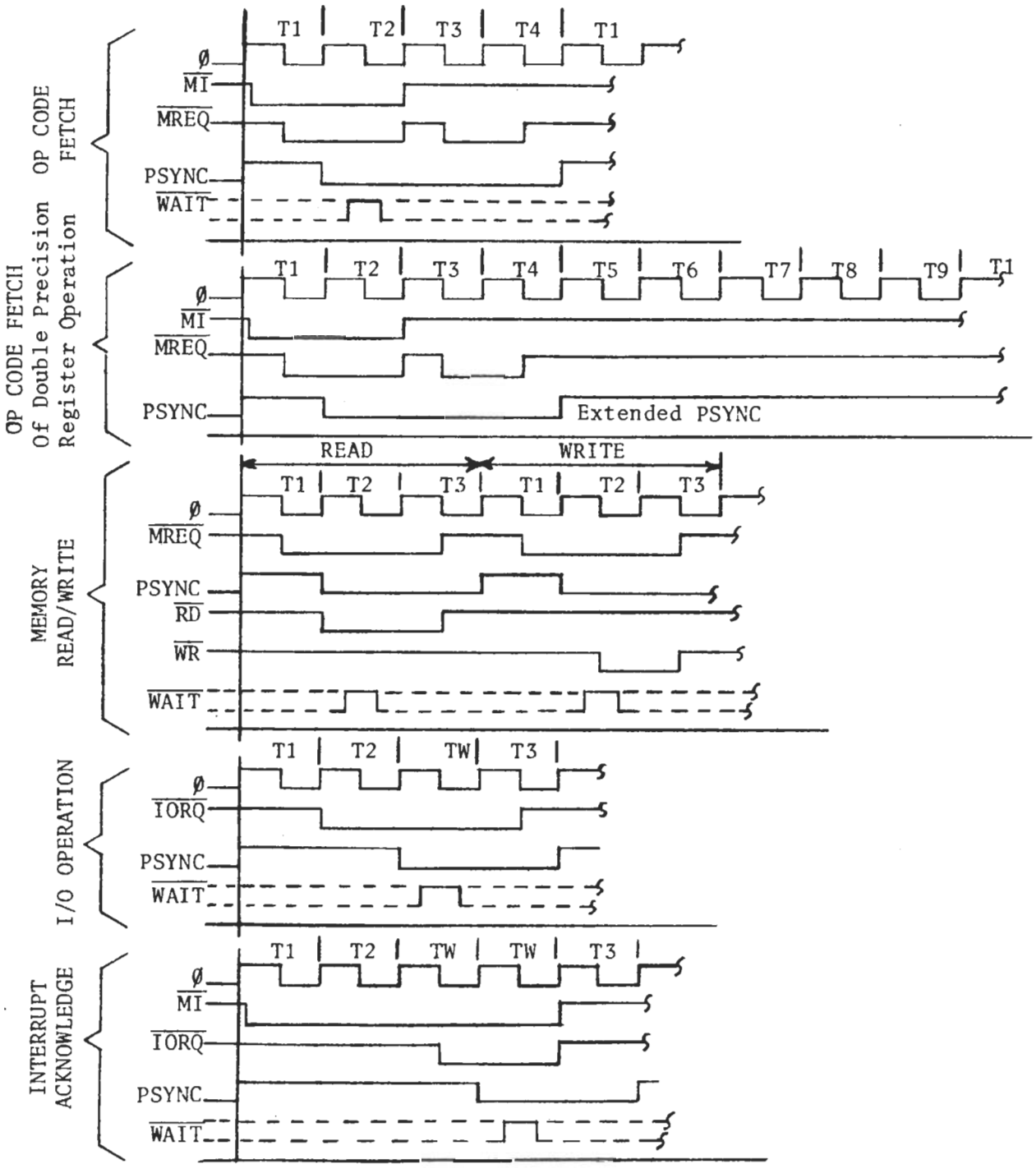
PSYNC is generated on the CB2 when $\overline{\text{IORQ}}$ and $\overline{\text{MEMRQ}}$ are both at logic 1 on the leading (rising) edge of Phase 2. (See Figures 5.1.1a & b.) Generating PSYNC this way guarantees that the PSYNC signal will go low one-half cycle prior to when the processor expects the first wait request, if needed, which is identical to the 8080 timing for PSYNC and $\overline{\text{WAIT}}$.

One problem does occur when generating PSYNC this way; some operations cause the PSYNC to exceed one clock cycle in width (as much as 6 cycles). This occurs during I/O operations and when the Z-80 must do internal operations during the M1 machine cycle before proceeding to the next machine operation, such as: index operations, double precision register to register operations, double precision register pushes to the stack, etc. These extra long PSYNC pulses are acceptable to other S-100 boards as long as only one Phase 2 and Phase 1 pulse occurs during PSYNC. The CB2 has circuits to guarantee only one Phase 2 and

FIGURE 5.1.1 PSYNC



a. SCHEMATIC



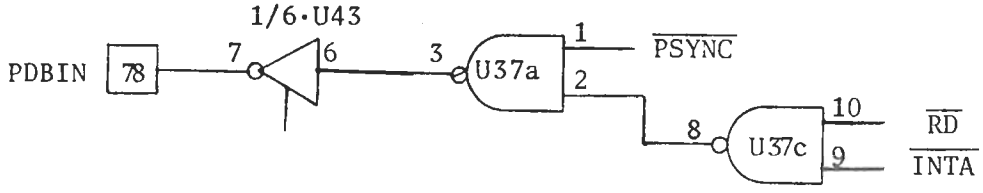
b. TIMING

Phase 1 pulse during PSYNC (see Paragraph 5.2 which describes the clock section).

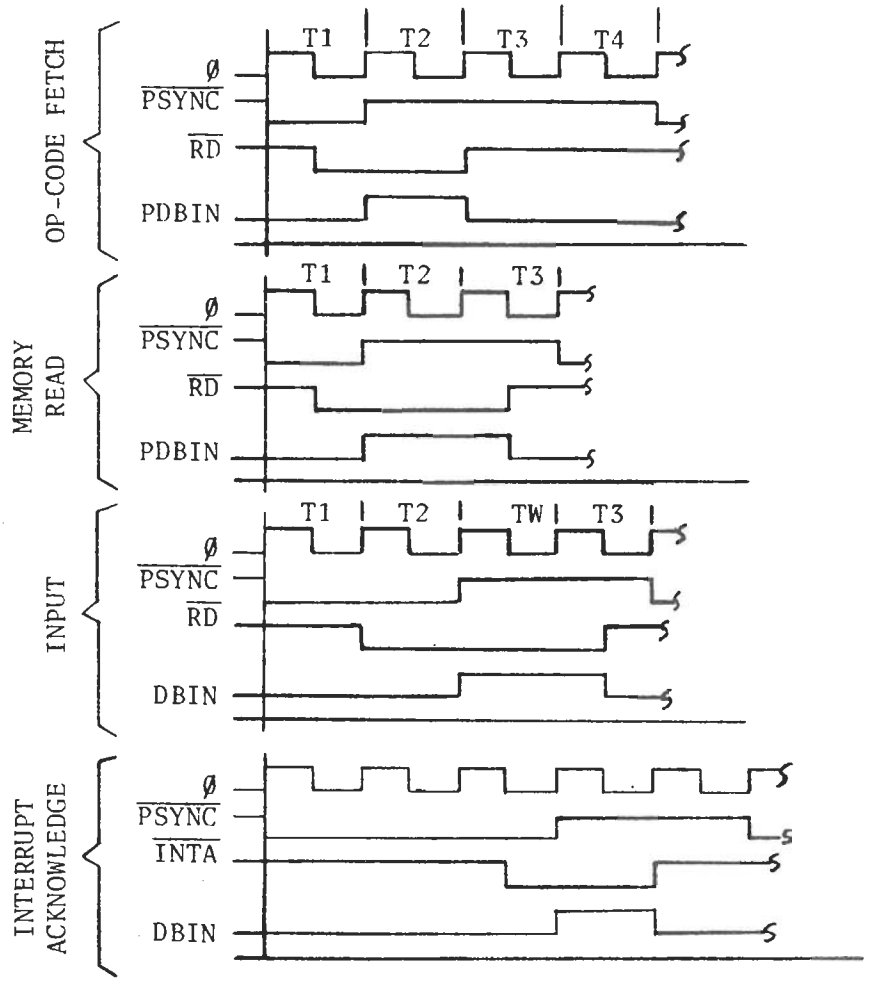
5.1.2 PDBIN

This signal is used to gate data onto the Z-80's input when data is to be transferred to the CPU from external devices (such as memory and input ports).

FIGURE 5.1.2 PDBIN



a. SCHEMATIC



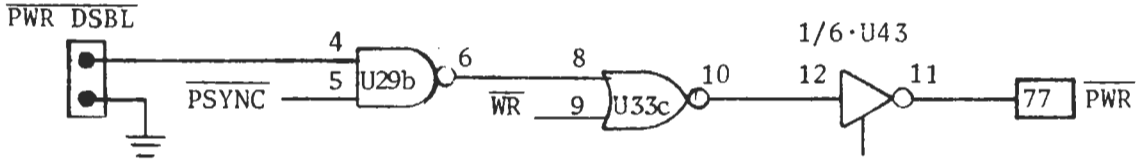
b. PDBIN TIMING

PDBIN occurs during any data transfer into the CPU. The Z-80 $\overline{RD}$ signal occurs during all memory reads and input operations, but not during interrupt acknowledge. Therefore, this signal is generated when $\overline{RD}$ or $\overline{INTA}$ occurs (U37 pins 10 & 9). PDBIN in the 8080 does not occur while PSYNC is high; therefore, $\overline{PSYNC}$ is used to inhibit PDBIN by U37 pin 1.

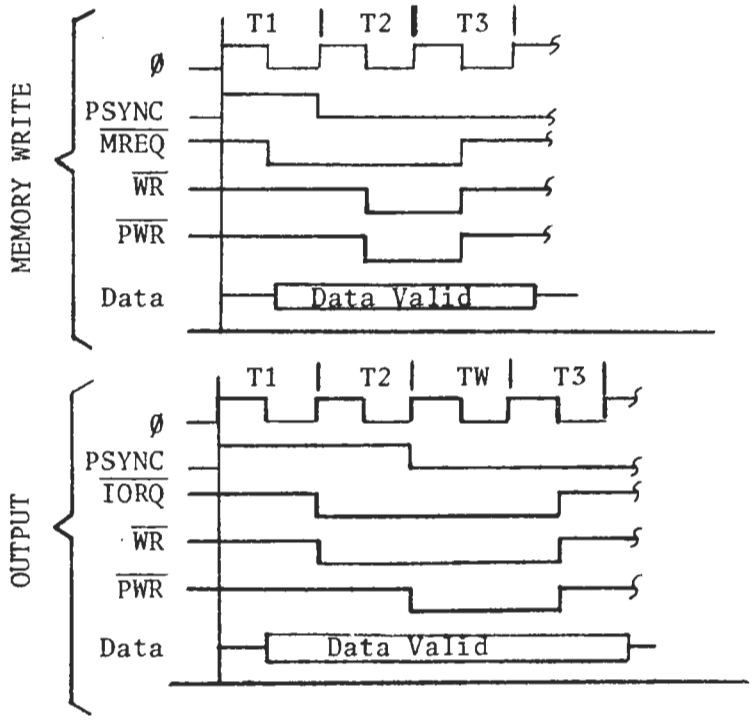
5.1.3 $\overline{PWR}$

This signal occurs during any memory write or output operation and is used to strobe the data into the memory or output port device.

FIGURE 5.1.3 PWR



a. SCHEMATIC



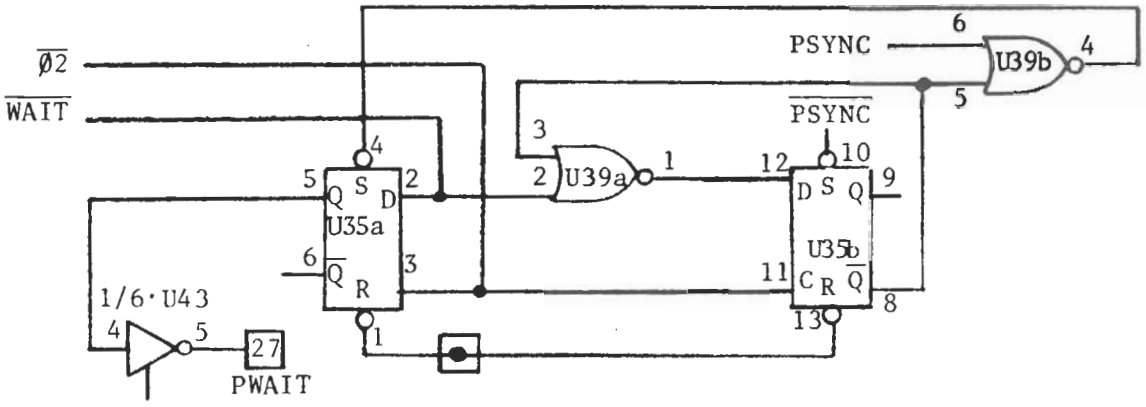
b. TIMING DIAGRAMS

The 8080 does not produce $\overline{WR}$ until after PSYNC; therefore, PSYNC is used to inhibit $\overline{PWR}$ (U29 pin 5). $\overline{DWR}$ is a special input at the top of the CB2 card that can be used as an inhibit signal to protect memory from being written into.

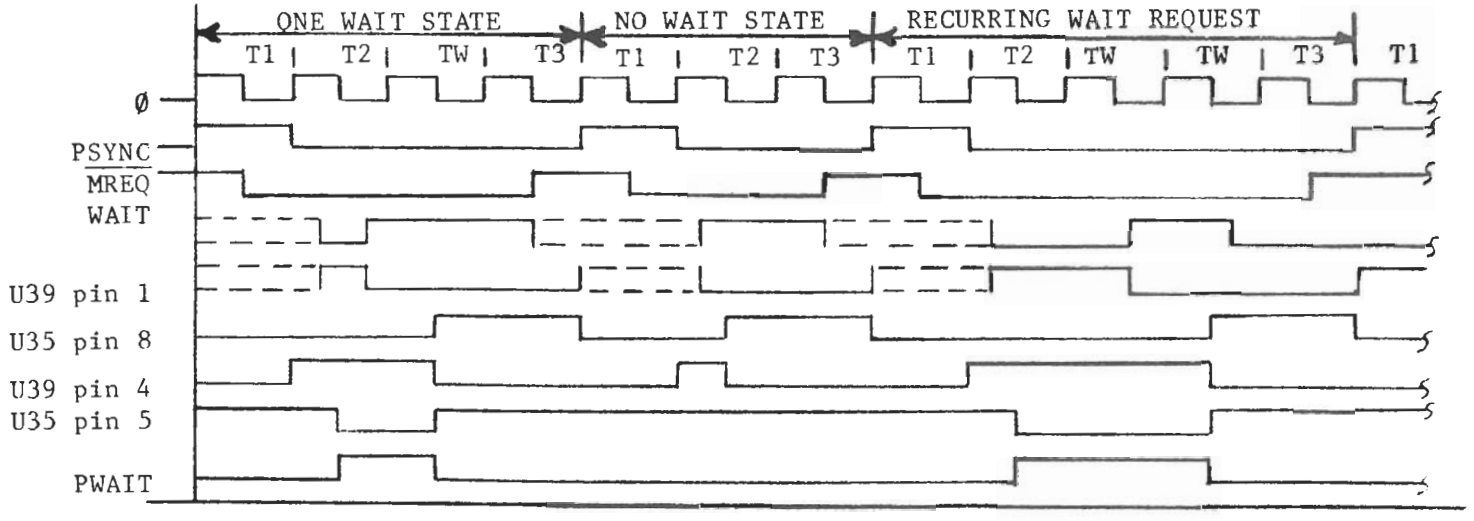
5.1.4 PWAIT

This signal indicates when the CPU is in a wait state. Some Z-80 CPU cards use XRDY or PRDY as the PWAIT signal on the S-100 bus. This is good for most cases, but some S-100 cards use the PWAIT to generate one wait state by feeding PWAIT inverted to XRDY or PRDY. When this happens, the PWAIT and XRDY or PRDY signals will oscillate. Therefore, the PWAIT signal on the CB2 is synchronized with Phase 2.

FIGURE 5.1.4 PWAIT



a. SCHEMATIC



b. TIMING DIAGRAM

The PWAIT circuit consists of: two flip-flops, U35A & B; two NOR gates, U39B & C; and a tri-state driver, U34B, as shown in Figure 5.1.4. At the beginning of each machine cycle, PSYNC sets both flip-flops. If a $\overline{WAIT}$ signal is present at the falling edge of Ø2, then U35A changes state to indicate a PWAIT status. The PWAIT status will continue until the $\overline{WAIT}$ signal is gone at the falling edge of $\overline{Ø2}$. Since the Z-80 CPU also checks for the $\overline{WAIT}$ signal on the falling edge of Ø2, this circuit reliably indicates when the CPU is waiting.

If a second $\overline{WAIT}$ signal were applied after the CPU left the WAIT state, the CPU would not accept it until the next machine cycle. Therefore, U35B, and U39B and C are used to inhibit any PWAIT signals after $\overline{WAIT}$ goes away the first time, or if it is not present on the first falling edge of Ø2 after PSYNC. U35B is clocked to the RESET state by Ø2 if $\overline{WAIT}$ is high. Because U35B $\overline{Q}$ is now high, U39B & C will always remain low so that U35B cannot change state and U35A is always being set (PWAIT inactive state). This will continue until PSYNC occurs and sets U35B once again.

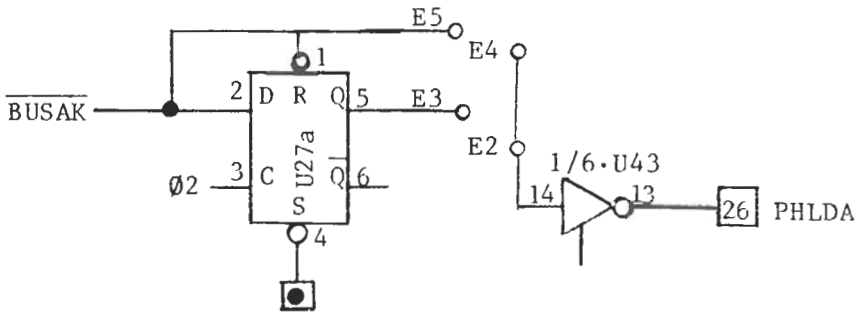
5.1.5 PHLDA

This signal indicates to an external device that the CPU is ready to turn over the bus control during a DMA operation. Two methods of asserting and removing PHLDA are provided on the CB2. The first is the Z-80's $\overline{BUSAK}$ signal inverted, which is found on most CPU cards and is obtained by connecting E4 and E5 together. The second method uses U27 to synchronize PHLDA to Ø2. This delays PHLDA slightly, which guarantees that all lines are tri-stated by the CPU when PHLDA is asserted, and that the CPU has reapplied all signals just prior to removing PHLDA. This mode allows a cleaner DMA transfer of control on the S-100 bus. In order to select this method, E4 to E5 must be opened and E2 to E3 must be connected.

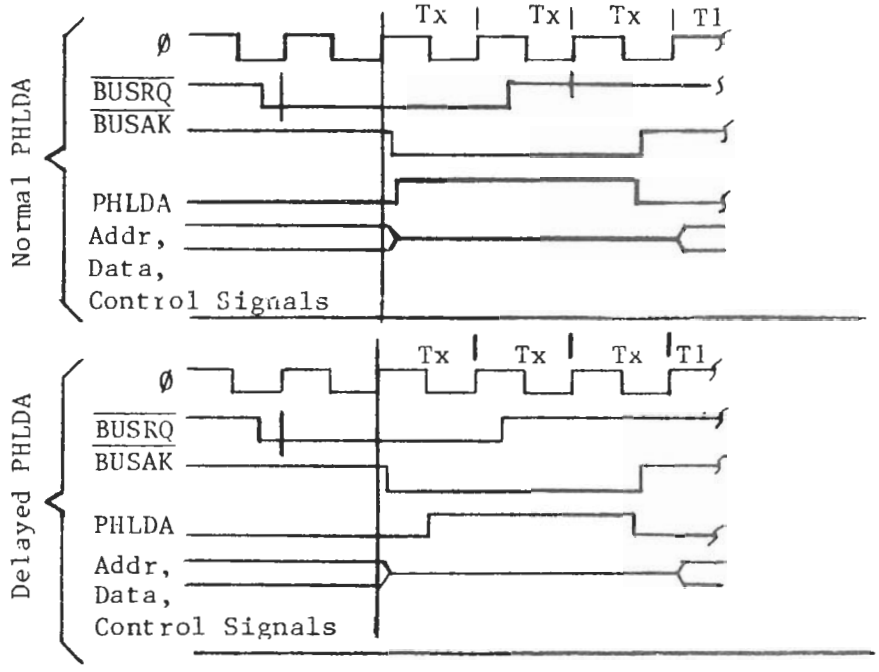
5.1.6 $\overline{PSTVAL}$

This is a new IEEE standard signal and goes low to indicate when status is valid on S-100 bus. This signal goes low at Ø1 during PSYNC and returns to a high state at the next Ø1 clock after PSYNC. This signal is created by clocking PSYNC into U10B by the Ø1 clock.

FIGURE 5.1.5 PHLDA



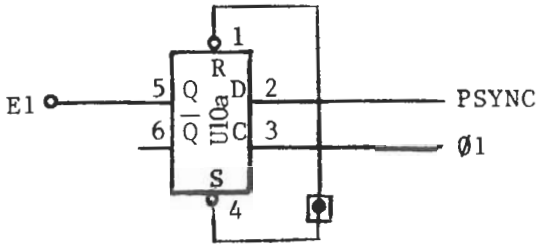
a. SCHEMATIC



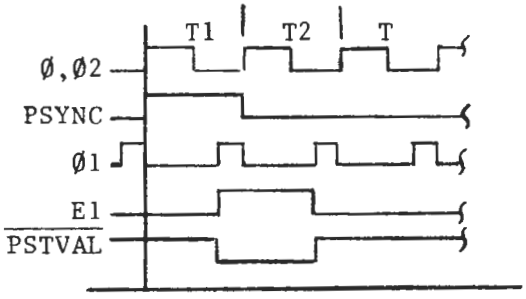
b. TIMING DIAGRAM

$\overline{\text{PSTVAL}}$ was allocated to pin 25 on the S-100 bus, which is the Ø1 pin on the old S-100 bus standard. Therefore, the user will have to decide which signal he wants to use. If $\overline{\text{PSTVAL}}$ is desired, then connect E1 to E44 and E42 to E43.

FIGURE 5.1.6 $\overline{\text{PSTVAL}}$



a. SCHEMATIC



b. TIMING DIAGRAM

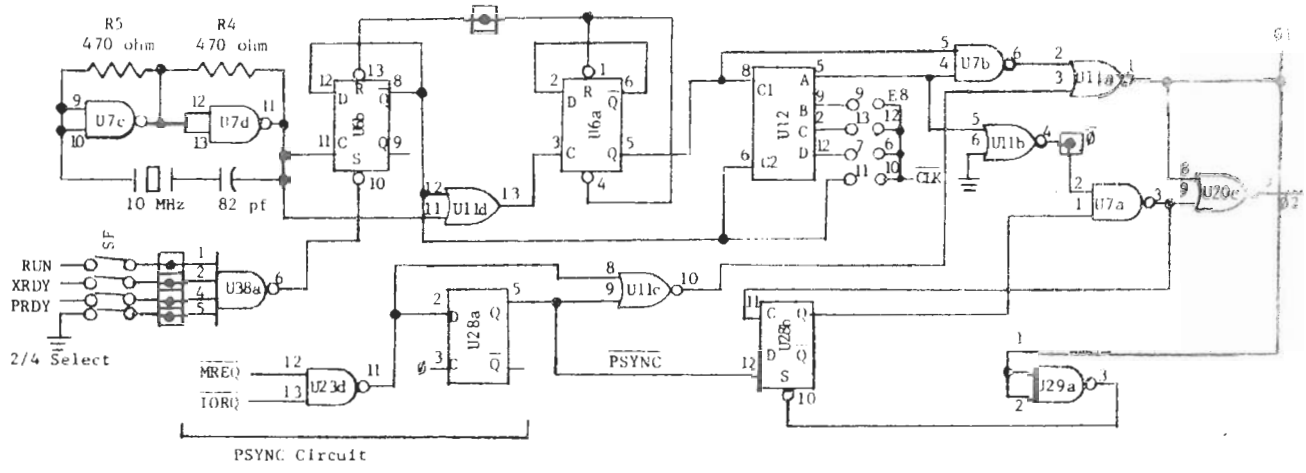
5.2 CPU Clock Circuits

The CB2 clock circuits consist of a crystal oscillator, a selectable divide-by-4/8 circuit, a circuit to generate a non-overlapping Ø1/Ø2, a circuit to inhibit all but one Ø1/Ø2 pulse during extended PSYNC's (see Figure 5.1.1), and a selectable fixed clock frequency for the CLK signal on the S-100 bus. The following descriptions will all refer to Figure 5.2.

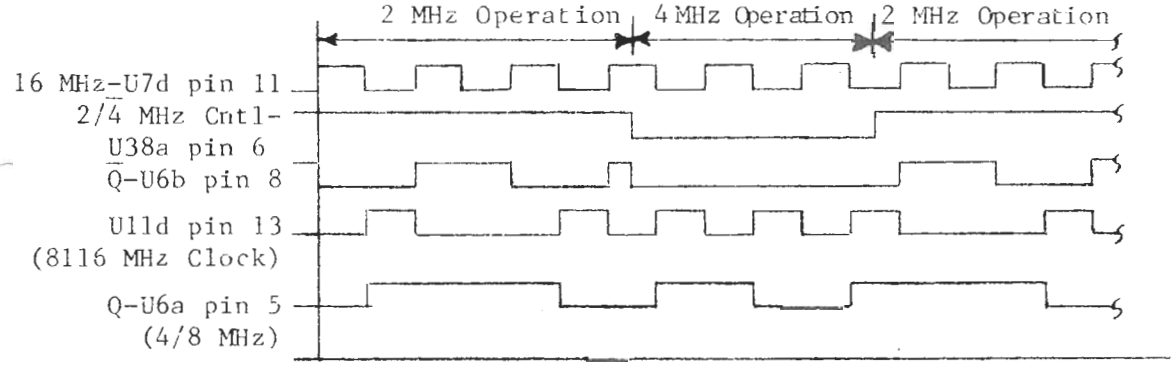
5.2.1 Crystal Oscillator

The oscillator circuit consists of two NAND gates (U7C and U7D) connected to form an oscillator with the 16 MHz crystal as the tuned element. Resistors R4 and R5 are feedback resistors to bias the NAND gates to operate in their linear regions. Capacitor C4 provides a DC voltage block for the crystal, which could be overstressed by a large DC potential. It also provides an extra phase shift to insure reliable operation.

FIGURE 5.2 CPU CLOCK CIRCUIT (Page 1 of 2)



a. SCHEMATIC

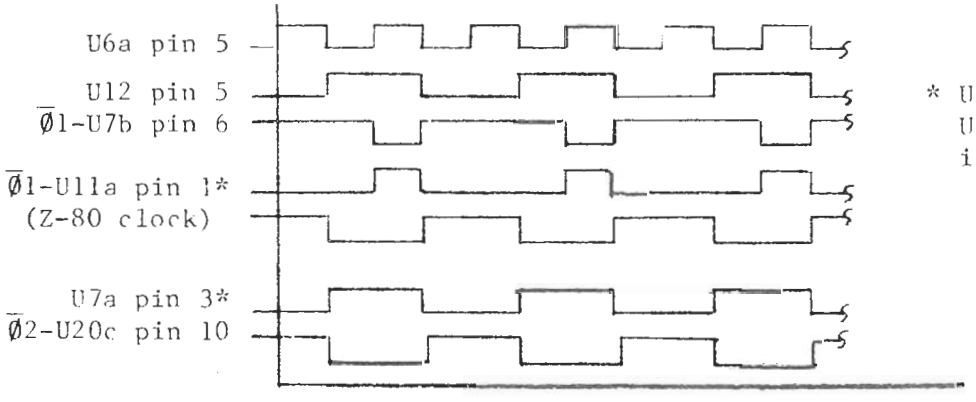


U38a TRUTH TABLE

RUN	XRDY	PRDY	2/4 Select	2/4 MHz Cntl
1	1	1	1	0
0	X	X	X	1
X	0	X	X	1
X	X	0	X	1
X	X	X	0	1

X=Don't care

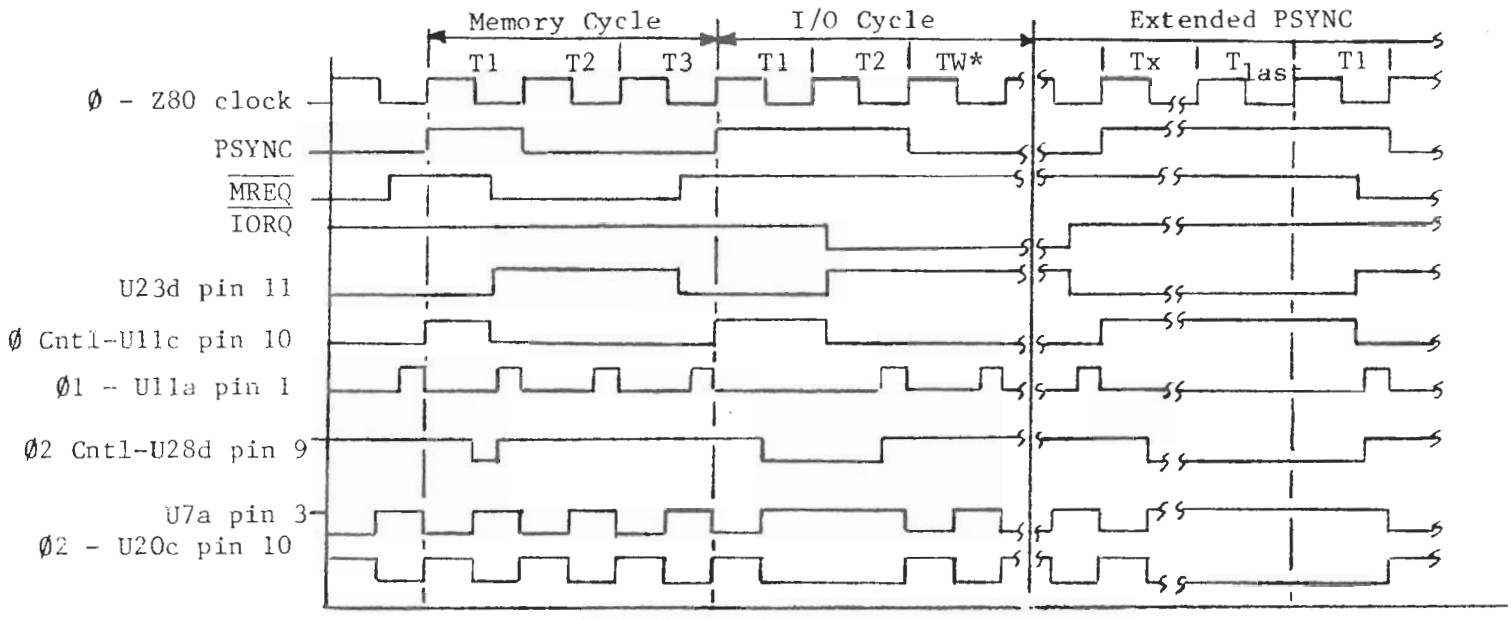
b. 2/4 MHz CIRCUIT TIMING



* U11a pin 3 is at logic 0 and U7a pin 1 is at logic 1, which is the non-inhibit state.

c. Ø1/Ø2 GENERATION CIRCUIT TIMING

FIGURE 5.2 CPU CLOCK CIRCUIT (Page 2 of 2)



d. Ø1/Ø2 INHIBIT CIRCUIT TIMING

5.2.2 Divide by 4/8 Circuit

This circuit consists of U6, U7, U11, and U12, which produce the two frequencies necessary to synthesize Ø1 and Ø2 for both 2 and 4 MHz operation.

The flip-flop U6B, when held in the set state by U38A, applies a constant logic 0 to U11D pin 12. The other U11D input (pin 11) is the crystal osciallator's output (16 MHz), which passes straight through U11 and is inverted. This provides the clock to U6A for 4 MHz operation.

When U6B is not held in the set state by U38A (a logic 1 at U6 pin 10), it changes states at half the frequency of the 16 MHz osciallator and inhibits every other clock pulse out of U11. This provides an 8 MHz clock to U6A for a 2 MHz operation of the CB2.

The dividers U6A and U12 divide the output of U11 by 4 to provide the phases necessary to synthesize Ø1 and Ø2.

5.2.3 Ø1/Ø2 Circuit

The Ø1 circuit consists of U7B and U11A. U7B produces a $\overline{Ø1}$ pulse by combining U12-QA (which is $\overline{Ø2}$ before it is

processed through the control gates) and U6-Q. The Ø1 pulse is produced by gating $\overline{Ø1}$ through U11A along with the Ø1 control signal, which is used to inhibit Ø1 during extended PSYNC's.

The Ø2 circuit consists of U11B, U7A, and U20C. U11B inverts the $\overline{Ø2}$ signal of U12-QA to produce the Z-80 clock. The Z-80 clock is gated (U7A) by the Ø2 control (which eliminates all but the first Ø2 pulse during extended PSYNC's) to produce $\overline{Ø2}$-PRIME.

The $\overline{Ø2}$-PRIME signal is gated and inverted by U20C, along with Ø1, to produce a Ø2 signal which cannot occur until after Ø1 falls. In this way, Ø1 and Ø2 are guaranteed not to overlap.

5.2.4 Ø1/Ø2 Inhibit Circuits

The Ø1 inhibit circuit consists of U11C, which combines $\overline{PSYNC}$ from U28A pin 5 and ($\overline{MREQ}$ · $\overline{IORQ}$) to produce a logic 1 when both of these signals are a logic 0. When U11C is at a logic 1, Ø1 is inhibited by U11A. This occurs during PYSNC until eihter $\overline{MREQ}$ or $\overline{IORQ}$ goes to a logic Ø, which allows Ø1 to occur and then PSYNC falls when Ø2 occurs.

The Ø2 inhibit circuit consists of U28B and U29A. U28B is triggered by Z-80 $\overline{CLOCK}$ and its D input is $\overline{PSYNC}$. Therefore, U28B-Q output is generally a logic 1 until PSYNC occurs. At this time, the Q output of U28B will go low on the rising edge of Z-80 $\overline{CLOCK}$. Now Ø2 cannot occur again until $\overline{Ø1}$ (generated by U29A) occurs. Effectively, all Ø2 clocks during PSYNC are inhibited, except for the first one.

During a normal PSYNC of one clock width, there is no change to Ø1 and Ø2. During a stretched PSYNC, there is still only one Ø1 and Ø2 pulse, but they may be separated by the equivalent of several clock cycles of time.

5.2.5 $\overline{CLK}$

In the original S-100 bus, this signal is the same frequency as Ø2 (2 MHz but with the opposite phase). In the new IEEE bus standard, it is still 2 MHz but has no definite phase relationship to Ø2.

The CB2 $\overline{CLK}$ circuit consists of part of U12, which divides the 16 MHz clock by 8. The 74197 does this by dividing by 2 three times. The output of each divide-by-2 stage and the 16 MHz clock are available to the user to be used as the $\overline{CLK}$ signals. This means the user can select either 16, 8, 4, or 2 MHz as $\overline{CLK}$.

5.3 CPU Status (S) Signals

In the original S-100 8080 CPU, these signals were taken from the Data Bus during PSYNC, and were then latched onto the S-100 bus through an 8212 or similar tri-stateable latch. The "S" signals indicate the type of data transfer to be performed (i.e., Memory, I/O, or Interrupt Acknowledge), the direction of data transfer (i.e., writing or reading) and the state of the CPU (i.e., Op-Code Fetch, stacking operation, and whether interrupts were enabled).

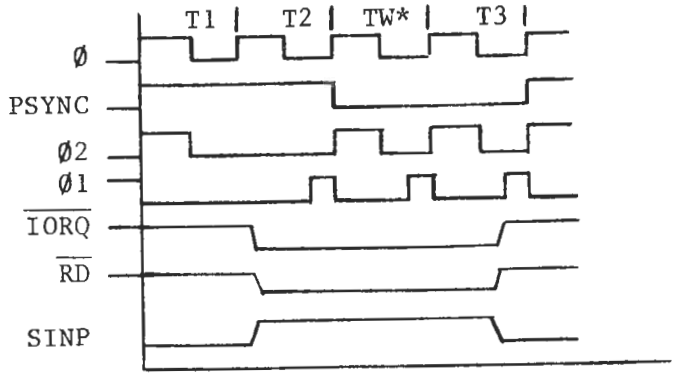
These signals do not occur on the data bus of the Z-80 as they do in the 8080. They are generated by logically combining the Z-80 control signals. An optional 2/4 MHz status signal is included to indicate when the CB2 is in 2 or 4 MHz mode of operation.

5.3.1 SINP

SINP (input) is used to indicate when the CPU is executing an input operation and is used by I/O circuits, along with address, to determine when they are being accessed. SINP is generated by U31B when $\overline{IORQ}$ and $\overline{RD}$ are both at logic 0. See Figure 5.3.1b for a timing diagram of an input operation.

FIGURE 5.3.1 SINP

a. SCHEMATIC

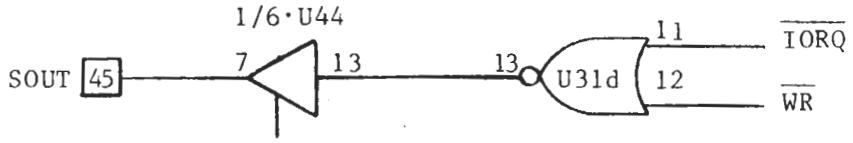


b. SINP TIMING

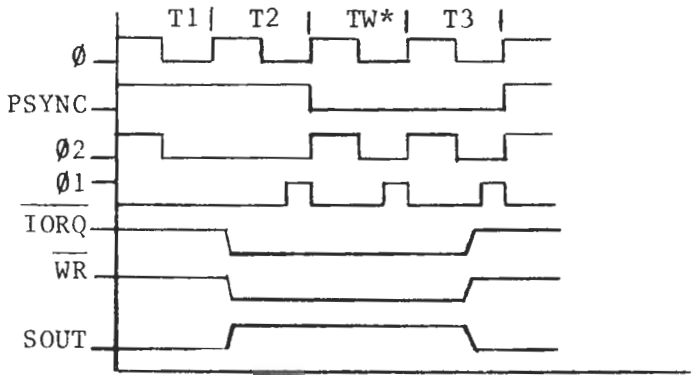
5.3.2 SOUT

SOUT (output) is used to indicate when the CPU is executing an output operation and is used by I/O circuits, along with address, to determine when they are being accessed. SOUT is generated by U31D when IORQ and WR are both at logic 0. See Figure 5.3.2b for a timing diagram of an output operation.

FIGURE 5.3.2 SOUT



a. SCHEMATIC

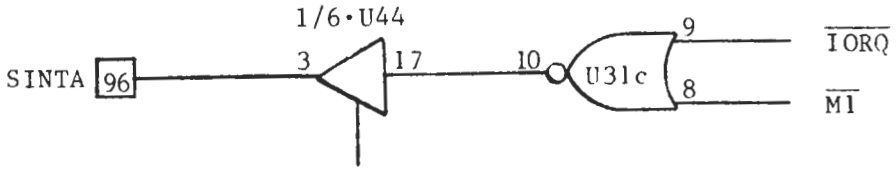


b. SOUT TIMING

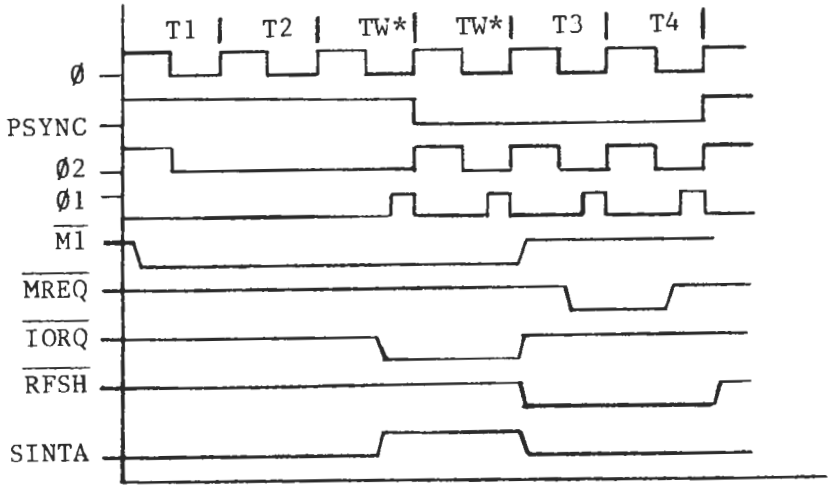
5.3.3 SINTA

SINTA (interrupt acknowledge) is used to indicate when the CPU is ready to receive a byte from an interrupting device. SINTA is generated by U31C when IORQ and M1 are both at logic 0. See Figure 5.3.3b for a timing diagram of an interrupt acknowledge operation.

FIGURE 5.3.3 SINTA



a. SCHEMATIC

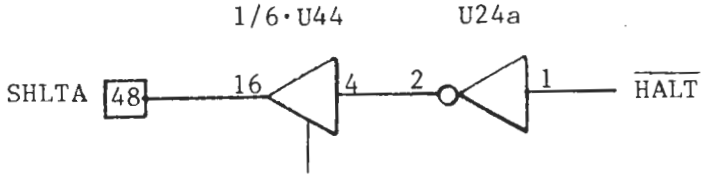


b. SINTA TIMING

5.3.4 SHLTA

SHLTA (halt acknowledge) is used to indicate when the CPU is in a halted state. A RESET or Interrupt is required to resume operation. SHLTA is generated by inverting the CPU HALT signal through U24A.

FIGURE 5.3.4 SHLTA Schematic



5.3.5 SM1

SM1 indicates, to external devices, when the CPU is in an Op-Code Fetch cycle. This signal is basically the same in 8080 and Z-80 operation, except for when the CPU is in a HALT state. The Z-80 puts out an M1 and the 8080 does not. Therefore, SM1 is the inversion of $\overline{M1}$ from the Z-80 and is inhibited by the SHLTA signal.

5.3.6 SMEMR

SMEMR (memory read) status indicates to external devices that a memory read operation is taking place.

The SMEMR circuit consists of U41B & C, U30B, U24C, and U37B. U41C puts out a logic 1 when both $\overline{MREQ}$ and $\overline{RD}$ are low. This logic 1 passes through U24C/U37B to become SMEMR, unless inhibited by U30B. Normally, U30B's $\overline{Q}$ output is a logic 1, but an interrupt acknowledge sets U30B, which inhibits SMEMR until the next M1 cycle.

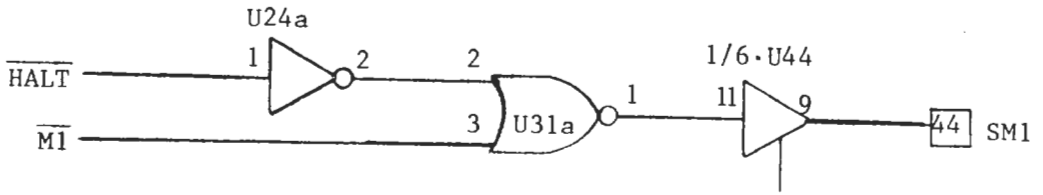
The reason for a SMEMR inhibit circuit on interrupts is because of the way the Z-80 CPU handles status on 2 or 3 byte instructions during an interrupt operation. The 8080 CPU did not turn on SMEMR during an interrupt operation, since it was not a memory operation. The Z-80 will try to indicate SMEMR on the second and third byte of an interrupt operation, which would cause a hardware conflict between the interrupt controller board and a memory board on the S-100 bus. The CB2 is designed to inhibit the SMEMR signal during an interrupt operation until the next SM1 cycle, to prevent bus conflicts.

5.3.7 $\overline{SWO}$

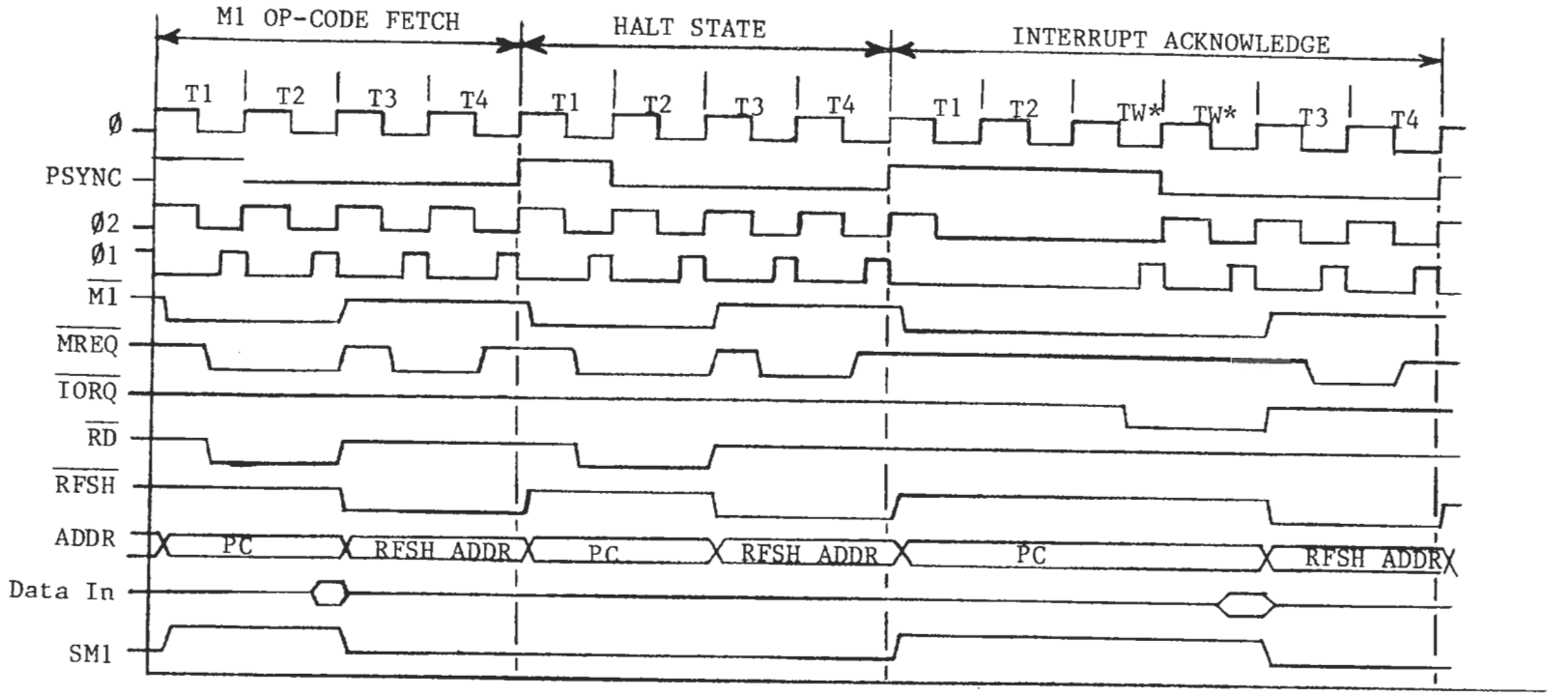
This signal indicates to external devices when data is being put on the data bus during a memory write or output operation.

The $\overline{SWO}$ circuit consists of U37D and U30A. The signal $\overline{WR}$ (from the Z-80) occurs too late in a memory write operation, so $\overline{RD}$ is used to generate the $\overline{SWO}$ signal. Therefore, if the CPU is not reading data, then the operation is a data out transfer.

$\overline{SWO}$ is generated by U37B, which inverts $\overline{RD}$. Because $\overline{RD}$ does not remain low during the entire memory read or input operations, U30A is used to inhibit $\overline{SWO}$ until the next PSYNC, which does occur on an M1 cycle. In this way, $\overline{SWO}$ does not change except under PSYNC, and does occur prior to $\overline{PWR}$ as it should.



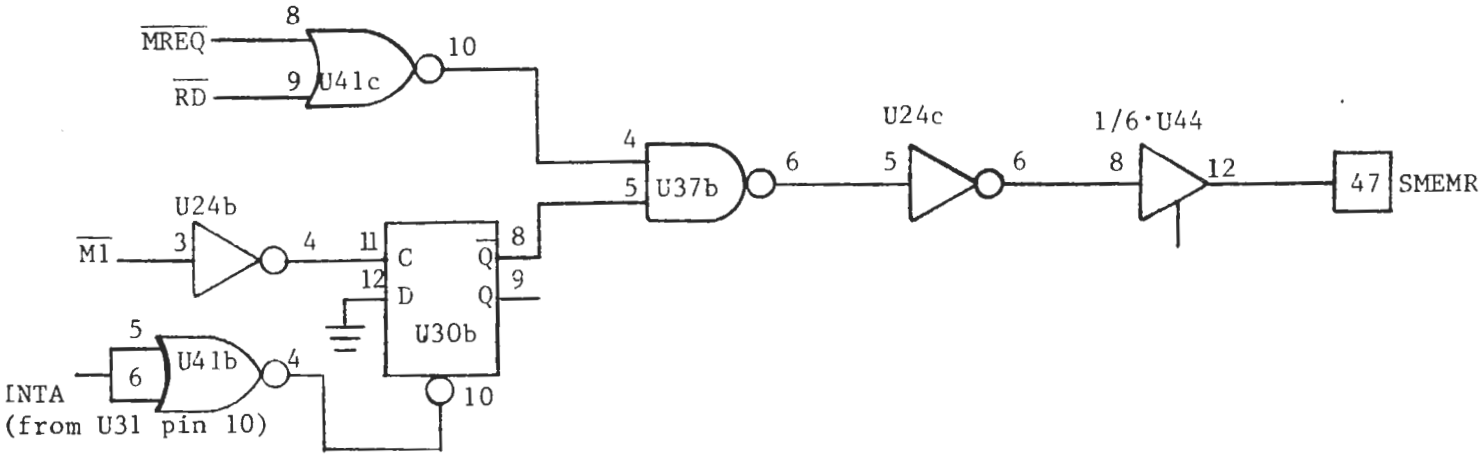
a. SCHEMATIC



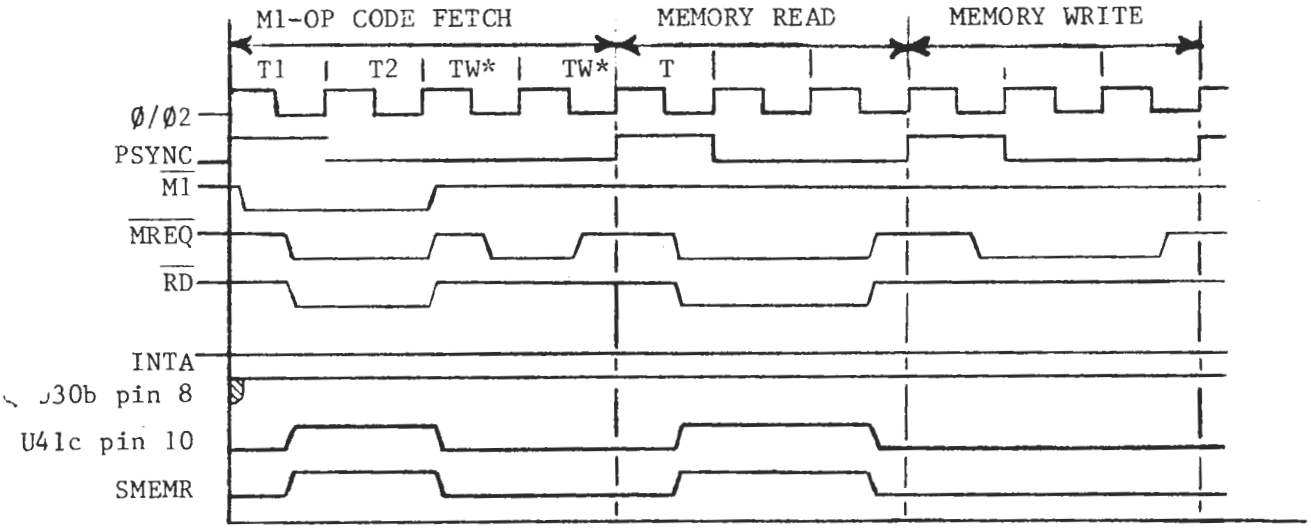
b. SM1 TIMING

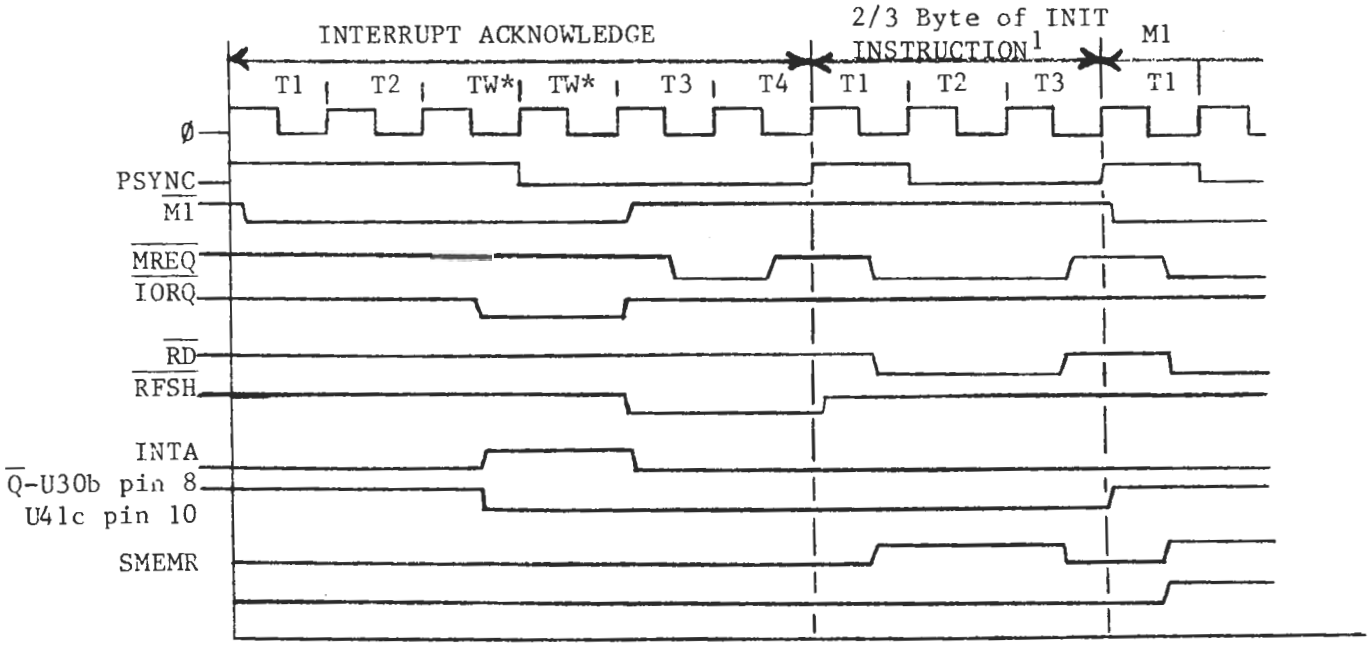
FIGURE 5.3.5 SM1

FIGURE 5.3.6 SMEMR



a. SCHEMATIC

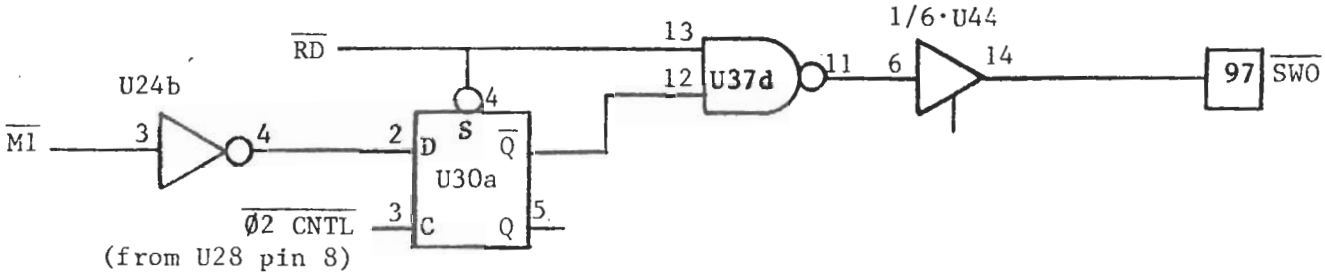




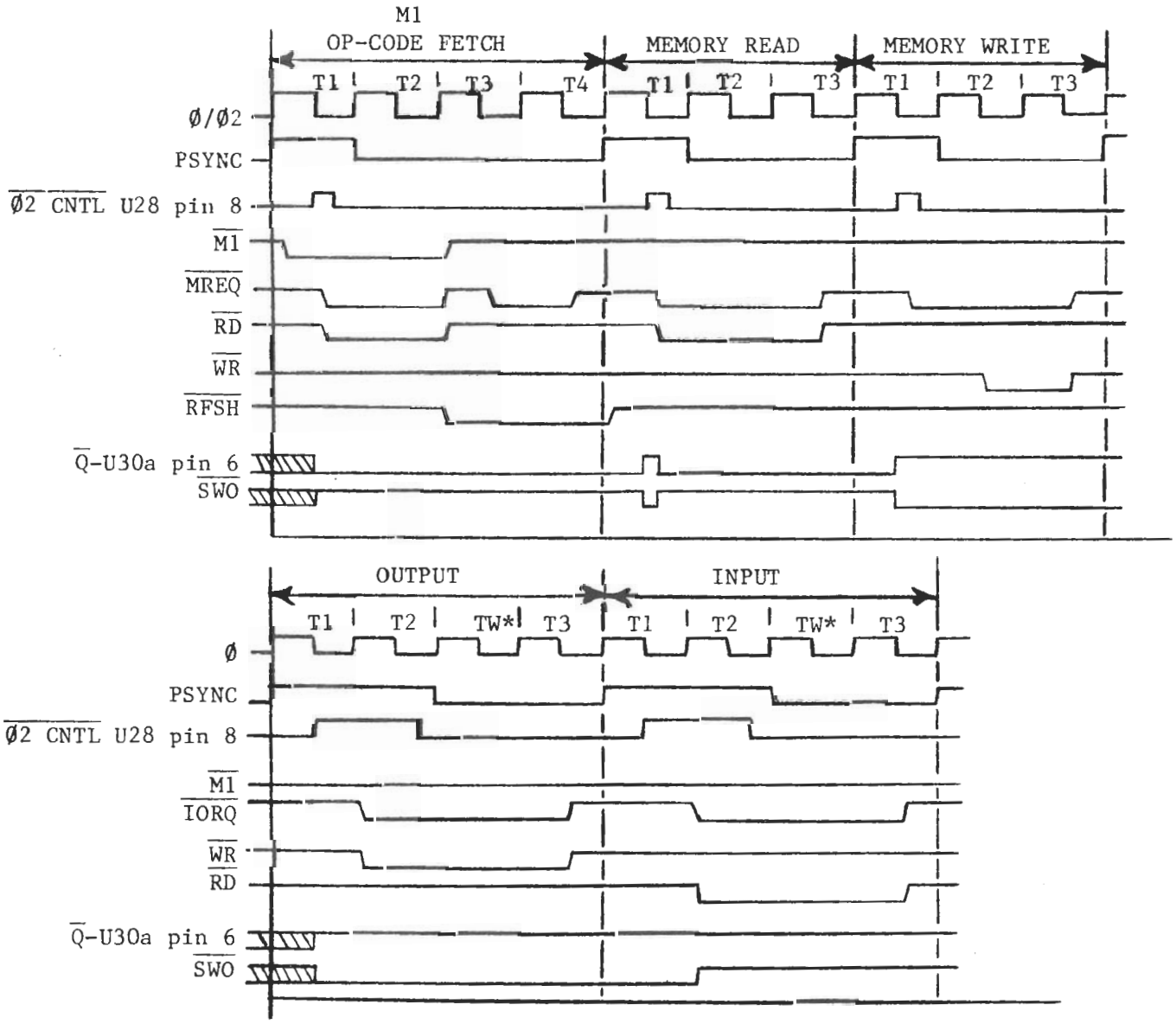
[1] This cycle applies only if the interrupt instruction has an address byte or word (i.e., JMP or CALL).

b. SMEMR TIMING

FIGURE 5.3.7 $\overline{SWO}$



a. SCHEMATIC



b. $\overline{SWO}$ TIMING

.3.8 4/$\overline{2}$ MHz* (Special Option)

This signal indicates the CPU clock rate to external devices. U26B inverts the 2/4 MHz control signal from U38A to generate this signal. A logic 1 means the CB2 is operating at 4 MHz, and a logic Ø indicates 2 MHz. Because this is not a standard S-100 signal, it remains for the user to connect it to the bus if desired. Bus pin 98 is STACK on the old S-100; it is 4/2 MHz for Cromemco systems; it is $\overline{\text{ERROR}}$ for the new IEEE standard.

5.4 External Control Signals

These are signals generated by external devices to control the CPU operation. They include XRDY, PRDY, $\overline{\text{PHOLD}}$, $\overline{\text{PINT}}$, $\overline{\text{NMI}}$, $\overline{\text{PRESET}}$/$\overline{\text{POC}}$, SINGLE STEP, RUN, $\overline{\text{SSW DSBL}}$, $\overline{\text{C/C DSBL}}$, $\overline{\text{STATUS DSBL}}$, $\overline{\text{ADDR DSBL}}$, and $\overline{\text{DO DSBL}}$.

5.4.1 The RDY Signals

The XRDY and PRDY signals are used to cause the CPU to enter into wait cycles. With these signals, slow memory and I/O devices can slow down the processor to their pace. They also provide a means for a front panel to stop the processor. The on board RUN/STOP and SINGLE-STEP circuits will also be discussed in this section.

5.4.1.1 XRDY and PRDY

The basic XRDY and PRDY circuit is made up of U34A & B, U20A, and U21. The XRDY and PRDY signals go to both the A & B AND gates of U34. U34B immediately sends a logic 0 to the Z-80 $\overline{\text{WAIT}}$ input when either XRDY or PRDY goes low. This allows an external device to request a wait state as late as 90 ns prior to the first falling edge of Ø2 after PSYNC goes low. This is needed because some status signals do not occur until just before PSYNC falls. The output of U34A goes to the reset and D inputs of U21A. This holds U21A reset until XRDY and PRDY are both high, and the next Ø2 pulse strobes a logic 1 in. While reset, U21A $\overline{\text{Q}}$ is a logic 1 and U20A is a logic 0. Therefore, U34B remains low, holding the CPU in a wait state, and U21A insures that the wait state is removed in sync to Ø2.

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* This signal is similar to the speed flag used by Cromemco.

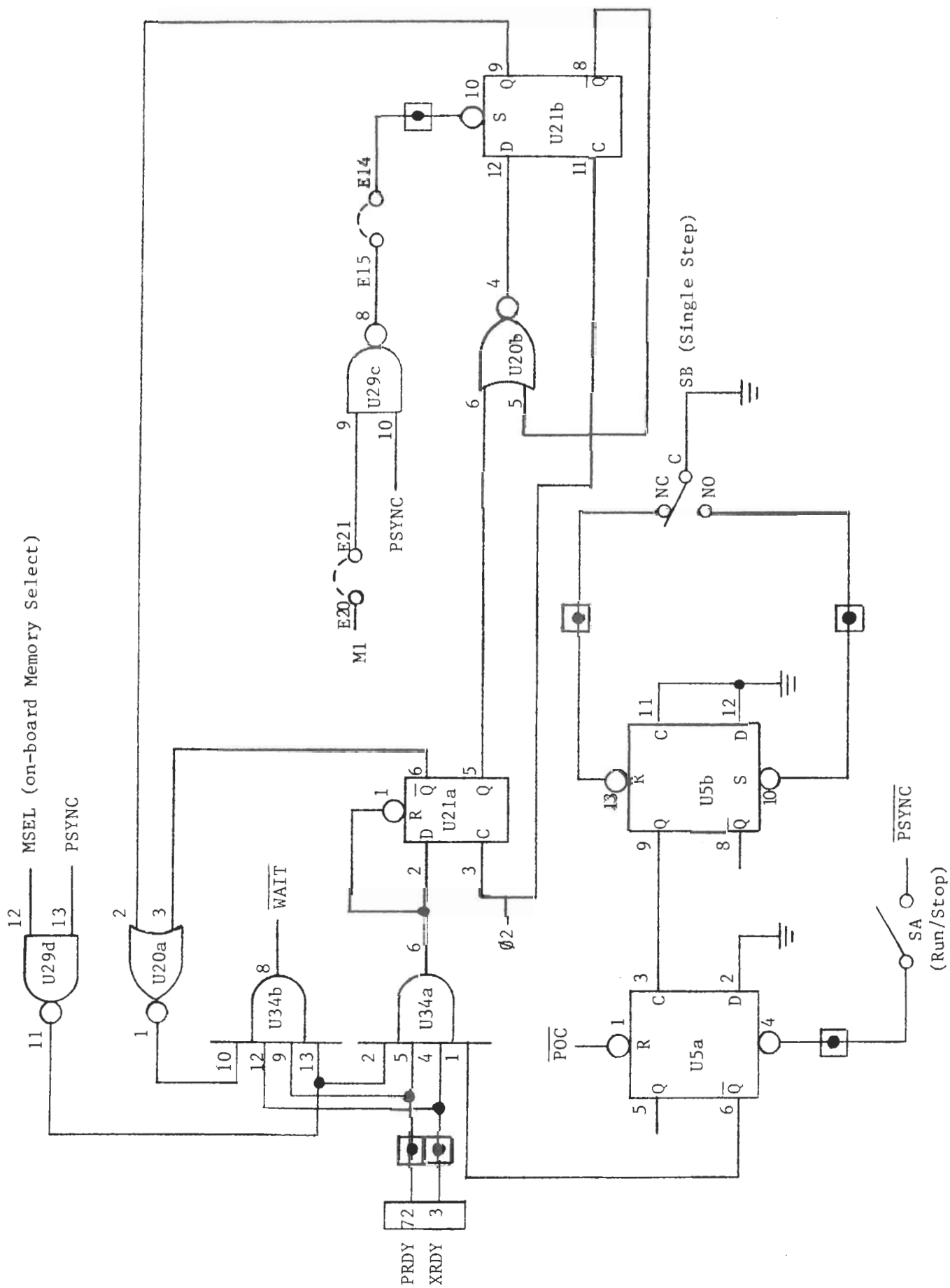
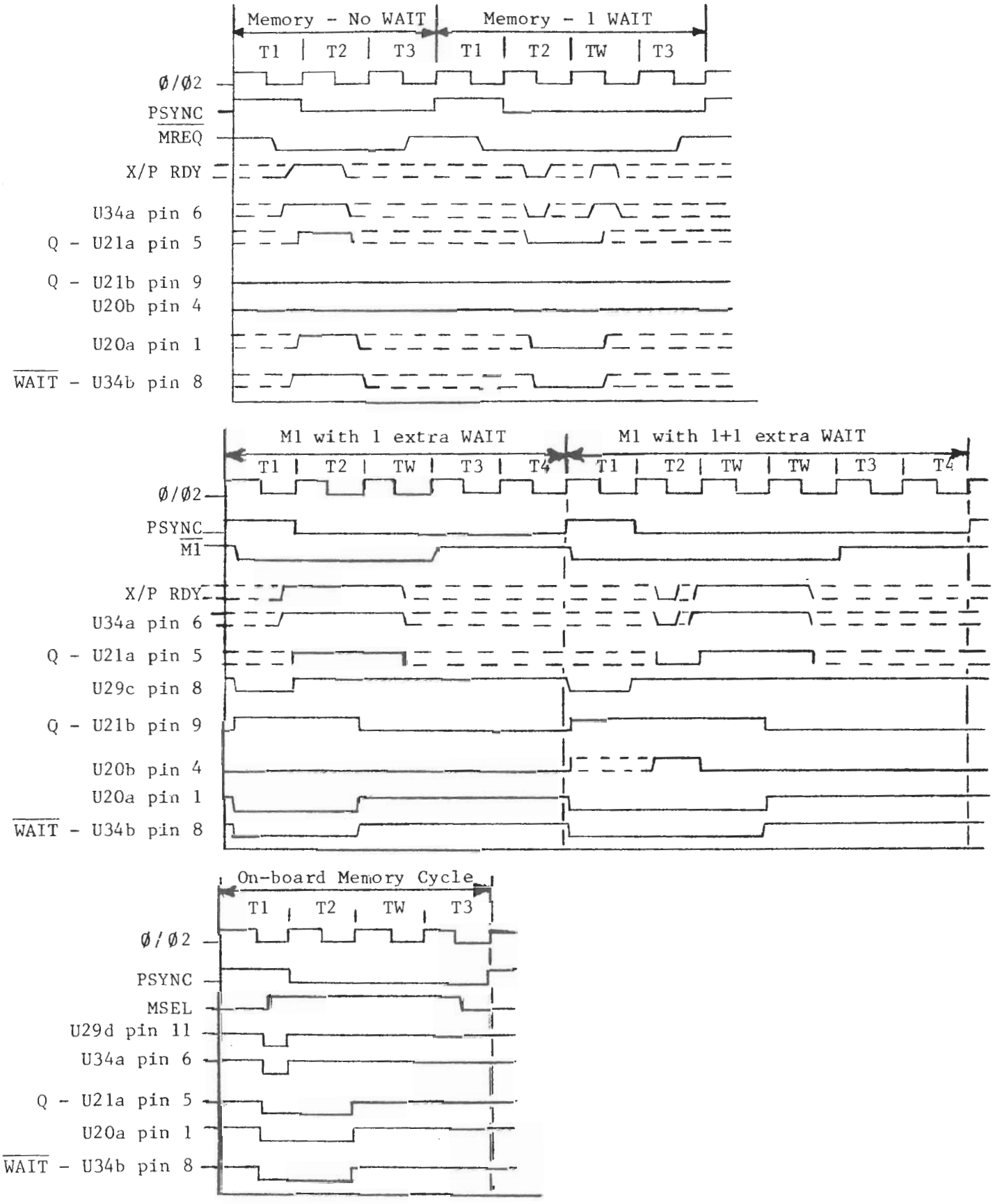


FIGURE 5.4.1 RDY CIRCUIT
a Schematic

FIGURE 5.4.1 RDY CIRCUIT
b. XRDY & PRDY Timing



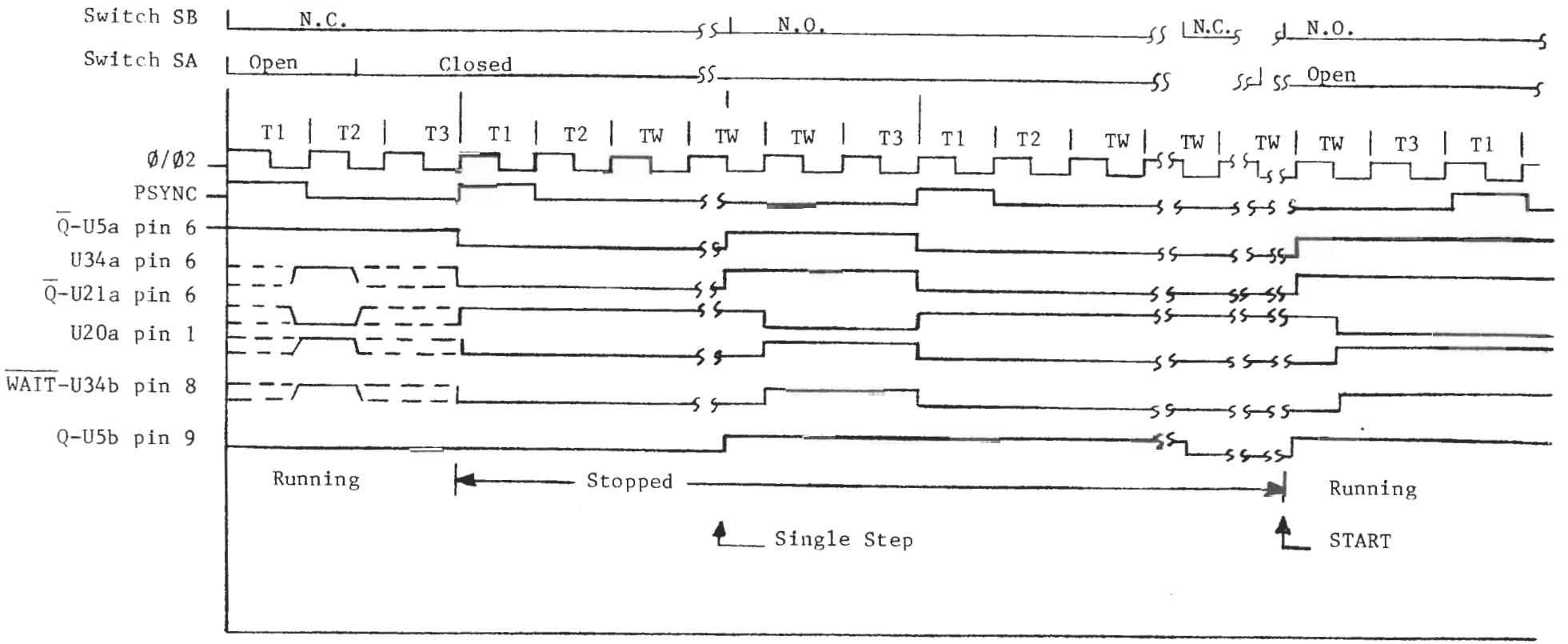


FIGURE 5.4.1 RDY - RUN/STOP - SINGLE-STEP CIRCUIT
c. RUN/STOP and SINGLE-STEP Timing

5.4.1.2 On-Board Memory Wait

The on-board memory, when enabled, generates one wait state by gating PSYNC and MADDR (from the memory chip select circuit) through U29D to apply a logic 0 to U34A & B. This logic 0 looks the same as an XRDY or PRDY, and remains low as long as PSYNC is high. Therefore, one wait state is sent to the CPU.

5.4.1.3 Extra M1 Wait State

An extra wait state can be added to each M1 cycle through the circuit of U20A & B, U21B, and U29C. This cirucit was incorporated in the wait circuit because the M1 cycle on the Z-80 is shorter than the other cycles. U29C combines PSYNC and M1 to set U21B, with a logic 1 to U20A. U20A (through U34B) causes a logic 0 to be applied to the CPU $\overline{\text{WAIT}}$ input. If XRDY or PRDY are also requesting a wait state, then U20B will see a logic 0 on both inputs, and a logic 1 is applied to U21B's D input. Therefore, U21B remains set until U21A changes state and then, one cycle later, U21B will be reset. If no XRDY or PRDY wait states are requested, then U21B is reset after one wait state is generated because of U20B applying a logic 0 to U21B's D input. U21B can be set only through its $\overline{\text{SET}}$ input because when it is in the reset state, it applies a logic 1 (U21B $\overline{Q}$ output) to U20B, and a logic 1 on either of U20B's inputs causes a logic 0 to be applied to U21B's D input.

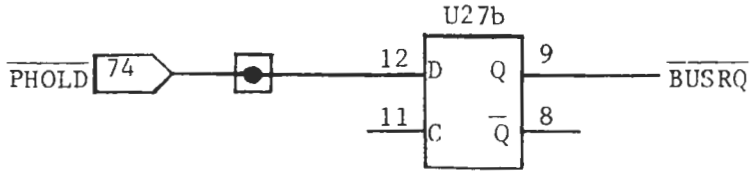
5.4.1.4 On-Board RUN/STOP and SINGLE-STEP

The on-board RUN/STOP (R/S) and SINGLE-STEP (SS) allow the user to do some limited troubleshooting of the CPU and computer systems without a front panel. The R/S flip-flop U5A is set by PSYNC whenever switch SA is closed. This applies a logic 0 (U5A-$\overline{Q}$) to U34A, which puts the CPU in a wait state. The CPU will remain in a wait state until U5B is reset by a clock pulse from U5A. When clocked by U5A, U5B will release the CPU from the wait state but will again stop the CPU at the next PSYNC if SA remains closed. In this way, the CPU is single-stepped. To restart the CPU, the switch SA is opened and SB is toggled to clock U5B. The flip-flop U5A is used as a switch debouncer.

5.4.2 $\overline{\text{PHOLD}}$

The $\overline{\text{PHOLD}}$ is applied to U27B, which synchronizes it with Ø2. $\overline{\text{PHOLD}}$ indicates that another device wishes to gain control of the bus for a DMA (Direct Memory Access) operation.

FIGURE 5.4.2 $\overline{\text{PHOLD}}$



5.4.3 $\overline{\text{PINT}}$ and $\overline{\text{PNMI}}$

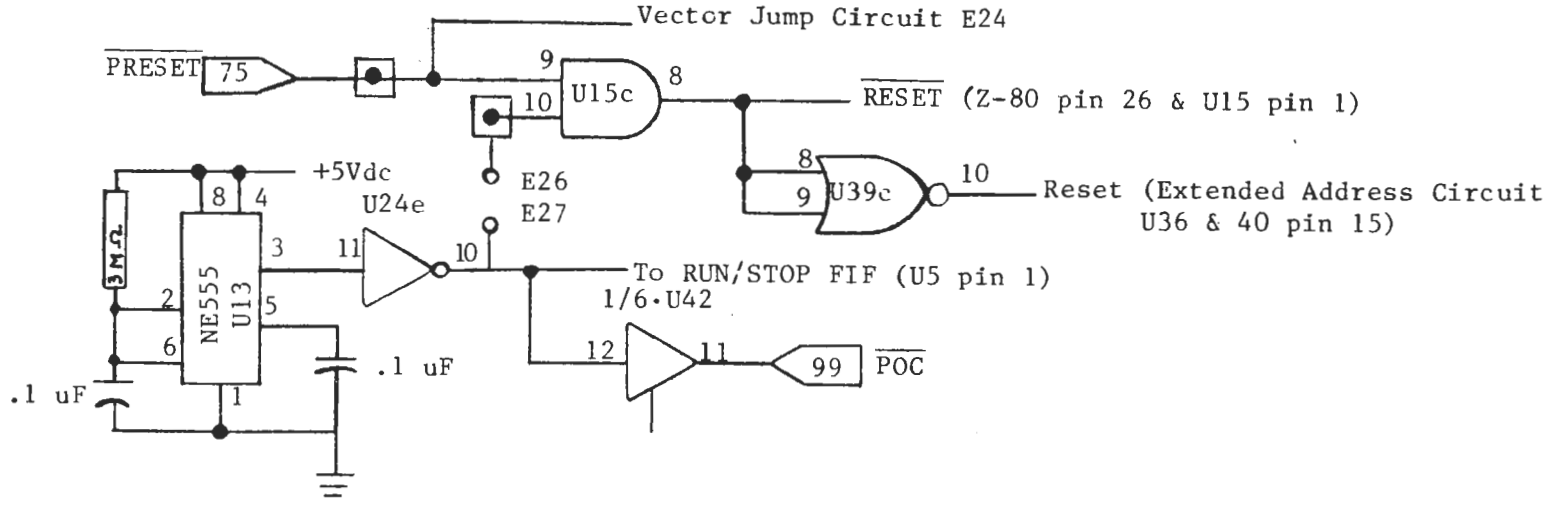
These are interrupt request signals from other devices, and are buffered by U15B & D. $\overline{\text{PINT}}$ will be serviced by the CPU if the interrupts are enabled. $\overline{\text{PNMI}}$ is always serviced since the interrupt enable flag in the CPU has no effect on it.

5.4.4 $\overline{\text{PRESET}}$/$\overline{\text{POC}}$

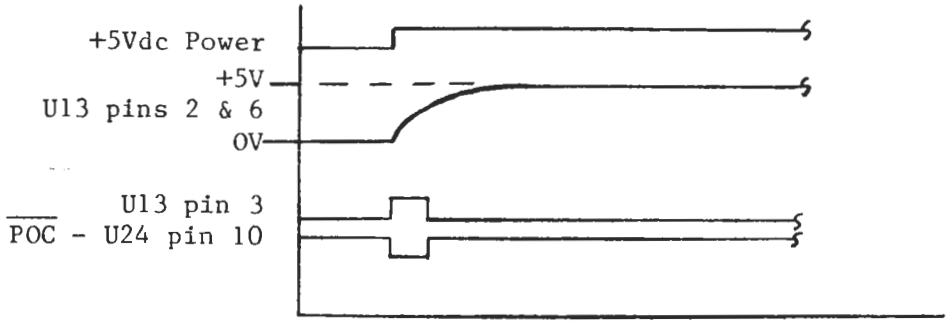
$\overline{\text{PRESET}}$ is buffered and combined optionally with $\overline{\text{POC}}$ to produce a $\overline{\text{RESET}}$ to the CPU when either input is low. $\overline{\text{PRESET}}$ resets the CPU, the PSYNC circuit, and the vector jump circuit.

$\overline{\text{POC}}$ is generated by U13 (555 timer) connected as an oscillator, except the discharge transistor (pin 7) is not connected. Therefore, upon application of power, the 555 turns on (pin 2 is below 1/3 Vcc) and the capacitor charges up. When the voltage on the capacitor reaches 2/3 Vcc (pin 6), the 555 output is turned off. The capacitor remains charged as long as power is applied. U24 inverts the 555 output to produce a $\overline{\text{POC}}$. $\overline{\text{POC}}$ resets RUN/STOP flip-flop (so the CPU comes up running if the RUN/STOP switch is open), and is applied to the $\overline{\text{POC}}$ bus driver, and is optionally applied to U15C to reset the CPU and PSYNC circuit.

FIGURE 5.4.4 $\overline{\text{PRESET}}$ & $\overline{\text{POC}}$



a. SCHEMATIC



b. $\overline{\text{POC}}$ TIMING DIAGRAM

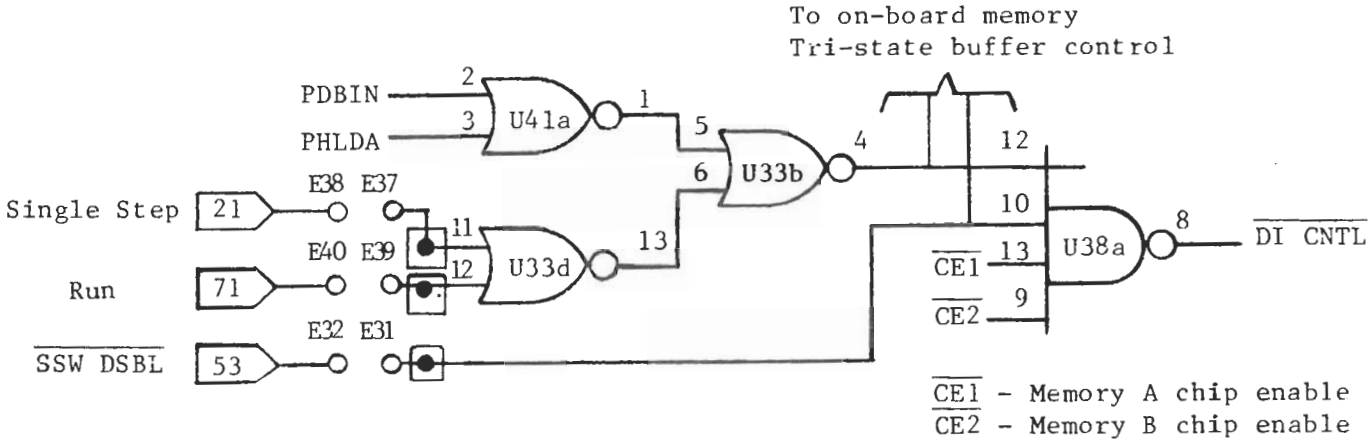
5.4.5 SINGLE-STEP - RUN - $\overline{\text{SSW DSBL}}$

These three signals, along with PDBIN, PHLDA, Memory A and B $\overline{\text{CS}}$ (which are on-board signals), control the data coming into the CPU's bi-directional data bus. This is necessary to insure that the DATA-IN (DIØ thru DI7) and the on-board-memory tri-state drivers are not enabled when the CPU is trying to output data, and to allow front panel circuits to place instructions on the CPU's data bus without interference from other devices.

The RUN and SINGLE-STEP signals are similar, except that the RUN signal can also control the 2/4 MHz operation of the board. Both of these signals are generated by front panel circuits to control the DI bus and on-board memory

(when both are low, the DI bus and on-board memory are disabled). See Figure 5.4.5b for a truth table of this circuit operation. RUN, SINGLE-STEP, and $\overline{\text{SSW DSBL}}$ are optional signals on the CB2 because they are not part of the new IEEE standard bus. If not connected to the bus, they default to allow the CPU to operate normally.

FIGURE 5.4.5 SINGLE-STEP - RUN - $\overline{\text{SSW DSBL}}$



a. SCHEMATIC

PDBIN	PHLDA	SINGLE STEP	RUN	$\overline{\text{SSW DSBL}}$	U41a	U33d	U33b	$\overline{\text{CE1}}$	$\overline{\text{CE2}}$	U38a	DATA IN BUS	ON-BOARD MEMORY READ
1	X	1	X	1	0	0	1	1	1	0	Enabled	Disabled
1	X	X	1	1	0	0	1	1	1	0	Enabled	Disabled
X	1	1	X	1	0	0	1	1	1	0	Enabled	Disabled
X	1	X	1	1	0	0	1	1	1	0	Enabled	Disabled
0	0	X	X	X	1	X	0	X	X	1	Disabled	Disabled
X	X	0	0	X	X	1	0	X	X	1	Disabled	Disabled
X	X	X	X	0	X	X	X	X	X	1	Disabled	Disabled
1	X	1	X	1	0	0	1	0	1	1	Disabled	Enabled
1	X	X	1	1	0	0	1	0	1	1	Disabled	Enabled
X	1	1	X	1	0	0	1	0	1	1	Disabled	Enabled
X	1	X	1	1	0	0	1	0	1	1	Disabled	Enabled
1	X	1	X	1	0	0	1	1	0	1	Disabled	Enabled
1	X	X	1	1	0	0	1	1	0	1	Disabled	Enabled
X	1	1	X	1	0	0	1	1	0	1	Disabled	Enabled
X	1	X	1	1	0	0	1	1	0	1	Disabled	Enabled

b. TRUTH TABLE

$\overline{\text{SSW DSBL}}$, when low, disables the DI bus tri-state drivers and the on-board memory tri-state drivers, so an external circuit (i.e., front panel) can put data on the CPU's internal data bus via the header W2.

5.4.6 (STATUS, ADDR, C/C & DO) $\overline{\text{DSBL}}$ Signals

These signals, when low, disable the CPU's status, address, control, and data output tri-state drivers. These signals allow external devices to take control of the S-100 bus during DMA data transfers.

5.5 Address Bus

The Z-80 has 16 address lines (65,536 possible memory locations and 256 I/O ports) that are not multiplexed with anything else. These address lines are buffered by 74LS244 octal bus drivers as shown in Figure 5.5. Two sets of buffers drive the high address lines (A8 thru A15) in order to duplicate the low address onto the high address bus during I/O operations (as does an 8080 CPU). IC's U1A & B, U3D, and U23A control the address bus buffers, as shown in the truth table of Figure 5.5b. The multiplexing of the low address onto the high address bus during I/O operations is optional, and is enabled by connecting E22 to E23 on the CB2.

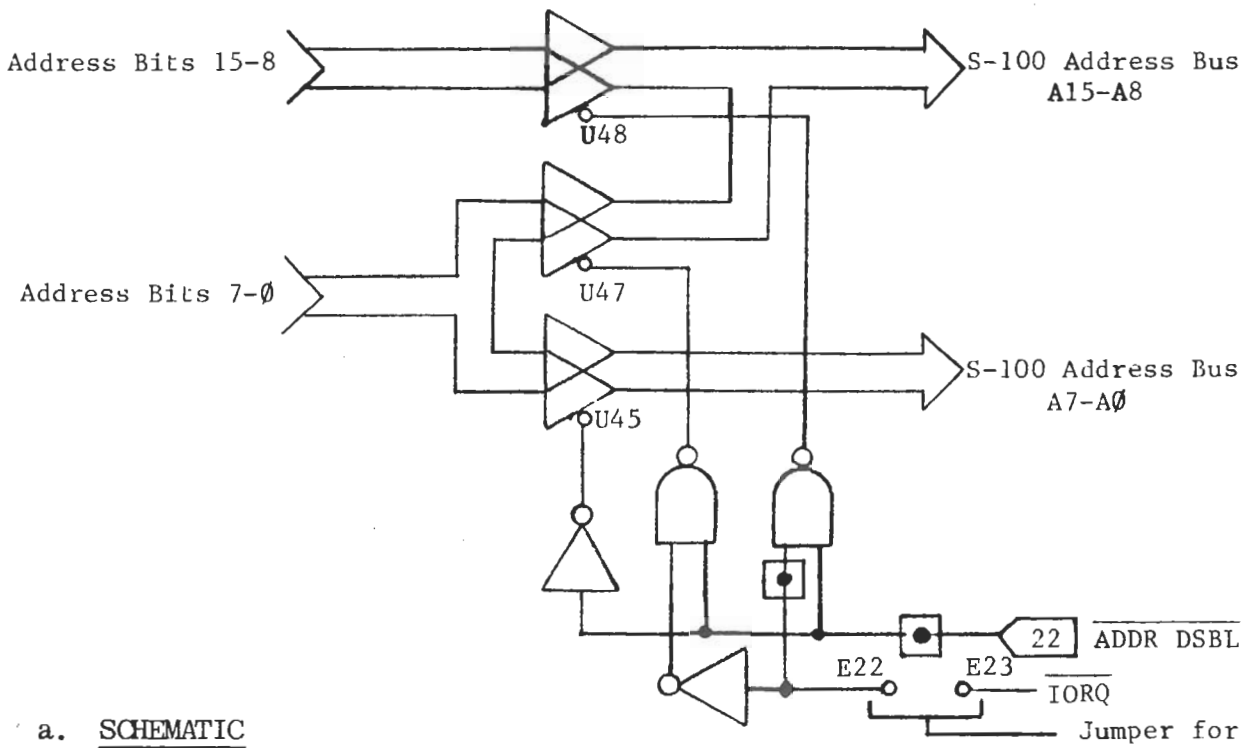
5.6 Data Bus

The data bus in the S-100 system consists of two 8-bit buses: a data-out bus (DO Ø thru 7) for data transfers from the CPU to external devices (i.e., memory and I/O cards), and a data-in bus (DI Ø thru 7) for data transfers from external devices to the CPU.

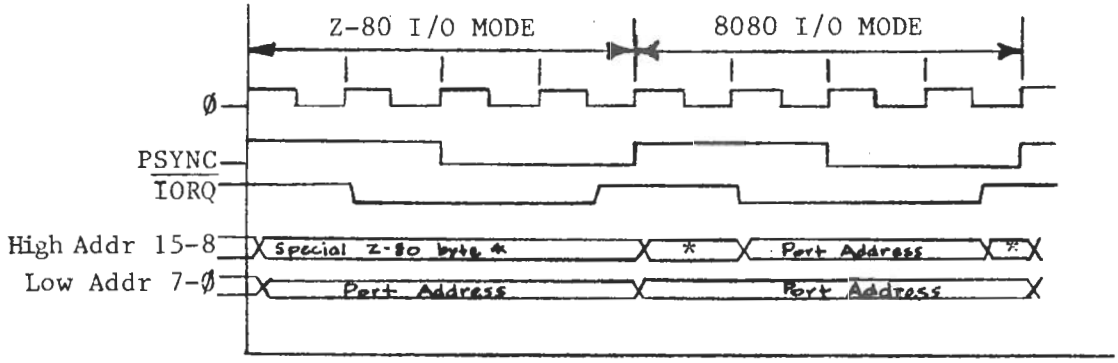
The data-out bus is driven by U49 (which buffers the CPU data lines from the heavy loads on the DO bus) and is normally enabled (since only the CPU drives this bus, except during DMA operations). $\overline{\text{DO DSBL}}$ controls tri-stating of this bus on the CB2.

The data-in bus is buffered by U50, which is tri-stated during CPU write operations, on-board memory operations, and certain front panel operations. Tri-state control of the data-in bus (U50) is discussed in Section 5.4.5 of this manual. The data-in bus lines are pulled up to +5 Vdc by RP9 (SIP) and R18, which helps to guarantee a logic 1 on the bus when nothing is driving it.

FIGURE 5.5 ADDRESS BUS



a. SCHEMATIC



* The high address bits during I/O in the Z-80 contain the accumulator contents during normal I/O and contain the B register bits during block transfer I/O (B register is the byte counter).

b. ADDRESS BUS I/O TIMING

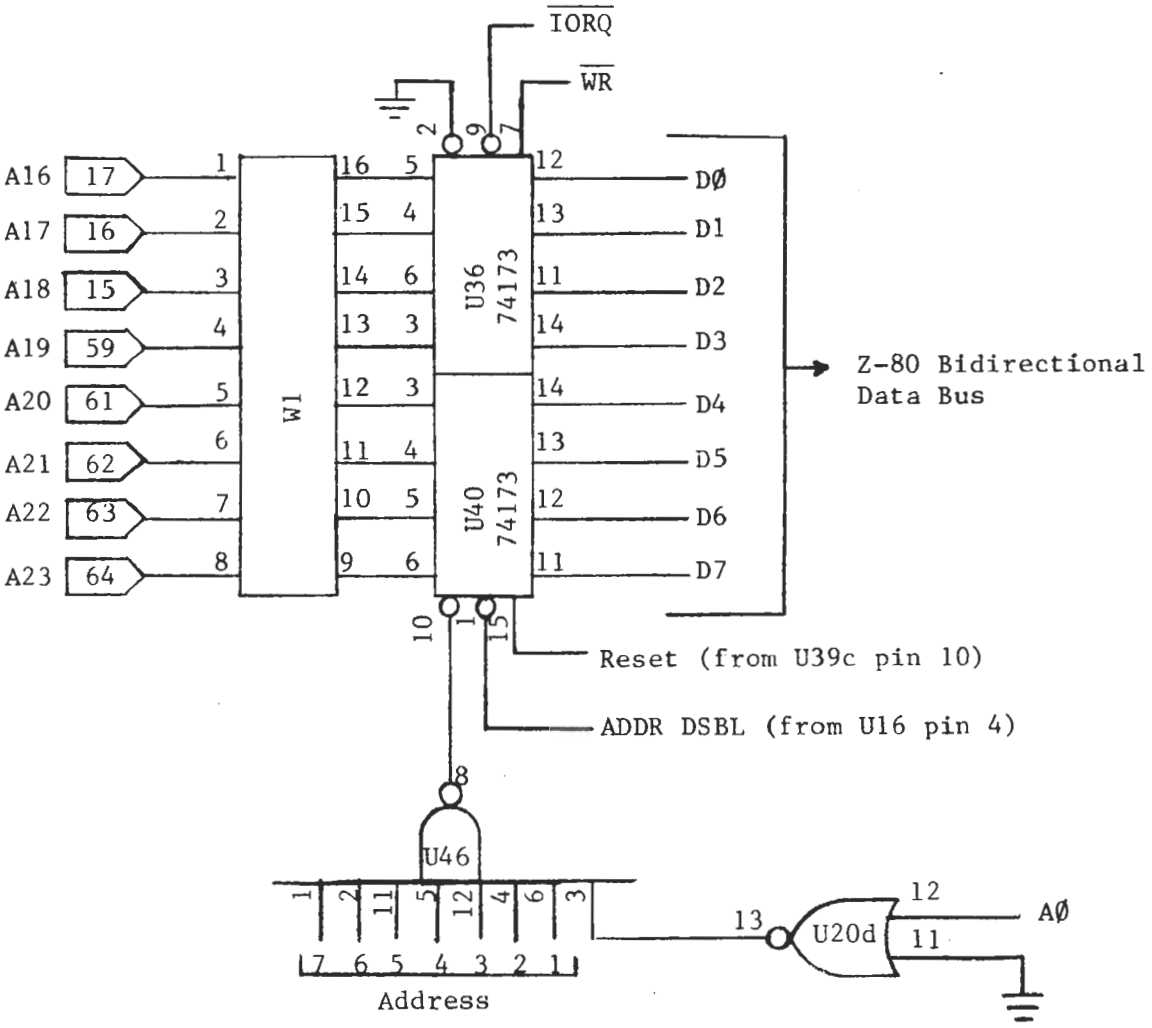
Internally, the CPU data bus is bi-directional and has a pull-up resistor network (RP8 and R17) to help speed up the transitions from logic 0 to logic 1 on the internal bus lines. Also, a header socket (W2) is provided. This allows front panel circuits to drive and sense the CPU data bus directly.

5.7 Extended Address Port

This circuit is an output port at address ØFEH. U46 and U20d decode the address ØFEH and put a logic 0 on U36 & 40 pin 10 as one write enable. $\overline{IORQ}$ from the Z-80 provides the other write enable to U36 & 40 at pin 9. The data is clocked into U36 & 40 (pin 7) by $\overline{WR}$. The latches U36 & 40 are reset when the CPU is reset, so the address will be ØØØØØØH. The tri-state output enable is controlled by U1, as are the low address buffers.

The port output goes to a header socket (W1) so that it can be used as an output port, or can be used as extended address bits (if W1 is strapped straight across).

FIGURE 5.7 EXTENDED ADDRESS PORT



5.8 On-Board Memory

There are two on-board-memory sockets with independent address circuits. Each socket can accept either 2716, 2732, or TMS 4016 memory chips.

Data is transferred to and from the memories through the tri-state buffers U18 and U19. U18, U19, and the output enable ($\overline{OE}$) of the memories are controlled by U2A & B. When one of the memories is selected (U3C, pin 8=logic 1), and $\overline{SSW\ DSBL}$ is high, and DBIN is high, then U2B outputs a logic 0 to enable data onto the CPU data bus. When any one of the signals to U2B is low, the U18 is tri-stated and U19 is turned on. Because the memories are also tri-stated, U19 and the memories are not in conflict.

The chip select ($\overline{CS}$) circuit is identical for both memories. Therefore, memory A will be described and the appropriate circuit elements for the B memory will be indicated in parentheses ().

U9 provides buffering and address inversion for the upper 6 address bits (upper 5 bits for 4K memories) to the address comparator circuit. The address for memory A is selected by dip switch SC (SD) and is compared by U8 & U14D (U4 & U14A). When the address bits and the dip switch settings are in opposite logic states, the comparator outputs will all be a logic 1. The outputs are open collector and pulled up by a resistor. Therefore, if any XOR gate has matching inputs it will be a logic 0 to U3 pin 2 (U3 pin 5). When U3A (U3B) receives a logic 1 from the comparator and MREQ from inverter U14C, then memory A (B) is selected. The chip select ($\overline{CS}$) for memory A only is enabled by either Vector Jump enable or by the output of U3A. (A jump instruction should be the first three addresses of Memory A if a POC or RESET is strapped for a vector jump.) U3C produces a logic 1 (MSEL) when either memory is selected.

Pin 21 on the memories is a multi-purpose pin. It is an address (A11) input for 2732. It is $\overline{WR}$ input for TMS 4016 (or equivalent 2K RAM). It is the Vpp pin on the 2716, which is held at the +5 Vdc during normal operation. The switches of SE select which type of input (A11, WR, or +5Vdc) each memory will receive.

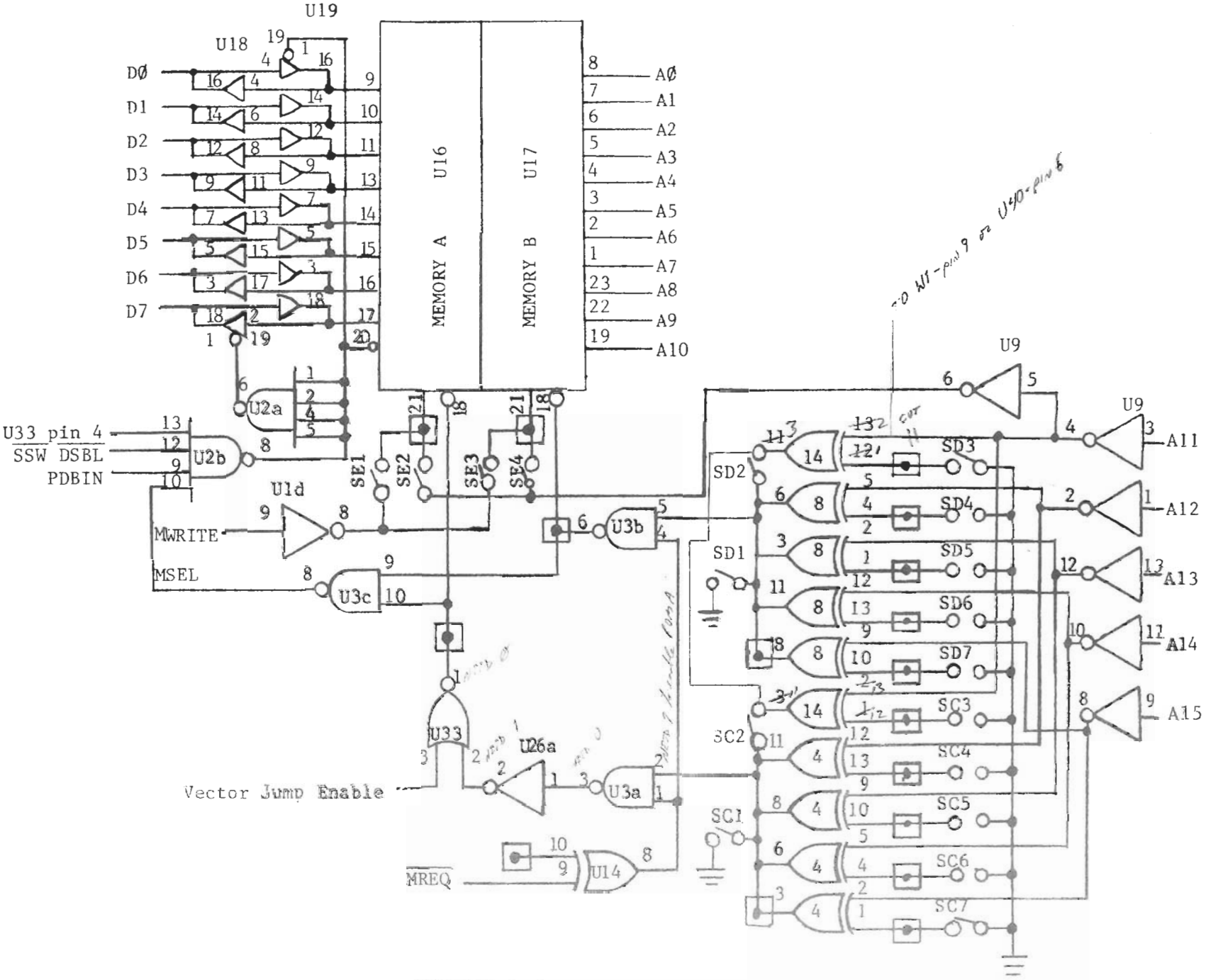


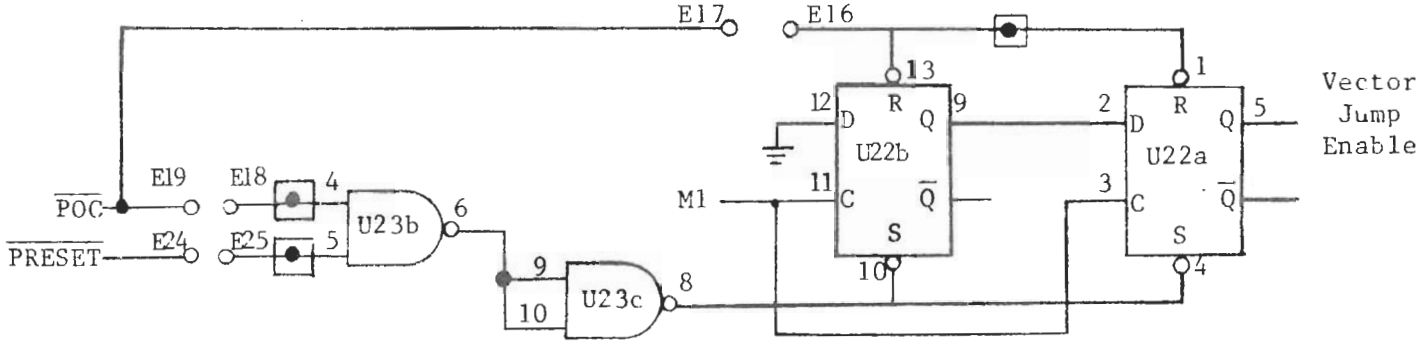
FIGURE 5.8 ON-BOARD MEMORY

5.9 Vector Jump

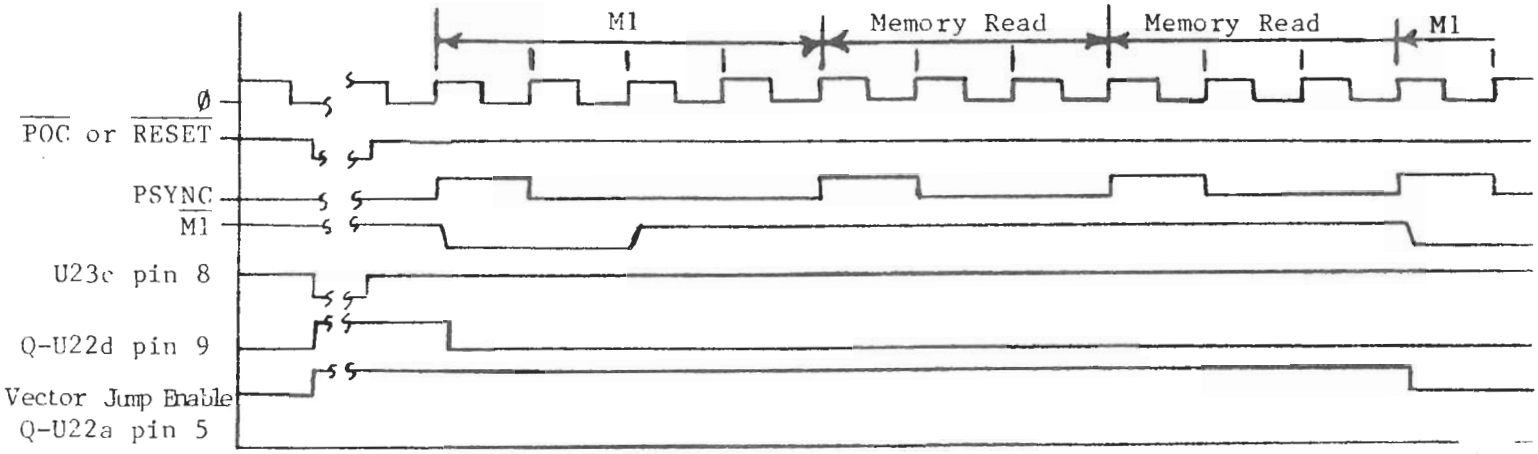
A vector jump is initiated by $\overline{POC}$ and/or $\overline{PRESET}$ when jumpers E18 & E19 and/or E24 & E25 respectively are installed. U23B & C form an AND gate so that when either input is low, U22A & B are both set. If no vector jump is desired, the E18, E19, E24 & E25 should be left open and E16 & E17 should be connected, so that U22A & B are reset by $\overline{POC}$.

U22A & B are connected to form a two-bit shift register that will shift logic 0's across when clocked. M1 is the clock signal for the shift register. Therefore, U22B is clocked to logic 0 on the first M1, which is the vector jump Op-Code Fetch. U22A is clocked to a logic $\emptyset$ on the second M1, which releases memory A and allows the computer to operate normally. In this way, one instruction at the beginning of memory A is executed (which should be a jump instruction).

FIGURE 5.9 VECTOR JUMP



a. SCHEMATIC



b. VECTOR JUMP TIMING

6.0 TROUBLESHOOTING HINTS

This section assumes the user has some basic knowledge of logic circuits and has read the theory of operation section of this manual. It is also assumed that the user has or has access to a voltmeter and a logic probe or an oscilloscope.

6.1 Verify that all IC's are in the correct sockets, and that none of the IC pins are bent under, and the IC is installed with the correct orientation.

6.2 Verify that each regulator is putting out +5 volts.

6.3 Verify that all necessary options have been connected properly.

6.4 Check for proper settings of DIP switches.

6.5 Inspect the back side of the board for any solder bridges. Run a small sharp knife blade between traces that may appear suspicious. A magnifying glass is recommended for this inspection.

6.6 If the CPU does not appear to be working, then make the following checks:

6.6.1 Verify that the RUN/STOP switch is in the RUN position and try toggling the SINGLE-STEP switch.

6.6.2 Verify the clock (2 MHz or 4 MHz) at Z-80 pin 6. (WARNING: IF THERE IS NO CLOCK AT THE Z-80, THE Z-80 COULD BE DAMAGED. THEREFORE, REMOVE THE Z-80 UNTIL THE CLOCK IS FIXED.)

6.6.3 Verify +5Vdc at Z-80 pin 11.

6.6.4 Verify that $\overline{\text{RESET}}$ at Z-80 pin 26 is not continuously low.

6.6.5 Verify that $\overline{\text{WAIT}}$ at Z-80 pin 24 is not continuously low.

6.6.6 Verify that $\overline{\text{BUSRQ}}$ at Z-80 pin 25 is not continuously low.

6.6.7 Verify that $\overline{\text{C/C DSBL}}$, $\overline{\text{STATUS DSBL}}$, $\overline{\text{DO DSBL}}$, $\overline{\text{SSW DSBL}}$, and $\overline{\text{ADDR DSBL}}$ are all at a logic 1 (> +2.4 volts) at S-100 bus pins 19, 18, 23, 53, and 22 respectively.

6.6.8 Verify that PSYNC at S-100 bus pin 76 is pulsing.

6.6.9 Verify that PDBIN at S-100 bus pin 78 is pulsing.

6.6.10 Verify that the vector jump enable signal at U22 pin 5 is at a logic 0.

6.6.11 Verify proper operation U2 pin 8, which enables data onto the CPU data bus from the on-board memories.

6.7 If you have trouble with the RUN/STOP, SINGLE-STEP, or $\overline{\text{PRDY}}$ circuit:

6.7.1 Set the RUN/STOP switch to the STOP position; then verify the following signals:

	Location	Logic State
a.	U5/pin 6	Logic Ø
b.	U5/pin 1	Logic 1
c.	U5/pin 4	Logic 1*
d.	U5/pin 9	Logic Ø
e.	U34/pin 6	Logic Ø
f.	U21/pin 6	Logic 1
g.	U21/pin 3	pulsing
h.	U20/pin 1	Logic Ø
i.	U34/pin 8	Logic Ø
j.	U32/pin 24	Logic Ø
k.	U20/pin 2	Logic Ø

*This pin should pulse negative once when the RUN/STOP switch is toggled to the STOP position.

6.7.2 Switch over and hold the SINGLE-STEP switch; then verify that U5 pin 9 is a logic 1.

6.7.3 Verify that the indicated signals occur each time the SINGLE-STEP switch is toggled:

	Location	Logic State
a.	U5/pin 4	Negative pulse
b.	U5/pin 6	Positive pulse
c.	U34/pin 6	Positive pulse
d.	U21/pin 6	Negative pulse
e.	U20/pin 1	Positive pulse
f.	U34/pin 8	Positive pulse
g.	U20/pin 2	Logic Ø (no pulse)

6.7.4 Set the RUN/STOP switch to the RUN position and verify that U5 pin 6 remains a logic Ø.

6.7.5 Toggle the SINGLE-STEP switch once and verify that U5 pin 6 changes to a logic 1.

6.8 If you have trouble with the vector jump circuit:

6.8.1 If vector jump is desired:

6.8.1.1 Verify that E16 to E17 is not connected.

6.8.1.2 Verify that E18 to E19 and/or E24 to E25 is connected.

6.8.1.3 Set the RUN/STOP switch to the STOP position and initiate the vector jump circuit with RESET or POWER-ON, depending on which option is selected. Then make the following logic tests:

	Location	Logic State
a.	U23/pin 8	Logic 1*
b.	U22/pin 3 & 11	Logic 1
c.	U22/pin 9	Logic Ø
d.	U22/pin 5	Logic 1
e.	U22/pin 12	Logic Ø
f.	U33/pin 1	Logic Ø
g.	U3/pin 8	Logic 1
h.	U29/pin 11	Logic 1*
i.	U2/pin 8	Logic Ø
j.	U18/pin 1 & 19	Logic Ø

	Location	Logic State
k.	U16/pin 20	Logic Ø
l.	U2/pin 6	Logic 1
m.	U19/pin 1 & 19	Logic 1

*These pins will pulse to logic Ø at the time of RESET and/or POWER-ON.

6.8.1.4 Verify that the desired vector jump code appears at DØ thru D7 on U18 pins 16, 14, 12, 9, 7, 5, 3, and 18 respectively. If it is a RESTART instruction, go to 6.8.1.7.

6.8.1.5 Toggle the SINGLE-STEP switch once and repeat the logic measurements of 6.8.1.3 thru 6.8.1.4, except that 6.8.1.3a will not pulse to logic Ø.

6.8.1.6 Repeat 6.8.1.5 until the entire vector jump code has been read into the CPU.

6.8.1.7 Toggle the SINGLE-STEP switch once and make the following logic tests:

	Location	Logic State
a.	U22/pin 1 & 13	Logic 1
b.	U22/pin 4 & 10	Logic 1
c.	U22/pin 5 & 9	Logic Ø
d.	U22/pin 3 & 11	Logic 1

6.8.1.8 Verify that the CPU (Z-80) is at the correct address by looking at the CPU address pins.

6.8.2 If vector jump is not desired:

6.8.2.1 Verify that E16 to E17 is connected.

6.8.2.2 Verify that E18 to E19 and/or E24 to E25 is not connected.

6.8.2.3 Set the RUN/STOP switch to the STOP position and apply power to the system, verifying a negative pulse on U22 pins 1 & 13. Then make the following logic tests:

	Location	Logic State
a.	U22/pin 5 & 19	Logic Ø
b.	U22/pin 1 & 13	Logic 1
c.	U22/pin 4 & 10	Logic 1
d.	U22/pin 2 & 12	Logic Ø

6.9 If you have trouble with the on-board memory:

6.9.1 Measure the memory (U16 & U17) Vcc voltage (+5.0 Vdc) at pin 24.

6.9.2 Check the addressing circuit as follows:

6.9.2.1 Disable the vector jump circuit by disconnecting E18 to E19 and E24 to E25 and connecting E16 to E17. Also, open switch SE positions 1 & 3 and close positions 2 & 4.

6.9.2.2 Set the RUN/STOP switch to the STOP position and power up the card.

6.9.2.3 With the memories removed and both address switches set to ØØH (open all positions except position 2), verify the following signals:

	Location	Logic State
a.	U9/pins 2,4,6,8, 10 & 12	Logic 1
b.	U3/pin 5	Logic 1
c.	U3/pin 2	Logic 1
d.	U14/pin 9	Logic Ø
e.	U14/pin 8	Logic 1
f.	U3/pin 6	Logic Ø
g.	U3/pin 3	Logic Ø
h.	U26/pin 2	Logic 1
i.	U33/pin 1	Logic Ø
j.	U3/pin 8	Logic 1
k.	U38/pin 8	Logic 1
l.	U16 & U17/pins 1 thru 8, 19,21, 22 & 22	Logic Ø

6.9.3 Check the data circuits as follows:

6.9.3.1 Perform 6.9.2.1 thru 6.9.2.2 and verify the following signals:

	Signal	Location	Logic State
a.	MADDR	U2/pin 10	Logic 1
b.	PDBIN	U2/pin 9	Logic 1
c.	$\overline{\text{SSW DSBL}}$	U2/pin 12	Logic 1
d.	DBUS CNTL	U2/pin 13	Logic 1
e.	$\overline{\text{MEMOE}}$	U2/pin 8	Logic Ø
f.	$\overline{\text{OE}}$	U16 & U17/pin 20	Logic Ø
g.	--	U18/pin 1 & 19	Logic Ø
h.	--	U2/pin 6	Logic 1

6.9.3.2 Remove power from the board, close switch SD position 1, set up switch SE for the type of memory used, insert a memory IC into U16, reapply power and verify the following signals:

	Location	Logic State
a.	U16/pin 18	Logic Ø
b.	U17/pin 18	Logic 1
c.	U16/pin 20	Logic Ø
d.	U18/pin 1 & 19	Logic Ø
e.	U19/pin 1 & 19	Logic 1
f.	U18/pin 16	= U18/pin 4
g.	U18/pin 14	= U18/pin 6
h.	U18/pin 12	= U18/pin 8
i.	U18/pin 9	= U18/pin 11
j.	U18/pin 7	= U18/pin 13
k.	U18/pin 5	= U18/pin 15
l.	U18/pin 3	= U18/pin 17
m.	U18/pin 18	= U18/pin 2

6.9.3.3 Repeat 6.9.3.2, except close switch SC position 1, open switch SD position 1, insert the memory IC into the U17 position, and verify the following signals:

	Location	Logic State
a.	U16/pin 18	Logic 1
b.	U17/pin 18	Logic Ø
c. thru m.	Same as 6.9.3.2 c. thru m.	

6.9.4 If RAM memory is being used, then check the memory write function as follows:

6.9.4.1 Check the MWRITE option at E35 & E36.

6.9.4.2 Perform 6.9.2.1.

6.9.4.3 Remove any memory IC's from U16 & U17 and remove IC U18.

6.9.4.4 Perform 6.9.2.2.

6.9.4.5 Verify a logic 1 on all data lines at U32 pins 7, 8, 9, 10, 12, 13, 14, and 15 (this is a RST 7 instruction).

6.9.4.6 Verify a logic Ø at U32 pin 27.

6.9.4.7 SINGLE-STEP the CPU once and check the following signals:

	Location	Logic State
a.	U2/pin 9	Logic Ø
b.	U2/pin 8	Logic 1
c.	U2/pin 6	Logic Ø
d.	U19/pin 1 & 19	Logic Ø
e.	U19/pin 16	= U19/pin 4
f.	U19/pin 14	= U19/pin 6
g.	U19/pin 12	= U19/pin 8
h.	U19/pin 9	= U19/pin 11
i.	U19/pin 7	= U19/pin 13
j.	U19/pin 5	= U19/pin 15
k.	U19/pin 3	= U19/pin 17
l.	U19/pin 18	= U19/pin 2
m.	U1/pin 8	Logic Ø

6.10 <u>If you have trouble with the extended address/output port</u>:

6.10.1 Execute the following program:

```
100:  3E 00          MVI  A, ØØH
102:  D3 FE    LOOP: OUT  ØFEH
104:  C3 02 01       JMP  LOOP
```

6.10.2 Set the RUN/STOP switch to the STOP position.

6.10.3 While observing the $\overline{\text{IORQ}}$ (U32 pin 20), SINGLE-STEP the CPU until $\overline{\text{IORQ}}$ goes to logic Ø.

6.10.4 Verify the following signals:

	Signal	Location	Logic State
a.	AØ	U46/pin 3	Logic 1
b.	A1	U46/pin 6	Logic 1
c.	A2	U46/pin 4	Logic 1
d.	A3	U46/pin 12	Logic 1
e.	A4	U46/pin 5	Logic 1
f.	A5	U46/pin 11	Logic 1
g.	A6	U46/pin 2	Logic 1
h.	A7	U46/pin 1	Logic 1
i.	$\overline{\text{PORT ENABLE}}$	U46/pin 8	Logic Ø
j.	IORQ	U36 & U40/pin 9	Logic Ø
k.	RESET	U36 & U40/pin 15	Logic Ø
l.	$\overline{\text{WR}}$	U36 & U40/pin 7	Logic Ø
m.	ADDR DSBL	U36 & U40/pin 1	Logic Ø
n.	--	U36 & U40/pin 2	Logic Ø
o.	DØ	U36/pin 12	Logic Ø
p.	D1	U36/pin 13	Logic Ø
q.	D2	U36/pin 11	Logic Ø
r.	D3	U36/pin 14	Logic Ø
s.	D4	U40/pin 14	Logic Ø
t.	D5	U40/pin 13	Logic Ø
u.	D6	U40/pin 12	Logic Ø
v.	D7	U40/pin 11	Logic Ø
w.	OUT Ø	U36/pin 5	Logic Ø
x.	OUT 1	U36/pin 4	Logic Ø
y.	OUT 2	U36/pin 6	Logic Ø
z.	OUT 3	U36/pin 3	Logic Ø
$\overline{\text{A}}$	OUT 4	U40/pin 3	Logic Ø
$\overline{\text{B}}$	OUT 5	U40/pin 4	Logic Ø
$\overline{\text{C}}$	OUT 6	U40/pin 5	Logic Ø
$\overline{\text{D}}$	OUT 7	U40/pin 6	Logic Ø

6.10.5 Execute the following program:

```
100:  3E FF              MVI  A, ØFF H
102:  D3 FE        LOOP: OUT  ØFEH
104:  C3 02 01           JMP  LOOP
```

6.10.6 Repeat 6.10.2 thru 6.10.4, except 6.10.4 o. thru $\overline{D}$ will be a logic 1.

6.10.7 SINGLE-STEP once and verify U36 & U40 pins 9 & 7 are a logic 1.

6.11 If you have trouble with I/O operations:

6.11.1 Check that the I/O ADDR jumper option is correct for your system (see 4.1.5).

6.11.1.1 If your I/O boards require the I/O address on the high address lines (A8-A15), then jumper E22 to E23 should be connected.

6.11.1.2 If your I/O boards only use the low 8 bits of the address bus, then jumper E22 to E23 is not needed.

6.11.2 Execute a short program as shown in the following example:

```
100:  DB XX            LOOP:  IN  PORT   XX=port number
102:  C3 00 01                JMP LOOP
```

where PORT is any I/O port. Then STOP the CPU with the RUN/STOP switch.

6.11.2.1 SINGLE-STEP the CPU with the SINGLE-STEP switch while observing the SINP (S-100 bus pin 46) and stop when it is high.

6.11.2.2 Verify that the following signals are correct:

	Signal	Location	Logic State
a.	PDBIN	S-100/pin 78	Logic 1
b.	IORQ	U25/pin 5	Logic Ø
c.	SINP	S-100/pin 46	Logic 1
d.	$\overline{\text{I/O ADDR CNTL}}$	U23/pin 2	Logic Ø*
e.	$\overline{\text{HADDR EN}}$	U48 pin 1 & 19	Logic 1*
f.	$\overline{\text{I/O ADDR EN}}$	U47/pin 1 & 19	Logic Ø*

* Verify these signals only if the I/O jumper option is connected.

6.11.2.3 Toggle the SINGLE-STEP switch once and verify that the following signals are correct:

	Signal	Location	Logic State
a.	PDBIN	S-100/pin 78	Logic 1
b.	$\overline{\text{IORQ}}$	U25/pin 5	Logic 1
c.	SINP	S-100/pin 46	Logic Ø
d.	$\overline{\text{I/O ADDR CNTL}}$	U23/pin 2	Logic 1
e.	$\overline{\text{HADDR EN}}$	U48/pin 1 & 19	Logic Ø
f.	$\overline{\text{I/O ADDR EN}}$	U47/pin 1 & 19	Logic 1
g.	$\overline{\text{M1}}$	U25/pin 3	Logic Ø

6.11.2.4 Change the program as follows:

```
102:  D3 XX        LOOP:  OUT  PORT   XX=port number
104:  C3 02 01            JMP  LOOP
```

and repeat steps 6.11.2.1 thru 6.11.2.3, except steps a & c should be as follows:

	Signal	Location	Logic State
a.	$\overline{\text{PWR}}$	S-100/pin 77	Logic Ø/1
c.	SOUT	S-100/pin 45	Logic 1/Ø

for 6.11.2.2 and 6.11.2.3 respectively.

6.12 If you have trouble with the PWAIT status:

6.12.1 Stop the CPU by setting the RUN/STOP switch to the STOP position.

6.12.2 Make the following logic tests:

	Location	Logic State
a.	U32/pin 26	Logic Ø
b.	U35/pin 2	Logic Ø
c.	U39/pin 2	Logic Ø
d.	U39/pin 13	pulsing
e.	U35/pin 1 & 13	Logic 1
f.	U35/pin 4	Logic 1
g.	U39/pin 6	Logic Ø
h.	U35/pin 8	Logic Ø
i.	U39 pin 5	Logic Ø
j.	U35/pin 5	Logic Ø
k.	U39/pin 3	Logic Ø
l.	U39/pin 1	Logic 1

	Location	Logic State
m.	U35/pin 10	Logic 1
n.	U43/pin 1 & 15	Logic Ø
o.	U24/pin 8	Logic Ø
p.	U24/pin 9	Logic 1
q.	U43/pin 4	Logic Ø
r.	U43/pin 5	Logic 1

6.12.3 Verify that the following signals occur when the SINGLE-STEP switch is toggled:

	Location	Logic State
a.	U32/pin 24	Positive pulse
b.	U35/pin 2	Positive pulse
c.	U39/pin 2	Positive pulse
d.	U35/pin 1 & 13	Logic 1 (no pulse)
e.	U35/pin 4	Negative pulse
f.	U39/pin 6	Positive pulse
g.	U35/pin 8	Positive pulse
h.	U39/pin 5	Positive pulse
i.	U35/pin 5	Positive pulse
j.	U39/pin 3	Positive pulse
k.	U39/pin 1	Negative pulse
l.	U35/pin 10	Negative pulse
m.	U43/pin 1 & 15	Logic Ø (no pulse)
n.	U43/pin 4	Positive pulse
o.	U43/pin 5	Negative pulse

6.13 If you have any trouble with phase one (Ø1) or $\overline{\text{STVAL}}$ at the S-100 bus pin 25, check the following items:

6.13.1 Verify that the Ø1/$\overline{\text{STVAL}}$ option has been properly connected. Only one of the two options may be used at any one time.

6.13.2 If the option is strapped for Ø1 operation, verify the following logic conditions:

	Location	Logic Condition
a.	U6/pin 5	Pulsing continuously
b.	U12/pin 8	Pulsing continuously
c.	U7/pin 5	Pulsing continuously
d.	U12/pin 5	Pulsing at ½ the U6 pin 5 frequency
e.	U7/pin 4	Same as (d) above
f.	U7/pin 6	Negative pulses
g.	U11/pin 2	Negative pulses
h.	U11/pin 3	Positive pulses
i.	U11/pin 1	Positive pulses (Ø1)
j.	U11/pin 8	Negative pulses
k.	U11/pin 9	Negative pulses
l.	U42/pin 6	Positive pulses (Ø1)
m.	U42/pin 7	Positive pulses (Ø1)
n.	U42/pin 1 & 15	Logic Ø

Also, verify +5Vdc on each of the above IC's power input pin, and ground continuity for each IC's ground return pin.

6.13.3 If the option is strapped for $\overline{\text{STVAL}}$, verify the following logic conditions:

	Location	Logic Condition
a.	U10/pin 2	Positive pulses (PSYNC)
b.	U10/pin 3	Positive pulses (Ø1)
c.	U10/pin 1 & 4	Logic 1
d.	U10/pin 5	Positive pulses (STVAL)
e.	U43/pin 10	Positive pulses ($\overline{\text{STVAL}}$)
f.	U43/pin 9	Negative pulses ($\overline{\text{STVAL}}$)
g.	U43/pin 1 & 15	Logic Ø (C/C DSBL)

Also, verify +5Vdc on each of the above IC's power input pin and ground continuity for each IC's ground return pin.

6.14 If you have trouble with phase two (Ø2), verify the following logic conditions:

	Location	Logic Conditions
a.	U11/pin 6	Logic Ø
b.	U11/pin 5	2/4 MHz clock (50% duty cycle)
c.	U11/pin 4*	2/4 MHz clock (50% duty cycle)
d.	U7/pin 2	2/4 MHz clock
e.	U7/pin 1	Negative pulses

	Location	Logic Condition
f.	U7/pin 3	Pulsing
g.	U29/pin 1 & 2	Positive pulses
h.	U29/pin 3	Negative pulses
i.	U28/pin 1Ø	Negative pulses
j.	U28/pin 13	Logic 1
k.	U28/pin 11	Pulsing
l.	U28/pin 12	Negative pulses
m.	U28/pin 9	Negative pulses
n.	U20/pin 9	Pulsing
o.	U20/pin 8	Positive pulses
p.	U20/pin 1Ø	Pulsing
q.	U42/pin 4	Pulsing
r.	U42/pin 5	Pulsing
s.	U42/pin 1 & 15	Logic Ø

Also, verify +5Vdc on each of the above IC's power input pin and ground continuity for each IC's ground return pin.

CB2 MANUAL REGISTRATION FORM

In our effort to continually upgrade our documentation, we would appreciate any feedback that you may have concerning this manual. Please mail your comments and suggestions to SSM Customer Service at the address below.

COMMENTS & CORRECTIONS ON SSM CB2 INSTRUCTION MANUAL

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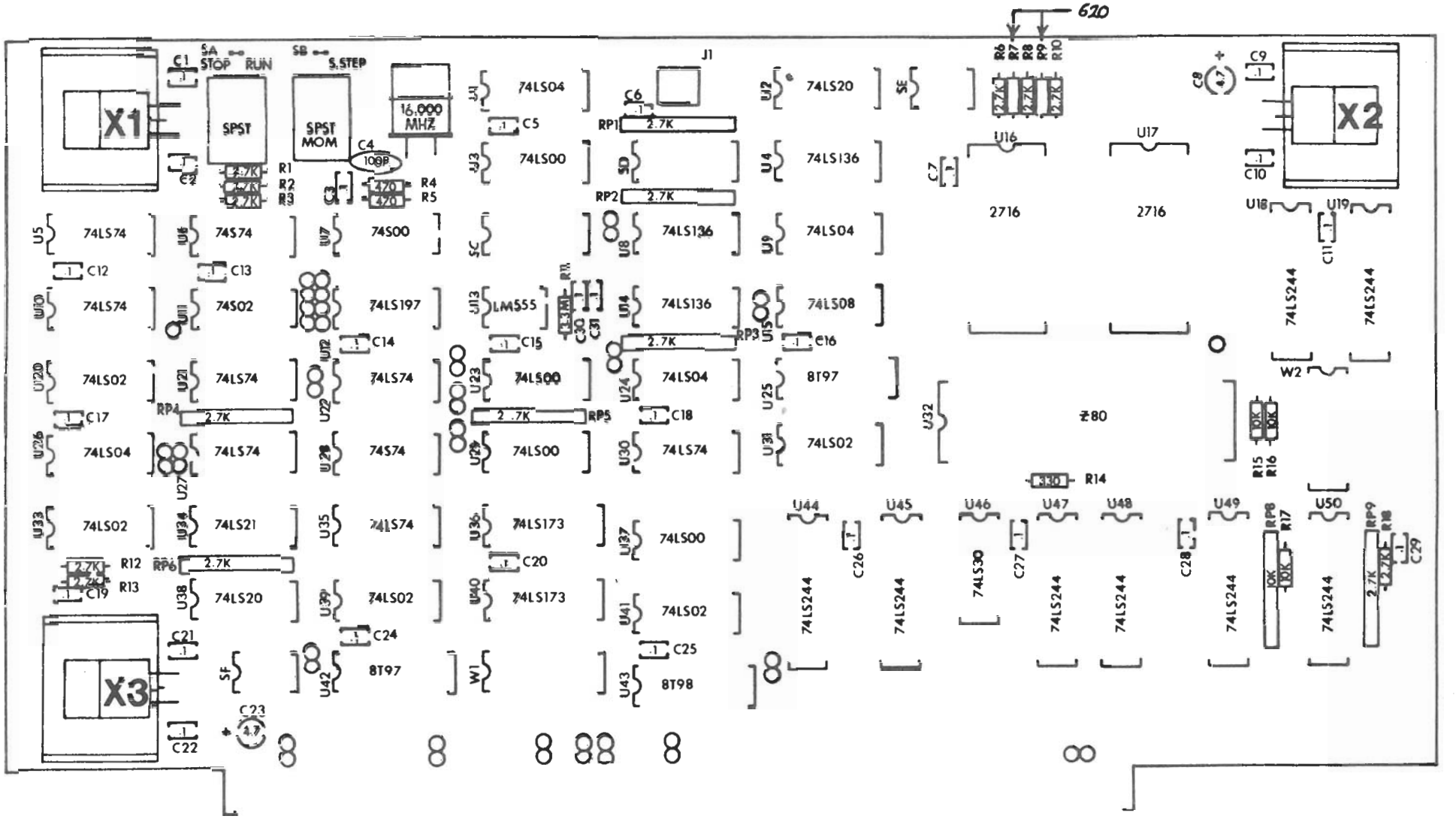

ASSEMBLY DRAWING

SILKSCREEN / LAYER A&B&D
CB2
REV 4

CB2
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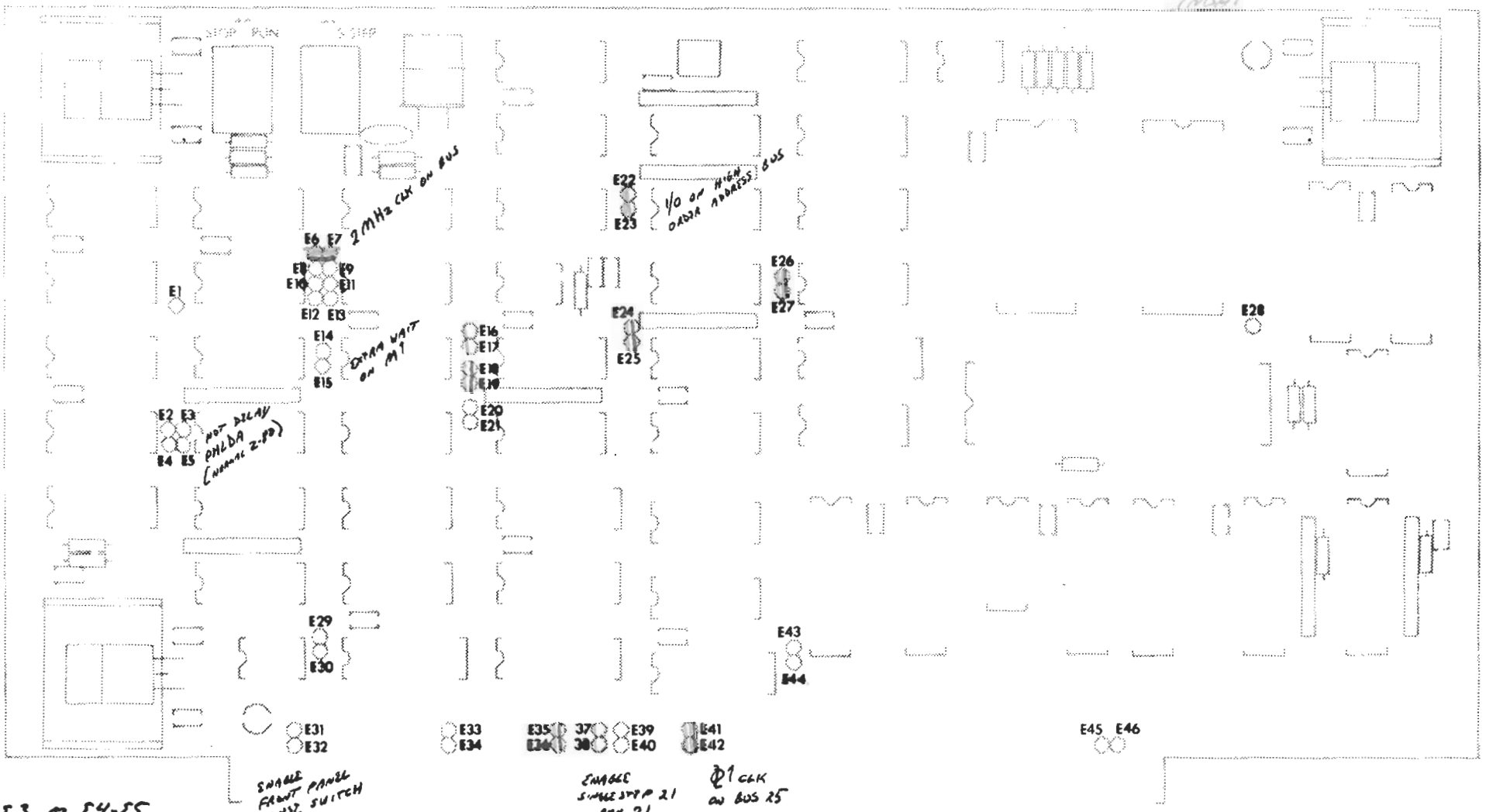

SSM

E2-E3 or E4-E5
E6-E7
E18-E19
E35-E36
E41-42
E24-25
E26-27
E28-29 + E30-BUS

JUMPER DRAWING

CB2

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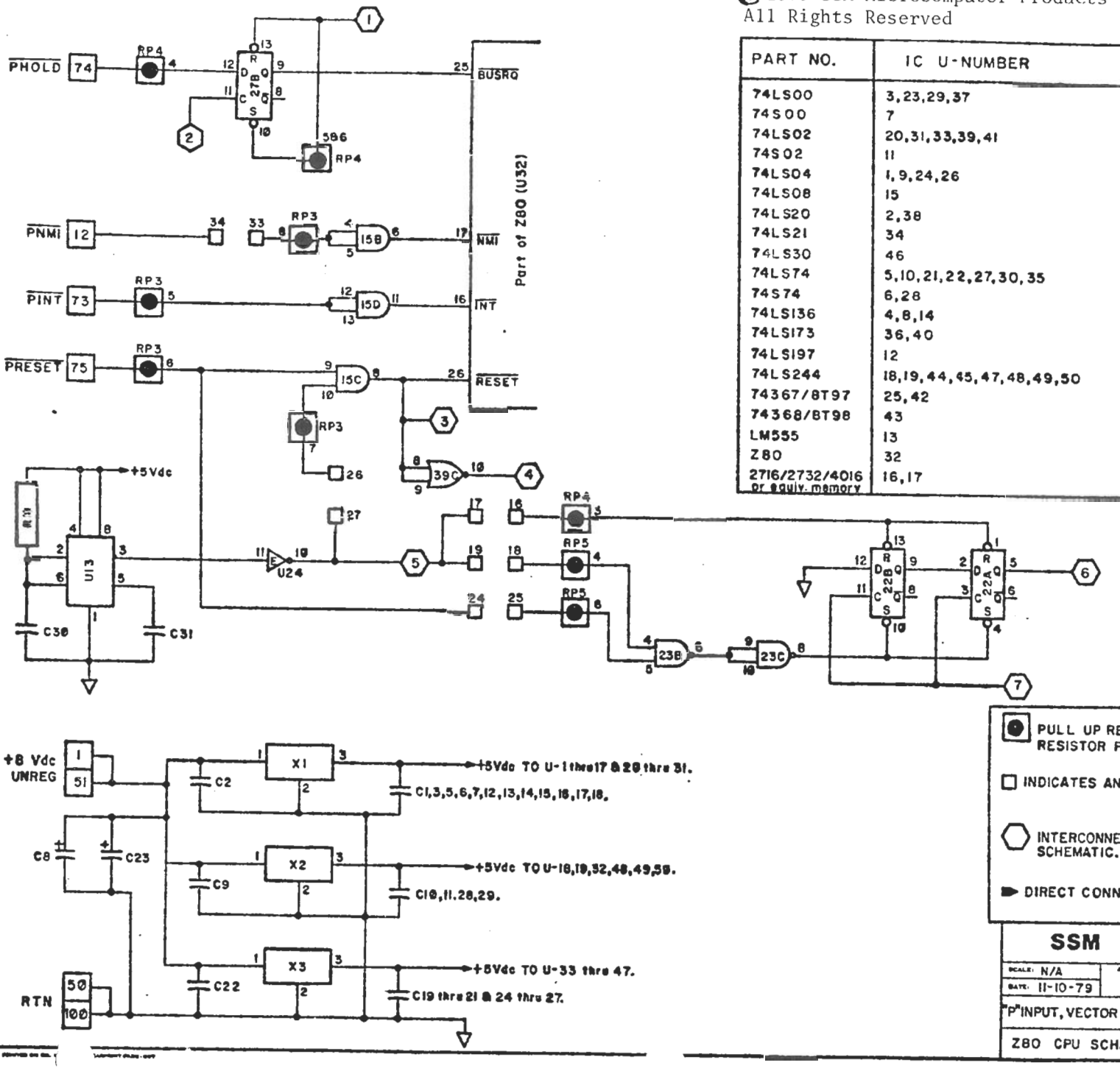
CB2 SCHEMATIC INTERPAGE CONNECTION LIST

	Schematic Page					Function Name
	1	2	3	4	5	
1	S	D	D	-	-	Logic 1 (pull up resistor to Vcc)
2	D	S	-	-	-	Ø2
3	S	-	D	-	-	$\overline{\text{RESET}}$
4	S	-	-	-	D	RESET
5	S	D	-	-	-	$\overline{\text{POC}}$
6	S	-	-	D	-	Vector Jump Enable
7	D	D	S	-	-	M1
8	-	S	D	-	-	Z80-Ø (Z80 Clock)
9	-	D	S	-	-	$\overline{\text{PSYNC}}$
10	-	D	S	-	-	$\overline{\text{IORQ}}$ + $\overline{\text{MREQ}}$
11	-	S	D	-	-	2/4 MHz Control
12	-	D	S	-	-	MWRITE to on-board memory
13	-	S	-	D	-	MWRITE S100
14	-	D	S	-	-	RUN
15	-	S	D	-	-	$\overline{\text{Ø2 CONTROL}}$
16	-	D	-	S	D	MADDR (high = on board memory enabled)
17	-	D	S	-	-	PSYNC
18	-	S	D	-	-	$\overline{\text{Ø2}}$
19	-	S	D	-	-	$\overline{\text{PWAIT}}$
20	-	-	S	D	-	$\overline{\text{MREQ}}$
21	-	-	S	D	D	$\overline{\text{IORQ}}$
22	-	-	S	-	D	$\overline{\text{WR}}$
23	-	-	S	-	D	PDBIN
24	-	-	S	-	D	DATA-IN Control
25	-	-	-	S	D	U16 PIN 21 (Memory A variable func)
26	-	-	-	S	D	U17 PIN 21 (Memory B variable func)
27	-	-	-	S	D	AØ thru A1Ø for on board memory
28	-	-	-	S	D	ADDR DSBL
29	-	-	-	S	D	PORT FE ADDRESS DECODED
30	-	-	-	S	D	Memory B chip Select ($\overline{\text{CS}}$)
31	-	-	-	S	D	Memory A chip Select ($\overline{\text{CS}}$)

-: No connection.

S: Indicates which page the signal originates on.

D: Indicates which page(s) the signal goes to.



PART NO.	IC U-NUMBER	Vcc Pin No.	RTN Pin No.
74LS00	3,23,29,37	14	7
74S00	7	14	7
74LS02	20,31,33,39,41	14	7
74S02	11	14	7
74LS04	1,9,24,26	14	7
74LS08	15	14	7
74LS20	2,38	14	7
74LS21	34	14	7
74LS30	46	14	7
74LS74	5,10,21,22,27,30,35	14	7
74S74	6,28	14	7
74LS136	4,8,14	14	7
74LS173	36,40	16	8
74LS197	12	14	7
74LS244	18,19,44,45,47,48,49,50	20	10
74367/8T97	25,42	16	8
74368/8T98	43	16	8
LM555	13	4,8	1
Z80	32	11	29
2716/2732/4016 or equiv. memory	16,17	24	12

PULL UP RESISTOR, MAY BE PART OF A SIP RESISTOR PACK (RP).

INDICATES AN OPTION (E) PAD ON THE CPU BOARD

INTERCONNECT BETWEEN PAGES OF THIS SCHEMATIC.

DIRECT CONNECTION TO A Z80 PIN.

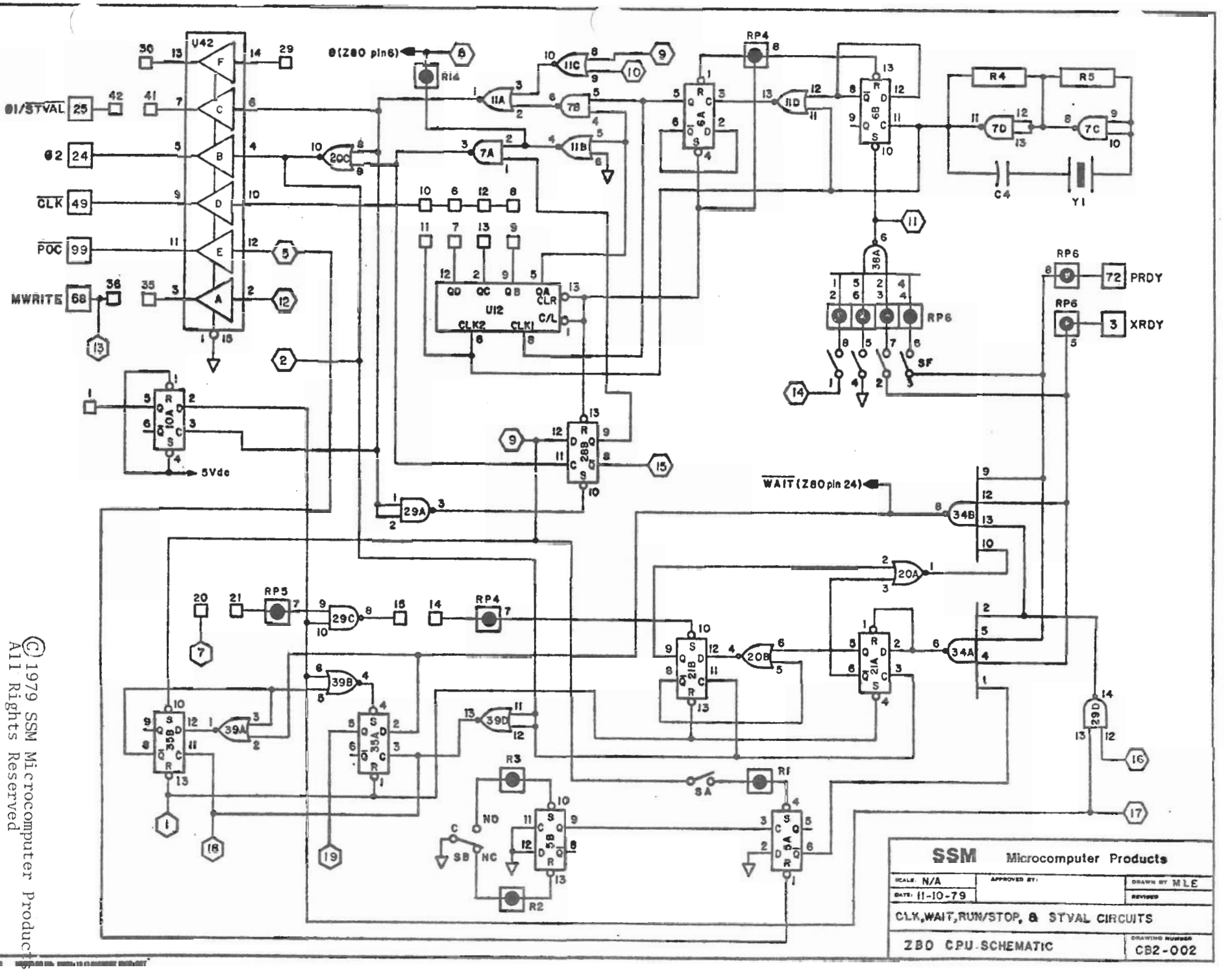
SSM Microcomputer Products

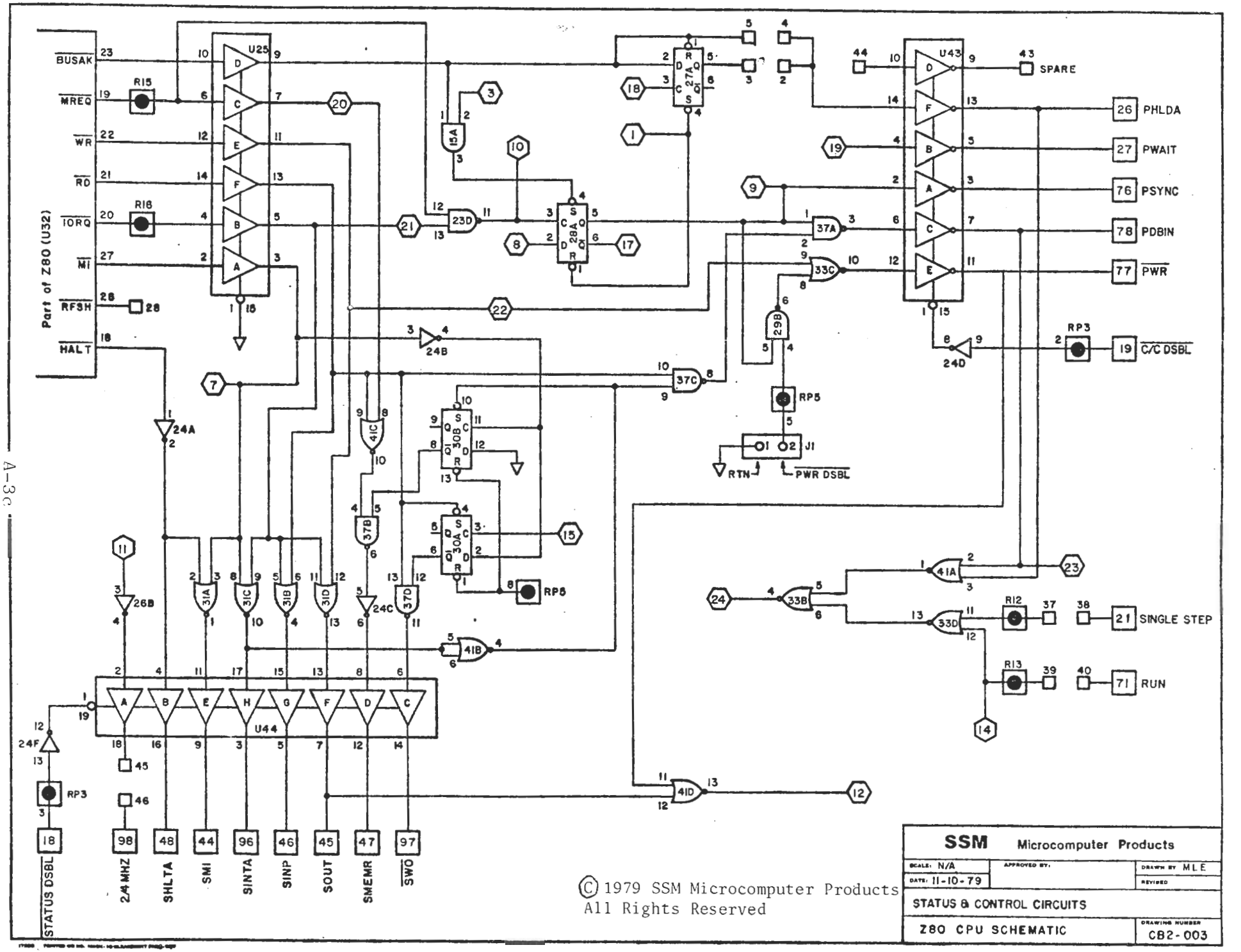
SCALE: N/A	APPROVED BY:	DRAWN BY MLE
DATE: 11-10-79		REVISED

"P" INPUT, VECTOR JUMP, & POWER SUPPLY CIRCUITS

Z80 CPU SCHEMATIC

DRAWING NUMBER CB2-001



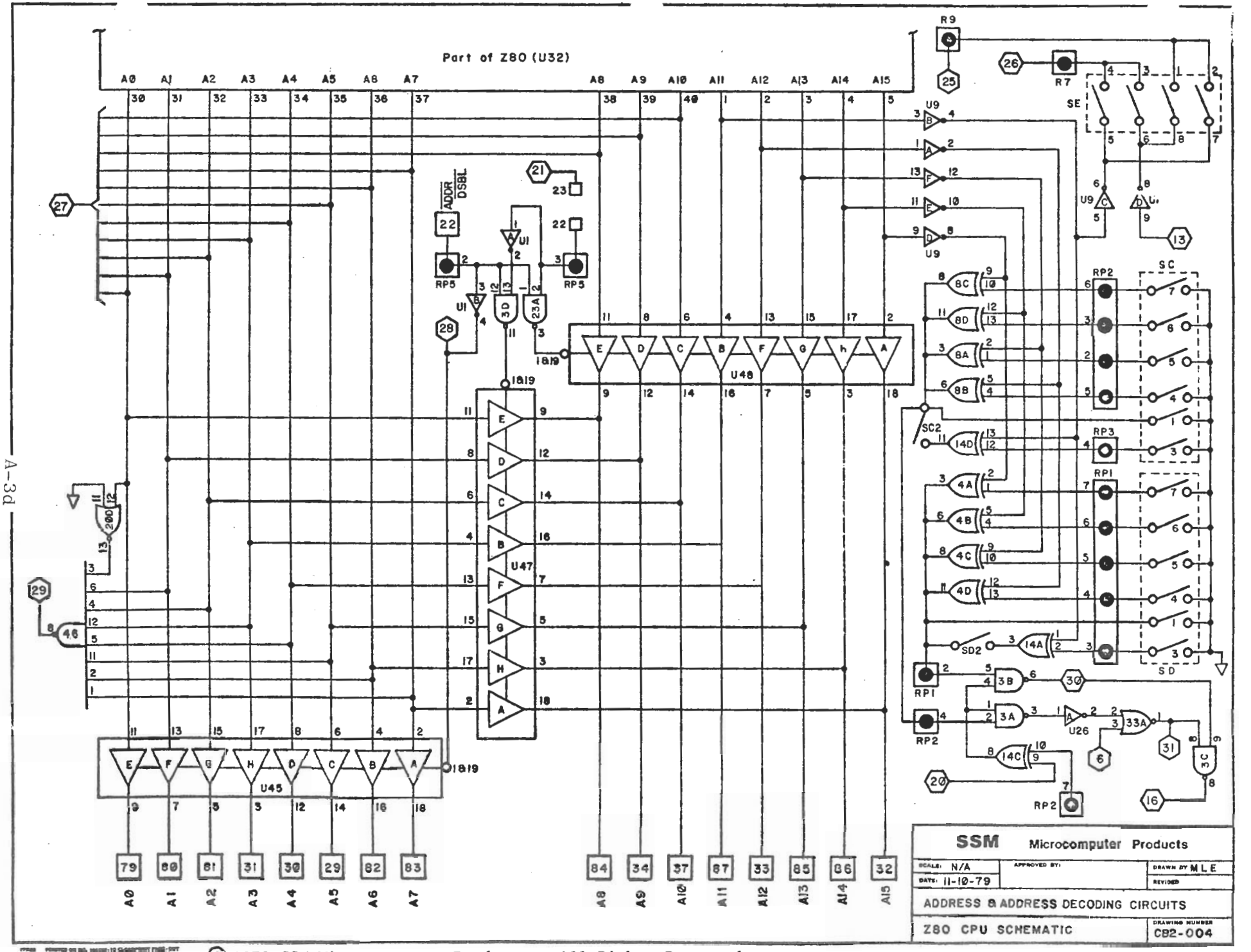


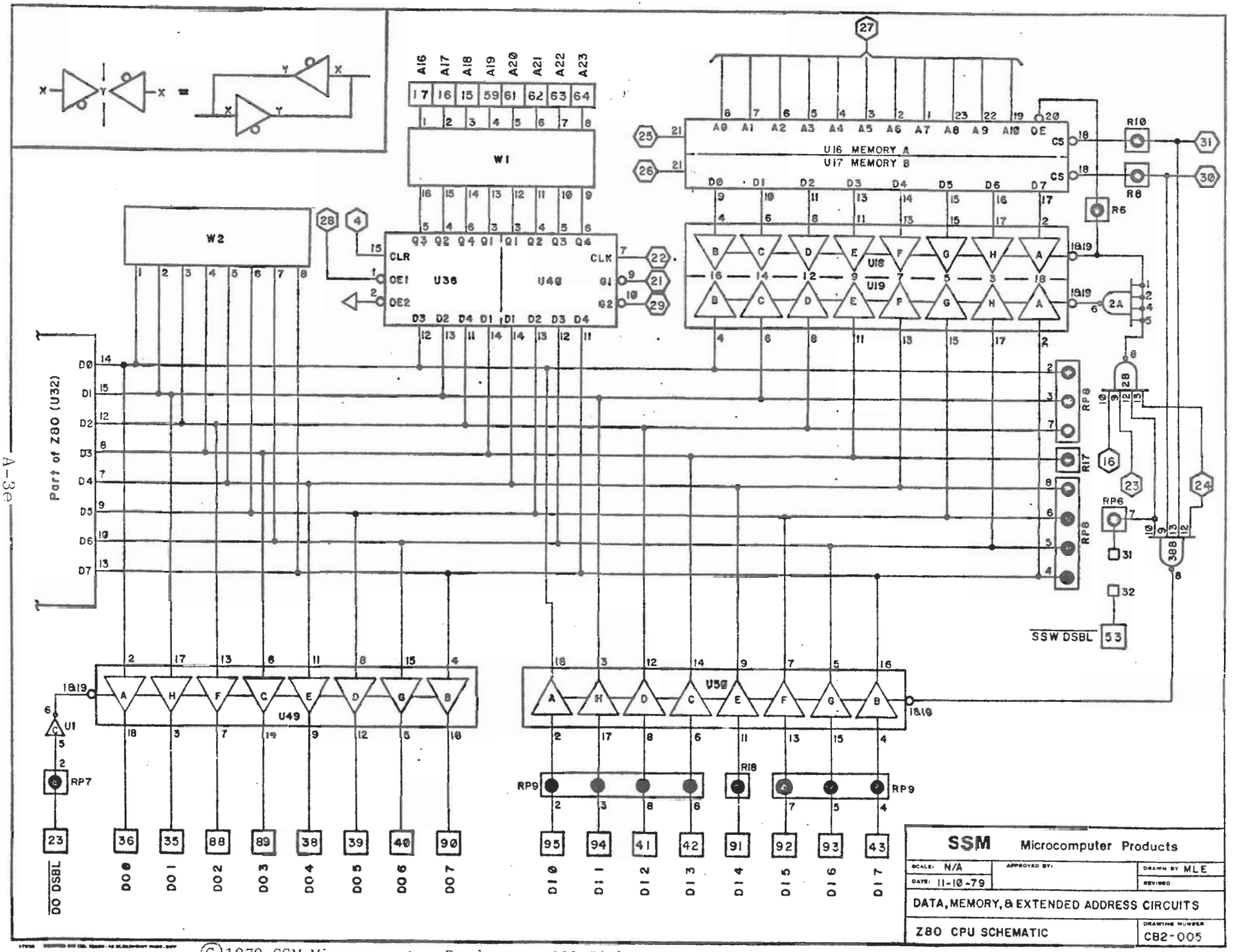
SSM Microcomputer Products

SCALE: N/A	APPROVED BY:	DRAWN BY MLE
DATE: 11-10-79		REVISED

STATUS & CONTROL CIRCUITS

Z80 CPU SCHEMATIC — DRAWING NUMBER CB2-003





CB2 BUS PIN DEFINITIONS
and
CROSS REFERENCE TABLE

BUS PIN	SIGNAL	REFERENCED IN SECTION(S)	BUS PIN	SIGNAL	REFERENCED IN SECTION(S)
1	+8V Unreg.		26	PHLDA	4.1.1, 5.1.5
2			27	PWAIT	5.1.4
3	XRDY	5.4.1, 5.4.1.1	28		
4			29	A5	5.5
5			30	A4	5.5
6			31	A3	5.5
7			32	A15	5.5
8			33	A12	5.5
9			34	A9	5.5
10			35	DO 1	5.6
11			36	DO Ø	5.6
12	$\overline{\text{PNMI}}$ *	4.1.10, 5.4.3	37	A1Ø	5.5
13			38	DO 4	5.6
14			39	DO 5	5.6
15	A18 *	4.4, 5.7	40	DO 6	5.6
16	A17 *	4.4, 5.7	41	DI 2	5.6
17	A16 *	4.4, 5.7	42	DI 3	5.6
18	$\overline{\text{STATUS DSBL}}$	5.4.6	43	DI 7	5.6
19	$\overline{\text{C/L DSBL}}$	5.4.6	44	SM1	5.3.5
20			45	SOUT	5.3.2
21	Single Step	4.1.12, 5.4.1.4, 5.4.5	46	SINP	5.3.1
22	$\overline{\text{ADDR DSBL}}$	5.4.6	47	SMEMR	5.3.6
23	$\overline{\text{DO DSBL}}$	5.4.6	48	SHLTA	5.3.4
24	Ø2	5.2, 5.2.2, 5.2.3 5.2.4	49	$\overline{\text{CLK}}$	4.1.2, 5.2, 5.2.5
25	Ø1/$\overline{\text{STVAL}}$ **	4.1.15, 5.1.6, 5.2, 5.2.2, 5.2.3, 5.2.4	50	Ground	

BUS PIN	SIGNAL	REFERENCED IN SECTION(S)	BUS PIN	SIGNAL	REFERENCED IN SECTION(S)
51	+8V Unreg.		76	PSYNC	5.1.1
52			77	$\overline{\text{PWR}}$	5.1.3
53	$\overline{\text{SSW DSBL}}$ *	4.1.9, 5.4.5	78	PDBIN	5.1.2
54			79	AØ	5.5
55			80	A1	5.5
56			81	A2	5.5
57			82	A6	5.5
58			83	A7	5.5
59	A19	4.4, 5.7	84	A8	5.5
60			85	A13	5.5
61	A2Ø	4.4, 5.7	86	A14	5.5
62	A21	4.4, 5.7	87	A11	5.5
63	A22	4.4, 5.7	88	DO 2	5.6
64	A23	4.4, 5.7	89	DO 3	5.6
65			90	DO 7	5.6
66			91	DI 4	5.6
67			92	DI 5	5.6
68	MWRITE *	4.1.11	93	DI 6	5.6
69			94	DI 1	5.6
70			95	DI Ø	5.6
71	RUN *	4.1.12, 5.4.1.4, 5.4.5	96	SINTA	5.3.3
			97	$\overline{\text{SWO}}$	5.3.7
72	PRDY	5.4.1, 5.4.1.1	98	2/4 MHz indicator	4.1.14, 5.3.8
73	$\overline{\text{PINT}}$	5.4.3			
74	$\overline{\text{PHOLD}}$	5.4.2	99	$\overline{\text{POC}}$	4.1.6, 5.4.4
75	$\overline{\text{PRESET}}$	5.4.4	100	Ground	

* Optional
**Either Ø1 or $\overline{\text{STVAL}}$ may be selected

CB2 PARTS LIST

Chip Pack

1 - U7	74S00
4 - U3,23,29,37	74LS00
1 - U11	74S02
5 - U20,31,33,39,41	74LS02
4 - U1,9,24,26	74LS04
1 - U15	74LS08
2 - U2,38	74LS20
1 - U34	74LS21
1 - U46	74LS30
2 - U6,28	74S74
7 - U5,10,21,22,27,30,35	74LS74
3 - U4,8,14	74LS136
2 - U36,40	74LS173
1 - U12	74LS197
8 - U18,19,44,45,47-50	74LS244
2 - U25,42	74367/8T97
1 - U43	74368/8T98
1 - U13	LM555
1 - U32	Z80/780C/MK3880

Socket Pack

2 - SD,SC	7 position Dip switch
2 - SE,SF	4 position Dip switch
1 - SA	DPST switch
1 - SB	DPST(M) Momentary switch
1	8 pin sockets
3	14 pin sockets
7	16 pin sockets
8	20 pin sockets
2	24 pin sockets
1	40 pin sockets

Capacitor Pack

1 - C4	100 pf ceramic disk
28 - C1-3,5-7,9-22,24-31	.1 uf mono.
2 - C8,23	4.7 uf Dip tantalum

Resistor Pack

1 - R14	330 ohm ¼W (Orange, Orange, Brown)
2 - R4,5	470 ohm ¼W (Yellow, Violet, Brown)
9 - R1-3,6,8,10,12,13,18	2.7K ohm ¼W (Red, Violet, Red)
2 - R7,9	620 ohm ¼W (Blue, Red, Brown)
3 - R15-17	10K ohm ¼W (Brown, Black, Orange)
1 - R11	3.3M ohm ¼W (Orange, Orange, Green)
7 - RP1-6,9	2.7K ohm Single In-Line Package (SIP)
1 - RP8	10K ohm SIP

Regulator/Hardware Pack

1 - Y1	16 MHZ Crystal
3 - X1,2,3	7805/340T-5
3	Heatsinks
3	Sets #6 Hardware
1	2 pin molex (male)
46 (Minimum)	Header pins (0.1 inch spacing)

Miscellaneous

1	PC Board
30	14 pin sockets
1	Instruction manual

Product Specification

Z-80® CPU
Z-80A CPU

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

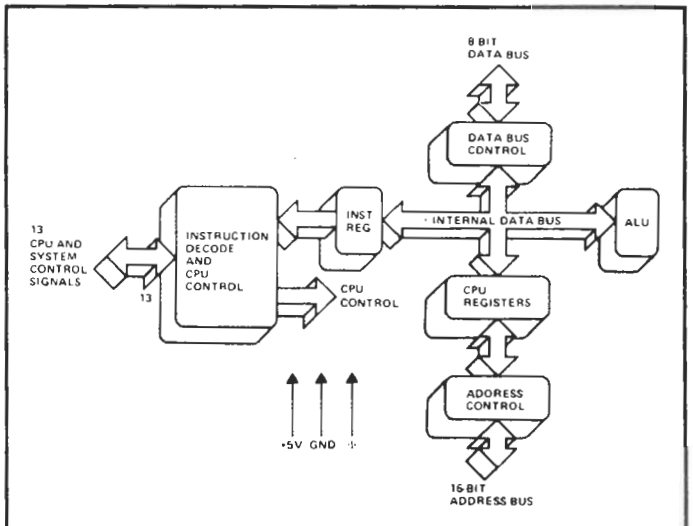
The Z80 and Z80A CPU's are third generation single chip microprocessors with unrivaled computational power. This increased computational power results in higher system through-put and more efficient memory utilization when compared to second generation microprocessors. In addition, the Z80 and Z80A CPU's are very easy to implement into a system because of their single voltage requirement plus all output signals are fully decoded and timed to control standard memory or peripheral circuits. The circuit is implemented using an N-channel, ion implanted, silicon gate MOS process.

Figure 1 is a block diagram of the CPU, Figure 2 details the internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

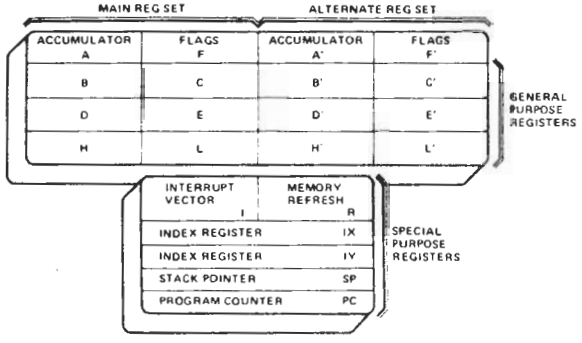
The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to a interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

FEATURES

- Single chip, N-channel Silicon Gate CPU.
- 158 instructions—includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations with more useful addressing modes such as indexed, bit and relative.
- 17 internal registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces standard speed static or dynamic memories with virtually no external logic.
- 1.0 μs instruction execution speed.
- Single 5 VDC supply and single-phase 5 volt Clock.
- Out-performs any other single chip microcomputer in 4-, 8-, or 16-bit applications.
- All pins TTL Compatible
- Built-in dynamic RAM refresh circuitry.

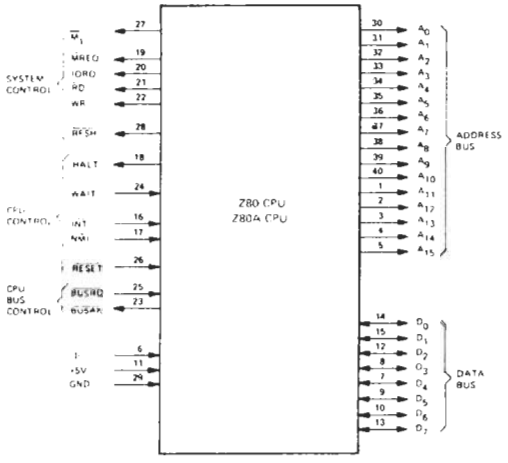


Z80, Z80A CPU BLOCK DIAGRAM



Z80, Z80A CPU REGISTERS

Z-80, Z-80A CPU Pin Description



Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus) — Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.

D_0-D_7 (Data Bus) — Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$ (Machine Cycle one) — Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.

$\overline{MREQ}$ (Memory Request) — Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/ Output Request) — Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

$\overline{RD}$ (Memory Read) — Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write) — Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh) — Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state) — Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$ (Wait) — Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

$\overline{INT}$ (Interrupt Request) — Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.

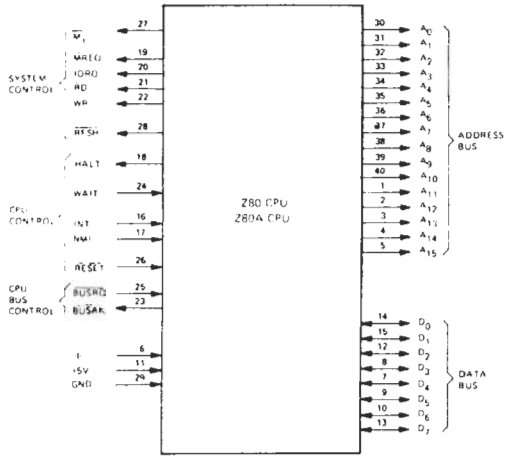
$\overline{NMI}$ (Non Maskable Interrupt) — Input, active low. The non-maskable nterrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H.

$\overline{RESET}$ — Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

$\overline{BUSRQ}$ (Bus Request) — Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge) — Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Z-80, Z-80A CPU Pin Description



Z80, Z80A CPU PIN CONFIGURATION

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$\overline{RFSH}$ (Refresh) Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state) Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

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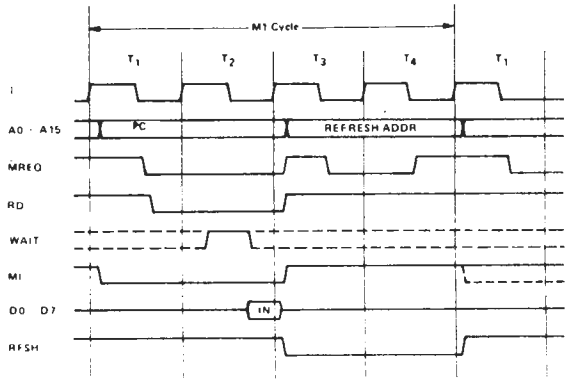
$\overline{BUSRQ}$ (Bus Request) Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge) Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Timing Waveforms

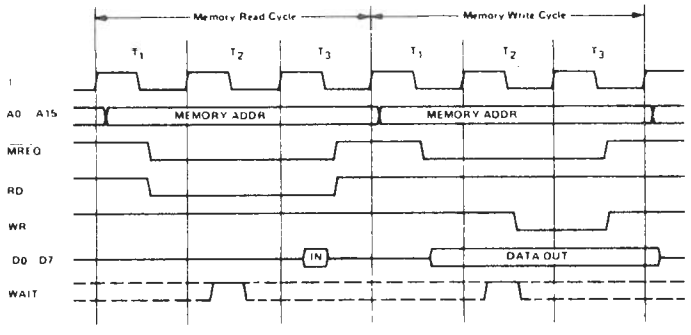
INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later $\overline{MREQ}$ goes active. The falling edge of $\overline{MREQ}$ can be used directly as a chip enable to dynamic memories. $\overline{RD}$ when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal $\overline{RFSH}$ indicates that a refresh read of all dynamic memories should be accomplished.



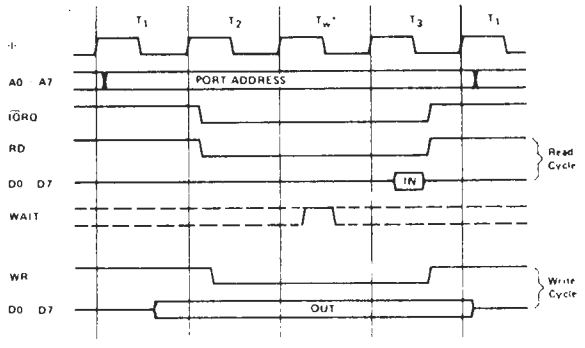
MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M_1 cycle). The $\overline{MREQ}$ and $\overline{RD}$ signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the $\overline{MREQ}$ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The $\overline{WR}$ line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.



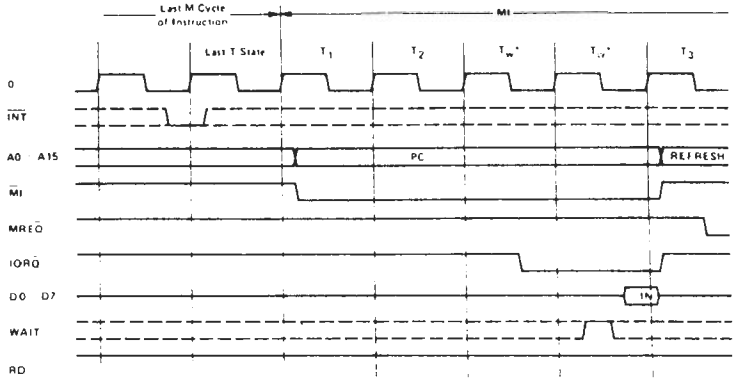
INPUT OR OUTPUT CYCLES

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required.



INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M_1 cycle is generated. During this M_1 cycle, the $\overline{IORQ}$ signal becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented.



Instruction Set

The following is a summary of the Z80, Z80A instruction set showing the assembly language mnemonic and the symbolic operation performed by the instruction. A more detailed listing appears in the Z80-CPU technical manual, and assembly language programming manual. The instructions are divided into the following categories:

- 8-bit loads
- 16-bit loads
- Exchanges
- Memory Block Moves
- Memory Block Searches
- 8-bit arithmetic and logic
- 16-bit arithmetic
- General purpose Accumulator & Flag Operations
- Miscellaneous Group
- Rotates and Shifts
- Bit Set, Reset and Test
- Input and Output
- Jumps
- Calls
- Restarts
- Returns

In the table the following terminology is used.

- b ≡ a bit number in any 8-bit register or memory location
- cc ≡ flag condition code
  - NZ ≡ non zero
  - Z ≡ zero
  - NC ≡ non carry
  - C ≡ carry
  - PO ≡ Parity odd or no over flow
  - PE ≡ Parity even or over flow
  - P ≡ Positive
  - M ≡ Negative (minus)
- d ≡ any 8-bit destination register or memory location
- dd ≡ any 16-bit destination register or memory location
- e ≡ 8-bit signed 2's complement displacement used in relative jumps and indexed addressing
- L ≡ 8 special call locations in page zero. In decimal notation these are 0, 8, 16, 24, 32, 40, 48 and 56
- n ≡ any 8-bit binary number
- nn ≡ any 16-bit binary number
- r ≡ any 8-bit general purpose register (A, B, C, D, E, H, or L)
- s ≡ any 8-bit source register or memory location
- s_b ≡ a bit in a specific 8-bit register or memory location
- ss ≡ any 16-bit source register or memory location
- subscript "L" ≡ the low order 8 bits of a 16-bit register
- subscript "H" ≡ the high order 8 bits of a 16-bit register
- ( ) ≡ the contents within the ( ) are to be used as a pointer to a memory location or I/O port number

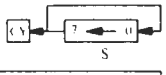
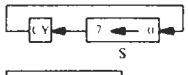
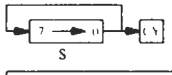
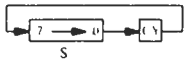
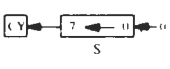
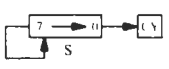
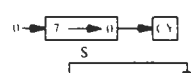
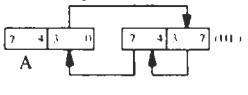
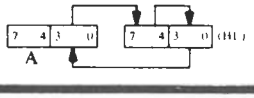
8-bit registers are A, B, C, D, E, H, L, I and R
16-bit register pairs are AF, BC, DE and HL
16-bit registers are SP, PC, IX and IY

Addressing Modes implemented include combinations of the following:

- Immediate
- Immediate extended
- Modified Page Zero
- Relative
- Extended
- Indexed
- Register
- Implied
- Register Indirect
- Bit

	Mnemonic	Symbolic Operation	Comments
8-BIT LOADS	LD r, s	r ← s	s ≡ r, n, (HL), (IX+e), (IY+e)
	LD d, r	d ← r	d ≡ (HL), r (IX+e), (IY+e)
	LD d, n	d ← n	d ≡ (HL), (IX+e), (IY+e)
	LD A, s	A ← s	s ≡ (BC), (DE), (nn), I, R
	LD d, A	d ← A	d ≡ (BC), (DE), (nn), I, R
16-BIT LOADS	LD dd, nn	dd ← nn	dd ≡ BC, DE, HL, SP, IX, IY
	LD dd, (nn)	dd ← (nn)	dd ≡ BC, DE, HL, SP, IX, IY
	LD (nn), ss	(nn) ← ss	ss ≡ BC, DE, HL, SP, IX, IY
	LD SP, ss	SP ← ss	ss = HL, IX, IY
	PUSH ss	$(SP-1) \leftarrow ss_H$; $(SP-2) \leftarrow ss_L$	ss = BC, DE, HL, AF, IX, IY
	POP dd	$dd_L \leftarrow (SP)$; $dd_H \leftarrow (SP+1)$	dd = BC, DE, HL, AF, IX, IY
EXCHANGES	EX DE, HL	DE ↔ HL	
	EX AF, AF'	AF ↔ AF'	
	EXX	$\begin{pmatrix} BC \\ DE \\ HL \end{pmatrix} \leftrightarrow \begin{pmatrix} BC' \\ DE' \\ HL' \end{pmatrix}$	
	EX (SP), ss	$(SP) \leftrightarrow ss_L$, $(SP+1) \leftrightarrow ss_H$	ss ≡ HL, IX, IY

	Mnemonic	Symbolic Operation	Comments
MEMORY BLOCK MOVES	LDI	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1	
	LDIR	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1 Repeat until BC = 0	
	LDD	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1	
	LDDR	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1 Repeat until BC = 0	
MEMORY BLOCK SEARCHES	CPI	A-(HL), HL ← HL+1 BC ← BC-1	
	CPIR	A-(HL), HL ← HL+1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	A-(HL) sets the flags only. A is not affected
	CPD	A-(HL), HL ← HL-1 BC ← BC-1	
	CPDR	A-(HL), HL ← HL-1 BC ← BC-1, Repeat until BC= 0 or A = (HL)	
8-BIT ALU	ADD s	A ← A + s	
	ADC s	A ← A + s + CY	CY is the carry flag
	SUB s	A ← A - s	
	SBC s	A ← A - s - CY	s ≡ r, n, (HL) (IX+e), (IY+e)
	AND s	A ← A ∧ s	
	OR s	A ← A ∨ s	
	XOR s	A ← A ⊕ s	

	Mnemonic	Symbolic Operation	Comments
8-BIT ALU	CP s	A - s	s = r, n (HL) (IX+e), (IY+e)
	INC d	d ← d + 1	d = r, (HL) (IX+e), (IY+e)
	DEC d	d ← d - 1	
16-BIT ARITHMETIC	ADD HL, ss	HL ← HL + ss	ss ≡ BC, DE HL, SP
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL - ss - CY	
	ADD IX, ss	IX ← IX + ss	ss ≡ BC, DE, IX, SP
	ADD IY, ss	IY ← IY + ss	ss ≡ BC, DE, IY, SP
	INC dd	dd ← dd + 1	dd ≡ BC, DE, HL, SP, IX, IY
	DEC dd	dd ← dd - 1	dd ≡ BC, DE, HL, SP, IX, IY
GP ACC. & FLAG	DAA	Converts A contents into packed BCD following add or subtract.	Operands must be in packed BCD format
	CPL	$A \leftarrow \overline{A}$	
	NEG	A ← 00 − A	
	CCF	$CY \leftarrow \overline{CY}$	
	SCF	CY ← 1	
MISCELLANEOUS	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable Interrupts	
	EI	Enable Interrupts	
	IM 0	Set interrupt mode 0	8080A mode
	IM 1	Set interrupt mode 1	Call to 0038_H
	IM 2	Set interrupt mode 2	Indirect Call
ROTATES AND SHIFTS	RLC s		s ≡ r, (HL) (IX+e), (IY+e)
	RL s		
	RRC s		
	RR s		
	SLA s		
	SRA s		
	SRL s		
	RLD		
	RRD		

	Mnemonic	Symbolic Operation	Comments
BIT S, R, & T	BIT b, s	$Z \leftarrow \overline{s_b}$	Z is zero flag
	SET b, s	$s_b \leftarrow 1$	s ≡ r, (HL) (IX+e), (IY+e)
	RES b, s	$s_b \leftarrow 0$	
INPUT AND OUTPUT	IN A, (n)	A ← (n)	
	IN r, (C)	r ← (C)	Set flags
	INI	(HL) ← (C), HL ← HL + 1 B ← B - 1	
	INIR	(HL) ← (C), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	IND	(HL) ← (C), HL ← HL - 1 B ← B - 1	
	INDR	(HL) ← (C), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
	OUT(n), A	(n) ← A	
	OUT(C), r	(C) ← r	
	OUTI	(C) ← (HL), HL ← HL + 1 B ← B - 1	
	OTIR	(C) ← (HL), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	OUTD	(C) ← (HL), HL ← HL - 1 B ← B - 1	
	OTDR	(C) ← (HL), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
JUMPS	JP nn	PC ← nn	cc ≡ NZ PO, Z PE, NC P, C M
	JP cc, nn	If condition cc is true PC ← nn, else continue	
	JR e	PC ← PC + e	
	JR kk, e	If condition kk is true PC ← PC + e, else continue	kk ≡ NZ NC, Z C
	JP (ss)	PC ← ss	ss = HL, IX, IY
	DJNZ e	B ← B - 1, if B = 0 continue, else PC ← PC + e	
CALLS	CALL nn	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, PC ← nn	cc ≡ NZ PO, Z PE, NC P, C M
	CALL cc, nn	If condition cc is false continue, else same as CALL nn	
RESTARTS	RST L	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, $PC_H \leftarrow 0$ $PC_L \leftarrow L$	
RETURNS	RET	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$	cc ≡ NZ PO, Z PE, NC P, C M
	RET cc	If condition cc is false continue, else same as RET	
	RETI	Return from interrupt, same as RET	
	RETN	Return from non-maskable interrupt	

Z-80 CPU A.C. Characteristics

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	4	[12]	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	180	[E]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	180	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145	nsec	C_L = 50pF
	$t_{F(AD)}$	Delay to Float		110	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		230	nsec	C_L = 50pF
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
	$t_{S\bar{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	60		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time	0		nsec	
$\overline{MREQ}$	$t_{DL\Phi(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		100	nsec	C_L = 50pF
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{DH\bar{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{w(MRL)}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(MRH)}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90	nsec	C_L = 50pF
	$t_{DL\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100	nsec	
	$t_{DH\bar{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		110	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100	nsec	C_L = 50pF
	$t_{DL\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		100	nsec	
	$t_{DH\bar{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	nsec	C_L = 50pF
	$t_{DL\bar{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90	nsec	
	$t_{DH\bar{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100	nsec	
	$t_{w(\overline{WR}L)}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		130	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		130	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180	nsec	C_L = 50pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		150	nsec	
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{S(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{S(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110	nsec	
$\overline{RESET}$	$t_{S(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		100	nsec	
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec	

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 40$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 60$

[5] $t_{dcm} = t_c - 210$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 210$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 80$

[8] $t_{w(MRL)} = t_c - 40$

[9] $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 30$

[10] $t_{w(\overline{WR}L)} = t_c - 40$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 80$

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

NOTES

A Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

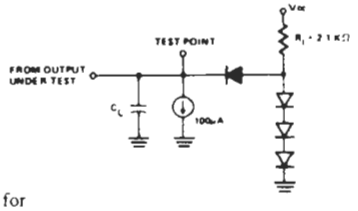
C The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D Output Delay vs. Loaded Capacitance

TA = 70 C Vcc = +5V ±5%

Add 10nsec delay for each 50pf increase in load up to a maximum of 200pf for the data bus & 100pf for address & control lines

E Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum



Load circuit for Output

Z-80A CPU A.C. Characteristics

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	.25	[12]	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	110	[E]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	110	2000	nsec	
	$t_{r,f}$	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	nsec	C_L = 50pF
	$t_{F(AD)}$	Delay to Float		90	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		150	nsec	C_L = 50pf
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	50		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time		0	nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		85	nsec	C_L = 50pf
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		85	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		85	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		85	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		85	nsec	C_L = 50pf
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		85	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		65	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80	nsec	
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		80	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		100	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		100	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130	nsec	C_L = 50pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		120	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	50		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		100	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		100	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	60		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80	nsec	
	t_{mr}	M1 Stable Prior to IORQ (Interrupt Ack.)	[11]		nsec	

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 65$

[2] $t_{aci} = t_c - 70$

[3] $t_{ca} = t_{w(\Phi L)} + t_r - 50$

[4] $t_{caf} = t_{w(\Phi L)} + t_r - 45$

[5] $t_{dcm} = t_c - 170$

[6] $t_{dci} = t_{w(\Phi L)} + t_r - 170$

[7] $t_{cdf} = t_{w(\Phi L)} + t_r - 70$

[8] $t_{w(\overline{MRL})} = t_c - 30$

[9] $t_{w(\overline{MRH})} = t_{w(\Phi H)} + t_f - 20$

[10] $t_{w(\overline{WRL})} = t_c - 30$

[11] $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

NOTES

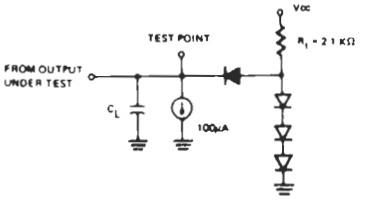
A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance
TA = 70°C Vcc = +5V ±5%
Add 10nsec delay for each 50pf increase in load up to maximum of 200pf for data bus and 100pf for address & control lines.

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum

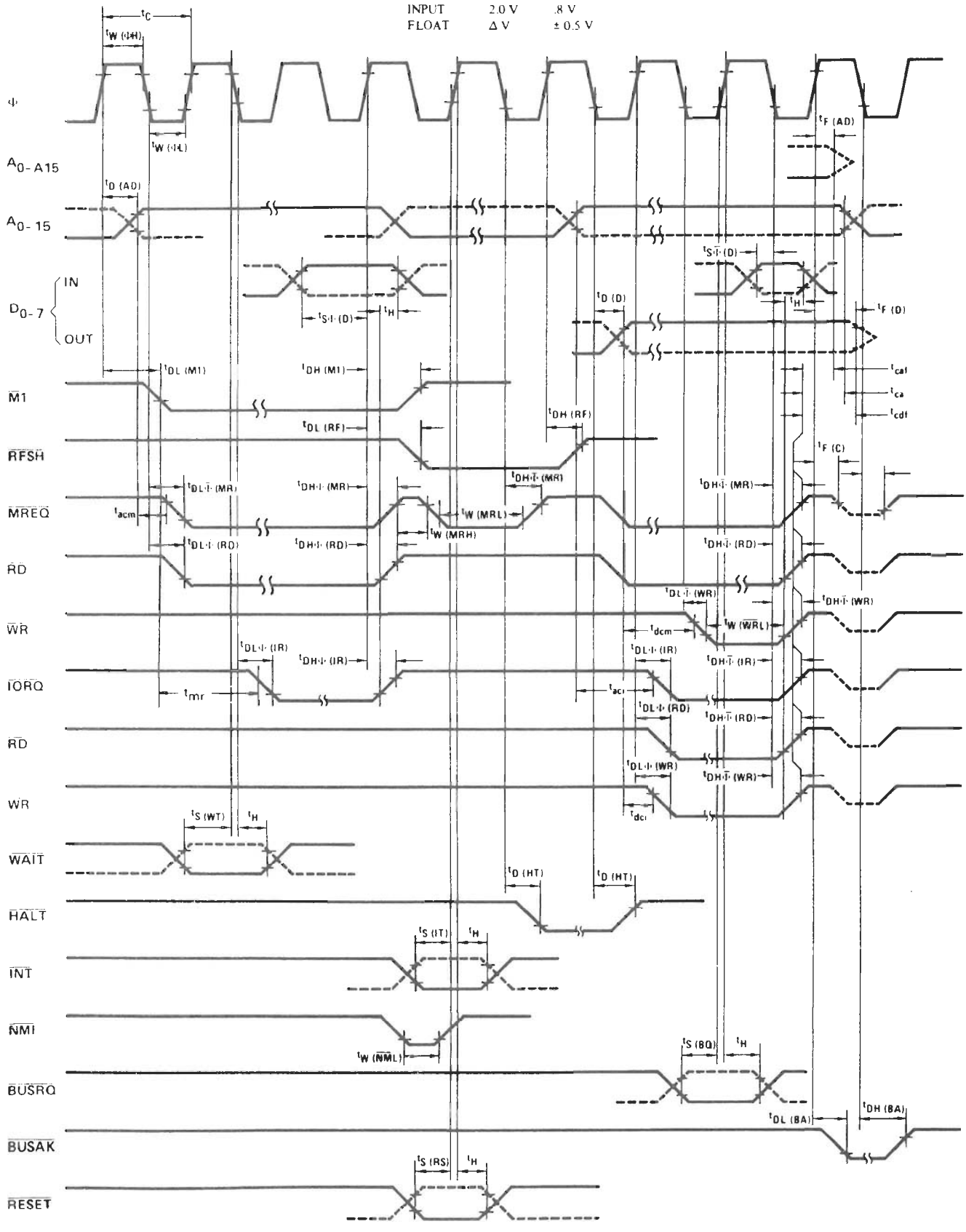


Load circuit for Output

A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{cc} -.6V	.45V
OUTPUT	2.0 V	.8 V
INPUT	2.0 V	.8 V
FLOAT	Δ V	± 0.5 V



Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{cc}.

I_{cc} = 200 mA

Z-80 CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc}-.6		V_{cc}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-250μA
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z-80 CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C
E – Extended 5V ±5% -40° to 85°C
M – Military 5V ±10% -55° to 125°C

Z-80A CPU D.C. Characteristics

T_A =0°C to 70°C, V_{cc} =5V±5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc}-.6		V_{cc}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-250μA
I_{CC}	Power Supply Current		90	200	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

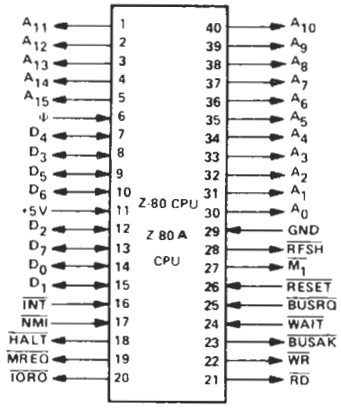
T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_Φ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

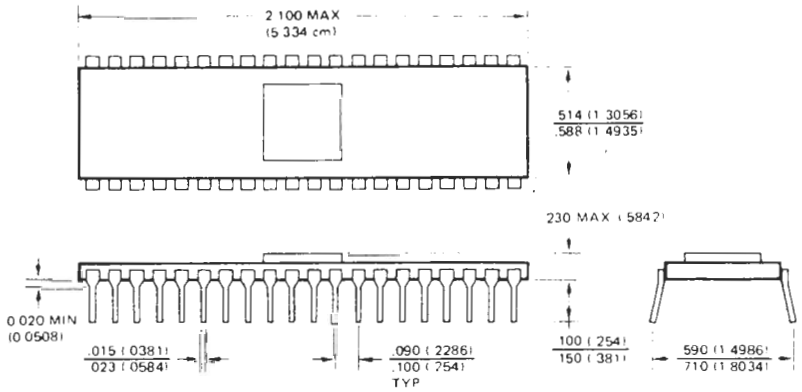
Z-80A CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C

Package Configuration



Package Outline



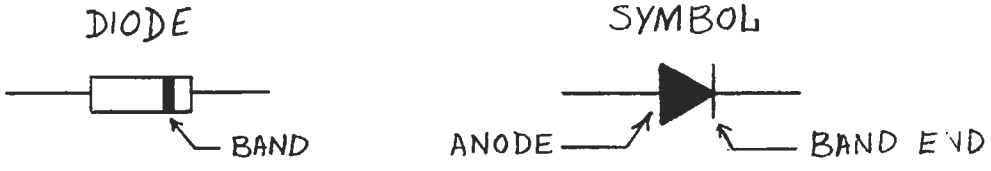
*Dimensions for metric system are in parentheses

CB2 ENGINEERING NOTE

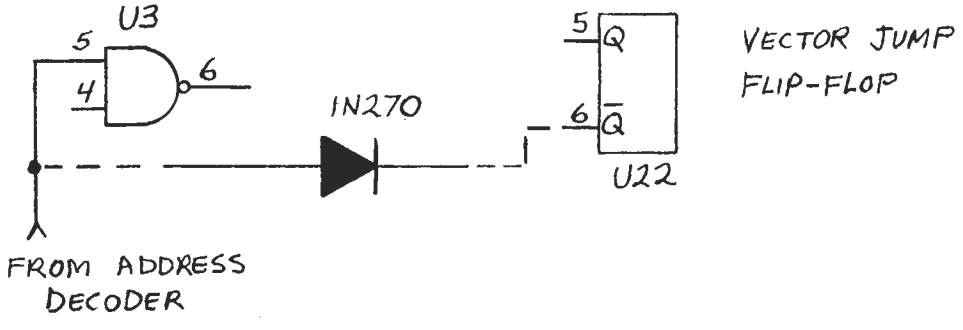
PROBLEM: USING ON-BOARD VECTOR JUMP OPTION WITH THE SECOND RAM/ROM SOCKET ADDRESSED AT ØØØØ HEX. The CB2 cannot read the bytes from the first ROM socket (U16) during a vector jump process.

CAUSE: During POC or RESET, the data from the U16 is sent to the Z80 chip for the first instruction fetch cycle, if the vector jump option is selected. During this fetch cycle, the CPU's address was reset to ØØØØ Hex. If the second socket (U17) is addressed to ØØØØ Hex, then there is a data conflict between U16 and U17. (This problem does not occur with external memory addressed at ØØØØ Hex.)

FIX: The second socket (U17) must be disabled during an on-board vector jump operation. Connect a 1N270 diode (germanium) between the jump circuit and the address decoder for U17.



Connect the anode of the diode to U3, pin 5, and the cathode (band end) to U22, pin 6.



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5-13-81
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