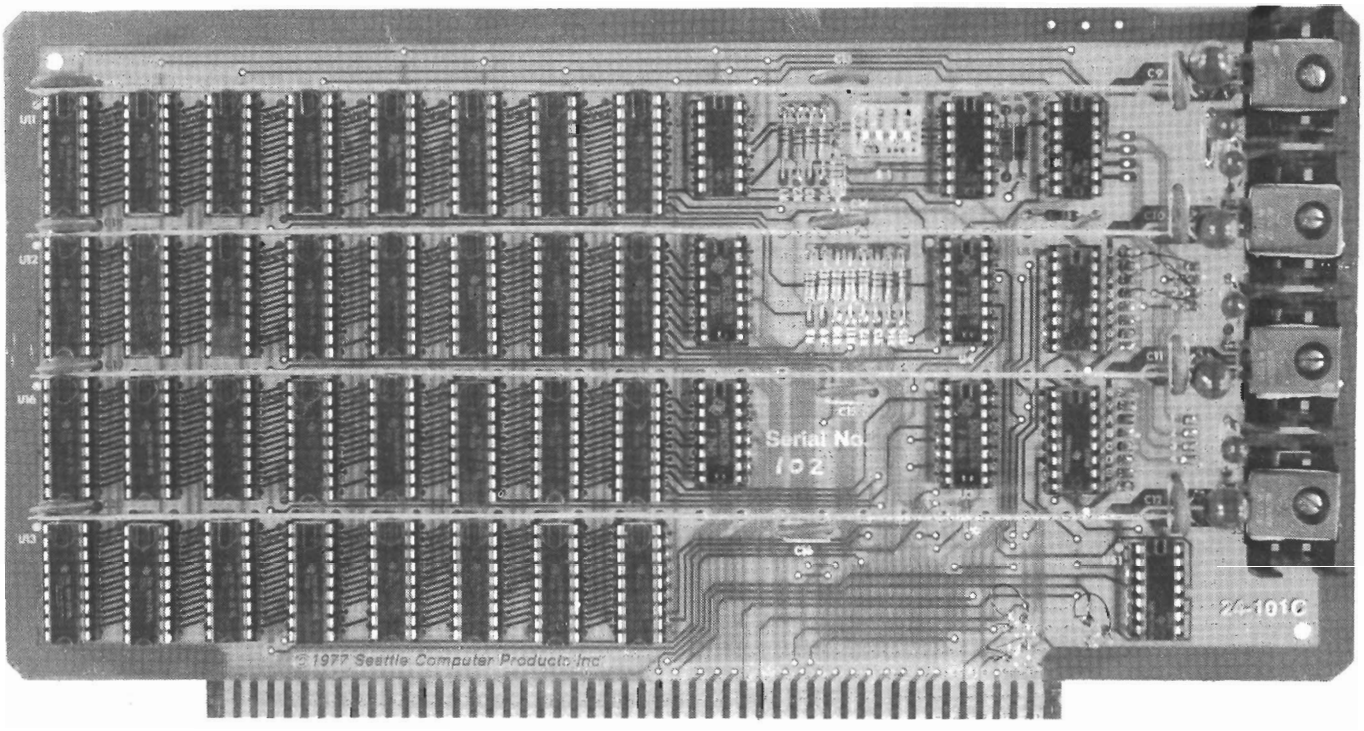
Model 24-101 16K RAM Memory Board



This board is fully compatible with the S-100 bus and should interface without difficulty to the MITS 8080, IMSAI, Poly 88, Sol 20, Cromemco, Alpha-Micro, and similar microprocessor systems. It was designed to operate without wait states with a Z-80A processor operating at 4 Mhz. when populated with the 250 nsec. memory chip. With the 450 nsec. chip, it will operate in 2 Mhz. systems without wait states. Its fully static design ensures "no clocking or interference problems" when used for DMA.

Operation Manual

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Seattle Computer Products, Inc.
1114 Industry Drive, Seattle, WA. 98188
(206) 255-0750

One-Year Limited Warranty

WARRANTEE AND WARRANTY PERIOD

The Seattle Computer Products Inc. (hereinafter referred to as SCPI) Model 24-101 16K RAM Board Warranty extends to the original purchaser and all subsequent owners of the board for the period of one year from the time the board is first purchased by the user and for such additional times as the board may be out of the owner's possession for the purpose of receiving warranty service at the factory.

WARRANTY COVERAGE

The board is warranted to be free of defects in material and workmanship and to perform within the specifications outlined on page 8 of this manual during the period of the warranty. THIS WARRANTY DOES NOT COVER DAMAGE AND IS VOID IF THE BOARD HAS BEEN DAMAGED BY NEGLECT, ACCIDENT, UNREASONABLE USE (INCLUDING INPUT VOLTAGES AND AMBIENT TEMPERATURES EXCEEDING THOSE ALLOWED BY THE SPECIFICATIONS), IMPROPER SERVICE, OR OTHER CAUSES NOT ARISING OUT OF DEFECTS IN MATERIAL OR WORKMANSHIP.

WARRANTY PERFORMANCE

During the warranty period, SCPI will repair or replace defective boards or components upon written notice that a defect exists. Defective memory ICs must be returned to SCPI prior to replacement. Other components will be replaced without the part being returned to the factory WITH THE EXCEPTION THAT SCPI IN ALL CASES RETAINS THE RIGHT TO EXAMINE THE DEFECTIVE BOARD PRIOR TO COMPONENT REPLACEMENT. In the event the return of the board or part is requested or required under this warranty, the owner must ship the board or part prepaid to SCPI. SCPI will pay all postage for shipment of boards back to the owner or parts to the owner. All repairs or replacements by SCPI under this warranty will be performed within five days following receipt of notice of defect or return of components as called for under this warranty.

WARRANTY DISCLAIMERS

ANY IMPLIED WARRANTIES ARISING FROM THE SALE OF THIS MEMORY BOARD ARE LIMITED IN DURATION TO THE WARRANTY PERIOD DEFINED ABOVE. SCPI SHALL NOT BE LIABLE FOR LOSS OF USE OF THE MEMORY BOARD OR ANY SYSTEM INTO WHICH IT IS INSTALLED OR FOR DAMAGES INCURRED BY THE PURCHASER OR ANY SUBSEQUENT USER OF THE BOARD. Some states do not allow the exclusion or limitation of implied warranties or consequential damages, so the above limitations may not apply to every purchaser.

LEGAL REMEDIES

This warranty gives the purchaser specific legal rights. He may have additional rights which vary from state to state.

MAILING INSTRUCTIONS

In the event it becomes necessary to return the memory board or other components to SCPI, also return a written explanation of the difficulty encountered along with your name, address and phone number. Package the items in a crushproof mailing container with adequate packing material to prevent damage, and mail postpaid to:

Seattle Computer Products, Inc.
1114 Industry Drive, Seattle, WA. 98188
(206) 255-0750

THEORY OF OPERATION

It is suggested that you fold out the schematic contained at the back of this manual so that you can refer to it while reading this section. The design of the board is straight foreword. There are no trick circuits. It should be relatively easy to understand, and even easier to troubleshoot, if the need arises.

Certain assumptions should be made as an aid in understanding the operation of the board. After a general understanding of the circuitry has been obtained, the effect of changing these assumptions should present no undue difficulties. The assumptions are:

1: MWRITE, SINP, and SOUT are used in your system and these lines have a "low" signal on them.

2: You have selected the following address slots for the board:

0 (0000H to 0FFFH)
1 (1000H to 1FFFH)
2 (2000H to 2FFFH)
3 (3000H to 3FFFH)

3: The memory has not been protected.

The key to understanding the operation of the board is to consider it to be a "Memory Array" with supporting circuits for buffering and reading and writing control.

Memory Array

The Memory Array includes 32 4Kx1 static RAM chips organized as four "columns" of 4K by 8 bits each. All address changes or write commands are fed to all 32 chips, however, only the eight chips which are "selected" by the "low" CS signal will be active. Data to the board (CPU Data Out Bus) is continually being sent to all 32 chips, however, to "write" new data into the chips requires several actions including a low CS signal to the particular column and a WRITE command. The output of the chips is in the "high impedance state" unless the chip is selected.

Note the identification of the chips: U11 is column 1, bit 1; U12 is column 1, bit 2; etc. In general, the first digit of the IC number in the Memory Array defines the column while the second defines the bit.

Address Buffers

Address lines A-0 through A-11 are buffered by 74LS367 buffers. These buffers provide low loading to the processor bus and high current output for fast switching of address information to the Memory Array. The buffers are enabled at all times so the address information at the chips continually follows the bus.

Column Select

The Column Select circuitry accepts addresses A-12 through A-15 as inputs along with the signals SINP and SOUT. The basic function of the circuit is to determine if the CPU is addressing memory contained on this particular board. The ground rules for examining the circuit call for SINP and SOUT to be "low" and memory slots 0, 1, 2, and 3 to be selected for this board.

Assume the CPU outputs "4XXX" as an address. This is decoded by the two 78LS138 ICs as a low output on pin 11 of U8. All of the other outputs remain high. The board will disregard the following "read" or "write" commands issued by the CPU because this particular board has not been addressed.

In this next example, assume the CPU outputs the address "2XXX". This is decoded by the circuit to produce a low output on pin 13 of U8 which (in our example) has been jumpered to "column 3" and sent out of the Column Select part of the circuit to three locations:

1. The low CS3 signal goes to the Memory Array where it activates a column of eight out of the 32 chips.

2. It goes to the Data Out Buffer Control where it enables the circuit to receive the CPU "read" command.

3. It goes to the Memory Write circuit where it is one of the signals used to determine whether the "write path" should be enabled.

The effect of this signal in the three destinations will be considered separately in the sections of the manual devoted to the particular circuits.

Memory Write

The Memory Write section has two basic functions: allowing writing into the memory on the board when the CPU commands it, and preventing the writing if the particular memory slot has been "protected". Following our assumptions, consider the MWRITE input "low".

Three cases will serve to illustrate the operation of this circuitry. First, assume a write cycle directed to address "1XXX" with no "memory protect". The addresses have been outputted by the CPU. The Address Buffers have sent A-0 through A-11 to the Memory Array. The Columns Select circuitry has decoded A-12 through A-15 and sent a low CS signal to column 2 of the Memory Array, activating the eight chips in that memory slot. Data has been sent to the Memory Array. Now--WR (low) is presented to the Memory Write circuit.

This signal is inverted twice through U51 and presented to the input pin 14 of U4, the Memory Write Buffer. In this example, the buffer has already been enabled and the Memory Write Signal is sent through the buffer to all 32 chips in the Memory Array. The eight chips which have been "activated" by the low CS signal will "write" the data presented by the CPU Data Out Bus into the memory cells specified by the address.

In the preceding paragraph it was stated that the Memory Write Buffer had been previously enabled by a low CS signal. Let us examine how this took place. When A-12 through A-15 were decoded by the Column Select Circuit, a low CS2 signal was generated which was sent to pin 9 of U5. U5 acts as an inverter resulting in a high signal being presented to pin 6 of U6. In the absence of a Memory Protect function, pin 5 of U6 is held high by the 2.2K pull-up resistor connected to +5 volts. The output of this gate, pin 4, will be low if both of the inputs are high. This low on the output is tied directly to pin 15 of the Memory Write Buffer and thus enables the buffer.

For the second example, assume memory slot 2 (1000H to 1FFFH) has been "protected". This is accomplished by setting memory protect switch 2 to the "on" position. This grounds input pin 5 of U6. (Note: on some schematics the switches are incorrectly labled--they should read (left to right) 4,3,2,1) The inputs to this gate are now "high" for the CS2 signal and "low" for the switch. The output will go "high", disabling the Memory Write Buffer and preventing a Memory Write Signal from being sent to the Memory Array.

The third example assumes memory slots 1, 3, and 4 are "protected" and slot 2 is not. The three Memory Protect Switches being closed presents a low to three of the four U6 gates. The gate logic produces a "high" at the outputs of these three gates. However, the number 2 switch is open, allowing a high to be presented to pin 5 of U6. Pin 6 is also high (CS2 being low and then inverted). The output of this NAND gate is low. Since the outputs of all four U6 gates are "wired-or" together, the low on pin 4 of U6 pulls the line down, thus enabling the Memory Write Buffer.

Data Out Buffers

The Data Out Buffers present data to the CPU Data In Bus from the Memory Array upon command of the CPU. Each of the buffers is capable of sourcing 2.6 ma. for a high signal and sinking 16 ma. for a low. They are in the high impedance state when not enabled. Bus loading in the high impedance state is 20 uamps. The Output Buffer Enable Signal must be low to enable the buffers.

Data Out Buffer Control

This circuit determines when the Data Out Buffers should be enabled. The MEMR signal will be discussed in the "Configuration" section. Assume here that it is "high".

When the CPU desires data from memory, DBIN will go high. For this to result in an active Output Buffer Enable Signal, two conditions must be met: first, one of the CS lines must be low, signifying that one of the Memory Array columns on THIS BOARD has been addressed, and second, RAM Disable must be high. The action of the low CS signal is to cause pin 8 of U7 to be high. With all of the inputs of the other U7 gate being high, the output (Output Data Enable Signal) will be low, enabling the buffers.

If this particular board is not selected, there will be no low CS signal, causing pin 1 to be low. This low on the input of the gate prevents pin 6 from being low.

Some systems have an active low RAM Disable or Phantom Line which allows more than one memory device to occupy the same address space. For these systems, the bus line used for this purpose may be tied to point "W" which maintains the Output Buffers in the high impedance state whenever the low signal is present at "W".

Data In Conditioning

This circuit uses pull-up resistors which essentially eliminate DC bus loading for a "high" signal. Maximum loading for a "low" is less than 250 uamps. The resistors also serve the purpose of bypassing transients on the CPU Data Out Bus lines.

Power System

The Power System consists of four nearly identical circuits. Considering the one containing U52, C1 prevents oscillations of the regulator input circuit. C5, C9, C13, and C17 provide transient suppression on the +5 volt output line. Bus bars are used for this design. They provide a very low impedance power distribution line and greatly reduce voltage transients on the line. The regulator provides both overcurrent and thermal shutdown in the event of a fault on the +5 volt line.

CONFIGURATION

This RAM board contains jumpers which will allow you to customize it to any known S-100 bus microcomputer. As received from the factory, the board will plug directly into an IMSAI without modification. This is the configuration most commonly used. Subsequent sections of this manual will show you how to alter these jumpers if your system requires a different configuration.

For in-factory testing, the address jumpers are set at the lowest 16K. The next section describes how to alter these jumpers to locate memory at other addresses.

Selecting Memory Slots

The Memory Array on the board is organized as four "columns" of 4K bytes. Each of these columns is independently addressable to any 4K slot in the 64K available to most CPUs. The four highest address bits (A-12 through A-15) are decoded by the Column Select section of the board to produce 16 active low signals which may be chosen from to obtain chip select for the Memory Array. Any four of these may be chosen to connect to the four "columns" of the array.

Located on the board to the right of U8 and U9 can be seen 16 wire-wrap pins with the numbers 0 through F opposite them. Each of these pins represents one 4K slot out of the 16 available. Farther to the right of each IC can be seen four additional pins. These represent the four "columns" of the Memory Array.

As received from the factory, memory slot 0000H to 0FFFH has been already connected to "column 1". The next three memory slots have been connected to columns 2, 3, and 4 in a similar manner.

Let us suppose you wish to change the address of the board from the factory settings to 8000H to BFFFH. To do this you would first have to remove the wire-wrap connections from the pins representing slots 0, 1, 2, and 3, and then reconnect them to the pins representing slots 8, 9, A, and B. Other memory addresses may be selected in a like manner.

CAUTION: There are two sets of "column pins" -- one opposite each 74LS138. It is possible to connect a chip select output to the same number pin in both the upper and the lower group. To do so would cause the memory to operate incorrectly. The proper connection will use each column pin only once. (If you use column 1 in the upper group, don't use it again in the lower group.)

SINP, SOUT Signals

SINP and SOUT signals are used in most systems to indicate that a CPU read of an input port or a write to an output port is in progress. In some systems the addresses of these ports overlap addressable memory. To handle the conflict, a high on either the SINP or SOUT line is used to disable RAM memory. This memory board allows this disabling function.

Whether your system uses SINP and SOUT can be determined by checking the schematic of the system for the presence of the two signals on bus lines 45 and 46. If the signals are used, the board is wired correctly as received. If the signals are not used, change the location of jumpers "X" and "Y" (located in the lower right hand corner of the board) from the "8 o'clock" to the "5 o'clock" position.

MWRITE Signal

The MWRITE signal is generally used in two ways: as a status signal which indicates that the current CPU cycle is a "write cycle" and the memory "Data In Buffers" should be enabled, or, as an auxiliary write command (as for example--from the front panel). IMSAI and MITS systems use it as a front panel write command. Jumper "Z" is connected at the factory for this front panel write function.

This board does not use Data In Buffers. If MWRITE is used in your system solely to enable this type buffer, the signal is not needed for this board and the jumper may be connected to the "8 0'clock" or ground position.

MEMR Signal

Some systems use MEMR as a status signal similar to MWRITE above. This board uses a pull-up resistor on this line and the board will function properly with both the systems which use and those which do not use this command.

Memory Disable

Some systems locate ROM and RAM in the same address space. To resolve the conflict, and active low Memory Disable or Phantom signal is generated by the CPU board to disable RAM whenever a ROM read is in progress.

Unfortunately, the location on the bus of this signal is not consistent from one system to another. S-100 bus line 67 is most commonly used for the signal.

If your system uses an active low signal for RAM Disable, jumper the S-100 edge connector finger reserved for it to hole "W" which is located near the upper right hand corner between U6 and U7. When soldering to the finger, use care that the board will still go into its socket after the jumper has been installed. No connection is necessary to hole "W" if your system does not have the RAM Disable feature.

Memory Protect

It is sometimes desirable to protect memory from being overwritten. This option is particularly attractive after the computer operator has spent considerable time "keying in" a lengthy program. On this board, each of the four columns may be separately protected to prevent unintentional memory changes.

This board contains a DIP switch with four switches labled 1 through 4. To protect a 4K block of memory, move the switch corresponding to the memory "column" to the "on" or up position. This switch should be accessible when your RAM board is installed in your computer.

REPAIR SERVICE

Seattle Computer Products Inc. will perform repair service and provide replacement parts at nominal rates for its products which are not under warranty. As cost of replacement parts vary from time to time, a current replacement price list may be obtained upon request. For service work, the owner will be notified prior to any work being performed if the cost to him exceeds $20 (exclusive of transportation and insurance costs).

SPECIFICATIONS - MODEL 24-101 16K RAM BOARD - 250 and 450 nsec. Memory Chips

Electrical Characteristics

Parameter	Conditions	Min	Typ(1)	Max	Units
Signal Input Level		-0.5		5.5	volts
Power Supply Voltage		7.5	(2)	9.0	volts
Power Supply Current			1.6(3)		amps
High Level Input Voltage	All signal inputs	2.0		5.5	volts
Low Level Input Voltage	All signal inputs	-0.5		0.8	volts
High Level Input Current	Vcc=5.5V				
A-0 through A-11	Vi=2.7V			20	uamps
A-12 through A-15				40	uamps
SINP, SOUT				40	uamps
DBIN, MWRITE, WR				20	uamps
MEMR, RAM DISABLE				-210	uamps
CPU Data Out Bus				-64	uamps
Low Level Input Current	Vcc=5.5V				
A-0 through A-11	Vi=0.4V			0.4	ma
A-12 through A-15				0.72	ma
SINP, SOUT				0.72	ma
DBIN, MWRITE, WR				0.36	ma
MEMR, RAM DISABLE				0.46	ma
CPU Data Out Bus				0.24	ma
Data Out Buffers	Vcc=5.5V				
High Voltage Out		2.4	3.1		volts
Low Voltage Out			0.2	0.5	volts
High Level Output Current				2.6	ma
Low Level Output Current				16.0	ma
High-Z Output Current		-20		+20	uamps

AC Characteristics - 250 nsec Memory Chip

Read Timing (Access time = Cycle Time)					
Data Valid from Address on Bus				294	nsec
Write Timing					
Minimum Cycle				272	nsec

AC Characteristics - 450 nsec Memory Chip

Raad Timing (Access Time = Cycle Time)					
Data Valid from Address on Bus				494	nsec
Write Timing					
Minimum Cycle				472	nsec

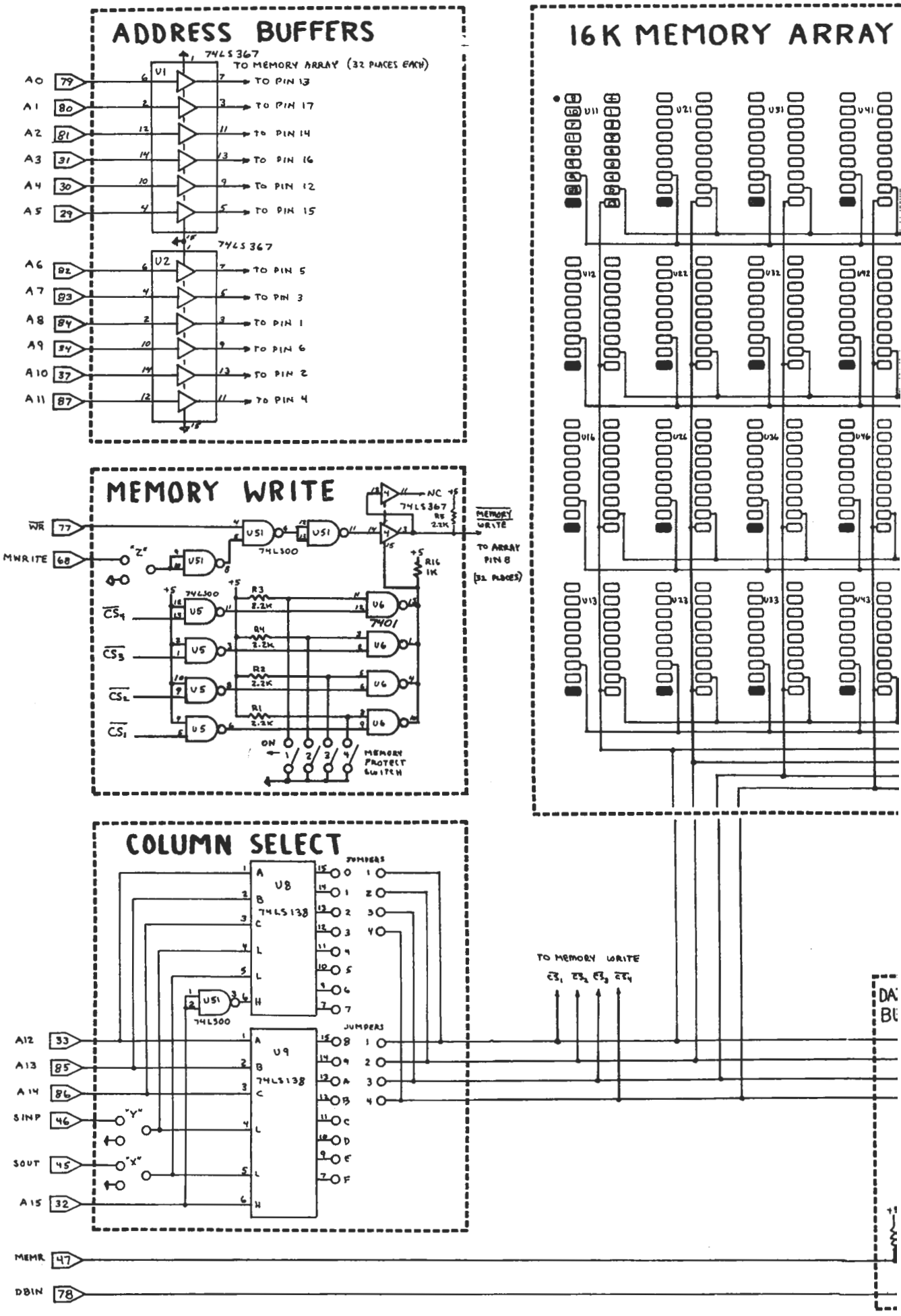
Thermal Characteristics

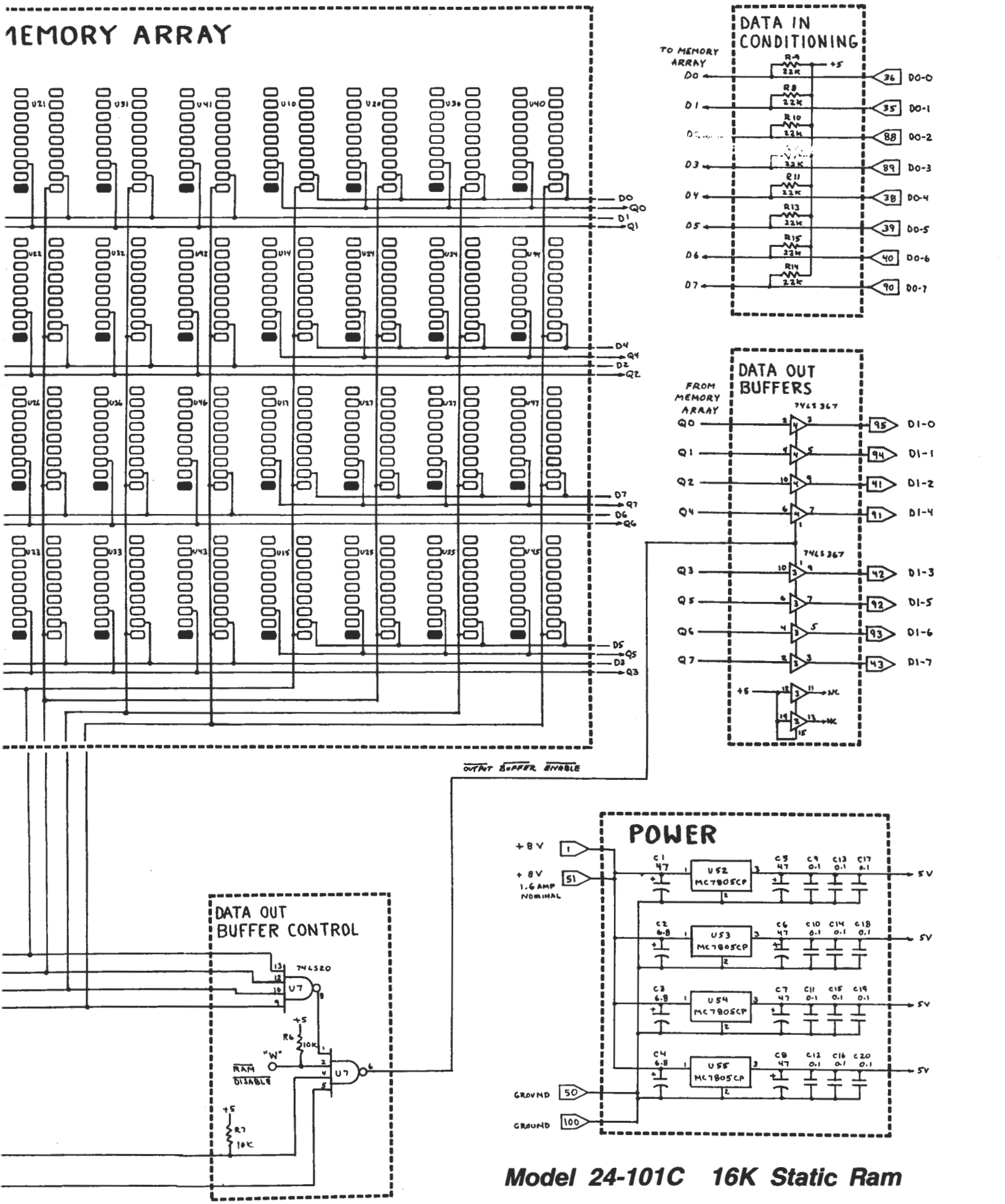
While all components on this board are qualified for a minimum of 0 to 70 degrees C. temperature environment, the board is warranted to operate correctly between 5 and 65 degrees C. only.

Note 1: Typ is at 25 degrees C.

Note 2: The input regulators will handle voltages exceeding +9, however, if the RMS value exceeds +9, convection cooling may be insufficient to dissipate the heat generated and forced air circulation may be required.

Note 3: The 1.6 amp current requirement specification at 25 degrees C. is nominal and may vary ± 10 % dependent upon memory chip lot and tolerance of the voltage regulators.





Model 24-101C 16K Static Ram