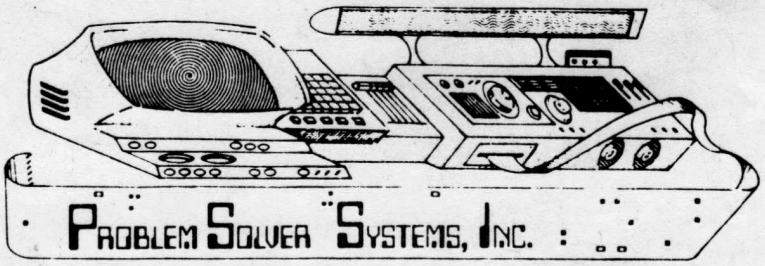
888-5079



888-4764

Manufacturers of QuanTronics Computer Products
8040 DEERING AVE. · SUITE 10 · CANOGA PARK, CA. 91304

QUANTRONICS

MODEL MM8 8K RAM SYSTEM
INSTRUCTIONS

This 8K Static Random Access Memory System is manufactured and tested to the highest possible quality standards. If properly operated and cared for, it will give many years of trouble-free service. It is important that you remember to turn-off power on your computer before installing or removing the memory board.

SWITCHES:

The MM8 is supplied with two seven position DIP switches. When setting these switches, it is recommended to use a pencil or other small pointed object to push the switch lever, thus ensuring that the switch lever is firmly snapped into position. A relatively small amount of positional offset could cause the switch to be (OFF) when it should be (ON). (ON) means that the portion of the switch nearest the top of the board is pushed in toward the board.

ADDRESSING:

Address selection is accomplished using switch S2, positions 1, 2, & 3. The address position can be placed on any 8K memory boundary. Switch S2 positions 4, 5, 6, and 7 are used when less than 8K of memory is desired on one board. If only 2K or 4K of memory is being used, address lines A12 and A11 may be assigned to the address of the board by turning (ON) switch S2, position 4 (for 4K) or position 5 (for 2K). If the full 8K complement is present on the board, both of these switches should be in the (ON) position, and positions 6 and 7 should be in the (OFF) position. If it is desired to use only 4K, leave position 7 (OFF) and position 6 (ON). For 2K operation, both should be (ON).

To position the MM8 at any 8K memory boundary, simply remember that positions 1-3 on S2 when (ON) determines memory address zero. Turning (ON) position 1 adds 32K to this address and similarly, positions 2 and 3 add 16 and 8K respectively. To position at 40K, therefore, switch position 1 and 3 would be (ON). To position at 8K, switch 3 would be (OFF). In all cases, the memory boundary position is determined by the sum of switches 1 through 3.

ADDRESS SELETION CHART

	Address Range Hex	High Order Bits A15	A14	A13	A12	A11	DIP Switch Setting (S2) 1	2	3	4	5	6	7
8K	0000 - 1FFF	0	0	0	0	0	ON	ON	ON	ON	ON	OFF	OFF
16K	2000 - 3FFF	0	0	1	0	0	ON	ON	OFF	ON	ON	OFF	OFF
24K	4000 - 5FFF	0	1	0	0	0	ON	OFF	ON	ON	ON	OFF	OFF
32K	6000 - 7FFF	0	1	1	0	0	ON	OFF	OFF	ON	ON	OFF	OFF
40K	8000 - 9FFF	1	0	0	0	0	OFF	ON	ON	ON	ON	OFF	OFF
48K	A000 - BFFF	1	0	1	0	0	OFF	ON	OFF	ON	ON	OFF	OFF
56K	C000 - DFFF	1	1	0	0	0	OFF	OFF	ON	ON	ON	OFF	OFF
64K	E000 - FFFF	1	1	1	0	0	OFF	OFF	OFF	ON	ON	OFF	OFF

MEMORY PROTECTION:

In order to use the memory protect option, it is first necessary to install the spare memory I.C. supplied with the system into the empty socket on the board. (I.C. 47) This memory I.C. is used to retain protect status when the memory protect switch activated. If your computer system is not equipped with a memory protect switch, it is advisable to leave I.C. 47 out of its socket, as the memory I.C. tends to power -up in a random state and could cause unwanted memory protection. Selection of memory areas to be protected is accomplished using switch S1, positions 1 through 5. These switches effectively disable address lines 12 through 8 respectively. When (ON) the following areas of memory are protected:

Protected Portion	Switch 1 Position 5	4	3	2	1
All but lower 256 bytes	ON	ON	ON	ON	ON
All but lower 512 bytes	OFF	ON	ON	ON	ON
All but lower 1024 bytes	OFF	OFF	ON	ON	ON
All but lower 2048 bytes	OFF	OFF	OFF	ON	ON
All but lower 4096 bytes	OFF	OFF	OFF	OFF	ON
NONE	OFF	OFF	OFF	OFF	OFF

If not using the protect feature it is advisable to leave all five (S1, positions 1 through 5) positions in the (OFF) position.

WAIT CYCLES:

In the event that your computer is capable of operation at a faster rate than the memory system you have chosen, provision is made to synchronize the memory to the computer using the PREADY line of the S100 bus. Switch S1 positions 6 and 7 select from zero to 2 wait cycles. Selection is made as follows:

	Switch 1 Position 6	7
0 wait states	ON/OFF*	ON
1 wait states	ON	OFF
2 wait states	OFF	OFF

*Position doesn't matter

INPUT/OUTPUT:

Provision is made on the MM8 to allow input or output to peripheral devices using the S100 input (SINP) and output (SOUT) functions. Assertion of either function deselects the MM8, thus allowing the computer to communicate.

directly with I/O devices without interference from the memory.

TESTING:

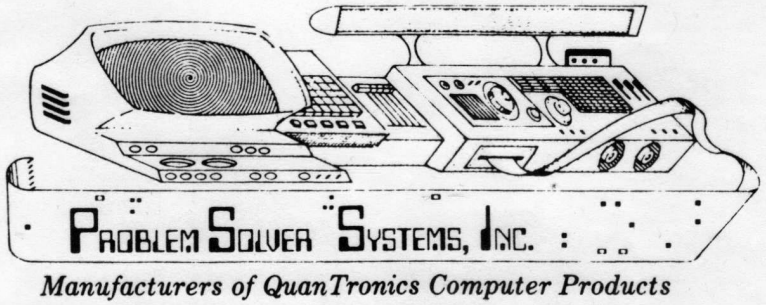
Each MM8 memory board undergoes a thorough testing program consisting of a 40 hour burn-in with power on followed by one-hour of our proprietary "Blitz test" which operates the boards at their maximum rate, and fails them if they make one error.

WARRANTY

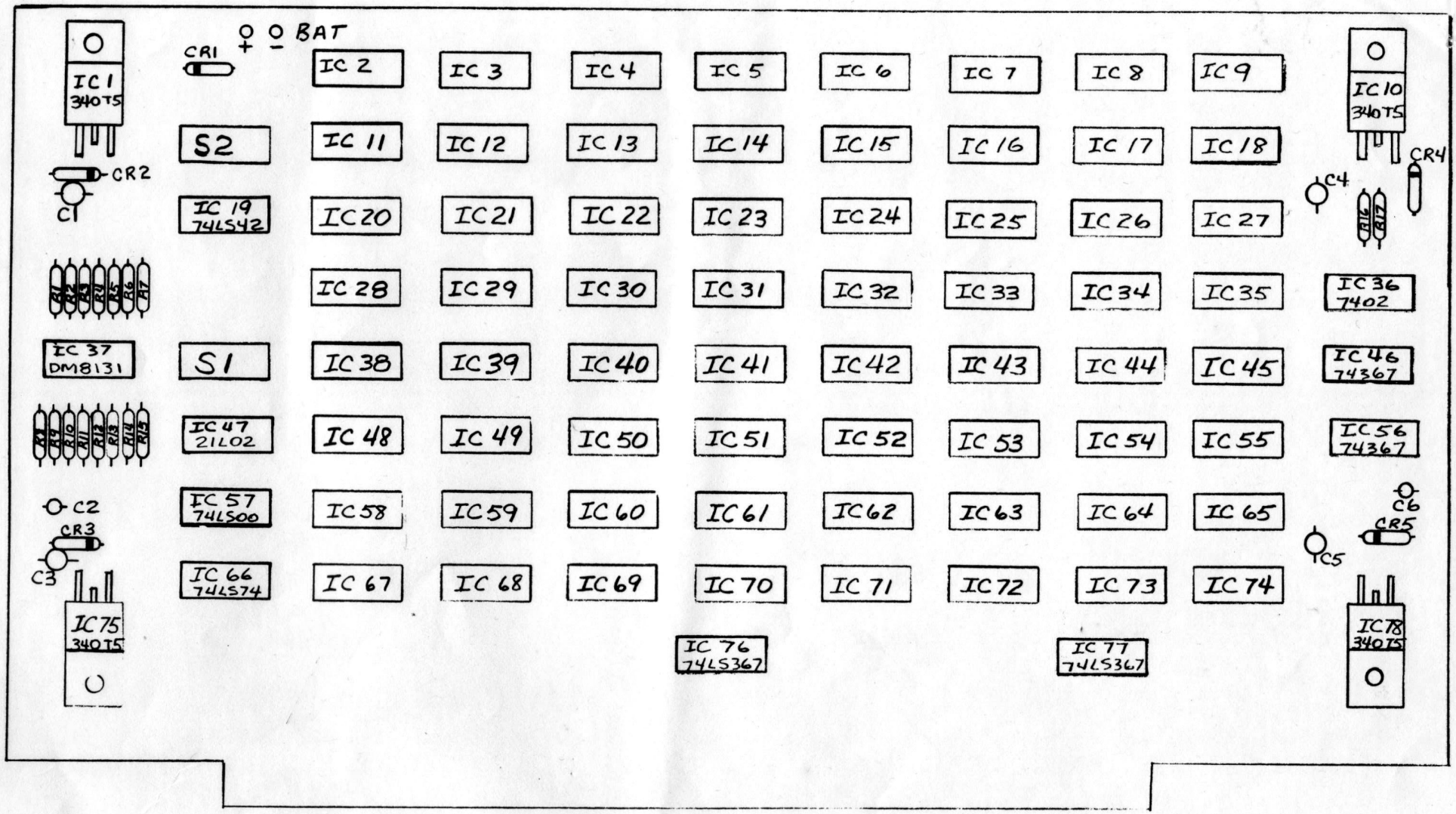
Problem Solver Systems, Inc. (Manufacturers of Quantronics Computer Products) offer a 120 day warranty an all parts and materials. This warranty covers every conceivable failure except for misuse or abuse of the memory system. Determination of misuse or abuse is determined solely by Problem Solver Systems, Inc. To obtain warranty repair or replacement, you may return it to the place of purchase or directly to the manufacturer along with proof of purchase date. Your memory system will be returned to you postpaid, promptly.

OUT OF WARRANTY SERVICE:

Problem Solver Systems, Inc. services everything we sell promptly and at a reasonable cost. If our product requires service, return it to us postpaid and it will be tested promptly.
We will then advise you of the repair cost either by phone (if you include your number) or by postcard. The minimum repair fee is $7.50 and the maximum is $50.00. Repair and shipping requires one working day after approval.



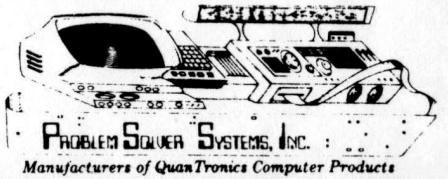
Manufacturers of QuanTronics Computer Products
8040 DEERING AVE. · SUITE 10 · CANOGA PARK, CA. 91304

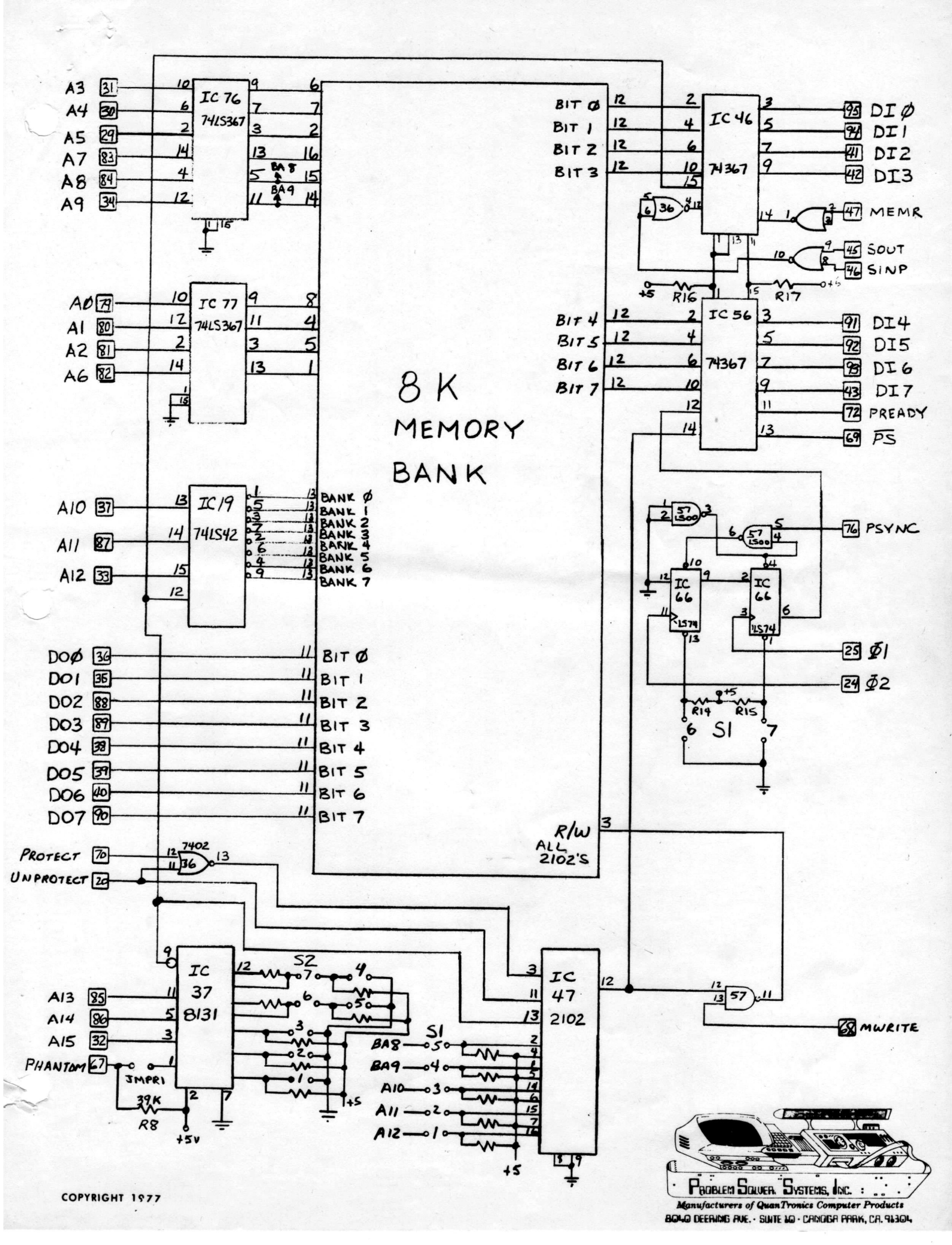


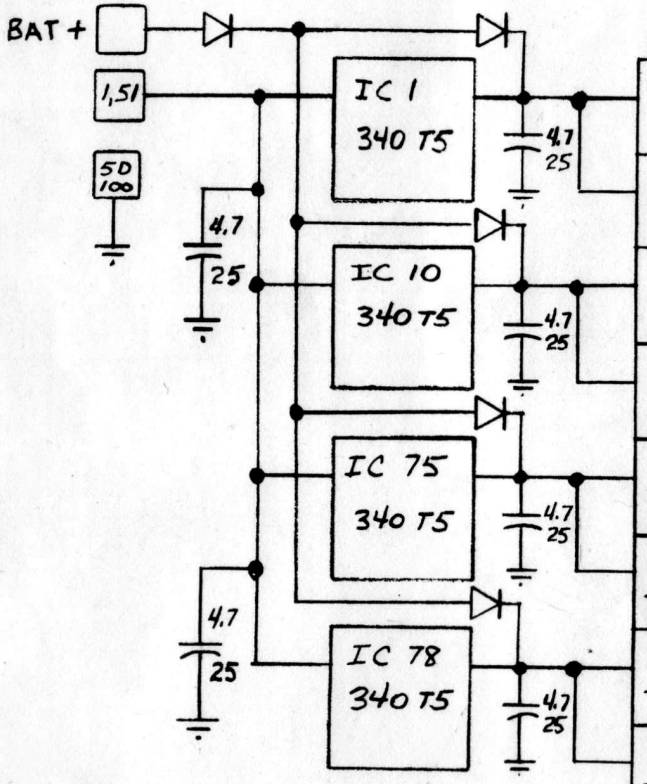
QUANTRONICS

MM8 T.M.

component placement




8K MEMORY BANK
IC 76 74LS367
IC 77 74LS367
IC 19 74LS42
IC 46 74367
IC 56 74367
IC 66
IC 37 8131
IC 47 2102
A3 A4 A5 A7 A8 A9
A0 A1 A2 A6
A10 A11 A12
BA8 BA9
BANK 0 BANK 1 BANK 2 BANK 3 BANK 4 BANK 5 BANK 6 BANK 7
DO0 DO1 DO2 DO3 DO4 DO5 DO6 DO7
BIT 0 BIT 1 BIT 2 BIT 3 BIT 4 BIT 5 BIT 6 BIT 7
DI 0 DI 1 DI 2 DI 3 DI 4 DI 5 DI 6 DI 7
MEMR SOUT SINP PREADY PS PSYNC
Φ1 Φ2
R/W ALL 2102'S
MWRITE
PROTECT UNPROTECT
7402
S1 S2
JMPR1
39K R8
R14 R15 R16 R17
+5 +5V
PHANTOM
A13 A14 A15
BA8 BA9 A10 A11 A12
COPYRIGHT 1977
PROBLEM SOLVER SYSTEMS, INC.
Manufacturers of QuanTronics Computer Products
8040 DEERING AVE. · SUITE 10 · CANOGA PARK, CA. 91304



BIT Ø	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	
IC 2	IC 3	IC 4	IC 5	IC 6	IC 7	IC 8	IC 9	1ST 1K BANK
IC 11	IC 12	IC 13	IC 14	IC 15	IC 16	IC 17	IC 18	2ND 1K BANK
IC 20	IC 21	IC 22	IC 23	IC 24	IC 25	IC 26	IC 27	3RD 1K BANK
IC 28	IC 29	IC 30	IC 31	IC 32	IC 33	IC 34	IC 35	4TH 1K BANK
IC 38	IC 39	IC 40	IC 41	IC 42	IC 43	IC 44	IC 45	5TH 1K BANK
IC 48	IC 49	IC 50	IC 51	IC 52	IC 53	IC 54	IC 55	6TH 1K BANK
IC 58	IC 59	IC 60	IC 61	IC 62	IC 63	IC 64	IC 65	7TH 1K BANK
IC 67	IC 68	IC 69	IC 70	IC 71	IC 72	IC 73	IC 74	8TH 1K BANK

QUANTRONICS

MM8 T.M.

MEMORY BANK LAYOUT

PROBLEM SOLVER SYSTEMS, INC.
Manufacturers of QuanTronics Computer Products